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LINE	PART NUMBER	QTY	
1	MS-2604104 4.95	1	OC 409848

Service Manual

TRS-80®

Model II Computer Graphics Upgrade Kit

Catalog Number 26-4104
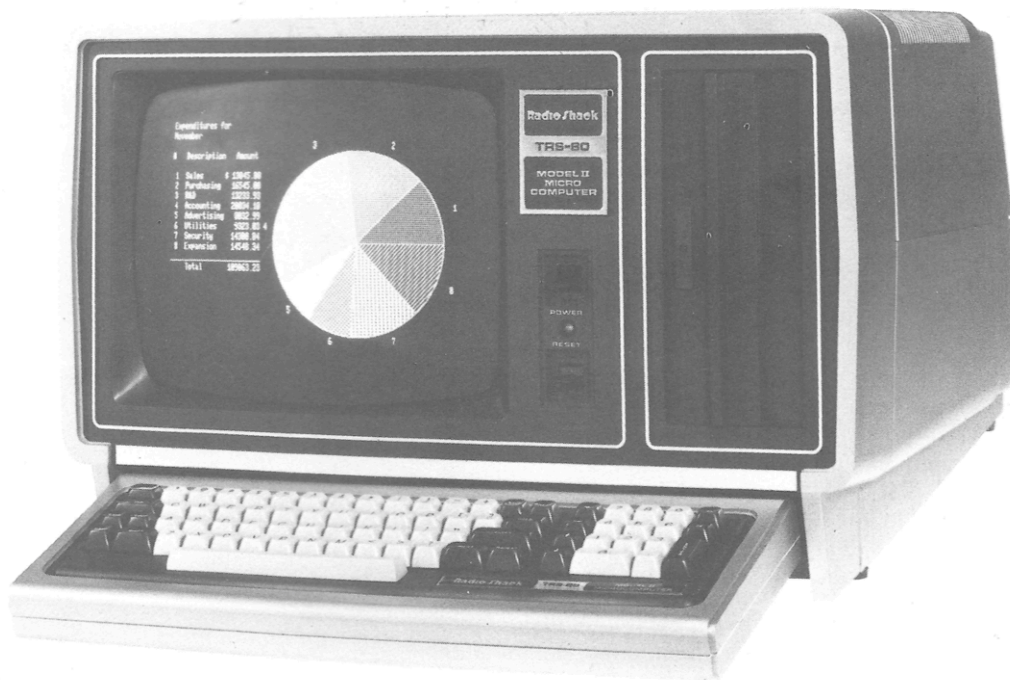
Contents

1/Specifications

Power Requirements (Supplied by Model II)	5V at 65Ø mA +12V at 15Ø mA −12V at 15mA
Operating Conditions	Same as Model II
I/O Requirements	16 Contiguous Z8Ø Hardware I/O Ports, user selectable
Time required to write a data word	1.3 Microseconds (Minimum) 65.5 Microseconds (Maximum)

2/Installation Instructions

Installation

Before the Graphics Board can be installed, the CPU board of
the Model II must be fitted with the DMA WAIT Modification.
This modification consists of a ROM IC and a series of cuts
and jumps which is also used for the Hard Disk system.

Look at the CPU Board. REV A, B, and C Boards must be
modified. REV D Boards do not need to be modified. If the
Model II is fitted with this modification, proceed to the
next section.

Modifying the CPU Board

Follow the procedure below carefully:

1. Disconnect the cables connecting the CPU Board and
    remove the board.

2. Remove and discard U11. Install the new Boot ROM in its
    place. Be sure to position the ROM correctly (marked
    end toward U12).

3. Cut the following traces on the CPU Board and add the
    following jumper wires. Refer to Figures 1, 2, and 3.

    •   Cut the foil to isolate U13 Pin 6.
    •   Cut the foil to isolate U4 Pin 12.

Jumpers

IC	Pin	to	IC	Pin
U21	1		U24	8
U21	6		U4	12
U21	4		JØ	48
U21	5		U15	11
U15	12		U2Ø	13
U15	13		U24	4
U24	3		U2Ø	14

Table 1. Jumpers to CPU Board
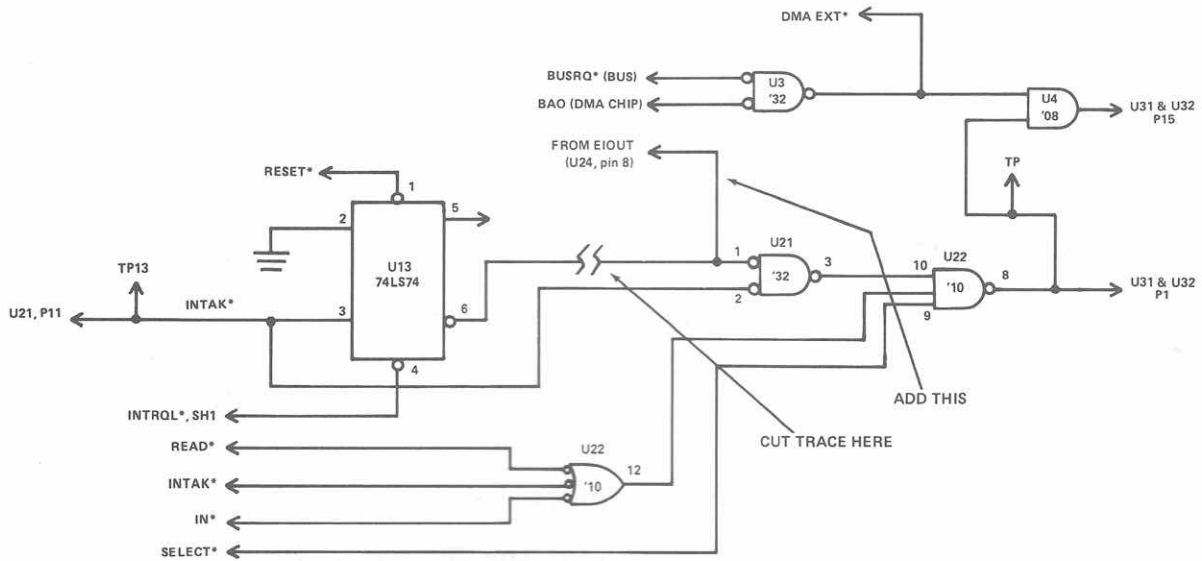
Figure 1. Interrupt Modification for CPU Board
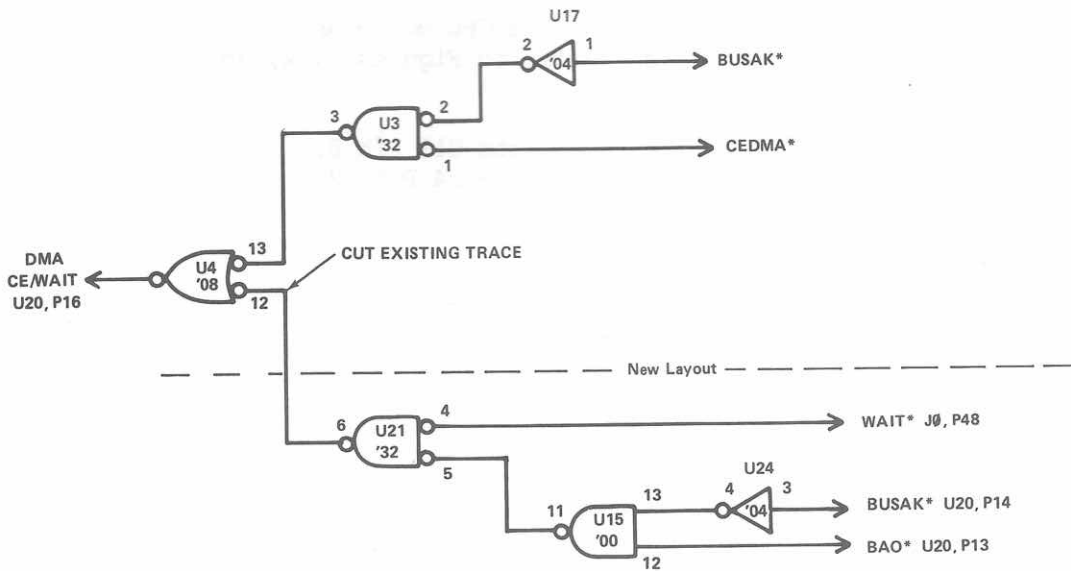
Figure 2. DMA Modification to CPU Board

CUT TRACE HERE
U4, Pin 12

CUT TRACE HERE
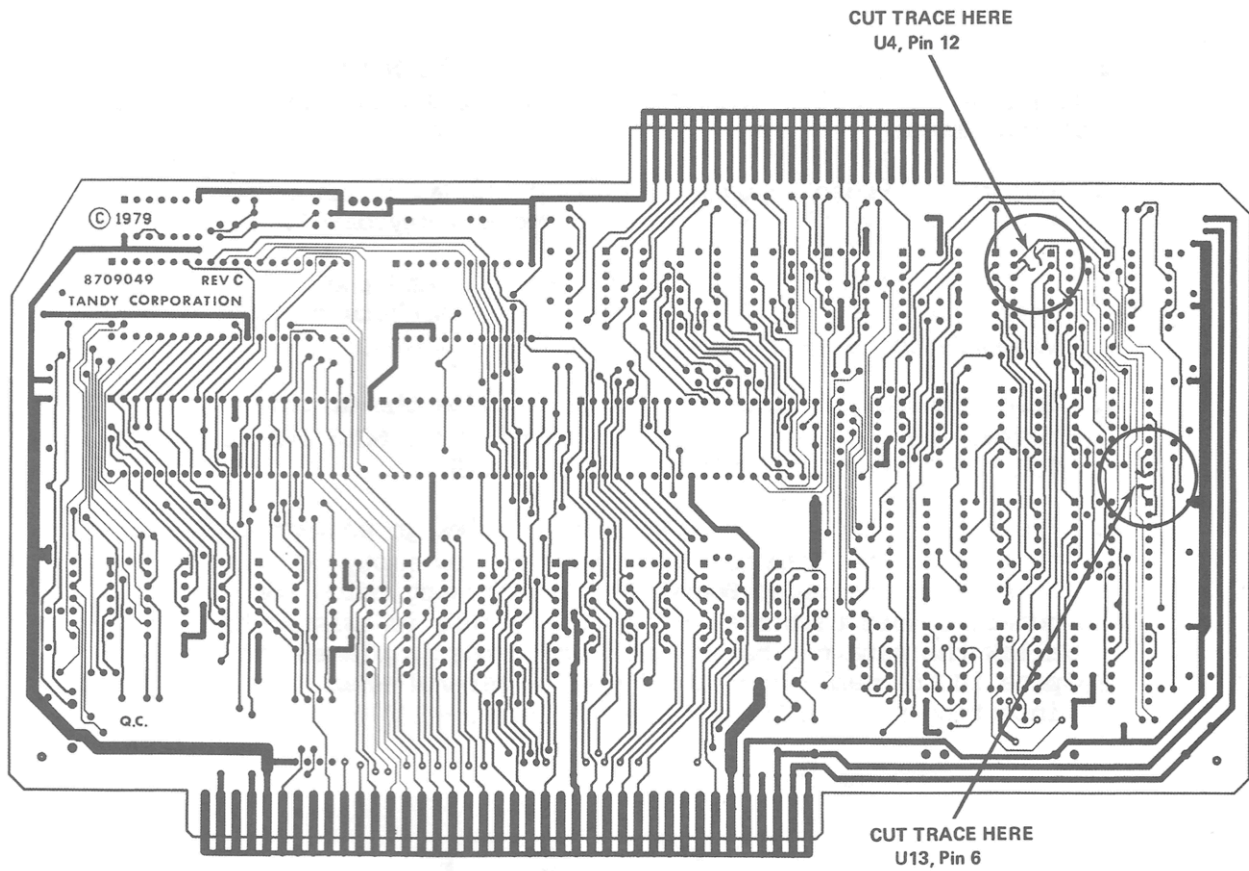U13, Pin 6

Figure 3. CPU Board Modified

Installing the Circuit Board

Once the Model II is working normally with the WAIT modification installed, set the Power Switch to the OFF position. Then:

1. Remove the Video/Keyboard card from the Model II. Be sure to remove the two cables (video and keyboard).

2. CAREFULLY remove the MC6845 VDG IC (U11) and the character generator ROM (U9) from their sockets on the Video/Keyboard card.

3. Insert those two IC's into the sockets on the Graphics board. The VDG goes in U38, the ROM in U25. NOTE THAT THE ROM IS REVERSED FROM THE OTHER CHIPS.

4. Install the two ribbon cables. The cables go between the headers on the Graphics Board and the now empty IC sockets on the Video Board. See the drawing below for details. Note that the 24 conductor cable is twisted to allow the retainer bar to hold the cards in place. The pins in the cable are fragile so be careful when inserting them in the sockets.
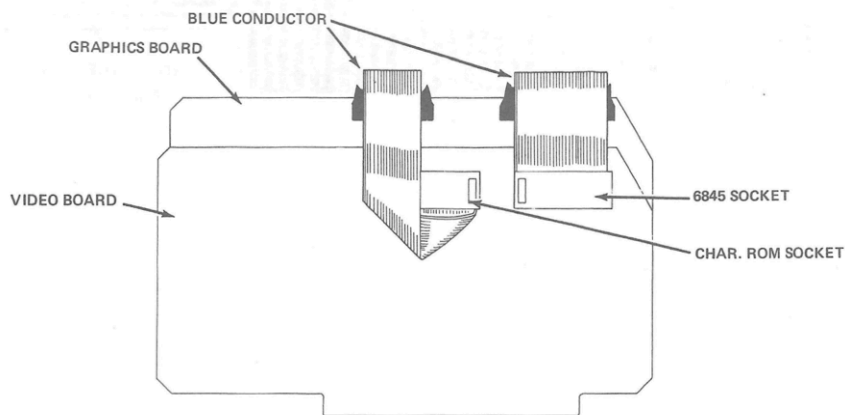
Figure 4. Cable Installation

5. Check to see that the DIP switch on the Graphics Board is set to 8ØH (OFF,ON,ON,ON). See Figure 5.
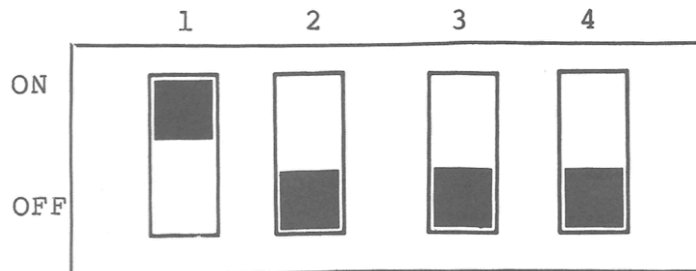
Figure 5. DIP Switch Settings

6. Insert the two boards in adjacent slots in the Model II motherboard. Replace the two cables on the Video Board.

7. Run the Graphics Board Test HIRES. This is contained on the Diagnostics Diskette AXX-2Ø34.

8. If the test results are positive, replace the retainer bar and cover. If the test fails, recheck all cables and be sure that the IC's are correctly installed. Check also to see that a pin isn't folded under an IC. Refer to **3/Troubleshooting** for more help.

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3/Block Diagram
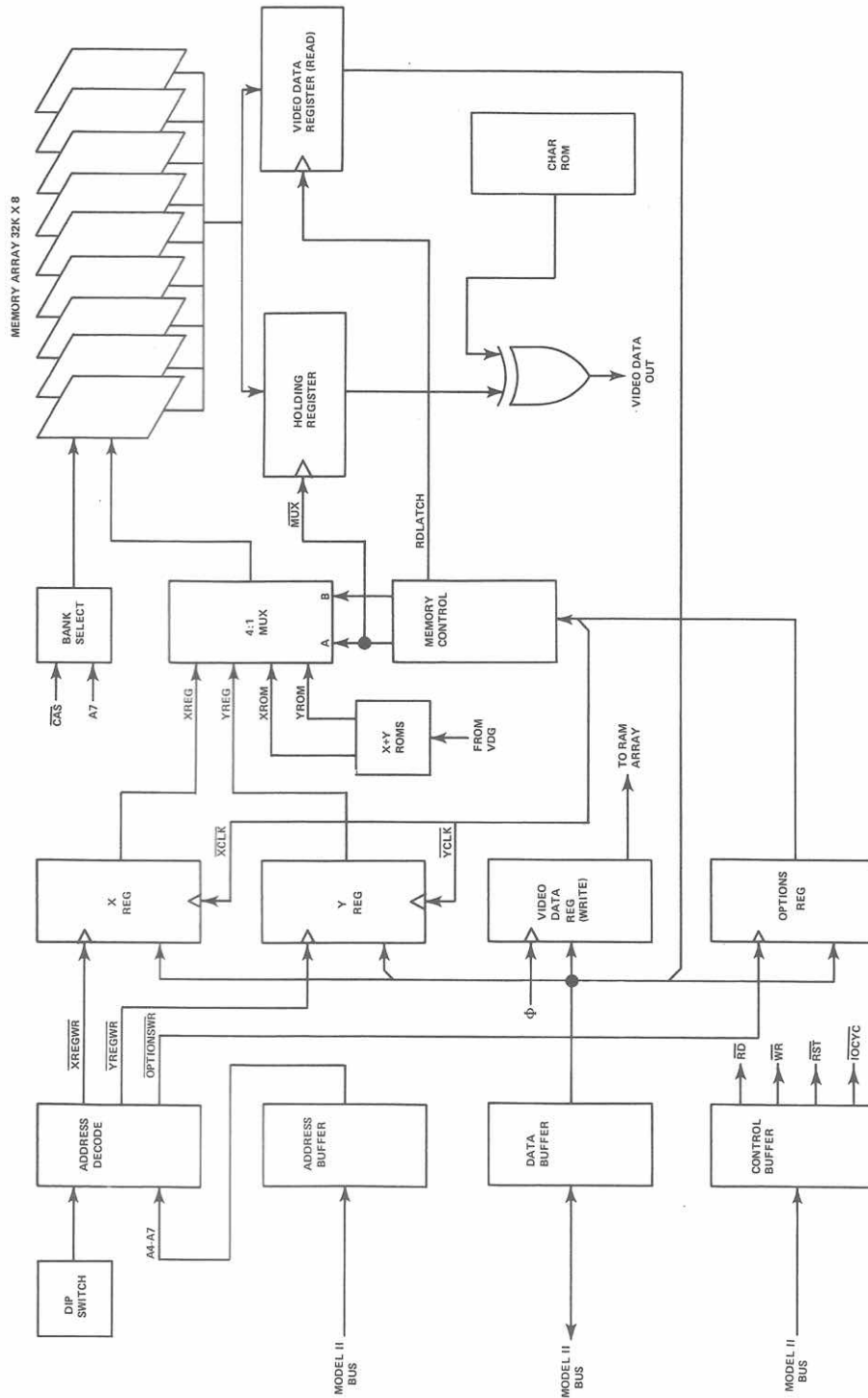
4/Troubleshooting

First isolate the problem to the Graphics Board. Then run
the Graphic Board Test HIRES, contained on the Diagnostic
Diskette AXX-2Ø34.

Some specific symptoms and suggestions.

Computer "hangs up", won't respond to <RESET>
(DMA has seized the bus.)

. Insure "wait mod" is installed on CPU board.

. Check the M1* Mod (cuts and jumps on Rev "A" boards)

Won't read or write to Screen
(U28 not receiving proper commands)

. Check address decoding (U22,U23,DIP Switch)

. Check signals on U28

Places dots erratically on the screen.
(Linear Address Generator malfunction)

. X and Y ROMs reversed, or malfunctioning

. Check shorts and opens near X and Y ROMS

Writes but won't read
(U18 and related circuitry)

. Check for proper signals at pins 1 and 11 of U18

After board warms up, dots seem to fade in and out, or wont
erase.
(RAM Problems)

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. Some dynamic RAMs (marked MK4315) may need to be replaced due to this problem.

5/Timing Chart

20 NS

GENERATED BY Z-80 ADDRESS DECODE

VIDRAM (WR or RD)

WAIT

RAS

MUX

CAS

XY/CRTC

VWR

RDLATCH
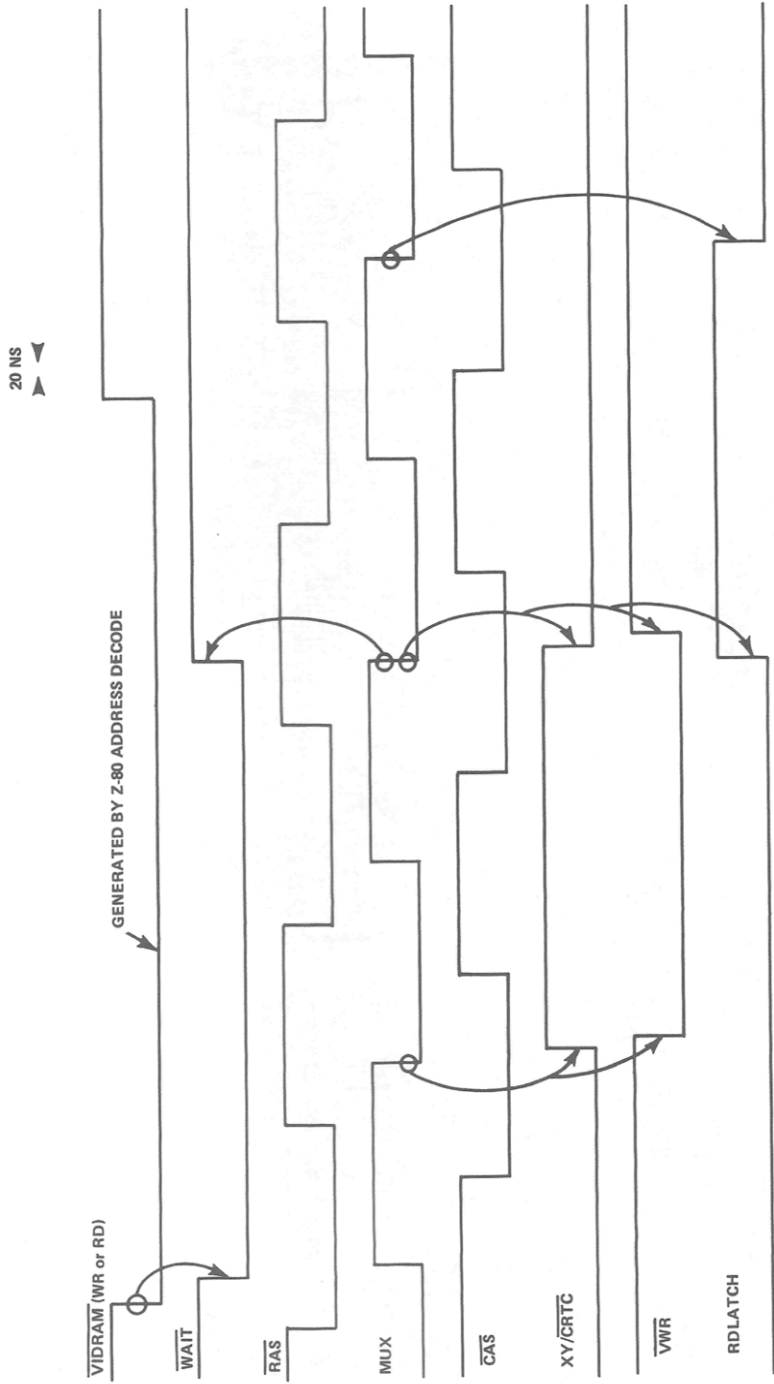
NOTES:

1. DATA LATCHED ON MUX FALLING EDGE.

2. A TYPICAL TIMING RELATIONSHIP IS
   SHOWN. VIDRAM IS ASYNCHRONOUS
   TO THE OTHER SIGNALS.

6/Printed Circuit Board Art
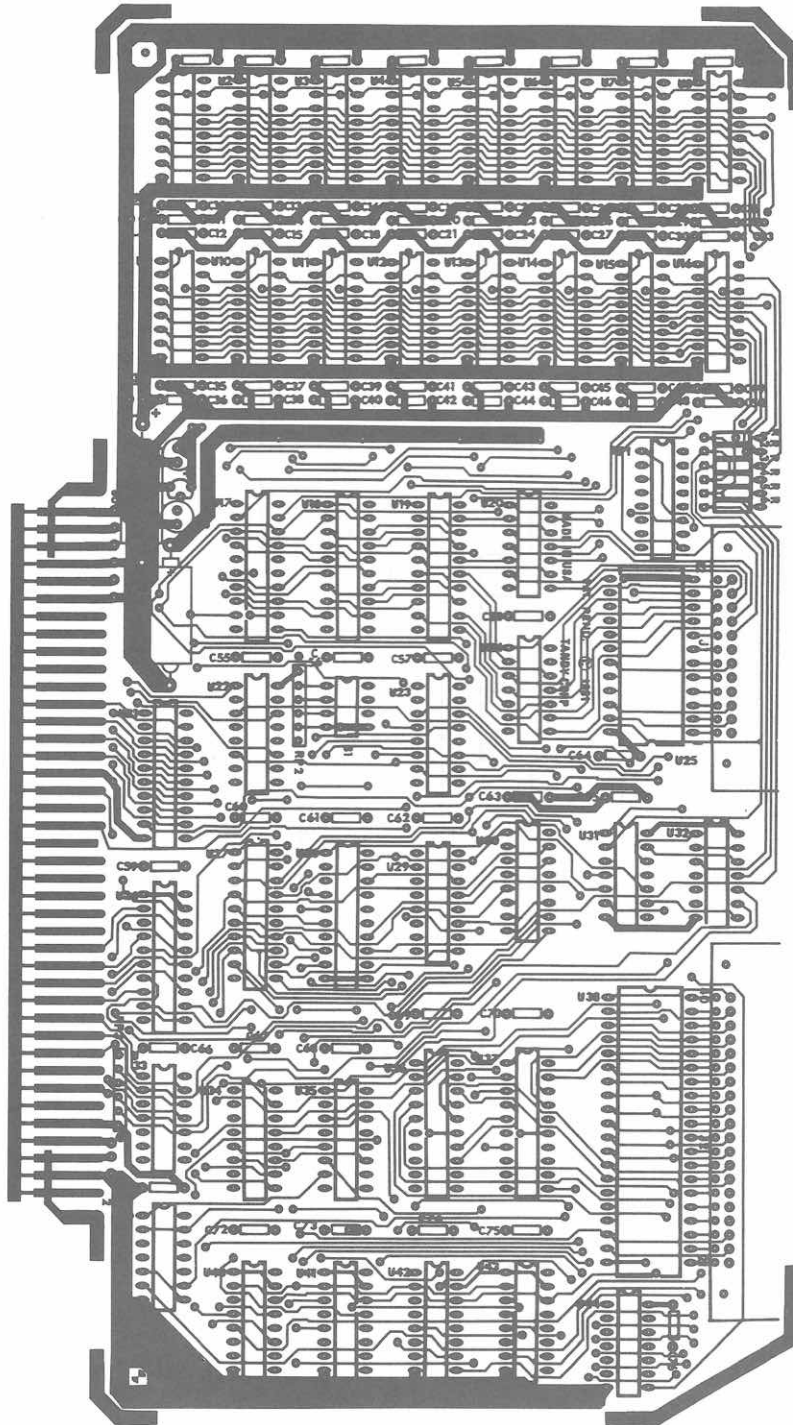
7/Parts List

Electrical Parts

Capacitors

C1	1UF 5ØV MONO AXIAL	837-41Ø4
to		
C7	1UF 5ØV MONO AXIAL	837-41Ø4
C8	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
C9	1ØUF 25V ELECTR. RADIAL	832-61Ø2
C1Ø	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
to		
C33	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
C34	1ØUF 25V ELECTR. RADIAL	832-61Ø2
C35	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
to		
C5Ø	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
C52	1ØUF 25V ELECTR. RADIAL	832-61Ø2
C53	1ØUF 25V ELECTR. RADIAL	832-61Ø2
C54	1ØØUF 16V ELECTR. AXIAL	831-71Ø7
C55	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
C56	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
C57	1ØØUF 16V ELECTR. AXIAL	831-71Ø7
C58	Ø.1UF 5ØV MONO AXIAL	837-41Ø4
to		
C76	Ø.1UF 5ØV MONO AXIAL	837-41Ø4

Resistors

R1	33 OHM 1/4WATT 5%	82Ø-7Ø33
to		
R6	33 OHM 1/4WATT 5%	82Ø-7Ø33
RP1	PAK 16-PIN DIP 27 OHM	829-ØØ27
RP2	PAK 6-PIN SIP 1K OHM	829-Ø21Ø
RP3	PAK 6-PIN SIP 1K OHM	829-Ø21Ø

Integrated Circuit

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U1	4116 16K X 1 DYNAMIC RAM 200NS 16-PIN	804-2016
to		
U16	4116 16K X 1 DYNAMIC RAM 200NS 16-PIN	804-2016
U17	SN74LS273NDS OCTAL FLIP-FLOP " 20-PIN	902-0273
U18	SN74LS374NDS OCTAL FLIP-FLOP " 20-PIN	902-0374
U19	SN74LS273NDS OCTAL FLIP-FLOP " 20-PIN	902-0273
U20	SN74LS8NDS QUAD 2-IN EXCLUSIVE OR " 14-PIN	901-0086
U21	AM8303B OCTAL INVERT TRANSCEIVER AMD 20-PIN	980-6030
U22	N74S85NB 4-BIT MAGNITUDE COMP. 16-PIN	901-0085
U23	SN74LS155NDS DECODER	902-0155
U24	SN74LS8NDS QUAD 2-IN EXCLUSIVE OR " 14-PIN	901-0086
U24	SN74LS240NDS OCTAL BUS INVERTER " 20-PIN	902-0240
U27	SN74LS273NDS OCTAL FLIPFLOP " 20-PIN	902-0273
U28	16R4 PAL CHIP MMI 16-PIN	
U29	SN74LS191NDS UP/DOWN BINARY CNTR" 16-PIN	902-0191
U30	SN74LS191NDS UP/DOWN BINARY CNTR" 16-PIN	902-0191
U31	N74S04NB HEX INVERTER " 14-PIN	901-0004
U32	N74S32NB QUAD 2-IN OR " 14-PIN	900-1032
U33	N7407NB HEX BUFFER OPEN-C	900-0007
U34	SN74LS191NDS UP/DOWN BINARY CNTR" 16-PIN	902-0191
U35	SN74LS191NDS UP/DOWN BINARY CNTR" 16-PIN	902-0191
U38		
U39	N74S00NB QUAD 2-IN NAND	901-0000
U40	SN74LS153NDS DUAL DATA SELECTOR " 16-PIN	902-0153
U41	SN74LS153NDS DUAL DATA SELECTOR " 16-PIN	902-0153
U42	SN74LS153NDS DUAL DATA SELECTOR " 16-PIN	902-0153
U43	SN74LS153NDS DUAL DATA SELECTOR " 16-PIN	902-0153

ROM

U36	TBP28L22 256K X 8 "Y" ROM 60NS 20-PIN	904-0022
U37	TBP28L22 256K X 8 "X" ROM 60NS 20-PIN	904-1022

Voltage Regulator

VR1	REGULATOR 79L05 ACP	805-1905

Mechanical Parts

	ASSY. CABLE, (CHR. GEN.) 5.0" AMP # 6	870-9274
	ASSY. CABLE, (VDG") 8.5" AMP # 6	870-9273
J1	HEADER, 24-PIN (DUAL 12-POS. .100")	851-9134
J2	HEADER, 40-PIN (DUAL 20-POS. .100")	851-9135
S1	SWITCH, DIP 4-POS. AMP #3-435668-4 8-PIN	850-6550
U1	SOCKET, 16-PIN	850-9003

to

U16	SOCKET, 16-PIN	850-9003
U25	SOCKET, 24-PIN	850-9001
U28	SOCKET, 20-PIN	850-9009
U36	SOCKET, 20-PIN	850-9009
U37	SOCKET, 20-PIN	850-9009
U38	SOCKET, 40-PIN	850-9002

DISKETTE, SYSTEM	879-2044
MANUAL, SERVICE/INSTALLATION	874-9326
MANUAL, OPERATIONS	889-7001

ADDRESS DECODE
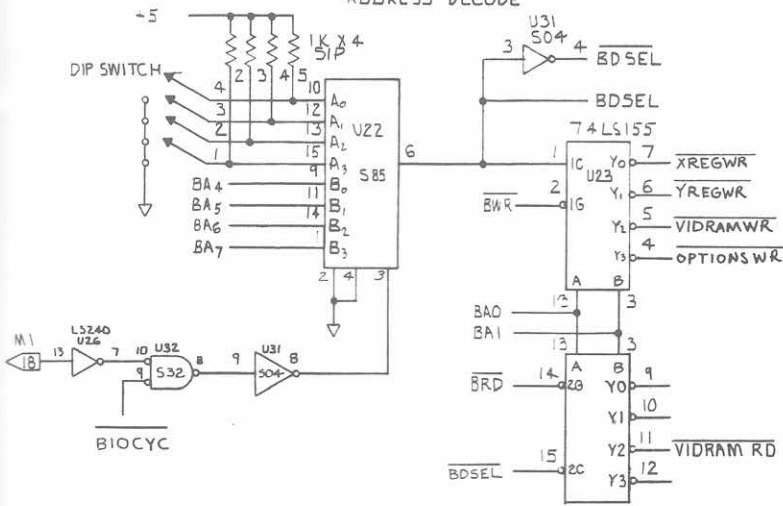
X LINE DRAWING REGISTER 4 X LS191

MODEL II INTERFACE

INTERNAL DATA BUSS

Y LINE DRAWING REGISTER

INCLUDED IN PAL LOGIC 16R4

VID IN
CLK X BIT/RUN RD
VID OUT
CLK X SIT/RUN WR
XCLK

VID IN
CLK Y SIT/RUN RD
VID OUT
CLK Y SIT/RUN WR
YCLK

PAL 16R4

U28

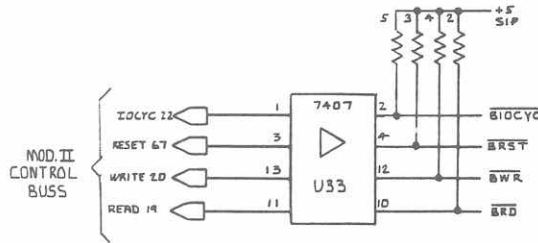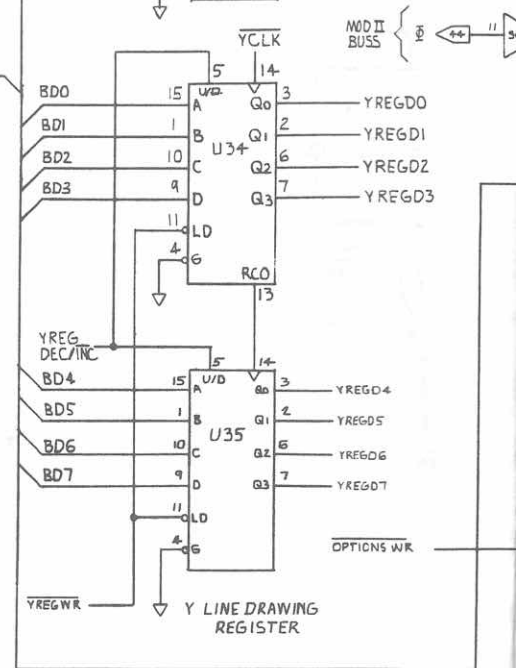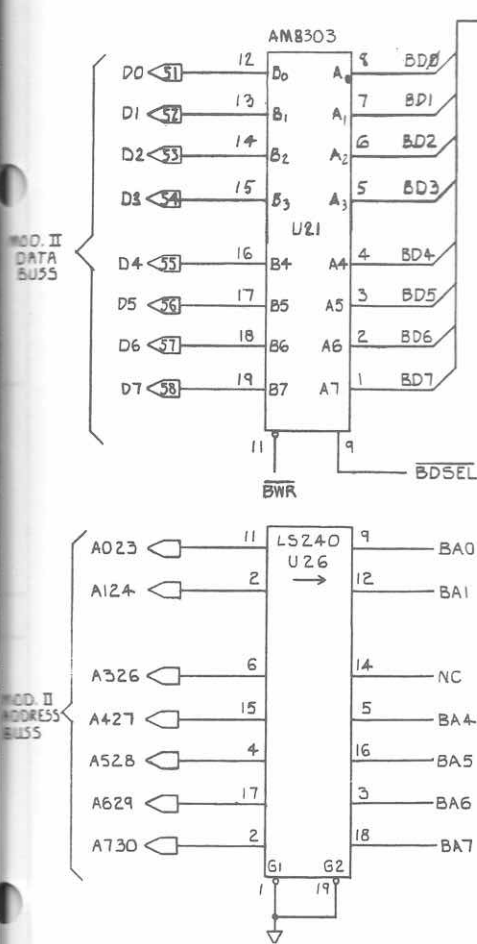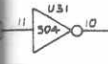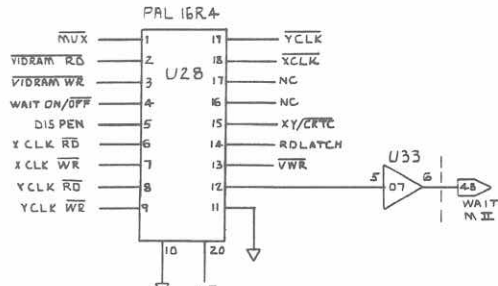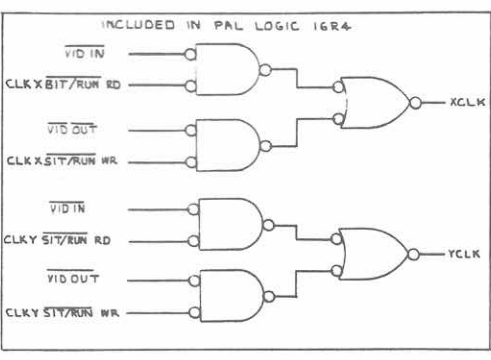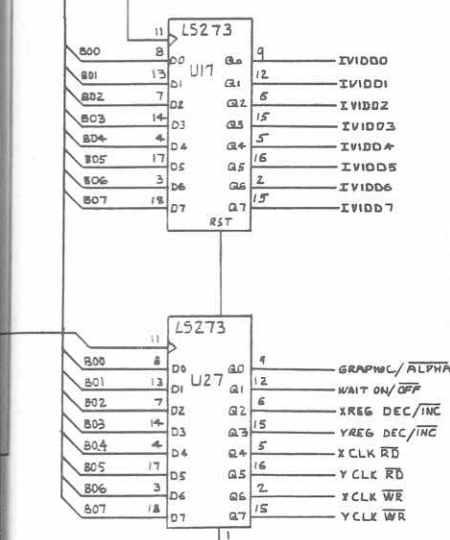|			
MUX	1	17	YCLK
VIDRAM RD	2	18	XCLK
VIDRAM WR	3	17	NC
WAIT ON/OFF	4	16	NC
DIS PEN	5	15	XY/CRTC
Y CLK RD	6	14	RDLATCH
X CLK WR	7	13	VWR
YCLK RD	8	12	
YCLK WR	9	11	

10   20
+5

U31
504
11   10

U33
5 D7 6
4-B
WAIT
M II

DATA REGISTER

LS273
U17
RST

B00	D0	Q0	IVIDD0
B01	D1	Q1	IVIDD1
B02	D2	Q2	IVIDD2
B03	D3	Q3	IVIDD3
B04	D4	Q4	IVIDD4
B05	D5	Q5	IVIDD5
B06	D6	Q6	IVIDD6
B07	D7	Q7	IVIDD7

LS273
U27

B00	D0	Q0	GRAPHIC/ALPHA
B01	D1	Q1	WAIT ON/OFF
B02	D2	Q2	XREG DEC/INC
B03	D3	Q3	YREG DEC/INC
B04	D4	Q4	X CLK RD
B05	D5	Q5	Y CLK RD
B06	D6	Q6	X CLK WR
B07	D7	Q7	Y CLK WR

OPTIONS REGISTER

40 = PIN HEADER

HEADER PIN #'S ARE SAME AS 6845 PIN #'S

25 24 23 22 1

6845
SOCKET
U38

2	RES	L3	35
3	LPSTB	L2	36
17	CURSOR	L1	37
40	VSY	L0	38
34	HSY	DSP	18
26	D7	CCLK	14
27	D6	C10	13
28	D5	C9	12
29	D4	C8	11
30	D3	C7	10
31	D2	C6	9
32	D1	C5	8
33	D0	C4	7
		C3	6
20	VCC	C2	5
		C1	4
		C0	

+5   20

LINEAR ADDRESS GENERATOR

YROM 256X8

U37

19	A7	D6	YROMD7
18	A6	D5	YROMD6
17	A5	D4	YROMD5
	A4	D3	YROMD4
4	A3	D2	YROMD3
2	A2	D1	YROMD2
1	A0	D0	YROMD1
		S0	
		S1	

YROMD0
DISPEN
CCLK

2BL22 [2]
T.I. PROMS

XROM 250X8
U36

19	A7	D7	
18	A6	D6	
17	A5	D5	
5	A4	D4	
4	A3	D3	
3	A2		
15	S1		
16	S2	D1	XROMD5
2	A1	D0	XROMD4
1	A0		

XROMD3
XROMD2
XROMD1
XROMD0

[6] +116 200ns

U2 U3 U4 U5 U6 U7 U8

DO DI (14 2) for each

U10 U11 U12 U13 U14 U15 U16

DO DI (14 2)

IVIDD1 IVIDD2 IVIDD3 IVIDD4 IVIDD5 IVIDD6 IVIDD7

OVIDD1 OVIDD2 OVIDD3 OVIDD4 OVIDD5 OVIDD6 OVIDD7

VIDRAM RD

RDLATCH OVIDD0 OVIDD1 OVIDD2 OVIDD3 OVIDD4 OVIDD5 OVIDD6 OVIDD7

ODD3 OVIDD4 OVIDD5 OVIDD6 OVIDD7

| 4 | 17 | 3 | 18 |
| D4 | D5 | D6 | D7 |

.73 U19

| 11 | 1 | 8 | 13 | 7 | 14 | 4 | 17 | 3 | 18 |
| | E | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |

74LS374 U18

| Q4 | Q5 | Q6 | Q7 |
| 5 | 16 | 2 | 19 |

| Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 |
| 9 | 12 | 6 | 15 | 5 | 16 | 2 | 19 |

BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7

VROMD4 VROMD5 VROMD6 VROMD7
10 9 4 5 13 12 1 2

U20 LS86 U20 LS86 U20 LS86 U20 LS86
8 6 11 3

INTERNAL DATA BUS

14 15 16 17

HEADER

8 A0   VPP 21 +5
7 A1   VCC 24 +5
6 A2
5 A3   CHR D0 9   VROMD0
4 A4   ROM D1 10   VROMD1
3 A5   U25 D2 11   VROMD2
2 A6   D3 13   VROMD3
1 A7   D4 14   VROMD4
23 A8   D5 15   VROMD5
22 A9   D6 16   VROMD6
19 A10   D7 17   VROMD7
   OE GND CS
   20 12   18

DWG NO	SIZE
8000117	D
SCALE	SHEET 2 OF 2

9/Theory of Operation

Introduction

The Model II Graphics Board provides 640 horizontal dots and
240 vertical dots on the video screen for high-resolution
graphics. This is the same number of dots used by the
character generator: 80 characters each using 8 dots or 640
dots per line. Each character is 10 dots vertically, so 24
lines uses 240 dots. The graphics dots are accessed through
the I/O port specified by the DIP switch setting.

The Graphics Board attaches to the Video/Keyboard card using
two ribbon cables.

Theory of Operation

Refer to the Block Diagram and Schematic Diagram for the
following discussion.

Bus Interface and Address Decoding

The Graphics Board is fully buffered from the CPU. The lower
eight address lines (A0-A7) are buffered by U26, and the Z80
control lines by U33. Since U33 is an open collector device,
RP4 pulls the outputs up. The Model II data bus is inverted
on the motherboard so an inverting bi-directional buffer
(U21) is used on the data lines. This buffer has two control
lines, DIR (direction, pin 11) and a TRI-STATE control
(DISable,pin 9). The DIR line is connected to BWR* (buffered
write) which tells the buffer if we wish to read from or
write to the data bus. When BWR* is LOW, we are writing to
the Graphics Board.

The disable line is controlled by BSEL* (board select). With
any access to the Graphics board I/O port, this line goes
LOW which turns the buffer on. When the board is not being
accessed, this line is HIGH and the buffer is off.

I/O decoding is done by high speed 4-bit comparator U22 and
dual decoder U23. The comparator scans address lines A4-A7
and the setting of the DIP switch S1. When the two are equal
AND an I/O instruction is requested (signified by BIOCYC*

going LOW) then BSEL* will go LOW. The equals output of the 74S85 turns on decoder U23 which uses the lower two address lines (AØ and A1), BWR*, and BRD* to produce the proper strobes for the registers.

The OR gate on BIOCYC* is shut off when M1 is active, preventing Graphic Board access when external devices are acknowledging interrupts. M1 is inverted and ANDed with the I/O cycle to disable the board on Interrupt Acknowledge.

Since only the lower two address lines are being used, the Graphics Board is "mirrored" four times within the 16 byte boundary defined by the DIP switch setting. Also, the same address is used for reads and writes to the data register. Table 1 shows how the addresses are decoded:

ADDRESS	FUNCTION
8ØH	X Register Write
81H	Y Register Write
82H	Video Data Write or Read
83H	Options Write
84H	X Register Write
etc	etc

Table 2. Address Decoding

If a starting address other than 8ØH is desired, any 16 byte boundary from ØØH to FØH may be selected using S1. However, all Radio Shack software is compatible with the 8ØH I/O port address. When the switch is ON, the bit in the boundary definition will be Ø. For example, to select I/O port boundary 3ØH, the switches will be ON, ON, OFF, OFF (ØØ11).

Registers (X Address, Y Address, Data, and Options)

Since the Graphics Board is asynchronous with the Model II (this is explained in detail later) the are several octal registers which hold data until the Graphics Board is ready to use it.

The two address registers are actually bi-directional binary counters. U29 and U3Ø are for the X address, and U34 and U35

are for the Y address. Each pair of counters has three control lines; write (XREGWR*, YREGWR*), count direction (XREG DEC/INC*, YREG DEC/INC*), and count clock (XCLK*, YCLK*). The write strobes are generated by the address decoding circuitry. A negative pulse will load the registers with the data on the bus.

The two other signals are generated from the custom logic array (called the "Memory Controller") U28. The count control lines are used to automatically increment or decrement the address registers after a read or write. This greatly speeds up the software in many applications.

The Options register U27 is used to select the user programmable options. These are described below. See Table 2.

Ø   GRAPHICS/ALPHA*

Turns on and off the graphics. A "1" will turn graphics ON.

1   WAITS ON/OFF*

If WAITS are ON the screen will not "hash" when reading or writing to graphics. A "1" selects WAITS.

2   XREG DEC/INC*

Selects whether the X register will decrement or increment. "1" will select decrement.

3   YREG DEC/INC*

Selects whether the Y register will decrement or increment. "1" will select decrement.

4   X CLK RD*

If address clocking desired, a "Ø" will clock the X address up or down AFTER a read depending on the status of BIT 2.

5   Y CLK RD*

If address clocking desired, a "Ø" will clock the Y address up or down AFTER a read depending on the status of BIT 2.

6   X CLK WR*

A "Ø" will clock AFTER a write.

7   Y CLK WR*

A "Ø" will clock AFTER a write.

Bit	Function
Ø	Graph/Alpha
1	Wait/No Wait
2	x Dec/Inc
3	y Dec/Inc
4	x Read Set/Run
5	y Read Set/Run
6	x Write Set/Run
7	y Write Set/Run

Table 3 Options Programming

If clocking of the addresses is not needed, the upper four
bits will then all be 1's (Fx hex).

There are two separate data registers; one for writing data
to the graphics memory (U17) and one for reading data from
the graphics memory (U18). Both are accessed through the
same I/O port. A Z-8Ø OUT will write data, and an IN will
read data.

The write register is clocked on each falling edge of the
system 4 MHz clock. This is to guarantee that the data will
always be valid when the Memory Controller IC begins a write
to RAM.

The read register is an octal latch with TRI-STATE outputs.
When the Memory Controller detects a read cycle, it will
first latch the RAM data using the RD LATCH control line.
When the *WAIT line from the Memory Controller is released
the Z-8Ø executes the IN instruction and reads the data.

CRTC and Address Translation

The 6845 is a Video Display Generator (VDG) which normally
provides monitor sync signals and addresses to scan a
character generator ROM. These addresses are referred to as
"Line" and "Column" addresses, corresponding to the
horizontal lines on the CRT and the vertical columns of the
characters. Since these addresses are scanning a ROM which
is set up for a certain character size (in this case 8 X
1Ø), they do not map to the graphic coordinates directly.

The Graphics Board uses two very fast (6Ø ns) bipolar PROMS (U36 and U37) to translate the "Line-Column" addresses to "Absolute X-Y" addresses. After the addresses emerge from the PROMS, they will map to the addresses in the X and Y registers.

Graphics Memory

The memory section of the Graphics Board is the most complex, and the most likely to malfunction. It consists of four parts: the Memory Controller IC, the address multiplexers, memory timing, and the holding register. Sixteen 2ØØ ns 16K dynamic memories are used to store the graphics data, providing a total of 32K, although only 19.2K (8Ø X 24Ø) is used.

To understand how the memory section works, refer to the system timing diagram.

It is important to note that the graphics memory is asynchronous with respect to the CPU. In order to sync up, the Memory Controller IC uses the WAIT* line on the Z-8Ø. This is not to be confused with the WAIT option of the Options register, which uses the DISPEN signal from the 6845 to suspend memory access until the beam of the CRT is being blanked. Refer to the Model II Technical Reference Manual for more details.

The brain of the memory section is the Memory Controller, U28. This is a custom IC whose functions are:

. Monitor the VID RAM RD* and VID RAM WR* lines to detect a graphics memory access.

. Monitor the Options register and send the proper signals to the X and Y registers.

. Sync the Graphics board to the Model II using the WAIT* line.

. Generate the signals to read and write to the graphics RAM.

The memory ICs have multiplexed address lines, and must be provided the proper timing signals (RAS* and CAS*) and make sure the addresses are at the RAMS at the proper time. This

is accomplished by taking the character clock (CCLK) from
the VDG and using a digital delay line (U44) to derive the
timing signals.

The VDG addresses are stable 160 ns after the falling edge
of CCLK. CCLK is inverted by U31 producing RAS*. RAS* is
delayed 100 ns and inverted to form MUX. The MUX signal is
used to switch between the upper and lower RAM addresses.
The inverse of MUX, MUX*, is used by the Memory Controller
as a timing reference. MUX is then delayed 150 ns to form
CAS*.

There are two ways to address graphics RAM:

.   Use the X and Y registers to read and write dots.

.   Use the VDG to scan memory and display the contents on
     the CRT.

Certainly, the VDG has control most of the time. The VDG
scanning time is used to refresh the dynamic memories.

The contention problem is solved by using two sets of
addresses, the XREGD0-XREGD6 and YREGD0-YREGD7 set for the
registers and the XROMD0-XROMD6 and YROMD0-YROMD7 set for
the VDG. Normally, the VDG has control of the RAM and these
addresses are incremented in a linear fashion (0-79 out of
the XROM and 0-239 out of the YROM) each CCLK cycle.

The Memory Controller assumes the VDG has the RAM addresses
and keeps the XY/VDG* line LOW. This selects the VDG
addresses in the four dual 4:1 multiplexers U40-43. The
other multiplexer control line is connected to MUX, so the
addresses switch between RAS* and CAS*.

Since there are two RAM banks, Y address line D7 splits the
screen into two halves at the 128th line. The top half of
screen RAM is in RAMS U1-U8 while the lower half of the
screen is contained in RAMS U9-U16. High speed NAND gate U34
is used to select between the two banks of RAM.

The 4116 RAMS used do not have a separate chip select input
so a technique called "gated CAS*" is used to turn on each
RAM bank. A Multiplexer consisting of a 74S00 NAND gate
(which doesn't use the MUX as the other multiplexers do) and
a pair of OR gates (U32) gate CAS* to the RAMS.

The RAMS provide TRI-STATE outputs and have on-chip latches
for the outputs, which are configured in parallel. The
outputs go to a holding register to delay the graphic data
one CCLK period from reaching the Video Board. This is done

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by octal latch U19. The clear input of the latch turns the graphics on and off and the GRAPHIC/ALPHA* line from the options register is connected here.

It is important to note that while the VDG is scanning the graphics RAM, it is simultaneously scanning the regular screen RAM on the Video Board. This means that the Graphics Board must be able to do a memory access in one CCLK period, which is 641 ns. The time for a memory access is approximately:

VDG address stable + ROM delay + Mux delay + RAM delay = Access time.

160 ns   + 120 ns   + 30 ns   + 260 ns   =
570ns

which is plenty of time. This does not take into account the time the Z-80 is in a WAIT state, which at worst case is 640 ns with the WAIT option off and 64.6 uS with the WAIT option on.

By using the holding register, the graphics data is available at the same time as the video data (from the character generator U25). The separate data is EXCLUSIVE OR-ed together by U20 and U24 to form the composite video data sent to the Video Board to be shifted out to the CRT.