



ModelSim-Altera Software Simulation

User Guide



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This user guide describes simulation using the ModelSim-Altera Starter Edition or ModelSim-Altera Edition software.

The Quartus® II software supports HDL design simulation at register transfer (RTL) and gate levels in various industry-standard simulators. You can use the Quartus II NativeLink feature to integrate your EDA simulator within the Quartus II design flow and streamline simulation processing steps.

For more tool-specific guidelines, refer to *Aldec Active-HDL and Riviera-PRO Support*, *Synopsys VCS and VCS MX Support*, *Cadence Incisive Enterprise Simulator Support*, or *Mentor Graphics ModelSim and QuestaSim Support* in the *Quartus II Handbook*.

Prerequisites

This user guide assumes you have a working knowledge of the following subjects:

- Verilog HDL, SystemVerilog, or VHDL hardware description languages
- Subjects covered in the Quartus II software “Getting Started Tutorial”

Starting the ModelSim-Altera Software with the Quartus II Software

To start the ModelSim-Altera software, follow these steps:

1. Unzip the provided Quartus II design example project `counter.zip`.
2. Start the Quartus II software and open the design example Quartus II project file `counter.qpf`.

Setting Up EDA Tool Options

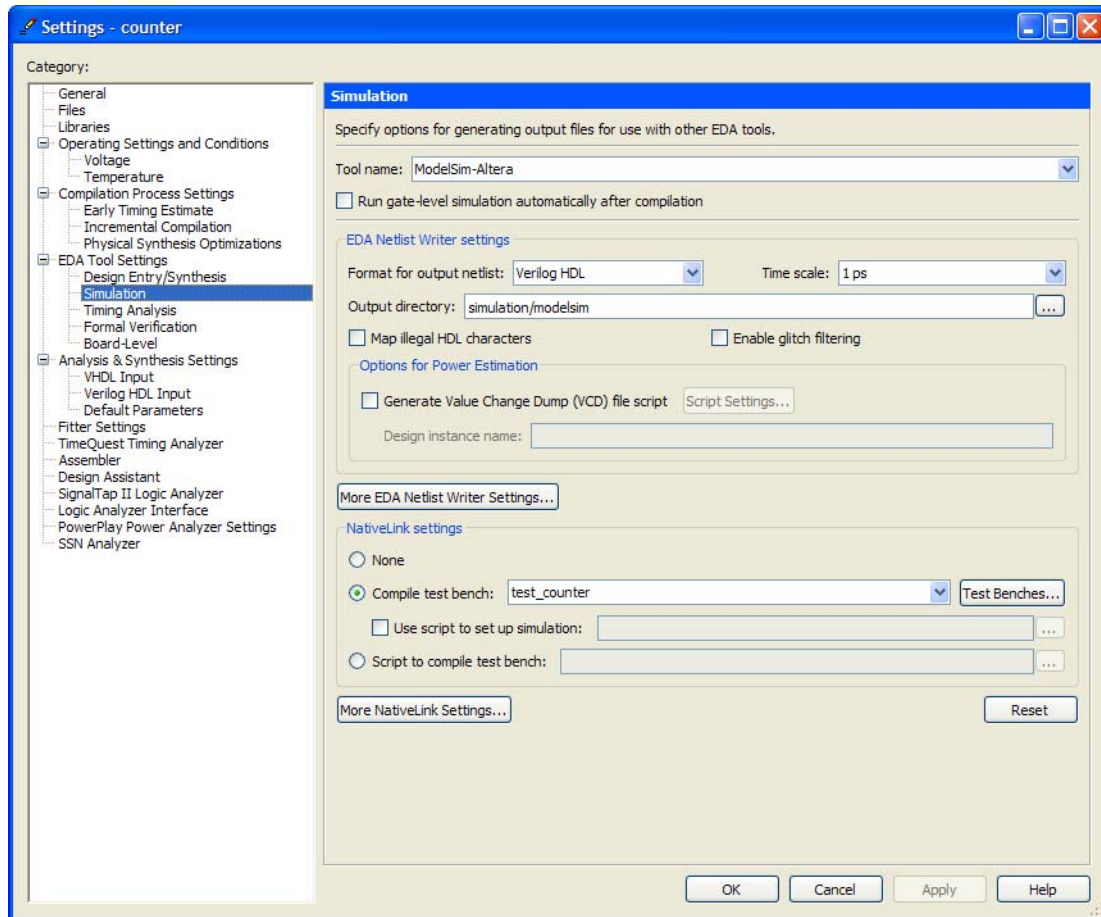
You can specify where your third-party EDA simulators are installed with the EDA tool options settings in the Quartus II software. These settings enable you to start third-party EDA simulators from the Quartus II software. The ModelSim-Altera tool path is automatically added during Quartus II installation.

Setting Up the Simulation


To set up the Model-Sim Altera simulation environment, follow these steps:

1. On the Tools menu, click **Options** and specify the location of your simulator executable file on the **EDA Tool Options** page.
2. On the Assignments menu, click **Settings**.
3. In the **Settings** dialog box, under **EDA Tool Settings**, select **Simulation**. The **Simulation** page appears. (Figure 1–1).

Figure 1–1. Simulation Page (Settings Dialog Box)



1. In the **Tool name** list, select **ModelSim-Altera**. Ensure that **Run gate-level simulation automatically after compilation** box is turned off.
2. Under **EDA Netlist Writer settings**, in the **Format for output netlist** list, select **Verilog HDL**. Ensure that the **Map illegal HDL characters**, **Enable glitch filtering**, and **Generate Value Change Dump (VCD) file script** boxes are turned off.
3. Under **NativeLink settings**, select **None**.

 For more information about the Quartus II NativeLink feature, refer to the *Simulating Altera Designs* chapter in volume 3 of the *Quartus II Handbook*.

Running ModelSim-Altera from the Quartus II Software

To generate the ModelSim-Altera automation script (.do file), start the ModelSim-Altera software, and then compile the design files, follow these steps:

1. On the Processing menu, point to **Start**, and then click **Start Analysis & Elaboration**.

2. On the Tools menu, point to **Run Simulation Tool** and then click **RTL Simulation**. The Quartus II software starts the ModelSim-Altera simulator. You can ignore error or warning messages about the `tcounter.v` file. In the next section you create stimulus waveforms and export the waveforms into `tcounter.v` testbench file.

Creating Stimulus Waveforms

This section guides you in adding signals to the Wave window, creating the clock waveform, and creating the reset waveform.

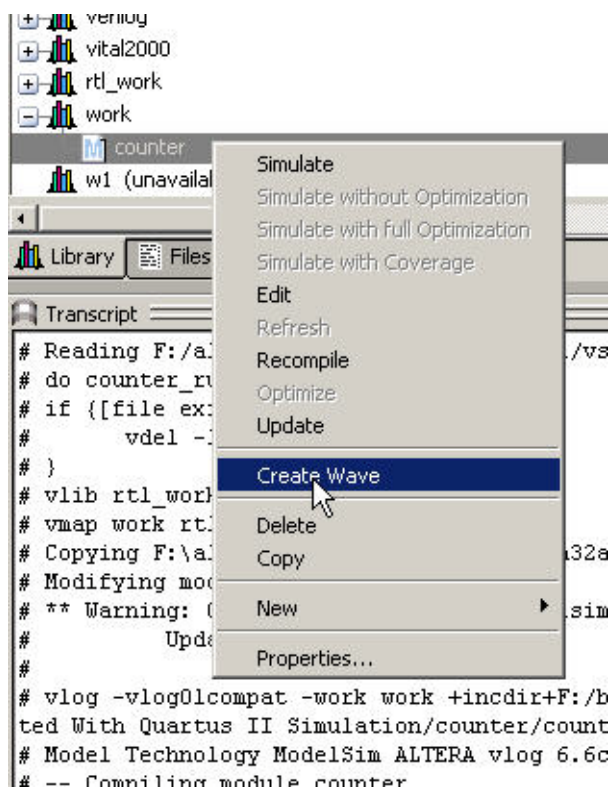
Adding Signals to the Wave Window

To add signals to the Wave window, follow these steps:

1. In the ModelSim-Altera GUI, expand **Work** in the Library window, and then right-click `counter`.
2. Click **Create Wave** (Figure 1-2).

Three signals (`clk`, `reset`, and `count`) from the counter design example are added in the Wave window, where you can create stimulus waveforms for each signal to simulate the design. In this example, you will create stimulus waveforms for the `clk` and `reset` signals. The `count` signal is not needed and can be deleted.

Figure 1-2. Create Wave on the Shortcut Menu

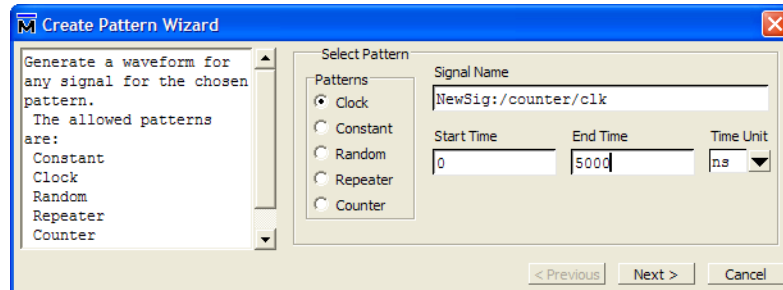


3. Right-click the `count` signal in the Wave window, and then click **Delete**.

Creating the Clock Waveform

1. Right-click the `clk` signal in the waveform, point to **Edit**, and then click **create/modify**. The Create Pattern Wizard appears (Figure 1-3).


Figure 1-3. Create Pattern Wizard



2. Under **Patterns**, select **Clock**.
3. For **Start Time**, enter 0, for **End Time**, enter 5000, and for **Time Unit**, enter ns.
4. Click **Next**.
5. For **Clock Period**, enter 100, for **Time Unit** enter ns, and for **Duty Cycle**, enter 50.
6. Click **Finish**.

Creating the Reset Waveform

1. Right-click the `reset` signal in the waveform, point to **Edit**, and then click **create/modify**.
2. In the Create Pattern Wizard, under **Patterns**, select **Constant**.
3. For **Start Time**, enter 0, for **End Time**, enter 5000, and for **Time Unit**, enter ns.
4. Click **Next**.
5. Enter `st0` (Strong 0) for **Value**.
6. Click **Finish**.

 For more information, refer to *Chapter 13, Generating Stimulus with Waveform Editor* in the *ModelSim User's Manual*. In the ModelSim-Altera software, on the Help menu, point to **PDF Documentation**, and then click **User's Manual**.

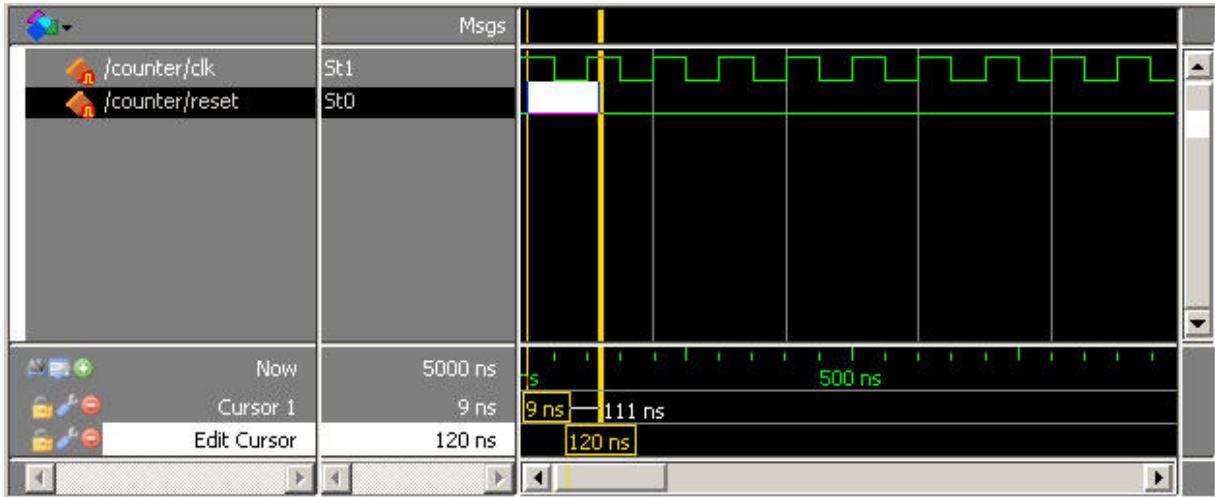
Modifying Stimulus Waveforms

To modify stimulus waveforms, follow these steps:

1. Click in the waveform window to enable the Wave menu.
2. On the Wave menu, point to **Mouse Mode** and then click **Edit Mode**. Make sure the Wave window is activated. To activate it, click in the Wave window.

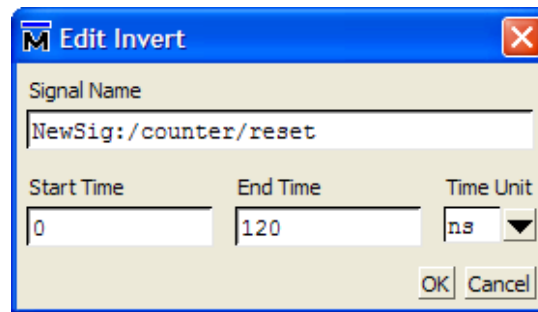
3. Select the **reset** signal from 0 ns to approximately 120 ns. The selection does not need to be exact (Figure 1-4).

Figure 1-4. Inverted Waveform for reset Signal



4. On the Wave menu, point to **Wave Editor**, and then click **Invert**. The **Edit Invert** dialog box appears (Figure 1-5).

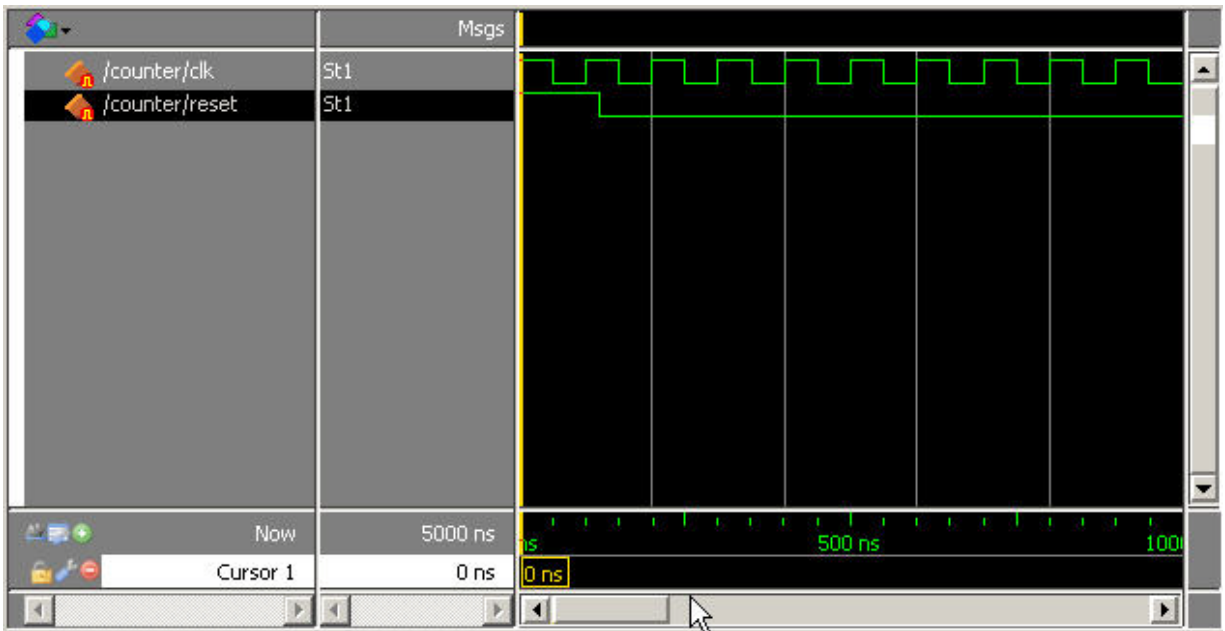
Figure 1-5. Edit Invert Dialog Box



5. For **Start Time**, enter 0, for **End Time**, enter 120, and for **Time Unit**, enter ns.

- Click OK to invert the waveform. Figure 1-6 shows the inverted waveform.

Figure 1-6. Inverted Waveform for reset Signal (0–120 ns)



Starting Simulation

To start the simulation, follow these steps:

- Expand the **Work** library, right-click **counter** and click **Simulate**.
- Drag the **count** signal from the Objects window to the Wave window.
- In the Transcript window, type the command `run -all` ↵.

After you type the `run -all` command, the example **counter** design is simulated with the created stimulus waveforms for the **clk** and **reset** signals. The **clk** signal is a continuous clock waveform. The **reset** signal is asserted for the first 120 ns. When the **reset** signal is deasserted after 120 ns, the counter begins to increment, once on each rising edge of **clk**. The output signal **count** produces the simulated waveform, in the Wave window, adjacent to the stimulus waveforms.

Exporting Created Stimulus Waveforms as an HDL Testbench

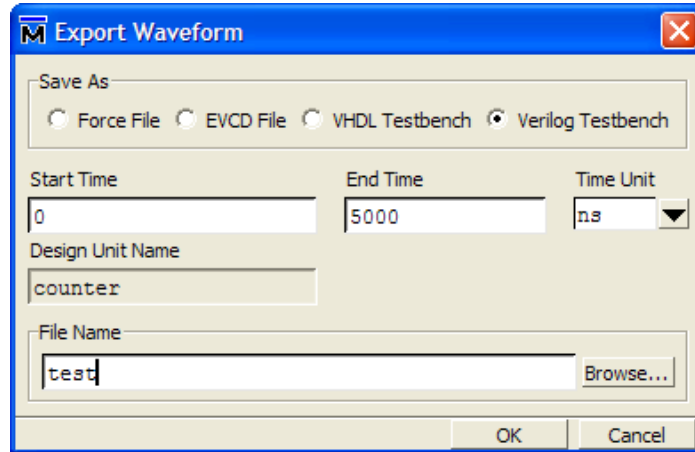
An HDL testbench file is typically written in the same hardware description language as your design, and interacts with your design as an instantiated module. An HDL testbench file is conceptually similar to a waveform like the one created in “[Creating Stimulus Waveforms](#)” on page 1-3, but because it is written in HDL, it is able to accommodate more complexity and flexibility than a graphical waveform.

The stimulus waveforms you created for the simulation can be exported as a HDL testbench file. You can then use the HDL testbench file to simulate your design again without manually recreating the stimulus waveforms.

To export the stimulus waveform as an HDL testbench, perform the following steps:

1. Click in the **Wave** window to ensure it is active.
2. On the File menu, point to **Export** and then click **Waveform**. The **Export Waveform** dialog box appears (Figure 1-7).

Figure 1-7. Export Waveform Dialog Box



3. In the **Export Waveform** dialog box, under **Save As**, select **Verilog Testbench**.
4. For **Start Time**, enter 0, for **End Time**, enter 5000, and for **Time Unit**, enter ns.
5. In the **File Name** box, type the name of your testbench or click the **Browse** button.
6. Click **OK**.

The testbench appears in the *<Quartus II project folder>\simulation\modelsim* folder. You can use the testbench file for the simulation of your Quartus II design.

This section provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
January 2013	2.0	Updated Linux and GUI information.
June 2011	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General) (Software Licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com









Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, D: drive, and chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> .
<i>italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pof file.

Visual Cue	Meaning
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
“Subheading Title”	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code> , <code>tdi</code> , and <code>input</code> . The suffix <code>n</code> denotes an active-low signal. For example, <code>resetn</code> . Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code> . Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>).
	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
 CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
 WARNING	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.