Radio Shack®

Service Manual

26-3501/3503

TRS-80 Pocket Computer and Cassette Interface

Catalog Number: **26-3501**
26-3503

CUSTOM MANUFACTURED FOR RADIO SHACK A DIVISION OF TANDY CORPORATION

TABLE OF CONTENTS

1. SPECIFICATIONS

Display

- Display tube: LF8017JE
- Display method: 5 x 7 dot matrix liquid crystal
- Display capacity: 24 columns (alphanumerics and symbols)

Basic functions

- Computational capacity: 12 digits of mantissa and 2 digits of exponent.
- Computational method: According to mathematical formula (with priority consideration and judge function)
- Capacities:
  - Program memory; 1424 steps, max
  - Data memory; Fixed memory
    - 26 memories
    - Flexible memory (commonly usable with the program memory)
    - 178 memories, max.
  - Reserve program; 18 kinds, 48 steps, max.
  - Input buffer: 80 steps
- Buffers:
  - Data buffer; 8 stages
  - Functional buffer; 16 stages (but 15 stages for parenthesis)
  - Subroutine buffer; 4 stages
  - "FOR NEXT" stagement buffer; 4 stages

Arithmetic functions

Acd (+), Subtract (−), Multiply (×), Divide (/), Power raising (^)

Trigonometric functions:	SIN (sine), COS (cosine), TAN (tangent)
Inverse trigonometric functions:	ASN (sine $^{-1}$), ACS (cosine $^{-1}$), ATN (tangent $^{-1}$)
Logarithmic functions:	LOG (common logarithm), LN (natural logarithm [ln])
Exponential functions:	EXP (exponential)
Angular transformations:	DMS (decimal notation to sexagesimal notation) DEG (sexagesimal notation to decimal notation)
Square root extraction:	$\sqrt{}$
Signum function:	SGN
Absolute value:	ABS (|X|)
Integration:	INT

Execution of arithmetic operation is commanded by the ENTER key.

Editorial functions

Cursor shift:	► (right), ◄ (left)
Insertion:	INS
Deletion:	DEL
Line control:	↓ (down), ↑ (up)

Programming language

BASIC (Beginner's All purpose Symbolic Instruction Code)

Power source

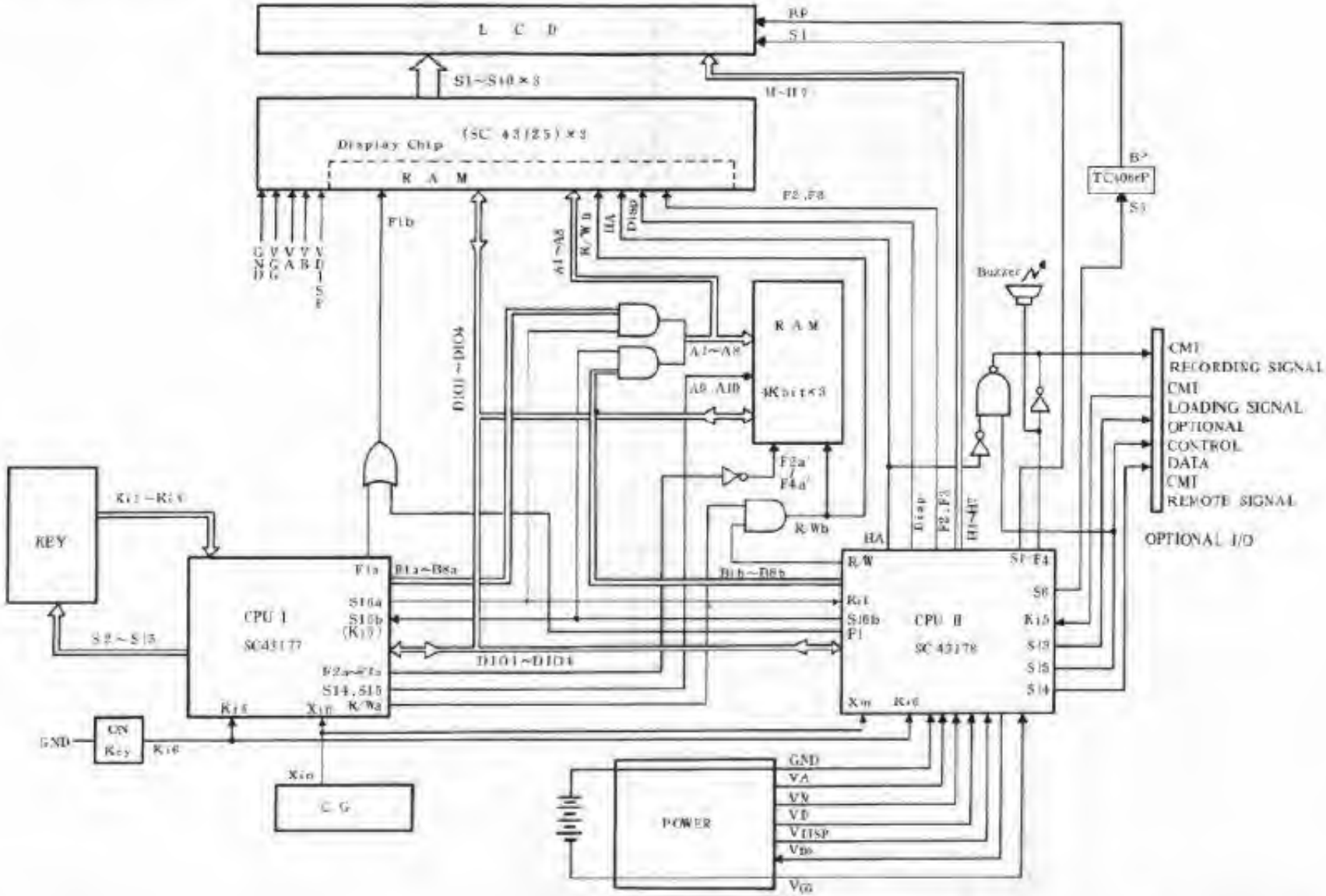
Battery:	Four MR44 (mercury batteries)
Battery life:	300 hours
Power consumption:	0.011W
Automatic power shutoff:	About 6 minutes

Miscellaneous

Data protection:	Program memory, data memory, reserve program memory
Peripheral unit:	Audio cassette unit (recording/reading of the program memory, data memory and reserve program memory)
Optional	26-3503 (audio cassette interface)
Physical dimensions:	175(W) x 70(D) x 44(H) mm (6.8(W) x 2.7(D) x 1.7(H) inches)
Weight:	Approx. 170g (0.37 lbs) ... 26-3501 Approx. 240g (0.53 lbs) (with batteries) ... 26-3503

For complete details of operating the TRS-80 Pocket Computer, refer to the Owner's Manual.

2. BLOCK DIAGRAM



System configuration (see the system block diagram)

The system consists of the following components:

1. CPU I (SC43177) x 1
2. CPU II (SC43178) x 1
3. 4K-bit RAM (TC5514P x 3)
4. Display chip (SC43125 x 3, with built-in RAM)
5. 2AND gate (TC4011UBP x 1)
6. 2AND 2OR (TC4019BP x 1)
7. Inverter (TC4069BP x 1)
8. Quard Analog Switch Multiplexer (TC4066BP)
9. LCD (24-digit FEM dot LCD)
10. Key
11. Crystal (CSB2560)

Brief overview of CPU I and CPU II

The CPUs are provided with internal ROM, and the CPUs have the following assignments:

CPU I

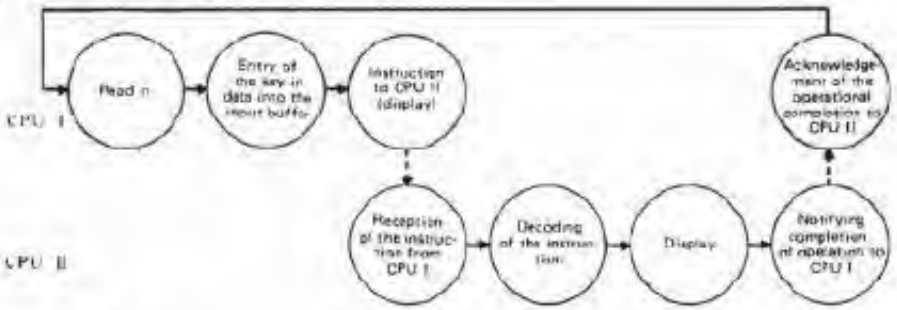
Key input routine
Acknowledgement of the remaining program
One instruction to one program step additional incorporation
Interpreter: Program execute statement Cassette control statement Command statement Printer control (reserved)
Execution of manual operation
Power shutoff control
Clock stop control

CPU II

Display processing routine Input buffer Computational result Error
Arithmetic routine
Character generator
Cassette routine
Print routine
Buzzer
Recognition of printer (reserved)
Power off
Clock stop

- The CPU I functions to read key-in data or read the instruction to be executed from the RAM, and decides what is to be done for the control of arithmetical operations (i.e., control of arithmetic sequence, memorizing of arithmetical data, and its readout), or interpret the syntax of the BASIC instruction for deciding what is to be executed, or determines and prepares the information to be displayed, but CPU I does not perform any execution by itself. It only arranges the data and information in proper sequence and acts to provide instruction code to the CPU II via the buffer. On the other hand, CPU II constantly receives execution instructions from CPU I via the transfer buffer and executes operations per each instruction or exchanges data, depending on the situation. Although it shares execution functions and performs some auxiliary CPU roles, it does not perform any decision by itself.

Eg: Actions of CPU I and CPU II at the time of key data entry.

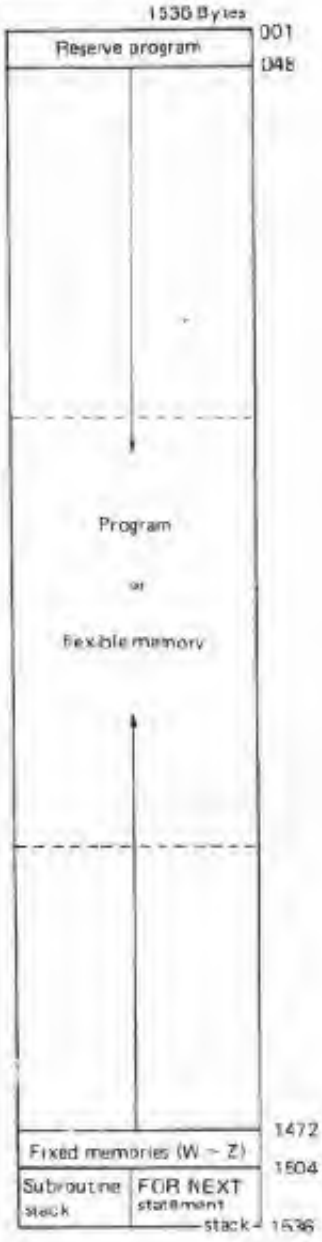


For manual operation of the Pocket Computer, the instruction code (key code) is written into the RAM in the display chip (input buffer) after information is put through the keyboard and converted into the instruction code by CPU I, then this instruction code (display) is transferred to the CPU II via the transfer buffer. As CPU II receives this instruction, CPU II then decodes this instruction (display) and executes display processing. Upon the completion of this processing, it notifies CPU I, and CPU I confirms the completion of the task by the CPU II before terminating their functions.

Overview of RAM

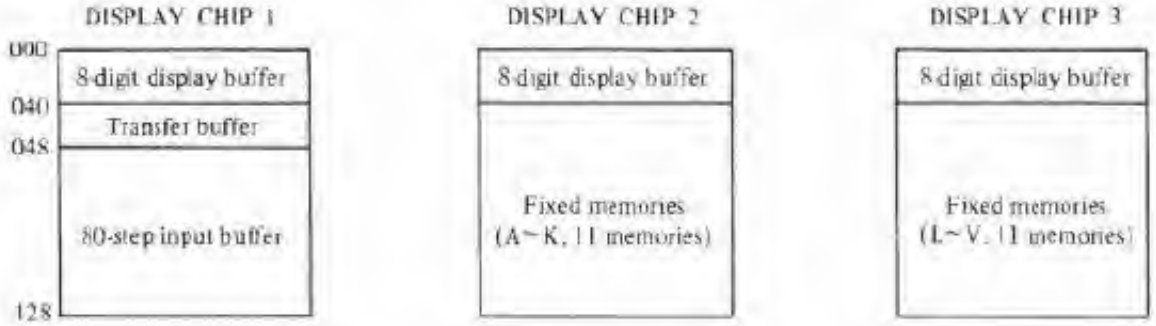
Three C-MOS RAMs (1 ~ 3 chips, 4K bits each) plus RAM incorporated in the display chip are used in this Pocket Computer, as described below:

- Map of 4K-bit RAM



Although RAM area is mainly shared by the program, data and reserve program memories, it is also used for the subroutine stack, FOR NEXT statement stack and fixed memories (W, X, Y, Z).

- Map of the RAM incorporated in the display chip
  There are three 1K-bit RAMs (128 bytes each) incorporated in each display chip (SC43123), with the following configurations:



- 8-digit display buffer
  40 bytes of 8-digit display buffer is used as a display data buffer during displaying and also used as a buffer memory for arithmetical results during arithmetical operations.

- Fixed memory
  The total memory of 176 bytes (from the display chip 2 and 3) is used as a fixed memories, A~V (22 memories).

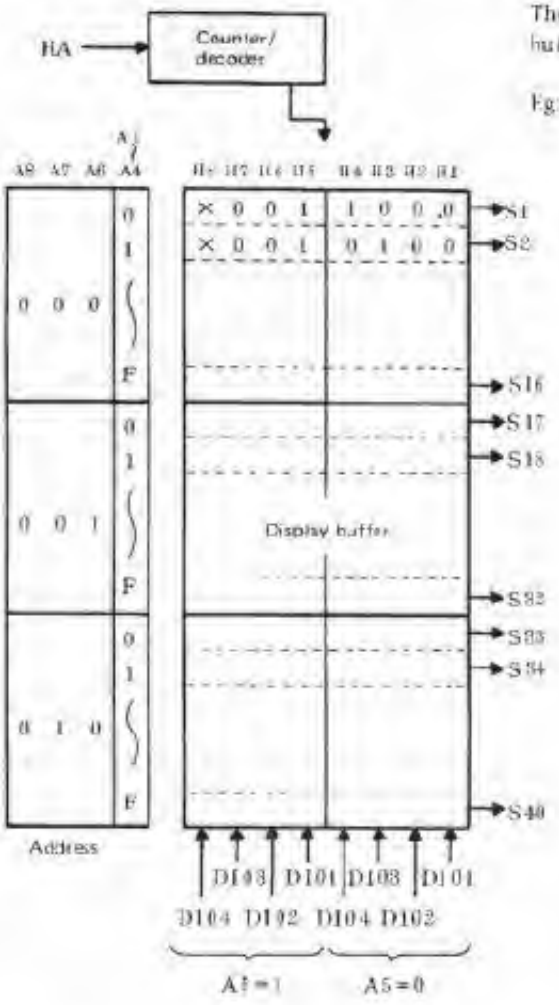
- Transfer buffer
  8 bytes (1 memory equivalent) of Display Chip 1 is used as a transfer buffer for transactions of instructions between CPU I and CPU II.

- Input buffer
  Remaining 80 bytes (10 memories equivalent) of Display Chip 1 is used for the input buffer, as follows:
  1. Any information entered through the keyboard is stored in this buffer, allowing up to 80 steps.
  2. The display contents are stored by CPU I, and CPU II selects data.
  3. When an arithmetical instruction is entered, its procedure is stored in this buffer by CPU I, and CPU II performs operations according to the procedure.
  4. When a program or reserve program is to be recorded or read out during the execution of the cassette control instruction, action takes place through this input buffer.

Overview of Display

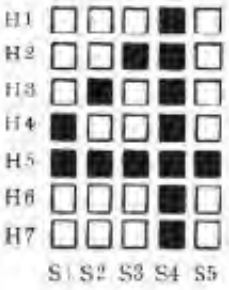
The contents of the display as indicated by CPU I is received by CPU II via the input buffer and are converted into respective character codes, they are transferred to the display buffer in the Display Chip through the address data bus.

- Designation of the display data
  The following structure is observed in the display buffer in the Display Chip.



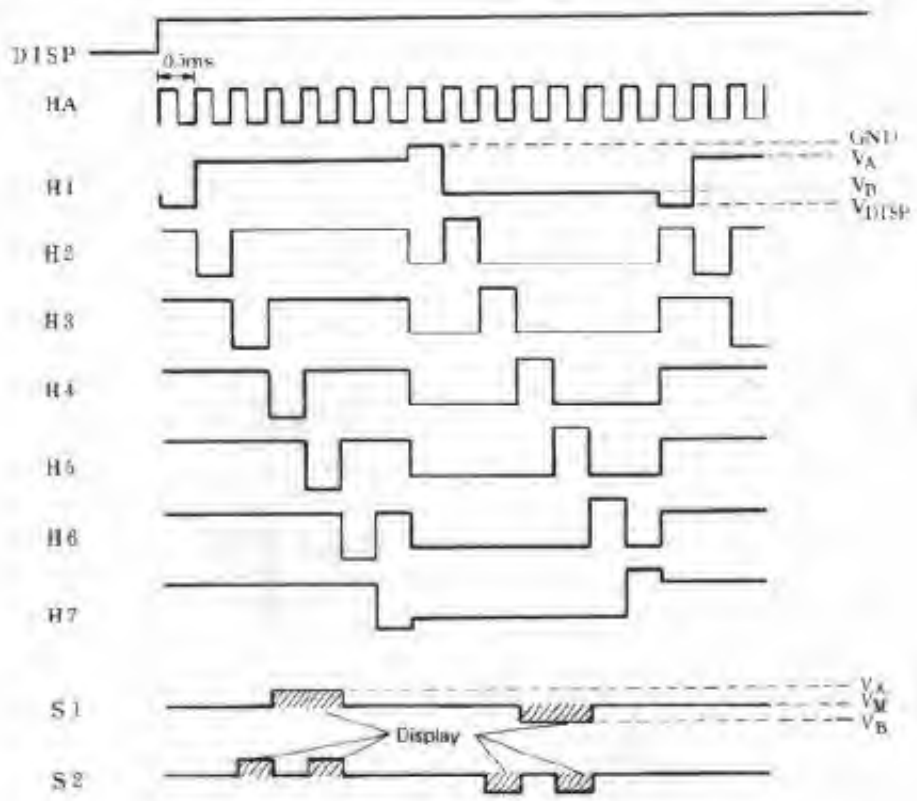
There are 8 x 40 = 320 bits (40 bytes) of area in the display buffer in the Display Chip.

Eg: Display numerical "4"



The numeral "4" (to be displayed by CPU II) is converted into the relevant character code and carried through on the address data bus. First, the segment S1 is selected with the address A8~A1 "00000000" to store the data DI04~DI01 "1000" in the display buffer (see above illustration). To store the second 4 bits of the data, only A5 in the address in turned "1" to make the address "00010000" to store data "0001". In the same manner, address "00000001" is selected for storing the first 4-bit data "0100" for segment S2 and the second 4-bit data "0001" is stored with the address "00010001".

Timing Signals for Displaying "4"

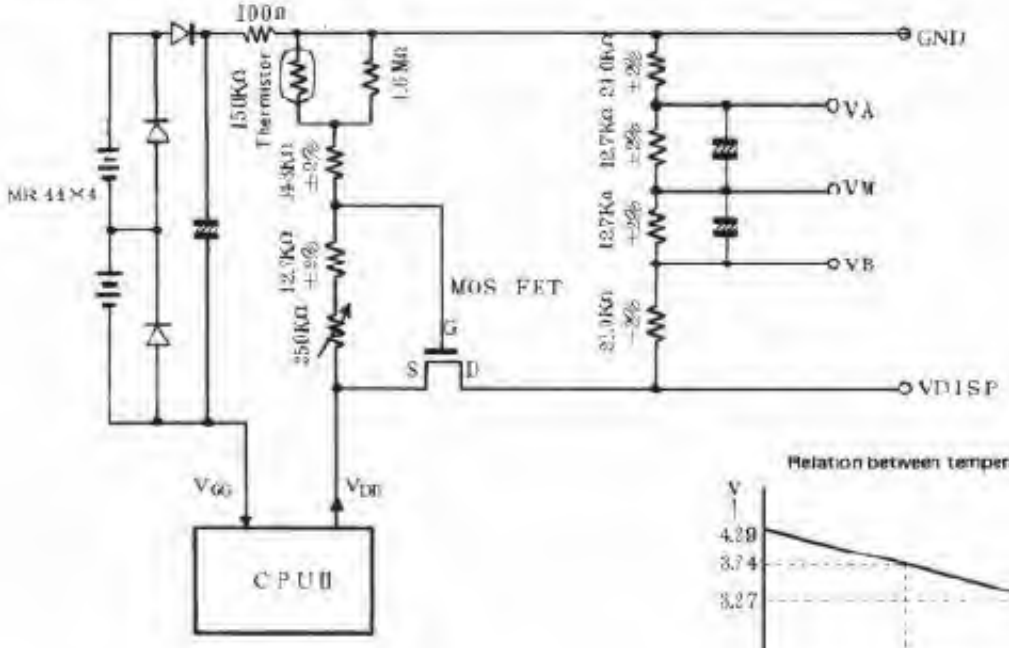


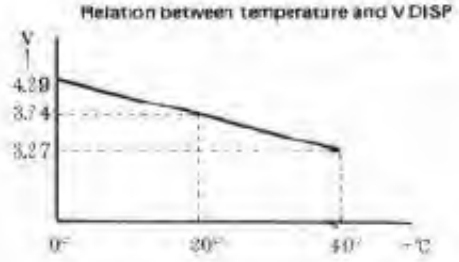
HA: Clock frequency for the counter. This signal is counted and decoded to perform synchronization with the common signal, H1 ~ H7, generated from CPU II.

DSIP: With high level of this signal, processing of display operation is indicated (RAM data designated by H1 ~ H8 is sent out on S1 ~ S40).

The data stored in the display buffer is carried through S1 ~ S40 (illustrated above) to be fed to the LCD. (To indicate "4" on the display, H4 and H5 are engaged for S1, H3 and H5 for S2, etc., through S6 ~ S40.)

Overview of Power supply





- The liquid crystal reference voltage VDISP is generated by the above circuitry to avoid blurred characters or contrast variations that might degrade display performance (which would be caused by a slight voltage variation in the liquid crystal reference voltage VDISP).

A. VDD is generated in CPU II, referenced to VGG.

B. The gate voltage of MOS FET is controlled by the 250KΩ pot to regulate the voltage for VDISP. The Thermister is provided to compensate for temperature variation.

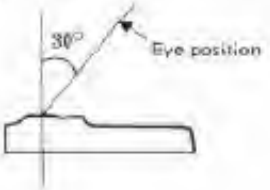
C. Reference voltage VDISP is divided by resistor combinations to provide VA, VM and VB.

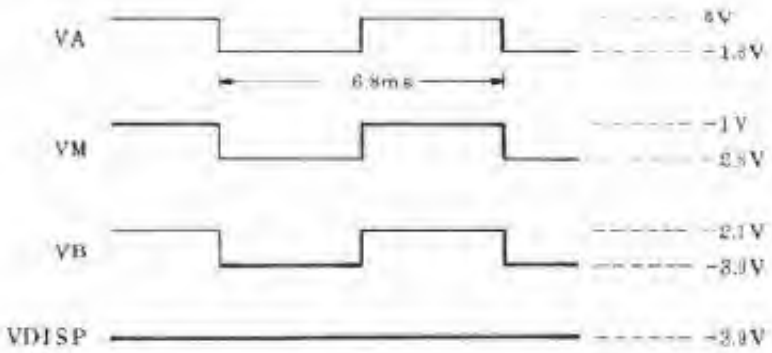
VDISP:	Low voltage for common signals (H) ~(47) for LCD
VA:	High voltage for segment signals (S1~S40)
VM:	Intermediate voltage for common and segment signals
VB:	Low voltage for segment signals.

NOTE: VA, VM and VB become pulses, with an amplitude of several volts, due to the influence of the LSI.

Adjustment of reference voltage VDISP

VDISP had been precisely adjusted to −3.74V at an ambient temperature of 20°C and −4.29V at 0°C. If it is necessary to readjust the voltage after servicing the LCD or changing some components, be sure to look at the Display from a 30° angle (from vertical) while adjusting the pot.





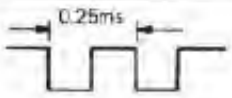
3. LSI SIGNAL DESCRIPTIONS

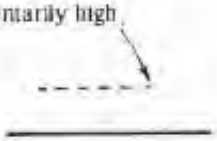
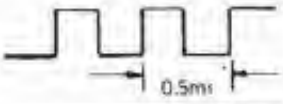
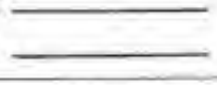
SC43177 (CPU I)

Pin No.	Signal name	In/Out	Description
1 2 3 4	F4a F3a F2a F1a	Out Out Out Out	Chip Enable signal (RAM3 select signal) Chip Enable signal (RAM2 select signal) Chip Enable signal (RAM1 select signal) Chip Enable signal (Display chip 1 select signal, for input buffer and transfer buffer usage) During display: Low During read-in: turns momentarily high 
6	V_{GG}	In	Source voltage ("-" voltage of battery)
7	V_{GG}	In	
8	Xin	In	Basic clock (pulse signal, 256kHz)
9 10	TEST1 TEST2		Connected to GND
11	RESET	In	All Reset Switch input Normally high but turns low when the All Reset Switch is pressed.
12	R/Wa	Out	RAM Data Read/Write signal During display: High Pressing a key causes it to momentarily go low.
13 14 15 16	DIO1 DIO2 DIO3 DIO3	In/Out In/Out In/Out In/Out	Data Bus (for address designation of the input buffer and transfer buffer in RAM and Display Chip 1) During display: High  During read-in: Low
17 18 19 20 21 22 23 24	B8a B7a B6a B5a B4a B3a B2a B1a	Out Out Out Out Out Out Out Out	Address Bus (for address designation of the input buffer and transfer buffer in RAM and Display Chip 1). During display Momentary generation During read-in 
30	GND	In	Source voltage (0V)
40	SIba	Out	Busy signal to CPU II (High during execution in CPU I) During display: Low During read in: turns momentarily high
41 42	Sn Si	Out Out	Key Strobe signal, RAM Address signal Key Strobe signal, RAM Address signal

Pin No.	Signal name	In/Out	Description
43 44 45 46 47 48 49 50 51 52 53 54	Sl3 Sl2 Sl1 Sl0 S9 S8 S7 S6 S5 S4 S3 S2	Out Out Out Out Out Out Out Out Out Out Out Out	Key Strobe signal During display: High Pressing a key causes it to momentarily go low
55 56 57 58	Ki1 Ki2 Ki3 Ki4	In In In In	Key input signal During display: Low Pressing a key causes it to momentarily go high
59	S16b (Ki5)	In	Busy signal of CPU II (high during execution of CPU II) During display: Low Pressing a key causes it to momentarily go high

SC43178 (CPU II)

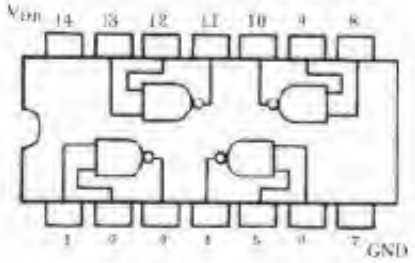
Pin No.	Signal	In/Out	Description
1	F4	Out	Buzzer signal When the buzzer is off: Low When the buzzer is on: High 
2 3 4	F3 F2 F1	Out Out Out	Chip Enable signal (Display chip 3 select signal) Chip Enable signal (Display chip 2 select signal) Chip Enable signal (Display chip 1 select signal) During display: Low During read-in: Turns momentarily high
5 6 7	V_{DD} V_{GG} V_{GG}	Out In In	For liquid crystal drive voltage preparation ($V_{DD} \approx V_{GG}$) Source voltage ("–" voltage of the battery)
8	Xin	In	Basic clock (Pulse signal, 256kHz)
11	RESET	In	All Reset Switch input
12	R/W	Out	RAM Data Read/Write signal During display: High During read-in: Turns momentarily low

Pin No	Signal name	In/Out	Description
13 14 15 16	DIO4 DIO3 DIO2 DIO1	In/Out In/Out In/Out In/Out	Data Bus (for data transaction between RAM and display chip) During display: High During read-in: Turns low 
17 18 19 20 21 22 23 24	B8b B7b B6b B5b B4b B3b B2b B1b	Out Out Out Out Out Out Out Out	Address Bus (for address designation of the display chip) During display: B1b = high, B2b = low, B3b = low, B4b = low, B5b = high, B6b = high, B7b = low, B8b = low During read-in: Turns momentarily high 
25	HA	Out	Display signal (Common signal counting pulse) Generated during display 
26	DISP	Out	Display command signal During display: High During execution: Low
27 28 29	VM VA GND	In In In	LCD display voltage (Intermediate voltage of the segment signal) LCD display voltage (High voltage of the segment signal) Supply voltage (0V)
30 31 32 33 34 35 36	H4 H7 H3 H6 H2 H5 H1	Out Out Out Out Out Out Out	LCD common signals (backplate)
37 38	V_{DISP} V_B	In In	LCD display voltage (Low voltage of the common signal) LCD display voltage (Low voltage of the segment signal)
39	S16	Out	Busy signal to the CPU I (High during execution in CPU II) During display: Low Pressing a key causes it to momentarily go high. 
40 41	S15 S15	Out Out	Record signal to the cassette tape and print data. Remote signal to the MT.
42	S13	Out	Busy signal to printer.
43	S12	Out	Expansion signal During display: Low Pressing the CA (ON) key causes an instant pulse generation. 

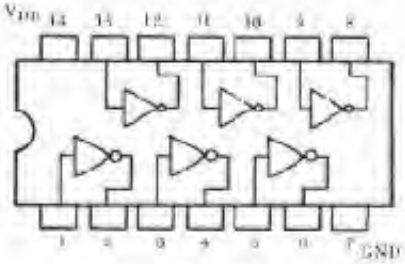
Pin No	Signal name	In/Out	Description
49	S6	Out	For DEF symbol display (engaged: low, not engaged: high)
54	S1	Out	For symbol display (SHIFT, DEG, RAD, GRAD, RESERVE, PRO, RUN) Same waveform as the segment signal.
55	Ki1 (S16a)	In	CPU 1 Busy signal (High during execution in CPU I)
56	Ki2	In	Expansion signal To be connected to SI 2 (CPU II).
57	Ki3	In	Printer Busy signal Low when the printer is not operated.
58	Ki4	In	Printer connection identifying signal. Low when the printer is not connected.
59 60	Ki5 Ki6	In In	Cassette recall signal ON key input signal.

IC Pin-out

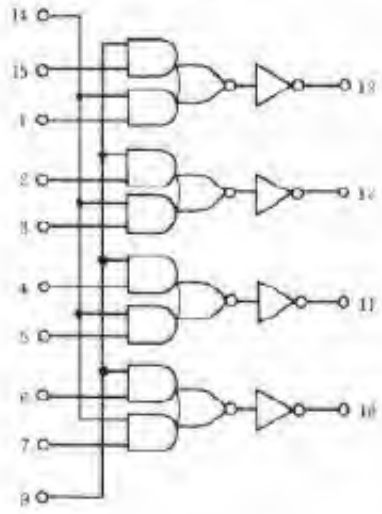
TC4011BP
(Quad 2-input positive NAND gate)



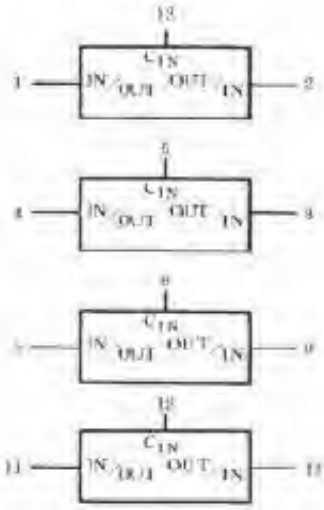
TC4069P
(HEX inverter)



TC4019BP
(Quad AND-OR select gate)

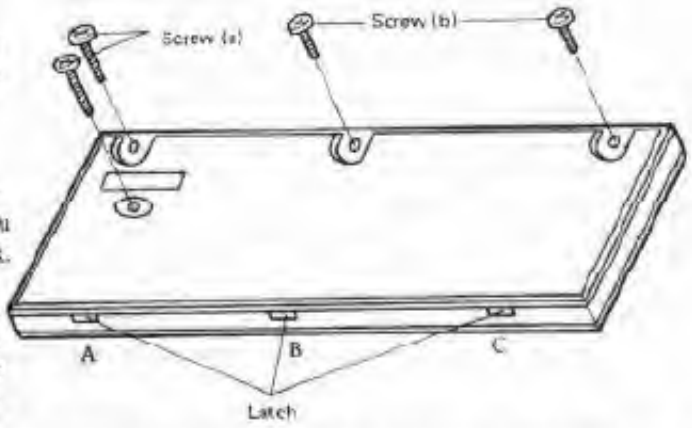


TC4066BP
(Quad bilateral switch)



4. BEFORE SERVICING

- **Disassembly procedure**
  1. Remove 2 screws (a) and 2 screws (b).
  2. From the screw side, separate the upper cabinet from the lower cabinet (they are latched together at three points, A, B and C).



- **Repairing procedure**
  1. The back of the arithmetic printed board will be exposed after the removal of the lower cabinet. You can check the arithmetic printed board from the back.
  2. Replacement of the CPU II is possible.
  3. If the key printed board is to be checked, the arithmetic printed board has to be bent at a right angle after removing the screws (d) and (e). Inspection of the CPU I is possible if the buzzer is removed after removing screw (c).
  4. The key printed board can be dismounted by removing 9 screws (f) and 2 screws (g). Take care as you remove the printed board, so you don't spill the key tops.

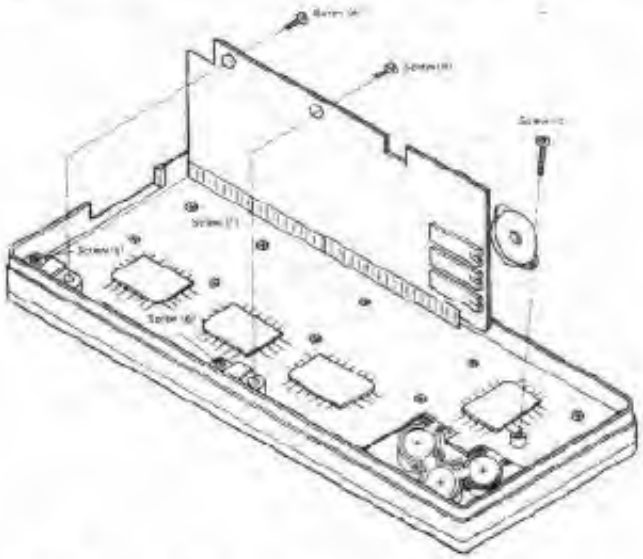
- **Replacement of the LSI**
  1. Only a very fine soldering pencil should be used for replacing the LSI.
  2. Be sure to first remove the key printed board from the upper cabinet, if the LSI on the key printed board is to be removed. If the LSI is removed while the key printed board is on the upper cabinet, there is a possibility of deforming the key rubber with the heat of the soldering pencil.
  3. Be sure to cut each pin of the defective IC.

- **Measuring current consumption**

  Power source voltage: 4.72V

  Current consumption:

After pressing the ON key:	Under 850μA
After pressing the OFF key:	Under 12μA



5. CASSETTE TAPE & INTERFACE

For details of operation and connection, refer to the Owner's Manual for the TRS-80 Pocket Computer.

Notes on suitable recorders

While Radio Shack's CTR-80A is the intended Cassette Recorder, others can be used. The following notes may be helpful:

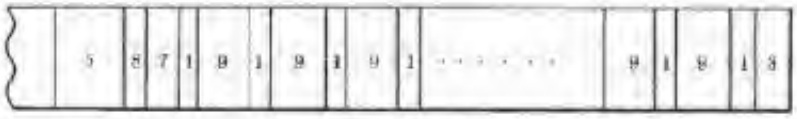
1. Cassettes or open-reel types can be used.
2. Mic input jack must have an input impedance of 1K or less, with a sensitivity level of at least 3mV.
3. Earphone output must have an output impedance of 10K or less and an output level of 1 volt or more.
4. Allowable distortion is ±15%, with frequency response from 2 to 4kHz.

6. CASSETTE OPERATION

Recording

Recording method

Recording format of program or reserve program

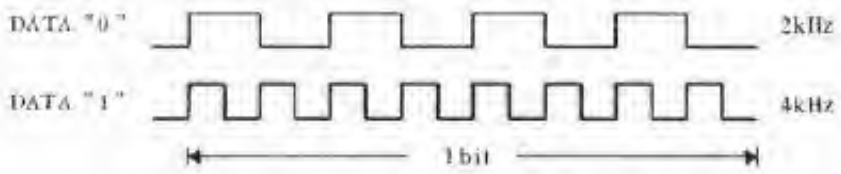


Data memory recording format

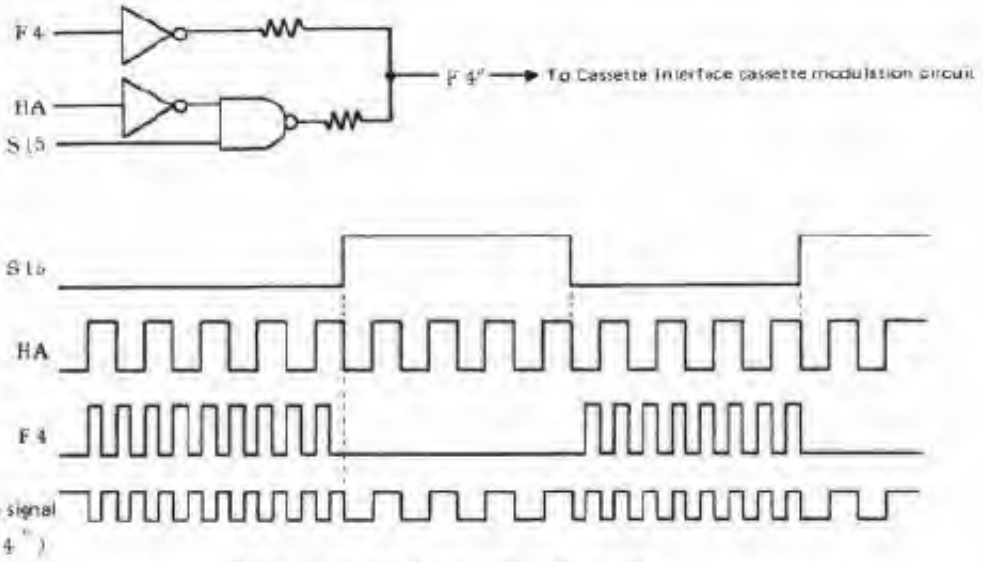
1 = Check sum code (after every 8 steps or one data memory.)
2 = 8 steps of program or reserve program
3 = End code of recording.
4 = This gap, compised of all "1s", is inserted at each line to fill up the full 80 steps, during which time the next 80 steps of data to be input is prepared in the input buffer.
5 = All "1s" are recorded for a period of about 6 seconds in order to avoid non-recordable area located at the beginning of the tape; it also is used for cuing of the recording head.
6 = Program or reserve program name is indicated.
7 = File name
8 = Data memory is indicated with this code
9 = Area for one data memory.

Recording method

Data "0" and "1" are identified by changing the frequency of the recording signal (F4")



Recording signal (F4") generation circuit

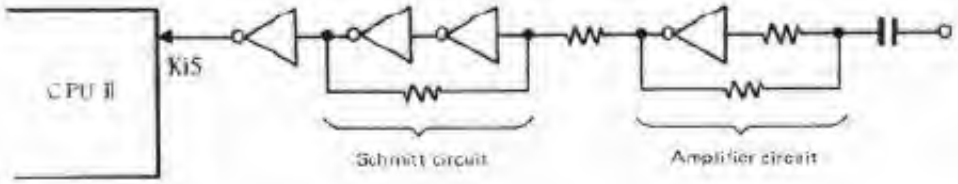


Signal waveform at the time of recording

When a recording signal "1" is to be recorded, S15 is set low and signal F4 (clock pulse of ≅ 4kHz) is output during that period. When a recording signal "0" is to be recorded, S15 is set high and F4 output is inhibited during that period [at which time the reverse signal of HA (clock pulse of ≅ 2kHz) is carried on the recording signal].
This signal is supplied to the MIC jack of the tape recorder via the modulation circuit of the Cassette Interface.

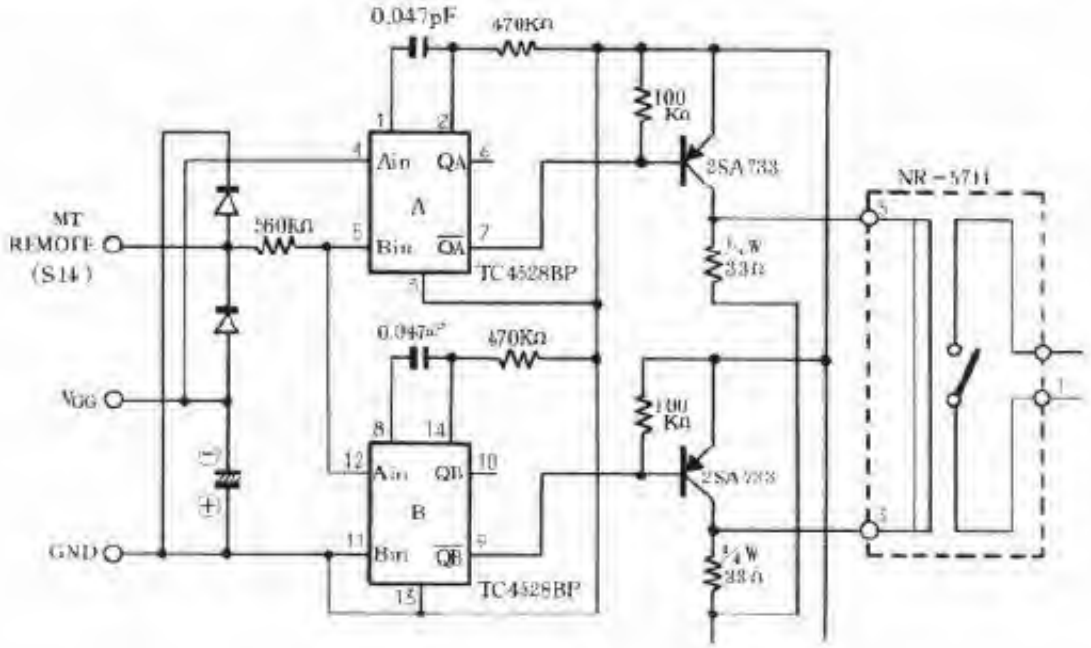
Reproduction

Output signal from the EAR jack of the tape recorder is amplified and shaped in the Schmitt circuit, to be input to CPU II through Ki5 terminal of CPU II.

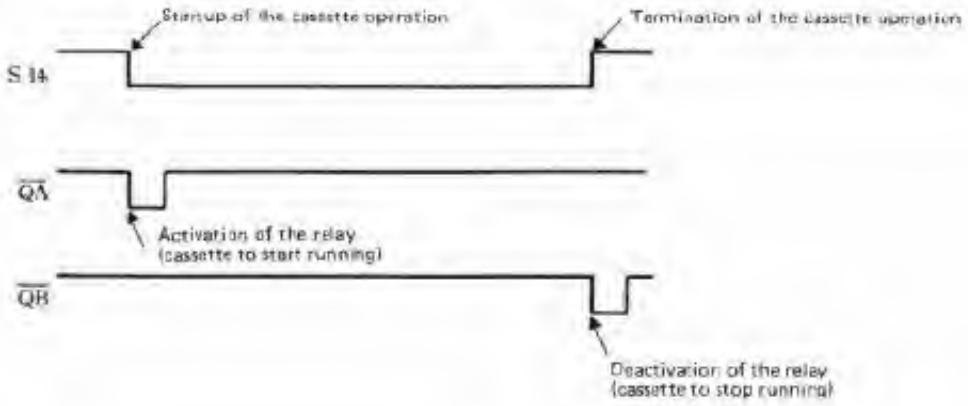


Remote control

The Cassette Interface will control the REMOTE jack automatically for record, playback and verify commands.



The IC-4528P is a mono-stable multivibrator (to perform trigger and reset functions from the single chip).
"A" outputs a pulse which is dependent on the time constant of CR at the falling edge of the input signal, and "B" outputs a pulse which is dependent on the time constant of CR at the rising edge of the input signal. The relay operates ON and OFF according to the current flow to the coil, and is activated when "A" is active and deactivated when "B" is active.



Testing the Cassette Interface

1. Writing test data into the Pocket Computor

First enter test data to check the Interface.

No.	Read in	Display	Remarks
1	[MODE] ~ [MODE]	> RESERVE	Display RESERVE mode.
2	NEW	NEW_ RESERVE	
3	[ENTER]	> RESERVE	
4	[SHFT] Z	Z:_ RESERVE	
5	P. # [SHFT] ▼A▼ [SHFT] ; A(204)	Z: P. # ▼A▼; A(204) RESERVE	
6	[ENTER]	Z: PRINT # ▼A▼ ; A(204) RESERVE	
7	[SHFT] X	X:_ RESERVE	
8	L # [SHFT] ▼A▼ [SHFT] ; A(204)	X: 1. # ▼A▼; A(204)_ RESERVE	
9	[ENTER]	X: INPUT # ▼A▼; A(204) RESERVE	
10	[SHFT] [SPC]	_ RESERVE	
11	A(204)	: A(204) RESERVE	
12	[ENTER]	: A(204)	
13	[MODE]	> DEF	
14	[MODE]	> RUN	
15	[SHFT] [SPC] = 100	A(204) = 100_ RUN	
16	[ENTER]	RUN 100	

2. Checking the Cassette Interface

Assumes that step 1 has already been executed.

No.	Read in	Display	Remarks
1	[OFF]		
2			Connect the Cassette Interface to the tape recorder.
3			Connect the Pocket Computer to the Cassette Interface.
4	[ON]	> RUN	Make sure that RUN is on the display (use [MODE] key)
5		> RUN	Position Tape correctly.

No.	Read in	Display		Remarks
6		>	RUN	Press REC and PLAY button.
7	SHFT Z	PRINT #▼A▼; A(204)_	RUN	
8	ENTER		RUN	The cassette will run and produce sound.
9		>	RUN	The cassette will stop and sound will cease.
10		>	RUN	Rewind the tape to the beginning of the recording.
11		>	RUN	Press PLAY button.
12	SHFT X	INPUT #▼A▼; A(204)_	RUN	
13	ENTER		RUN	The cassette will run and produce sound.
14		>	RUN	The cassette will stop and sound will cease.
15	SHFT SPC	A(204)_	RUN	
16	ENTER	RUN	100.	
17		RUN	100.	Push STOP button.
18	OFF			
19				Disconnect units and cables.

I. Inspection is required if any of following conditions occur:
   1. If cassette starts to run at Step 6.
   2. If cassette fails to run or no sound is heard at Step 8.
   3. If cassette does not stop at Step 9.
   4. If no sound is heard at Step 13.

II. Repeat the procedure if the following occurs:
   1. When "5 ... ..." is displayed at Step 13, repeat operation from Step 10. If the same indication is still on the display, repeat the procedure from Step 5 after entering "A(204)=100". If the same indication remains on the display even after this, detailed inspection is required.
   2. When "100." is not displayed at Step 16, repeat operation from Step 10. If the specific indication does not appear on the display, repeat the procedure from Step 5 after entering "A(204)=100". If the specific indication is not to appear on the display even after this, detailed inspection is required.

Repairing the Cassette Interface

Program

```
10 : PRINT #▼0▼; A(201) : PAUSE 1
   0 : GOTO 10
```

Use the following procedures to evaluate the Cassette Interface.

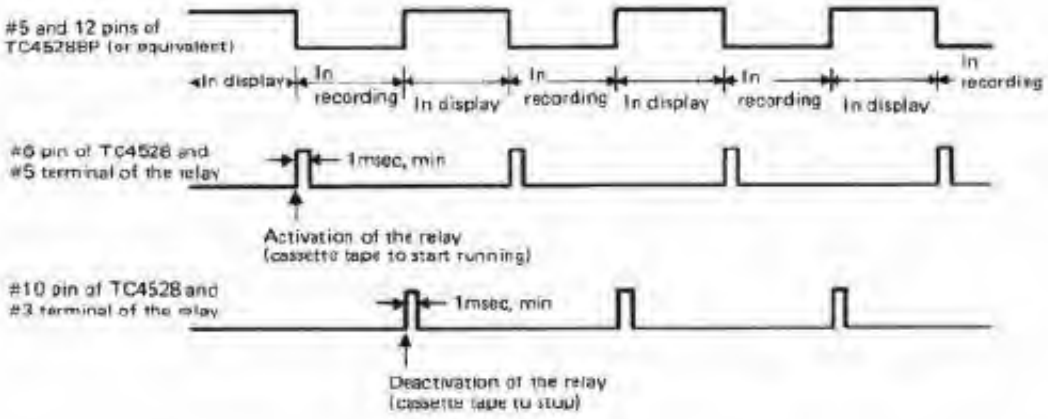
No.	Read in	Display	Plug			Tape recorder			Remarks
			EAR PHONE	MIC	REM OTE	PLAY	REC	STOP	
1	([OFF])								Connect Computer to Interface.
2	[ON]	> RUN	○	○					Determine recording location on the tape.
3		> RUN	○	○	○	○	○		Make sure that the tape does not run.
4	CS. [SHFT] ▼A	CS.▼A RUN	○	○	○	○	○		
5	[ENTER]	RUN	○	○	○	○	○		The tape starts to run and recording sound will be heard.
6		> RUN	○	○	○			○	The sound will cease and the tape will stop when ">" is displayed.
7		> RUN	○	○					Rewind tape to the beginning of the recording.
8		> RUN	○	○	○	○			
9	CLO.? [SHFT]▼A	CLO.?▼A RUN	○	○	○	○			
10	[ENTER]	RUN	○	○	○	○			The display contents will disappear, tape will start and sound will be produced.
11		> RUN	○	○	○			○	Sound and tape will stop when ">" is displayed.
12		RUN							
13	[OFF]								

○ = Connected or activated

[NOTES]

1. Check the Computer, if the cassette tape keeps running in Step 3, fails to run in Step 5, or the tape does not stop in Step 6.
2. Check the recording circuit of the Interface if no recording sound is audible at Step 5.
3. If no sound is audible at Step 10, playback another recorded tape to check if sound is audible with that tape. If sound is not audible with that tape, check the reproducing circuit of the Interface. If sound is audible with the second tape, check the recording circuit of the Interface.

No.	Read in	Display	Remarks
1	RUN	RUN_ RUN	No tape recorder motion.
2	ENTER	RUN	Recording sound is audible.
3		RUN	Recording sound ceases and "10." is displayed for about 1 second.
4		RUN	



Cassette ON/OFF control must be properly executed when the above signals are observed during execution of program.

7. CHECK PROGRAM

		READ IN	DISPLAY
1		ON	>
2		ALL RESET	>
3		5/9 ENTER	5 . 5 5 5 5 5 5 5 5 5
4		MODE	>
5		1 P . SHFT " O K SHFT " ENTER	1 : P R I N T " O K "
6		2 SHFT " Z SHFT " P .	2 " Z " P
7		SHFT # S SHFT # ENTER	2 : " Z " P R I N T " S "
8		3 B E E P 2 ENTER	3 : B E E P 2
9		MODE	>
10		G R A D ENTER	>
11		SHFT SPC 0 1 4 7 ENTER	0 1 4 7
12		MODE	>
13		SHFT Z	S
14		MODE SHFT SPC	0 1 4 7
15		CL R A D . ENTER	>
16		R . ENTER	O K
17		ENTER	S
18		ENTER	>
19		OFF	
20			
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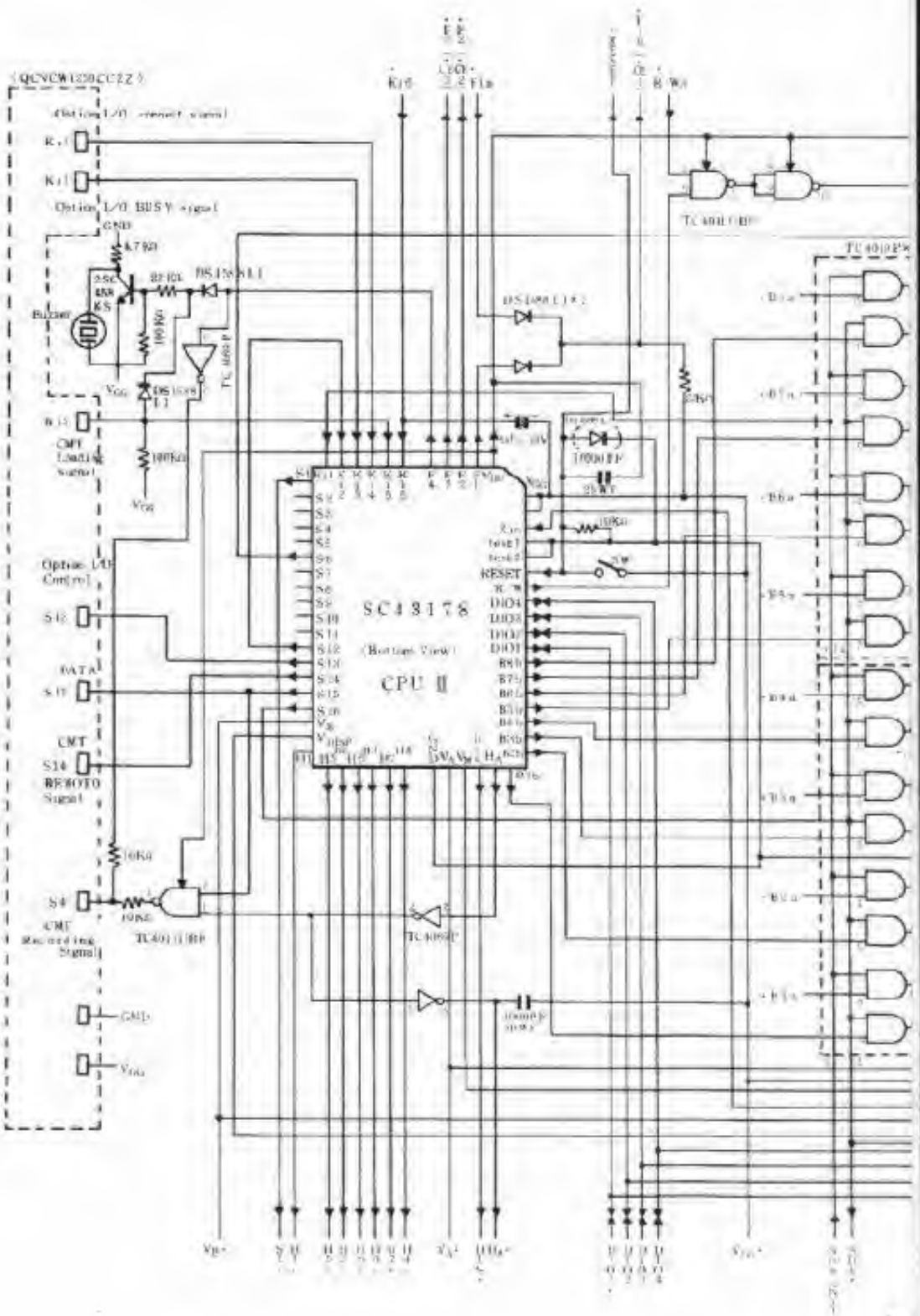
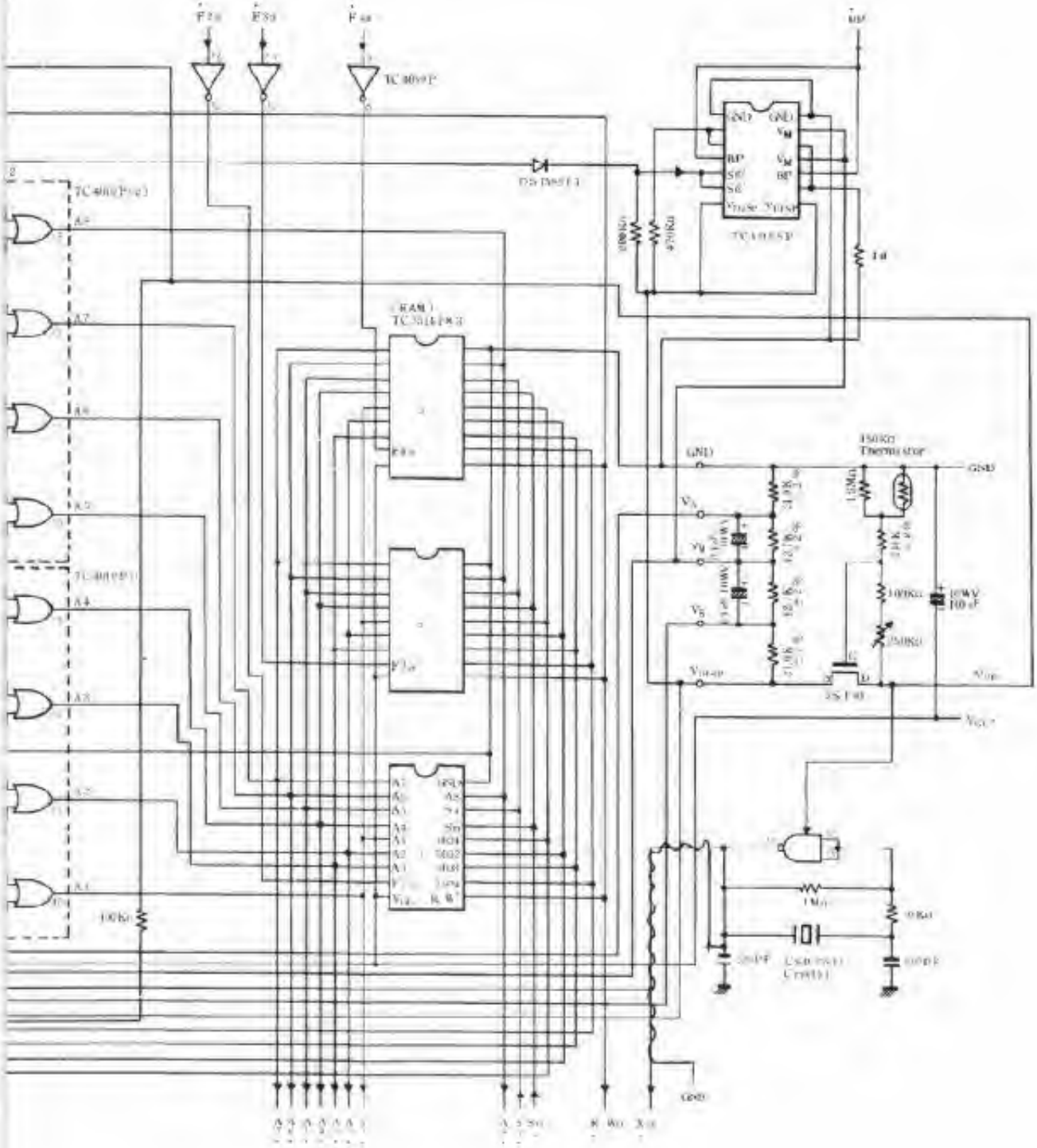
					SYMBOL										Cassete				
)	21	22	23	24	SHFT	DEG	RAD	GRAD	DEF	RUN	PRO	RES. ERVE	Sound		PLAY	REC	STOP	REMOTE	
						○				○									
	E	−	0	1		○				○									
						○					○								
					(○)	○					○								
					(○)	○					○								
					(○)	○					○								
						○					○								
						○						○							
								○				○							
					(○)			○				○							
								○	○										
					(○)			○	○										
					(○)			○		○									
							○			○									
							○			○									
							○			○									
							○			○			○						

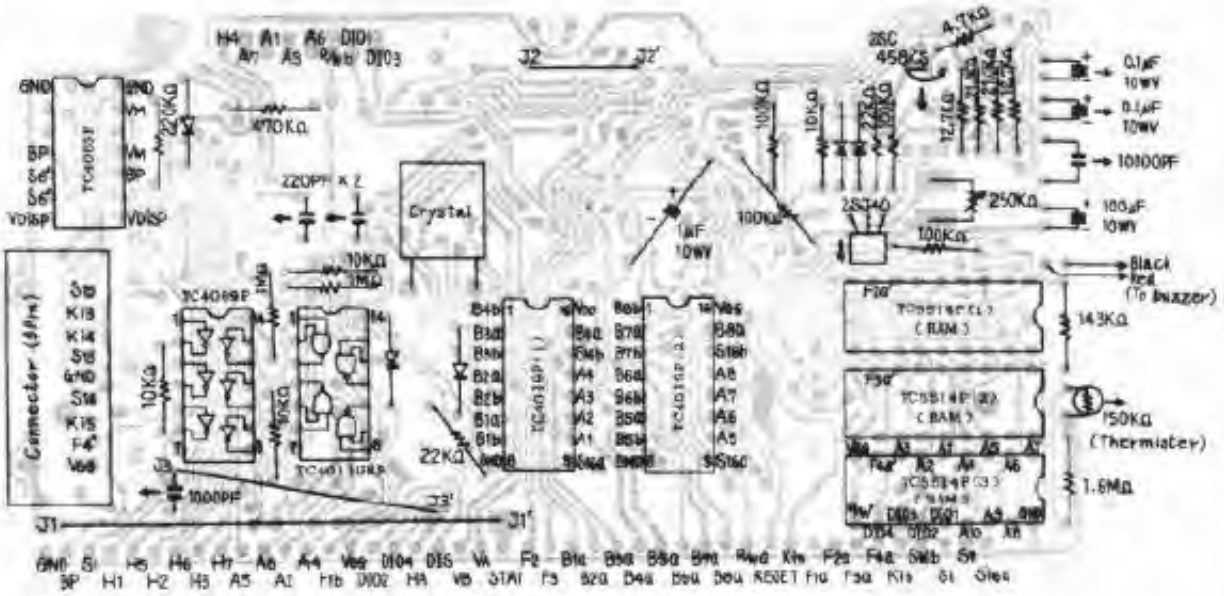
Circuit Diagram



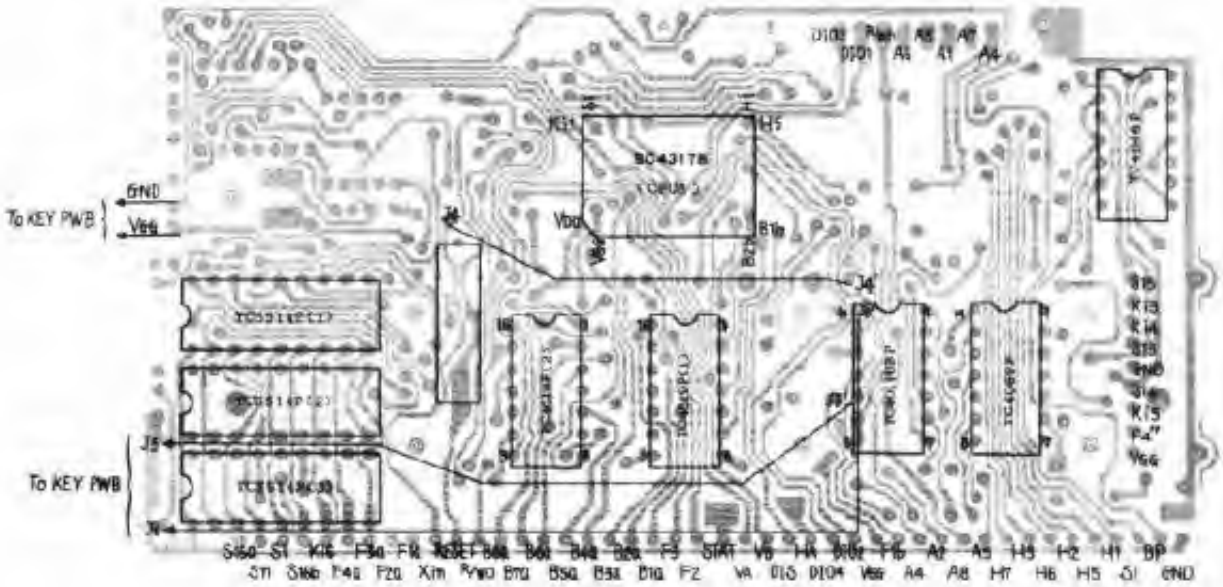
& SIGNALS POSITION



Operation P.C.B.

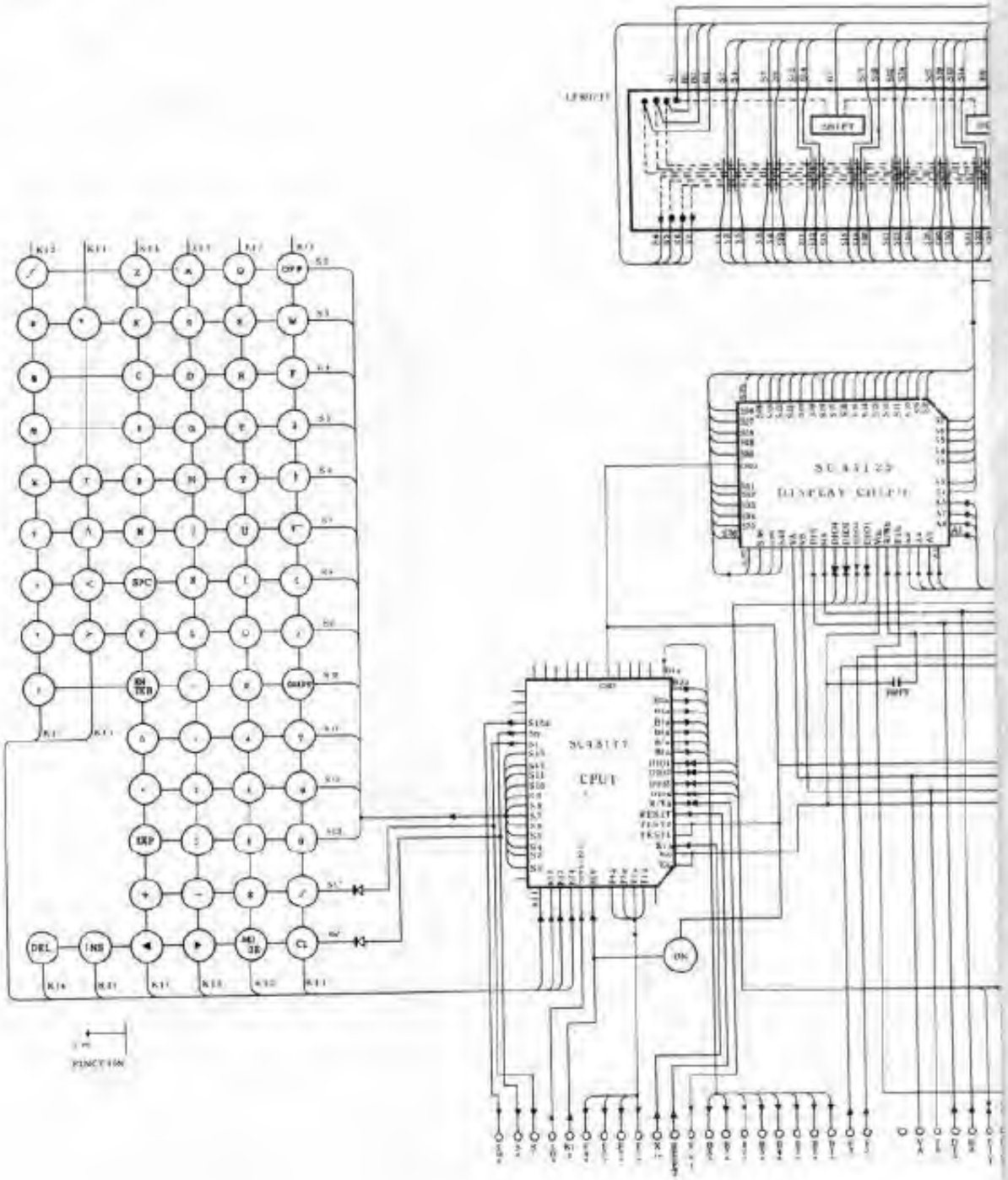


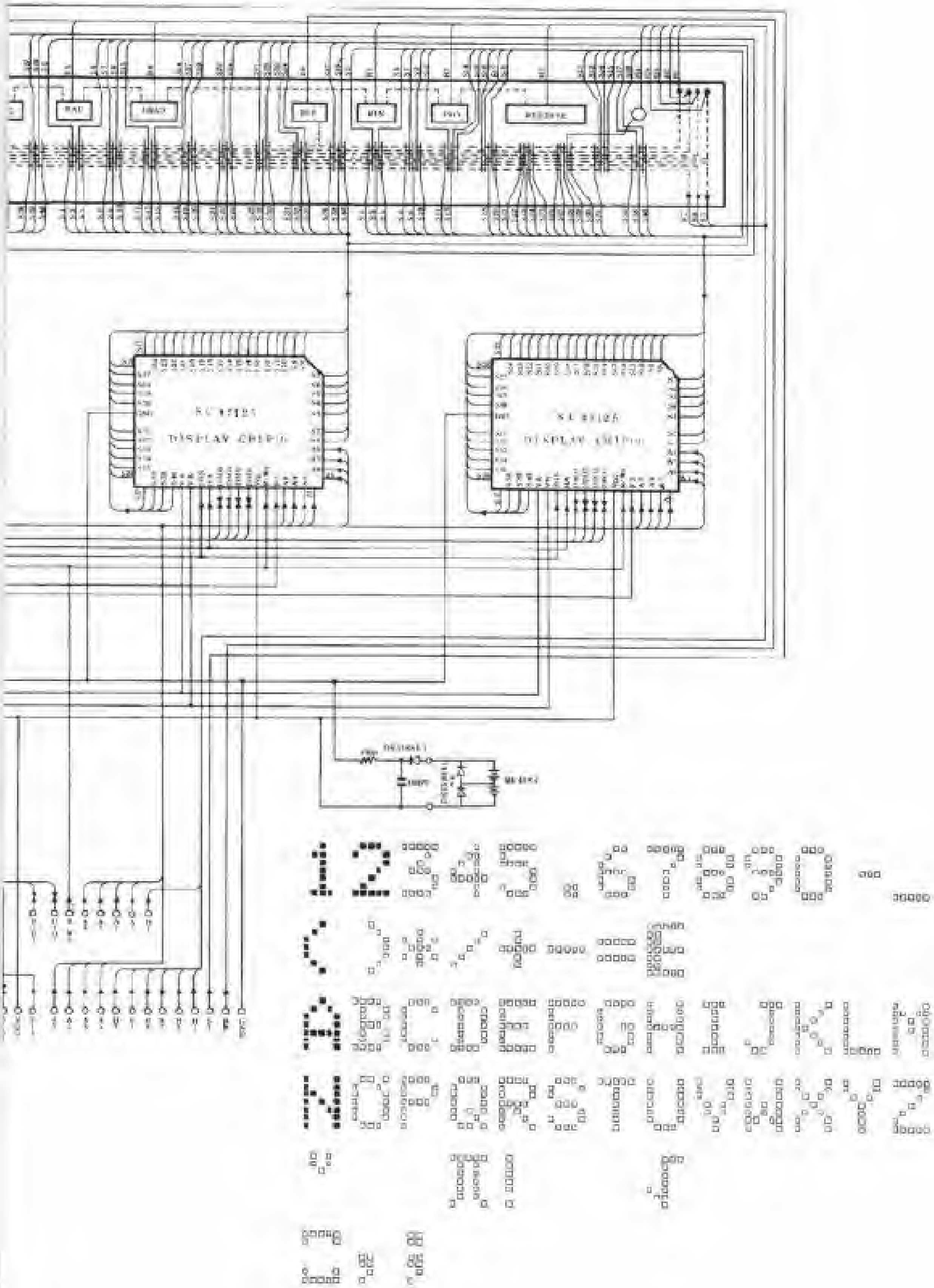
TOP VIEW



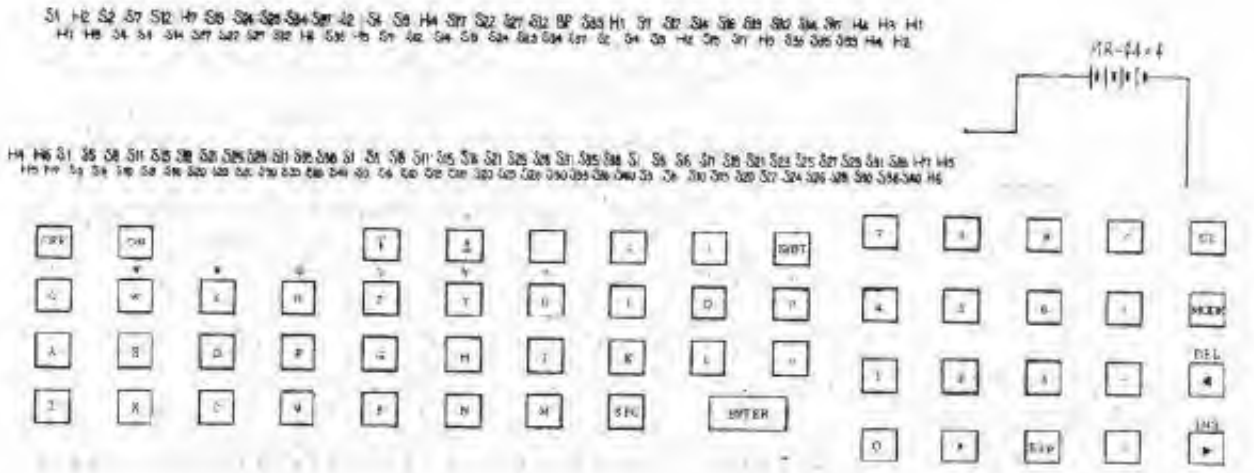
BOTTOM VIEW

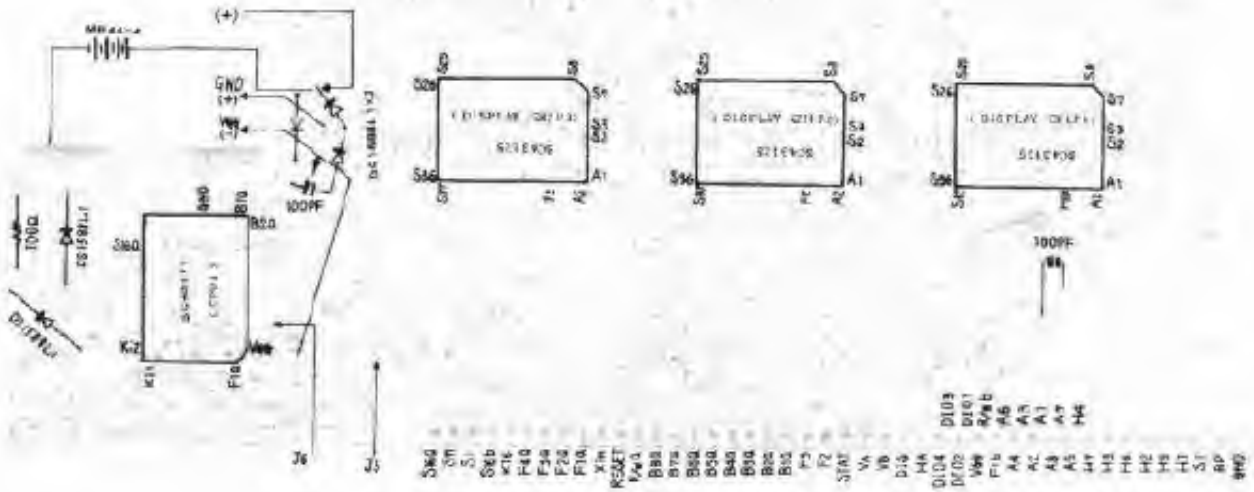
Key Circuit



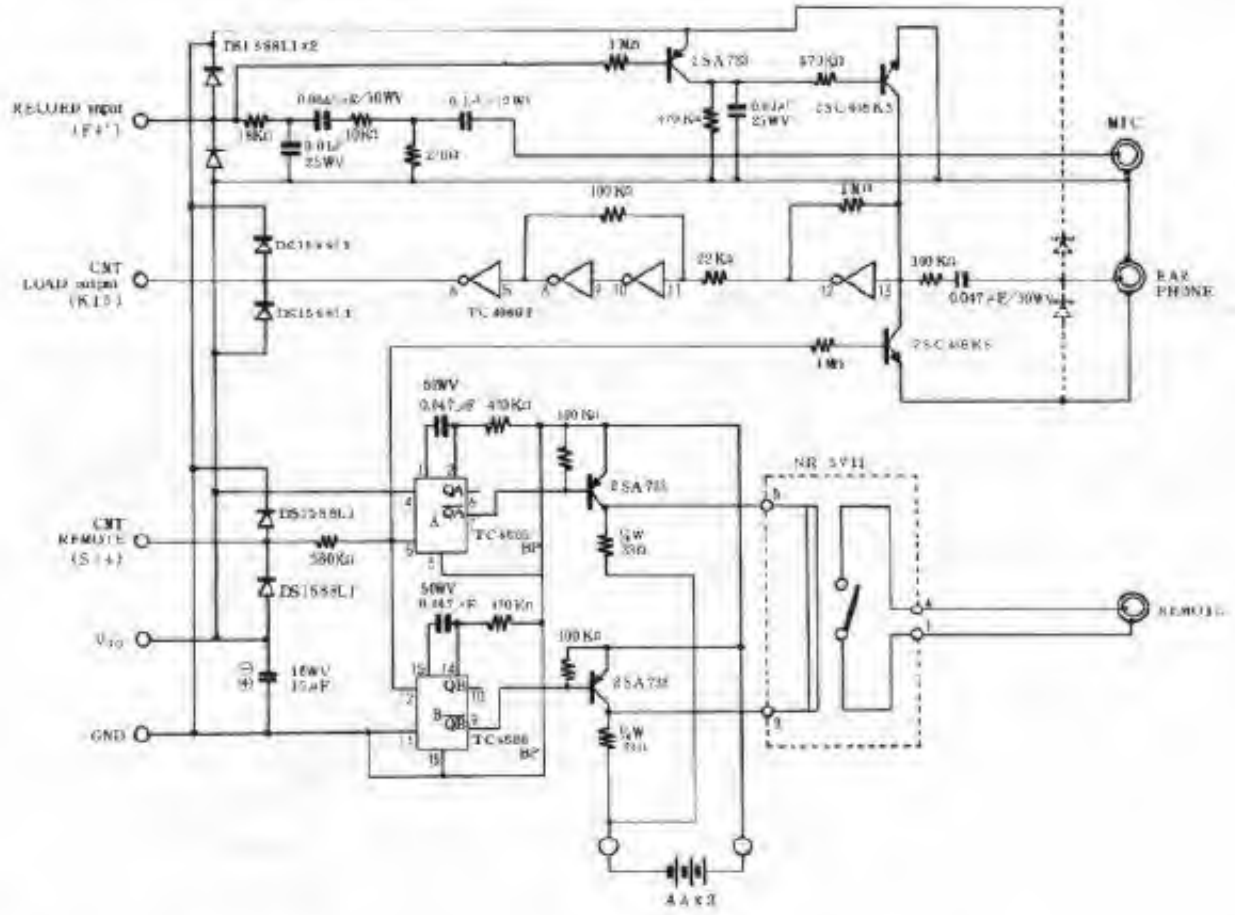


Key P.C.B.

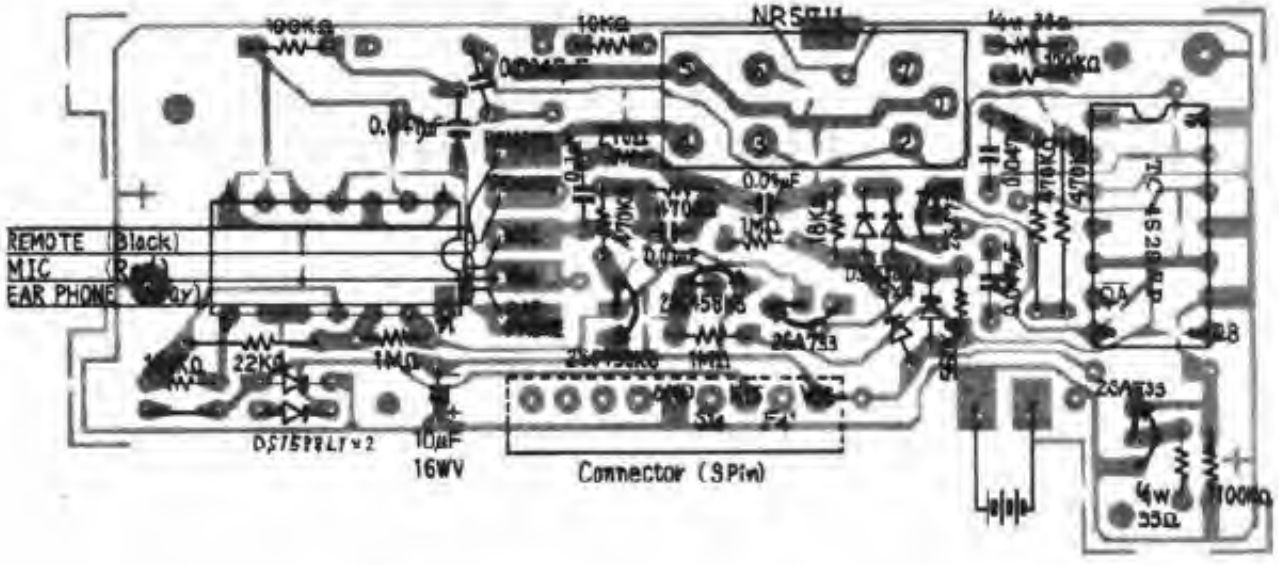




Interface Circuit Diagram



Interface P. C.B.



9. PARTS LIST FOR 26-3501

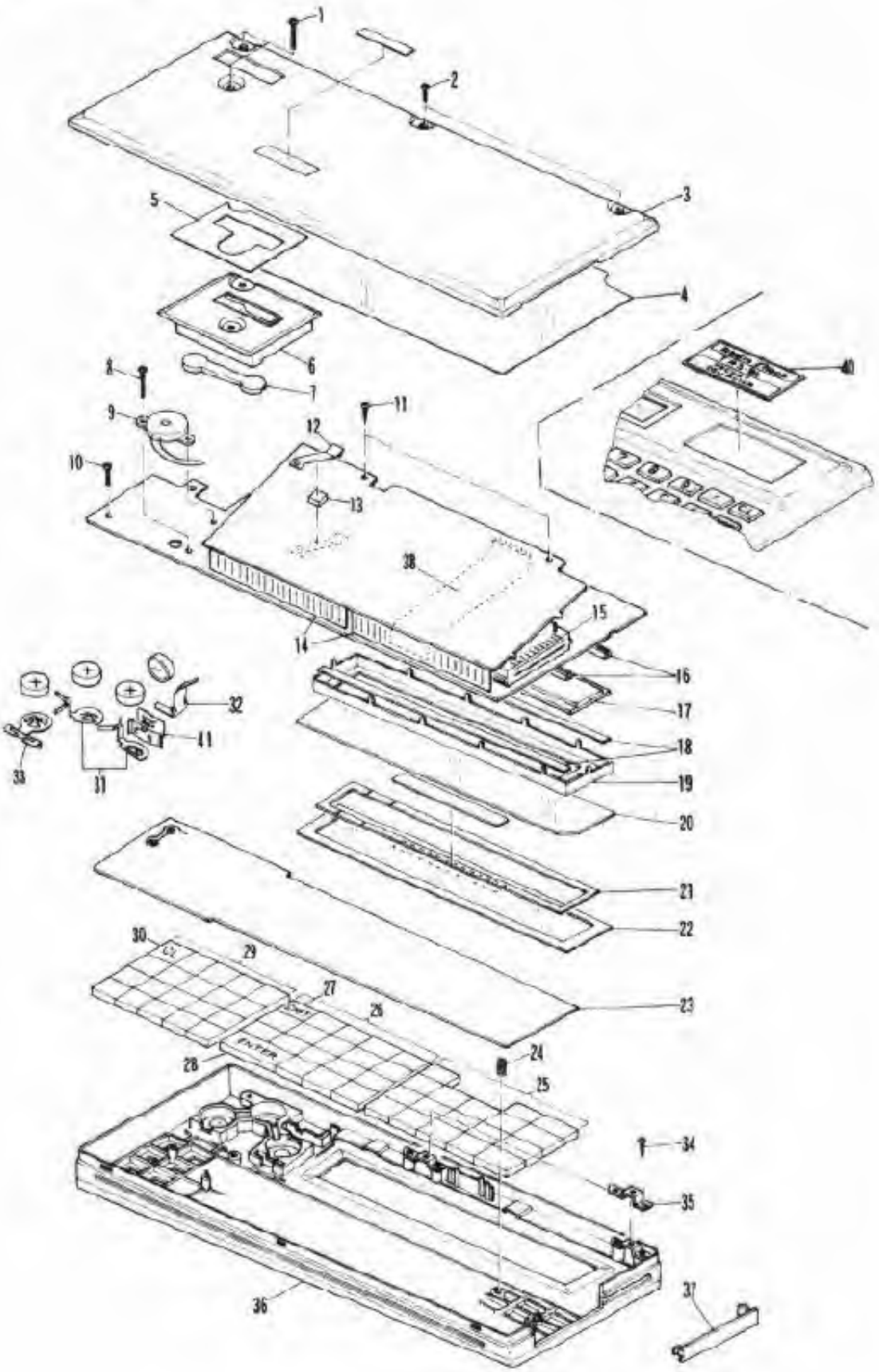
Ref. No.	Description	RS Location	Manufacturer Part Number
1	Special screw (M2 x 13)	AHD-1586	LX-BZ1084CCZZ
2	Special screw (M2 x 5)	AHD-1587	LX-BZ1032CCZZ
3	Bottom cabinet	AZ-5633	HDECA1765CCZZ
4	Insulator sheet	AHB-9950	PZETL1355CCZZ
5	Tape for interface lock plate	AHB-9951	PTPEH1062CCZZ
6	Interface lock plate	AZ-5634	LCHSS1091CCZZ
7	Lid for interface lock plate	ADA-0314	GFTAA1246CCZZ
8	Screw (M2 x 9)	AHD-1588	XBPSD20P09000
9	Buzzer	B-7073	RALMB1006CCZZ
10	Special screw (M2 x 5)	AHD-1589	LX-BZ1060CCZZ
11	Screw (M2 x 5)	AHD-1590	XTPSD20P05000
12	All reset switch	AS-0692	QCNTM1036CCZZ
13	Cushion for reset switch	AHB-9957	PCUSS1081CCZZ
14	Flexible wire (22 pin)	AW-2521	QCNW-1135CCZZ
15	Connector (9 pin) for Cassette Interface	AJ-0831	QCNCW1259CC01
16	Rubber connector for LCD	ART-2985	PGUMS1190CCZZ
17	LCD	AL-1180	VVLLF8017JE-1
18	Tape for LCD	AHB-9953	PTPEH1033CCZZ
19	Frame for LCD	ART-2986	LANGK1290CCZZ
20	Filter for LCD	AG-0430	PFILW1230CCZZ
21	Display mask	ART-2987	HDECA1527CCZZ
22	Display filter	ART-2991	PFILW1228CCZZ
23	Key rubber	ART-2988	PGUMM1254CCZZ
24	Ground spring	AHB-9923	MSPRC1098CCZZ
25	Key top (18 key) (Left halves)	AK-4274	JKNBZ1515CC04
26	Key top (17 key) (Right halves)	AK-4275	JKNBZ1515CC05
27	Key top (SHFT) (20 pcs/1 set)	AK-4219	JKNBZ1516CC02
28	Key top (ENTER) (10 pcs/1 set)	AK-4220	JKNBZ1566CC01
29	Key top (Numeral)	AK-4221	JKNBZ1621CC01
30	Key top (CL) (20pcs/1 set)	AK-4222	JKNBZ1622CC01
31	Battery terminal (+, –)	AHB-9954	QTANZ1287CCZZ
32	Battery terminal (+)	AHB-9955	QTANZ1292CCZZ
33	Battery terminal (–)	AHB-9956	QTANZ1250CCZZ
34	Screw (M2 x 4)	AHD-1591	XUSSD20P04000
35	Bracket for bottom cabinet	AHB-9957	LANGT1336CCZZ
36	Top cabinet	AZ-5635	CCABB2381CC01
37	Lid for connector	ADA-0315	GFTAA1245CCZZ
38	Flexible wire (8 pin)	AW-2522	QCNW-1137CCZZ
39	Soft case	AZ-5636	UBAGC1230CCZZ

Ref. No.	Description	RS Location	Manufacturer Part Number
40	Badge	AHB-9961	HBDGE1341CCZZ
41	Battery terminal (+, −)	AHB-9958	QTANZ1293CCZZ
	PCB (Key unit)	AX-8546	DUNTK5567CCZZ
	PCB (CPU unit)	AX-8547	DUNTK5568CCZZ
	Template	AHB-9959	LPLTP1070CCZZ
	Name label	AHB-9960	TLABZ1295CCZZ
	Carbon resistor 1/8W 143K 2%	AN0583CBB	RR-DZ1006CCZZ
	Carbon resistor 1/8W 12.7K 2%	AN0584CBB	RR-DZ1007CCZZ
	Carbon resistor 1/8W 21K 2%	AN0308CBB	RR-DZ1008CCZZ
	Variable resistor (250K)	AP-7105	RVR-M8510CCZZ
	Capacitor (Electrolytic) 100μF 10V +80/−20%	ACC105ZJCP	VCEAAU1AW107O
	Capacitor (Ceramic) 220PF 50V ±10%	ACC221KJCP	VCKYPU1HB221K
	Diode, DS1588L1	ADX-1405	VHDDS1588L1-1
	Thermister (150K)	AT-1218	VHH154KD-5/-1
	LSI (Display chip), TC43125	AXX-3032	VHiSC43125/-1
	LSI (CPU-1), SC43177	AXX-3033	VHiSC43177/-1
	LSI (CPU-2), SC43178	AXX-3034	VHiSC43178/-1
	IC, TC4011UBP	AMX-4439	VHiTC4011UBP1
	IC, TC4019P	AMX-4440	VHiTC4019P/-1
	IC, TC4066P	AMX-4441	VHiTC4066P/-1
	IC, TC4069P	AMX-4442	VHiTC4069P/-1
	LSI (Ram)	AXX-3035	VHiTC5514P/-1
	Solid resistor 1/8W 1.6Mohm 5%	AN0536EBB	VRC-MT26G165J
	Carbon resistor 1/8W 100 ohm 5%	AN0132EBB	VRD-ST26Y101J
	Carbon resistor 1/8W 22K 5%	AN0311EBB	VRD-ST26Y223J
	Carbon resistor 1/8W 10K 5%	AN0281EBB	VRD-ST26Y103J
	Carbon resistor 1/8W 100K 5%	AN0371EBB	VRD-ST26Y104J
	Carbon resistor 1/8W 1Mohm 5%	AN0445EBB	VRD-ST26Y105J
	Carbon Resistor 1/8W 4.7K 5%	AN0247EBB	VRD-ST26Y472J
	Carbon resistor 1/8W 470K 5%	AN0423EBB	VRD-ST26Y474J

Ref. No.	Description	RS Location	Manufacturer Part Number
40	Badge	AHB-9961	HBDGE1341CCZZ
41	Battery terminal (+, −)	AHB-9958	QTANZ1293CCZZ
	PCB (Key unit)	AX-8546	DUNTK5567CCZZ
	PCB (CPU unit)	AX-8547	DUNTK5568CCZZ
	Template	AHB-9959	LPLTP1070CCZZ
	Name label	AHB-9960	TLABZ1295CCZZ
	Carbon resistor 1/8W 143K 2%	AN0583CBB	RR-DZ1006CCZZ
	Carbon resistor 1/8W 12.7K 2%	AN0584CBB	RR-DZ1007CCZZ
	Carbon resistor 1/8W 21K 2%	AN0308CBB	RR-DZ1008CCZZ
	Variable resistor (250K)	AP-7105	RVR-MB5100CZZ
	Capacitor (Electrolytic) 100µF 10V +80/−20%	ACC105ZJCP	VCEAA01AW107O
	Capacitor (Ceramic) 220PF 50V ±10%	ACC221KJCP	VCKYPU1HB221K
	Diode, DS1588L1	ADX-1405	VHDDS1588L1-1
	Thermister (150K)	AT-1218	VHH154KD-5/-1
	LSI (Display chip), TC43125	AXX-3032	VHiSC43125/-1
	LSI (CPU-1), SC43177	AXX-3033	VHiSC43177/-1
	LSI (CPU-2), SC43178	AXX-3034	VHiSC43178/-1
	IC, TC4011UBP	AMX-4439	VHiTC4011UBP1
	IC, TC4019P	AMX-4440	VHiTC4019P/-1
	IC, TC4066P	AMX-4441	VHiTC4066P/-1
	IC, TC4069P	AMX-4442	VHiTC4069P/-1
	LSI (Ram)	AXX-3035	VHiTC5514P/-1
	Solid resistor 1/8W 1.6Mohm 5%	AN0536EBB	VRC-MT26G165J
	Carbon resistor 1/8W 100 ohm 5%	AN0132EBB	VRD-ST26Y101J
	Carbon resistor 1/8W 22K 5%	AN0311EBB	VRD-ST26Y223J
	Carbon resistor 1/8W 10K 5%	AN0281EBB	VRD-ST26Y103J
	Carbon resistor 1/8W 100K 5%	AN0371EBB	VRD-ST26Y104J
	Carbon resistor 1/8W 1Mohm 5%	AN0445EBB	VRD-ST26Y105J
	Carbon Resistor 1/8W 4.7K 5%	AN0247EBB	VRD-ST26Y472J
	Carbon resistor 1/8W 470K 5%	AN0423EBB	VRD-ST26Y474J

Ref. No.	Description	RS Location	Manufacturer Part Number
	Transistor 2SC458KS	AA2SC458KS	VS2SC458KS/-1
	MOS FET 2SJ40	AMX-4443	VS2SJ40-///-1
	Capacitor (Tantalum) 0.1μF 10V +80/−20%	ACC104ZCTP	RC-SZ1005CCZZ
	Crystal (256 kHz)	AMX-2780	RCRSP1024CCZZ
	Capacitor (Tantalum) 100pF 50V ±10%	ACC101KJCP	VCKYPU1HB101K
	Capacitor (Tantalum) 10000pF 25V ±20%	ACC103MFTM	VCTYPU1EX103M
	Capacitor (Tantalum) 1μF 10V +80/−20%	ACC105ZCTP	RC-SZ1007CCZZ
	Carbon resistor 1/8W 220K 5%	AN0396EBB	VRD-ST2BY224J
	Capacitor (Ceramic) 1000pF 50V ±10%	ACC102KJCP	VCKYPU1HB102K

EXPLODED VIEW(26-3501)



10. PARTS LIST FOR 26-3503

Ref. No.	Description	RS Location	Manufacturer Part Number
1	Bottom cabinet	AZ-5637	GCABA2389CCZZ
2	Special screw (M2 × 8)	AHD-1592	LX-BZ1038CCZZ
3	Rubber foot	AF-0294	GLFGG1012CC77
4	Battery lid	ADB-0356	GFTAB1247CC2Z
5	Screw (M2 × 6)	AHD-1593	XTBSD20P06000
6	Plug with wires	AW-2523	QPLGJ1008CCZZ
7	Connector (9 pin)	AJ-6833	QCNCM1260CC01
8	Screw (M2 × 5)	AHD-1594	XTBSD20P05000
9	Holder for lock plate		LHLDZ1153CCZZ
10	Battery terminal (–)	AHB-9962	QTANZ1266CCZZ
11	Battery terminal (+)	AHB-9963	QTANZ1072CCZZ
12	Decoration panel A	ART-2992	HDECA1775CCZZ
13	Decoration panel B	ART-2993	HDECA1776CCZZ
14	Top cabinet	AZ-5639	GCABB2390CC2Z
	Capacitor (Electrolytic) 10μF 16V +80/–20%	ACC106ZDAP	VCEAAU1CW106Q
	Capacitor (Mylar) 0.0047μF 50V ±10%	ACC472KJMP	VCQYKU1HM472K
	Capacitor (Mylar) 0.047μF 50V ±10%	ACC473KJMP	VCQYKU1HM473K
	Capacitor (Tantal) 0.01μF 25V ±20%	ACC103MFTP	VCTYPU1EX103M
	Capacitor (Tantal) 0.1μF 12V ±20%	ACC104MDTP	VCTYPU1NX104M
	Diode, DS1588L1	ADX-1405	VHDDS1588L1-1
	Relay	AR-8127	VHiNR5711//-1
	IC, TC4069P	AMX-4442	VHiTC4069P/-1
	IC, TC4528BP	AMX-4444	VHiTC4528BP-1
	Carbon resistor 1/8W 10K 5%	AN0281EBB	VRD-ST2BY103J
	Carbon resistor 1/8W 100K 5%	AN0371EBB	VRD-ST2BY104J
	Carbon resistor 1/8W 1Mohm 5%	AN0445EBB	VRD-ST2BY105J
	Carbon resistor 1/8W 18K 5%	AN0303EBB	VRD-ST2BY183J
	Carbon resistor 1/8W 22K 5%	AN0311EBB	VRD-ST2BY223J
	Carbon resistor 1/8W 270 ohm 5%	AN0155EBB	VRD-ST2BY271J
	Carbon resistor 1/8W 470K 5%	AN0423EBB	VRD-ST2BY474J

Ref No.	Description	RS Location	Manufacturer Part Number
	Carbon resistor 1/8W 560K 5%	AN0429EBB	VRD-ST2BY564J
	Carbon resistor 1/4W 33 ohm 5%	AN0087EEB	VRD-ST2EY330J
	Transistor 2SA733	AA2SA733	VS2SA733-//-1
	Transistor 2SC458KS	AA2SC458KS	VS2SC458KS/-1

EXPLODED VIEW(26-3503)