

# PORTATONE PSR - 740/PSR - 640 SERVICE MANUAL



PSR-740

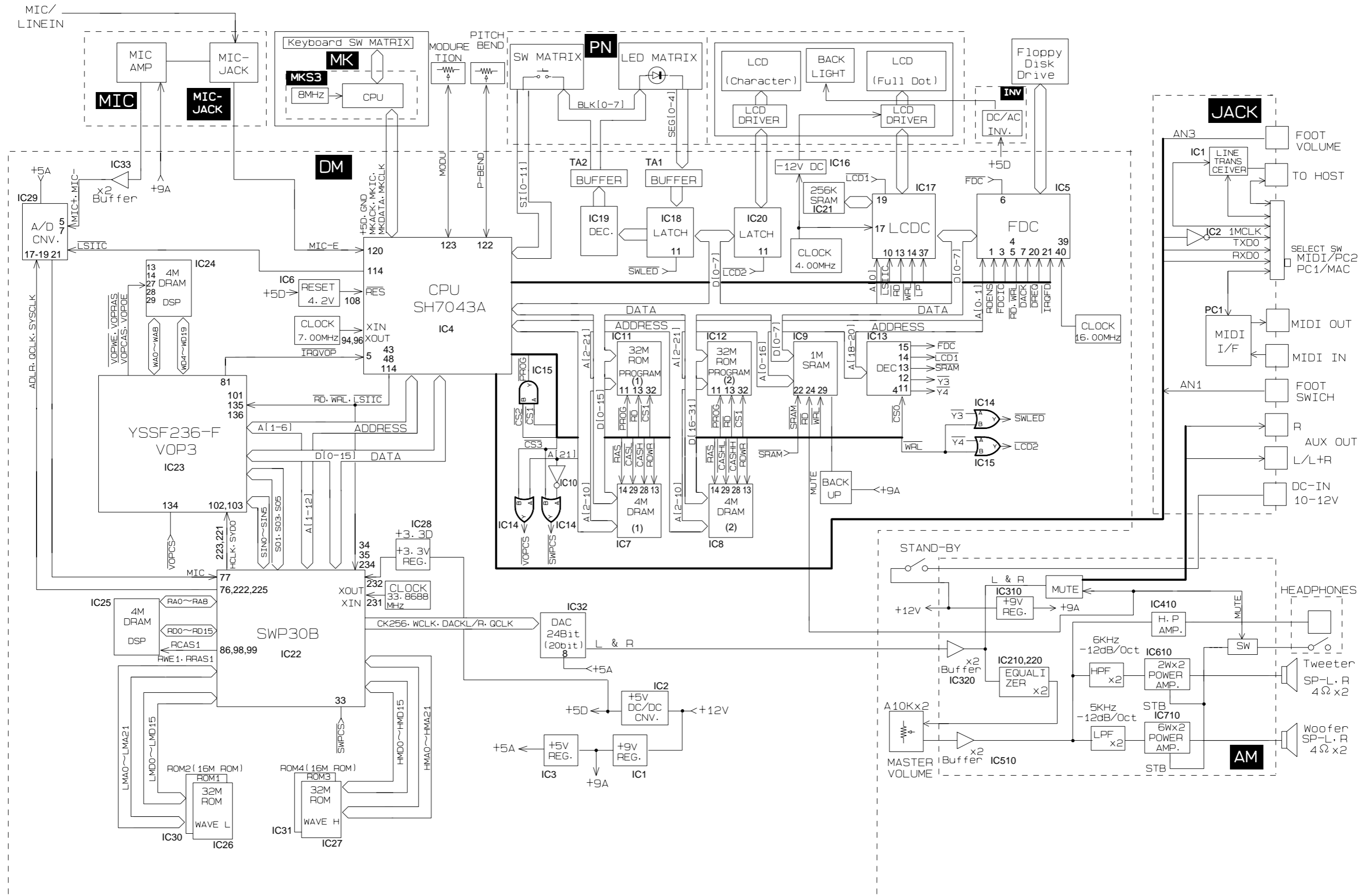


PSR-640

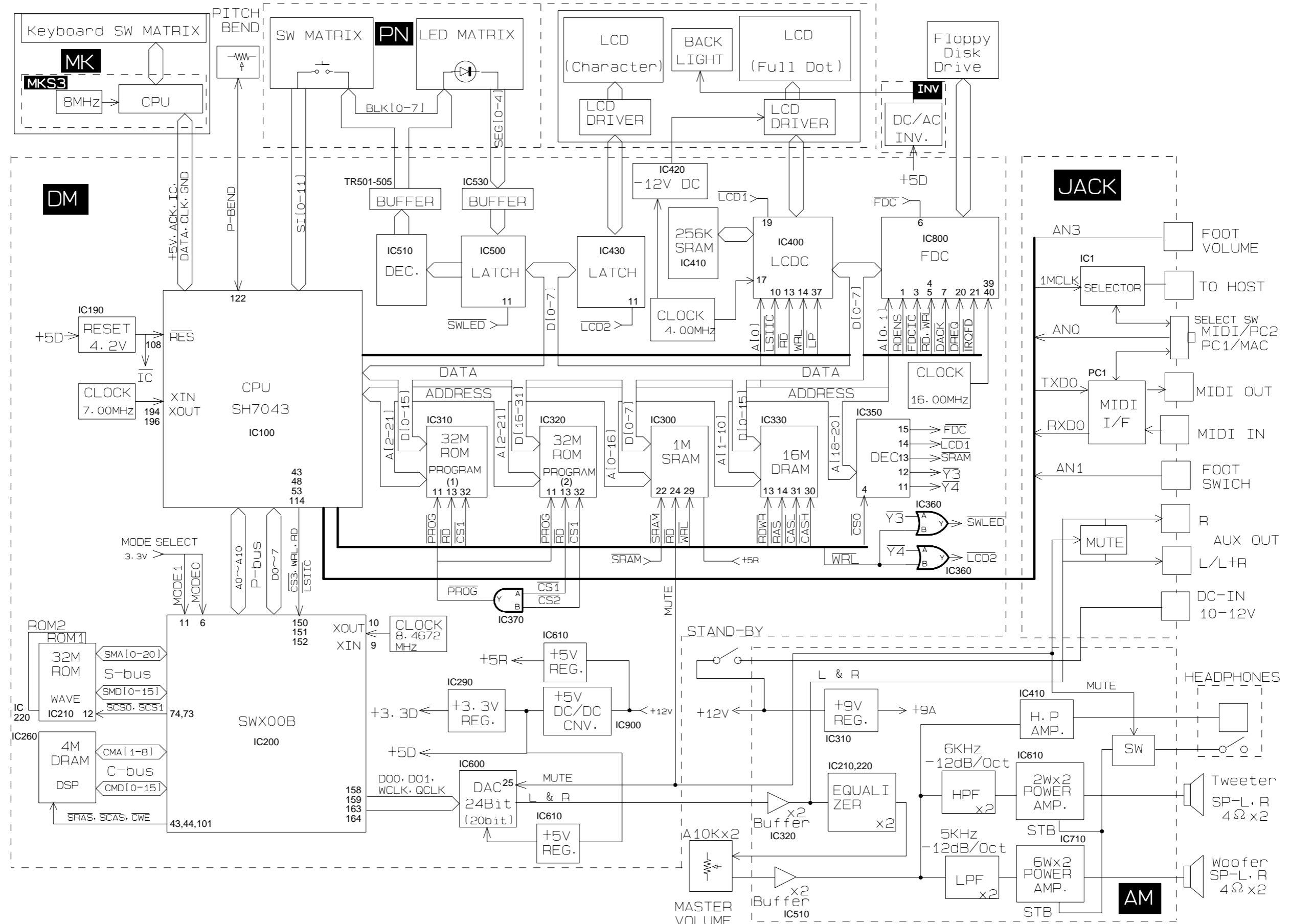
## ■ CONTENTS

SPECIFICATIONS .....	3/4
PANEL LAYOUT .....	5
PSR-740 BLOCK DIAGRAM .....	6
PSR-640 BLOCK DIAGRAM .....	7
CIRCUIT BOARD LAYOUT .....	8
DISASSEMBLY PROCEDURE .....	10
LSI PIN DESCRIPTION .....	14
IC BLOCK DIAGRAM .....	19
CIRCUIT BOARDS .....	20
TEST PROGRAM .....	25/27
DATA INITIALIZATION .....	29
ALERT MESSAGE LIST .....	30/32
MIDI DATA FORMAT .....	34
PSR-740 MIDI IMPLEMENTATION CHART .....	49
PSR-640 MIDI IMPLEMENTATION CHART .....	50
PARTS LIST	
OVERALL CIRCUIT DIAGRAM	

**PSR-740 BLOCK DIAGRAM**



**PSR-640 BLOCK DIAGRAM**



# LSI PIN DESCRIPTION

## ● SH-7043A (XW485100) CPU

## SH-7043 (XW180100) CPU

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	/WRHH/PA23	O	HH write/Port A	73	D15	I/O	Data bus	
2	DACK0/PE14	O	DMA transfer strobe/Port E	74	D14	I/O		
3	/WRHL/PA22	O	HL write/Port A	75	D13	I/O		
4	/CASHH/PA21	I/O	HH Column address strobe/Port A	76	D12	I/O	Power supply	
5	DACK1/PE15	O	DMA transfer strobe/Port E	77	VCC			
6	VSS		Ground	78	D11	I/O	Data bus	
7	A0	O	Address bus	79	VSS		Ground	
8	A1	O						
9	A2	O						
10	A3	O						
11	A4	O						
12	VCC		Power supply	84	D6	I/O	Data bus	
13	A5	O	Address bus	85	VCC			Power supply
14	VSS		Ground	86	D5	I/O	Data bus	
15	A6	O	Address bus	87	VSS		Ground	
16	A7	O						
17	A8	O						
18	A9	O						
19	A10	O						
20	A11	O						
21	A12	O						
22	A13	O						
23	A14	O						
24	A15	O	Power supply	98	NMI	-	Non-maskable interrupt	
25	A16	O	Address bus	99	VCC/FW		Power supply	
26	VCC		Power supply	100	PA16	I/O	Port A	
27	A17	O	Address bus	101	PA17	I/O	Port A	
28	VSS		Ground	102	MD1		Mode select	
29	/CASHL/PA20	I/O	HL Column address strobe/Port A	103	MD0		Mode select	
30	PA19	I/O	Port A	104	PLL VCC		PLL Power supply	
31	/RAS/PB2	O	Row address strobe/Port B	105	PLL CAP		PLL capacitor	
32	/CASL/PB3	O	Column address strobe (low) /Port B	106	PLL VSS		PLL Ground	
33	PA18	I/O	Port A	107	CK/PA15	I/O	Clock/Port A	
34	/CASH/PB4	O	Column address strobe (high) /Port B	108	/RES		Reset	
35	VSS		Ground	109	DREQ0/PE0	I/O	DMA transfer request/Port E	
36	RDWR/PB5	O	DRAM read/write /Port B	110	TIOC0B/PE1	I/O	MTU input capture/output compare (ch 0)/Port E	
37	A18	O	Address bus	111	/DREQ1/PE2	I/O	DMA transfer request/Port E	
38	A19	O						
39	A20	O	Address bus	112	VCC		Power supply	
40	VCC		Power supply	113	PE3	I/O	Port E	
41	A21	O	Address bus	114	PE4	I/O		
42	VSS		Ground	115	PE5	I/O		
43	/RD	O	Read	116	PE6	I/O		
44	/WDTOVF	O	Watch dog timer overflow	117	VSS		Ground	
45	D31	I/O	Data bus	118	AN0 /PF0		Analog input/Port F	
46	D30	I/O	Data bus	119	AN1 /PF1			
47	/WRH	O	High write	120	AN2 /PF2			
48	/WRL	O	Low write	121	AN3 /PF3			
49	/CS1	O	Chip select	122	AN4 /PF4			
50	/CS0	O	Chip select	123	AN5 /PF5			
51	/IRQ3/PA9/TCLKD	I/O	Interrupt request/Port A/clock	124	AVSS			Analog ground
52	/IRQ2/PA8/TCKLC	I/O	Interrupt request/Port A/clock	125	AN6 /PF6			Analog input /Port F
53	/CS3	O	Chip select	126	AN7 /PF7			Analog input /Port F
54	/CS2	O	Chip select	127	AVREF			Analog reference voltage
55	VSS		Ground	128	AVCC		Analog power supply	
56	D29	I/O	Data bus	129	VSS		Ground	
57	D28	I/O						
58	D27	I/O						
59	D26	I/O						
60	D25	I/O	Ground	130	RxD0		Receive data	
61	VSS		Ground	131	TxD0	O	Transmit data	
62	D24	I/O	Data bus	132	/IRQ0/SCK0		Interrupt request/Serial clock	
63	VCC		Power supply	133	RxD1		Receive data	
64	D23	I/O	Data bus	134	TxD1/PA4	I/O	SCI/Port A	
65	D22	I/O						
66	D21	I/O						
67	D20	I/O						
68	D19	I/O						
69	D18	I/O						
70	D17	I/O						
71	VSS			Ground	135	VCC		Power supply
72	D16	I/O	Data bus	136	/IRQ1/SCK1		Interrupt request/Serial clock	
				137	PE7	I/O	Port E	
				138	PE8	I/O		
				139	PE9	I/O		
				140	PE10	I/O	Ground	
				141	VSS			
				142	PE11	I/O		
				143	PE12	I/O		
				144	PE13	I/O	Port E	

## ● HG73C205AFD (XU947C00) SWX00B TONE GENERATOR

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	ICN	I	Initial clear	85	CMA3	O	Program address bus
2	RFCLKI	I	PLL Clock	86	CMA8	O	Program address bus
3	TM2	I	PLL Control	87	CMA2	O	Program address bus
4	AVDD_PLL		Power supply	88	CRD	O	read signal
5	AVSS_PLL		Ground	89	CMA1	O	Program address bus
6	MODE0	I	SWX dual mode	90	CUB	O	high byte effective signal
7	VCC7		Power supply	91	VCC91		Power supply
8	GND8		Ground	92	GHND92		Ground
9	XIN	I	crystal oscillator	93	CS1	O	CS signal
10	XOUT	O	crystal oscillator	94	CMA0	O	Program address bus
11	MODE1	I	SWX separate mode	95	CLB	O	low byte effective signal
12	TEST0	I	TEST pin	96	CMA12	O	} Program address bus
13	TESTON	I	TEST pin	97	CMA11	O	
14	AN0-P40	I	A/D converter	98	CMA10	O	
15	AN1-P41	I	A/D converter	99	CMA9	O	
16	AN2-P42	I	A/D converter	100	GND100		
17	AN3-P43	I	A/D converter	101	CWE	O	write signal
18	AVDD_AN		Power supply	102	CMA16	O	Program address bus
19	AVSS_AN		Ground	103	CMA15	O	Program address bus
20	TXD0	O	for MIDI or TO-HOST	104	CMA14	O	Program address bus
21	TXD1	O	for MIDI	105	CMA13	O	Program address bus
22	EXCLK	I	Crystal oscillator	106	CMD8	I/O	Program memory Data bus
23	SMD11	I/O	Wave memory data bus	107	CMD7	I/O	Program memory Data bus
24	SMD4	I/O	Wave memory data bus	108	CMD9	I/O	Program memory Data bus
25	SMD3	I/O	Wave memory data bus	109	CMD6	I/O	Program memory Data bus
26	SMD12	I/O	Wave memory data bus	110	CMD10	I/O	Program memory Data bus
27	SMD10	I/O	Wave memory data bus	111	CMD5	I/O	Program memory Data bus
28	SMD5	I/O	Wave memory data bus	112	CMD11	I/O	Program memory Data bus
29	SMD2	I/O	Wave memory data bus	113	CMD4	I/O	Program memory Data bus
30	SMD13	I/O	Wave memory data bus	114	CMD12	I/O	Program memory Data bus
31	SMD9	I/O	Wave memory data bus	115	CMD3	I/O	Program memory Data bus
32	SMD6	I/O	Wave memory data bus	116	CMD13	I/O	Program memory Data bus
33	SMD1	I/O	Wave memory data bus	117	CMD2	I/O	Program memory Data bus
34	SMD14	I/O	Wave memory data bus	118	CMD14	I/O	Program memory Data bus
35	VCC35		Power supply	119	VCC119		Power supply
36	GND36		Ground	120	GND115		Ground
37	SMD8	I/O	Wave memory data bus	121	CMD1	I/O	Program memory Data bus
38	SMD7	I/O	Wave memory data bus	122	CMD15	I/O	Program memory Data bus
39	SMD0	I/O	Wave memory data bus	123	CMD0	I/O	Program memory Data bus
40	SMD15	I/O	Wave memory data bus	124	CMA21	O	Program address bus
41	SOE	O	read signal	125	PDT15	I/O	} SWX access data bus
42	SWE	O	write signal	126	PDT14	I/O	
43	SRAS	O	RAS signal	127	PDT13	I/O	
44	SCAS	O	CAS signal	128	PDT12	I/O	
45	REFRESH	O	REFRESH signal	129	PDT11	I/O	
46	CS0	O	CS signal	130	PDT10	I/O	
47	SMA0	O	Memory address bus	131	PDT9	I/O	} Power supply
48	SMA16	O	Memory address bus	132	PDT8	I/O	
49	VCC49		Power supply	133	VCC133		Power supply
50	GND50		Ground	134	GND134		Ground
51	SMA1	O	Memory address bus	135	PDT7	I/O	} SWX access data bus
52	SMA15	O	Memory address bus	136	PDT6	I/O	
53	SMA2	O	Memory address bus	137	PDT5	I/O	
54	SMA14	O	Memory address bus	138	PDT4	I/O	
55	SMA3	O	Memory address bus	139	PDT3	I/O	
56	SMA13	O	Memory address bus	140	PDT2	I/O	
57	SMA4	O	Memory address bus	141	PDT1	I/O	
58	SMA12	O	Memory address bus	142	PDT0	I/O	
59	SMA5	O	Memory address bus	143	VCA143		Power supply
60	GND60		Ground	144	GND144		Ground
61	VCC61		Power supply	145	PAD2	I	} SWX access address bus
62	SMA11	O	Memory address bus	146	PAD1	I	
63	SMA6	O	Memory address bus	147	PAD0	I	
64	SMA10	O	Memory address bus	148	VCC148		Power supply
65	SMA7	O	Memory address bus	149	GND149		Ground
66	SMA9	O	Memory address bus	150	PCS	I	Chip select
67	SMA17	O	Memory address bus	151	PWR	I	write enable
68	SMA8	O	Memory address bus	152	PRD	I	read enable
69	SMA18	O	Memory address bus	153	RXD0	I	for Midi or TO-HOST
70	SMA19	O	Memory address bus	154	RXD1	I	for Midi or Key scan
71	SMA20	O	Memory address bus	155	SCLKI	I	EXT Clock
72	SMA21	O	Memory address bus	156	ADIN	O	A/D converter
73	SMA22	O	Memory address bus	157	ADLR	O	A/D converter LR clock
74	SMA23	O	Memory address bus	158	DO0	O	DAC
75	CMA20	O	Program address bus	159	DO1	O	DAC
76	CMA19	O	Program address bus	160	SYSCCLK	O	1/2 clock
77	VCC77		Power supply	161	VCC161		Power supply
78	GND78		Ground	162	GND162		Ground
79	CMA18	O	Program address bus	163	WCLK	O	for DAC LR clock
80	CMA17	O	Program address bus	164	QCLK	O	1/12 clock
81	CMA5	O	Program address bus	165	BCLK	O	IIS-DAC clock
82	CMA6	O	Program address bus	166	SYI	I	Synch signal
83	CMA4	O	Program address bus	167	IRQ0	I	Interrupt request
84	CMA7	O	Program address bus	168	NMI	I	Interrupt request

● TC203C760HF-002 (XS725A00)  
SWP30B (AWM Tone Generator coped with MEG) Standard Wave Processor

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	VSS		(Ground)	121	VSS		(Ground)	
2	CA0	I	Address bus internal register	122	HMD0	I/O	Wave memory data bus (Upper data memory)	
3	CA1	I						
4	CA2	I						
5	CA3	I						
6	CA4	I						
7	CA5	I						
8	CA6	I						
9	CA7	I						
10	CA8	I						
11	CA9	I						
12	CA10	I						
13	CA11	I						
14	VSS		(Ground)	123	HMD1	I/O		
15	CD0	I/O	Data bus of internal register	124	HMD2	I/O		
16	CD1	I/O						
17	CD2	I/O						
18	CD3	I/O						
19	CD4	I/O						
20	CD5	I/O						
21	CD6	I/O						
22	CD7	I/O						
23	CD8	I/O						
24	CD9	I/O						
25	CD10	I/O						
26	CD11	I/O						
27	CD12	I/O						
28	CD13	I/O						
29	CD14	I/O						
30	VDD		(Power supply)	125	HMD3	I/O		
31	VSS		(Ground)	126	HMD4	I/O		
32	CD15	I/O	Chip select	127	HMD5	I/O		
33	/CS	I		Write strobe	128	HMD6	I/O	
34	/WR	I		Read strobe	129	HMD7	I/O	
35	/RD	I			130	HMD8	I/O	
36	VDDSD		(Power supply)	131	HMD9	I/O		
37	SYSH0	O	NSYS/LNSYS upper 16 bits	132	HMD10	I/O		
38	SYSH1	O						
39	SYSH2	O						
40	SYSH3	O						
41	SYSH4	O						
42	SYSH5	O						
43	SYSH6	O						
44	SYSH7	O						
45	KONO0	O		Key on data				
46	KONO1	O						
47	KONO2	O						
48	KONO3	O						
49	VSS		(Ground)	133	HMD11	I/O		
50	SYSL0	I/O	NSYS input/LNSYS output lower 8 bits	134	HMD12	I/O		
51	SYSL1	I/O						
52	SYSL2	I/O						
53	SYSL3	I/O						
54	SYSL4	I/O						
55	SYSL5	I/O						
56	SYSL6	I/O						
57	SYSL7	I/O						
58	KONI0	I	Key on data					
59	KONI1	I						
60	VDDSD			(Power supply)				
61	VSS			(Ground)				
62	KONI2	I	DAC output					
63	KONI3	I						
64	DAC0	O						
65	DAC1	O	DAC0/DAC1 word clock	135	HMD13	I/O		
66	WCLK	O	MEL wave data output	136	HMD14	I/O		
67	MELO0	O						
68	MELO1	O						
69	MELO2	O						
70	MELO3	O						
71	MELO4	O						
72	MELO5	O						
73	MELO6	O						
74	MELO7	O						
75	VDDSD		(Power supply)	137	HMD15	I/O		
76	ADLR	O	ADC word clock					
77	MELI0	I						
78	MELI1	I						
79	MELI2	I	MEL wave data input					
80	MELI3	I						
81	MELI4	I						
82	MELI5	I						
83	MELI6	I						
84	MELI7	I						
85	VSS			(Ground)				
86	/RCAS	O		DRAM column address strobe				
87	RA8	O						
88	RA7	O						
89	RA6	O						
90	VDD		(Power supply)					
91	VSS		(Ground)					
92	RA5	O	DRAM address bus					
93	RA4	O						
94	RA3	O						
95	RA2	O						
96	RA1	O						
97	RA0	O						
98	/RRAS	O						
99	/RWE	O						
100	VSS		(Ground)	138	VSS		(Ground)	
101	RD7	I/O	DRAM data bus	139	HMA0	O		
102	RD6	I/O						
103	RD5	I/O						
104	RD4	I/O						
105	RD3	I/O						
106	RD2	I/O						
107	RD1	I/O						
108	RD0	I/O						
109	VSS			(Ground)				
110	RD17	I/O						
111	RD16	I/O						
112	RD15	I/O						
113	RD14	I/O						
114	RD13	I/O						
115	RD12	I/O						
116	RD11	I/O						
117	RD10	I/O						
118	RD9	I/O						
119	RD8	I/O						
120	VDDSD		(Power supply)	140	HMA1	O		
				141	HMA2	O		
				142	HMA3	O		
				143	HMA4	O		
				144	HMA5	O		
				145	HMA6	O		
				146	HMA7	O		
				147	HMA8	O		
				148	HMA9	O		
				149	HMA10	O		
				150	VDD		(Power supply)	
				151	VSS		(Ground)	
				152	HMA11	O	Wave memory address bus (Upper 16 bits)	
				153	HMA12	O		
				154	HMA13	O		
				155	HMA14	O		
				156	HMA15	O		
				157	HMA16	O		
				158	HMA17	O		
				159	HMA18	O		
				160	HMA19	O		
				161	HMA20	O		
				162	HMA21	O		
				163	HMA22	O		
				164	HMA23	O		
				165	HMA24	O		
				166	VSS		(Ground)	
				167	/MRAS	O	RAS when DRAM(s) is connected to wave memory	
				168	/MCAS	O		CAS when DRAM(s) is connected to wave memory
				169	/MOE	O		
				170	/MWE	O	Wave memory write enable	
				171	VSS		(Ground)	
				172	LMD0	I/O	Wave memory data bus (Lower data memory)	
				173	LMD1	I/O		
				174	LMD2	I/O		
				175	LMD3	I/O		
				176	LMD4	I/O		
				177	LMD5	I/O		
				178	LMD6	I/O		
				179	LMD7	I/O		
				180	VDDSD		(Power supply)	
				181	VSS		(Ground)	
				182	LMD8	I/O	Wave memory address bus (Lower data memory)	
				183	LMD9	I/O		
				184	LMD10	I/O		
				185	LMD11	I/O		
				186	LMD12	I/O		
				187	LMD13	I/O		
				188	LMD14	I/O		
				189	LMD15	I/O		
				190	VSS		(Ground)	
				191	LMA0	O	DRAM row address strobe	
				192	LMA1	O		
				193	LMA2	O		
				194	LMA3	O		
				195	LMA4	O		
				196	LMA5	O		
				197	LMA6	O		
				198	LMA7	O		
				199	LMA8	O		
				200	LMA9	O		
				201	LMA10	O		
				202	LMA11	O		
				203	VSS		(Ground)	
				204	LMA12	O	DRAM row address strobe	
				205	LMA13	O		
				206	LMA14	O		
				207	LMA15	O		
				208	LMA16	O		
				209	LMA17	O		
				210	VDD			(Power supply)
				211	VSS			(Ground)
				212	LMA18	O	DRAM row address strobe	
				213	LMA19	O		
				214	LMA20	O		
				215	LMA21	O		
				216	LMA22	O		
				217	LMA23	O		
				218	LMA24	O		
				219	VSS			(Ground)
				220	SYO	O	Sync. signal for master clock	
				221	SYOD	O		Sync. signal for HCLK/QCLK
				222	QCLK	O		
				223	HCLK	O	1/6 master clock (128 Fs)	
				224	CK256	O	1/3 master clock (256 Fs)	
				225	SYSCCLK	O	1/2 master clock (384 Fs)	
				226	VDDSD		(Power supply)	
				227	SYI	I	Sync. clock	
				228	MCLKI	I		Master clock input
				229	MCLKO	O	Master clock output	
				230	VDD		(Power supply)	
				231	XIN	I	Crystal osc. input	
				232	XOUT	O	Crystal osc. output	
				233	VSS		(Ground)	
				234	/IC	I	Initial clear	
				235	CHIP2	I		2 chips mode enable
				236	SLAVE	I		Master/Slave select when 2 chips mode
				237	/TESTO	I		
				238	/ACI	I	Test pin	
				239	DCTEST	I		
				240	VDDSD			(Power supply)

● YSS236-F (XT013A00) VOP3

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	VSS		Power supply	81	SO7	O	Serial output	
2	WA17	O		82	SO6	O		
3	WA16	O	83	SO5	O			
4	WA15	O	External memory address bus	84	VDD		Ground	
5	WA14	O		85	VSS			Power supply
6	WA13	O		86	SO4	O		
7	WA12	O		87	SO3	O	Serial output	
8	WA11	O		88	SO2	O		
9	WA10	O		89	SO1	O		
10	VDD		Ground	90	SO0	O	Data enable for DAC SWP00 format key on output	
11	VSS			91	WDCK	O		
12	WA09	O	External memory address bus	92	SWPKON	O		EG interrupt
13	WA08	O		93	IRQN	O		
14	WA07	O		94	VDD		Ground	
15	WA06	O		95	VSS			Power supply
16	WA05	O		96	XTAL_I	I	Quartz crystal terminal	
17	WA04	O		97	XTAL_O	O	Quartz crystal terminal	
18	WA03	O	Ground	98	MCLK	O	Oscillate clock output	
19	WA02	O		99	VDD			
20	VDD		Ground	100	VSS		Power supply	
21	VSS			101	MICN	I		Initial clear
22	WA01	O	External memory address bus	102	CLKIN	I	Master clock input	
23	WA00	O		103	SYWIN	I	Sync.signal input	
24	WEN	O	External memory control (WEN)	104	SYW	O	Sync.signal output	
25	OEN	O		External memory control (OEN)	105	SYWD	O	Sync.signal output
26	RASN	O	External memory control (RASN)		106	VDD		Ground
27	CASN	O		External memory control (CASN)	107	VSS		
28	CEN	O	External memory control (CEN)		108	CLKO	O	For test (512 fs output)
29	VDD			109	WCLK	O	2 times sync.clock output (256 fs)	
30	VSS		Ground	110	HCLK	O	4 times sync.clock output (128 fs)	
31	WD19	I/O		Power supply	111	QCLK		O
32	WD18	I/O	External memory data bus		112	TSTCI	I	PLL test input
33	WD17	I/O		Ground	113	VDD		
34	WD16	I/O			Power supply	114	VSS	
35	WD15	I/O		Ground		115	(NC)	
36	WD14	I/O			Power supply	116	VDD(PLL)	O
37	VDD			Ground		117	CPO	O
38	VSS		118		CPIN	I	PLL control input	
39	WD13	I/O	External memory data bus	119	REF	I		PLL control input
40	WD12	I/O		Ground	120	VSS(PLL)		
41	WD11	I/O			Power supply	121	(NC)	
42	WD10	I/O		Ground		122	VDD	
43	WD09	I/O			Power supply	123	VSS	
44	WD08	I/O		Ground		124	TSTCS	I
45	WD07	I/O	Power supply		125	CA6	I	
46	VDD			Ground	126	CA5	I	CPU address bus
47	VSS		Power supply		127	CA4	I	
48	WD06	I/O		External memory data bus	128	CA3	I	Ground
49	WD05	I/O	Power supply		129	CA2	I	
50	WD04	I/O			Ground	130	VDD	
51	WD03	I/O	Power supply			131	VSS	
52	WD02	I/O			Ground	132	CA1	I
53	WD01	I/O	Power supply			133	CA0	I
54	WD00	I/O		Ground	134	CSN	I	Chip select
55	VDD		Power supply		135	RDN	I	
56	VSS			Ground	136	WRN	I	Register write
57	TST2	O	Test output		137	BTYP		
58	TST1	O		Ground	138	VDD		Power supply
59	TST0	O	Memory select		139	VSS		
60	MS	I		LR clock for ADC	140	CD15	I/O	CPU data bus
61	LRCLK	O	Serial input		141	CD14	I/O	
62	SI7	I		Ground	142	CD13	I/O	CPU data bus
63	SI6	I	Power supply		143	CD12	I/O	
64	VDD			Ground	144	CD11	I/O	CPU data bus
65	VSS		Power supply		145	VDD		
66	SI5	I		Serial input	146	VSS		Ground
67	SI4	I	Power supply		147	CD10	I/O	
68	SI3	I			Ground	148	CD09	I/O
69	SI2	I	Power supply			149	CD08	I/O
70	SI1	I			Ground	150	CD07	I/O
71	SI0	I	Power supply			151	CD06	I/O
72	DB1	I		Output bit type select for DAC	152	CD05	I/O	CPU data bus
73	DB0	I	Ground		153	VDD		
74	VDD			Power supply	154	VSS		Power supply
75	VSS		Output mode select for DAC		155	CD04	I/O	
76	ODFM	I		Ground	156	CD03	I/O	CPU data bus
77	OFS3	I	Power supply		157	CD02	I/O	
78	OFS2	I		Ground	158	CD01	I/O	CPU data bus
79	OFS1	I	Serial output format select		159	CD00	I/O	
80	OFS0	I		Power supply	160	VDD		Ground





● **HD63266F** (X1939A00) **FDC** (Floppy Disk Controller)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	8"/5"	I	Data transmission speed	33	/TRKO	I	Track 00 signal	
2	XTALSET	I	Clock select	34	/INDEX	I	Index signal	
3	/RESET	I	Rest	35	/RDATA	I	Read data input from FDD	
4	E//RD	I	Enable/Read	36	XTAL2	I	} Clock	
5	RW//WR	I	Read/write/Write	37	EXTAL2	I		
6	/CS	I	Chip select	38	NC	I	} Clock	
7	/DACK	I	DMA acknowledge	39	XTAL1	I		
8	RS0	I	} Register select	40	EXTAL1	I	} Ground	
9	RS1	I						
10	VSS1	I	} Ground	41	VSS4	I	} Ground	
11	VSS2	I						
12	D0	I/O	} Data bus	42	VSS5	I	} Power supply	
13	D1	I/O						
14	D2	I/O						
15	D3	I/O						
16	D4	I/O						
17	D5	I/O						
18	D6	I/O						
19	D7	I/O	} Drive select	43	NC	I	} Ground	
20	/DREQ	O		DMA request	44	VCC2		I
21	/IRQ	O		Interrupt request	45	VCC3		I
22	/DEND	I		Data end	46	VCC4		I
23	VSS3	I	Ground	47	/WGATE	O	Write control	
24	1/2 EX1	I	} Power supply	48	/WDATA	O	Writ data to FDD	
25	VCC1	I		Power supply	49	VSS6	I	Ground
26	NUM1	I		Power supply	50	/STEP	O	Step signal to control head of FDD
27	NUM3	I	} Ground	51	/HDIR	O	Direction	
28	IFS	I		Host interface select	52	/HLOAD	O	Head load
29	SFORM	I		Format data	53	/HSEL	O	Head select
30	/INP	I	Index pulse	54	VSS7	I	} Ground	
31	/READY	I	Ready from FDD	55	/DS0	O		
32	/WPRT	I	Write control signal	56	/DS1	O	} Drive select	
				57	/DS2	O		
				58	/DS3	O	} Ground	
				59	VSS8	I		
				60	/MON0	O	} Motor on	
				61	/MON1	O		
				62	/MON2	O		
				63	/MON3	O	} Ground	
				64	VSS9	I		

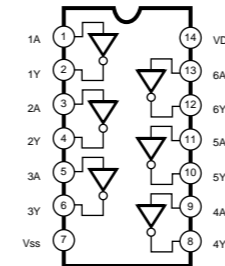
● **SED1335F0B** (XQ595A00) **LCDC** (LCD Controller)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION		
1	VA5	O	} VRAM address bus	31	XD2	O	} Data bus output for 4 bit dot		
2	VA4	O							
3	VA3	O							
4	VA2	O							
5	VA1	O							
6	VA0	O	} VRAM read/write	32	XD1	O	} S driver enable, chain clock		
7	/VWR	O		VRAM read/write	33	XD0		O	
8	/VCE	O		Memory control	34	XECL		O	Data bus shift clock
9	/VRD	-		Not used	35	XSCL		O	Ground
10	/RES	I		Initial clear	36	Vss		-	X driver latch pulse
11	NC	-		Not used	37	LP		O	Frame signal for X/Y driver
12	NC	-		Not used	38	WF		O	Power down signal for displaying off mode
13	/RD	I	Read strobe	39	YDIS	O	Scan start signal		
14	/WR	I	Write strobe	40	YD	O	Scan shift clock		
15	SEL2	I	Bus select	41	YSCL	O	} VRAM data bus		
16	SEL1	I	Bus select	42	VD7	I/O			
17	OSC1	I	Clock	43	VD6	I/O			
18	OSC2	O	Clock	44	VD5	I/O			
19	/CS	I	Chip select	45	VD4	I/O			
20	A0	I	Data mode select	46	VD3	I/O			
21	Vdd	-	Power supply	47	VD2	I/O			
22	D0	I/O	} Data bus	48	VD1	I/O			
23	D1	I/O							
24	D2	I/O							
25	D3	I/O							
26	D4	I/O							
27	D5	I/O							
28	D6	I/O							
29	D7	I/O	} VRAM address bus	49	VD0	I/O			
30	XD3	O		Data bus output for 4 bit dot	50	VA15	O		
				51	VA14	O	} VRAM address bus		
				52	VA13	O			
				53	VA12	O			
				54	VA11	O			
				55	VA10	O			
				56	VA9	O			
				57	VA8	O			
				58	VA7	O			
				59	VA6	O			
				60	NC	-		Not used	

■ **IC BLOCK DIAGRAM**

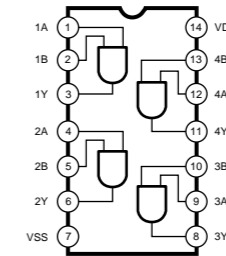
- **SN74HCU04NSR** (XC723A00) **SN74HCU04N** (IG142250)  
Hex Inverter

DM: IC10,16(PSR-740) IC420(PSR-640)  
JACK: IC02



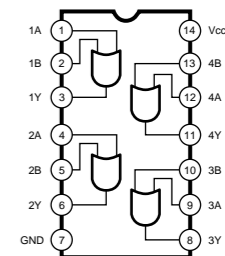
- **SN74HC08NSR** (XD831A00) **HD74LVCO8FP** (XU720A00)  
Quad 2 Input AND

DM: IC15(PSR-740) IC370(PSR-640)



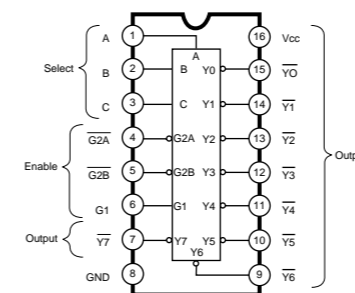
- **TC74HC32AF** (XN241A00)  
Quad 2 Input OR

DM: IC14(PSR-740) IC360(PSR-640)



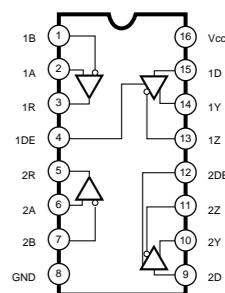
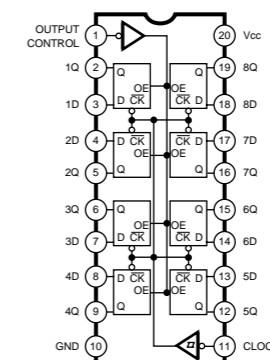
- **TC74HC138AF** (XM970A00) **TC74HC138AFEL** (XW762A00)  
3 to 8 Demultiplexer

DM: IC13,19(PSR-740) IC350,510(PSR-640)



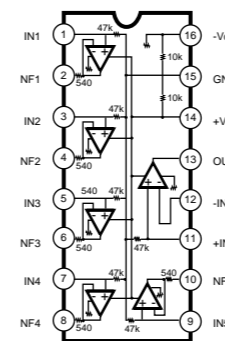
- **SN74HC374ANSR** (XQ042A00) **SN75C1168N** (XU463A00)  
Octal 3-State D-Type Flip-Flop / Line Driver / Receiver

DM: IC18,20(PSR-740) IC430,500(PSR-640)



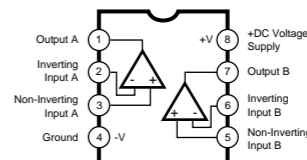
- **M5227P** (XF751A00)  
5-Band Graphic Equalizer

AM: IC210,220



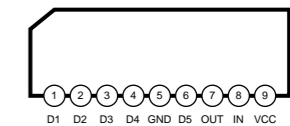
- **M5223AFP** (XV117A00) **M5223AL** (XW373A00)  
Dual Operational Amplifier

DM: IC33(PSR-740)  
MIC: IC100(PSR-740)



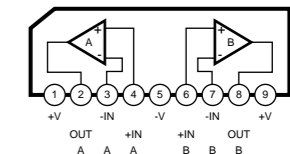
- **LB1443N** (XF483A00)  
LED Driver

MIC: IC001(PSR-740)



- **μPC4570HA** (XB247A00)  
Dual Operational Amplifier

AM: IC320,510



## ■ TEST PROGRAM

### A. PREPARATION

- 1) PA-6 (AC adaptor) is used.
- 2) The volume is usually moved to the use position when no volume change is required.
- 3) Measuring instruments: frequency counter, level meter (with JIS-C filter)  
Note: Connect a stereo plug to the [PHONES] jack at 33 ohms.
- 4) Jigs: foot switch, MIDI cable, floppy disk (2HD & 2DD)

### B. HOW TO ENTER THE TEST PROGRAM

#### AUTOMODE

While pressing the C3#, F3 and G3# keys, turn the [STANDBY/ON] switch on.

#### MANUALMODE

While pressing the C2#, F2 and G2# keys, turn the [STANDBY/ON] switch on.

### C. PROCEEDING THROUGH THE TEST PROGRAM

#### AUTOMODE

When the test program is started, the test is automatically executed.

When confirmation is necessary, the test program stops operating and waits for the instruction. At this time, press the [START/STOP] button; the next test is automatically executed.

#### MANUALMODE

The LCD will display "TEST" when entering the test program.

To select the program number, use the [BACK] and [NEXT] buttons.

To execute the test, press the [START/STOP] button.

To proceed to the next test, press the [START/STOP] button.

### D. TEST PROGRAM LIST

TEST NO.	LCD (initial)	Test Functions and Judgment Criteria
1	001: Version	Displays ROM version ROM (Program, Wave) versions are displayed alternately on the LCD.
2	002: Rom Chk1	Checks the ROM The test results appear on the LCD.
3	003: Ram Chk1	Checks all the RAMs that are connected to the CPU The test results appear on the LCD.
4	004: WaveRomChk1	Checks the WAVE ROMs that are connected to the CPU The test results appear on the LCD.
7	007: FDD Chk	Insert the floppy disks one by one (2DD and 2HD). Checks the floppy disk drive unit
9	009: Eff1Ram Chk	Checks the effect RAM1
10	010: Eff2Ram Chk (PSR-740 only)	Checks the effect RAM2
11	011: TG1 Chk	Outputs the sine wave by changing the channels in sequence from C1 to C6 After auto-scaling is finished, individual keys can be played. (If playing two or more keys simultaneously, the first pressed key has priority to make a sound.)
13	013: Pitch Chk	Connect the frequency counter to the [PHONES] jack. Sets PAN to Center and produces a signal at 440 +/- 0.22 Hz Check that the correct signal is produced.
14	014: Output R	Connect the level meter (with a JIS-C filter) to the [PHONES] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum and check the output level (1 kHz). PHONESL: less than -50.0 dBm PHONESR: -8.0 dBm +/- 2 dB Connect the monaural plugs of the level meter (with a JIS-C filter) to the [AUX OUT] jacks. AUX OUT L: less than -50.0 dBm AUX OUT R: -6.0 dBm +/- 2 dB

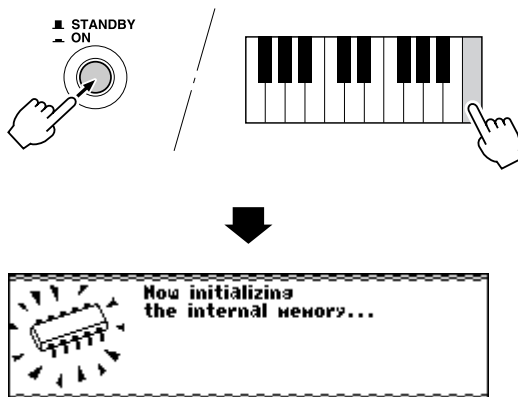
15	015: Output L	Connect the level meter (with a JIS-C filter) to the [PHONES] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum and check the output level (1 kHz). PHONESL: -8.0 dBm +/- 2 dB PHONESR: less than -50.0 dBm Connect the monaural plugs of the level meter (with a JIS-C filter) to the [AUX OUT] jacks. AUX OUTL: -6.0 dBm +/- 2 dB AUX OUTR: less than -50.0 dBm
19	019: D/A Noise	Connect the level meter (with a JIS-C filter) to the [PHONES] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum. Check D/A converter noise. PHONES L/R: Less than -72.0 dBm (PSR-740), Less than -80.0 dBm (PSR-640)
20	020: SW,LED Chk	Check the switches on the panel. Press the switches that are displayed on the LCD. A pre-assigned note is output when pressing the switch. (With some switches, the corresponding LED will light up.) The test results appear on the LCD.
21	021: All LED On	Check that the all LEDs on the panel are on.
22	022: Red LED On	Check that the all red LEDs on the panel are on.
23	023: GreenLED on	Check that the all green LEDs on the panel are on.
28	028: All LCD On	Check that all LCD dots are on. The LCD becomes black.
29	029: All LCD Off	Check that all LCD dots are off. The LCD becomes white.
31	031: Pedal1 Chk	Connect the foot switch (FC-4 or FC-5) to the [FOOT SWITCH] jack. Check that the C3 note is output when pressing and releasing the pedal and the C4 note is output when pressing the pedal again.
33	033: PB Chk	Check that the C3 note is output when rotating the [PITCH BEND] wheel to minimum and the C4 note is output when rotating it to maximum.
34	034: MOD Chk	Check that the C3 note is output when rotating the [MODULATION] wheel to minimum and the C4 note is output when rotating it to maximum.
35	035: EXP Pedal Chk	Connect the expression pedal (FC-7) to the [FOOT VOLUME] jack. Check that the C3 note is output and the LCD displays 0 when pressing the expression pedal to the lowered position and the C4 note is output and the LCD displays 127 when backing it to the raised position.
37	037: Midi Chk	After connecting the [MIDI IN] jack and [MIDI OUT] jack with a MIDI cable, execute the test. Set the [HOST SELECT] switch to MIDI Check that the C4 note is output and that the test results appear on the LCD.
38	038: To Host Chk	For factory test use only
39	039: MIC Chk (PSR-740 only)	Connect a microphone to the [MIC/LINE IN] jack and speak to it. Set the [MIC/LINE] select switch to MIC and set the [INPUT VOLUME] at maximum. Check that the voice is converted to the 1-octave- upper tone without noise.
41	041: Rom Chk2	Checks the ROMs that are connected to the CPU. The test results appear on the LCD.
42	042: Ram Chk2	Checks the RAMs that are connected to the CPU. The test results appear on the LCD.
43	043: WaveRomChk2	Checks the WAVE ROM. The test results appear on the LCD.
46	046: BackUp Chk2	Performs the RAM back-up check. Check that the display reads "NG," then turn off the power switch. Enter the test program and perform the RAM back-up checks, then check again. Check that the LCD displays "OK." Note: Do not turn on the power switch by normal mode while standing by, as the RAM data will be lost.
47	047: Factory Set	All the RAMs are initialized and set to the factory preset data when executing this test. The results appear on the LCD.
48	048: Test Exit	Exit from the test program after executing this test.

\* NOTE: The above tests **Nos. 41-46**, require approximately 25 minutes to conduct.

If the time is not available to perform the tests, proceed the test No.47 by pressing several the [NEXT] button.

## DATA INITIALIZATION

All data can be initialized and restored to the factory preset condition by turning on the power while holding the highest (rightmost) white key on the keyboard. "Now initializing the internal memory..." will appear briefly on the display.



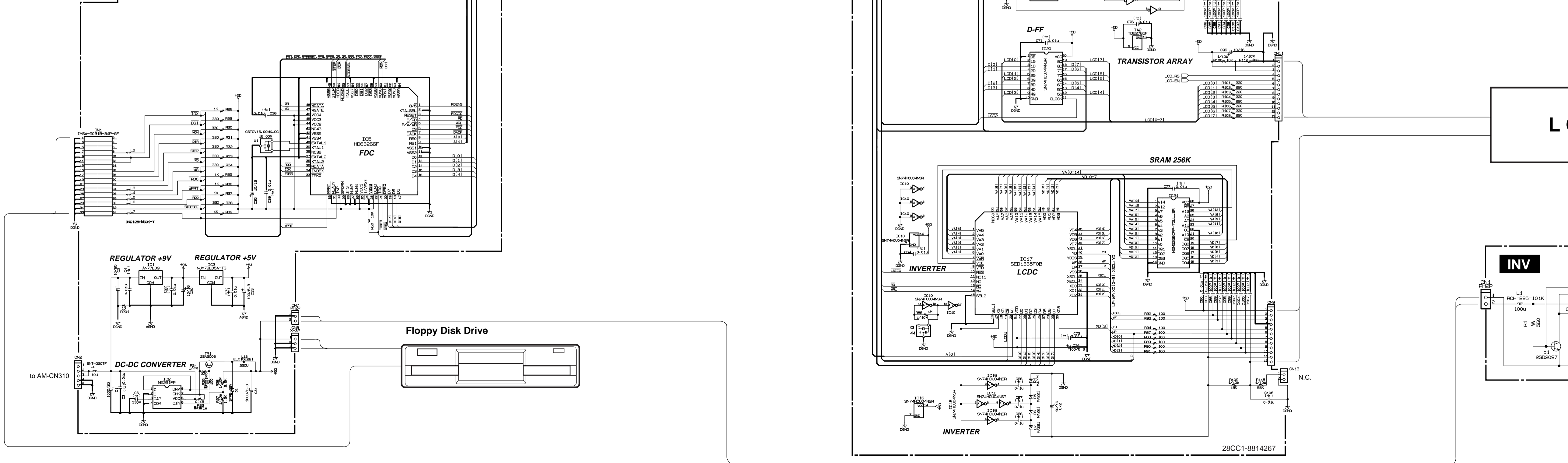
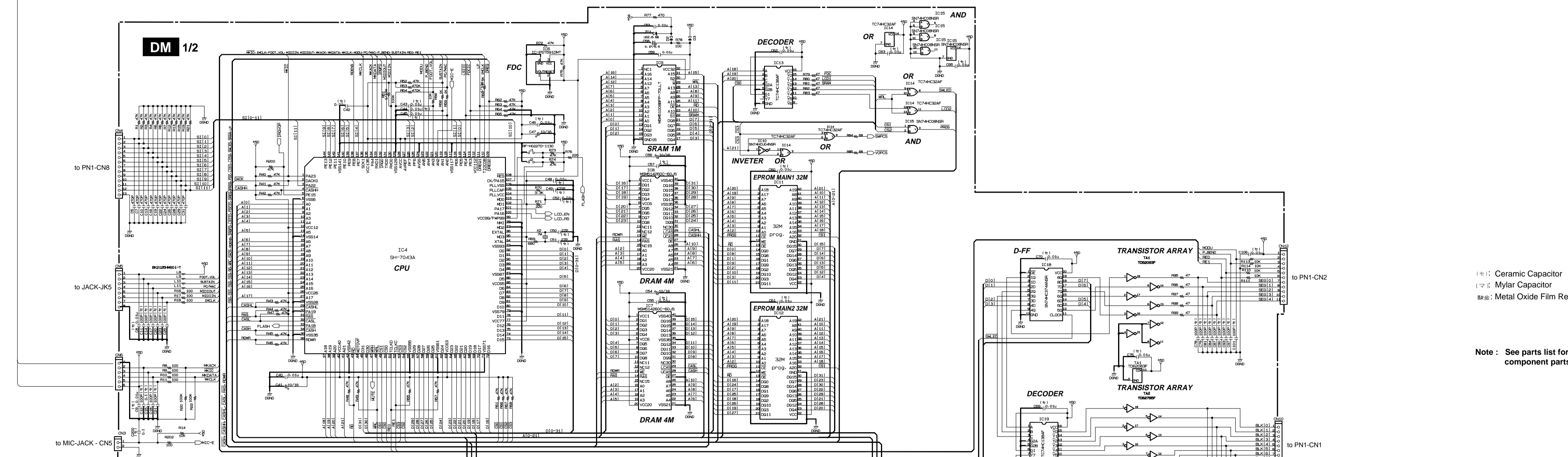
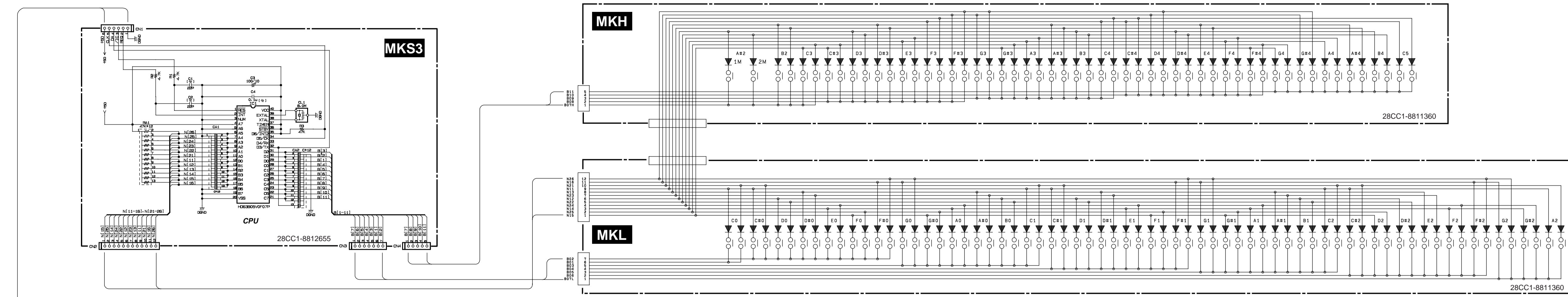
### ⚠ CAUTION

- *All registration and User Style/Pad memory data, plus the other settings listed above, will be erased and/or changed when the data initialization procedure is carried out.*
- *Carrying out the data initialization procedure will usually restore normal operation if the PSR-740/640 freezes or begins to act erratically for any reason.*

## ■ ALERT MESSAGE LIST

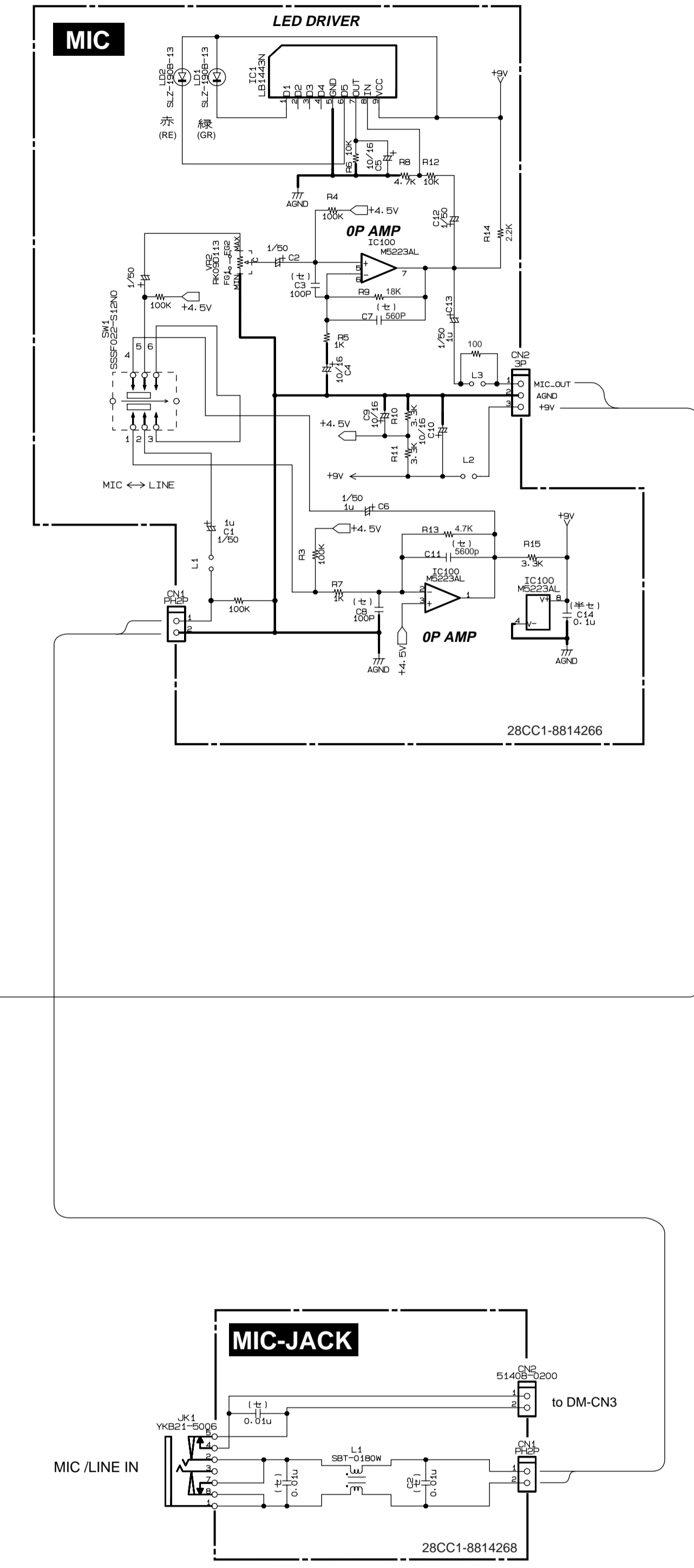
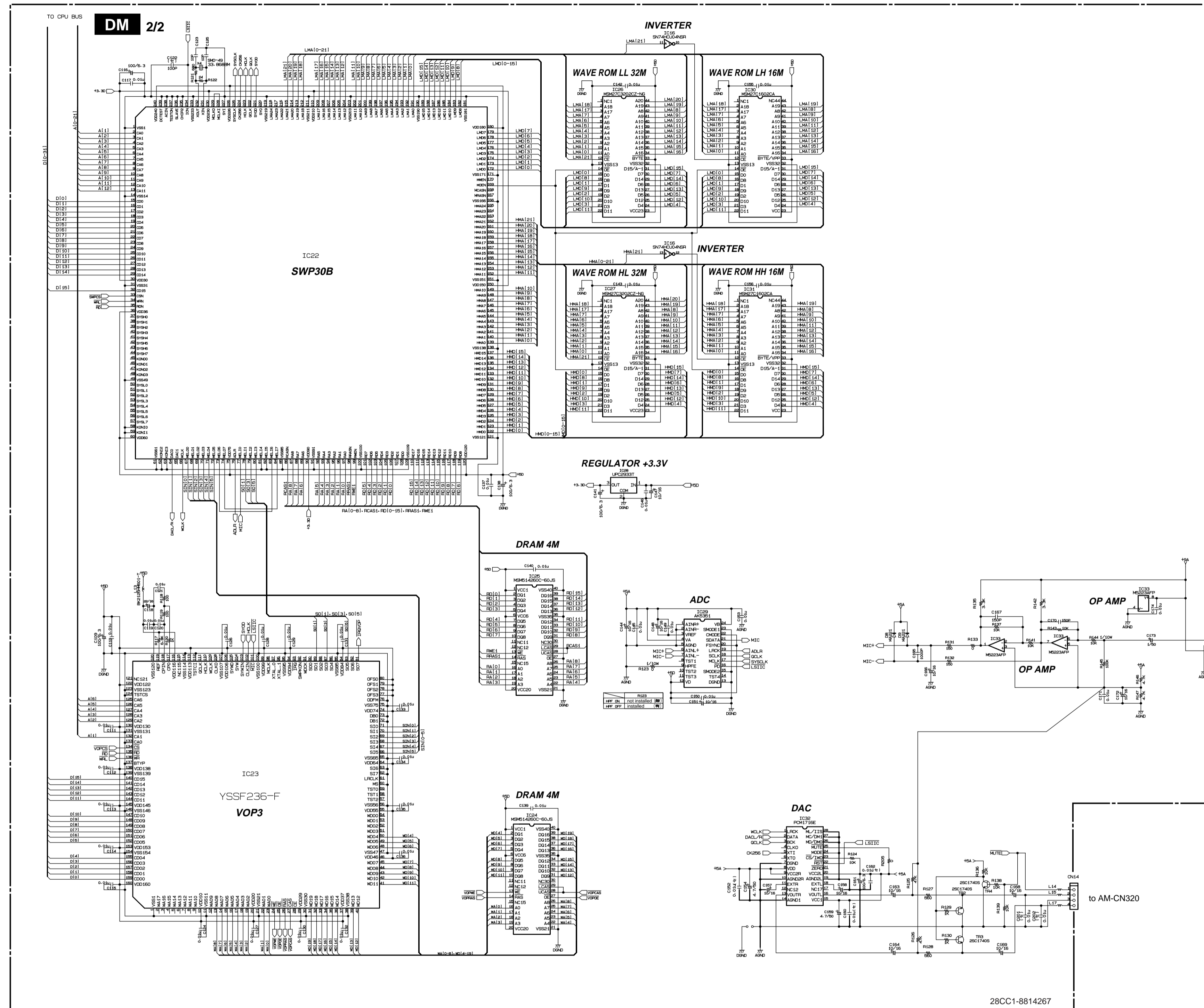
<p><b>No file on disk!</b> <b>Insert another disk.</b></p>	<p>The disk contains no file to be loaded, copied, or be deleted. Insert the disk that contains files to be loaded, copied, or deleted.</p>
<p><b>Unformatted disk!</b></p>	<p>An unformatted disk is inserted.</p>
<p><b>Disk error!</b></p>	<p>An error occurred during execution of a disk operation. Try changing the disk. This message also may appear when executing the Load operation if the internal memory becomes full.</p>
<p><b>Disk write-protected!</b></p>	<p>The floppy disk's write-protect tab is set to ON. Remove the disk, set write-protect to off, re-insert the disk and attempt the operation again.</p>
<p><b>Disk file protected!</b> <b>Can't copy or record this file.</b></p>	<p>The file is a purposely "copy-protected" disk. The Copy function is not possible.</p>
<p><b>No disk!</b> <b>Insert a disk.</b></p>	<p>There is no floppy disk inserted into the disk drive. Insert a disk.</p>
<p><b>Disk removed!</b></p>	<p>An error occurred because the disk was removed during a disk operation. Never remove a disk during a disk operation since this could damage both the disk and the drive.</p>
<p><b>Disk full!</b> <b>Cannot continue.</b></p>	<p>The disk's memory capacity is full and no additional data can be recorded. Delete one or more unneeded songs (using Delete), and attempt the operation again.</p>
<p><b>Wrong disk!</b> <b>Reinsert the proper disk.</b></p>	<p>When using the Copy operation, the inserted disk is different from the source or destination disk. Remove the disk and re-insert the proper Disk.</p>
<p><b>Same name on disk!</b> <b>Change the file name.</b></p>	<p>More than one file has the same name on the disk. Change the name.</p>
<p><b>Cannot record!</b> <b>Maximum of 60 songs can be recorded.</b></p>	<p>Maximum of 60 songs can be recorded. Delete one or more unneeded songs (using Delete), and attempt the song recording again.</p>
<p><b>Memory full!</b> <b>Cannot continue.</b></p>	<p>If the internal memory becomes full during Style/Pad recording, this message will appear on the display and recording will stop.</p>

<b>Memory full! Clear unnecessary data.</b>	This message appears when executing the Quantize or Recording operations (in the Style Recording mode) when the internal memory is full.
<b>Data not found!</b>	This message appears when you attempt to edit, quantize or clear the track which contains no data in the Record mode.
<b>User style full!</b>	This message indicates that recording a new User style cannot be started when all three User styles have recorded data. Make sure to clear at least one of the three User styles before recording a new User style.
<b>Cannot quantize the preset data.</b>	This message appears when you attempt to edit or quantize the track (other than RHYTHM) which contains preset data in the Style Record mode.
<b>Cannot operate during recording.</b>	This function cannot be used during Song/Style/Pad recording.
<b>Cannot set the MIDI function during disk operations, etc.</b>	The MIDI function cannot be set during recording, playback, and disk operations.
<b>Cannot turn harmony ON during Style/Pad recording.</b>	Harmony cannot be turned on during Style/Pad recording.
<b>Cannot turn DSP ON during Style/Pad recording.</b>	DSP cannot be turned on during Style/Pad recording.
<b>Cannot enter the functions during Pad recording.</b>	This message appears to indicate you cannot enter the function when you select Multi Pad function in the Multi Pad Recording mode.
<b>Backup error!</b>	The backup data is faulty. Use the data initialization function.
<b>Now initializing the internal memory...</b>	All data can be initialized and restore to the factory preset condition by turning the STANDBY switch ON while holding the highest (rightmost) white key on the keyboard.
<b>Host is offline!</b>	This message may appear when the Host Select switch is set appropriately and the serial cable is connected to the TO HOST but not to the PC's serial port (or the cable is properly connected to the PC which is currently turned off).



(C) Ceramic Capacitor  
 (M) Mylar Capacitor  
 (R) Metal Oxide Film Resistor

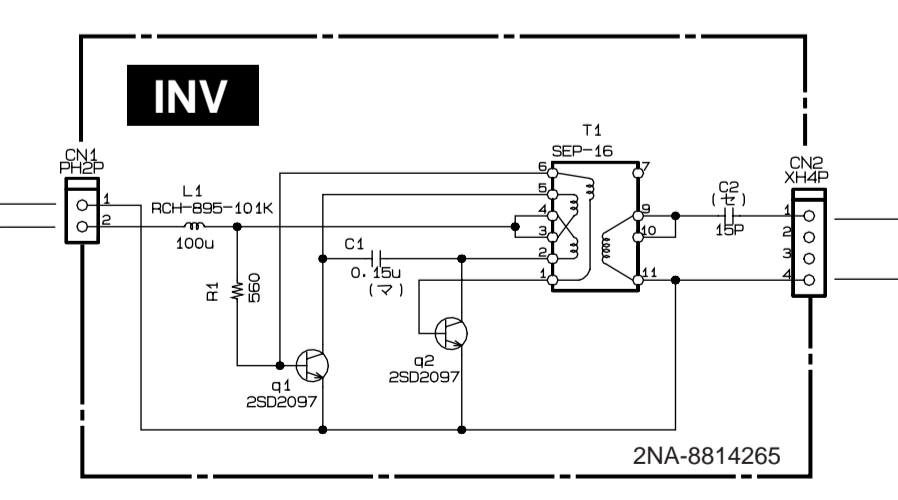
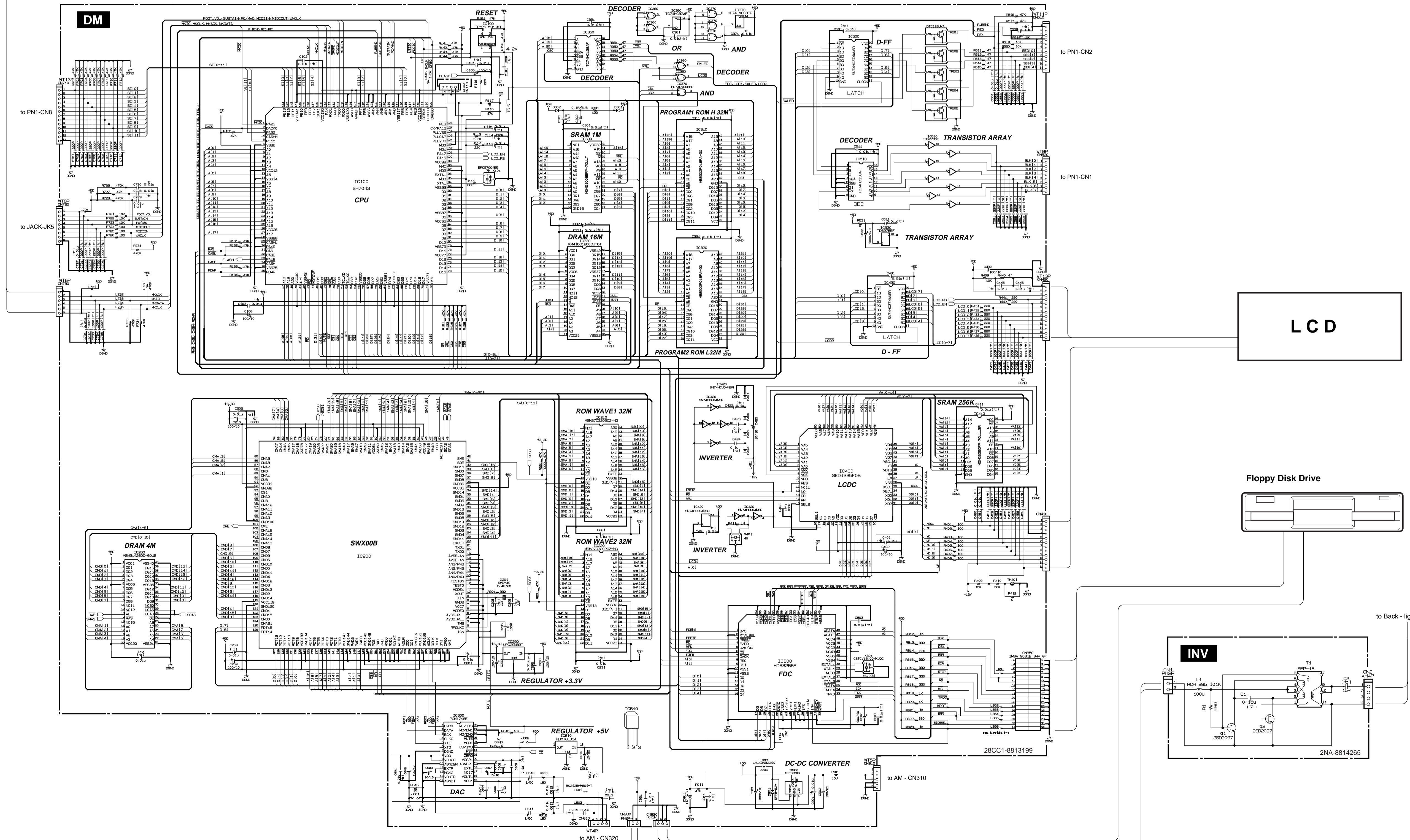
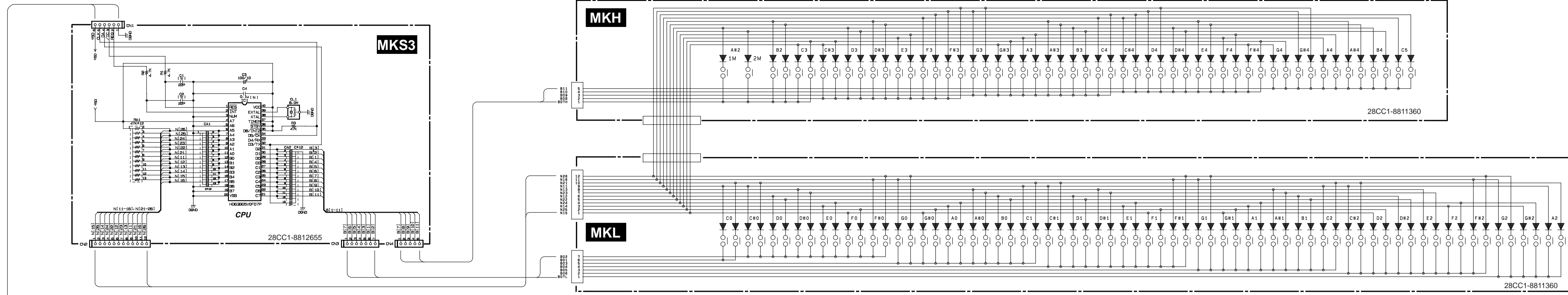
Note : See parts list for details of circuit board component parts



⊕: Ceramic Capacitor  
⊕±: Semi-Conductive Ceramic Capacitor

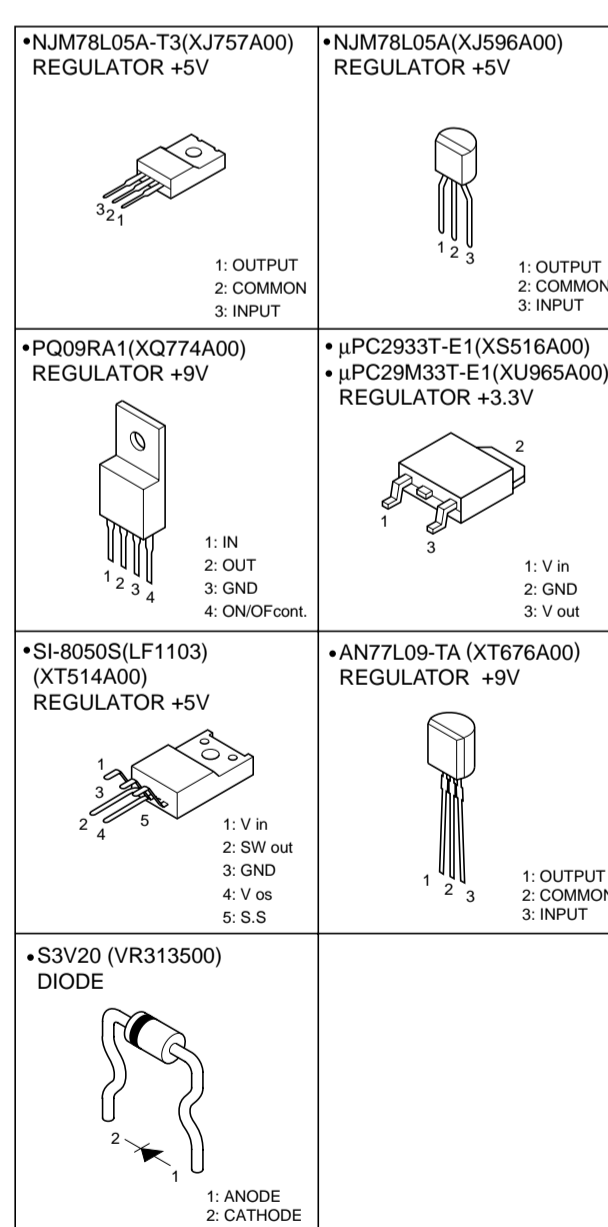
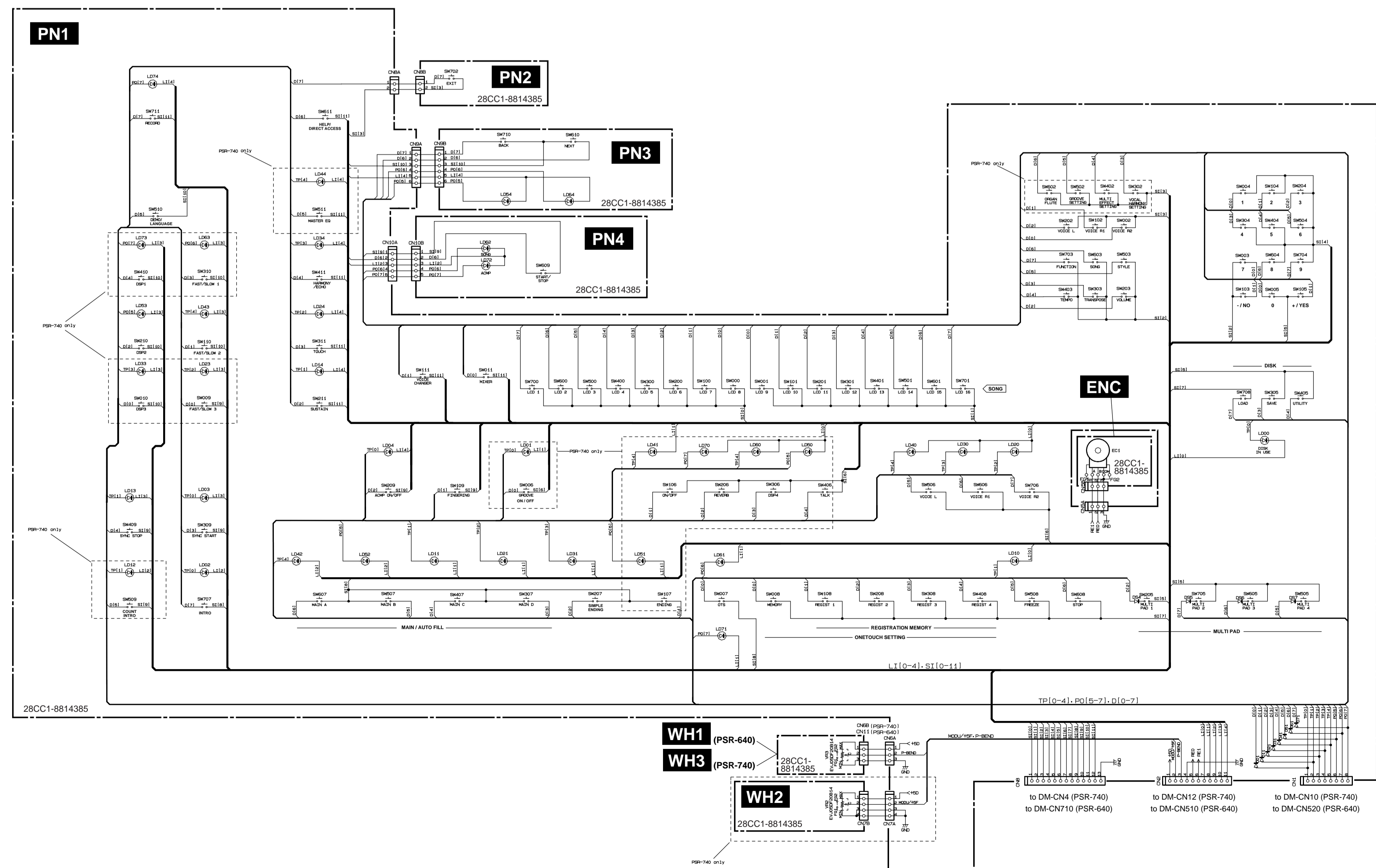
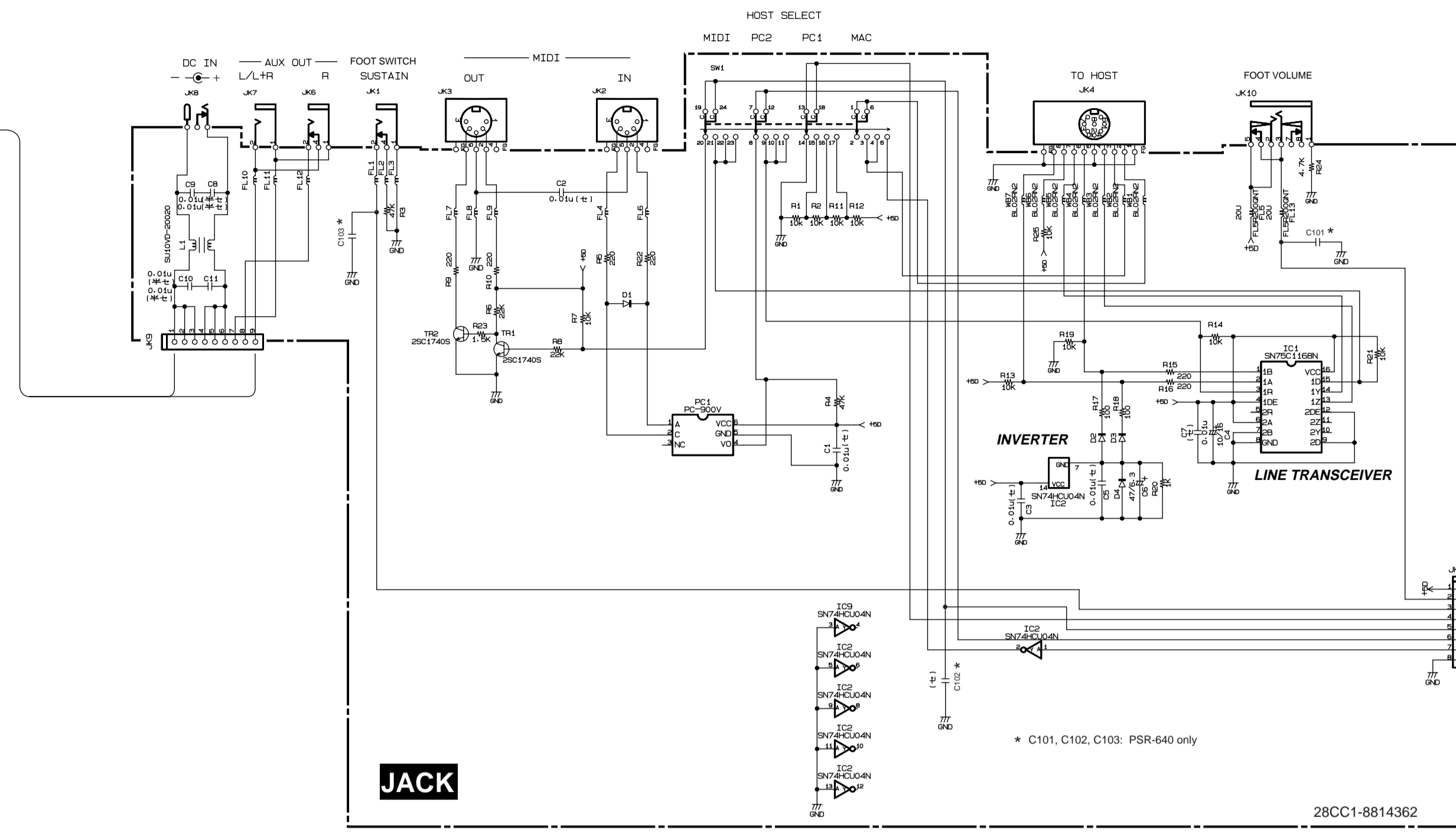
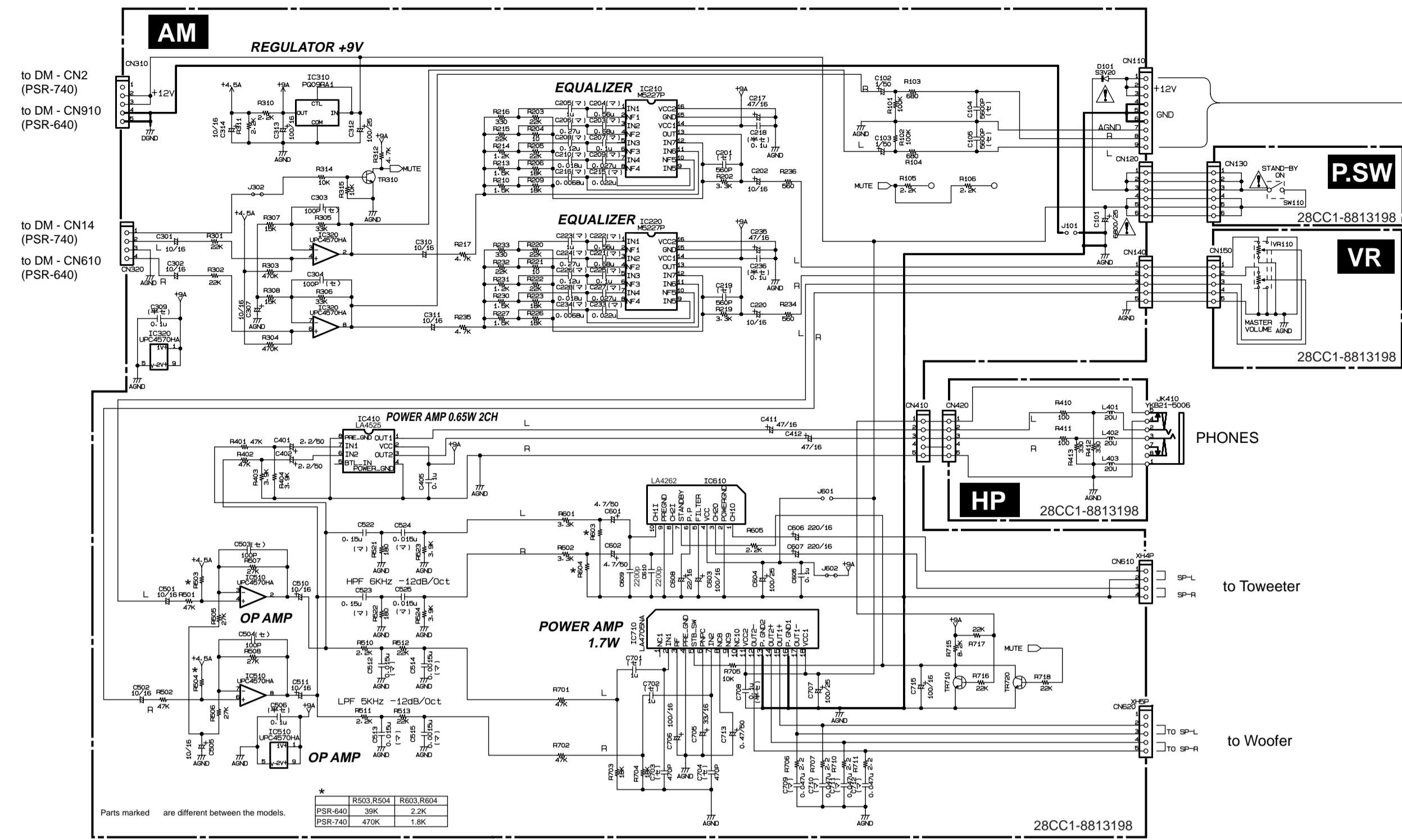
Note: See parts list for details of circuit board component parts





Note: See parts list for details of circuit board component parts

⊞: Ceramic Capacitor  
⊞: Mylar Capacitor



Note : See parts list for details of circuit board component parts

■ TO SERVICE PERSONNEL  
Critical Components Information  
Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.

- : Ceramic Capacitor
- ▣ : Semi-Conductive Ceramic Capacitor
- ▢ : Mylar Capacitor