Parallel ATA Interface Reference Design Guide

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Revision History

Rev.	Date	History
0.1	2012/2/7	1. 1st release

1. Scope

This document is intended as a guide for designing a custom system mainboard for Parallel ATA (PATA) interface. This guide includes reference schematics for the external circuitry required to implement the Parallel ATA (PATA) peripheral functions, as well as related comments and application notes. The circuits presented in this guide are typical application circuits. They may not be suitable for all applications. In particular, additional components may need to be added to these circuits in order to meet specific inquiry.

This reference design guide specifies the optional operating features of a parallel and serial bus transport described. It provides a common attachment interface for the physical and electrical requirements, schematic guidelines and layout guidelines.

2. Parallel Interface Physical and Electrical Requirements

2.1 Electrical characteristics

Table 1 defines the DC characteristics of the interface signals. Table 2 defines the AC characteristics. These characteristics apply to both host and device unless otherwise specified.

Description		Min	Max
I_{oL}	Driver sink current (See note 1)	4 mA	
I_{oLDASP}	Driver sink current for DASP (See note 1)	12 mA	
I_{oH}	Driver source current (See note 2)	400 μA	
$I_{oHDMARQ}$	Driver source current for DMARQ (See note 2)	500 μA	
I_Z	Device pull-up current on DD(15:8), DD(6:0), and STROBE when released	-100 μA	200 μA
I_{ZDD7}	Device pull-up current on DD7 when released	-100 μA	10 μA
V_{iH}	Voltage input high	2.0 VDC	5.5 VDC
V_{iL}	Voltage input low		0.8 VDC
V_{oH}	Voltage output high at IoH min (See note 3)	2.4 VDC	
V_{oL}	Voltage output low at IoL min (See note 3)		0.5 VDC
Additional DC characteristics for Ultra DMA modes greater than 4			
V_{DD3}	DC supply voltage to drivers and receivers	3.3 V - 8%	3.3 V + 8%
V+	Low to high input threshold	1.5 V	2.0 V
V–	High to low input threshold	1.0 V	1.5 V
V_{HYS}	Difference between input thresholds: $((V+_{current\ value}) - (V-_{current\ value}))$	320 mV	
V_{THRAVG}	Average of thresholds: $((V+_{current\ value}) + (V-_{current\ value}))/2$	1.3 V	1.7 V
V_{oH2}	Voltage output high at -6 mA to +3 mA (at V_{oH2} the output shall be able to supply and sink current to V_{DD3}) (See note 3)	VDD3 - 0.51 VDC	VDD3 + 0.3 VDC
V_{oL2}	Voltage output low at 6 mA (See note 3)		0.51 VDC

NOTES –
1. I_{oLDASP} shall be 12 mA minimum to meet legacy timing and signal integrity.
2. I_{oH} value at 400 μA is insufficient in the case of DMARQ that is pulled low by a 5.6 kΩ resistor.
3. Voltage output high and low values shall be met at the source connector to include the effect of series termination.
4. A device shall have less than 64 μA of leakage current into a 6.2 KΩ pull-down resistor while the INTRQ signal is in the released state.

Table 1. DC Characteristics

	Description	Min	Max
S_{RISE}	Rising edge slew rate for any signal (See note 1)		1.25 V/ns
S_{FALL}	Falling edge slew rate for any signal (See note 1)		1.25 V/ns
C_{host}	Host interface signal capacitance at the host connector (See note 2)		25 pf
C_{device}	Device interface signal capacitance at the device connector (See note 2)		20 pf
Additional AC characteristics for Ultra DMA modes greater than mode 4			
S_{RISE2}	Rising edge slew rate for DD(15:0) and STROBE (See note 1)	0.40 V/ns	1.0 V/ns
S_{FALL2}	Falling edge slew rate for DD(15:0) and STROBE (See note 1)	0.40 V/ns	1.0 V/ns
V_{DSSOH}	Induced signal to conductor side of device connector for any non-switching data signal at VoH due to simultaneous switching of all other data lines high and low by the device (See note 3)	V_{DD3} - 500 mV	
V_{DSSOL}	Same as V_{DSSOH} except non-switching data signal at VoL (See note 3)		500 mV
V_{HSSOH}	Induced signal to conductor side of host connector for any non-switching data signal at VoH due to simultaneous switching of all other data lines high and low by the host (See note 3)	V_{DD3} - 600 mV	
V_{HSSOL}	Same as V_{HSSOH} except non-switching data signal at VoL (See note 3)		600 mV
V_{RING}	AC voltage at recipient connector (See note 4)	-1.0 V	6.0 V
$C_{device2}$	Device capacitance measured at the connector pin (See note 2)		17 pf
C_{ratio}	Ratio of the highest DD(15:0) or STROBE signal capacitance as measured at the connector to the lowest DD(15:0) or STROBE signal capacitance.		1.5
V_{ihPEAK}	The highest voltage reached on a rising transition at the recipient connector within 3 ns of crossing 1.5 V (See note 5)	2.2 V	
V_{ihRING}	The lowest voltage on a high signal at the recipient connector at any time after the rising edge crosses VihPEAK until activity driven low by a subsequent falling transition (See note 5)	1.7 V	
V_{ilPEAK}	The lowest voltage reached on a falling transition at the recipient connector within 3 ns of crossing 1.5 V (See note 5)		0.8 V
V_{ilRING}	The highest voltage on a low signal at the recipient connector at any time after the falling edge crosses V_{ilPEAK} until activity driven high by a subsequent rising transition (See note 5)		1.3 V

NOTES -
1. Signal integrity may be improved by using slower slew rates at slower transfer rates.
2. Capacitance measured at 1 MHz.
3. Please refer to “Information Technology - AT Attachment – 8 ATA/ATAPI Parallel Transport (ATA8-APT)” 4.2.1.2 for measurement details.
4. The sender shall not generate voltage peaks higher then these absolute limits on DD (15:0) with all data lines switching simultaneously and a single recipient at end of cable. The test load shall be an 18" long, 40-conductor cable in Ultra DMA mode 2, as well as, an 18", long 80-conductor cable operated in the highest Ultra DMA mode supported.
5. V_{ihPEAK}, V_{ihRING}, V_{ilPEAK}, and V_{ilRING} shall be met in a functioning system across all patterns and shall be met when measured at any connector.

Table 2. DC Characteristics

2.2 Cable configuration

The following table defines the host transceiver configurations for a dual cable system configuration for all transfer modes.

Transfer mode	Optional host transceiver configuration	Recommended host transceiver configuration	Mandatory host transceiver configuration
All PIO and Multiword DMA	One transceiver may be used for signals to both ports.	DIOR-, DIOW-, and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW-, and IORDY or CS0- and CS1- shall have a separate transceiver for each port.
Ultra DMA 0, 1, 2	One transceiver may be used for signals to both ports except DMACK-.	DIOR-, DIOW-, and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW-, and IORDY or CS0- and CS1- shall have a separate transceiver for each port. DMACK- shall have a separate transceiver for each port.
Ultra DMA modes > 2	One transceiver may be used for signals to both ports for RESET-, INTRQ, DA(2:0), CS0-, CS1-, and DASP-.	RESET-, INTRQ, DA(2:0), CS0-, CS1-, and DASP- should have a separate transceiver for each port.	All signals shall have a separate transceiver for each port except for RESET-, INTRQ, DA(2:0), CS0-, CS1-, and DASP-.

The following table defines the system configuration for connection between devices and systems for all transfer modes. For Ultra DMA modes requiring an 80-conductor cable, that cable should meet requirements for 80-conductor cables.

Transfer mode	Single device direct connection configuration (See note 1)	40-conductor cable connection configuration	80-conductor cable connection configuration
All PIO and Multiword DMA	May be used.	May be used.	May be used (See note 2)
Ultra DMA 0, 1, 2	May be used.	May be used.	May be used (See note 2)
Ultra DMA modes > 2	May be used (See note 3).	Shall not be used.	May be used (See note 3).

NOTES -
1. Direct connection is a direct point-to-point connection between the host connector and the device connector.
2. 80-conductor cable assemblies may be used in place of 40-conductor cable assemblies to improve signal quality for data transfer modes that do not require an 80-conductor cable assembly.
3. Either a single device direct connection configuration or an 80-conductor cable connection configuration shall be used for systems operating with Ultra DMA modes greater than 2.

3. Schematic Guidelines

3.1 IDE Port Schematic Guidelines

The IDE port can support two storage disks or other ATAPI devices. These two storage disks on the port are wired in parallel, which is accomplished by plugging both drives into a single flat ribbon cable equipped with two socket connectors. A jumper can be manually set on each IDE storage disk for selecting master or slave mode.

If two storage disks are used in the master/slave mode, the IDE_CBLID# of both storage disks must be connected together as in Figure 1. These pairs of pins negotiate between the master and slave storage disks. The storage disks may not function correctly unless these pins are interconnected. If two storage disks are plugged into one standard IDE cable, the cable will interconnect the pins properly by itself.

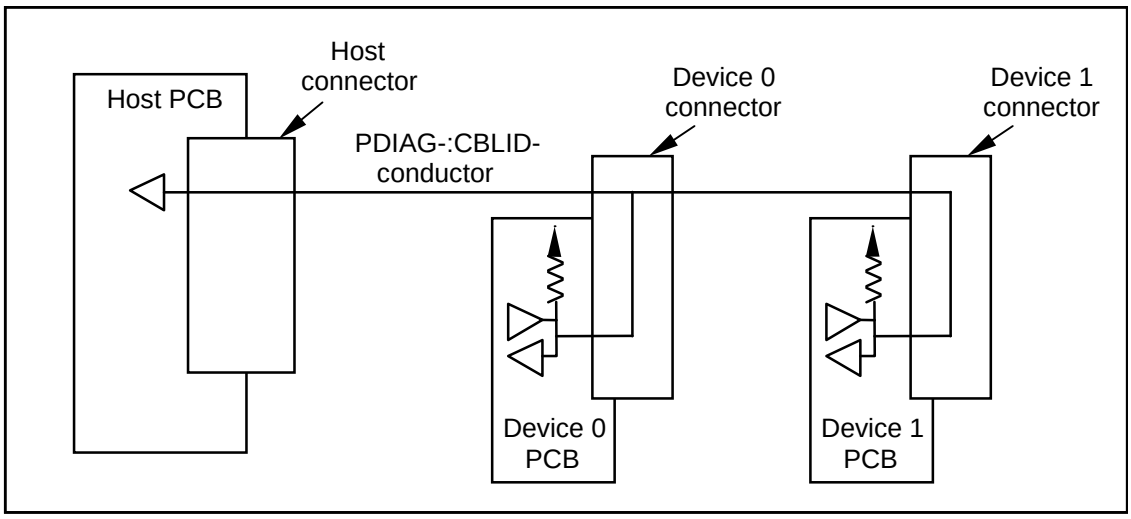

Figure 1. IDE Master/Slave Handshake Signals Connection

The DASP-S# (pin 39 on IDE connector or pin 45 on CF connector) should be also connected between master and slave storage disks.

A diagram illustrating connections from the Module connector to a 0.1-inch pitch, two-row, 40-pin header suitable for use with standard parallel ATA drives is shown in Figure 2. No pull-ups or other termination are required.

An industry standard 80-pin, 0.25-inch pitch cable is used for Ultra-DMA 66 and 100 drives. The cable assemblies have sockets with 40 positions. The extra 40 conductors on the 80-conductor cable are tied to GND to isolate the adjacent signals for improved signal integrity.

3.1.1 IDE 40-Pin Header and Schematic

Power to the parallel ATA drive is handled on a separate 4-pin connector and is not shown here. The 40-pin IDE header is used with a 40-pin, 0.5-inch pitch, and flat cable for slower drives.

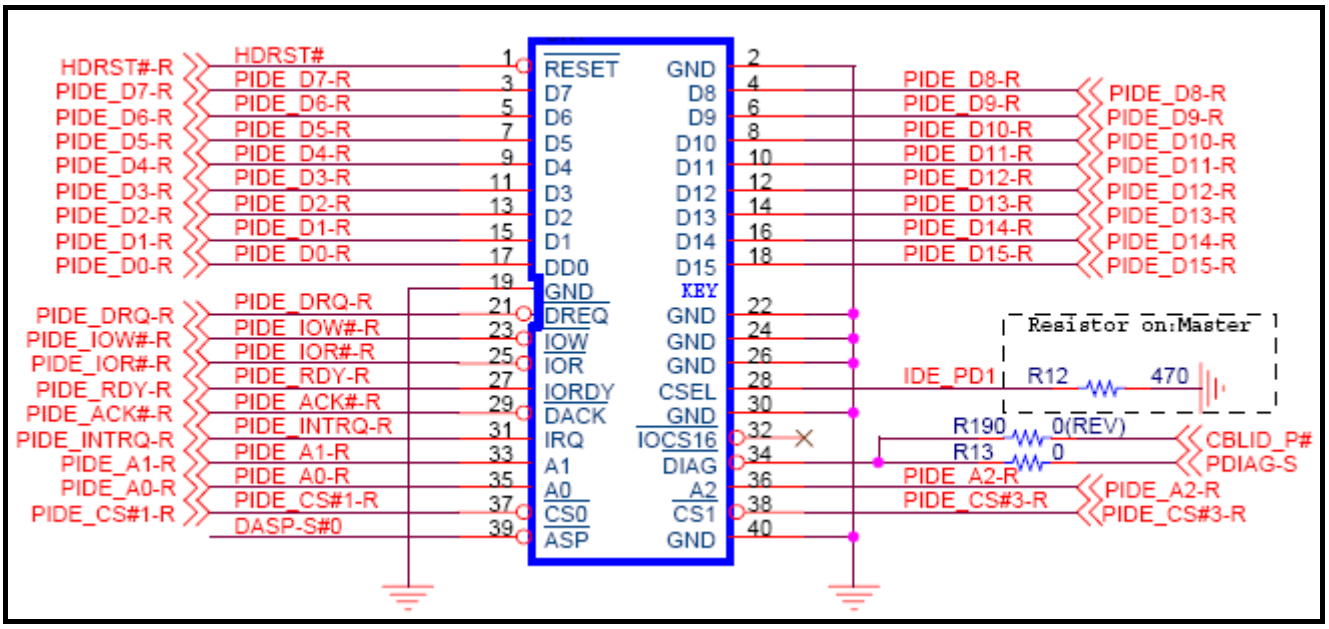

Figure 2. IDE 40-Pin Connector Schematic

3.1.2 IDE 44-Pin Header and Schematic

Figure 3 shows a 44-pin, 2mm-pitch header used for 2.5”-IDE drives. The cabling used is a 44-pin, 1mm-pitch, flat-ribbon cable. Power to the drive is supplied over the 44-pin cable on Conductors 41 and 42. The drive-activity LED shown is driven by signal pin, ATA_ACT#.

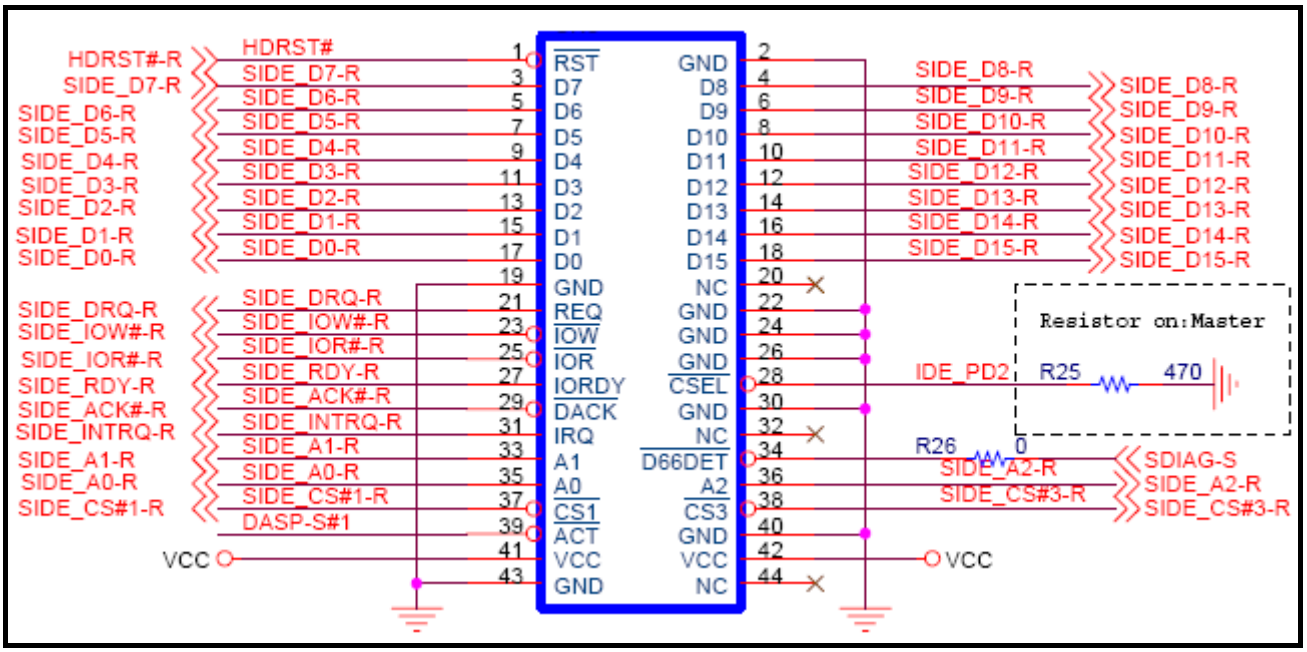

Figure 3. IDE 44-Pin Connector Schematic

3.1.3 IDE Port Implementation Notes

- The IDE port connector shown is a standard 40-pin IDC flat-cable header, which is used with 3.5 inch IDE storage disk. These storage disks require a separate power cable to provide them with 5 and 12V operating power.

- The IDE port connector shown is a 44-pin, 2mm header of the type used with 2.5 inch IDE storage disk. The pinout is the same as for the standard connector, with the addition of pins 41, 42, 43 and 44 which provide 5V power to the drive. It does not require a separate power cable.

- Each IDE port can support two storage disks. The two storage disks on each port are wired in parallel, which is accomplished by plugging both drives into a single flat ribbon cable equipped with two socket connectors. A jumper is typically manually set on each storage disks to set it for “master” or “slave” operation.

- If two storage disks are used in the master/slave mode on the same IDE port, the DASP# pins of both storage disks must be connected together. Also, the PDIAG# pins of both storage disks must be connected together. These pairs of pins negotiate between the master and slave storage disks. The storage disk may not function correctly unless these pins are interconnected. If two storage disks are plugged into a single IDE cable, the cable will interconnect the pins properly. If the two storage disks on one port are integrated on the baseboard or plugged into separate connectors, care should be taken to tie the corresponding pins together. On a standard IDE connector, PDIAG# is Pin 34 and DASP# is Pin 39.

- The DASP# and PDIAG# pins from the primary and secondary IDE ports should NOT be tied together. They should only be connected between the devices that share a single port.

3.2 CompactFlash (CF) Socket on IDE Port Schematic Guidelines

3.2.1 CompactFlash (CF) Socket and Schematic

For the IDE application, the CompactFlash (CF) card cannot be hot-plugged. If hot-plug support is necessary, the PCI-based Card-Bus controller chip can be integrated onto the platform and used to control the CF hot-plug function. Figure 4 shows the CF schematics.

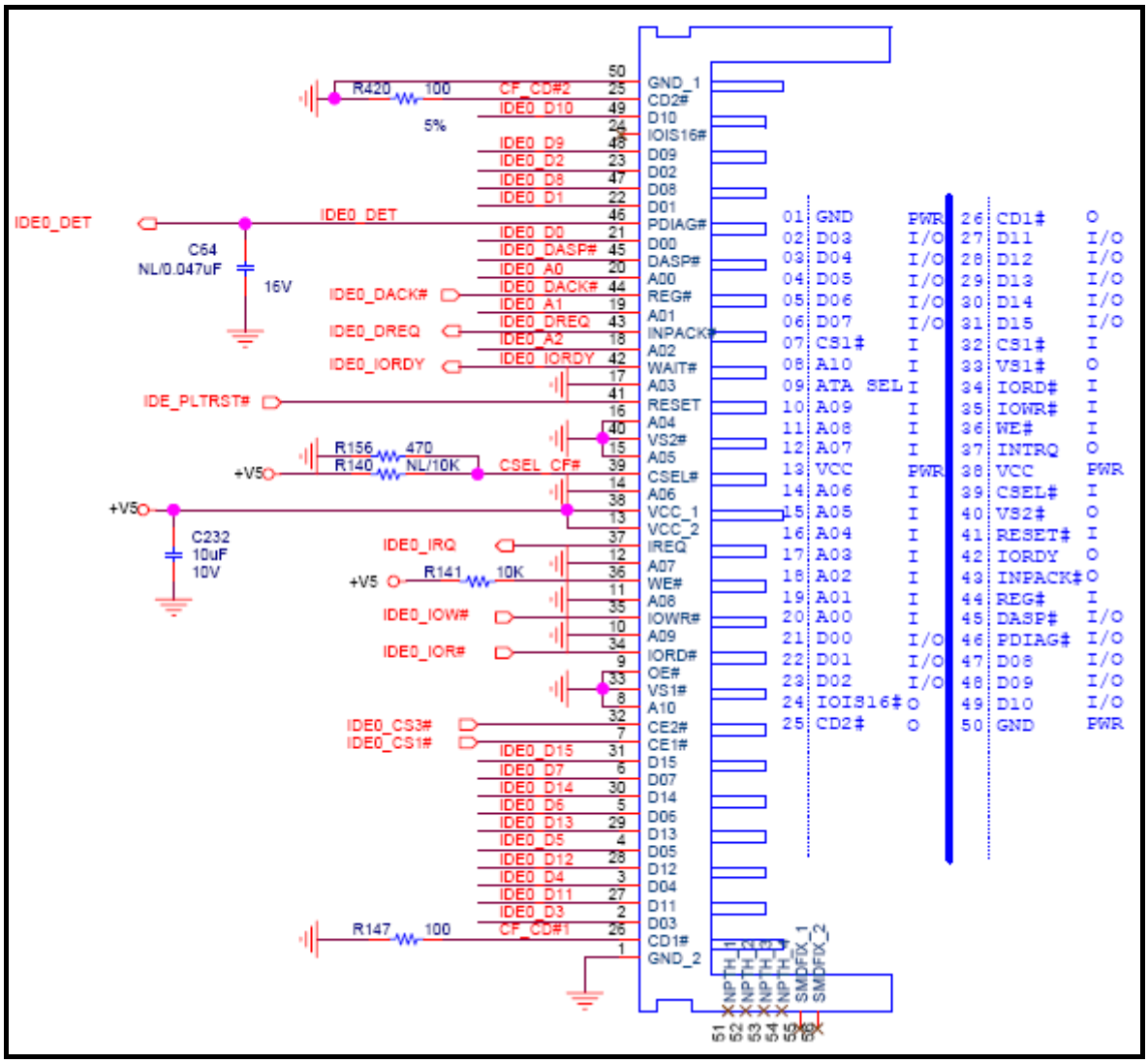

Figure 4. CompactFlash (CF) Socket Schematic

3.2.2 CompactFlash (CF) Socket on IDE Port Implementation Notes

- The CF card can be configured as a slave device by changing the voltage level of the CSEL signal.

- The CF card can be configured as a slave device when the CSEL signal is set as non-connection. If two CF cards (or one CF card and one hard drive) are used in the master/slave mode on the same IDE port, the IDE_CBLID# and DASP-S#0 pins on both devices must be connected. The signal negotiates the communication between the master

and slave devices.

3.3 UDMA Support

SQFlash storage devices support UDMA ATA 33/ 66/ 100 data transfer modes. If an advanced IDE data transfer mode such as UDMA 66/ 100 is required, the 80-pin type IDE connector and cable are needed for signal integrity.

To provide better signal integrity, the optional 80-conductor cable assembly is specified for use with 40-pin connectors. Use of this assembly is mandatory for systems operating at Ultra DMA modes greater than 2.

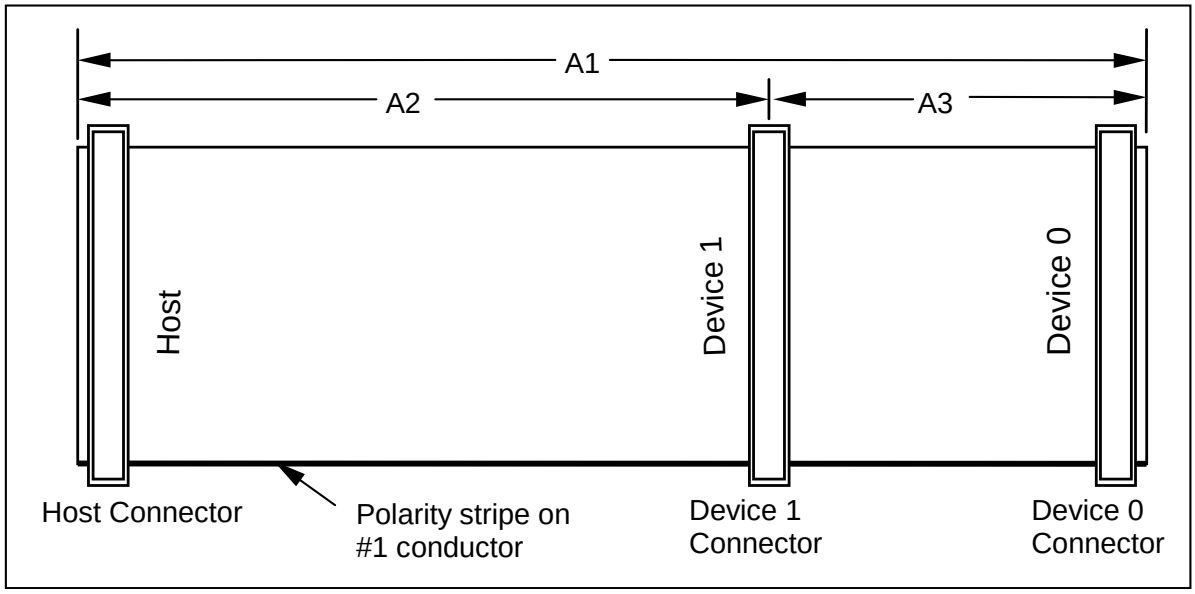

Figure 5. 80-conductor cable configuration

Dimension	Millimeters	Inches
A 1	457.20 max	18.00 max
A 2	127.00 min	5.00 min
A 3	152.40 max	6.00 max
A2 min shall be greater than or equal to A3.		

Table 3. 80-conductor cable configuration

4. Layout Guidelines

The IDE interface can be routed with 6-mil traces on 6-mil spaces (dependent upon stack-up parameters), and must be less than 7 inches in length (from ICH to platform IDE connector).

The maximum length difference between the data signals and the strobe signal (IDE_IOR# and IDE_IOW#) should be less than 100 mils. Refer to Advantech's layout checklist for the details of each platform. Use Daisy Chain not Y type routing if both IDE and CF connectors are needed.