

# IL1 Block Diagram

B --> C  
2008-01-08

- VTERM(+0.9V)
- VTT(+1.05V)
- +1.5VSUS
- +1.5V
- +1.8VMEM
- +1.8V
- +2.5V
- 3VPCU
- +3.3V
- +3.3VSUS
- LCD\_3.3V
- LCD\_5V
- +5V

**C7-M (ULV)**

VCORE:+1.196 ~ +0.748  
VCCP:+1.05V  
VCCA:+1.8V or +1.5V

**CPU VCORE**

**Clock Gengerator  
ICS9UM700**

**CRT**

**7" LCD**

**VX800(U)**

VTT:VCCP (+1.05V)  
VCC15:+1.5V or +1.2V  
VCC33:+3.3V  
VCCMEM:+1.8V  
VSUS15:+1.5VSUS  
VSUS33:+3.3VSUS

**DDRII  
256M/512M/1GB**

**1.8" HDD(option)**

**NAND FLASH  
Controler SM223**

**1/2/4 GB  
NAND FLASH**

**RJ-45** - **10/100 Ethernet  
RTL8100CL**

**RJ-11** - **Modem DDA  
CSP1040**

**Int. SPK** - **HDA CODEC  
ALC267**

**Audio Jack**

**Int. Mic** - **SD/MMC/MS  
3 IN 1 Card SLOT**

VID[0:6]

+/- CPU CLK

+/- HCLK

V4  
BUS

CHA

IDE

USB

USB

USB

LPC BUS

**EC  
KB3310**

**Camera Conn.**

**Camera  
Module**

**WLAN Conn.**

**WLAN  
Module**

**USB PORT X2**

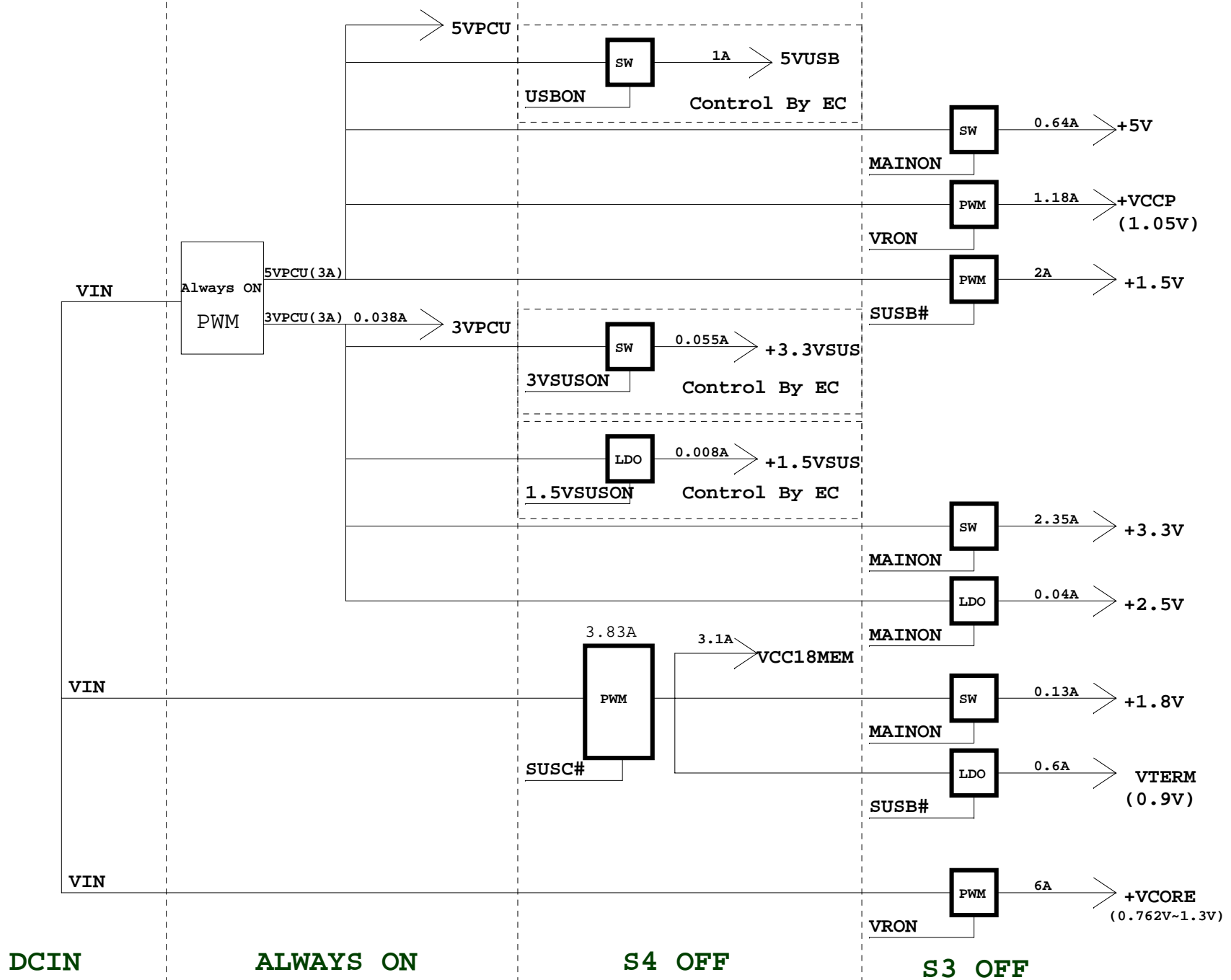
**SPI  
Flash**

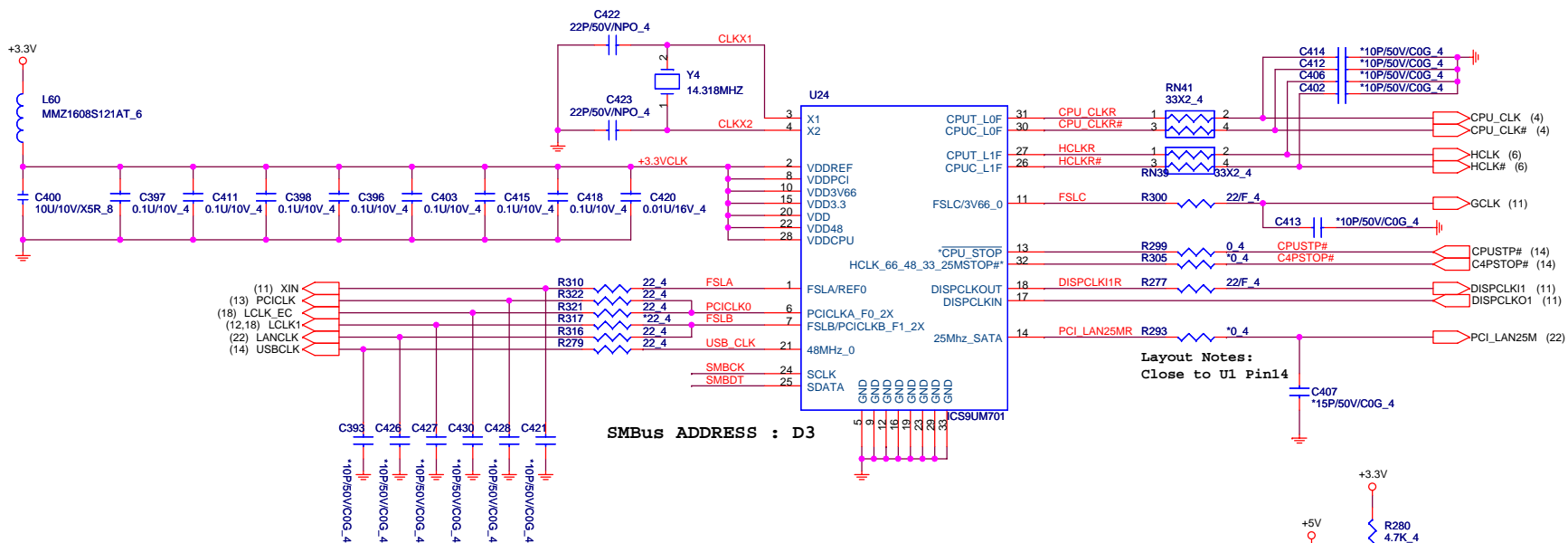
**Int. KB**

**T/P**

**Battery**

**Charger**





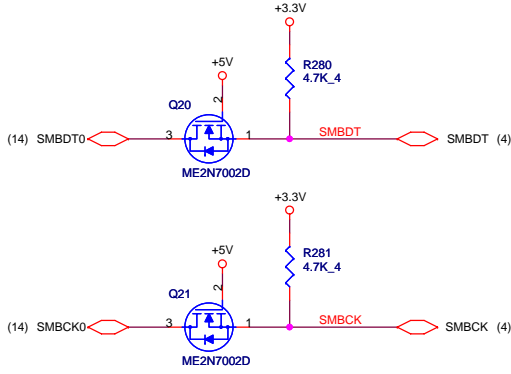
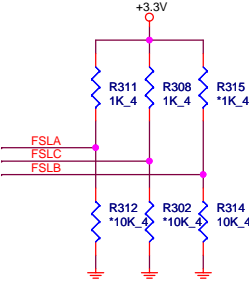
Layout Notes:  
Close to U1 Pin14

SMBus ADDRESS : D3

- (11) XIN
- (13) PCICLK
- (18) LCLK\_EC
- (12,18) LCLK1
- (22) LANCLK
- (14) USBCLK

ICS9UM701 ON : 0 OFF : 1

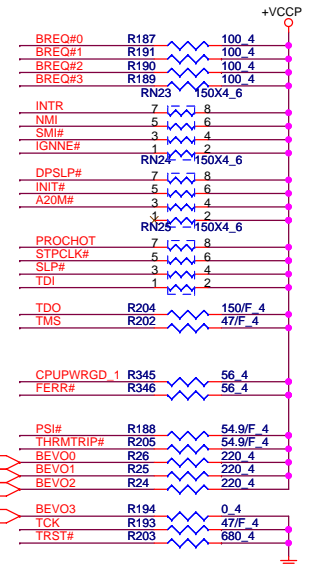
3	2	1	CPU	PCI
FSLA	FSLC	FSLB	266.66	33
0	0	0	133.33	33
0	0	1	200	33
1	0	1	166.66	33
0	1	0	333.33	33
1	1	0	100	33
0	1	1	400	33
1	1	1	200	33





C7M\_1GHz

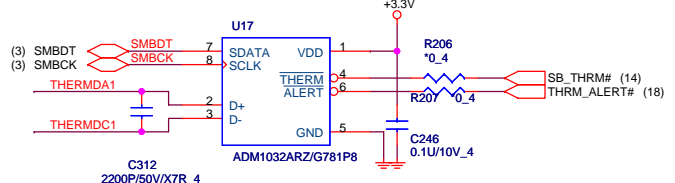
Reserve for internal pull-up resistor verify




Resistor must be close to the CPU



Resistor must be close to the CPU

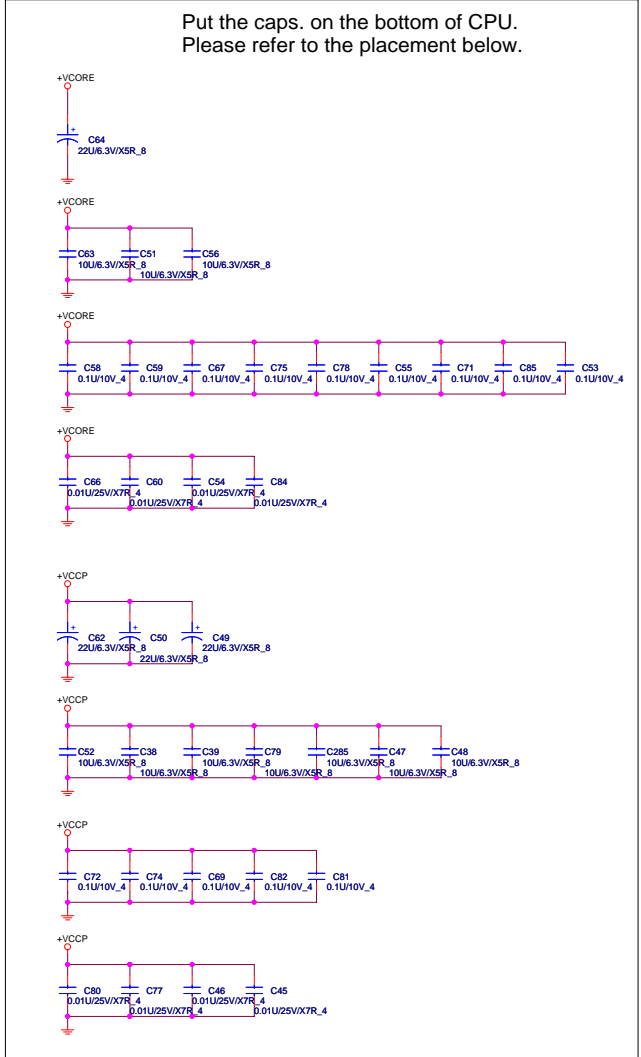
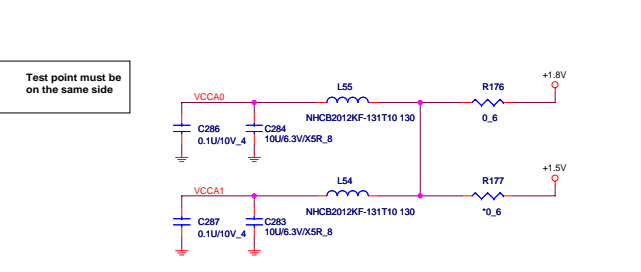
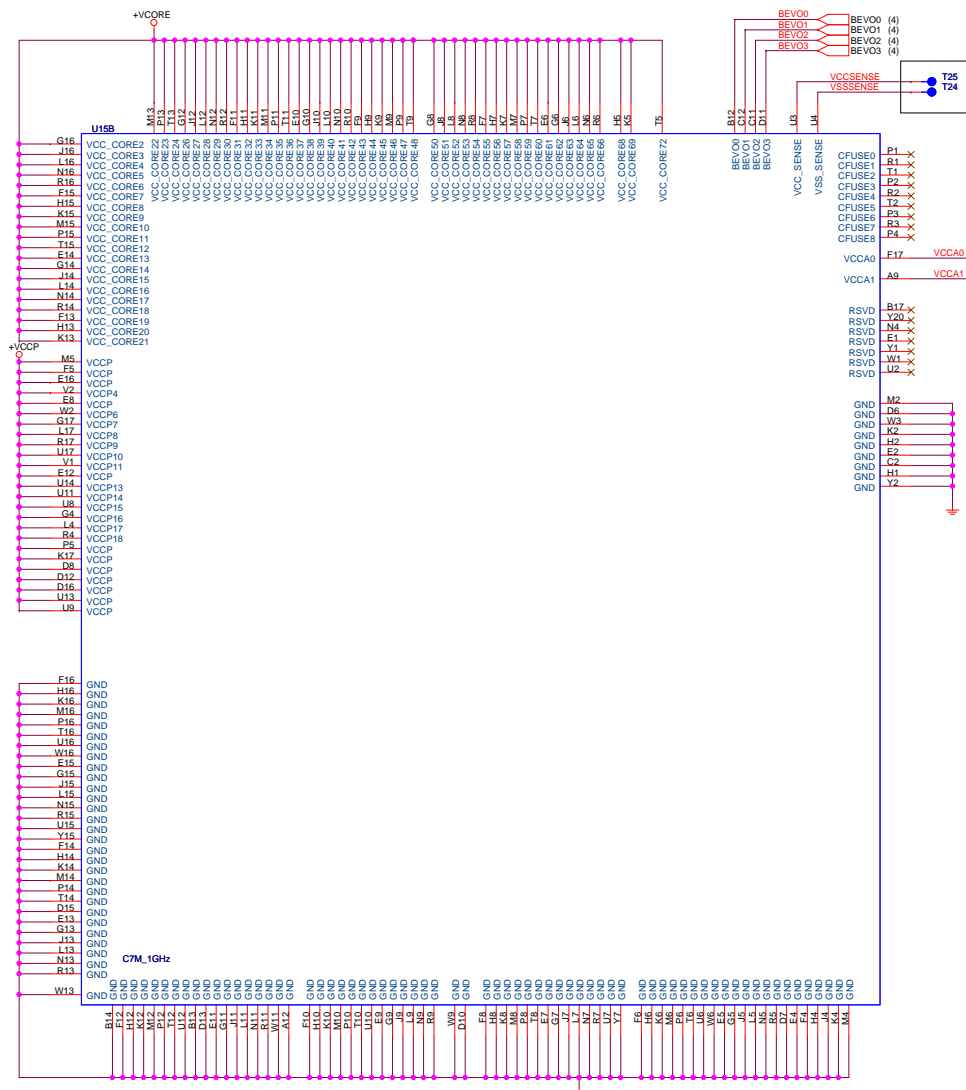


SMBus ADDRESS: 4C

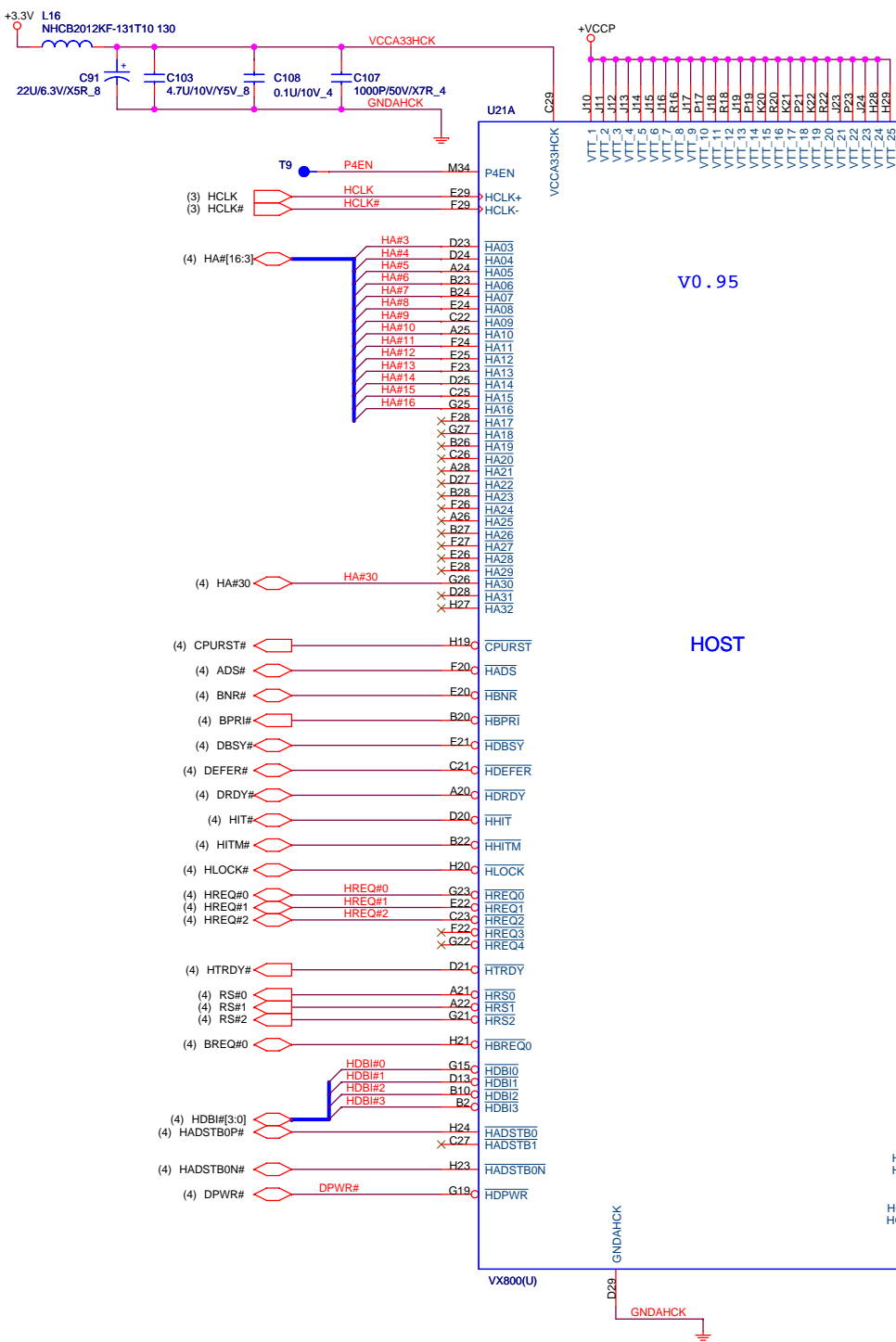


**PROJECT : IL1**  
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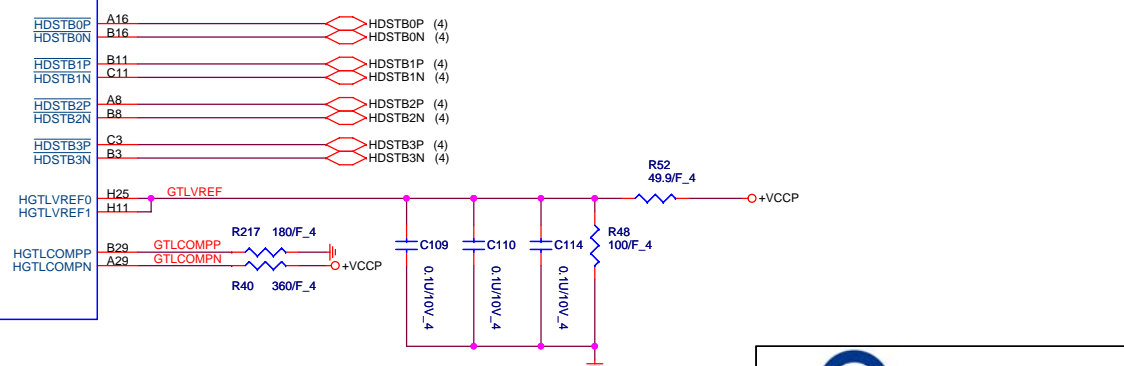
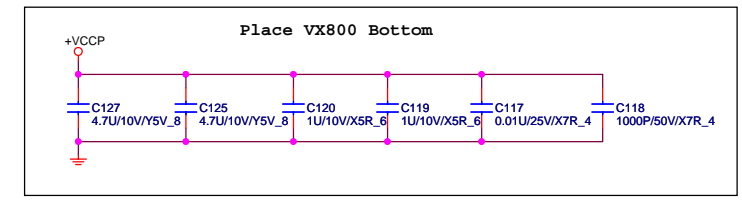
Size A3	Document Number <b>CPU C7M V4BUS</b>	Rev 1A
Date: Friday, January 11, 2008		Sheet 4 of 30



ky@h@h@h@hotmail.com




HD00	E17	HD#0
HD01	D15	HD#1
HD02	A17	HD#2
HD03	C15	HD#3
HD04	C14	HD#4
HD05	F15	HD#5
HD06	E16	HD#6
HD07	D17	HD#7
HD08	C17	HD#8
HD09	B15	HD#9
HD10	A14	HD#10
HD11	F16	HD#11
HD12	E14	HD#12
HD13	D16	HD#13
HD14	B14	HD#14
HD15	H15	HD#15
HD16	F12	HD#16
HD17	H13	HD#17
HD18	D11	HD#18
HD19	H12	HD#19
HD20	E13	HD#20
HD21	G14	HD#21
HD22	E12	HD#22
HD23	A13	HD#23
HD24	A13	HD#24
HD25	C13	HD#25
HD26	A12	HD#26
HD27	F11	HD#27
HD28	G11	HD#28
HD29	G13	HD#29
HD30	D12	HD#30
HD31	B12	HD#31
HD32	G9	HD#32
HD33	B7	HD#33
HD34	F10	HD#34
HD35	C9	HD#35
HD36	D9	HD#36
HD37	A9	HD#37
HD38	A10	HD#38
HD39	C10	HD#39
HD40	G10	HD#40
HD41	C7	HD#41
HD42	D8	HD#42
HD43	F10	HD#43
HD44	D7	HD#44
HD45	E8	HD#45
HD46	H9	HD#46
HD47	F9	HD#47
HD48	C5	HD#48
HD49	A4	HD#49
HD50	C6	HD#50
HD51	C2	HD#51
HD52	D4	HD#52
HD53	A6	HD#53
HD54	D5	HD#54
HD55	A2	HD#55
HD56	A5	HD#56
HD57	E6	HD#57
HD58	D3	HD#58
HD59	D1	HD#59
HD60	C1	HD#60
HD61	B4	HD#61
HD62	A1	HD#62
HD63	B6	HD#63



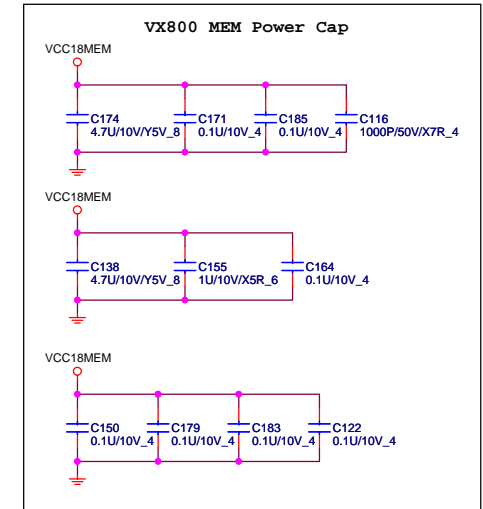
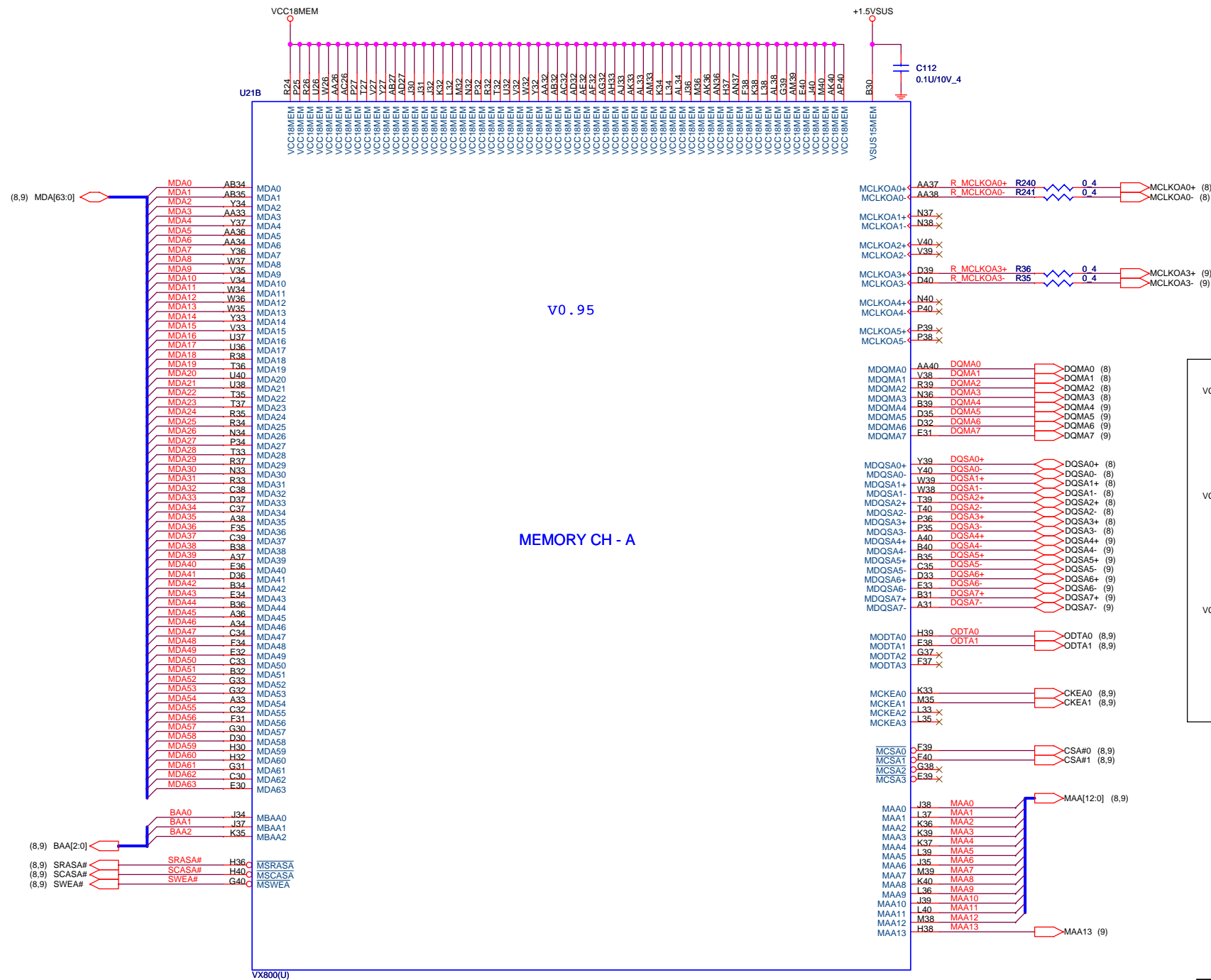
V0.95

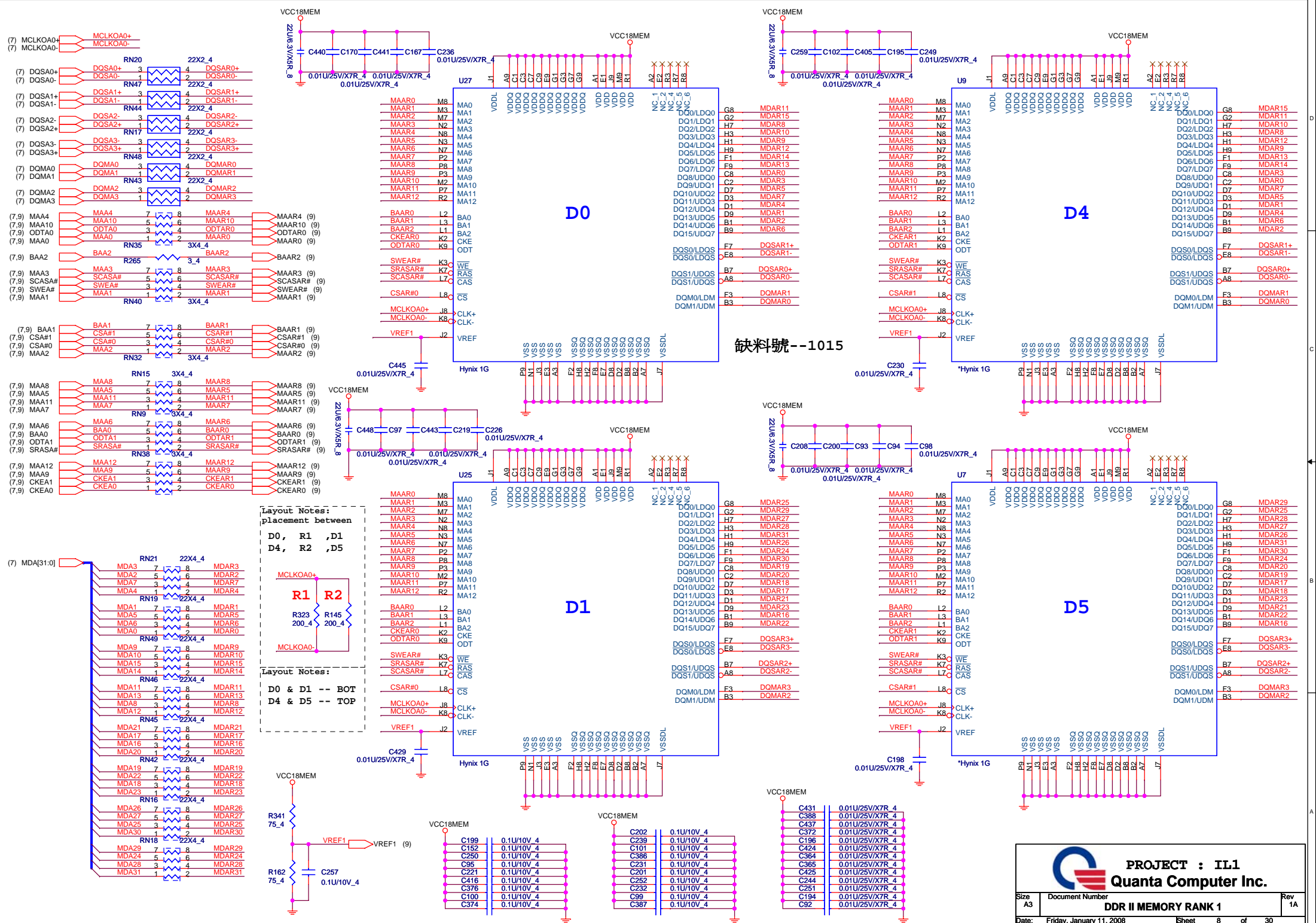
HOST



**PROJECT : IL1**  
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**Layout Notes:**  
 placement between  
 D0, R1 ,D1  
 D4, R2 ,D5

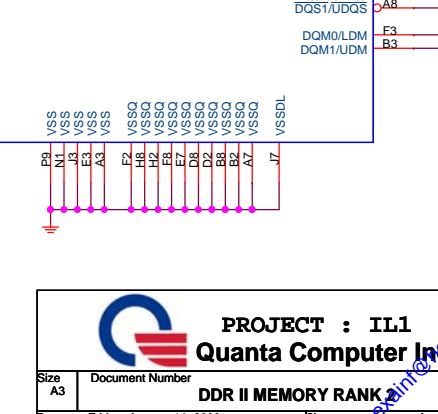
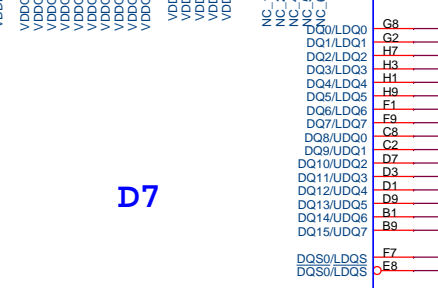
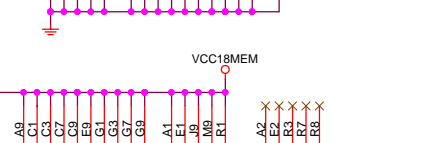
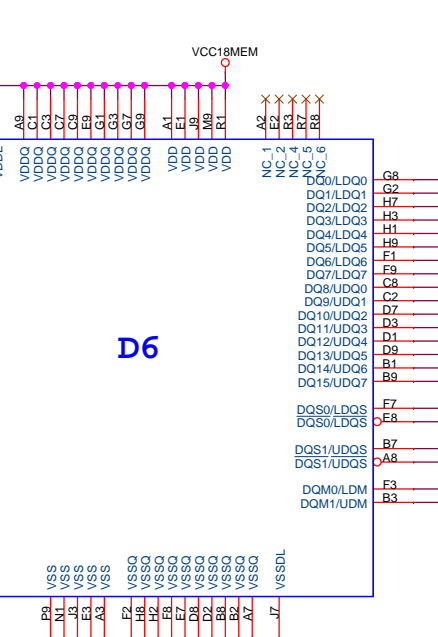
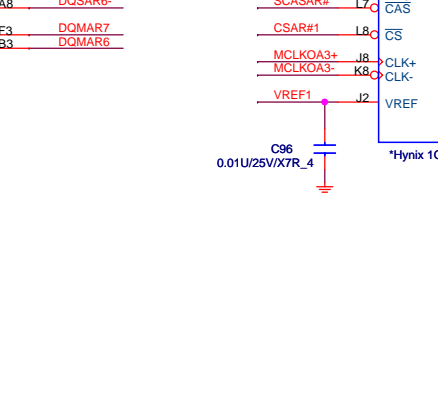
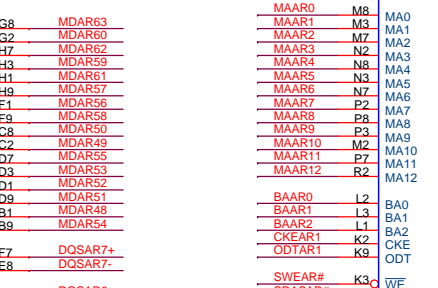
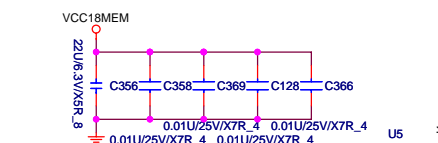
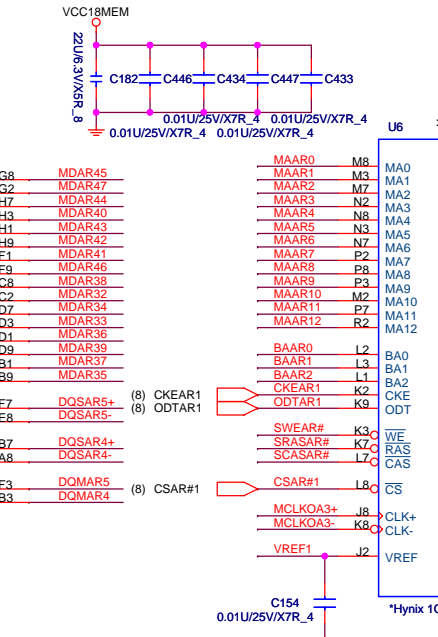
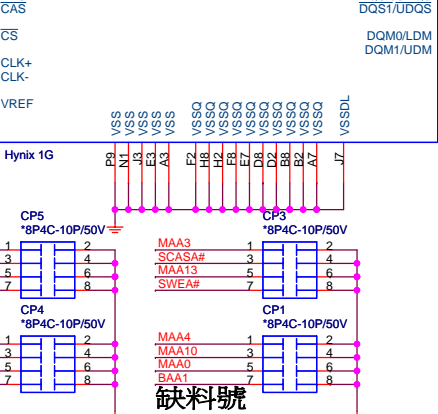
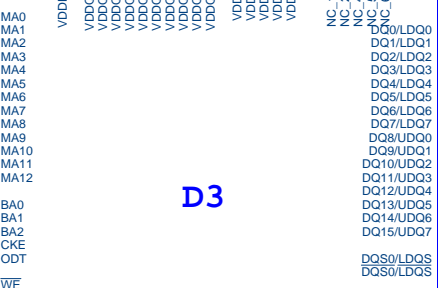
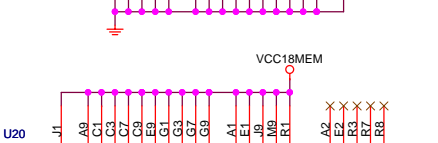
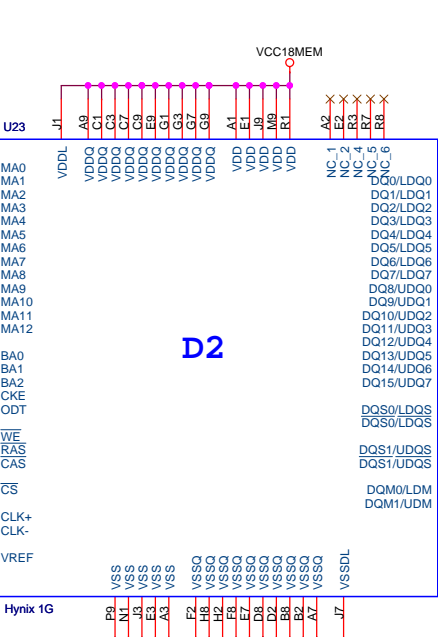
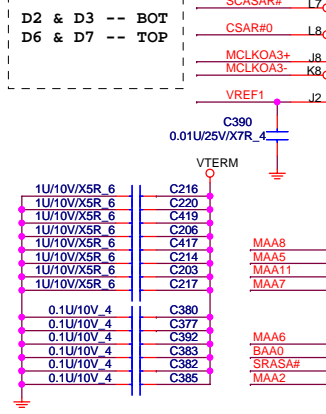
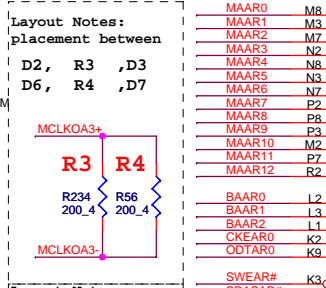
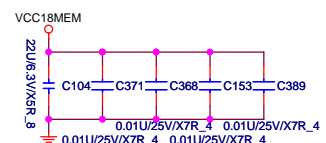
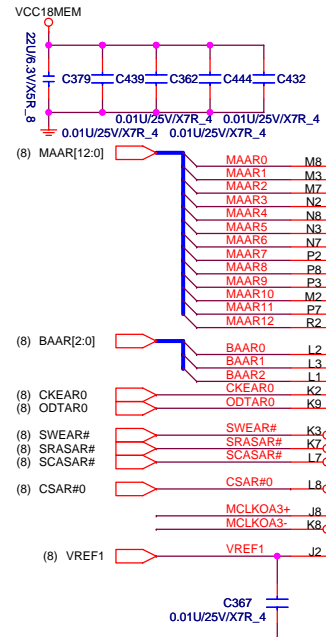
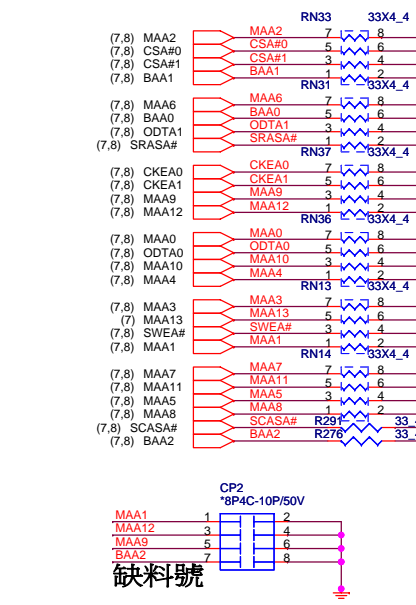
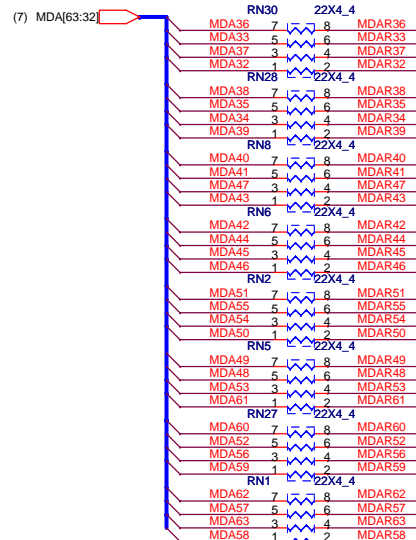
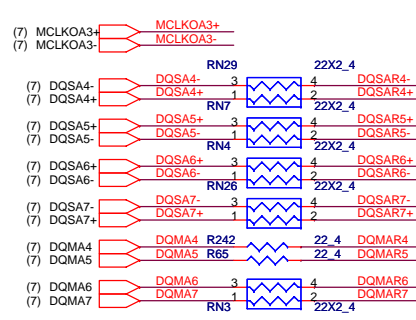
**Layout Notes:**  
 D0 & D1 -- BOT  
 D4 & D5 -- TOP

缺料號--1015


**PROJECT : IL1**  
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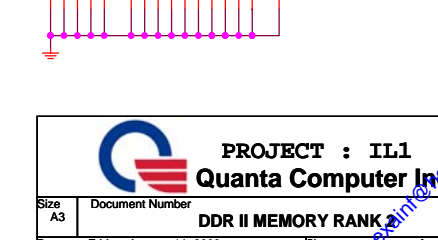
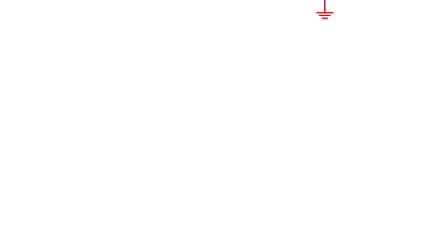
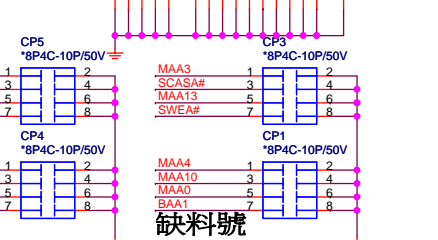
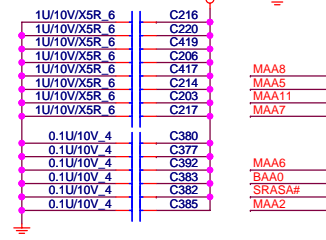
Size A3	Document Number <b>DDR II MEMORY RANK 1</b>	Rev 1A
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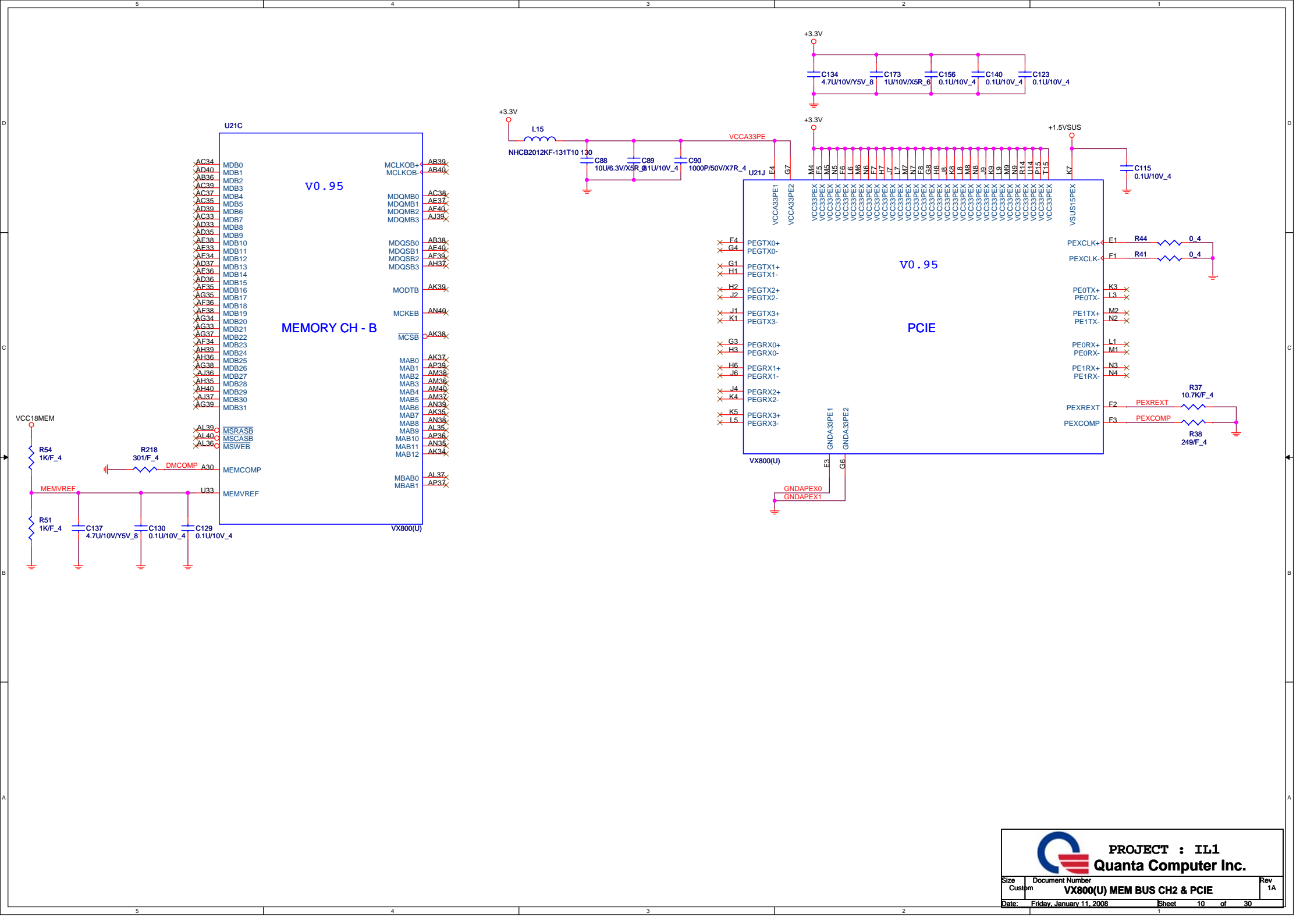
**Layout Notes:**  
 placement between  
 D2, R3, D3  
 D6, R4, D7

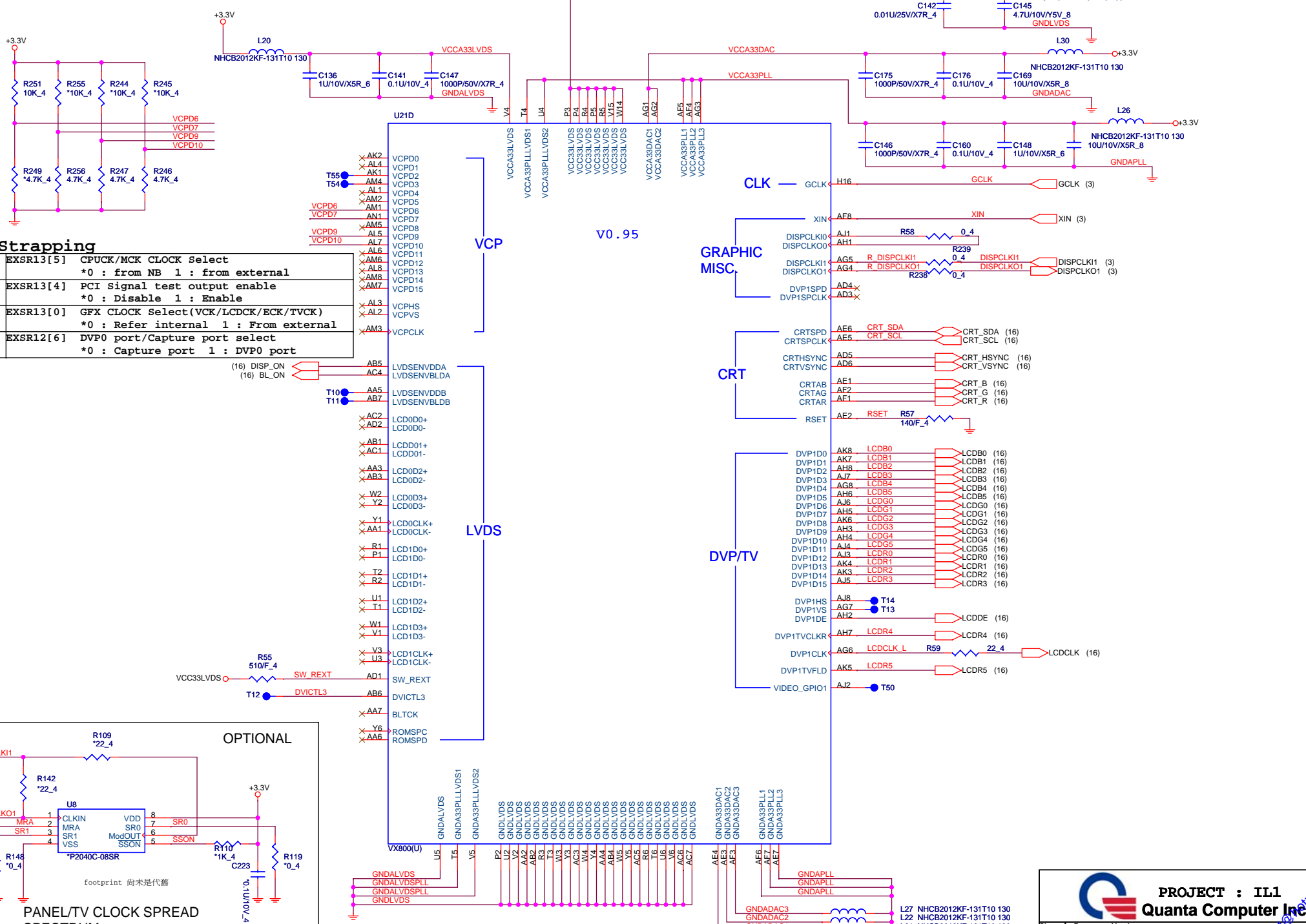
**Layout Notes:**  
 D2 & D3 -- BOT  
 D6 & D7 -- TOP



**PROJECT : IL1**  
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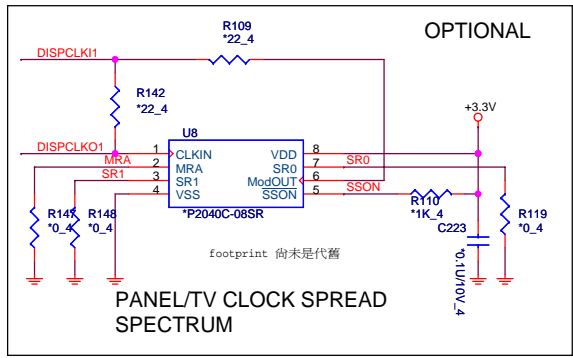
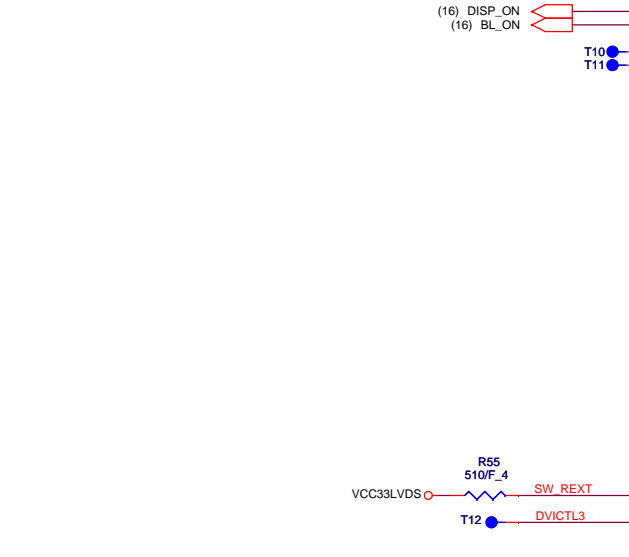
Size A3 Document Number **DDR II MEMORY RANK** Rev 1A  
 Date: Friday, January 11, 2008 Sheet of 30






### GFX Strapping

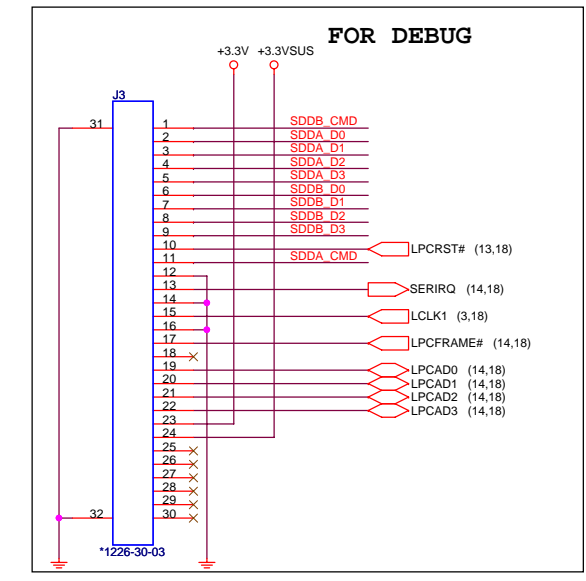
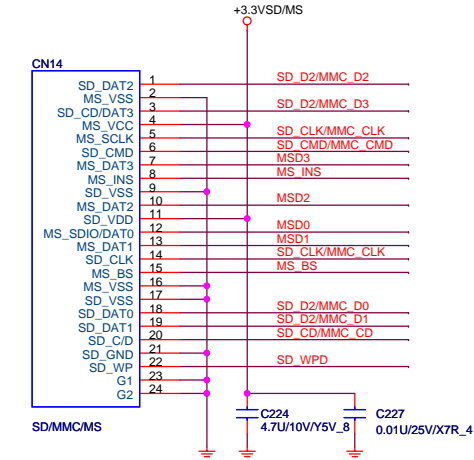
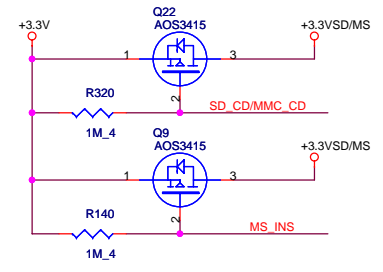
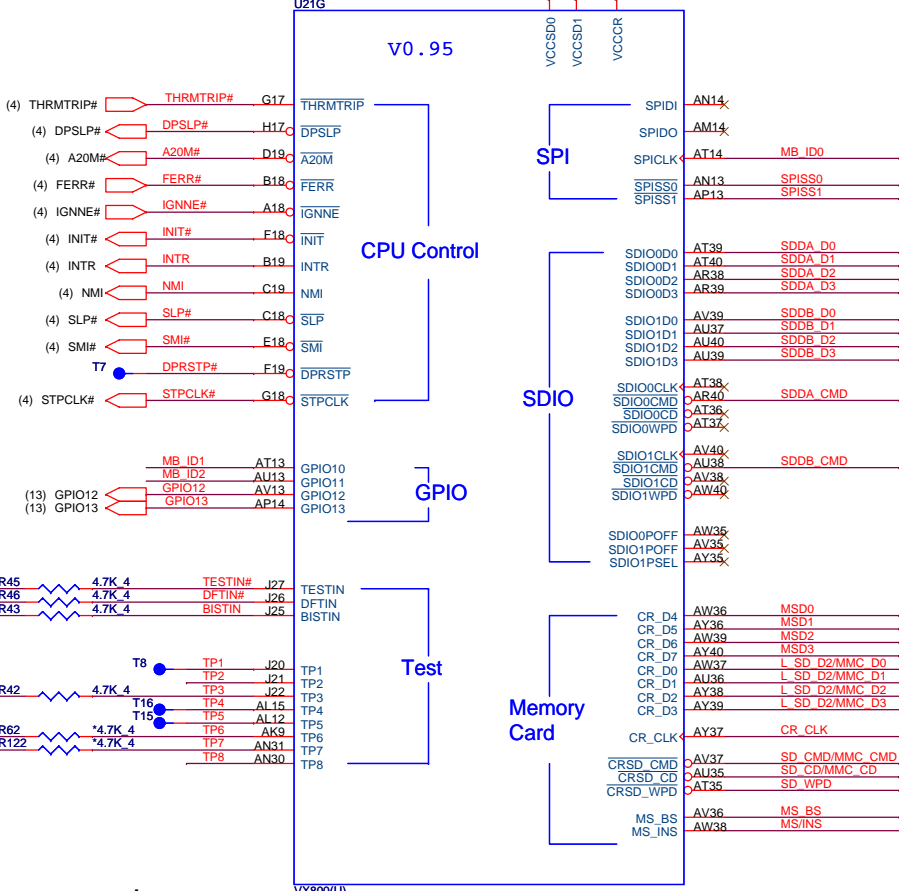
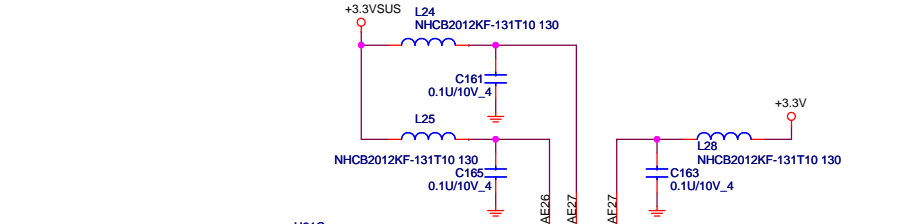
VCPD10	EXSR13[5]	CPUCK/MCK CLOCK Select	
[DCD#2]		*0 : from NB 1 : from external	
VCPD9	EXSR13[4]	PCI Signal test output enable	
[TD2]		*0 : Disable 1 : Enable	
VCPD7	EXSR13[0]	GFX CLOCK Select (VCK/LCDCK/ECK/TVCK)	
[CTS#1]		*0 : Refer internal 1 : From external	
VCPD6	EXSR12[6]	DVP0 port/Capture port select	
[RTS#1]		*0 : Capture port 1 : DVP0 port	





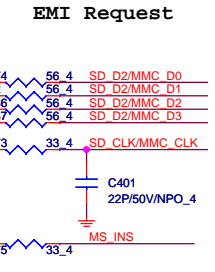
**PROJECT : IL1**  
**Quanta Computer Inc.**

Size A3	Document Number <b>VX800(U) VIDEO BUS</b>	Rev 1A
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**SB Strapping**

Pin	0:on 1:off	Function
SPISS1/ SPISS0 (2/1)	00	IDE
	01	NFC
	10	CE ATA

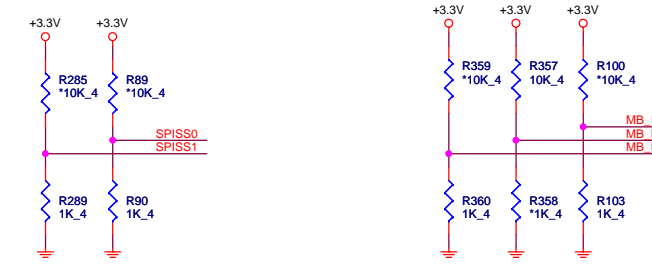


**TP2**

0 ( default )	Normal mode
1	Debug mode

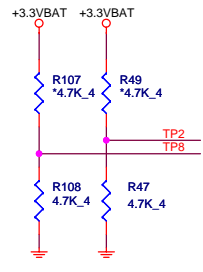
**TP8 ( SWMODE )**

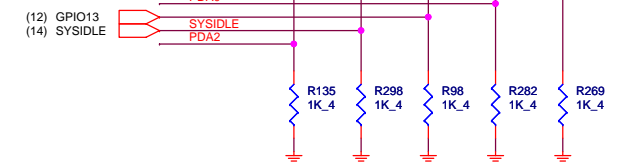
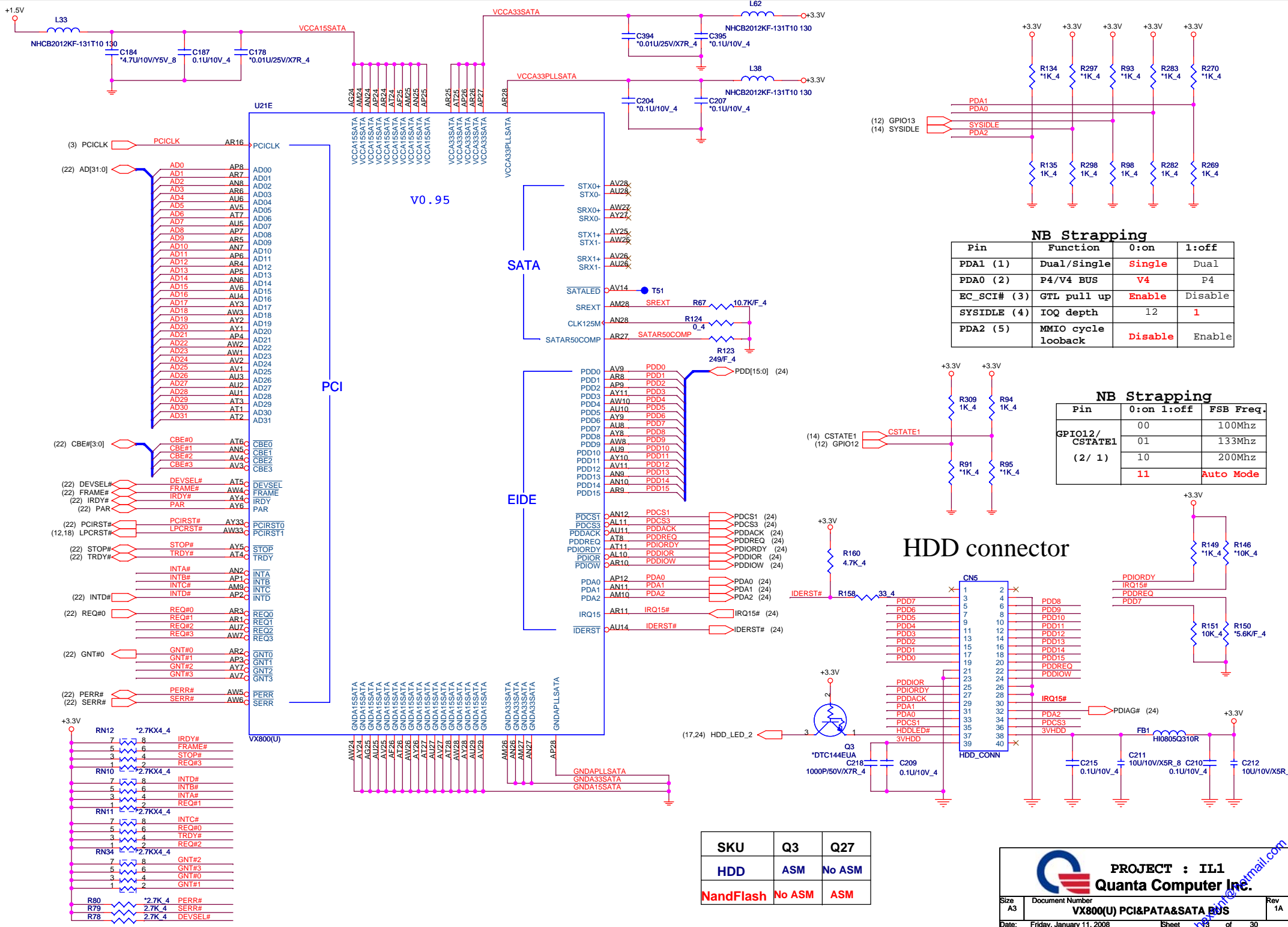
0 ( default )	Voltage mode
1	Current mode



**M/B ID Strapping**

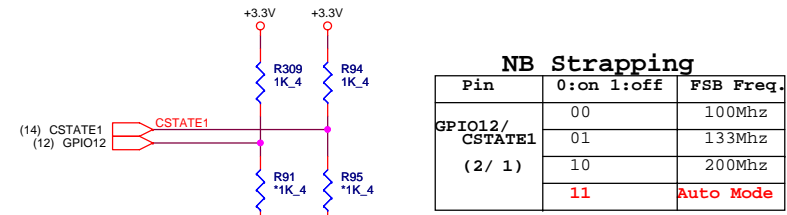
MBID	MB_ID2	MB_ID1	MB_ID0
A	0	0	0
B	0	0	1
C	0	1	0





### NB Strapping

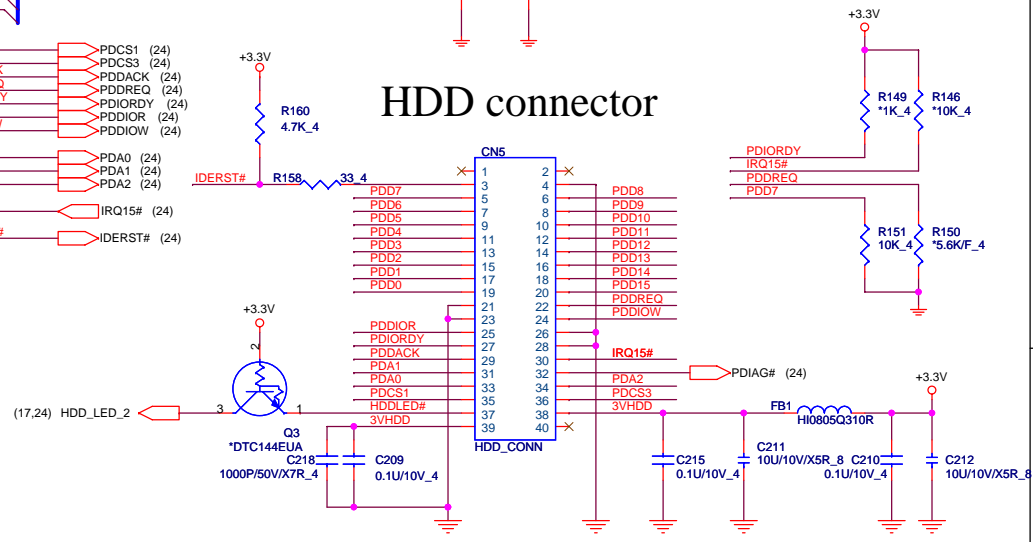
Pin	Function	0:on	1:off
PDA1 (1)	Dual/Single	Single	Dual
PDA0 (2)	P4/V4 BUS	V4	P4
EC_SCI# (3)	GTL pull up	Enable	Disable
SYSIDLE (4)	IOQ depth	12	1
PDA2 (5)	MMIO cycle looback	Disable	Enable




### NB Strapping

Pin	0:on	1:off	FSB Freq.
GPIO12/ CSTATE1 (2 / 1)	00		100Mhz
	01		133Mhz
	10		200Mhz
	11		Auto Mode

## HDD connector

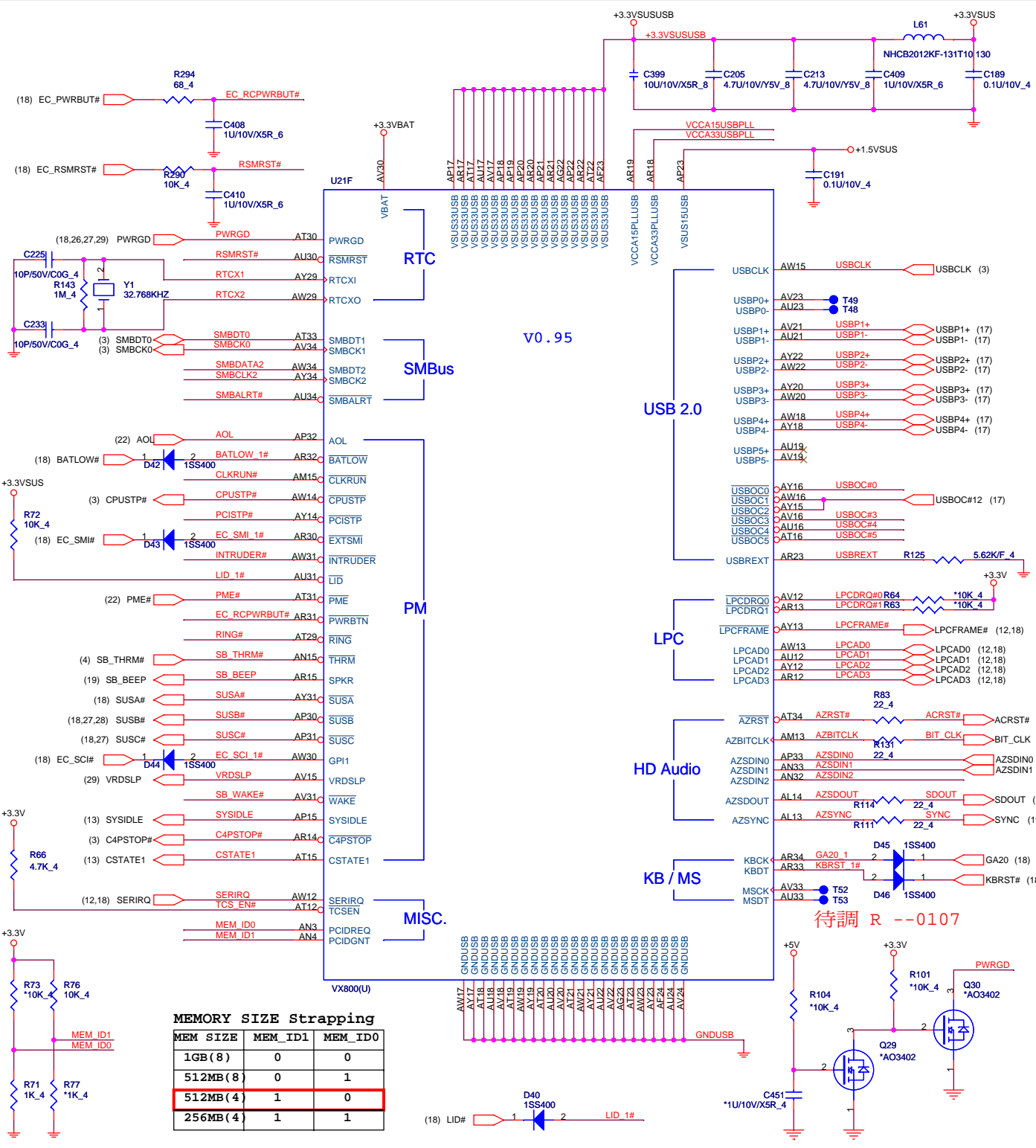


SKU	Q3	Q27
HDD	ASM	No ASM
NandFlash	No ASM	ASM



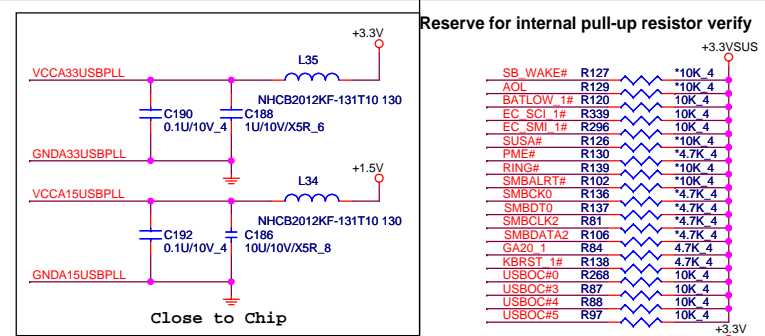
**PROJECT : IL1**  
**Quanta Computer Inc.**

Size A3	Document Number <b>VX800(U) PCI&amp;PATA&amp;SATA BUS</b>	Rev 1A
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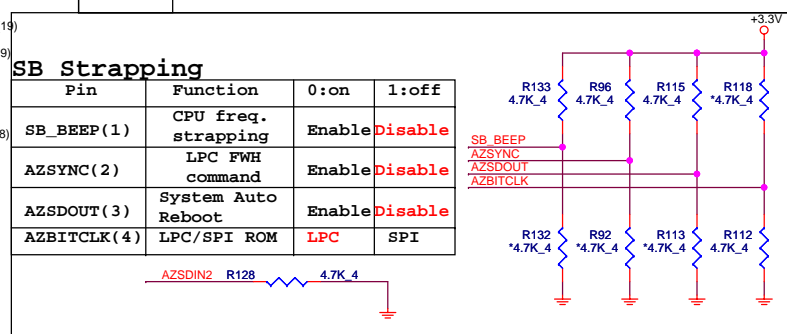
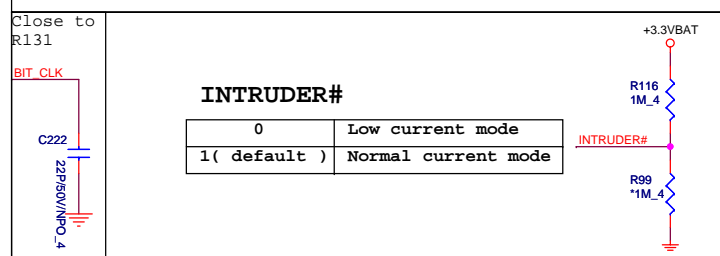
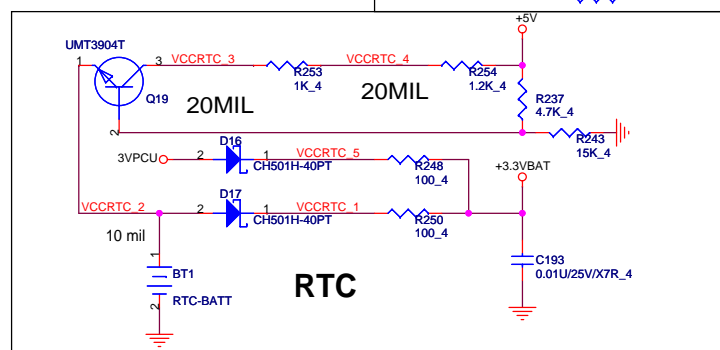


### MEMORY SIZE Strapping

MEM SIZE	MEM_ID1	MEM_ID0
1GB (8)	0	0
512MB (8)	0	1
512MB (4)	1	0
256MB (4)	1	1

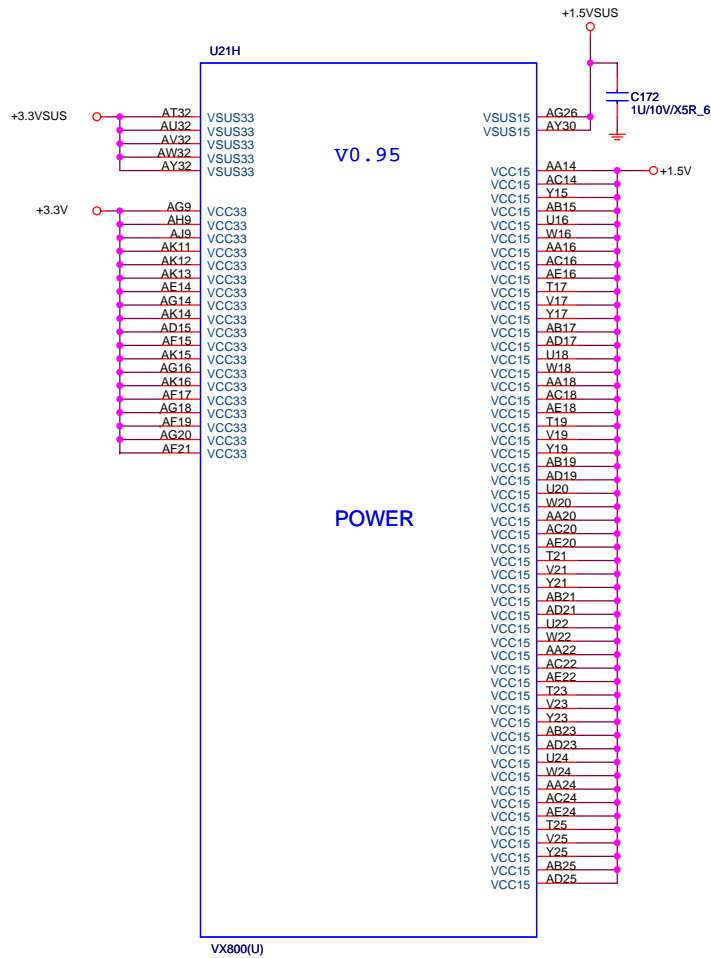


- Reserve for internal pull-up resistor verify
- SB\_WAKE# R127 \*10K 4
  - AOL R129 \*10K 4
  - BATLOW\_1# R120 \*10K 4
  - EC\_SCI\_1# R339 \*10K 4
  - EC\_SMI\_1# R296 \*10K 4
  - SUSA# R126 \*10K 4
  - PME# R130 \*4.7K 4
  - RING# R139 \*10K 4
  - SMBALRT# R102 \*10K 4
  - SMBCK0 R136 \*4.7K 4
  - SMBDT0 R137 \*4.7K 4
  - SMBCLK2 R81 \*4.7K 4
  - SMBDATA2 R106 \*4.7K 4
  - GA20\_1 R134 \*4.7K 4
  - KBRST\_1# R138 \*4.7K 4
  - USBOC#0 R268 \*10K 4
  - USBOC#3 R87 \*10K 4
  - USBOC#4 R88 \*10K 4
  - USBOC#5 R97 \*10K 4
  - SB\_THRM# R86 \*4.7K 4
  - SERIRQ R306 \*4.7K 4
  - PCISTP# R284 \*4.7K 4
  - CPUSTP# R267 \*4.7K 4
  - CLKRUN# R85 \*4.7K 4
  - VRDSLP R117 \*4.7K 4
  - C4PSTOP# R304 \*4.7K 4

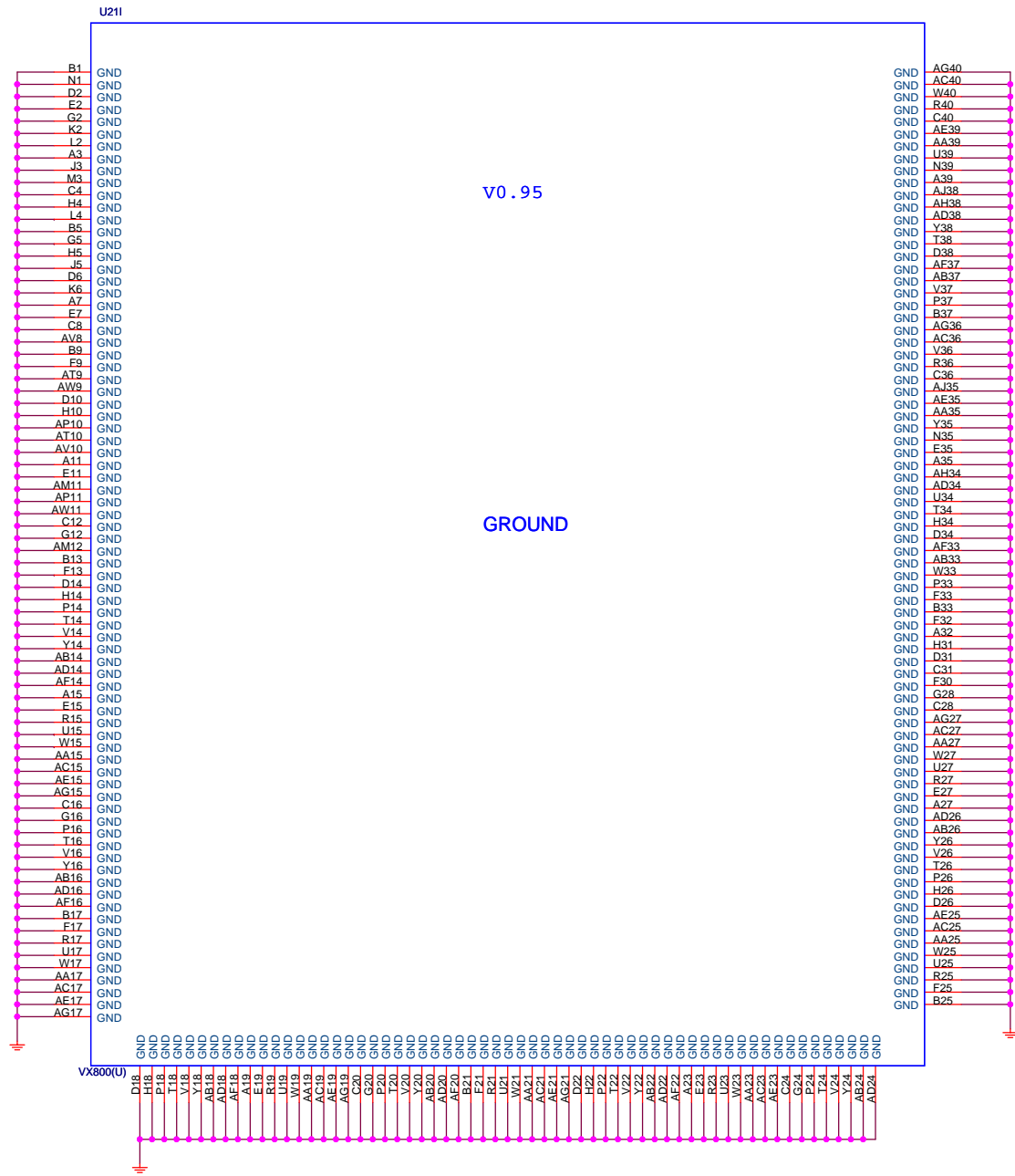
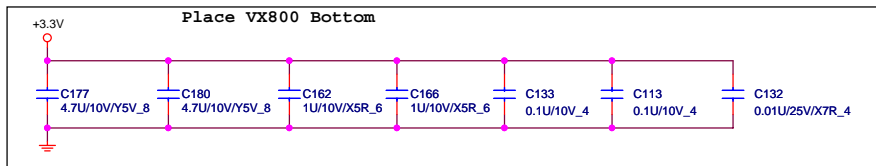
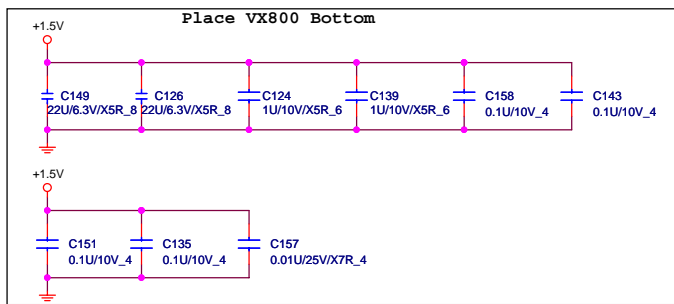


**PROJECT : IL1**  
**Quanta Computer Inc.**

Size A3	Document Number <b>VX800(U) USB&amp;LPC&amp;DAC&amp;PM</b>	Rev 1A
Date: Friday, January 11, 2008	Sheet 14 of 30	



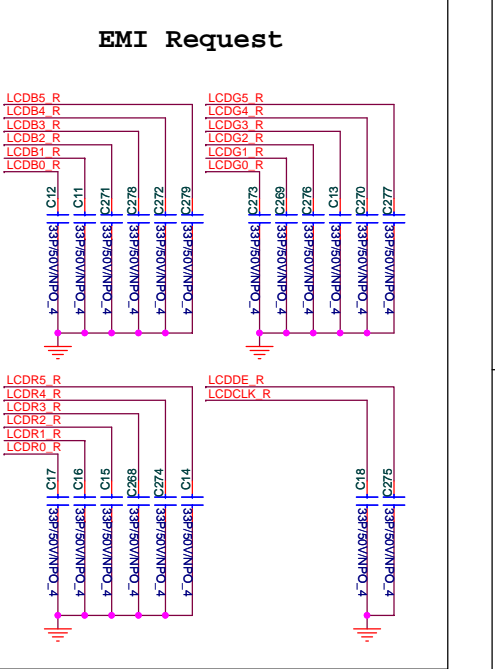
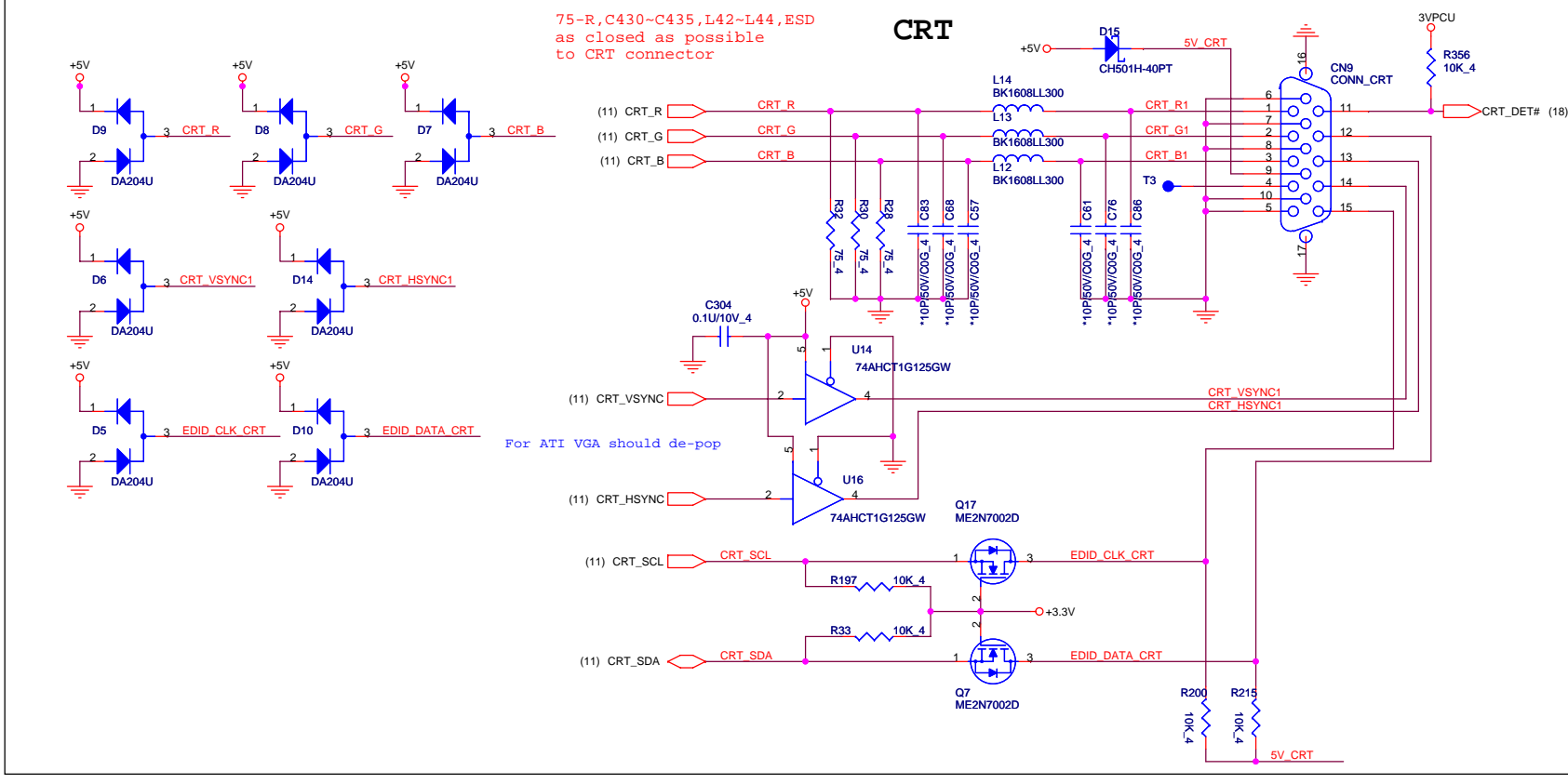
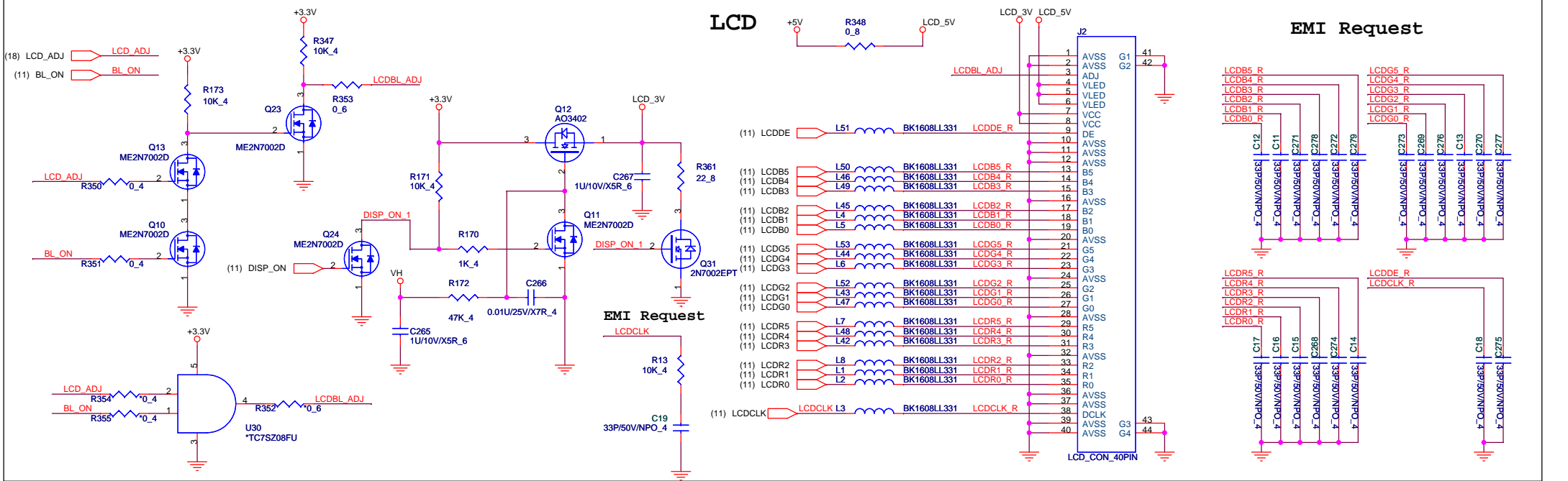
VX800(U)



VX800(U)

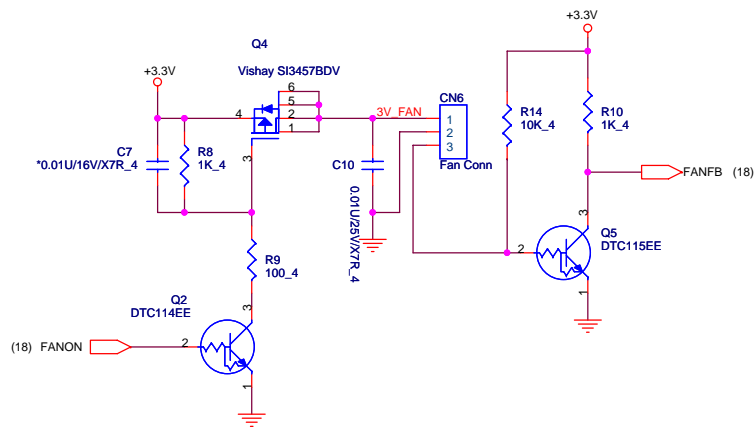
**PROJECT : IL1**  
**Quanta Computer Inc.**

Size A3	Document Number <b>VX800(U) POWER&amp;GND</b>	Rev 1A
Date: Friday, January 11, 2008	Sheet 1 of 30	

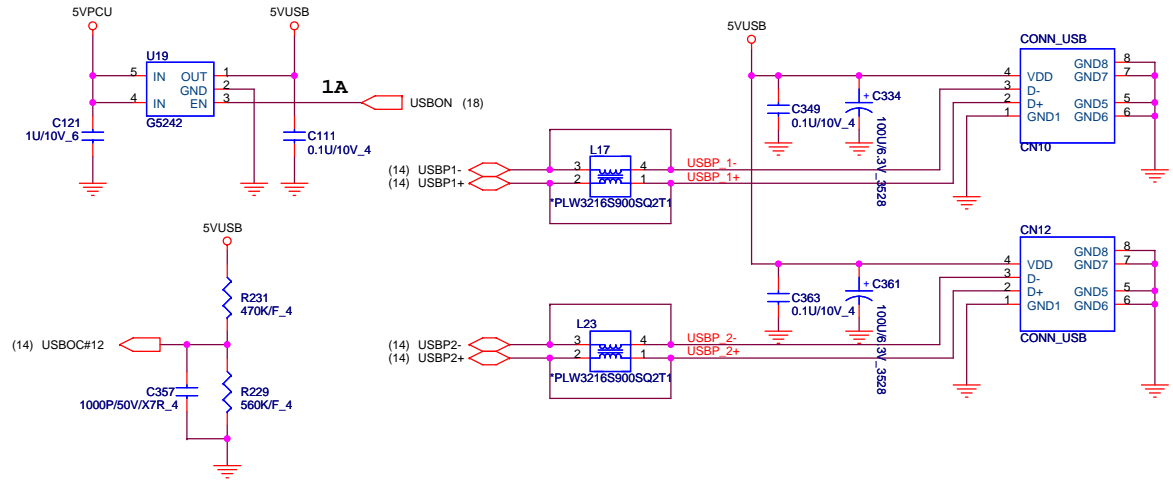




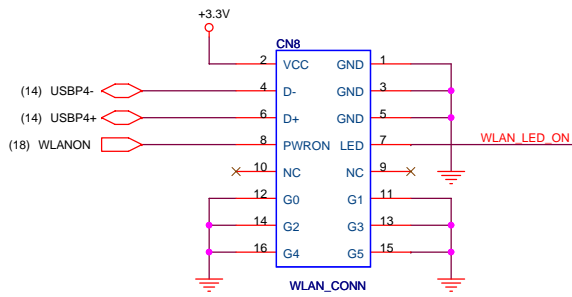
# FAN



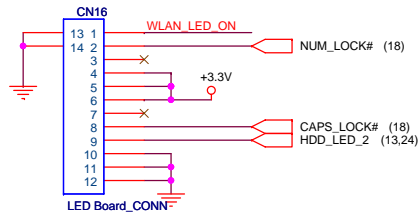
# USB X 2 PORTS



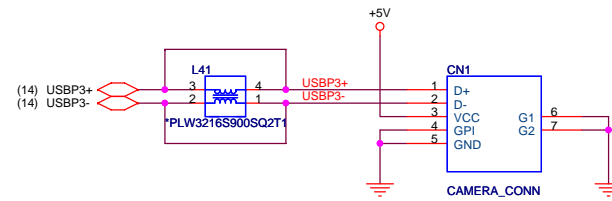
# WLAN

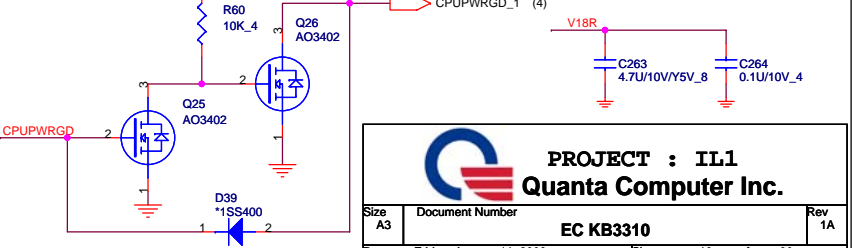
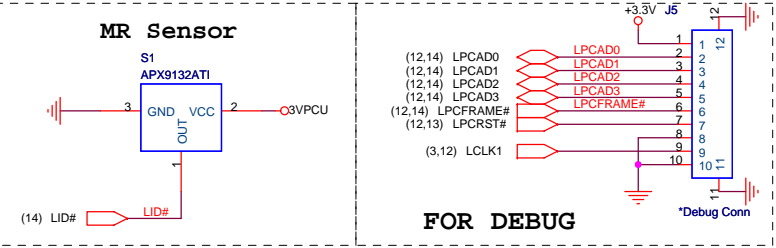
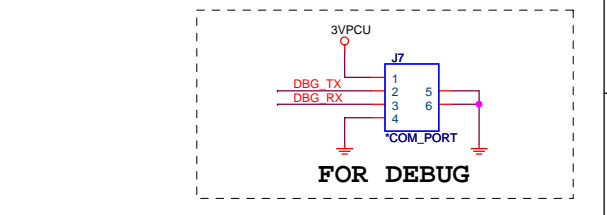
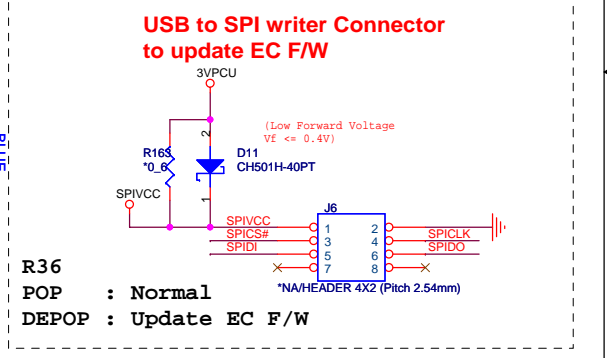
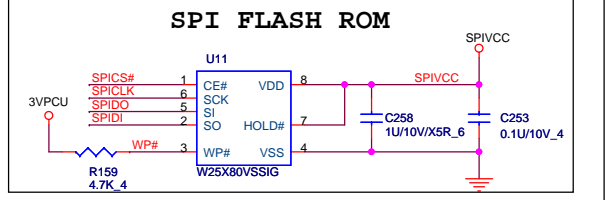
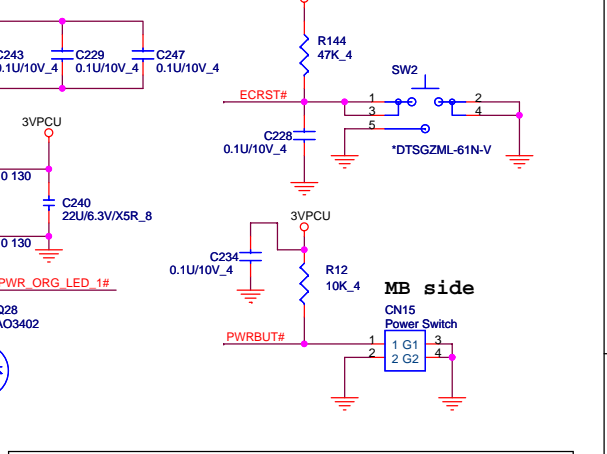
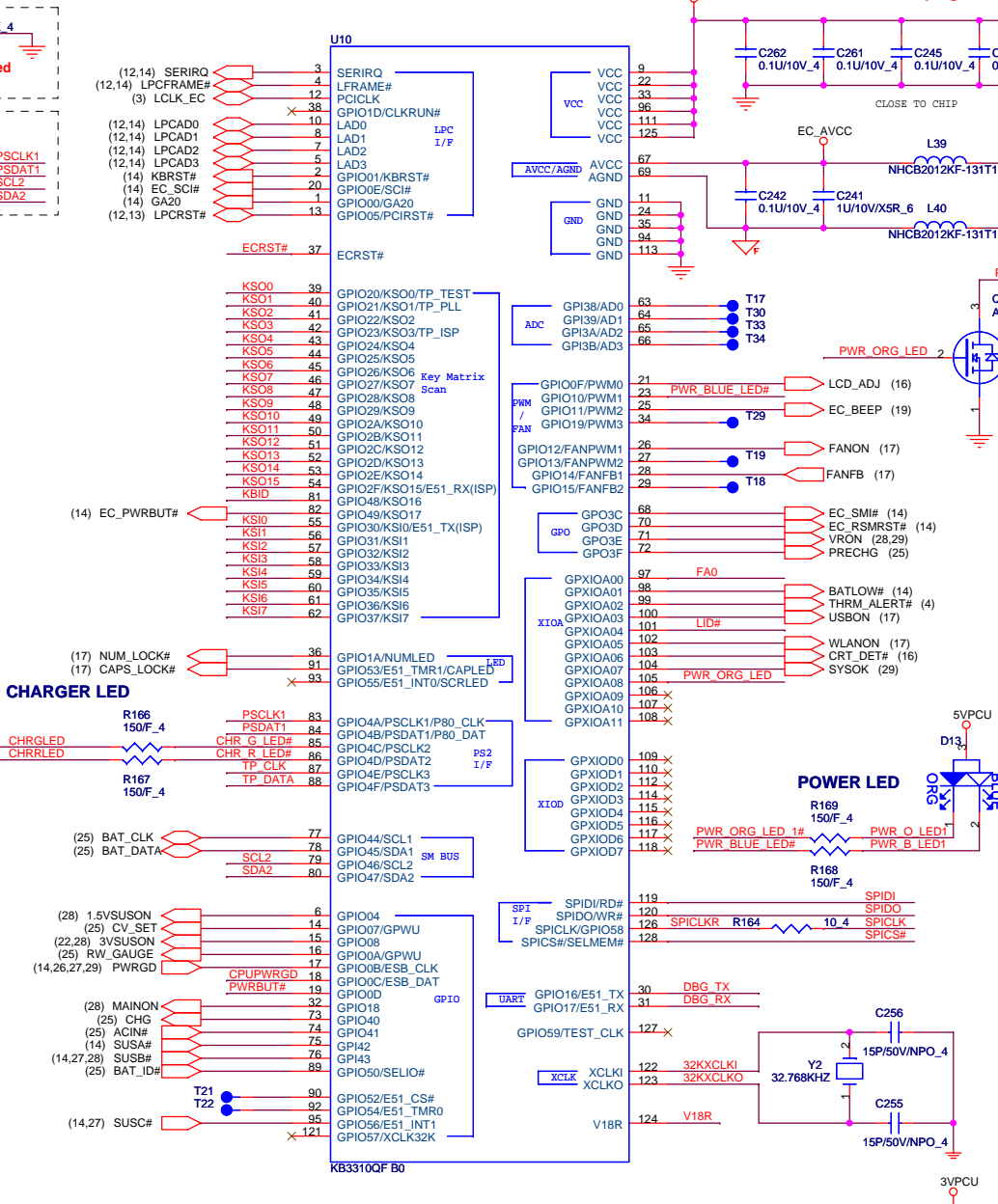
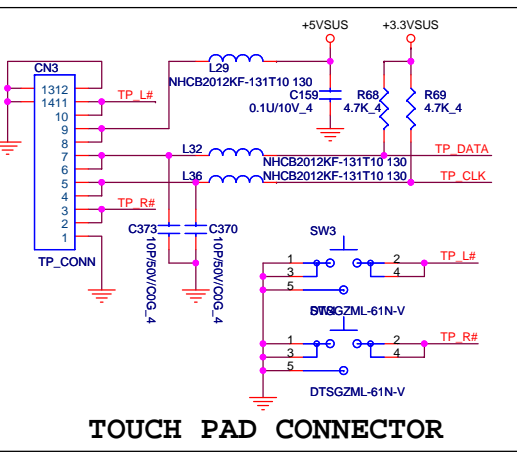
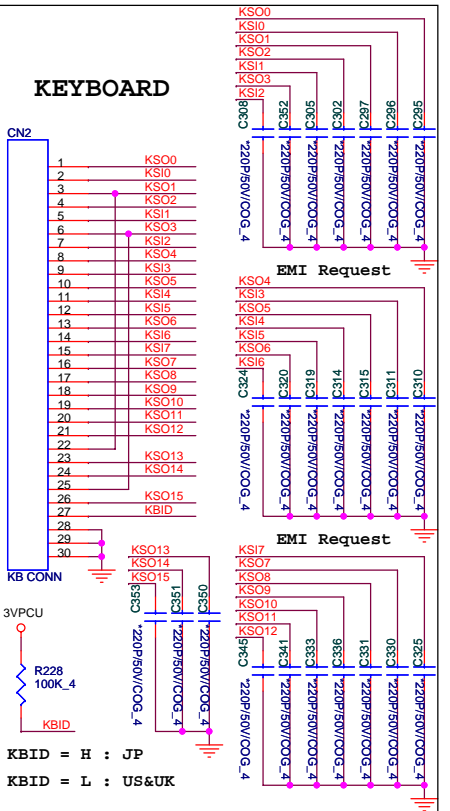
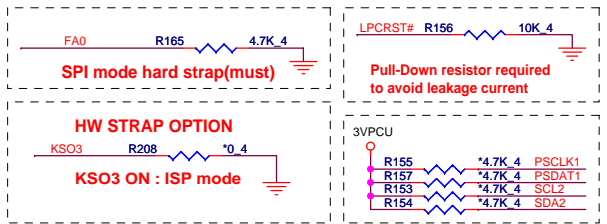


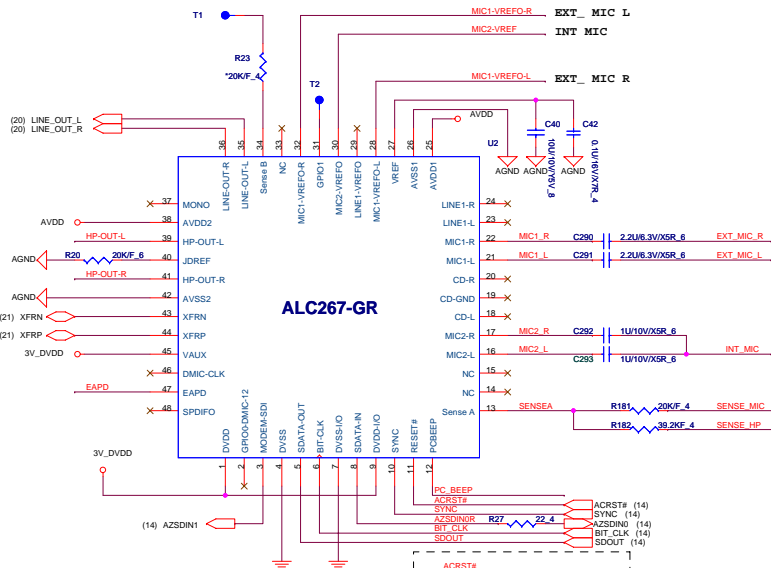
# LED Board



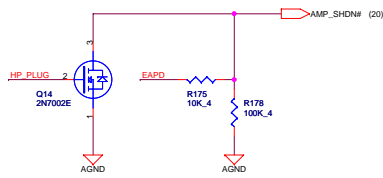
# CAMERA



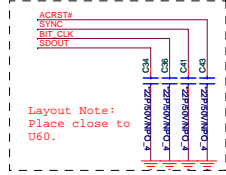
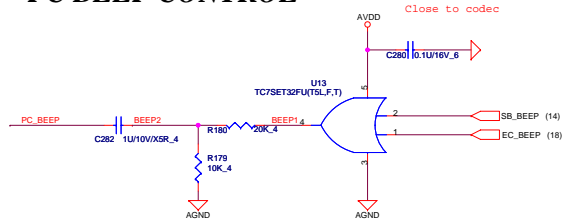




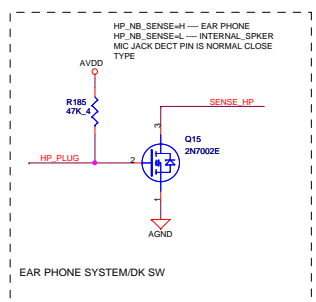
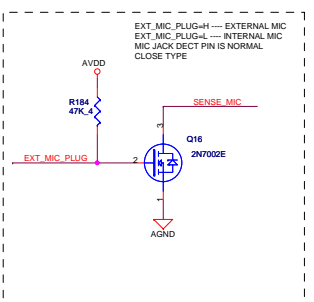
HP_PLUG	EAPD	AMP_SHDN#
0	0	0
0	1	1
1	0	0
1	1	0



### PC BEEP CONTROL

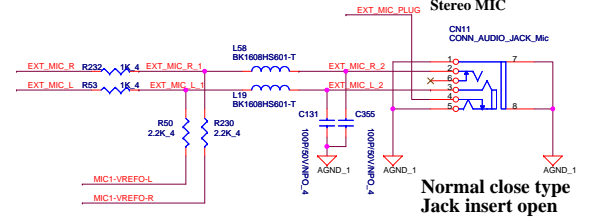


Layout Note:  
Place close to U60.

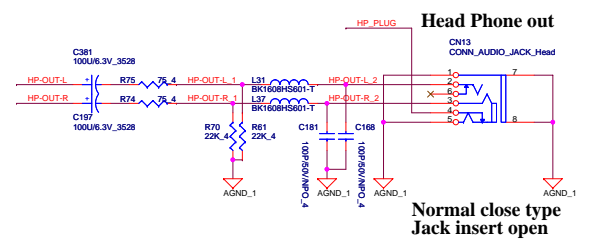


EAR PHONE SYSTEM/CLK SW

### External Microphone Jack

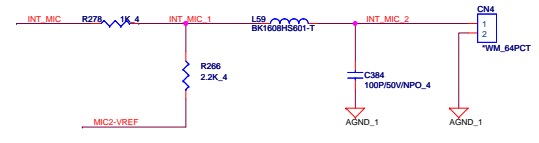


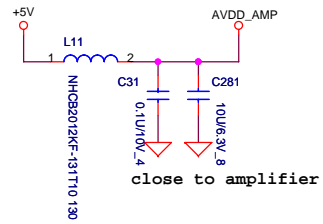
Normal close type  
Jack insert open



Normal close type  
Jack insert open

### INT\_MIC





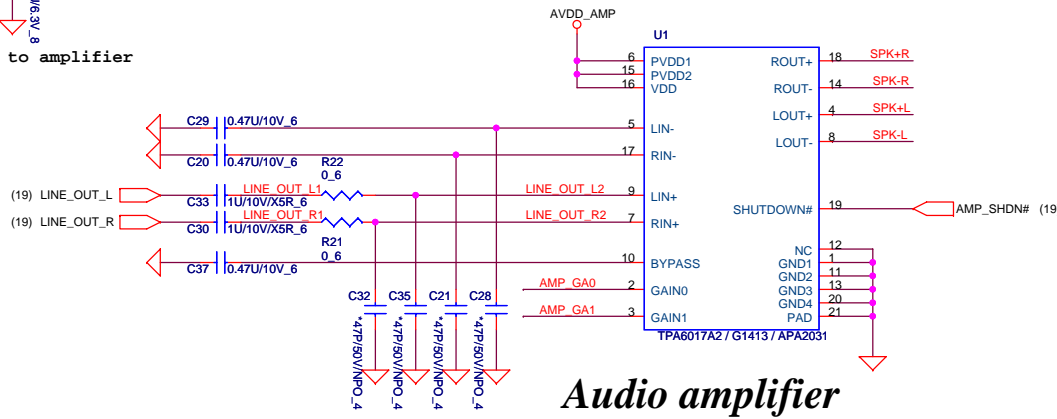
### Full Scale Output Voltage

LINE - OUT ----- 1.4Vrms/Typical

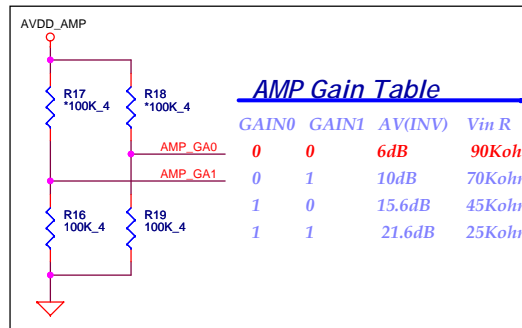
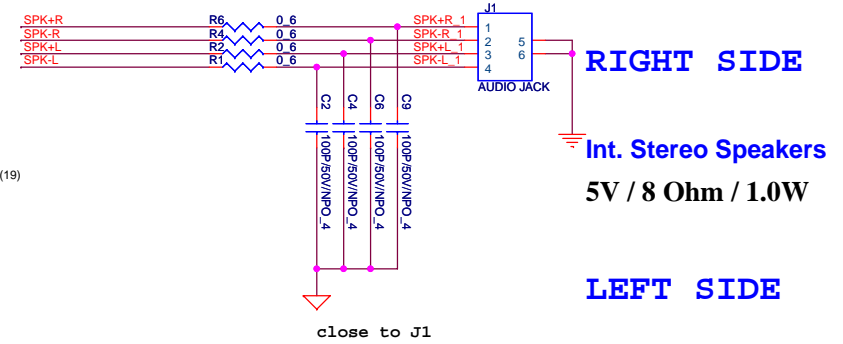
HP - OUT ----- 1.4Vrms/Typical

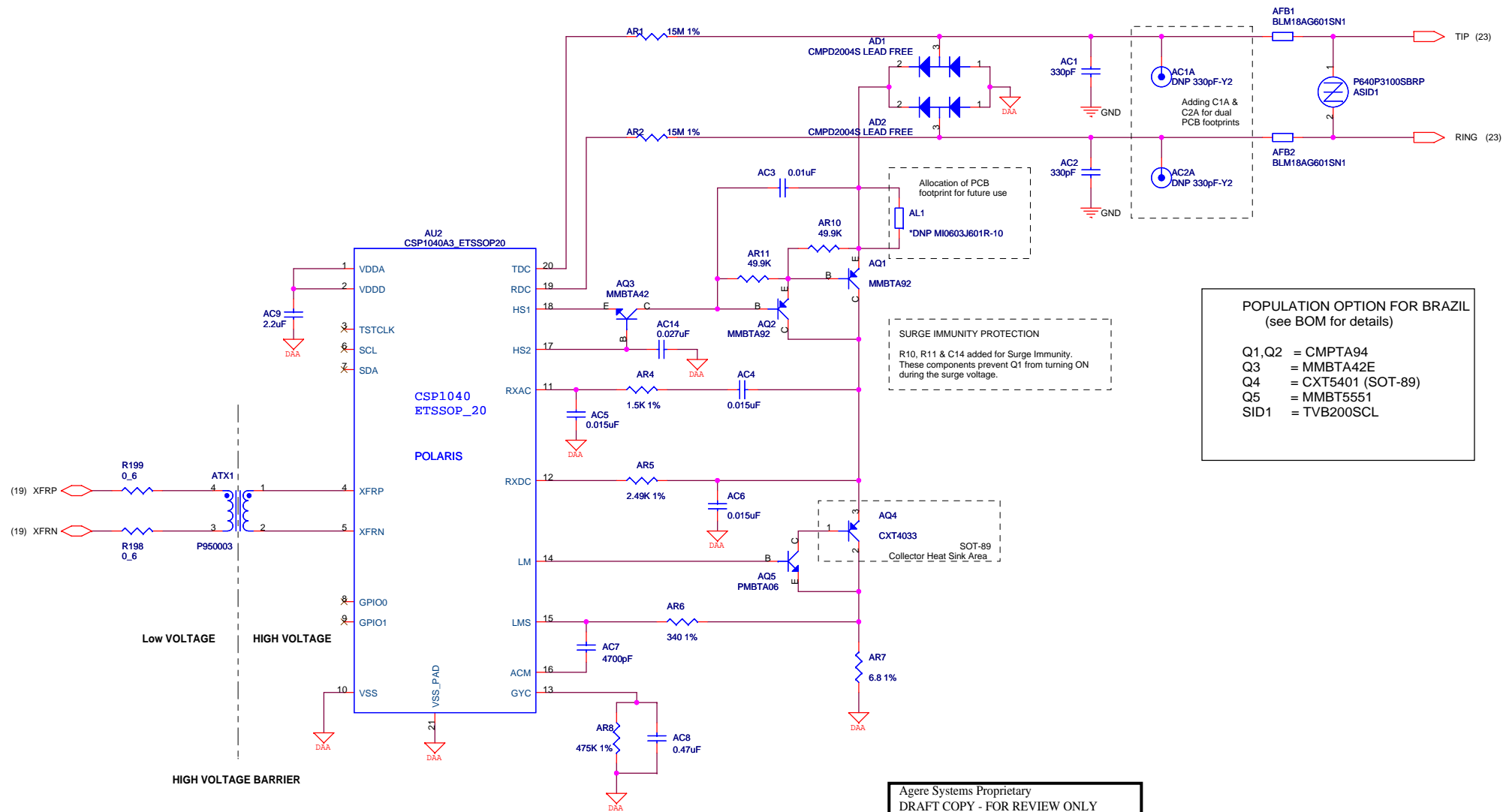
Step Size = 1.0 dB / 0 ~ - 64 dB / Total 64 Step

Gain = 6 dB / Input = 1.4Vrms (0dB) / Output = 2.794Vrms / Speaker 0.976W



### Audio amplifier



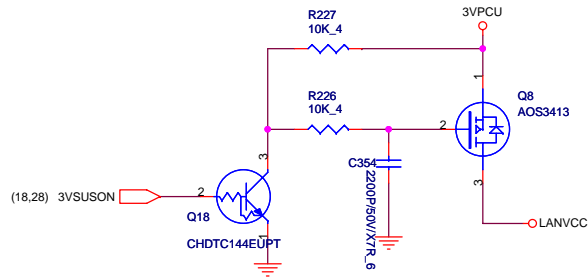


**POPULATION OPTION FOR BRAZIL**  
(see BOM for details)

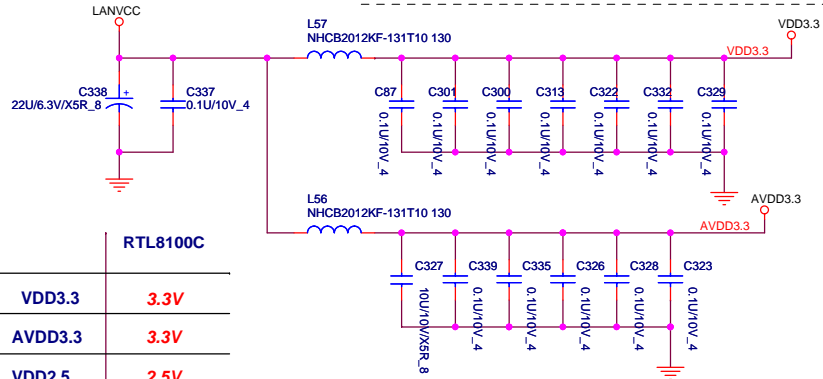
- Q1, Q2 = CMPTA94
- Q3 = MMBTA42E
- Q4 = CXT5401 (SOT-89)
- Q5 = MMBT5551
- SID1 = TVB200SCL

Agere Systems Proprietary  
DRAFT COPY - FOR REVIEW ONLY  
SUBJECT TO CHANGE

		<b>PROJECT : IL1</b>	
		<b>Quanta Computer Inc.</b>	
Size A3	Document Number <b>MODEM</b>	Rev 1A	
Date: Friday, January 11, 2008	Sheet 1	of 30	

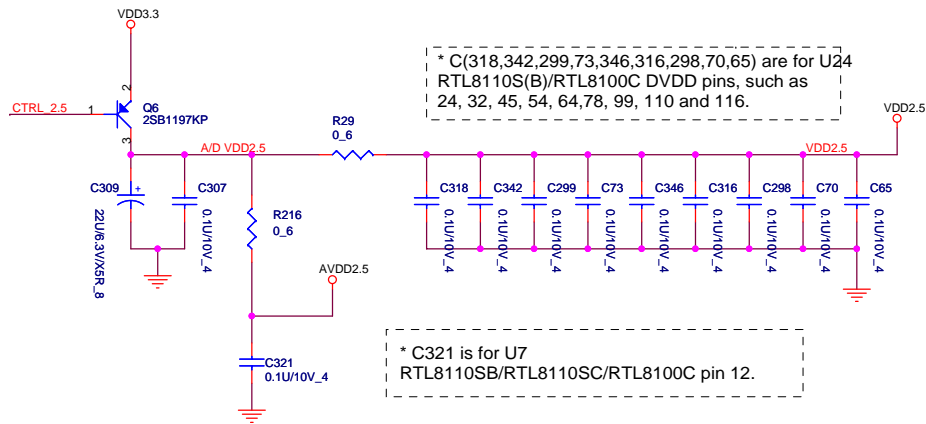


\* C(87,301,300,313,322,332,329) are for U24 RTL8110S(B/C)/RTL8100C VDD33 pins, such as 26, 41, 56, 71, 84, 94 and 107.



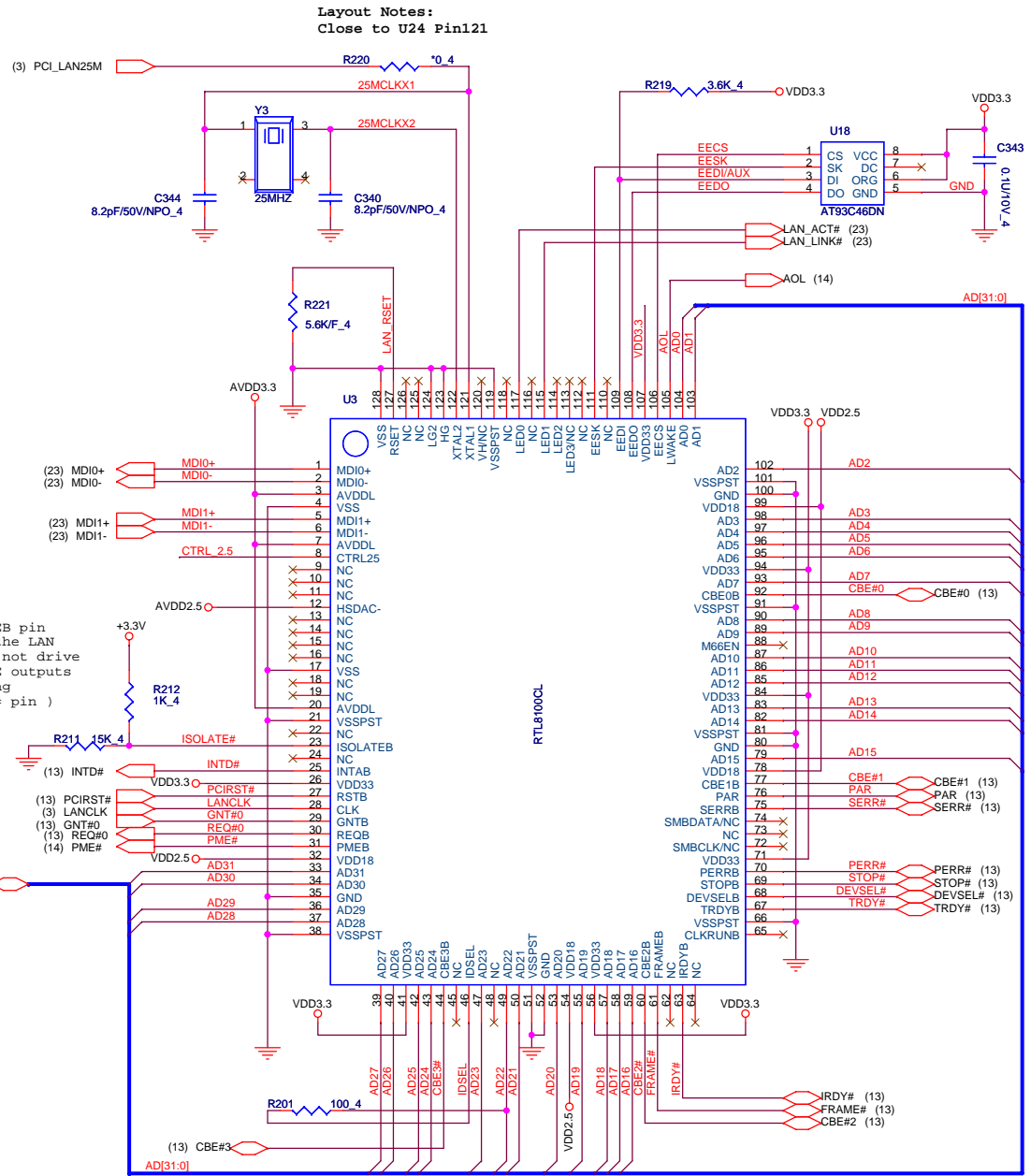
RTL8100C	
VDD3.3	3.3V
AVDD3.3	3.3V
VDD2.5	2.5V
AVDD2.5	2.5V

\* C(327,339,335,326,328,323) are for U24 RTL8110S(B/C)/RTL8100C AVDDL pins, such as 3, 7, 16, and 20.



\* C(318,342,299,73,346,316,298,70,65) are for U24 RTL8110S(B)/RTL8100C DVDD pins, such as 24, 32, 45, 54, 64, 78, 99, 110 and 116.

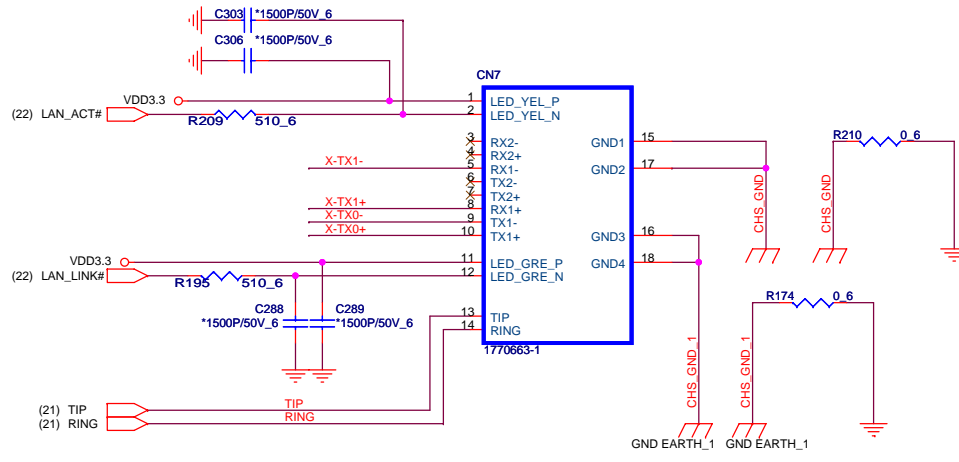
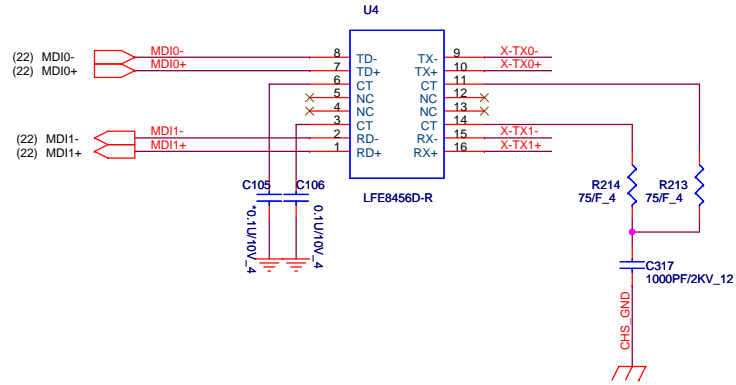
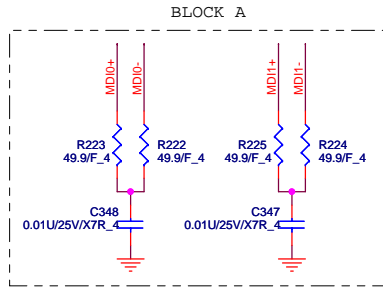
\* C321 is for U7 RTL8110SB/RTL8110SC/RTL8100C pin 12.

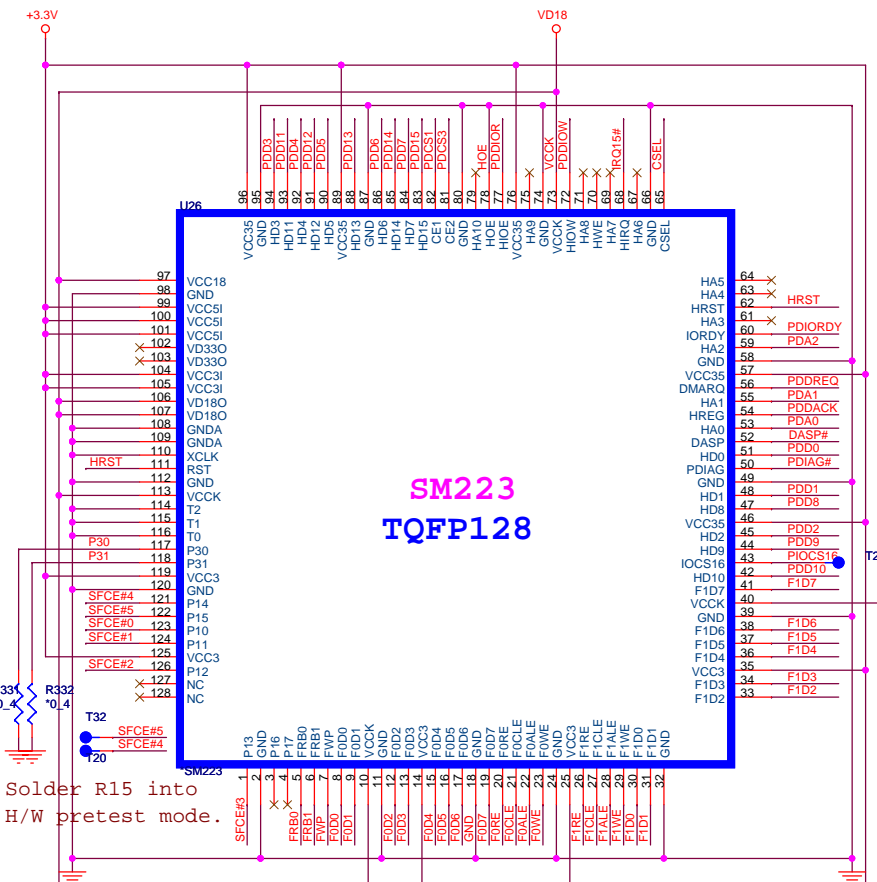
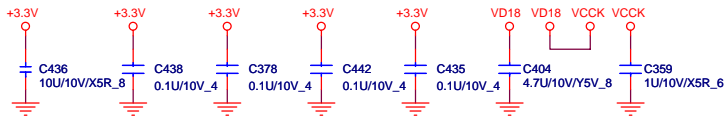


Layout Notes:  
Close to U24 Pin121

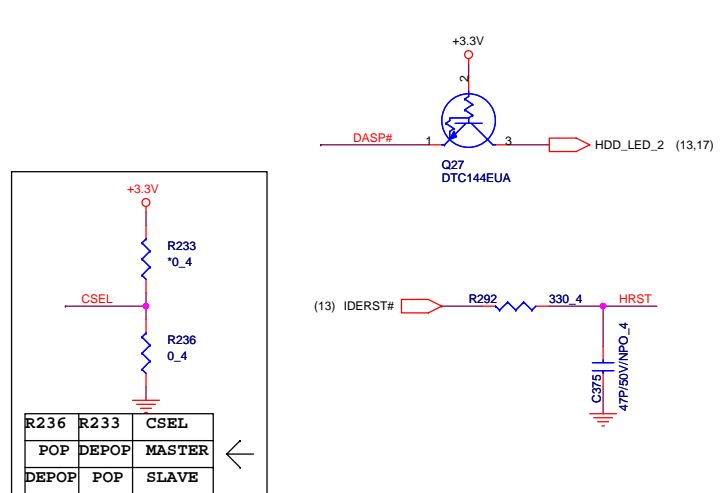
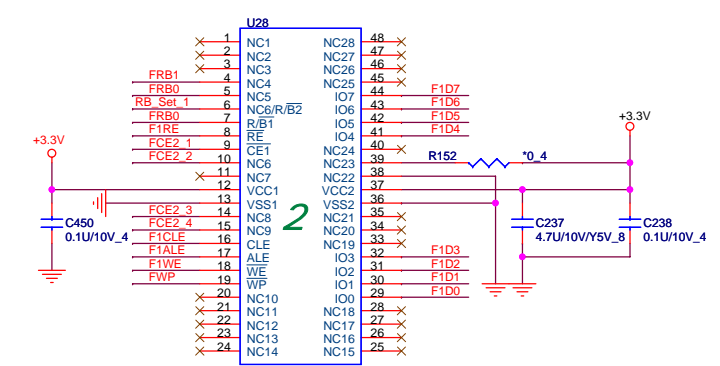
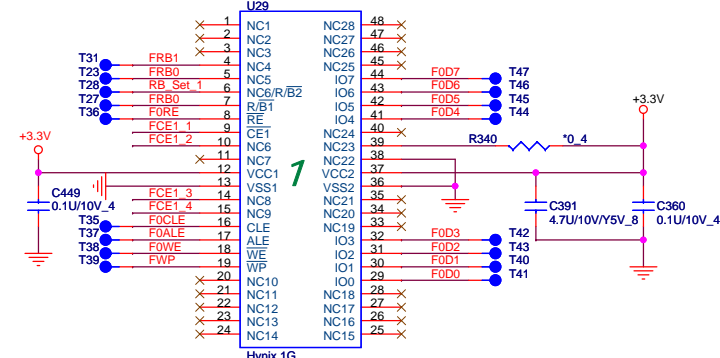
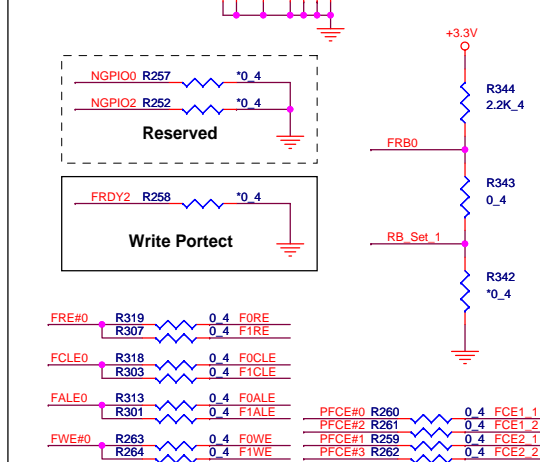
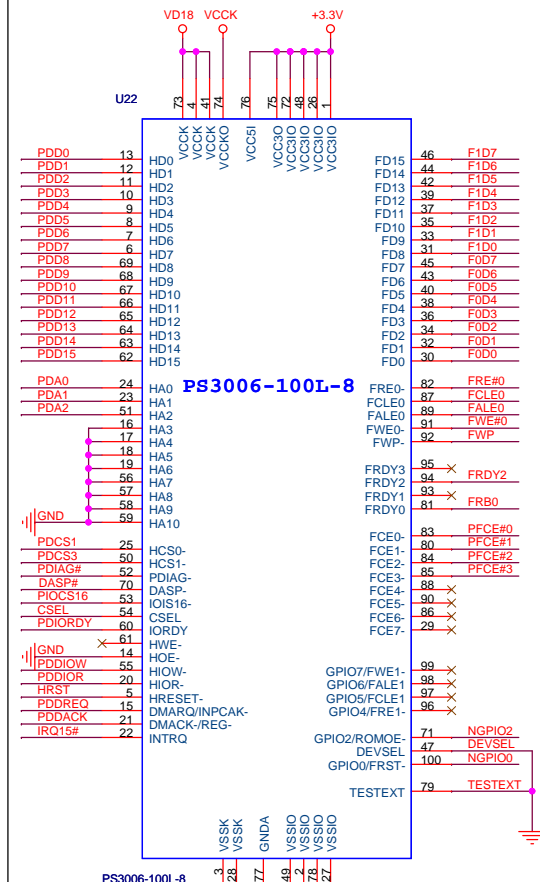
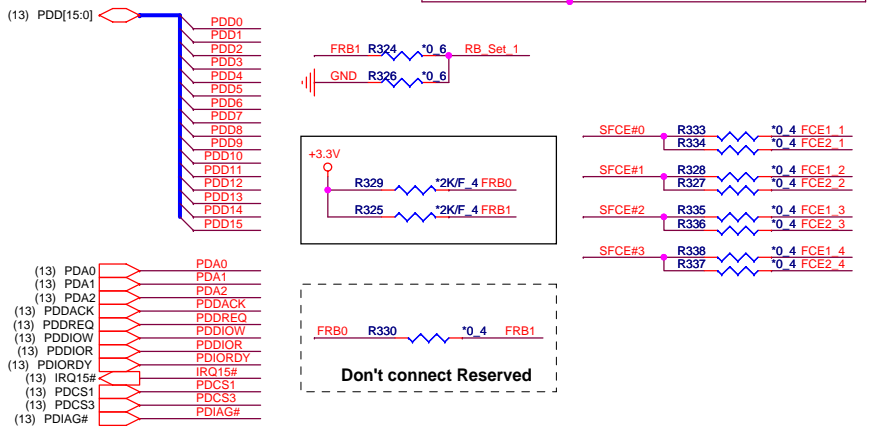
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE\_WAKE# pin)

PCI-IDSEL:  
INTD & AD22



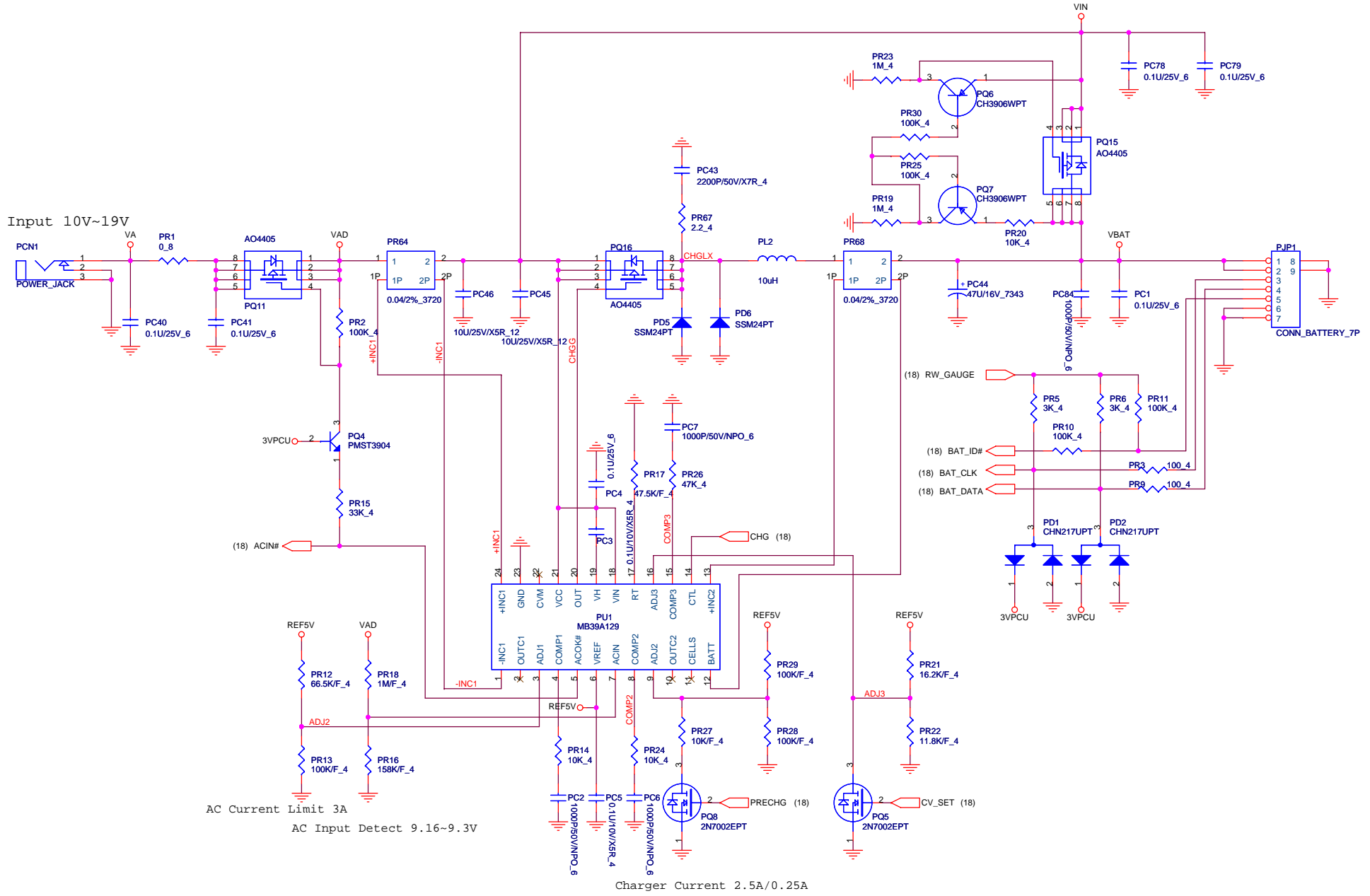


Solder R15 into H/W pretest mode.





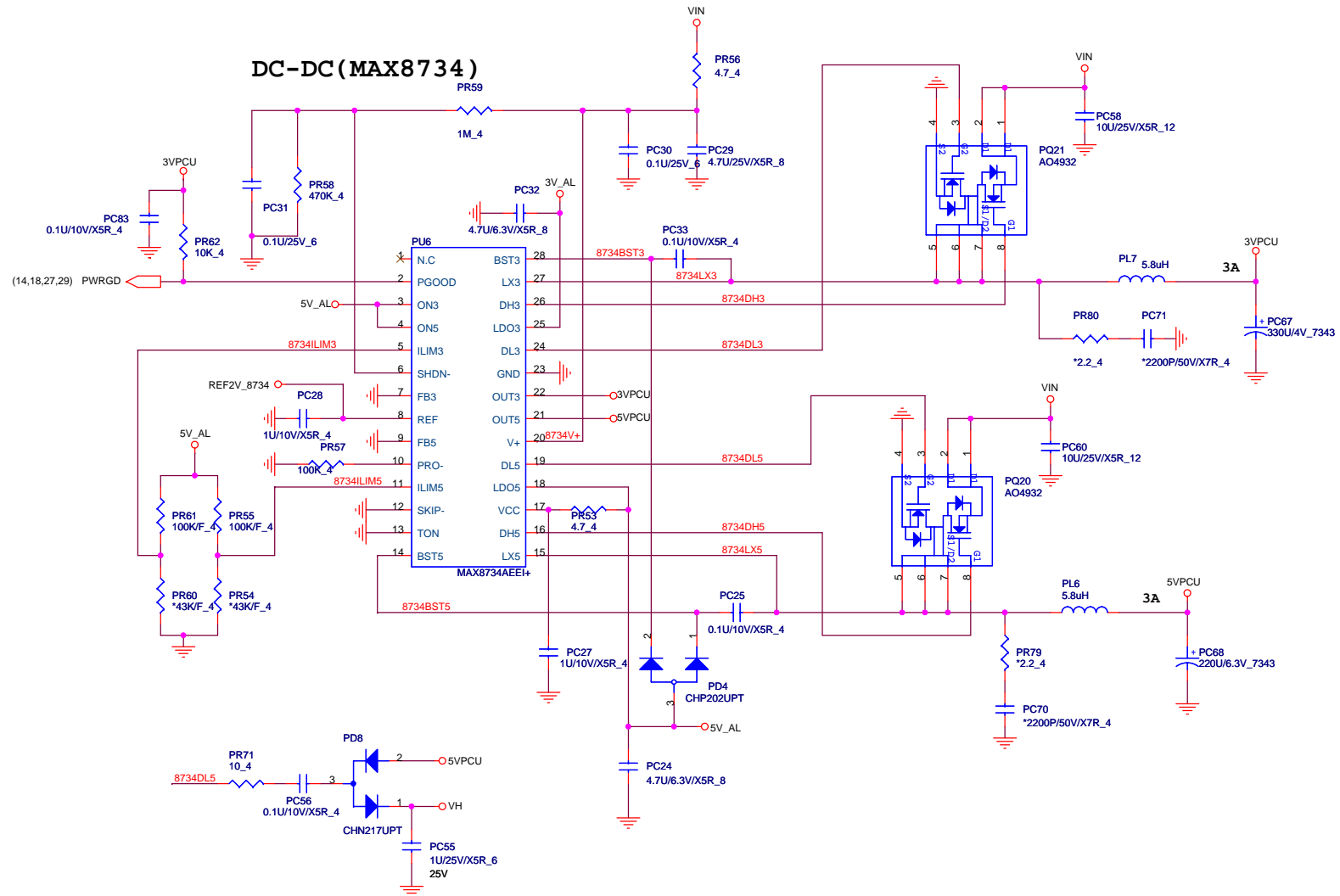
Input 10V~19V




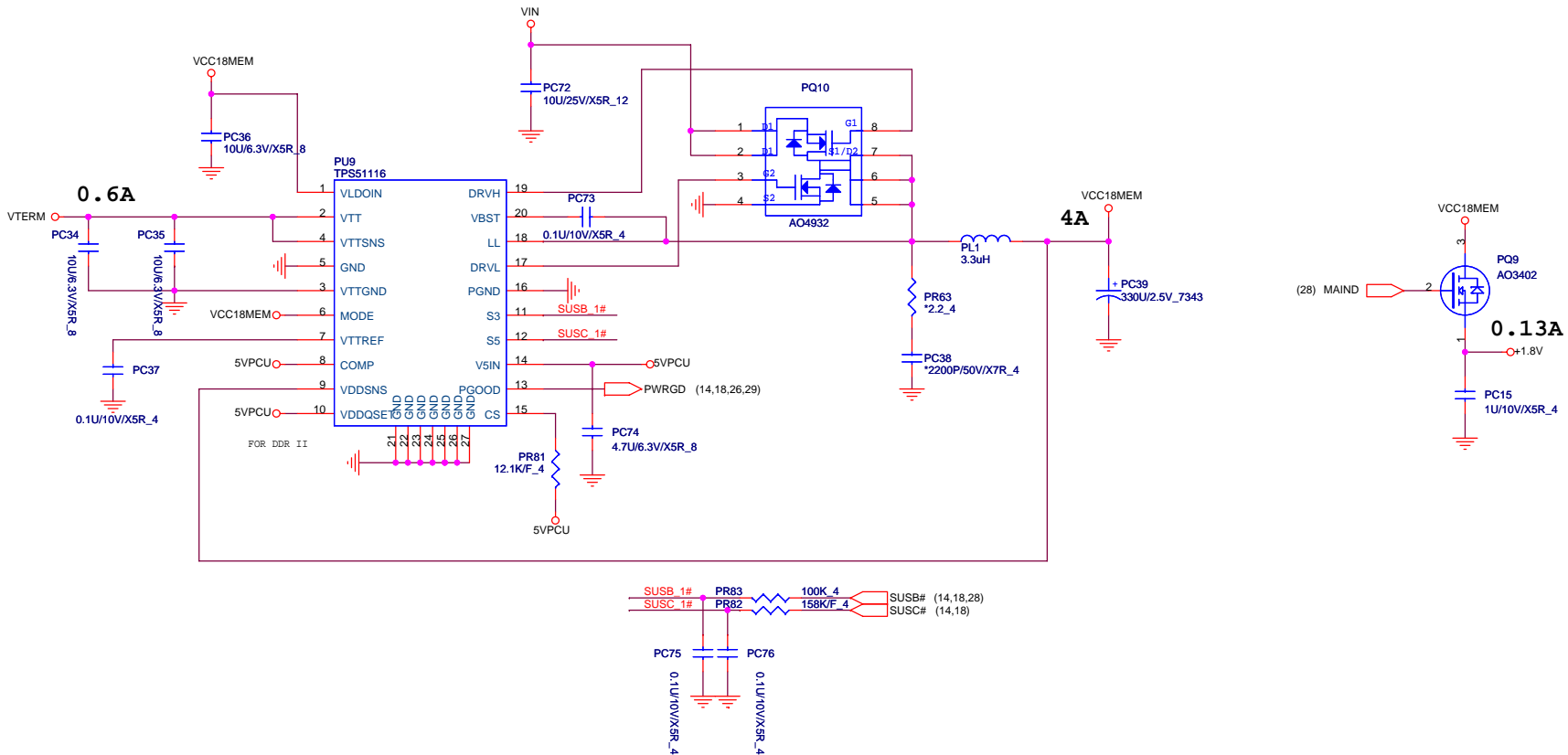
AC Current Limit 3A  
 AC Input Detect 9.16~9.3V

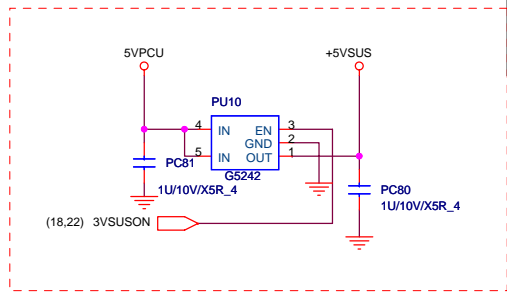
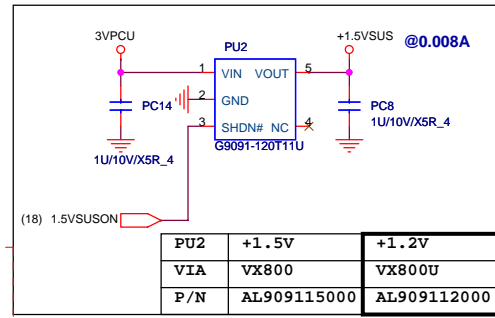
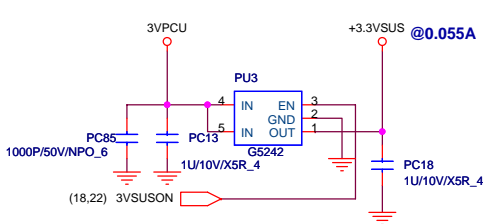
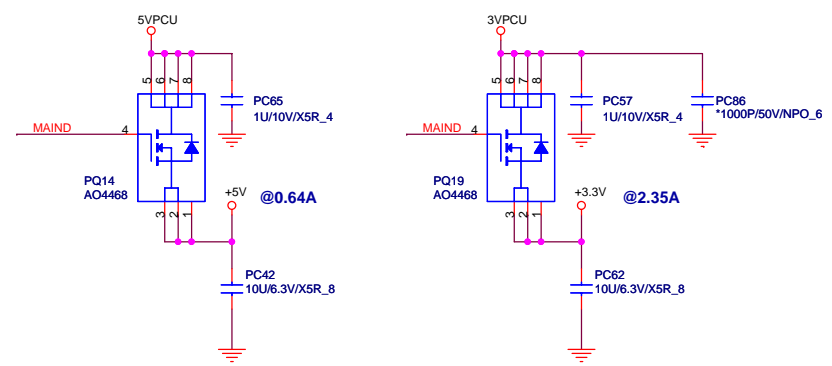
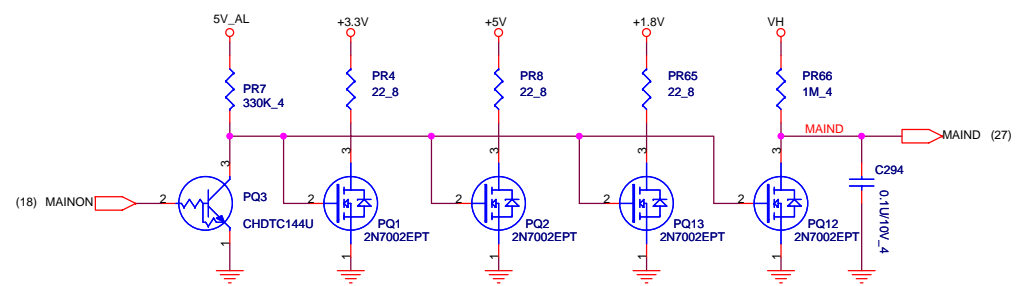
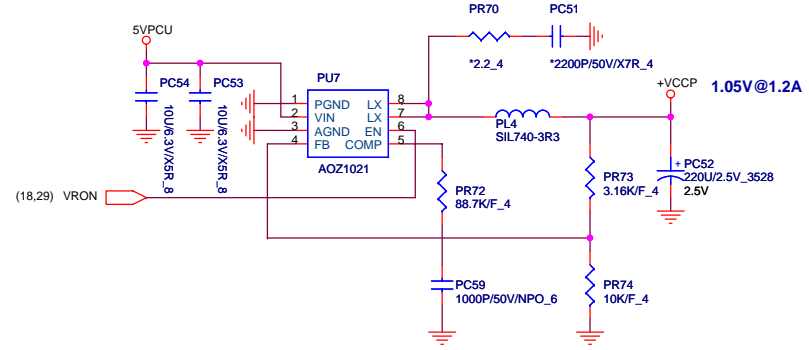
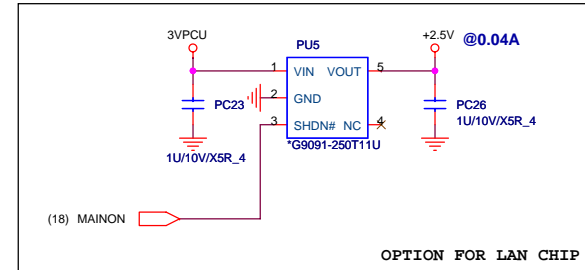
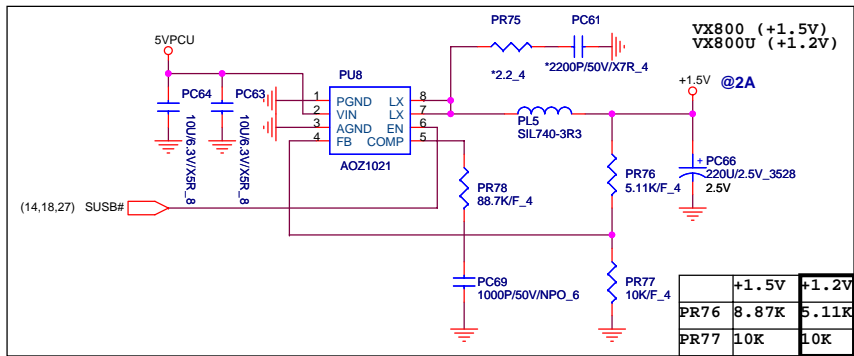
Charger Current 2.5A/0.25A

# DC-DC (MAX8734)



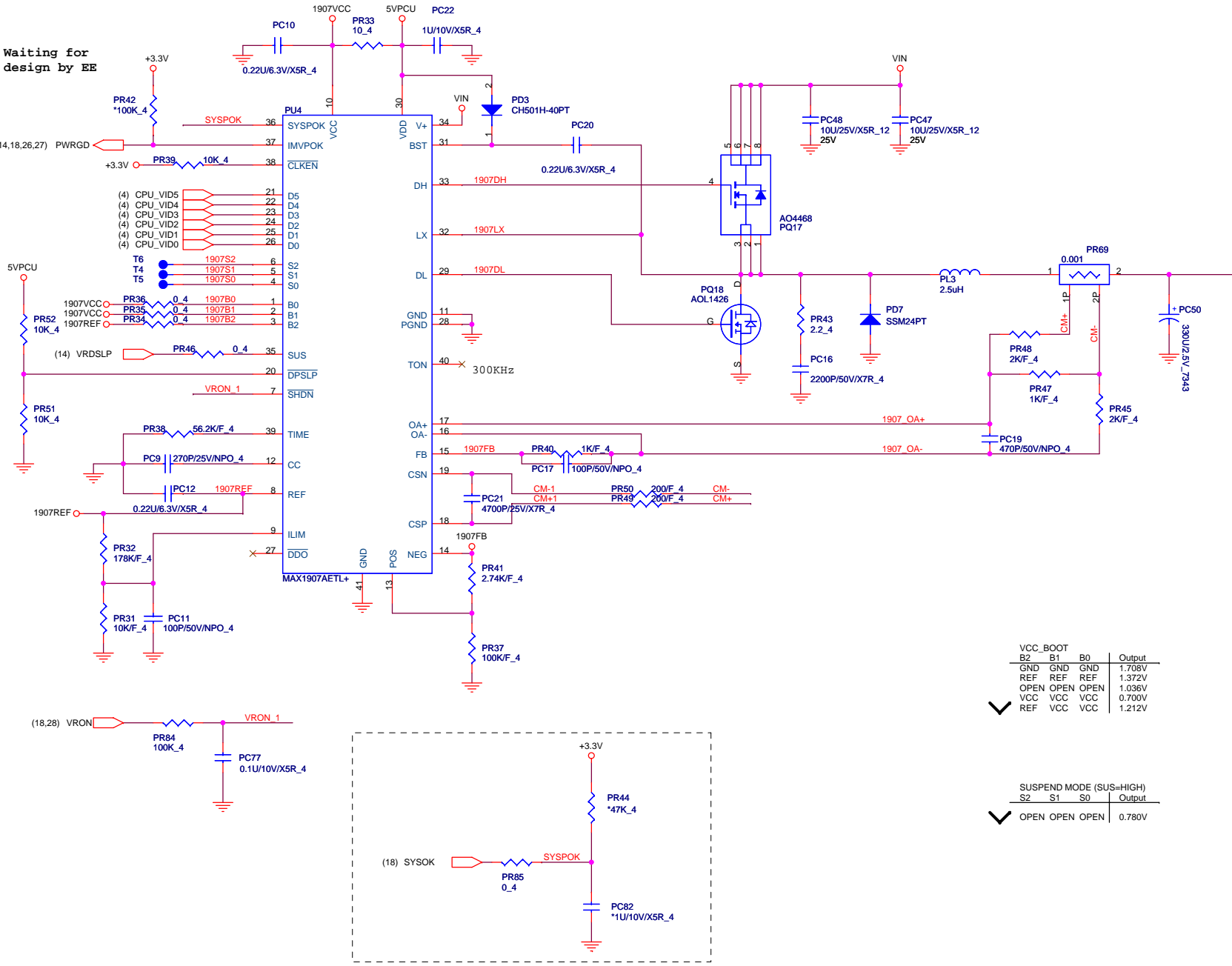
 <b>PROJECT : IL1</b> <b>Quanta Computer Inc.</b>		Rev
		1A
Size	Document Number	<b>DC/DC 5V/3.3V (MAX8734)</b>
A3		
Date:	Friday, January 11, 2008	Sheet
		26 of 30





# CPU CORE(MAX1907)

Waiting for design by EE



VCC_BOOT	B2	B1	B0	Output
GND	GND	GND	GND	1.708V
REF	REF	REF	REF	1.372V
OPEN	OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	VCC	0.700V
REF	VCC	VCC	VCC	1.212V

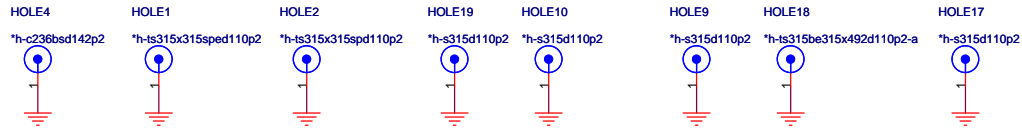
SUSPEND MODE (SUS=HIGH)	S2	S1	S0	Output
OPEN	OPEN	OPEN	OPEN	0.780V

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	1	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	1	0	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	1	1	0	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	1	1	1.052V	0	0	0	1	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	1	0	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	1	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

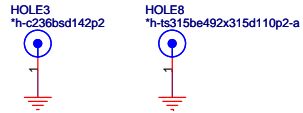
**PROJECT : IL1**  
**Quanta Computer Inc.**

Size A3 Document Number **DC/DC CPU CORE (MAX1907A)** Rev 1A  
 Date: Friday, January 11, 2008 Sheet 29 of 30

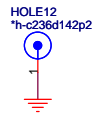
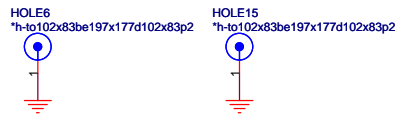
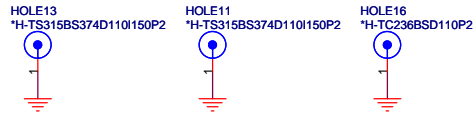
# SCREW HOLE



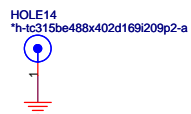
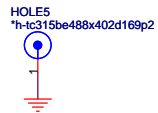
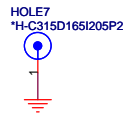
## Mount NUT - TOP




## Mount NUT - TOP



## Mount NUT - BOT



		<b>PROJECT : IL1</b>	
		<b>Quanta Computer Inc.</b>	
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