1. It is extremely important for each group to bring the following

1- Page 2 of this document printed and filled in with the group #, names of the students, their sections, their ID's (رقم الجلوس). Do not fill other empty cells in the table.
2- Your report, which includes
    a. Complete analysis including drawing, K-Map, unused states analysis,…etc.
    b. Complete Verilog Code with a print out (screen snap-shot) of the simulation output.
3- A softcopy of the Verilog Code to test it on a machine.
4- Your hardware implementation on a Breadboard.
5- Any document that you used or helped you to implement your project, e.g., data sheets, schematic diagrams, etc.

2. The groups should attend according to the following schedule

	8:30 am	12pm	3pm
Sunday	Groups 1-12	Groups 13-21	Groups 22-30
Monday	Groups 31-42	Groups 43-51	Groups 52-60

So, for example, on Sunday **exactly** at 8:30am all of the first 12 groups should attend. At 12pm groups 13, 14, …, and 21 should attend; and so on.

Any group of students miss their designated time will be considered absent. Also, any student, who does not attend with his group, will be considered absent.

Group #:

					ID's (رقم الجلوس)	Section	Student Name		
									1
									2
									3
									4
									5