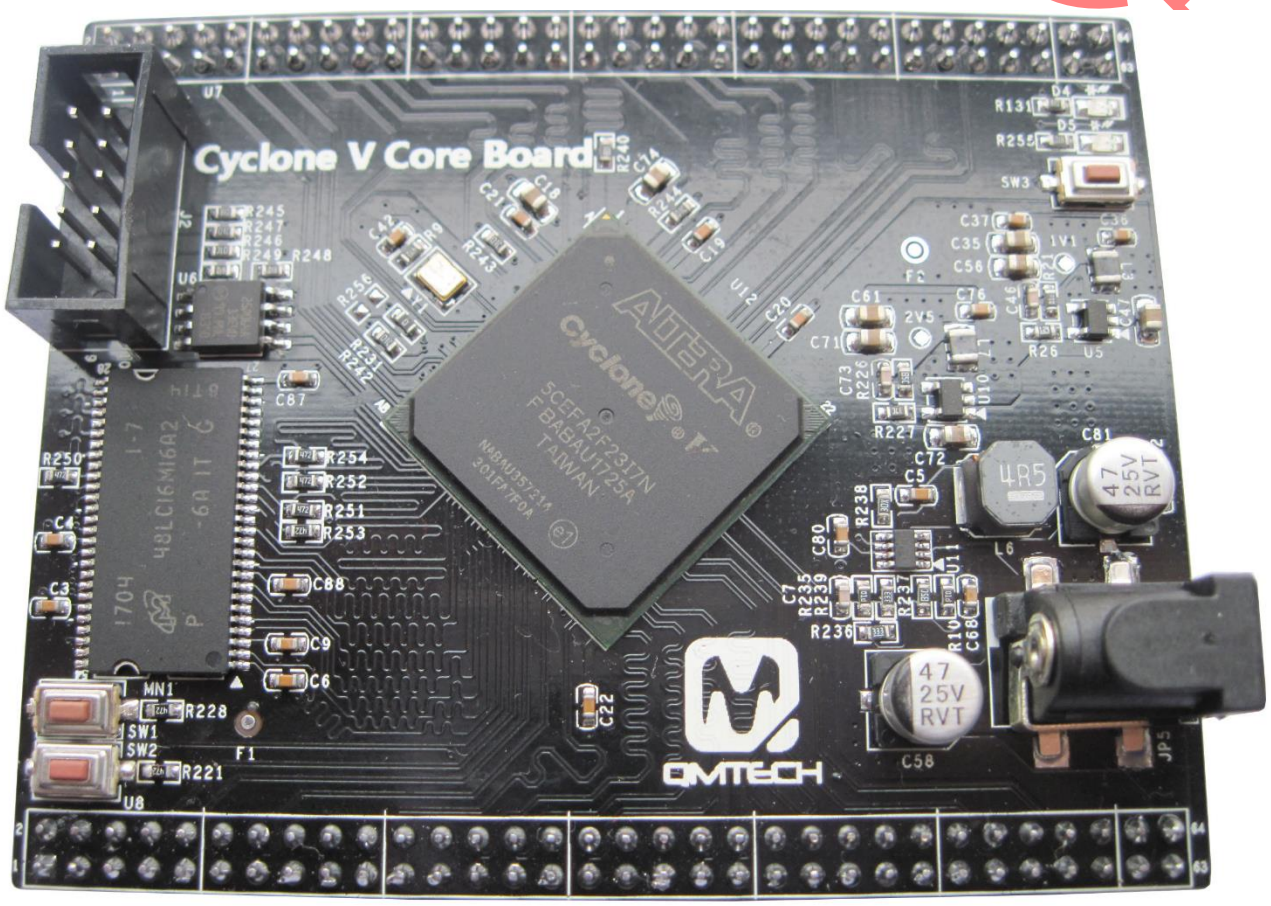
CYCLONEV_5CEFA2 CORE BOARD

USER MANUAL



Preface

The QMTech® Cyclone V SDRAM Development Kit uses Altera(Intel) 5CEFA2F23 device to demonstrate the industry's lowest system cost and power, along with performance levels that make the device family ideal for differentiating your high-volume applications. You'll get up to 40% lower total power compared with the previous generation, efficient logic integration capabilities, integrated transceiver variants, and SoC FPGA variants with an ARM®-based hard processor system (HPS).

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1. Introduction

1.1 Document Scope

This demo user manual introduces the QM_CycloneV_5CEFA2 core board and describes how to setup the core board running with application software Altera Quartus II 15.1. Users may employee the on board rich logic resource FPGA 5CEFA2F23I7N and large SDRAM memory MT48LC16M16 to implement various applications. The core board also has 108 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the QM_CycloneV_5CEFA2:

- On-Board FPGA: 5CEFA2F23I7N;
- On-Board FPGA external crystal frequency: 50MHz;
- 5CEFA2F23I7N has rich block RAM resource up to 1760Kb;
- 5CEFA2F23I7N has 25K Logic elements;
- On-Board N25Q064 SPI Flash, 8M bytes for user configuration code;
- On-Board 32MB Micron SDRAM, MT48LC16M16A2;
- On-Board 3.3V power supply for FPGA by using MP2315 wide input range DC/DC;
- QM_CycloneV_5CEFA2 core board has two 64p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- QM_CycloneV_5CEFA2 core board has 3 user switches;
- QM_CycloneV_5CEFA2 core board has 2 user LEDs;
- QM_CycloneV_5CEFA2 core board has JTAG interface, by using 10p, 2.54mm pitch header;
- QM_CycloneV_5CEFA2 core board PCB size is: 6.7cm x 8.4cm;
- Default power source for core board is: 1A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

1.3 Kit Top View

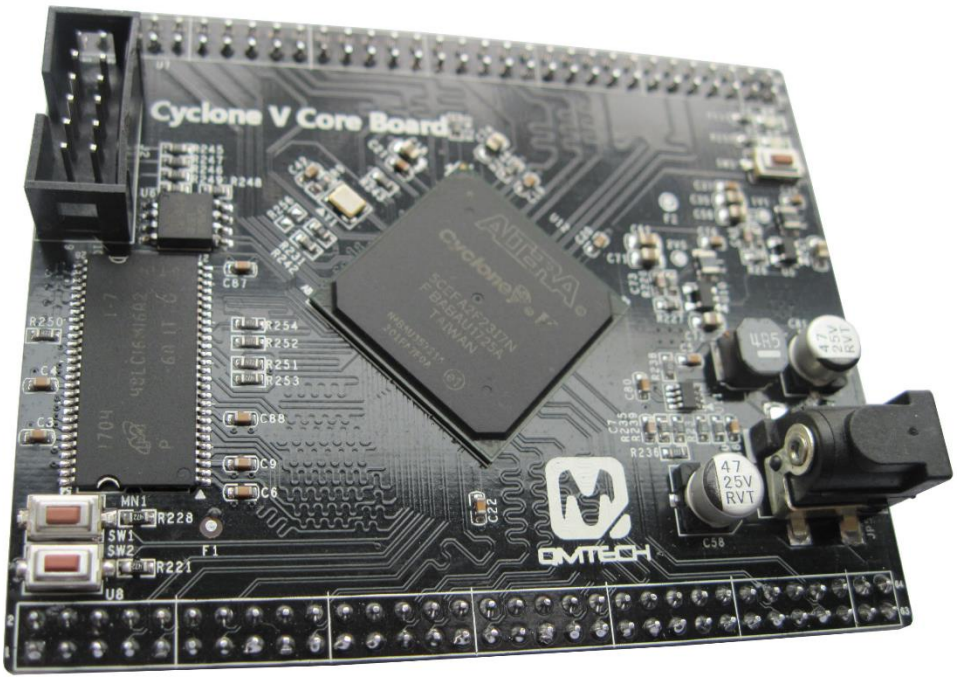


Figure 1-1. QM_CycloneV_5CEFA2 Top View

2. Getting Started

Below image shows the dimension of the QM_CycloneV_5CEFA2 core board: 67.1mm x 84.1mm. The unit in below image is millimeter(mm).

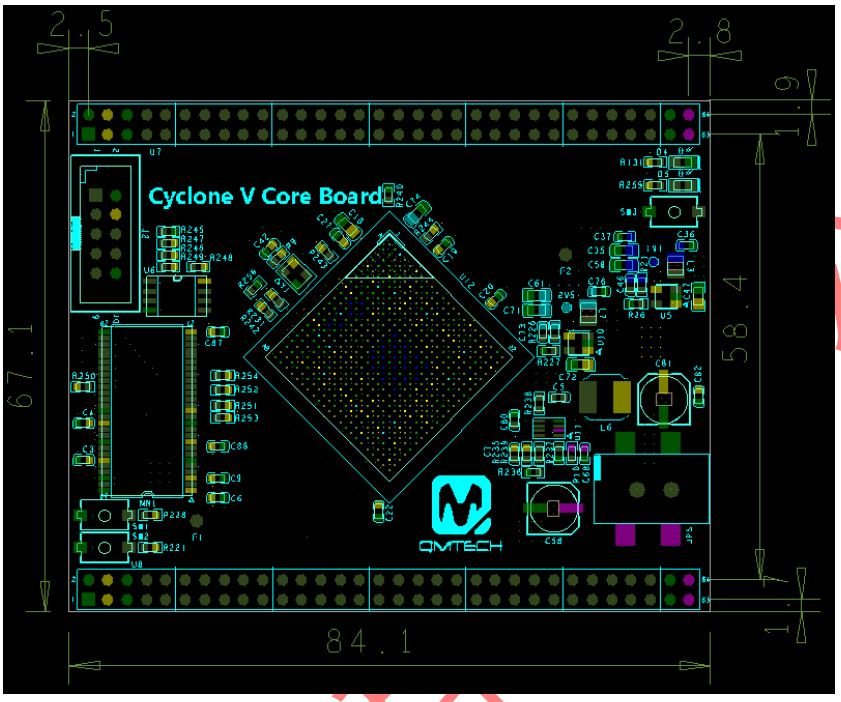
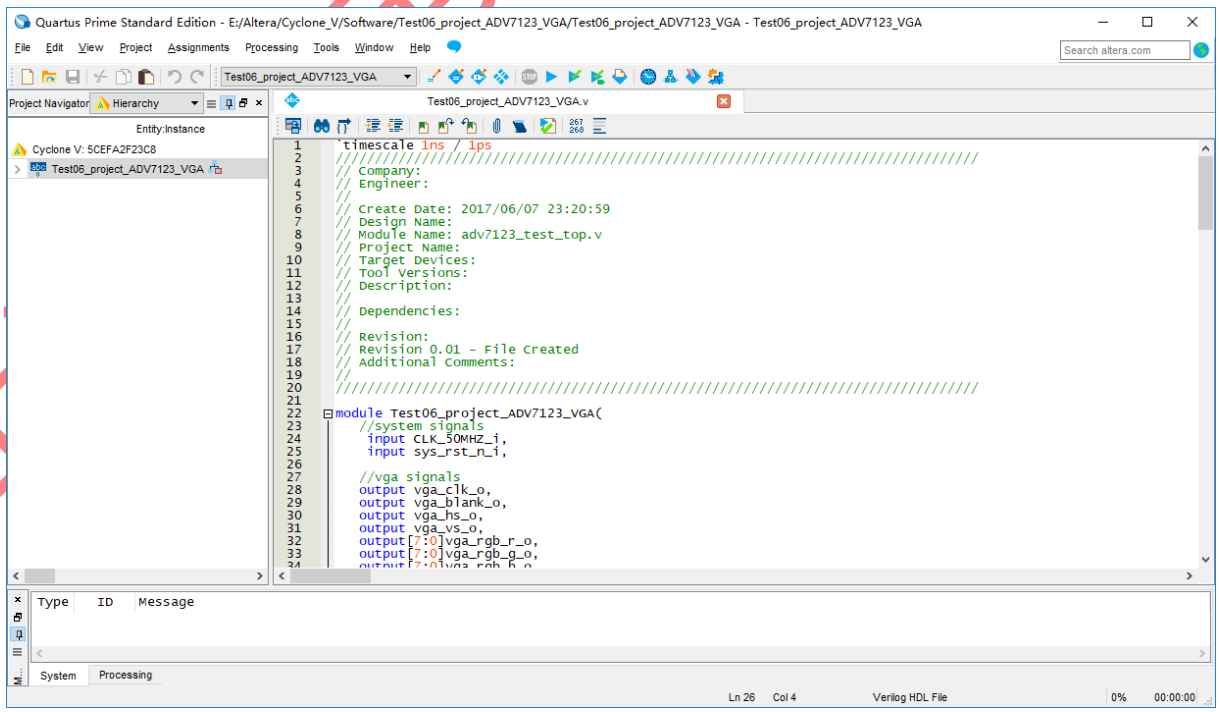


Figure 2-1. QM_CycloneV_5CEFA2 Dimension

The QM_CycloneV_5CEFA2 core board tool chain consists of Altera Quartus II 15.1, Altera USB Blaster cable, 5CEFA2F23 core board and 5V DC power supply. Below image shows the Altera Quartus II 15.1 development environment which could be downloaded from Altera(Intel) office website:



2.2 QM_CycloneV_5CEFA2 Hardware Design

2.2.1 QM_CycloneV_5CEFA2 Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header or the 64P header U7/U8. Users may refer to the hardware schematic for the detailed design. The on board LED D4 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V.

Note: FPGA core supply 1.1V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.

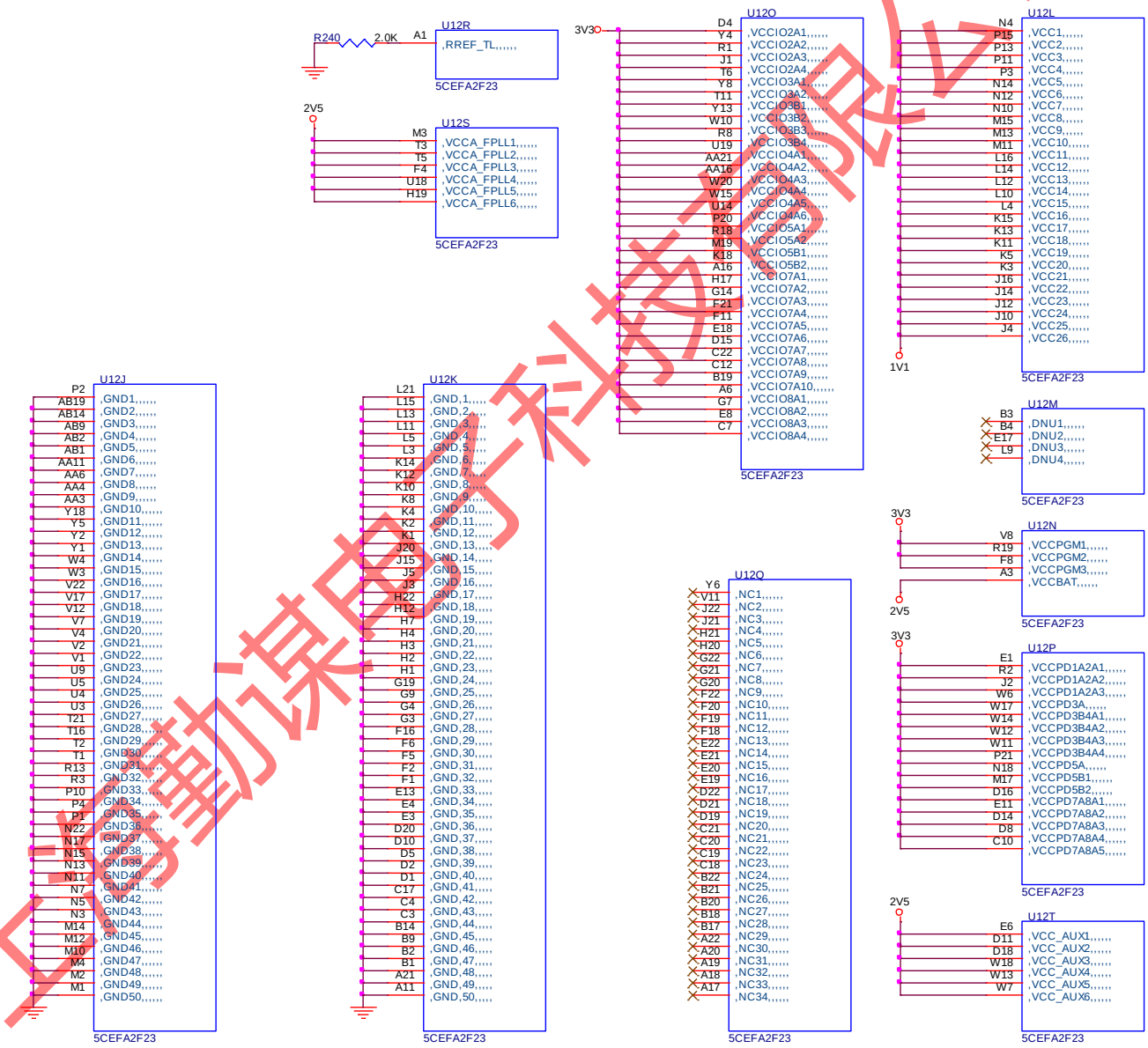


Figure 2-2. Power Supply for the FPGA

2.2.2 QM_CycloneV_5CEFA2 SDRAM Memory

QM_CycloneV_5CEFA2 has on board 16bit width data bus, 32MB memory size MT48LC16M16 SDRAM provided by Micron. Below image shows the detailed hardware design:

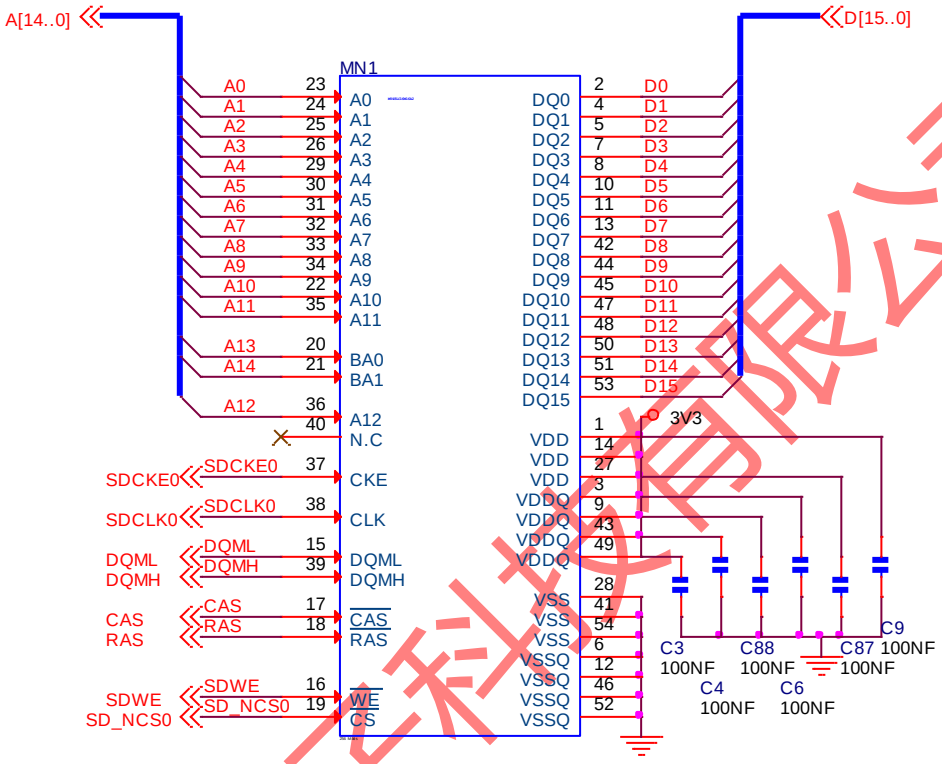


Figure 2-3. SDRAM

2.2.3 QM_CycloneV_5CEFA2 SPI Boot

QM_CycloneV_5CEFA2 boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using N25Q064 manufactured by Micron, with 64Mbit memory storage.

Note: The SPI Flash is designed with x1 mode.

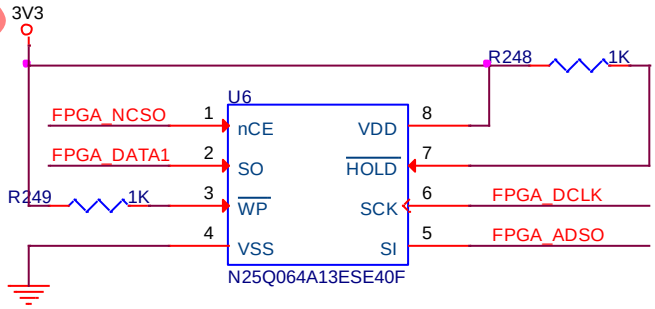


Figure 2-4. SPI Flash

Below image shows the hardware configuration of MSEL[4:0]: 10011, in which way will make the FPGA boot from Active Serial (x1 or x4) Standard Mode:

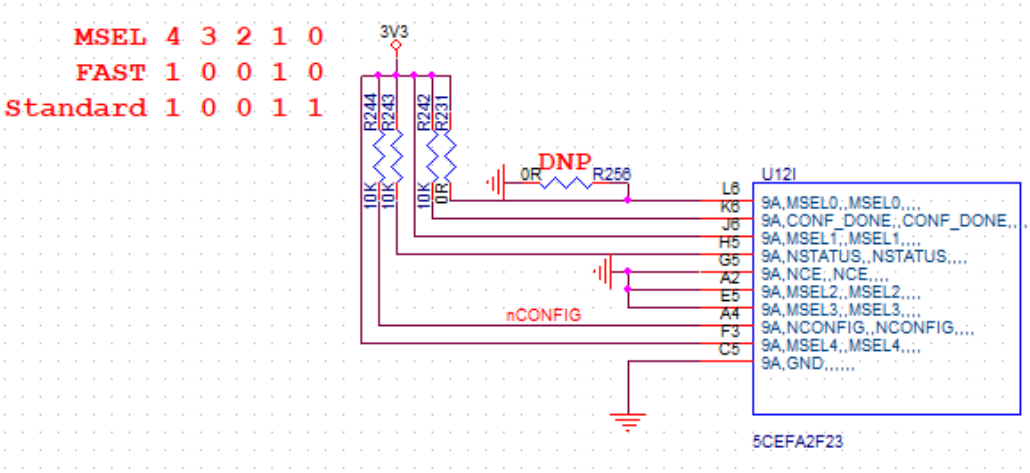


Figure 2-5. MSEL Settings

2.2.4 QM_CycloneV_5CEFA2 System Clock

The QM_CycloneV_5CEFA2 has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/°c. Below image shows the detailed hardware design:

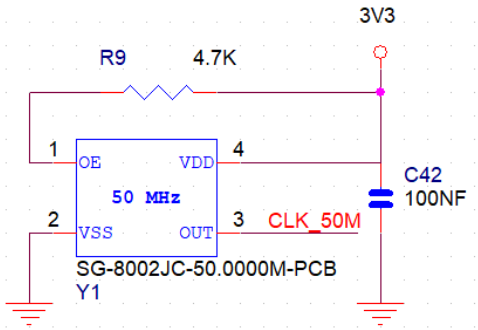


Figure 2-6. 50MHz System Clock

2.2.1 QM_CycloneV_5CEFA2 JTAG Port

The on board JTAG port uses 10P 2.54mm pitch header which could be easily connected to Altera USB blaster cable. Below image shows the hardware design of the JTAG port:

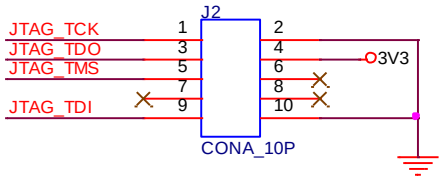


Figure 2-7. JTAG Port

2.2.2 QM_CycloneV_5CEFA2 Power Supply

The core board's 3.3V power supply is using high efficiency DC/DC chip MP2315 provided by MPS Inc. The MP2315 supports wide voltage input range from 4.5V to 24V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the MP2315 hardware design:

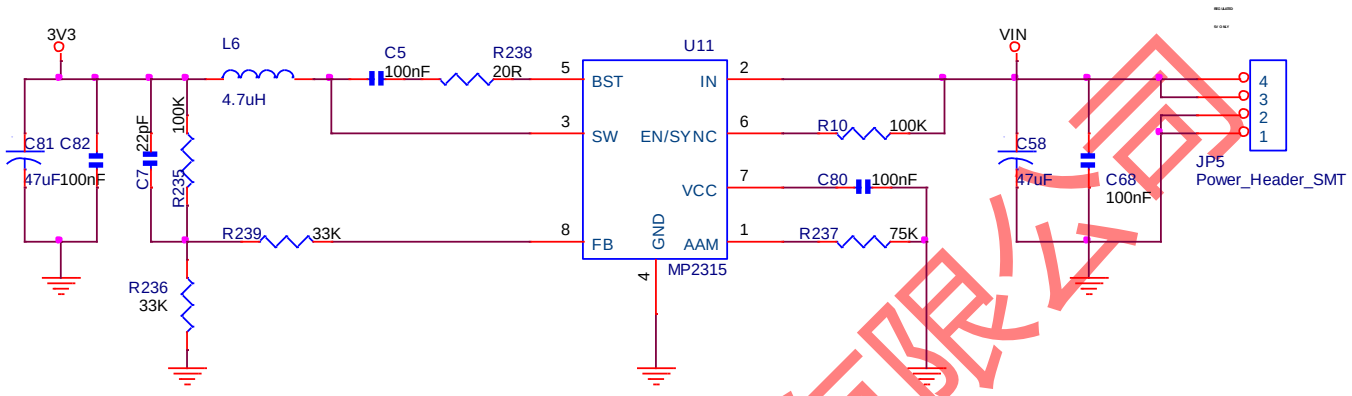


Figure 2-8. MP2315 Hardware Design

The core board's 2.5V and 1.1V FPGA core voltage power supply is using high efficiency DC/DC chip NCP1529 provided by On-Semi Inc.

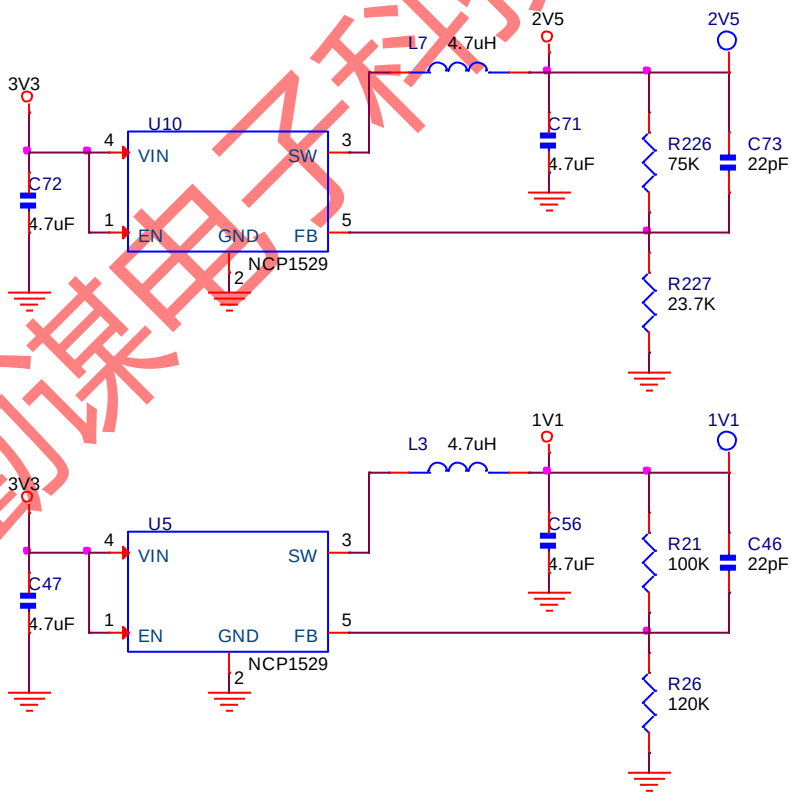


Figure 2-9. NCP1529 Hardware Design

2.2.3 QM_CycloneV_5CEFA2 Extension IO

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

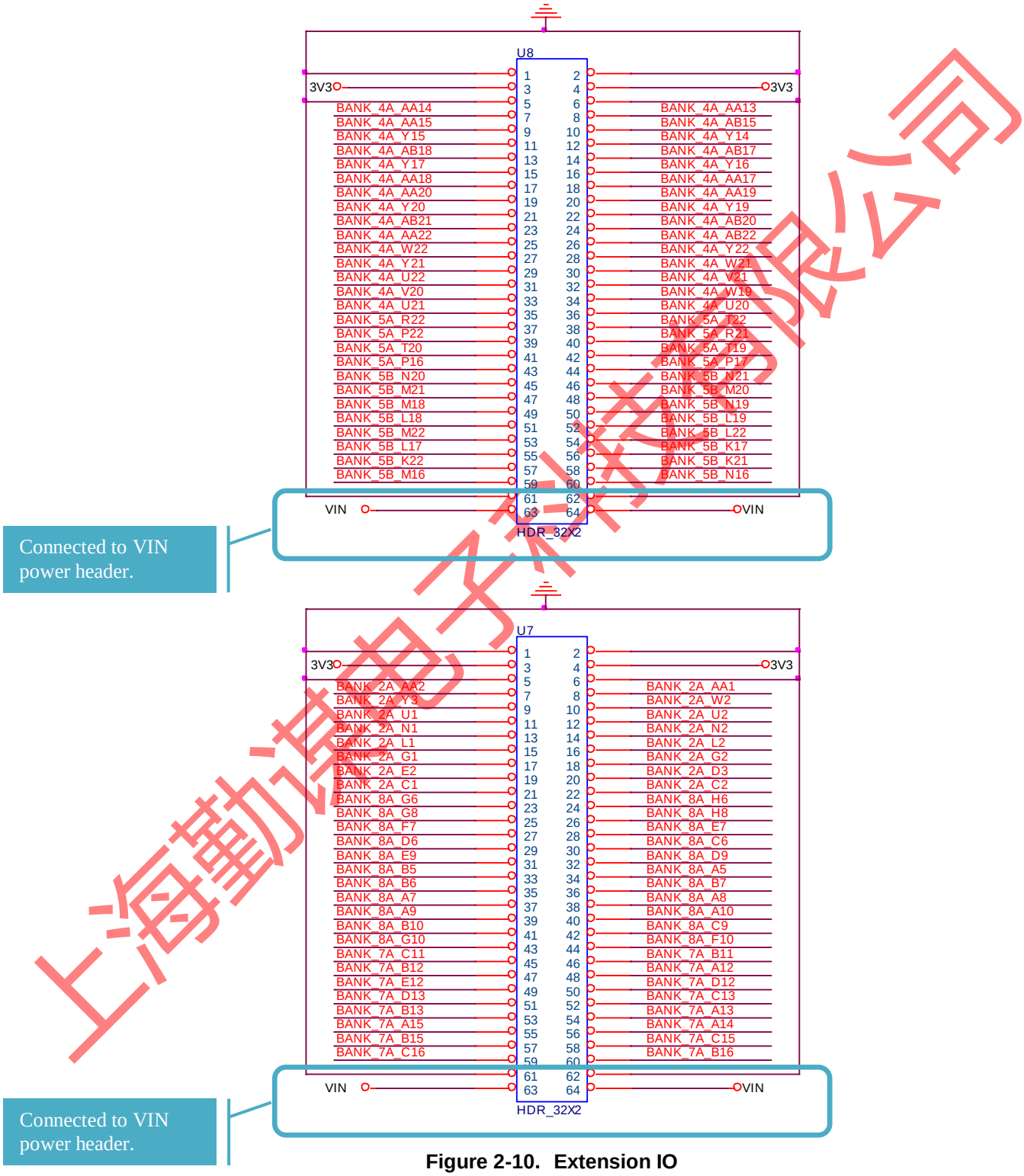


Figure 2-10. Extension IO

2.2.4 QM_CycloneV_5CEFA2 User LED

Below image shows one user LED and 3.3V power supply indicator:

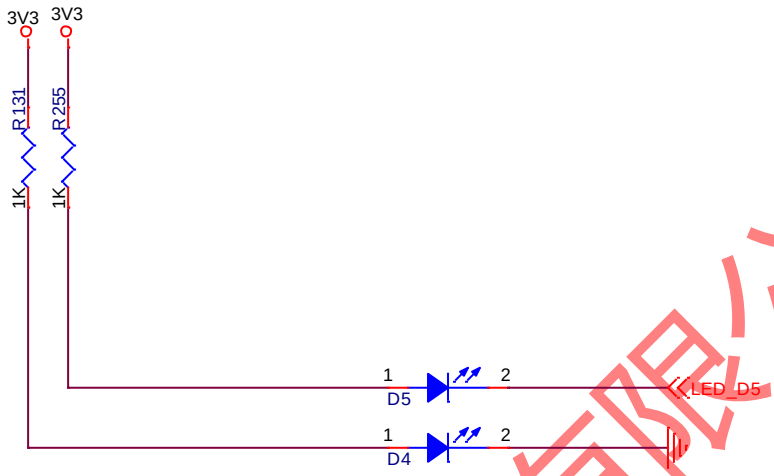


Figure 2-11. User LEDs

2.2.5 QM_CycloneV_5CEFA2 User Key

Below image shows the nCONFIG key and two user keys:

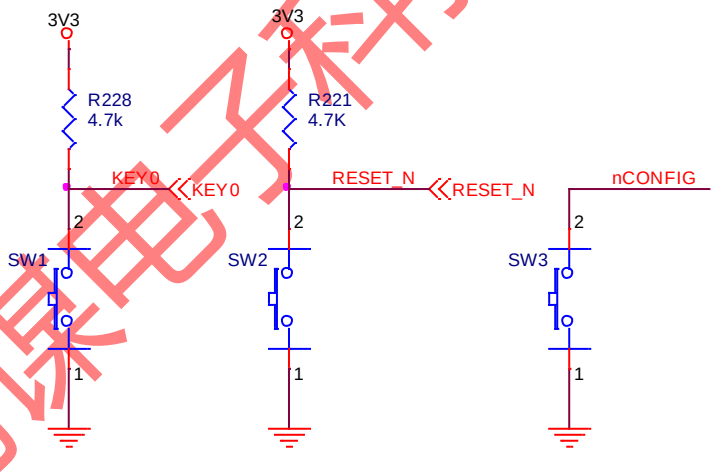


Figure 2-12. User Keys

3. Reference

[1] 5cefa2-sdram_20171202_V01.pdf
[2] cv_5v2_Cyclone V Device Handbook.pdf
[3] an662_Arria V and Cyclone V Design Guidelines.pdf
[4] cv_51001_Cyclone V Device Overview.pdf
[5] cv_51002_Cyclone V Device Datasheet.pdf
[6] pcg-01014_Cyclone® V Device Family Pin Connection Guidelines.pdf

4. Revision

Doc. Rev.	Date	Comments
0.1	1/1/2018	Initial Version.
1.0	7/1/2018	V1.0 Formal Release.