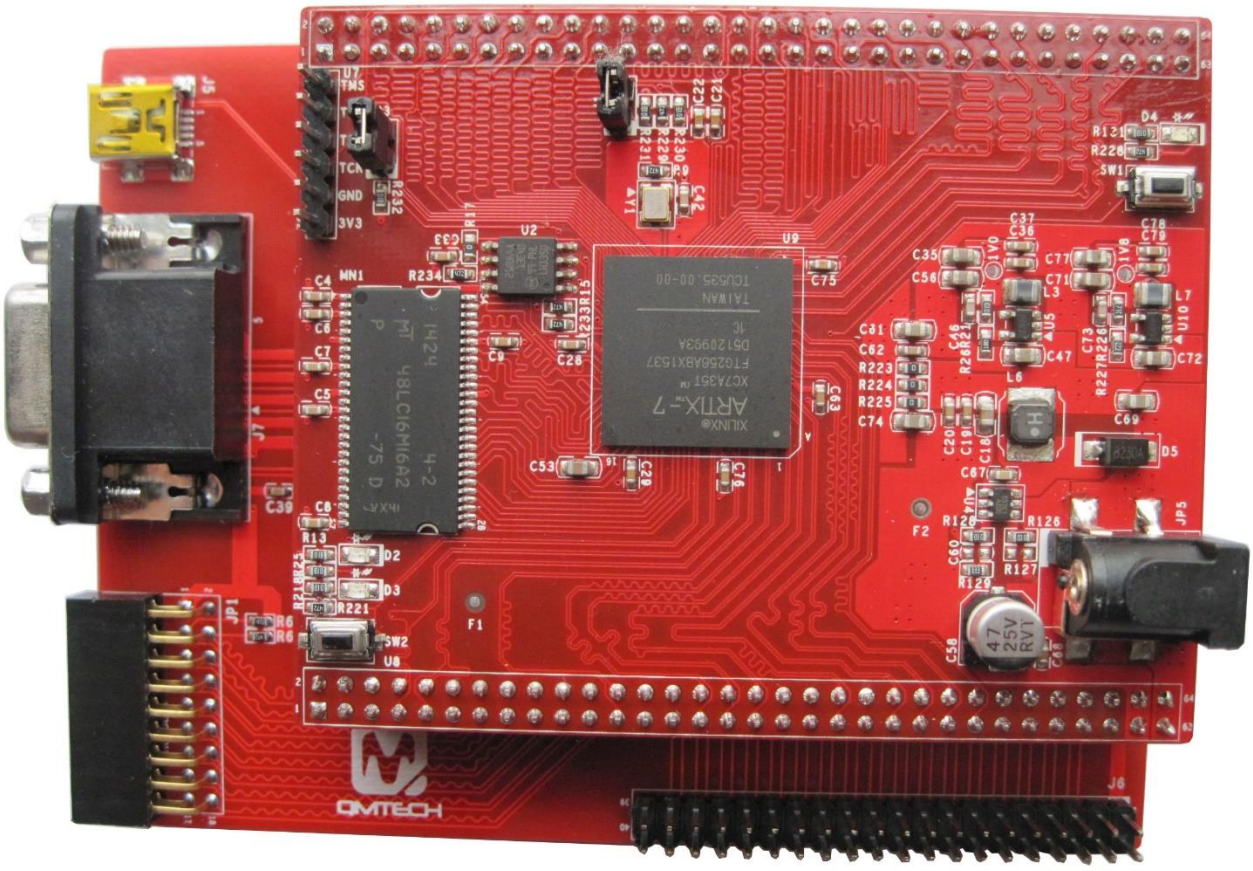
QM_XC7A35T SDRAM DB

USER MANUAL



Preface

The QMTech® XC7A35T SDRAM Development Kit uses Xilinx Artix®-7 devices to demonstrate the highest performance-per-watt fabric, transceiver line rates, DSP processing, and AMS integration in a cost-optimized FPGA. Featuring the MicroBlaze™ soft processor and 1,066Mb/s DDR3 support, the family is the best value for a variety of cost and power-sensitive applications including software-defined radio, machine vision cameras, and low-end wireless backhaul.

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1. QM_XC7A35T_SDRAM DB Introduction

1.1 Kit Overview

QM_XC7A35T_SDRAM Daughter Board provides several user interfaces to meet different customer needs. Below section lists the detailed info of these user interfaces:

- USB to UART Serial Port, by using Silicon Labs' CP2102-GMR chip.
- 24bit(RGB888) VGA display interface, by using Analog Device's ADV7123-KSTZ140 chip;
- High speed USB 2.0 peripheral controller, by using Cypress' CY7C68013A-56LTXC chip;
- Reserved CMOS/CCD camera interface, by using 18pin female header;
- Extended 40 pin male header to provide 34 user IOs, which could be used to connect customized modules, e.g. ADC/DAC module, Ethernet module, Audio module;

1.2 Daughter Board Top View

Below figure shows the daughter board of QM_XC7A35T_SDRAM development kit. The daughter board's dimension is 81.28mm x 108.71mm. All the functional chips' power supply is injected from the 64P female connector, detailed connection refer to the hardware schematic.

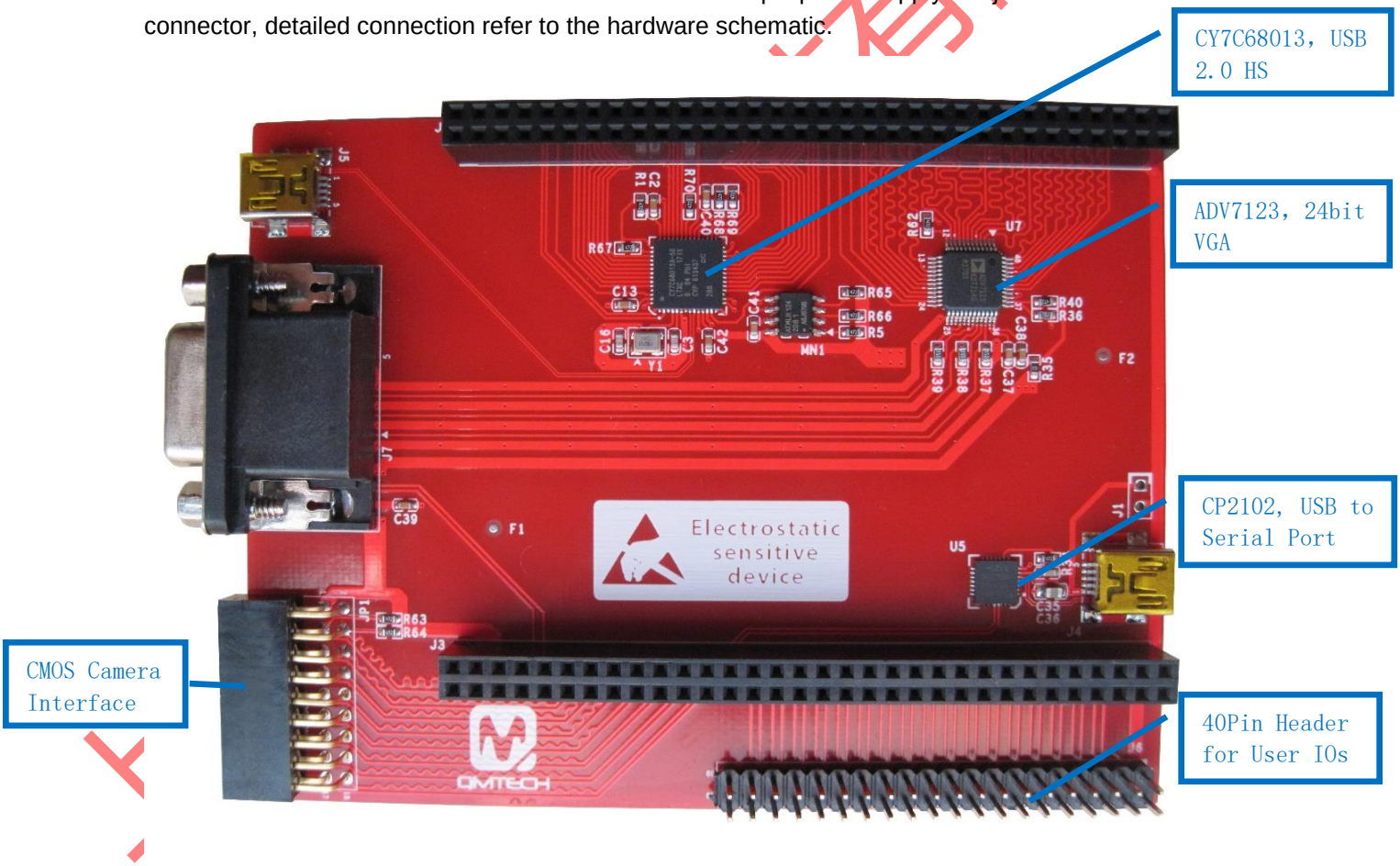


Figure 1-1. Top View of QM_XC7A35T_SDRAM Daughter Board

2. Experiment (1): USB to Serial Port

The CP2102-GMR is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102-GMR includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CP2102-GMR on the QM_XC7A35T_SDRAM daughter board.

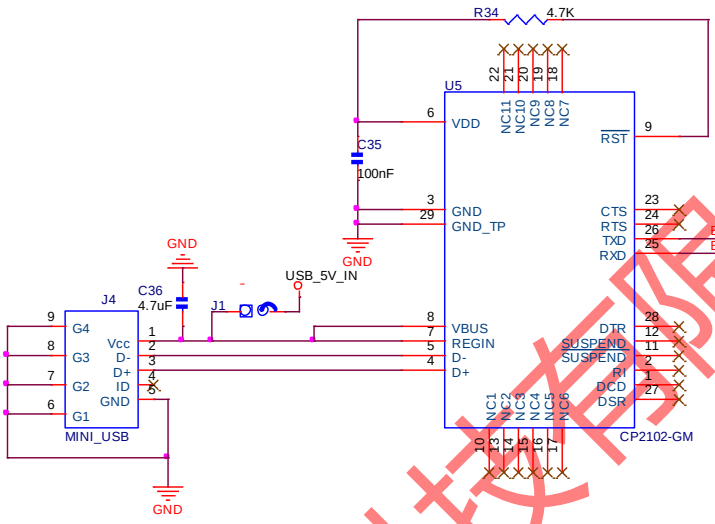
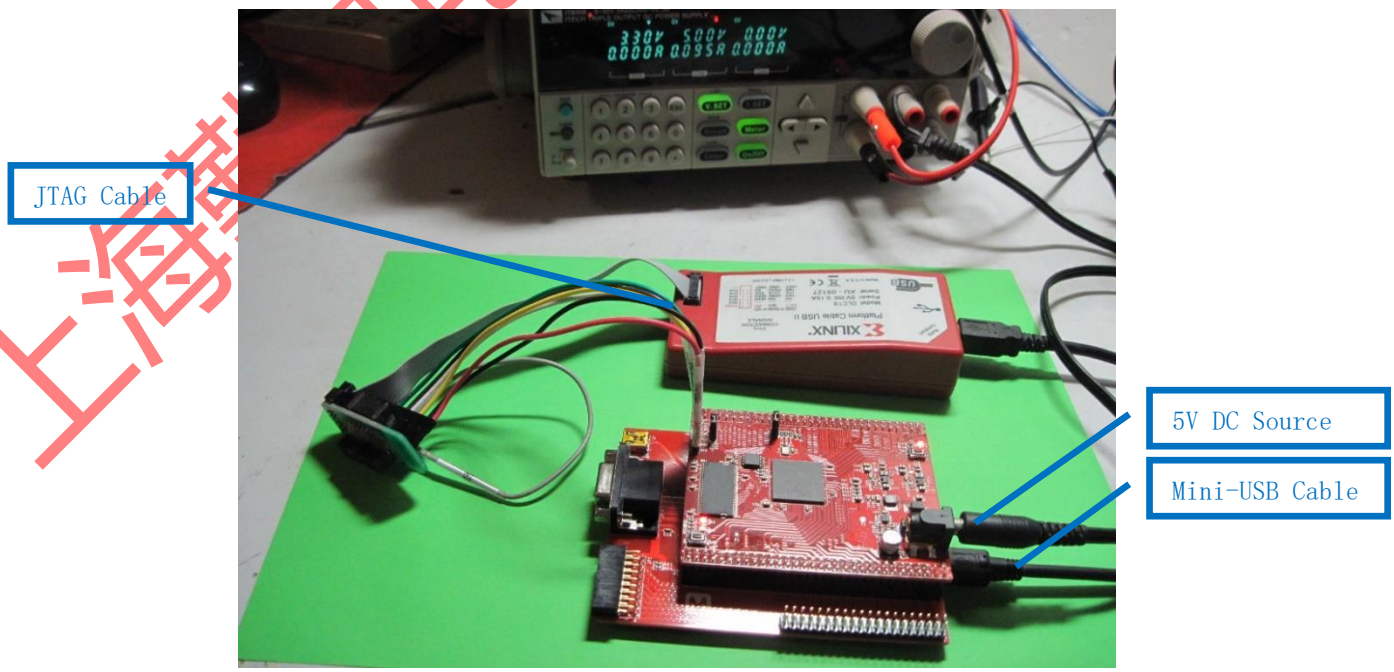


Figure 2-1. CP2102 Hardware Design

Before start to test the CP2102-GMR's USB to UART serial communication function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB platform cable's VREF, GND, TDI, TMS, TCK, TDO pins shall be connected to QM_XC7A35T_SDRAM core board's JTAG interface. Then power on the development kit with 5V DC power source. Xilinx USB platform cable's indicator LED's color will turn from brown into green. At the same time, the Mini-USB cable shall also be plugged in the board, below figure shows an example hardware setup:



All the test examples are developed in the Xilinx Vivado 2016.4 environment. Open the CP2102 test project located in this release folder: /Software/Test06_project_usb_uart. Below figure shows the example project of **uart_top**:

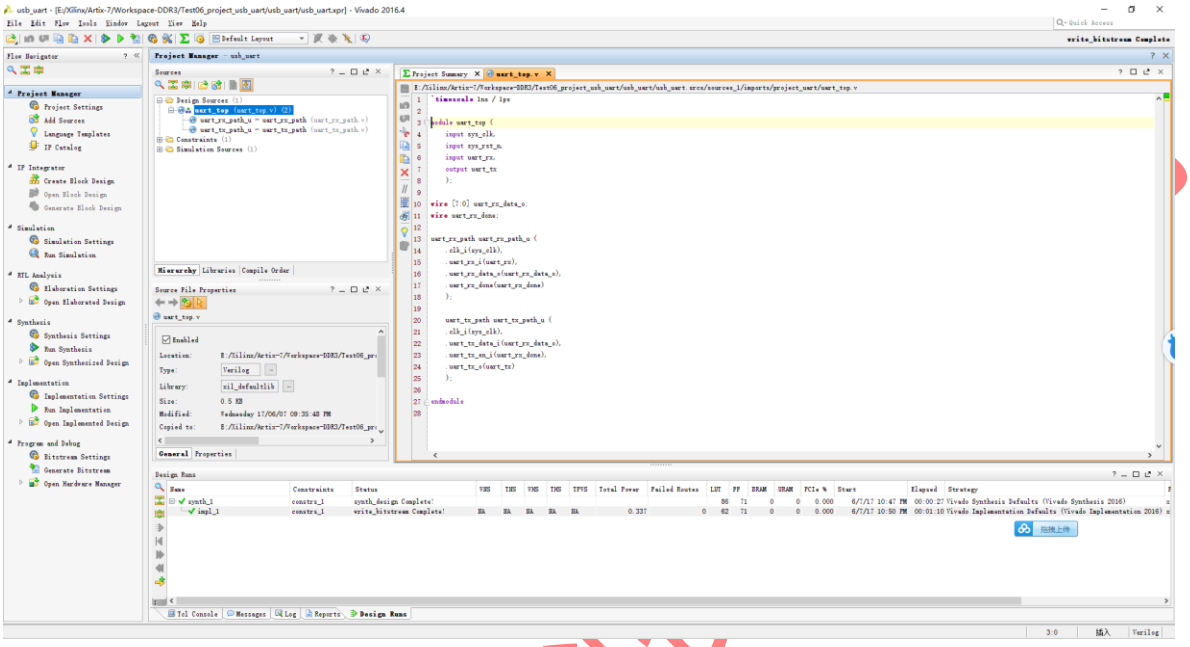


Figure 2-2. CP2102 UART Communication Test Example

In this example project, the default communication parameters are: 9600bps, 8 data bit, No Parity Check, 1 stop bit. If users want to test other communication parameters, change the source code accordingly.

uart_rx_path.v

```
`timescale 1ns / 1ps

module uart_rx_path(
    input clk_i,
    input uart_rx_i,

    output [7:0] uart_rx_data_o,
    output uart_rx_done,
    output baud_bps_tb          //for simulation
    );

parameter [12:0] BAUD_DIV     = 13'd5208;   //波特率时钟，9600bps，50Mhz/9600=5208
parameter [12:0] BAUD_DIV_CAP = 13'd2604;   //波特率时钟中间采样点，50Mhz/9600/2=2604

reg [12:0] baud_div=0;                      //波特率设置计数器
reg baud_bps=0;                             //数据采样点信号
reg bps_start=0;                            //波特率启动标志
always@(posedge clk_i)
begin
    if(baud_div==BAUD_DIV_CAP)              //当波特率计数器计数到采样点时，产生采样信号baud_bps
```

uart_tx_path.v

```
`timescale 1ns / 1ps

module uart_tx_path(
    input clk_i,

    input [7:0] uart_tx_data_i,         //待发送数据
    input uart_tx_en_i,                 //发送发送使能信号

    output uart_tx_o
);

parameter BAUD_DIV     = 13'd5208;      //波特率时钟，9600bps，50Mhz/9600=5208，波特率可调
parameter BAUD_DIV_CAP = 13'd2604;      //波特率时钟中间采样点，50Mhz/9600/2=2604，波特率可调

reg [12:0] baud_div=0;                  //波特率设置计数器
reg baud_bps=0;                         //数据发送点信号,高有效
(* MARKDEBUG = "TRUE" *)reg [9:0] send_data=10'b1111111111;     //待发送数据寄存器，1bit起始信号+8bit有效信号+1bit结束信号
(* MARKDEBUG = "TRUE" *)reg [3:0] bit_num=0;                    //发送数据个数计数器
reg uart_send_flag=0;                   //数据发送标志位
reg uart_tx_o_r=1;                      //发送数据寄存器，初始状态位高
```

After the CP2102 communication test project correctly synthesized, implemented and generated bit file, users could use Xilinx program tool to program the generated bit file into FPGA. Below image shows the FPGA program status with program tool.

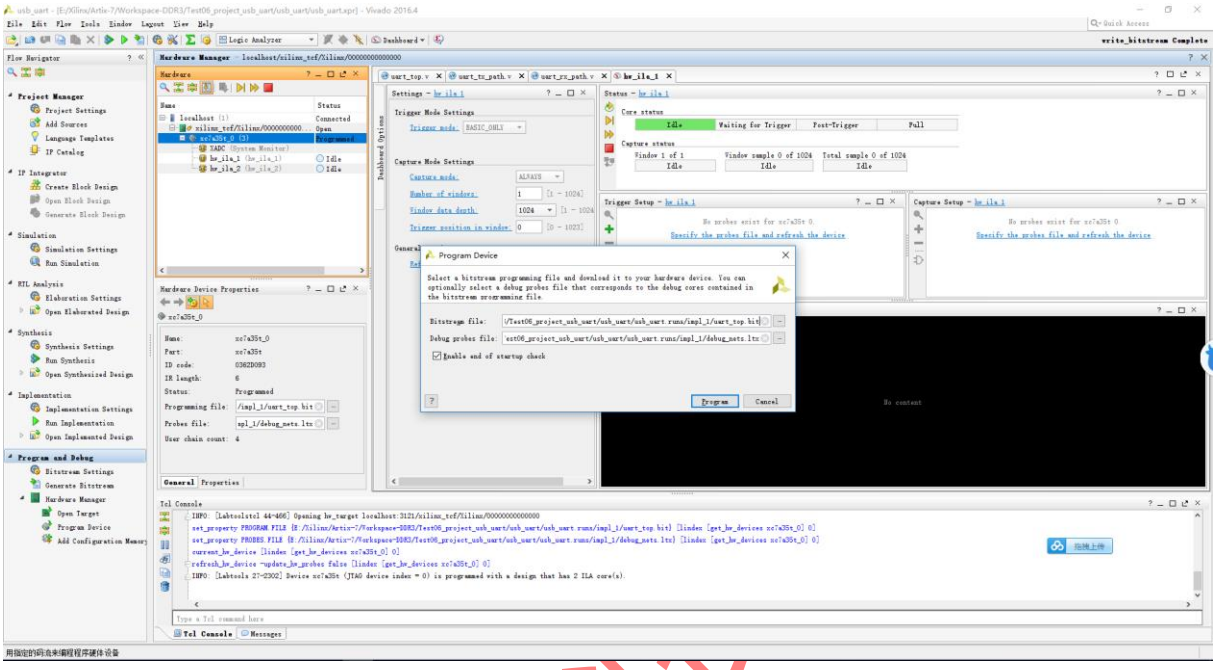


Figure 2-3. Program the FPGA

The CP2102 example test project's main functionality is performing an UART loopback communication. The FPGA program will send the received UART data back to the PC. Below figure shows user employees some PC based UART test tool to send data to FPGA: *http://www.cmsoft.cn QQ:10865600*. After a short while the PC UART test tool will receive the same data stream from FPGA, which means the CP2102 loopback test program is running correctly.

Figure 2-4. UART Loopback Test

3. Experiment (2): VGA Display

The ADV7123 is a triple high speed, digital-to-analog converter on a single monolithic chip. It consists of three high speed, 10-bit, video DACs with complementary outputs, a standard TTL input interface, and a high impedance, analog output current source. The QM_XC7A35T_SDRAM daughter board provides 24bit(RGB888) VGA display function by using ADV7123-KSTZ140. Below figure shows the hardware design of the ADV7123 chip, the lowest two bits of each color channel are directly connected to GND:

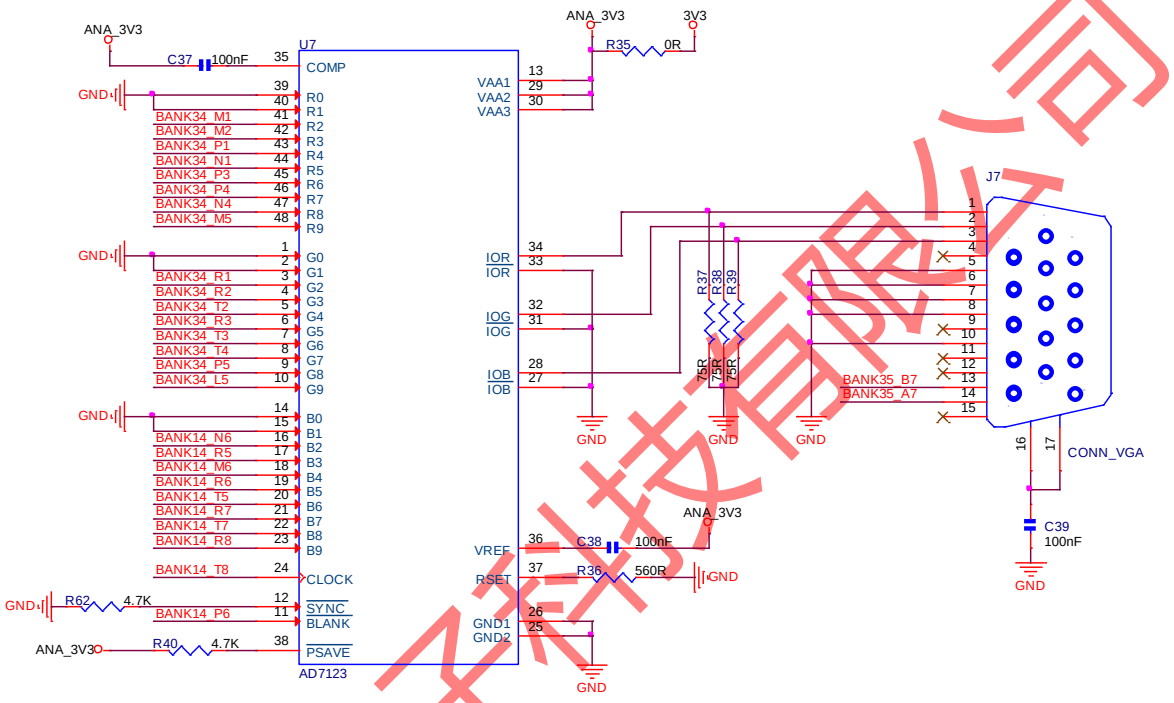
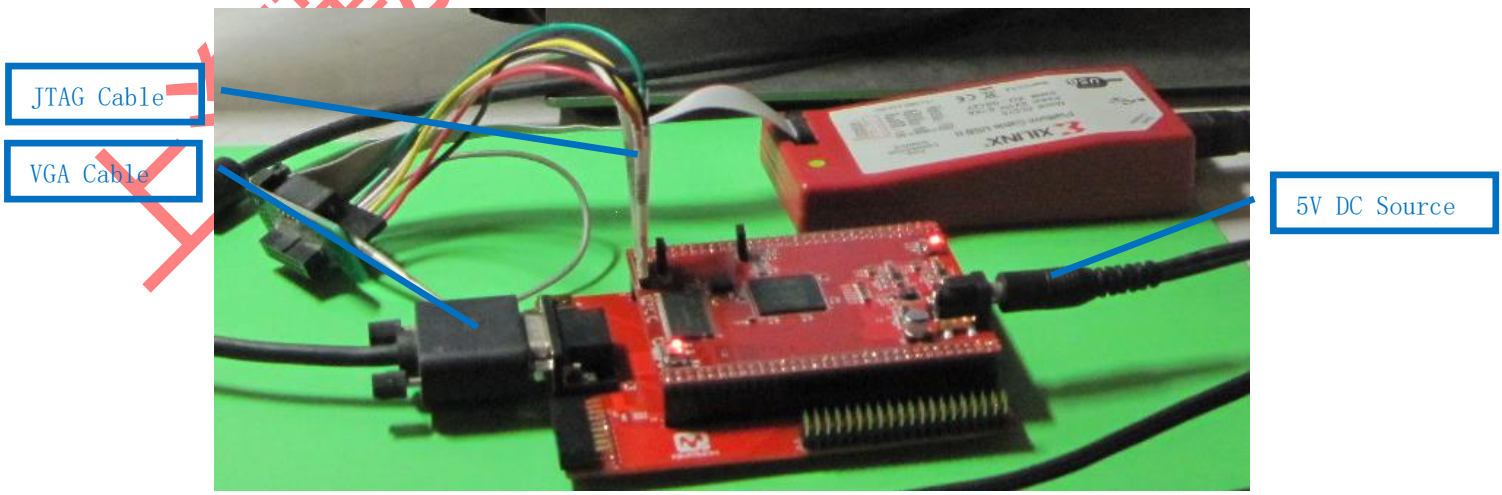


Figure 3-1. ADV7123 Hardware Design

Before start to test the VGA display function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB platform cable's VREF, GND, TDI, TMS, TCK, TDO pins shall be connected to QM_XC7A35T_SDRAM core board's JTAG interface. Then power on the development kit with 5V DC power source. Xilinx USB platform cable's indicator LED's color will turn from brown into green. At the same time, the VGA cable shall also be plugged in the board, below figure shows an example hardware setup:



All the test examples are developed in the Xilinx Vivado 2016.4 environment. Open the VGA test project located in this release folder: /Software/Test07_project_vga_adv7123. Below figure shows the example project of **VGA_test**:

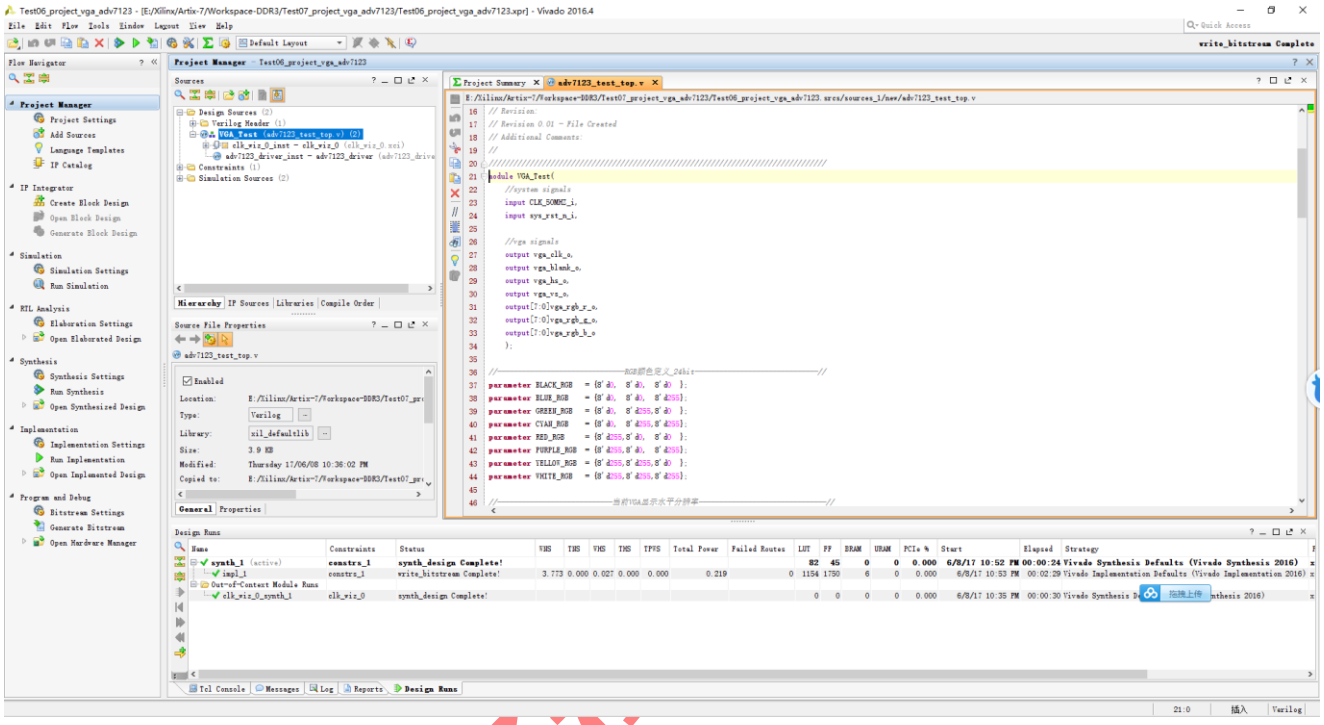


Figure 3-2. VGA Display Function Test

In this example project, the default VGA output resolution parameter is 1280x1024@60Hz. If users want to test other display parameters, change the source code accordingly.

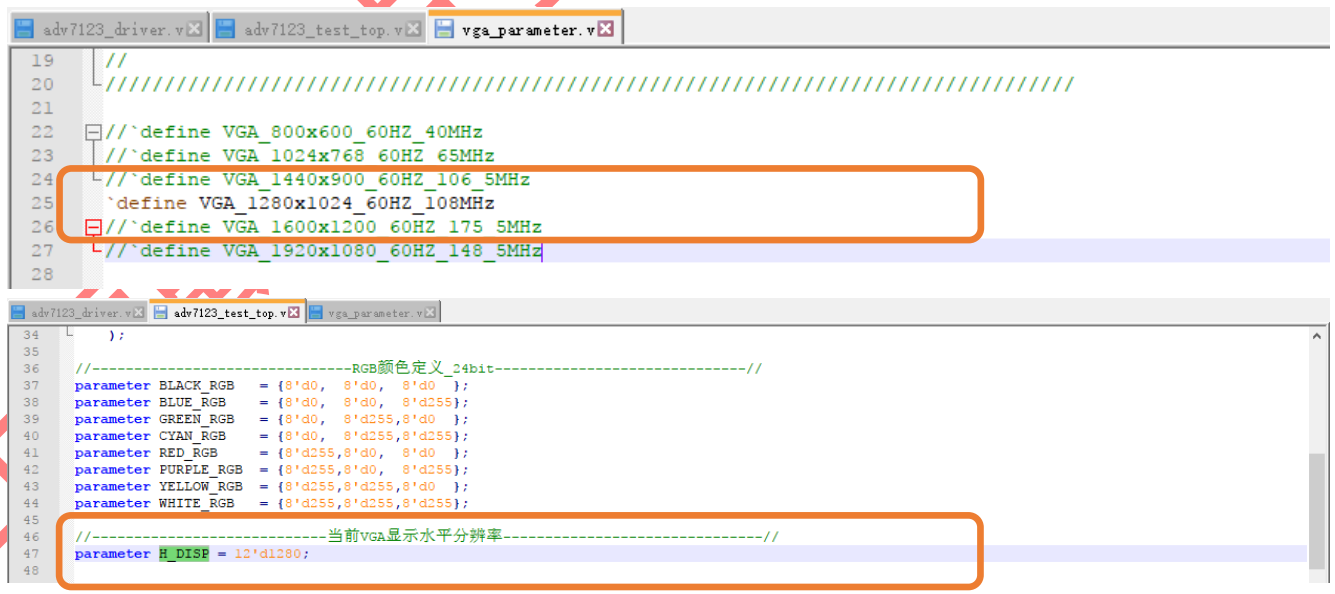


Figure 3-3. VGA Display Parameters

After the VGA display test project correctly synthesized, implemented and generated bit file, users could use Xilinx program tool to program the generated bit file into FPGA. Below image shows the FPGA program status with program tool.

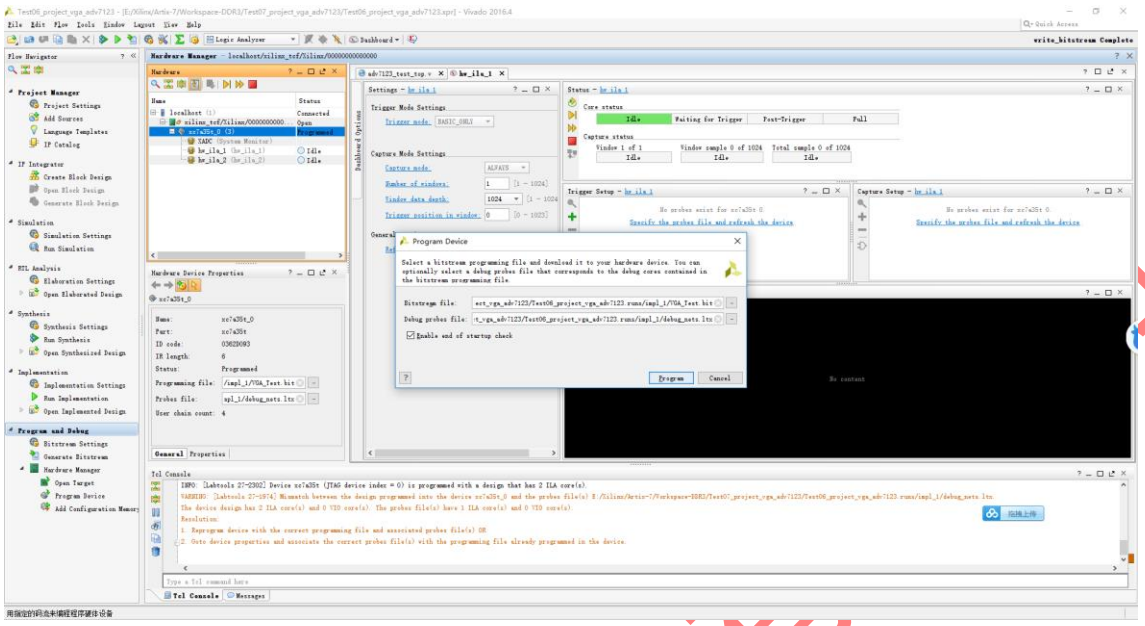


Figure 3-4. Program FPGA

After the FPGA correctly loaded the VGA_Test bit file, the VGA monitor will display the color bar output from development kit's VGA port. Below image shows the example color bar pattern.

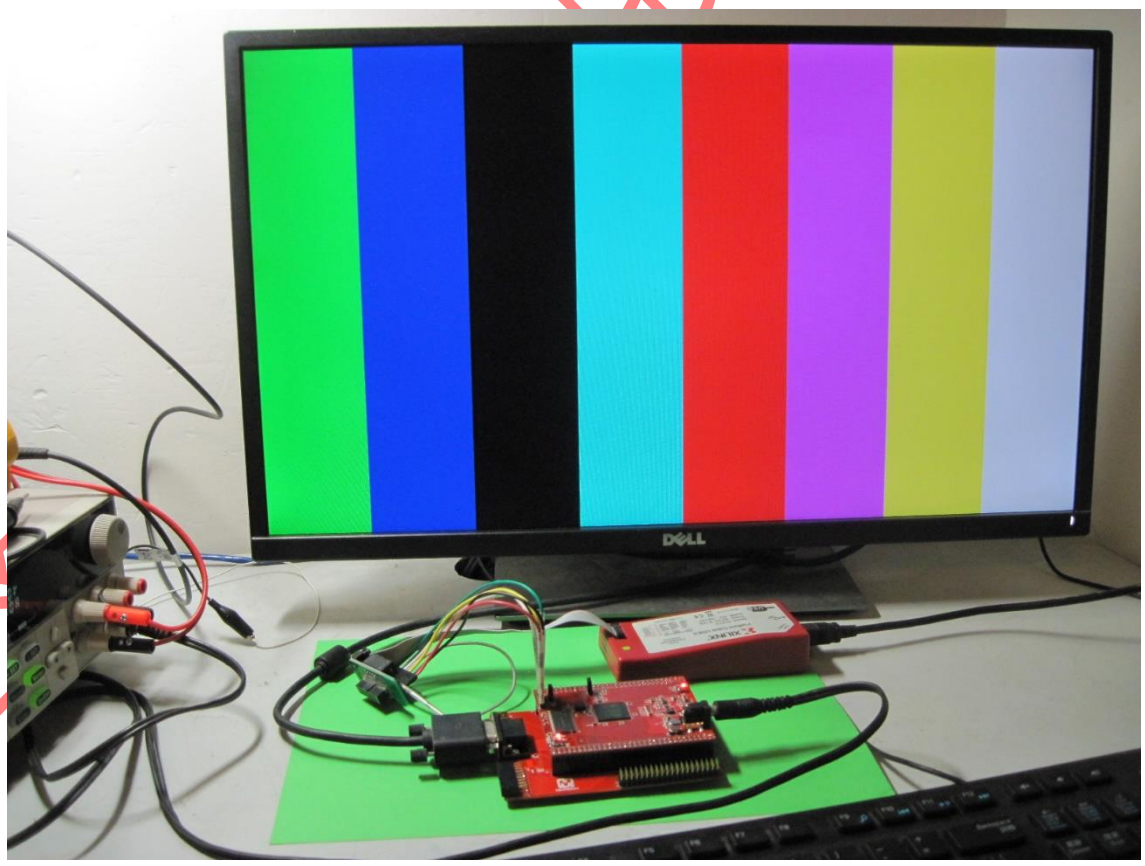


Figure 3-5. VGA Display Test

4. Experiment (3): CY7C68013A USB 2.0 Slave FIFO

Cypress's EZ-USB® FX2LP™ CY7C68013A is a low-power version of the EZ-USB FX2™ (CY7C68013), which is a highly integrated, low-power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a cost-effective solution that provides superior time-to-market advantages with low power to enable bus-powered applications. The QM_XC7A35T_SDRAM daughter board provides slave FIFO interface by using CY7C68013A. Below figure shows the hardware design of the CY7C68013A chip:

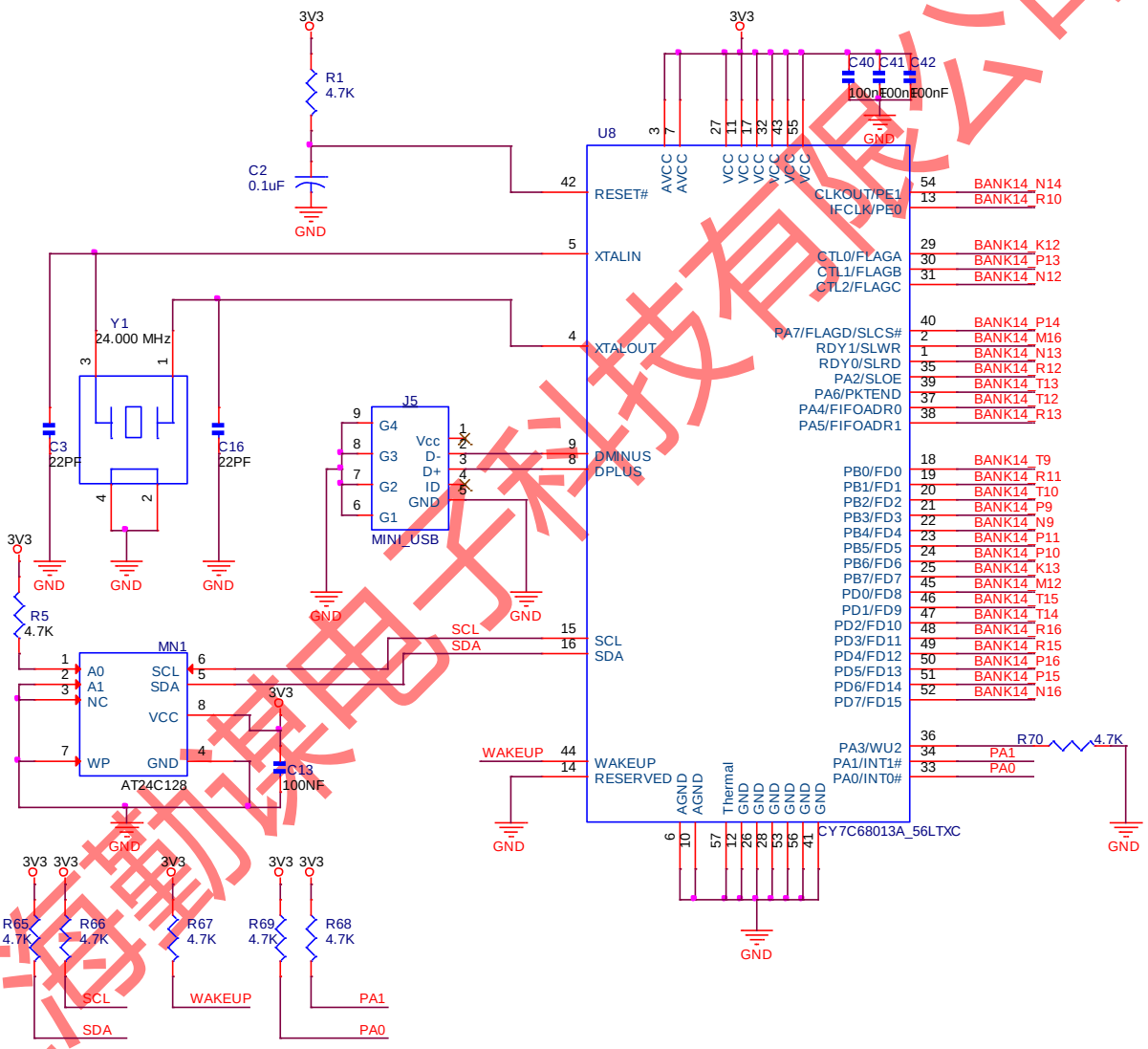


Figure 4-1. CY7C68013A-56LTXC Hardware Design

Before start to test the USB slave FIFO function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB platform cable's VREF, GND, TDI, TMS, TCK, TDO pins shall be connected to QM_XC7A35T_SDRAM core board's JTAG interface. Then power on the development kit with 5V DC power source. Xilinx USB platform cable's indicator LED's color will turn from brown into green. At the same time, the Mini-USB cable shall also be plugged in the board, below figure shows an example hardware setup:

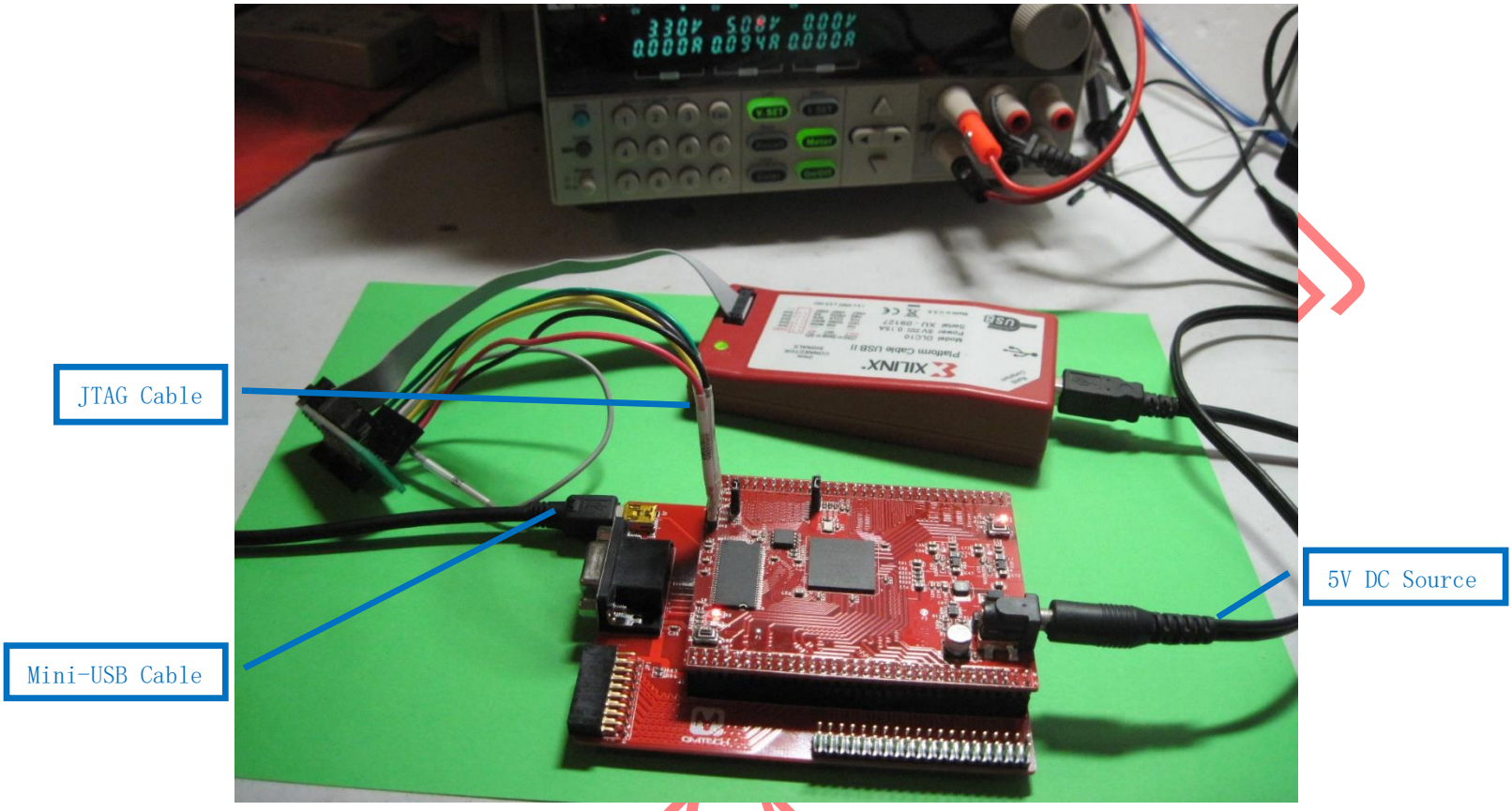


Figure 4-2. Hardware Connections

Users also need to install the PC based USB driver and test software provided by Cypress. These driver and test suite could be retrieved by installing the **CySuiteUSB_3_4_7_B204.exe**. KeilC51V9.00 is also suggested to be installed to compile the CY7C68013A firmware. All of those software packages could be found in the Release folder: /Software/Test04-CY7C68013_USB_2.0_HS.

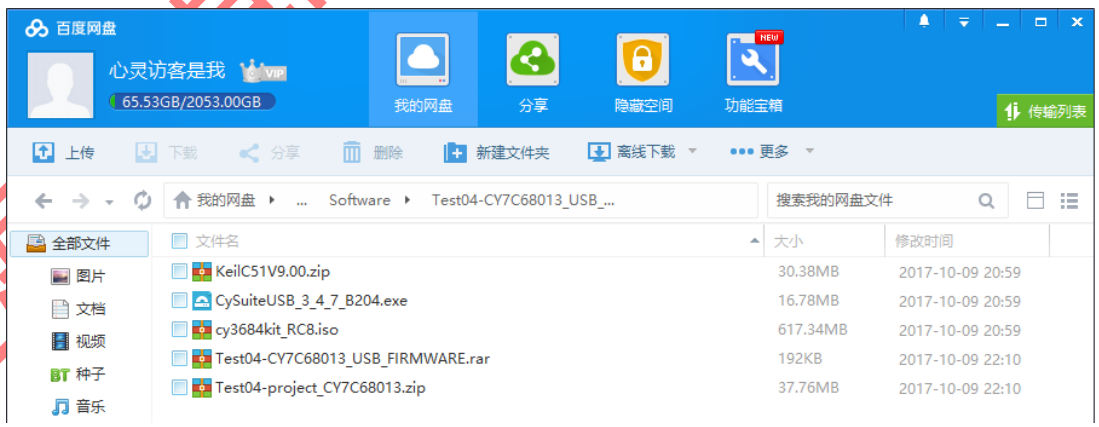


Figure 4-3. USB 2.0 Test Software Package

The windows device manager will inform users to install USB driver, after the Mini-USB cable connected to the PC's USB host connector. The CY7C68013A USB driver could be found in below folder: cy3684kit_RC8-> Drivers->Win7->x86. The **cy3684kit_RC8.iso** could be downloaded from Cypress official site.

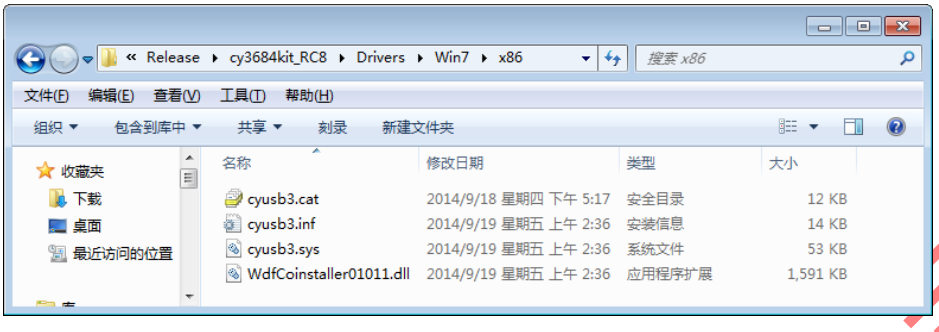


Figure 4-4. CY7C68013 USB Driver

After the CY7C68013 USB driver is correctly installed, the device manager will display the enumerated USB device: ”Cypress FX2LP No EEPROM Device”.

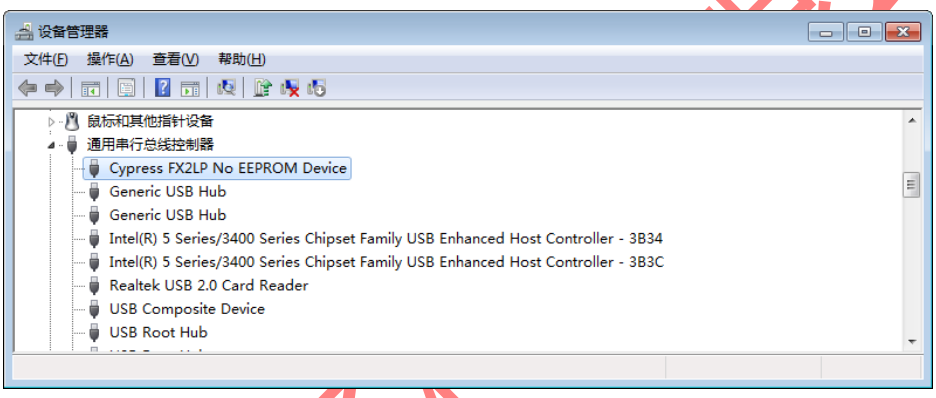
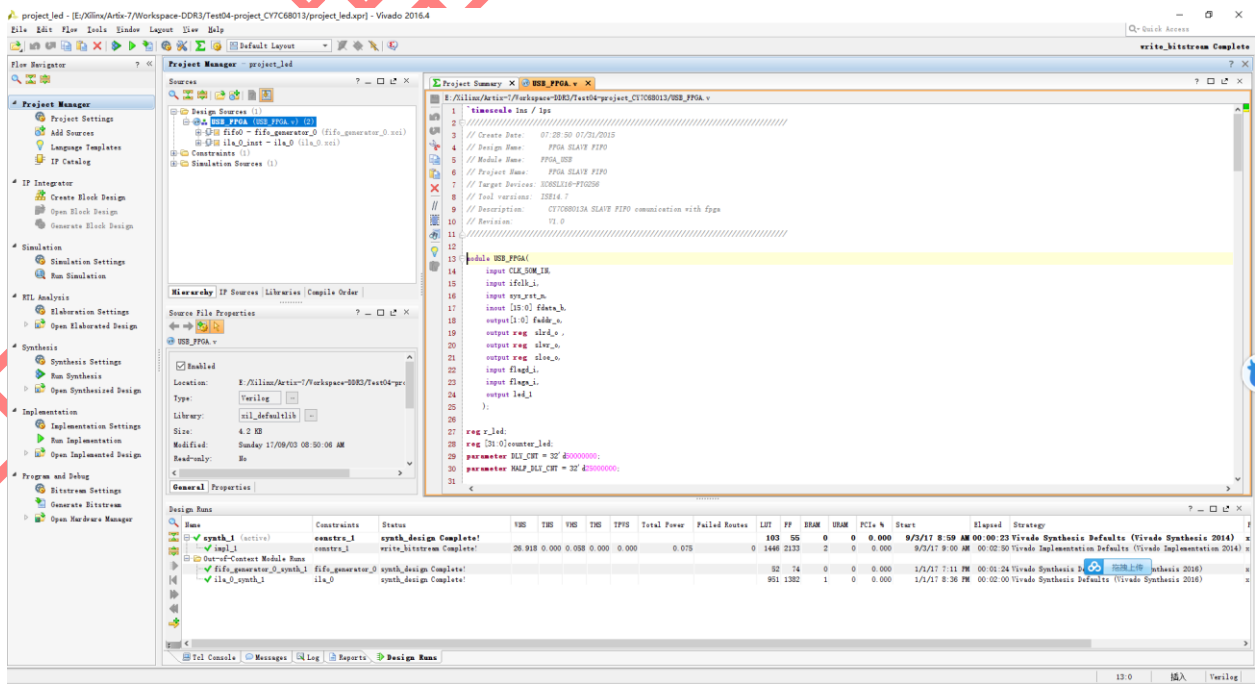


Figure 4-5. Cypress FX2LP No EEPROM Device

Use Vivado 2016.4 to open the Slave FIFO test project located in Release folder: /Software/Test04-CY7C68013_USB_ 2.0_HS/Test04-project_CY7C68013. Below figure shows the example project of **USB_FPGA**:



After the Slave FIFO test project correctly synthesized, implemented and generated bit file, users could use Xilinx program tool to program the generated bit file into FPGA. Below image shows the FPGA program status with program tool.

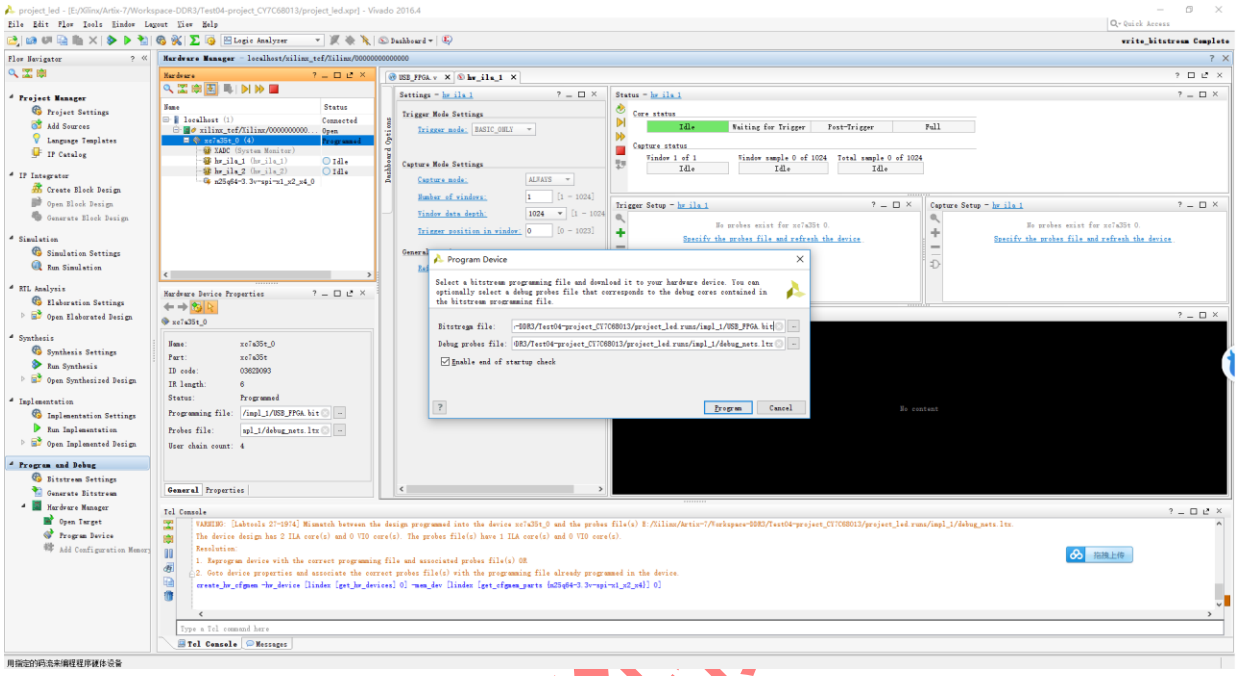


Figure 4-6. FPGA Program

Then, users need to download Slave FIFO firmware into CY7C68013A's internal RAM or external EEPROM. First step: Windows Start->Cypress->Cypress Suite USB 3.4.7->CyConsole:

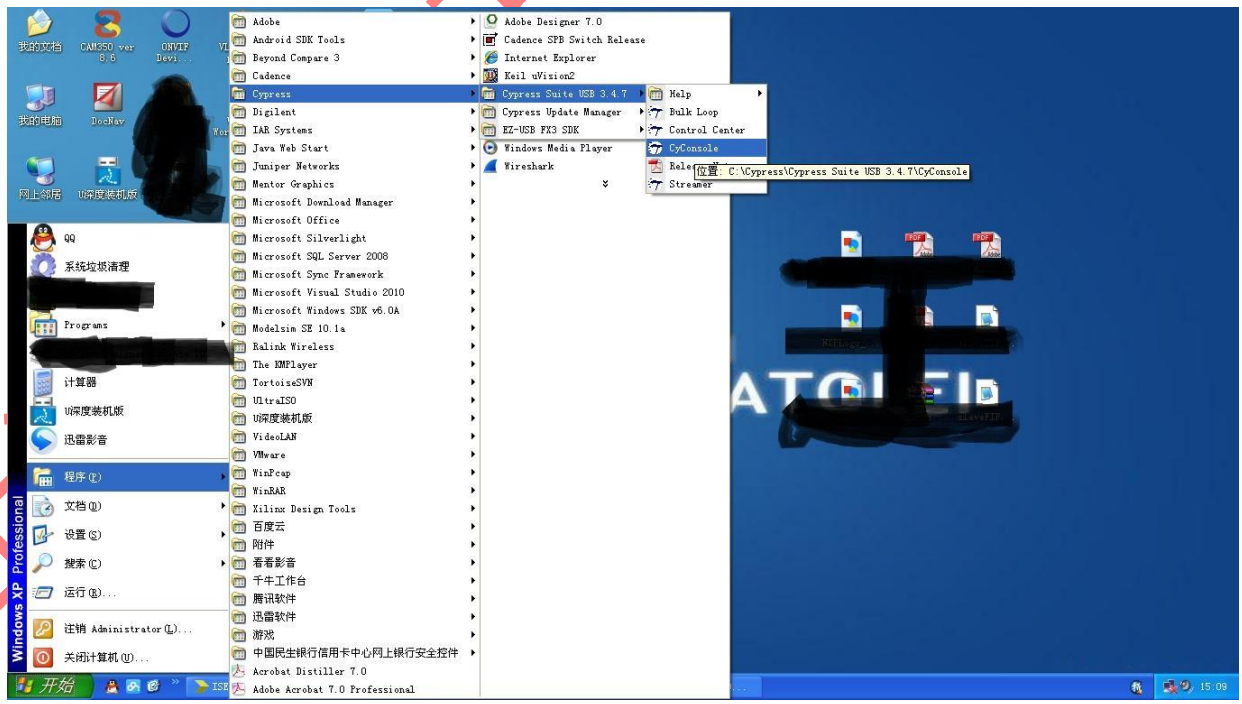


Figure 4-7. Open CyConsole Software

Click menu **Options**, select **EZ-USB Interface**:

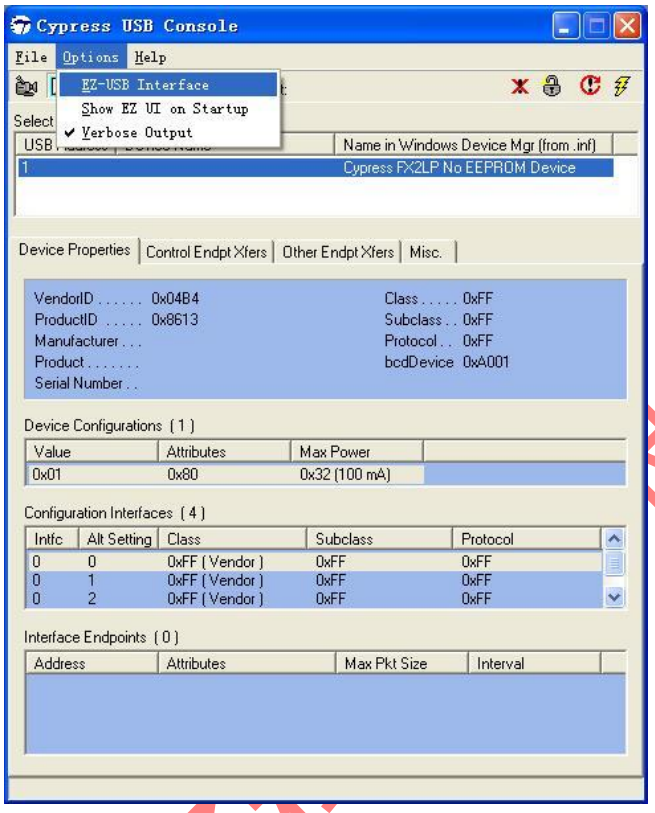
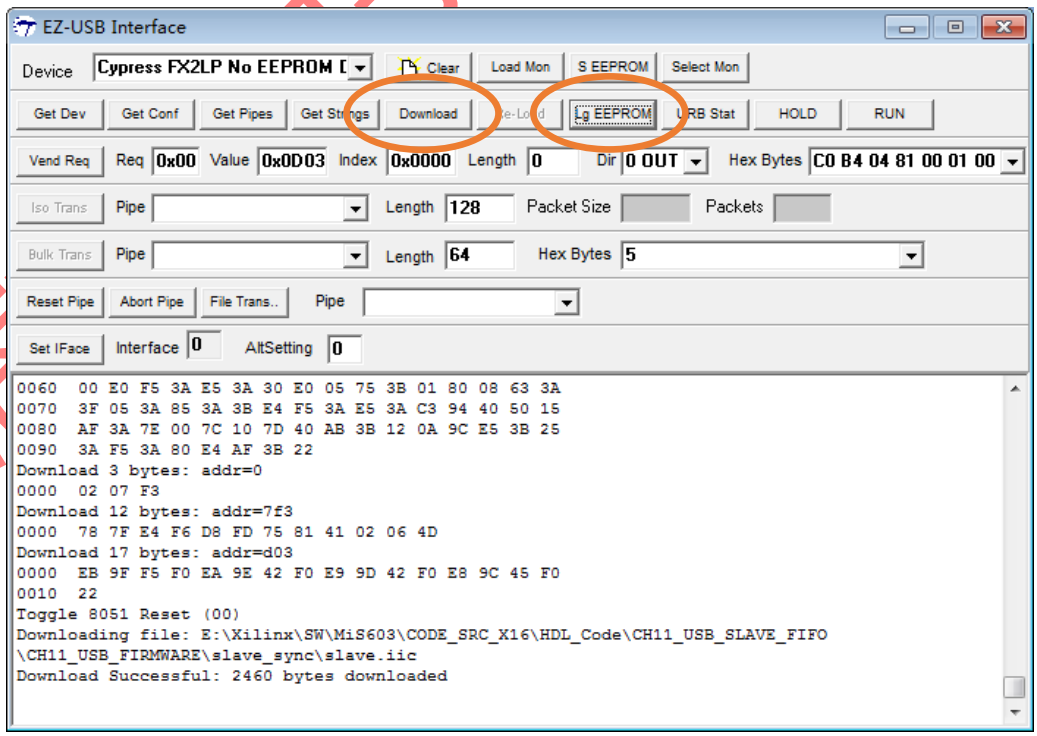


Figure 4-8. Choose EZ-USB Interface

The EZ-USB Interface displays the Device information: Cypress FX2LP No EEPROM Device:



Click **Download** button and select **Slave.hex**. The Slave.hex is located in Release folder: \software\Test04-CY7C68013_USB_FIRMWARE\USB_SLAVE_FIFO\USB_FIRMWARE\slave_sync。Notice: if users want to download firmware into external EEPROM, click **Lg EEPROM** and select **Slave.iic**.

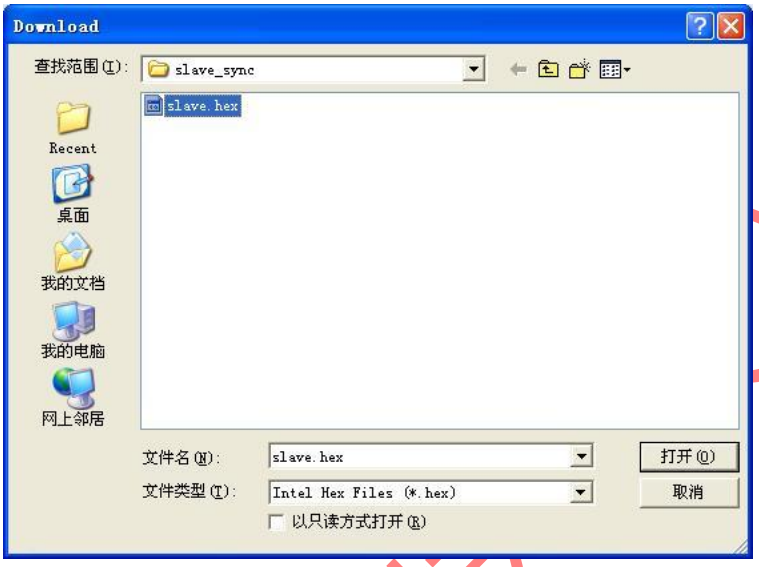


Figure 4-9. Program Slave.hex

After the Slave FIFO firmware successfully downloaded, the EZ-USB Interface will display new enumerated device: **QinMou-X16**。And then users could send 512 bytes of hex value 0x55 into USB **Endpoint 2 OUT** by clicking **Bulk Trans** button:

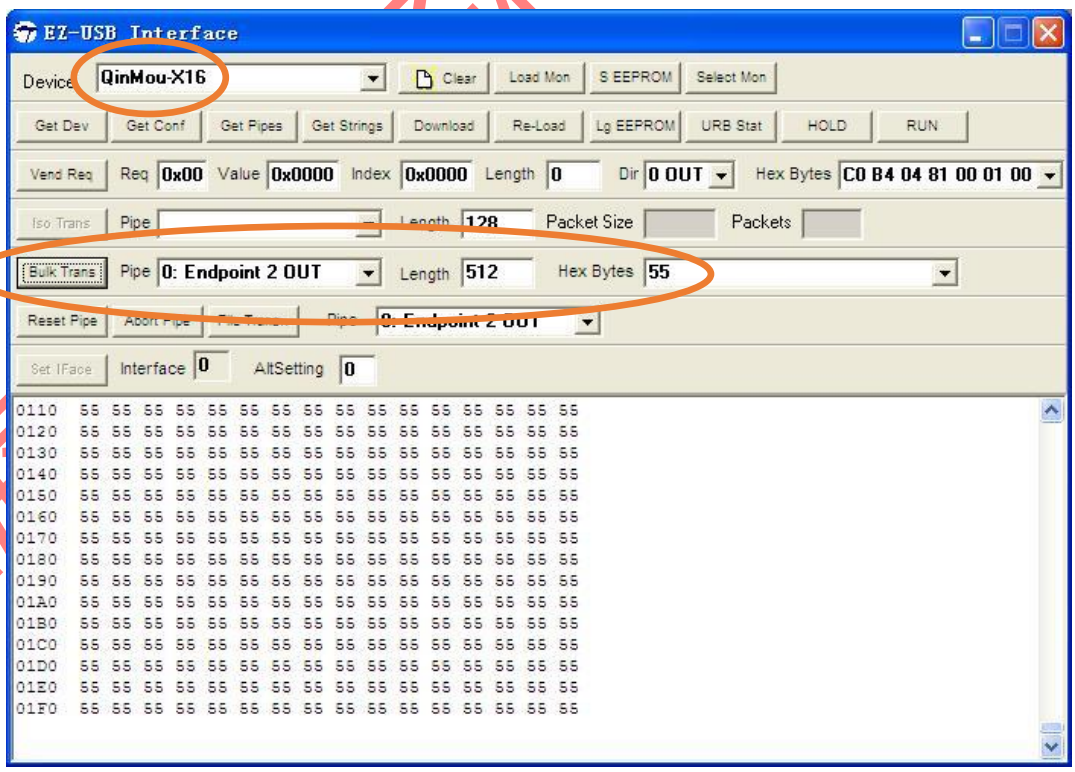


Figure 4-10. New QinMou-X16 Device and Send Test Datas

Then, change the **Pipe** selection into **Endpoint 6 IN**. After click the **Bulk Trans** button, the log window will display all the received data from USB Endpoint 6 IN. From below image, users could see all the 512 bytes of hex value 0x55 are correctly read back from Slave FIFO.

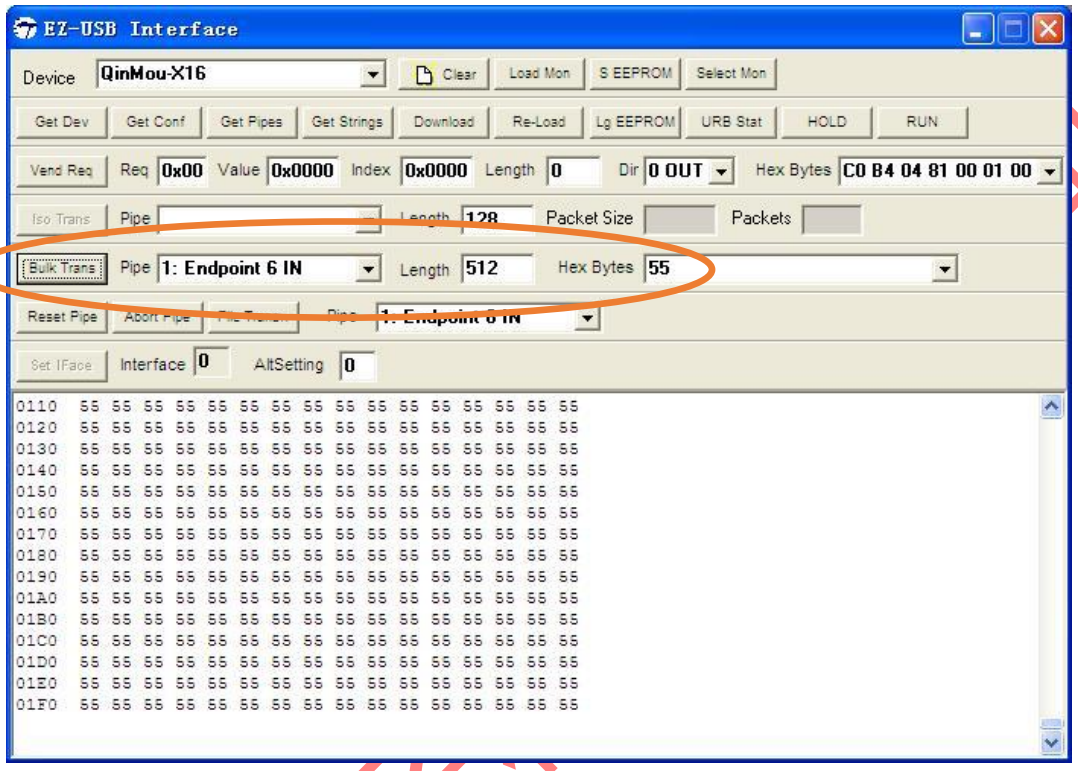


Figure 4-11. Receive Test Data

5. Reference

[1] ug380-Configuration.pdf
[2] ug385-Package.pdf
[3] ug394-Power Managment.pdf
[4] M25P80.pdf
[5] LPC-Link-II_Rev_C.pdf
[6] Xc7a35t-sdram-v02.pdf

6. Revision

Doc. Rev.	Date	Comments
0.1	11/07/2017	Initial Version.
1.0	11/18/2017	V1.0 Formal Release.