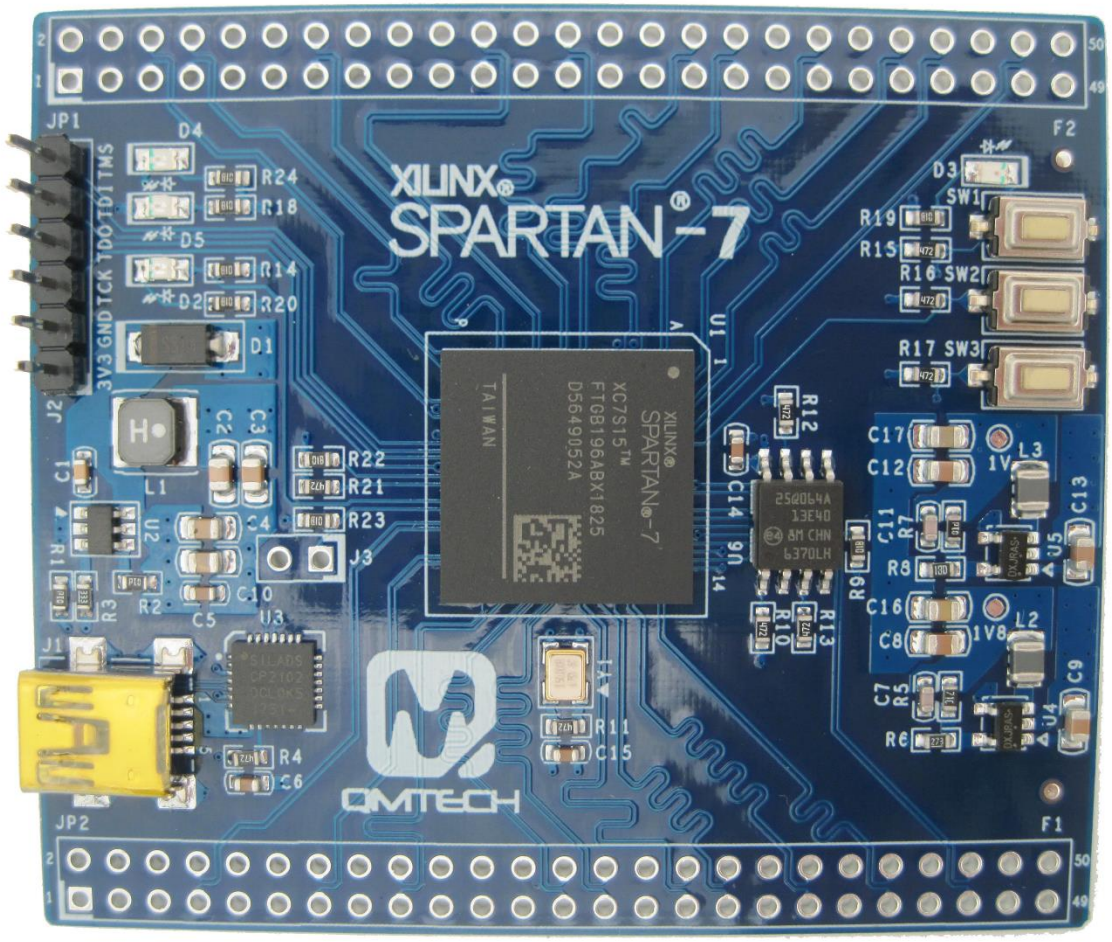
XILINX SPARTAN-7 CORE BOARD

USER MANUAL



Preface

The QMTech® Spartan-7 Core Board uses Xilinx XC7S15 device to demonstrate the newest addition to the Cost-Optimized Portfolio, offer the best in class performance per watt, along with small form factor packaging to meet the most stringent requirements. These devices feature a MicroBlaze™ soft processor running over 200 DMIPs with 800Mb/s DDR3 support built on 28nm technology. Additionally, Spartan-7 devices offer an integrated ADC, dedicated security features, and Q-grade (-40 to +125°C) on all commercial devices. These devices are ideally suited for industrial, consumer, and automotive applications including any-to-any connectivity, sensor fusion, and embedded vision.

Table of Contents

1. Introduction

1.1 Document Scope

This demo user manual introduces the QM_Spartan-7 development board and describes how to setup the development board running with application software Xilinx Vivado 2018.2. Users may employee the on board rich logic resource FPGA XC7S15-1FTGB196C to implement various applications. The development board has 88 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the QM_Spartan-7 development board:

- On-Board FPGA: XC7S15-1FTGB196C;
- On-Board FPGA external crystal frequency: 50MHz;
- XC7S15-1FTGB196C has rich block RAM resource up to 360Kb;
- XC7S15-1FTGB196C has 12,800 logic cells;
- On-Board N25Q064 SPI Flash, 8M bytes for user configuration code;
- On-Board 3.3V power supply for FPGA by using MP2359 wide input range DC/DC;
- QM_Spartan-7 development board has two 50p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- QM_Spartan-7 development board has 3 user switches;
- QM_Spartan-7 development board has 4 user LEDs;
- QM_Spartan-7 development board has JTAG interface, by using 6p, 2.54mm pitch header;
- QM_Spartan-7 development board has USB to UART Serial Port, by using Silicon Labs' CP2102-GMR chip.
- QM_Spartan-7 development board PCB size is: 6.6cm x 5.7cm;
- Default power source for board is from Mini USB: 1A@5V DC;

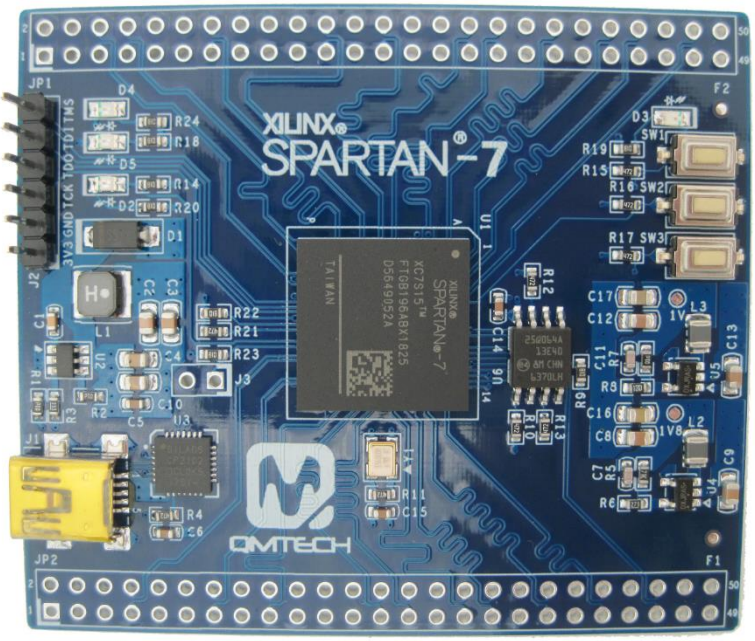


Figure 1-1. QM_Spartan-7 Development Board Overview

2. Getting Started

Below image shows the dimension of the QM_Spartan-7 development board: 6.6cm x 5.7cm. The unit in below image is millimeter(mm).

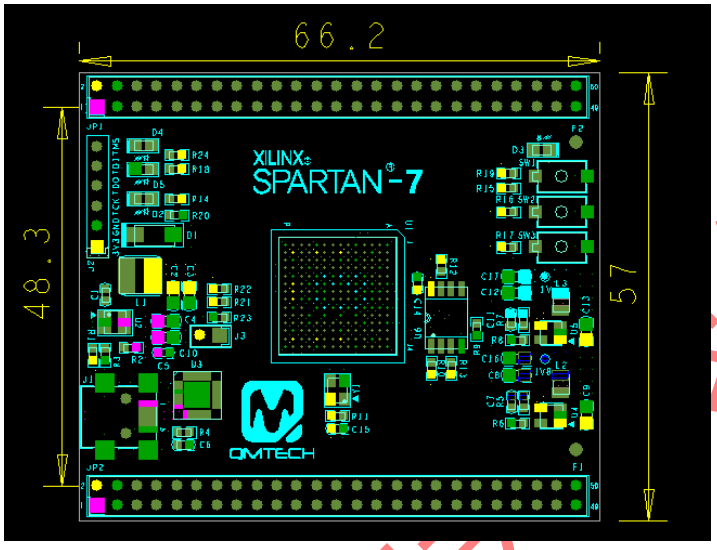


Figure 2-1. QM_Spartan-7 Development Board Dimension

2.1 Install Development Tools

The QM_Spartan-7 development board tool chain consists of Xilinx Vivado 2018.2, Xilinx USB platform cable, Mini USB cable for power supply. Below image shows the Xilinx Vivado 2018.2 development environment which could be downloaded from Xilinx office website:

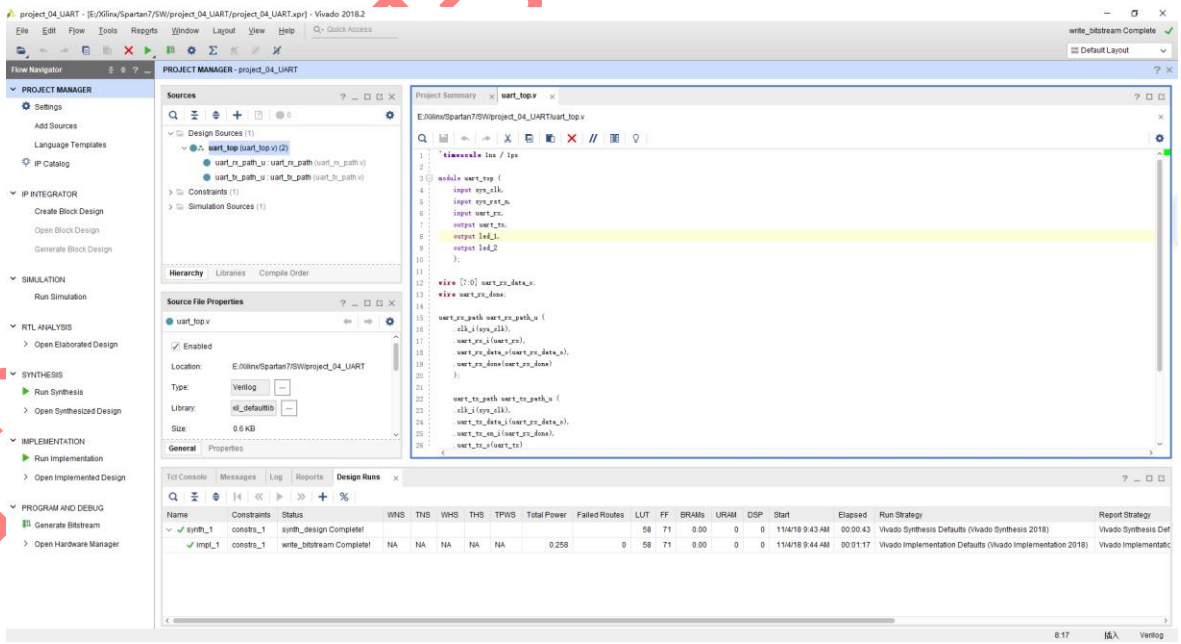


Figure 2-2. Vivado 2018.2

Below image shows the JTAG connection between Xilinx USB platform cable and QM_Spartan-7 development board:

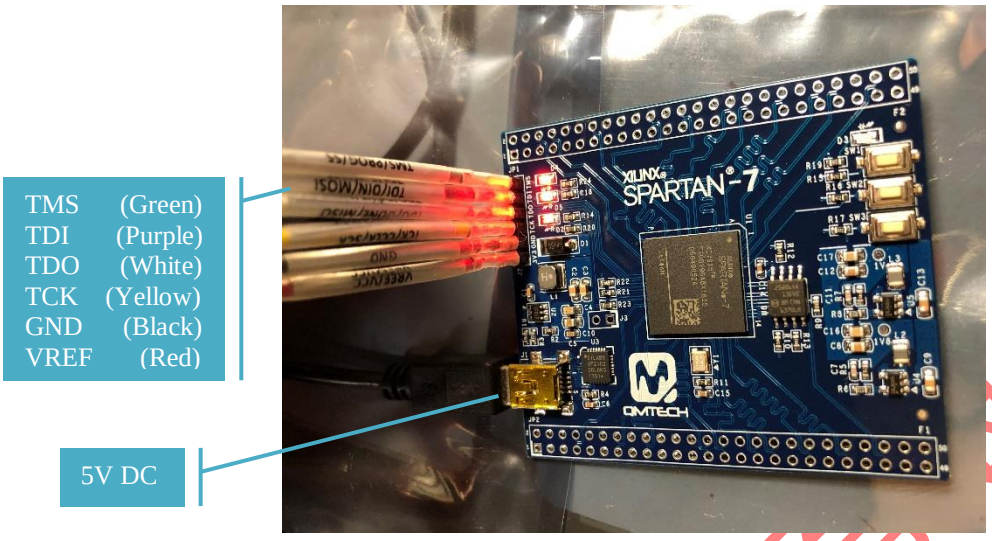


Figure 2-3. JTAG Connection and Power Supply

Once the FPGA test program is correctly 【Synthesized】, 【Implemented】 and 【Generated with Bitstream】, users may click the 【Open Target】 option to connect the XC7S15 FPGA.

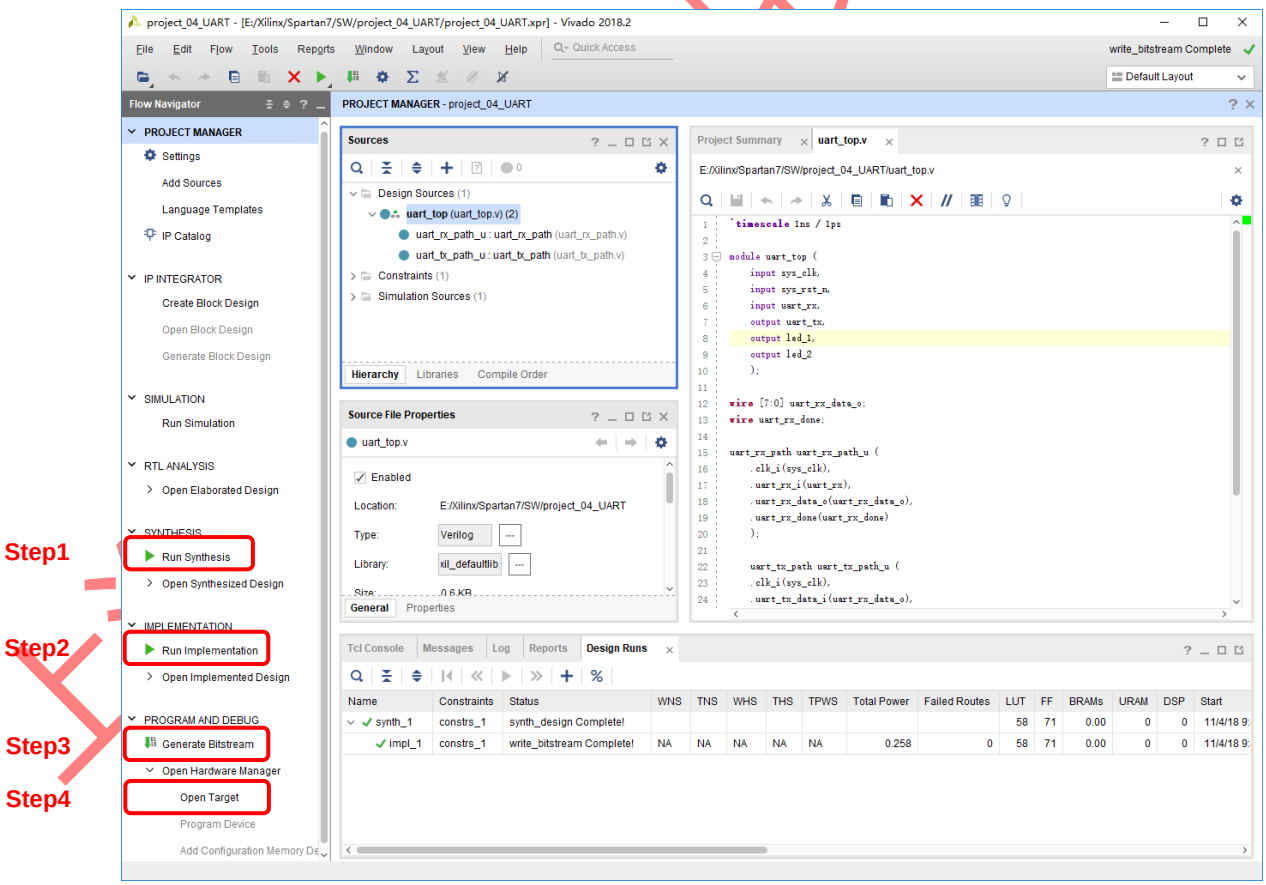


Figure 2-4. Vivado to Connect FPGA

Chip info like xc7s15_0(1) is shown in Hardware Manager as below image. Users then could right click the device to choose 【Program Device】to load the Bitstream *.bit into FPGA or to choose【Add Configuration Memory Device】to program the *.mcs file into on-board SPI flash.

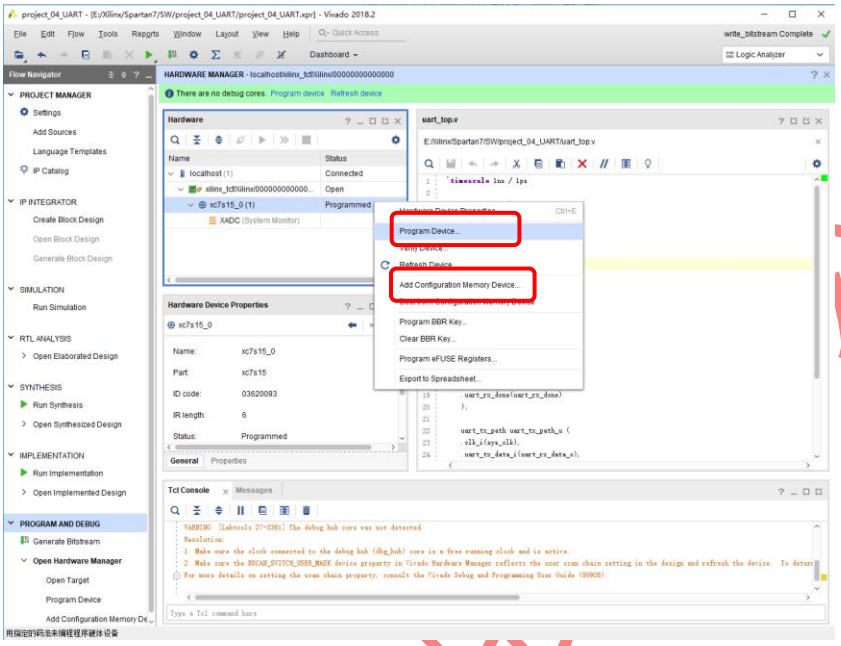


Figure 2-5. Program FPGA

Users could convert the *.bit file into the *.mcs file by using the Vivado tool. Choose the 【Tools】on the menu bar and then select 【Generate Memory Configuration File】, and then configure the parameters shown in below image:

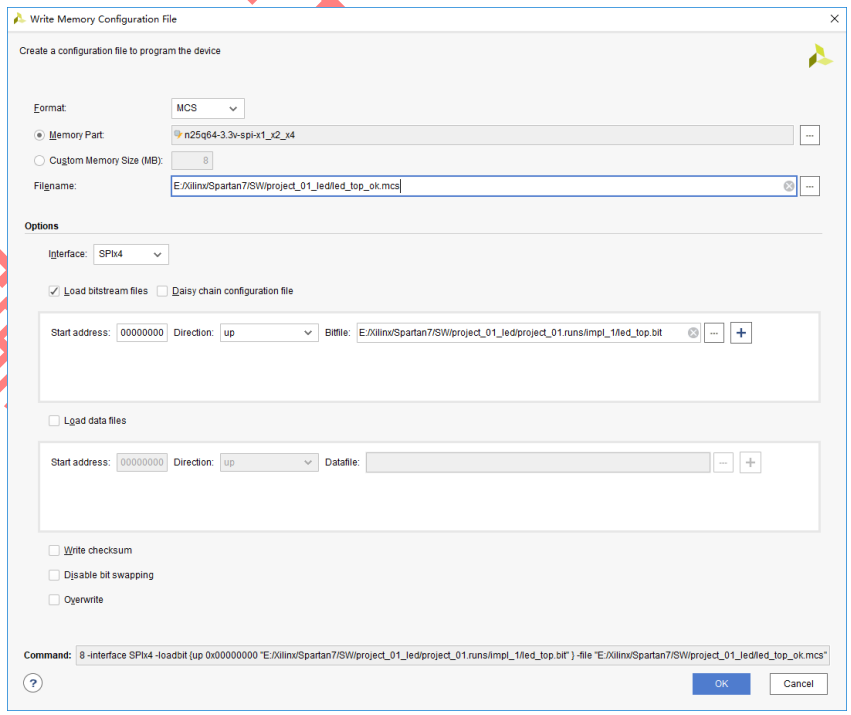


Figure 2-6. Generate *.mcs File

2.2 QM_Spartan-7 Hardware Design

2.2.1 QM_Spartan-7 Power Supply

The development board needs 5V DC input as power supply which could be directly injected from JP1/JP2 header or the Mini USB connector. Users may refer to the hardware schematic for the detailed design. The on board LED D5 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. Detailed design refer to hardware schematic.

Note: FPGA core supply 1.0V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.

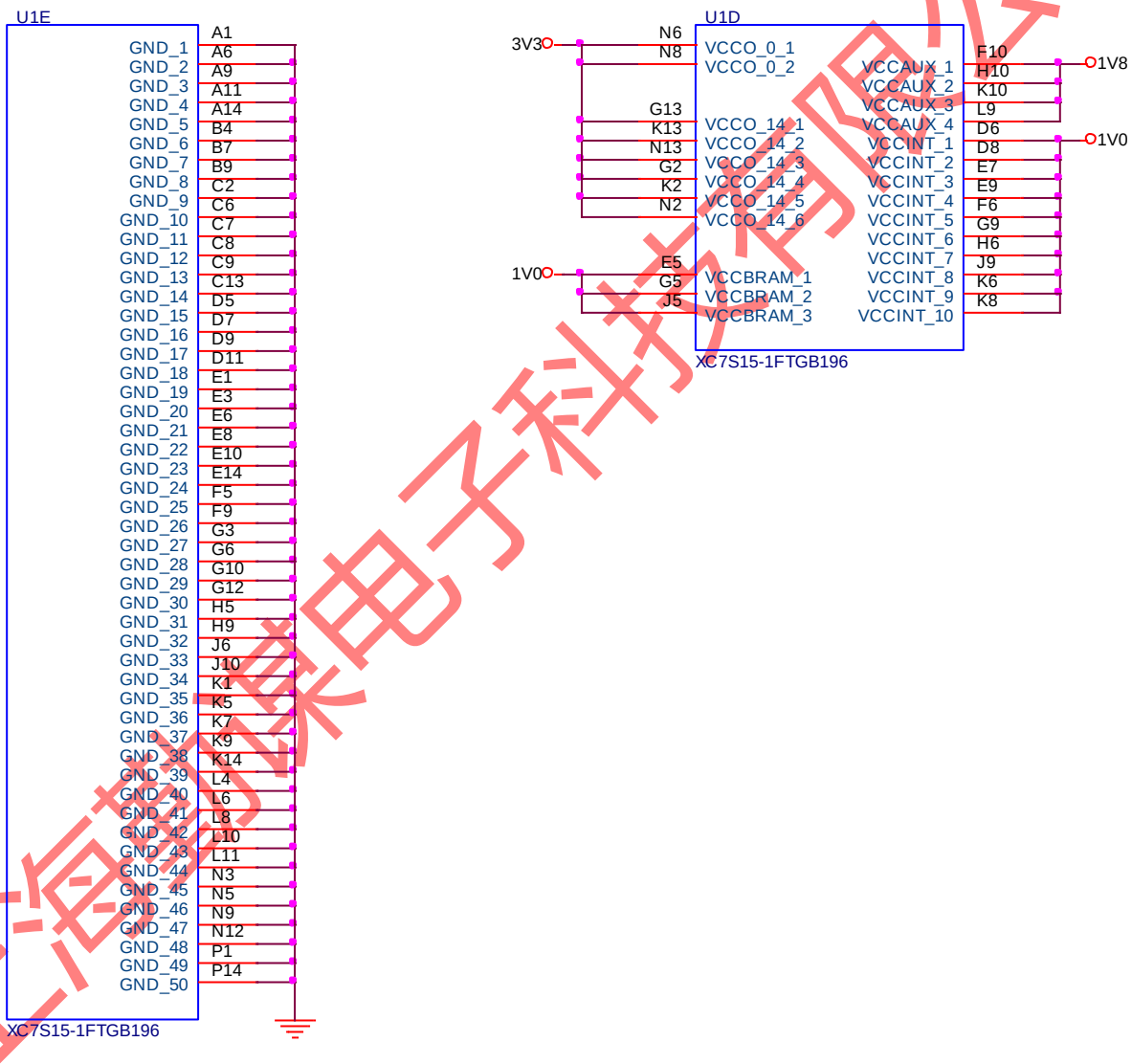


Figure 2-7. Power Supply for the FPGA

2.2.1 QM_Spartan-7 3.3V Power Supply

The development board's 3.3V power supply is using high efficiency DC/DC chip MP2359 provided by MPS Inc. The MP2359 supports wide voltage input range from 4.5V to 24V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the MP2359 hardware design:

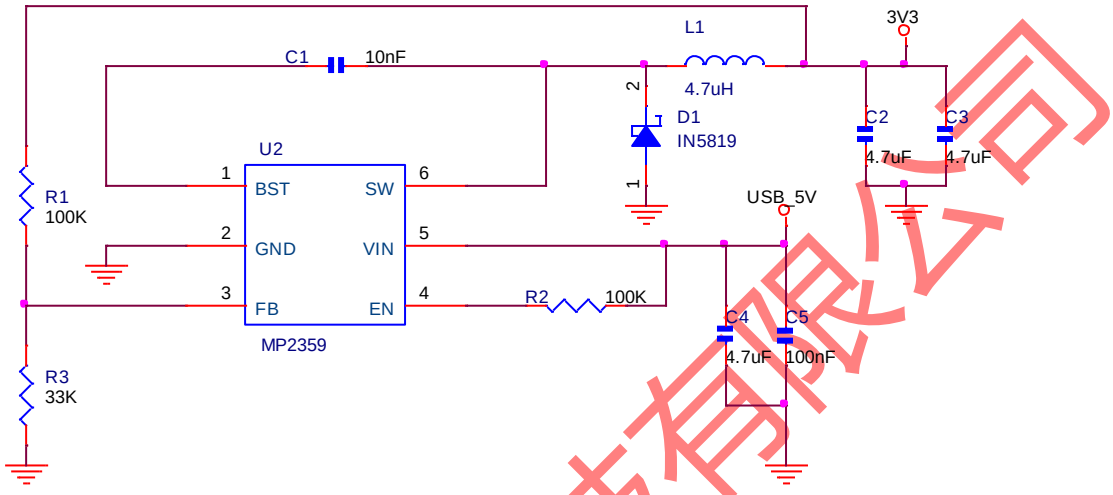


Figure 2-8. MP2359 Hardware Design

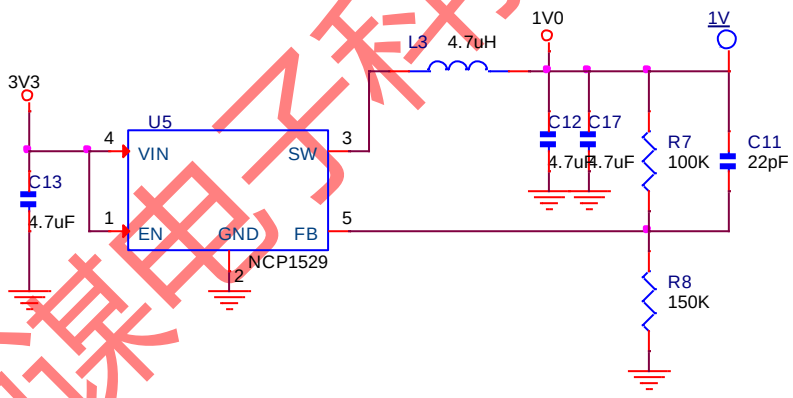


Figure 2-9. 1.0V Core Voltage DC/DC

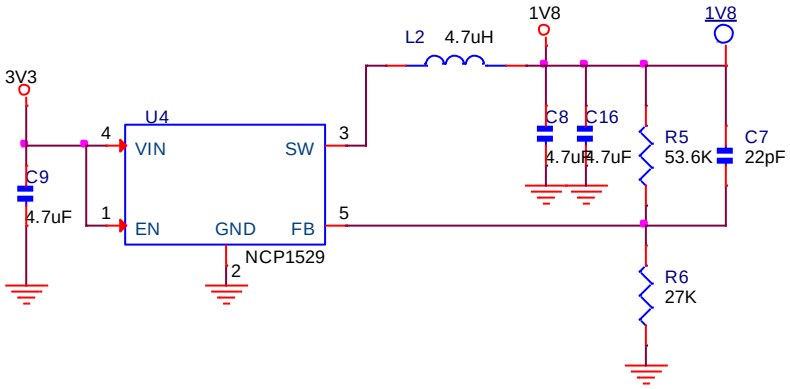


Figure 2-10. 1.8V AUX Voltage DC/DC

2.2.2 QM_Spartan-7 SPI Boot

In default, XC7S15 boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using N25Q064 manufactured by Micron, with 64Mbit memory storage.

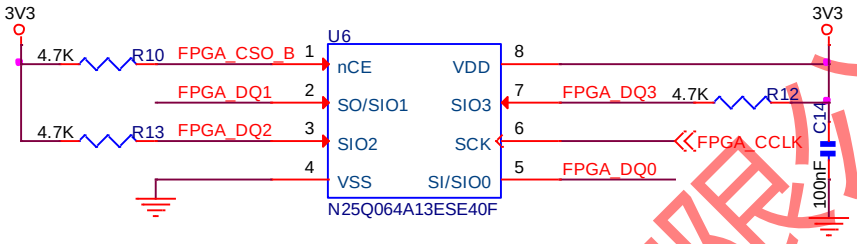


Figure 2-11. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on. In default, the jumper J3 is under open status.

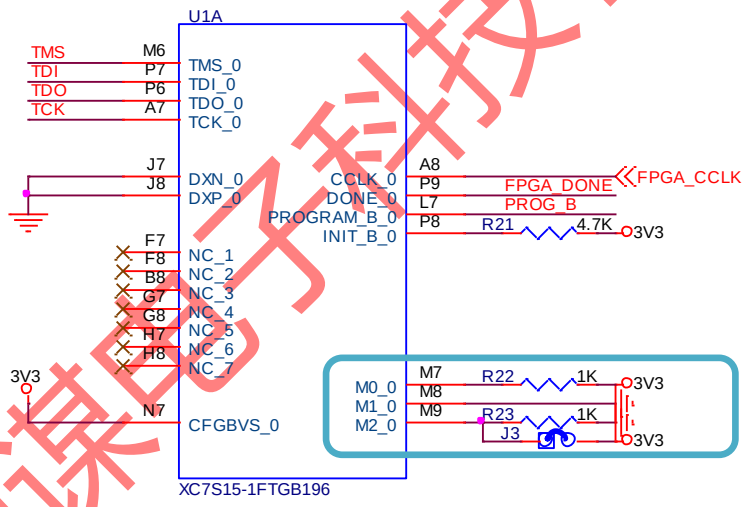


Figure 2-12. M0:M1 Hardware Settings

The LED D2 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D2 could be used as FPGA loading status indicator.

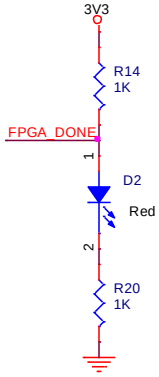


Figure 2-13. FPGA_DONE Status Indicator

2.2.3 QM_Spartan-7 System Clock

FPGA chip XC7S15-1FTGB196C has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

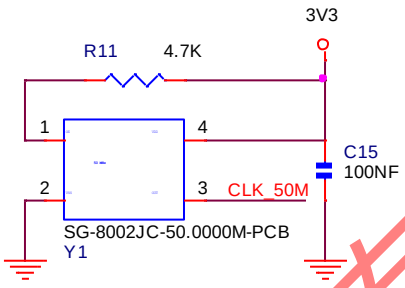


Figure 2-14. 50MHz System Clock

2.2.4 QM_Spartan-7 JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

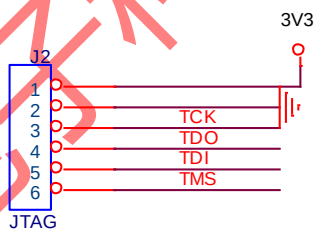


Figure 2-15. JTAG Port

2.2.5 QM_Spartan-7 User LED

Below image shows two user LEDs and one LED for 3.3V power supply indicator:

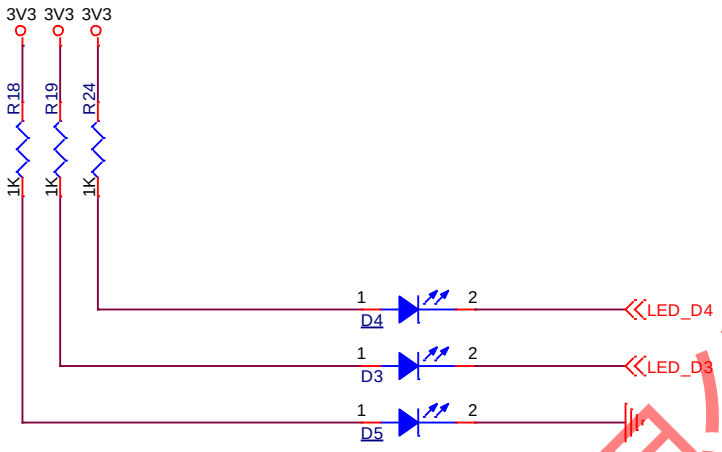


Figure 2-16. LEDs

2.2.6 QM_Spartan-7 Extension IO

The development board has two 50P 2.54mm pitch headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

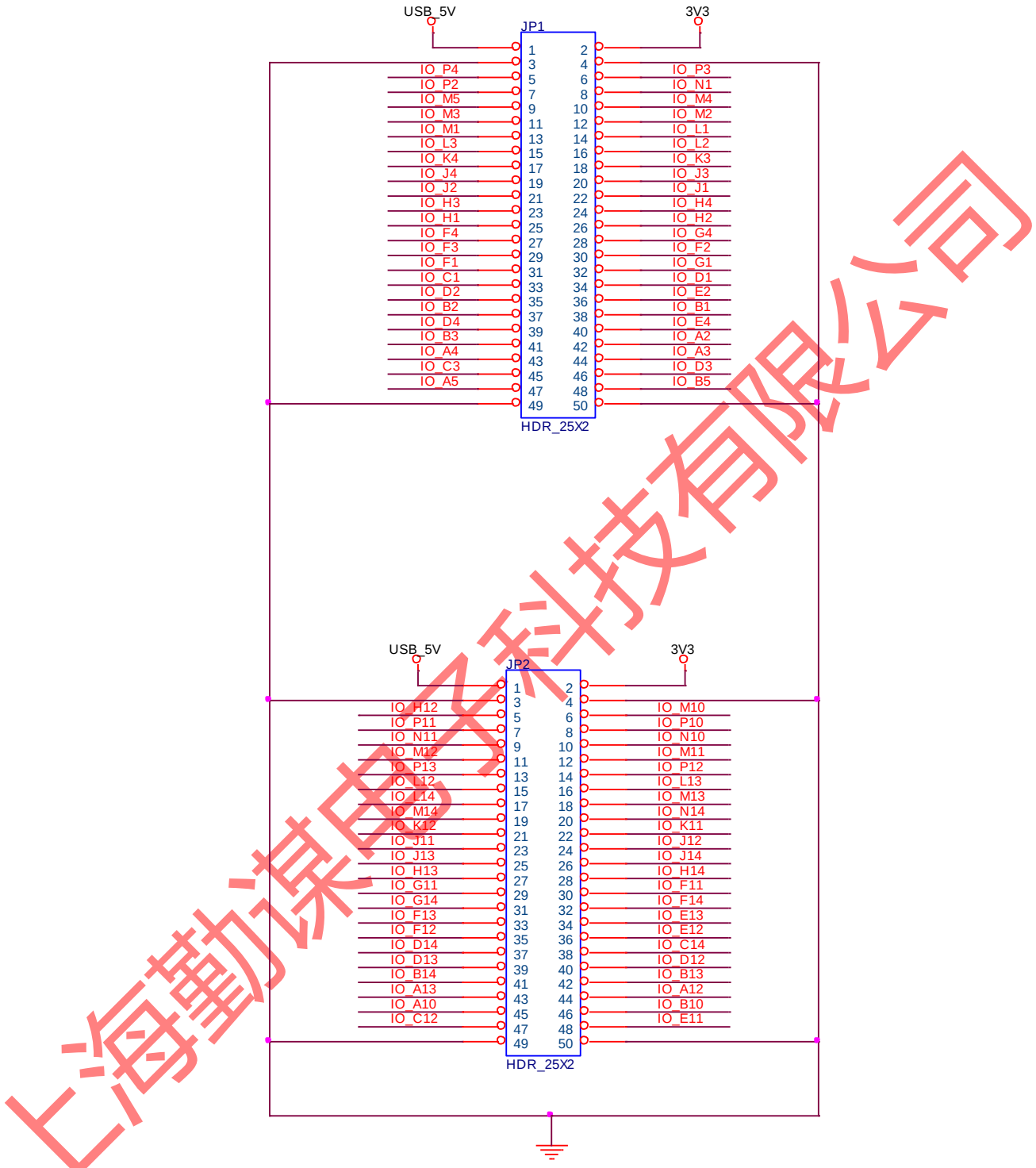


Figure 2-17. Extension IO

2.2.7 QM_Spartan-7 User Key

Below image shows the PROGRAM_B key and two user keys:

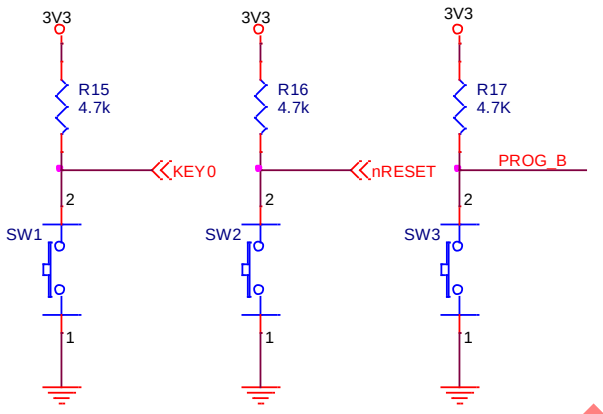


Figure 2-18. Keys

2.2.8 QM_Spartan-7 UART Port

The CP2102-GMR is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102-GMR includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CP2102-GMR on the QM_Spartan-7.

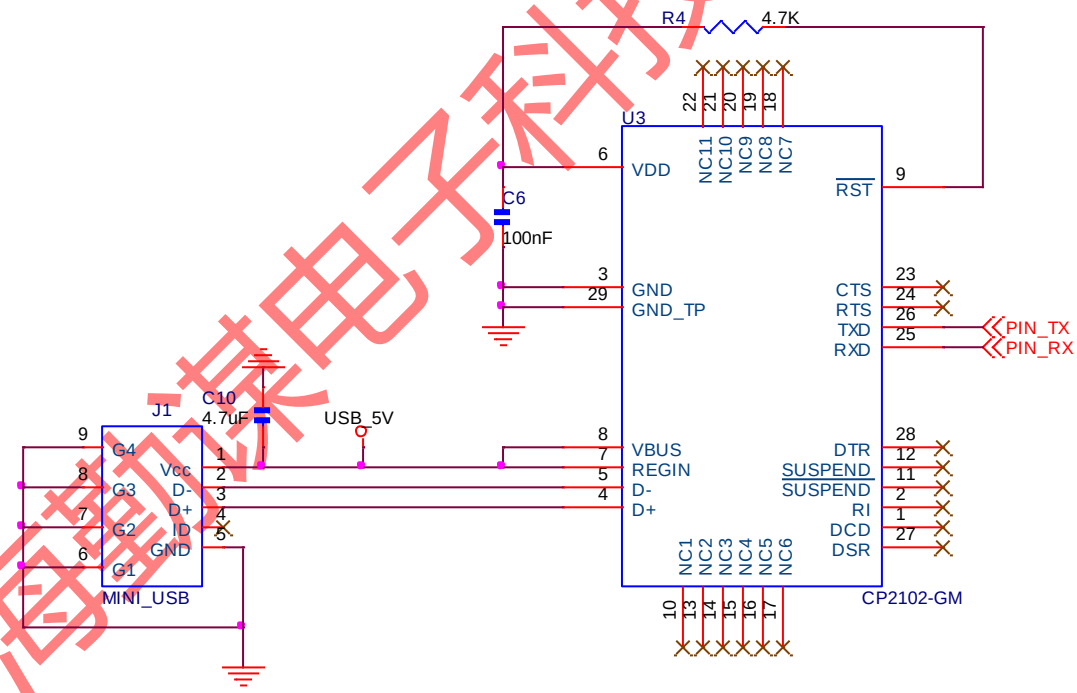


Figure 2-19. UART Port

3. Reference

[1] ug470_7Series_Config.pdf
[2] ds181_Artix_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] n25q_64a_3v_65nm.pdf
[5] MP2359.pdf
[6] NCP1529-D.PDF

4. Revision

Doc. Rev.	Date	Comments
0.1	05/12/2018	Initial Version.
1.0	05/12/2018	V1.0 Formal Release.