QM_CYCLONE10_10CL006 DB

USER MANUAL (QUARTUS 17.0)



Preface

The QMTech® Cyclone 10 Core Board uses Intel® (Altera) 10CL006 device to demonstrate the industry's lowest system cost and power, along with performance levels that make the device family ideal for differentiating your high-volume applications. All Intel® Cyclone® 10 LP FPGAs require only two core power supplies for operation, simplifying your power distribution network and saving you board costs, board space, and design time. The flexibility of the Intel® Cyclone® 10 LP FPGA enables you to design in a smaller, lower cost device, lowering your total system costs.

Users could visit QMTECH official website from here: http://www.chinaqmtech.com/

Table of Contents

1. QUARTUS PRIME 17.0 INSTALLATION	1. QUARTUS PRIME 17.0 INSTALLATION		
PEGA PROJECT COMPILE, *.SOF DOWNLOAD AND *.JIC PROGRAM7 2.1 CREATE NEW PROJECT	PGA PROJECT COMPILE, *.SOF DOWNLOAD AND *.JIC PROGRAM7 2.1 CREATE NEW PROJECT	1.	QUARTUS PRIME 17.0 INSTALLATION
2.1 CREATE NEW PROJECT 7 2.2 COMPILE THE PROJECT 12 2.3 PIN ASSIGNMENT 13 2.4 DOWNLOAD *.SOF INTO FPGA 15 2.5 PROGRAM *.JIC INTO SPI FLASH 18 3. SIGNALTAP II LOGIC ANALYZER 22 4. REFERENCE 26 5. REVISION 27	2.1 CREATE NEW PROJECT 7 2.2 COMPLE THE PROJECT 12 2.3 PIN ASSIGNMENT 13 2.4 DOWNLOAD*SOF INTO PPGA 15 2.5 PROGRAM * JICINTO SPI FLASH 18 3. SIGNALTAP II LOGIC ANALYZER 22 4. REFERENCE 26 5. REVISION 27	2.	FPGA PROJECT COMPILE, *.SOF DOWNLOAD AND *.JIC PROGRAM 7
3. SIGNALTAP II LOGIC ANALYZER	3. SIGNALTAP II LOGIC ANALYZER		2.1 Create New Project
4. REFERENCE	4. REFERENCE	3.	SIGNALTAP II LOGIC ANALYZER
5. REVISION	5. REVISION	4.	REFERENCE
		4. 5.	REFERENCE



Quartus Prime 17.0 Installation 1.

The revolutionary Intel® Quartus® Prime Design Software includes everything you need to design for Intel® FPGAs, SoCs, and CPLDs from design entry and synthesis to optimization, verification, and simulation. Dramatically increased capabilities on devices with multi-million logic elements are providing designers with the ideal platform to meet next-generation design opportunities.

The Intel® Quartus® Prime Software design flow comprises of the following high-level steps:



The Quartus Prime software version 17.0 supports the following device families: Stratix IV, Stratix V, Arria II, Arria V, Arria V GZ, Arria 10, Cyclone 10 LP, Cyclone IV, Cyclone V, MAX I, MAX V, and MAX 10 FPGA. Below image shows the startup UI of Quartus II Prime 17,0:

Te té Vez Pagid Assymption Processo Tropic Comparison Nerrar City Accompation Nerrar City	Train Window Hell	CONTRACTOR NORMAL CONTRACTOR NORMAL CONTRACTOR NORMAL CONTRACTOR NORMAL CONTRACTOR CONTE	Documentation Training	About Quartus Prime X Sourts Prese Version 15.18 Built 165 1021/2015 5J Sandwrd Editor Patches Installed Tione	Second ables com
Image: Project Resignation Image: Project Resignation Image: Project Resignation	b Start	Comparing New Project Wizard	Documentation Training Support	About Quartus Prime X Sourius Prime Versan 15.1.0 Built 165 10010015 5J Standard Editor Patches installed: Nore	P Colleg P Colleg
Project Langulor I angulor	Start	New Project Wizard	C Documentation Training Support	About Quartus Prime X Sourban Prime Venansi 11.1 8 Built 165 10212011 5.1 Sandard Editer Petches Installer: Nore	P Catalog 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Compliation Herarchy	Start	Designing New Project Wizard	Documentation Training	About Quartus Prime X About Quartus Prime Versen 15.10 Built 105 1021/2015 SJ Standard Editor Patches Installer Note	Device Family (Syctome V(EldocotTisUsEUST) *
	F	New Project Wizard	Documentation Training	About Quartus Prime X About Quartus Prime X Dantus Prese Vesson 15.15 Built 155 102102155 5J Standard Editor Photoes Installed: Nore	V Restance P Very Project Directory No Selection Available Ubrary Basic functions Dose
		New Project Wizard	Coursentation	About Quartus Prime X About Quartus Prime X Quartus Prime Version 15.1.8 Build 165 150210215 SJ Standard Editor Patches Installed None	Vision Constants Vision Constants Vision Constants Vision Constants Vision Constants Dep
		New Project Wizard	Training	Quartus Prime Version 15. 1.0 Build 185 10/21/2015 SJ Standard Edition Patches Installed: None	No Selection Available Library Basic Functions DSP
		New Project Wizard	Training Support	Patches Installed: None	Library Basic Functions DSP
		•	Support		> DSP
		•	Support		
		•••		Convirient (C) 1991-2015 Altera Corporation All rights reserved. Quarturs is a	> Interface Protocols
		and the second se	What's New	outprogram to the second secon	Memory Interfaces and Controllers Processors and Perpherals University Descent
		· 1	Matification Contex	and are the copyrighted property of third parties.	Search for Partner IP
		Open Project	Monication Center		
	1				
	Recei	nt Projects			
		DE0_CV_SDRAM_Nios_Test.qpf (E /Altera/Software/ Test07_USB_Slave_FIFO.qpf (E /Altera/Software/Te Test06_project_ADV7123_VGA.qpf (E /Altera/Softwa		international treaties. Unauthorized reproduction or distribution of this program, or any protein of it, may result in severe out and criminal penalties, and will be prosecuted to the maximum extent possible under the law.!	
				ОК Нер	
	Close	page alter project load			
	L) Dont	show this screen again			+ 451

Figure 1-1. Quartus II Prime 17.0

After the Quartus II Prime 17.0 is correctly installed, users still need to install the device package from Intel official website. Below lists the download center address:

https://www.intel.com/content/www/us/en/programmable/downloads/download-center.html

In the Intel Download Center website, select the tab of ' Select by Device' and then all the available device packages will be listed as below image. The device used in this user manual is Cyclone10 LP series and the detailed chip part number is 10CL006YU256C8G, so please download the device package for Quartus II 17.0: cyclone10lp-17.0.0.595.qdz.









Below window will pop up and click Next:

🕥 Installing Quartus Prim	e Standard Edition 17.0.0.595 Devices	_		×	
	Setup - Quartus Prime Standard Edition 17.0.0.595 Devices				
intel	Welcome to the Quartus Prime Standard Edition 17.0.0.595 Devices Setup Wizar	d.			
	The Quartus Prime software requires that your system have sufficient physical RAI targeting specific devices. You can check the "Memory Recommendations" secti Prime Software and Device Support Release Notes" (https://www.altera.com/sup m.html) for detailed memory requirements for a particular device.	M to co ion in th pport/lit	mpile desi e "Quartu erature/lit-	gns s	\wedge
	For more information about Intel FPGA software, go to http://www.altera.com.				
					7
	< Back Next	:>	Cano	el	

Figure 1-4. Install Device Package

Choose the Download Directory where contains the cyclone10lp-17.0.0.595.qdz file:

S Installing Quartus Prime Standard Edition 17.0.0.595 Devices	-		×
Download Directory		(int	el
Specify the directory that contains the Quartus Prime device files (.qdz). Download directory: C:\Users\evelovely\Downloads			
If you need to download device support files, you can download them from the Download Center page of the Int <u>http://dl.altera.com/?edition=standard/#tabs-2</u>	el FPGA	website:	
InstallBuilder	>	Cano	el :





 Installing Quartus Prime Standard Edition 17.0.0.595 Devices
 ×

 Select Components

 Select the components you want to install

 Image: Components

 Image: Components

 Image: Components

 </td

Choose the device package needs to be installed and click Next:

Figure 1-6, Install the Device Package

User could also install the device package by using Quartus II Prime 17.0 Device Installer directly:



Figure 1-7. Device Installer



2. FPGA Project Compile, *.sof Download and *.jic Program

2.1 Create New Project

Click [File] \rightarrow [New Project Wizard...] to create a new project:



Figure 2-2. New Quartus Prime Project



In below [New Project Wizard] page, choose Next:

🕥 New Project Wizard		×
Introduction		
The New Project Wizard helps you create a new project and preli	iminary project settings, including the following:	
Project name and directory Name of the top-level design entity Project files and libraries Target device family and device EDA tool settings You can change the settings for an existing project and specify a use the various pages of the Settings dialog box to add functional	additional project-wide settings with the Settings command (Assignments menu). You car lify to the project.	
		7
Don't show me this introduction again		
	< Back Next > Einish Cancel Help	

Figure 2-3. New Project Wizard

Set the target working folder below 【What is the working directory for this project?】. Set the new project name below 【What is the name of this project?】. And finally set the example project name: Test01_Project_LED shown as below.

	🕥 New Project Wizard
	Directory, Name, Top-Level Entity
	What is the working directory for this project?
	E:/test
	What is the name of this project?
	Test01_Project_LED
	What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
	Test01_Project_LED
	Use Existing Project Settings
× ×	<u></u>
\sqrt{N}	
	< <u>Back</u> <u>Next</u> <u>Finish</u> Cancel <u>H</u> elp

Figure 2-4. Set Working Directory and Project Name



Select [Empty Project] and then click Next:

S New Project Wizard	×
Project Type	
Select the type of project to create.	
Empty project	-
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.	
Project template Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the <u>Design Store</u> .	
< <u>B</u> ack <u>N</u> ext> Einish Cancel <u>H</u> elp	

Figure 2-5. Create Empty Project

If user already has some source code, please add all these necessary files in this step:

	Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.	
	Elle name:	<u>A</u> do
	٩	X Add
	File Name Type Library Design Entry/Synthesis Tool HDL Version	Remo
		Up
		Dow
•		Proper
_X-X,		
Y		

Figure 2-6. Add Source Code



Choose the FPGA Chip number: 10CL006YU256C8G

	n of the Quartus Prin	ne software	in which your	target device is su	menu. pported, refer to the	e <u>Device Support List</u> webpage.	
Device family				Show in 'Availabl	e devices' list		
Eamily: Cyclone 10 I	P		•	Pac <u>k</u> age:	UFBGA	•	
Dev <u>i</u> ce: All			~	Pin <u>c</u> ount:	256	•	
Target device				Core speed grade	e: 8	•	
	ad housing Sinter			Name filter:			
	ed by the Fitter			Show advanc	ed devices		
O Other: n/a	A A A A A A A A A A A A A A A A A A A	vices use		Device and Pin Op	tions		17
vailable devices:							
Name	Core Voltage	LEs	Total I/O	s GPIOs	Memory Bits	Embedded multiplier 9-	
10CL006YU256C8G	1.2V	6272	177	177	276480	30	
10CL010YU256C8G	1.2V	10320	177	177	423936	46	
	1.21/	15408	163	163	516096	112	
10CL016YU256C8G	1.2.*						
10CL016YU256C8G 10CL025YU256C8G	1.2V	24624	151	151	608256	132	

Figure 2-7. Select Device

Summary page will be shown and click [Finish it there's nothing needs to be changed:

🕥 New Project Wizard		×
Summary		
,		
When you click Finish, the project will be created with t	he following settings:	
Project directory:	C:/Users/evelovely/Desktop	
Project name:	Test01-LED	
Top-level design entity:	Test01-LED	
Number of files added:	0	
Number of user libraries added:	0	
Device assignments:		
Design template:	n/a	
Family name:	Cyclone 10 LP	
Device:	10CL010YU256C8G	
Board:	n/a	
EDA tools:		
Design entry/synthesis:	<none> (<none>)</none></none>	
Simulation:	<none> (<none>)</none></none>	
Timing analysis:	0	
Operating conditions:		
VCCINT voltage:	1.2V	
Junction temperature range:	0-85 °C	
	< <u>B</u> ack <u>N</u> ext > <u>F</u> inish Cancel	Help

Figure 2-8. Project Summary Page



V



After the Empty Project created, below image will be shown:



Users may add example source file Test01_Project_LED.v into this Empty Project shown as below:



Table 2-3. Add Source File





After the newly added source file loaded into project, user can view the source code shown as below:

Figure 2-9. View of Source Code

2.2 Compile the Project

Users could use the button [Start Compilation – Ctrl + L] shown in below image to compile the project:







There will be compilation report after the compile finished, in which shows the info like logical element resource usage, how many PLLs are used, etc. Below image shows an example Compilation Report:

•	•		•	· ·		•
🕥 Quartus Prime Standard Edition - E:/Alte	era/MAX10/Software/Test01_LED/Test	01_LED - Test01_LED			- C	×
<u>File Edit View Project Assignments Pro</u>	cessing <u>T</u> ools <u>W</u> indow <u>H</u> elp 🤜				Search altera.com	n 🍯
□ た 日 + □ □ つ で Test01	LED 👻 🏒 🗳 🤇	🗳 🚸 💷 🕨 🖌 🧏 🔤 🎯) 🕹 👋 🚂			
Project Navigator 🔥 Hierarchy 🔹 💻 🗗 🛪	Test01_LED.v	🗵 👇	Compilation Report - Test01_LED			
Entity:Instance	Table of Contents 📮 🗗	Flow Summary				
MAX 10: 10M02SCU169C8G	Flow Summary	Flow Status	Successful - Mon Apr 23 22:27:50 2018 15 1 0 Ruid 195 10/21/2015 SL Standard Edition			
ស៊ីថី Test01_LED វាំង	Fiow Settings Fiow Non-Default Global Settings Fiow Non-Default Global Settings Fiow Elapsed Time Fiow Clog Fow OS Summary Fiow Usg Assembler Fitter PowerPlay Power Analyzer Fibw Messages	Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total combinational functions Dedicated logic registers Total registers Total registers	Test01_LED Test01_LED MAX 10 10M02SCU169C8G Final 64 / 2,304 (1 3 %) 64 / 2,304 (1 3 %) 34 / 2,304 (1 %) 34 4 / 130 (3 %)			
	Flow Suppressed Messages TimeQuest Timing Analyzer	Total virtual pins Total memory bits Embedded Multiplier 9-bit elements	0 0/110,592(0%) 0/32(0%)			
		Total PLLs	0/1(0%)			
<	< > >	UFM blocks	0/1(0%)			
Type ID Message A 332148 Timing requireme > 0 332146 Worst-case setup > 0 332140 Norst-case setup > 0 332140 Norst-case setup 0 332140 No Recovery path 0 332140 No Recovery path 0 332140 Vorst-case minim 0 332102 Design is not fu 0 32102 Design is not fu 0 Quartus prime Ti 0 293000 Quartus prime Ti	nts not met slack is -1.000 slack is 0.252 s to report to report um pulse width slack is -3. lly constrained for hold re mequest Timing Analyzer was ll Compilation was successf	000 equirements quirements successful. 0 errors, ul. 0 errors, 12 warnin	4 warnings gs			>
2 System Processing (123)						-
					100%	00:01:22

2.3 PIN Assignment

There are several ways to assign the Pins for the example project. Method 1: Choose [Assignment] \rightarrow [Pin Planner]:

Compilation Report

Figure 2-11.

	🕥 Quartus Prime Standa	rd Edition Ev/Altors/MAX10/Software/Te	ost01_LED/	Test	01_LED - Test01_LED		- C	ı ×
1	File Edit View Project	Assignments Processing Tools Window	v Help	•			Search altera.com	6
1	🗋 🗖 🖶 🗹 🗂 💼	Device		6 (5 🚸 💷 🕨 🖌 🤘 🚫	A 🔌 🚂		
P	roject Navigator 🝌 Hierarchy	Settings Ctrl+S	Shift+E).v	🗵 👇	Compilation Report - Test01_LED		
-	Entity	SAssignment Editor Ctrl+S	Shift+A	₽ ₽	Flow Summary			
	MAX 10: 10M02SCU169C8	Pin Planner Ctri+S	Smitt+N		Flow Status	Successful - Mon Apr 23 22:27:50 2018		^
	😳 Test01_LED 📥	Remove Assignments			Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Standard Edition		
		Back-Annotate Assignments	iet	ttings	Top-level Entity Name	Test01_LED		
		Import Assignments			Family	MAX 10		
		Export Assignments			Device	10M02SCU169C8G		
		Assignment Groups			Timing Models	Final		
		A Logislock Register Mindow ANJ			Total logic elements	64/2,304(3%) 64/2,304(3%)		
		EdgicLock Regions Window Alt+E			Dedicated logic registers	34/2.304(1%)		
		Partitions window Alt+D	ver Analyzer		Total registers	34		
		Flow Messages	s		Total pins	4 / 130 (3 %)		
		Flow Suppresse	ed Messages	s	Total virtual pins	0		
		> TimeQuest Timin	ng Analyzer		Total memory bits	0/110,592(0%)		
-					Total PLLs	0/12(0%)		
	¢	> <		>	UFM blocks	0/1(0%)		
	*			-				
	A Type 10 Mes	ing requirements not met						
	A 332146 Wors	st-case setup slack is -1.000						
	■ 332146 Wors	st-case hold slack is 0.252						
	332140 No I	Recovery paths to report						
	0 332140 No I	Removal paths to report	1	~ ~				
	332140 WOF:	ion is not fully constrained f	TACK 15 ·	-3.(n re	ouuirements			
	332102 Des	ion is not fully constrained f	for hold	rec	auirements			
	Quai	rtus Prime TimeQuest Timing An	nalyzer v	was	successful. 0 errors, 4	warnings		
	0 293000 Quai	rtus Prime Full Compilation wa	as succe	ssfi	ul. O errors, 12 warning	js		~
	e s							>
	System Processing (123)						
ŧ	Edits pin assignments						100%	00:01:22











Method 2: Prepare a *.csv file from other project, then use [Assignment] \rightarrow [Import Assignment] to import the existing *.csv file to allocate the Pin assignment:



Figure 2-14. Import Assignment



2.4 Download *.sof into FPGA

After the test example correctly compiled, the Quartus will generate a *.sof file which could be directly loaded into FPGA to check whether implemented functions perform as expected. User could use $Tools \rightarrow Programmer$ to start a new download:



Figure 2-15. Programmer

Make sure the USB Blaster's cable are correctly connected to FPGA's JTAG port before using Programmer to download *.sof file. Then click [Auto Detect] to check the hardware setup is okay or not:



Figure 2-16. JTAG Setup



Ardware Setup	USB-Blaster [USB-0]		Mode:	ITAG	•	Progre	55	100% (St	(ccessful)	
Enable real-time IS	5P to allow background programming	when available								
. 10	File	Device	Checksum	Usercode	Program/	Verify	Blank-	Examine	Security	
P [™] Start					Configure	,	Check		Bit	
[™] Stop	<none></none>	10CL006Y	00000000	<none></none>						
💏 Auto Detect										
🗙 Delete										
🎽 Add File										
Change File	<									_
Save File										
Add Device	(intel)									
1 [%] Up										
儿 Down										
	10CL006Y									
	+ 100									
										_
										_
ck 【None〕	Column to choos	Figure 2- se the ⁺ .sof file	7. D to be lo	etect Fl baded in	PGA ito FPG	A.				
ck None	Column to choos	Figure 2- se the *.sof file	Z. D to be lo [Test01_LED.c	etect Fl baded in	PGA ito FPG	A.		_		
CK None	Column to choos Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help	Figure 2: se the *.sof file /Test01_LED - Test01_LED	Z. D to be lo [Test01_LED.c	etect Fl baded in	PGA to FPG	A.		Search al	Ltera.com	
CK [None] Programmer - E:/ ile Edit View Pi	Column to choos Altera/Cyclone_10/SW/Test01_LED, rocessing Tools Window Help [USB-Blaster [USB-0]	Figure 2.4 se the ¹ .sof file	Z. D to be lo (Test01_LED.c	etect Fl baded in hdf)*	PGA to FPG	A. Progre	ess:	Search al	tera.com	
CK None Programmer - E:/ ile Edit View Pi Hardware Setup Enable real-time ISI	Column to choos Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help [USB-Blaster [USB-0] P to allow background programming	Figure 2: se the *.sof file /Test01_LED - Test01_LED - when available	Z D to be lo [Test01_LED.c] Mode:	etect Fl baded in dfj*	PGA to FPG	A.	ess:	Search al	L tera.com	
CK [None) Programmer - E:/ ile Edit View Pi Andreware Setup Enable real-time ISI P ³ b Start	Column to choos Altera/Cyclone_10/SW/Test01_LED, rocessing Tools Window Help USB-Blaster [USB-0] P to allow background programming File	Figure 2:1 se the *.sof file /Test01_LED - Test01_LED - when available Device	7. D to be lo (Test01_LED.c Mode: .	etect Fl paded in dfj* JTAG	PGA to FPG	A. Progra	ess:	Search al 100% (S Examine	tera.com Successful) Security	/
CK [None] Programmer - E:/ le Edit View Pi A Hardware Setup Enable real-time ISI P ¹ Start B ¹ Start Stop	Column to choos Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help USB-Blaster [USB-0] P to allow background programming File	Figure 2- se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006Y	7. D to be lo (Test01_LED.c Mode: .	etect Fl paded in dfj* JTAG Usercode	PGA to FPG	A. Progra	ess: Blank- Check	Search at 100% (S Examine	tera.com Successful) Bit	/
CK NONE	Column to choos Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help [USB-Blaster [USB-0] P to allow background programming File	Figure 2: se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006Y	7. D to be lc (Test01_LED.c Mode: . Checksum 00000000 ramming File	etect Fl paded in df]* JTAG Usercode <none></none>	PGA to FPG	A. Progra	ess: Blank- Check	Search al 100% (S Examine	ctera.com	1
CK None Programmer - E:/ ile Edit View Pi Hardware Setup Enable real-time ISI Plu Start Blu Stap Auto Detect X Delete	Column to choos Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help USB-Blaster [USB-0] P to allow background programming File	Figure 2 se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006Y	Z. D to be lc (Test01_LED.c Mode: Checksum 00000000 ramming File	etect Fl paded in df)* JTAG Usercode <none></none>	PGA to FPG	A. Progra	ess:	Search all	successful) Bit	y
CK [None) Programmer - E:/ le Edit View Pi Ardware Setup Enable real-time ISI Più Start Biù Stop Auto Detect Add File	Column to choos Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help USB-Blaster [USB-0] P to allow background programming File	Figure 2: se the *.sof file /Test01_LED - Test01_LED - when available Device 10CL006Y Select New Prog Look in:	Z. D to be lo [Test01_LED.c] Mode: [Checksum 00000000 ramming File Altera\Cyclone_	etect Fl paded in dfj* JTAG Usercode <none></none>	PGA to FPG	A. Progre Verify	ess:	Search all	tera.com	y
CK [None] Programmer - E:/ ile Edit View Pi Attributer Setup Enable real-time ISI Più Start Più Start	Column to choos Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help USB-Blaster [USB-0] P to allow background programming File	Figure 24 se the *.sof file /Test01_LED - Test01_LED - when available Device 10CL006Y Select New Proc Look in:	Z. D to be lo [Test01_LED.c] Mode: [Checksum 00000000 ramming File Altera\Cyclone_ Name	etect Fl paded in df]" JTAG Usercode <none></none>	PGA to FPG	A. Progre Verify les Type c File	Blank- Check	Search at 100% (S Examine Modified	tera.com	y
CK [None] Programmer - E:/ ie Edit View Pi Hardware Setup Enable real-time ISI P ¹⁰ Start P ¹⁰ Sta	Column to choos	Figure 2: se the *.sof file /Test01_LED - Test01_LED - when available Device 10CL006V Select New Proc Look in:	7. D to be lo (Test01_LED.c Mode: [Checksum 00000000 ramming File Altera\Cyclone_ Name 0utput file Test01_LED.	etect Fl paded in df)" JTAG Vsercode <none></none>	PGA to FPG	A. Progra Verify les rype c File of File	ess: Blank- Check Date I 2018/ 2018/	Search al 100% (S Examine Modified (5/1 10.43-3 (5/1 10.40.0	successful) Security Bit	y
CK NONE Programmer - E:/ ie Edit View Pi Hardware Setup Enable real-time ISI P ¹ ¹⁰ Start P ¹⁰ Start P ¹⁰ Start P ¹⁰ Start P ¹⁰ Start P ¹⁰ Start P ¹⁰ Auto Detect Auto Detect P Add File Change File Save File	Column to choos	Figure 2: se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006V Select New Prog Look in: EX My Comp evelovely	7. D to be lo (Test01_LED.c Mode: _ Checksum 00000000 ramming File Altera\Cyclone_ Name 0utput file Test01_LED	etect Fl paded in df]" JTAG (Usercode <none> 10\SW\Test01. Support</none>	PGA to FPG	A. Progra Verify les Sype c File of File	ess: Blank- Check Date I 2018/	Search al 100% (S Examine Modified (5/1 10:40:0	successful) Security Bit	y
CK [None] Programmer - E:/ ie Edit View Pr Atardware Setup Enable real-time ISI P ¹ ^b Start P ¹ ^b	Column to choos	Figure 2: se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006V Select New Proc Look in: EX My Comp evelovely	Z. D to be lc (Test01_LED.c Mode: . Checksum 00000000 ramming File Altera\Cyclone_ Name Output file Test01_LEC	etect Fl paded in df]" JTAG (Usercode <none> 10\SW\Test01 Si D.sof</none>	PGA to FPG	A. Progra Verify les ype c File of File	ess: Blank- Check Date I 2018/	Search al 100% (S Examine Modified /5/1 10:40:0	successful) Security Bit Ei Ei	y
CK NONE Programmer - E:/ le Edit View Pi Hardware Setup Enable real-time ISI P ¹ b Start P ¹ b Start P ¹ b Start P ¹ b Start P ¹ b Add File P ¹ Change File Add Device P ¹ b Up	Column to choos	Figure 2: se the *.sof file /Test01_LED - Test01_LED - when available Device 10CL006V Select New Proc Look in:	Z. D to be lc [Test01_LED.c Mode: [Checksum 00000000 ramming File Altera\Cyclone_ Name Output file Test01_LEC	etect Fl paded in ddf)" JTAG Usercode <none> _10\SW\Test01_ Si D.sof</none>	PGA to FPG	A. Progra Verify les ype c File of File	ess: Blank- Check Date 1 2018/ 2018/	Search al 100% (S Examine Modified (5/1 10:40:0	successful) Security Bit I I I I I I I I I I I I I I I I I I I	y
CK NONE Programmer - E:/ le Edit View Pr the	Column to choos	Figure 2 se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006Y Select New Proc Look in:	Z. D to be lo (Test01_LED.c Mode: Checksum 00000000 ramming File Altera\Cyclone_ Name Doutput file Test01_LED	etect Fl paded in ddf)" JTAG Usercode <none></none>	PGA to FPG	A. Progra Verify les c File of File	ess: Blank- Check Date I 2018/ 2018/	Search al 100% (S Examine Modified (5/1 10:43:3) (5/1 10:40:0	successful) Security Bit	y
CK NONE Programmer - E:/ ile Edit View Pr the	Column to choose Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help USB-Blaster [USB-0] P to allow background programming File Cnone> C	Figure 2 se the *.sof file //rest01_LED - Test01_LED - when available Device 10CL006Y Select New Proc Look in:	Z. D to be lc [Test01_LED.c Mode: [Checksum 00000000 ramming File Altera\Cyclone_ Name Doutout file Test01_LEC	etect Fl paded in df]" JTAG (Usercode <none></none>	PGA to FPG	A. Progra Verify les c File of File	ess: Blank- Check Date I 2018/ 2018/	Search al 100% (S Examine Modified (5/1 10:43-3) (5/1 10:40-0	successful) Security Bit 2	y
CK NONE Programmer - E:/ ile Edit View Pr that Hardware Setup Enable real-time ISI P ¹ D Start P ¹ D	Column to chooss	Figure 2 se the *.sof file //rest01_LED - Test01_LED - when available Device 10CL006Y Select New Proc Look in:	Z. D to be lc (Test01_LED.c Mode: Checksum 00000000 ramming File Altera\Cyclone Name Output file Test01_LEC	etect Fl paded in df)* JTAG Usercode <none></none>	PGA to FPG	A. Progra Verify les c File of File	ess: Blank- Check Date I 2018/ 2018/	Search al 100% (S Examine Modified (5/1 10:43:3 (5/1 10:40:0	Security Bit 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	y
CK NONE	Column to choose Altera/Cyclone_10/SW/Test01_LED rocessing Tools Window Help USB-Blaster [USB-0] P to allow background programming File <none></none>	Figure 2 se the *.sof file //rest01_LED - Test01_LED when available Device 10CL006Y Select New Prog Look in: EN My Comp 2 evelovely	Z. D to be lc (Test01_LED.c Mode: _ Checksum 00000000 ramming File Altera\Cyclone_ Name output file Test01_LEC	etect Fl paded in df)* JTAG Usercode <none></none>	PGA to FPG	A. Progra Verify les c File of File	ess: Blank- Check Date I 2018/ 2018/	Search al 100% (S Examine Modified (5/1 10:43:3 (5/1 10:40:0	Security Bit 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	y y
ck None	Column to choos	Figure 2 se the *.sof file /Test01_LED - Test01_LED - when available Device 10CL006Y Select New Prog Look in: Ex My Comp evelovely	Z. D to be lo [Test01_LED.c Mode: _ Checksum 00000000 ramming File Altera\Cyclone_ Name 0utput file Test01_LED	etect FI paded in df)* JTAG Usercode <none></none>	PGA to FPG	A. Progra Verify les CEIe of File	ess: Blank- Check Date I 2018/ 2018/	Search all 100% (S Examine Modified (5/1 10:40:0	Security Bit	y
ck None	Column to choos	Figure 2 se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006Y Select New Prog Look in: EX My Comp Revelovely File name: Test01	Z. D to be lc [Test01_LED.c Mode: _ Checksum 00000000 ramming File Altera\Cyclone_ Name file Name file Name file Name file LED.sof	etect FI paded in dfj* JTAG Usercode <none></none>	PGA to FPG	A. Progra Verify les C File of File	ess: Blank- Check Date I 2018/ 2018/	Search all 100% (S Examine Modified (5/1 10:40:0	Security Bit Control Control C	y
ck None	Column to choos	Figure 2 se the *.sof file /Test01_LED - Test01_LED when available Device 10CL006Y Select New Prog Look in: Ex My Comp evelovely File name: Test01 Extra factor	Z. D to be lc [Test01_LED.c Mode: _ Checksum 00000000 ramming File Altera\Cyclone_ Name 0utput file Test01_LEC	etect FI paded in df)* JTAG Usercode <none> 10\SW\Test01. Si D.sof</none>	PGA to FPG	A. Progra Verify les rype c Eile of File	ess: Blank- Check Date I 2018/ 2018/	Search all 100% (S Examine Modified (5/1 10:40:0	Security Bit Coper	Y

Below image shows the FPGA has been detected by the Programmer:

Figure 2-18. Choose *.sof File



<u>E</u> dit <u>V</u> iew	Processing Tools Window Help							Search alte	era.com	9
Hardware Setup	USB-Blaster [USB-0]	available	Mode: J	TAG	•	Prog	ress:	100% (St	iccessful)	
Mu Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Eras
== Stop	output_files/Test01_LED.sof	10CL006YU256	0008EC0E	0008EC0E						
Auto Detect										
× Delete										
Add File										
Change Sile	<									>
Change File										_
Add Device T ^N 는 Up I ^N 는 Down										

Then toggle [Program/Configure] and click the [Start] button to start a new program:

Figure 2-19. Program *.sof

If the *.sof file is correctly programed, the Progress bar will show info like: 100%(Successful). Then users could check whether the LEDs on FPGA board blinking or not.



Figure 2-20. Program Successful



2.5 Program *.jic into SPI Flash

QM_CYCLONE10_10CL006 core board has mounted an external SPI Flash with 8MB capacity. The hardware design chooses Active Serial x 1 method to make the FPGA could boot up from external SPI Flash after power on. In this section, it describes how to program eternal SPI Flash through JTAG port. The SPI Flash is non-volatile device which means the programmed *.jic file will never lose its content after power down.

The SPI Flash programing file *.jic is converted by *.sof file described in previous chapter. So make sure *.sof could be correctly running on FPGA before performing below steps. Step1: choose the Quartus II Prime 15.1file convert tool by click [File] \rightarrow [Convert Programming File]:

				Search anera.com
	New	Ctrl+N	Project_LED - 🗸 🎸 🗇 💿 🕨 🖌 🖉 🖉 🛦 🔌 😭	
0	Open	Ctri+O	Test01_Project_LED.v 🛛	IP Catalog 🔲 🗗 🛪
	Close	Ctri+F4		x =
8	New Project Wizard		1 'timescale ins / ips	
8	Open Project	Ctrl+J	2 // Company:	 Installed P Reviewt Directory
	Save Project		4 // Engineer:	 Project birectory
	Close Project		6 // Create Date: 13:40:55 02/28/2016	M Library
-			7 // Design Name: 8 // Modula Name: Test01 Project LED	> Basic Functions
ы	Save	Ctri+S	9 // Project Name:	> DSP
	Save As		10 // Target Devices: 11 // Tool versions:	> Interface Protocola
æ	Save All	Ctrl+Shift+S	12 // Description:	> Memory Interfaces and Controllers
	File Properties		13 14 // Dependencies:	> Processors and Peripherals
			15 // Revision:	> University Program
	Create / Update	,	17 // Revision 0.01 - File Created	Search for Partner IP
_	Colport		18 // Additional Comments:	
	Convert Programming File	s	20 1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/1/	
IFP)	Dana Catur		22 Impound restor_Project_LED(
(44)	Page Jenup		23 input sys_rst_n,	
2	Print Prevew	044.0		
8	Print	CEN+P	26 L 27 parameter DLY CNT = 32'd50000000:	
	Recent Files	,	28 parameter HALF_DLY_CNT = 32'd25000000;	
	Descel Designed		30 (*mark_debug = "true"*)reg r_led;	
	Recent Projects	,	31 (*mark_debug = "true"*)reg [31:0]count;	
	Exit	At+F4	33 //counter control	
_			34 always@(posedge sys_clk or negedge sys_rst_n) 35 @beoin	
			36 if(!sys_rst_n)	
			37 E begin count <= 32'd0;	
			39 - end 40 else if(court -= DIX_CNT)	
			41 A beain	*
<			> <	> T 2000
×	Type ID Mes	sage		^
69	332102 Des	ign is not f	ully constrained for hold requirements	
-	> 0 Qua	rtus prime T	Imequest Inming Analyzer was successful. V errors, 5 Warnings	
2	U 293000 Qua	cua er me e	un compriación mas auccessian, o enora, o mannings	×
8	<			>
8	System (7) Processi	on (111)		

Figure 2-21. Convert Programming File Tool

Change the settings following below figure: choose EPCQ64, generated file name output_file.jic, etc.

	Conversion setup file	is	2.4				
XX	Output programming Programming file typ Options/Boot info.	file	uration File (.jic) EPCQ64	•	Mode:	Active Serial	•
	Advanced	Create Memory M Create CvP files (Create config dat	difference file: ap File (Generate output Generate output_file.per a RPD (Generate output_	NONE file.map) iph.jic and output_file.c file_auto.rpd)	ore.rbf)		v V
	Input files to convert	ata area	Properties	Start Add	dress		Add He <u>x</u> Data
	SOF Data		Page_0	<auto></auto>			Add Sof Page





🛍 Convert Programming File - E:/Altera/Software/Test01_Project_LED/Test01_Project_LED - Test01_Project_LED 🦷 👘 × File Tools Window Search altera.com 6 Conversion setup files Open Conversion Setup Data.. Save Conversion Setup. Output programming file Programming file type: JTAG Indirect Configuration File (.jic) Options/Boot info... Configuration device: EPCQ64 Ŧ Mode: Active Serial Marked Options × File name: output_files/output_file.jic Advanced... Remote/Local update difference file: Disable EPCS/EPCQ ID check Create Memory Map File (Generate Disable AS mode CONF_DONE error check Create CvP files (Generate output Create config data RPD (Generate of Post-chain bitstream pad bytes: defaul Post-device bitstream pad bytes default Input files to convert Prope Bitslice padding value: 1 🔻 Add Hex Data File/Data area Flash Loader QSPI Flash single IO mode dummy clock: Unchangeable Add Sof Page SOF Data Page_0 QSPI Flash quad IO mode dummy clock: Unchangeable Add Device... OK Cancel Remove Up Down Properties Generate Close Help **Advanced** Options Figure 2-23. Select [Flash Loader] and then click [Add Device] button: Convert Programming File - E:/Altera/Software/Test01_Project_LED/Test01_Project_LED - Test01_Project_LED _ \times <u>File T</u>ools <u>W</u>indow Search altera.com 6 Conversion setup files Open Conversion Setup Data... Save Conversion Setup. Output programming file Programming file type: JTAG Indirect Configuration File (.jic) • Active Serial Options/Boot info... Configuration device: EPCQ64 Mode: • File name: output_files/output_file.jic Advanced... Remote/Local update difference file: NONE Create Memory Map File (Generate output_file.map) Create CvP files (Generate output_file.periph.jic and output_file.core.rbf) Create config data RPD (Generate output_file_auto.rpd) Input files to convert Add Hex Data Start Address File/Data area Properties Flash Loader Add Sof Page Page 0 SOF Data <auto> Add Device Remove Up Properties Generate Close Help

Click the [Advanced...] option, and set these below two options in the red rectangle in Disable status:





Choose the target Flash Loader device: 10CL006Y:

	Select Devices		×
	Device family	Device name	
	Arria 10		∧ New
	Arria GX		New
	Arria II GX	10CL010Y	Import
	Arria II GZ	10CL010Z	Export
	Arria V	10CL016Y	Export.
	Arria V GZ	10CL016Z	Edit
		10CL025Y	Remove
	Cyclone 10 LP	10CL025Z	Kentove
	Cyclone II	10CL040Y	Uncheck All
	Cyclone III	10CL040Z	
	Cyclone III LS	10CL055Y	
	Cyclone IV E	10CL055Z	
	Cyclone IV GX	10CL080Y	
	Cyclone V	10CL080Z	
	HardCopy II	10CL120Y	
	V Usade south		~
			OK Cancel
[Generate]	Convert Programming File - E:/Altera/Cyclone_10 Elle Iools Window Specify the input files to convert and the type of program You can also import input file information from other file future use. Conversion action files	/SW/Test01_LED/Test01_LED - Test01_LED	- C X
	Open Conversion Setup Data	Save Conversion Setup	
	- Output programming file		
	Programming file type:	ile (iic)	
	in ogramming me type. DrAd munect configuration P	ine (c)res	•
	Options/Boot info Configuration device: EPCOG	4 Mode: Active Serial	• • •
	Options/Boot Info Configuration device: EPCQ6-	4 ▼ Mode: Active Serial	•
	Options/Boot Info Configuration device: EPCQ6- File pame: output_files/output_file.jic Advanced Remote/Local update difference	4 Mode: Active Serial	• •
>	Options/Boot Info Configuration device: EPCQ6 File game: output_files/output_filejic Advanced Remote/Local update differenc Ø Create Memory Map File (Ge	4 Mode: Active Serial	• • •
×	Options/Boot Info. Configuration device EPCQ6 File game output_files/output_file.jic Advanced Remote/Local update difference Advanced C create Memory Map File (Ge Create CVP files (Generate o	4 Mode: Active Serial te file: NONE enerate output_file.map) utput_file.periph.jic and output_file.core.rbf)	
× ./	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic: Advanced Remote/Local update difference Advanced Create Memory Map File (Georate o Create CvP files (Generate o Create config data RPD (Ger	4 Mode: Active Serial ef file: NONE enerate output_file.map) utput_file_periph.jic and output_file.core.rbf) herate output_file_auto.rpd)	· · · · · · · · · · · · · · · · · · ·
	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update difference Create Memory Map File (Ge Create CVP files (Generate o Create config data RPD (Generate o Input files to convert	4 Mode: Active Serial te file: NONE enerate output_file.map) utput_file.periph.jic and output_file.core.rbf) nerate output_file_auto.rpd)	· · ·
-	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update difference ØC reate Memory Map File (Gr Create Memory Map File (Gr Create CVP files (Generate o Create config data RPD (Gen Input files to convert File/Data area Prop	4 Mode: Active Serial te file: NONE enerate output_file.map) utput_file.periph.jic and output_file.core.rbf) nerate output_file_auto.rpd) perties Start Address	Add Heg Data
-	Options/Boot info Configuration device: EPCO6 File game: output_files/output_file.jic Advanced Remote/Local update differenc ØC reate Memory Map File (Generate o Create CvP files (Generate o Input files to convert File/Data area Prop Y Flash Loader Prop	4 Mode: Active Serial refile: NONE refile	Add Heg Data
	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update difference ØC reate Memory Map File (Gr Create CVP files (Generate o Input files to convert Create config data RPD (Gen File/Data area Prop Y< Flash Loader	4 Mode: Active Serial te file: NONE enerate output_file.map) utput_file.periph.jic and output_file.core.rbf) nerate output_file_auto.rpd) perties Start Address sauto>	Add Heg Data Add Epic
	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update difference Create Memory Map File (Generate o Create CVP files (Generate o Input files to convert File/Data area Prop Y Flash Loader 10CL006Y Y SOF Data Page_0 Text01_LED.sof 10CL006YU25	4 Mode: Active Serial e file: NONE enerate output_file.map) uutput_file.periph.jic and output_file.core.rbf) nerate output_file_auto.rpd) perties Start Address <auto> 56</auto>	Add Heg Data Add Sof Page Add Ele. Remove
	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update differenc ØC reate Nemory Map File (Generate o Create config data RPD (Gen Input files to convert File/Data area Prop V Flash Loader ProgOV V SOF Data Page_0 10CL006YU25	4 Mode: Active Serial ce file: NONE enerate output_file.map) uutput_file.periph.jic and output_file.core.rbf) nerate output_file_auto.rpd) perties Start Address <auto> 56</auto>	Add Heg Data Add Ele Remove
	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update difference Create CVP files (Generate o Create Config data RPD (Generate o Input files to convert File/Data area Prop Y Flash Loader Prop(CLOBGY Y SOF Data Page_0 10CLODEYU25	4 Mode: Active Senal cefile: NONE cefile: NONE cenerate output_file.map) cutput_file.periph.jic and output_file.core.rbf) cenerate output_file_auto.rpd) cenerate output_file_auto.rpd cenerate output_file_auto.rpd cenerate output_file.core.rbf? cene	Add Heg Data Add Jof Page Add Ele Remove Up
	Options/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update difference Øcreate Memory Map File (Generate o Create CVP files (Generate o Create config data RPD (Generate o Create config data RPD (Generate o Input files to convert File/Data area Prop Y Flash Loader 10CL006Y Y< SOF Data	4 ▼ Mode: Active Serial te file: NONE enerate output_file.map) utput_file.periph.jic and output_file.core.rbf) nerate output_file_auto.rpd) perties Start Address <auto> 56</auto>	Add Heg Data Add Sof Page Add Eile Remove Up Down Properties
	Qptions/Boot info Configuration device: EPC06 File game: output_files/output_file.jic Advanced Remote/Local update difference Øcreate Memory Map File (Generate o Create CvP files (Generate o Create config data RPD (Generate o Create config data RPD (Generate o Input files to convert File/Data area Prop Y Flash Loader 10CL006V Y< SOE Data	4 ▼ Mode: Active Serial te file: NONE enerate output_file.map) utput_file_periph.jic and output_file.core.rbf) nerate output_file_auto.rpd) perties Start Address <auto> 56</auto>	Add Heg Data Add Sof Page Add Ele Remove Up Down Properties





After the output_file.jic correctly generated, run the $[Tools] \rightarrow [Programmer]$. And then click [Add File...] to choose the output_file.jic.

etup USB-Blaster [USB-0]		Mo	de: JTAG		•	Progres	is:		
File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase
<none></none>	10CL006Y	0000000	<none></none>						
ct	Nelect New	Programming	File						×
	Look in:	F:\Altera\Cvc	lone 10\SW\T	Test01 FD\o	utput file	•	00	0	
	My Comp	Name	^	Size	Typ		Date Modifi	ed.	
	evelovely	output	t_file.jic	8.	.0 MB jic F	ile	2018/8/25	18:24:04	
				35	50 KB sof	File	2018/5/1 1	0:40:07	
↓ TDO	File name:								Open
	The stress D			• : • : • -	lun + 11n)			-	Canaal

Figure 2-27. Choose *jic File

Toggle [Program/Configure] and then click [Star] button to program the external SPI Flash. Program status will be shown in the [Progress] bar. After the *.jic correctly programmed, user may repower on the board to check whether the FPGA could boot from external SPI Flash.







3. SignalTap II Logic Analyzer

The SignalTap II Embedded Logic Analyzer is a system-level debugging tool that captures and displays signals in circuits designed for implementation in Intel's FPGAs. The user is expected to have access to a computer that has Quartus II 17.0 software installed. The detailed example in this chapter was obtained using Quartus II version 17.0, but newer versions of the software can also be used.

After successfully compiling the Test04_SDRAM project and setting pin assignments, select SignalTap II Logic Analyzer from the tools dropdown menu (as shown below). Ensure the JTAG programmer (USB Byte Blaster) is connected between the board and the computer.

			- /	
Quartus Prime Standard Edition - E:/Altera/Cyclone	10/SW/Test04_SDRAM/Test04_SDRAM - Test04_SI	DRAM	- 0	×
File Edit View Project Assignments Processing	Tools Window Help		Search altera.com]•/
Project Navigator A Hearchy Q Q Ø Ø X EntityLinstance	Run Simulation Tool Ca. Launch Simulation Library Compiler Launch Design Space Explorer II TimeQuest Timing Analyzer		IP Catalog	5 ×
2 MM Test04_SDRAM 10 4 7 8 9 10	Advisors Adviso	///// R, _N,	Project Directory No Selection Available Library Basic Functions DSP Interface Protocols	
11 16 16 19 19 20 20 21 22 23 24 24 24 25 24 25 27 27 27 27 27 27 27 27 27 27 27 27 27		, ,, ,, ,, ,, //////	Memory Interfaces and Controllers Processors and Peripherals University Program Search for Partner IP	
 20 31 32 34 35 35 37 38 39 39 31 34 35 35 36 37 38 39 31 34 35 35 36 37 38 39 39 30 	P Catalog Nios II Software Build Tools for Eclipse Osys Tcl Scripts Customize		+ Add	_
x Type ID Message Ø □ ≡ § § ≤	Options License Setup install Devices			>
System Processing			0% 00:00:0	

Figure 3-1. Open SignalTap II Logic Analyzer

Below image shows the UI of the SignalTap II:

	Image: SignalTap II Logic Analyzer Elle Edit View Project P Image: Im	r - E:/Altera/Cyclon rocessing Iools 20 Part Content Add nodes Status Not running	e_10/SW/Te Window b to the curren Enabled	st04_SDRAM/Ter jelp t instance LEs: 0 0 cells	st04_SDRAM - Te Memory: 0 0 bits	st04_SDRAM - [s Small: 0/0 NA	ttp1.stp]* Medium: 1/30 NA	X Large: 0/0 NA	Search atter JTAG Chain Configuration: JTAG ready Hardware: USB-Blaster [USB-0] Device: @1:10CL006(Y[2]/10CL010(Y]; * >> SOF Manager:	Com
	auto_signalizap_0 Node Type Allas Double-click to add nodes Type Data Setup	łame	Lock mod Data Enal O	e: Allow all c Irigger Enat	hanges De Trigger Cond 1⊡ Basic AN	v itions D v		Signal Con Clock Data Sample c Segm	hguration: lepth: 128 RAM type: Auto ented: 2 64 sample segments	×
Y	Hierarchy Display:	×	Data Log: 📔	الله naltap_0					0%	×





*** SignalTap II Logic Analyzer - E:/Altera/Cyclo Elle Edit View Project Processing Tools Image: Image:<	Ine_10/SW/Test04_SDRAM/Test Window Help s to the current instance Enabled LEs: 0 O cells	t04_SDRAM - Test04_SDRAM Memory: 0 Small: 0/t 0 bits NA	1 - [stp2.stp]*	Se JTAG Chain Configuration: JTAG rea Hardware: USB-Blaster [USB-0] Device: @1:10CL006(Y[Z)/10CLU >> SOF Manager:]	arch altera.com Hdy Se up Download	3 ation, etup, 1 *.sof
auto_signaltap_0 Node Type Alias ame Double-click to add nodes	Lock mode: Allow all c Data Enable Trigger Enable 0 0	hanges		Signal Configuration: Clock: Data Sample depth: 128 PAM type: Auto		
Monitor Signals				Segmented: 2 64 sample segments Nodes Allocated: Auto O Manual:	Signal Sampling	Clock
		Ca	apture Data	Pipeline Factor: 0 Buffer Size Jous Input port: Nodes Allocated: O Auto Manual: Record data discontinuities Disable storage qualifier Trigger Nodes Allocated: Auto Manual: Trigger flow controt: Sequential Trigger position: Trigger conditions: 1 Trigger in Trig		
Hierarchy Display: ×	Data Log: 🛐				×	
auto_signaltap_0	auto_signaltap_0				0% 00.00.00	

Below image shows the settings of the Test04_SDRAM example project:

Figure 3-3. Signal Tap II Logic Analyzer Main Window

Double click the [Node] column shown in the above image. Below window will pop up and user clicks the [List] button to add the signals need to be monitored:

% Node Finder Named: Options Filter: SignalTap It: post-fitting			List R
Look In: DEC_CV_SDRAM_RTL_Test Matching Nodes: DEC_CV_SDRAM_RTL_Test > DRAM_DO DEAM_DO[1]=nput DEAM_DO[1]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput DEAM_DO[2]=nput	Assignments Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned	Name	Include subentities M Hierarchy view Assignments Assignments

Figure 3-4. Set Capturing Signals



All the signals added in the above step will be displayed in the [setup] page. Please also select the signal sampling clock [DRAM_CLK] :

	Status	Enabled I	En: 2101	Inmony 14E409	Small: NA	Madium: NA	Large: NA	^	The chair contiguration. The ready
auto -	signaltan 0 Not running		101 cells 1	45408 hits	NA NA	NA NA	NA NA		Hardware: USB-Blaster [USB-0] Setu
									Device: @1: SCE(BA2 FA2) (0x02B150DD) Scan (0 >> SOF Manager: Image: Image:
igger: 20	17/11/30 21:27:03 #1	Lock mode:	Allow all change	s					Signal Configuration:
	Node	Data Enable	Trigger Enable	Trigger Condit	ions				Clearly DRAM CLK
pe Alia	s Name	142	142	1 Basic AND	-				CIOUX. DIVAM_CER
•				XXXXXh					Data
	RW_Test:u2 readdata[150]			XXXXXh					Sample depth: 1 K 🔻 RAM type: Auto 💌
	E-RW_Test:u2 write_count[40]			XXh					Segmented: 2 512 sample segments
	RW_Test:u2 clk_cnt[310]			XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX					
	RW_Test:u2 drv_status_fail								Nodes Allocated: Auto Manual: 142
	RW_Test:u2 drv_status_pass								Storage qualifier:
	RW_Test:u2 drv_status_test_complete								Type: 🔛 Continuous 💌
•				Xh					Input part: auto sto external storage qualifier
	RW_Test:u2 iBUTTON		\checkmark						
•	RW_Test:u2 iCLK								Nodes Allocated: Auto Manual: 142
	RW_Test:u2 iRST_n								Record data discontinuities
	RW_Test:u2 read								Disable storage qualifier
	RW_Test:u2 write								
	RW_Test:u2 trigger								Trigger
	E-RW_Test:u2 address[240]			XXXXXXXXXX					
	E RW_Test:u2 cal_data[310]			00000000					Nodes Allocated: Auto Manual: 142
•	H-RW_Test:u2 pre_button[10]			Xh					Trigger flow control: Sequential
Data	B Setup	Data Log.	ap_0		/				

Figure 3-5. Sampling Signals and Clocks

User needs to click the 【Compile】 button shown in the below image to recompile the whole project. Then user may download the newly compiled soft into FPGA.

🟸 SignalTap II Logic Analyzer	- E:/Altera/Cyclon	e_10/SW/Te	st04_SDRAM/Tes	t04_SDRAM - Test	04_SDRAM - [stp	o1.stp]			-	
<u>File Edit View Project Pro</u>	ocessing <u>T</u> ools	<u>W</u> indow <u>I</u>	Help						Search altera.c	om
🗃 📒 つで 🕸 💧 🕨	8 0									
Instance Manager: 🍡 💫 🔳	Invalid JTA	5 configurati	on					×	JTAG Chain Configuration: JTAG ready	
Instance	Status	Enabled	LEs: 1355	Memory: 78848	Small: 0/0	Medium: 11/30	Large: 0/0		Hardware: USB-Blaster [USB-0]	Setup
🕄 auto_signaltap_0	Not running	\checkmark	1355 cells	78848 bits	0 blocks	9 blocks	0 blocks			
									Device: @1: 10CL006(Y Z)/10CL010(Y : •	Scan Chair
									>> SOF Manager: 👗 🕕 files/Test04_SDR	AM.sof

Figure 3-6. Compile the SignalTap II Project

User could click the button [AutoRun Analysis] or button [Run Analysis] to start the waveform capture:

X	% SignalTap II Logic Analyzer - E:/Altera/Cyclone_10/SW/Test04_SDRAM/Test04_SDRAM - Test04_SDRAM - [stp1.stp] Elle Edit View Processing Tools Window Help Image: Page State											com	×]•
	Instance Manager. 🍡 👂 📕	Invalid JTAG configuration								JTAG Chain Configuration:	JTAG ready		×
	Instance	Status	Enabled	LEs: 1355	Memory: 78848	Small: 0/0	Medium: 11/30	Large: 0/0		Hardware: USB-Blaster [USB	8-0] 🔻 Setu		
-	🕄 auto_signaltap_0	Not running		1355 cells	78848 bits	0 blocks	9 blocks	0 blocks		Device: Q1: 10CL006(VI	- 7)/10CL010[V]: ▼	Scop Ch	ain
										>> SOF Manager:	liles/Test04_SE	DRAM.sof	

Figure 3-7. Start Capture



Below two images show the SDRAM data write and SDRAM data read:

log: Trig @ 2 Type Alias	Offloading acq.	1355 cells 78	848 bits 0 blocks								
log: Trig @ 2 Type Alias				9 blocks 0 blocks						Device: @1: 10CL00	6(Y Z)/10CL010(Y
log: Trig @ 2 Type Alias										>> SOF Manager.	iles/Test04
Type Alias	2018/08/26 10:07:52 (0:0:0.1 elapsed) a1						ar				
	Name	-366 -365	-364 -363	-3¢2 -3¢1	-360 -3	159 -358 ECCEN	-3\$7 -3\$6	-355	-354	-353 -352	-351
	RW_Testu2[readdata[15.0] RW_Testu2[readdata[15.0]	(oth) ort	Y ost V	ozh X och V	ont	0000h	th Y and Y	oab Y	Y ar	Y and V	075
	RW_Test-u2[pre_button[1.0] RW_Test-u2[pre_button[1.0]	<u></u>	X	viii A usn A	000	2h	<u>v</u> en X	van A 04h	A Ush	<u>∧ uon ∧</u>	ν
	RW_restu2[c_state[3.0] RW_Testu2[address[23.0]		10 64	λλλλλλλλ	<u>∡n ∧ 3h</u>	ĵ		1h C4152	sh		
	RW_Testu2 drv_status_fail RW_Testu2 drv_status_pass										
	RW_Testu2 drv_status_test_complete RW_Testu2 write										
	RW_Testu2 trigger RW_Testu2 iBUTTON										
*	RW_Testu2 ICLK RW_Testu2 IRST_n										
	RW_Testu2 read RW_Testu2 same										
a Data	Setur.	د									
erarchy Dis	splay: x	Data Log: 🛐									
✓ • Te	est04_SDRAM	auto_signaltap_0									
⊻ ⇒	ww_Testu2										
auto_sign	naltap_0										
SignalTap I e Edit V	II Logic Analyzer - E:/Altera/Cyclone View Project Processing Tools	10/SW/Test04_SDRAM/Test04_SI Window Help	DRAM - Test04_SDRAM - [s	stp1.stp]*							Search a
0 1	0 (** 🔲 🕨 😫 🚱										
tance Mana	ager: 🔃 😥 🔳 🔛 Acquisition	In progress	mon: 79949	Madaun 1100					×	JTAG Chain Configurati	on: JTAG ready
ance 🛃 auto_si	status ignaltap_0 Offloading acq	2 1355 cells 78	848 bits 0 blocks	9 blocks 0 blocks	,					Hardware: USB-Blaster	[USB-0]
										Device: @1: 10CL0	
										>> SOF Manager.	les/Test0
og: Trig @ 2	2018/08/26 10:08:31 (0:0:0.1 elapsed) #3	1				click to insert time bi	ar				
ype Alias	Name RW_Test:u2 writedata[15.0]	-366 -365	-364 -363	-3¢2 -3¢1	-360 -3	159 -358 5555h	-3\$7 -3\$6	-355	-354	-353 -353	-351
a	RW_Test:u2 readdata[15.0] RW_Test:u2 write_count[4.0]		X ooh	X oth X	ozh X ozh	5555h X 04h X 05	ih X och X	ozh X osh		ooh X	oth X
	RW_Test:u2[pre_button[10] RW_Test:u2[c_state[3_0]	Ab	X zh X	ah X sh Y		3h	h		X 7h	X ah Y	sh Y
•	RW_Testu2 address[23.0]	4CB19Eh	X	An		e 4CB19Fh			~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	A	4CB1A0h
•	RW_Testu2 drv_status_fail RW_Testu2 drv_status_pass										
	RW_Testu2 drv_status_test_complete RW_Testu2 write										
	RW_Testu2 trigger RW_Testu2 iBUTTON										
	RW_Testu2 ICLK										
-	RW_l'estu2 IRST_n RW_Testu2 read										
2	RW_Testu2 same										
•											
•											
•											
•		<									
Data	🚎 Setup	¢									
Data	■ Setup splay: × □	CData Log:									
Data ierarchy Dis 2 Te 2 2	Setup splay: X stb4_SDRAM RW_Testu2	< Data Log: ☑ auto_signaltap_0									
Data Ierarchy Dis Ierarchy Dis Ierarchy Dis Ierarchy Dis Ierarchy Dis Ierarchy Dis Ierarchy Dis Ierarchy Dis	Setup splay, x est04_SDRAM rRW_Testu2	Cata Log: 💽									
Data erarchy Dis 2 Te	R Setup splay: X ext04_SDRAM RW_Testu2	c Data Log: 🔁									
■ Data erarchy Dis I ■ Te I ■ Te	E Setup poly: x ext04 SDBAM RW_Testu2	¢ Data Log: ⊡] 2010_signaltap_0									
	RW_Testu2 BST_IN RW_Testu2 RST_IN RW_Testu2 Red RW_Testu2 same									r	

Figure 3-9. Waveform for Reading Data from SDRAM



Reference 4.

- 10cl006-sdram-v01.pdf
 c10lp-51002.pdf
 c10lp-51003.pdf

- [4] pcg-01021.pdf
 [5] cyclone-10-lp-product-table.pdf
 [6] an800.pdf
- [7] aib-01029.pdf



5. Revision

Doc. Rev.	Date	Comments	
0.1	30/12/2018	Initial Version.	
1.0	11/01/2019	Formal Release.	
		HAN AND AND AND AND AND AND AND AND AND A	

