QM_MAX10_10M02SCU169 DB

USER MANUAL (QUARTUS 15,1)



The QMTech® QM_MAX10_10M02SCU169 Development Board uses Intel® 10M02SCU169 device to demonstrate Intel® MAX® 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single chip small form factor programmable logic device. Building upon the single chip heritage of previous MAX device families, densities range from 2K – 50K LEs, using either single or dual-core voltage supplies. The MAX 10 FPGA family encompasses both advanced small wafer scale packaging (3 mm x 3 mm) and high I/O pin count packages offerings.

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1. Quartus Prime 15.1 Installation

The revolutionary Intel® Quartus® Prime Design Software includes everything you need to design for Intel® FPGAs, SoCs, and CPLDs from design entry and synthesis to optimization, verification, and simulation. Dramatically increased capabilities on devices with multi-million logic elements are providing designers with the ideal platform to meet next-generation design opportunities.

The Intel® Quartus® Prime Software design flow comprises of the following high-level steps:



The Quartus Prime software version 15.1 supports the following device families: Stratix IV, Stratix V, Arria II, Arria V, Arria V GZ, Arria 10, Cyclone IV, Cyclone V, MAX II, MAX V, and MAX 10 FPGA. Below image shows the startup UI of Quartus II Prime 15.1:

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Figure 1-1. Quartus II Prime 15.1

After the Quartus II Prime 15.1 is correctly installed, users still need to install the device package from Intel official website. Below lists the download center address: https://www.intel.com/content/www/us/en/programmable/downloads/download-center.html

In the Intel Download Center website, select the tab of 'Select by Device' and then all the available device packages will be listed as below image. The device used in this user manual is MAX10 series CPLD and the detailed chip part number is 10M02SCU169C8G, so please download the device package for Quartus II 15.1: max10-15.1.0.185.qdz.



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		Quartus Edition	Version Listing
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			 ▲ 16.1 ▲ 16.0 ▲ 15.1
		Subscription Edition	 ↓ 15.0 ↓ 14.1 ↓ 14.0
		Web Edition	 ↓ 15.0 ↓ 14.1 ↓ 14.0

Figure 1-2. Download Device Package

Open Quartus II 15.1, Click Tools \rightarrow Install Device and then select the downloaded device package:

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Choose the device package needs to be installed and click Next:

Figure 1-6. Install the Device Package

User could also install the device package by using Quartus II Prime 15.1 Device Installer directly:







2. CPLD Project Compile and Download

2.1 Create New Project

Click [File] \rightarrow [New Project Wizard...] to create a new project:



Figure 2-2. New Quartus Prime Project



In below [New Project Wizard] page, choose Next:

🕥 New Project Wizard	×	
Introduction		
The New Project Wizard helps you create a new project and preliminary project settings, including the following:		
Project name and directory Name of the top-level design entity		
Project files and libraries Target device family and device		
EDA tool settings		
You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.		
		// //
		•
Don't show me this introduction again		
	_	
< <u>Back</u> <u>Next</u> > <u>Finish</u> Cancel <u>Help</u>		

Figure 2-3. New Project Wizard

Set the target working folder below 【What is the working directory for this project?】. Set the new project name below 【What is the name of this project?】 And finally set the example project name: Test01_Project_LED shown as below.

		· · · · · · · · · · · · · · · · · · ·				
What is the working direc	tory for this project?					
E:/test						
What is the name of this g	roject?					
Test01_Project_LED						
What is the name of the to	p-level design entity for	this project? This name	e is case sensitive and	d must exactly match	the entity name in the d	tesign file.
Test01_Project_LED						
Use Existing Project Setti	ngs					

Figure 2-4. Set Working Directory and Project Name



Select [Empty Project] and then click Next:

🍞 New Project Wizard		×
Project Type		
Select the type of project to create.		
Empty project		
Create new project by specifying project files and libraries, target	device family and device, and EDA tool settings	
O Project template		
Create a project from an existing design template. You can choose templates from the <u>Design Store</u> .	e from design templates installed with the Quartus Prime software, or d	ownload design
	< Back Next > Finish Cancel	Help
		.::
	X /	
Figure 2-5. C	reate Empty Project	
Figure 2-5. C ady has some source code, please ado	reate Empty Project	step:
Figure 2-5. C ady has some source code, please add	reate Empty Project	step:
Figure 2-5. C ady has some source code, please add	reate Empty Project	step: ×
Figure 2-5. C ady has some source code, please add New Project Wizard Add Files	reate Empty Project	step: ×
Figure 2-5. C ady has some source code, please add New Project Wizard Add Files Select the design files you want to include in the project. Click Add All t	reate Empty Project d all these necessary files in this s	step: ×
Figure 2-5. C ady has some source code, please add New Project Wizard Add Files Select the design files you want to include in the project. Click Add All th Note: you can always add design files to the project later.	reate Empty Project d all these necessary files in this s	step: ×
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Figure 2-5. C addy has some source code, please add New Project Wizard Add Files Select the design files you want to include in the project. Click Add All the New You can always add design files to the project later. Elle name: File Name Type Library Design Entry/Synthesis Tool HDL variables HDL va	reate Empty Project all these necessary files in this a add all design files in the project directory to the project	Step: X Add Add AJ Remove Up Down Properties
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Figure 2-5. c Add has some source code, please add New Project Wizard Add Files Select the design files you want to include in the project. Click Add All the to: you can always add design files to the project later. Ele name: File Name Type Library Design Entry/Synthesis Tool HDL view Speciry the path names of any non-default librares.	reate Empty Project 1 all these necessary files in this s a add all design files in the project directory to the project.	Step: Add Add AJ Bemove Do Properties

Figure 2-6. Add Source Code



Choose the CPLD Chip number: 10M02SCU169C8G

Family: M4					Show in 'Available	devices' list			
	AX 10 (DA/DF/DC/SA/	SF/SC)		•	Package:	UFBGA		-	
Devices:	MAX 10 SC			•	Pin count:	169		-	
					Core Speed grade	8		-	
Target devic	ice				u sere op <u>o</u> od grade.	-			
O Auto de	evice selected by the I	Fitter			Name filter:				
vailable dev	lices:								
vailable dev.	rices:	age I Fe	Total I/Os	CPI	Os Memory B	ite Embedded mu	utinlier 9 hit eleme	inte	7
vailable dev Name 10M02SCU16	rices: Core Volt 69C8G 3.3V	2304	Total I/Os 130	CP 130	0e Memory F 110592	ite Embedded mu	ltiplier 0 hit eleme	inte 1	
vailable dev Name IOM02SCU16 IOM04SCU16	vices: 69C8G 3.3V 69C8G 3.3V	2304 4032	Total I/Oe 130	130	Os Memory F 110592 193530	ite Embedded mi 32 40	ltiplier 9 bit eleme	nte 1	
Vallable dev Name IOM02SCU16 IOM04SCU16 IOM08SCU16	vices: 69C8G 3.3V 69C8G 3.3V 69C8G 3.3V 69C8G 3.3V	2304 2304 4032 8064	Total I/Os 130 130 130	130 130 130	Os Memory F 110592 193536 387072	ite Embedded mi 32 40 48	Itinlier 9 hit eleme	nte 1 1 1	

Figure 2-7. Select Device

Summary page will be shown and click [Finish] if there's nothing needs to be changed:

	A
🕽 New Project Wizard	×
Summary	
When you click Finish, the project will be created with the following settings:	
Project directory:	C:/Users/evelovely/Desktop
Project name:	test
Top-level design entity:	test
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	MAX 10 (DA/DF/DC/SA/SF/SC)
Device:	10M02SCU169C8G
EDA tools:	
Design entry/synthesis:	<none> (<none>)</none></none>
Simulation:	<none> (<none>)</none></none>
Timing analysis:	0
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C
	< Back Navts Finish Cancel Help
L	Cancel <u>Heip</u>







After the Empty Project created, below image will be shown:

Table 2-1. Empty Project

Users may add example source file Test01_Project_LED.v into this Empty Project shown as below:









After the newly added source file loaded into project, user can view the source code shown as below:

Figure 2-9. View of Source Code

2.2 Compile the Project

Users could use the button [Start Compilation – Ctrl + L] shown in below image to compile the project:



Figure 2-10. Compilation



There will be compilation report after the compile finished, in which shows the info like logical element resource usage, how many PLLs are used, etc. Below image shows an example Compilation Report:

•			•	• •	•	
🔇 Quartus Prime Standard Edition - E:/Alter	a/MAX10/Software/Test01_LED/Test0	01_LED - Test01_LED			- 0	×
<u>File Edit View Project Assignments Proce</u>	essing <u>T</u> ools <u>W</u> indow <u>H</u> elp 🤜				Search altera.com	6
🗋 🔚 🚽 👉 🛅 💼 🤊 🤆 🛛 Test01_Li	ED 🔹 🖌 🎸 🤇	🛠 🚸 💷 🕨 🗶 💺 😂 🚳	🕹 🔖 🚂			
Project Navigator 🝌 Hierarchy 🔹 💷 🗗 🗙	Test01_LED.v	🗵 🐥	Compilation Report - Test01_LED			
Entity:Instance	Table of Contents 📮 🗗	Flow Summary				
MAX 10: 10M02SCU169C8G 時間 Test01_LED 市	Flow Summary Flow Settings Flow Vestings Flow Lop-Default Global Settings Flow Lopsed Time Flow Log Assembler Fiter PowerPlay Power Analyzer Flow Messages Flow Suppressed Messages	[Flow:Status] Cluartus Prime Version Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total combinational functions Dedicated logic registers Total combinational functions Dedicated logic registers Total virtual pins Total virtual pins Total virtual pins Total virtual pins	Successful- Mon Apr 23 22:27:50 2018 15:10 Buiki 165 10/21/2015 SJ Standard Edition Test01_LED MAX 10 10M02SCU169CBG Final 64 / 2,304 (1 %) 64 / 2,304 (1 %) 34 4 / 130 (3 %) 0 0 / 110.592 (0 %)			
< >>	TimeQuest Timing Analyzer	Embedded Multiplier 9-bit elements Total PLLs UFM blocks	0 / 32 (0 %) 0 / 1 (0 %) 0 / 1 (0 %)			
× Type ID Message Ø 332148 timing requirement > 0 332146 worst-case setup : > 0 332146 worst-case hold s' 0 332146 worst-case setup : 0 332140 No Recovery paths 0 332140 worst-case minimu 0 332140 worst-case minimu 0 332102 Design is not ful 0 332102 Design is not ful 0 293000 Quartus Prime Tim 0 293000 Quartus Prime Ful	ts not met slack is -1.000 lack is 0.252 to report to report pulse width slack is -3.0 ly constrained for setup re ly constrained for hold rec equest Timing Analyzer was l compilation was successfu	2000 equirements uirements successful. O errors, 4 Jl. O errors, 12 warnin	4 warnings gs			~
System Processing (123)					100%	00:01:22

2.3 PIN Assignment

There are several ways to assign the Pins for the example project. Method 1: Choose [Assignment] \rightarrow [Pin Planner]:

Compilation Report

Figure 2-11.

🕥 Quartus Prime Standard S	Edition Ev/Altors/MAX10/Software/Test01-LED	D/Test0	1_LED - Test01_LED		- 0	×
File Edit View Project Ass	ssignments Processing Tools Window Help	•			Search altera.com	
🗋 🗖 🖬 🗲 🗇 💼 🔽	Device	& 👌	s 🚸 💷 🕨 🖌 🤘 🚫	A 🔌 🙀		
Project Navigator 🔥 Hierarchy	Settings Ctrl+Shift+E	ED.v		Compilation Report - Test01_LED		
Entit	Assignment Editor Ctrl+Shift+A	д 8	Flow Summary			
A MAX 10: 10M02SCU169C8	Pin Planner Ctri+Shift+N		Flow Status	Successful - Mon Apr 23 22:27:50 2018		^
Test01_LED	Remove Assignments		Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Standard Edition		
1	Back-Annotate Assignments	lettings	Top-level Entity Name	Test01 LED		
	Import Assignments		Family	MAX 10		
	Export Assignments		Device	10M02SCU169C8G		
	Assignment Groups		Timing Models	Final		
			Total logic elements	64/2,304(3%)		
	LogicLock Regions Window Alt+L		Dedicated logic registers	64/2,304(3%) 34/2 304(1%)		
- C	Design Partitions Window Alt+D		Total registers	34		
	Flow Maccanae	.ci	Total pins	4 / 130 (3 %)		
	Flow Suppressed Message	oes	Total virtual pins	0		
	> TimeQuest Timing Analyzer	er	Total memory bits	0/110,592(0%)		
			Total PLLs	0/12(0%)		
(UFM blocks	0/1(0%)		~
						*
Type ID Messag	ge requirements not met					^
4 332146 Worst-	-case setup slack is -1.000					
≡ 332146 Worst-0	-case hold slack is 0.252					
332140 No Reco	covery paths to report					
1 332140 No Remo	noval paths to report					
332146 Worst-0	-case minimum pulse width slack is	-3.00	ouirements			
a 332102 Design	is not fully constrained for hold	ld requ	uirements			
> 0 Quartus	us Prime TimeQuest Timing Analyzer	was s	successful. 0 errors, 4	l warnings		
g 0 293000 Quartus	us Prime Full Compilation was succe	essfu	1. 0 errors, 12 warning	gs		~
sage						>
System Processing (123))					
Edits pin assignments					100% 0	0:01:22





🕥 Quartus Prime Standard Edition - E:/Altera	a/MA	X10/Software/Test01_I	LED/Test01_LED - T	est01_LED					- (n x
<u>File Edit View Project Assignments Processing Tools Window H</u> elp 🤜							Search altera.cor	m 🜖		
🗋 🔚 🚽 👉 🖺 💼 🔈 ୯ 🛛 Test01_LLE	D	•	/ 🗳 🗳 🔅 💷) K 4) 🔕 🕹 🔌 🚂					
Project Navigator 🝌 Hierarchy 🔹 = 📮 🗗 🗙	4	Test01_LED.v		Compilation Rep	oort - Test01_LED 🛛 🛛	of Pin	Planner	×		
Entity:Instance		Report		1 8 ×			Top View - Wire	Bond		
A MAX 10: 10M02SCU169C8G		Report not available				MA	X 10 - 10M02SC	U169C8G		
Test01_LED							steen, r			
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		Early Pin	Planning							
	*	Run VO A	ssignment Analysis			~ 📿				
		Export Pi	n Assignments				stan, t			
	P	Pin Finder	. Ko Eatt V	•					Filter Dien: el	
	4	B Node Name	Direction		tion //O Bank	V/PEE Oroup	Eitter Location	I/O Standard	Perserved	- Current S
	2	out led 1	Output	PIN F9	6	B6 N0	PIN F9	3 3-V I VTTI	Reserved	8mA (defa
	*	out led_2	Output	PIN_F10	6	B6_N0	PIN_F10	3.3-V LVTTL		8mA (defa
		sys_clk	Input	PIN_H6	2	B2_N0	PIN_H6	3.3-V LVTTL		8mA (defa
	io 4	<pre>sys_rst_n <<new node="">></new></pre>	Input	PIN_G13	5	B5_N0	PIN_G13	3.3-V LVIIL		8mA (deta
	*	ş								_
< >>	¥	AIN <								>
* Type ID Message										^
🗗 🔥 332148 Timing requirement	ts n	ot met								
A 332146 Worst-case setup	slac	k is -1.000								
332146 Worst-case hold s	Tack	15 0.252								>
System Processing (123)										
									10001	00.04.00

Below image shows PIN settings for this test example:

Figure 2-13. PIN Assignment

Method 2: Prepare a *.csv file from other project, then use [Assignment] \rightarrow [Import Assignment] to import the existing *.csv file to allocate the Pin assignment:



Figure 2-14. Import Assignment



2.4 Download *.sof into FPGA

After the test example correctly compiled, the Quartus will generate a *.sof file which could be directly loaded into FPGA to check whether implemented functions perform as expected. User could use $Tools \rightarrow Programmer to start a new download:$



Figure 2-15. Programmer

Make sure the USB Blaster's cable are correctly connected to CPLD's JTAG port before using Programmer to download *.sof file. Then click [Auto Detect] to check the hardware setup is okay or not:



Figure 2-16. JTAG Setup



							_		
Hardware Setup	USB-Blaster [USB-0]		Calact David	M	ode: ITAG	~	Progress:		
Enable real-time ISP	to allow background progr	amming when av	 Select Device 			^			
billio Chart	File	Devic	Found devices with s	shared JTAG ID for de	vice 1. Please select	t your device.	xamine Sec	urity Erase	ISP
™ Start			10M02SC				E	Bit	CLAMP
™™ Stop			O 10M02SCES						
Auto Detect									
🗙 Delete									
Add File									
Change File									
Save File									
Add Device									
† ^ሢ b Up									
J‰ Down						ок			
	L								
s click 【N		to choo	Figure ose the *.sof /Test01_LED - Test0	2-17. file to be	oaded into	CPLD.			
rs click 【N ogrammer - E:/A dit View Proce	one Column	e/Test01_LED/	Figure ose the *.sof /Test01_LED - Test0	2-17. file to be	oaded into	CPLD.		Search	- D
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Below image shows the CPLD has been detected by the Programmer:

Figure 2-18. Choose *.sof File



Programmer - E	E:/Altera/MAX10/Software	- /Test01_LED/Test	t01_LED - Test0	1_LED - (Chain	1.cdf]*			-	-	_		X
Ele Edt View Processing Iools Search altera.com Search altera.com Iools Mode: JTAG Progress:												
Start	File	Device 10M02SCU169	Checksum 00030FC3	Usercode 00030FC3	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
Auto Detect												
Add File												
Add Device		- -1										
1 ^{mb} Up 1 ^{mb} Down		69										

Then toggle [Program/Configure] and click the [Start] button to start a new program:

Figure 2-19. Program *.sof

If the *.sof file is correctly programed, the Progress bar will show info like: 100%(Successful). Then users could check whether the LEDs on CPLD board blinking or not.



Figure 2-20. Program Successful



2.5 Program *.pof File into CPLD

The Quartus will generate *.pof file after the test project is correctly compiled. The *pof file could be program into CPLD's internal FLASH which means the content will not be kept even after repower on. Below image shows how to program the *.pof file by Programmer Tool:

SP to allow background	-0]	iable		Mode: JT	AG	•	Progress: 100%	(Successful)
File	Device	Select N	ew Programmir	ıg File				;
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		My Co	mputer Name	^	Size	Type	Date Modified	
		evelov	ely Test	01_LED.pof		82 KB pof File	2018/4/23 22:27:40	
						0017.00	LUIGINED EL ET. IU	
1	0M02SC							
↓		File name:	Test01_LED.pof					Open

Figure 2-21 Select * pof File

After correctly loaded *.pof file, toggle all the options in Program/Configure column. And then click the Start button to program the CPLD. Once the CPLD successfully programmed, users may re-plugin the Mini USB cable to repower on the development board. Then users could check whether the functionality implemented in *.pof is correctly executed.







Reference 3.

- [1] max10-10m02_08_core_board_v01.pdf
- [2] m10_datasheet.pdf[3] m10_handbook.pdf
- [4] m10_overview.pdf
- [5] ug_m10_adc.pdf
- [6] pcg-01014_Cyclone® V Device Family Pin Connection Guidelines.pdf
 [7] Intel® MAX® 10 FPGA Device Family Pin Connection Guidelines



4. Revision

	l	
Doc. Rev.	Date	Comments
0.1	30/12/2018	Initial Version.
1.0	11/01/2019	Formal Release.

