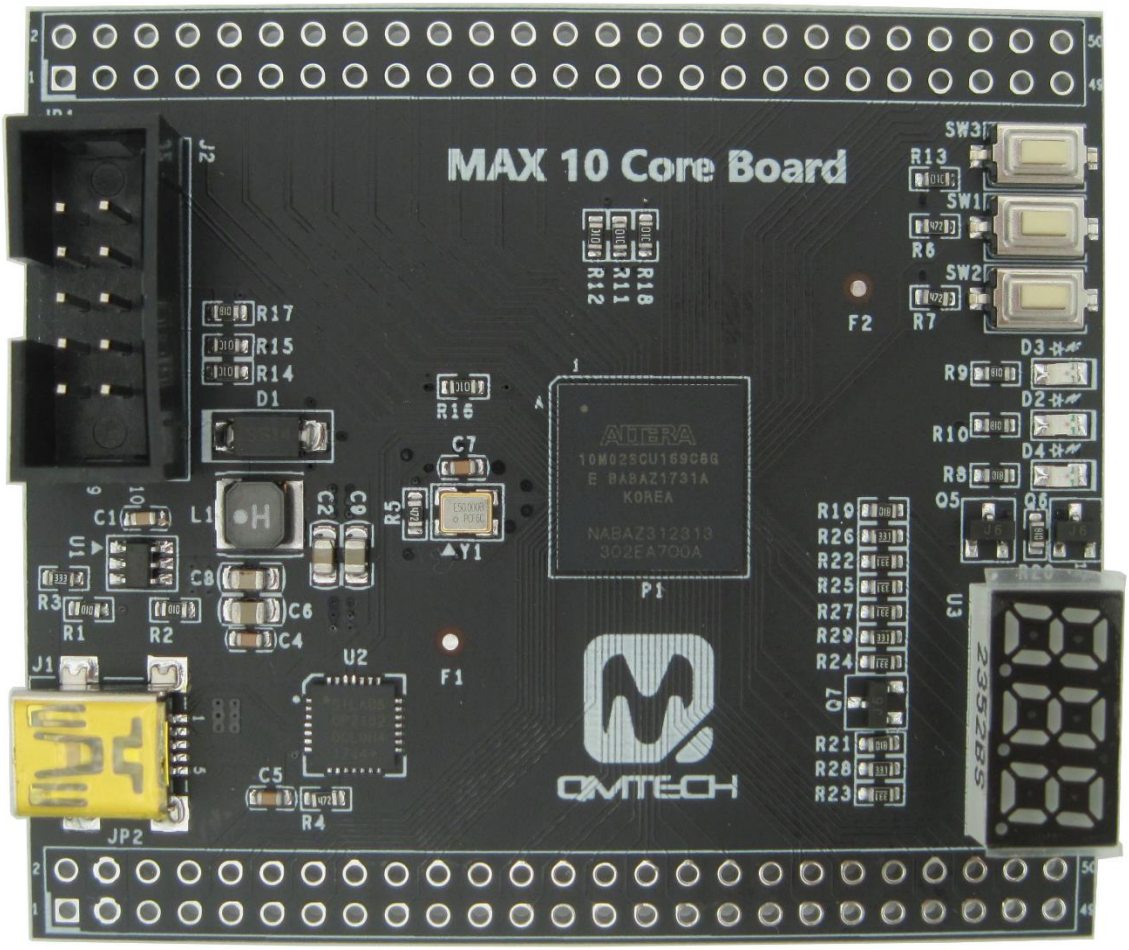
QM_MAX10_10M02SCU169 DB

USER MANUAL(QUARTUS 15.1)



Preface

The QMTech® QM_MAX10_10M02SCU169 Development Board uses Intel® 10M02SCU169 device to demonstrate Intel® MAX® 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single chip small form factor programmable logic device. Building upon the single chip heritage of previous MAX device families, densities range from 2K – 50K LEs, using either single or dual-core voltage supplies. The MAX 10 FPGA family encompasses both advanced small wafer scale packaging (3 mm x 3 mm) and high I/O pin count packages offerings.

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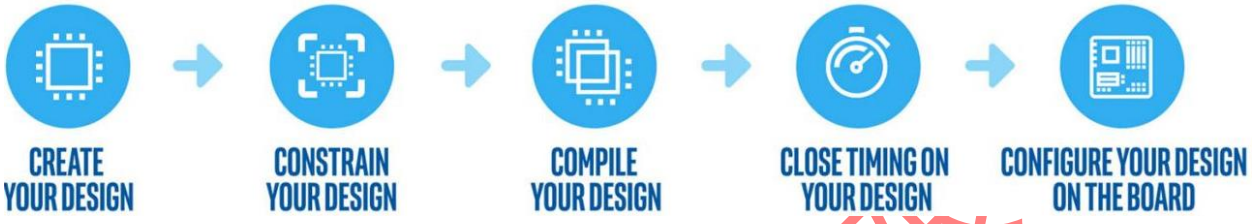
1. Quartus Prime 15.1 Installation

The revolutionary Intel® Quartus® Prime Design Software includes everything you need to design for Intel® FPGAs, SoCs, and CPLDs from design entry and synthesis to optimization, verification, and simulation. Dramatically increased capabilities on devices with multi-million logic elements are providing designers with the ideal platform to meet next-generation design opportunities.

The Intel® Quartus® Prime Software design flow comprises of the following high-level steps:



The Quartus Prime software version 15.1 supports the following device families: Stratix IV, Stratix V, Arria II, Arria V, Arria V GZ, Arria 10, Cyclone IV, Cyclone V, MAX II, MAX V, and MAX 10 FPGA. Below image shows the startup UI of Quartus II Prime 15.1:

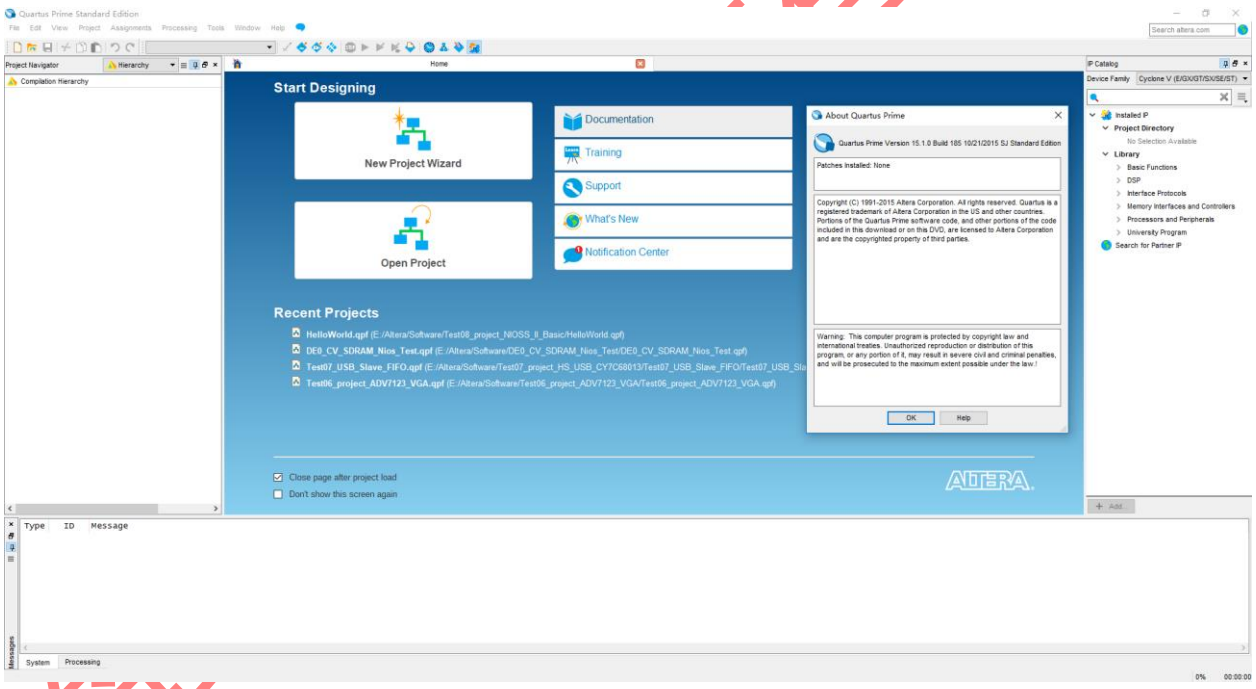


Figure 1-1. Quartus II Prime 15.1

After the Quartus II Prime 15.1 is correctly installed, users still need to install the device package from Intel official website. Below lists the download center address:

https://www.intel.com/content/www/us/en/programmable/downloads/download-center.html

In the Intel Download Center website, select the tab of ' Select by Device' and then all the available device packages will be listed as below image. The device used in this user manual is MAX10 series CPLD and the detailed chip part number is 10M02SCU169C8G, so please download the device package for Quartus II 15.1: max10-15.1.0.185.qdz.

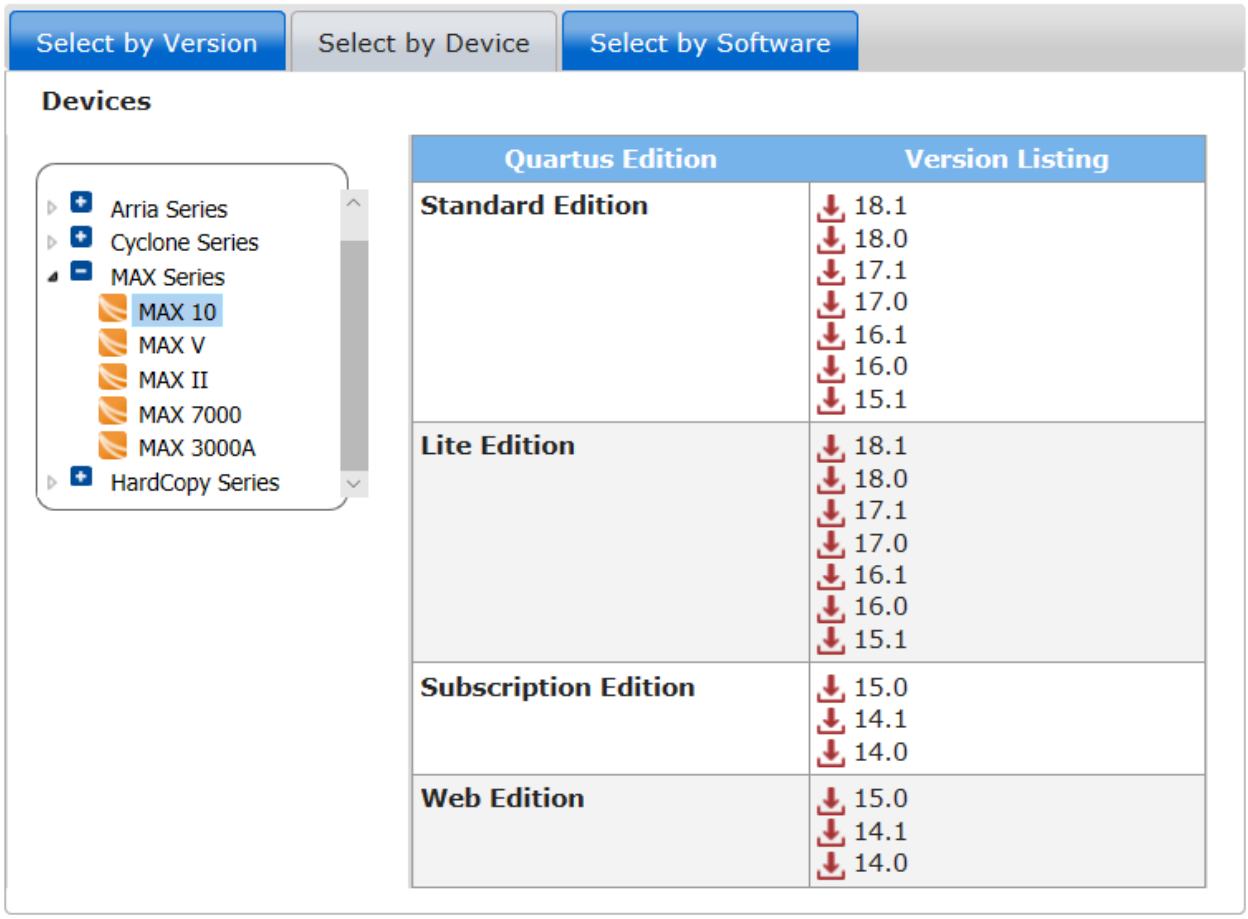


Figure 1-2. Download Device Package

Open Quartus II 15.1, Click Tools → Install Device and then select the downloaded device package:

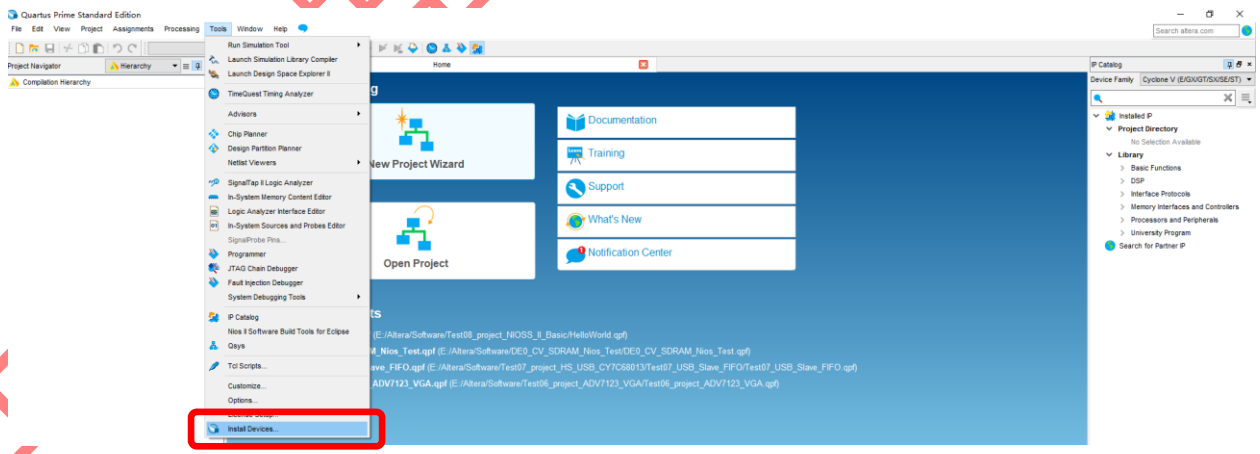


Figure 1-3. Install Device Package

Below window will pop up and click Next:

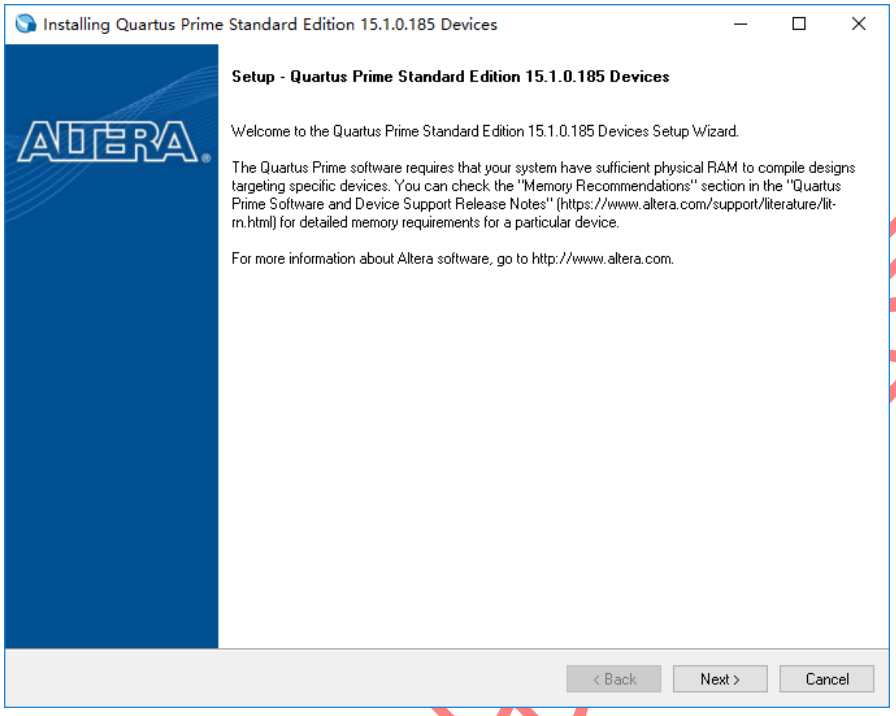


Figure 1-4. Install Device Package

Choose the Download Directory where contains the max10-15.1.0.185.qdz file:

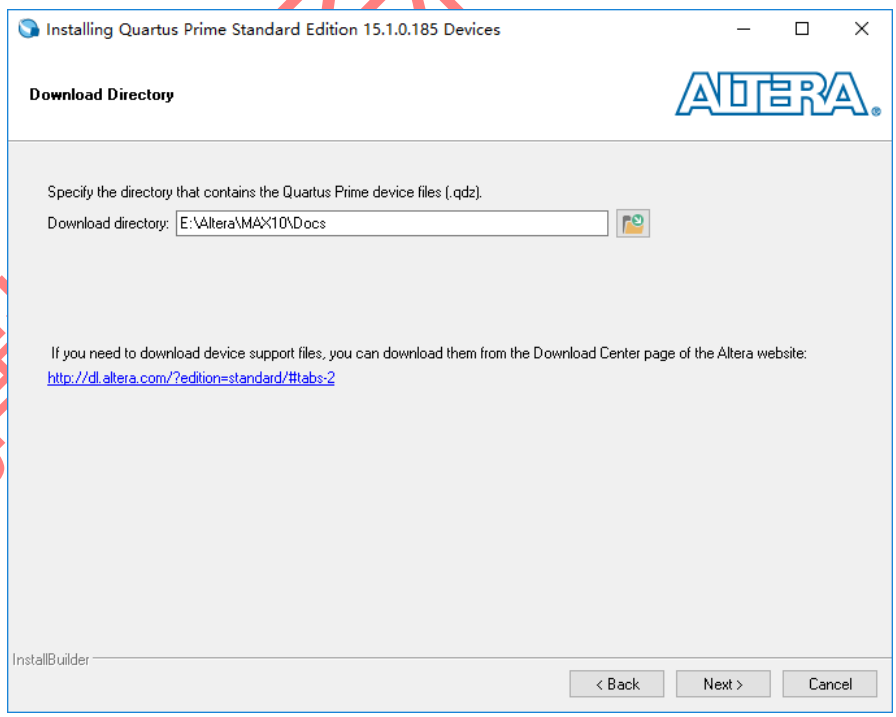


Figure 1-5. Choose Device Package

Choose the device package needs to be installed and click Next:

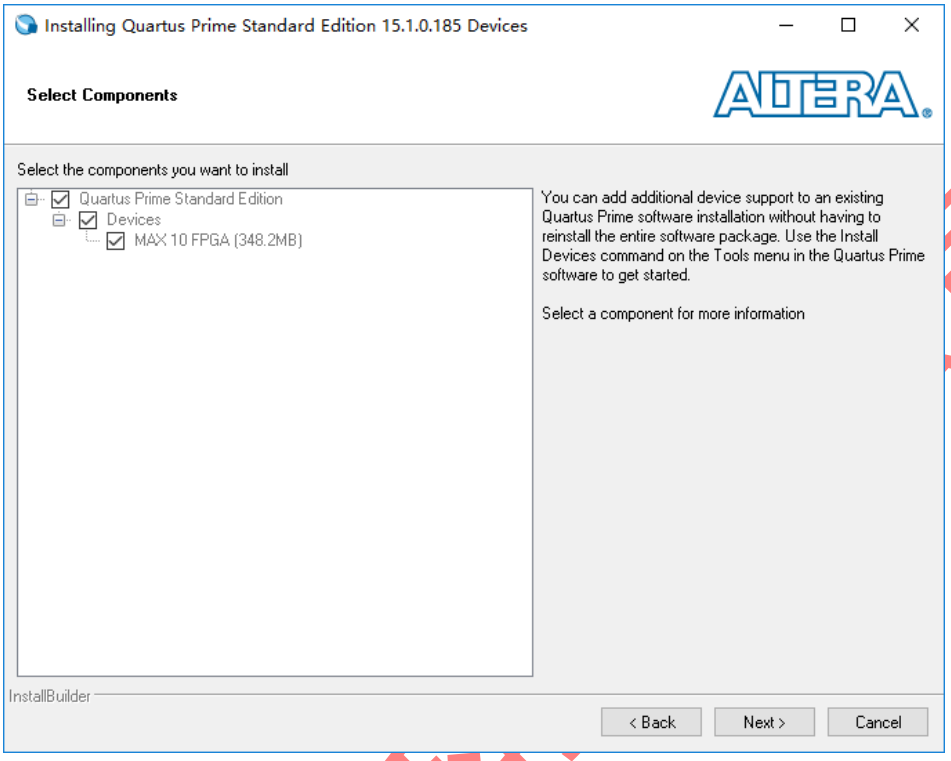


Figure 1-6. Install the Device Package

User could also install the device package by using Quartus II Prime 15.1 Device Installer directly:

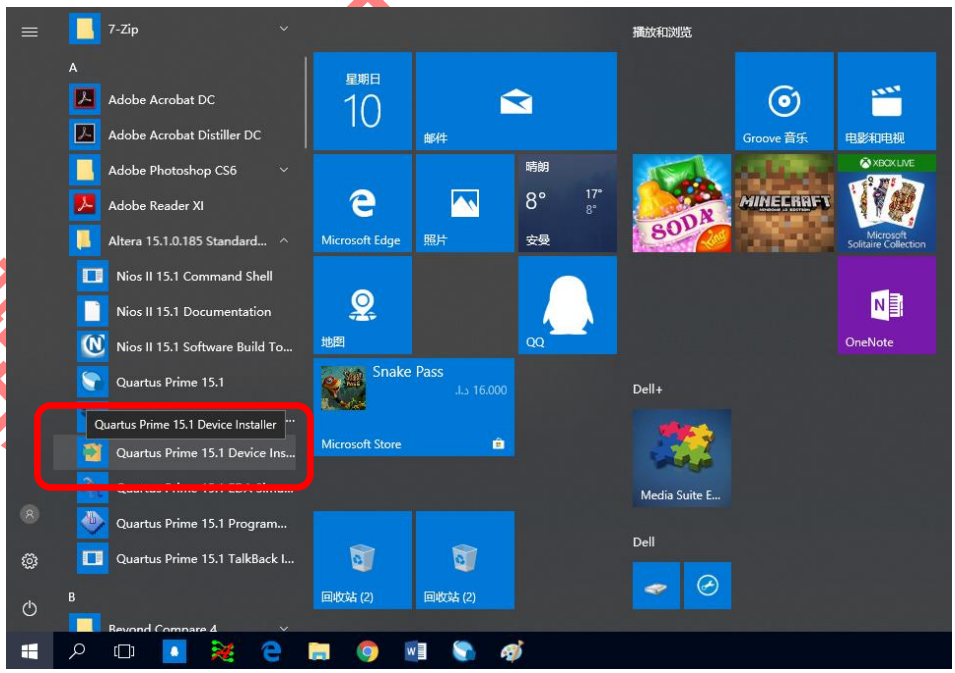


Figure 1-7. Device Installer

2. CPLD Project Compile and Download

2.1 Create New Project

Click【File】→【New Project Wizard…】 to create a new project:

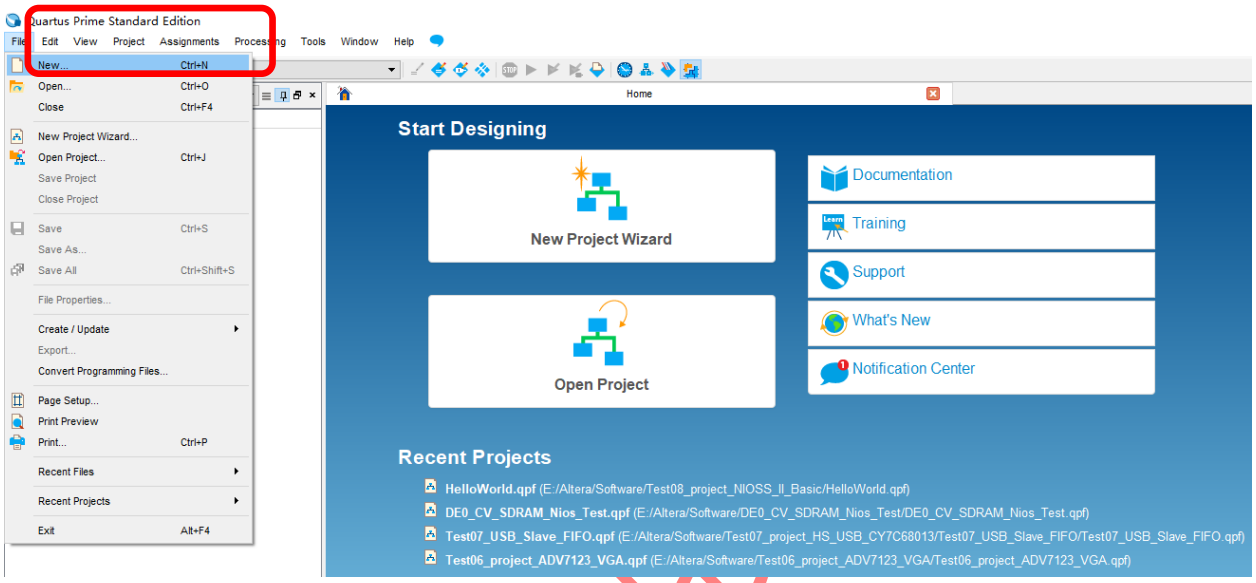


Figure 2-1. Create New Project

Choose【New Quartus Prime Project】:

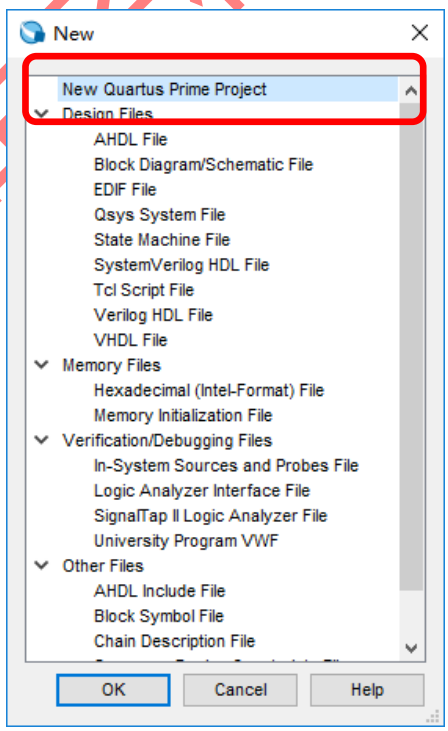


Figure 2-2. New Quartus Prime Project

In below【New Project Wizard】page, choose Next:

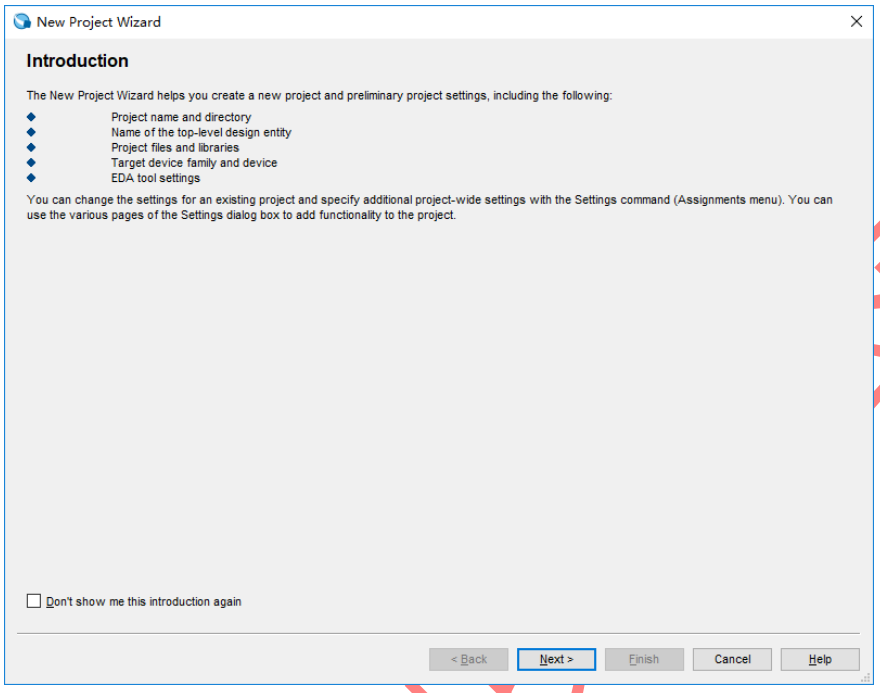


Figure 2-3. New Project Wizard

Set the target working folder below 【What is the working directory for this project?】. Set the new project name below 【What is the name of this project?】. And finally set the example project name: Test01_Project_LED shown as below.

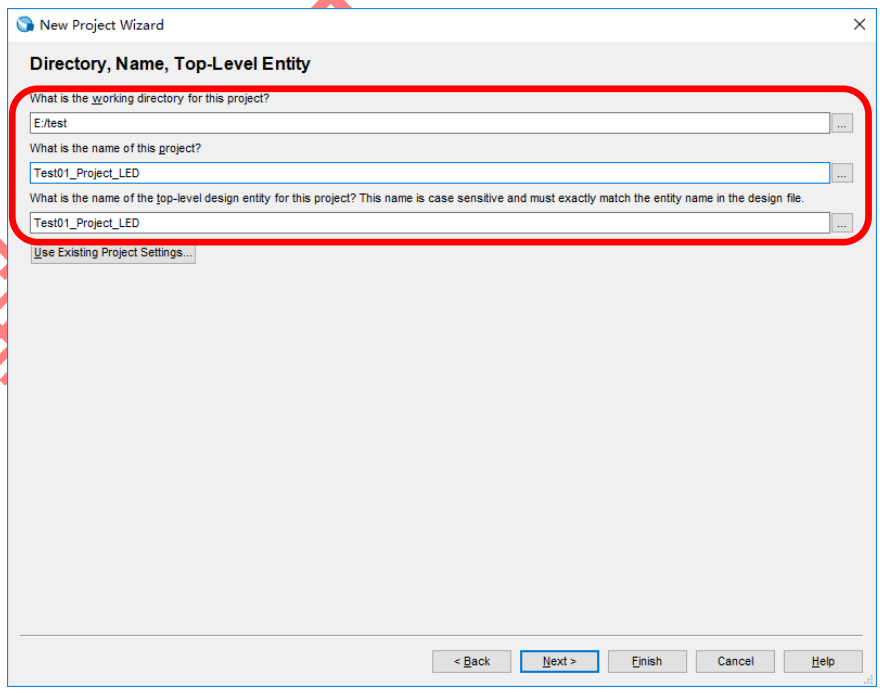


Figure 2-4. Set Working Directory and Project Name

Select【Empty Project】and then click Next:

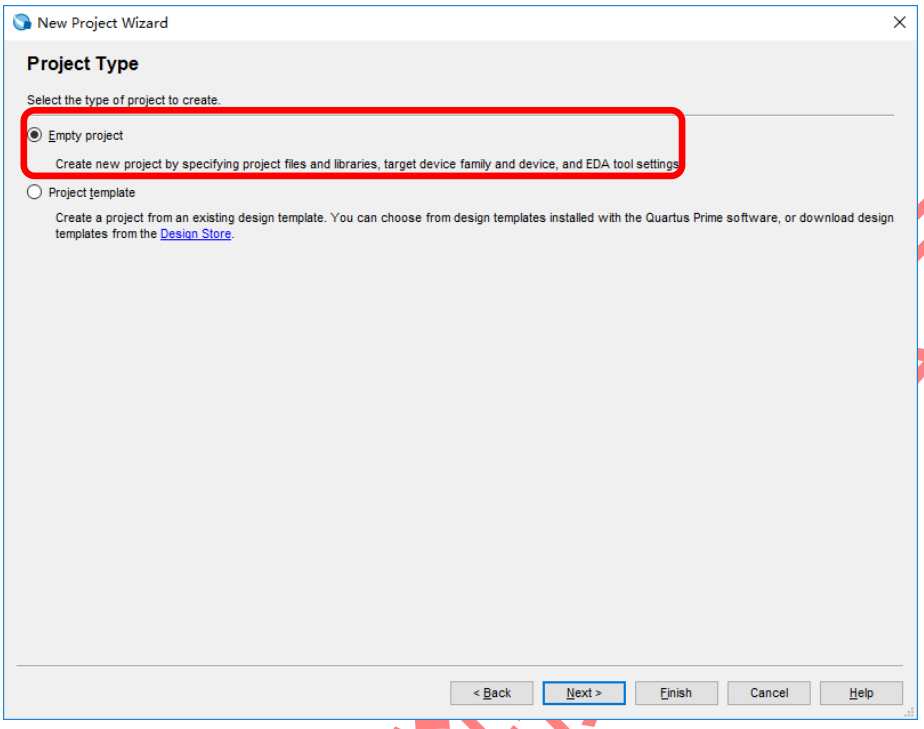


Figure 2-5. Create Empty Project

If user already has some source code, please add all these necessary files in this step:

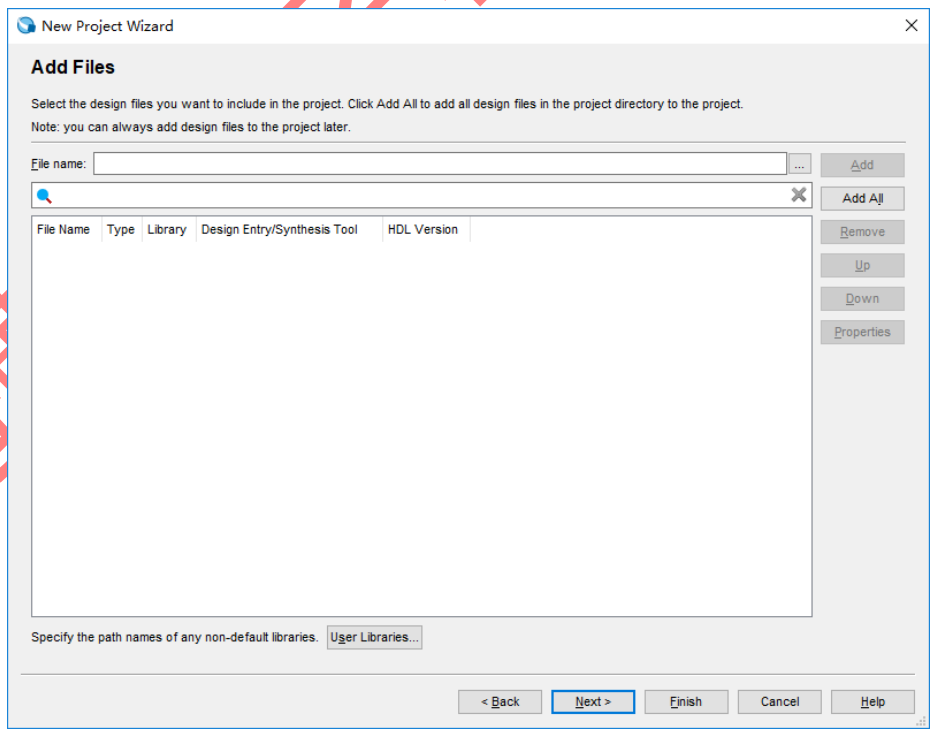


Figure 2-6. Add Source Code

Choose the CPLD Chip number: 10M02SCU169C8G

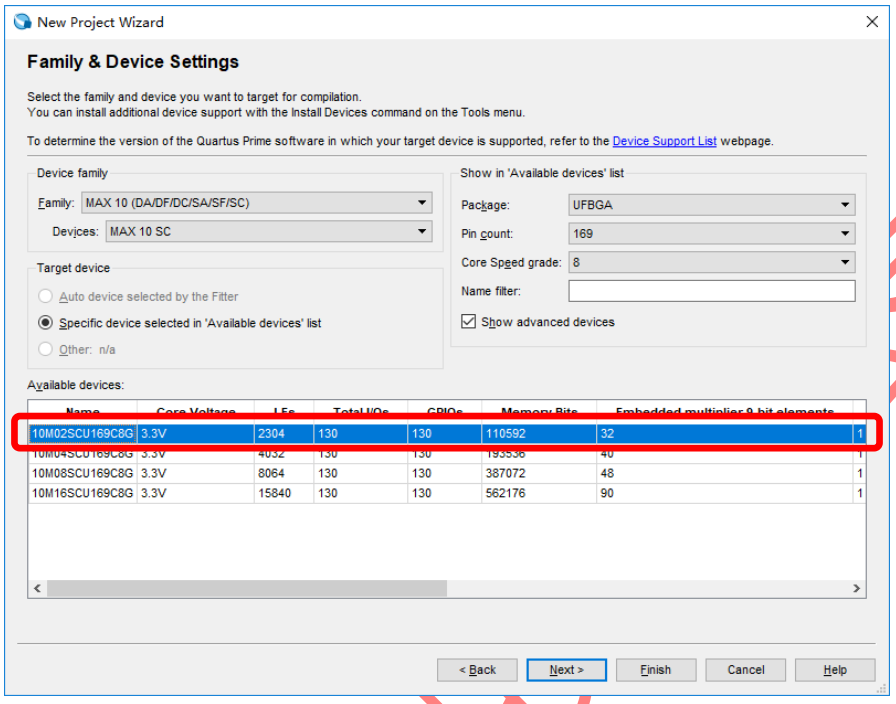


Figure 2-7. Select Device

Summary page will be shown and click【Finish】if there's nothing needs to be changed:

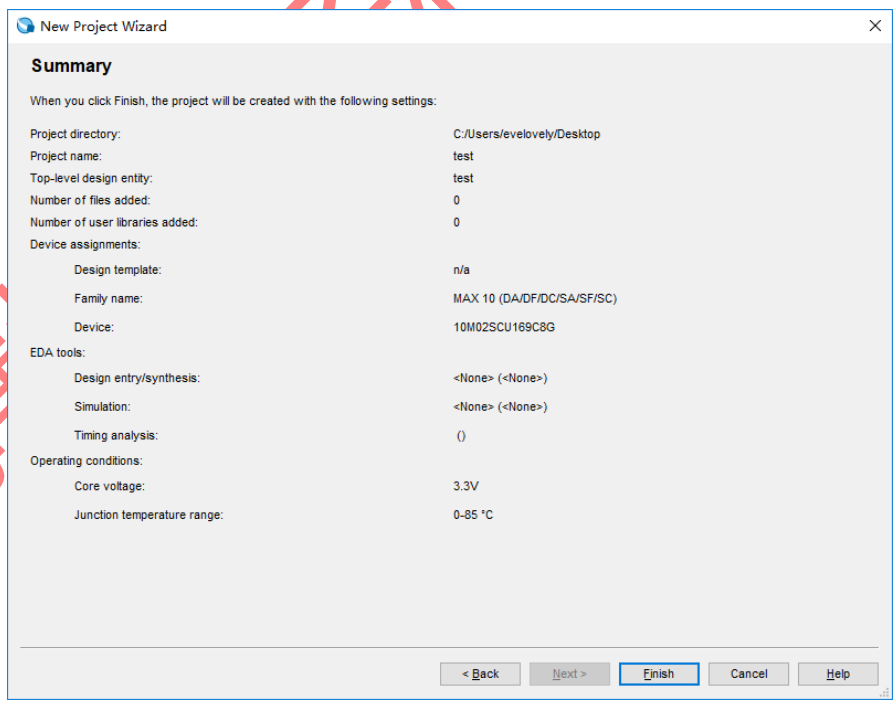


Figure 2-8. Project Summary

After the Empty Project created, below image will be shown:

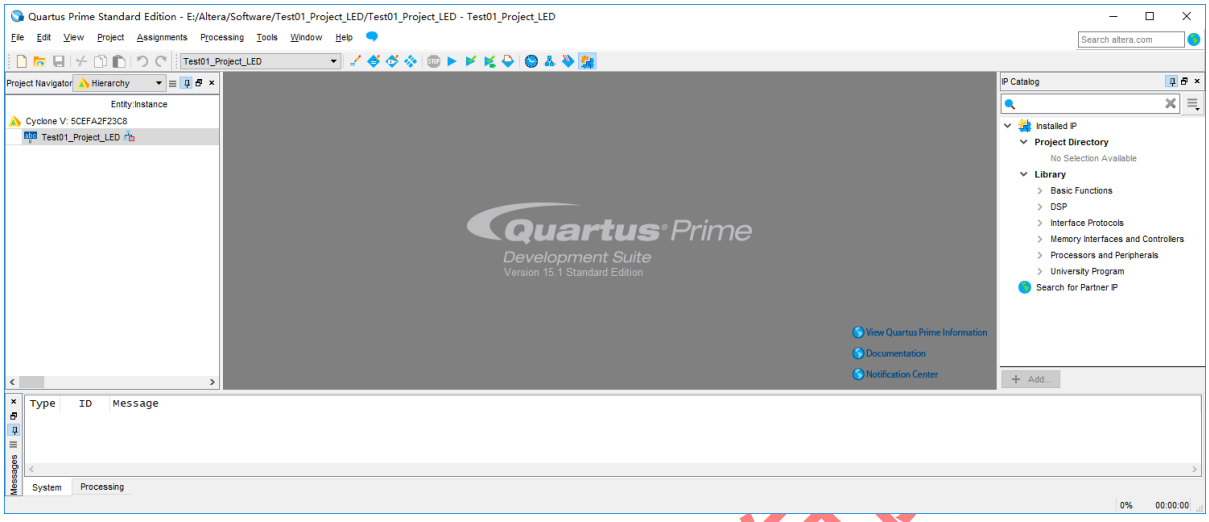


Table 2-1. Empty Project

Users may add example source file Test01_Project_LED.v into this Empty Project shown as below:

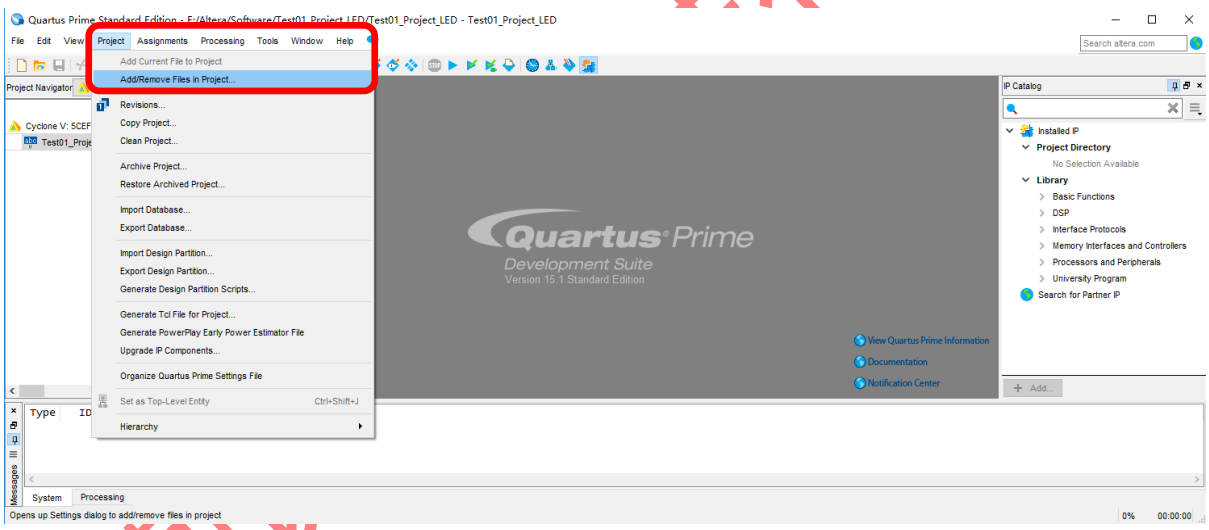


Table 2-2. Add Source File

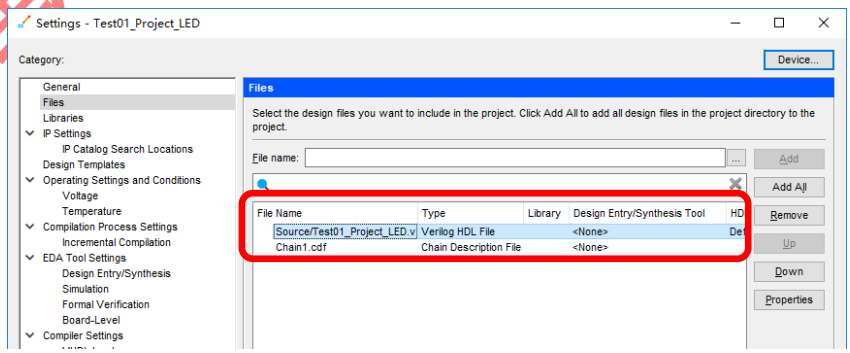


Table 2-3. Add Source File

After the newly added source file loaded into project, user can view the source code shown as below:

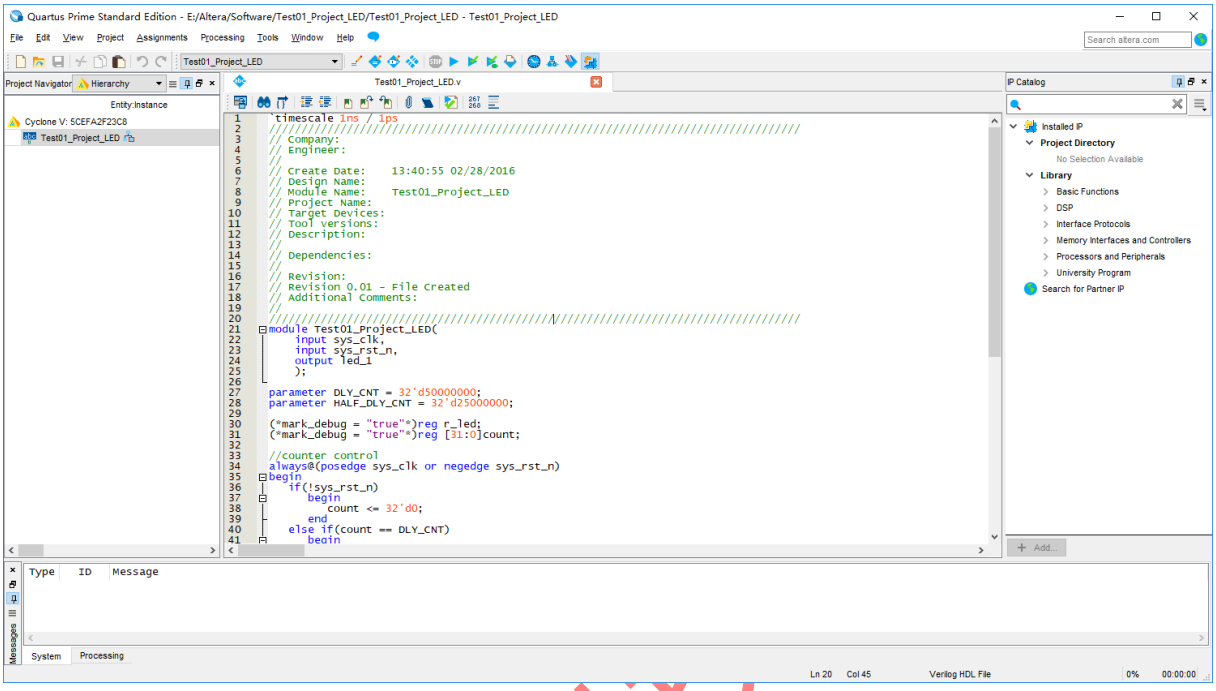


Figure 2-9. View of Source Code

2.2 Compile the Project

Users could use the button【Start Compilation – Ctrl + L】shown in below image to compile the project:

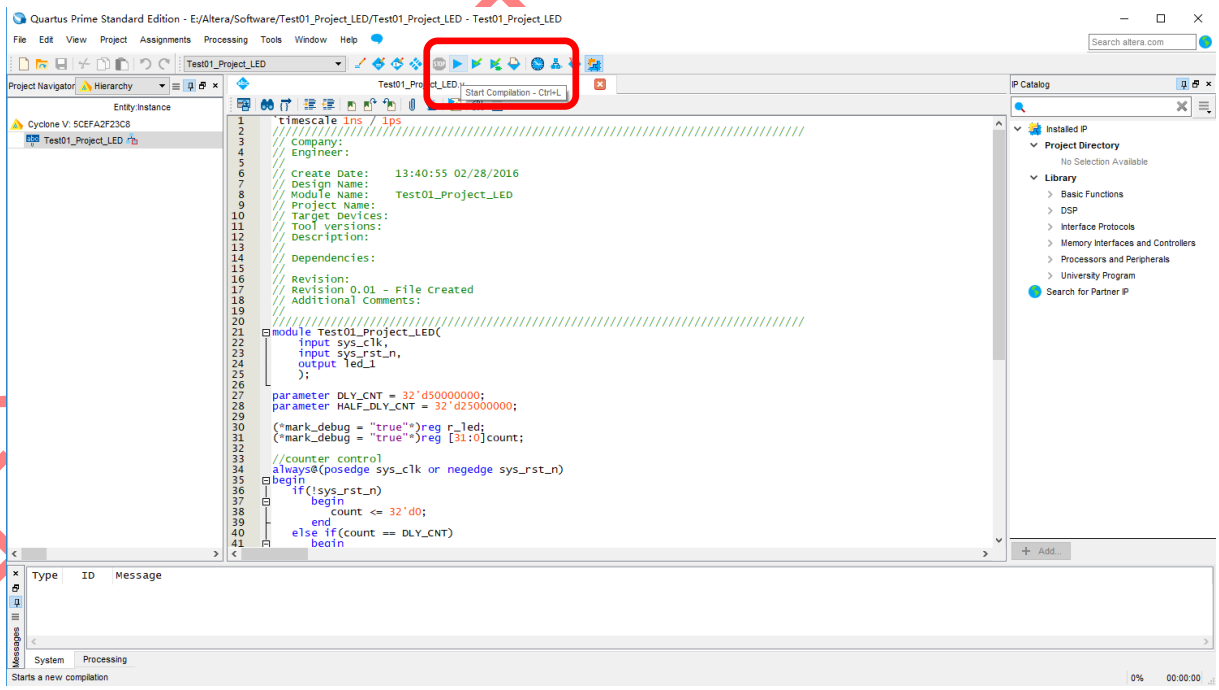


Figure 2-10. Compilation

There will be compilation report after the compile finished, in which shows the info like logical element resource usage, how many PLLs are used, etc. Below image shows an example Compilation Report:

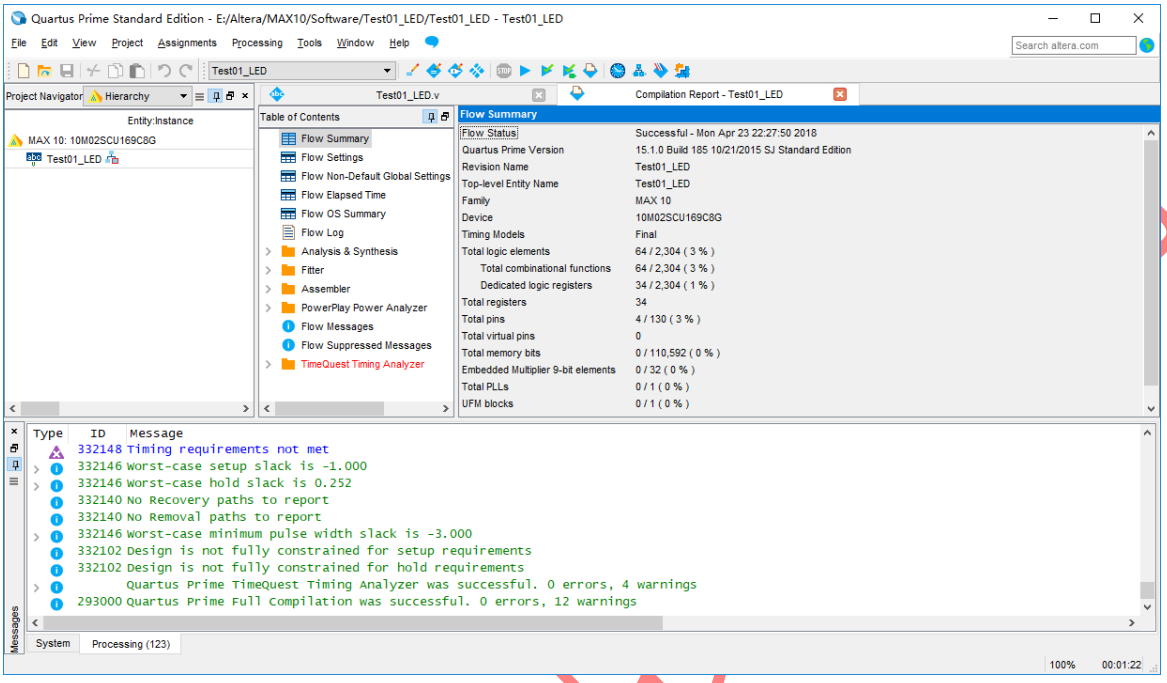


Figure 2-11. Compilation Report

2.3 PIN Assignment

There are several ways to assign the Pins for the example project. Method 1: Choose【Assignment】→【Pin Planner】:

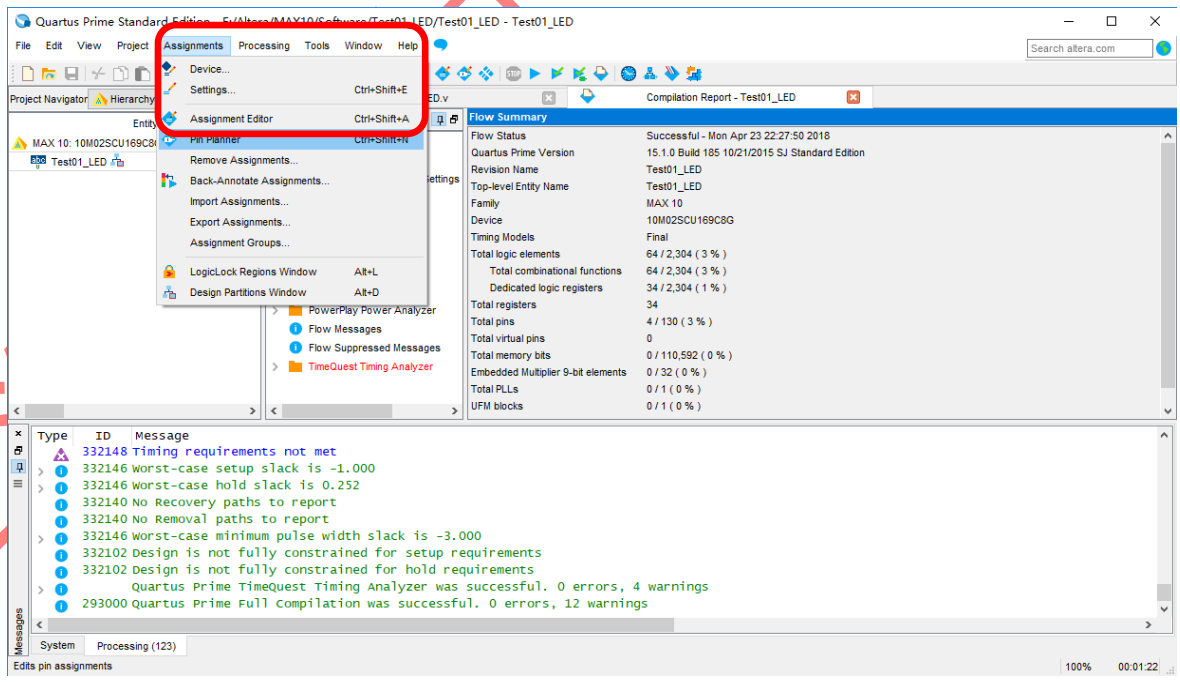


Figure 2-12. Pin Planner

Below image shows PIN settings for this test example:

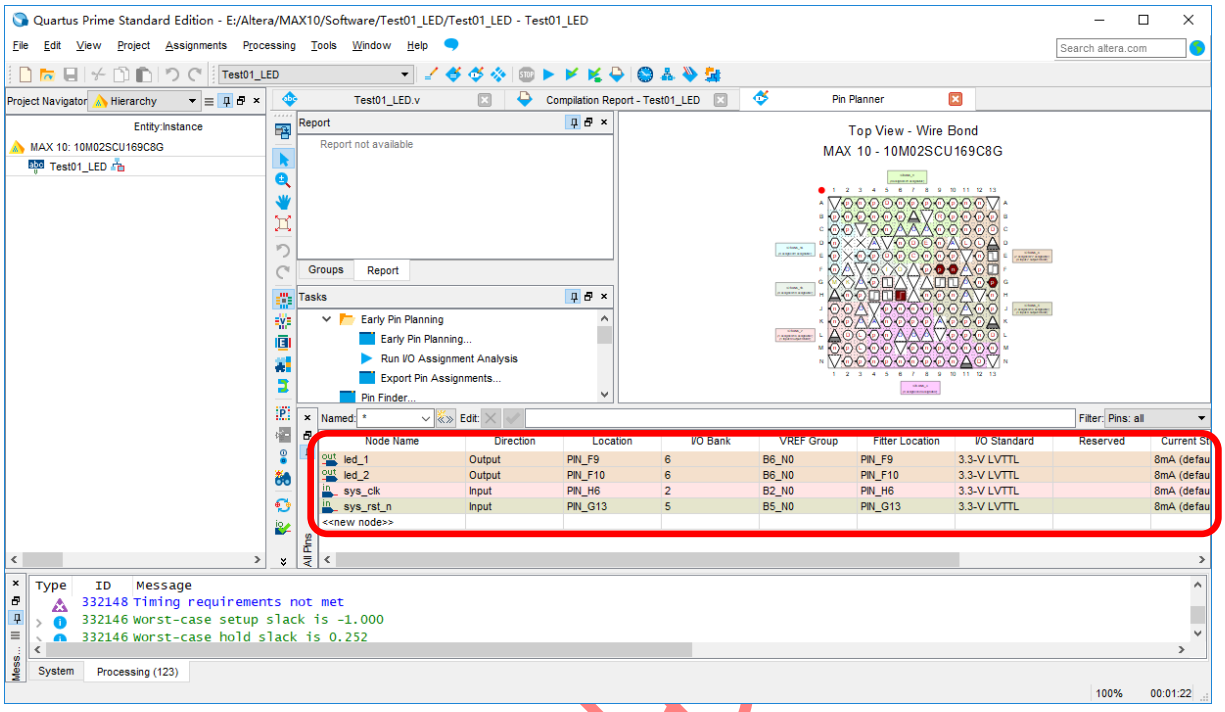


Figure 2-13. PIN Assignment

Method 2: Prepare a *.csv file from other project, then use【Assignment】→ 【Import Assignment】to import the existing *.csv file to allocate the Pin assignment:

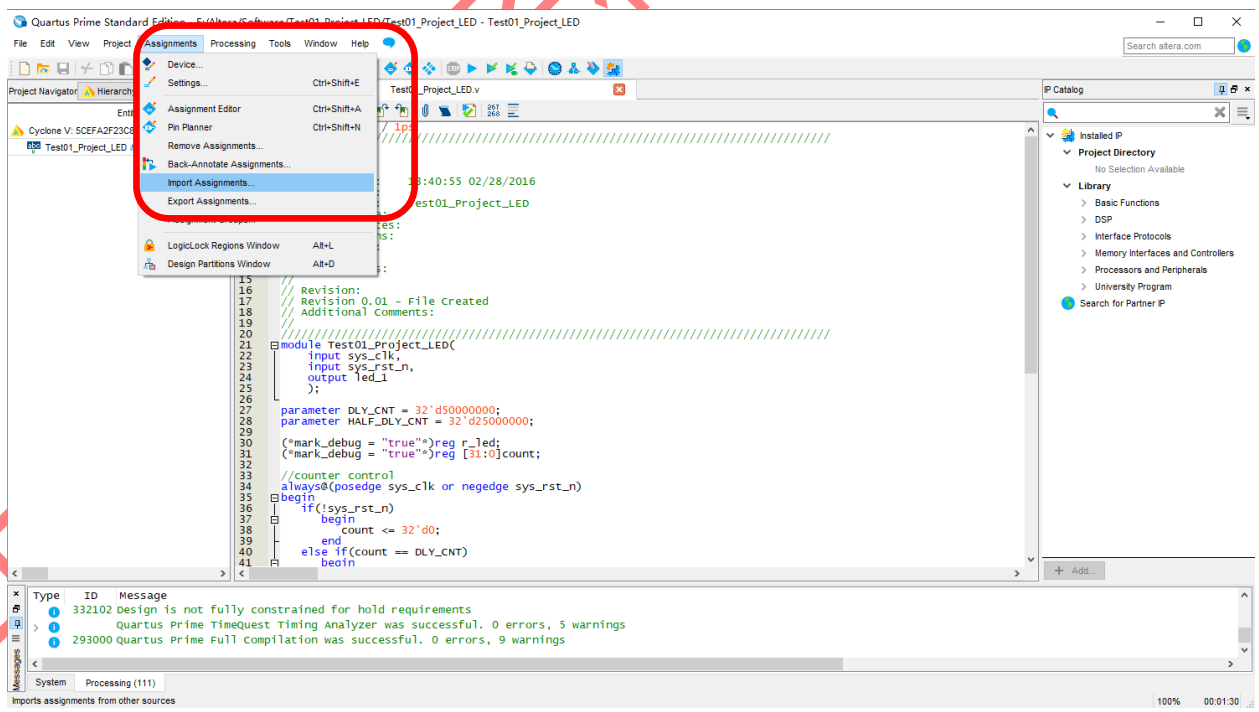


Figure 2-14. Import Assignment

2.4 Download *.sof into FPGA

After the test example correctly compiled, the Quartus will generate a *.sof file which could be directly loaded into FPGA to check whether implemented functions perform as expected. User could use 【Tools】→【Programmer】to start a new download:

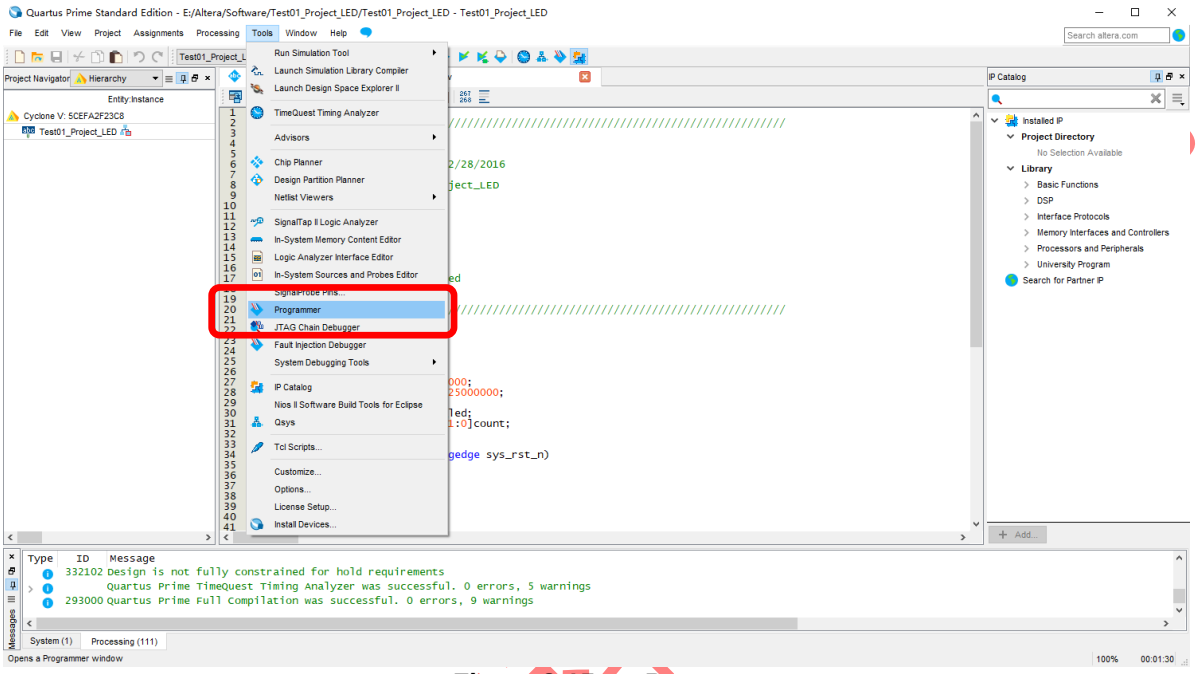


Figure 2-15. Programmer

Make sure the USB Blaster's cable are correctly connected to CPLD's JTAG port before using Programmer to download *.sof file. Then click【Auto Detect】to check the hardware setup is okay or not:

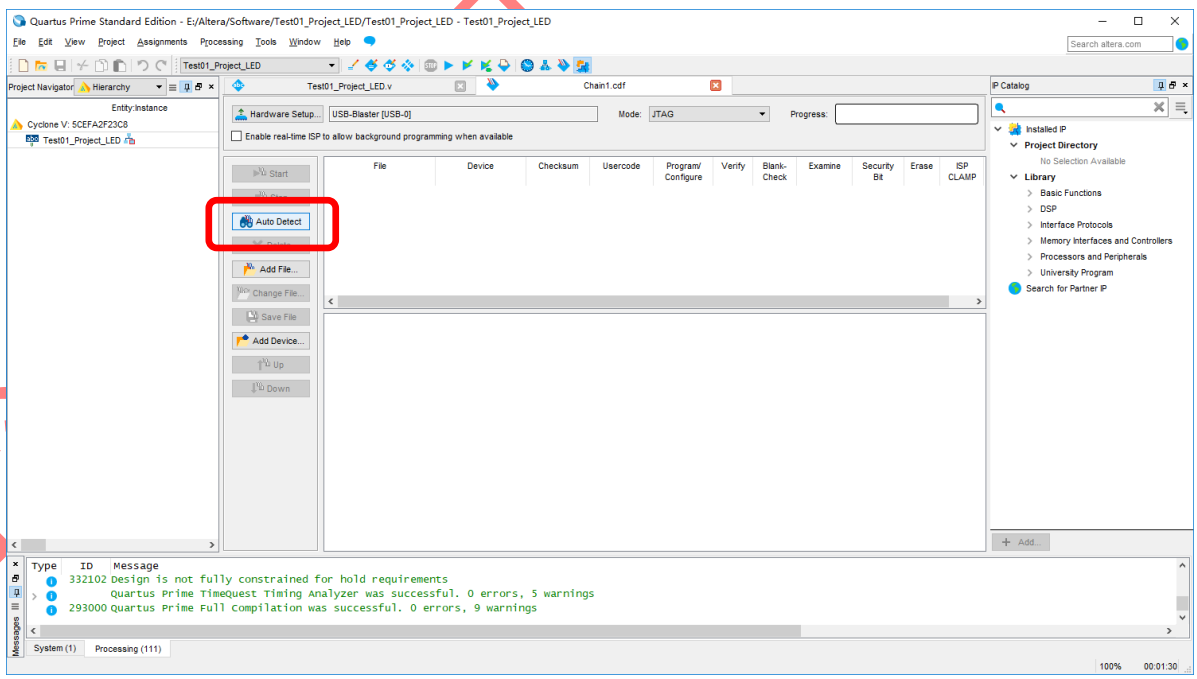


Figure 2-16. JTAG Setup

Below image shows the CPLD has been detected by the Programmer:

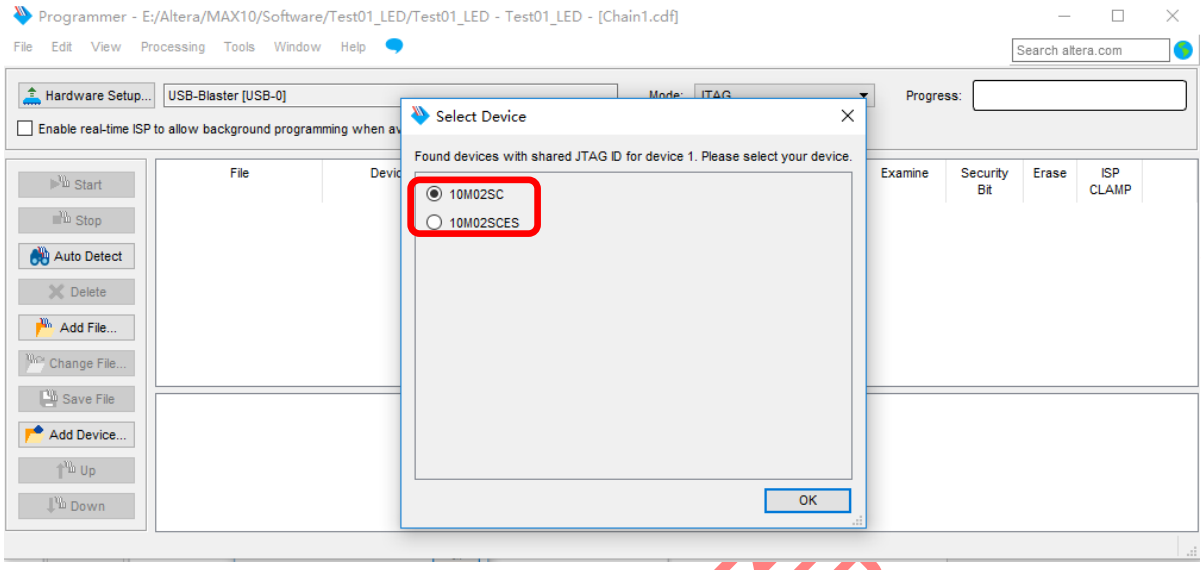


Figure 2-17. Detect CPLD

Users click【None】column to choose the *.sof file to be loaded into CPLD.

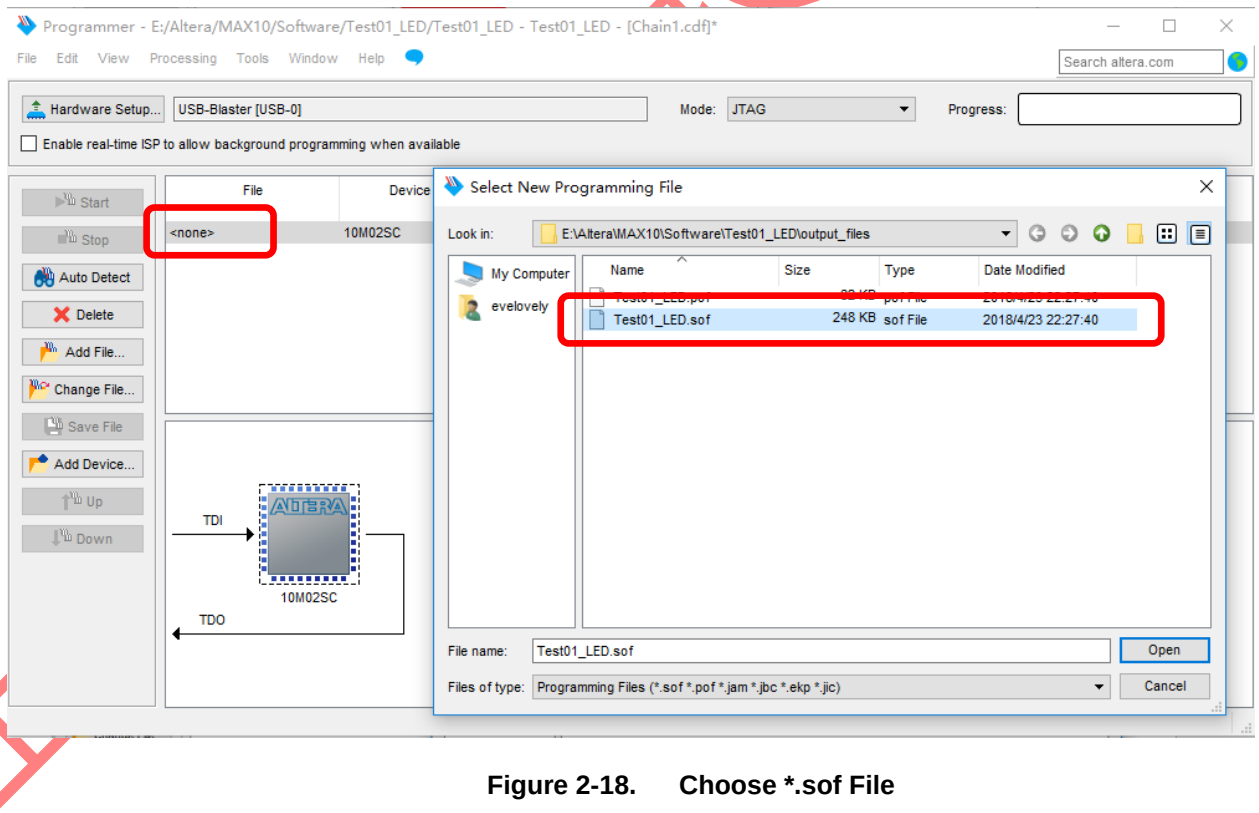


Figure 2-18. Choose *.sof File

Then toggle【Program/Configure】 and click the【Start】button to start a new program:

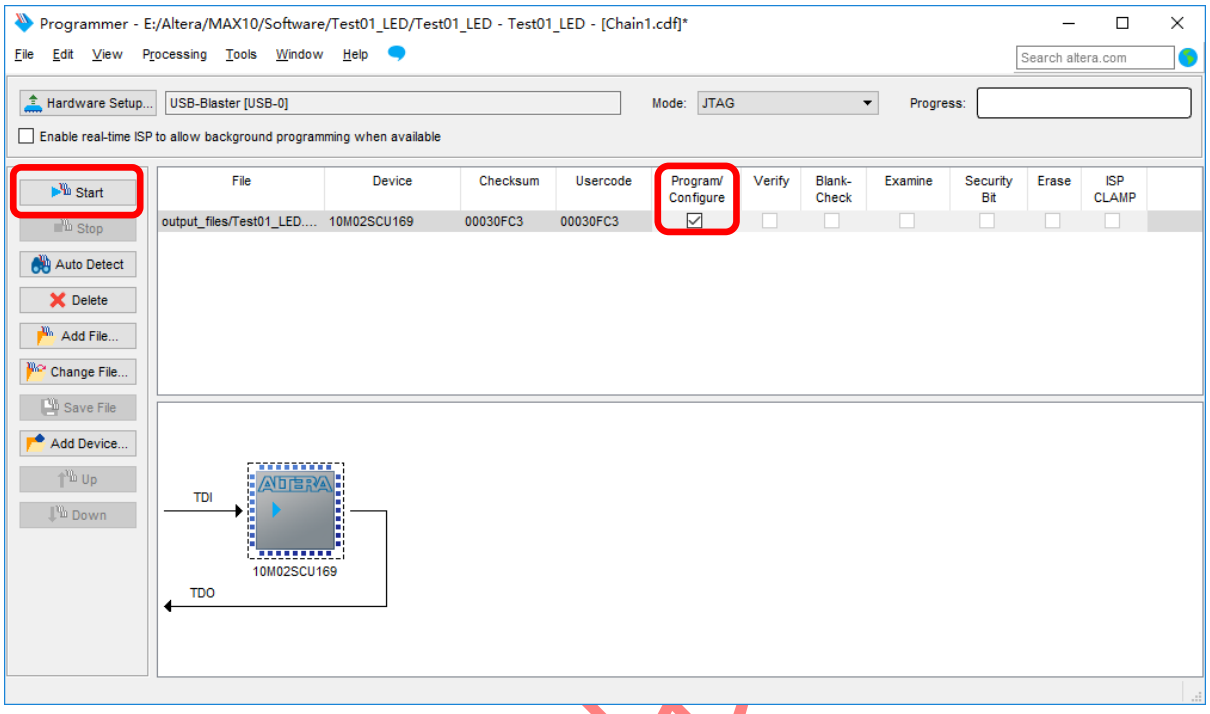


Figure 2-19. Program *.sof

If the *.sof file is correctly programed, the Progress bar will show info like: 100%(Successful). Then users could check whether the LEDs on CPLD board blinking or not.

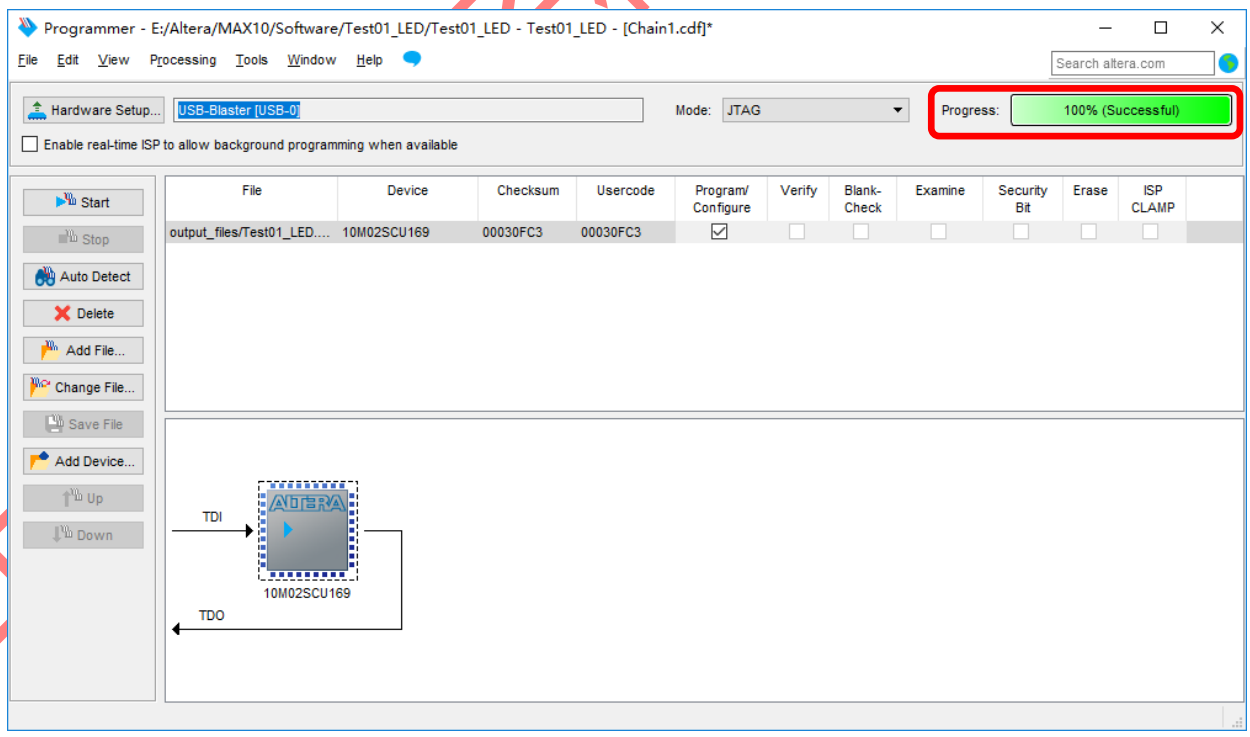


Figure 2-20. Program Successful

2.5 Program *.pof File into CPLD

The Quartus will generate *.pof file after the test project is correctly compiled. The *pof file could be program into CPLD's internal FLASH which means the content will not be kept even after repower on. Below image shows how to program the *.pof file by Programmer Tool:

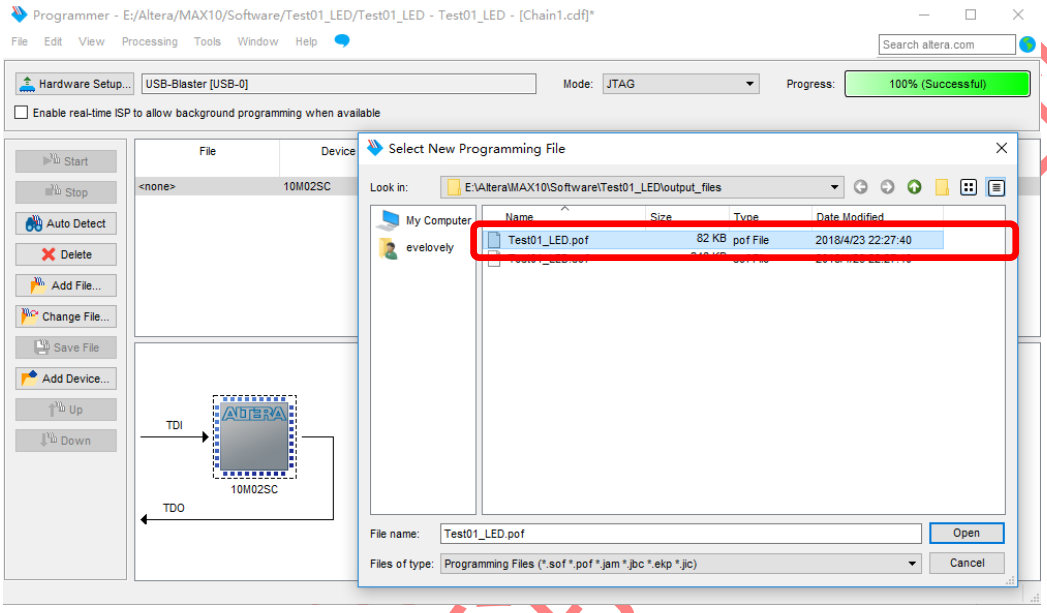


Figure 2-21. Select *.pof File

After correctly loaded *.pof file, toggle all the options in Program/Configure column. And then click the Start button to program the CPLD. Once the CPLD successfully programmed, users may re-plugin the Mini USB cable to repower on the development board. Then users could check whether the functionality implemented in *.pof is correctly executed.

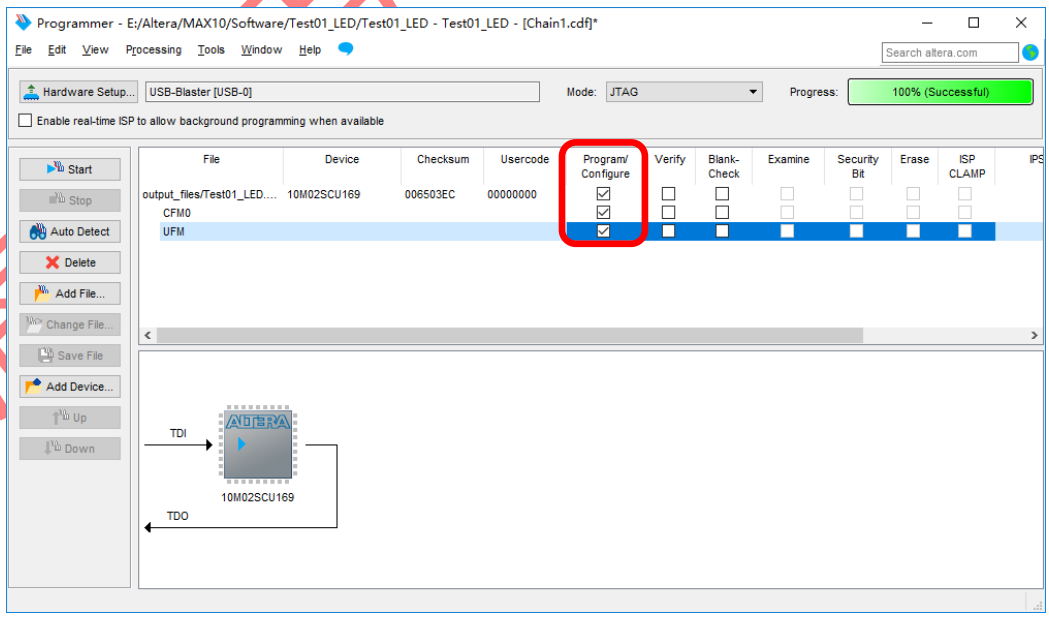


Figure 2-22. Program *.pof

3. Reference

[1] max10-10m02_08_core_board_v01.pdf
[2] m10_datasheet.pdf
[3] m10_handbook.pdf
[4] m10_overview.pdf
[5] ug_m10_adc.pdf
[6] pcg-01014_Cyclone® V Device Family Pin Connection Guidelines.pdf
[7] Intel® MAX® 10 FPGA Device Family Pin Connection Guidelines

4. Revision

Doc. Rev.	Date	Comments
0.1	30/12/2018	Initial Version.
1.0	11/01/2019	Formal Release.