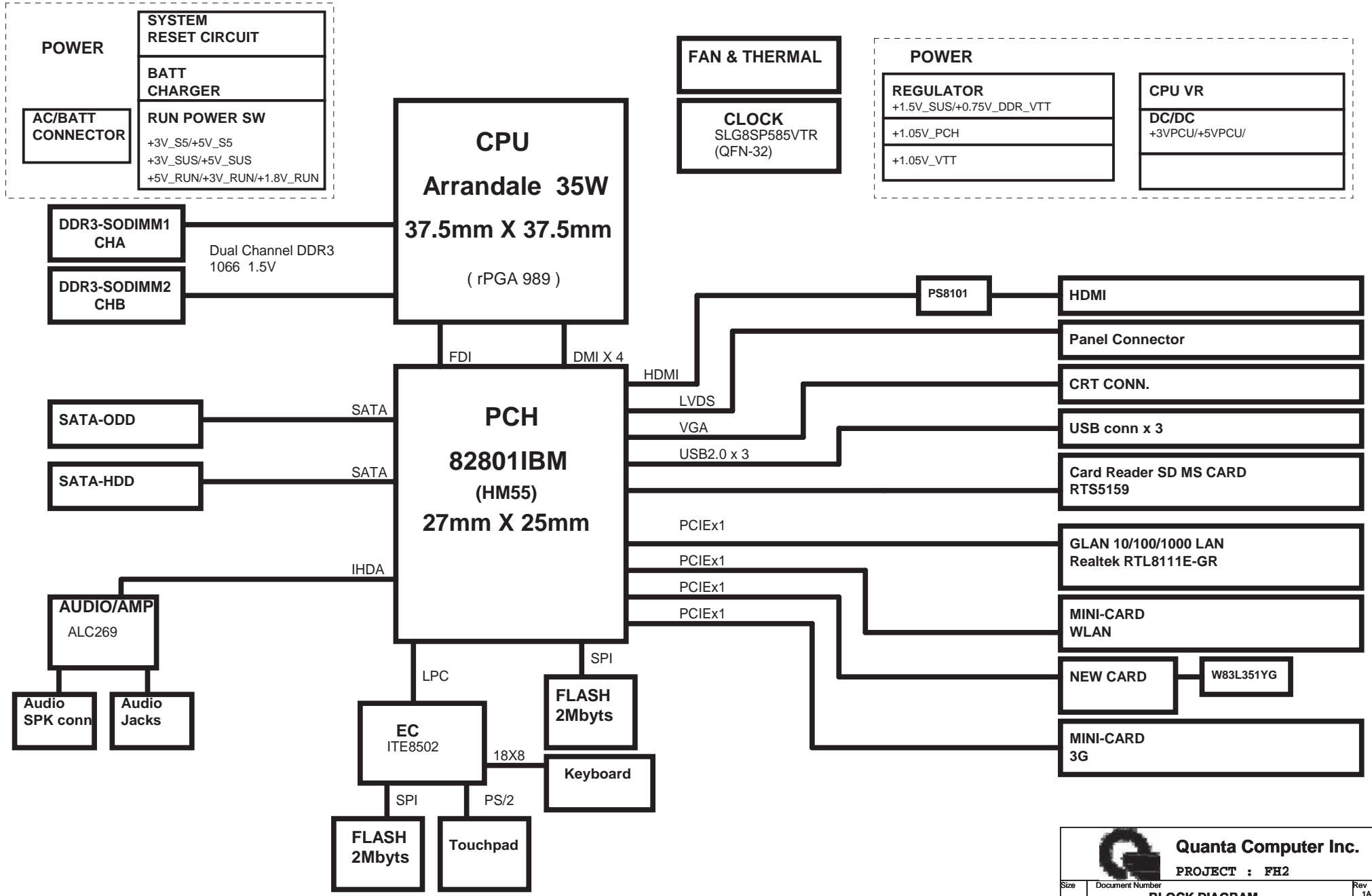


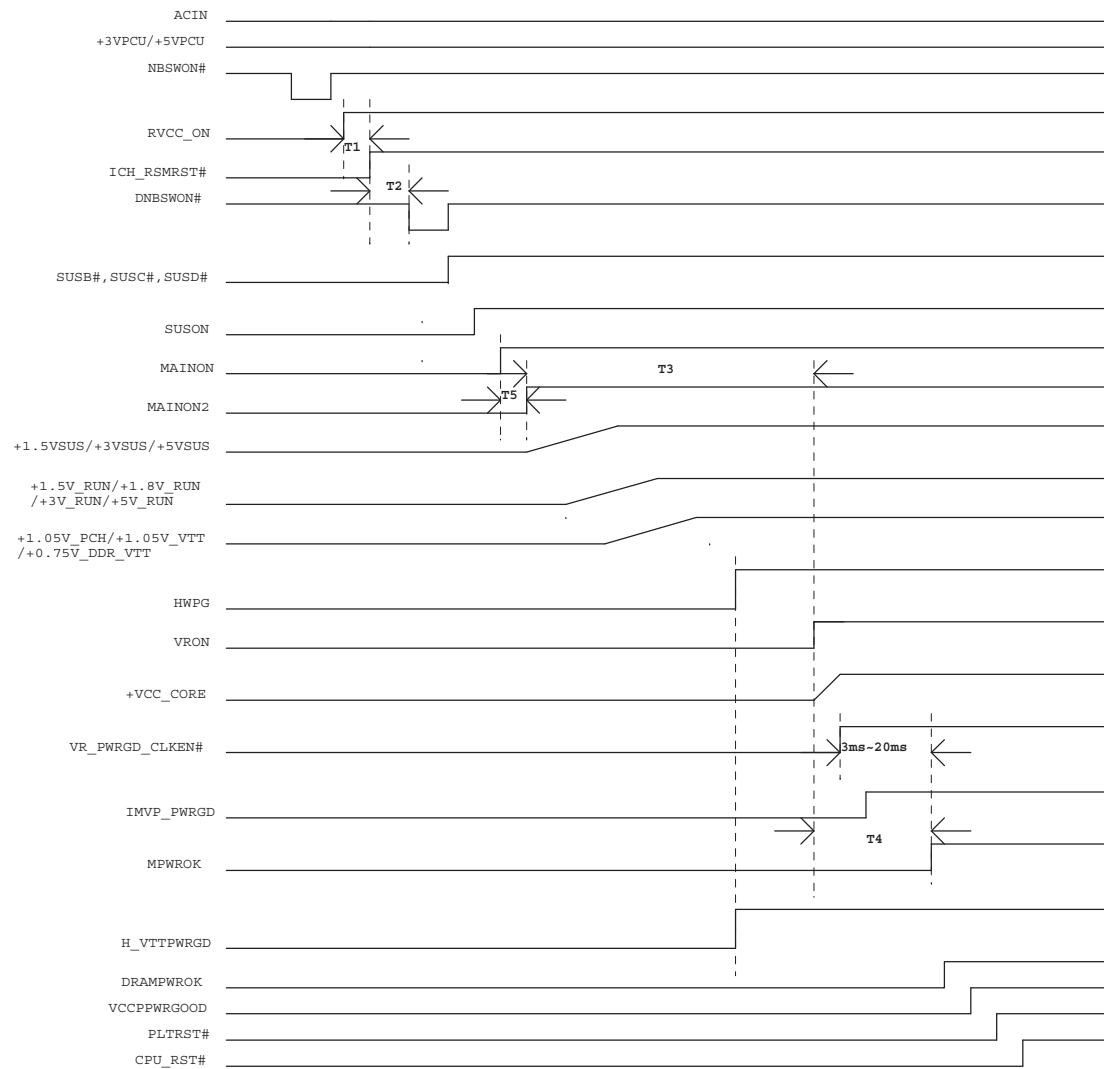
Intel Calpella BLOCK DIAGRAM

Intel Calpella Arrandale UMA

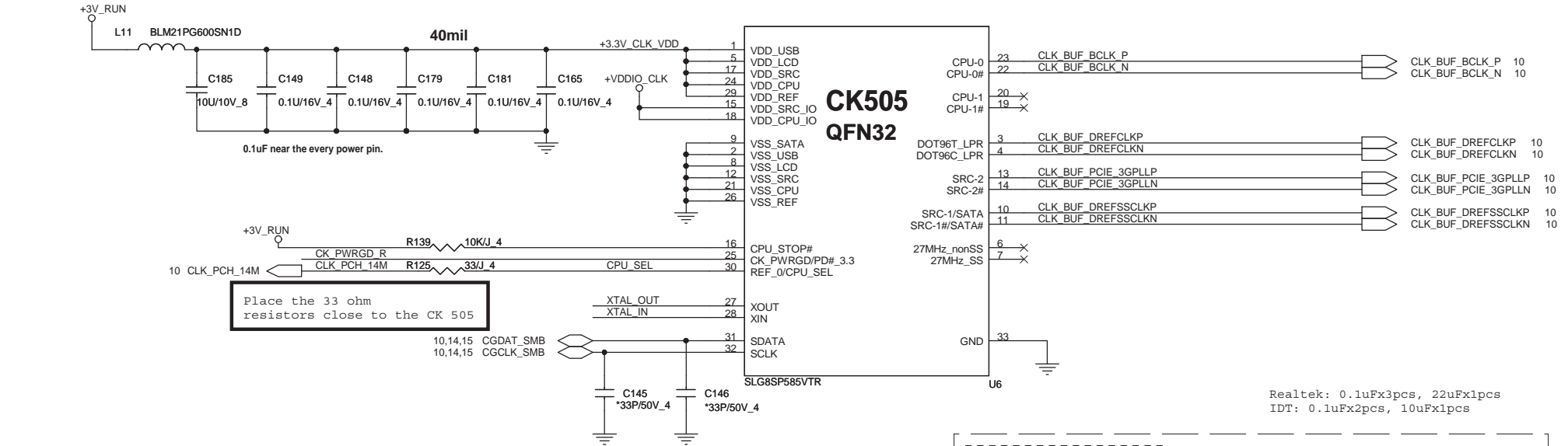


Power Sequence

PAGE	DESCRIPTION
01	Schematic Block Diagram
02	Front Page
03	Clock Generator
04-07	Arrandale
08-13	Ibex Peak-M
14-15	DDRIII SO-DIMM(204P)
16	LCD/CCD CONN
17	CRT CONN
18	Card Reader (RTS5159)
19	LAN RTL8111E-GR/RJ45
20	HDD/ODD/HOLE
21	USB/BLUE TOOTH
22	MINI-Card (WLAN/3G)/ XDP
23	KB/TOUCH PAD/LED
24	CODEC (ALC269)
25	EC_ITE8502
26	FAN/SW/NEWCARD
27	+5V/+3V (RT8206B)
28	+1.05V/+1.8V (RT8204C)
29	CPU Core (ADP3212)
30	+1.05V_VTT (VT358)
31	UMA GPU CORE (RT8152C)
32	DDR3 (RT8207)
33	DISCHARGE/3VS5/5VS5/LAN
34	CHARGER (ISL88731)
35	Clock Distribution
36	Power Tree
37	SMBUS Address

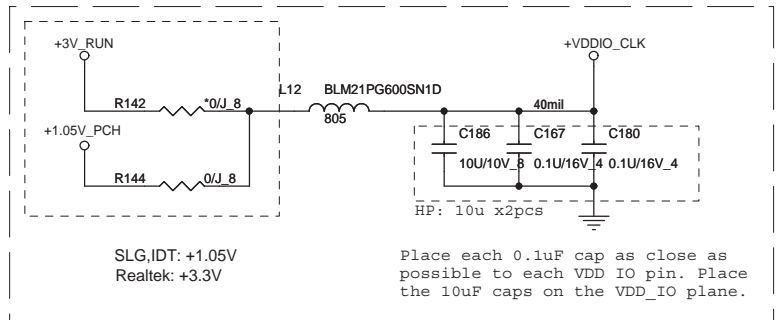
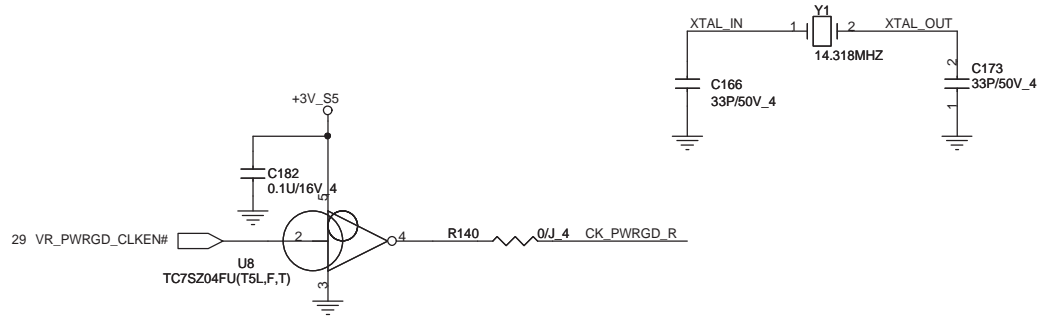


T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
 T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
 T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
 T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
 Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
 SPEC:3ms~20ms
 T5: MAINON to MAINON2 = 500us



Place the 33 ohm resistors close to the CK 505

Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



SLG.IDT: +1.05V
Realtek: +3.3V

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

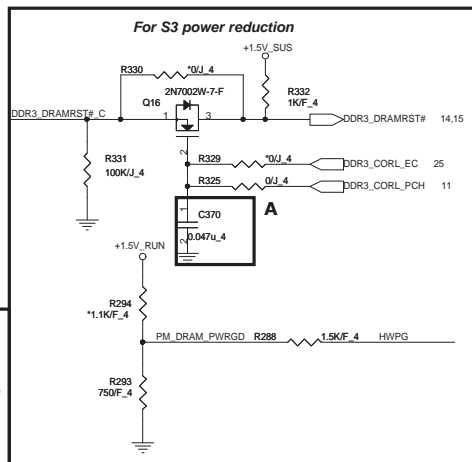
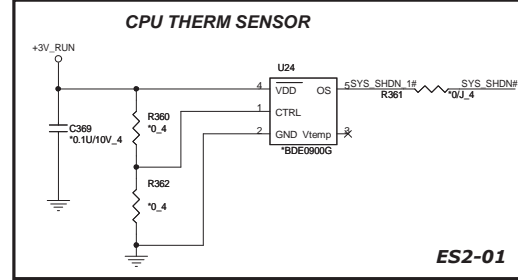
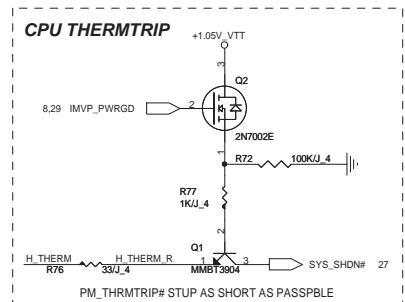
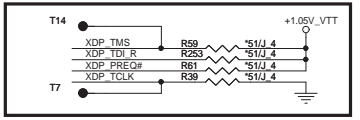
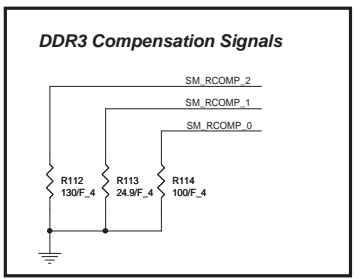
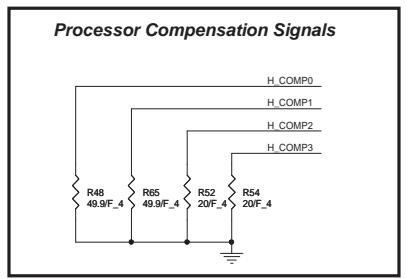
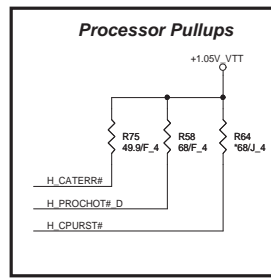
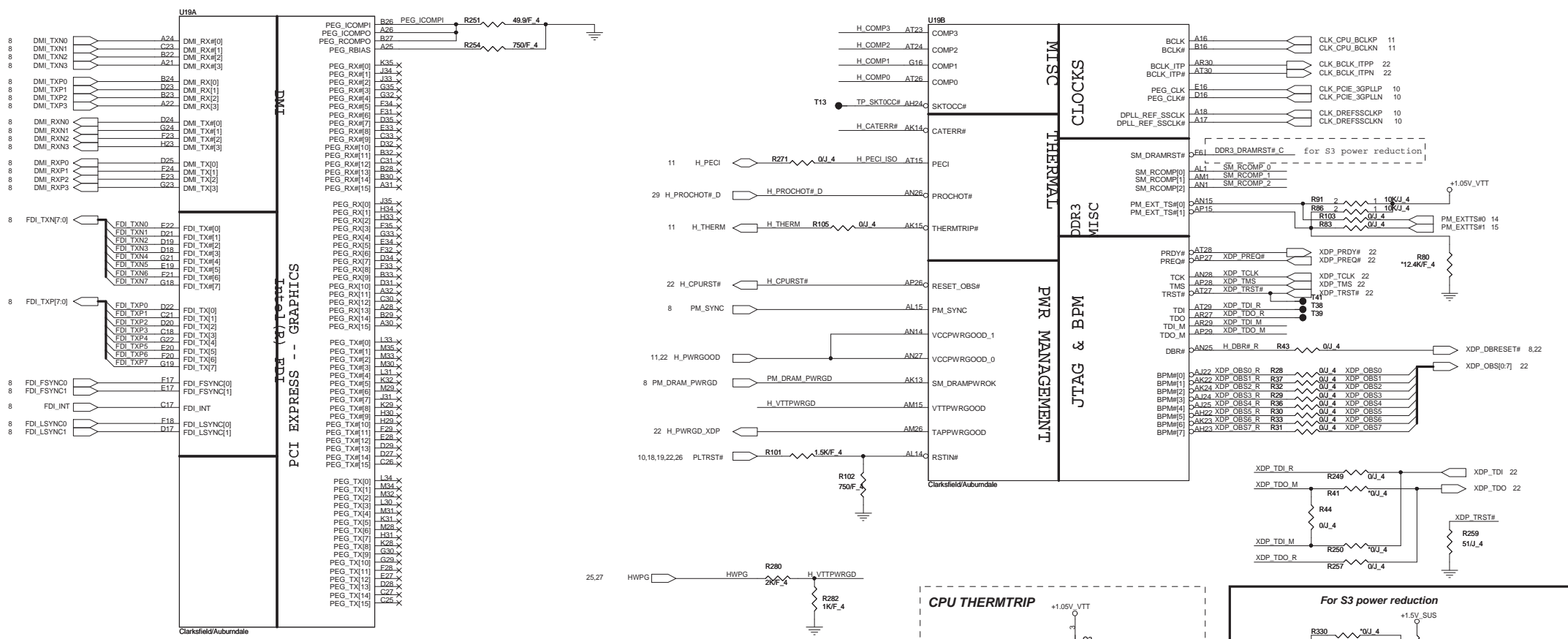


PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

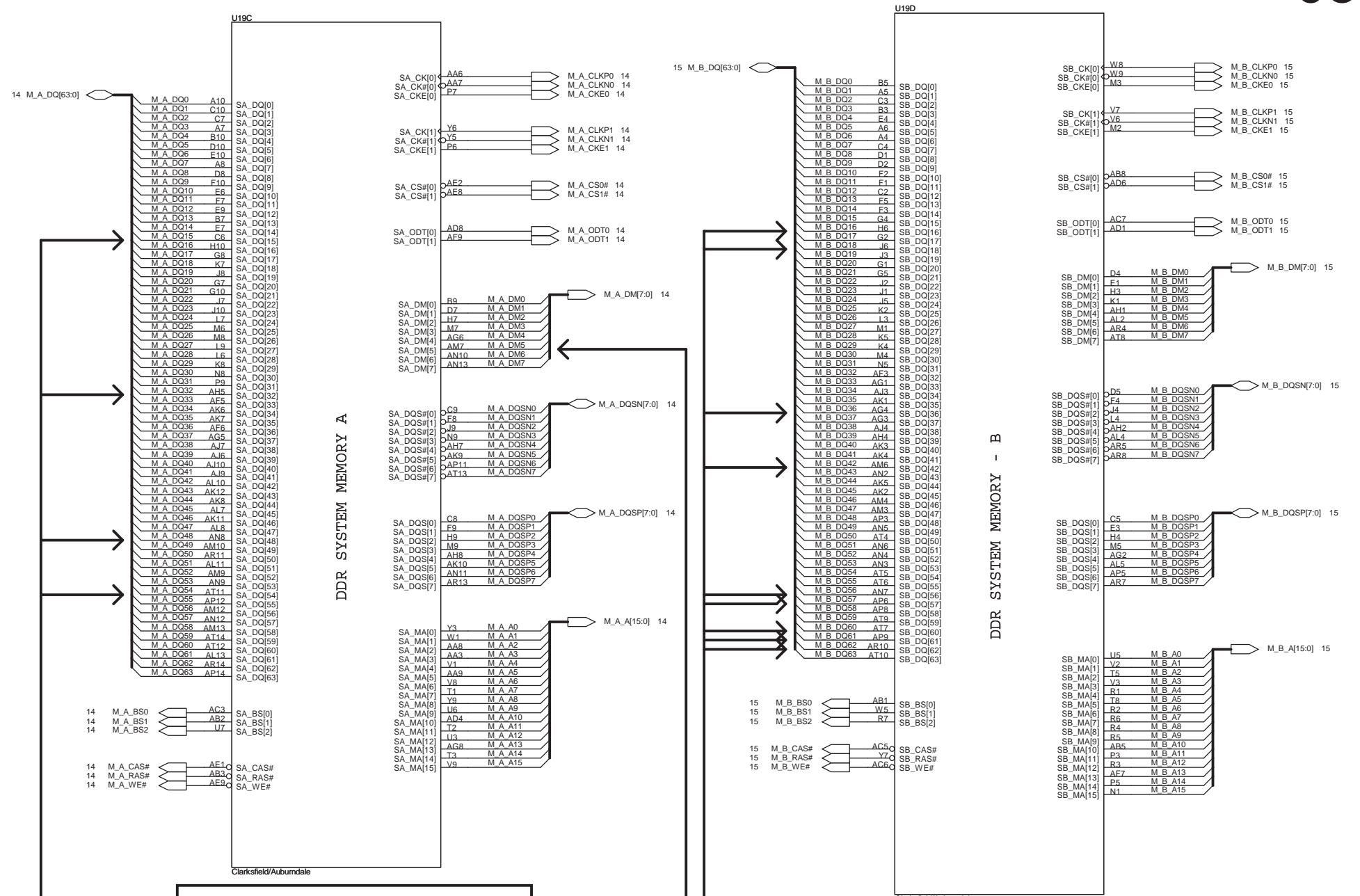
Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev 1A
Clock Generator		
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Quanta Computer Inc.
PROJECT : FB2
ARRANDALE 1/4
 Date: Monday, December 21, 2009 4 of 38
 Sheet 4 of 38

ES2-01



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

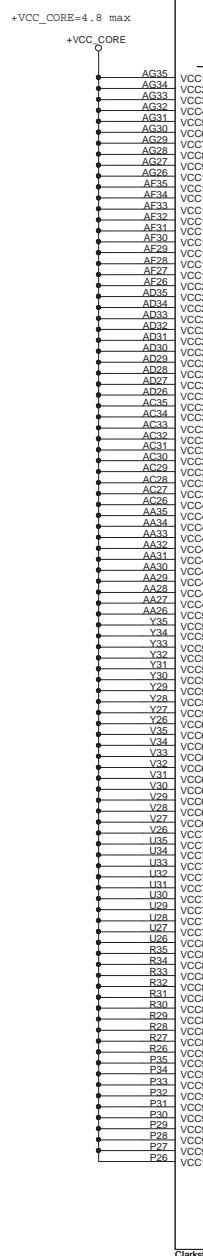
Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

Quanta Computer Inc.
PROJECT : FB2

Size Document Number
ARRANDALE 2/4 Rev 1A

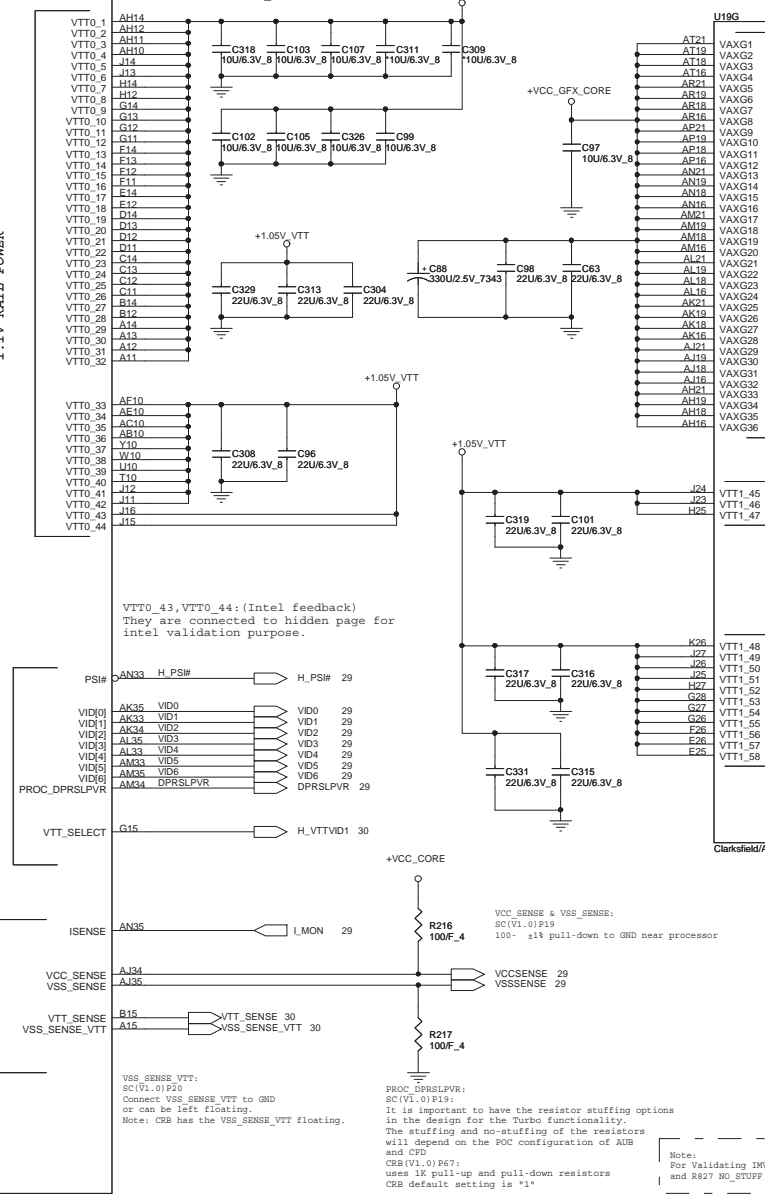
Date: Monday, December 21, 2009 Sheet 5 of 38

CPU Core Power



POWER

1.1V RAIL POWER



U19F

1.05V_VTT=1.8 max

1.05V_VTT

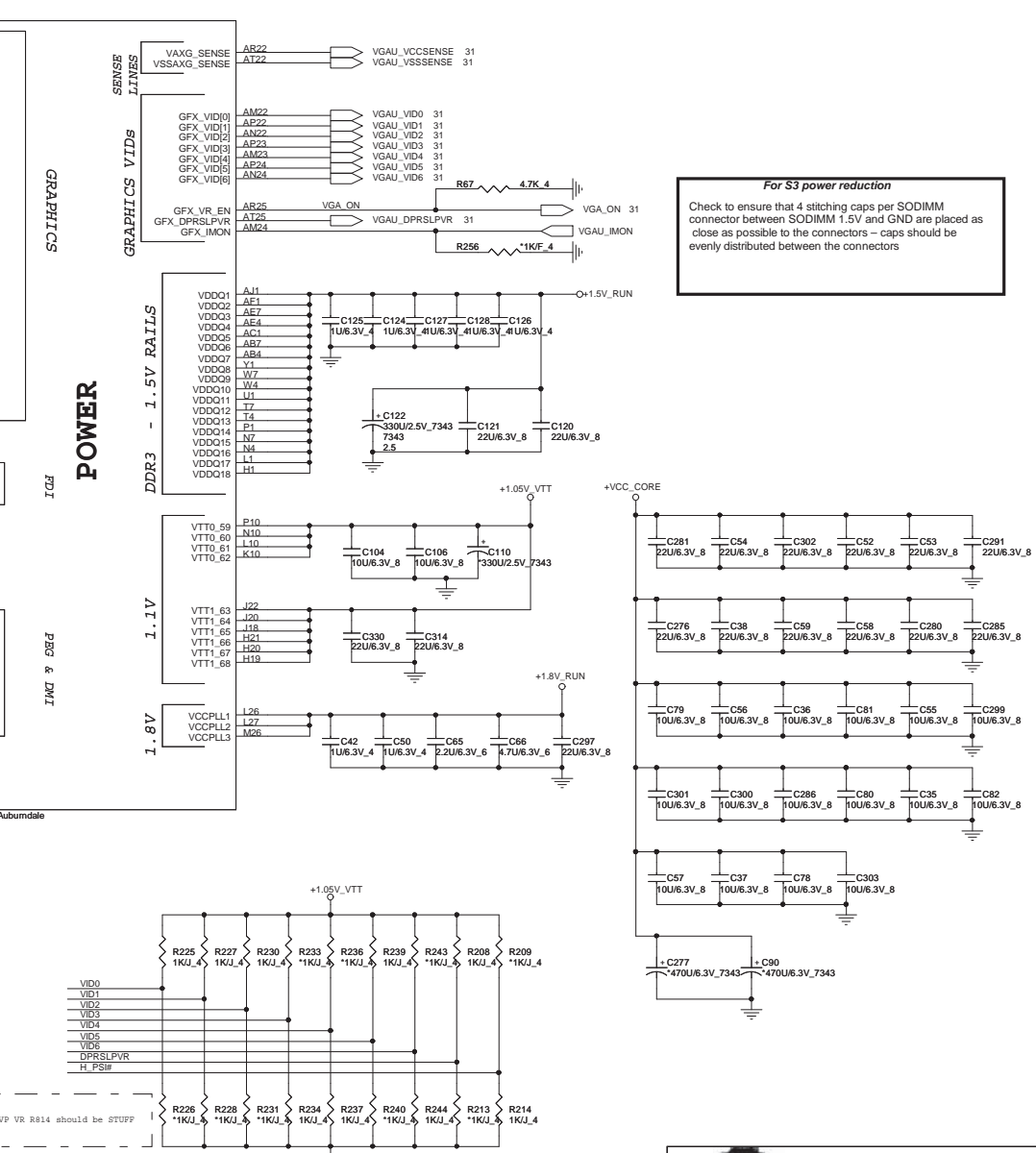
1.05V_VTT

U19G

GRAPHICS

DDR3 - 1.5V RAILS

1.1V

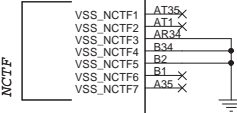
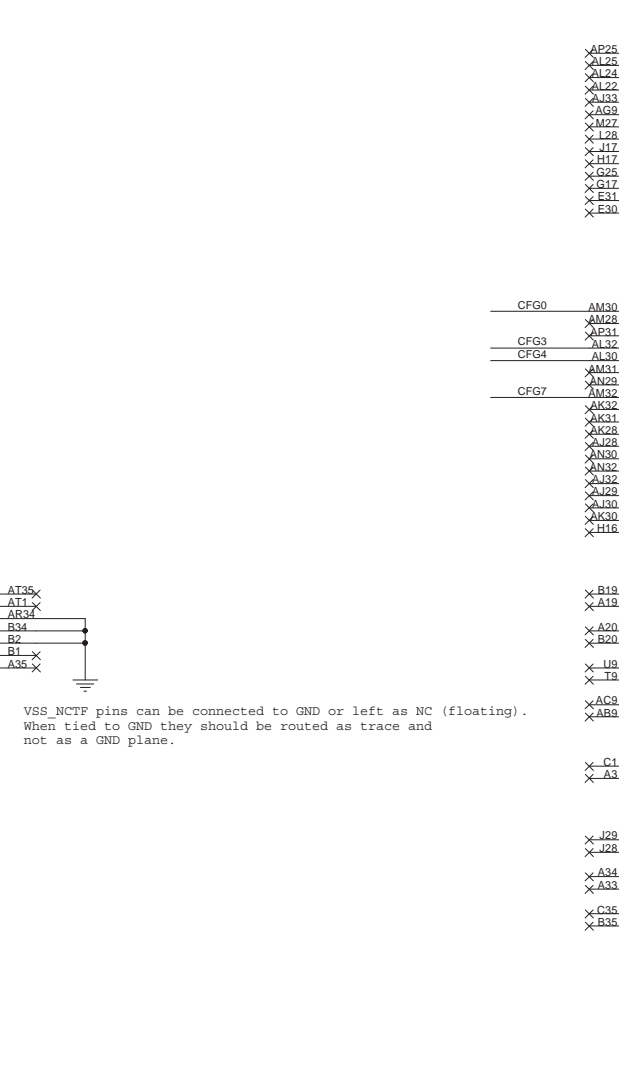
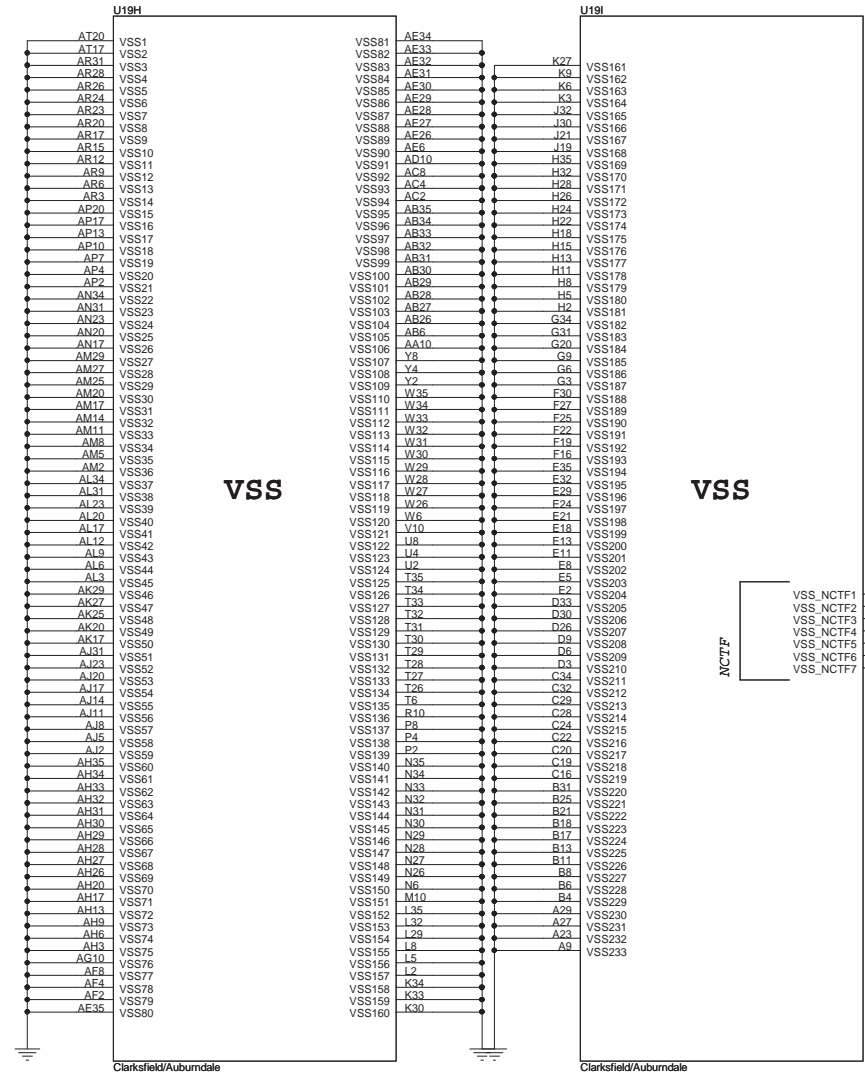


For S3 power reduction
Check to ensure that 4 stitching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors - caps should be evenly distributed between the connectors

AUBURDALE/CLARKSFIELD PROCESSOR (POWER)

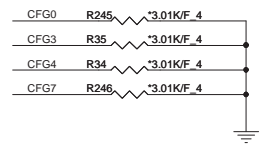
Quanta Computer Inc.
PROJECT : FH2

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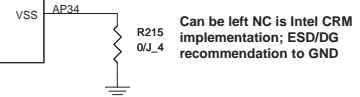


VSS_NCTF pins can be connected to GND or left as NC (floating).
When tied to GND they should be routed as trace and not as a GND plane.

The Clarksfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static lane Reversal)	Normal Operation	Lane Numbers Reversed



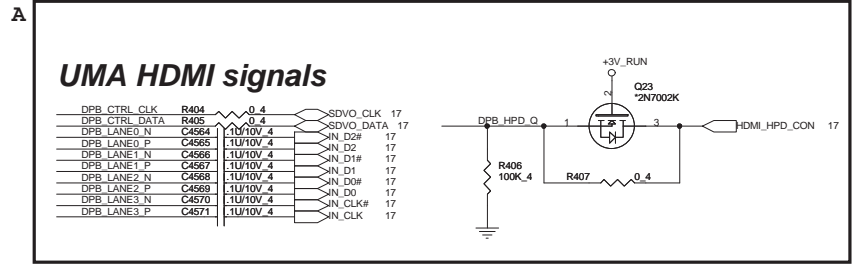
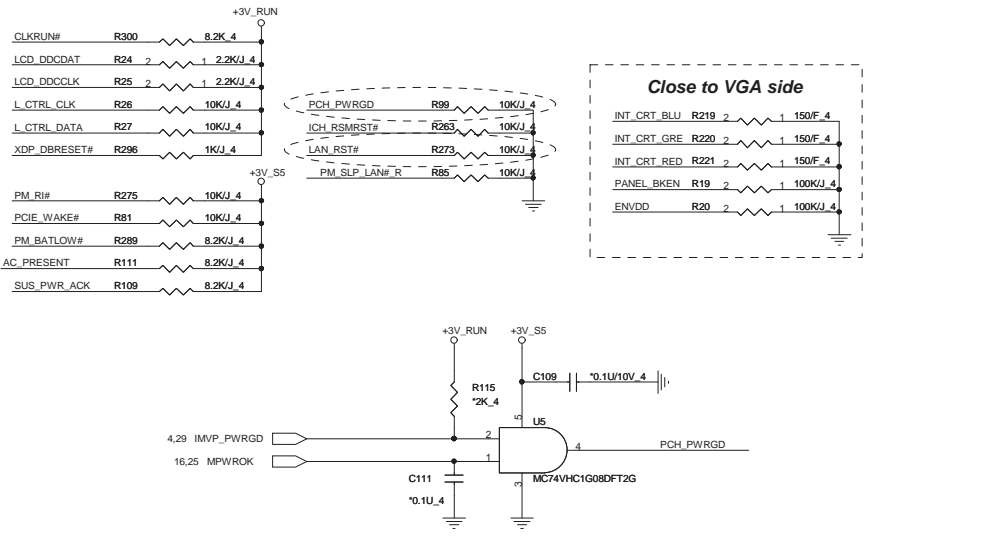
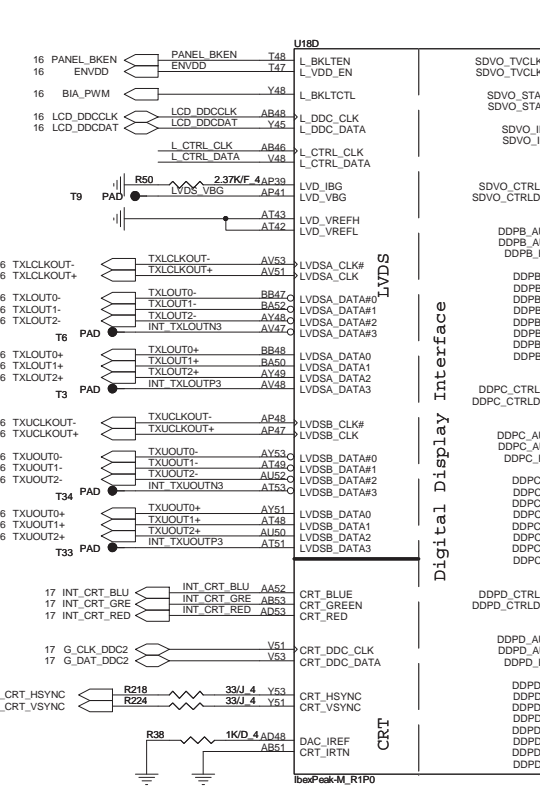
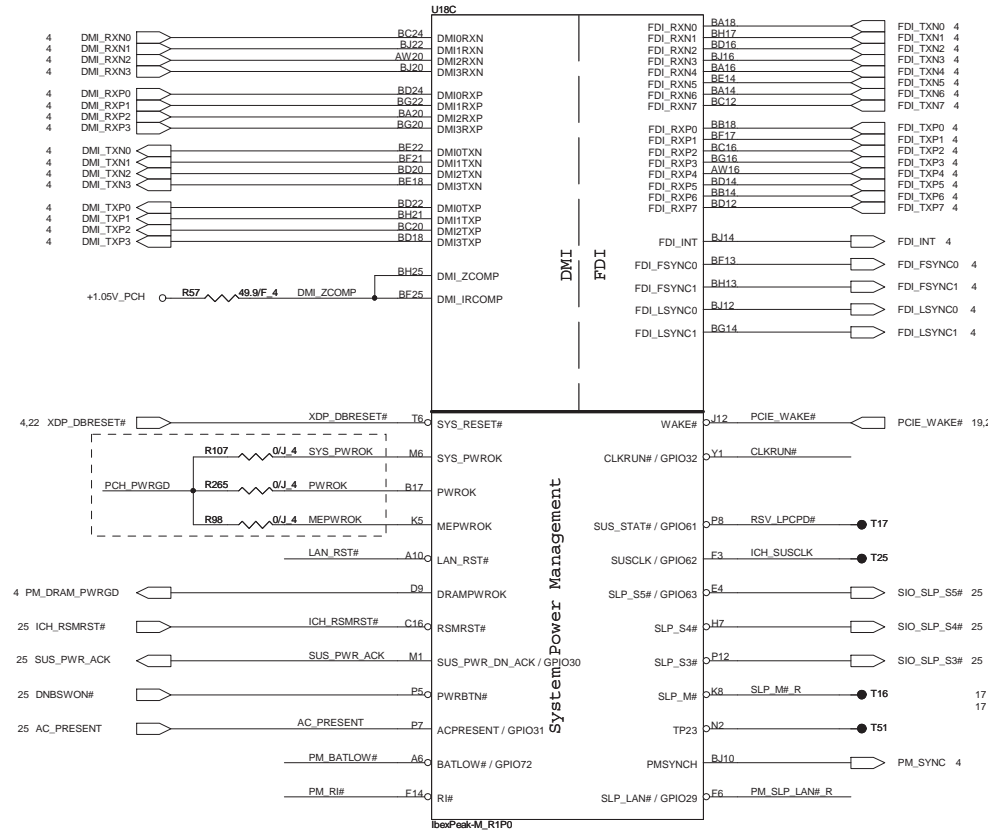
Quanta Computer Inc.
PROJECT : FH2

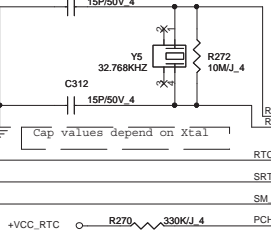
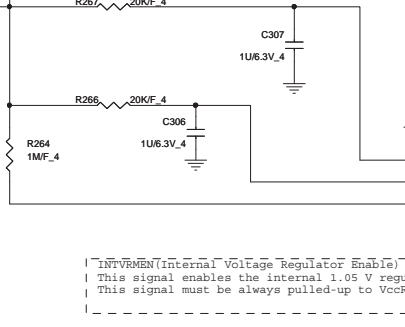
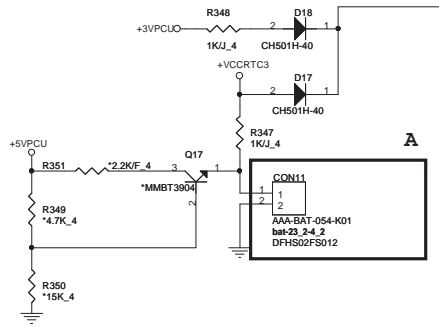
Size Document Number Rev 1A
ARRANDALE 4/4

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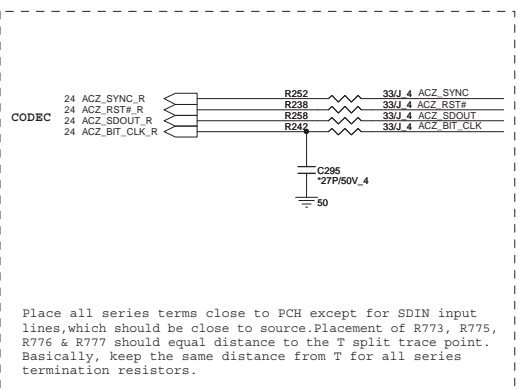
IBEX PEAK-M (DMI, FDI, GPIO)

IBEX PEAK-M (LVDS, DDI)





INTVRMEN (Internal Voltage Regulator Enable)
 This signal enables the internal 1.05 V regulators.
 This signal must be always pulled-up to VccRTC.

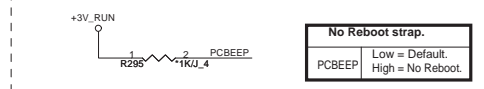


Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled
--------	----------------------------------

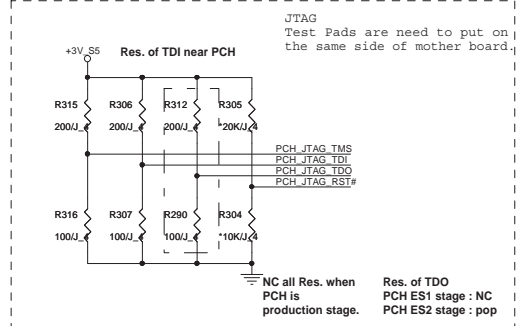
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.



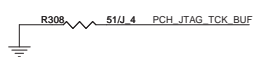
No Reboot strap.

PCBEEP Low = Default.
High = No Reboot.



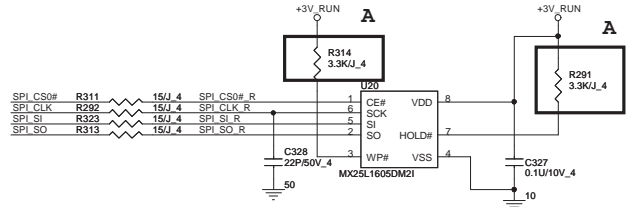
JTAG
 Test Pads are need to put on the same side of mother board.

Res. of TDO
 PCH ES1 stage : NC
 PCH ES2 stage : pop



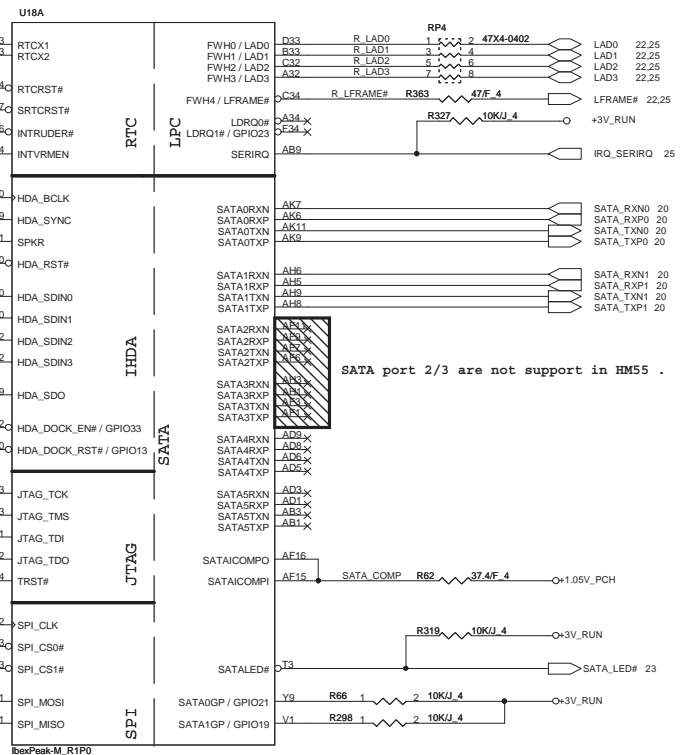
Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For PCH 32Mbit (4M Byte)



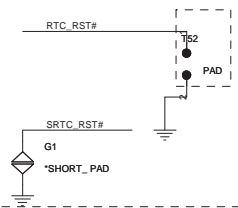
A

A



SATA port 2/3 are not support in HM55 .

RESET JUMP (Near ROOM DOOR)

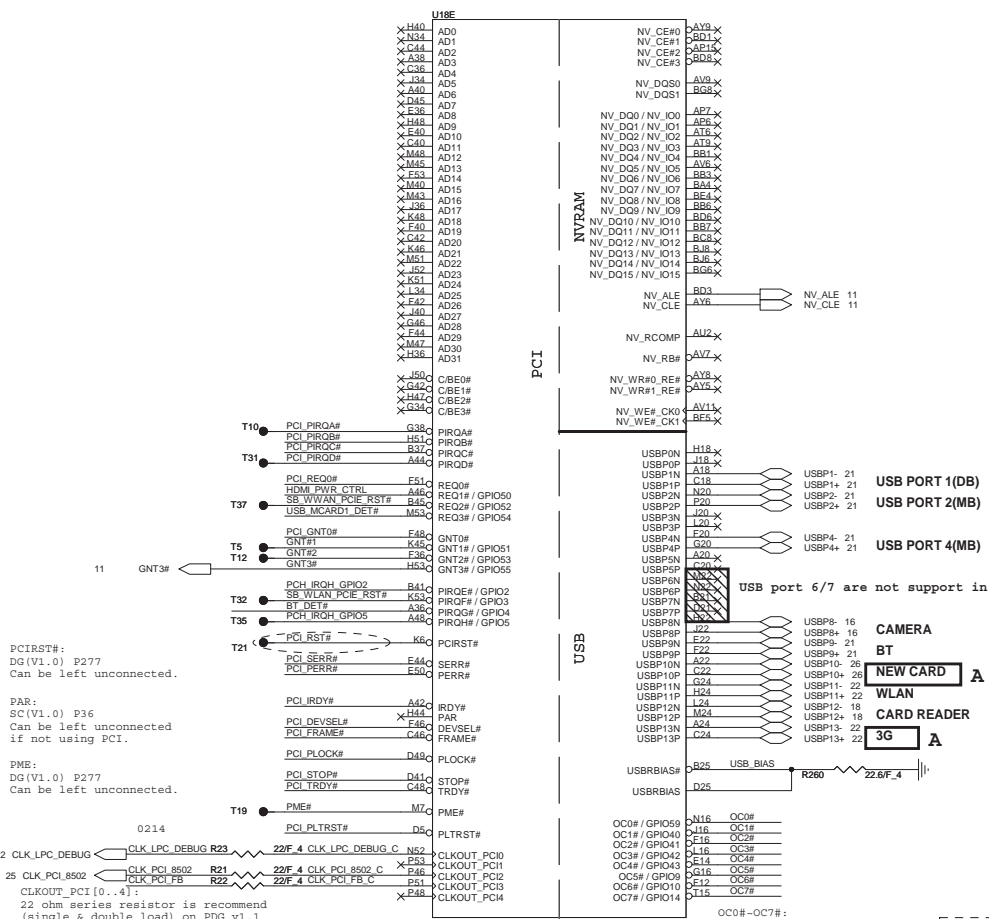


Quanta Computer Inc.
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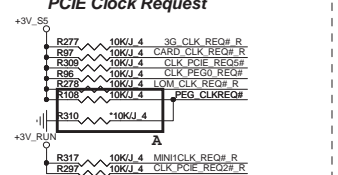
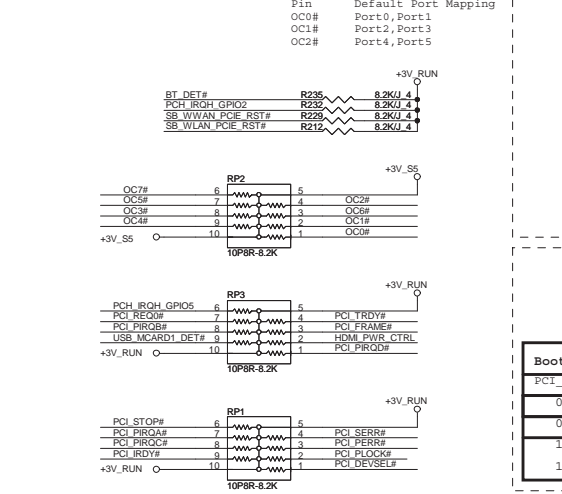
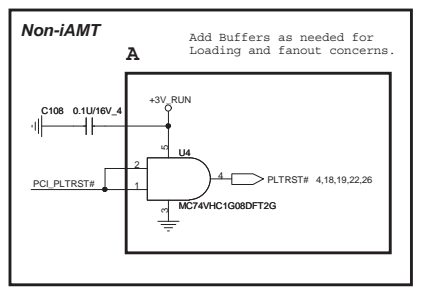
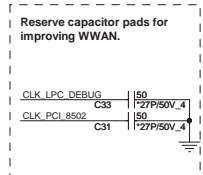
Place TX DC blocking caps close PCH.



PCIIRSTH: DG(V1.0) P277 Can be left unconnected.

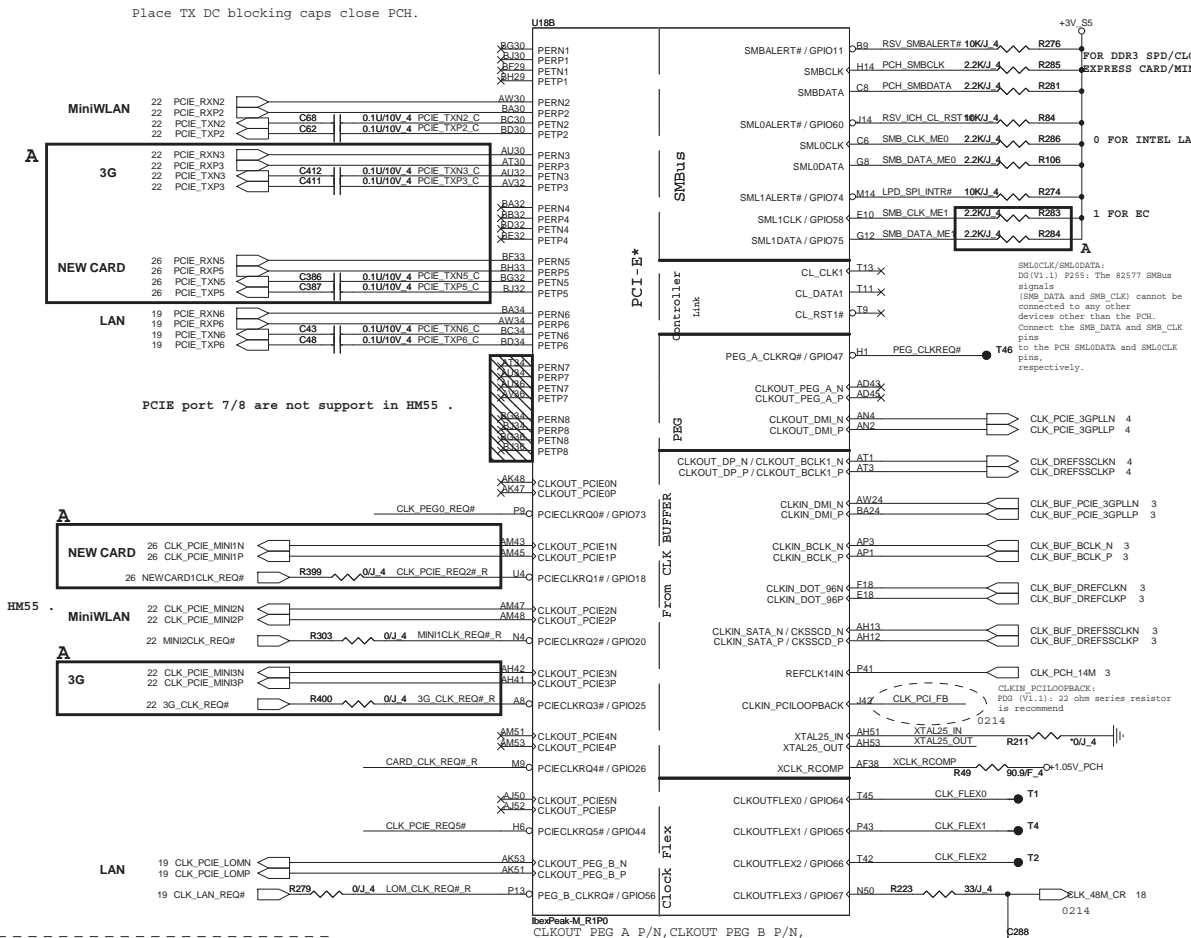
PAR: SC(V1.0) P36 Can be left unconnected if not using PCI.

PME: DG(V1.0) P277 Can be left unconnected.



Boot BIOS Strap

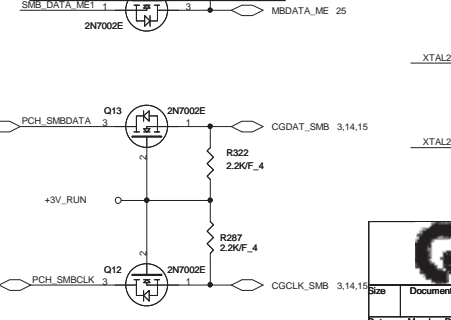
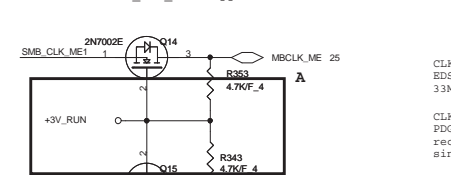
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI



PCIe port 7/8 are not support in HM55 .

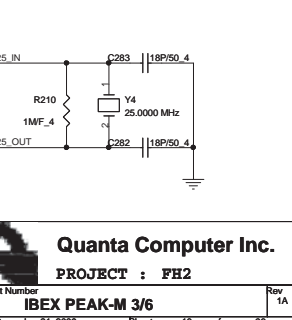
USB port 6/7 are not support in HM55 .

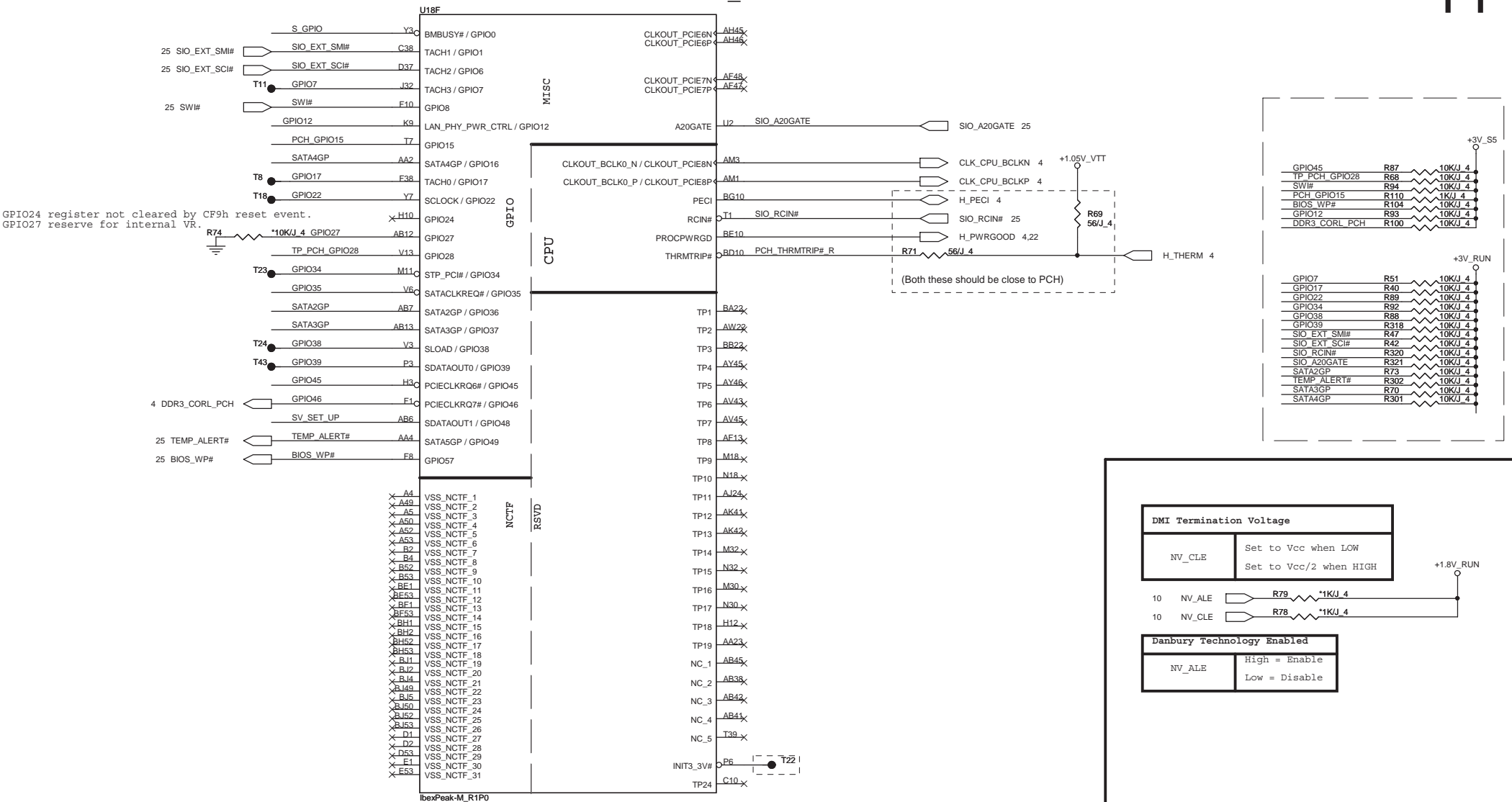
ibexPeak-M_R1P0
 CLKOUT_PEG_A_P/N, CLKOUT_PEG_B_P/N, CLKOUT_DMI_P/N, support GEN-1 and GEN-2



CLKOUTFLEX3: RDS(V1.0) :support 48MHz 33MHz and 14.31818MHz.

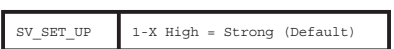
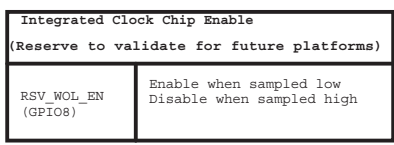
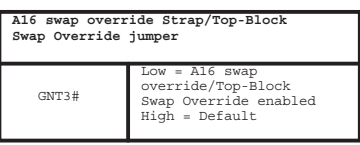
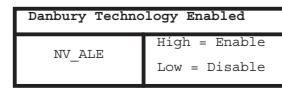
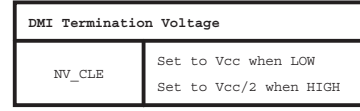
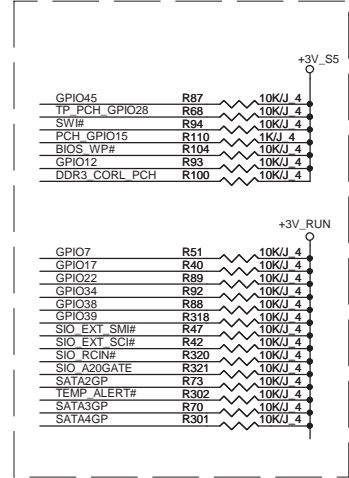
CLKOUTFLEX[0..3]: PD2 v1.1: 22 ohm series resistor is recommend (PCI & non PCI routing, single & double load)





GPIO24 register not cleared by CF9h reset event.
GPIO27 reserve for internal VR.

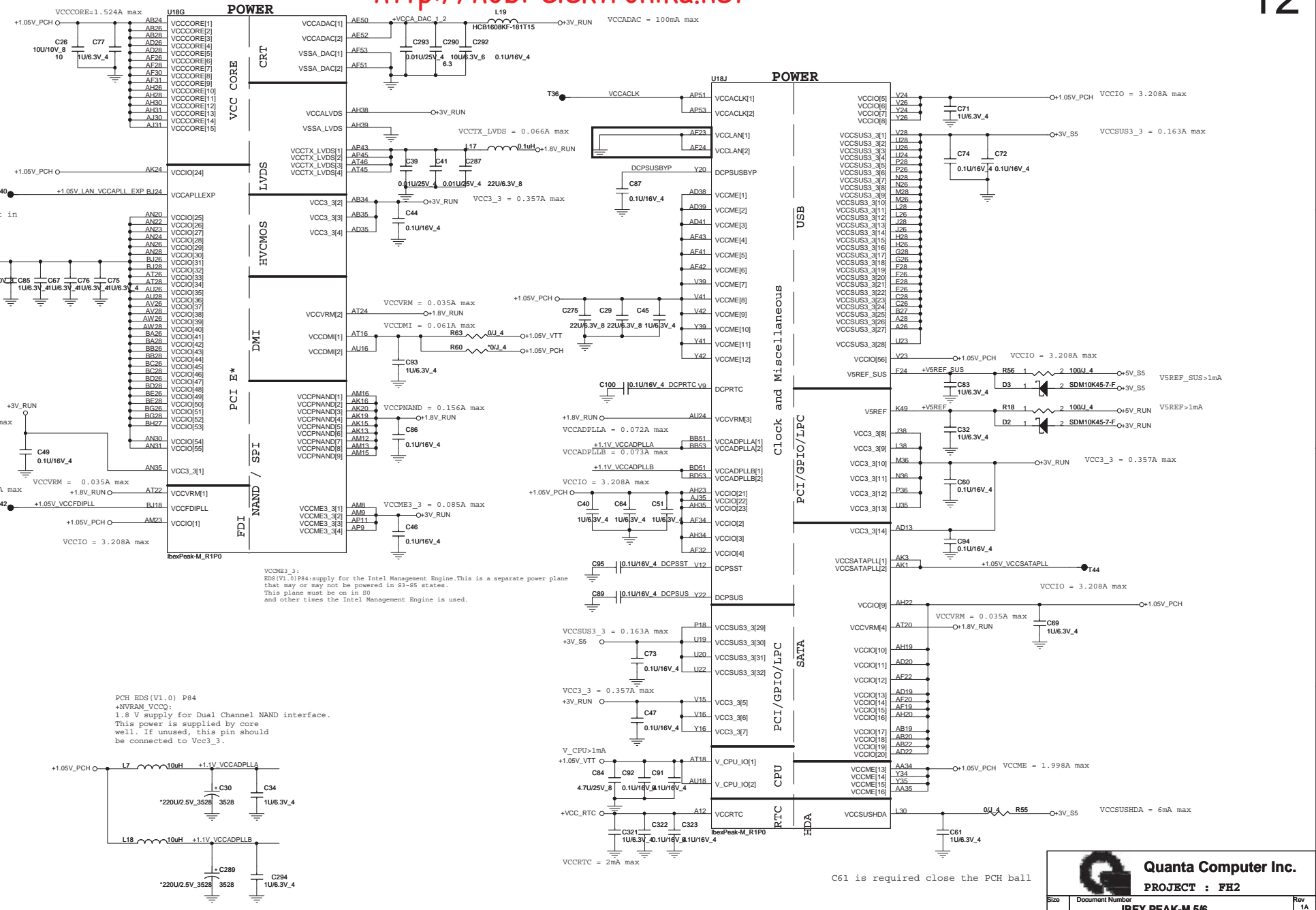
(Both these should be close to PCH)



BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3.3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

IBEX PEAK-M (POWER)



PCH EDS (V1.0) P84
 +NVRAM_VCCQ:
 1.8 V supply for Dual Channel NAND interface.
 This power is supplied by core
 well. If unused, this pin should
 be connected to Vcc3_3.

VCCME3_3:
 ES0(V1.0)P84 supply for the Intel Management Engine. This is a separate power plane
 that may or may not be powered in S3-S5 states.
 This plane must be on in S0
 and other times the Intel Management Engine is used.

C61 is required close the PCH ball

Quanta Computer Inc.
 PROJECT : FH2

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IBEX PEAK-M (GND)

U18H


AB16	VSS[0]		
AA19	VSS[1]	VSS[80]	AK30
AA20	VSS[2]	VSS[81]	AK31
AA22	VSS[3]	VSS[82]	AK32
AM19	VSS[4]	VSS[83]	AK34
AA24	VSS[5]	VSS[84]	AK35
AA26	VSS[6]	VSS[85]	AK38
AA28	VSS[7]	VSS[86]	AK43
AA30	VSS[8]	VSS[87]	AK46
AA31	VSS[9]	VSS[88]	AK49
AA32	VSS[10]	VSS[89]	AK5
AB11	VSS[11]	VSS[90]	AK8
AB15	VSS[12]	VSS[91]	AL2
AB23	VSS[13]	VSS[92]	AL52
AB30	VSS[14]	VSS[93]	AM11
AB31	VSS[15]	VSS[94]	BB44
AB32	VSS[16]	VSS[95]	AD24
AB39	VSS[17]	VSS[96]	AM20
AB43	VSS[18]	VSS[97]	AM22
AB47	VSS[19]	VSS[98]	AM24
AB5	VSS[20]	VSS[99]	AM26
AB8	VSS[21]	VSS[100]	AM28
AC2	VSS[22]	VSS[101]	BE42
AC52	VSS[23]	VSS[102]	AM30
AD11	VSS[24]	VSS[103]	AM31
AD12	VSS[25]	VSS[104]	AM32
AD16	VSS[26]	VSS[105]	AM34
AD23	VSS[27]	VSS[106]	AM35
AD30	VSS[28]	VSS[107]	AM38
AD31	VSS[29]	VSS[108]	AM39
AD32	VSS[30]	VSS[109]	AM42
AD34	VSS[31]	VSS[110]	AM44
AU22	VSS[32]	VSS[111]	AM46
AD42	VSS[33]	VSS[112]	AV22
AD46	VSS[34]	VSS[113]	AM49
AD49	VSS[35]	VSS[114]	AM7
AE2	VSS[36]	VSS[115]	AA50
AE7	VSS[37]	VSS[116]	BB10
AE4	VSS[38]	VSS[117]	AN32
AF12	VSS[39]	VSS[118]	AN50
Y13	VSS[40]	VSS[119]	AN52
AH49	VSS[41]	VSS[120]	AP12
AU4	VSS[42]	VSS[121]	AP42
AF35	VSS[43]	VSS[122]	AP46
AP13	VSS[44]	VSS[123]	AP49
AP34	VSS[45]	VSS[124]	AP5
AF45	VSS[46]	VSS[125]	AP8
AF46	VSS[47]	VSS[126]	AR2
AF49	VSS[48]	VSS[127]	AR52
AF5	VSS[49]	VSS[128]	AT11
AG2	VSS[50]	VSS[129]	AT12
AG52	VSS[51]	VSS[130]	AT32
AH11	VSS[52]	VSS[131]	AT36
AH15	VSS[53]	VSS[132]	AT41
AH16	VSS[54]	VSS[133]	AT47
AH24	VSS[55]	VSS[134]	AT7
AH32	VSS[56]	VSS[135]	AV12
AV18	VSS[57]	VSS[136]	AV16
AH43	VSS[58]	VSS[137]	AV20
AH47	VSS[59]	VSS[138]	AV24
AH7	VSS[60]	VSS[139]	AV30
AJ19	VSS[61]	VSS[140]	AV34
AJ2	VSS[62]	VSS[141]	AV38
AJ20	VSS[63]	VSS[142]	AV42
AJ22	VSS[64]	VSS[143]	AV46
AJ23	VSS[65]	VSS[144]	AV49
AJ26	VSS[66]	VSS[145]	AV5
AJ28	VSS[67]	VSS[146]	AV9
AJ32	VSS[68]	VSS[147]	AW14
AJ34	VSS[69]	VSS[148]	AW18
AT5	VSS[70]	VSS[149]	AW2
AJ4	VSS[71]	VSS[150]	BE3
AK12	VSS[72]	VSS[151]	AW32
AM41	VSS[73]	VSS[152]	AW36
AN19	VSS[74]	VSS[153]	AW40
AK26	VSS[75]	VSS[154]	AW52
AK22	VSS[76]	VSS[155]	AY11
AK23	VSS[77]	VSS[156]	AY43
AK28	VSS[78]	VSS[157]	AY47
	VSS[79]	VSS[158]	

IbexPeak-M_R1P0

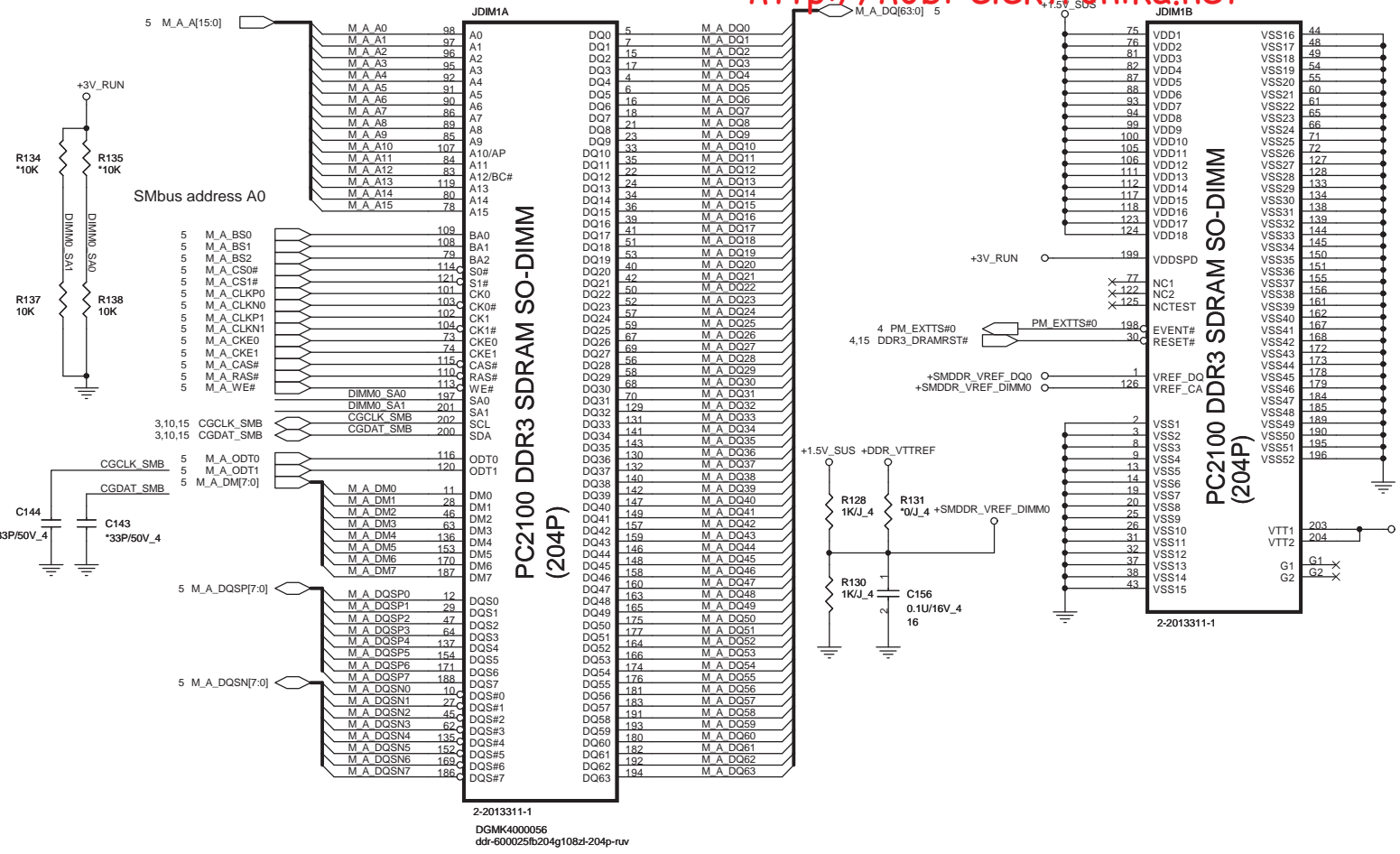
U18I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L22
B7	VSS[169]	VSS[269]	L32
BG12	VSS[170]	VSS[270]	L36
BB12	VSS[171]	VSS[271]	L40
BB16	VSS[172]	VSS[272]	L52
BB20	VSS[173]	VSS[273]	M12
BB24	VSS[174]	VSS[274]	M16
BB30	VSS[175]	VSS[275]	M20
BB34	VSS[176]	VSS[276]	M34
BB38	VSS[177]	VSS[277]	M38
BB42	VSS[178]	VSS[278]	M42
BB49	VSS[179]	VSS[279]	M46
BB5	VSS[180]	VSS[280]	M49
BC10	VSS[181]	VSS[281]	M5
BC14	VSS[182]	VSS[282]	M8
BC18	VSS[183]	VSS[283]	P11
BC2	VSS[184]	VSS[284]	AD15
BC22	VSS[185]	VSS[285]	P22
BC32	VSS[186]	VSS[286]	P30
BC40	VSS[187]	VSS[287]	P32
BC44	VSS[188]	VSS[288]	P34
BC44	VSS[189]	VSS[289]	P42
BC52	VSS[190]	VSS[290]	P45
BH9	VSS[191]	VSS[291]	P47
BD48	VSS[192]	VSS[292]	R2
BD49	VSS[193]	VSS[293]	R52
BD5	VSS[194]	VSS[294]	T12
BE12	VSS[195]	VSS[295]	T41
BE16	VSS[196]	VSS[296]	T46
BE20	VSS[197]	VSS[297]	T49
BE24	VSS[198]	VSS[298]	T5
BE30	VSS[199]	VSS[299]	T8
BE34	VSS[200]	VSS[300]	U30
BE38	VSS[201]	VSS[301]	U32
BE42	VSS[202]	VSS[302]	U34
BE46	VSS[203]	VSS[303]	P38
BE48	VSS[204]	VSS[304]	V11
BE50	VSS[205]	VSS[305]	P16
BE6	VSS[206]	VSS[306]	V19
BE8	VSS[207]	VSS[307]	V20
BF3	VSS[208]	VSS[308]	V22
BF49	VSS[209]	VSS[309]	V30
BF51	VSS[210]	VSS[310]	V31
AG50	VSS[211]	VSS[311]	V32
BG18	VSS[212]	VSS[312]	V34
BG24	VSS[213]	VSS[313]	V35
BG4	VSS[214]	VSS[314]	V38
BG50	VSS[215]	VSS[315]	V43
BH11	VSS[216]	VSS[316]	V45
BH15	VSS[217]	VSS[317]	V46
BH19	VSS[218]	VSS[318]	V47
BH23	VSS[219]	VSS[319]	V49
BH31	VSS[220]	VSS[320]	V5
BH35	VSS[221]	VSS[321]	V7
BH39	VSS[222]	VSS[322]	V8
BH43	VSS[223]	VSS[323]	W2
BH47	VSS[224]	VSS[324]	W52
BH7	VSS[225]	VSS[325]	Y11
C12	VSS[226]	VSS[326]	Y12
C50	VSS[227]	VSS[327]	Y15
D51	VSS[228]	VSS[328]	Y19
E12	VSS[229]	VSS[329]	Y23
E16	VSS[230]	VSS[330]	Y28
E20	VSS[231]	VSS[331]	Y30
E24	VSS[232]	VSS[332]	Y32
E30	VSS[233]	VSS[333]	Y38
E34	VSS[234]	VSS[334]	Y43
E38	VSS[235]	VSS[335]	Y46
E42	VSS[236]	VSS[336]	P49
E46	VSS[237]	VSS[337]	Y5
E48	VSS[238]	VSS[338]	Y6
E6	VSS[239]	VSS[339]	Y8
F8	VSS[240]	VSS[340]	P24
F49	VSS[241]	VSS[341]	T43
F5	VSS[242]	VSS[342]	AD51
G10	VSS[243]	VSS[343]	ATR
G14	VSS[244]	VSS[344]	AD47
G18	VSS[245]	VSS[345]	Y47
G2	VSS[246]	VSS[346]	AT12
G22	VSS[247]	VSS[347]	AM6
G32	VSS[248]	VSS[348]	AT13
G36	VSS[249]	VSS[349]	AM5
G40	VSS[250]	VSS[350]	AK45
G44	VSS[251]	VSS[351]	AK39
G52	VSS[252]	VSS[352]	AV14
AF39	VSS[253]	VSS[353]	
H16	VSS[254]	VSS[354]	
H20	VSS[255]	VSS[355]	
H30	VSS[256]	VSS[356]	
H34	VSS[257]	VSS[357]	
H38	VSS[258]	VSS[358]	
H42	VSS[259]	VSS[359]	

IbexPeak-M_R1P0

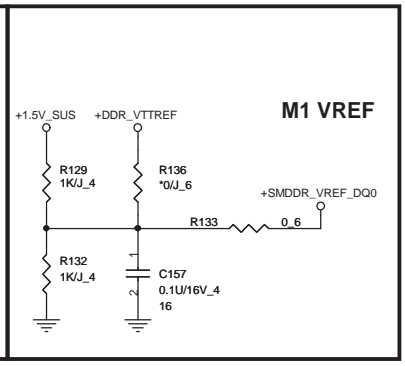
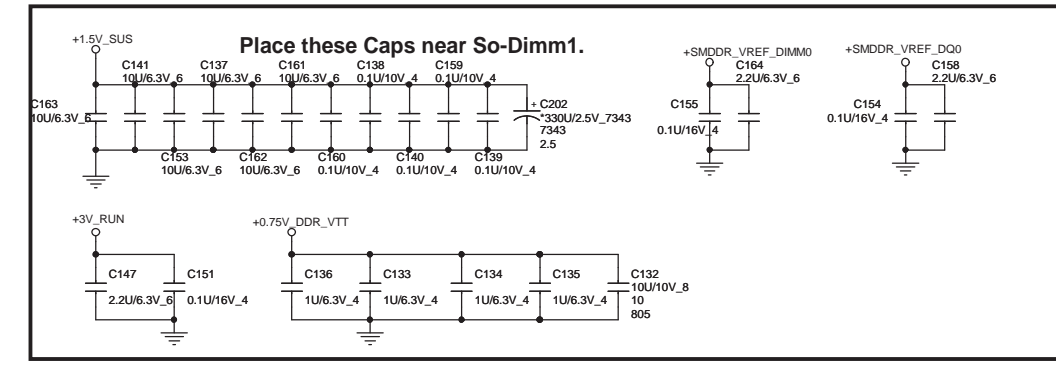
 **Quanta Computer Inc.**
PROJECT : FH2

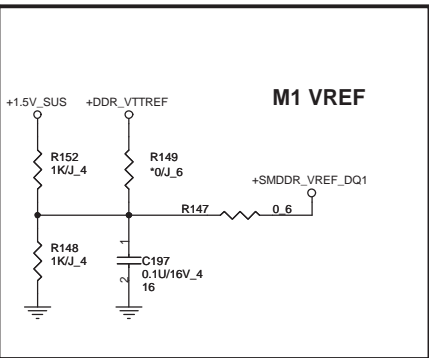
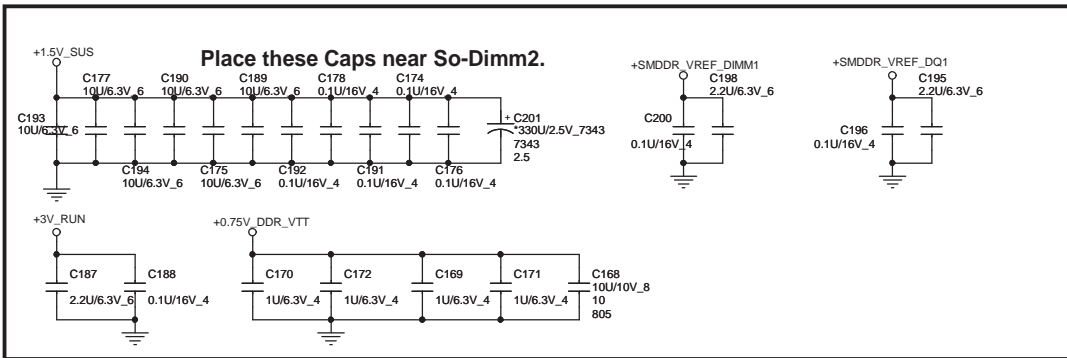
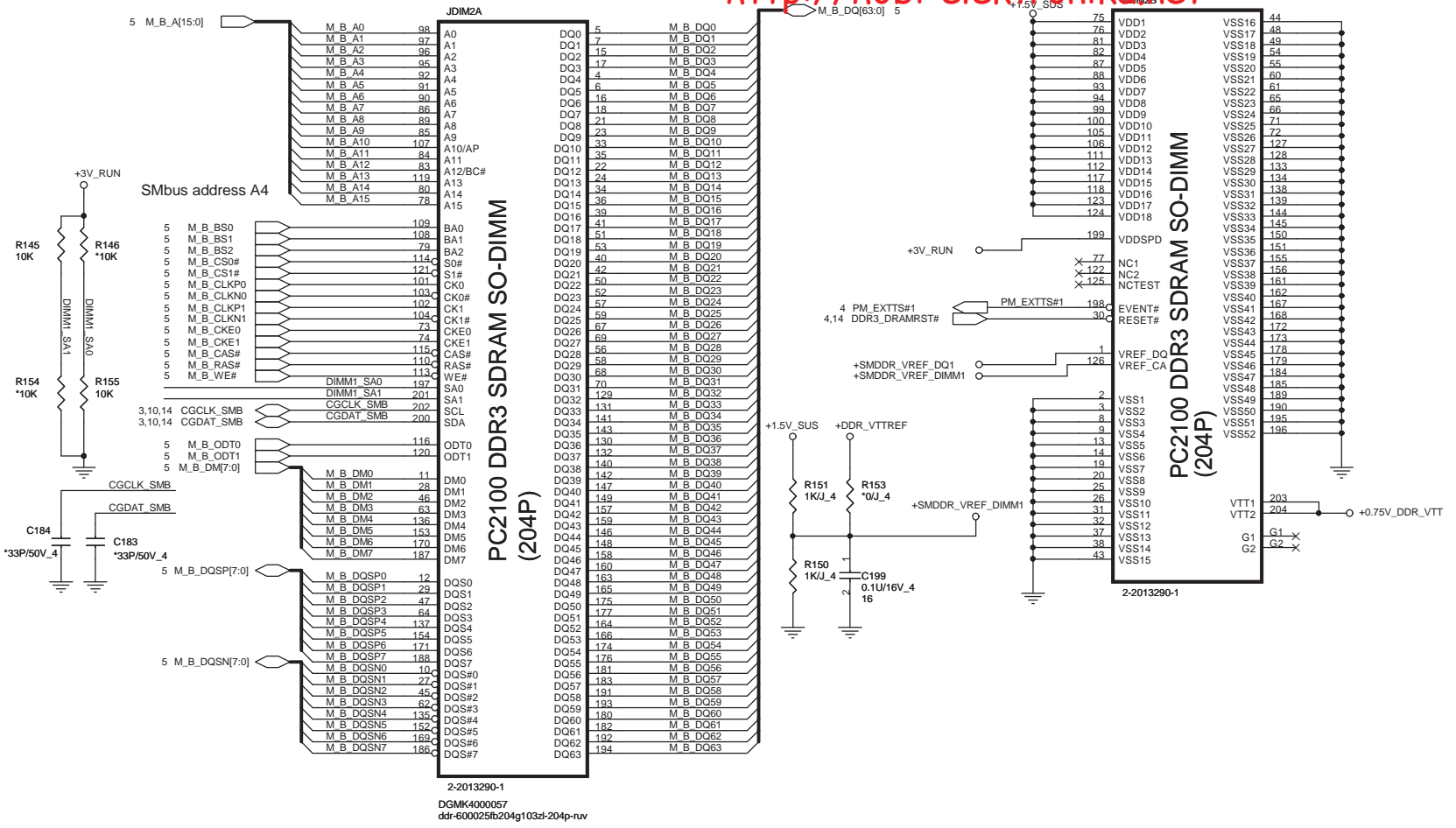
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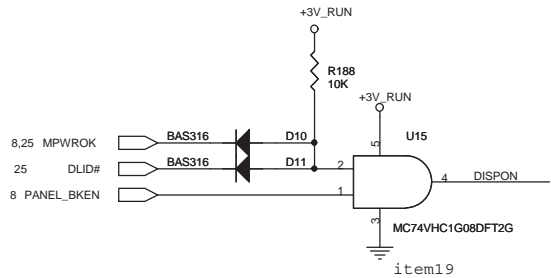
Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. For fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1: Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2: A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3: Intel investigating future processor VREF DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.

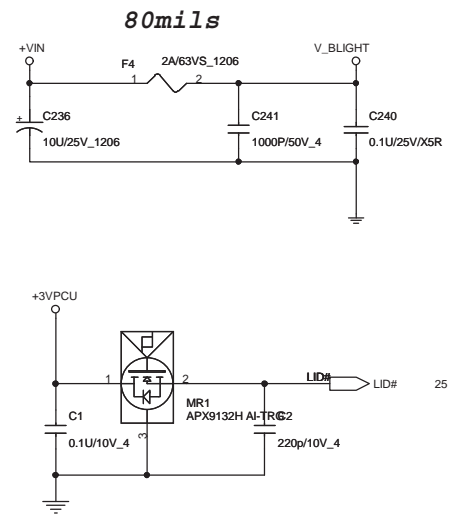




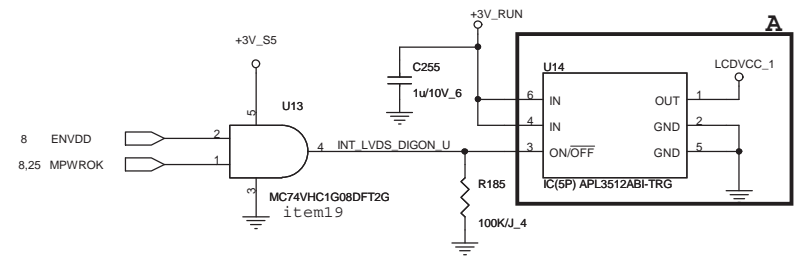
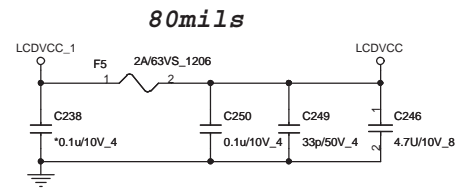
Backlight Control(LDS)



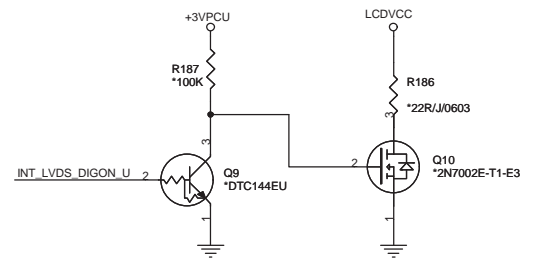
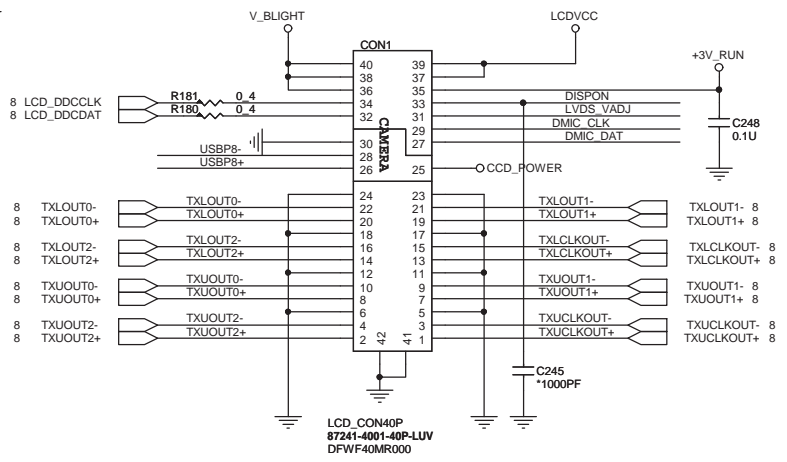
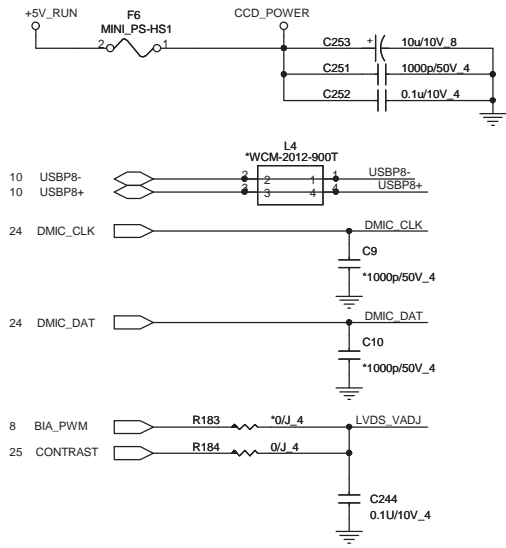
BACKLIGHT POWER



LED Panel POWER SWITCH(LVDS) 16

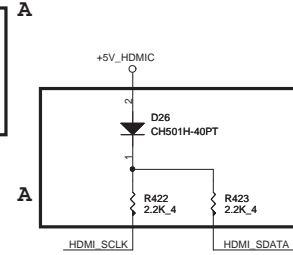
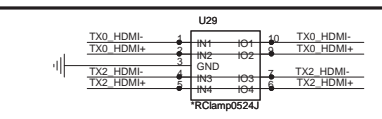
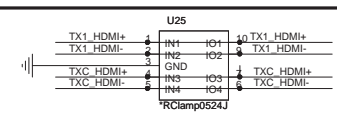
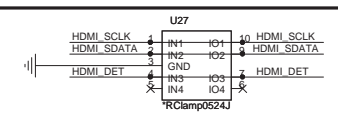
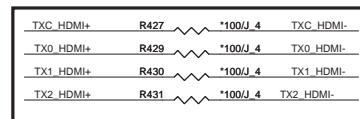
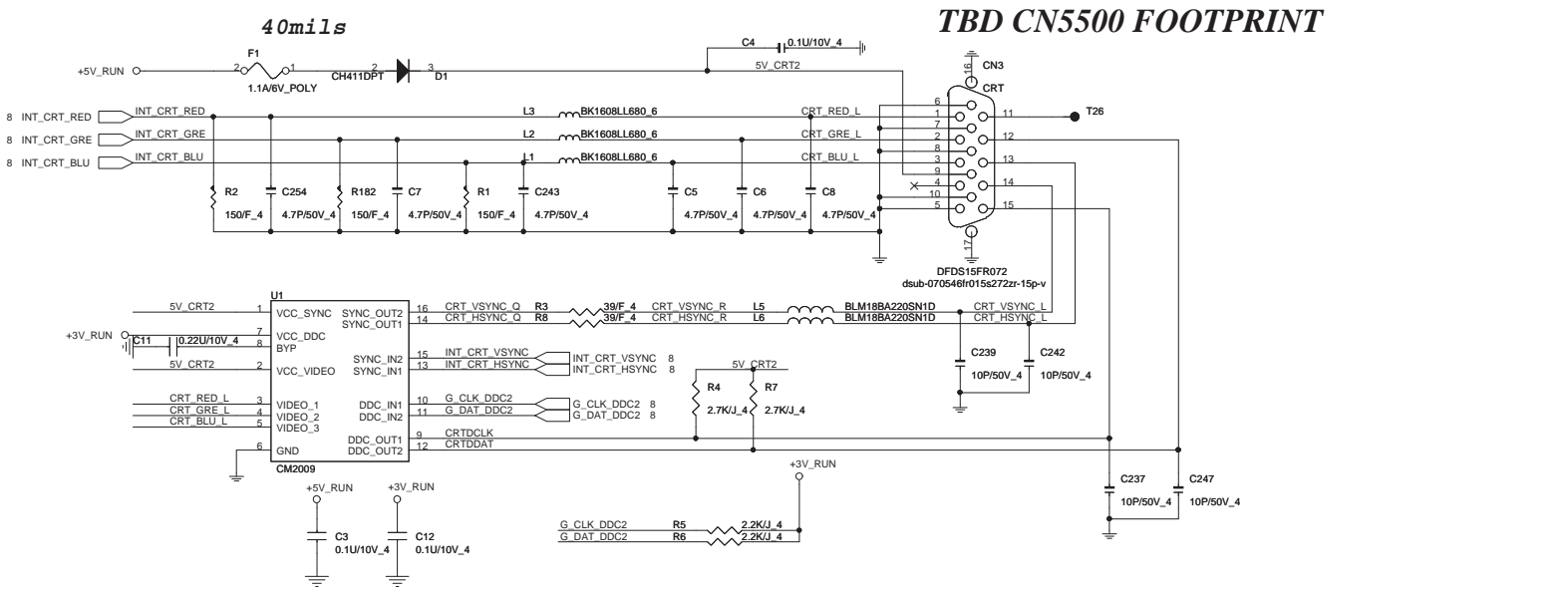


LVDS/CCD



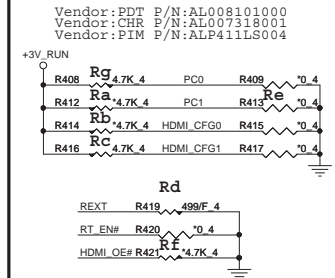
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reserve for EMI

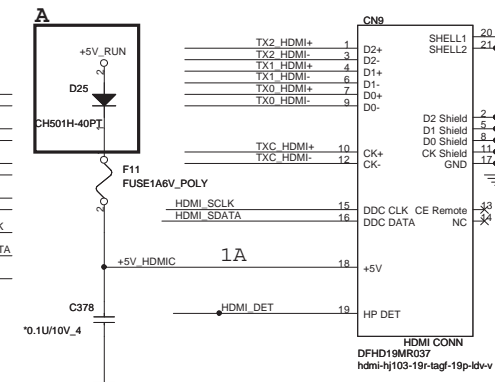
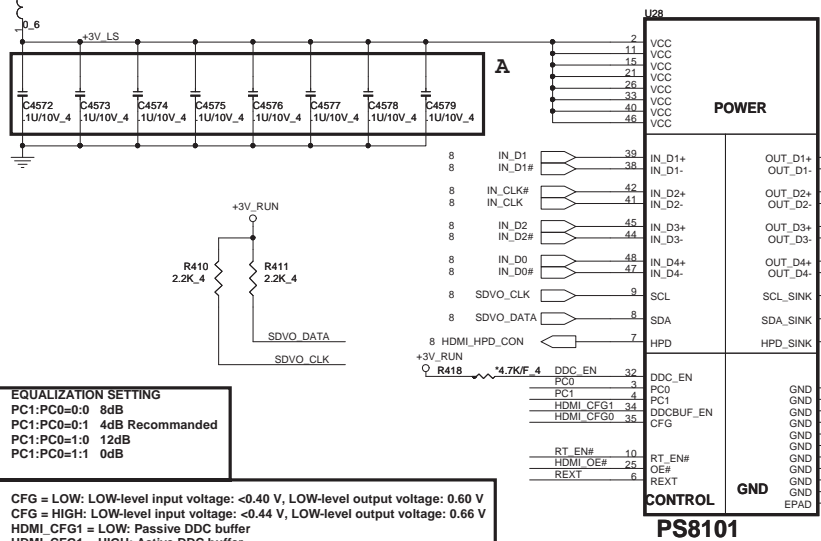
Signals		PDT	CHR	PIM
PC1	Ra	NC	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K



EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

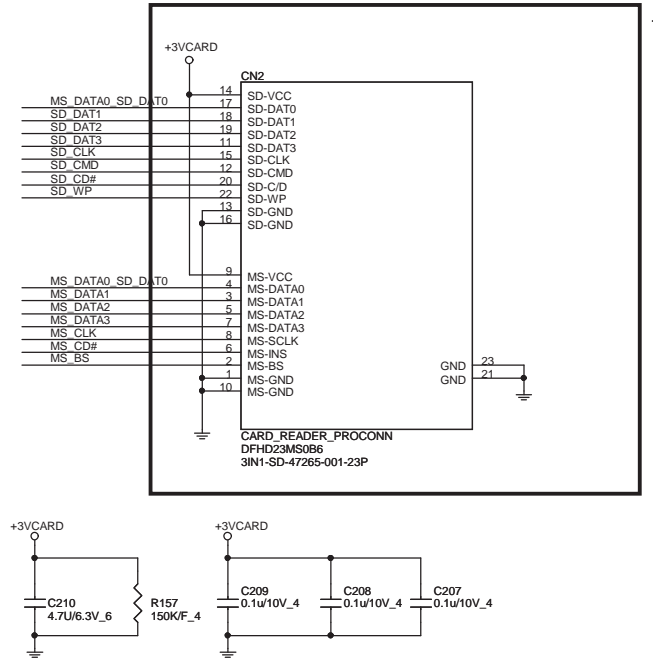
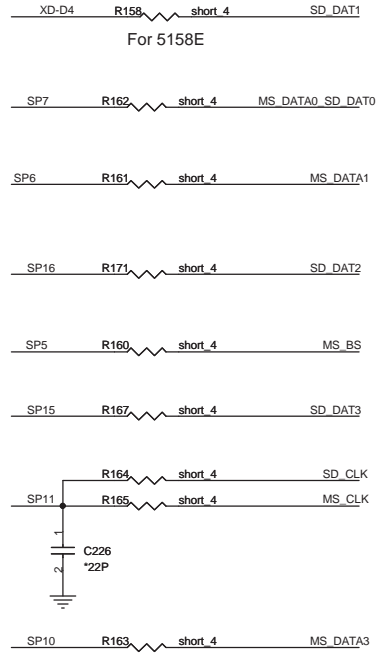
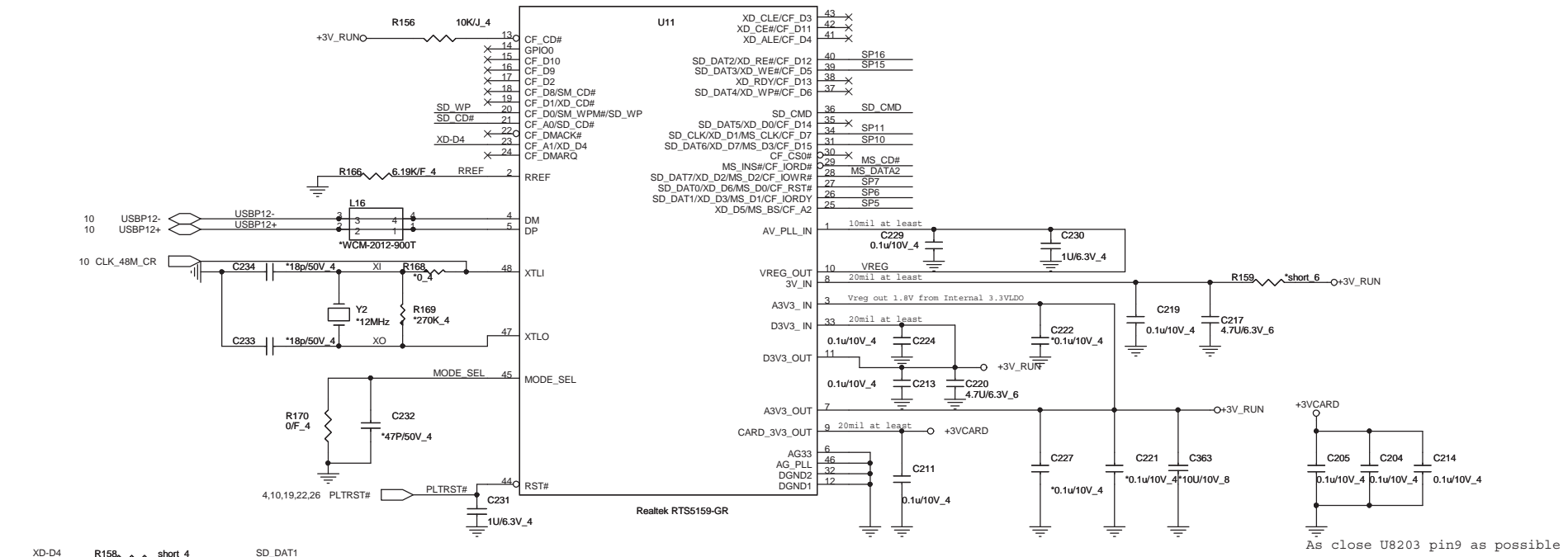
CFG = LOW: LOW-level input voltage: <0.40 V, LOW-level output voltage: 0.60 V
 CFG = HIGH: LOW-level input voltage: <0.44 V, LOW-level output voltage: 0.66 V
 HDMI_CFG1 = LOW: Passive DDC buffer
 HDMI_CFG1 = HIGH: Active DDC buffer

HDMI



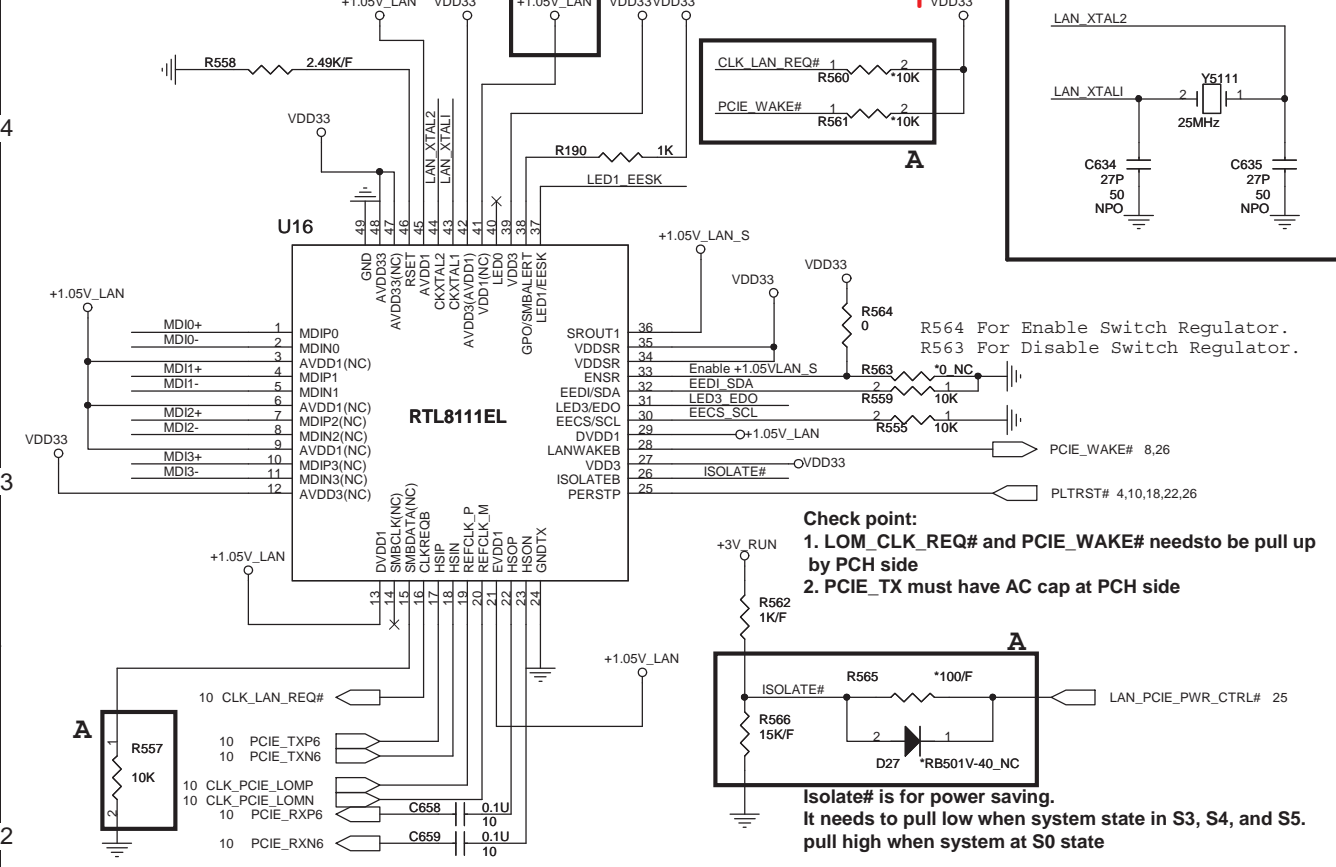
Quanta Computer Inc.
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Size	Document Number	Rev
	CRT CONN/HDMI	1A
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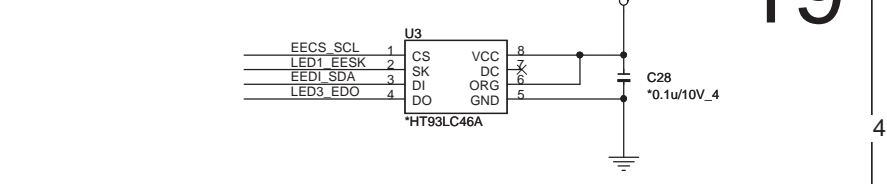


As close U8203 pin9 as possible

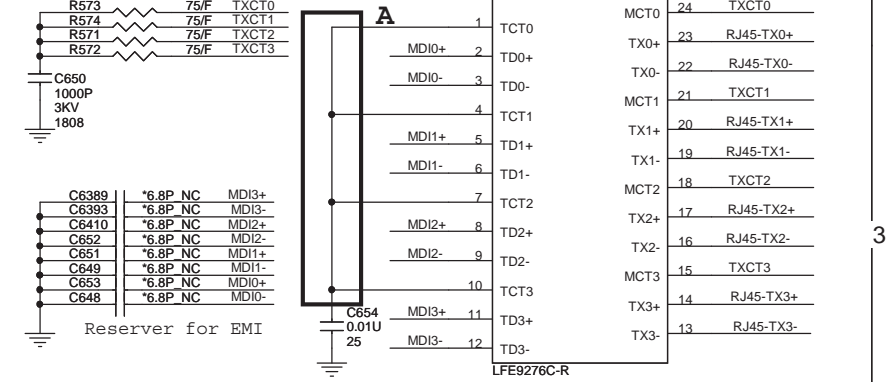
LAN



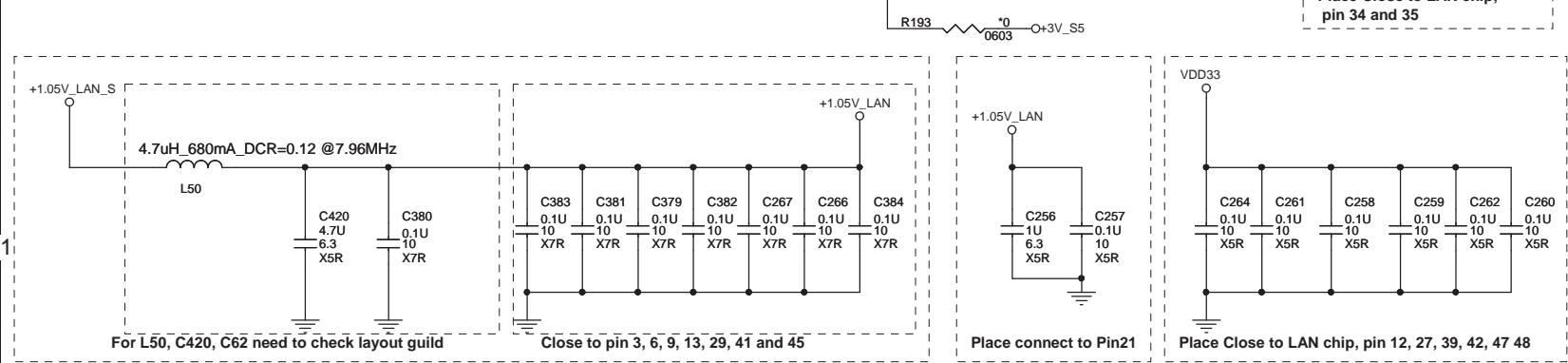
LAN EEPROM



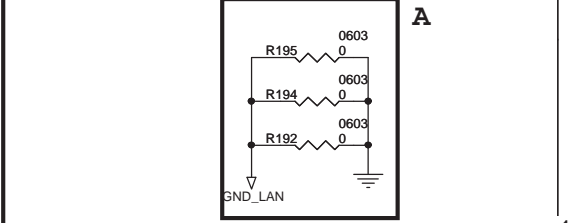
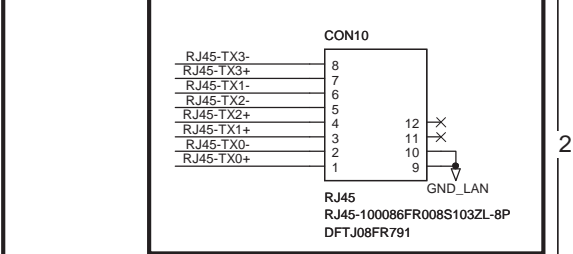
10/100 Transformer



LAN Power



RJ45



Quanta Computer Inc.
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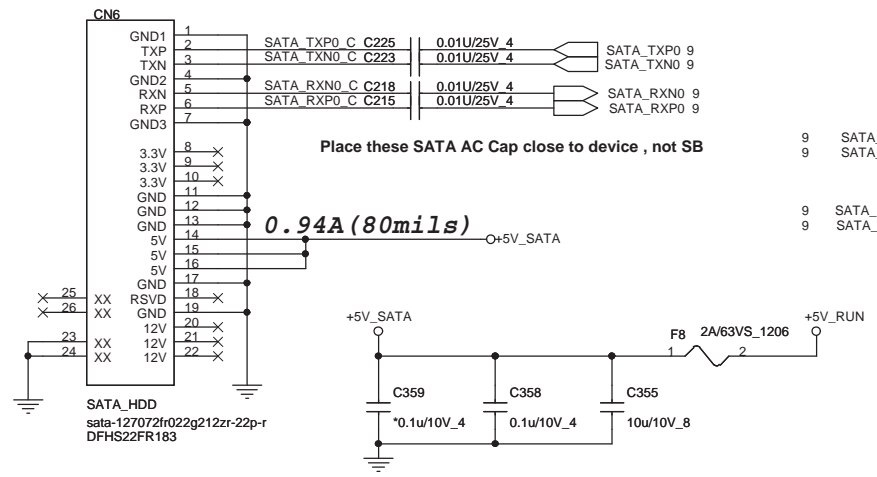
A

B

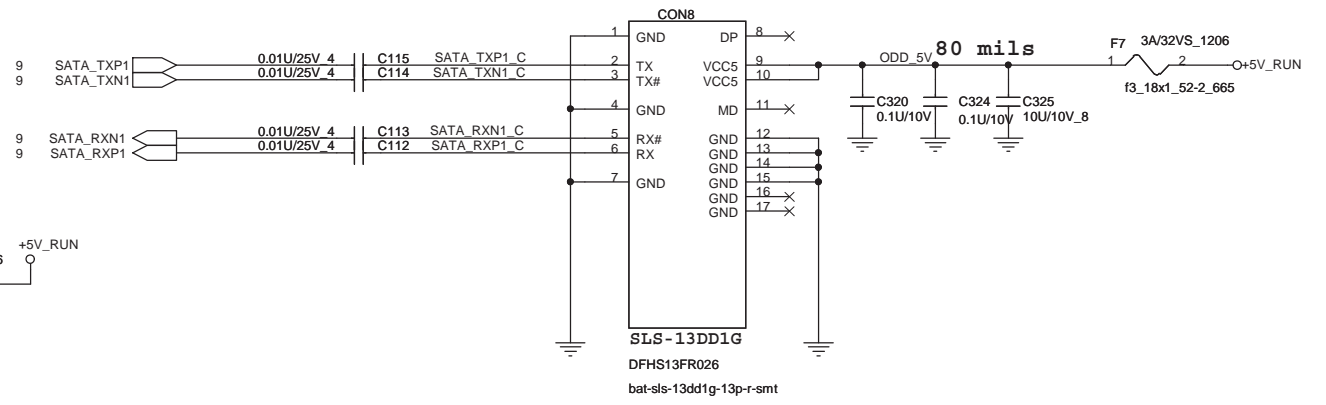
C

D

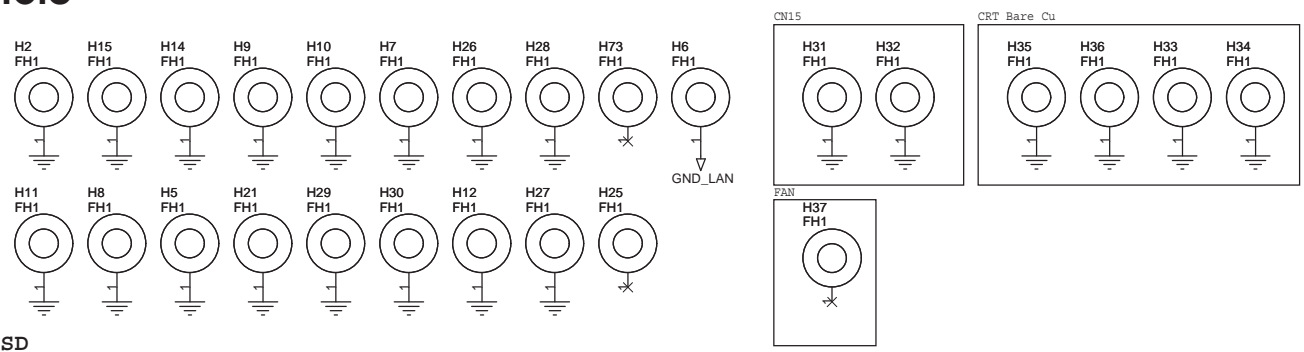
E



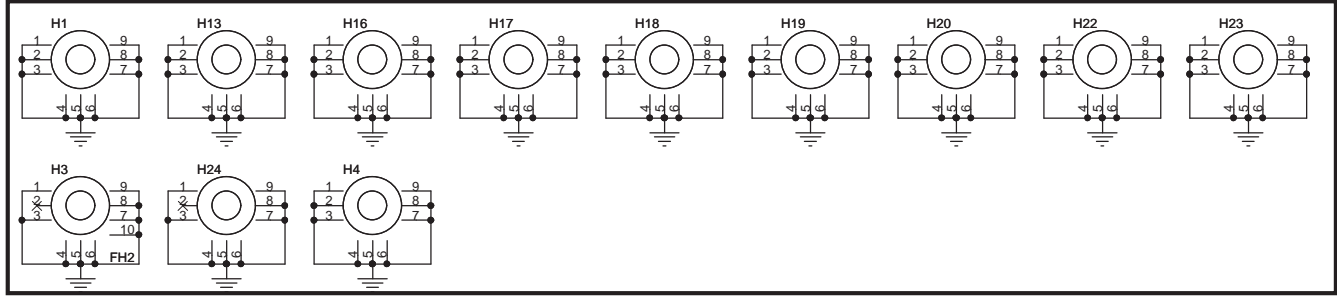
ODD CONN



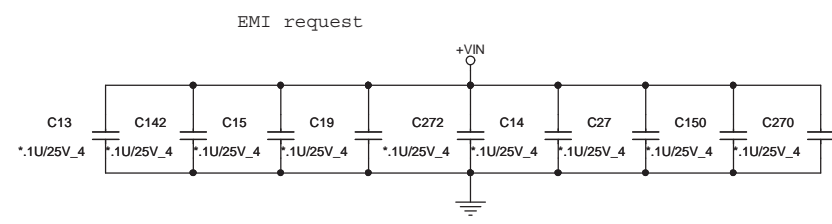
Hole



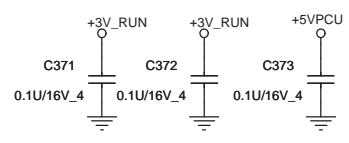
ESD



Decoupling Cap

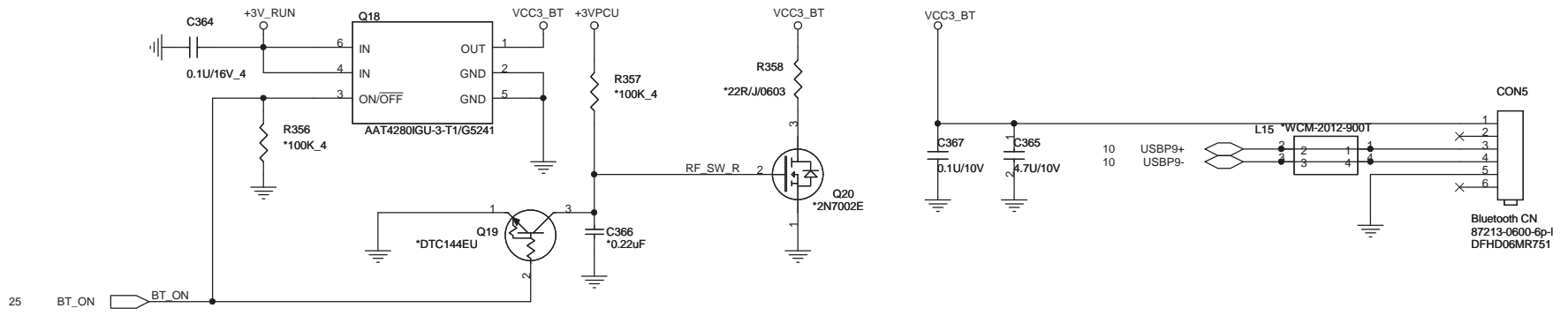


EMI(Decoupling Cap)

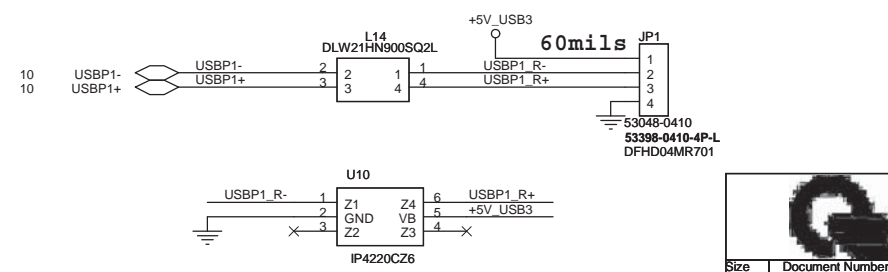
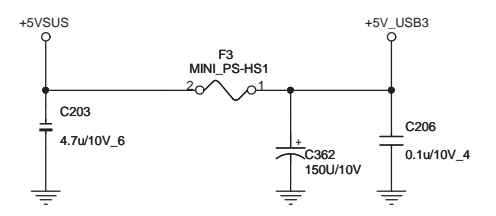
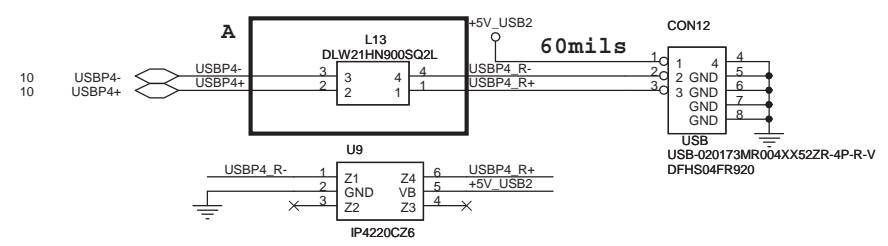
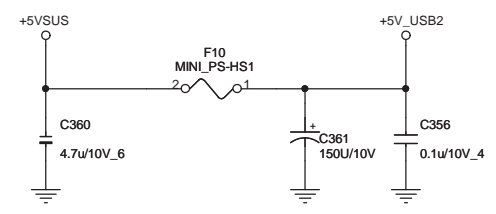
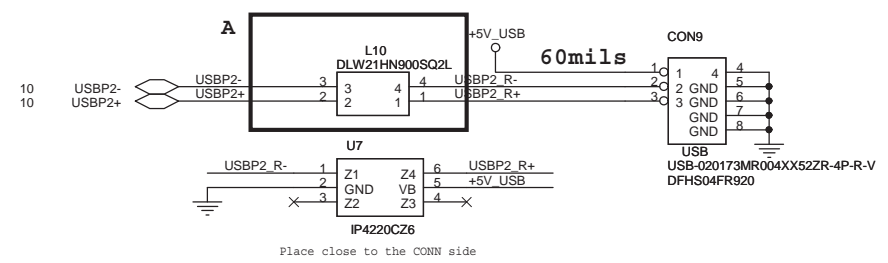
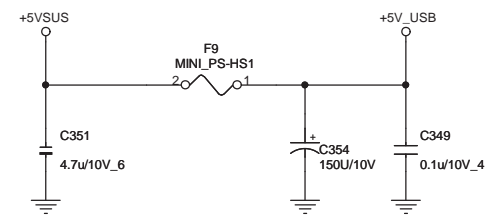


Quanta Computer Inc.
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	HDD/ ODD/HOLE	1A
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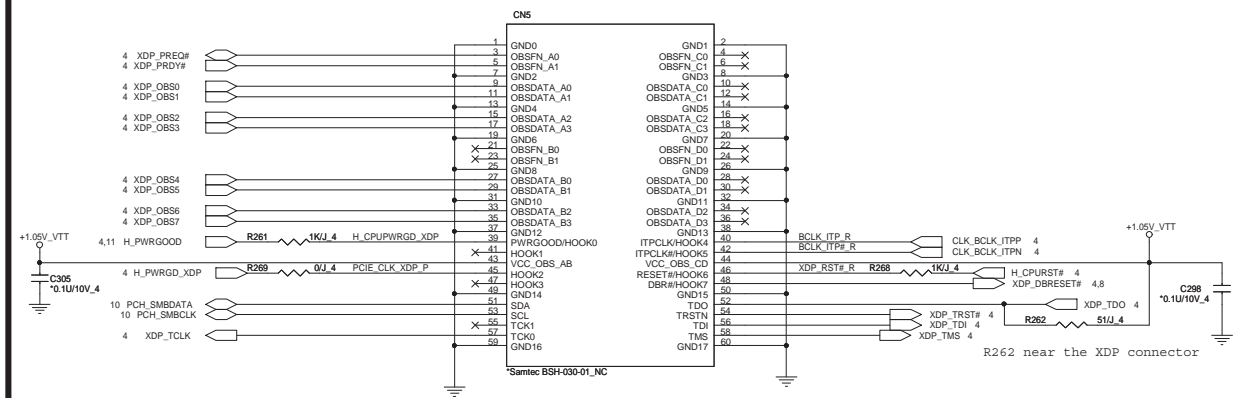
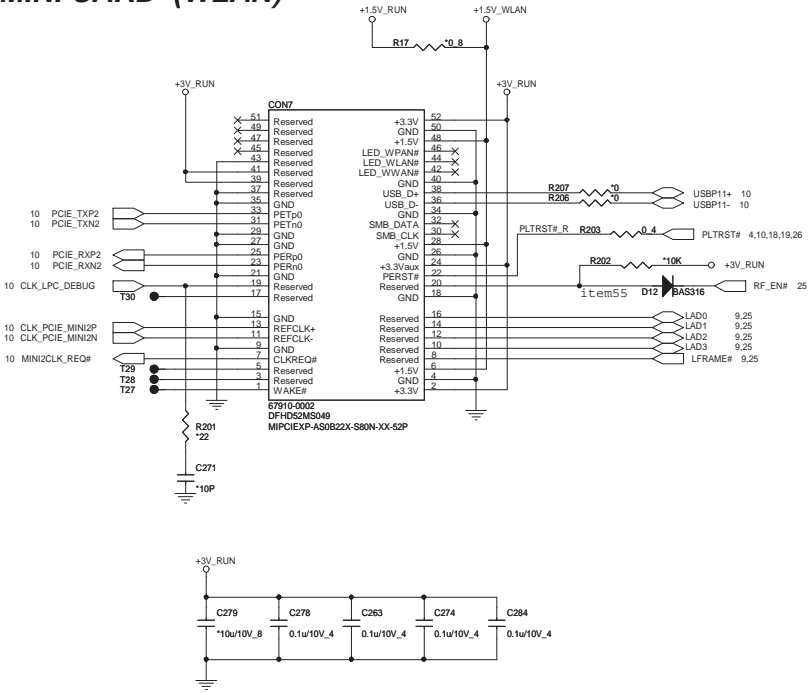
USB Connector



Quanta Computer Inc.
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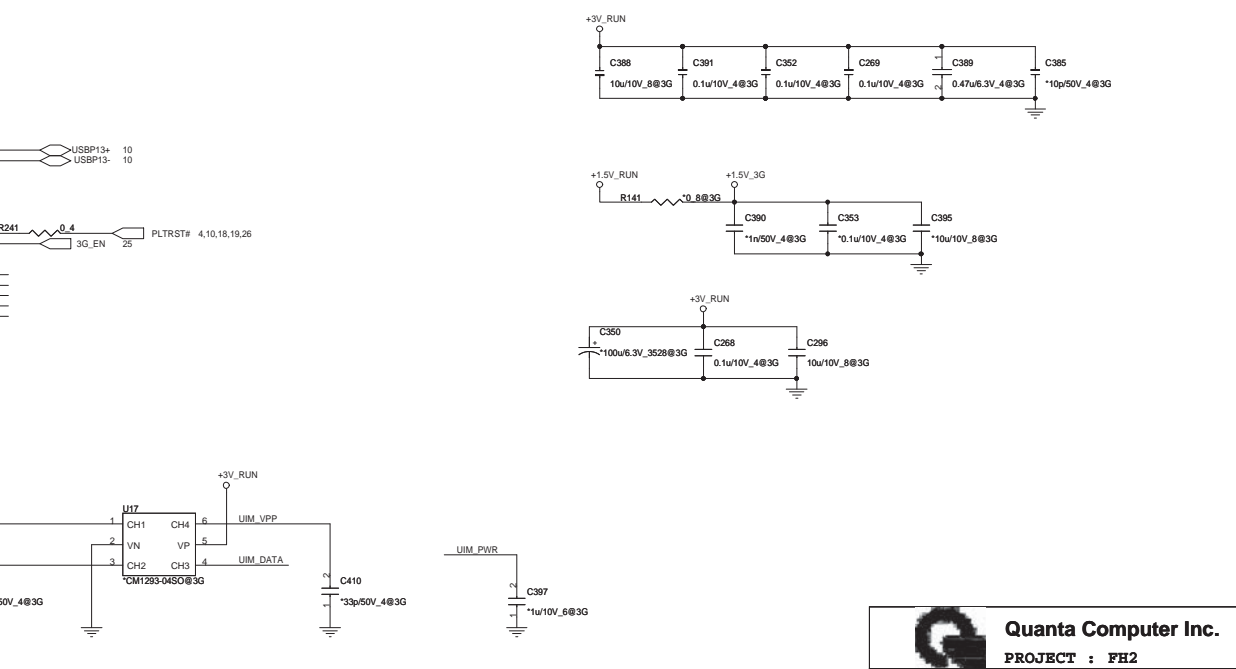
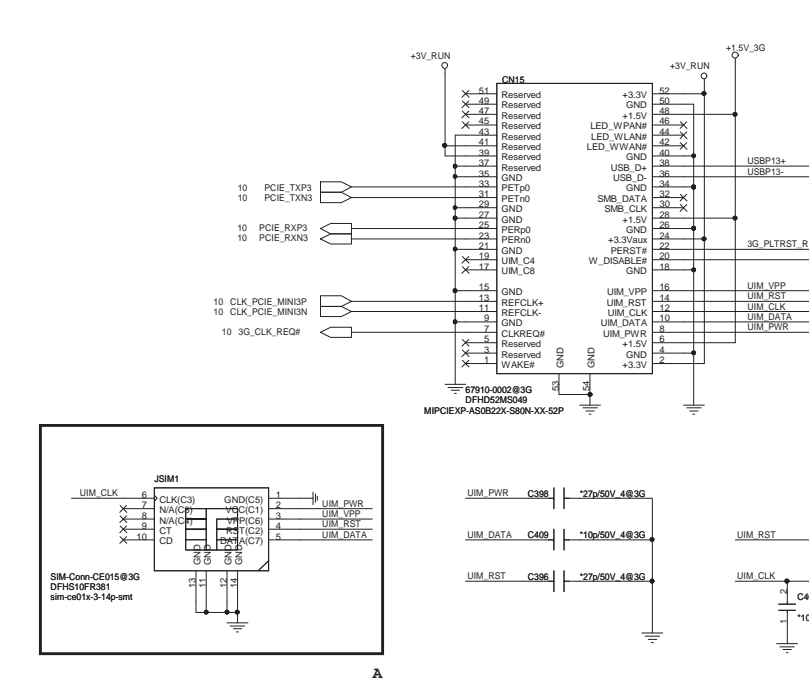
Size	Document Number	Rev
	USB/BLUE TOOTH	1A
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MINI CARD (WLAN)

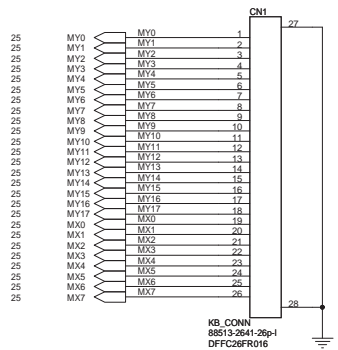


It is for debug, request vevdeez provide 200 pcs sample.

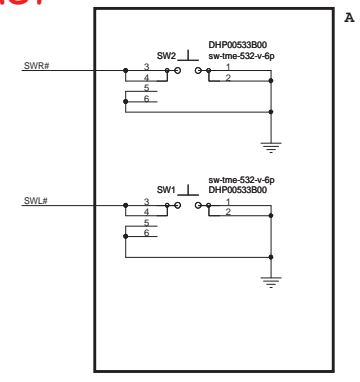
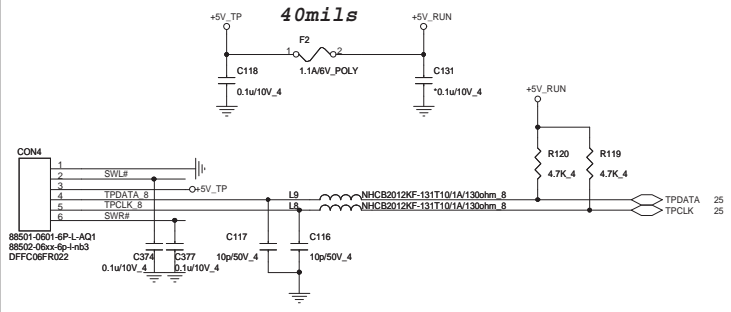
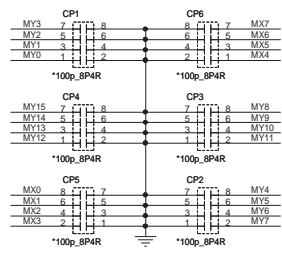
Mini Card2-3G(MNC)



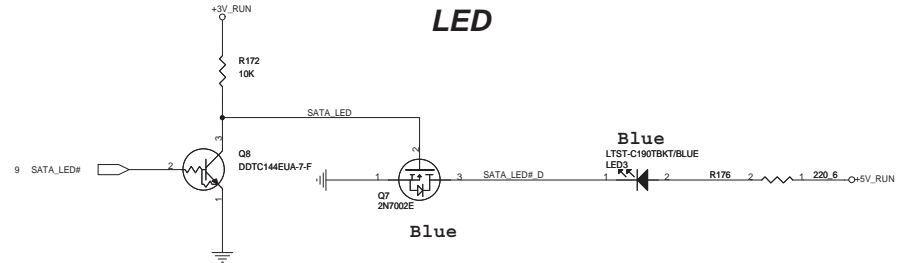
Keyboard(KBC)



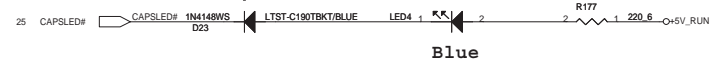
For EMI Reserve Caps for debug



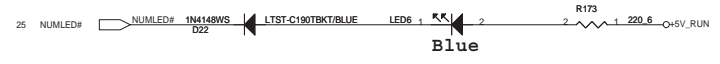
HDD/ODD



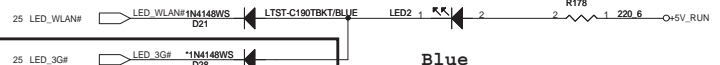
CAPS LED



NUM LED



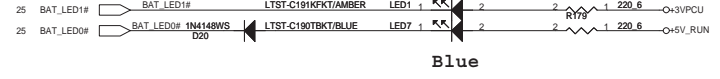
WLAN



3G

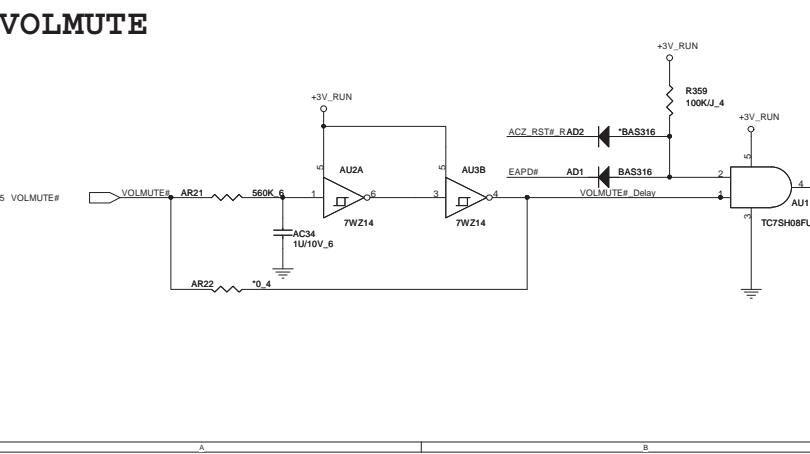
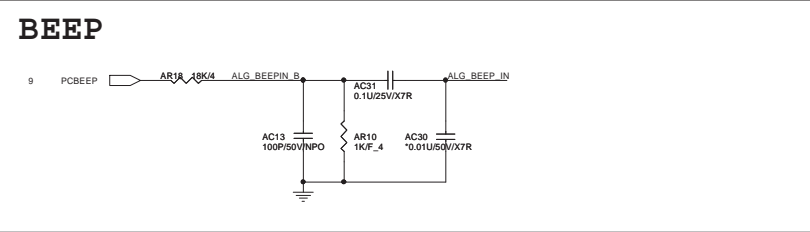
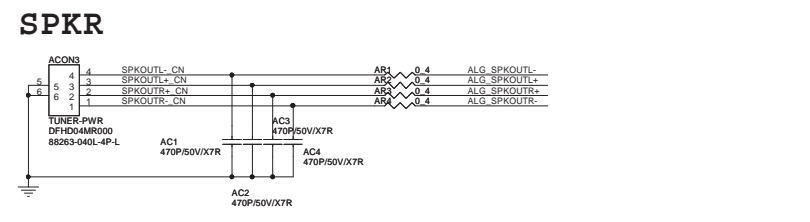
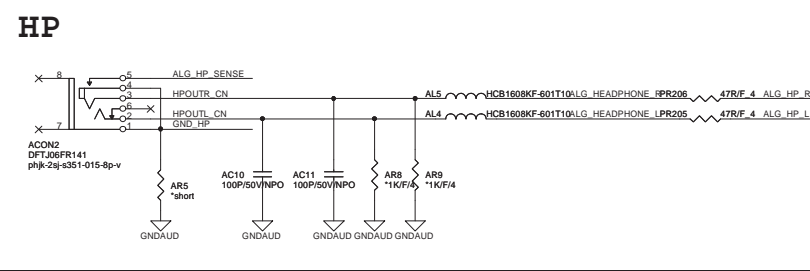
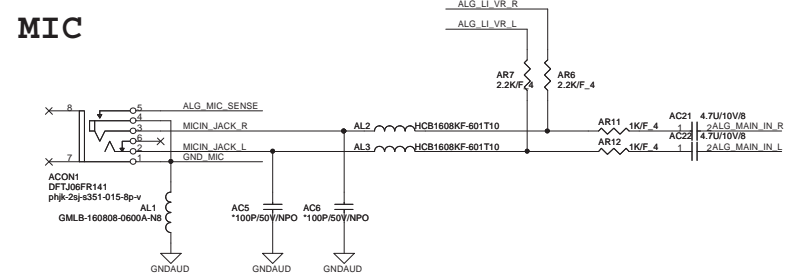


Battery



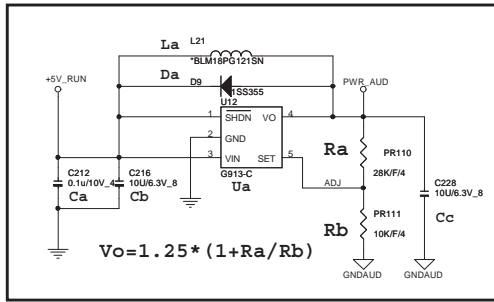
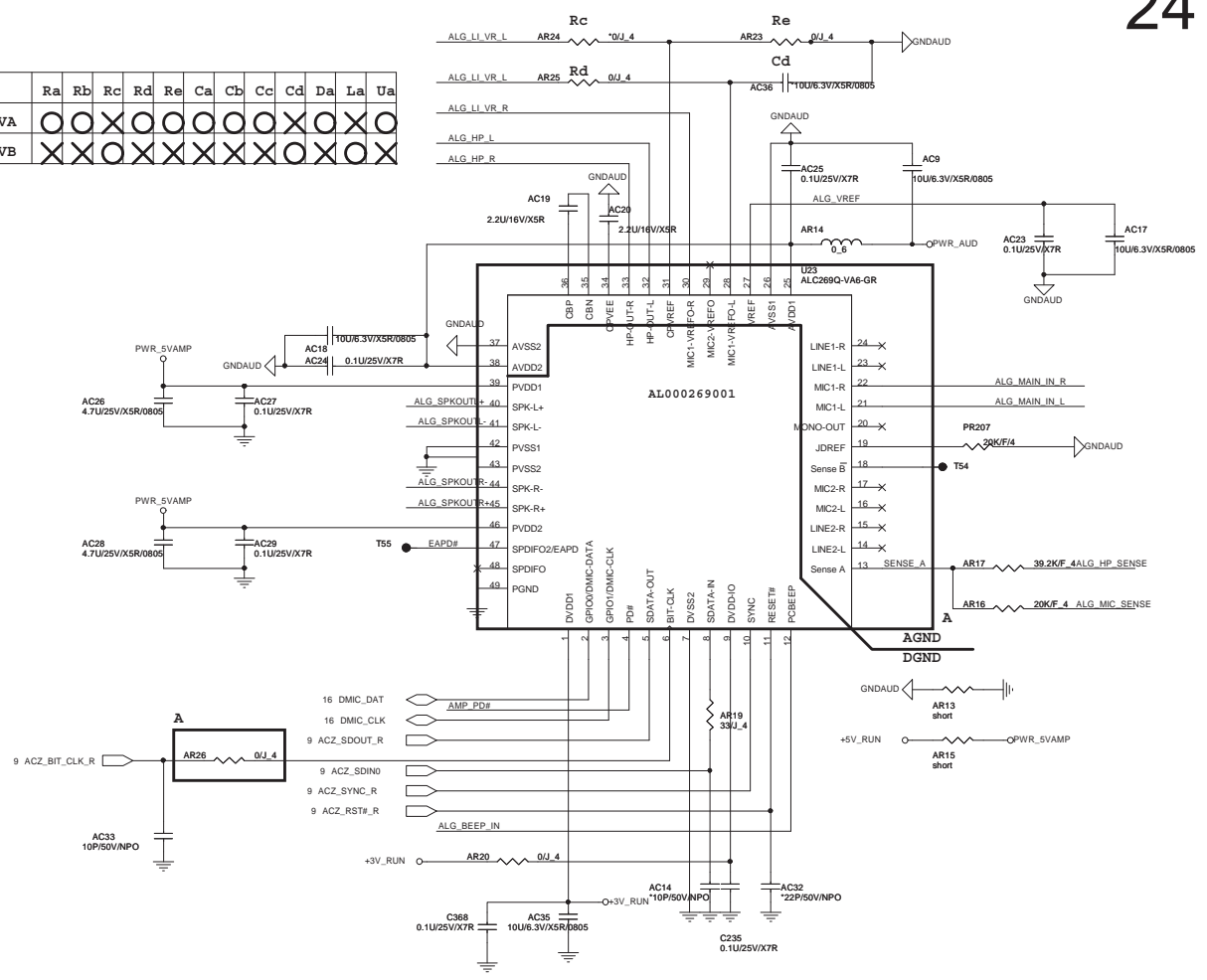
Power Status

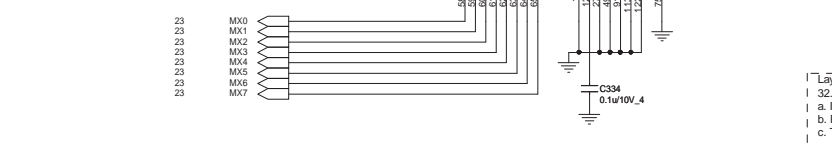
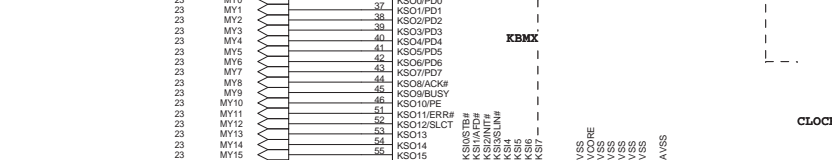
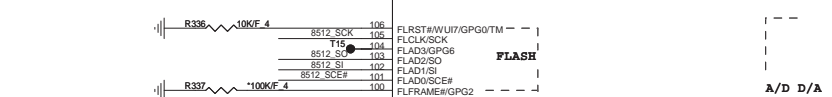
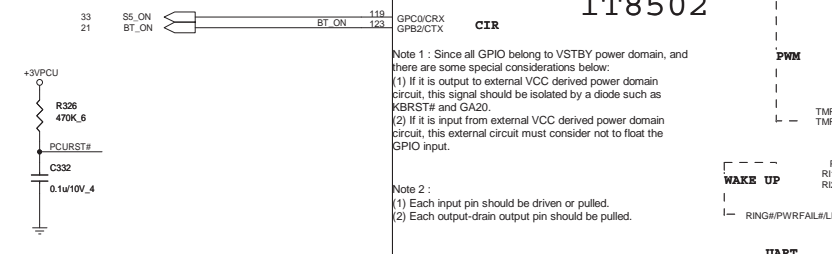
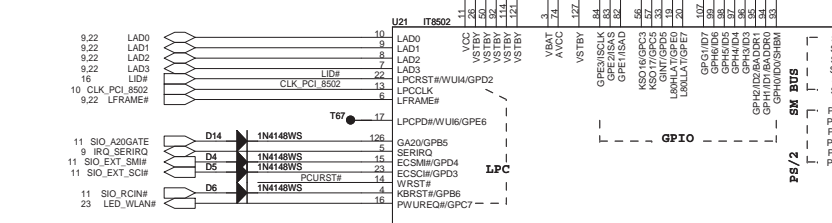
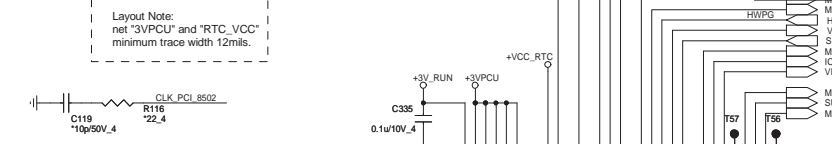
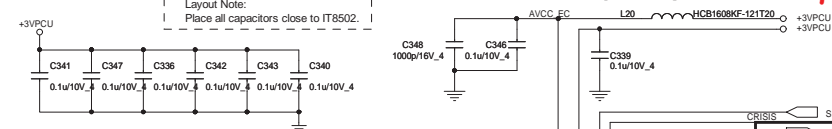




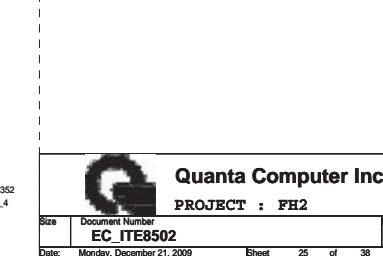
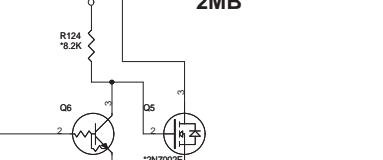
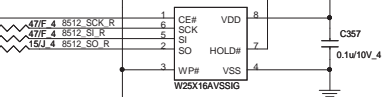
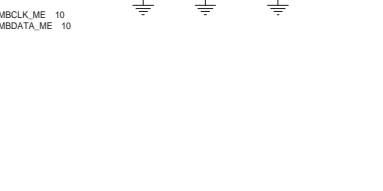
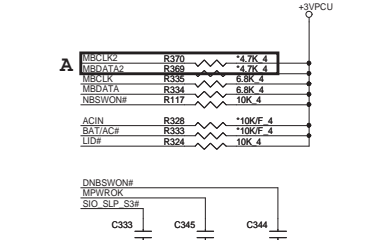
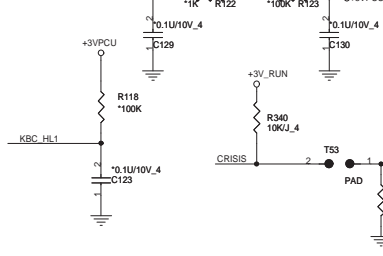
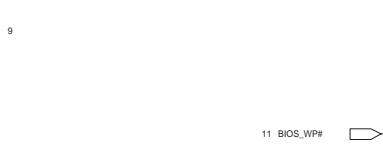
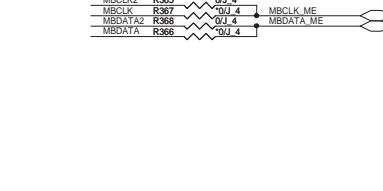
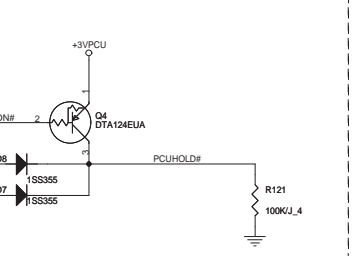
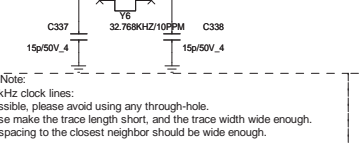
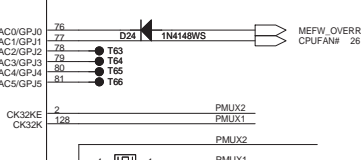
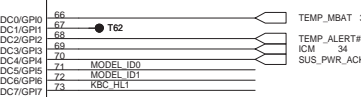
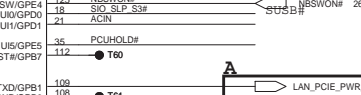
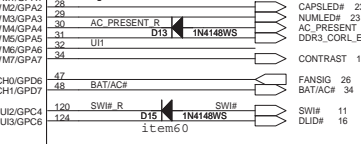
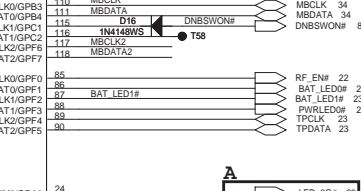
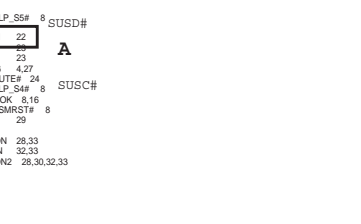
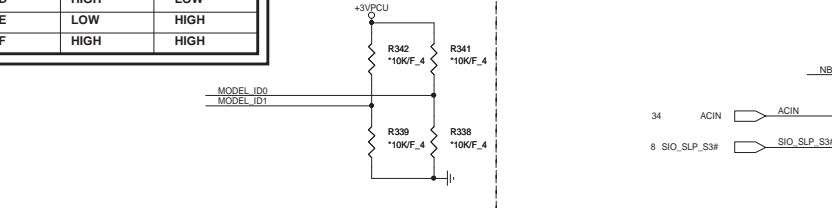
U23	Ra	Rb	Rc	Rd	Re	Ca	Cb	Cc	Cd	Da	La	Ua
ALC269Q-VA	○	○	○	○	○	○	○	○	○	○	○	○
ALC269Q-VB	○	○	○	○	○	○	○	○	○	○	○	○

Codec ALC269

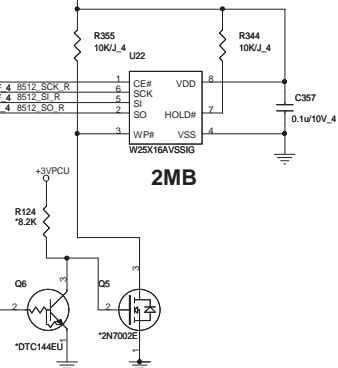




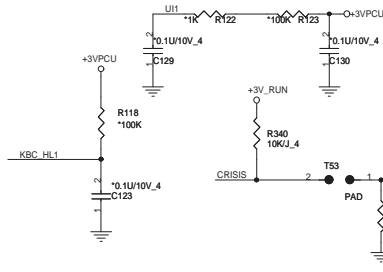
PCB REV	MODEL_ID0	MODEL_ID1
C	LOW	LOW
D	HIGH	LOW
E	LOW	HIGH
F	HIGH	HIGH

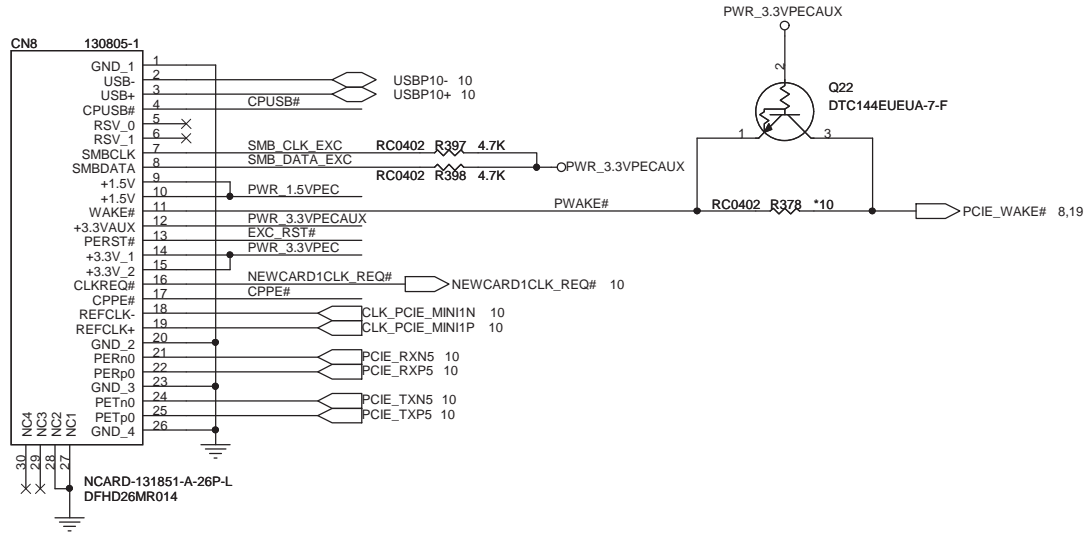
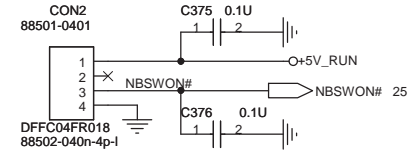
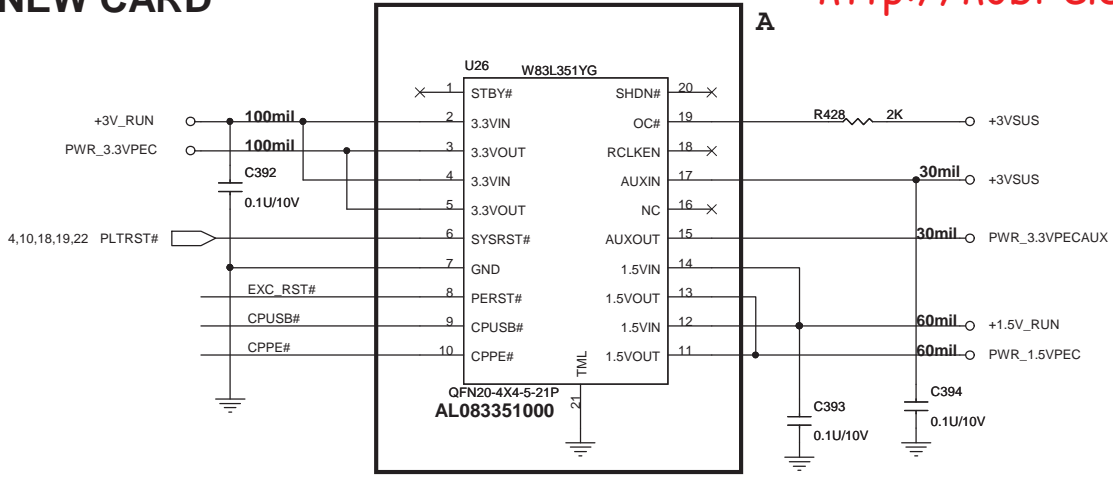


BIOS Write Protect

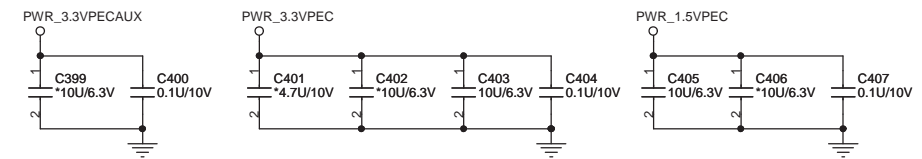
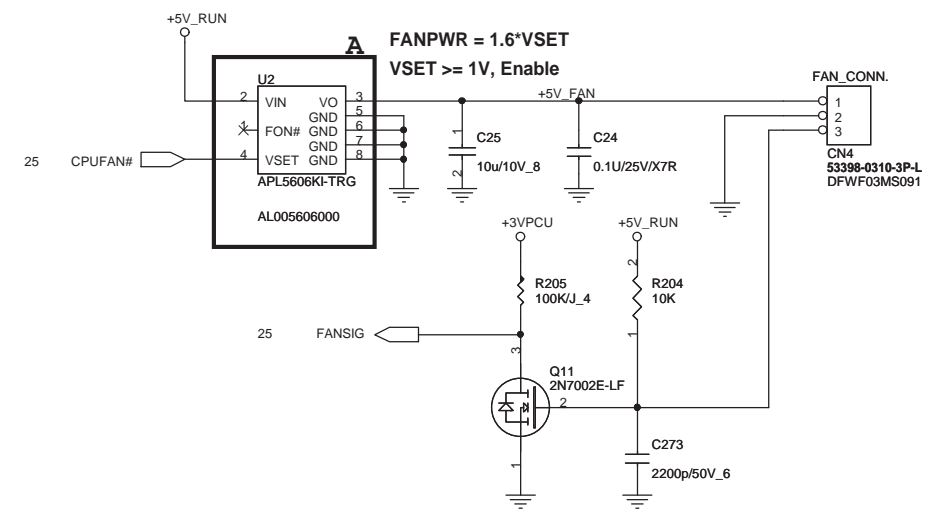


Near ROOM DOOR





CPU FAN CTRL

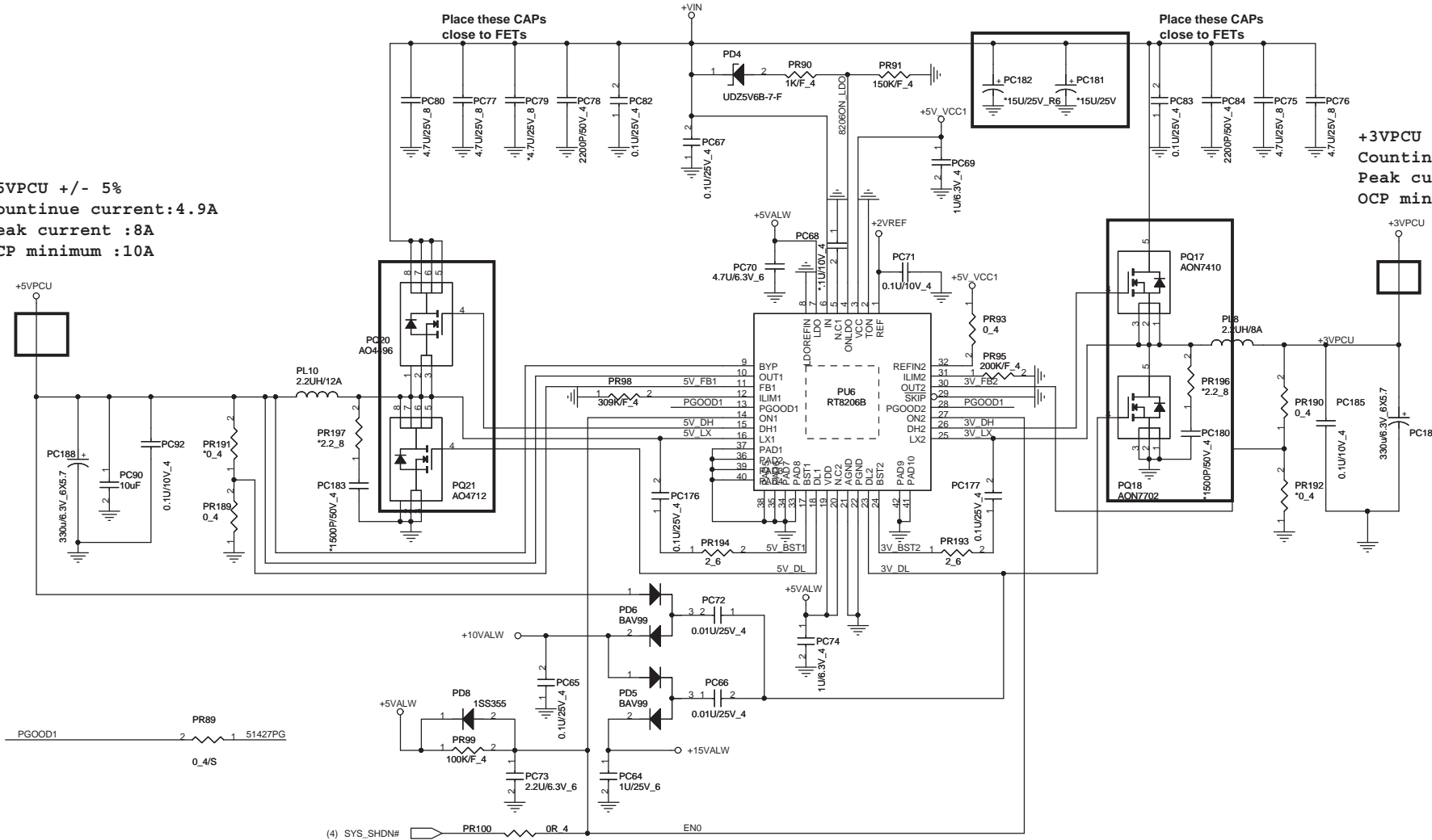


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PROJECT : FH2

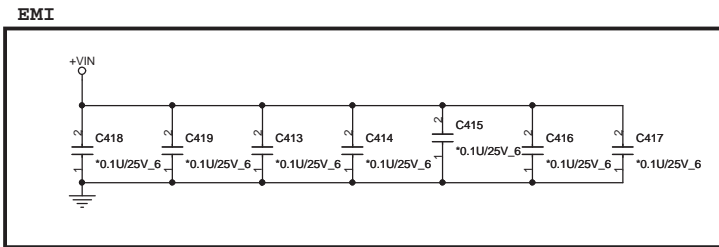
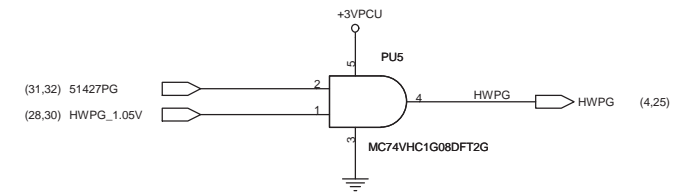
Size	Document Number	Rev
	FAN/SW/NEWCARD	1A
Date:	Monday, December 21, 2009	Sheet 26 of 38

+5VPCU +/- 5%
 Countinue current:4.9A
 Peak current :8A
 OCP minimum :10A

+3VPCU +/- 5%
 Countinue current:5.1A
 Peak current:6A
 OCP minimum 7.5A



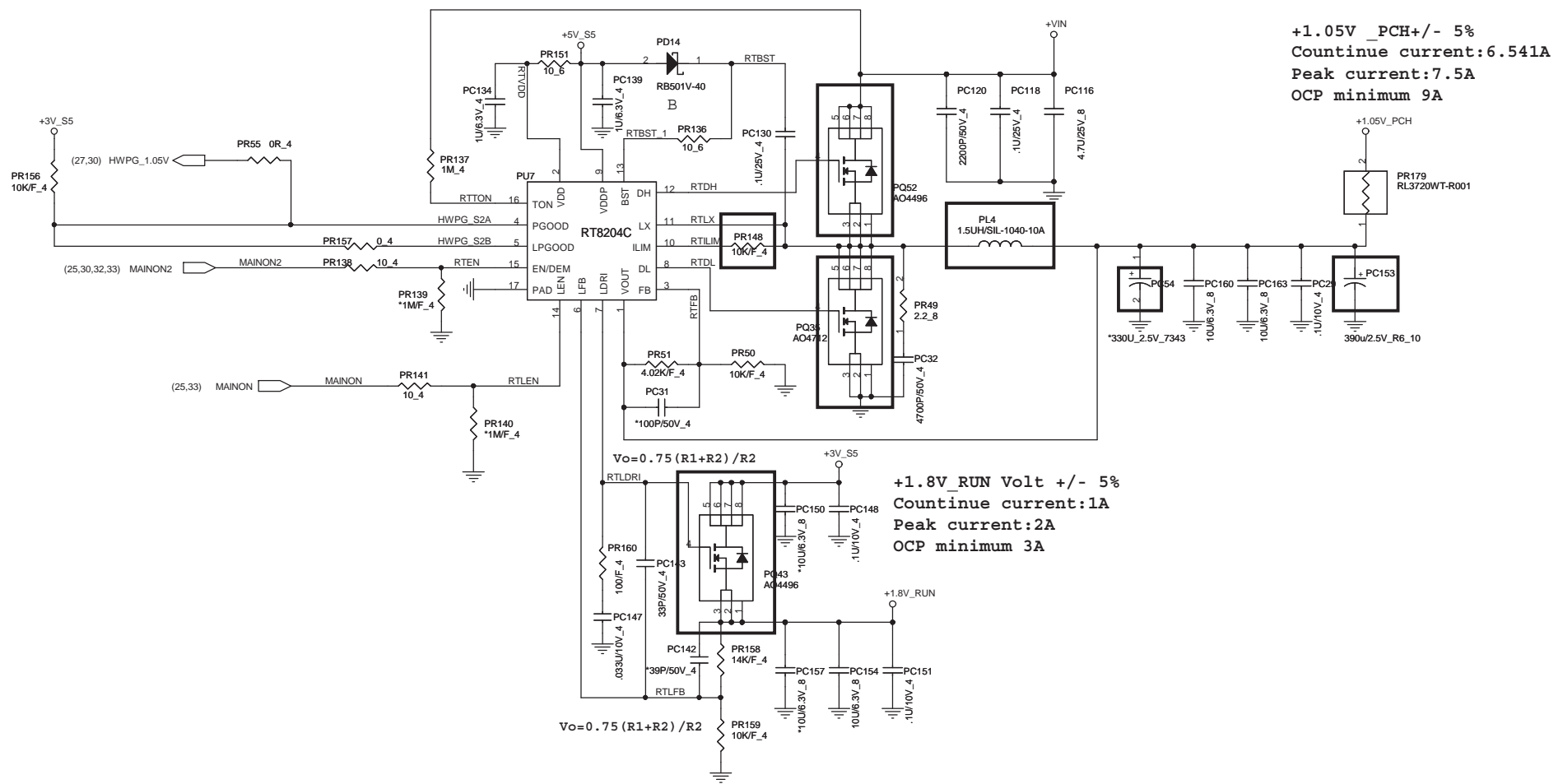
(4) SYS_SHDN# PR100 0R 4 EN0



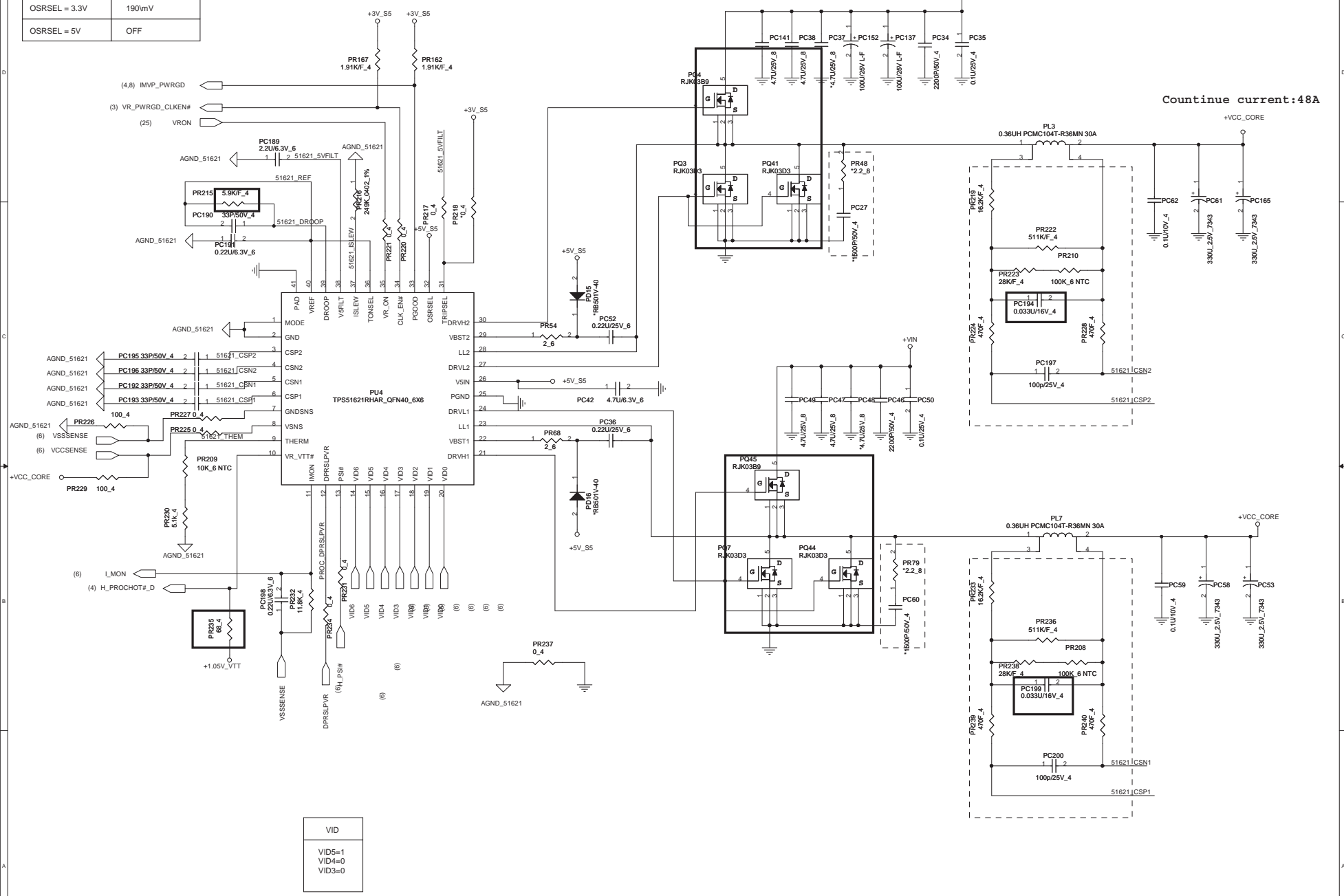
Quanta Computer Inc.
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Size	Document Number	Rev
		1A

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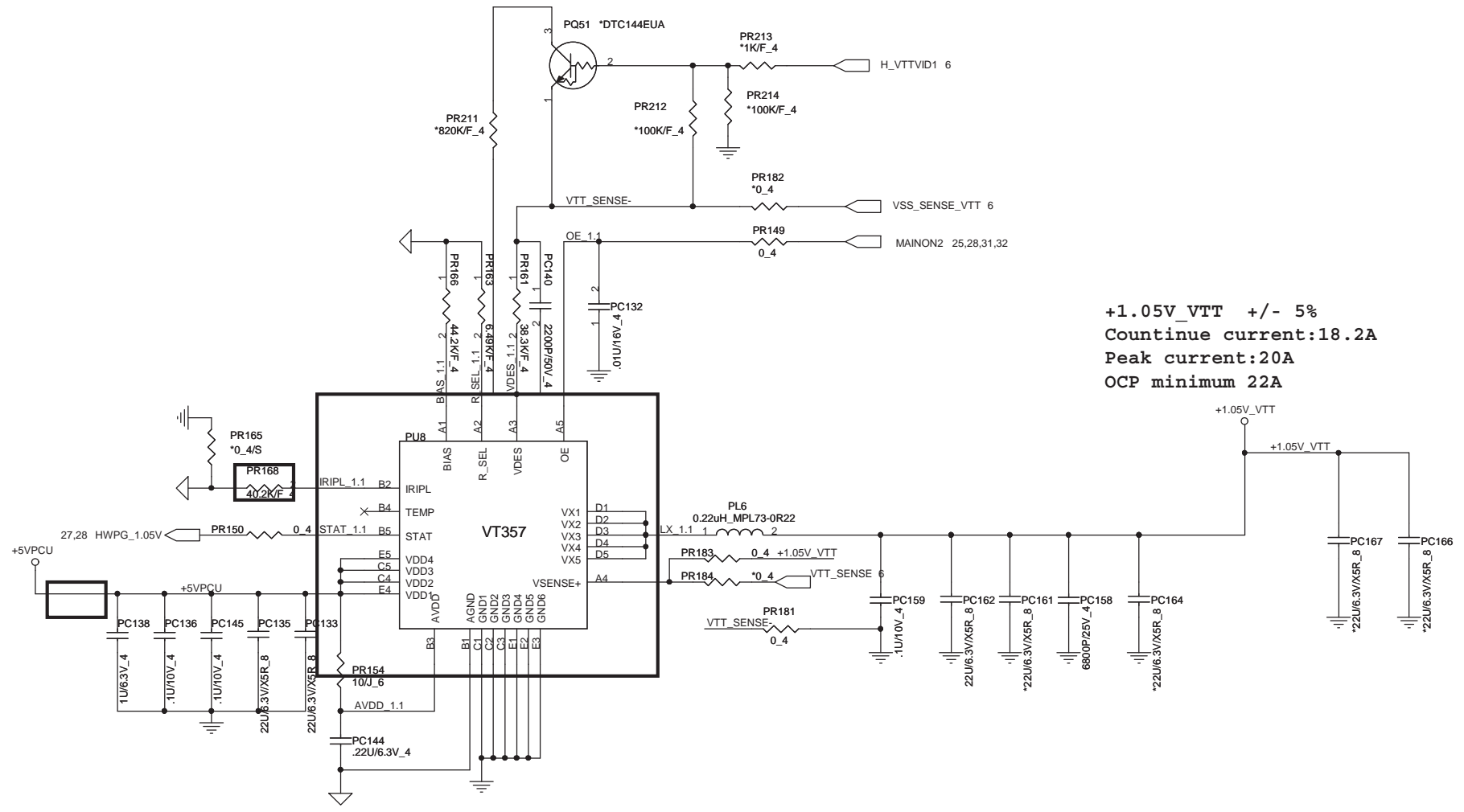
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OSRSEL = REF	145mV
OSRSEL = 3.3V	190mV
OSRSEL = 5V	OFF




Continue current:48A

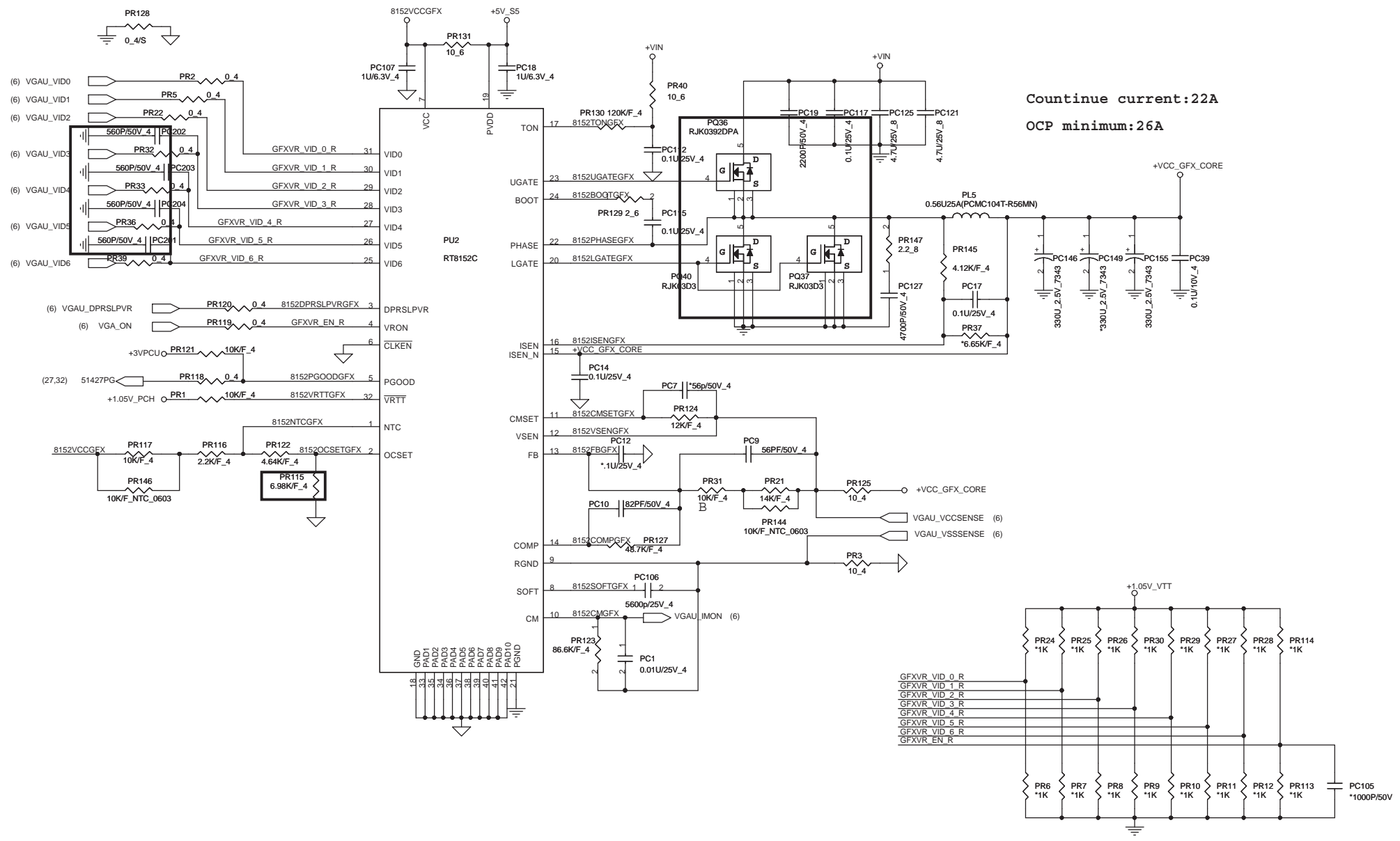
VID
VID5=1
VID4=0
VID3=0

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Size	Document Number	Rev
	CPU Core (TPS51621)	1A
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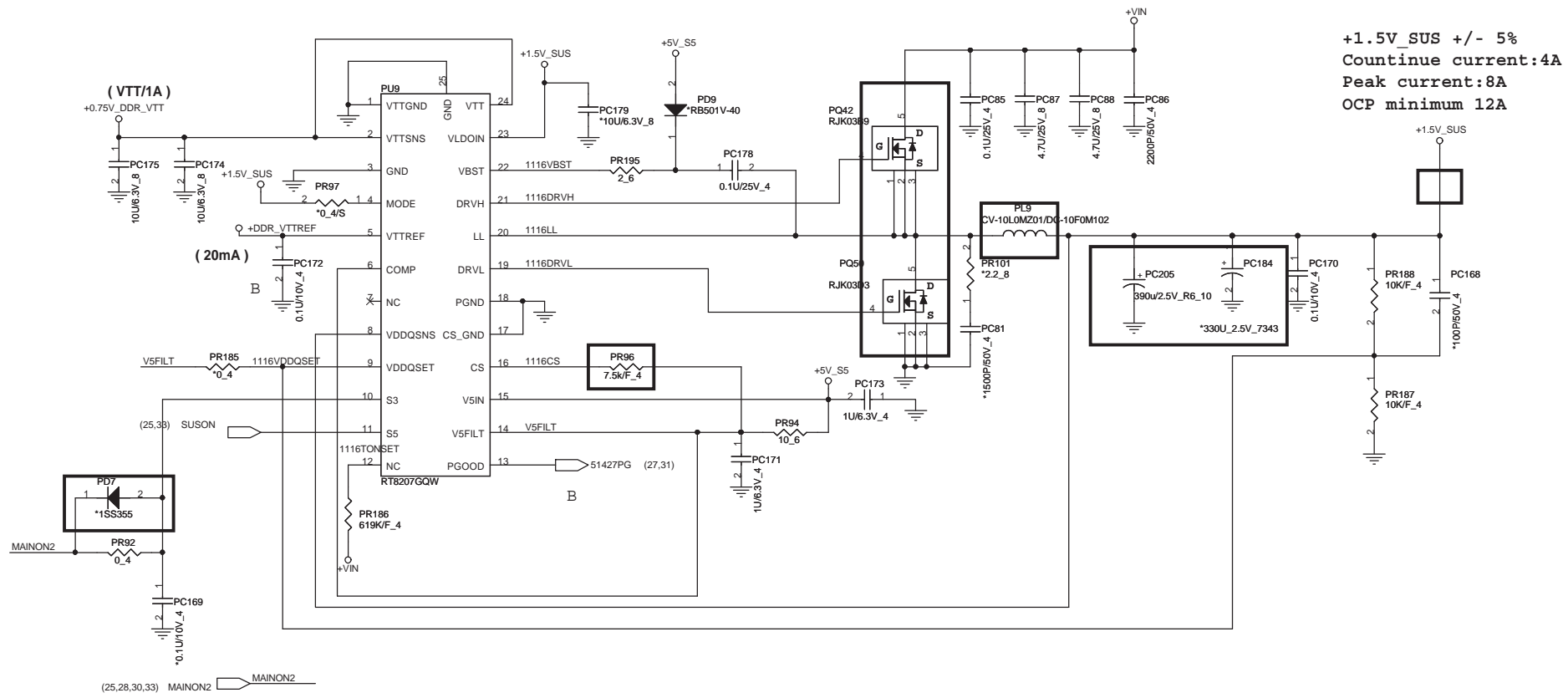


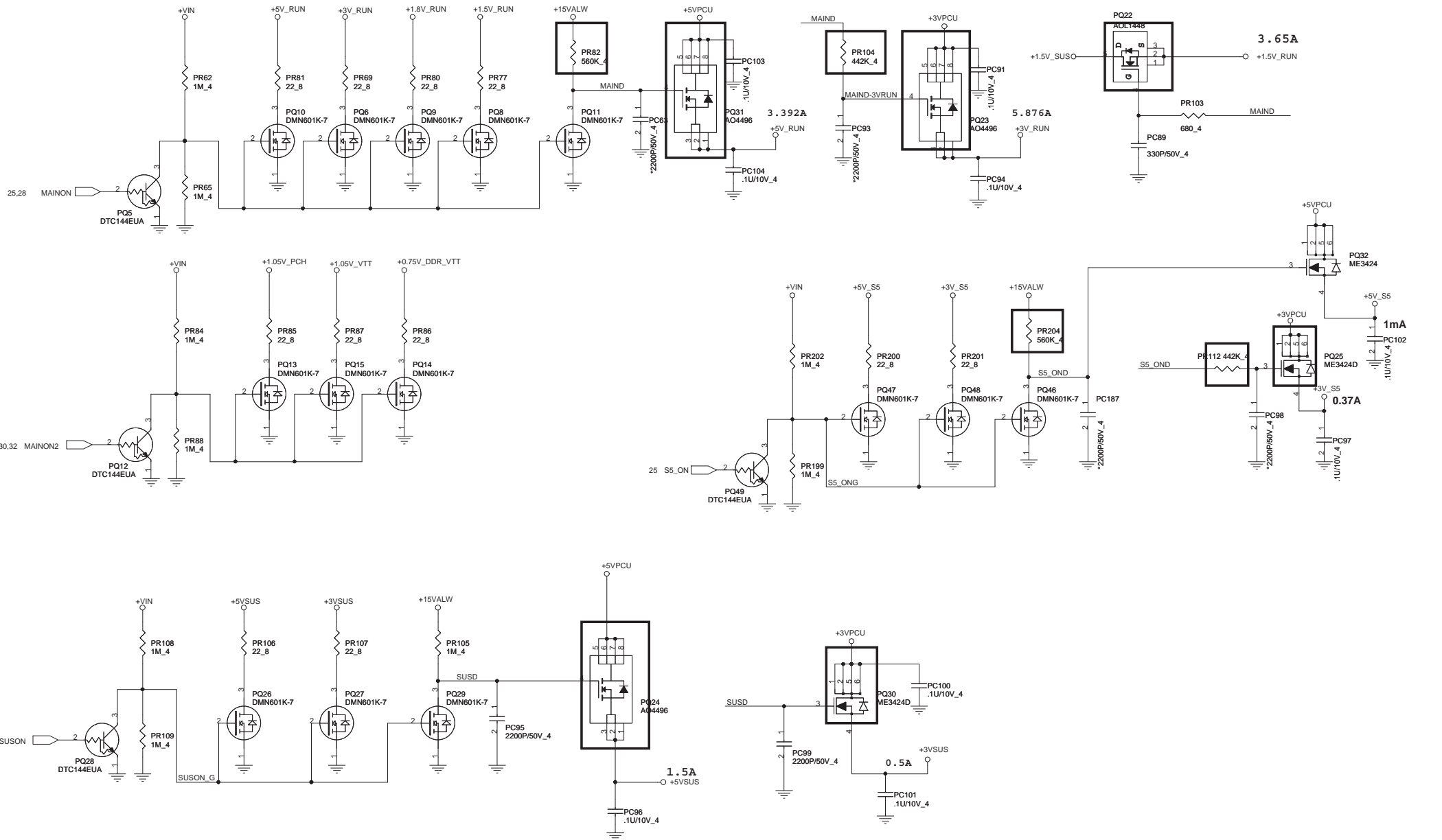
+1.05V_VTT +/- 5%
 Countinue current:18.2A
 Peak current:20A
 OCP minimum 22A

 Quanta Computer Inc. PROJECT : FH1A		Size	Document Number	Rev
		+1.05V_VTT (VT358)		1A
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Continue current:22A
 OCP minimum:26A





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		1A
DISCHARGE/3VS5/5VS5/LAN		
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