Field Engineering Education Student Self-Study Course

## Preface

This is Book 4 of the System/360 Introductory Programming Student Self-Study Course.

## Course Contents

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## Prerequisite

- Systems experience ( 1400 series with tapes, 7000 series with tapes) or a basic computer concepts course.
- Books 1, 2, and 3 of this Introductory Programming course.

Instructions to the student and advisor

- This course is to be used by the student in accordance with the procedure in the Instructions to the Student section in Book 1 of this course.
- The course is to be administered in accordance with the procedure in the System/360 Introductory Programming Administrator Guide, Form \#R23-2972.

This edition, R23-2958-1, is a minor revision of the preceding edition, but it does not obsolete R23-2958-0. Numerous changes of a minor nature have been made throughout the manual.

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## How to use this book

There are four sections to this text. At the beginning of each section, there is a list of Learning Objectives which you will be expected to learn as a result of studying that particular section. Instead of having review questions at the end of each section, this book has a programming exercise in the last section and review questions for the entire book. You can evaluate your understanding of the book as you do this exercise. You will go through this book in a serial fashion. That is, you will not be expected to skip or branch around. The answer to each frame is in the next frame. You may find it helpful to use a standard IBM card to cover the answers as you read the frames.

Periodically, as you go through this book, you will be directed to study areas of the System/360 Principles of Operation manual. This will help you to become familiar with the manual so that it may be used as reference material at a later date.

THE CONTENTS OF THIS BOOK

This book deals mainly with the "branching, logical and decimal" instructions of the System/360. Some of these instructions are part of the Standard Instruction set and some are part of the Decimal Feature Instruction set.

| SEC TION I | Branching Operations |
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| SEC TION II | Logical Operations |
| SECTION III | Decimal Operations |
| SECTION IV | Analyzing Decimal Feature Programs |

ALPHABETICAL INDEX

# System/360 Branching, Logical and Decimal Operations 

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- Section I: Branching Operations Section II: Logical Operations Section III: Decimal Operations Section IV: Analyzing Decimal Feature Programs <br> LEARNING OBJECTIVES
}

At the end of this section, you should be able to do the following when given the mnemonic of any 'branching" instruction.

1. State instruction length and format.
2. State location and format of operands.
3. Determine the result and where it will be located.
4. State effect on condition code.
5. State which program checks are possible.

## Branching Operations

The first section of this text deals with the "branch" instructions of the System/360. You have previously learned how the PSW is used to control the sequence of instruction fetching and execution. You have also learned how the normal sequence of instruction fetching can be changed by (a) an interrupt, (b) the "load PSW" instruction and, (c) a "branch" instruction. You have also studied one of the 'branch" instructions: "branch on condition."

In the IBM System/360 Principles of Operations manual, briefly study the following areas of the Branching section.

Branching
Normal Sequential Operation
Branch On Condition

After completing these areas, you may proceed to the next frame.

The address of the next instruction to be fetched is contained in bits $40-63$ of the $\qquad$
$\qquad$ -

After an instruction has been fetched, bits 0 and 1 of its Op code are used to update bits $\qquad$ through $\qquad$ of the PSW. Updating this instruction address portion (bits $\overline{40-63}$ ) of the PSW consists of increasing it by $\qquad$ , $\qquad$ or $\qquad$ -.

If bits 0 and 1 of the "current" instruction's Op code are 00 (RR format), the instruction address is increased by $\qquad$ -

If bits 0 and 1 of the "current" instruction's Op code are 01 or 10 , the instruction address is increased by $\qquad$ -

If bits 0 and 1 of the "current" instruction's Op code are 11 , the instruction address is increased by $\qquad$ .

Given the following symbolic program, indicate (decimally) the contents of bits 40-63 of the PSW after the program is executed. (If necessary, use the Alphabetic List of Instructions in the Appendix of the Principles of Operation manual as a reference.)


2068; Each instruction The sequential manner of instruction fetching can be changed by means of increased the address by 4 . a "branch" instruction. When a branch is taken, the address of the "branch to" location replaces .

BRANCH ON CONDITION INSTRUCTION - REVIEW

The instruction address (bits 40-63) in the PSW.

The second operand fields in all "branch" instructions indicate the "branch to" location. Given the following BCR instruction, bits 40-63 of the PSW will be replaced by bits $8-31$ of register $\qquad$ .


Given the following BC instruction, bits $40-63$ of the PSW will be replaced by $\qquad$ (the effective generated address/ the contents of the storage area).

the effective generated address

Show the binary bit structure of bits $40-63$ of the PSW after executing the previous instruction.


In the "branch on condition" instruction, the condition code is tested against the R1 field or (as it is sometimes referred to) the $\qquad$ field.
M1 or Mask Each bit of the mask field (bits 8-11) is used to test for a specific setting of the PSW $\qquad$ -.

Bit position 8 is used to test for a condition code setting of $\qquad$ .

00
Bit position 9 tests for a condition code setting of $\qquad$ .

Bit position 10 tests for a condition setting of $\qquad$ and bit position 11 is used to test for a condition code setting of $\qquad$ .

More than one condition code setting can be tested for at the same time
11 by setting the appropriate bits of the mask field. Show the mask field bits that will test for a condition code setting of 10 or 11 .


BC INSTRUCTION MASK FIELD

Show the mask field bits that are necessary to branch on an equal or high indication after a "compare" instruction.


BC INSTRUCTION MASK FIELD

The "branch on condition" instruction can be used as an "unconditional branch" instruction. Show the mask field bits that would accomplish this.


1111 (expressed hexadecimally as F )

The "branch on condition" instruction will never result in a branch if the mask field contains $\qquad$ _. $\qquad$

0000
If the R 2 field of a BCR (not BC ) instruction contains 000, a branch (can/cannot) occur.
cannot
Which of the following "branch" instructions will not result in a branch? (Circle one or more.)
a.

b.

c.

d.

| 47 | 1 | 0 | 0 | 000 |
| :--- | :--- | :--- | :--- | :--- |

b. because the mask field is zero
c. because the R 2 field is zero

Answers a and d above will result in a branch if the condition code is 11 .

## BRANCH AND LINK INSTRUCTION

$\qquad$
Let's continue now and study another "branch" instruction. Read the description of the "branch and link" instruction in the Branching section of your Principles of Operation manual.

The mnemonic for the "branch and link" instruction is $\qquad$ .

The "branch and link" instruction can be either of the RR format or the RX format. The mnemonic used for the RR "branch and link" is $\qquad$ .

## 4 Branching Operations

BAL The BAL instruction always results in a branch. The BALR instruction BALR will not result in a branch if the R 2 field is $\qquad$ -.

## zero

In all cases (even when the R2 field is zero), bits 32-63 of the PSW a re stored in the register specified by the $\qquad$ field.

## R1

The address that is stored by a "branch and link" instruction is the address of the instruction that would have been executed if the branch were not taken.

Given the following symbolic program, show what bits $8-31$ of register 1 will contain after the BALR instruction is executed.


| LH | $0,0(0,7)$ |
| :--- | :--- |
| AH | $0,2(0,7)$ |
| BALR | 1,3 |
| STH | $0,4(0,7)$ |

$\operatorname{Reg} 1=2058$
Write the mnemonic of the instruction whose address was stored in register 1 in the previous problem. $\qquad$

## STH

The reason for storing the address of the next sequential instruction during a "branch and link" operation is to provide a linkage between routines. This is illustrated as follows:


As you can see above, the "branch and link" instruction will:

1. Cause the address of the STH instruction of routine $A$ to be stored in register 1.
2. A branch will be taken to the SH instruction in routine B (as specified by the contents of register 3 ).
3. The last instruction in routine $B$ is an unconditional branch (because the mask field contains 15) back to the STH instruction in routine A .
4. The address of the STH instruction was obtained from register 1 where it was stored from the preceding BALR instruction.

| BALR | 1,0 |
| :--- | :--- |
| AR | 2,2 |

In the above program, the BALR instruction will cause bits $32-63$ of the PSW to be stored in register $\qquad$ , and a branch $\qquad$ (is/is not) taken.

1 is not

The BALR instruction, with an R2 field of zero, may be used to load a base address into a general register. Examine the following program; then read the following frames.


Assuming that 2000 is the address of the BALR instruction, what address will be placed in register 12 ? $\qquad$

2002; Note that only bits 40-63 of the PSW are referred to in our discussions. Although bits 32-39 are also placed in register 12, they are ignored in generating addresses later on. Only bits $8-31$ of a register are used in address generation.
Because the R2 field of the BALR instruction is zero, a branch (will/will not) be taken.
will not
The second operand of the LH instruction will have a base address of
$\qquad$ and a displacement of $\qquad$ -.

The last instruction (BCR) will cause an "unconditional branch to" location
$\qquad$ .

Write the mnemonic of the instruction at location 2002.

LH; Actually this program will never end because of the "unconditional branch back to" the LH instruction.

Thus far you have seen two main uses for the "branch and link" instruction. It can be used to:

1. Branch to some routine and automatically provide the programmer with an $\qquad$ to branch back to. Hence, the name of the instruction: "branch and link."
2. Provide the programmer with a way to load his initial base address into a g r -.

## BRANCH ON COUNT INSTRUCTION

address
general register

The next "branch" instruction you will study is used to control the number of times a program loop is executed. Read the description of the "branch on count" instructions in the Branching section of your Principles of Operation manual.

Just like the "branch on condition" and the "branch and link" instructions, the "branch on count" instruction can be in two formats. List them:
$\qquad$

RR BCT is the mnemonic for the RX format of "branch on count." The mnemonic for the $R R$ format is $\qquad$ _.

BCTR Like the BCR and BALR instructions, the BCTR instruction will not result in a branch if the $R 2$ field contains $\qquad$ .
zero The "branch on count" instruction (either BCT or BCTR) will always reduce the 1 st operand by a value of $\qquad$ -.
one $\quad$ The "branch on count" instruction will result in a branch if the 1st operand ___ (has/has not) been reduced to zero.

| has not | The reduction of the 1st operand occurs ___ (before/after) deciding <br> whether to branch. |
| :--- | :--- |
| before | 06 |

Assuming that register 7 contains a value of +1 , the above "branch on count" instruction (will/will not) result in a branch.
will not; This is because the BCT instruction will reduce register 7 by 1 before deciding whether or not to branch. This will bring the contents of register 7 to zero.


Assuming that register 7 contains a value of zero, the above "branch on count" instruction $\qquad$ (will/will not) result in a branch.
will; Since the register is reduced by 1 before testing for a branch, register 7 was reduced to a value of -1 and the branch did occur. In this case, the preceding instruction would have to be executed $2^{32}$ times before register 7 could be reduced to zero.

Examine the following program.


Assuming that 2000 is the address of the first instruction, how many times will the above program be executed? Circle one of the following:
a. 2000
b. 4000
c. 2002
d. 2004
e. None of the above
c; A value of 2002 was placed in register 11 by the first instruction. Each time the last instruction (BCTR) was executed, this value was reduced by 1 and a branch was taken back to the second instruction. On the 2002 nd time through the program, the contents of register 11 was reduced to zero by the BCTR instruction and a branch would not occur.

## BRANCH ON INDEX HIGH INSTRUCTION

The next "branch" instruction you will learn is "branch on index high." This is a complex instruction, so take your time. Read the description of this instruction in the Branching section of your Principles of Operation manual.

The "branch on index high" instruction has a mnemonic of $\qquad$ .

BXH The BXH instruction uses the RS format. Label the fields of the RS format.


| OP CODE | R1 | R3 | B2 | D2 |
| :--- | :--- | :--- | :--- | :--- |

As with the other "branch" instructions you have learned, the generated storage address ( B 2 and D 2 fields) is the $\qquad$ .
"branch to" location
The R1 field in the BXH instruction is the address of the $\qquad$ operand.

Normally the number in an instruction field specifies which operand it is. For example, R1 specifies the 1st operand. However, in the case of the BXH instruction, the R3 field is used to specify the $\qquad$ operand.
first second

The second operand is the R3 field register.
The third operand of a BXH instruction is also in a register. If the R3 field is even, the third operand is in the next odd-numbered register. That is, if the R3 field is 4 , the second operand is in register $\qquad$ and the third operand is in register $\qquad$ _.

4
5
If the R3 field of a BXH instruction is odd, the second and third operands are in the same register. That is, if the R3 field is 5 , the second operand is in register $\qquad$ and the third operand is also in register $\qquad$ .

5

5
Given the following "branch on index high" instruction, indicate the locations of the three operands.

| 86 | 4 | 6 | 0 | 100 |
| :---: | :---: | :---: | :---: | :---: |

1st operand is in register
2nd operand is in register
$\qquad$ .

3 rd operand is in register $\qquad$ -
$\qquad$


In the BXH instruction, the second operand is added to the 1 st operand and the sum is algebraically compared to the 3 rd operand. Given the above instruction, register $\qquad$ will be added to register $\qquad$ and the sum will be compared algebraically to register $\qquad$ .

| 4 | In the BXH instruction, the resulting sum replaces the first operand after |
| :--- | :--- |
| being compared with the |  |
| 5 |  |$\quad$| (1st/2nd/3rd) operand. |
| :--- |

1st Given the following, indicate (in hex) the contents of the registers after execution of the BXH instruction.

| 86 | 4 | 6 | 0 | 100 |
| :---: | :---: | :---: | :---: | :---: |

Everything in hex

|  | Before | After |
| :--- | :---: | :---: |
| Register 4 | 00000010 |  |
| Register 6 | FFFFFFFF |  |
| Register 7 | 00000008 |  |

Register $4 \quad 0000000 \mathrm{~F} \quad$ In the preceding problem, a value of -1 was added to a value of +16 Register 6 Unchanged and the sum of +15 replaced the 1 st operand.
Register 7 Unchanged

Given the following "branch on index high" instruction, indicate the locations of the three operands.


1st operand is in register 2nd operand is in register 3 rd operand is in register
$\qquad$ .
$\qquad$ -.
$\qquad$ -. 1 st and 2 nd operands always replaces the $\qquad$ (1st/2nd/3rd) operand.
$\qquad$
The sum of the 1 st and 2 nd operands is algebraically compared with the
$\qquad$ operand.

In an algebraic comparison, positive numbers are $\qquad$ (lower,' higher) than negative numbers.
higher In the "branch on index high" instruction, the branch occurs if the sum is higher than the $\qquad$ (1st/2nd/3rd) operand.

3rd

| 86 | 4 | 6 | 0 | 100 |
| :--- | :--- | :--- | :--- | :--- |


| Register 4 | 00000000 |  |
| :--- | :--- | :--- |
| Register 6 | 00000001 | In Hex |
| Register 7 | 00000010 |  |

In the above BXH instruction, a branch $\qquad$ (will/will not) occur.
will not

| 86 | 4 | 8 | 0 | 100 |
| :--- | :--- | :--- | :--- | :--- |

Register $4 \quad 00000000$
Register $8 \quad 00000010 \quad$ In Hex
Register 900000010

In the above BXH instruction, a branch $\qquad$ (will/will not) occur.
will not; This is because the sum is equal to but not higher than the third operand.

| 86 | 3 | 6 | 0 | 100 |
| :--- | :--- | :--- | :--- | :--- |


| Register 3 | 00000010 |  |
| :--- | :--- | :--- |
| Register 6 | 00000001 | In Hex |
| Register 7 | 00000010 |  |

In the above BXH instruction, a branch $\qquad$ (will/will not) occur.

| 86 | 3 | 8 | 0 | 100 |
| :---: | :---: | :---: | :---: | :---: |


| Register 3 | FFFFFFFF |  |
| :--- | :--- | :--- |
| Register 8 | FFFFFFFF | In Hex |
| Register 9 | 00000001 |  |

In the above BXH instruction, a branch $\qquad$ (will/will not) occur.
will not; The sum of registers 8 and 3 is

| 86 | 3 | 5 | 0 | 100 |
| :--- | :--- | :--- | :--- | :--- | a value of -2 . This is less than the +1 in register 9.


| Register 3 | 00000001 |  |
| :--- | :--- | :--- |
| Register 5 | 00000001 | In Hex |
| Register 6 | 00000002 |  |

In the above BXH instruction, a branch $\qquad$ (will/will not) occur.
will; Register 6 is not used in the preceding problem. The R3 field is odd. As a result, register 5 is used for both the 2 nd and 3 rd operands. The sum of registers 5 and 3 is a value of +2 , which, of course, is higher than the contents of register 5 .


| Register 3 | 00000010 |  |
| :--- | :--- | :--- |
| Register 5 | FFFFFFFF | In Hex |
| Register 6 | 000001 FF |  |

In the above BXH instruction, a branch $\qquad$ (will/will not) occur.
will; A 2nd operand of -1 is being added to a 1 st operand value of +16 and the sum of +15 is high compared to the 3 rd operand value of -1 .

Show in hex the contents of bits 40-63 of the PSW after the preceding instruction has been executed.


PSW


On a successful branch, the generated storage address replaces the instruction address portion of the PSW.

BRANCH ON INDEX LOW OR EQUAL INSTRUCTION

You are now ready to study the "branch on index low or equal" instruction. It is very similar to the BXH instruction. Read the description of this instruction (BXLE) in the Branching section of your Principles of Operation manual.

BXLE is the mnemonic for the " $\qquad$ on $\qquad$ or

## $\qquad$ " instruction.

"branch on index low or equal"

The BXLE instruction is similar to the BXH instruction in that the operand is added to the $\qquad$ operand and the sum is algebraically operand. compared to the $\qquad$
$\qquad$
Indicate the location of the operands in the following BXLE instruction.
1st
3rd

| 87 | 3 | 6 | 0 | 100 |
| :---: | :---: | :---: | :---: | :---: |

1st operand is in register $\qquad$ .
2nd operand is in register $\qquad$ .
3 rd operand is in register $\qquad$ .
does not With the BXLE instruction, a branch only occurs when the sum of 1st and 2nd operands is $\qquad$ or $\qquad$ compared with the 3rd operand.
low
equal

| 87 | 4 | 6 | 0 | 100 |
| :--- | :--- | :--- | :--- | :--- |


| Register 4 | 00000008 |  |
| :--- | :--- | :--- |
| Register 6 | 00000001 | In Hex |
| Register 7 | 00000010 |  |

In the above BXLE instruction, a branch $\qquad$ (will/will not) occur.
will; The sum is lower than the contents of register 7 .

| 87 | 5 | 5 | 0 | 100 |
| :--- | :--- | :--- | :--- | :--- |

Register 500000001 In Hex

When the same register is used for both the 1 st and 3 rd operands, the sum is compared with the original contents of the register. In the above BXLE instruction, a branch $\qquad$ (will/will not) occur.
will not; In this case, the same register is used for all three operands. The 3 rd operand is the original contents of reg 5 . Obviously, then the System/360 will have to bring the contents of this register into ALU (Arithmetic and Logic Unit) and store it in some register so its original contents will not be lost when the 1st and 2nd operands are added together. If at a later time, this instruction is executed again, the sum from the first execution would be used as the 3rd operand.

## EXECUTE INSTRUCTION

The "branch on condition, branch and link, branch on count, branch on index high, branch on index low or equal" instructions are the only actual "branch" instructions in the System/360. There is, however, another instruction called "execute" which does not change the instruction address in the PSW. However, it does cause one instruction in main storage to be executed out of sequence. That is, instead of branching from one routine to another, the "execute" instruction will cause one instruction in another routine to be executed without leaving the original routine.

Read the description of the "execute" instruction in the Branching section of your Principles of Operation manual.

## 14 Branching Operations

$\qquad$ " instruction.


No; The "execute" instruction is not a "branch" instruction. Instead, it causes an instruction to be executed that is not in the sequence presently being executed. In the previous program example, the "execute" instruction at 2052 caused the instruction at 8500 to be executed. Then the normal sequence of instruction execution continued with the instruction at 2056.

If the R1 field of the "execute" instruction is other than zero, the loworder byte of the specified register will be ORed with the $\qquad$ (1st/2nd) byte of the instruction to be executed.

If you are not familiar with the function of ORing and ANDing bits, go to the Principles of Operation manual. Read the OR and AND examples in the Instruction Use Examples area of the Appendix.

Given the following, write the instruction that is actually executed.


THE INSTRUCTION THAT IS ACTUALLY EXECUTED.


The instruction that was actually executed causes the contents of register $\qquad$ to be algebraically added to the contents of register $\qquad$ -.

10
15
The ORing of the 2nd byte of the instruction with the low-order byte from the register is done in the ALU. As a result, the instruction in storage
$\qquad$ (remains the same/is changed).
remains the same
Given the following, write the instruction that will be executed in ALU. Remember that the bytes are ORed!


| $1 A$ | $A$ | $B$ |
| :---: | :---: | :---: |

Bits 24-31 of register 1 are ORed with bits $8-15$ of the AR instruction as shown below.


| $\mathbf{A}$ | $\mathbf{B}$ |
| :--- | :--- |

As a result of the instruction shown in the previous example, the "execute" instruction would cause (via the "add" instruction) the contents of register $\qquad$ to be added to contents of register $\qquad$ .

11
10

Write the AR instruction that remains in storage as a result of the instruction in the preceding example.


There are three programming interrupts possible with an "execute" instruction.

1. Specification exception
2. Addressing exception
3. Execute exception

A specification exception can occur on an "execute" instruction if the generated effective address of the instruction to be executed is $\qquad$ (odd/even).
odd; Remember that all instructions must start on an even address.

An addressing exception can occur on an "execute" instruction if the generated effective address of the instruction to be executed $\qquad$ (is/is not) available on the particular System/360 installation.
is not
An execute exception can occur on an "execute" instruction if the system is directed to another " $\qquad$ " instruction.
"execute"


The above "execute" instruction will result in a(n) $\qquad$ exception.
specification; The generated address is odd.


The above "execute" instruction will result in a(n) $\qquad$ exception.
execute


The above "execute" instruction will probably result in a(n) $\qquad$ exception.
addressing

Choose the correct branching instruction mnemonic from the list on the right and write it next to the proper instruction name.

| NAME | MNEMONIC |  |
| :---: | :---: | :---: |
| Branch on Condition $=$ | $\underline{\mathrm{BC}} \mathrm{BCR}$ | BXH |
| Branch and Link = |  | BCTR |
| Branch on Count = |  | BALR |
| Branch on Index High = | - | EX |
| Branch on Index Low or Equal = | - | BXLE |
|  |  | BCT |
| Execute = | - | BAL |


| BC | BCR | Go to the IBM System $/ 360$ Principles of Operation manual and study the |
| :--- | :--- | :---: |
| BAL | BALR | following areas of the Branching section. |
| BCT | BCTR | Decision-Making |
| BXH | Instruction Formats |  |
| BXLE | Branching Instructions |  |
| EX | Branching Exceptions |  |

# System/360 Branching,Logical and Decimal Operations 

Section I: Branching Operations<br>- Section II: Logical Operations<br>Section III: Decimal Operations<br>Section IV: Analyzing Decimal Feature Programs<br>SECTION II LEARNING OBJECTIVES

At the end of this section, you should be able to do the following when given the mnemonic of any logical instruction.

1. State instruction length and format.
2. State location and format of operands.
3. Determine the result and where it will be located.
4. State effect on condition code.
5. State which program checks are possible.

## Logical Operations

This section of the text covers the group of instructions known as the logical operations. These "logical" instructions allow you to move data around in storage, compare alphameric data, AND and OR two data fields, and also allow you to do other miscellaneous operations. The "logical" instructions use all give instruction formats and work with both fixed and variable length data fields. Read the following introductory material in the Logical Operations section of your Principles of Operation manual.

## Logical Operations <br> Data Format <br> Condition Code <br> Instruction Format <br> Instructions

A number of the instructions in the Logical Operations section are not covered in this section of your self-study text. They include the four "logical shift" instructions (which you learned earlier in your text on Fixed Point Binary Operations) and the two "edit" instructions which are part of the Decimal Feature on System/360. The two "edit" instructions are covered later in this self-study text in the Decimal Operations section.

MOVE INSTRUCTION

Read the description of the following instructions in the Logical Operations section of your Principles of Operation manual.

| Mnemonic | Descriptive Title |
| :--- | :--- |
| MVI | Move Immediate |
| MVC | Move Characters |

The "move immediate" instruction uses the SI format. Label the fields of the SI format.


| OP CODE | 12 | B1 | D1 |
| :---: | :---: | :---: | :---: |

Operands that are carried in the instruction itself are called operands.
immediate
In the MVI instruction, the immediate operand is one $\qquad$ long and is the $\qquad$ (1st/2nd) operand. The instruction will move the byte of immediate data to main $\qquad$ -
byte
2nd
storage

The MVI instruction will cause the byte in main storage to be replaced by a byte from the $\qquad$ . The main storage address $\qquad$ (does/does not) have to be even.

The MVI instruction can move $\qquad$ (more than one/only one)
instruction
does not; Any byte in main storage can be addressed. byte of data.
only one; Only the immediate byte in the instruction.

Given the following (in hex) show the contents of main storage after the MVI instruction is executed.


| 00 | FA | 00 | 00 | 00 |
| :--- | :--- | :--- | :--- | :--- |

MVI is the mnemonic for the move immediate. MVC is the mnemonic for
$\qquad$
$\qquad$ —.
move characters
The MVC instruction uses the SS format because both operands are
$\qquad$ (fixed/variable) length fields in main storage.

The MVC instruction moves bytes (characters) from one area of main storage to another. The number of characters is determined by the 2nd byte of the MVC instruction. This byte is called the $\qquad$ field.

## L1

The length code (L1) can represent a count of from zero to $\qquad$ . Since the number of bytes in a field is equal to the length code +1 , a length code of zero would mean $\qquad$ byte.

A length code of 255 in the MVC instruction would cause $\qquad$ bytes to one be moved.


As in most System/ 360 operations, the 1 st operand receives the results. In the above MVC instruction, $\qquad$ bytes would be moved from location
$\qquad$ to location $\qquad$ .

256
3840
2048

Given the following, show the contents of the indicated storage area after the MVC instruction is executed. Everything is shown in hex.


| $\mathrm{C1}$ | C 2 | $\mathrm{C3}$ | $\mathrm{C4}$ | $\mathrm{C5}$ | $\mathrm{C6}$ | $\mathrm{C7}$ | CB | $\mathrm{C9}$ | CA |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

2048

| $F O$ | $F O$ | $F O$ | $F O$ | $F O$ | $F O$ | $F O$ | $F O$ | $F O$ | $F O$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

3840


2048


The bytes moved by the MVC instruction: (Circle one of the following)
a. Must be packed decimal data.
b. Must be in the halfword signed binary format.
c. Can be in any format.
d. Must be EBCDIC characters.
c; The bytes that are moved are not checking for coding. The title of the instruction (move characters) implies, however, that this instruction could be used to move EBCDIC characters from one area of storage to another. For instance, data could be moved from an input area to a work area without being changed. After the data has been processed in a work area, it could be moved to an output area.

The following drawing illustrates this point.


Because the bytes are moved one at a time, the MVC instruction can also be used to propagate one character throughout an area. Given the following, show the resulting storage contents.



In the preceding problem, the following occurred:
1st; The instruction looks at the first location (2048), finds the 00 and moves it to 2049 where it replaces the F1.

2nd; The instruction looks at the next location (2049), finds the 00 and moves it to 2050.
3 rd ; The leftmost byte continues to be moved (propagated) to the right.

## MOVE NUMERICS INSTRUCTION

$\qquad$
Read the description of the "move numerics" instruction in the Logical Operations section of your Principles of Operation manual.

|  | MVN is the mnemonic for the " |  |  |  |  |  |  | " instruction. |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| "move numerics" | The MVE instruction moved the entire byte from the 2nd operand. <br> The MVN instruction only moves bits $\qquad$ (0-3/4-7). |  |  |  |  |  |  |  |  |  |
| 4-7 | The MVN instruction moves bits $4-7$ of each byte from the $\qquad$ (1st/ 2 nd ) operand to bits 4-7 of the $\qquad$ (1st/2nd) operand. |  |  |  |  |  |  |  |  |  |
| 2nd | Given the following, show the resulting contents of the 1 st operand. |  |  |  |  |  |  |  |  |  |
|  | c 1 | c2 | c3 | c 4 | c5 | c6 | c7 | c 8 |  |  |
| 4 |  |  |  |  |  |  |  |  |  |  |
| MVN |  |  |  |  |  |  |  |  |  |  |
|  | D |  | 07 | 0 |  | 80 |  | 0 | FOO |  |
|  | 1 ST OPERAND $\longleftarrow$ |  |  |  |  |  |  |  |  |  |
|  | Fo | Fo | Fo | Fo | Fo | Fo | Fo | Fo | BEFORE |  |
|  | $20_{4}^{4} 8$ |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  | AFTER |  |


| F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Given the following, show the resulting contents of the main storage area.


The numeric portion of the leftmost byte was moved (propagated) to the right, byte by byte, 7 times.

## MOVE ZONES INSTRUC TION

$\qquad$

Read the description of the "move zones" instruction in the Logical Operations section of your Principles of Operation manual.

MVZ is the mnemonic for the " $\qquad$
$\qquad$ " instruction.
$\qquad$
"move zones" The MVN instruction moved bits 4-7 of each byte from the 2 nd operand to the $1 s^{2}$ operand.

The MVZ instruction moves bits $\qquad$ through $\qquad$ .

0, 3 Just like the MVC and MVN instructions, the MVZ instruction processes the data field from left-to-right, one $\qquad$ at a time.
$\qquad$

26 Logical Operations

Given the following, show the resulting contents of the 1st operand.


| $F 1$ | $F 2$ | $F 3$ | $F 4$ | $F 5$ | $F 6$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

Given the following, show the resulting contents of the 1 st operand.


AFTER


The zone portion of the leftmost byte was moved (propagated) to the right.

Assume that the MVN, MVC or MVZ instruction has a 1st operand address that is one higher than the 2 nd operand address. The corresponding numerics, character, or zones of the first byte from the 2 nd operand will be propagated to the $\qquad$ (left/right).

b; The protection key in the PSW being zero will allow the data to be stored and a protection exception will not result.

If a generated storage address in the preceding group of "move" instructions is not available, an $\qquad$ exception will occur.

| addressing | The two programming exceptions possible on the "move" instructions are |
| :--- | :--- |
| protection <br> addressing | The "move" instructions <br> condition code. |

do not change Let's take a look at a few symbolic programming examples using the instructions you have learned. First let's review the RR, RX, and RS formats.

| Format | Symbolic |  | Example |  |
| :---: | :--- | :--- | :--- | :--- |
|  |  | Mnemonic R1, R2 | AR | 2,3 |
| RX |  | Mnemonic R1, D2 (X2, B2) | AH | $2,1000(0,3)$ |
| RS | Mnemonic R1, R3, D2 (B2) | BXH 2, 4, 1000 (3) |  |  |

The SI format will be shown like this:

$$
\text { Mnemonic } \quad \mathrm{D} 1(\mathrm{~B} 1), \mathrm{I} 2
$$

Such as:
MVI $2048(0), 0$
The preceding would look like this in actual machine language:

| 92 | 00 | 0 | 800 |
| :---: | :---: | :---: | :---: |

$$
\text { MVI } \quad 2048(0), 0
$$

Show the binary bit structure of the byte placed in location 2048 after the execution of the above instruction. $2048=$ $\qquad$

00000000 MVI 4095 (0), 255
The above instruction would cause a binary bit structure of $\qquad$ to be placed in location $\qquad$ .

11111111 4095

The SS format will be shown like this:

| Mnemonic | D1 (L, B1), D2 (B2) |
| :--- | :--- |
| MVC | $2048(8,0), 3840(0)$ |

The preceding instruction would look like this in actual machine language.

| 02 | 07 | 0 | 800 | 0 | $F 00$ |
| :--- | :--- | :--- | :--- | :--- | :--- |

Notice that the length code in the symbolic example showed the number of bytes while the length code in machine language is one less than the total number of bytes.

$$
\text { MVC } \quad 2048(16,0), 3840(\theta)
$$

The above instruction would cause the bytes in locations $\qquad$ through
$\qquad$ to be moved to locations $\qquad$ through $\qquad$ .

3840, 3855
2048, 2063

Given the following, show the resulting contents of the storage area.

| MVI | $2048(0), 0$ |
| :--- | :--- |
| MVC | $2049(7,0), 2048(0)$ |



| 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

In the preceding problem, the MVI instruction placed a byte of all zero bits in location 2048. Then the MVC instruction propagated this byte into the seven bytes to the right (2049-2055).

## COMPARE LOGICAL INSTRUCTION

You learned three "compare" instructions when you were studying the fixed point instructions. Their mnemonics are:

| CR | Compare, RR format |
| :--- | :--- |
| C | Compare, RX format |
| CH | Compare Halfword, RX format |

These three "compare" instructions compared on an algebraic basis. In other words, they treated the operands as signed binary integers. The operands were either positive or negative numbers. The "compare logical" instructions you will now learn also treat the operands as binary information. However, they will be considered as unsigned binary fields. For example, consider the comparison of the following binary fields on an algebraic basis.


Because the 1st operand is a positive number (+1) and the 2 nd operand is a negative number ( -1 ), the 1 st operand is high and the PSW condition code would be set to $\qquad$ _.

If the same fields were compared on a logical basis, they would be treated as unsigned integers and the absolute values would be compared as follows:
\(\left.\begin{array}{l}Compare <br>

Logical\end{array}\right\}\)| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |$\quad$| 1st Operand |
| :--- |
| 1 | 1 |  | 1 | 1 | 1 | 1 | 1 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |$\quad$ 2nd Operand

In the above example, the 1 st operand would compare low and the PSW condition code would be set to $\qquad$ . This occurs because an unsigned value of 1 is being compared with an unsigned value of 255 .

01
The programmer must know what format his data is in before he can compare it. If his data consists of signed binary words or halfwords, he would use his three "algebraic" instructions: CR, C, CH. If his data consists of unsigned binary fields, he would use the "logical" instructions. As a point of interest, the EBCDIC code is so arranged that the special and alphameric characters will collate on a binary basis. That is, the "compare logical" instructions are used to compare EBCDIC characters.

Let's look at the bit sequence of the EBCDIC characters.
Write the EBCDIC code for the character "A." $\qquad$

Write the EBCDIC code for the character " Z ." $\qquad$

11101001 |  | "A" | 11000001 |
| :--- | :--- | :--- |
|  | "Z" | 11101001 |

On a compare logical basis, which is low? $\qquad$ ("A" or "Z")

"A" | "1" | 11110001 |
| :--- | :--- |
|  | "Z" |
|  | 11101001 |

On a compare logical basis, which is low? $\qquad$ ("1" or "Z")
"Z"
"\#"
"A"

On a compare logical basis, which is low?
"\#"
The preceding examples should agree with the collating sequence you are familiar with in your past experience with punched card equipment or equipment which used the standard BCD code (BA 8421). This is illustrated as follows:


You now have an idea of the difference between algebraic and logical comparisons. You can also see when they are used. Read the descriptions of the "compare logical" instructions in the Logical Operations section of your Principles of Operation manual.

CL is the mnemonic for $\qquad$ .
compare logical
The CL instruction uses the RX format. CLR is the mnemonic for the "compare logical" instruction that uses the $\qquad$ format.

RR
In both the CL and CLR instruction, the 1st operand is the register specified by the $\qquad$ field. The instructions cause a $\qquad$ (logical/algebraic) comparison. As a result of the comparison, the is set.

R1
logical
The condition code settings of $00,01,10$ indicate that the $\qquad$ (1st/2nd) condition code operand is equal, low, or high compared to the $\qquad$ (1st/2nd) operand. After a compare operation, it is impossible to have a condition code of
$\qquad$ -

1st
2nd
11

Given the following CLR instruction, indicate the resulting condition code bits in the PSW.


Condition Code $=$

01 ; If the CR (compare algebraic) instruction had been used, the 1st operand would have been high.

Given the following $C L$ instruction, indicate the resulting condition code.


Condition Code $=$ $\qquad$

10; By examining the four high-order bits, you can see that the 1st operand is high.
1st operand - 1000
2nd operand - 0111

Besides the CLR and CL instructions, System/360 can also compare logical using the SI and SS formats. CLI is the mnemonic for the " $\qquad$ _ " instruction.

| "compare logical | The "compare logical immediate" instruction uses the SI format. In this <br> format, the 1st operand is in <br> imstruction). |
| :--- | :--- | _-.



LOCATION 2048

In the above CLI instruction, the 1st operand is $\qquad$ (low/high) and the resulting condition code is $\qquad$ _.
low
01 ; In the SI format, the 1st operand is in main storage.


In the above CLI instruction, the 1st operand is $\qquad$ (low/high) and the resulting condition code is $\qquad$ .
$\qquad$
high The CLR and CL instructions compare one (byte/word/half-
10 word) of data with another.

The CLI instruction compares one $\qquad$ (byte/word/halfword) of data with another.

| word <br> byte | The compare logical operation can also be done with the ___ (SS/RS) <br> format. |
| :--- | :--- |
| SS | CLC is the mnemonic for the "compare logical" instruction which uses <br> the format. |
| SS | CLC means Compare Logical Characters. This instruction has an 8-bit <br> length code and can compare up to |

$\qquad$

The name of the CLC instruction indicates that characters are being compared. Actually, bytes are being compared on an unsigned binary (logical) basis. As was previously pointed out, however, the EBCDIC code assigned to characters is arranged so that they will collate on a binary basis.


In the above CLC instruction, $\qquad$ character(s) will be compared and the condition code will be set to $\qquad$ .
two; One from each operand. 01

The coding of the byte at location 2048 above could represent the EBCDIC character " $\qquad$ ".
"G"; Because hex
C7 = bits 11000111
which equal the
EBCDIC "G."

The coding of the byte at location 2049 could represent the EBCDIC character " $\qquad$ ."
"M" The coding of the byte at location 2050 could represent the EBCDIC character " $\qquad$ ."
"X" The coding of the byte at location 2051 could represent the character " $\qquad$ ."

## "4"



$$
\begin{array}{lll}
\text { LOCATIONS 2048-2051 JOHN } \\
\text { LOCATIONS 2052-2055 } & \text { LUKE }
\end{array}
$$

Given the above characters and CLC instruction, the condition code will be set to $\qquad$ .

01 ; In the preceding problem, JOHN was the 1 st operand and LUKE was the 2nd operand. The highorder character ( $J$ ) of the 1st operand was lower than the high-order character ( L ) of the 2nd operand.

$$
\begin{aligned}
& \text { "J" - } 11010001 \\
& \text { "L" - } 11010011
\end{aligned}
$$

| 05 | 07 | 0 | 800 | 0 | $F 00$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

$$
\begin{array}{lll}
\text { LOCATIONS } 2048-55 & - & \text { JOHNSTON } \\
\text { LOCATIONS } 3840-47 & - & \text { JOHANSEN }
\end{array}
$$

Given the above characters and CLC instruction, the condition code will be set to $\qquad$ .

10; On the first three high-order characters (JOH), both operands are equal. On the fourth character, the 1st operand will compare high as follows:

| 1st operand | - $N "-11010101$ |  |
| :--- | :--- | :--- | :--- |
| 2nd operand | - | " $"$ - 11000001 |


|  | You should now realize that the comparing is done for all practical purfose <br> from <br> (left to right/right to left). |
| :--- | :--- |
| left to right | As a result of comparing the bytes from left to right, it is not necessary to <br> examine the entire field. The compare operation assumes that the fields <br> are equal to begin with. In examining the bytes from left to right, the <br> system can end the compare operation as soon as it finds an u <br> condition. |
| unequal | List the mnemonics and the instruction formats of the four "compare <br> logical" instructions. |



The CR instruction will treat the contents of a particular register as a signed integer (sign and 31 bits). The CLR instruction treats the contents of the same register as an unsigned 32-bit integer. As a result, the condition code setting may vary, depending on the instruction used.

Given the contents of the following two registers, indicate the resulting condition code for the instruction shown.

a.

b.

$\qquad$
a. 01 - Reg 2 has a negative number.
b. 10 - Reg 2 has a higher value.

Assume that a card record punched in standard hollerith card code has been read in main storage. The record contained alphabetic characters. To compare two fields in this record, which would you do? $\qquad$ (compare logical/compare algebraic).

Given two fields of zoned decimal data, what would you do? (Circle one of the following.)
a. Compare Algebraic
b. Compare Logical
c. Neither of the above
c ; See the following for explanation.


Normally, the "compare logical" instruction is used to compare alphameric information. However, a zoned decimal field presents a special problem. Assume we wish to compare a +11 with a -11 . The +11 should be high but look below.


As you can see above, the minus sign bits (due to the 11 -hole card punch) would cause the negative number to be high. The plus sign bits (1100) are, of course, due to a 12-hole card punch.

You have now been shown a problem without a solution. One solution, of course, would be to change (via instructions) the data to the binary format and use the "compare algebraic" instruction. Another solution is to place the data (via the "pack" instruction) in the packed format. Then you can compare decimal. We will be covering this instruction later on in this textbook.

Right now, we will continue with more "logical" instructions. The next group of instructions you will study can truly be called "logical" instructions. They allow the programmer to mix data fields together on a basis of AND, OR, as well as Exclusive OR logic.

The "and" instruction is used to mix two operands on a logical AND basis. The definition of an AND condition is this: If both bits are 1, the resulting bit is 1. Otherwise, it is zero.

The following will illustrate the result of ANDing two bytes together.
BIT POSITIONS
$\begin{array}{llllllll}0 & 1 & 2 & 3 & 4 & 5 & 6 & 7\end{array}$
1st Operand
2nd Operand
Result $\quad 101010100$

Notice that only in bit positions 0 and 4 were both bits set to 1 . As a result, only bits 0 and 4 of the result are 1 . As in most System/360 operations, the result will replace the 1st Operand.

Given the following two bytes, show the result after they are ANDed together.

| 1st Operand | 011110110 |
| :--- | :--- |
| 2nd Operand | 110011100 |

Result

01000100 ; Notice again that the operands are ANDed together on a bit-by-bit basis. There is no connection (carry) from one bit position to another.

Show the result of the following AND operation.

| 1 st Operand | 11000011 |
| :--- | :--- |
| 2nd Operand | 10000001 |

Result

In a typical user's program, the programmer will occasionally use data as a programmable switch. That is, in a flowchart, a branch decision will occasionally be based on whether a switch is on or off.

For example:


Notice that switch A is used to determine whether to read a card or punch a card. Also, notice that the flowchart assumes that there is a method of turning the switch on and off.

One use of the "and" instruction is to turn off program switches.

0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Assume that bit position 7 of the byte shown above represents a program switch. In order to turn off this program switch, bit position 7 of the second operand must be $\qquad$ (1/0).

0 ; See below.

| 1st Operand |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 2nd Operand |  |  |  |  |  |  |  |  |
| Result | 01100000 | 1 | 1 |  |  |  |  |  |
|  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
|  | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

Since a byte contains 8 bits it can hold $\qquad$ program switches. A word can contain $\qquad$ program switches.

It is desired to turn off one program switch in a byte without affecting the other switches. Show the 2nd operand necessary to turn off only the switch in bit position 6 .

1st Operand $\quad 10110110$
2nd Operand
Result
10110100

11111101 ; Notice that It is desired at the beginning of the program to be sure that all of the only bit position 6 was program switches are off. Show the necessary 2 nd operand. changed. This 2nd operand would work with any 1 st operand and still turn off only position 6 .

1st Operand 0110001008 program switches 2nd Operand $\qquad$

00000000
Now that you can turn off program switches, how about turning them on?

The "and" instructions can be used to turn off program switches. The "or" instructions can be used to turn on program switches. The definition of an OR condition is this: If either bit is 1 , the resulting bit is 1. Otherwise, it is zero.

The following will illustrate the result of ORing two bytes together.

| 1 st Operand | 10101010 |
| :--- | :--- |
| 2nd Operand | 10011100 |
| Result | 10111110 |

Notice that only in bit positions 1 and 7 neither bit was set to 1 . Consequently, only bits 1 and 7 of the result are set to 0 . The remaining bits contain a 1.

Given the following operands, show the result if they are ORed together.
1st Operand 01110110
2nd Operand $\quad 11001100$
Result
$11111110 \quad$ Show the result of the following OR operation.
1st Operand $\quad 11000011$
2nd Operand $\quad 10000001$
Result

Assume that bit position 7 of the byte shown above is a program switch. In order to turn on this program switch, bit position 7 of the 2 nd operand must be $\qquad$ (0/1).

1; See below.

| 1 st Operand | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 2nd Operand |  |  |  |  |  |  |  |  |
| Result | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |$\quad$|  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

It is desired to turn on one program switch in a byte without affecting the others. Show the necessary 2nd operand to turn on only the switch in bit position 2.

1st Operand 11010110
2nd Operand

Show the result of ORing the previous answer with the 1 st operand.

| 1 st Operand | 11010110 |
| :--- | :--- |
| 2nd Operand | $\underline{0} 0100000$ |

Result

11110110
It is desired at the beginning of a program to be sure that all of the program switches are initially on. Show the necessary 2 nd operand.

| 1st Operand | $0.1100010 \quad 8$ program switches |  |
| :--- | :--- | :--- |
| 2nd Operand |  |  |

## AND INSTRUCTION - OR INSTRUCTION

11111111 Read the description of the "and" and "or" instructions in the Logical Operations section of your Principles of Operation manual.

The mnemonic of the "and" instruction uses the letter $\qquad$ -

The mnemonic of the "or" instruction uses the letter $\qquad$ .

| N | Both the "and" and "or" instructions can use four formats. Use the <br> following mnemonics and indicate the instruction format and whether it <br> is an "and" or "or" instruction. |
| :--- | :--- | :--- |
| O |  |

a; The condition code reflects the status of the entire result. It can either be zero or non-zero.

Given the following, show the contents of the registers after the instruction is executed.



Given the following, show the contents of the instruction and the storage byte after the instruction is executed.

$\qquad$


Given the following, show the storage contents after the instruction is executed.


| Location | Before | After |
| :---: | :---: | :---: |
| 2048 | DE |  |
| 2049 | A0 |  |
| 2050 | 7 F |  |
| 2051 | 8B |  |
| 2052 | 9 E |  |
| 2053 | 01 |  |
| 2054 | 72 |  |
| 2055 | F1 |  |


| Location |  | After |
| :--- | :--- | :--- |
|  | 2048 |  |
| DE |  |  |
| 2049 |  | A1 |
| 2050 |  | 7 F |
| 2051 |  | FB |
| 2052 |  | 9 E |
| 2053 |  | 01 |
| 2054 |  | 72 |
| 2055 |  | F1 |

Given the following "or" instruction, show the contents of register 0 and the condition code after the instruction is executed.


2052 9E
2053 01

2055 F1


IN HEX
LOCATION CONTENTS

|  |  | 2048 | 80 |
| :---: | :---: | :---: | :---: |
|  |  | 2049 | 7E |
|  |  | 2050 | 01 |
|  |  | 2051 | F0 |
|  | AFTER |  |  |

Condition Code $=$ $\qquad$

## EXC LUSIVE OR INSTRUCTION

Reg 0 807FB1FF

Condition Code 01

So far you have had a good look at the "and" and "or" instructions. You have seen how they can be used to turn on and turn off program switches. Another instruction that can be used to alternately turn on and turn off a program switch is the "exclusive or" instruction. The definition of an Exclusive OR condition is this:

If one and only one of the bits is 1 , the result is 1 . Otherwise, it is zero.

The following will illustrate the result of Exclusive ORing two bytes.

| 1st Operand | 0101010 |
| :---: | :---: |
| 2nd Operand | 10011100 |
| Result | 00110 |

Notice that in bit positions 2, 3, 5 and 6 one and only one of the bits was a 1. So only these positions of the result have a 1 . In bit position 0 , both bits were 1 and the result was 0 . In bit position 1 , both bits were 0 and the result was 0 .

Given the following operands, show the result of Exclusive ORing them.

| 1st Operand | 01110110 |
| :---: | :---: |
| 2nd Operand | 11001100 |
| Result |  |

$10111010 \quad$ Show the result of the following Exclusive OR operation.

| 1st Operand | 11000011 |
| :--- | :--- |
| 2nd Operand | 10000001 |

Result
$01000010 \quad$ It is desired to change only one program switch in a byte without affecting the others. Show the 2nd operand necessary to change only the switch in bit position 3 .

1st Operand $\quad 11010011$
2nd Operand


Assume that bit position 7 of a byte is a program switch. In order to change the setting of this program switch, bit position 7 of the 2 nd operand must be (0/1).

1; See below.
1st Operand
2nd Operand

Result $\quad$| 0 | 1 | 0 | 0 | 0 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | 1110

Read the description of the "exclusive or" instructions in the Logical Operations section of your Principles of Operation manual.
$\qquad$
The letter X is used for the mnemonic of an " $\qquad$ " instruction.
"exclusive or" Like the "and" and "or" instructions, the "exclusive or" instruction uses ( $1 / 2 / 3 / 4$ ) formats.

4
List the mnemonics and formats of the four "exclusive or" instructions.

| Mnemonic | Format |
| :--- | :--- |
| - | - |
| - | - |


| Mnemonic |  | Format |
| :--- | :--- | :--- |
|  |  | $R R$ |
| X |  | $R X$ |
| XI |  | SI |
| XC |  | SS |

Just like the "and" and "or" instructions, the "exclusive or" instruction will cause the condition code to be set to $\qquad$ (00/01/10/11) for an allzero result.

For a non-zero result, the "exclusive or" instruction will set bits 34-35 of the PSW to $\qquad$

## TEST UNDER MASK INSTRUCTION

01
So far, you can turn off, turn on, or change a program switch by use of the "and, or, exclusive or" instructions, respectively. However, you still can't test them. The "branch on condition" instruction is not sufficient. This instruction will only let you find out if all switches are either on or off. To be able to test a specific switch (or some but not all switches) will require another instruction. This instruction is known as "test under mask." The "test under mask" instruction will let you examine specific bits (program switches) and set the condition code accordingly. Then the "branch on condition" instruction can be used effectively.

Read the description of the "test under mask" instruction in the Logical Operations section of your Principles of Operation manual.

TM is the mnemonic for " $\qquad$
$\qquad$
$\qquad$ ."
"test under mask"
The TM instruction uses the $\qquad$ format. The instruction can be used to test program switches. These switches must be in $\qquad$ (main storage/general registers).

SI main storage

The "test under mask" instruction will test one $\qquad$ (byte/halfword/ word).
byte A byte can contain 8 program switches. The TM instruction can test _ (only one/all) of them at one time.
all
The TM instruction can, if desired, test as few as $\qquad$ program switch(es) at a time.
one The bits (program switches) to be tested with the TM instruction are determined by the instruction's $\qquad$ field.

I2
The I2 field corresponds bit-by-bit with the main storage byte to be tested. If all bits in the main storage byte are to be tested, the 12 field must contain (in hex).

FF To test only bit position 0 , the I2 field of the TM instruction must contain
$\qquad$ (in hex).

## 48 Logical Operations

The function of the TM instruction is to set the condition code. A condition code of 00 would indicate that all of the selected bits are zero. Assume that the I2 field of a TM instruction is FF. A condition code of 00 would indicate that the storage byte contains $\qquad$ (in hex).

00; An I2 field of FF
If a TM instruction results in a condition code of 11 , it would indicate that would test all bits. A condition code of 00 all of the selected bits are one. If the I2 field of the instruction used contained FF, it would mean that the storage byte contains $\qquad$ (in hex). would then indicate that all bits of the byte are zero.

## FF

A condition code of 01 is also possible after executing a TM instruction. This condition code (01) would indicate that some but not all of the selected bits contain a one. Given the following, what would the resulting condition code be?


Condition Code $=$ $\qquad$

01 After executing a TM instruction, it is not possible to have a condition code of $\qquad$ .

10


The above "test under mask" instruction would result in a condition code of $\qquad$ .

00

| 91 | 13 | 0 | 800 |
| :---: | :---: | :---: | :---: |

The above TM instruction would result in a condition code of $\qquad$ .
$\left.\begin{array}{|c|c|c|c|c|c|}\hline 91 & 0 & 800 & \text { LOCATION } 2048 & 6 A\end{array}\right]$

The above "test under mask" instruction would result in a condition code of $\qquad$ _.


The above TM instruction would result in a condition code of $\qquad$ .

00

| 91 | 10 | 0 | 800 |
| :---: | :---: | :---: | :---: |

The above TM instruction would result in a condition code of $\qquad$ .

At this point, you can turn program switches on and off. You can also test them. The instructions that you have been using can be used for purposes other than program switches.

The "and, or exclusive or" instructions can also be used to examine records for specific requirements. Consider the case of a program where it is desired to find all employees whose qualifications fit a particular job description. The following byte will show the minimum requirements for the job.


According to the preceding requirements, the employee must have a
$\qquad$ degree. However, he does not need to be an $\qquad$ or an $\qquad$ .


With the TM instruction, the condition code is set according to the status of the selected bits. To meet the minimum requirements, the selected bits in the employee's qualifications must be all (ones/zeroes).
ones If the selected bits are all ones, the TM instruction would cause the condition code to be set to $\qquad$ (00/11).

11
The TM instruction could then be followed by a "branch on condition. " Write the mask field necessary for a successful branch when the employee meets the minimum requirements. If necessary, review the BC instruction mask field on page 3 of this book or in the Principles of Operations manual.


IN HEX


[^1]Now suppose that a branch is not desired when the employee meets the minimum requirements. Write the necessary mask field in the $B C R$ instruction.

TM

| 91 | $E 4$ | 0 | 800 |
| :--- | :--- | :--- | :--- |

BCR

| 17 | 1 |
| :--- | :--- | :--- |

$\mathrm{E} \longleftarrow \mathrm{Hex} ; \quad 1110 \longleftarrow$ Binary
Since a condition code of 10 is not possible after a "test under mask" instruction, the following could also be used for the mask field:

$$
C \leftarrow \text { Hex; } \quad 1100 \longleftarrow \text { Binary }
$$

Suppose that we now change the conditions. We have been looking for an employee who meets the minimum requirements. We did not care if he exceeded those requirements.

Given the following requirements, circle those employees who at least meet the minimum requirements.


Employee A
Employee B
Employee C
Employee D
Employee E

11101000
11000110
11101100
11110100
11100000

Employee C
Employee D

Referring to the preceding problem, did any of the employees meet the minimum without exceeding the minimum requirements?

The "exclusive or" instruction can be used to find those employees who meet but do not exceed the minimum requirements. This is shown as follows:


Given the above "exclusive or" instruction and the qualifications of Employee C, the condition code will be set to $\qquad$ (00/01).
$01 \longleftarrow$ Indicates a non-zero result. This is shown as follows:


If employee $C$ had met without exceeding the minimum requirements, the condition code would have been set to $\qquad$ (00/01).
$00 \longleftarrow$ Indicates a zero result.

You have been studying the "and, or, exclusive or and test under mask" instructions. You have seen that their usage is not limited to program switches. Let's continue our study of logical instructions.

## INSERT CHARAC TER - STORE CHARACTER INSTRUCTIONS

The two instructions that you will study next are the "insert character" and "store character" instructions. Read the description of these instructions in the Logical Operations section of your Principles of Operation manual.

IC is the mnemonic for the " $\qquad$ " instruction.

STC is the mnemonic for the " $\qquad$ " instruction.
"insert character"
"store character"

RX
do not change
byte
Both the IC and STC instructions use the $\qquad$ instruction format. These instructions $\qquad$ (change/do not change) the condition code.

The IC and STC instructions use a storage-to-register concept. These two instructions transfer one $\qquad$ (byte/halfword/word) of data.

The "insert character" instruction will place the storage operand in bits through __ of the specified register.

24, 31; The low-order The remaining bits (0-23) of the specified register: (Circle one) byte.
a. Are zeroed out.
b. Remain unchanged.
b
Given the following IC instruction, show the resulting contents of the specified register.


47 A B 0 F A 6
Was the condition code changed by the preceding instruction? $\qquad$

No The "store character" instruction will place in the storage operand the contents of bits $\qquad$ through $\qquad$ from the specified register.

Given the following STC instruction, show the resulting contents of the storage location.


17
If the address of the storage operand is not available on the particular installation, an $\qquad$ exception will be recognized.
addressing
Any instruction that changes the contents of main storage is subject to the storage protection feature. As a result, the $\qquad$ (IC/STC) instruction can cause a protection exception.

STC
A protection or addressing exception will cause a $\qquad$ interrupt.

## LOAD ADDRESS INSTRUC TION

program Read the description of the "load address" instruction in the Logical Operations section of your Principles of Operation manual.
$\qquad$
LA is the mnemonic for the " $\qquad$
$\qquad$ " instruction.
"load address" The LA instruction has an Op code of 41 (in hex). From bits 0-1 of this Op code you can tell that it uses the $\qquad$ format.

| RX | Bits 0-1 of Op Code | Format |
| :---: | :---: | :---: |
|  | 00 | RR |
|  | 01 | RX |
|  | 10 | RS, SI |
|  | 11 | SS |

The "load address" instruction will place in the specified register: (Circle one of the following.)
a. A word from main storage.
b. The generated storage address.
$\qquad$ through ___ of the specified register.

8, 31
As a result of an LA instruction, bits $0-7$ of the specified register: (Circle one of the following. )
a. Remain unchanged.
b. Are zeroed out.
b
Given the following "load address" instruction, show the resulting contents of the specified register.

$00000800 \quad$ Given the following "load address" instruction, show the resulting contents of the register.


00001000 ; In the preceding problem, the contents of register 1 was used as a base address in generating an effective storage address:

|  | Base Address | 000800 |  |
| :---: | :---: | :---: | :---: |
| $\pm$ | Displacement | 800 | Hex Addition |
|  | Effective Addres | 001000 |  |

The effective address was then placed in register 1.

Given the following "load address" instruction, show the resulting contents of the register.


00002000
Given the following "load address" instruction, show the resulting contents of the register.


00003000
The preceding instructions showed how successive base addresses could be loaded into general registers. Let's take another look at these instructions in a symbolic program.

LA $\quad 1,2048(0,0)$
LA $1,2048(0,1)$
LA $\quad 2,0(1,1)$
LA $3,0(2,1)$
Examine the preceding program. Then indicate below (decimally) the base address that will be in each register at the completion of the program.

$$
\begin{array}{ll}
\text { Register } & 1 \\
\text { Register } 2 \\
\text { Register } &
\end{array}
$$

Reg 14096
Reg 28192
Reg 312288

The last two "logical" instructions for you to study are the "translate" instruction and the "translate and test" instruction. If you do not have systems experience and are unfamiliar with the terms translate or table look up, these instructions will be among the most difficult of those you have encountered. Therefore, let's examine the concept of translating before reading the description of these instructions.

First of all, there is data to be translated. This data may be in any code form we wish. The only code you have studied in the System/360 is EBCDIC. There are, of course, other codes in use with computers. For instance, there is an 8 -bit paper tape code and the 8 -bit ASCII code. The "translate" instruction will allow us to translate data from one code to another, byte by byte.

The "translate" instruction will allow us to translate bytes of data: (Circle one of the following.)
a. From one character code to any other character code.
b. Only from EBCDIC to some other character code.
c. Only to EBCDIC from some other character code.
d. Only from EBCDIC to ASCII.
a; The bytes to be translated can be in any character code. These bytes can be translated to any other desired code.

Let's look at this concept of translating from a programmer's viewpoint and see how he would handle a simplified translating problem.


The basic job that is to be accomplished is the printing of a report. Input to the system is in the form of $\qquad$ -.

IBM cards
Assume that the cards were punched on a card punch that did not have special character keys. The machine could only punch numeric and alphabetic characters.

The operator who punched the cards used alphabetic symbols to represent the special characters. For example, the character $P$ was used to represent $a+$ sign.

Special Characters
+
-
$\#$
$\$$
\&
$\&$

Alphabetic Symbol
P
M
N
D
C
A

The chart shows how each of the special characters was represented by an alphabetic character.

Given the following listings on a source document, indicate the characters that the operator actually punched in the cards.

Source Document IBM Card
$-79 ¢$
\$120+
E \& F \& \# 3

The input cards that are used in our simplified application $\qquad$
M79C (do/do not) contain special character punching.
EAFAN3
$\qquad$
The output of this simplified application is to be in $\qquad$ form. [t is desired to have the listings on the printed report contain the special characters rather than the alphabetic symbols. Therefore, the computer must convert or $t$ the input data before sending it to the printer.
printed
translate

Now, let's see how the programmer can use the "translate" instruction to solve the problem just discussed.

First, two tables must be established. They are the function table and the argument table.

The f $\qquad$ table consists of the desired characters. In our application, the function table will consist of the $\qquad$ (special/ alphabetic) characters.

The a $\qquad$ table consists of all the data that may have to be special converted. In our application, the argument table will consist of the symbols.
argument
alphabetic

In the next step, the programmer writes down all the possible data to be converted. Then he arranges it in binary bit sequence and forms the a $\qquad$ table.

| Argument Table |  |  |  |
| :--- | :--- | :--- | :--- |
| A |  | 1100 | 0001 |
|  | US (Unused Symbol) | 1100 | 0010 |
| C |  | 1100 | 0011 |
| D |  | 1100 | 0100 |
|  | US | 1100 | 0101 |
|  | US | 1100 | 0110 |
|  | US | 1100 | 0111 |
|  | US | 1100 | 1000 |
|  | US | 1100 | 1001 |
|  | US | 1100 | 1010 |
|  | US | 1100 | 1011 |
|  | US | 1100 | 1100 |
| M |  | 1100 | 1101 |
| N |  | 1100 | 1110 |
|  | US | 1100 | 1111 |
| P |  | 1101 | 0000 |


storage Go to the Principles of Operation manual and read the description of the function "translate" instruction in the Logical Operations section. Do not read storage the description of the "translate and test" instruction at this time.

The byte or bytes in the first operand are the characters that are to be converted or $t$ $\qquad$ . They are called a bytes. In the simplified application that you just studied, a first operand argument byte could be a $\qquad$ (D/\$).

## translated

 argument DThe second operand is the $f$ $\qquad$ table. In the simplified application, the address of the second operand would be $\qquad$ .
function
6807

The "translate" instruction does the following:

1. Takes the binary bit value of an argument byte and adds it to the second operand's address.
2. The resulting address is used to locate a function byte.
3. The function byte replaces the argument byte (1st operand).


The above instruction will translate $\qquad$ byte(s). The character to be translated is a $\qquad$ . The instruction goes to location 7003 in the function table (refer to the preceding simplified function table) and finds a $\qquad$ character. It takes this $\$$ character and puts it in location $\qquad$ where it replaces the D.

1
D
\$
0300

Now, let's go back and review the entire concept of translating and use a more typical application.

To translate, a table of the desired code must be available. For instance, assume that we wished to translate from EBCDIC to the 8-bit ASCII code. For simplicity we will only deal with the characters A-H. As a result our table will be only 8 bytes long.

The above table is located in main storage in 8 successive byte locations. As you can see, the bytes in the table are called $\qquad$ bytes.
function
The function bytes represent: (Circle one of the following.)
a. The bytes to be translated.
b. The desired character code.
b; The desired character code.

Besides the table of function bytes, which represent the desired code, there must also be data bytes which need translation. The following is a five-character record which needs translating:

The bytes to be translated are called $\qquad$ bytes.
argument
The above record of five EBCDIC characters is to be translated by using a table of $f$ $\qquad$ bytes.

The "translate" instruction consists of replacing the characters to be translated with the characters of the desired code. In other words, the
$\qquad$ bytes are replaced with the correct $\qquad$ bytes.
argument function

The "translate" instruction will replace all of the argument bytes with the desired characters from the function table.

Given the following function table and argument bytes, show the resulting contents of the argument field.

| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

OFCTION TABLE

| $c$ | AFTER |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |  |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |  |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |  |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |  |

ARGUMENT FIELD OF FIVE EBCDIC CHARACTERS


You should now know what is meant by a function byte or an argument byte. You should also realize that the argument bytes are to be replaced by the desired function bytes. We can review the translating concept by asking ourselves "How does the machine know which function bytes to select?" The answer lies in the organization of the function table. This table must be arranged so that the desired characters match the binary sequence of the argument table. This is shown as follows:


Table of all possible argument bytes is arranged on paper, in binary bit sequence. The table is used to develop the correct sequence for the function table.

Table of function bytes is arranged to match the respective argument bytes.

The table of FUNCTION bytes in storage is arranged so that: (Circle one of the following.)
a. The function bytes are in binary sequence.
b. The binary sequence of the argument bytes determines the sequence of FUNCTION bytes.
b
Go back to the Principles of Operation manual and reread the description of the "translate" instruction.

TR is the mnemonic for the " $\qquad$ " instruction.
"translate" The "translate" instruction has a hexadecimal Op code of DC. From bits $0-1$ of this Op code you can tell that the TR instruction uses the format.

SS
The 1st operand of the TR instruction represents: (Circle one of the following.)
a. The bytes to be translated.
b. The desired coded bytes.
a
The 2nd operand of the TR instruction represents: (Circle one of the following.)
a. The function bytes.
b. The argument bytes.
a
The function table must be long enough to take care of all expected bit combinations of the argument bytes.

The length code refers to: (Circle one of the following.)
a. The argument bytes.
b. The function bytes.
c. Both argument and function bytes.

To find the desired character in the function table, the argument byte is added to the beginning of the table.

Given the following argument byte, what bit combination will replace it?


10101111; The 1st operand's binary bit value (decimal 2) was added to the 2 nd operand's address (decimal 3840). The byte at location 3842 replaced the 1st operand.

You should now understand why the function table must be arranged according to the binary sequence of the argument bytes. This is because the argument byte is added to the initial table address. The coded character at that location then replaces the argument byte.

| DR | 17 | 0 | 800 | 0 | $F 00$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

Given the above "translate" instruction. How many argument bytes will be translated? $\qquad$ (Remember that the instruction is shown in hex.)

24; 17 in hex equals 00010111 in Binary which equals 23 in Decimal, and a length code always is one less than the total number of bytes.

Given the following "translate" instruction, show with six hex digits the starting address of the data bytes. The data bytes are the argument bytes.


Starting Address of Data Bytes $=$ $\qquad$

| DC | 17 | 0 | 800 | 0 | $F 00$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

Given the above "translate" instruction, show with six hex digits the starting address of the function table. $\qquad$

000 F 00

| DC | 17 | 0 | 800 | 0 | $F 00$ |
| :--- | :--- | :--- | :--- | :--- | :--- |

Given the above "translate" instruction, how many bytes are in the function table? $\qquad$ This question can be tricky, so answer carefully.

Unknown; The proper function byte is selected from the table by adding the argument byte to the starting address of the table. As a result, the table might contain a maximum of 256 bytes. This would depend on the total number of characters in the codes involved.

| ARGUMENT BYTE - 00110001 CHARACTER ADDRESS (IN HEX) $=$ |
| :--- |
| $\left.\begin{array}{\|c\|c\|c\|c\|c\|c\|}\hline \text { TR } & \text { DC } & 17 & 0 & 800 & 0\end{array}\right]$ F00 |

Given the above "translate" instruction, show with six hex digits the address of the character that will replace the argument byte.

000 F 31 ; As shown below.
The following byte is added to the starting address of the function table:
Shown in
Hex $\left\{\begin{array}{ll}000 \mathrm{~F} 00 & - \\ 31 & \text { Table Address } \\ \frac{-}{000 \mathrm{~F} 31} & \text { Argument Byte }\end{array} \quad \begin{array}{l}\text { Address of function byte selected to } \\ \end{array}\right.$
ARGUMENT BYTE - 11001001
TR

| DC | 17 | 0 | 800 | 0 | CHARACTER ADDRESS (IN HEX) $=$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

Given the above "translate" instruction and one of the argument bytes, show with six hex digits the address of the function byte that will be selected.

ARGUMENT BYTE - 11110111 $\qquad$
TR

| DC | 17 | 0 | 800 | 0 | $F 00$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

Given the above, show the six hex digits of the address of the selected function byte.

## 000 FF 7

Given the following data, show the contents of the argument field after the "translate" instruction is executed.


| Location |  |  |
| :---: | :---: | :---: |
|  | After |  |
| 2048 |  | 07 |
| 2049 |  | 02 |
| 2050 |  | 11 |
| 2051 |  | 02 |
| 2052 |  | 05 |
| 2053 |  | 11 |
| 2054 |  | 03 |
| 2055 |  | 02 |

The "translate" instruction can be summarized as follows:

1. The translation will be done by replacing an argument byte with a function byte from a table.
2. The length code (L field) gives the number of the argument bytes less one. A length code of 7 would indicate 8 argument bytes.
3. The address of the 1 st operand is the address of the argument bytes (those to be translated).
4. The address of the 2 nd operand is the address of the function table (those bytes which will be used to replace or translate the argument bytes).
5. In order to obtain the proper function bytes, the table must be arranged according to the binary bit sequence of the argument bytes.
6. The argument byte is added to the function table address. The resulting address is used to select a byte from the function table and replace the argument byte with it.
7. The "translate" instruction continues until all the argument bytes (determined by the length code) have been translated.

## TRANSLATE AND TEST INSTRUCTION

Read the description of the "translate and test" instruction in the Logical Operations section of your Principles of Operation manual.

In the "translate" instruction, the argument bytes are replaced with function bytes. In the "translate and test" instruction, the argument bytes
(are replaced with function bytes)
remain unchanged).
remain unchanged Is any translation actually done by the "translate and test" instruction?
$\qquad$

No
The "translate and test" instruction tests the argument bytes by selecting the corresponding function bytes. The test results are recorded by changing the $\qquad$
$\qquad$ .
condition code How does the machine know which function bytes are to be tested? $\qquad$
$\qquad$
$\qquad$

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It adds the argument byte to the starting address of the function table. The function byte at the resulting address is then tested.

The selected function byte is tested to see if it is $\qquad$ .
zero What happens if the function byte is zero?
$\qquad$

The operation continues with the next argument byte being added to the table address and another function byte being selected.

If all of the function bytes selected by the argument bytes are zero, the operation is completed by setting the condition code to $\qquad$ _.

00 (Binary) which is 0 in hex.

After a "translate and test" instruction, a condition code of 00 would indicate: (Circle one.)
a. That one of the selected function bytes was zero.
b. That all of the selected function bytes were zero.
c. That none of the selected function bytes were zero.
d. That all of the argument bytes were zero.
b ; A condition code of 00 would indicate that all of the argument bytes had been used in selecting function bytes. It would also mean that all of the selected function bytes were zero. It does not mean that all of the function bytes in the table are zero. It means that the selected ones were zero.

The "translate and test" instruction is used to examine a data field (the argument bytes) for characters with special meaning. The function table would again be arranged (as in the "translate" instruction) according to the binary sequence of the data code.

For all characters that do not have a special meaning (non-significant characters), the function byte location would contain zero.

For all characters that do have a special meaning (significant characters), the function byte location would contain some non-zero bit configuration.

A resulting condition code of 00 would then indicate that the entire data field had been examined and that no significant characters were found. By significant characters, we mean those with special meaning in a data field.

If a character with special meaning (significant character) is found, the instruction is terminated. A significant character would be indicated by selecting a function byte that was (zero/non-zero).

non-zero | If a significant character is found before the entire data field is examined, |
| :--- |
| the resulting condition code is 01 and the operation |
| (continues/is terminated). |.

is terminated
After a TRT instruction, a condition code of 01 would mean: (Circle one of the following.)
a. No significant character was found.
b. All the argument bytes were used and a significant character was found.
c. A significant character was found.
d. One or more significant characters were found.
c; As soon as a significant character is found, the operation is terminated without testing any more bytes

A condition code of 01 then means thet a significant character was found and some argument bytes haven't been tested. If the last argument byte is significant, the condition code is set to 10 .

After a TRT instruction, a condition code of 10 would mean: (Circle one of the following.)
a. All argument bytes were used and none located a non-zero function byte.
b. All of the argument bytes were not used. One of them was significant.
c. The last argument byte located a non-zero function byte.
d. All the argument bytes were used. One or more were significant.
c
After a "translate and test" instruction, which of the following condition codes would indicate that the entire field of argument bytes hasn't been examined? (Circle one of the following.)

## 00

01
10

01
Which of the following condition codes would indicate that none of the argument bytes had special meaning? (Circle one of the following.)

00
01

Either a condition code of 01 or 10 will indicate that a significant character was found. Why then does the programmer need both settings?

If the code were 01 , the programmer would have to execute the TRT instruction again to see if the remaining argument bytes contained any characters with special meaning.
decimal data field in storage (composed of argument bytes)


The purpose of the TRT instruction is to find significant characters in a data field. In the example above, the instruction could be used to find the location of commas in a decimal field. It would not make sense to know that there is a significant character without knowing where it is located. As a result, the TRT does more than just set the condition code. The address of the significant argument byte is placed in bits 8-31 of register 1.

When a TRT instruction results in a condition code of 01 or 10 , register 1 will contain: (Circle one of the following.)
a. The address of a function byte.
b. A function byte.
c. The address of an argument byte.
d. An argument.
c; When an argument byte which contains a significant character is found, its address is placed in register 1. If the condition code is 00 , register 1 is unchanged.

Besides placing the address of the significant argument byte in register 1 , the TRT instruction will also place the non-zero function byte in bits 24-31 of register 2. The rest of register 2 remains unchanged.

Given the following TRT instruction, show the resulting condition code and the contents of register 1 and 2 .



The 1st argument byte pointed to a zero function byte (the second byte in the function table).
The second argument byte pointed to a non-zero function byte (the first byte in the table).
The non-zero function byte is placed in the low order 8 bits of register 2 .
The address of the argument byte is placed in the low order 24 bits of register 1 . The rest of registers 1 and 2 remains unchanged.

The length code indicates a total of 8 bytes. Since a significant character was detected prior to using all argument bytes, the condition code is 01 .

The "translate and test" instruction can be summarized as follows:

1. The TRT instruction uses the SS format in which the length code gives the number of argument bytes less one.
2. The 1st operand consists of the argument bytes (the field that is to be searched for characters that have special meaning).
3. The 2nd operand consists of function bytes. These function bytes are pre-arranged according to the binary sequence of the argument bytes. The locations in this table that match the special meaning argument bytes have non-zero bit configurations.
4. An argument byte is added to the starting address of the function bytes. The function byte at the resulting address is tested for a non-zero bit configuration. If it is non-zero, the operation is terminated. The address of the argument byte is put into register 1 and the corresponding non-zero function byte is placed in register 2. The condition code is set to 01 or 10 , depending on whether or not the last argument byte has been translated.
5. If all tested function bytes are zero, the operation is terminated by setting the condition code to 00 . Registers 1 and 2 remain unchanged.

# System/360 Branching, Logical and Decimal Operations 

Section I: Branching Operations
Section II: Logical Operations

- Section III: Decimal Operations

Section IV: Analyzing Decimal Feature Programs

SECTION III LEARNING OBJECTIVES

At the end of this section, you should be able to do the following when given the mnemonic of any decimal feature instruction.

1. State instruction length and format.
2. State location and format of operands.
3. Determine the result and where it will be located.
4. State effect on condition code.
5. State which program checks are possible.

## Decimal Operations

This section of your self-study text covers the eight instructions which make up the decimal (sometimes called commercial) feature of System/360. This feature is optional on models 30,40 and standard on models 50-70. The instructions are as follows:

| Mnemonic |  | Title |
| :--- | :--- | :--- |
| AP |  | Add Decimal |
| SP |  | Subtract Decimal |
| ZAP |  | Zero and Add |
| CP |  | Compare Decimal |
| MP |  | Multiply Decimal |
| DP |  | Divide Decimal |
| ED |  | Edit |
| EDMK |  | Edit and Mark |

All of the above instructions use the SS format. As indicated by their mnemonics, both operands of the first six instructions must be in the (packed/zoned) decimal format.
packed
The "edit" and "edit and mark" instructions are used to change packed data to the zoned format and insert the punctuation necessary for a printed report.

Besides the eight decimal instructions, one other instruction will also be covered in this section. It is "move with offset." This instruction is part of the System/360's standard instruction set. However, you will find it easier to understand if it is covered here.

Before studying the decimal instructions, read the following introductory material in the Decimal Arithmetic section of your Principles of Operation manual.

```
Decimal Arithmetic
    Data Format
    Number Representation
    Condition Code
    Instruction Format
    Instructions (do not read the description of the individual
    instructions)
```

A numeric field punched in the standard card code will be brought into main storage in the $\qquad$ (zoned/packed) format.

## zoned

Assume that columns 21-25 of an IBM card contain the following punches:
Col. 214 hole punch
Col. $22 \quad 6$ hole punch
Col. $23 \quad 3$ hole punch
Col. $24 \quad 9$ hole punch
Col. 25 12, 1 hole punches
Show in hex how the above data field would appear after being read into main storage, starting at location 2048.


| F4 | F6 | F3 | F9 | C 1 |
| :--- | :--- | :--- | :--- | :--- |

A zoned decimal data field can be changed to the packed format by means of $\qquad$ .
a "pack" instruction; You previously used this instruction when you studied the binary operations. At that time, you used it to change zoned data to packed data, which was then converted to binary with another instruction.

Show how the following data field would look if it were packed into 3 bytes.


Show how the following data field would look if it were packed into 5 bytes.


| 00 | 00 | 46 | 39 | 10 |
| :---: | :---: | :---: | :---: | :---: |

Notice that the resulting field is extended with high-order zeroes.

At this point you may want to review the "pack" as well as the "unpack" instructions. If so, you will find their descriptions in the Decimal Arithmetic section of your Principles of Operation manual.

System/360 carries its negative binary numbers in complement form. On the other hand; its decimal numbers (whether positive or negative) are always carried in $\qquad$ (true/complement) form.

In the packed decimal format, the sign is represented by bits $4-7$ of the low-order bytes. Valid sign bit combinations are in the range of $\qquad$ to $\qquad$ .

The standard minus sign bit combinations are 1101 if operating in EBCDIC Mode or 1011 if in ASCII Mode. This is determined by bit 12 of the PSW.

The standard plus sign bit combinations are 1100 for EBCDIC mode and 1010 for ASCII mode.

```
PSW bit 12 is 0 - EBCDIC
PSW bit 12 is 1 - ASCII
```

For the remainder of this section, we will assume that the system is always in EBCDIC mode. That is, PSW bit 12 is zero.

The standard EBCDIC plus and minus sign bit combinations are such that a 12-hole card punch or an 11-hole card punch over the units position of a data field will represent a plus or minus sign respectively. A numeric data field that is punched into a card without the appropriate zone punch over the low-order digit will have a sign bit combination of 1111. That is normal for numbers in the EBCDIC code. This sign bit combination is considered plus. To summarize, these are the sign codes you can expect with the EBCDIC code:


Although the remaining combinations between 1010 and 1111 are valid sign codes, the preceding three combinations are the ones you will more likely encounter.

The instructions of the decimal feature use the SS format. In this format both operands are in main storage. With the exception of the two "edit" instructions, each operand will have its own four-bit length code. That is, the packed decimal operands can be from 1-16 bytes long.

Label the fields of the following SS format.


| OP CODE | L1 | L2 | B1 | D1 | B2 | D2 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Given the following SS format.

| OP CODE | 7 | 4 | 0 | 800 | 0 | FOO |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

The 1st operand starts at byte location 2048 and is The 2nd operand starts at byte location 3840 and is $\qquad$
bytes long. bytes long.

## ADD DECIMA L INSTRUC TION

Let's begin our study of the decimal instructions. The first instruction to learn is "add decimal." Read its description in the Decimal Arithmetic section of your Principles of Operation manual.

AP is the menmonic for the " $\qquad$
$\qquad$ " instruction.
"add decimal"; The ending letter of P tells us that both operands must be in the packed decimal format.

In the "add decimal" instruction, the sum of the 1st and 2nd operands replaces the $\qquad$ operand.

Since all packed decimal numbers are in true form, the signs of the field must be analyzed prior to any addition. If the signs are different (one plus and one minus), the 2nd operand is $\qquad$ (added to/ subtracted from) the first operand.

Subtraction on a computer is done by means of $\qquad$ addition.

Given the following AP instruction, show the resulting contents of the 1 st operand.


| 11 | 74 | 28 | $8 C$ |
| :--- | :--- | :--- | :--- |

The 2nd operand $\qquad$ (was/was not) changed by the preceding problem.
was not
In the preceding problem, two positive numbers were added together. The resulting positive sum would set the condition code to $\qquad$ .

10 Given the following AP instruction, show the resulting 1st operand field and the condition code.


In the preceding problem, two $\qquad$ (positive/negative) numbers were added together and the sum was $\qquad$ (positive/negative)

[^2]negative If the signs of the two operands are different, the 2nd operand is effectively negative subtracted from the 1 st operand. Given the following AP instruction, show the resulting 1 st operand and condition code.



COND. CODE 10

Given the following AP instruction, show the resulting 1st operand and condition code.



COND. CODE 01

As you previously learned, subtraction in a computer is usually done by means of complement addition.

Complement addition consists of adding the two operands after: (Circle one of the following.)
a. Complementing one of the operands.
b. Complementing both of the operands.
a
Given the following "add decimal" instruction with operands that have different signs, subtract the operands by complementing the 2nd operand and then adding.


C OMPLEMENT OF 2 ND OPERAND

FinAL RESULT


Complement of 2nd operand $=68001$

Final Result $=$| 15 | 02 | $0 c$ |
| :--- | :--- | :--- |

The result of complement addition could be in either true form or in complement form. How would the system know that the preceding answer was in true form? $\qquad$
$\qquad$ .

There was a carry out of the high-order digit during complement addition.

If there were no carry out of the high-order digit, the system would know that the answer was in complement form. What must the system do before the instruction is completed? $\qquad$

It must re-complement the answer and change the sign of the result field (1st operand).

Given the following "add decimal" instruction with operands that have different signs, subtract the 2 nd operand from the 1 st operand by means of complement addition.


| 50 | 47 | 3 | 1 |
| :--- | :--- | :--- | :--- |



Since decimal data is always carried in true form, the signs must be analyzed. Given the following signs, indicate whether the fields are true or complement added. The instruction is "add decimal." (Circle the correct answer for each set of signs.)

## 1st Operand $\quad$ nd Operand

a.
$+$

- True add/Complement add
True add/Complement add
b.
c. - - True add/Complement add
d. $\quad+\quad$ True add/Complement add
a. True add
b. Complement add
c. True add
d. Complement add

Given the following AP instruction, show the resulting contents of the 1 st operand and the condition code.



COND. CODE 00

In the previous problem, there are two equal values with different signs. In actual operation, the second operand would have its high order propagated with zeros so that it matches the first operand. These high order zeros would be complemented along with the rest of the second operand.

Since one quantity would be subtracted from the other, the result would be zero as indicated by the condition code setting. A zero result is always plus. That is the reason for changing the sign of the 1st operand from minus to plus.

The original length of the 1st operand will never be exceeded regardless of the result. Carries beyond the 1st operand's high order are lost. When there is a high-order carry, the condition code is set to $\qquad$ .

11 A carry out of the high order during an AP instruction is called a
$\qquad$ -.

A decimal overflow $\qquad$ (can/cannot) cause a program interrupt.
can When will a decimal overflow not cause a program interrupt? $\qquad$

When the appropriate Is the "set program mask" instruction a privileged one? mask bit in the PSW is set to zero.

No; The problem pro-
What else can cause a decimal overflow besides a high-order carry? grammer can change the program mask $\qquad$ (PSW bits 36-39) whenever he wishes.

The number of significant digits in the 2nd operand exceeding the length of the 1st operand.
d
Which of the following can cause a decimal overflow on an AP instruction? (Circle one of the following.)

|  | 1st Operand |  |  |  |  | 2nd Operand |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: |
| a. | 22 | 7 C |  | 00 | 90 | 7 C |  |  |
| b. | 50 | 0 D |  | 50 | 0 D |  |  |  |
| c. | 04 | 7 C |  | 01 | 00 | 1C |  |  |

d. All of the above
d
Besides a decimal overflow, there are other programming exceptions that can occur on an "add decimal" instruction. They are:

1. Operation - If the decimal feature is not installed on a system, any of the eight decimal instructions are considered illegal.
2. Protection - Since the results of the instruction replace the contents of main storage, this instruction is subject to a storage protection violation. The protection exception occurs if the storage key does not match the protection key in the PSW.
3. Addressing - Any instruction which addresses main storage for an operand is subject to an addressing exception. This exception occurs when the address is not available on a particular system (such as an address 16000 on an 8 K system).
4. Data - All packed decimal operands are checked for valid digits and sign. All of the digit positions must be coded from $0000-1001$. The sign position must be coded from 1010-1111.

What would happen if the "add decimal" instruction were used to add two zoned decimal fields? $\qquad$

A data exception Would a protection exception be recognized on an "add decimal" instruction would be recognized and a program interrupt would occur.

No; The two keys do not need to match if the protection key is zero.

The decimal feature is optional on models 30 and 40 of System/360. What would happen if an "add decimal" instruction was fetched on a model 30 which doesn't have the decimal feature installed?

## SUBTRACT DECIMAL INSTRUCTION

An operation exception would be recognized and a program interrupt would occur.

The next instruction to be covered is the "subtract decimal" instruction. Read the description of the SP instruction in the Decimal Arithmetic section of your Principles of Operation manual.

The mnemonic for the "subtract decimal" instruction is $\qquad$ .

SP The operation of "subtract decimal" instruction is similar in all respects to the "add decimal" instruction. The only difference is that the AP instruction adds and the SP instruction subtracts.

Given the following signs, indicate whether the fields will be true or complement added on an AP instruction. (Circle the answers.)

## 1st Operand 2nd Operand

| a. | + | - | True add/Cormplement add |
| :--- | :--- | :--- | :--- |
| b. | + | + | True add/Complement add |
| c. | - | - | True add/Complement add |
| d. | - | + | True add/Complement add |

a. Complement add
b. True add
c. True add
d. Complement add

Given the following signs, indicate whether the operands will be true or complement added on an SP instruction. (Circle the answers.)

1st Operand 2nd Operand

| a. | + | + | True add/Complement add |
| :--- | :--- | :--- | :--- |
| b. | + | - | True add/Complement add |
| c. | - | + | True add/Complement add |
| d. | - | - | True add/Complement add |

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a. Complement
b. True
c. True
d. Complement

One use of the "subtract decimal" instruction is to zero out a packed decimal field. Show the resulting contents of the 1st operand for the following SP instruction.


The SP instruction can also be used to zero out the low order of a field. Show the result of the following instruction.

Notice that a zero difference results in a plus sign.


| 41 | 00 | 00 | $0 D$ |
| :--- | :--- | :--- | :--- |

Notice that since only part of the field was zeroed out, the sign remained minus.

What would happen on the following instruction?


Your response: $\qquad$

A data exception would be recognized and a program interrupt would occur. This occurs because the 2nd operand's low-order byte contains 21. Bits $4-7$ of this byte would be recognized as an invalid sign code.

1ST OPERAND


2 ND OPERAND

The next decimal instruction is "zero and add." Its mnemonic is ZAP. Read the description of this instruction in the Decimal Arithmetic section of your Principles of Operation manual.

The ZAP instruction will replace the $\qquad$ (1st/2nd) operand with the (1st/2nd) operand.

1st
Is the 1st operand (data) used on a ZAP instruction? $\qquad$
2nd

No; It is ignored. Does the 2nd operand need to be in the packed decimal format or can any type of data be moved by the ZAP instruction? $\qquad$
$\qquad$ _.

The 2 nd operand must be valid packed decimal data or a data exception will be recognized and cause a program interrupt.

Do both operands on a ZAP have to be of equal length? $\qquad$

No What happens to the extra bytes of the 1st operand when the 1st operand is longer than the 2nd operand? $\qquad$ -.

They are zeroed out. If the 1 st operand is too short to contain all of the significant digits from the 2nd operand, a $\qquad$
$\qquad$ will be recognized.
decimal overflow Given the following ZAP instruction, show the resulting contents of the 1st operand and the condition code.


Given the following ZAP instruction, show the resulting contents of the 1st operand and the condition code.


Given the following ZAP instruction, show the resulting contents of the 1st operand and the condition code.


COND. CODE $\qquad$

| 23 | 71 | $0 C$ |
| :--- | :--- | :--- |

COND. CODE 10
COND. CODE 10

In the previous problem, the 2 nd operand was longer than the 1 st operand. Why wasn't a decimal overflow indicated in the condition code? $\qquad$
$\qquad$ -

All significant digits from the 2nd operand were able to fit in the 1 st operand.

Given the following ZAP instruction, show the resulting contents of the 1st operand and the condition code.


| 76 | 54 | $3 C$ |
| :--- | :---: | :---: |

Will a program interrupt occur after the preceding instruction is executed?
$\qquad$

Yes; This is assuming that the decimal overflow mask bit in the PSW's Program Mask is set to 1. If the mask bit is set to 0 , the program interrupt does not occur. However, since the condition code indicates a decimal overflow, the next instruction could be a "branch on condition."

Besides the data and decimal overflow exceptions, the ZAP instruction is subject to other exceptions. They are: $\qquad$ _, $\qquad$ and $\qquad$ -.

## COMPARE DECIMAL INSTRUCTION

Operation (if the decimal feature is not installed) Addressing Protection

The next instruction you will study is the "compare decimal" instruction. This instruction makes an algebraic comparison of two packed decimal fields. It does not compare alphameric information. The "compare logical" instruction which you previously studied is used for that purpose. Read the description of the "compare decimal" instruction in the Decimal Arithmetic section of your Principles of Operation manual.

If the fields addressed by a CP instruction are not in the packed decimal format, a $\qquad$ exception will be recognized.
data
The result of the comparison is recorded in the $\qquad$
$\qquad$ .
condition code
A condition code of 00 would indicate that the operands were $\qquad$ -


2nd
A condition code of 10 would indicate that the $\qquad$ (1st/2nd) operand was high.
$\qquad$
The "compare decimal" instruction $\qquad$ (does/does not) change the operands.
does not
Show the resulting condition code for the following "compare decimal" instruction.


COND. CODE $\qquad$

00 ; Both operands were equal.

COND. CODE $\qquad$

10; Since the 1 st operand is positive, it is high.


Show the resulting condition code for the following CP instruction.

Show the resulting condition code for the following "compare decimal" instruction.


COND. CODE $\qquad$

01; Even though the 1st operand is longer, its algebraic value is less than that of the 2 nd operand.

Show the resulting condition code for the following "compare decimal" instruction.


COND. CODE $\qquad$

01; The numeric value of the 1st operand is greater; however, both operands are negative. Algebraically, a small negative number is greater than a large negative number as shown below.



Show the resulting condition code for the following "compare decimal" instruction.


COND. CODE $\qquad$

## MULTIPLY DECIMAL INSTRUCTION

10; The 1st operand is less negative and therefore algebraically greater.

You are ready to study the "multiply decimal" instruction. Its mnemonic is MP and like the other decimal instructions, it operates with packed decimal data. Before reading the description of this instruction, let's take a few simple examples.

In the MP instruction, the 1st operand is the multiplicand. The 2nd operand is the multiplier. As with most instructions, the product will replace the $\qquad$ (multiplicand/multiplier).
multiplicand; It is the 1 st operand. l

a. Multiplicand
b. Multiplier

For the preceding MP instruction, show the resulting contents of the multiplicand.


## 90 Decimal Operations



Show the resulting product for the following MP instruction.



Like signs give a positive product.


Can the resulting product for the above MP instruction fit into the multiplicand field? $\qquad$

No; The rule of thumb is that the number of digits in the product is equal to the sum of the number of significant digits in both operands.

To prevent the product from overflowing the multiplicand field on a "multiply decimal," the System/360 has the following restriction on the multiplicand.

The number of high-order zeroes in the multiplicand must be at least equal to the number of digits in the multiplier. This includes high-order zeroes in the multiplier. For example:


Read the description of the "multiply decimal" instruction in the Decimal Arithmetic section of your Principles of Operation manual.


The above MP instruction will result in a $\qquad$ exception and cause a program interrupt.
data; Because the number of high-order zeroes in the multiplicand is less than the size of the multiplier.

What must be done to prevent a specification exception on an MP instruction? $\qquad$

The multiplier must be shorter than the multiplicand and cannot have a length code greater than 7 ( 15 digits and a sign).

One problem that is often encountered after a multiply operation is the placement of the decimal point. For instance, 0001120 C multiplied by 00010 C equals 0011200 C . However, suppose these numbers represented dollars and cents, such as:

| $\$ 11.20$ |
| ---: |
| $\$ \quad .10$ |
| 0000 |
| 1120 |
| $\$ 1.1200$ |

As you can see, the decimal point was shifted by the multiplication.

What is usually necessary is shifting the product to the right in order to reestablish the proper place for the decimal point. There are no "shift" instructions for the storage-to-storage operations. However, the "move" instructions (which were covered under Logical Operations) can be used to effectively shift storage data.

In our previous example, the product had to be shifted two places to the right in order to maintain the decimal point. For instance:

$$
\begin{array}{r}
00011.20 \mathrm{C} \\
\times \quad 0.10 \mathrm{C} \\
\hline 001.1200 \mathrm{C}
\end{array}
$$

The above product really should be like this: 00001.12 C . This can be accomplished by use of the "move numerics" (MVN) instruction followed by a "zero and add" (ZAP). See the example below.

PROGRAM TO MULTIPLY AND TO CORRECT THE DECIMAL POINT


STORAGE CONTENTS BEFORE EXECUTION OF THE ABOVE INSTRUCTIONS


STORAGE CONTENTS

AFTER MP


AFTER MVN


AFTER ZAP


Any time a packed decimal field is to be shifted an even number of places to the right, the MVN instruction can be used to place the sign next to the new low-order digit. As shown previously, the packed decimal field can then be shifted to the right by use of the ZAP instruction.

To right shift a packed decimal field an odd number of places, the "move with offset" instruction can be used. You haven't studied this instruction yet. The following is an example of how the "move with offset" (MVO) instruction works.


Note that the 2nd operand replaced the 1st operand. However the sign of the 1st operand (rightmost four bits) was left undisturbed. Now let's see how the MVO instruction can be used to effectively right shift a packed decimal data field an odd number of digit places.


Notice that this instruction does not disturb the sign of the 1st operand. By offsetting each group of four bits in their bytes, an effective shift of an odd number of places is accomplished as the 2 nd operand is moved into the 1 st operand.

## MOVE WITH OFFSE T INSTRUCTION

Read the description of the MVO instruction in the Decimal Arithmetic section of your Principles of Operation manual.

Given the following MVO instruction, show the resulting contents of the 1st operand.


BEFORE 2048


AFTER 2048


| 00 | 05 | 41 | $0 C$ |
| :--- | :--- | :--- | :--- |

Is the data moved by the MVO instruction checked to see if it is valid packed decimal data? $\qquad$

No; You have seen it being used to right shift packed decimal data an odd number of places. However, any type of data can be moved by this instruction.

Is the MVO instruction part of the System/360 decimal feature? $\qquad$

No; The MVO instruction is part of the standard instruction set.

Go to the Appendix in the Principles of Operation manual. Find the List of Instructions by Set and Feature. You will see the instructions that make up the standard instruction set and also the ones that make up the decimal feature.

So far you have seen how to right shift packed decimal data an even number of decimal places by using an MVN instruction followed by a ZAP. You used an MVO instruction to right shift an odd number of decimal places. How about left shifting packed decimal data?

Left shifting of decimal data is a little more complex. For instance, suppose the following data field is to be shifted two places to the left.

| 00 | 47 | 12 | 76 |
| :--- | :--- | :--- | :--- |

After being shifted it should look like this:

| 47 | 12 | 70 | $0 C$ |
| :--- | :--- | :--- | :--- |

The preceding shift can be done by the following three instructions:

| D2 | 02 | 0 | 800 | 0 | 801 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| F1 | 00 | 0 | 803 | 0 | F00 |



LOCATION 2048

| 00 | 47 | 12 | 70 |
| :--- | :--- | :--- | :--- |



After executing the MVC (Move Characters) instructions, locations 20482051 would look like this:

2048-2051


In the preceding MVC instruction, locations 2049-2051 were moved a byte at a time into locations 2048-2050. The fields were processed in a left to right direction.

The 2nd instruction (MVO) would take the constant of zero from location 3840 and move it into the high order of location 2051. Since the length codes are zero, only location 2051 is changed. The result would look like this:

$$
2048-2051
$$



The third instruction (NI) is an "and immediate" instruction. The immediate operand (F0) is ANDed with location 2050 as shown below:

| Immediate Operand | 11110000 |
| :--- | ---: |
| Location 2050 | 01111100 |
| Result | 01110000 |

Locations 2048-2051 now look like the desired result:

2048-2051


The preceding series of instructions is only one way of left shifting an even number of places.


Given the above sequence of instructions, how many places was the data field shifted? $\qquad$

4; As shown below:


Now let's shift an odd number of places:


To achieve the above result requires an effective shift of three places. This can be accomplished as follows:

| F1 | 3 | 4 | 0 | 800 | 0 | 800 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| F1 MVo | 1 | 0 | 0 | 803 | 0 | F00 |

LOCATIONS 2048-2052 00 | 00 | 00 | 47 | 12 | $7 C$ |
| :--- | :--- | :--- | :--- | :--- |

LOCATION 3840
00
$\qquad$
After executing the 1st MVO instruction, locations 2048-2052 would look like this:

| 04 | 71 | 27 | C 2 | 70 |
| :--- | :--- | :--- | :--- | :--- |

$\qquad$
After executing the 2 nd MVO instruction, locations 2048-2052 would look like this:

| 04 | 71 | 27 | 00 | $0 c$ |
| :--- | :--- | :--- | :--- | :--- |

The preceding is the desired result.

Show the resulting contents of locations 2048-2052 for the following sequence of instructions.


LOCATION 3840
00


| 00 | 14 | 72 | 39 | $0 c$ |
| :--- | :--- | :--- | :--- | :--- |

You have seen some ways of shifting packed decimal data. By proper use of the "move" instructions, you should be able to come up with other methods. For now, let's continue on to the "divide decimal" instruction.

## DIVIDE DECIMAL INSTRUCTION

You are now ready to study the "divide decimal" instruction. The following is a "divide decimal" instruction:


As you can see above, the dividend is the $\qquad$ (1st/2nd) operand and the divisor is the $\qquad$ operand.

1st
2nd

As in the other instructions you have studied, the generated effective
storage addresses refer to the fields.
$\qquad$ (high/low) order byte of the data

The mnemonic for the "divide decimal" instruction is DP. This indicates that the divide instruction operates on $\qquad$ (packed/zoned) decimal data.
packed

| FD | $F$ | 6 | 0 | 800 | 0 | 810 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

The above DP instruction has a dividend that is $\qquad$ bytes in length.

Sixteen bytes of packed decimal data can contain $\qquad$ digits and a sign.

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Given the above DP instruction, a value of $\qquad$ will be divided by a value of $\qquad$ .
$+2560$
$+16$

The DP instruction will have as a result both a quotient and a remainder. These two results will be in the packed decimal format and will replace the dividend. The quotient will replace the high order and the remainder will replace the low order of the dividend. The following example will illustrate this.


NOTE: The remainder is always the same size as the divisor!

Given the following "divide decimal" instruction, show the resulting contents of the dividend field.


| 12 | oc | 00 | oc |
| :---: | :---: | :---: | :---: |

The remainder is placed in the low order of the dividend field and always contains the same number of bytes as the $\qquad$ .
$\qquad$
divisor or 2nd operand

The quotient is placed in the dividend field just to the left of the
$\qquad$ .
$\qquad$
remainder
Read the description of the "divide decimal" instruction in the Decimal Arithmetic section of your Principles of Operation manual.

The address of the quotient of a DP instruction will be the same as the original $\qquad$ .
dividend or 1st operand $\qquad$
divisor
If the quotient cannot be fitted into its area, a $\qquad$
$\qquad$ exception will be recognized.
decimal divide
When a decimal divide exception is recognized, the dividend field will (remain unchanged/contain part of the quotient).
$\qquad$
The size of the quotient will be equal to the dividend size minus the
$\qquad$ size.
$\qquad$
$\qquad$

A Decimal Divide exception can be determined by aligning the leftmost digit of the divisor (2nd operand) with the next to leftmost digit of the dividend (1st operand). The divisor should be greater than that part of the dividend with which it is aligned.

## For example:

The following operands would result in a decimal divide exception because the divisor is not greater than the aligned section of the dividend.

| 1st operand (dividend) | 00 | 16 | 0 C |
| :--- | ---: | :--- | :--- |
| 2nd operand (divisor) | 0 | 16 | C |

The following operands would NOT result in a decimal divide exception because the divisor is greater than the aligned section of the dividend.

```
1st operand (dividend)
2nd operand (divisor)
00 15 9C
    0 16 C
```



The above instruction $\qquad$ (would/would not) result in a decimal divide exception.

Would; This is because the high-order divisor digit (5) is not greater than the two high-order digits of the dividend (06).

How can you be sure that the quotient can't be fitted into its area unless the preceding rule is met? Let's work out the problem.


The original dividend was three bytes in length. The remainder of +440 will take up two bytes. The quotient of +11 cannot be fitted into the remaining byte.

Of course, no division takes place when the decimal divide exception is recognized. The System $/ 360$ will check to be sure that the divisor is greater than the aligned section of the dividend. If not, division does not take place and a program interrupt occurs.

Given the following DP instruction, show the resulting contents of the dividend.


| 09 | 99 | 99 | 99 | $0 c$ |
| :---: | :---: | :---: | :---: | :---: |

In the preceding problem, the divisor was not greater than the aligned section of the dividend. A decimal divide exception was recognized, the dividend was left unchanged, and a program interrupt was taken.

Another programming rule that applies to the "divide decimal" instruction is this:

The divisor must be shorter than the dividend and cannot exceed eight bytes. That is, L2 < L1 and L2 < 8.

| $F D$ | 9 | 8 | 0 | 800 | 0 | 810 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

The above DP instruction will result in a specification error because the divisor's length code is greater than $\qquad$ -

7

| FD | 3 | 3 | 0 | 800 | 0 | 804 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

The above DP instruction will result in a specification error because
$\qquad$ ...

The divisor is not shorter than the dividend.

Let's summarize the "divide decimal's" data fields.

1. The Dividend
a. The 1st operand is the dividend.
b. The dividend has a maximum size of 31 digits and a sign.
c. The dividend will be replaced by the quotient and remainder.
d. The dividend must have at least one high-order zero digit.
2. The Divisor
a. The 2nd operand is the divisor
b. The divisor has a maximum size of 15 digits and a sign.
c. In all cases, the divisor must be shorter than the dividend.
(Frame continued on next page.)
3. The Remainder
a. The remainder replaces the low order of the dividend field.
b. The remainder has the same length as the divisor.
c. The sign of the remainder is the same as the sign of the original dividend.
4. The Quotient
a. The quotient replaces the high order of the dividend field.
b. The size of the quotient is equal to the dividend size minus divisor size (L1 - L2).
c. Since the quotient is placed in the high order of the divide field, its address will be the same as the dividend's.
d. The sign of the quotient follows the rules of algebra.
(1) Like signs $=+$
(2) Unlike signs = -
5. Decimal Divide Exception
a. This exception indicates that the quotient would be too large to be fitted into its allotted field.
b. This exception is recognized whenever the divisor is not greater than the aligned section of the dividend. It is for this reason that the dividend must have at least one high-order zero digit.
c. The decimal divide exception is recognized prior to any division. The dividend field is left unchanged and a program interrupt is taken.
6. Specification Exception

This exception is recognized on a "divide decimal" instruction whenever:
a. The divisor is longer than eight bytes.
b. The dividend is not longer than the divisor.

## EDIT INSTRUCTION

The two remaining instructions that make up the decimal feature are the "edit" instruction and the "edit and mark" instruction. The purpose of these edit operations is to produce easy-to-read documents by inserting the proper punctuation into a data record. The data to be edited is called the source field and must be in the packed decimal format. Consider the following source field:


In its present format, the preceding field cannot be printed. The data must be in EBCDIC before being printed.

Onc of the functions of the edit operation is to change a source field from the $\qquad$ format to the $\qquad$ decimal format.
packed zoned

If changing from the packed to the zoned format were all that was necessary to produce a legible report, the "edit" instruction wouldn't be necessary. The "unpack" instruction, which you previously studied, would be sufficient. For instance, if the previous packed decimal operand were changed to the zoned format, it would look like this:

| PACKED | 00 | 12 | 49 | 07 | 10 |
| :---: | :---: | :---: | :---: | :---: | :---: |


| ZONED | FO | FO | F1 | F2 | F4 | F9 | FO | F7 | F1 | F0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

If the above zoned decimal field were printed, it would look like this:

$$
\begin{array}{lllllllllll}
0 & 0 & 1 & 2 & 4 & 9 & 0 & 7 & 1 & 0 & G
\end{array}
$$

By examining the printed document, you could tell by looking at the loworder character (G) that it was a positive number with a low-order digit of 7. However, the printed document is still not too legible. Perhaps the number represents money. It would be better if it could look like this:

$$
\$ 1,249,071.07
$$

As well as other editing, this would require inserting the commas and decimal points in the right places. This is another function of the edit operations.

The edit operation will change a packed decimal field which is called the
$\qquad$ field, into the zoned format and insert the necessary punctuation characters.
source
The edit operation consists of moving the source field into a pattern field. The pattern field will be made up of EBCDIC characters that will control the editing. The final edited result will replace the PATTERN field.


During an edit operation, the $\qquad$ field is edited under control of the $\qquad$ field.


2nd Like most instructions, the results of the edit operation replace the 1 st operand which is the $\qquad$ field.
pattern
The length code refers to the pattern field which can be a maximum of bytes in length.

The characters in the pattern field determine the editing that will take place. The high-order (leftmost) character in the pattern field is known as the fill character. For many edit operations, the fill character would be an EBCDIC blank ( 01000000 ).

The fill character is used in the edit operation to replace certain characters in the pattern field. You will see this more clearly later.

The fill character is the $\qquad$ byte in the
field.
leftmost pattern

Any of the 256 possible EBCDIC combinations can be used as the fill character. However, in many edit operations the fill character will consist of an EBCDIC $\qquad$ -.
blank; For explanatory purposes, a blank will be represented by a small $b$ in a field such as JOHNbSMITH. Of course, blanks won't be printed out.

Besides the fill character, there are three more characters in the pattern field that have special meaning. They are:

1. The Digit Select Character.
2. The Significance Start Character.
3. The Field Separator Character.

These three characters can appear anywhere in the pattern field.

The digit select character has the following bit structure: 00100000 . There is no character symbol for this combination. It is normally represented by a small "d" just as blanks are represented by a small "b."

When a digit select character is encountered in a pattern field, it is usually replaced by a digit from the source field. If the source digit is a high-order zero, the fill character is used instead to replace the digit select character. By using a blank as the fill character, high-order zeroes can be blanked out.

If an asterisk is used as the fill character, asterisk protection for paychecks can be achieved.

What characters can replace a digit select character in the pattern field? 1.
2.

1. A digit from the source field.
2. A fill character.

What symbol is used to denote a digit select character? $\qquad$
d; Actually, the binary bit of a digit select character is 00100000 or a hex 20 . There is no character for this combination on any of the System/360 printers. The " d " is used to represent this combination in your textbooks.

Let's look at an example of the use of the fill character and the digit select character.


Prior to the "edit" instruction, the pattern was brought out of the constant storage area and put in the $p$ $\qquad$ f $\qquad$ .

## pattern field

 The leftmost position of the pattern field contains the fill character which in this example is a $\qquad$ . The remaining positions of the pattern field contain $\qquad$ characters.

Since a digit select character is replaced by a source digit or the fill character, the system needs some way of knowing which of the two to choose. This is determined by a remembering device called the S trigger in the system's circuitry.

The S trigger can be set to one of two states: 0 state or 1 state.
When set to 1 , the $S$ trigger indicates that the digits from the source field are significant. As a result, the digit select characters in the pattern field are replaced with the digits from the source field.

At the beginning of the edit operation, the $S$ trigger is set to 0 . As long as the $S$ trigger is 0 , the digit select characters in the pattern field are replaced with the fill character.

What determines whether a digit select character is replaced with a source digit or with the fill character?

The S trigger

0

At the beginning of the edit operation, the S trigger is set to $\qquad$ (1/0).

When the $S$ trigger is set to 0 , a digit select character in the pattern field is replaced with $\qquad$ -.
the fill character
When the $S$ trigger is set to 1 , a digit select character in the pattern field is replaced with $\qquad$ .
the digit from the source field

Both the source field and the pattern field are processed left to right, a character or digit at a time. Each time the digit from the source field replaces a digit select character, the 4 -bit digit has the proper EBCDIC or ASCII zone bits inserted. PSW bit 12 determined whether the EBCDIC or ASCII zone bits are inserted. For the purposes of this text, we will assume that the system is in EBCDIC mode.

The $S$ trigger is set to 0 at the beginning of the edit operation. It is set to 1 by one of two methods:

1. A significant (non-zero) digit from the source field.
2. A significance start character in the pattern field.

The significance start character has a bit pattern of 00100001 (hex 21). This bit pattern has no character symbol. The symbol for the left parenthesis is used to represent a significance start character such as "(".

Which symbol, "d," "b," ")," or "(," is used to represent each of the following?

Blank = $\qquad$
Significance Start Character $=$ $\qquad$ Digit Select Character = $\qquad$

Blank = "b"
Significance Start Character = " $("$
Digit Select Character $=$ " d "

What two characters can set the $S$ trigger to 1 ?

1. $\qquad$ -.
2. $\qquad$ .
3. A non-zero digit from the source field.
4. A significance start character in the pattern field.

A significance start character is replaced (as was the digit select character) by either a digit from the source field or by the fill character. For example:

SOURCE FIELD
(TWO DIGITS/BYTE)

PATTERN FIELD (ONE CHARACTER/BYTE)

(OESULT


BEGINNING OF CYCLE
$S$ TRIGGER


The edit operation begins by examining the fill character. If it is not a digit select or a significance start character, it is left in place in the pattern field. Then the next pattern character is examined. In the previous example, this was a significance start character. The high-order source digit is then examined. Because the source digit is zero and the S trigger is 0 (at this time), the significance start character is replaced with the fill character. However, the significance start character does set the $S$ trigger to 1 so that all subsequent source digits are significant. The remaining pattern characters in our example are digit select characters which are replaced with source digits.

Given the 1st few characters of a source and pattern field below, show the resulting contents of the pattern field after editing.


SOURCE FIELD

PATTERN FIELD

RESULT
$\begin{array}{llllll}\mathrm{b} & \mathrm{b} & \mathrm{b} & 1 & 2 & 4\end{array}$
In the previous problem, there was no significance start character. As a result, the two high-order zeroes from the source field did not go into the pattern field. The fill character was used instead. Once significance was started, the remaining pattern characters were replaced by source digits.

Once significance is started, the $S$ trigger will remain on until one of two things happens:

1. The sign of the source field is examined and is plus.
2. A field separator character (00100010) is recognized.

The field separator character is used when two or more packed decimal source fields are to be edited into a pattern with one instruction field. We'll examine this later. For now, let's discuss the handling of the sign.

Since the sign is in the right half of the source field's low-order byte, it can be examined at the same time as the low-order digit is examined. The sign itself is skipped over but, if plus, the $S$ trigger is set to zero. The following will illustrate this.


PATTERN FIELD ( 1 character/byte)

| b | b | b | 1 | 2 | 4 | 9 | 0 | 7 | 1 | 0 | 7 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

RESULT


When a pattern character is examined and is not one of the three special control characters, it is left in place if the $S$ trigger is 1 . Otherwise, it is replaced by the fill character.

The source field is not examined. The usual method of indicating a negative quantity in a printed report is with the letters "CR." If we take another look at the previous example and add the CR symbol, this would be the result:

| 00 | 12 | $49 \quad 07$ |  | 10 | 7 C | 6 BYTES PATTERN |  | 14 BYTES |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| b | d | d | d | d | d | d | d | d | d | d | d | C | R |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| b | b | b | 1 | 2 | 4 | 9 | 0 | 7 | 1 | 0 | 7 | b | b |

Because the plus sign set the $S$ trigger to 0 , the remaining pattern characters (CR) were replaced by the fill character. If the sign of the source field had been minus, the " CR " would have been left in the pattern field.

Let's take the following source field and produce the edited result.

Source | 00 | 12 | 49 | 07 | 10 | 70 |
| :--- | :--- | :--- | :--- | :--- | :--- |

Edited Result blblar 249,071 . 07 b C R b

The original pattern would look like this:

Pattern $\quad b d d d, d d d, d d d . d d b C R b$
Notice that the commas, decimal point, and "CR" were left in place. This occured because the $S$ trigger was set to 1 and remained there.

Given the following, show the edited result.
Source

| 00 | 14 | 71 | $3 C$ |
| :--- | :--- | :--- | :--- |

Pattern
b d d , d d d. d d b C R b

Result

-     -         -             -                 -                     -                         -                             -                                 -                                     -                                         -                                             -                                                 - 

b b b b 147 . 13 b b b b
Of course, the blanks in the previous answer won't print in the final printed report which would look like this:

$$
147.13
$$

Read the description of the "edit" instruction in the Logical Operations section of your Principles of Operation manual.

Which of the following can set the $S$ trigger to 0 ? (Circle one or more.)
a. Digit Select Character
b. Significance Start Character
c. Field Separator Character
d. Beginning of edit operation
e. Plus sign in source field
$\mathrm{c}, \mathrm{d}, \mathrm{e}$
Which of the following can set the $S$ trigger to 1 ? (Circle one or more.)
a. Digit Select Character
b. Significance Start Character
c. Minus sign in source field
d. 1st non-zero character in source field
e. Field Separator Character

| $\mathrm{b}, \mathrm{d}$ | A digit select |
| :---: | :---: |
|  |  |
|  | trigger is 1. |

fill character source digit

A significance start character in the pattern is replaced by the if the $S$ trigger is 0 or by a $\qquad$ if the S trigger is 1.
fill character source digit

A field separator character always sets the $S$ trigger to 0 and is replaced by the $\qquad$
$\qquad$ --.

Characters in the pattern other than the control characters are either replaced by the $\qquad$ if the $S$ trigger is 0 or are

Show the results of the following "edit" instruction.
fill character left in place


| 1st Operand | b d d | d d (. d d b C R |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 2nd Operand | 0 | 7 | 9 | 4 | 7 | 6 | 9 | Characters) |$\quad$| (digits and sign) |
| :--- |

b b 7,947 . 69 b b b
$\qquad$
Show the result of the following "edit" instruction.

| ED | $0 C$ | 0 | 800 | 0 | 900 |
| :---: | :---: | :---: | :---: | :---: | :---: |


| 1st Operand | $b$ | $d$ | $d$ | d $d$ | (. d d b C R | (characters) |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 2nd Operand | 0 | 0 | 0 | 0 | 0 | 6 | 9 | D | Result 000069 D (digits and sign)

b b b b b b b . 69 b C R
$\qquad$
Referring to the previous problem, show the result for the following pattern.
Pattern $\quad b \mathrm{~d} \mathrm{~d}, \mathrm{~d} \mathrm{~d} \mathrm{~d} . \mathrm{d} \mathrm{d} \mathrm{b} \mathrm{C} \mathrm{R}$
Result
b b b b b b b b 69 b C R; Note that a significance start character should be in the pattern to protect the decimal point in case the amount is less than a dollar.

Show the result of the following "edit" instruction.

| ED |
| :--- |
| DE |

$$
\begin{array}{llllllllllllll}
\text { 1st Operand } & * & d & d & & d & d & (. & d \mathrm{~d} \text { b C R } \\
\text { 2nd Operand } & 0 & 0 & 0 & 0 & 0 & 6 & 9 & \mathrm{C}
\end{array}
$$

[^3]The following "edit" instruction will edit multiple adjacent source fields. Show the result.


b b 17.76 b b b b b b b b b b b b b; Note that the field separator character set the S trigger to zero. No significant digits were found in the 2nd source field. As a result, the pattern characters were replaced by the fill character (blanks).

Up to this point you have seen that the "edit" instruction can be used to:

1. Eliminate high-order zeroes
2. Provide asterisk protection
3. Handle sign control (CR)
4. Provide punctuation
5. Blank out an all-zero field
6. Edit multiple adjacent fields via the field separator character
7. Protect the decimal point by use of the significance start character. This character can also be used to retain high-order zeroes when desired.

## EDIT AND MARK INSTRUCTION

The "edit" instruction makes no provision for using a floating currency symbol (such as $\$$ ) as part of the editing process. For this edit feature, the "edit and mark" instruction must be used. Read the description of the "edit and mark" instruction in the Logical Operations section of your Principles of Operation manual.

ED is the mnemonic for the "edit" instruction while EDMK is the mnemonic for the " $\qquad$
$\qquad$
$\qquad$ " instruction.
"edit and mark"
Is there anything that the ED instruction can do that the EDMK instruction can't do ? $\qquad$ (Yes/No)

The EDMK instruction causes the address of the 1 st significant digit of the result to be placed in general register 1.

Can the EDMK instruction be used to edit multiple fields? $\qquad$

Yes; However, the address in register 1 will only pertain to the last source field edited.

What happens on an EDMK instruction when significance is started by a significance start character? $\qquad$

No address is placed Does the EDMK instruction insert the floating currency symbol? $\qquad$ in register 1.

No; The symbol must be inserted by subsequent instructions.

The address placed in register 1 is: (Circle one of the following.) a. The location where the currency symbol (such as \$) should be inserted.
b. The location +1 where the currency symbol should be inserted.
b; Register 1 has the address of the 1st significant digit. The currency symbol (such as $\$$ ) should be placed just to the left of this digit.

What instruction can be used to reduce the address in register 1 by one?

Branch on By using the $R R$ format and an $R 2$ field of zero, register 1 can be reduced Count; with- For example: out a branch.


After the BCTR instruction, the "move character" instruction (MVC) can use register 1 as a base register and move a dollar sign (currency symbol) into the desired location. A. "move immediate" (MVI) instruction with the currency symbol as the immediate operand could also be used.

You have now completed your study of the System/360 standard instruction set with the decimal feature. You have not yet studied I/O operations. These will be covered in your next self-study book. For now, let's take a look at some programming examples.

# System/360 Branching,Logical and Decimal Operations 

| Section I: | Branching Operations |
| :--- | :--- |
| Section II: | Logical Operations |
| Section III: | Decimal Operations |
| Section IV: | Analyzing Decimal Feature Programs |

SECTION IV LEARNING OBJECTIVES

At the end of this section, you should be able to use decimal feature instructions to do the following:

Write programs, using stored data in the form of zoned or packed decimal, to solve the following equations.

| $\mathrm{A}+\mathrm{B}$ | $=\mathrm{C}$ |
| :--- | :--- |
| $\mathrm{A}+\mathrm{B}-\mathrm{C}$ | $=\mathrm{D}$ |
| $\mathrm{A} \times \mathrm{B}$ | $=\mathrm{C}$ |
| $\mathrm{A} \div \mathrm{B}$ | $=\mathrm{C}$ |
| $\mathrm{A} \times \mathrm{B}$ | $=\mathrm{D}$ |

## Analyzing Decimal Feature Programs

Notice: This section of the decimal operations is very important. Your $\overline{\text { ability }}$ to learn the System/360 and ultimately, to service the system, will depend upon your understanding of the following material. The material will require much effort and concentration. Don't expect it to be easy. Use the Principles of Operation manual for reference and/or review whenever you are unsure of the details of a branching, logical, or decimal instruction.

Remember, now is the time and here is the place to learn.

To make the following programs easier to read, we are using symbolic instructions. The symbolic instruction format similar to, but not necessarily identical to, the source language format required by the System/360 Assembler Program.

The RR format is shown this way:

$$
\text { Mnemonic } \quad R 1, \mathrm{R} 2
$$

Write the machine language instruction generated by the following symbolic statement: (The hex Op code for AR is 1A.)


The RX format is shown this way:

$$
\text { Mnemonic } \quad \mathrm{R} 1, \mathrm{D} 2(\mathrm{X} 2, \mathrm{~B} 2)
$$

Note - Decimal notation is used instead of hexadecimal in the symbolic format.

Write (in hex) the machine language instruction that corresponds to the following: (45 is the hex Op code for BAL.)

$$
\mathrm{BAL} \quad 15,2048(0,0)
$$




The RS format is shown this way:

$$
\text { Mnemonic } \quad \mathrm{R} 1, \mathrm{R} 3, \mathrm{D} 2(\mathrm{~B} 2)
$$

Write the machine language instruction that corresponds to the following: ( 86 is the hex Op code)

$$
\text { BXH } \quad 2,4,3840(3)
$$



The SI format is shown this way:
Mnemonic $\quad$ D1 (B1), I2
Write the machine language instruction for the following: (94 is the Op code)

NI $\quad 2048(0), 240$


The SS format will be shown this way for an 8-bit length code:
Mnemonic
D1 (L, B1), D2 (B2)

The SS format will be shown this way for instructions with two 4-bit length codes.

Mnemonic $\quad$ D1 (L1, B1), D2 (L2, B2)
Show the machine language instruction for the following: Note: 1. Op code is D2.
2. Symbolic length code is = total \# of bytes.

MVC $2048(256,0), 3840(0)$


| D2 | FF | 0 | 800 | 0 | $F 00$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

Show the machine language instruction for the following: (Op code is FD) DP $\quad 2048(15,0), 3840(8,0)$


## PROGRAM \#1

|  |  |  |
| :--- | :--- | :--- |
| BALR | 4,0 |  |
| LA | $6,2048(0,0)$ |  |
| ZAP | $4(2,6), 2(2,6)$ |  |
| AP | $4(2,6), 0(2,6)$ |  |
|  |  |  |
| Storage contains 017 C | 402 C | 0000 |

What would be the contents of locations 2048 through 2053 after Program \#1 is executed?

017C 402C 419C If you had the correct answer, proceed to Program \#2. Otherwise, continue on with the step-by-step analysis of Program \#1.

The 1st instruction is a "branch and link" instruction using the $\qquad$ format.

RR
Because the R2 field of the BALR instruction is zero, a branch $\qquad$ (does/does not) occur.
does not
What is placed in general register 4 as a result of the BALR instruction?
$\qquad$

The address of the next instruction's (LA) Op code.
NOTE: General register 4 is not used in Program \#1. However, it does provide us with a means of branching back to the program if we had wanted to.

The second instruction is "load address." The generated effective address will be loaded into register $\qquad$ .

6
Show (in hex) the contents of bits $8-31$ of register 6 after the LA instruction is executed. $\qquad$

000800
The 3 rd instruction will cause byte locations $\qquad$ through $\qquad$ to be placed in locations $\qquad$ through $\qquad$ .
$\qquad$

Note that in these symbol instructions, the length code is equal to the total number of bytes. Of course, in actual machine language instructions, the length code is one less than the total number of bytes.

What will be the contents of locations 2048-2053 after the ZAP instruction is executed? $\qquad$

017C 402C 402C . The last instruction of Program \#1 will cause byte locations ___ through $\qquad$ to be added to locations $\qquad$ through $\qquad$ .

2048, 2049
2052, 2053

What will be the contents of locations 2048-2053 after Program \#1 is executed? $\qquad$

PROGRAM \#2

| 017 C | $402 \mathrm{C} \quad 419 \mathrm{C}$ | LA | $1,16(0,0)$ |
| :--- | :--- | :--- | :--- |
|  |  | LA | $2,2048(0,0)$ |
|  |  | BALR | 3,0 |
|  |  | ZAP | $2(4,2), 0(2,2)$ |
|  |  | MP | $2(4,2), 0(2,2)$ |
|  |  | DP | $2(4,2), 0(2,2)$ |
|  |  | BCT | $1,6(0,3)$ |

Locations 2048-2053 contain 016C00000000

What will be the contents of locations 2048-2053 after Program \#2 is executed for the first time? $\qquad$


There will be a program interrupt during the 2 nd execution of the program. What exception will cause this program interrupt? $\qquad$

Data; The second time the "multiply" instruction is executed, the sign of the quotient will be recognized as an invalid packed decimal digit. To avoid this exception, the DP instruction should be followed by a ZAP instruction as shown below.

$$
\text { ZAP } \quad 2(4,2), 2(2,2)
$$

For your convenience, this is a repeat of Program \#2.

| LA | $1,16(0,0)$ |
| :--- | :--- |
| LA | $2,2048(0,0)$ |
| BALR | 3,0 |
| ZAP | $2(4,2), 0(2,2)$ |
| MP | $2(4,2), 0(2,2)$ |
| DP | $2(4,2), 0(2,2)$ |
| BCT | $1,6(0,3)$ |

Locations 2048-2053 contain 016 C 00000000

If you were able to answer the preceding questions correctly, proceed to Program \#3. Otherwise, continue with the following step-by-step analysis of Program \#2.

Show (in hex) the contents of general register 1 after executing the 1st

00000010 ; A value of 16 was loaded into register 1.
instruction of Program \#2.

Show (in hex) the contents of register 2 after the 2 nd instruction is executed.
$\qquad$
$\qquad$

The 3rd instruction is a "branch and link."
a. What address is placed in Register 3 ? $\qquad$
b. Does a branch occur? $\qquad$
a. The address of the Op code (ZAP) of the following instruction.
b. No; Because the R2 field is zero.
$\qquad$
Show the contents of locations 2048-2053 after the ZAP instruction is executed. $\qquad$

016 C 0000016 C Show the contents of locations 2048-2053 after the "multiply decimal" instruction is executed for the first time.

Show the contents of locations 2048-2053 after the "divide decimal" instruction is executed for the first time. $\qquad$
$\qquad$


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After a "divide decimal" instruction, the remainder is placed in the low order of the dividend field. All remainders (even zero) are the same length as the original $\qquad$ .

| divisor | The final instruction of Program \#2 is a "branch and count." Show (in hex) |
| :--- | :--- |
| the contents of register 1 after this instruction is executed for the 1st |  |
| time. |  |

0000000F; The register was reduced by one from 16 to 15 .

Since the contents of register 1 were not reduced to zero, a branch _ (will/will not) occur.
will On the System/360, a branch is taken by replacing $\qquad$ with the "branch to" location.
the instruction address portion of the PSW (bits 40-63)

What will be placed in PSW bits $40-63$ after the BCT instruction is executed?

The contents of register 3 plus a displacement value of 6 ; This effective address is the location of the "multiply decimal's" Op code.

What will happen the 2nd time the "multiply decimal" instruction is executed? $\qquad$
$\qquad$

A data exception will be recognized and cause a program interrupt. This occurs because the multiplicand (2050-2053) contains an invalid digit code.
$\begin{array}{lllll}016 \frac{\mathrm{C}}{\mathrm{C}} & 0 & 00 \mathrm{C} \\ & \text { Invalid }\end{array}$

Continue on to Program \#3.

The following 80 character EBCDIC card record is in locations 3840-3919 of main storage:

| Columns 1-6 | Man Number |  | Field A |
| :--- | :--- | :--- | :--- |
| Columns 10-12 | Hours Worked | (XX. X) | Field B |
| Columns 15-17 | Pay Rate | (X. XX) | Field C |
| Columns 20-24 | Deductions | (XXX. XX) | Field D |
| Columns 30-34 | Gross Pay | (XXX. XX) | Field E |
| Columns 40-44 | Net Pay | (XXX. XX) | Field F |

Given the above information, write a program that will calculate gross and net pay using the instructions of the decimal feature. Remember now, that the data you are working with is in EBCDIC (zoned decimal). The data in fields C, D, E, and F will eventually be sent to an output device and must end up in the proper data format.

Which of the following equations will solve for net pay? The fields are lettered from A to F as shown above.
a. $\quad \mathrm{F}=\frac{\mathrm{B} \times \mathrm{C}}{\mathrm{D}}$
b. $\quad \mathrm{F}=\mathrm{B} \times \mathrm{C}-\mathrm{E}$
c. $\quad \mathrm{F}=\mathrm{E}-\mathrm{D}$
c; Gross pay -
Write the equation that will solve for gross pay.
Deductions $=$ Net Pay
$\mathrm{E}=\mathrm{BxC}$
Now that we know the formula to use in solving our problem, the next step is to flowchart our program. Draw the flowchart you intend to use. NOTE: The data you are using is in EBCDIC.


Your flowchart should be similar to this one. If it is different, resolve the differences before continuing.

Using your flowchart, write the necessary symbolic instructions to solve the program. Assume your program will start at location 2048 and that register 1 contains 2048 as a base address. Remember to adjust the decimal point after a multiplication.

NOTE: Card record in locations 3840-3919

| PACK | 1821 | $(5,1), 1801(3,1)$ |
| :---: | :---: | :---: |
| PACK | 1806 | $(3,1), 1806$ (3, 1) |
| PACK | 1811 | $(5,1), 1811(5,1)$ |
| MP | 1821 | $(5,1), 1806$ (3, 1) |
| MVO | 1821 | $(5,1), 1821$ (4, 1) |
| MVC | 1831 | $(5,1), 1821$ (1) |
| SP | 1831 | $(5,1), 1811$ (5, 1) |
| UNPK | 1806 | $(3,1), 1806$ (3, 1) |
| UNPK | 1811 | $(5,1), 1811(5,1)$ |
| UNPK | 1821 | $(5,1), 1821$ (5, 1) |
| UNPK | 1831 | $(5,1), 1831(5,1)$ |

Your answer should agree to some extent with the above answer. If it does not, try to correct any differences before continuing on to Program \#4.

A man borrows $\$ 1,000$ from a bank. He agrees to pay off the debt in one year. As a result, a $6 \%$ service charge is added on to the principle.

Draw a flowchart for a program that will do the following:
a. Calculate the man's monthly payment.
$\left.\begin{array}{lr}\text { Principle } & \$ 1,000.00 \\ \text { Service Charge } & .06 \\ \text { No. of Monthly Payments } & 12 \\ \text { New Principles } & \text { XXXX. XX } \\ \text { Monthly Payment } & \text { XX. XX }\end{array}\right\}$ In Packed Decimal


Your flowchart should be similar to the preceding answer. Now write the necessary instructions that will make up the program. Your program may start anywhere in main storage, so load register 6 with the base address using the "branch and link" instruction. Assume the following data will be located 2050 bytes from the beginning of the program.

| 7 | Bytes | +100000 |
| :--- | :--- | :--- |
| 1 | Byte | +6 |
| 2 | Bytes | +12 |
| 7 | Bytes | New Principle |
| 7 | Bytes | Monthly Payment |$\quad$ In Packed Decimal


| BALR | 6,0 |
| :--- | :--- |
| MVC | $2058(7,6), 2048(6)$ |
| MP | $2058(7,6), 2055(1,6)$ |
| MVN | $2063(1,6), 2064(6)$ |
| ZAP | $2058(7,6), 2058(6,6)$ |
| AP | $2058(7,6), 2048(7,6)$ |
| MVC | $2065(7,6), 2058(6)$ |
| DP | $2065(7,6), 2056(2,6)$ |
| ZAP | $2065(7,6), 2065(5,6)$ |

Your solution should be similar to the preceding answer to corrent any differences before continuing to Program \#5.

PROGRAM \#5

The Indians sold the island of Manhattan to a foreign real estate firm 332 years ago for $\$ 24.00$ and a pair of wooden shoes. They converted the shoes into toy boats and deposited the money in a savings account where it has been drawing interest all these years at $3 \%$ compounded annually.

Draw a flow chart that will solve for the present value of the Indians' principle. You will be given only the following data which is displaced 500 bytes from the beginning of your program. Use register 1 for the base register and register 2 as a counter (use the "load address" instruction to initially set the counter).
$\left.\begin{array}{ll}* 5 \text { bytes } & +2400 \\ 1 \text { byte } & +3 \\ 5 \text { bytes } & \text { New Principle }\end{array}\right\} \quad$ In Packed Decimal
*The New Principle will not exceed 10 digits.


The preceding flowchart was more complicated than it need be. This was because you're given a constant of +3 to use as the Rate. As a result, you had to figure out the interest and then add the previous principle to it. If you had been given a constant of +103 to use, the flowchart could have been simpler.

Draw a flowchart to solve the previous problem. All information remains the same except this time you are given a two-byte constant of +103 rather than one byte of +3 .


Using the preceding flowchart, write the necessary symbolic instructions that will do the job. The following packed decimal data is displaced 500 bytes from the beginning of the program.

Beginning address of program $+500 \longrightarrow+$\begin{tabular}{l}
Data <br>
Beginning address of program $+505 \longrightarrow 2400$

$\quad$

(5 bytes) <br>
$(2$ bytes $)$
\end{tabular}

BALR 1, 0 Load Base Register
LA $2,332(0,0)-$ Load Counter
MP $\quad 498(5,1), 503(2,1)$
MVN $501(1,1), 502$ (1)
ZAP $498(5,1), 498(4,1)$
BCT $2,4(0,1)$
Your program should look similar to the one above. Notice that there is no "halt" instruction to end the program. Since the System/360 will usually operate under control of a supervisor program, a "supervisor call" instruction could be used to indicate the end of the program.

Do you need a review? If you think that you may require a review of certain areas of this book, do the following:

Read the learning objectives at the beginning of each section.
You should review only those areas where you think that you cannot do what the objectives indicate.

Starting on the next page is a self-evaluation quiz. It will allow you to check your understanding of decimal operations.

## REVIEW QUESTIONS FOR BRANCHING, LOGICAL, AND DECIMAL OPERATIONS

- Use only the Appendix section of the Principles of Operation manual to answer these questions. When you are done, check your answers with the answers on page 141, and allow yourself five points for each correct answer. If your score is less than 80 , review the areas of this text that correspond with the questions answered incorrectly.

1. Branching is accomplished by:
a. Storing the PSW and fetching a new PSW.
b. Replacing the entire PSW with the 'branch to address. "
c. Replacing bits $40-63$ of the PSW with the "branch to address."
d. Adding bits 40-63 of the PSW to the effective generated address.
e. None of the above.
2. Which of the following M1 (Mask) fields would be used by a 'branch on condition" instruction to check only for a condition code of 11 ?
a. 0011
b. 1100
c. 1000
d. 0001
e. 1111
3. Which of the following "branch" instructions will always retain the previous contents of the PSW's instruction address?
a. Branch on Condition
b. Branch on Count
c. Branch and Link
d. Branch on Index High
e. Branch on Index Low or Equal
4. The "branch on count" instruction will:
a. Add a value of 1-16 to the first operand and unconditionally branch.
b. Add a value of 1 to the first operand and branch if there is a high order carry.
c. Subtract a value of 1 from the first operand and branch if the result is zero.
d. Branch if the count in the first operand has been reduced to zero by a previous instruction.
e. Subtract a value of 1 from the first operand and branch if the result is not zero.
5. The "branch on index high" instruction will branch after:
a. Reducing the first operand by 1 and comparing the result with a second operand.
b. Adding the second operand to the first operand and comparing the sum with a third operand.
c. Comparing the second operand to the first operand.
d. Using an index register to generate the "branch to address."
e. Determining that the value in the index register is greater than that in the base register.
6. Examine the following symbolic program. The starting address is decimal 2000.

| BALR | 1,0 |
| :--- | :--- |
| LA | $1,0(0,1)$ |
| LA | $2,8(0,1)$ |
| LPR | 2,2 |
| BCTR | 1,2 |

How many times will the "load positive" instruction be executed?
a. 2000
b. 2002
c. 2004
d. 2006
e. None of the above.
7. Which of the following symbolic instructions would zero out register 2.
a. $\mathrm{SR} \quad 2,2$
b. SLL 2, 0032 (0)
c. XR 2, 2
d. All of the above.
e. None of the above.
8. The "move zones" instruction
a. Moves bits $0-3$ of the second operand bytes into bits $0-3$ of the first operand.
b. Zeros out the zones of the first operand.
c. Processes the bytes in a right to left direction.
d. Can only move the bits from a maximum of sixteen bytes.
e. None of the above.
9. The "move with offset" instruction:
a. Does not change the right-most four bits in each byte of the first operand.
b. Moves a field from the second operand into the first operand, displacing it four bits to the left.
c. Processes the bytes in a left to right direction.
d. All of the above.
e. None of the above.
10. What is the result of the following "and" instruction?

a. 00000000
b. 00000001
c. FFFFFFFE
d. FFFFFFFF
e. None of the above.
11. What is the result of the following "exclusive or" instruction (SI format)?

a. 00
b. 55
c. 66
d. FF
e. None of the above.
12. The "compare logical" instruction can be used to compare:
a. Alphanumeric information
b. Zoned decimal operands
c. Packed decimal operands
d. All of the above.
e. None of the above.
13. Examine the following symbolic program.

LA $5,2048(0,0)$
LA $5,0(5,5)$
LA $6,0(5,5)$
LA $7,0(6,5)$
Indicate the base address (decimally) that will be in register 6 at the end of the program.
a. 2048
b. 4096
c. 6144
d. 8192
e. 10240
14. The "translate" instruction can be used to translate bytes of data:
a. From one character code to any other character code.
b. Only from EBCDIC to some other character code.
c. Only to EBCDIC from some other character code.
d. Only from ASCII to EBCDIC.
e. None of the above.
15. Given the following "translate" instruction and an argument byte (in hex), choose the correct statement.
TR INSTRUCTION

| DC | 00 | 0 | 800 | 0 | $F 00$ |
| :---: | :---: | :---: | :---: | :---: | :---: |

ARGUMENT BYTE $\rightarrow$ F7
a. The argument byte will be replaced by the function byte from hex location 0008 F7.
b. The argument byte will be replaced by the function byte from hex location 000FF7.
c. The argument byte will replace the function byte at hex location 0008F7.
d. The argument byte will replace the function byte at hex location 000FF7.
e. None of the above.
16. After a "translate and test" instruction, a condition code of 01 would mean:
a. No significant character was located.
b. All the argument bytes were used and a significant character was located.
c. One or more significant characters were located.
d. One significant character was located and replaced with a function byte.
e. One significant character was located and its address is in register 1.
17. Which of the following can cause a decimal overflow on an AP instruction?

| 1st operand | 2nd operand |
| :--- | :--- |
| $\quad 479 \mathrm{C}$ | 520 C |
| a. 472 C | 00376 C |
| b. $\quad 047 \mathrm{C}$ | 01000 C |
| c. |  |
| d. All of the above. |  |
| e. None of the above. |  |

18. Show the storage contents after executing the following "multiply decimal" instruction.
MP INSTRUCTION

| FC | 1 | 0 | 0 | 100 | 0 | 102 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

HEX LOCATIONS $100-102 \rightarrow 09706 C$

| a. | 58 | 2 D | 6 C |
| :--- | ---: | ---: | ---: |
| b. | 00 | 58 | 2 D |
| c. | 58 | 2 C | 6 C |
| d. | 00 | 58 | 2 C |
| e. | 09 | 7 D | 6 C |

19. Which of the following pattern fields would be necessary in order to produce the following edit result?

| Source Fields | $00076 \mathrm{D} \quad$ in packed decimal digits |
| :--- | :--- |
| Edited Fields | $* * * * .76 \mathrm{~b} \mathrm{CR} \mathrm{b}$ |

a. $\quad * d d d . d d b c R b$
b. $\quad * d d d . d d b b b b$
c. $\quad \mathrm{bdd})$. $\mathrm{dd} \mathrm{d}^{* * * *}$
d. $* * *)$ ) ddbCR b
e. $\quad * \mathrm{dd}) . \mathrm{ddb} C R \mathrm{~b}$
20. The "edit and mark" instruction will:
a. Edit the field and put the dollar sign next to the most significant digit.
b. Edit the field and put the address of the most significant digit minus 1 in register 1.
c. Edit the field and put the address of the most significant character in register 1.
d. Not edit the field.
e. Not edit the field but will set the condition code to 00 if no significant characters are located.

## ANSWERS TO REVIEW QUESTIONS

1. c
2. d
3. c
4. e
5. b
6. b
7. d
8. a
9. b
10. d
11. b
12. a
13. d
14. a
15. b
16. e
17. c
18. a
19. e
20. c

You have now completed your study of the System/360's standard instruction set and the decimal feature with the exception of input-output operations. These I/O operations will be covered in your next self-study book.

Before proceeding to the next book of this System/360 Introductory Programming Course, fill out and return the Course Evaluation Sheet (located in the back of this book).

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## Book 4 System/360 Branching,Logical and Decimal Operations Student Course Evaluation

You can make this course and all future courses more useful by answering the questions on both sides of this sheet and giving us your comments.

Do you feel that you have an adequate understanding of the learning objectives that are listed at the beginning of the following sections?
Section I: Branching Operations
Section II: Logical Operations
Section III: Decimal Operations
Yes
Yes
YesNo $\qquad$ Section IV: Analyzing Decimal
Feature Programs
Yes
No $\qquad$

List any technical errors you found in this book.

## Comments

| Student Name | Man Number | B/O Number | Area Number |
| :---: | :---: | :---: | :---: |
| Student: Please review this evaluation with the person administering the course; then remove it from the book and send to the FE Education Center via IBM mail. <br> - Were you given a copy of this text to write in and keep? . . . . . . . . . Yes $\square$ No $\square$ <br> - How many hours per day were scheduled for this course? <br> - Were you interrupted during this time? . . . . . . . . . . . . . . . . . . Yes $\square$ No $\square$ <br> - How many hours were needed to complete this course? <br> - Did you require assistance during this course? . . . . . . . . . . . . . . Yes $\square$ No $\square$ (If your answer is yes, explain in the comments section) <br> - Indicate your understanding of the total course. Excellent $\square$ Good $\square$ Fair $\square$ Poor $\square$ |  |  |  |
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[^0]:    Copies of this and other IBM publications can be obtained through IBM Branch Offices. Address comments concerning the content of this publication to: IBM, FE Education Planning, Dept. 911, Poughkeepsie, N. Y., 12602

[^1]:    1 - Hex;
    $0001 \longleftarrow$ Binary
    Tests for a condition code of 11

[^2]:    COND. CODE O1

[^3]:    $* * * * * * * .69 * * *$; Note that the use of an asterisk as the fill character will provide asterisk check protection.

