A Quick User Guide on

Peking University-Stanford University Resistive Random Access Memory (RRAM) SPICE Model

Version: 2.0Beta

Patent Pending.

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1. Model Files

Table 1. Summary of Model Files

File Name	Description
RRAM_v2.0Beta	RRAM SPICE Model File

Additional Files

File Name	Description
User Guide	
RRAM Model v2.0Beta Quick User Guide.pdf	This User Guide in PDF format.
References/Publications	[1]-[5]
Sample Decks	
test_RRAM_SET.sp	Example HSPICE decks: SET operation
test_RRAM_RESET.sp	Example HSPICE decks: RESET operation
AC_RRAM_SET.sp	Example HSPICE decks: SET pulse
AC_RRAM_RESET.sp	Example HSPICE decks: RESET pulse

This documentation pertains to the model files in the RRAM SPICE Model v2.0Beta package. A brief summary and description of the model files included in the package are shown in Table 1. This model is a beta-version intended for advanced users. There are still issues such as occasional non-convergence. Please report issues to the developers. For users who prefer a more stable model, please download RRAM v1.0.0 from the NCN NEEDS: https://nanohub.org/publications/19

The package should include all and only these files, plus this User Guide document. A summary of the model scope is in *2. Scope of the Model*; details regarding model usage and instantiation can be found in *3. Model Usage*; and *4. Model Description and Parameters* describes the model assumptions and default parameters. *5. Sample results*.

2. Scope of the Model

Table 2 below summarizes the scope of the model.

Table 2. Summary of the Scope of the RRAM Model

Device Types	Metal-Oxide Bipolar RRAM
Device Dimensions:	
Switching Layer Thickness	~2 nm - 5 nm
Formed filament width	~1 nm - 5 nm
Initial filament width	~0.5 nm
Cell Size	~5 nm × 5 nm to 100 μm × 100 μm
Number of RRAMs / device	1 to Unlimited
Physics Aspects & Practical Non-idealities:	
Filament Growth	Two-dimensional growth of one dominant filament
Electronic Conduction	Combined: Ohmic & generalized tunneling mechanism
Device parasitic effects	RC components of MIM structure
Temperature and Heat Conduction	Joule heating
Variations: Resistance States	Included
Variations: Switching Voltages	Included
Dynamic Current Fluctuations	Included for RESET process

This model was designed for fast and accurate simulation of metal-oxide based RRAM devices [1]. The model captures typical DC and AC electrical behaviors of metal-oxide based RRAM devices with physics-based compact model descriptions. The model assumes a conductive filament (CF) evolution process described by a change of the CF geometry during SET/RESET processes under various bias conditions. The core of the model is a two-dimension description of CF, which includes both CF gap region and the CF width as the control variables, where the CF dimensions are not limited. Parasitic effects are also modeled, including both parasitic resistance of switching layer and electrodes, and parasitic MIM capacitance. Intrinsic variation effects such as statistical distributions of resistance states and switching voltages after SET/RESET processes as well as current fluctuations during RESET are supported, which has made this model the first one supporting the complete suite of RRAM variation effects to date. Since the model invoked in HSPICE or other SPICE software is a two-terminal component, it can thus be easily implemented in any circuit including memory array structures such as 1R, 1D1R, 1T1R and 1S1R [2]-[4].

3. Model Usage

The model is developed in Verilog-A, and can be instantiated in HSPICE or other SPICE tools (with the appropriate Verilog-A support). This section illustrates how to instantiate the model in HSPICE.

3.1 Model Variants – Standard Model vs. Dynamic Model

Two model variants are available:
1) Standard RRAM Model (if parameter "switch" == 0)
2) Dynamic RRAM Model (if parameter "switch" == 1)
The Standard Model is recommended for describing the ensemble-average DC switching behavior. The Dynamic Model is recommended for applications that involve dynamic current fluctuations and variations of RRAM cell characteristics.

3.2 Convergence and Settings

For improved accuracy and convergence, include the following lines of code at the beginning of the SPICE deck:

```
**************************************************
.option converge = 0
.option RUNLVL = 6
.option METHOD=GEAR
**************************************************
```

3.3 Model Instantiation

To instantiate the devices in the model, the library must be included at the beginning of the SPICE deck.

```
.hdl RRAM_v2.0Beta.va
```

The Verilog-A compiler should automatically compile the Verilog-A model when the SPICE deck is compiled. The Verilog-A compilation should only occur the first time the model is used and can take a few minutes. Afterwards, the model does not need to be recompiled for different simulation runs or different SPICE decks.

To instantiate an RRAM device, use the appropriate syntax below. The usage of this model is similar to that of the Si CMOS transistor model.

* Standard RRAM Model
-Hspice 2013.03 SP2
X_RRAM TE BE RRAM_v2.0Beta < **switch = 0 Parameter_Name = Parameter_Value**>

*Dynamic RRAM Model
-Hspice 2013.03
X_RRAM TE BE RRAM_v2.0Beta < **switch = 1 Parameter_Name = Parameter_Value**>

The port definitions, *TE and BE,* for the RRAM are for the top electrode and the bottom electrode, respectively. The ports *TE* and *BE* are not interchangeable in this model due to nature of the asymmetry of the RRAM programming mechanism and the details of the model implementation.

The device parameters indicated in the < ... > are optional and can be set differently for each device instance. If the device parameters are omitted, default or global values set in the parameter definition file are used. The syntax for setting a parameter is: *parameter_name = value or parameter*

Please see Table 3 for the definitions and default values of the device parameters.

Figure 1 illustrates the basic physical model for the set and reset programming of the RRAM [1]. Figure 2 shows the model assumptions for the filament evolutions processes and corresponding models of electrical transport and parasitic effects.

4. Model Assumptions and Parameters

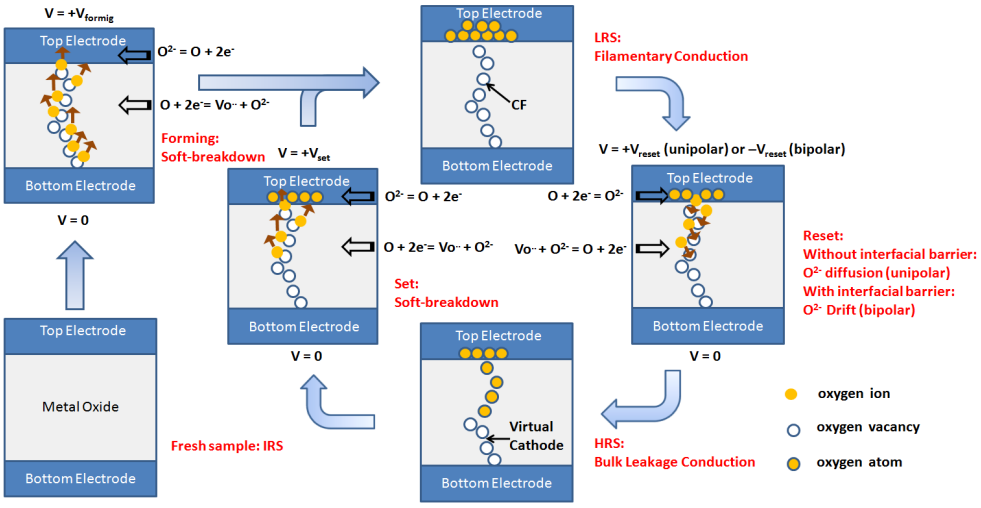

Fig. 1. Schematic of RRAM operation mechanisms, which serve as the physical basis of the analytical SPICE model.

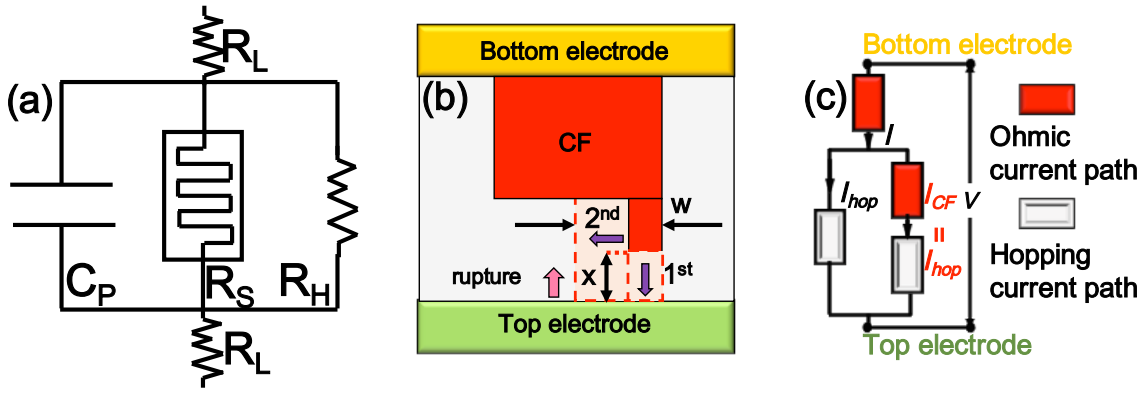

Fig. 2. Illustration of the RRAM SPICE model. (a) Equivalent circuit of RRAM cell composed of resistive switching element and parasitic elements. (b) Schematic of conductive filament evolution. (c) Equivalent circuit of resistive switching element modeling the metal-like and hopping current paths.

Table 3. Model Parameter Descriptions and Default Values			
Parameters	Descriptions	Default Value	Suggested Range[1]
I_0	hopping current density	10^{13} A/m^2	[1e10,1e15]
ρ	resistivity of the CF	19.64 μΩ·m	[0.1,1000]
a	distance between V_O	0.25 nm	[0.2,0.4]
f	V_O vibration frequency	10^{13} Hz	[0.8e13,1.2e13]
E_a	average active energy of V_O	0.7 eV	[0.5,1.2]
E_h	hopping barrier of O^{2-}	1.12 eV	[0.8,1.4]
E_i	electrode/oxide interface	0.82 eV	[0.6,1.2]
α_a & α_h	energy enhancement factor	0.75 nm	0.75
γ	voltage enhancement factor	1.5	1.5
Z & e	charge number & unit charge	1 & e	1 & e
R_{th}	effective thermal resistance	5×10^5 K/W	[2e5,1e6]
R_H	oxide parasitic resistance	200 MΩ	[1e6,1e9]
R_L	electrode contact resistance	20 Ω	(0,25]
C_P	electrode parasitic capacitance	20 fF	(0,25]
L_0	initial switching layer length	3 nm	[1,10]
x_0	initial gap length	{L_0, 0}	L_0/0
WCF	switching layer width	5 nm	[1,10]
Weff	effective width	0.5 nm	0.5
w_0	initial CF width	{0.5 nm, WCF}	(0,WCF]
V_T	characteristic voltage	0.4 V	0.4
T0	ambient temperature	300 K	(4,500)
Switch	"model switch"	0	{0,1}
deltaGap	Gap varying rate	4e-5 m/s	[0,1e-4]
deltaCF	CF width varying rate	1e-4 m/s	[0,5e-4]
crit_x	Gap variation fitting point	0.5 nm	[0, L_0]

[1]The entire range and all possible combinations of the parameters have not been tested. The range listed represents reasonable values based on experimental observations and physical insights. The units should be the same as the default values.

5. Sample Results

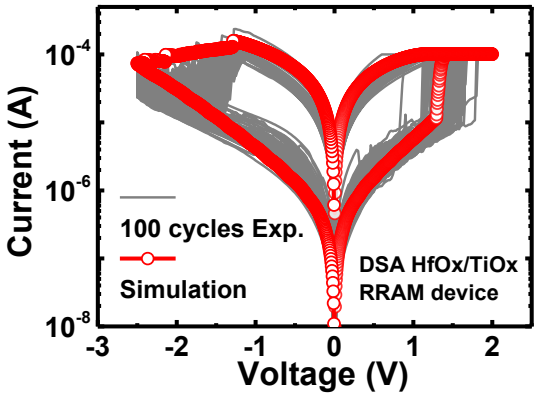

Fig. 3. Typical DC switching I-V curves.

Note: the RRAM SPICE model runs in a dynamic way so that DC characteristics can only be obtained by simulating transient operations under stair-like voltage sweeps similar to realistic measurement setup.

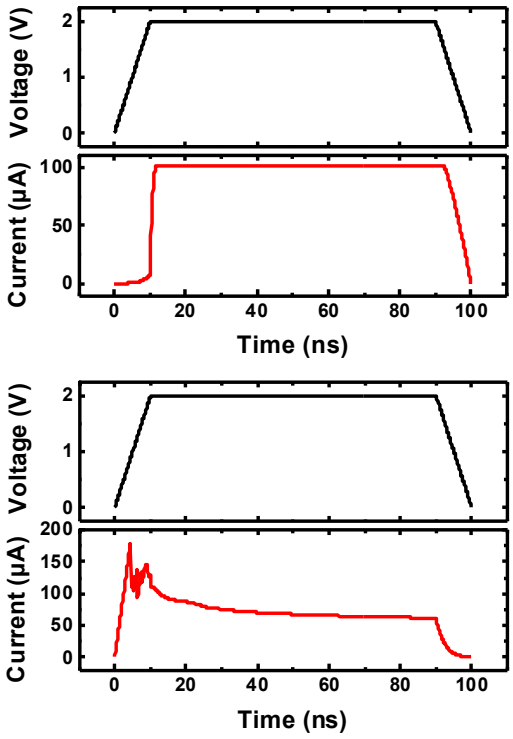

Fig. 4. Typical transient SET and RESET operation with pulse applied.

6. References

[1] H.-S P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. Chen, and M.-J. Tsai, "Metal–Oxide RRAM," *Proceedings of IEEE*, vol.100, no.6, pp. 1951-1970, June 2012, DOI: 10.1109/JPROC.2012.2190369

[2] H. Li, Z. Jiang, P. Huang, Y. Wu, H.-Y. Chen, B. Gao, X. Liu, J. Kang, and H.-S. P. Wong, "Variation-aware, reliability-emphasized design and optimization of RRAM using SPICE model," *Design, Automation & Test in Europe (DATE)*, pp. 1426 – 1430, 2015

[3] Z. Jiang, S. Yu, Y. Wu, J. H. Engel, X. Guan, and H.-S. P. Wong, "Verilog-A Compact Model for Oxide-based Resistive Random Access Memory (RRAM)," *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 41 – 44, 2014. DOI: 10.1109/SISPAD.2014.6931558

[4] H. Li, P. Huang, B. Gao, B. Chen, X. Liu, and J. Kang, "A SPICE Model of Resistive Random Access Memory for Large-Scale Memory Array Simulation," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 211 – 213, 2014. DOI: 10.1109/LED.2013.2293354

[5] X. Guan, S. Yu, and H.-S. P. Wong, "A SPICE Compact Model of Metal Oxide Resistive Switching Memory With Variations," *IEEE Electron Device Lett.,* pp. 1405 – 1407, 2012. DOI: 10.1109/LED.2012.2210856

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