S5P4418

Powered by nexell

Application Processor

Revision 0.10

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User's Manual

SAMSUNG ELECTRONICS

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Chip Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
0.00	Oct. 01, 2014	• First draft	Chongkun Lee
0.10	Oct. 22, 2014	• 2nd draft	Chongkun Lee

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Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

List of Acronyms

Abbreviations/Acronyms	Expanded Form
ADC	Analog Digital Converter
DMAC	Direct Memory Access Controller
ethernet MAC	ethernet Media Access Control
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
JTAG	Joint Test Action Group
LVDS	Low Voltage Differential Signaling
MFC	Multi Format Codec
MPEG-TS	Moving Picture Experts Group-Transport Stream
NFCON	Nand Flash Controller
PDM	Pulse Density Modulation
PPM	Pulse Period Measurement for IR remote receiver
PWM	Pulse Width Modulation
RTC	Real Time Clock
SPDIF	Sony Philips Digital Interconnect Format
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver And Transmitter
VIP	Video Input Processor

1 Product Overview

1.1 Introduction

S5P4418 is a system-on-a-chip (SoC) based on the 32-bit RISC processor for tablets and cell-phones.

Designed with the 28 nm low power process, features of S5P4418 include:

- Cortex-A9 Quad core CPU
- Highest memory bandwidth
- Full HD display
- 1080p 60 frame video decoding and 1080p 30 frame encoding hardware
- 3D graphics hardware
- High-speed interfaces such as eMMC4.5 and USB 2.0

S5P4418 uses the Cortex-A9 quad core, which is 50 % overall performance higher than Cortex-A8 core. It provides 6.4 GB/s memory bandwidth for heavy traffic operations such as 1080p video encoding and decoding, 3D graphics display and high resolution image signal processing with Full HD display. The application processor supports dynamic virtual address mapping, which helps software engineers to fully utilize the memory resources with ease.

S5P4418 provides the best 3D graphics performance with wide range of APIs, such as OpenGL ES 1.1, 2.0.Superior 3D performance fully supports Full HD display. The native dual display, in particular, supports Full HD resolution of a main LCD display and 1080p 60 frame HDTV display throughout HDMI, simultaneously. Separate post processing pipeline enables S5P4418 to make a real display scenario.

1.2 Features

- 28 nm, HKMG (High-K Metal Gate) Process Technology
- 513 pin FCBGA Package, 0.65mm Ball Pitch, 17 × 17 mm Body size
- Cortex-A9 Quad Core CPU
- High Performance 3D Graphic Accelerator
- Full-HD Multi Format Video Codec
- Supports various memory: x32 LPDDR2/3, LVDDR3(Low Voltage DDR3), DDR3 up to 800MHz
- Supports MLC/SLC NAND Flash with Hardwired ECC algorithm (4/8/12/16/24/40/60-bit)
- Supports Dual Display up to 2048x1280, TFT-LCD, LVDS, HDMI 1.4a, MIPI-DSI output
- Supports 3ch ITUR.BT 656 Parallel Video Interface and MIPI-CSI
- Supports10/100/1000M-bit Ethernet MAC
- Supports 3ch SD/MMC, 5ch UARTs,32ch DMAs, 4ch Timer, Interrupt Controller, RTC
- Supports 3ch I2S, SPDIF Rx/Tx, 3ch I2C, 3ch SPI, 8ch 12bit ADC, 3ch PWM and GPIOs, 1ch PPM
- Supports MPEG-TS Serial/Parallel Interface and MPEG-TS HW Parser
- Supports 1ch USB 2.0 Host, 1ch USB 2.0 OTG, 1ch USB HSIC Host
- Supports Security functions (AES, DES/TDES, SHA-1, MD5 and PRNG) and Secure JTAG
- Supports various Power Mode (Normal, Sleep, Deep-Sleep, Stop)
- Supports various boot modes including NAND (with ECC detection and correction), SPI Flash/EEPROM, NOR, USB and UART

1.3 Block Diagram

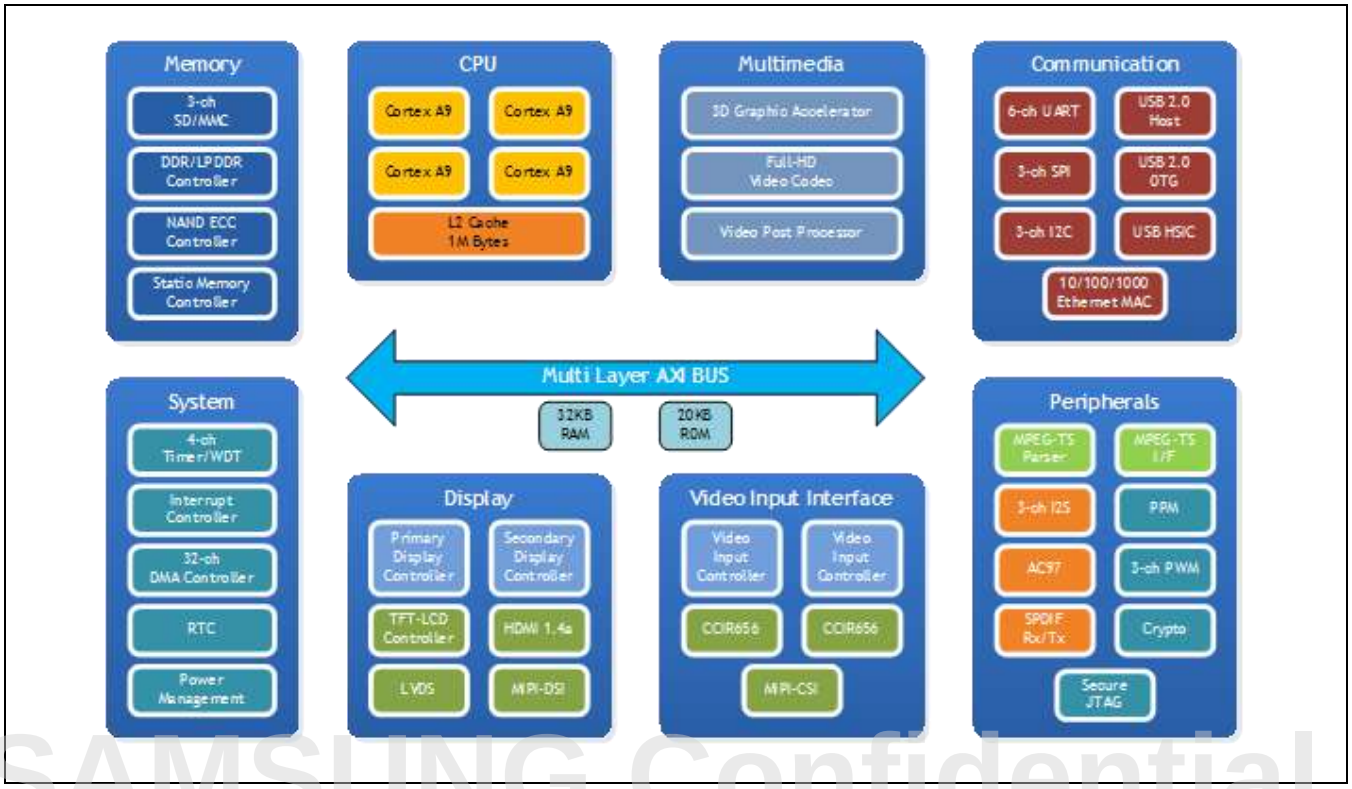


Figure 1-1 Block Diagram

1.4 Brief Functional Specification

1.4.1 CPU

- Cortex-A9 Quad Core
- L1 Cache
  - 32 Kbyte I-Cache, 32 Kbyte D-Cache
- L2 Cache
  - 1 Mbyte Shared Cache
- Co-Processor
  - VFP (Vector Floating Point Processor), Neon Processor

1.4.2 Clock &Power Management

- 4 Spread-Spectrum PLLs
- External Crystal: 24 MHz (for PLL), 32.768 kHz (for RTC)
- Supports for various power mode
  - Normal, Idle, Stop
  - Suspend to RAM (Sleep, Deep Sleep)

1.4.3 DMA

- 32-ch DMAs
- Operation Mode
  - Memory-to-Memory Transfer
  - Memory to IO Transfer, IO to Memory Transfer

1.4.4 Interrupt Controller

- Vectored Interrupt Controller
- Supports 64-ch Interrupt Sources
- Supports following features
  - fixed hardware interrupt priority levels
  - programmable interrupt priority levels
  - hardware interrupt priority level masking
  - programmable interrupt priority level masking
  - IRQ and FIQ generation
  - software interrupt generation
  - test registers
  - raw interrupt status
  - interrupt request status

1.4.5 Timer & Watchdog Timer

- 4-ch Timer with Watchdog Timer
- Normal interval timer mode with interrupt request
- Internal reset signal is activated when the timer count value reaches 0 (time-out)
- Level-triggered interrupt mechanism

1.4.6 RTC

- 32-bit Counter
- Support Alarm Interrupt

1.4.7 Memory Controller

- System Memory Controller
  - Supports LPDDR2/LPDDR3/LVDDR3(Low Voltage DDR3)/DDR3 SDRAM up to 2 Gbytes
  - Supports 1.2 V to 1.5 V power
  - Max Operation Frequency: 800 MHz
  - Data Bus width: 32-bit
- Static Memory Controller
  - Multiplexed Address: up to 24-bit
  - SRAM, ROM and NAND Flash
  - Burst Read/Write
- NAND Flash Controller
  - Supports SLC/MLC NAND Flash
  - Supports MLC NAND Boot
  - Hardwired ECC Algorithm
- 4/8/12/16/24/40/60-bit BCH Error Correction

1.4.8 GPIO Controller

- Various GPIO Interrupt Modes
  - Rising Edge, Falling Edge, High Level, Low Level Detection
- Individual Interrupt Generation

1.4.9 Ethernet MAC Controller

- Standard Compliance
  - IEEE 802.3az-2010, for Energy Efficient Ethernet (EEE)
  - RGMII specification version 2.6 from HP/Marvell
- MAC supports the following features
  - 10, 100, and 1000 Mbps data transfer rates with the following PHY interfaces:
    - RGMII interface to communicate with an external gigabit PHY
  - Full-duplex operation:
    - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
    - Optional forwarding of received Pause frames to the user application
  - Half-duplex operation:
    - CSMA/CD Protocol support
    - Flow control using backpressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
    - Frame bursting and frame extension in 1000 Mbps half-duplex operation
  - Preamble and start of frame data (SFD) insertion in Transmit path
  - Preamble and SFD deletion in the Receive path
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Automatic Pad and CRC Stripping options for receive frames
  - Flexible address filtering modes, such as:
    - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
    - Up to 96 additional 48-bit perfect (DA) address filters that can be selected in blocks of 32 and 64registers
    - Up to 31 48-bit SA address comparison check with masks for each byte
    - 64-bit, 128-bit, or 256-bit Hash filter (optional) for multicast and unicast (DA) addresses
    - Option to pass all multicast addressed frames
    - Promiscuous mode to pass all frames without any filtering for network monitoring
    - Pass all incoming packets (as per filter) with a status report
  - Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 KB of size
  - Programmable Interframe Gap (IFG) (40-96 bit times in steps of 8)
  - Option to transmit frames with reduced preamble size
  - Separate 32-bit status for transmit and receive packets
  - IEEE 802.1Q VLAN tag detection for reception frames
  - Additional frame filtering:
    - VLAN tag-based: Perfect match and Hash-based (optional) filtering
    - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
  - Separate transmission, reception, and control interfaces to the application
  - MDIO master interface (optional) for PHY device configuration and management
  - Standard IEEE 802.3az-2010 for Energy Efficient Ethernet
  - CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control

- Programmable watchdog timeout limit in the receive path

1.4.10 SD/MMC Controller

- 3 Independent SD/MMC Controller and Ports
- Secure Digital Memory (SD mem- version 3.0)
- Secure Digital I/O (SDIO - version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA - version 1.1)
- Multimedia Cards (MMC - version 4.41, eMMC 4.5)
- Supports following features of MMC4.41
- Support following features of eMMC4.5
- Support clock speed up to 50 MHz
- Support PIO and DMA mode data transfer
- Support 1/4-bit data bus widths
  - Overlay SPI signals to same GIOs from SSP/SPI controller

1.4.11 PPM

- Pulse Period Measurement for IR remote receiver

1.4.12 PWM

- 3-ch PWM Controller
- Five 32-bit Timers
- Two 8-bit Clock Prescalers providing first level of division for the PCLK, Five Clock Dividers and Multiplexers providing second level of division for the Prescaler clock and Two External Clocks
- Programmable Clock Select Logic for individual PWM Channels
- Four Independent PWM Channels with Programmable Duty Control and Polarity
- Static Configuration: PWM is stopped
- Dynamic Configuration: PWM is running
- Supports Auto-Reload Mode and One-Shot Pulse Mode
- Supports for two external inputs to start PWM
- Dead Zone Generator on two PWM Outputs
- Supports DMA Transfers
- Optional Pulse or Level Interrupt Generation
- The PWM has two operation modes:
  - Auto-Reload Mode
    - Continuous PWM pulses are generated based on programmed duty cycle and polarity
  - One-Shot Pulse Mode
    - Only one PWM pulse is generated based on programmed duty cycle and polarity

1.4.13 ADC

- 8-ch analog input port
- Supports following features
  - Resolution: 12-bit
  - Conversion rate: 1 MSPS
  - Input range: 0 to AVDD18
  - Input frequency: up to 100 kHz
  - Digital output: CMOS Level (0 to AVDD10)

1.4.14 I2C

- 3-ch I2C bus controller
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; master can operate as master-transmitter or as master-receiver
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF
- Repeated START and early termination function are not support
- High speed mode, combined format, 10bit address are not supported

1.4.15 SPI/SSP

- 3-ch SPI Controller
- Master or slave operation.
- Programmable clock bit rate and prescale.
- Separate transmit and receive first-in, first-out memory buffers, 16 bits wide, 8 locations deep.
- Programmable choice of interface operation, SPI, Microwire, or TI synchronous serial.
- SPI Protocol, SSP Protocol, Microwire Protocol
- DMA request servicing of the transmit and receive FIFO
- Inform the system that a receive FIFO over-run has occurred
- Inform the system that data is present in the receive FIFO after an idle period has expired
- Only support DMA burst length 4
- Maximum SSP CLKGEN's frequency is 100 MHz
- SSP Receive Timeout Period: 64 cycle of SSP CLKGEN's clock
- Max Operation Frequency
  - Master Mode: 50 MHz (Receive Data is 20 MHz)
  - Slave Mode: 8 MHz

1.4.16 MPEG-TS

- Supports Serial & Parallel MPEG-TS Interface
- Supports Hardwired MPEG2-TS parser for Set-top and IPTV

1.4.17 UART& ISO7816 Sim Card Interface

- 5-ch UART controller
- Programmable use of UART or IrDA SIR input/output.
- Separate 32 × 8 transmit and 3 2 ×12 receive First-In, First-Out (FIFO) memory buffers to reduce CPU interrupts.
- Programmable FIFO disabling for 1-byte depth.
- Programmable baud rate generator. This enables division of the reference clock by (1 × 16) to (65535 × 16) and generates an internal × 16 clock. The divisor can be a fractional number enabling you to use any clock with a frequency >3.6864 MHzas the reference clock.
- Standard asynchronous communication bits (start, stop and parity). These are added prior to transmission and removed on reception.
- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts.
- Support for Direct Memory Access (DMA).
- False start bit detection.
- Line break generation and detection.
- Support of the modem control functions CTS, DCD, DSR, RTS, DTR, and RI.
- Programmable hardware flow control.
- Fully-programmable serial interface characteristics:
  - data can be 5, 6, 7, or 8 bits
  - even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - baud rate generation, dc up to UARTCLK/16
- IrDA SIR ENDEC block providing:
  - programmable use of IrDA SIR or UART input/output
  - support of IrDA SIR ENDEC functions for data rates up to 115200 bps half-duplex
  - support of normal 3/16 and low-power (1.41-2.23 μs) bit durations
  - programmable division of the UARTCLK reference clock to generate the appropriate bit duration for low-power IrDA mode.
- Identification registers that uniquely identify the UART. These can be used by an operating system to automatically configure itself.

1.4.18 USB

- 1-ch USB 2.0 Host and 1-ch USB2.0 HSIC Host
  - fully compliant with the Universal Serial Bus Specification, Revision 1.1, Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 2.0, and the openHCI: Open Host Controller Interface Specification for USB, Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.
  - At the USB 2.0 physical interface, the controller provides the following:
- UTMI: UTMI+ Level 3, Revision 1.0
- High-Speed Inter-Chip (HSIC), Version 1.0
  - Supports ping and split transactions
  - UTMI/UTMI+ PHY interface clock supports 30-MHz operation for a 16-bit interface or 60-MHz operation for an 8-bit interface
  - Heterogeneous selection of UTMI+ or HSIC interfaces per port using strap pins. In Heterogeneous mode, only the 8-bit interface (60 MHz) is supported.
- 1-ch USB 2.0 OTG Controller
  - supports both device and host functions and complies fully with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.3a and Revision 2.0. It can also be configured as a host-only or device-only controller, fully compliant with the USB 2.0 Specification.
  - Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.3)
  - Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 2.0)
  - Software configurable to OTG1.3 and OTG2.0 modes of operation
  - Support for the following speeds:
    - High-Speed (HS, 480-Mbps),
    - Full-Speed (FS, 12-Mbps) and
    - Low-Speed (LS, 1.5-Mbps) modes
  - Multiple options available for low power operations
  - Multiple DMA/non DMA mode access support on the application side
  - Multiple Interface support on the MAC-Phy
  - Supports 16 bidirectional endpoints, including control endpoint 0.
  - Supports Session Request Protocol (SRP)
  - Supports Host Negotiation Protocol (HNP)
  - Supports up to 16 host channels. In Host mode, when the number of device endpoints to be supported is more than the number of host channels, software can reprogram the channels to support up to 127 devices, each having 32 endpoints (IN + OUT), for a maximum of 4,064 endpoints.
  - Includes automatic ping capabilities

1.4.19 I2S

- 3-ch I2S Controller for 5.1-ch Audio output
- 16-bit/24-bit Master & Slave Mode
- Supports various interface mode
  - I2S, Left-justified, Right-Justified, DSP mode
- Supports TDM mode for Digital MIC interface
- Supports SPDIF Rx/Tx

1.4.20 AC97

- 1-Ch AC97
- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In
- DMA-based operation and interrupt based operation
- All of the channels support only 16-bit samples
- Variable sampling rate AC97 Codec interface (48 kHz and below)
- 16-bit, 16 entry FIFOs per channel
- Only primary Codec support

1.4.21 SPDIF Tx, Rx

- SPDIF Tx
  - Supports linear PCM up to 24-bit per sample
  - Supports Non-linear PCM formats such as AC3, MPEG1 and MPEG2
  - 2x24-bit buffers which is alternately filled with data
- SPDIF Rx
  - Serial, unidirectional, self-clocking interface
  - Single wire-single signal interface
  - Easy to work because it is polarity independent

1.4.22 PDM

- Supports receiving 2 channel audio data with 1 data pin
  - 1 output clock pin
  - 2 data pins (total 4 channel accepts available)
- Fixed output clock frequency
- Supports select of the timing of data capture
- Supports DMA interface
- Supports a user configuration of Coefficient. (Butterworth Low-pass Filter)

1.4.23 Display Controller

- Supports Dual Display
- Supports 3 Layers, Gamma Correction and Color Control (Brightness, Contrast, Hue and Saturation)
- Supports various Pixel Format
  - RGB/BGR 444,555,565,888 with/without Alpha channel
- Resolution
  - Up to 2048 x 1280 @60 Hz
- Supports various LCD
  - I80 Interface, RGB, Serial RGB, LVDS output
  - Supports MIPI-DSI 4 data lanes
- HDMI Interface
  - HDMI 1.4a, HDCP 1.4 Complaint
  - Supports Video format:
    - 480p @59.94 Hz/60 Hz, 576p@50 Hz
    - 720p @50 Hz/59.94 Hz/60 Hz
    - 1080p @50 Hz/59.94 Hz/60 Hz
    - Primary 3D Video Formats
    - Other various formats up to148 MHz Pixel Clock
  - Supports Color Format: 4:4:4 RGB/YCbCr , 4:2:2 YCbCr
  - Pixel Repetition: Up to x4
  - Supports Bit Per Color: 8-bit, 10-bit ,12-bit (NOTE: 16-bit not supported)
  - Dedicated block for CEC function
  - Supports: Linear-PCM, Non-linear PCM and high-bitrate audio formats (Audio Sample packets and HBR packets for audio transmission)
  - Integrated HDCP Encryption Engine for Video/Audio content protection (Authentication procedure are controlled by S/W, not by H/W)
  - A dedicated CEC module (Separated for power/clock domain separation)
  - SPDIF Interface and I2S interface for Audio Input
  - Supports level-triggered Interrupt and SFR for HPD
  - Supports AES KEY Decryption Function for external HDCP Key management

- LVDS Interface
  - Output clock range: 30M to 90 MHz
  - 35:7 data channel compression up to 630Mbps on each LVDS channel
  - Power down mode
  - Up to 393.75 Mbytes/sec bandwidth
  - Falling clock edge data strobe
  - Narrow bus reduces cable size and cost
  - PLL requires no external component
  - 6 LVDS output channels (5 data channels, 1 clock channel)
- MIPI-DSI
  - Complies to MIPI DSI Standard Specification V1.01r11
    - Maximum resolution ranges up to WUXGA (1920 x 1200)
    - Supports 1, 2, 3, or 4 data lanes
    - Supports pixel format: 16 bpp, 18 bpp packed, 18 bpp loosely packed (3 byte format), and 24 bpp
  - Interfaces
    - Complies with Protocol-to-PHY Interface (PPI) in 1.5 Gbps MIPI D-PHY
    - Supports RGB Interface for Video Image Input from display controller
    - Supports I80 Interface for Command Mode Image input from display controller
    - Supports PMS control interface for PLL to configure byte clock frequency
    - Supports Prescaler to generate escape clock from byte clock

1.4.24 Video Post Processor

- 3D De-interlace Controller
- Fine Scalar for video: Poly-phase filter

1.4.25 Video Input Processor

- Max. 8192 x 8192 resolution support
- Supportsx2 8-bit BT656, 601 format
- Supports MIPI-CSI
  - General Features
    - Support primary and secondary Image format
      - YUV420, YUV420(Legacy),YUV420(CSPS), YUV422 of 8-bits and 10-bits
      - RGB565, RGB666, RGB888
      - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
      - Compressed format: 10-6-10, 10-7-10, 10-8-10
      - All of User defined Byte-based Data packet
    - Support embedded byte-based non Image data packet and generic short packets.
    - Compatible to PPI(Protocol-to-PHY Interface) in MIPI D-PHY Specification
    - Support 4 channel virtual channel or data interleave
  - Standard Compliance
- Compliant to MIPI CSI2 Standard Specification V1.01r06
- D-phy standard specification V1.0

1.4.26 Multi Format MPEG codec

- Decoder
  - H.264
    - BP, MP, HP profile, Level 4.2 up to 1920 × 1080, 50 Mbps
  - MPEG4 ASP
    - Advanced Simple Profile up to 1920 × 1080, 40 Mbps
  - H.263
    - Profile3 up to 1920 × 1080, 20 Mbps
  - VC-1
    - SP/MP/AP profile, Level 3 up to 1920 × 1080, 2048 × 1024, 45 Mbps
  - MPEG-1/2
    - Main Profile, High Level up to 1920 × 1080, 80 Mbps
  - VP8
    - up to 1920 × 1080, 20 Mbps
  - Theora
    - up to 1280 × 720, 20 Mbps
  - AVS
    - Jizhun Profile, Level 6.2 up to 1920 × 1080, 40 Mbps
  - RV8/9/10
    - up to 1920 × 1080, 40 Mbps
  - MJPEG
    - Baseline profile up to 8192 × 8192

- Encoder
  - H.264
    - Baseline Profile, Level 4.0 up to 1080p, 20 Mbps
  - MPEG4
    - Simple Profile, Level 5.6 up to 1080p, 20 Mbps
  - H.263
    - Profile3, Level 70 up to 1080p, 20 Mbps
  - MJPEG
    - Baseline Profile up to 8192×8192

1.4.27 3D Graphic Controller

- Supports OpenGL|ES 1.0 and 2.0
- Supports OpenVG 1.1
- GPU is a hardware accelerator for 2D and 3D graphics systems.
- The GPU consists of:
  - one to four Pixel Processors (PPs)
  - a Geometry Processor (GP)
  - a Level 2 Cache Controller (L2)
  - a Memory Management Unit (MMU) for each GP and PP included in the GPU
  - a Power Management Unit (PMU).
- Pixel processor features
  - each pixel processor used processes a different tile, enabling a faster turnaround
  - programmable fragment shader
  - alpha blending
  - complete non-power-of-2 texture support
  - cube mapping
  - fast dynamic branching
  - fast trigonometric functions, including arctangent
  - full floating-point arithmetic
  - frame buffer blend with destination Alpha
  - indexable texture samplers
  - line, quad, triangle and point sprites
  - no limit on program length
  - perspective correct texturing
  - point sampling, bilinear, and trilinear filtering
  - programmable mipmap level-of-detail biasing and replacement
  - stencil buffering, 8-bit
  - two-sided stencil
  - unlimited dependent texture reads

  - 4-level hierarchical Z and stencil operations
  - Up to 512 times Full Scene Anti-Aliasing (FSAA). 4x multisampling times 128xsupersampling
  - 4-bit per texel compressed texture format.
- Geometry processor features
  - programmable vertex shader
  - flexible input and output formats
  - autonomous operation tile list generation
  - indexed and non-indexed geometry input
  - primitive constructions with points, lines, triangles and quads.
- Level 2 cache controller features
  - sizes of 32 KB
  - 4-way set-associative
  - supports up to 32 outstanding AXI transactions
  - implements a standard pseudo-LRU algorithm
  - cache line and line fill burst size is 64 bytes
  - supports eight to 64 bytes uncached read bursts and write bursts
  - 128-bit interface to memory sub-system
  - support for hit-under-miss and miss-under-miss with the only limitation of AXI ordering rules.
- MMU features
  - accesses control registers through the bus infrastructure to configure the memory system.
  - each processor has its own MMU to control and translate memory accesses that the GPU initiates.
- PMU features
  - programmable power management
  - powers up and down each GP, PP and Level 2 cache controller separately
  - controls the clock, isolation and power of each device
  - provides an interrupt when all requested devices are powered up

1.4.28 Security IP

- On-chip secure boot ROM/RAM
- Hardware Crypto Accelerator
  - DES/TDES, AES, SHA-1, MD5 and PRNG
- Supports Secure JTAG

1.4.29 Unique Chip ID

- Supports 128-bit Unique Chip ID register

1.4.30 Operating Conditions

- Operation Voltage
  - Core: 1.0 V
  - CPU: 1.0 V to 1.3 V
  - DDR Memory: 1.2 to 1.5 V
  - I/O: 3.3 V
- Operation Temperature
  - T.B.D

1.4.31 Package

- 513 pin FCBGA
- Ball Pitch: 0.65 mm
- Body Size: 17 × 17 mm

2 Mechanical Dimension and I/O Pin Description

2.1 Mechanical Dimension

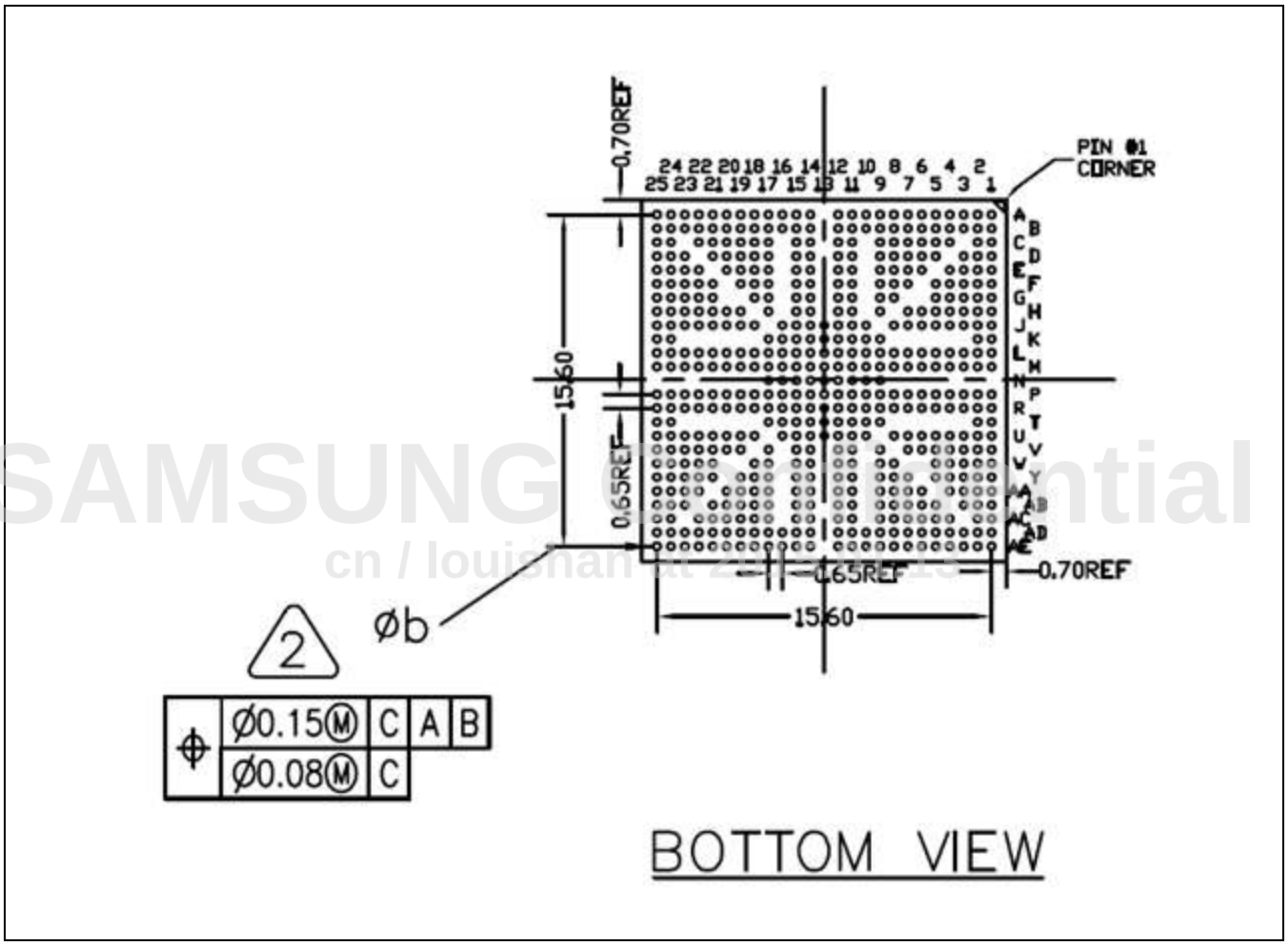


Figure 2-1 Mechanical Dimension - Bottom View

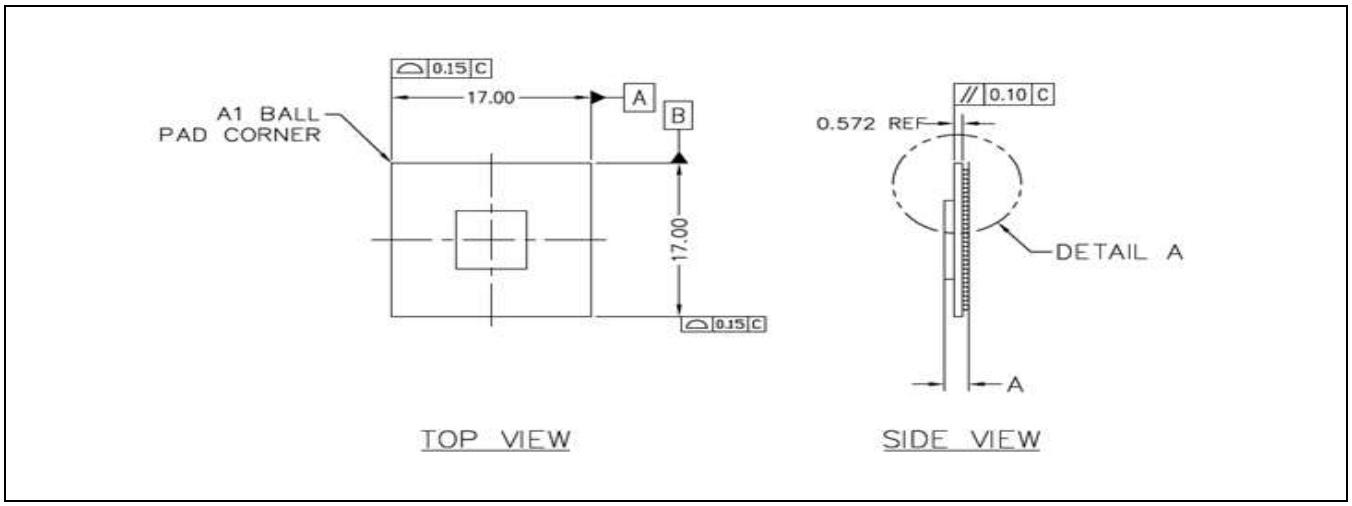
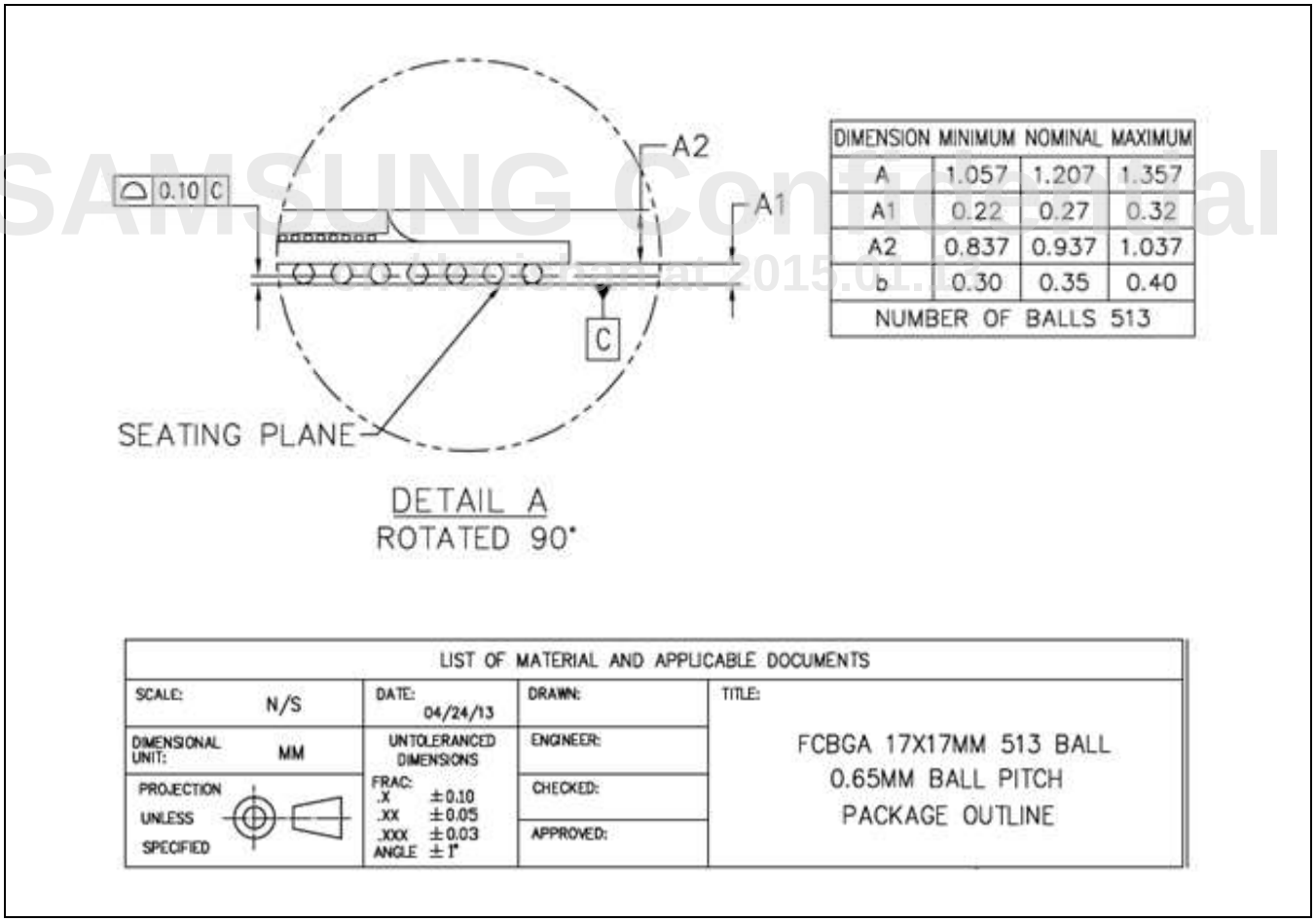


Figure 2-2 Mechanical Dimension - Top, Side View



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	1.057	1.207	1.357
A1	0.22	0.27	0.32
A2	0.837	0.937	1.037
b	0.30	0.35	0.40
NUMBER OF BALLS 513			

Figure 2-3 Mechanical Dimension - Dimension Value

2.2 FCBGA Ball Map

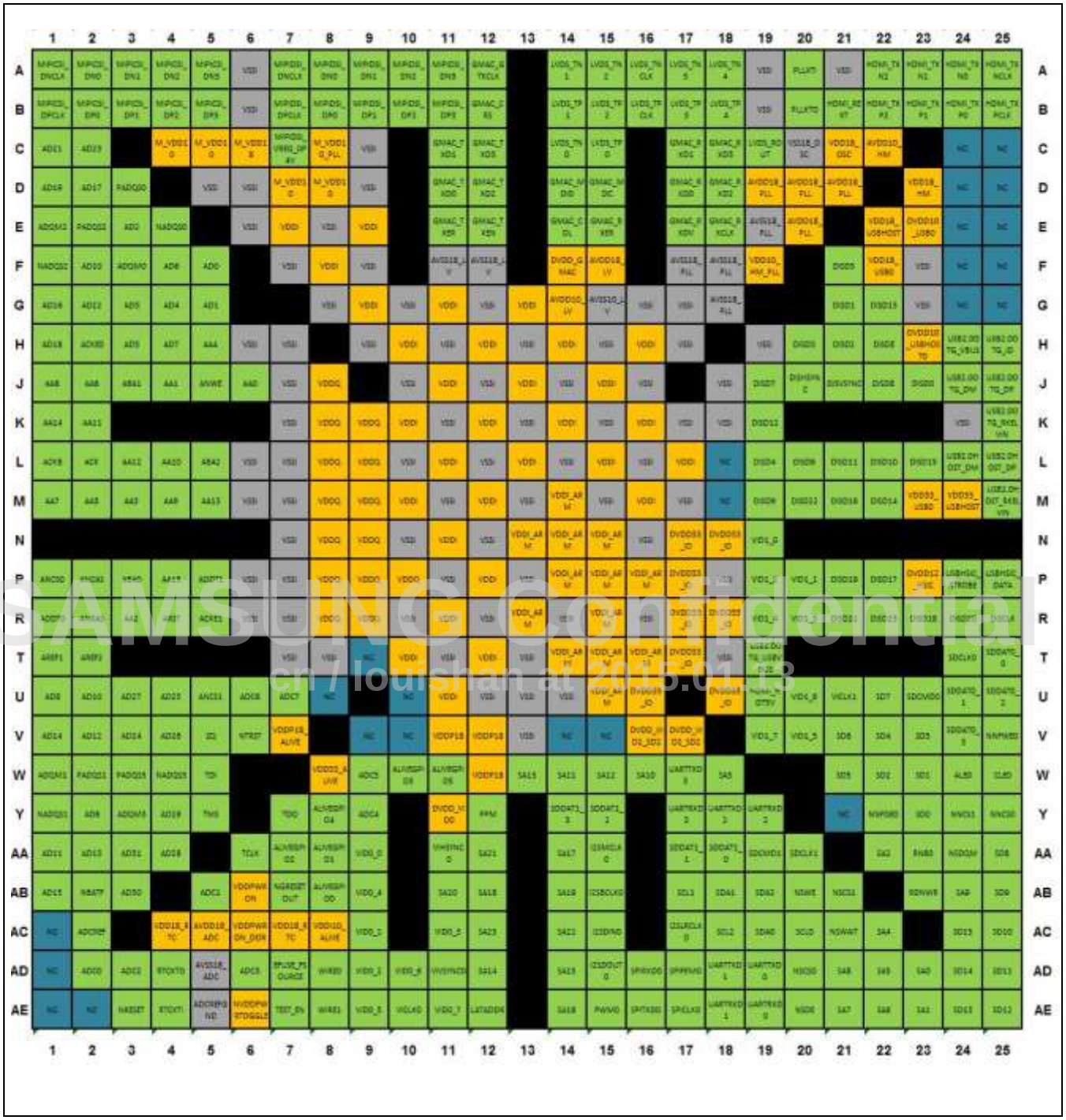
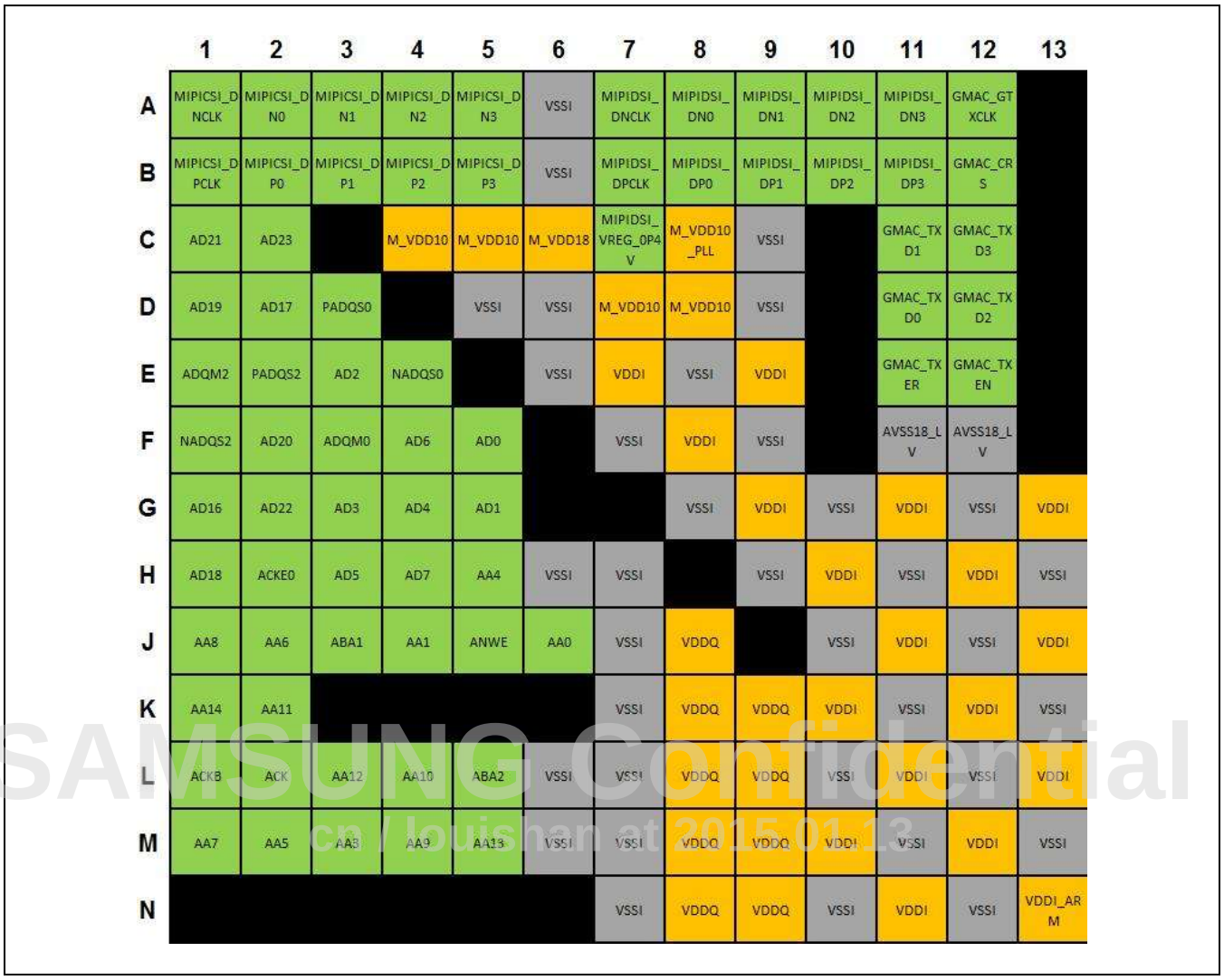


Figure 2-4 FCBGA Ball Map (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13
A	MIPICSI_DNCLK	MIPICSI_DN0	MIPICSI_DN1	MIPICSI_DN2	MIPICSI_DN3	VSSI	MIPIDSI_DNCLK	MIPIDSI_DN0	MIPIDSI_DN1	MIPIDSI_DN2	MIPIDSI_DN3	GMAC_GTXCLK	
B	MIPICSI_DPCLK	MIPICSI_DP0	MIPICSI_DP1	MIPICSI_DP2	MIPICSI_DP3	VSSI	MIPIDSI_DPCLK	MIPIDSI_DP0	MIPIDSI_DP1	MIPIDSI_DP2	MIPIDSI_DP3	GMAC_CRS	
C	AD21	AD23		M_VDD10	M_VDD10	M_VDD18	MIPIDSI_VREG_0P4V	M_VDD10_PLL	VSSI		GMAC_TXD1	GMAC_TXD3	
D	AD19	AD17	PADQS0		VSSI	VSSI	M_VDD10	M_VDD10	VSSI		GMAC_TXD0	GMAC_TXD2	
E	ADQM2	PADQS2	AD2	NADQS0		VSSI	VDDI	VSSI	VDDI		GMAC_TXER	GMAC_TXEN	
F	NADQS2	AD20	ADQM0	AD6	AD0		VSSI	VDDI	VSSI		AVSS18_LV	AVSS18_LV	
G	AD16	AD22	AD3	AD4	AD1			VSSI	VDDI	VSSI	VDDI	VSSI	VDDI
H	AD18	ACKE0	AD5	AD7	AA4	VSSI	VSSI		VSSI	VDDI	VSSI	VDDI	VSSI
J	AA8	AA6	ABA1	AA1	ANWE	AA0	VSSI	VDDQ		VSSI	VDDI	VSSI	VDDI
K	AA14	AA11					VSSI	VDDQ	VDDQ	VDDI	VSSI	VDDI	VSSI
L	ACKB	ACK	AA12	AA10	ABA2	VSSI	VSSI	VDDQ	VDDQ	VSSI	VDDI	VSSI	VDDI
M	AA7	AA5	AA3	AA9	AA13	VSSI	VSSI	VDDQ	VDDQ	VDDI	VSSI	VDDI	VSSI
N							VSSI	VDDQ	VDDQ	VSSI	VDDI	VSSI	VDDI_ARM

Figure 2-5 FCBGA Ball Map (Top View) - Upper Left Side

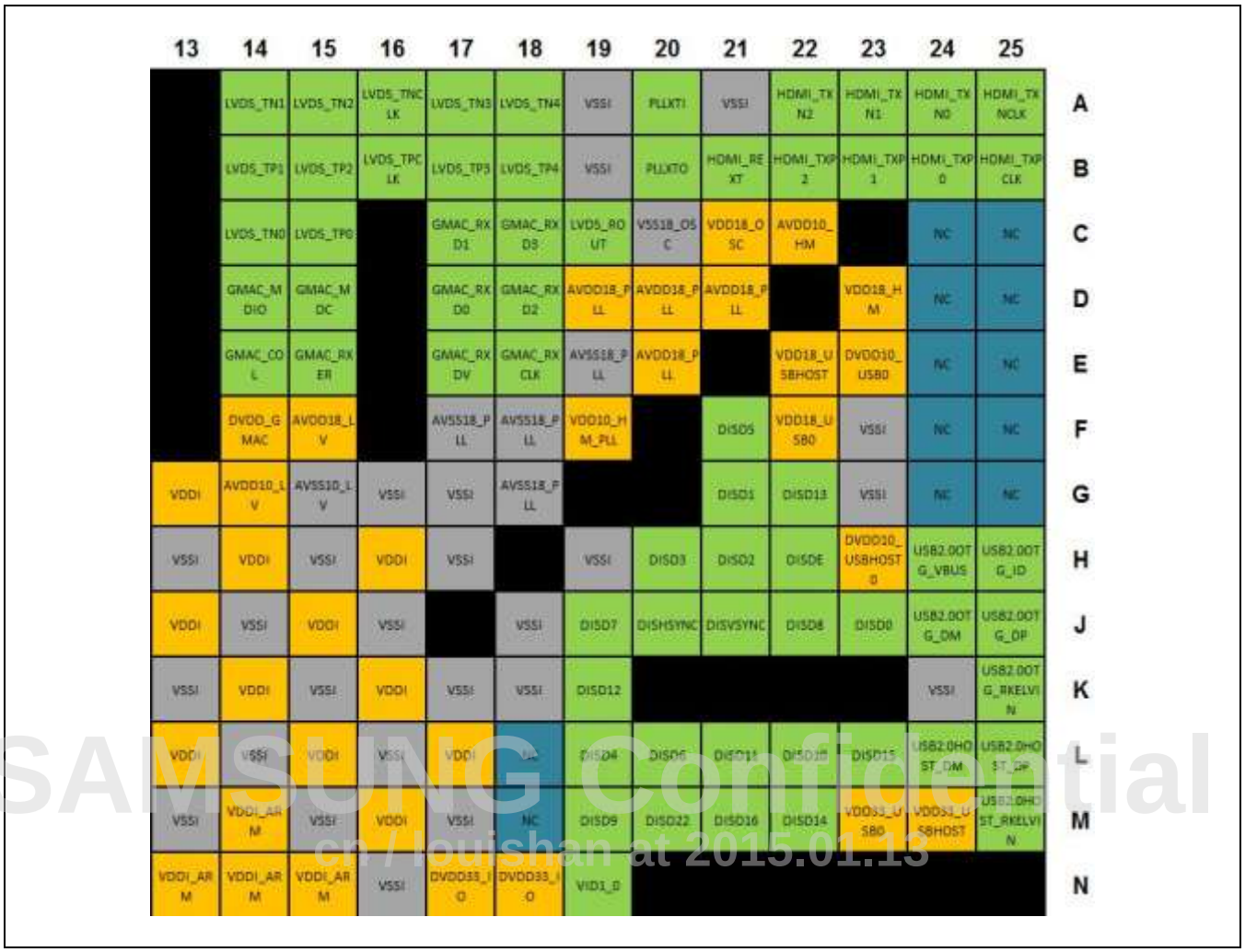


Figure 2-6 FCBGA Ball Map (Top View) - Upper Right Side

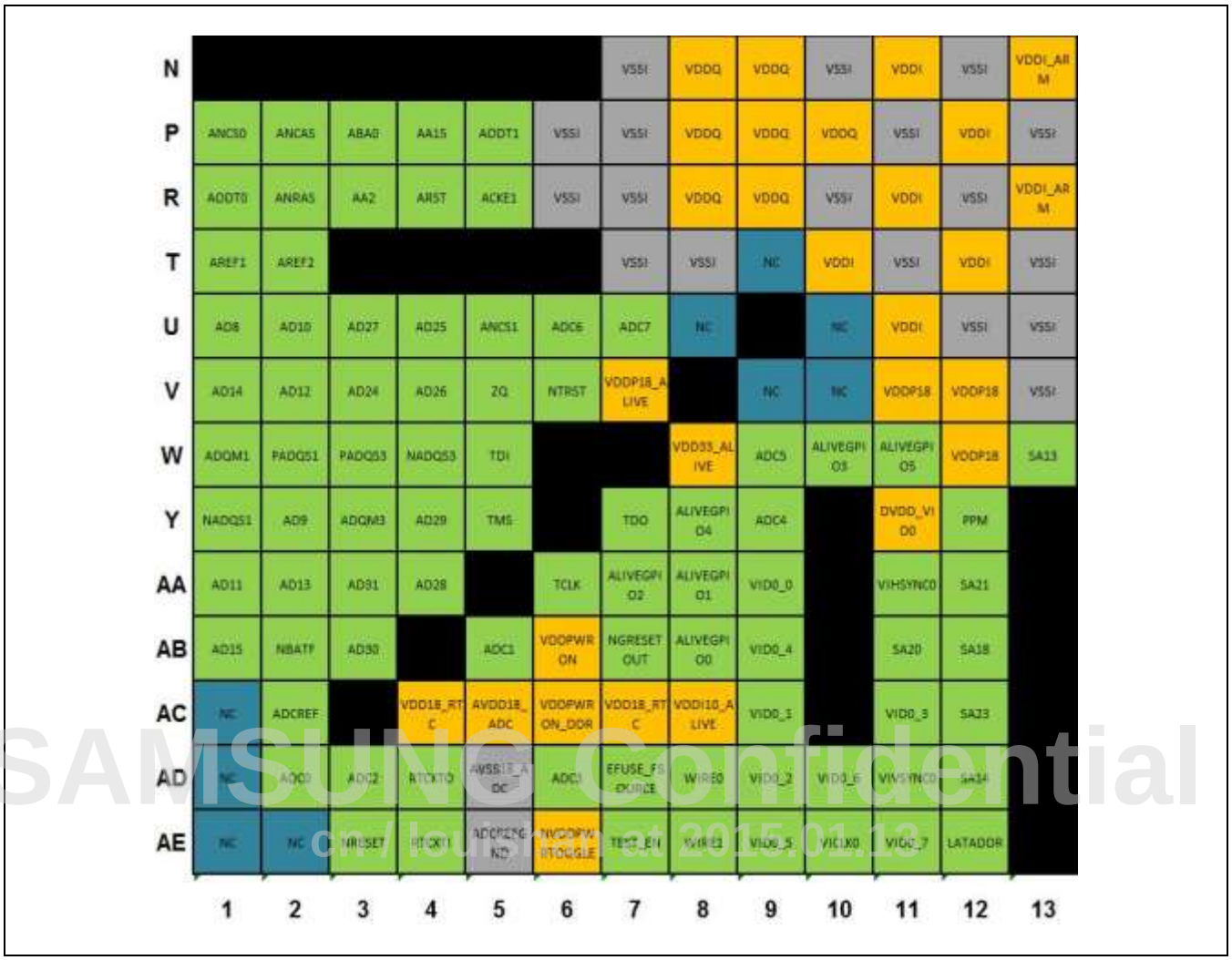


Figure 2-7 FCBGA Ball Map (Top View) - Lower Left Side

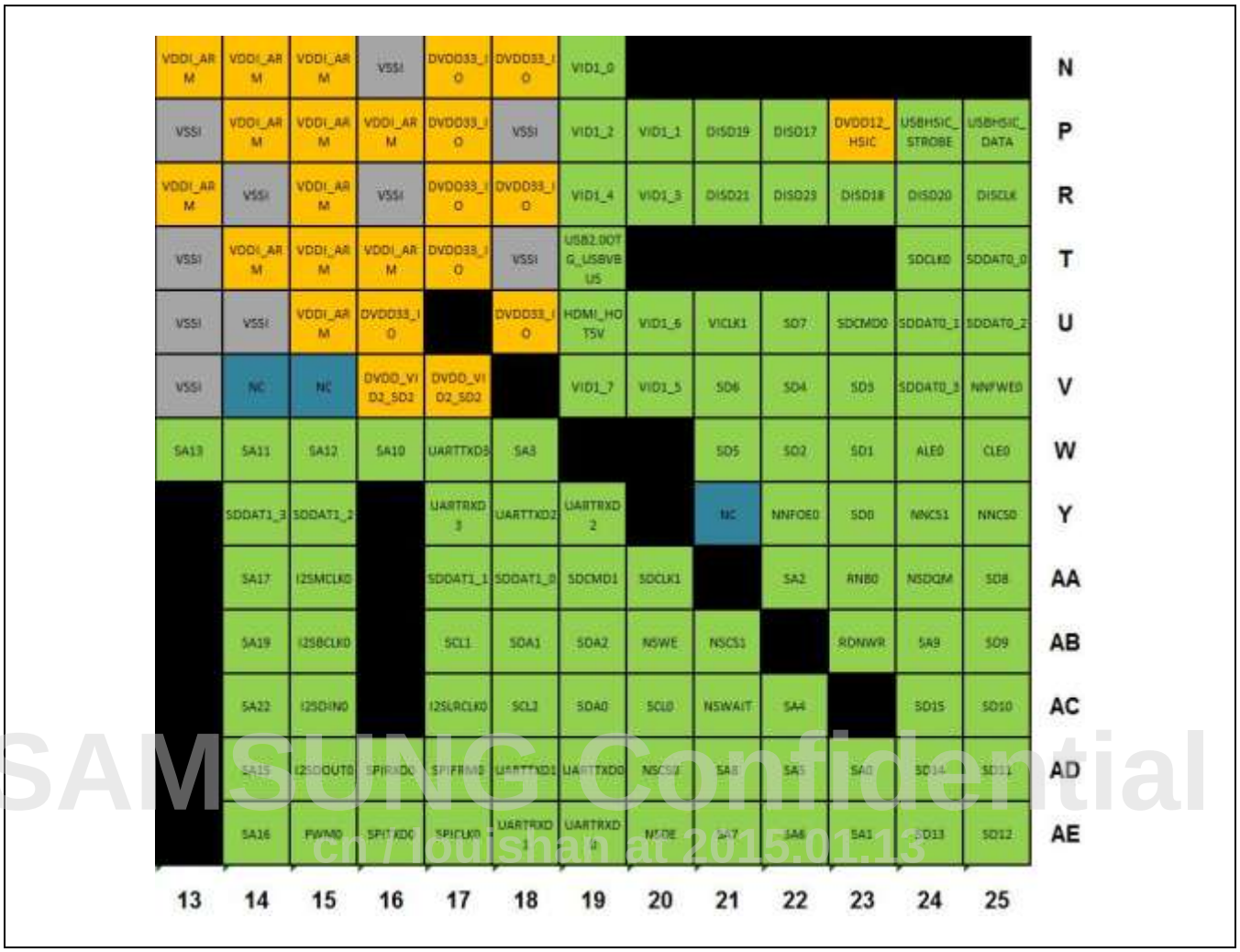


Figure 2-8 FCBGA Ball Map (Top View) - Lower Right Side

2.3 I/O Function Description

2.3.1 Ball List Table

Table 2-1 Ball Function Table

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
A1	MIPICSI_DNCLK	S	IO	N	MIPICSI_DNCLK	–	–	–
A2	MIPICSI_DN0	S	IO	N	MIPICSI_DN0	–	–	–
A3	MIPICSI_DN1	S	IO	N	MIPICSI_DN1	–	–	–
A4	MIPICSI_DN2	S	IO	N	MIPICSI_DN2	–	–	–
A5	MIPICSI_DN3	S	IO	N	MIPICSI_DN3	–	–	–
A6	VSSI	G	–	N	–	–	–	–
A7	MIPIDSI_DNCLK	S	IO	N	MIPIDSI_DNCLK	–	–	–
A8	MIPIDSI_DN0	S	IO	N	MIPIDSI_DN0	–	–	–
A9	MIPIDSI_DN1	S	IO	N	MIPIDSI_DN1	–	–	–
A10	MIPIDSI_DN2	S	IO	N	MIPIDSI_DN2	–	–	–
A11	MIPIDSI_DN3	S	IO	N	MIPIDSI_DN3	–	–	–
A12	GMAC_GTXCLK	S	IO	N	GPIOE24	GMAC_GTXCLK	–	–
A14	LVDS_TN1	S	IO	N	LVDS_TN1	–	–	–
A15	LVDS_TN2	S	IO	N	LVDS_TN2	–	–	–
A16	LVDS_TNCLK	S	IO	N	LVDS_TNCLK	–	–	–
A17	LVDS_TN3	S	IO	N	LVDS_TN3	–	–	–
A18	LVDS_TN4	S	IO	N	LVDS_TN4	–	–	–
A19	VSSI	G	–	N	–	–	–	–
A20	PLLXTI	S	I	N	PLLXTI	–	–	–
A21	VSSI	G	–	N	–	–	–	–
A22	HDMI_TXN2	S	O	N	HDMI_TXN2	–	–	–
A23	HDMI_TXN1	S	O	N	HDMI_TXN1	–	–	–
A24	HDMI_TXN0	S	O	N	HDMI_TXN0	–	–	–
A25	HDMI_TXNCLK	S	O	N	HDMI_TXNCLK	–	–	–
B1	MIPICSI_DPCLK	S	IO	N	MIPICSI_DPCLK	–	–	–
B2	MIPICSI_DP0	S	IO	N	MIPICSI_DP0	–	–	–
B3	MIPICSI_DP1	S	IO	N	MIPICSI_DP1	–	–	–
B4	MIPICSI_DP2	S	IO	N	MIPICSI_DP2	–	–	–
B5	MIPICSI_DP3	S	IO	N	MIPICSI_DP3	–	–	–
B6	VSSI	G	–	N	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
B7	MIPIDSI_DPCLK	S	IO	N	MIPIDSI_DPCLK	–	–	–
B8	MIPIDSI_DP0	S	IO	N	MIPIDSI_DP0	–	–	–
B9	MIPIDSI_DP1	S	IO	N	MIPIDSI_DP1	–	–	–
B10	MIPIDSI_DP2	S	IO	N	MIPIDSI_DP2	–	–	–
B11	MIPIDSI_DP3	S	IO	N	MIPIDSI_DP3	–	–	–
B12	GMAC_CRS	S	IO	N	GPIOE23	GMAC_CRS	–	–
B14	LVDS_TP1	S	IO	N	LVDS_TP1	–	–	–
B15	LVDS_TP2	S	IO	N	LVDS_TP2	–	–	–
B16	LVDS_TPCLK	S	IO	N	LVDS_TPCLK	–	–	–
B17	LVDS_TP3	S	IO	N	LVDS_TP3	–	–	–
B18	LVDS_TP4	S	IO	N	LVDS_TP4	–	–	–
B19	VSSI	G	–	N	–	–	–	–
B20	PLLXTO	S	O	N	PLLXTO	–	–	–
B21	HDMI_REXT	S	–	N	HDMI_REXT	–	–	–
B22	HDMI_TXP2	S	O	N	HDMI_TXP2	–	–	–
B23	HDMI_TXP1	S	O	N	HDMI_TXP1	–	–	–
B24	HDMI_TXP0	S	O	N	HDMI_TXP0	–	–	–
B25	HDMI_TXPCLK	S	O	N	HDMI_TXPCLK	–	–	–
C1	AD21	S	IO	N	AD21	–	–	–
C2	AD23	S	IO	N	AD23	–	–	–
C4	M_VDD10	P	–	N	–	–	–	–
C5	M_VDD10	P	–	N	–	–	–	–
C6	M_VDD18	P	–	N	–	–	–	–
C7	MIPIDSI_VREG_0P4V	S	–	N	MIPIDSI_VREG_0P4V	–	–	–
C8	M_VDD10_PLL	P	–	N	–	–	–	–
C9	VSSI	G	–	N	–	–	–	–
C11	GMAC_TXD1	S	IO	N	GPIOE8	GMAC_TXD1	–	–
C12	GMAC_TXD3	S	IO	N	GPIOE10	GMAC_TXD3	–	–
C14	LVDS_TN0	S	IO	N	LVDS_TN0	–	–	–
C15	LVDS_TP0	S	IO	N	LVDS_TP0	–	–	–
C17	GMAC_RXD1	S	IO	N	GPIOE15	GMAC_RXD1	SPIFRM1	–
C18	GMAC_RXD3	S	IO	N	GPIOE17	GMAC_RXD3	–	–
C19	LVDS_ROUT	S		N	LVDS_ROUT	–	–	–
C20	VSS18_OSC	G	–	N	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
C21	VDD18_OSC	P	–	N	–	–	–	–
C22	AVDD10_HM	P	–	N	–	–	–	–
C24	NC	–	–	–	–	–	–	–
C25	NC	–	–	–	–	–	–	–
D1	AD19	S	IO	N	AD19	–	–	–
D2	AD17	S	IO	N	AD17	–	–	–
D3	PADQS0	S	IO	N	PADQS0	–	–	–
D5	VSSI	G	–	N	–	–	–	–
D6	VSSI	G	–	N	–	–	–	–
D7	M_VDD10	P	–	N	–	–	–	–
D8	M_VDD10	P	–	N	–	–	–	–
D9	VSSI	G	–	N	–	–	–	–
D11	GMAC_TXD0	S	IO	N	GPIOE7	GMAC_TXD0	VIVSYNC1	–
D12	GMAC_TXD2	S	IO	N	GPIOE9	GMAC_TXD2	–	–
D14	GMAC_MDIO	S	IO	N	GPIOE21	GMAC_MDIO	–	–
D15	GMAC_MDC	S	IO	N	GPIOE20	GMAC_MDC	–	–
D17	GMAC_RXD0	S	IO	N	GPIOE14	GMAC_RXD0	SPICLK1	–
D18	GMAC_RXD2	S	IO	N	GPIOE16	GMAC_RXD2	–	–
D19	AVDD18_PLL	P	–	N	–	–	–	–
D20	AVDD18_PLL	P	–	N	–	–	–	–
D21	AVDD18_PLL	P	–	N	–	–	–	–
D23	VDD18_HM	P	–	N	–	–	–	–
D24	NC	–	–	–	–	–	–	–
D25	NC	–	–	–	–	–	–	–
E1	ADQM2	S	O	N	ADQM2	–	–	–
E2	PADQS2	S	IO	N	PADQS2	–	–	–
E3	AD2	S	IO	N	AD2	–	–	–
E4	NADQS0	S	IO	N	NADQS0	–	–	–
E6	VSSI	G	–	N	–	–	–	–
E7	VDDI	P	–	N	–	–	–	–
E8	VSSI	G	–	N	–	–	–	–
E9	VDDI	P	–	N	–	–	–	–
E11	GMAC_TXER	S	–	N	GPIOE12	GMAC_TXER	–	–
E12	GMAC_TXEN	S	IO	N	GPIOE11	GMAC_TXEN	–	–
E14	GMAC_COL	S	IO	N	GPIOE13	GMAC_COL	VIHSYNC1	–
E15	GMAC_RXER	S	IO	N	GPIOE22	GMAC_RXER	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
E17	GMAC_RXDV	S	IO	N	GPIOE19	GMAC_RXDV	SPITXD1	–
E18	GMAC_RXCLK	S	IO	N	GPIOE18	GMAC_RXCLK	SPIRXD1	–
E19	AVSS18_PLL	G	–	N	–	–	–	–
E20	AVDD18_PLL	P	–	N	–	–	–	–
E22	VDD18_USBHOST	P	–	N	–	–	–	–
E23	DVDD10_USB0	P	–	N	–	–	–	–
E24	NC	–	–	–	–	–	–	–
E25	NC	–	–	–	–	–	–	–
F1	NADQS2	S	IO	N	NADQS2	–	–	–
F2	AD20	S	IO	N	AD20	–	–	–
F3	ADQM0	S	O	N	ADQM0	–	–	–
F4	AD6	S	IO	N	AD6	–	–	–
F5	AD0	S	IO	N	AD0	–	–	–
F7	VSSI	G	–	N	–	–	–	–
F8	VDDI	P	–	N	–	–	–	–
F9	VSSI	G	–	N	–	–	–	–
F11	AVSS18_LV	G	–	N	–	–	–	–
F12	AVSS18_LV	G	–	N	–	–	–	–
F14	DVDD_GMAC	P	–	N	–	–	–	–
F15	AVDD18_LV	P	–	N	–	–	–	–
F17	AVSS18_PLL	G	–	N	–	–	–	–
F18	AVSS18_PLL	G	–	N	–	–	–	–
F19	VDD10_HM_PLL	P	–	N	–	–	–	–
F21	DISD5	S	IO	N	GPIOA6	DISD5	–	–
F22	VDD18_USB0	P	–	N	–	–	–	–
F23	VSSI	G	–	N	–	–	–	–
F24	NC	–	–	–	–	–	–	–
F25	NC	–	–	–	–	–	–	–
G1	AD16	S	IO	N	AD16	–	–	–
G2	AD22	S	IO	N	AD22	–	–	–
G3	AD3	S	IO	N	AD3	–	–	–
G4	AD4	S	IO	N	AD4	–	–	–
G5	AD1	S	IO	N	AD1	–	–	–
G8	VSSI	G	–	N	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
G9	VDDI	P	–	N	–	–	–	–
G10	VSSI	G	–	N	–	–	–	–
G11	VDDI	P	–	N	–	–	–	–
G12	VSSI	G	–	N	–	–	–	–
G13	VDDI	P	–	N	–	–	–	–
G14	AVDD10_LV	P	–	N	–	–	–	–
G15	AVSS10_LV	G	–	N	–	–	–	–
G16	VSSI	G	–	N	–	–	–	–
G17	VSSI	G	–	N	–	–	–	–
G18	AVSS18_PLL	G	–	N	–	–	–	–
G21	DISD1	S	IO	N	GPIOA2	DISD1	–	–
G22	DISD13	S	IO	N	GPIOA14	DISD13	–	–
G23	VSSI	G	–	N	–	–	–	–
G24	NC	–	–	–	–	–	–	–
G25	NC	–	–	–	–	–	–	–
H1	AD18	S	IO	N	AD18	–	–	–
H2	ACKE0	S	O	N	ACKE0	–	–	–
H3	AD5	S	IO	N	AD5	–	–	–
H4	AD7	S	IO	N	AD7	–	–	–
H5	AA4	S	O	N	AA4	–	–	–
H6	VSSI	G	–	N	–	–	–	–
H7	VSSI	G	–	N	–	–	–	–
H9	VSSI	G	–	N	–	–	–	–
H10	VDDI	P	–	N	–	–	–	–
H11	VSSI	G	–	N	–	–	–	–
H12	VDDI	P	–	N	–	–	–	–
H13	VSSI	G	–	N	–	–	–	–
H14	VDDI	P	–	N	–	–	–	–
H15	VSSI	G	–	N	–	–	–	–
H16	VDDI	P	–	N	–	–	–	–
H17	VSSI	G	–	N	–	–	–	–
H19	VSSI	G	–	N	–	–	–	–
H20	DISD3	S	IO	N	GPIOA4	DISD3	–	–
H21	DISD2	S	IO	N	GPIOA3	DISD2	–	–
H22	DISDE	S	IO	N	GPIOA27	DISDE	–	–
H23	DVDD10_USBH	P	–	N	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
	OST0							
H24	USB2.0OTG_VBUS	S	IO	N	USB2.0OTG_VBUS	–	–	–
H25	USB2.0OTG_ID	S	IO	N	USB2.0OTG_ID	–	–	–
J1	AA8	S	O	N	AA8	–	–	–
J2	AA6	S	O	N	AA6	–	–	–
J3	ABA1	S	O	N	ABA1	–	–	–
J4	AA1	S	O	N	AA1	–	–	–
J5	ANWE	S	O	N	ANWE	–	–	–
J6	AA0	S	O	N	AA0	–	–	–
J7	VSSI	G	–	N	–	–	–	–
J8	VDDQ	P	–	N	–	–	–	–
J10	VSSI	G	–	N	–	–	–	–
J11	VDDI	P	–	N	–	–	–	–
J12	VSSI	G	–	N	–	–	–	–
J13	VDDI	P	–	N	–	–	–	–
J14	VSSI	G	–	N	–	–	–	–
J15	VDDI	P	–	N	–	–	–	–
J16	VSSI	G	–	N	–	–	–	–
J18	VSSI	G	–	N	–	–	–	–
J19	DISD7	S	IO	N	GPIOA8	DISD7	–	–
J20	DISHSYNC	S	IO	N	GPIOA26	DISHSYNC	–	–
J21	DISVSYNC	S	IO	N	GPIOA25	DISVSYNC	–	–
J22	DISD8	S	IO	N	GPIOA9	DISD8	–	–
J23	DISD0	S	IO	N	GPIOA1	DISD0	–	–
J24	USB2.0OTG_DM	S	IO	N	USB2.0OTG_DM	–	–	–
J25	USB2.0OTG_DP	S	IO	N	USB2.0OTG_DP	–	–	–
K1	AA14	S	O	N	AA14	–	–	–
K2	AA11	S	O	N	AA11	–	–	–
K7	VSSI	G	–	N	–	–	–	–
K8	VDDQ	P	–	N	–	–	–	–
K9	VDDQ	P	–	N	–	–	–	–
K10	VDDI	P	–	N	–	–	–	–
K11	VSSI	G	–	N	–	–	–	–
K12	VDDI	P	–	N	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
K13	VSSI	G	–	N	–	–	–	–
K14	VDDI	P	–	N	–	–	–	–
K15	VSSI	G	–	N	–	–	–	–
K16	VDDI	P	–	N	–	–	–	–
K17	VSSI	G	–	N	–	–	–	–
K18	VSSI	G	–	N	–	–	–	–
K19	DISD12	S	IO	N	GPIOA13	DISD12	–	–
K24	VSSI	G	–	N	–	–	–	–
K25	USB2.0OTG_RKELVIN	S	IO	N	USB2.0OTG_RKELVIN	–	–	–
L1	ACKB	S	O	N	ACKB	–	–	–
L2	ACK	S	O	N	ACK	–	–	–
L3	AA12	S	O	N	AA12	–	–	–
L4	AA10	S	O	N	AA10	–	–	–
L5	ABA2	S	O	N	ABA2	–	–	–
L6	VSSI	G	–	N	–	–	–	–
L7	VSSI	G	–	N	–	–	–	–
L8	VDDQ	P	–	N	–	–	–	–
L9	VDDQ	P	–	N	–	–	–	–
L10	VSSI	G	–	N	–	–	–	–
L11	VDDI	P	–	N	–	–	–	–
L12	VSSI	G	–	N	–	–	–	–
L13	VDDI	P	–	N	–	–	–	–
L14	VSSI	G	–	N	–	–	–	–
L15	VDDI	P	–	N	–	–	–	–
L16	VSSI	G	–	N	–	–	–	–
L17	VDDI	P	–	N	–	–	–	–
L18	NC	–	–	–	–	–	–	–
L19	DISD4	S	IO	N	GPIOA5	DISD4	–	–
L20	DISD6	S	IO	N	GPIOA7	DISD6	–	–
L21	DISD11	S	IO	N	GPIOA12	DISD11	–	–
L22	DISD10	S	IO	N	GPIOA11	DISD10	–	–
L23	DISD15	S	IO	N	GPIOA16	DISD15	–	–
L24	USB2.0HOST_DM	S	IO	N	USB2.0HOST_DM	–	–	–
L25	USB2.0HOST_DP	S	IO	N	USB2.0HOST_DP	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
M1	AA7	S	O	N	AA7	–	–	–
M2	AA5	S	O	N	AA5	–	–	–
M3	AA3	S	O	N	AA3	–	–	–
M4	AA9	S	O	N	AA9	–	–	–
M5	AA13	S	O	N	AA13	–	–	–
M6	VSSI	G	–	N	–	–	–	–
M7	VSSI	G	–	N	–	–	–	–
M8	VDDQ	P	–	N	–	–	–	–
M9	VDDQ	P	–	N	–	–	–	–
M10	VDDI	P	–	N	–	–	–	–
M11	VSSI	G	–	N	–	–	–	–
M12	VDDI	P	–	N	–	–	–	–
M13	VSSI	G	–	N	–	–	–	–
M14	VDDI_ARM	P	–	N	–	–	–	–
M15	VSSI	G	–	N	–	–	–	–
M16	VDDI	P	–	N	–	–	–	–
M17	VSSI	G	–	N	–	–	–	–
M18	NC	–	–	–	–	–	–	–
M19	DISD9	S	IO	N	GPIOA10	DISD9	–	–
M20	DISD22	S	IO	N	GPIOA23	DISD22	–	–
M21	DISD16	S	IO	N	GPIOA17	DISD16	–	–
M22	DISD14	S	IO	N	GPIOA15	DISD14	–	–
M23	VDD33_USB0	P	–	N	–	–	–	–
M24	VDD33_USBHOST	P	–	N	–	–	–	–
M25	USB2.0HOST_RKELVIN	S	IO	N	USB2.0HOST_RKELVIN	–	–	–
N7	VSSI	G	–	N	–	–	–	–
N8	VDDQ	P	–	N	–	–	–	–
N9	VDDQ	P	–	N	–	–	–	–
N10	VSSI	G	–	N	–	–	–	–
N11	VDDI	P	–	N	–	–	–	–
N12	VSSI	G	–	N	–	–	–	–
N13	VDDI_ARM	P	–	N	–	–	–	–
N14	VDDI_ARM	P	–	N	–	–	–	–
N15	VDDI_ARM	P	–	N	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
N16	VSSI	G	–	N	–	–	–	–
N17	DVDD33_IO	P	–	N	–	–	–	–
N18	DVDD33_IO	P	–	N	–	–	–	–
N19	VID1_0	S	IO	N	GPIOA30	VID1_0	SDEX0	I2SBCLK1
P1	ANCS0	S	O	N	ANCS0	–	–	–
P2	ANCAS	S	O	N	ANCAS	–	–	–
P3	ABA0	S	O	N	ABA0	–	–	–
P4	AA15	S	O	N	AA15	–	–	–
P5	AODT1	S	O	N	AODT1	–	–	–
P6	VSSI	G	–	N	–	–	–	–
P7	VSSI	G	–	N	–	–	–	–
P8	VDDQ	P	–	N	–	–	–	–
P9	VDDQ	P	–	N	–	–	–	–
P10	VDDQ	P	–	N	–	–	–	–
P11	VSSI	G	–	N	–	–	–	–
P12	VDDI	P	–	N	–	–	–	–
P13	VSSI	G	–	N	–	–	–	–
P14	VDDI_ARM	P	–	N	–	–	–	–
P15	VDDI_ARM	P	–	N	–	–	–	–
P16	VDDI_ARM	P	–	N	–	–	–	–
P17	DVDD33_IO	P	–	N	–	–	–	–
P18	VSSI	G	–	N	–	–	–	–
P19	VID1_2	S	IO	N	GPIOB2	VID1_2	SDEX2	I2SBCLK2
P20	VID1_1	S	IO	N	GPIOB0	VID1_1	SDEX1	I2SLRCLK1
P21	DISD19	S	IO	N	GPIOA20	DISD19	–	–
P22	DISD17	S	IO	N	GPIOA18	DISD17	–	–
P23	DVDD12_HSIC	P	–	N	–	–	–	–
P24	USBHSIC_STROBE	S	IO	N	USBHSIC_STROBE	–	–	–
P25	USBHSIC_DATA	S	IO	N	USBHSIC_DATA	–	–	–
R1	AODT0	S	O	N	AODT0	–	–	–
R2	ANRAS	S	O	N	ANRAS	–	–	–
R3	AA2	S	O	N	AA2	–	–	–
R4	ARST	S	O	N	ARST	–	–	–
R5	ACKE1	S	O	N	ACKE1	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
R6	VSSI	G	–	N	–	–	–	–
R7	VSSI	G	–	N	–	–	–	–
R8	VDDQ	P	–	N	–	–	–	–
R9	VDDQ	P	–	N	–	–	–	–
R10	VSSI	G	–	N	–	–	–	–
R11	VSSI	G	–	N	–	–	–	–
R12	VDDI	P	–	N	–	–	–	–
R13	VDDI_ARM	P	–	N	–	–	–	–
R14	VSSI	G	–	N	–	–	–	–
R15	VDDI_ARM	P	–	N	–	–	–	–
R16	VSSI	G	–	N	–	–	–	–
R17	DVDD33_IO	P	–	N	–	–	–	–
R18	DVDD33_IO	P	–	N	–	–	–	–
R19	VID1_4	S	IO	N	GPIOB6	VID1_4	SDEX4	I2SDOUT1
R20	VID1_3	S	IO	N	GPIOB4	VID1_3	SDEX3	I2SLRCLK2
R21	DISD21	S	IO	N	GPIOA22	DISD21	–	–
R22	DISD23	S	IO	N	GPIOA24	DISD23	–	–
R23	DISD18	S	IO	N	GPIOA19	DISD18	–	–
R24	DISD20	S	IO	N	GPIOA21	DISD20	–	–
R25	DISCLK	S	IO	N	GPIOA0	DISCLK	–	–
T1	AREF1	P	IO	N	AREF1	–	–	–
T2	AREF2	P	IO	N	AREF2	–	–	–
T7	VSSI	G	–	N	–	–	–	–
T8	VSSI	G	–	N	–	–	–	–
T9	NC	–	–	–	–	–	–	–
T10	VDDI	P	–	N	–	–	–	–
T11	VSSI	G	–	N	–	–	–	–
T12	VDDI	P	–	N	–	–	–	–
T13	VSSI	G	–	N	–	–	–	–
T14	VDDI_ARM	P	–	N	–	–	–	–
T15	VDDI_ARM	P	–	N	–	–	–	–
T16	VDDI_ARM	P	–	N	–	–	–	–
T17	DVDD33_IO	P	–	N	–	–	–	–
T18	VSSI	G	–	N	–	–	–	–
T19	USB2.0OTG_USBVBUS	S	I	N	USB2.0OTG_USBVBUS	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
T24	SDCLK0	S	IO	N	GPIOA29	SDCLK0	–	–
T25	SDDAT0_0	S	IO	N	GPIOB1	SDDAT0_0	–	–
U1	AD8	S	IO	N	AD8	–	–	–
U2	AD10	S	IO	N	AD10	–	–	–
U3	AD27	S	IO	N	AD27	–	–	–
U4	AD25	S	IO	N	AD25	–	–	–
U5	ANCS1	S	O	N	ANCS1	–	–	–
U6	ADC6	S	IO	N	ADC6	–	–	–
U7	ADC7	S	IO	N	ADC7	–	–	–
U8	NC	–	–	–	–	–	–	–
U10	NC	–	–	–	–	–	–	–
U11	VDDI	P	–	N	–	–	–	–
U12	VDDI	P	–	N	–	–	–	–
U13	VSSI	G	–	N	–	–	–	–
U14	VSSI	G	–	N	–	–	–	–
U15	VDDI_ARM	P	–	N	–	–	–	–
U16	DVDD33_IO	P	–	N	–	–	–	–
U18	DVDD33_IO	P	–	N	–	–	–	–
U19	HDMI_HOT5V	S	I	N	HDMI_HOT5V	–	–	–
U20	VID1_6	S	IO	N	GPIOB9	VID1_6	SDEX6	I2SDIN1
U21	VICLK1	S	IO	N	GPIOA28	VICLK1	I2SMCLK2	I2SMCLK1
U22	SD7	S	IO	N	SD7	GPIOB23	–	–
U23	SDCMD0	S	IO	N	GPIOA31	SDCMD0	–	–
U24	SDDAT0_1	S	IO	N	GPIOB3	SDDAT0_1	–	–
U25	SDDAT0_2	S	IO	N	GPIOB5	SDDAT0_2	–	–
V1	AD14	S	IO	N	AD14	–	–	–
V2	AD12	S	IO	N	AD12	–	–	–
V3	AD24	S	IO	N	AD24	–	–	–
V4	AD26	S	IO	N	AD26	–	–	–
V5	ZQ	S	–	N	ZQ	–	–	–
V6	NTRST	S	IO	PU	NTRST	GPIOE25	–	–
V7	VDDP18_ALIVE	P	–	N	–	–	–	–
V9	NC	–	–	–	–	–	–	–
V10	NC	–	–	–	–	–	–	–
V11	VDDP18	P	–	N	–	–	–	–
V12	VDDP18	P	–	N	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
V13	VSSI	G	–	N	–	–	–	–
V14	NC	–	–	–	–	–	–	–
V15	NC	–	–	–	–	–	–	–
V16	DVDD_VID2_SD2	P	–	N	–	–	–	–
V17	DVDD_VID2_SD2	P	–	N	–	–	–	–
V19	VID1_7	S	IO	N	GPIOB10	VID1_7	SDEX7	I2SDIN2
V20	VID1_5	S	IO	N	GPIOB8	VID1_5	SDEX5	I2SDOUT2
V21	SD6	S	IO	N	SD6	GPIOB22	–	–
V22	SD4	S	IO	N	SD4	GPIOB20	–	–
V23	SD3	S	IO	N	SD3	GPIOB19	–	–
V24	SDDAT0_3	S	IO	N	GPIOB7	SDDAT0_3	–	–
V25	NNFWE0	S	IO	N	NNFWE0	nNFWE1	GPIOB18	–
W1	ADQM1	S	O	N	ADQM1	–	–	–
W2	PADQS1	S	IO	N	PADQS1	–	–	–
W3	PADQS3	S	IO	N	PADQS3	–	–	–
W4	NADQS3	S	IO	N	NADQS3	–	–	–
W5	TDI	S	IO	PU	TDI	GPIOE27	–	–
W8	VDD33_ALIVE	P	–	N	–	–	–	–
W9	ADC5	S	IO	N	ADC5	–	–	–
W10	ALIVEGPIO3	S	IO	N	ALIVEGPIO3	–	–	–
W11	ALIVEGPIO5	S	IO	N	ALIVEGPIO5	–	–	–
W12	VDDP18	P	–	N	–	–	–	–
W13	SA13	S	IO	N	SA13	GPIOC13	PWM1	SDnINT2
W14	SA11	S	IO	N	SA11	GPIOC11	SPIRXD2	USB2.0OTG_DrvVBUS
W15	SA12	S	IO	N	SA12	GPIOC12	SPITXD2	SDnRST2
W16	SA10	S	IO	PU	SA10	GPIOC10	SPIFRM2	–
W17	UARTTXD3	S	IO	N	GPIOD21	UARTTXD3	–	SDnCD1
W18	SA3	S	IO	N	SA3	GPIOC3	HDMI_CEC	SDnRST0
W21	SD5	S	IO	N	SD5	GPIOB21	–	–
W22	SD2	S	IO	N	SD2	GPIOB17	–	–
W23	SD1	S	IO	N	SD1	GPIOB15	–	–
W24	ALE0	S	IO	N	ALE0	ALE1	GPIOB12	–
W25	CLE0	S	IO	N	CLE0	CLE1	GPIOB11	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
Y1	NADQS1	S	IO	N	NADQS1	–	–	–
Y2	AD9	S	IO	N	AD9	–	–	–
Y3	ADQM3	S	O	N	ADQM3	–	–	–
Y4	AD29	S	IO	N	AD29	–	–	–
Y5	TMS	S	IO	PU	TMS	GPIOE26	–	–
Y7	TDO	S	IO	N	TDO	GPIOE29	–	–
Y8	ALIVEGPIO4	S	IO	N	ALIVEGPIO4	–	–	–
Y9	ADC4	S	IO	N	ADC4	–	–	–
Y11	DVDD_VID0	P	–	N	–	–	–	–
Y12	PPM	S	IO	N	GPIOD8	PPM	–	–
Y14	SDDAT1_3	S	IO	N	GPIOD27	SDDAT1_3	–	–
Y15	SDDAT1_2	S	IO	N	GPIOD26	SDDAT1_2	–	–
Y17	UARTRXD3	S	IO	N	GPIOD17	UARTRXD3	–	–
Y18	UARTTXD2	S	IO	N	GPIOD20	UARTTXD2	–	SDWP1
Y19	UARTRXD2	S	IO	N	GPIOD16	UARTRXD2	–	–
Y21	NC	–	–	–	–	–	–	–
Y22	NNFOE0	S	IO	N	NNFOE0	NNFOE1	GPIOB16	–
Y23	SD0	S	IO	N	SD0	GPIOB13	–	–
Y24	NNCS1	S	O	PU	NNCS1	–	–	–
Y25	NNCS0	S	O	N	NNCS0	–	–	–
AA1	AD11	S	IO	N	AD11	–	–	–
AA2	AD13	S	IO	N	AD13	–	–	–
AA3	AD31	S	IO	N	AD31	–	–	–
AA4	AD28	S	IO	N	AD28	–	–	–
AA6	TCLK	S	IO	PD	TCLK	GPIOE28	–	–
AA7	ALIVEGPIO2	S	IO	N	ALIVEGPIO2	–	–	–
AA8	ALIVEGPIO1	S	IO	N	ALIVEGPIO1	–	–	–
AA9	VID0_0	S	IO	N	GPIOD28	VID0_0	TSIDATA1_0	SA24
AA11	VIHSYNC0	S	IO	N	GPIOE5	VIHSYNC0	TSISYNC1	–
AA12	SA21	S	IO	N	SA21	GPIOC21	SDDAT2_1	VID2_4
AA14	SA17	S	IO	N	SA17	GPIOC17	TSIDP0	VID2_0
AA15	I2SMCLK0	S	IO	N	GPIOD13	I2SMCLK0	AC97_nRST	–
AA17	SDDAT1_1	S	IO	N	GPIOD25	SDDAT1_1	–	–
AA18	SDDAT1_0	S	IO	N	GPIOD24	SDDAT1_0	–	–
AA19	SDCMD1	S	IO	N	GPIOD23	SDCMD1	–	–
AA20	SDCLK1	S	IO	N	GPIOD22	SDCLK1	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AA22	SA2	S	IO	N	SA2	GPIOC2	–	–
AA23	RNB0	S	IO	N	RnB0	RnB1	GPIOB14	–
AA24	NSDQM	S	IO	PU	NSDQM	GPIOC27	PDMDATA1	–
AA25	SD8	S	IO	N	SD8	GPIOB24	TSIDATA0_0	–
AB1	AD15	S	IO	N	AD15	–	–	–
AB2	NBATF	S	I	N	NBATF	–	–	–
AB3	AD30	S	IO	N	AD30	–	–	–
AB5	ADC1	S	IO	N	ADC1	–	–	–
AB6	VDDPWRON	S	O	N	VDDPWRON	–	–	–
AB7	NGRESETOUT	S	O	N	NGRESETOUT	–	–	–
AB8	ALIVEGPIO0	S	IO	N	ALIVEGPIO0	–	–	–
AB9	VID0_4	S	IO	N	GPIOE0	VID0_4	TSIDATA1_4	–
AB11	SA20	S	IO	N	SA20	GPIOC20	SDDAT2_0	VID2_3
AB12	SA18	S	IO	N	SA18	GPIOC18	SDCLK2	VID2_1
AB14	SA19	S	IO	N	SA19	GPIOC19	SDCMD2	VID2_2
AB15	I2SBCLK0	S	IO	N	GPIOD10	I2SBCLK0	AC97_BCLK	–
AB17	SCL1	S	IO	N	GPIOD4	SCL1	–	–
AB18	SDA1	S	IO	N	GPIOD5	SDA1	–	–
AB19	SDA2	S	IO	N	GPIOD7	SDA2	–	–
AB20	NSWE	S	IO	PU	NSWE	GPIOE31	–	–
AB21	NSCS1	S	IO	PU	GPIOC28	NSCS1	UARTnRI1	–
AB23	RDNWR	S	IO	PU	RDNWR	GPIOC26	PDMDATA0	–
AB24	SA9	S	IO	N	SA9	GPIOC9	SPICLK2	PDMStrobe
AB25	SD9	S	IO	N	SD9	GPIOB25	TSIDATA0_1	–
AC1	NC	–	–	–	–	–	–	–
AC2	ADCREF	P	IO	N	–	–	–	–
AC4	VDD18_RTC	P	–	N	–	–	–	–
AC5	AVDD18_ADC	P	IO	N	–	–	–	–
AC6	VDDPWRON_DDR	S	O	N	VDDPWRON_DDR	–	–	–
AC7	VDD18_RTC	P	–	N	–	–	–	–
AC8	VDDI10_ALIVE	P	–	N	–	–	–	–
AC9	VID0_1	S	IO	N	GPIOD29	VID0_1	TSIDATA1_1	–
AC11	VID0_3	S	IO	N	GPIOD31	VID0_3	TSIDATA1_3	–
AC12	SA23	S	IO	N	SA23	GPIOC23	SDDAT2_3	VID2_6
AC14	SA22	S	IO	N	SA22	GPIOC22	SDDAT2_2	VID2_5

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AC15	I2SDIN0	S	IO	N	GPIOD11	I2SDIN0	AC97_DIN	–
AC17	I2SLRCLK0	S	IO	N	GPIOD12	I2SLRCLK0	AC97_SYNC	–
AC18	SCL2	S	IO	N	GPIOD6	SCL2	–	–
AC19	SDA0	S	IO	N	GPIOD3	SDA0	ISO7816	–
AC20	SCL0	S	IO	N	GPIOD2	SCL0	ISO7816	–
AC21	NSWAIT	S	IO	PU	NSWAIT	GPIOC25	SPDIFTX	–
AC22	SA4	S	IO	N	SA4	GPIOC4	UARTnDCD1	SDnINT0
AC24	SD15	S	IO	N	SD15	GPIOB31	TSIDATA0_7	–
AC25	SD10	S	IO	N	SD10	GPIOB26	TSIDATA0_2	–
AD1	NC	–	–	–	–	–	–	–
AD2	ADC0	S	IO	N	ADC0	–	–	–
AD3	ADC2	S	IO	N	ADC2	–	–	–
AD4	RTCXTO	S	O	N	RTCXTO	–	–	–
AD5	AVSS18_ADC	G	–	N	–	–	–	–
AD6	ADC3	S	IO	N	ADC3	–	–	–
AD7	EFUSE_FSOURCE	S	–	N	EFUSE_FSOURCE	–	–	–
AD8	WIRE0	S	I	N	WIRE0	–	–	–
AD9	VID0_2	S	IO	N	GPIOD30	VID0_2	TSIDATA1_2	–
AD10	VID0_6	S	IO	N	GPIOE2	VID0_6	TSIDATA1_6	–
AD11	VIVSYNC0	S	IO	N	GPIOE6	VIVSYNC0	TSIDP1	–
AD12	SA14	S	IO	N	SA14	GPIOC14	PWM2	VICLK2
AD14	SA15	S	IO	N	SA15	GPIOC15	TSICLK0	VIHSYNC2
AD15	I2SDOUT0	S	IO	N	GPIOD9	I2SDOUT0	AC97_DOUT	–
AD16	SPIRXD0	S	IO	N	GPIOD0	SPIRXD0	PWM3	–
AD17	SPIFRM0	S	IO	N	GPIOC30	SPIFRM0	–	–
AD18	UARTTXD1	S	IO	N	GPIOD19	UARTTXD1	ISO7816	SDnCD2
AD19	UARTTXD0	S	IO	N	GPIOD18	UARTTXD0	ISO7816	SDWP2
AD20	NSCS0	S	O	N	NSCS0	–	–	–
AD21	SA8	S	IO	N	SA8	GPIOC8	UARTnDTR1	SDnINT1
AD22	SA5	S	IO	N	SA5	GPIOC5	UARTnCTS1	SDWP0
AD23	SA0	S	IO	N	SA0	GPIOC0	TSERR0	–
AD24	SD14	S	IO	N	SD14	GPIOB30	TSIDATA0_6	–
AD25	SD11	S	IO	N	SD11	GPIOB27	TSIDATA0_3	–
AE1	NC	–	–	–	–	–	–	–
AE2	NC	–	–	–	–	–	–	–

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AE3	NRESET	S	I	N	NRESET	–	–	–
AE4	RTCXTI	S	I	N	RTCXTI	–	–	–
AE5	ADCREFGND	G	–	N	–	–	–	–
AE6	NVDDPWRTOGGLE	S	I	PU	NVDDPWRTOGGLE	–	–	–
AE7	TEST_EN	S	I	N	TEST_EN	–	–	–
AE8	WIRE1	S	–	N	WIRE1	–	–	–
AE9	VID0_5	S	IO	N	GPIOE1	VID0_5	TSIDATA1_5	–
AE10	VICLK0	S	IO	N	GPIOE4	VICLK0	TSICLK1	–
AE11	VID0_7	S	IO	N	GPIOE3	VID0_7	TSIDATA1_7	–
AE12	LATADDR	S	IO	N	LATADDR	GPIOC24	SPDIFRX	VID2_7
AE14	SA16	S	IO	N	SA16	GPIOC16	TSISYNC0	VIVSYNC2
AE15	PWM0	S	IO	N	GPIOD1	PWM0	SA25	–
AE16	SPITXD0	S	IO	N	GPIOC31	SPITXD0	–	–
AE17	SPICLK0	S	IO	N	GPIOC29	SPICLK0	–	–
AE18	UARTRXD1	S	IO	N	GPIOD15	UARTRXD1	ISO7816	–
AE19	UARTRXD0	S	IO	N	GPIOD14	UARTRXD0	ISO7816	–
AE20	NSOE	S	IO	PU	NSOE	GPIOE30	–	–
AE21	SA7	S	IO	N	SA7	GPIOC7	UARTnDSR1	SDnRST1
AE22	SA6	S	IO	N	SA6	GPIOC6	UARTnRTS1	SDnCD0
AE23	SA1	S	IO	N	SA1	GPIOC1	TSERR1	–
AE24	SD13	S	IO	N	SD13	GPIOB29	TSIDATA0_5	UARTTXD4
AE25	SD12	S	IO	N	SD12	GPIOB28	TSIDATA0_4	UARTRXD4

NOTE:

1. Type definition - S: Signal ball, P: Power ball, G: GND ball
2. IO pad type definition - I: Input, O: Output, IO: Input/Output
3. Internal Pull Up/Down definition - PU: Pull Up, PD: Pull Down, N: no Pull Up/Down

2.3.2 Ball List Table: Sorted by Function

2.3.2.1 MCU-A

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
F 5	AD0	S	AD0	–	–	–
G 5	AD1	S	AD1	–	–	–
E 3	AD2	S	AD2	–	–	–
G 3	AD3	S	AD3	–	–	–
G 4	AD4	S	AD4	–	–	–
H 3	AD5	S	AD5	–	–	–
F 4	AD6	S	AD6	–	–	–
H 4	AD7	S	AD7	–	–	–
U 1	AD8	S	AD8	–	–	–
Y 2	AD9	S	AD9	–	–	–
U 2	AD10	S	AD10	–	–	–
AA 1	AD11	S	AD11	–	–	–
V 2	AD12	S	AD12	–	–	–
AA 2	AD13	S	AD13	–	–	–
V 1	AD14	S	AD14	–	–	–
AB 1	AD15	S	AD15	–	–	–
G 1	AD16	S	AD16	–	–	–
D 2	AD17	S	AD17	–	–	–
H 1	AD18	S	AD18	–	–	–
D 1	AD19	S	AD19	–	–	–
F 2	AD20	S	AD20	–	–	–
C 1	AD21	S	AD21	–	–	–
G 2	AD22	S	AD22	–	–	–
C 2	AD23	S	AD23	–	–	–
V 3	AD24	S	AD24	–	–	–
U 4	AD25	S	AD25	–	–	–
V 4	AD26	S	AD26	–	–	–
U 3	AD27	S	AD27	–	–	–
AA 4	AD28	S	AD28	–	–	–
Y 4	AD29	S	AD29	–	–	–
AB 3	AD30	S	AD30	–	–	–
AA 3	AD31	S	AD31	–	–	–
J 6	AA0	S	AA0	–	–	–

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
J 4	AA1	S	AA1	–	–	–
R 3	AA2	S	AA2	–	–	–
M 3	AA3	S	AA3	–	–	–
H 5	AA4	S	AA4	–	–	–
M 2	AA5	S	AA5	–	–	–
J 2	AA6	S	AA6	–	–	–
M 1	AA7	S	AA7	–	–	–
J 1	AA8	S	AA8	–	–	–
M 4	AA9	S	AA9	–	–	–
L 4	AA10	S	AA10	–	–	–
K 2	AA11	S	AA11	–	–	–
L 3	AA12	S	AA12	–	–	–
M 5	AA13	S	AA13	–	–	–
K 1	AA14	S	AA14	–	–	–
P 4	AA15	S	AA15	–	–	–
P 3	ABA0	S	ABA0	–	–	–
J 3	ABA1	S	ABA1	–	–	–
L 5	ABA2	S	ABA2	–	–	–
D 3	PADQS0	S	PADQS0	–	–	–
W 2	PADQS1	S	PADQS1	–	–	–
E 2	PADQS2	S	PADQS2	–	–	–
W 3	PADQS3	S	PADQS3	–	–	–
E 4	NADQS0	S	NADQS0	–	–	–
Y 1	NADQS1	S	NADQS1	–	–	–
F 1	NADQS2	S	NADQS2	–	–	–
W 4	NADQS3	S	NADQS3	–	–	–
F 3	ADQM0	S	ADQM0	–	–	–
W 1	ADQM1	S	ADQM1	–	–	–
E 1	ADQM2	S	ADQM2	–	–	–
Y 3	ADQM3	S	ADQM3	–	–	–
R 2	ANRAS	S	ANRAS	–	–	–
P 2	ANCAS	S	ANCAS	–	–	–
P 1	ANCS0	S	ANCS0	–	–	–
U 5	ANCS1	S	ANCS1	–	–	–
L 2	ACK	S	ACK	–	–	–
L 1	ACKB	S	ACKB	–	–	–

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
H 2	ACKE0	S	ACKE0	–	–	–
R 5	ACKE1	S	ACKE1	–	–	–
J 5	ANWE	S	ANWE	–	–	–
R 4	ARST	S	ARST	–	–	–
R 1	AODT0	S	AODT0	–	–	–
P 5	AODT1	S	AODT1	–	–	–
T 1	AREF1	P	AREF1	–	–	–
T 2	AREF2	P	AREF2	–	–	–
V 5	ZQ	S	ZQ	–	–	–

2.3.2.2 MCU-S

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
Y 23	SD0	S	SD0	GPIOB13	–	–
W 23	SD1	S	SD1	GPIOB15	–	–
W 22	SD2	S	SD2	GPIOB17	–	–
V 23	SD3	S	SD3	GPIOB19	–	–
V 22	SD4	S	SD4	GPIOB20	–	–
W21	SD5	S	SD5	GPIOB21	–	–
V21	SD6	S	SD6	GPIOB22	–	–
U 22	SD7	S	SD7	GPIOB23	–	–
AA 25	SD8	S	SD8	GPIOB24	TSIDATA0_0	–
AB 25	SD9	S	SD9	GPIOB25	TSIDATA0_1	–
AC 25	SD10	S	SD10	GPIOB26	TSIDATA0_2	–
AD 25	SD11	S	SD11	GPIOB27	TSIDATA0_3	–
AE 25	SD12	S	SD12	GPIOB28	TSIDATA0_4	UARTRXD4
AE 24	SD13	S	SD13	GPIOB29	TSIDATA0_5	UARTTXD4
AD 24	SD14	S	SD14	GPIOB30	TSIDATA0_6	–
AC 24	SD15	S	SD15	GPIOB31	TSIDATA0_7	–
N19	SDEX0	S	GPIOA30	VID1_0	SDEX0	I2SBCLK1
P20	SDEX1	S	GPIOB0	VID1_1	SDEX1	I2SLRCLK1
P19	SDEX2	S	GPIOB2	VID1_2	SDEX2	I2SBCLK2
R20	SDEX3	S	GPIOB4	VID1_3	SDEX3	I2SLRCLK2
R19	SDEX4	S	GPIOB6	VID1_4	SDEX4	I2SDOUT1
V20	SDEX5	S	GPIOB8	VID1_5	SDEX5	I2SDOUT2

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
U20	SDEX6	S	GPIOB9	VID1_6	SDEX6	I2SDIN1
V19	SDEX7	S	GPIOB10	VID1_7	SDEX7	I2SDIN2
AD 23	SA0	S	SA0	GPIOC0	TSERR0	–
AE 23	SA1	S	SA1	GPIOC1	TSERR1	–
AA 22	SA2	S	SA2	GPIOC2	–	–
W18	SA3	S	SA3	GPIOC3	HDMI_CEC	SDnRST0
AC 22	SA4	S	SA4	GPIOC4	UARTnDCD1	SDnINT0
AD 22	SA5	S	SA5	GPIOC5	UARTnCTS1	SDWP0
AE 22	SA6	S	SA6	GPIOC6	UARTnRTS1	SDnCD0
AE 21	SA7	S	SA7	GPIOC7	UARTnDSR1	SDnRST1
AD 21	SA8	S	SA8	GPIOC8	UARTnDTR1	SDnINT1
AB 24	SA9	S	SA9	GPIOC9	SPICLK2	PDMStrobe
W16	SA10	S	SA10	GPIOC10	SPIFRM2	–
W 14	SA11	S	SA11	GPIOC11	SPIRXD2	USB2.0OTG_DrvVBUS
W15	SA12	S	SA12	GPIOC12	SPITXD2	SDnRST2
W13	SA13	S	SA13	GPIOC13	PWM1	SDnINT2
AD 12	SA14	S	SA14	GPIOC14	PWM2	VICLK2
AD 14	SA15	S	SA15	GPIOC15	TSICLK0	VIHSYNC2
AE 14	SA16	S	SA16	GPIOC16	TSISYNC0	VIVSYNC2
AA 14	SA17	S	SA17	GPIOC17	TSIDP0	VID2_0
AB 12	SA18	S	SA18	GPIOC18	SDCLK2	VID2_1
AB 14	SA19	S	SA19	GPIOC19	SDCMD2	VID2_2
AB 11	SA20	S	SA20	GPIOC20	SDDAT2_0	VID2_3
AA12	SA21	S	SA21	GPIOC21	SDDAT2_1	VID2_4
AC 14	SA22	S	SA22	GPIOC22	SDDAT2_2	VID2_5
AC 12	SA23	S	SA23	GPIOC23	SDDAT2_3	VID2_6
AA 9	SA24	S	GPIOD28	VID0_0	TSIDATA1_0	SA24
AE 15	SA25	S	GPIOD1	PWM0	SA25	–
AD 20	NSCS0	S	NSCS0	–	–	–
AB 21	NSCS1	S	GPIOC28	NSCS1	UARTnRI1	–
AB 20	NSWE	S	NSWE	GPIOE31	–	–
AE 20	NSOE	S	NSOE	GPIOE30	–	–
AB 23	RDNWR	S	RDNWR	GPIOC26	PDMDATA0	–
AA 24	NSDQM	S	NSDQM	GPIOC27	PDMDATA1	–
AC 21	NSWAIT	S	NSWAIT	GPIOC25	SPDIFTX	–

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AE 12	LATADDR	S	LATADDR	GPIOC24	SPDIFRX	VID2_7
W 25	CLE0	S	CLE0	CLE1	GPIOB11	–
W 24	ALE0	S	ALE0	ALE1	GPIOB12	–
AA 23	RNB0	S	RnB0	RnB1	GPIOB14	–
Y 22	NNFOE0	S	NNFOE0	NNFOE1	GPIOB16	–
V 25	NNFWE0	S	NNFWE0	nNFWE1	GPIOB18	–
Y 25	NNCS0	S	NNCS0	–	–	–
Y 24	NNCS1	S	NNCS1	–	–	–

2.3.2.3 Digital RGB

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
J23	DISD0	S	GPIOA1	DISD0	–	–
G21	DISD1	S	GPIOA2	DISD1	–	–
H21	DISD2	S	GPIOA3	DISD2	–	–
H20	DISD3	S	GPIOA4	DISD3	–	–
L19	DISD4	S	GPIOA5	DISD4	–	–
F21	DISD5	S	GPIOA6	DISD5	–	–
L20	DISD6	S	GPIOA7	DISD6	–	–
J19	DISD7	S	GPIOA8	DISD7	–	–
J22	DISD8	S	GPIOA9	DISD8	–	–
M19	DISD9	S	GPIOA10	DISD9	–	–
L22	DISD10	S	GPIOA11	DISD10	–	–
L21	DISD11	S	GPIOA12	DISD11	–	–
K19	DISD12	S	GPIOA13	DISD12	–	–
G22	DISD13	S	GPIOA14	DISD13	–	–
M22	DISD14	S	GPIOA15	DISD14	–	–
L23	DISD15	S	GPIOA16	DISD15	–	–
M21	DISD16	S	GPIOA17	DISD16	–	–
P22	DISD17	S	GPIOA18	DISD17	–	–
R23	DISD18	S	GPIOA19	DISD18	–	–
P21	DISD19	S	GPIOA20	DISD19	–	–
R24	DISD20	S	GPIOA21	DISD20	–	–
R21	DISD21	S	GPIOA22	DISD21	–	–
M20	DISD22	S	GPIOA23	DISD22	–	–
R22	DISD23	S	GPIOA24	DISD23	–	–
R25	DISCLK	S	GPIOA0	DISCLK	–	–
J21	DISVSYNC	S	GPIOA25	DISVSYNC	–	–
J20	DISHSYNC	S	GPIOA26	DISHSYNC	–	–
H22	DISDE	S	GPIOA27	DISDE	–	–

2.3.2.4 HDMI

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
B 24	HDMI_TXP0	S	HDMI_TXP0	–	–	–
A 24	HDMI_TXN0	S	HDMI_TXN0	–	–	–
B 23	HDMI_TXP1	S	HDMI_TXP1	–	–	–
A 23	HDMI_TXN1	S	HDMI_TXN1	–	–	–
B 22	HDMI_TXP2	S	HDMI_TXP2	–	–	–
A 22	HDMI_TXN2	S	HDMI_TXN2	–	–	–
B 25	HDMI_TXPCLK	S	HDMI_TXPCLK	–	–	–
A 25	HDMI_TXNCLK	S	HDMI_TXNCLK	–	–	–
Y 21	HDMI_CEC	S	SA3	GPIOC3	HDMI_CEC	SDnRST0
A 21	HDMI_HOT5V	S	HDMI_HOT5V	–	–	–
B 21	HDMI_REXT	S	HDMI_REXT	–	–	–

2.3.2.5 LVDS

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
C 15	LVDS_TP0	S	LVDS_TP0	–	–	–
C 14	LVDS_TN0	S	LVDS_TN0	–	–	–
B 14	LVDS_TP1	S	LVDS_TP1	–	–	–
A 14	LVDS_TN1	S	LVDS_TN1	–	–	–
B 15	LVDS_TP2	S	LVDS_TP2	–	–	–
A 15	LVDS_TN2	S	LVDS_TN2	–	–	–
B 17	LVDS_TP3	S	LVDS_TP3	–	–	–
A 17	LVDS_TN3	S	LVDS_TN3	–	–	–
B 18	LVDS_TP4	S	LVDS_TP4	–	–	–
A 18	LVDS_TN4	S	LVDS_TN4	–	–	–
B 16	LVDS_TPCLK	S	LVDS_TPCLK	–	–	–
A 16	LVDS_TNCLK	S	LVDS_TNCLK	–	–	–
C 19	LVDS_ROUT	S	LVDS_ROUT	–	–	–

2.3.2.6 MIPI DSI

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
B 8	MIPIDSI_DP0	S	MIPIDSI_DP0	–	–	–
A 8	MIPIDSI_DN0	S	MIPIDSI_DN0	–	–	–
B 9	MIPIDSI_DP1	S	MIPIDSI_DP1	–	–	–
A 9	MIPIDSI_DN1	S	MIPIDSI_DN1	–	–	–
B 10	MIPIDSI_DP2	S	MIPIDSI_DP2	–	–	–
A 10	MIPIDSI_DN2	S	MIPIDSI_DN2	–	–	–
B 11	MIPIDSI_DP3	S	MIPIDSI_DP3	–	–	–
A 11	MIPIDSI_DN3	S	MIPIDSI_DN3	–	–	–
B 7	MIPIDSI_DPCLK	S	MIPIDSI_DPCLK	–	–	–
A 7	MIPIDSI_DNCLK	S	MIPIDSI_DNCLK	–	–	–
C 7	MIPIDSI_VREG_0P4V	S	MIPIDSI_VREG_0P4V	–	–	–

2.3.2.7 MIPI CSI

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
B 2	MIPICSI_DP0	S	MIPICSI_DP0	–	–	–
A 2	MIPICSI_DN0	S	MIPICSI_DN0	–	–	–
B 3	MIPICSI_DP1	S	MIPICSI_DP1	–	–	–
A 3	MIPICSI_DN1	S	MIPICSI_DN1	–	–	–
B 4	MIPICSI_DP2	S	MIPICSI_DP2	–	–	–
A 4	MIPICSI_DN2	S	MIPICSI_DN2	–	–	–
B 5	MIPICSI_DP3	S	MIPICSI_DP3	–	–	–
A 5	MIPICSI_DN3	S	MIPICSI_DN3	–	–	–
B1	MIPICSI_DPCLK	S	MIPICSI_DPCLK	–	–	–
A1	MIPICSI_DNCLK	S	MIPICSI_DNCLK	–	–	–

2.3.2.8 VIP

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AA 9	VID0_0	S	GPIOD28	VID0_0	TSIDATA1_0	SA24
AC 9	VID0_1	S	GPIOD29	VID0_1	TSIDATA1_1	–
AD 9	VID0_2	S	GPIOD30	VID0_2	TSIDATA1_2	–
AC 11	VID0_3	S	GPIOD31	VID0_3	TSIDATA1_3	–
AB 9	VID0_4	S	GPIOE0	VID0_4	TSIDATA1_4	–
AE 9	VID0_5	S	GPIOE1	VID0_5	TSIDATA1_5	–
AE 10	VID0_6	S	GPIOE2	VID0_6	TSIDATA1_6	–
AE 11	VID0_7	S	GPIOE3	VID0_7	TSIDATA1_7	–
AD 10	VICLK0	S	GPIOE4	VICLK0	TSICLK1	–
AA 11	VIHSYNC0	S	GPIOE5	VIHSYNC0	TSISYNC1	–
AD 11	VIVSYNC0	S	GPIOE6	VIVSYNC0	TSIDP1	–
J 21	VID1_0	S	GPIOA30	VID1_0	SDEX0	I2SBCLK1
L 20	VID1_1	S	GPIOB0	VID1_1	SDEX1	I2SLRCLK1
M 20	VID1_2	S	GPIOB2	VID1_2	SDEX2	I2SBCLK2
P 20	VID1_3	S	GPIOB4	VID1_3	SDEX3	I2SLRCLK2
R 20	VID1_4	S	GPIOB6	VID1_4	SDEX4	I2SDOUT1
U 20	VID1_5	S	GPIOB8	VID1_5	SDEX5	I2SDOUT2
V 20	VID1_6	S	GPIOB9	VID1_6	SDEX6	I2SDIN1
W 21	VID1_7	S	GPIOB10	VID1_7	SDEX7	I2SDIN2
J 20	VICLK1	S	GPIOA28	VICLK1	I2SMCLK2	I2SMCLK1
E 14	VIHSYNC1	S	GPIOE13	GMAC_COL	VIHSYNC1	–
D 11	VIVSYNC1	S	GPIOE7	GMAC_TXD0	VIVSYNC1	–
AA 14	VID2_0	S	SA17	GPIOC17	TSIDP0	VID2_0
AB 12	VID2_1	S	SA18	GPIOC18	SDCLK2	VID2_1
AB 14	VID2_2	S	SA19	GPIOC19	SDCMD2	VID2_2
AB 11	VID2_3	S	SA20	GPIOC20	SDDAT2_0	VID2_3
Y 11	VID2_4	S	SA21	GPIOC21	SDDAT2_1	VID2_4
AC 14	VID2_5	S	SA22	GPIOC22	SDDAT2_2	VID2_5
AC 12	VID2_6	S	SA23	GPIOC23	SDDAT2_3	VID2_6
AE 12	VID2_7	S	LATADDR	GPIOC24	SPDIFRX	VID2_7
AD 12	VICLK2	S	SA14	GPIOC14	PWM2	VICLK2
AD 14	VIHSYNC2	S	SA15	GPIOC15	TSICLK0	VIHSYNC2
AE 14	VIVSYNC2	S	SA16	GPIOC16	TSISYNC0	VIVSYNC2

2.3.2.9 Ethernet MAC

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
D 11	GMAC_TXD0	S	GPIOE7	GMAC_TXD0	VIVSYNC1	–
C 11	GMAC_TXD1	S	GPIOE8	GMAC_TXD1	–	–
C 12	GMAC_TXD2	S	GPIOE9	GMAC_TXD2	–	–
D 12	GMAC_TXD3	S	GPIOE10	GMAC_TXD3	–	–
E 12	GMAC_TXEN	S	GPIOE11	GMAC_TXEN	–	–
E 11	GMAC_TXER	S	GPIOE12	GMAC_TXER	–	–
E 14	GMAC_COL	S	GPIOE13	GMAC_COL	VIHSYNC1	–
D 17	GMAC_RXD0	S	GPIOE14	GMAC_RXD0	SPICLK1	–
C 17	GMAC_RXD1	S	GPIOE15	GMAC_RXD1	SPIFRM1	–
D 18	GMAC_RXD2	S	GPIOE16	GMAC_RXD2	–	–
C 18	GMAC_RXD3	S	GPIOE17	GMAC_RXD3	–	–
E 18	GMAC_RXCLK	S	GPIOE18	GMAC_RXCLK	SPIRXD1	–
E 17	GMAC_RXDV	S	GPIOE19	GMAC_RXDV	SPITXD1	–
D 15	GMAC_MDC	S	GPIOE20	GMAC_MDC	–	–
D 14	GMAC_MDIO	S	GPIOE21	GMAC_MDIO	–	–
E 15	GMAC_RXER	S	GPIOE22	GMAC_RXER	–	–
B 12	GMAC_CRS	S	GPIOE23	GMAC_CRS	–	–
A 12	GMAC_GTXCLK	S	GPIOE24	GMAC_GTXCLK	–	–

2.3.2.10 MPEG-TS Interface

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AA 25	TSIDATA0_0	S	SD8	GPIOB24	TSIDATA0_0	–
AB 25	TSIDATA0_1	S	SD9	GPIOB25	TSIDATA0_1	–
AC 25	TSIDATA0_2	S	SD10	GPIOB26	TSIDATA0_2	–
AD 25	TSIDATA0_3	S	SD11	GPIOB27	TSIDATA0_3	–
AE 25	TSIDATA0_4	S	SD12	GPIOB28	TSIDATA0_4	UARTRXD4
AE 24	TSIDATA0_5	S	SD13	GPIOB29	TSIDATA0_5	UARTTXD4
AD 24	TSIDATA0_6	S	SD14	GPIOB30	TSIDATA0_6	–
AC 24	TSIDATA0_7	S	SD15	GPIOB31	TSIDATA0_7	–
AD 14	TSICLK0	S	SA15	GPIOC15	TSICLK0	VIHSYNC2
AE 14	TSISYNC0	S	SA16	GPIOC16	TSISYNC0	VIVSYNC2
AA 14	TSIDP0	S	SA17	GPIOC17	TSIDP0	VID2_0
AA 9	TSIDATA1_0	S	GPIOD28	VID0_0	TSIDATA1_0	SA24
AC 9	TSIDATA1_1	S	GPIOD29	VID0_1	TSIDATA1_1	–
AD 9	TSIDATA1_2	S	GPIOD30	VID0_2	TSIDATA1_2	–
AC 11	TSIDATA1_3	S	GPIOD31	VID0_3	TSIDATA1_3	–
AB 9	TSIDATA1_4	S	GPIOE0	VID0_4	TSIDATA1_4	–
AE 9	TSIDATA1_5	S	GPIOE1	VID0_5	TSIDATA1_5	–
AE 10	TSIDATA1_6	S	GPIOE2	VID0_6	TSIDATA1_6	–
AE 11	TSIDATA1_7	S	GPIOE3	VID0_7	TSIDATA1_7	–
AD 10	TSICLK1	S	GPIOE4	VICLK0	TSICLK1	–
AA 11	TSISYNC1	S	GPIOE5	VIHSYNC0	TSISYNC1	–
AD 11	TSIDP1	S	GPIOE6	VIVSYNC0	TSIDP1	–

2.3.2.11 UART_ISO7816

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AD 19	UARTTXD0	S	GPIOD18	UARTTXD0	ISO7816	SDWP2
AE 19	UARTRXD0	S	GPIOD14	UARTRXD0	ISO7816	–
AD 18	UARTTXD1	S	GPIOD19	UARTTXD1	ISO7816	SDnCD2
AE 18	UARTRXD1	S	GPIOD15	UARTRXD1	ISO7816	–
AC 22	UARTnDCD1	S	SA4	GPIOC4	UARTnDCD1	SDnINT0
AD 22	UARTnCTS1	S	SA5	GPIOC5	UARTnCTS1	SDWP0
AE 22	UARTnRTS1	S	SA6	GPIOC6	UARTnRTS1	SDnCD0
AE 21	UARTnDSR1	S	SA7	GPIOC7	UARTnDSR1	SDnRST1
AD 21	UARTnDTR1	S	SA8	GPIOC8	UARTnDTR1	SDnINT1
AB 21	UARTnRI1	S	GPIOC28	NSCS1	UARTnRI1	–
Y 18	UARTTXD2	S	GPIOD20	UARTTXD2	–	SDWP1
Y 19	UARTRXD2	S	GPIOD16	UARTRXD2	–	–
W 17	UARTTXD3	S	GPIOD21	UARTTXD3	–	SDnCD1
Y 17	UARTRXD3	S	GPIOD17	UARTRXD3	–	–
AE 24	UARTTXD4	S	SD13	GPIOB29	TSIDATA0_5	UARTTXD4
AE 25	UARTRXD4	S	SD12	GPIOB28	TSIDATA0_4	UARTRXD4

2.3.2.12 I2C

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AC 19	SDA0	S	GPIOD3	SDA0	ISO7816	–
AC 20	SCL0	S	GPIOD2	SCL0	ISO7816	–
AB 18	SDA1	S	GPIOD5	SDA1	–	–
AB 17	SCL1	S	GPIOD4	SCL1	–	–
AB 19	SDA2	S	GPIOD7	SDA2	–	–
AC 18	SCL2	S	GPIOD6	SCL2	–	–

2.3.2.13 SPI/SSP

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AE 16	SPITXD0	S	GPIOC31	SPITXD0	–	–
AD 16	SPIRXD0	S	GPIOD0	SPIRXD0	PWM3	–
AE 17	SPICLK0	S	GPIOC29	SPICLK0	–	–
AD 17	SPIFRM0	S	GPIOC30	SPIFRM0	–	–
E 17	SPITXD1	S	GPIOE19	GMAC_RXDV	SPITXD1	–
E 18	SPIRXD1	S	GPIOE18	GMAC_RXCLK	SPIRXD1	–
D 17	SPICLK1	S	GPIOE14	GMAC_RXD0	SPICLK1	–
C 17	SPIFRM1	S	GPIOE15	GMAC_RXD1	SPIFRM1	–
V 15	SPITXD2	S	SA12	GPIOC12	SPITXD2	SDnRST2
W 14	SPIRXD2	S	SA11	GPIOC11	SPIRXD2	USB2.0OTG_DrvVBUS
AB 24	SPICLK2	S	SA9	GPIOC9	SPICLK2	PDMStrobe
V 19	SPIFRM2	S	SA10	GPIOC10	SPIFRM2	–

2.3.2.14 PWM

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AE 15	PWM0	S	GPIOD1	PWM0	SA25	–
V 14	PWM1	S	SA13	GPIOC13	PWM1	SDnINT2
AD 12	PWM2	S	SA14	GPIOC14	PWM2	VICLK2
AD 16	PWM3	S	GPIOD0	SPIRXD0	PWM3	–

2.3.2.15 PPM

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
Y 12	PPM	S	GPIOD8	PPM	–	–

2.3.2.16 PDM

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AB 23	PDMDATA0	S	RDNWR	GPIOC26	PDMDATA0	–
AA 24	PDMDATA1	S	NSDQM	GPIOC27	PDMDATA1	–
AB 24	PDMStrobe	S	SA9	GPIOC9	SPICLK2	PDMStrobe

2.3.2.17 SPDIF

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AC 21	SPDIFTX	S	NSWAIT	GPIOC25	SPDIFTX	–
AE 12	SPDIFRX	S	LATADDR	GPIOC24	SPDIFRX	VID2_7

2.3.2.18 SD/MMC

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
T 25	SDDAT0_0	S	GPIOB1	SDDAT0_0	–	–
U 24	SDDAT0_1	S	GPIOB3	SDDAT0_1	–	–
U 25	SDDAT0_2	S	GPIOB5	SDDAT0_2	–	–
V 24	SDDAT0_3	S	GPIOB7	SDDAT0_3	–	–
T 24	SDCLK0	S	GPIOA29	SDCLK0	–	–
U 23	SDCMD0	S	GPIOA31	SDCMD0	–	–
AD 22	SDWP0	S	SA5	GPIOC5	UARTnCTS1	SDWP0
AE 22	SDnCD0	S	SA6	GPIOC6	UARTnRTS1	SDnCD0
Y 21	SDnRST0	S	SA3	GPIOC3	HDMI_CEC	SDnRST0
AC 22	SDnINT0	S	SA4	GPIOC4	UARTnDCD1	SDnINT0
AA 18	SDDAT1_0	S	GPIOD24	SDDAT1_0	–	–
AA 17	SDDAT1_1	S	GPIOD25	SDDAT1_1	–	–
Y 15	SDDAT1_2	S	GPIOD26	SDDAT1_2	–	–
Y 14	SDDAT1_3	S	GPIOD27	SDDAT1_3	–	–
AA 20	SDCLK1	S	GPIOD22	SDCLK1	–	–
AA 19	SDCMD1	S	GPIOD23	SDCMD1	–	–
Y 18	SDWP1	S	GPIOD20	UARTTXD2	–	SDWP1
W 17	SDnCD1	S	GPIOD21	UARTTXD3	–	SDnCD1
AE 21	SDnRST1	S	SA7	GPIOC7	UARTnDSR1	SDnRST1
AD 21	SDnINT1	S	SA8	GPIOC8	UARTnDTR1	SDnINT1
AB 11	SDDAT2_0	S	SA20	GPIOC20	SDDAT2_0	VID2_3
Y 11	SDDAT2_1	S	SA21	GPIOC21	SDDAT2_1	VID2_4
AC 14	SDDAT2_2	S	SA22	GPIOC22	SDDAT2_2	VID2_5
AC 12	SDDAT2_3	S	SA23	GPIOC23	SDDAT2_3	VID2_6
AB 12	SDCLK2	S	SA18	GPIOC18	SDCLK2	VID2_1
AB 14	SDCMD2	S	SA19	GPIOC19	SDCMD2	VID2_2
AD 19	SDWP2	S	GPIOD18	UARTTXD0	ISO7816	SDWP2
AD 18	SDnCD2	S	GPIOD19	UARTTXD1	ISO7816	SDnCD2

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
V 15	SDnRST2	S	SA12	GPIOC12	SPITXD2	SDnRST2
V 14	SDnINT2	S	SA13	GPIOC13	PWM1	SDnINT2

2.3.2.19 USB2.0 HOST

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
F 25	USB2.0HOST_DP	S	USB2.0HOST_DP	–	–	–
F 24	USB2.0HOST_DM	S	USB2.0HOST_DM	–	–	–
G 25	USB2.0HOST_RKELVIN	S	USB2.0HOST_RKELVIN	–	–	–

2.3.2.20 USB2.0 HSIC HOST

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
H 24	USBHSIC_DATA	S	USBHSIC_DATA	–	–	–
H 25	USBHSIC_STROBE	S	USBHSIC_STROBE	–	–	–

2.3.2.21 USB2.0 OTG

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
D 25	USB2.0OTG_DP	S	USB2.0OTG_DP	–	–	–
D 24	USB2.0OTG_DM	S	USB2.0OTG_DM	–	–	–
E 25	USB2.0OTG_RKELVIN	S	USB2.0OTG_RKELVIN	–	–	–
C 25	USB2.0OTG_ID	S	USB2.0OTG_ID	–	–	–
C 24	USB2.0OTG_VBUS	S	USB2.0OTG_VBUS	–	–	–
W 14	USB2.0OTG_DrvVBUS	S	SA11	GPIOC11	SPIRXD2	USB2.0OTG_DrvVBUS
E 24	USB2.0OTG_USBVBUS	S	USB2.0OTG_USBVBUS	–	–	–

2.3.2.22 I2S& AC97

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AD 15	I2SDOUT0	S	GPIOD9	I2SDOUT0	AC97_DOUT	–
AC 15	I2SDIN0	S	GPIOD11	I2SDIN0	AC97_DIN	–
AB 15	I2SBCLK0	S	GPIOD10	I2SBCLK0	AC97_BCLK	–
AA 15	I2SMCLK0	S	GPIOD13	I2SMCLK0	AC97_nRST	–
AC 17	I2SLRCLK0	S	GPIOD12	I2SLRCLK0	AC97_SYNC	–
R 20	I2SDOUT1	S	GPIOB6	VID1_4	SDEX4	I2SDOUT1
V 20	I2SDIN1	S	GPIOB9	VID1_6	SDEX6	I2SDIN1
J 21	I2SBCLK1	S	GPIOA30	VID1_0	SDEX0	I2SBCLK1
J 20	I2SMCLK1	S	GPIOA28	VICLK1	I2SMCLK2	I2SMCLK1
L 20	I2SLRCLK1	S	GPIOB0	VID1_1	SDEX1	I2SLRCLK1
U 20	I2SDOUT2	S	GPIOB8	VID1_5	SDEX5	I2SDOUT2
W 21	I2SDIN2	S	GPIOB10	VID1_7	SDEX7	I2SDIN2
M 20	I2SBCLK2	S	GPIOB2	VID1_2	SDEX2	I2SBCLK2
J 20	I2SMCLK2	S	GPIOA28	VICLK1	I2SMCLK2	I2SMCLK1
P 20	I2SLRCLK2	S	GPIOB4	VID1_3	SDEX3	I2SLRCLK2

2.3.2.23 ADC

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AE 3	ADC0	S	ADC0	–	–	–
AB 5	ADC1	S	ADC1	–	–	–
AD 3	ADC2	S	ADC2	–	–	–
AE 2	ADC3	S	ADC3	–	–	–
AC1	ADC4	S	ADC4	–	–	–
AD1	ADC5	S	ADC5	–	–	–
AD 2	ADC6	S	ADC6	–	–	–
AD 6	ADC7	S	ADC7	–	–	–

2.3.2.24 ALIVE GPIO

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AB 8	ALIVEGPIO0	S	ALIVEGPIO0	–	–	–
AA 8	ALIVEGPIO1	S	ALIVEGPIO1	–	–	–
AA 7	ALIVEGPIO2	S	ALIVEGPIO2	–	–	–
Y 9	ALIVEGPIO3	S	ALIVEGPIO3	–	–	–
Y 8	ALIVEGPIO4	S	ALIVEGPIO4	–	–	–
W 9	ALIVEGPIO5	S	ALIVEGPIO5	–	–	–

2.3.2.25 JTAG

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
V 6	NTRST	S	NTRST	GPIOE25	–	–
Y 5	TMS	S	TMS	GPIOE26	–	–
W 5	TDI	S	TDI	GPIOE27	–	–
AA 6	TCLK	S	TCLK	GPIOE28	–	–
Y 7	TDO	S	TDO	GPIOE29	–	–

2.3.2.26 Crystal PLL & RTC

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
A 20	PLLXTI	S	PLLXTI	–	–	–
B 20	PLLXTO	S	PLLXTO	–	–	–
AE 4	RTCXTI	S	RTCXTI	–	–	–
AD 4	RTCXTO	S	RTCXTO	–	–	–

2.3.2.27 Miscellaneous

Ball	Name	Type	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
AE1	NRESET	S	NRESET	–	–	–
AB 7	NGRESETOUT	S	NGRESETOUT	–	–	–
AB 6	VDDPWRON	S	VDDPWRON	–	–	–
AC 6	VDDPWRON_DDR	S	VDDPWRON_DDR	–	–	–
AE 6	NVDDPWRTOGGLE	S	NVDDPWRTOGGLE	–	–	–
AB 2	NBATF	S	NBATF	–	–	–
AE 7	TEST_EN	S	TEST_EN	–	–	–
AD 8	WIRE0	S	WIRE0	–	–	–
AE 8	WIRE1	S	WIRE1	–	–	–
AD 7	EFUSE_FSOURCE	S	EFUSE_FSOURCE	–	–	–

2.3.2.28 Power: VDD

Ball	Name	Type	Description
D5, D6, E6, E7, E8, G11, J12, J14, K11, K13, K15, L12, L14, L16, L17, M11, M13, M15, N12, P11, R12, T11, U12, V11, V12, W11, W12	VDDI	P	1.0 V for CORE
N14, N16, P13, P15, P16, R14, R15, R16, T14, T15, T16, U14, U15	VDDI_ARM	P	1.0 V to 1.3 V for CPU.
K9, K10, L9, L10, M9, M10, N9, N10, P9, P10, R9, R10, T9, T10	VDDQ	P	1.5 V for DDR3 IO
U10, U11, V9	VDDP18	P	1.8 V for Internal IO
L19, M19, P19, R18, R19, U18, U19, V17	DVDD33_IO	P	3.3 V for IO
E23	DVDD10_USB0	P	1.0 V for USB
G23	DVDD10_USBHOST0	P	1.0 V for USB HOST
F23	VDD18_USB0	P	1.8 V for USB
F21	VDD18_USBHOST	P	1.8 V for USB HOST
E22	VDD33_USB0	P	3.3 V for USB
G24	VDD33_USBHOST	P	3.3 V for USB HOST
H23	DVDD12_HSIC	P	1.2 V for USB HSIC HOST
AC8	VDDI10_ALIVE	P	1.0 V for ALIVE
V7	VDDP18_ALIVE	P	1.8 V for Internal IO ALIVE
W8	VDD33_ALIVE	P	3.3 V for ALIVE
AC4, AC7	VDD18_RTC	P	1.8 V for RTC

Ball	Name	Type	Description
D20	VDD18_OSC	P	1.8 V for Crystal
G14	AVDD10_LV	P	1.0 V for LVDS
F15	AVDD18_LV	P	1.8 V for LVDS
C22	AVDD10_HM	P	1.0 V for HDMI
F19	VDD10_HM_PLL	P	1.0 V for HDMI PLL
D23	VDD18_HM	P	1.8 V for HDMI
C8	M_VDD10_PLL	P	1.0 V for MIPI PLL
C4, C5, D7, D8	M_VDD10	P	1.0 V for MIPI
C6	M_VDD18	P	1.8 V for MIPI
AC5	AVDD18_ADC	P	1.8 V for ADC
AC2	ADCREF	P	1.8 V for ADC reference VDD
C21, D19, D21, E20	AVDD18_PLL	P	1.8 V for PLL
T13, U13	DVDD_VID2_SD2	P	2.8 V for VID2/SD2
AA12	DVDD_VID0	P	2.8 V for VID0
F14	DVDD_GMAC	P	2.8 V for Ethernet MAC

2.3.2.29 Power: GND

Ball	Name	Type	Description
A6, A19, B6, B19, C9, D9, E9, F7, F8, F9, F22, G8, G9, G12, G17, G21, G22, H6, H7, H9, H11, H12, H14, H15, H17, H19, H20, J7, J8, J10, J11, J13, J15, J16, J18, J19, K12, K14, K16, K17, L6, L7, L8, L11, L13, L15, L18, M6, M7, M8, M12, 14, M16, M17, M18, N11, N13, N15, N17, P6, P7, P8, P12, P14, P17, P18, R6, R7, R8, R11, R13, R17, T12, T17, U6, U7, U8, U16, W15, W18	VSSI	G	Digital GND
C20	VSS18_OSC	G	GND for 1.8 V Crystal VDD
G15	AVSS10_LV	G	GND for 1.0 V LVDS VDD
F11, F12	AVSS18_LV	G	GND for 1.8 V LVDS VDD
AD5	AVSS18_ADC	G	GND for 1.8 V ADC VDD
E19, F17, F18, G18	AVSS18_PLL	G	GND for 1.8 V PLL VDD

3 System Boot

3.1 Overview

S5P4418 supports various system boot modes. Boot Mode is determined by System Configuration when boot reset off.

- External Static Memory Boot
- Internal ROM Boot
  - NAND boot with Error Correction
  - SD/MMC/eMMC boot
  - SPI Serial EEPROM boot
  - UART boot
  - USB boot

3.2 Functional Description

3.2.1 System Configuration

Table 3-1 System Configuration by RST_CFG Pins

Pins	RST_CFG	Static Memory	SDFS(TBD)	UART	Serial Flash	SD MMC	USB Device	Nand
SD0	RST_CFG0	0	1	1	0	1	0	1
SD1	RST_CFG1	0	0	1	0	0	1	1
SD2	RST_CFG2	0	0	0	1	1	1	1
SD3	RST_CFG3	-	Port_Num0	Port_Num0	Port_Num0	Port_Num0	-	SELCS
SD4	RST_CFG4				ADDRWIDTH0	eMMCBOOTMODE		
SD5	RST_CFG5				ADDRWIDTH1	PARTITION		
SD6	RST_CFG6			BAUD	SPEED	eMMCBOOT		
SD7	RST_CFG7							
DISD0	RST_CFG8	LATADDR	LATADDR	LATADDR	LATADDR	LATADDR	LATADDR	LATADDR
DISD1	RST_CFG9	BUSWIDTH	0	0	0	0	0	0
DISD2	RST_CFG10							NANDPAGE1
DISD3	RST_CFG11							NANDTYPE0
DISD4	RST_CFG12							NANDTYPE1
DISD5	RST_CFG13							NANDPAGE0
DISD6	RST_CFG14		DECRYPT	DECRYPT	DECRYPT	DECRYPT	DECRYPT	DECRYPT
DISD7	RST_CFG15		I-Cache	I-Cache	I-Cache	I-Cache	I-Cache	I-Cache
VID1[0]	RST_CFG16		Next Try		Next Try	Next Try		Next Try
VID1[1]	RST_CFG17						SEL_VBUS	
VID1[2]	RST_CFG18		Next Port		Next Port	Next Port		Next Port
VID1[3]	RST_CFG19		Port_Num1		Port_Num1	Port_Num1		Port_Num1
VID1[4]	RST_CFG20		USE_FS		USE_FS(TBD)	USE_FS(TBD)		
VID1[5]	RST_CFG21							
VID1[6]	RST_CFG22							
VID1[7]	RST_CFG23		CORE_VOLTAGE	CORE_VOLTAGE	CORE_VOLTAGE	CORE_VOLTAGE	CORE_ VOLTAGE	CORE_ VOLTAGE

Table 3-2 System Configuration by Function

Name	Pin	RST_CFG	Note	
NANDTYPE[1:0]	DISD[4:3]	RST_CFG[12:11]	NAND flash Memory Type on SD Bus	0: Small Block 3 Address 1: Small block 4 Address 2: Large 4 Address 3: Large 5 Address
NANDPAGE [1:0]	DISD5	RST_CFG13	Pagesize of Large NAND Flash on SD Bus	0: 2K 1: 4K or above
SELCS	DISD2	RST_CFG10	NAND Chip Select	When SD bus → 0:nNCS0 1:nNCS1 When SDEX bus → nNCS1. (Not selectable)
DECRYPT	DISD6	RST_CFG14	AES ECB mode decrypt	0: not decrypt 1: decrypt
I-Cache	DISD7	RST_CFG15	I-Cache Enable	0: Disable 1: Enable
eMMC Boot Mode	SD4	RST_CFG4	SD / eMMC Boot Selection	0: Normal SD Boot 1: eMMC Boot
PARTITION	SD5	RST_CFG5	Boot Parition on eMMC	0: Default Partition 1: Boot Partition (Partition#1)
ADDRWIDTH[1:0]	SD[5:4]	RST_CFG[5:4]	Serial Flash Address width	0: 16-bit 1: 24-bit 2: 32-bit
eMMCBOOT	SD6	RST_CFG6	Alternative / Normal Boot Selection	0: Alternative Boot 1: Normal Boot
BAUD	SD6	RST_CFG6	UART Baudrate	0: 19200bps 1: 115200bps
SPEED	SD6	RST_CFG6	Serial Flash Speed	0: 1 MHz 1: 16 MHz
LATADDR	DISD0	RST_CFG8	Static Latched Address	0: None 1: Latched
BootMode[2:0]	SD[2:0]	RST_CFG[2:0]	Boot Mode Select	0: Static Memory 3: UART 4: SPI 5: SDMMC 6: USB 7: NAND
Port Num[1:0]				
Core Voltage				
Vbus_Level	VID1[1]	RST_CFG17	Vbus Detect Host Voltage Level	0: 5 V 1: 3.3 V
Boot Scenario				

Table 3-3 Boot Scenario

NextTry	USE_FS (TBD)	NextPort	Port SEL1	Port SEL0	BOOT MODE	Boot Scenario
x	x	x	x	x	6	USB
0	x	x	0	0	4	SPI0 → USB
				1		SPI1 → USB
			1	1		SPI2 → USB
				1		SPI0hs → USB
1	s	0	0	0		SPI0 → SDs0 → USB
				1		SPI1 → SDs1 → USB
			1	0		SPI2 → SDs0 → USB
				1		SPI0hs → SDs1 → USB
		1	0	0		SPI0 → SDs1 → USB
				1		SPI1 → SDs0 → USB
			1	0		SPI2 → SDs1 → USB
				1		SPI0hs → SDs0 → USB
0	x	x	0	0	1, 5	SD0 → USB
				1		SD1 → USB
			1	0		SD2 → USB
				1		SD2hs → USB
1	s	0	0	0		SD0 → SDs2 → USB
				1		SD1 → SDs0 → USB
			1	0		SD2 → SDs1 → USB
				1		SD2hs → SDs1 → USB
		1	0	0		SD0 → SDs1 → USB
				1		SD1 → SDs2 → USB
			1	0		SD2 → SDs0 → USB
				1		SD2hs → SDs0 → USB
0	x	x	x	0	7	NAND0 → USB
				1		NAND1 → USB
1	s	0	0	0		NAND0 → SDs0 → USB
				1		NAND1 → SDs1 → USB
			1	0		NAND0 → SDs2 → USB
				1		NAND1 → SDs2hs → USB
		1	0	0		NAND0 → SDs1 →USB
				1		NAND1 → SDs0 → USB
			1	0		NAND0 → SDs2hs →

NextTry	USE_FS (TBD)	NextPort	Port SEL1	Port SEL0	BOOT MODE	Boot Scenario
						USB
				1		NAND1 → SDs2 →USB

3.3 External Static Memory Boot

CPU executes External Static Memory Access without CPU Hold.

3.3.1 External Static Memory Boot Features

Supports 16/8-bit Static Memory

3.3.2 External Static Memory Boot System Configuration

Table 3-4 External Static Memory not System Configuration Setting Description

Pin Name	Function Name	Description
RST_CFG[7:0]	–	Don't care
RST_CFG8	CfgSTLATADD	Static Latched Address (user select) 0 = None 1 = Latched
RST_CFG[10:9]	–	Don't care
RST_CFG11	CfgSTBUSWidth	Static Bus Width (user select) 0 = 8-bit 1 = 16-bit
RST_CFG[14:12]	BOOTMODE[2:0]	Pull-down
RST_CFG[24:16]	–	Don't care

3.3.3 External Static Memory Boot Operation

In case of External Static Memory Boot, nSCS[0] is set to Address 0x00000000 by reset configuration and CPU can access Static Memory through MCU-S.

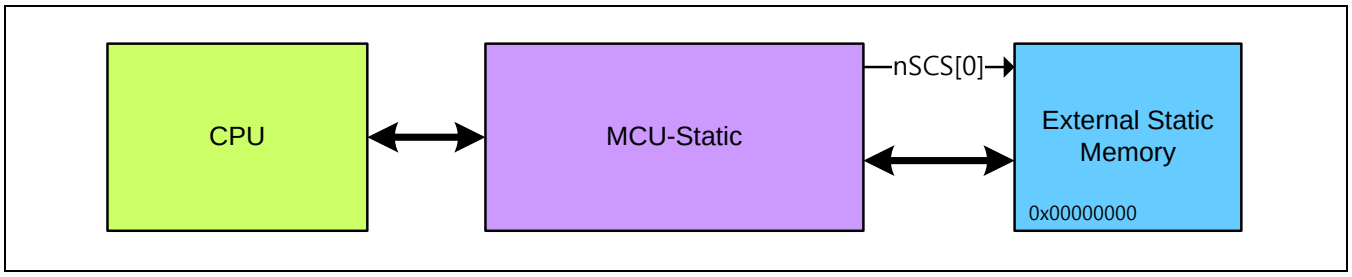


Figure 3-1 External Static Memory Boot

3.4 Internal ROM Boot

The chip has built-in 20 KB ROM. It is possible to set Internal ROM address to 0th address by setting CfgBOOTMODE of System Configuration to "3 to 7". After Reset, CPU executes instruction fetched from 0th address of the Internal ROM. Internal ROM has a code supporting various Booting methods. This ROM code executes User Bootcode by reading it through various media and loading it to specific memory. This Booting method is defined as internal ROM Booting (which is, from now on, called iROMBOOT).

iROMBOOT uses internal SRAM for storing stack or data. Therefore it is possible for the content of internal SRAM to change after iROMBOOT is executed.

3.4.1 Features

- Supports five booting modes: SPI Serial EEPROM BOOT, UART BOOT, USBBOOT, SDHCBOOT and NANDBOOT with Error Correction
- Supports CPU Exception Vector Redirection for OS systems without using MMU.
- Supports Fast Power Control: Set VDDPWRON and VDDPWRON_DDR as High.

3.4.2 System Configuration for the Internal ROM booting

iROMBOOT supports 5 Booting modes such as USBBOOT, UART BOOT, SPI Serial EEPROM BOOT, SDHCBOOT, and NANDBOOT with Error Correction. Every Booting mode supports various booting methods by referring to Reset states from SD[15:0] and SDEX[7: 0]. *Table 3-5* shows System configuration for each Booting mode.

Table 3-5 iROMBOOT System Configuration

Pins	iROMBOOT				
	UART	SPI Serial Flash	SDMMC	USB Device	NANDBOOT with Error Correction
RST_CFG[1:0]/ RST_CFG[17:16]	Don't care				NANDTYPE[1:0]
RST_CFG[2,18]					PAGESIZE
RST_CFG[3]					SELCS
RST_CFG[4,20]	DECRYPT				
RST_CFG[5 21]	I-CACHE				
RST_CFG[6]	Don't care			OTG Session Check	Don't care
RST_CFG[7]	Don't care		eMMC Boot Mode	Don't care	
RST_CFG[8]	LATADDR				
RST_CFG[9]	Don't care	ADDRWIDTH0	PARTITION	Don't care	
RST_CFG[10]		ADDRWIDTH1	eMMCBOOT		
RST_CFG[11]	BUSWIDTH = 0				
RST_CFG[14:12]	BOOTMODE = 3	BOOTMODE = 4	BOOTMODE = 5	BOOTMODE = 6	BOOTMODE = 7
RST_CFG[15]	Don't care				SEL SDEX

3.4.3 USB BOOT

iROMBOOT can load User Boot code via USB to memory and execute this code, which Booting method is called USBBOOT.

3.4.3.1 Features

- Supports Full speed or High Speed USB connection.
- Uses the USB Bulk transfer.
- Supports 64 bytes for Full speed and 512 bytes for High speed as Max packet size.

3.4.3.2 Operation

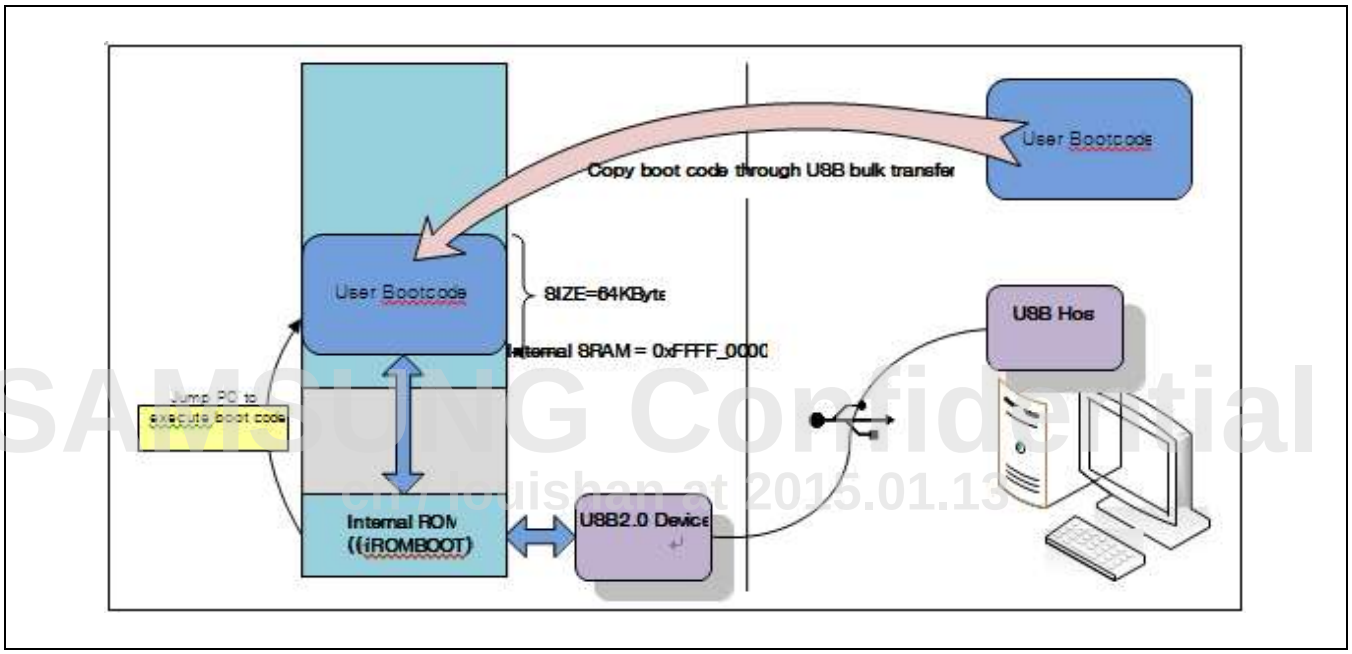


Figure 3-2 USBBOOT Operation

USB Host Program should transfer User boot code by using bulk transfer through EP2 of USB Device. The max packet size is changeable according to USB connection speed at Endpoint. In Full speed connection, USB Host Program can transfer the maximum 64 bytes as one packet and, in High speed connection, the maximum 512 bytes as one packet. USB Host Program should transfer the data packet of even size even though it can transfer the same packet as the max size or the packet smaller than the max size.

USBBOOT writes User Boot code from USB Host Program and USBBOOT executes User Boot code by changing PC to 0xFFFF0000 after it receives User Boot code size of 16 KB.

3.4.3.3 USB Descriptors

USB Host Program can get Descriptor of USBBOOT by using Get_Descriptor Request. *Table 3-6* shows Descriptor of USBBOOT. USBBOOT has one configuration, one interface, and two additional Endpoints except Control Endpoint. However, Endpoint 1 exists only for compatibility. Then USBBOOT only receives data by using Endpoint2 only.

Table 3-6 USBBOOT Description

Offset	Field	Size	USBBOOT Value		Description
			Full Speed	High Speed	
Device Descriptor					
0	bLength	1	18		Size of this descriptor in bytes
1	bDescriptorType	1	01h		DEVICE descriptor type
2	bcdUSB	2	0110h	0200h	USB spec release number in BCD
4	bDeviceClass	1	FFh		Class code
5	bDeviceSubClass	1	FFh		Subclass code
6	bDeviceProtocol	1	FFh		Protocol code
7	bMaxPacketSize0	1	64		Maximum packet size for EP0
8	idVender	2	04E8h		Vender ID
10	idProduct	2	1234h		Product ID
12	bcdDevice	2	0000h		Device release number in BCD
14	iManufacturer	1	0		Index of string descriptor describing manufacturer
15	iProduct	1	0		Index of string descriptor describing product
16	iSerialNumber	1	0		Index of string descriptor describing the device's serial number
17	bNumConfiguration	1	1		Number of possible configuration
Configuration Descriptor					
0	bLength	1	9		Size of this descriptor in bytes
1	bDescriptorType	1	02h		CONFIGURATION descriptor type
2	wTotalLength	2	32		Total length of data returned for this con figuration
4	bNumInterfaces	1	1		Number of interfaces
5	bConfigurationValue	1	1		Value to use as an argument to the Set Configuration
6	iConfiguration	1	0		Index of string descriptor describing this con figuration
7	bmAttribute	1	80h		Configuration characteristics
8	bMaxPower	1	25		Maximum power consumption
Interface Descriptor					
0	bLength	1	9		Size of this descriptor in bytes

Offset	Field	Size	USBBOOT Value		Description
			Full Speed	High Speed	
1	bDescriptorType	1	04h		INTERFACE descriptor type
2	bInterfaceNumber	1	0		Number of this interface
3	bAlternateSetting	1	0		Value used to select this alternate setting
4	bNumEndpoints	1	2		Value used to select this alternate setting for the interface
5	bInterfaceClass	1	FFh		Class code
6	bInterfaceSubClass	1	FFh		Subclass code
7	bInterfaceProtocol	1	FFh		Protocol code
8	iInterface	1	0		Index of string descriptor describing this interface
Endpoint Descriptor for EP1					
0	bLength	1	7		Size of this descriptor in bytes
1	bDescriptorType	1	05h		ENDPOINT descriptor type
2	bEndpointAddress	1	81h		The address of the endpoint
3	bmAttributes	1	02h		the endpoint's attributes
4	wMaxPacketSize	2	64	512	Maximum packet size
6	bInterval	1	0		Interval for polling endpoint for data transfers
Endpoint Descriptor for EP2					
0	bLength	1	7		Size of this descriptor in bytes
1	bDescriptorType	1	05h		ENDPOINT descriptor type
2	bEndpointAddress	1	02h		The address of the endpoint
3	bmAttributes	1	02h		the endpoint's attributes
4	wMaxPacketSize	2	64	512	Maximum packet size
6	bInterval	1	0		Interval for polling endpoint for data transfers

3.4.4 SDHCBOOT

iROMBOOT can execute User Boot code by reading it from SD memory card, MMC memory card, and eMMC and loading it to memory by using SDHC module. This method is called SDHCBOOT.

3.4.4.1 Features

- Supports SD/MMC memory card, and eMMC
- Supports High Capacity SD/MMC memory card
- Supports eMMC Booting
  - Supports Normal Booting and Alternate Booting
  - Supports only 4-bit data bus
  - Doesn't support BOOT_ACK
- Outputs 400 kHz SDCLK for Identification and 22.9 MHz SDCLK for Data Transfer

3.4.4.2 Operation

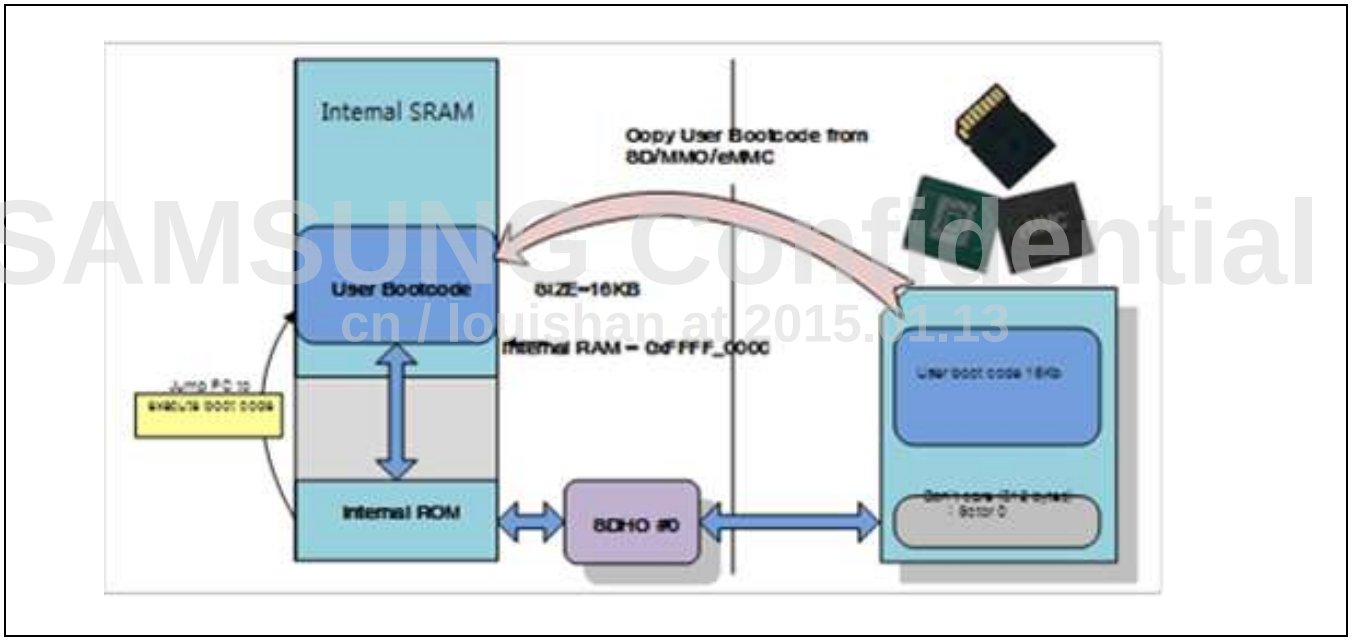


Figure 3-3 SDHCBOOT Operation

SDHCBOOT uses SDHC #0 module. The pins SDHC #0 module uses are GPIO A[29, 31] and GPIO B[1, 3, 5, 7].

SDHCBOOT provides various Booting methods according to CFG pins, in which the specification of each method is recommended to refer to *Table 3-1*.

User Boot code should be written as *Table 3-7* to Storage Device for the use of SDHCBOOT.

Table 3-7 Boot Data Format for SDHCBOOT

Sector	Name	Description
0	RESERVED	SDHCBOOT don't care data in 0^ th^ Sector. Therefore it is possible to use 0^ th^ Sector for storing MBR (Master Boot record), and to include User Boot code along with File System into one Physical Partition.
1 to 32	User Boot code	Boot code User made has 16 KB size from 2nd Sector to 32st Sector

The SDHCBOOT Booting process is as follows.

- eMMC Booting: SDHCBOOT executes eMMC Booting in case that CfgSDHCBM is 1.
  - When CfgEMMCBM is "1", Normal eMMC Booting is executed, and when CfgEMMCBM is "0", Alternate eMMC Booting is executed.
  - For eMMC Booting, SDHCBOOT always uses 4-bit data bus. Therefore BOOT_BUS_WIDTH of EXT_CSD should be set to "1." And BOOT_ACK of EXT_CSD should be set to "0" because BOOT_ACK is not available for eMMCBooting.
  - Normal SDMMC Booting is processed when no Data is transferred from Card in 1 second.
  - 512 bytes first transferred from Card are not used.
  - 512 bytes secondly transferred from Card are used.
  - User Boot code transferred from Card is loaded to internal SRAM to be executed.

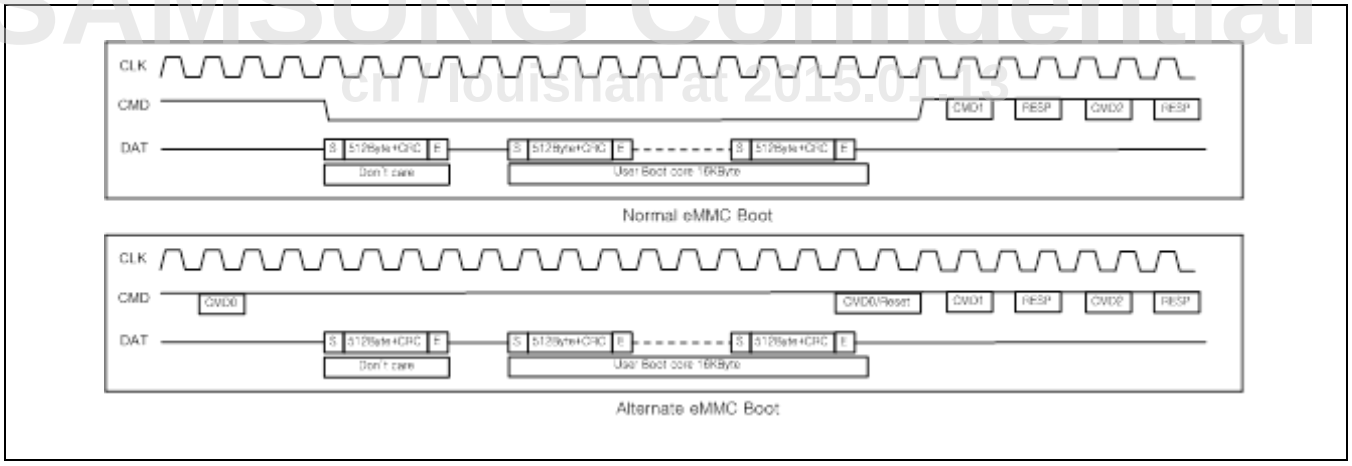


Figure 3-4 eMMC Boot

- Normal SDMMC Booting is executed when CfgSDHCBM is "0", or eMMC Booting fails.
  - Go idle state
  - SDHCBOOT identifies the type of Card and initializes.
  - The state of Card changes to Data Transfer Mode.
  - SDHCBOOT selects partition according to CfgPARTITION.
  - SDHCBOOT reads User Boot code from Sector #1, and load it to internal SRAM to be executed.

3.4.5 NANDBOOT with Error Correction

iROMBOOT provides the booting method which can correct any error in User Boot code stored in NAND Flash memory. This Booting method is described as NANDBOOT with Error Correction (which is abbreviated to NANDBOOTEC).

3.4.5.1 Features

- Supports Error Correction for up to 24-bit errors per 551 bytes: User Boot code 512 bytes + parity 39 bytes and 60-bit errors per 1129 bytes: User Boot code 1024 bytes + parity 105 bytes.
- Supports 512B, 2 KB, 4 KB, and above as the page size of the NAND flash memory.
- Supports NAND flash memories required RESET command to initialize them.
- Doesn't support the bad block management.

3.4.5.2 Operation

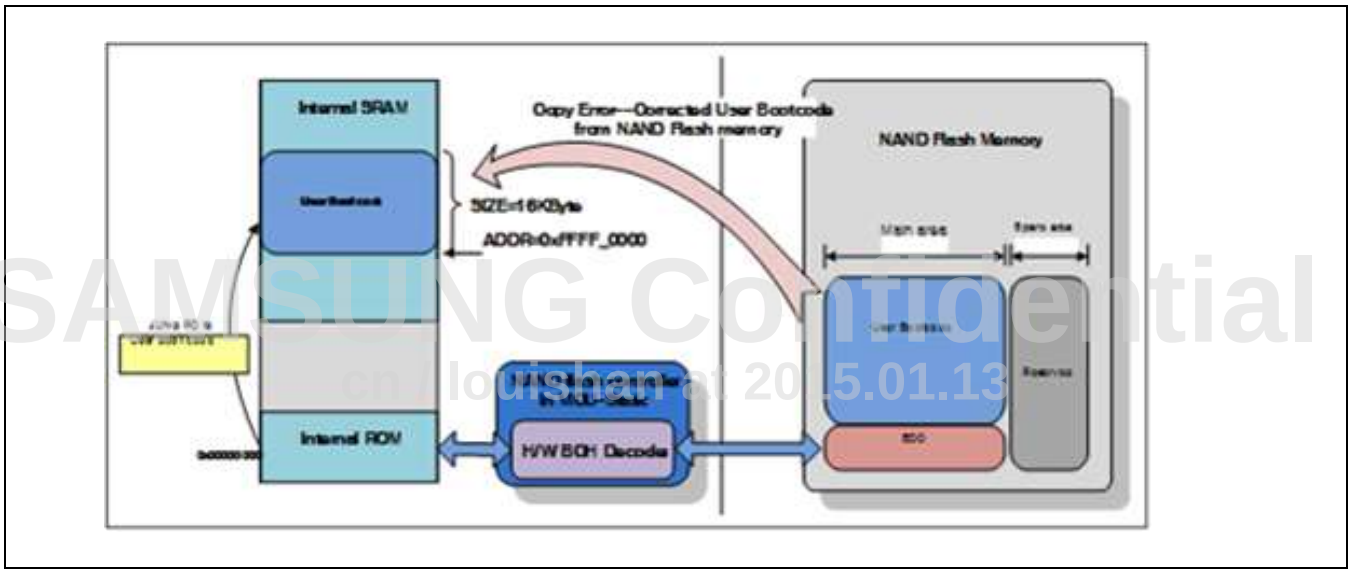


Figure 3-5 NANDBOOTEC Operation

NANDBOOTEC can correct the errors which occur in User Boot code stored in NAND flash memory. Whenever NANDBOOTEC reads User Boot code from NAND flash memory by 512 bytes or 1024 bytes, it gets to know whether any error of Data exists or not by using Error detection function of H/W BCH decoder included in MCU-S. In case of any error in Data, the maximum 24 or 60 errors can be corrected through H/W Error Correction. If Error Correction fails, Booting with USB Boot mode.

3.4.5.3 How to Store User Boot code into the NAND Flash Memory

Table 3-8 shows the written form of User Boot code into NAND flash memory. NANDBOOTEC uses the main memory of NAND flash memory and doesn't use the spared area of it.

Table 3-8 NAND Flash Memory Format for NANDBOOTEC

Sector	Data	Page Size	ECC #n	64 bytes × 8 = 512 bytes	
		512B	–	LSB (312-bit)	MSB (200-bit)
0	ECC #0	page #0	LSB 39 bytes	Reserved	
1	Bin #0	page #1	–	Parity for sector # (n × 8 + 1)	Reserved
2	Bin #1	page #2	–	Parity for sector # (n × 8 + 2)	Reserved
3	Bin #2	page #3	–	Parity for sector # (n × 8 + 3)	Reserved
4	Bin #3	page #4	–	Parity for sector # (n × 8 + 4)	Reserved
5	Bin #4	page #5	–	Parity for sector # (n × 8 + 5)	Reserved
6	Bin #5	page #6	–	Parity for sector # (n × 8 + 6)	Reserved
7	Bin #6	page #7	MSB 39 bytes	Parity for sector # (n × 8 + 7)	Reserved
8	ECC #1	page #8	–	–	–
9	Bin #7	page #9	–	–	–
10	Bin #8	page #10	–	–	–
11	Bin #9	page #11	–	–	–
12	Bin #10	page #12	–	–	–
13	Bin #11	page #13	–	–	–
14	Bin #12	page #14	–	–	–
15	Bin #13	page #15	–	–	–
16	ECC #1	page #16	–	–	–
17	Bin #14	page #17	–	–	–
18	Bin #15	page #18	–	–	–
19	Bin #16	page #19	–	–	–
20	Bin #17	page #20	–	–	–
21	Bin #18	page #21	–	–	–
22	Bin #19	page #22	–	–	–
23	Bin #20	page #23	–	–	–
24	ECC #2	page #24	–	–	–
25	Bin #21	page #25	–	–	–
26	Bin #22	page #26	–	–	–
27	Bin #23	page #27	–	–	–
28	Bin #24	page #28	–	–	–
29	Bin #25	page #29	–	–	–

Sector	Data	Page Size	ECC #n	64 bytes × 8 = 512 bytes	
		512B	–	LSB (312-bit)	MSB (200-bit)
30	Bin #26	page #30	–	–	–
31	Bin #27	page #31	–	–	–
32	ECC #3	page #32	–	–	–
33	Bin #28	page #33	–	–	–
34	Bin #29	Page #34	–	–	–
34	Bin #30	page #35	–	–	–
35	Bin #31	page # 36	–	–	–

Sector	Data	Page Size			ECC #n	128 bytes × 8 = 1024 bytes	
		2 KB	4 KB	8K	–	LSB (840-bit)	MSB (184-bit)
0	ECC #0	page #0	page #0	page #0	LSB 105 bytes	Reserved	
1	Bin #0	page #1			–	Parity for sector # (n × 8 + 1)	Reserved
2	Bin #1	page #2	page #1		–	Parity for sector # (n × 8 + 2)	Reserved
3	Bin #2	page #3			Parity for sector # (n × 8 + 3)	Reserved	–
4	Bin #3	page #4	page #2		–	Parity for sector # (n × 8 + 4)	Reserved
5	Bin #4	page #5		page #1	–	Parity for sector # (n × 8 + 5)	Reserved
6	Bin #5	page #6	page #3		–	Parity for sector # (n × 8 + 6)	Reserved
7	Bin #6	page #7			Parity for sector # (n × 8 + 7)	Reserved	–
8	ECC #1	page #8	page #4	page #2	–	–	–
9	Bin #7	page #9			–	–	–
10	Bin #8	page #10	page #5		–	–	–
11	Bin #9	page #11			–	–	–
12	Bin #10	page #12	page #6	page #3	–	–	–
13	Bin #11	page #13			–	–	–
14	Bin #12	page #14	page #7		–	–	–
15	Bin #13	page #15			–	–	–
16	ECC #1	page #16	page #8	page #4	–	–	–
17	Bin #14	page #17			–	–	–
18	Bin #15	page #18	page #9		–	–	–
–	–	–			–	–	–

3.4.6 Additional Information

3.4.6.1 ALIVE POWER Control

iROMBOOT changes VDDPWRON and VDDPWRON_DDR pins to High state after Reset in order to supports the fast response to nVDDPWRTOGGLE button. *Table 3-9* shows ALIVE module states after iROMBOOT Execution.

Table 3-9 ALIVE Power Control

Function	State	Description
VDDPWRON	High	Enable Core Power
VDDPWRON_DDR	High	Enable DDR Memory Power
nPADHOLD[2:0]	High	Disable PAD Retention
nPADHOLDEnb[2:0]	Low	

3.4.6.2 Exception Vector Redirection

Exception Handler of ARM CPU should exist from 0th address by 4 byte one after the other. User generally places the routine jumping to User's Exception Handler to the Exception Handler existing from 0th address. However, in case of iROMBOOT, User's Exception Handler is impossible to set at 0th address because ROM exists at 0thaddress. CPU Exception can be processed by mapping the arbitrary memory to 0th address when MMU is being used. However iROMBOOT provides the function redirecting Exception Handler for the System not using MMU.

iROMBOOT uses 32 bytes from the lowest address of internal SRAM as User Exception Vector Table. When Exception occurs, ROM Exception Handler in iROMBOOT lets PC jump to the address of User Exception Handler taken from User Exception Vector Table. Therefore Exception can be processed even at Physical address system by User's setting the address of User Exception Handler to User Exception Vector Table present in internal SRAM and that is equal to High Vector Address.

#define BASEADDR_SRAM 0xFFFF0000

Example 3-1 iROMBOOT Exception Handlers

```
//;=====================================================================
//; Vectors
//;=====================================================================
.global Vectors
Vectors:
                LDR             pc, ResetV              //; 00 - Reset
                LDR             pc, UndefV              //; 04 - Undefined instructions
                LDR             pc, SWIV                //; 08 - SWI instructions
                LDR             pc, PAbortV             //; 0C - Instruction fetch aborts
                LDR             pc, DAbortV             //; 10 - Data access aborts
                LDR             pc, UnusedV             //; 14 - Reserved (was address exception)
                LDR             pc, IRQV                //; 18 - IRQ interrupts
                LDR             pc, FIQV                //; 1C - FIQ interrupts

ResetV:
                .word           Reset_Handler
UndefV:
```

```
                .word       (BASEADDR_SRAM + 0x04) //; 04 - undef
SWIV:
                .word       (BASEADDR_SRAM + 0x08) //; 08 - software interrupt
PAbortV:
                .word       (BASEADDR_SRAM + 0x0C) //; 0C - prefetch abort
DAbortV:
                .word       (BASEADDR_SRAM + 0x10) //; 10 - data abort
UnusedV:
                .word       0                                   //; 14 - will reset if called...
IRQV:
                .word       (BASEADDR_SRAM + 0x18) //; 18 - IRQ
FIQV:
                .word       (BASEADDR_SRAM + 0x1C) //; 1C - FIQ

//;=====================================================================
//; Imports
//;=====================================================================

.global iROMBOOT

//;=====================================================================
//; Reset Handler - Generic initialization, run by all CPUs
//;=====================================================================

Reset_Handler:
```


3.4.6.3 Parity Generation for Error Correction

NANDBOOTEC can correct the maximum 24 errors in User Boot code 512 bytes and Parity 39 bytes or maximum 60 errors in User Boot code 1024 bytes and Parity 105 bytes. Therefore, by generating Parity 39 bytes at every 512 bytes of User Boot code, User should write the parity information to ECC Sector. For NANDBOOTEC, the number of Parity information varies according to the size of User Boot code. It is recommended to refer to the description of NANDBOOTEC about the site in which Parity information should be located.

3.4.6.4 CRC32 Error Check

UART and SPI Boot check 16368 (16384 - 16) bytes with CRC32 and if adding CRC32 fcs data to last of transfer of payload then CRC32 fcs will checking will success.

CRC32 fcs generator function.

```
#define POLY 0x04C11DB7L

unsigned int get_fcs(unsigned int fcs, unsigned char data)
{
        register int i;
        fcs ^= (unsigned int)data;
        for(i=0; i<8; i++)
        {
                if(fcs & 0x01)
                        fcs ^= POLY;
                fcs >>= 1;
        }
        return fcs;
}
```

```
#define POLY 0x04C11DB7L
unsigned int get_fcs(unsigned int fcs, unsigned char data)
{
        register int i;
        fcs ^= (unsigned int)data;
        for(i=0; i<8; i++)
        {
                if(fcs & 0x01)
                        fcs ^= POLY;
                fcs >>= 1;
        }
        return fcs;
}
```


3.4.6.5 Data Decryption with AES128 ECB Mode to Use Hidden Key

All boot mode data will decrypted with AES128 ECB mode to use hidden key by option.

Boot mode sd[4], sdex[4] can select weather data will decrypt or not decrypt.

4 System Control

4.1 Overview

The clock of the S5P4418 is roughly divided into FCLK, HCLK, MCLK, BCLK and PCLK are used for the ARM CPU core, AXI bus peripherals and APB bus peripherals, respectively. In addition, BCLK is the clock for the S5P4418 system bus. MCLK is the clock for SDRAM memory. The 2-PLL of the S5P4418 is called PLL0 and PLL1, respectively. The 2-PLL and EXTCLK are used to generate the above clocks (i.e. FCLK, HCLK, PCLK, BCLK, MCLK). All PLLs are designed to operate with an X-TAL input of 24MHz.

4.2 Features

- Embedded 4-PLL operating independently
- Output Frequency Range
  - PLL0: 40M to 2.5 GHz (non-dithered PLL)
  - PLL1: 40M to 2.5 GHz (non-dithered PLL)
  - PLL2: 35M to 2.2 GHz (dithered PLL)
  - PLL3: 35M to 2.2 GHz (dithered PLL)
- Frequency is changed by Programmable Divider (PDIV, MDIV, SDIV)
- Clock generation for all blocks in the chip
- The PLLs can be switched into Power Down mode by using the program.
- 32.768 kHz supported for Power Management
- Various Power Down Modes
- IDLE mode and STOP mode
- Various Wake Up sources

4.3 Block Diagram

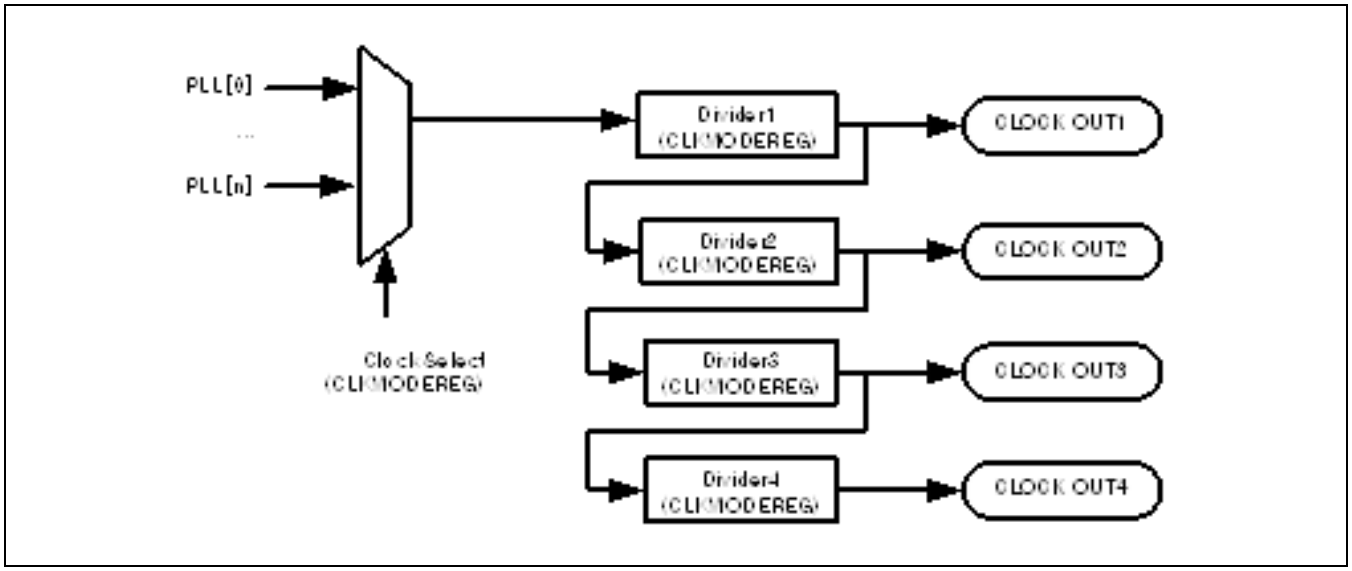


Figure 4-1 Block Diagram

The above figure shows a diagram for the clock manager in the S5P4418. As shown in the above figure, the S5P4418 has four PLLs. The S5P4418 receives the output of PLLs and generates all system clocks, the memory clock and the CPU clock with the output frequency selected among many PLLs.

4.4 Functional Description

4.4.1 PLL (Phase Locked Loop)

4.4.1.1 PMS Value

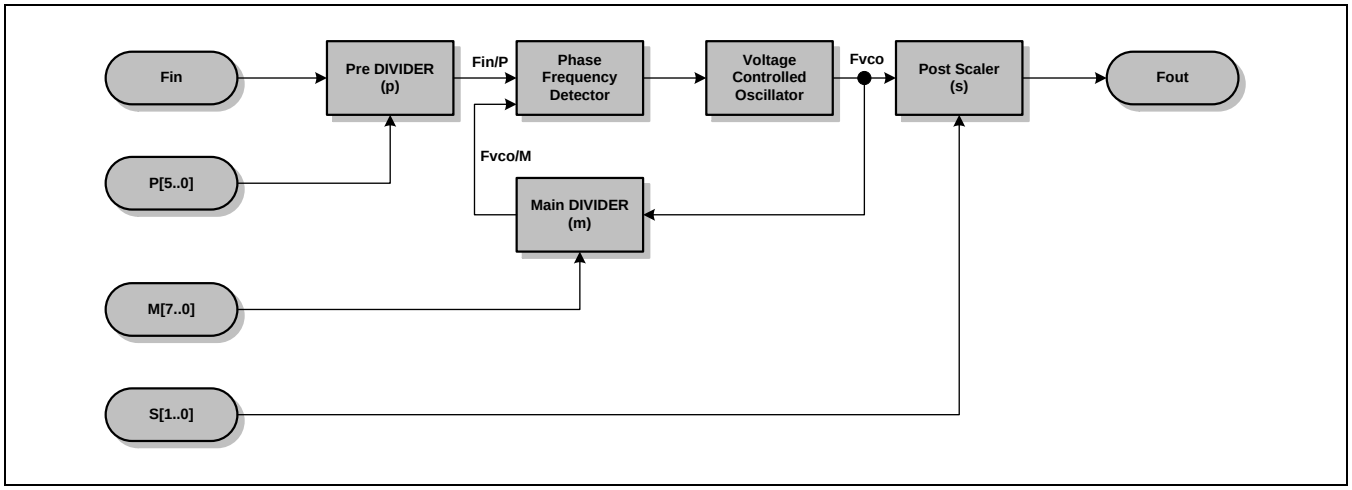


Figure 4-2 Block Diagram of PLL

For the aspect of PLL structure, *Figure 4-2* shows the block diagram for one PLL. Fin and Fout indicate input frequency and output frequency respectively. The S5P4418 has PLLs and can generate various programmable clocks by using each PLL.

If the Pre Divider receives a Fin input of 24 MHz, it divides the Fin with "P". After that, Phase Frequency Detector (PFD) compares the difference between Fin/P (Reference Clock) and Fvco/M (Feedback Clock). The amplitude of the voltage varies depending on the difference of the values compared between Fin/P and Fvco/M. If the reference clock is faster feed back block, the Voltage Controlled Oscillator (VCO) increases in proportion to the difference. If the reference clock is delayed than the feed clock, VCO is decreased, and it generates an Fvco clock. That is because VCO is a voltage value and plays the role of controlling the clock speed to be faster or slower. At this point, the voltage value is determined by the difference of the values compared between the reference clock and the feedback clock. If the Fvco is not a desired clock, the feedback is recreated through the Main Divider and compared in PFD. These steps are repeated until the reference clock and the feedback clock become equal. If proper FVCO is out, the final Fout clock is created as the divide value(s) of a Post Scaler. Finally, the desired clock frequency is determined by the p, m and s values.

As described above, Fout can be variously set by Fin and p/m/s values and the equation to specify p/m/s values is as follows: (Note that all PLL0/1/2/3 indicate Fout. Equation may vary for each case.)

- PLL x = (m x Fin)/(p x 2s)
- (x = 0,1,2,3, m = MDIV, p = PDIV, s = SDIV = 0, 1, 2, 3)
- The range of the MDIV and PDIV values for PLL x are as follows:
- Range of MDIV Value: 64 ≤ MDIV ≤ 1023
- Range of PDIV Value: 1 ≤ PDIV ≤ 63

The PDIV and the MDIV values should be selected by considering the VCO value and S5P4418's stable operation. The S5P4418 has PLLs and each PLL has different default values and operation ranges.

The basic frequencies for the S5P4418 are listed in the table below:

Table 4-1 Initial PDIV/MDIV/SDIV Value

PLL	INITIAL FREQUENCY	RECOMMENDED FREQUENCY (Fvco)	RECOMMENDED FREQUENCY (Fout)	INITIAL PDIV/MDIV/SDIV VALUE		
				PDIV	MDIV	SDIV
PLL0	550.000000 MHz	1250 to 2500 MHz	40 to 2500 MHz	6	550	2
PLL1	147.456 MHz	1250 to 2500 MHz	40 to 2500 MHz	6	590	4
PLL2	96 MHz	40 to 2200 MHz	1100 to 2200 MHZ	3	192	4
PLL3	125 MHz	40 to 2200 MHz	1100 to 2200 MHz	3	250	4

For all blocks except for CPU, the operation status (Run/Stop) of the memory controller should be checked before changing the PLL output frequency. In addition, the PLL change bit (PWRMODE.CHGPLL) should be set as "1" after PLL change (PLLSETREG0, PLLSETREG1).

Setting guide of PMSK

- p, m, s and k are decimal values of P[5:0], M[8:0], S[2:0] and K[15:0], respectively.
  - p = P[5:0] , m = M[8:0] , s = S[2:0], k = K[15:0]
- FFVCO and FFOUT are calculated by the following equation.
  - FFVCO = ((m+k/65536) × FFIN)/p
  - FFOUT = ((m+k/65536) × FFIN)/(p × 2s)
- While range of registers P[5:0], M[8:0] and S[2:0] are unsigned integers, K[15:0] is a two's complement integer.
  - 6'b00 0001 ≤ P[5:0] ≤ 6'b11 1111 and 2MHz ≤ FFREF(FFIN/p) ≤ 30 MHz
  - 9'b0 0100 0000 ≤ M[8:0] ≤ 9'b1 1111 1111
  - 3'b000 ≤ S[2:0] ≤ 3'b101
  - 16'b1000 0000 0000 0000 ≤ K[15:0] ≤ 16'b0111 1111 1111 1111
- Setting P[5:0] or M[8:0] to all zeros is strictly prohibited while RESETB is logic high. (6'b00 0000/9'b0 0000 0000)
- The division ratio of scaler is controlled by S[2:0] as summarized in *Table 4-2*.
- Setting S[2:0] to the values in the gray rows in *Table 4-2* is strictly prohibited.

Table 4-2 Division Ratio of Scaler

S[2:0]	Division Ratio
000	20 = 1
001	21 = 2
010	22 = 4
011	23 = 8
100	24 = 16
101	25 = 32

S[2:0]	Division Ratio
110	Prohibited
111	Prohibited

4.4.1.2 Setting Guide of SSCG_EN, SEL_PF, MFR and MRR

- When SSCG_EN is set to logic high, the spread spectrum mode is enabled.
- sel_pf, mfr and mrr are decimal values of SEL_PF[1:0], MFR[7:0] and MRR[5:0], respectively.
  - sel_pf = SEL_PF[1:0], mfr = MFR[7:0], mrr = MRR[5:0]
- Modulation frequency, MF, is determined by the following equation.
  - MF = FFIN/p/mfr/25[Hz]
- Modulation rate (pk-pk), MR, is determined by the following equation.
  - MR = mfr × mrr/m/26 × 100 [%]
- Modulation mode is determined by sel_pf.
  - 00 = down spread
    01 = up spread
    1x = center spread
- Range of registers.
  - 8'b0000 0000 ≤ MFR[7:0] ≤ 8'b1111 1111
  - 6'b00 0001 ≤ MRR[5:0] ≤ 6'b11 1111
  - 0 ≤ mrr × mfr ≤ 512
  - 2'b00 ≤ SEL_PF[1:0] ≤ 2'b10

4.4.1.3 PDIV/MDIV/SDIV Values for PLL0, PLL1

Table 4-3 PDIV/MDIV/SDIV Value for PLL0

Input Frequency	Output Frequency (MHz)	PDIV/MDIV/SDIV Value			Remark
		PDIV	MDIV	SDIV	
24 MHz	2000.000000	6	500	0	Maximum Available Frequency
24 MHz	1900.000000	6	475	0	–
24 MHz	1800.000000	4	300	0	–
24 MHz	1700.000000	6	425	0	–
24 MHz	1600.000000	6	400	0	–
24 MHz	1500.000000	4	250	0	–
24 MHz	1400.000000	6	350	0	–
24 MHz	1300.000000	6	325	0	–
24 MHz	1200.000000	4	400	1	–
24 MHz	1100.000000	6	550	1	–
24 MHz	1000.000000	6	500	1	–
24 MHz	900.000000	4	300	1	–
24 MHz	800.000000	6	400	1	Maximum Available Frequency
24 MHz	780.000000	4	260	1	–
24 MHz	760.000000	6	380	1	–
24 MHz	740.000000	6	370	1	–
24 MHz	720.000000	4	240	1	–
24 MHz	562.000000	6	562	2	–
24 MHz	533.000000	6	533	2	–
24 MHz	490.000000	6	490	2	–
24 MHz	470.000000	6	470	2	–
24 MHz	460.000000	6	460	2	–
24 MHz	450.000000	4	300	2	–
24 MHz	440.000000	6	440	2	–
24 MHz	430.000000	6	430	2	–
24 MHz	420.000000	4	280	2	–
24 MHz	410.000000	6	410	2	–
24 MHz	400.000000	6	400	2	–
24 MHz	399.000000	4	266	2	–
24 MHz	390.000000	4	260	2	–
24 MHz	384.000000	4	256	2	–
24 MHz	350.000000	6	350	2	–

Input Frequency	Output Frequency (MHz)	PDIV/MDIV/SDIV Value			Remark
		PDIV	MDIV	SDIV	
24 MHz	330.000000	4	220	2	–
24 MHz	300.000000	4	400	3	–
24 MHz	266.000000	6	532	3	–
24 MHz	250.000000	6	500	3	–
24 MHz	220.000000	6	440	3	–
24 MHz	200.000000	6	400	3	–
24 MHz	166.000000	6	332	3	–
24 MHz	147.45600	6	590	4	147.5 MHz (0.03% error
24 MHz	133.000000	6	532	4	–
24 MHz	125.000000	6	500	4	–
24 MHz	100.000000	6	400	4	–
24 MHz	96.000000	4	256	4	–
24 MHz	48.000000	3	96	4	–

4.4.1.4 PDIV/MDIV/SDIV Values for PLL2, PLL3

Table 4-4 PDIV/MDIV/SDIV Value for PLL1

Input Frequency	Output Frequency (MHz)	PDIV/MDIV/SDIV Value			Remark
		PDIV	MDIV	SDIV	
24 MHz	2000.000000	3	250	0	Maximum Available Frequency
24 MHz	1900.000000	3	238	0	–
24 MHz	1800.000000	3	225	0	–
24 MHz	1700.000000	3	213	0	–
24 MHz	1600.000000	3	200	0	–
24 MHz	1500.000000	4	250	0	–
24 MHz	1400.000000	3	175	0	–
24 MHz	1300.000000	3	163	0	–
24 MHz	1200.000000	3	150	0	–
24 MHz	1100.000000	3	275	1	–
24 MHz	1000.000000	3	250	1	–
24 MHz	900.000000	3	225	1	–
24 MHz	800.000000	3	200	1	Maximum Available Frequency
24 MHz	780.000000	3	195	1	–
24 MHz	760.000000	3	190	1	–

Input Frequency	Output Frequency (MHz)	PDIV/MDIV/SDIV Value			Remark
		PDIV	MDIV	SDIV	
24 MHz	740.000000	3	185	1	–
24 MHz	720.000000	3	180	1	–
24 MHz	562.000000	3	141	1	–
24 MHz	533.000000	3	267	2	–
24 MHz	490.000000	3	245	2	–
24 MHz	470.000000	3	235	2	–
24 MHz	460.000000	3	230	2	–
24 MHz	450.000000	3	225	2	–
24 MHz	440.000000	3	220	2	–
24 MHz	430.000000	3	215	2	–
24 MHz	420.000000	3	210	2	–
24 MHz	410.000000	3	205	2	–
24 MHz	400.000000	3	200	2	–
24 MHz	399.000000	4	266	2	–
24 MHz	390.000000	3	195	2	–
24 MHz	384.000000	3	192	2	–
24 MHz	350.000000	3	175	2	–
24 MHz	330.000000	3	165	2	–
24 MHz	300.000000	3	150	2	–
24 MHz	266.000000	3	266	3	–
24 MHz	250.000000	3	250	3	–
24 MHz	220.000000	3	220	3	–
24 MHz	200.000000	3	200	3	–
24 MHz	166.000000	3	166	3	–
24 MHz	147.45600	3	147	3	–
24 MHz	133.000000	3	266	4	–
24 MHz	125.000000	3	250	4	–
24 MHz	100.000000	3	200	4	–
24 MHz	96.000000	3	192	4	–
24 MHz	48.000000	3	96	4	–

4.4.1.5 PLL Power Down

The S5P4418 supports PLL Power Down mode to minimize power consumption. For example, if all system clocks are generated with PLL0 and PLL1 does not need to be used. Therefore, power does not need to be supplied to the PLL1. In such a case, the S5P4418 switches PLL1 into power down mode to reduce the power consumption. However, PLL0 cannot enter to the power down mode. PLL0 power down can be achieved by writing "1" to the CLKMODEREG0.PLLPWDN1.

4.4.2 Change PLL Value

When CPU want to change the PLL divider value, The PLL Change Bit (PWRMODE.CHGPLL bit) must be set to 1 after setting the PLL Setting Reset (PLLSETREG0, PLLSETREG1) to appropriate value.

Power management and Clock Controller blocks up the clock supplied to internal controllers because PLLs are unstable when PLL divider value is changed. After locking time, these blocks supply clock. CPU must check whether the blocks run or stop such as STOP mode.

4.4.3 Clock Generator

4.4.3.1 Clocks Summary

The 5 clocks created in the S5P4418 and the maximum frequencies for each clock are listed in the table below. The minimum frequency is not limited within the clock frequency limit creatable in PLL.

Table 4-5 S5P4418 Clock Summary

Clock Name	Min Frequency	Max Frequency (MHz)	Description
FCLKCPU0	–	800/1000 (1)	CPU CLOCK
HCLKCPU0	–	250	CPU BUS CLOCK
MDCLK	–	800	Memory DLL clock.
MCLK	(NOTE)	800	Memory clock. NOTE: Minimum frequency of MCLK is determined by SDRAM specification.
MBCLK	–	400	Memory BUS CLOCK(MCU CLOCK)
MPCLK	–	200	Memory Peripheral clock.
BCLK	–	333 MHz	SYSTEM BUS CLOCK (CORE CLOCK) CORE blocks operates on the basis of BCLK. (MPEG, DMA, etc…)
PCLK	–	166 MHz	PERIPHERAL BUS CLOCK CPU accesses a block register via I/O with PCLK.
GR3DBCLK	–	333	GPU clock
GR3DPCLK	–	–	Not used.
MPEGBCLK	–	300	MFC clock. (BUS and CODEC)
MPEGPCLK	–	150	MFC clock (Peripheral clock)

NOTE: In, note that the size of PCLK should be the half size of the BCLK when the maximum/minimum frequency values are specified.

1. CPU frequency is 800 MHz at 1.0 V and 1000 MHz at 1.1 V

4.4.3.2 CPU0 Clock

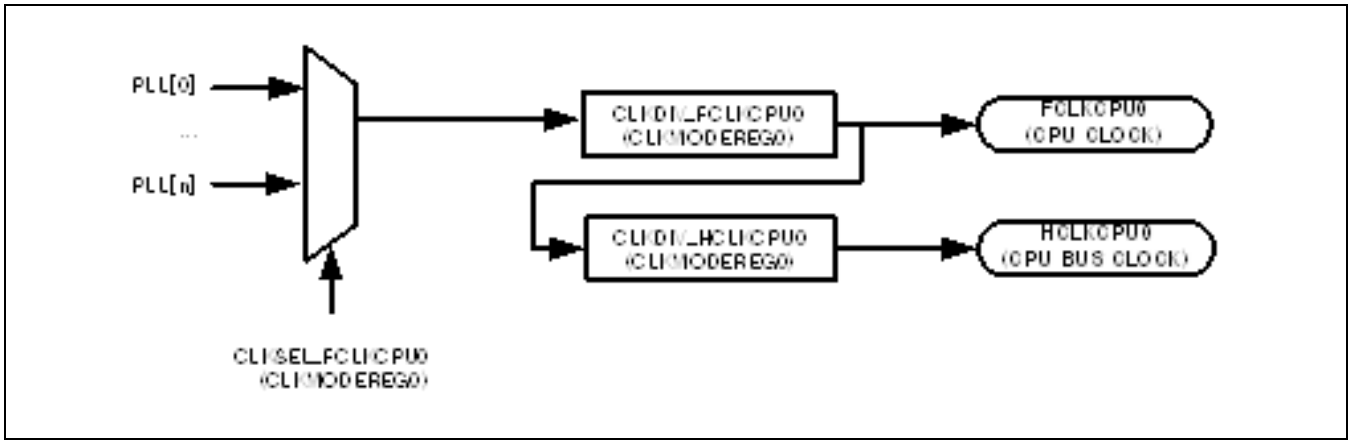


Figure 4-3 CPU Clock

Figure 4-3 shows a block diagram that creates the clock supplied to FCLKCPU0, which is the main CPU of the S5P4418.CLKMODEREG0 selects a desired PLL output from among PLLs. With the clock created from the selected PLL, the CLKDIV_FCLKCPU0 register and CLKDIV_HCLKCPU0 generates FCLKCPU0 to be supplied to the core block of CPU and HCLKCPU to be supplied to the AXI bus clock. Be careful not to set HCLKCPU over maximum speed. The frequency of FCLKCPU and HCLKCPU cannot be the same.

Any PLL can be used to generate the CPU clock, but it is recommended to use the PLL0

Recommended clock frequency as follows:

Table 4-6 Recommended Clock Frequency for CPU

CPU Operation Voltage	FCLKCPU0 (MHz)	HCLKC'P'U0 (MHz)
1.0 V	800	200
1.1 V	1000	250

4.4.3.3 System Bus Clock (Core clock)

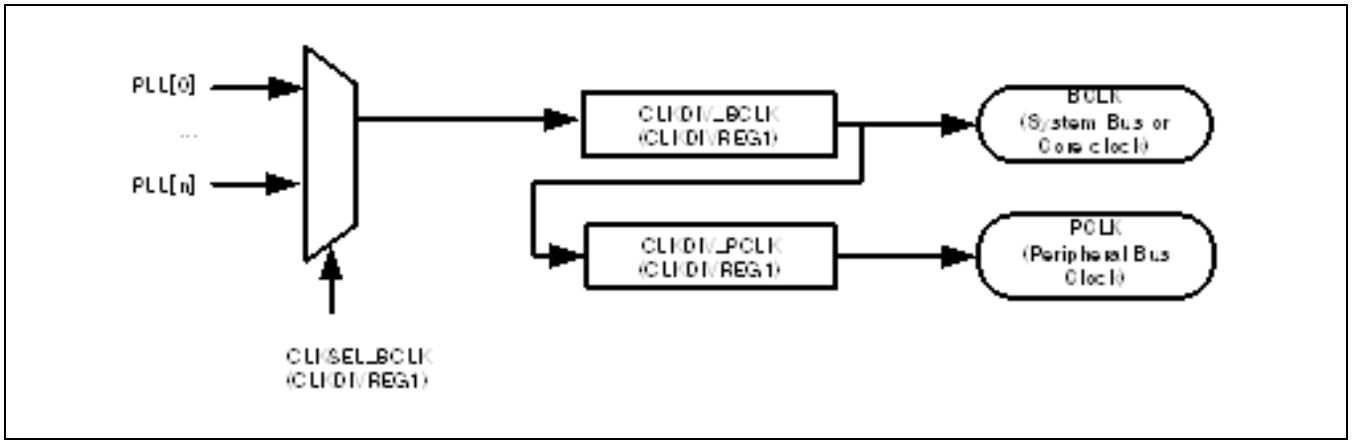


Figure 4-4 System BUS Clock

System bus clock (BCLK) is used as Core clock. The system bus clock is called [BCLK] and the half clock of BCLK is called [PCLK]. BCLK is the clock for all SOC Core operations. PCLK is used when the CPU accesses each block register via I/O. Therefore, PCLK should not be applied to the blocks not being used. Every block has PCLK enable/disable Register. The blocks that PCLK is applied to have (refer to each Section). These registers decide if PCLK is applied to a block only when the CPU accesses the corresponding block register or when it is always applied.

Clock frequency ratio should be as follows.

- BCLK:PCLK = 2:1

Recommended clock frequency as follows:

Table 4-7 Recommended clock Frequency for System BUS

Mode	BCLK (MHz)	PCLK (MHz)
max operation.	333	166

4.4.3.4 Memory Bus Clock (MCU Clock)

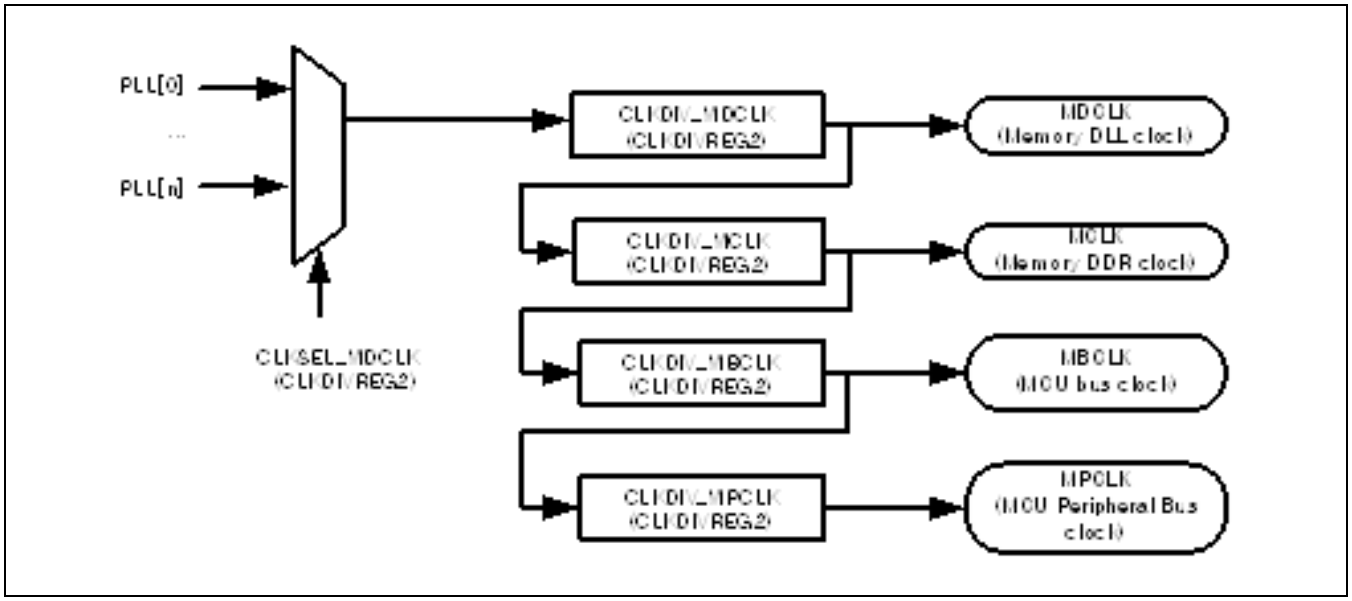


Figure 4-5 Memory BUS Clock

Memory bus clock (MCLK) is used as SDRAM, MCU Core clock. MDCLK is the clock for DLL of Memory Control Unit (MCU). MCLK is the DDR interface clock. MBCLK is bus clock of MCU. MPCLK is peripheral bus clock of MCU. The MCLK frequency should be the double that of the MBCLK frequency. (BCLK to MCLK is a 1:2 ratio)

Recommended clock frequency ratio is as follows.

- MDCLK:MCLK:MBCLK:MPCLK = 4:4:2:1

Recommended clock frequency as follows:

Table 4-8 Recommended clock Frequency for Memory BUS

Mode	MDCLK (MHz)	MCLK (MHz)	MBCLK (MHz)	MPCLK (MHz)
Fast	800 (NOTE)	800	400	200
Slow	800	200	100	50

NOTE: MDCLK should be divided by 2, i.e. CLKDIV_MDCLK should be 1.

4.4.3.5 GPU (Graphic Processing Unit) clock

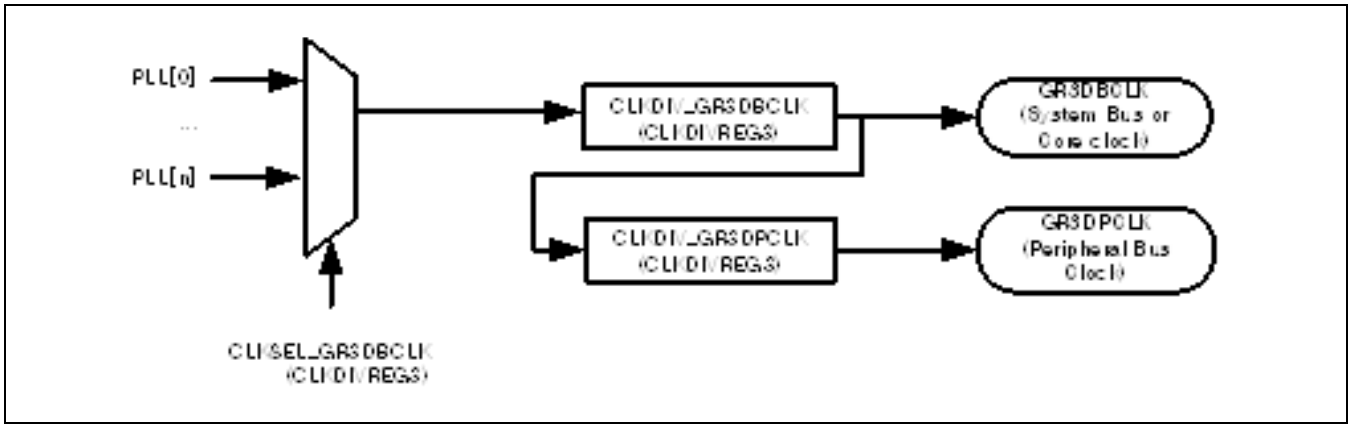


Figure 4-6 System BUS Clock

GPU clock (GR3DBCLK) is used as GPU core clock. GR3DPCLK is not used (reserved).

Recommended clock frequency as follows:

Table 4-9 Recommended clock Frequency for GPU

Mode	GR3DBCLK (MHz)	GR3DPCLK (MHz)
Max operation.	333	166 (not used)

4.4.3.6 MFC (Multi-Function Codec) clock

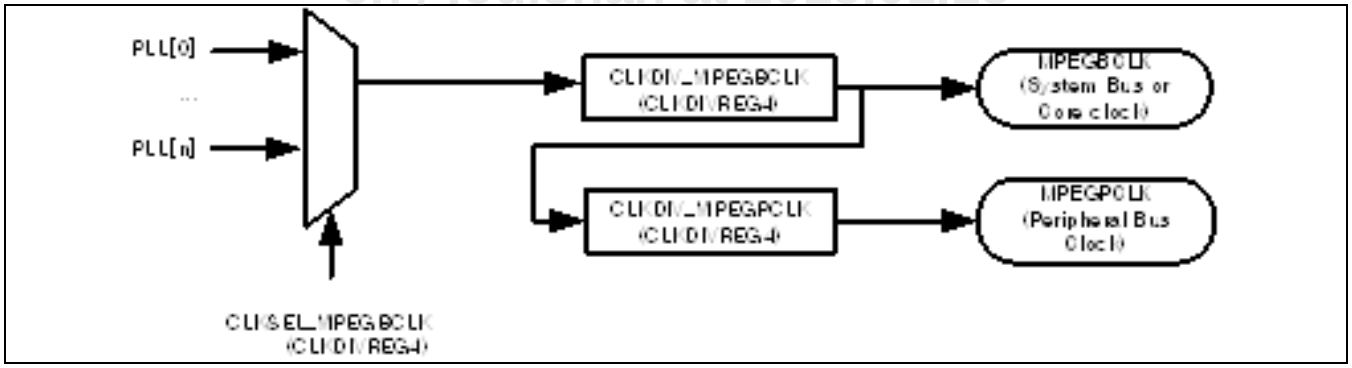


Figure 4-7 System BUS Clock

MFC clock (MPEGBCLK) is used as Multi-function codec clock. MPEGPCLK is used peripheral bus clock for MFC unit.

Recommended clock frequency as follows:

Table 4-10 Recommended clock Frequency for MFC

Mode	MPEGBCLK (MHz)	MPEGPCLK (MHz)
Max operation.	300	150

4.5 Power Manager

4.5.1 Power Manager Overview

The power manager of the S5P4418 provides the following functions to operate the system stably and reduce the power consumption.

- Power Up Sequence
- Reset Generation
- Power Management
- Change PLL Value

The key functions of the power manager are to control the Power up Sequence to make the S5P4418 stable after the power is supplied to the system and to manage the power effectively. Apart from this, it controls the reset configuration in initial operation.

In addition, this block generates various reset signals, such as External Reset Output (nRSTOUT), AliveGPIO Reset and Soft Reset.

- The S5P4418 provides various Power Down modes to reduce the system power consumption. The three Power modes provided by the S5P4418 are as follows: Normal Mode
  - IDLE Mode
  - STOP Mode
  - SLEEP Mode (See the "ALIVE" Section for SLEEP Mode)

4.5.2 Power Down Mode Operation

Figure 4-8 shows the state diagram for the Power Management Block. The figure indicates the entry conditions for each Power Down mode and all Wake Up conditions.

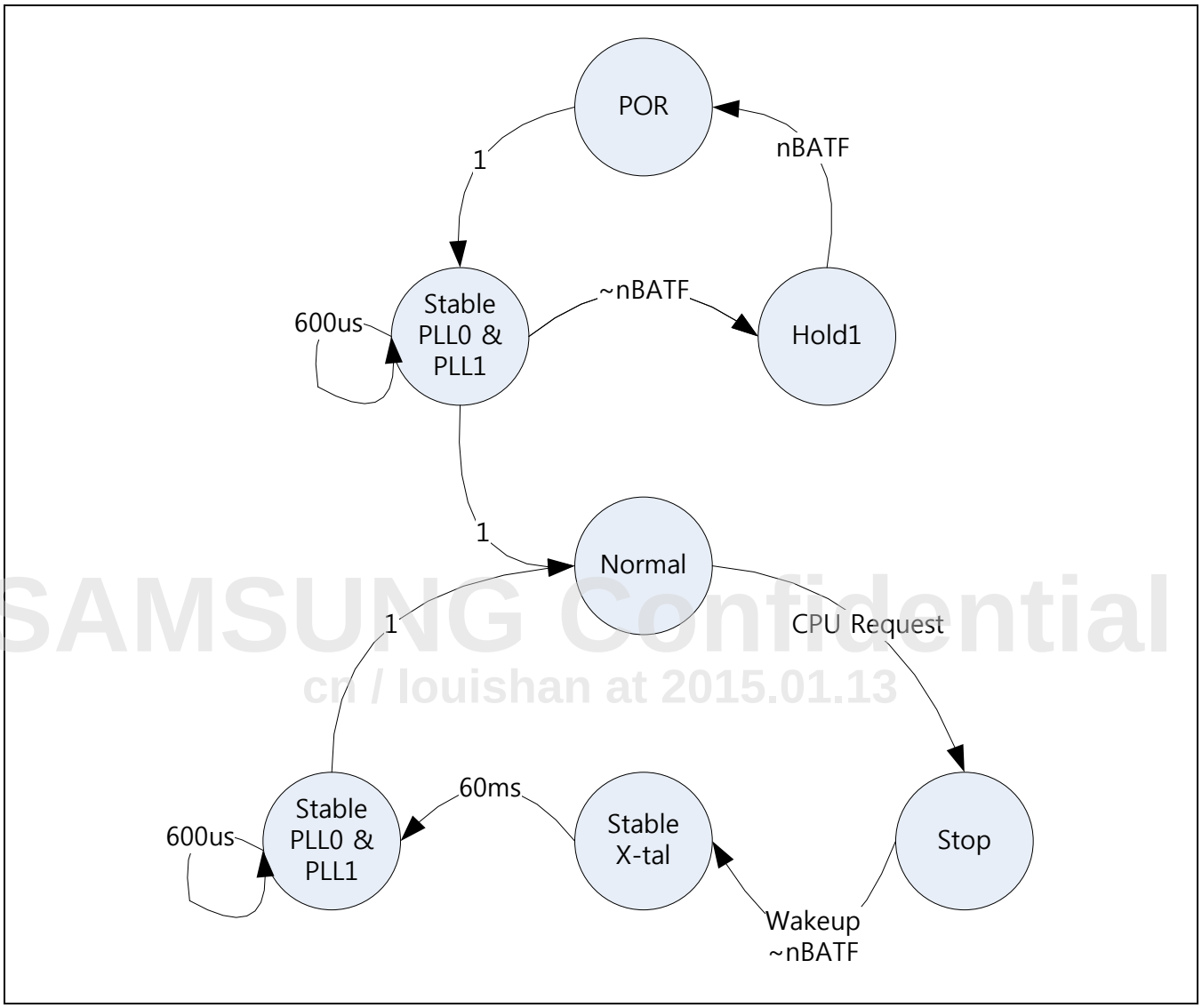


Figure 4-8 Power Management Sequence

- S5P4418 State
  - POR: Power On Reset State
  - Stable PLL: Wait for PLL locking time
  - NORMAL: Normal Operation State
  - STOP: Stop Operation Mode
  - Stable X-tal: Wait for Crystal's stable oscillation
  - Hold: Wait for nBATF = High.
- Wake Up Source
  - SWRST: Software Reset
  - SWRSTENB: Software Reset Enable
  - ALIVEGPIO Event: ALIVE GPIO Wake Up Event
  - CPUIRQ: Interrupt from CPU(IDLE Mode)
  - RTCIRQ: Interrupt from RTC
  - BAFT: Battery Fault
  - VDDPWRTOGGLE: VDDPWRTOGGLE Switch Push Button
  - WRST: Watchdog Reset

4.5.2.1 IDLE Mode

In the IDLE mode, since the power and clocks are supplied to all blocks except for the CPU clock, power consumption can be reduced a bit. To enter to IDLE mode, the PWRMODE.IDLE Register should be set as "1". In IDLE Mode, the CPU clock is not supplied, but the power is normally supplied and PLLs operate normally.

Wake-Up Source can use all the S5P4418 interrupts that can be generated by the Interrupt controller: GPIO Interrupt, Alive GPIO Interrupt, External Interrupt and RTC Interrupt. The interrupt for the Wake-Up Source should be enabled before entering to the IDLE Mode. The CPU returns to the previous status immediately after it is woken up in IDLE Mode.

4.5.2.2 STOP Mode

In STOP mode, the clock is not supplied to all bocks including the ARM Core, because the PLL also does not operate in the clock controller if the clock is not supplied to all blocks. However, the S5P4418 converts DRAM into Self Refresh mode to protect memory data before entering to STOP mode. Like IDLE mode, the PWRMODE.STOP should be set as "1" to enter to STOP mode.

The Wake Up source is slightly limited in STOP mode. The available Wake Up sources are RTC Interrupt, Alive GPIO Interrupt, etc. The Wake Up source is limited because the clock is not supplied to all the other blocks except for the power manager and RTC block. Since the RTC block uses a separate power and clock, only interrupts by the RTC clock can be used as a Wake Up source.

Unlike with IDLE mode, all PLLs stop when the system is woken up in STOP mode so that the system cannot return to the previous status, immediately. Therefore, the Wake Up time is about 70 ms longer than that of IDLE mode to stabilize the internal PLLs.

Table 4-11 Wake Up Condition and Power Down Mode Status

Power Down Mode	Power Supply	CPU Clock Supply	Other Clock Supply	SDRAM Mode	Wake Up Condition
IDLE MODE	ON	OFF	ON	NORMAL	RTC Interrupt, AliveGPIO Interrupt, All Interrupt to Interrupt Controller, External IRQ
STOP MODE	ON	OFF	OFF	Self Refresh	RTC Interrupt, AliveGPIO Interrupt

4.5.2.3 SLEEP Mode 1, SLEEP Mode 2

See the "ALIVE" Section for SLEEP Mode1 and SLEEP Mode2.

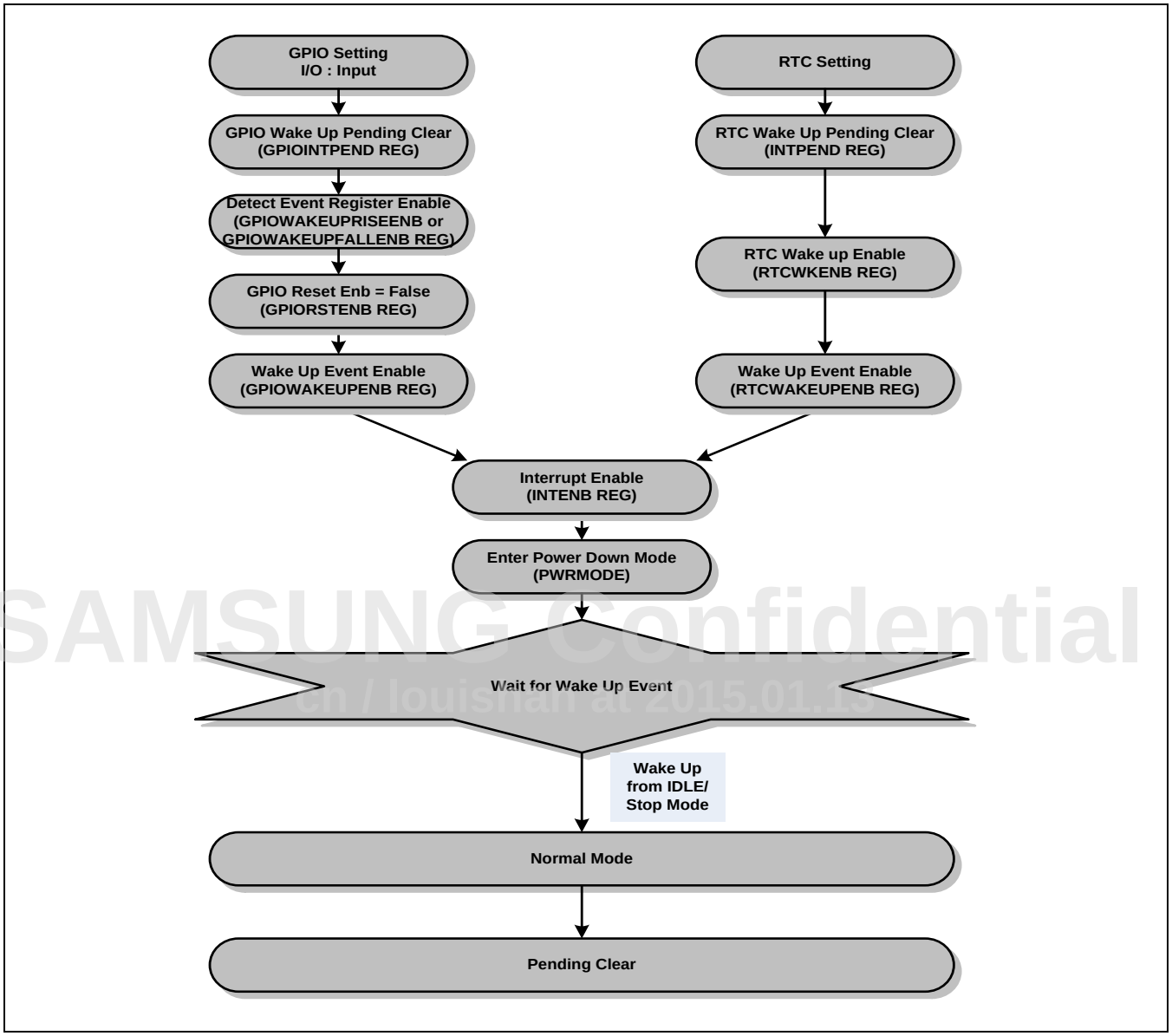


Figure 4-9 Power Down Mode Sequence

Figure 4-9 shows the sequence to enter the Power Down mode and the Wake Up procedure. First, the Wake Up source selects a desired event (interrupt) and specifies the attribute of the event. If the Wake up Source is GPIO, the setting is changed into Input and the Pending Clear is performed. In addition, the status to detect that an event (interrupt) is specified and Software Reset Enb is set as False for the worst case (If the Software Reset Enb switch is not implemented in terms of Hardware, False does not need to be specified). Finally, the system enables the relevant interrupt (if an interrupt is used) and enters a Power Down mode.

In this Power Down mode, the S5P4418 a waits a Wake Up event (interrupt). If the Wake Up event (Interrupt) occurs, the S5P4418 returns to normal mode and clears the relevant interrupt pending in terms of Software.

4.5.2.4 GPIO as a Wake up Source

GPIO is available for all Power Down modes. However, since the internal power and the clock status are not equal for each power modes, the operation status is a little different at each power mode.

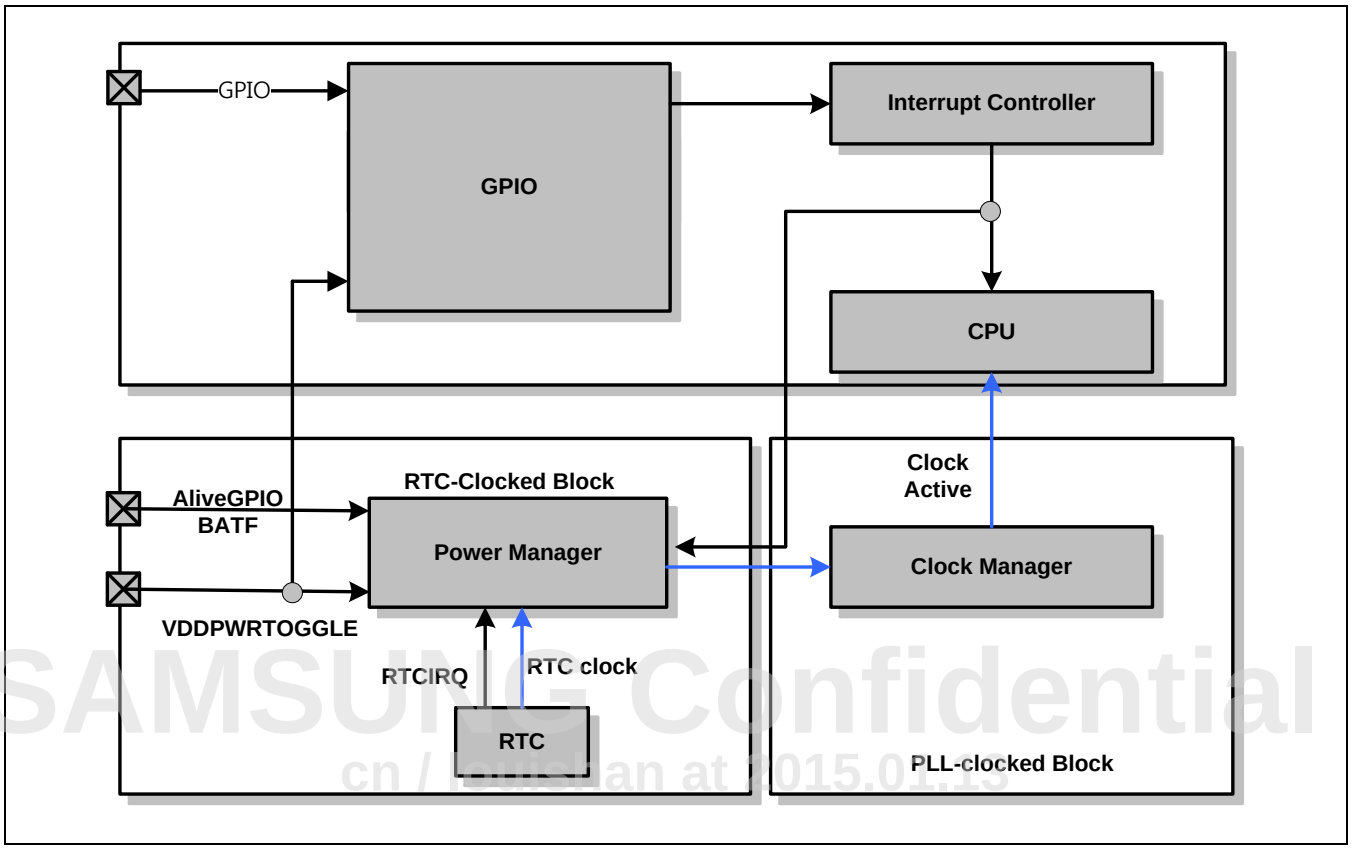


Figure 4-10 Wake Up Block Diagram

As shown in *Figure 4-10*, Power Manager use different clock. Since RTC-clock is always supplied to Power Manager Block, the PADs can be used as a Wake Up Source.

The description of the Wake Up procedures in Power Down mode is as follows:

- Wake Up in IDLE Mode

During IDLE mode, clock and the power for the other blocks are supplied normally except CPU clock. Therefore, the input received in GPIO is applied to the interrupt controller and wakes up the CPU.

- Wake Up in STOP Mode

In STOP mode, all clocks except for the RTC clock are not supplied (PLL and XTI are included). The interrupt controller does not operate in STOP mode. At this time, if a signal is entered to Power Manager, the power manager wakes up the clock manager, first. As a result of this Wake Up, all clocks, such as the PLL and PCLK, BCLK, MCLK and FCLK, are enabled and supplied to the CPU and the whole system. In other words, the system is woken up. The Wake Up time is about 70 ms longer than that of IDLE mode to stabilize the PLLs.

4.6 Reset Generation

4.6.1 Power on Reset Sequence

Power management block has the reset generation block. The reset generation block uses the nPORST which is sampled at RTC clock (32.768 kHz). And the RTC clock is used as main clock for power management. So Even if the RTC Function is not used, the RTC clock must be supplied.

Figure 4-11 shows the clock and reset behavior during the power-on reset sequence.

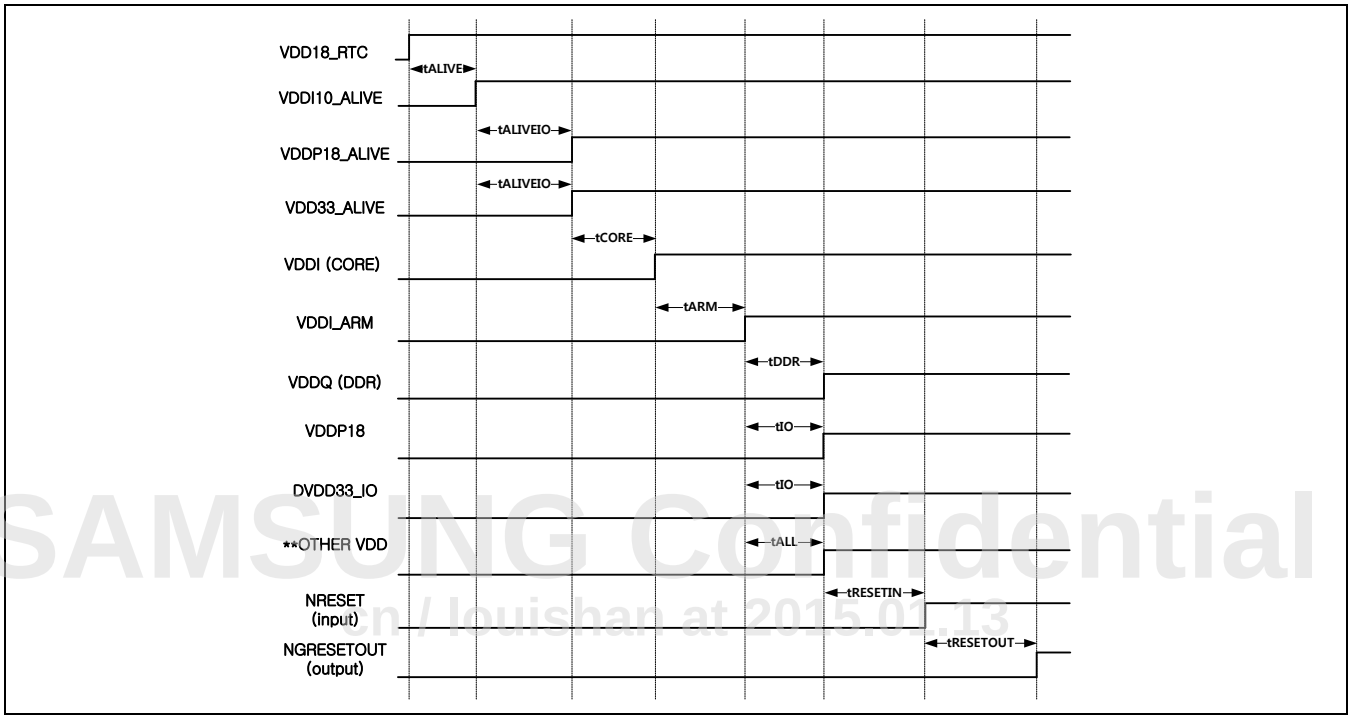


Figure 4-11 Power-On Reset Sequence

Table 4-12 Power-On Reset Timing Parameters

Symbol	Min (MSEC)	Max (MSEC)	Description
tALIVE	–50	Infinity	RTC to VDDI10_ALIVE
tALIVEIO	0	50	VDDI10_ALIVE to ALIVE IO power
tCORE	0	Infinity	VDDP18_ALIVE/VDD33_ALIVE to VDDI
tARM	0	50	VDDI to VDDI_ARM
tDDR	0	150	VDDI_ARM to VDDQ (DDR IO power)
tIO	0	150	VDDI_ARM to DVDD33_IO (normal IO power)
tALL	0	150	VDDI_ARM to DVDD33_IO (normal IO power)
tRESETIN	0	Infinity	All power on to assert nRESET
tRESETOUT	200	200	NRESET to NGRESETOUT

NOTE: Other VDD: this mean all other powers like analog power.

4.6.2 Sleep Mode Wakeup Sequence

All ALIVE and RTC power should be powered on before asserting sleep mode wakeup sequence.

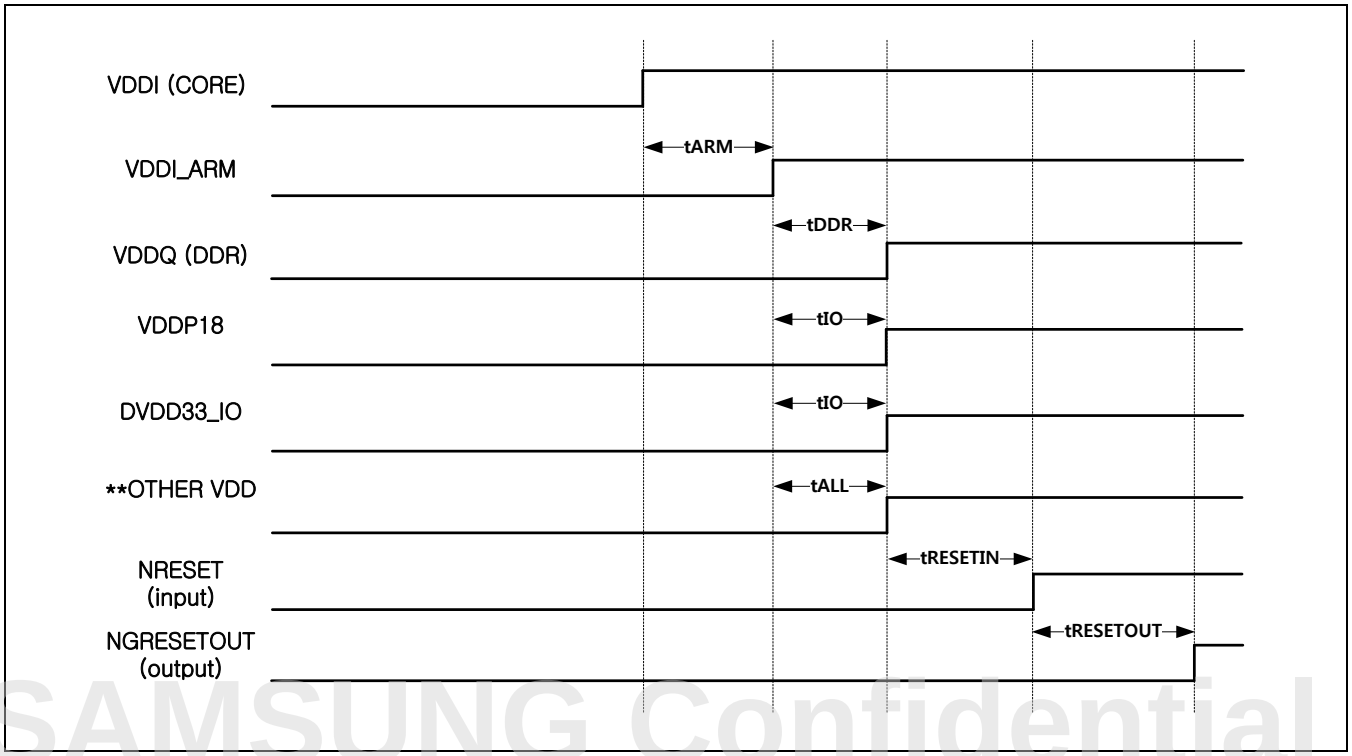


Figure 4-12 Power On Sequence for Wakeup

Table 4-13 Wakeup Timing Parameters

Symbol	Min (MSEC)	Max (MSEC)	Description
tARM	0	50	VDDI to VDDI_ARM
tDDR	0	150	VDDI_ARM to VDDQ (DDR IO power)
tIO	0	150	VDDI_ARM to DVDD33_IO (normal IO power)
tALL	0	150	VDDI_ARM to DVDD33_IO (normal IO power)
tRESETIN	0	Infinity	All power on to assert nRESET
tRESETOUT	200	200	NRESET to NGRESETOUT

NOTE: Other VDD: this mean all other powers like analog power.

4.6.3 Power off Sequence

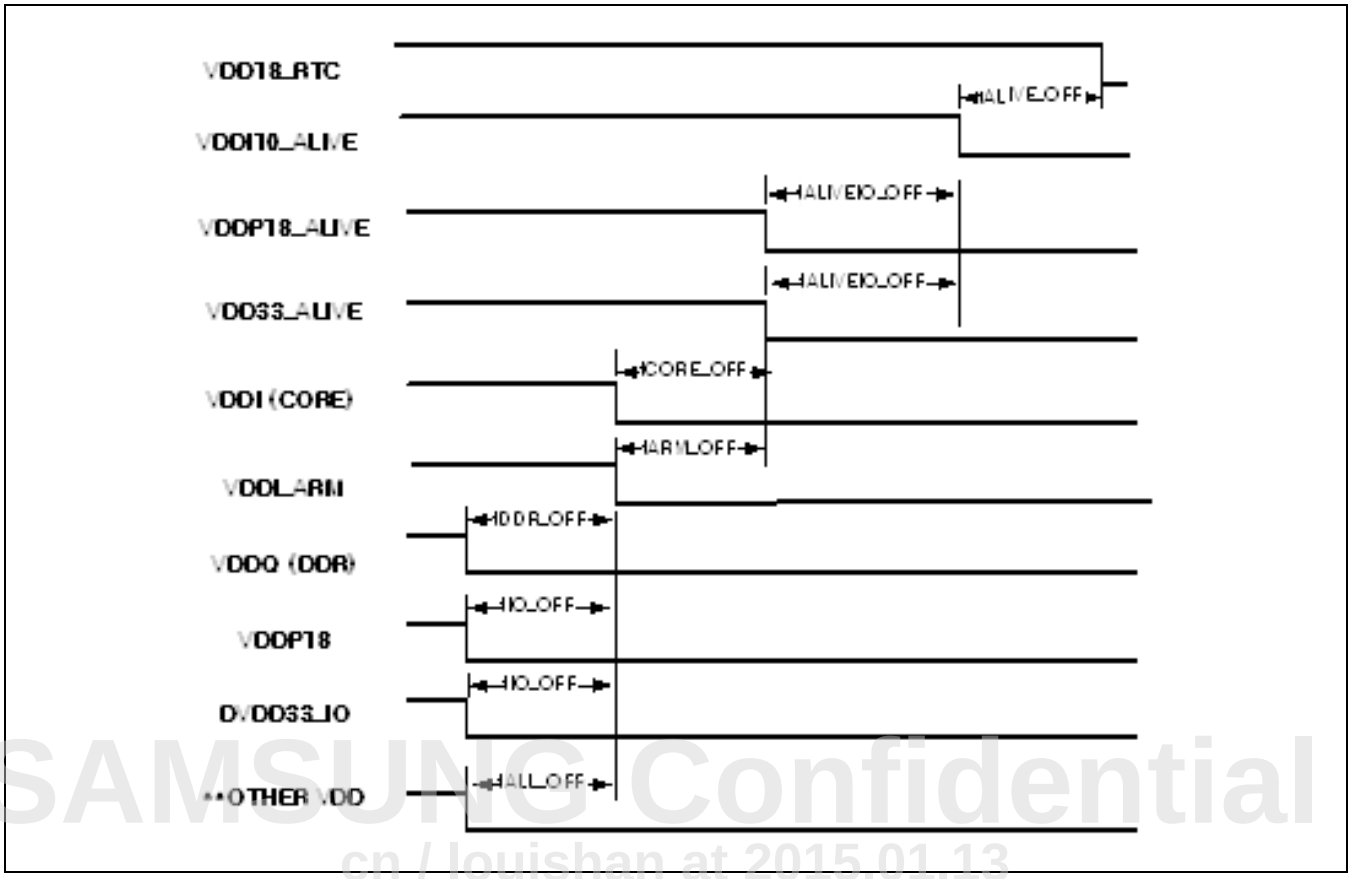


Figure 4-13 Power Off Sequence

Table 4-14 Power off Timing Parameters

Symbol	Min (MSEC)	Max (MSEC)	Description
tALIVE_OFF	–50	Infinity	ALIVE IO power to ALIVE CORE
tALIVEIO_OFF	0	50	ALIVE IO power to ALIVE core power
tCORE_OFF	0	Infinity	VDDI to ALIVE power
tARM_OFF	0	Infinity	VDDI_ARM to ALIVE power
tDDR_OFF	0	50	VDDQ (DDR IO power) to VDDI
tIO_OFF	0	50	DVDD33_IO (normal IO power) to VDDI
tALL_OFF	0	50	Other VDD power to VDDI

NOTE: Other VDD: this mean all other powers like analog power.

4.6.4 Software Reset and GPIO Reset

S5P4418 supports Software Reset that CPU can reset itself with Software reset. To generate Software Reset, SWRSTENB bit must be set to 1 before setting PWRMODE.SWRST bit. Software Reset mode does not need the time for stabilization clock because the software reset is requested in stable state differently from power on reset.

S5P4418 supports user defined GPIO Reset. The Power management block generates reset when the AliveGPIO pad defined as GPIO Reset source is asserted or de-asserted. The AliveGPIO pad is used as GPIO Reset source are defined at Wakeup Source Register. The GPIORSTENB bit set to 1 enables the AliveGPIO Reset source feature.

4.6.5 Watchdog Reset

The Watchdog timer block is used to resume the controller operation whenever it is disturbed by malfunctions such as system error, etc. When power management block detects the event from watchdog timer, it generates exactly the same reset as power on reset because the watchdog reset event occurs in malfunctions and unknown state.

4.6.5.1 nPORST, Software Reset, Watchdog Reset and GPIO Reset

S5P4418 has four reset states as below.

Table 4-15 Reset State

Blocks	Power On Reset	Watchdog Reset	GPIO Reset (Software Reset)	Wake Up (Idle, Stop)
Clock Manager	Reset	Reset	Reset	X
All Core (CPU and etc…)	Reset	Reset	Reset	X
GPIO	Reset	Reset	Reset	X
Power Manager (Except LASTPWRMODE Register)	Reset	Reset	Reset	X
LASTPWRMODE Register	Reset	X	X	X
RTC Registers (Except RTCCNTREAD Register)	Reset	Reset	Reset	X
RTCCNTREAD Register	X	X	X	X
nGRESETOUT (Output to PAD)	Reset	Reset	Reset	X

4.7 Tie Off

Tieoff block is a set of registers that includes special registers which don't need to be set in normal mode operation. Tieoff block includes special function registers for ARM, HDMI, DRAM controller, UART, USB2.0 HOST controller/Phy, USB2.0 OTG controller/Phy, Ethernet controller, AXI buses and the internal SRAM timing margin controls.

4.8 AXI BUS

ARM PL301 (AXI3 BUS interconnect) provides programmable function for AXI BUS and which includes QoS and Programmable Round-Robin.

4.8.1 Programmable Quality of Service (ProgQoS)

The QoS scheme works by tracking the number of outstanding transactions, and when a specified number is reached, only permits transactions from particular, specified masters.

The QoS scheme only provides support for slaves that have a combined acceptance capability, such as the PrimeCell Dynamic Memory Controller (PL340).

The QoS scheme has no effect until the AXI bus matrix calculates that, at a particular MI, there are a number of outstanding transactions equal to the value stored in the QoS tidemark Register. It then accepts transactions only from slave ports specified in the QoS access control Register. This restriction remains until the number of outstanding transactions is again less than the value stored in the QoS tidemark Register.

It is recommended that you assign low MI numbers to MIs that require QoS support. This approach aligns well with the cyclic priority scheme because MIs that require QoS support are typically those that can be considered high-ranking slaves. See the PrimeCell High-Performance Matrix (PL301) Technical Reference Manual.

Below Figure shows the implementation for an interconnection that supports two masters and one slave.

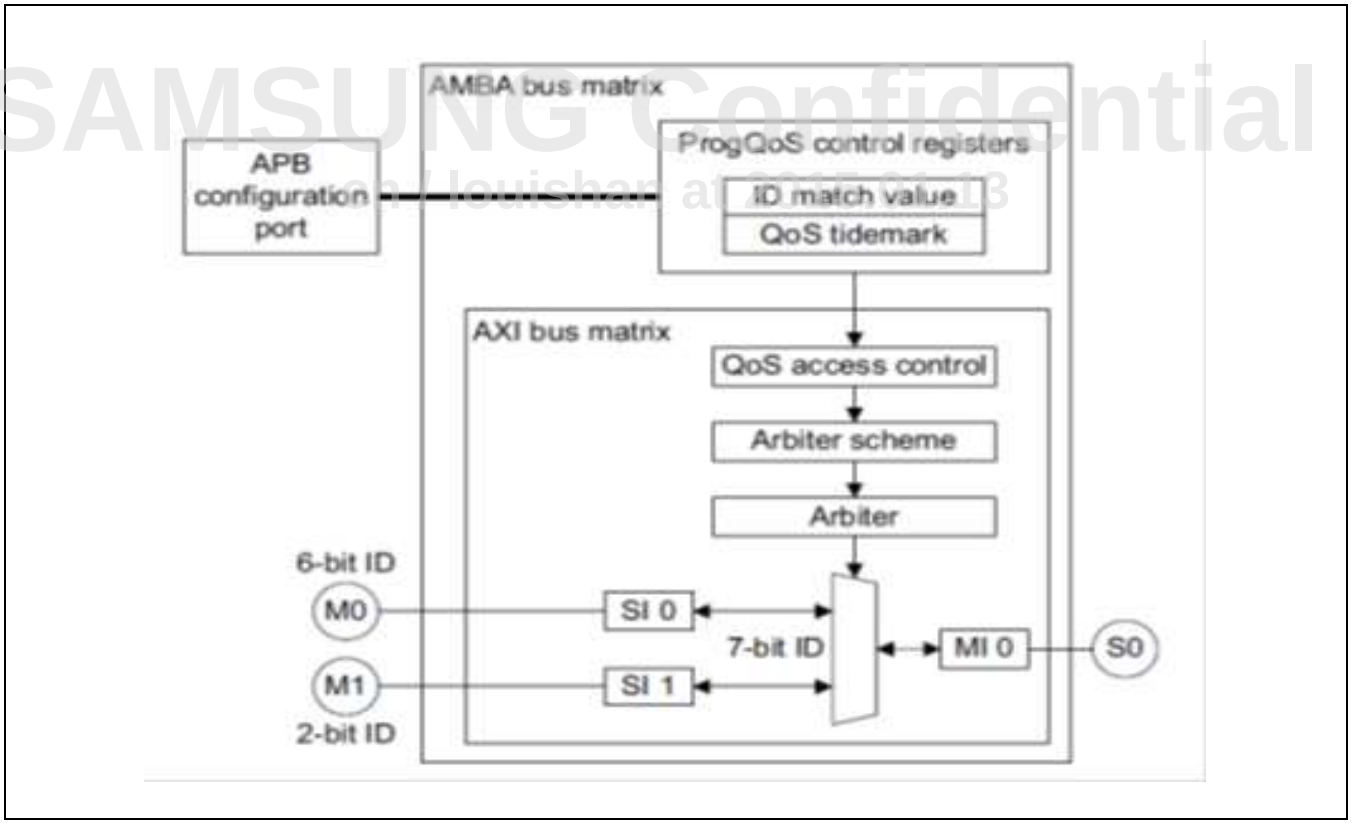


Figure 4-14 Example Implementation of ProgQoS Control Registers for 2×1 Interconnect

4.8.2 Arbitration scheme

You can configure each MI separately to have an arbitration scheme that is a programmable or fixed Round-robin (RR) scheme.

The AW and AR channels have separate arbiters and can be programmed, if applicable, and interrogated separately through the APB programming interface, but both AW and AR channels are configured identically. Because the AW and AR channels are arbitrated separately, an MI can permit simultaneous read and write transactions from different SIs.

The arbitration mechanism registers the arbitration decision for use in the subsequent cycle. An arbitration decision taken in the current cycle does not affect the current cycle.

If no SIs are active, the arbiter adopts default arbitration, that is, the highest priority SI. If this occurs and then the highest priority interface becomes active in the same cycle as, or before any other SI, then this does not constitute a grant to an active SI and the arbitration scheme does not change its state as a result of that transfer.

If a QoS provision is enabled and active, only a subset of SIs are permitted to win arbitration, and it cannot be guaranteed that the default arbitration is among these. In these circumstances, no transaction is permitted to use the default arbitration, and arbitration must occur when there is an active SI.

4.8.2.1 RR schemes

In these schemes, you can choose, at design time:

- the number of slots that are used
- the SI to which they are allocated
- their order.

There must be at least one slot per connected SI and there can be up to 32 slots. By allocating multiple slots for an SI, you can allocate access to the slave, on average, in proportion to the number of slots. If the slots are appropriately ordered, this can also reduce the maximum time before a grant is guaranteed. The SI associated with a slot can be interrogated from the APB programming interface and can be changed if the programmable RR scheme is chosen.

Whenever arbitration is granted to an active SI, the slots are rotated so that the slot currently in the highest priority position becomes the lowest, and all other slots move to a higher priority but maintain their relative order. This means that if an SI is the highest priority active SI, but is not the highest priority interface, then it continues to win the arbitration until it becomes the highest priority interface, and then the lowest priority interface subsequently.

Because the arbitration value is registered, the arbitration decision made in this cycle is used in the next cycle. This means that if the SI that currently holds the arbitration is still the highest priority active SI in this cycle, wins the arbitration again regardless of whether or not it is active in the next cycle as shown by the status of M3 in stages A, B, and C of below *Figure 4-15*.

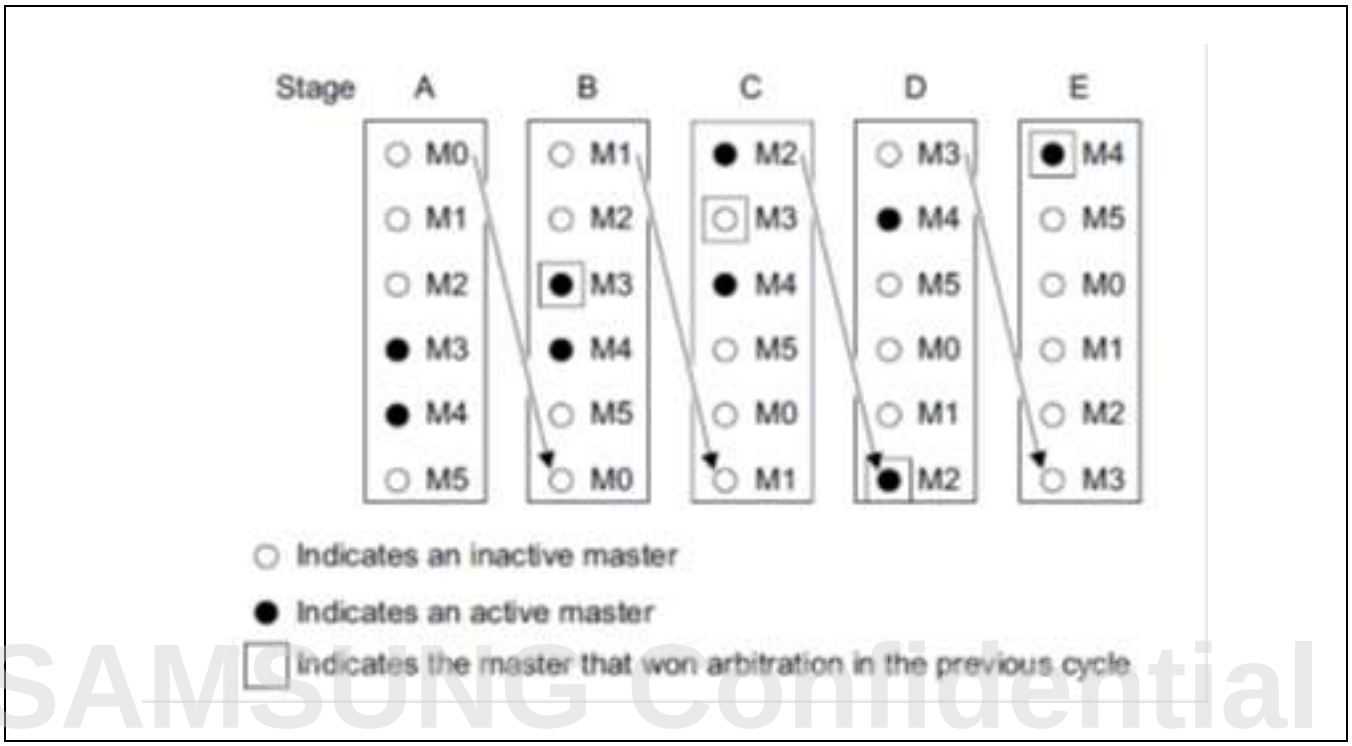


Figure 4-15 Example Operation of RR Arbitration Scheme

4.9 Register Description

4.9.1 Register Map Summary

4.9.1.1 Clock/Power Manager/Boot

- Base Address: 0xC001_0000

Register	Offset	Description	Reset Value
CLKMODEREG0	0000h	Clock Mode Register 0	0x0000_0000
CLKMODEREG1	0004h	CLOCK MODE REGISTER1	0x0000_0000
PLLSETREG0	0008h	PLL0 SETTING REGISTER	0x101A_2602
PLLSETREG1	000Ch	PLL1 SETTING REGISTER	0x101A_4E04
PLLSETREG2	0010h	PLL2 SETTING REGISTER	0x100C_C004
PLLSETREG3	0014h	PLL3 SETTING REGISTER	0x100C_0FA4
RSVD	0018h to 001Fh	Reserved	0x0000_0000
CLKDIVREG0	0020h	FCLKCPU0 SETTING REGISTER	0x0000_8208
CLKDIVREG1	0024h	BCLK SETTING REGISTER	0x0000_8208
CLKDIVREG2	0028h	CLKDIVREG2	0x0020_8000
CLKDIVREG3	002Ch	GR3DBCLK SETTING REGISTER	0x0000_8208
CLKDIVREG4	0030h	MPEGBCLK SETTING REGISTER	0x0000_8208
RSVD	0034h to 003Fh	Reserved	0x0000_0000
	0040h to 0047h		0x0000_0000
PLLSETREG0_SSCG	0048h	PLL0 SETTING REGISTER FOR SPREAD SPECTRUM	0x0000_0000
PLLSETREG1_SSCG	004Ch	PLL1 SETTING REGISTER FOR SPREAD SPECTRUM	0x0000_0000
PLLSETREG2_SSCG	0050h	PLL2 SETTING REGISTER FOR SPREAD SPECTRUM	0x0000_0000
PLLSETREG3_SSCG	0054h	PLL3 SETTING REGISTER FOR SPREAD SPECTRUM	0x0000_0000
GPIOWAKEUPRISEENB	0200h	RISING EDGE DETECT ENABLE REGISTER	0x0000_0003
GPIOWAKEUPFALLENB	0204h	FALLING EDGE DETECT ENABLE REGISTER	0x0000_0003
GPIORSTENB	0208h	GPIO RESET ENABLE REGISTER	0x0000_0003
GPIOWKENB	020Ch	GPIO WAKEUP ENABLE REGISTER	0x0000_0003
INTENB	0210h	GPIO INTERRUPT ENABLE REGISTER	0x0000_0003
GPIOINTPEND	0214h	GPIO INTERRUPT PENDING REGISTER	0x0000_0000
RESETSTATUS	0218h	RESET STATUS REGISTER	0x0000_0001
INTENABLE	021Ch	INTERRUPT ENABLE REGISTER	0x0000_0000
INTPEND	0220h	INTERRUPT PENDING REGISTER	0x0000_0000
PWRCONT	0224h	POWER MANGEMENT CONTROL REGISTER	0x0000_FF00
PWRMODE	0228h	POWER MANGEMENT MODE REGISTER	0x0000_0000

Register	Offset	Description	Reset Value
RSVD	022Ch	Reserved	0x0000_0000
PADSTRENGTHGPIOAL	0230h to 0238h	SCRATCH REGISTER	0x0000_0000
SYSRSTCONFIG	023Ch	SYSTEM RESET COFIGURATION REGISTER	0x0000_0000
RSVD	0240h to 03FFh	Reserved	0x0000_0000

4.9.1.1.1 CLKMODEREG0

- Base Address: 0xC001_0000
- Address = Base Address + 0000h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WAIT_UPDATE_PLL	[31]	RW	Wait flag updating-PLL for several RTC (32768 Hz) clocks 1 = In-process 0 = Done	1'b0
RSVD	[30:4]	–	reserved	1'b0
UPDATE_PLL[3]	[3]	RW	Update P,M,S values for PLL[3] 1 = Update 0 = None	1'b0
UPDATE_PLL[2]	[2]	RW	Update P,M,S values for PLL[2] 1 = Update 0 = None	1'b0
UPDATE_PLL[1]	[1]	RW	Update P,M,S values for PLL[1] 1 = Update 0 = None	1'b0
UPDATE_PLL[0]	[0]	RW	Update P,M,S values for PLL[0] 1 = Update 0 = None	1'b0

NOTE: The PMS values of PLL[n] is applied when UPDATE_PLL[n] is set to `1'.

4.9.1.1.2 CLKMODEREG1

- Base Address: 0xC001_0000
- Address = Base Address + 0004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:0]	–	Reserved	1'b0

4.9.1.1.3 PLLSETREG0

- Base Address: 0xC001_0000
- Address = Base Address + 0008h, Reset Value = 0x101A_2602

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
SSCG_EN	[30]	RW	PLL spread spectrum enable. This register is ignored for non-dithered PLL 1 = Enable 0 = Disable	1'b0
PD	[29]	RW	PLL Power down 1 = Power down 0 = Power on.	1'b0
nPLLBYPASS	[28]	RW	This register bypass PLL outputs. 1 = Normal PLL output 0 = X-tal clock (PLL input) is selected as PLL output.	1'b1
PLLOUTDIV	[27:24]	RW	PLL output for peripheral is divided by this register. PLL output for system clock is not affected by this register. 0 = Divide by one 1 = Divide by two N-1 = divide by N	4'b0
PDIV	[23:18]	RW	Pre Divider Value. Divider initially dividing 12 MHz to make PLL0 1 ≤ PDIV ≤ 63	6'd6
MDIV	[17:8]	RW	Main Divider Value. If the value of Fvco is not a desired clock, the value is divided into MDIV again after feedback. (This loop is continuously circulated until a desired clock frequency is made.) 64≤ MDIV ≤ 1023	10'd550
SDIV	[7:0]	RW	Post Scale Divider. Divide the value of Fvco by SDIV to obtain the desired PLL0 value finally. 0 ≤ SDIV ≤ 5	8'd2

4.9.1.1.4 PLLSETREG1

- Base Address: 0xC001_0000
- Address = Base Address + 000Ch, Reset Value = 0x101A_4E04

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
SSCG_EN	[30]	RW	PLL spread spectrum enable. This register is ignored for non-dithered PLL 0 = Disable 1 = Enable	1'b0
PD	[29]	RW	PLL Power down 0 = Power on 1 = Power down	1'b0
nPLLBYPASS	[28]	RW	This register bypass PLL outputs. 0 = X-tal clock (PLL input) is selected as PLL output 1 = Normal PLL output	1'b1
PLLOUTDIV	[27:24]	RW	PLL output for peripheral is divided by this register. PLL output for system clock is not affected by this register. 0 = Divide by one 1 = Divide by two N-1 = Divide by N	4'b0
PDIV	[23:18]	RW	Pre Divider Value. Divider initially dividing 12 MHz to make PLL0 1 ≤ PDIV ≤ 63	6'd6
MDIV	[17:8]	RW	Main Divider Value. If the value of Fvco is not a desired clock, the value is divided into MDIV again after feedback. (This loop is continuously circulated until a desired clock frequency is made.) 64≤ MDIV ≤ 1023	10'd590
SDIV	[7:0]	RW	Post Scale Divider. Divide the value of Fvco by SDIV to obtain the desired PLL0 value finally. 0 ≤ SDIV ≤ 5	8'd4

4.9.1.1.5 PLLSETREG2

- Base Address: 0xC001_0000
- Address = Base Address + 0010h, Reset Value = 0x100C_C004

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
SSCG_EN	[30]	RW	PLL spread spectrum enable. This register is ignored for non-dithered PLL 0 = Disable 1 = Enable	1'b0
PD	[29]	RW	PLL Power down 0 = Power on 1 = Power down	1'b0
nPLLBYPASS	[28]	RW	This register bypass PLL outputs. 0 = X-tal clock (PLL input) is selected as PLL output 1 = Normal PLL output	1'b1
PLLOUTDIV	[27:24]	RW	PLL output for peripheral is divided by this register. PLL output for system clock is not affected by this register. 0 = Divide by one 1 = Divide by two N-1 = Divide by N	4'b0
PDIV	[23:18]	RW	Pre Divider Value. Divider initially dividing 12 MHz to make PLL0 1 ≤ PDIV ≤ 63	6'd3
MDIV	[17:8]	RW	Main Divider Value. If the value of Fvco is not a desired clock, the value is divided into MDIV again after feedback. (This loop is continuously circulated until a desired clock frequency is made.) 64 ≤ MDIV ≤ 1023	10'd192
SDIV	[7:0]	RW	Post Scale Divider. Divide the value of Fvco by SDIV to obtain the desired PLL0 value finally. 0 ≤ SDIV ≤ 5	8'd4

4.9.1.1.6 PLLSETREG3

- Base Address: 0xC001_0000
- Address = Base Address + 0014h, Reset Value = 0x100C_0FA4

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
SSCG_EN	[30]	RW	PLL spread spectrum enable. This register is ignored for non-dithered PLL 0 = Disable 1 = Enable	1'b0
PD	[29]	RW	PLL Power down 0 = Power on 1 = Power down	1'b0
nPLLBYPASS	[28]	RW	This register bypass PLL outputs. 0 = X-tal clock (PLL input) is selected as PLL output 1 = Normal PLL output	1'b1
PLLOUTDIV	[27:24]	RW	PLL output for peripheral is divided by this register. PLL output for system clock is not affected by this register. 0 = Divide by one 1 = Divide by two N-1 = Divide by N	4'b0
PDIV	[23:18]	RW	Pre Divider Value. Divider initially dividing 12 MHz to make PLL0 1 ≤ PDIV ≤ 63	6'd3
MDIV	[17:8]	RW	Main Divider Value. If the value of Fvco is not a desired clock, the value is divided into MDIV again after feedback. (This loop is continuously circulated until a desired clock frequency is made.) 64≤ MDIV ≤ 1023	10'd250
SDIV	[7:0]	RW	Post Scale Divider. Divide the value of Fvco by SDIV to obtain the desired PLL0 value finally. 0 ≤ SDIV ≤ 5	8'd4

4.9.1.1.7 CLKDIVREG0

- Base Address: 0xC001_0000
- Address = Base Address + 0020h, Reset Value = 0x0000_8208

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	RW	Reserved	4'b0
RSVD	[26:21]	RW	Reserved	6'b0
RSVD	[20:15]	RW	Reserved	6'b1
CLKDIV_HCLKCPU0	[14:9]	RW	Divide value to create the clock of HCLKCPU0. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b Ex) For three clock divide, set this register to 000010b	6'b1
CLKDIV_FCLKCPU0	[8:3]	RW	Divide value to create the clock of FCLKCPU0. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1
CLKSEL_FCLKCPU0	[2:0]	RW	Select a clock source. If this bits is N, then PLL[N] is selected as clock source.	3'b0

4.9.1.1.8 CLKDIVREG1

- Base Address: 0xC001_0000
- Address = Base Address + 0024h, Reset Value = 0x0000_8208

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	RW	Reserved	4'b0
RSVD	[26:21]	RW	Reserved	6'b0
RSVD	[20:15]	RW	Reserved	6'b1
CLKDIV_PCLK	[14:9]	RW	Divide value to create the clock of PCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1
CLKDIV_BCLK	[8:3]	RW	Divide value to create the clock of BCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b	6'b1

Name	Bit	Type	Description	Reset Value
			Ex) For three clock divide, set this register to 000010b	
CLKSEL_BCLK	[2:0]	RW	Select a clock source. If this bits is N, then PLL[N] is selected as clock source.	3'b0

4.9.1.1.9 CLKDIVREG2

- Base Address: 0xC001_0000
- Address = Base Address + 0028h, Reset Value = 0x0020_8000

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	RW	Reserved	4'b0
CLKDIV_MPCLK	[26:21]	RW	Divide value to create the clock of MPCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1
CLKDIV_MBCLK	[20:15]	RW	Divide value to create the clock of MBCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1
CLKDIV_MCLK	[14:9]	RW	Divide value to create the clock of MCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b0
CLKDIV_MDCLK	[8:3]	RW	Divide value to create the clock of MDCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b0
CLKSEL_MDCLK	[2:0]	RW	Select a clock source. If this bits is N, then PLL[N] is selected as clock source.	3'b0

4.9.1.1.10 CLKDIVREG3

- Base Address: 0xC001_0000
- Address = Base Address + 002Ch, Reset Value = 0x0000_8208

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	RW	Reserved	4'b0
RSVD	[26:21]	RW	Reserved	6'b0
RSVD	[20:15]	RW	Reserved	6'b1
CLKDIV_GR3DPCLK	[14:9]	RW	Divide value to create the clock of GR3DPCLK. For "N"' clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1
CLKDIV_GR3DBCLK	[8:3]	RW	Divide value to create the clock of GR3DBCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1
CLKSEL_GR3DBCLK	[2:0]	RW	Select a clock source. If this bits is N, then PLL[N] is selected as clock source.	3'b0

4.9.1.1.11 CLKDIVREG4

- Base Address: 0xC001_0000
- Address = Base Address + 0030h, Reset Value = 0x0000_8208

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	RW	Reserved	4'b0
RSVD	[26:21]	RW	Reserved	6'b0
RSVD	[20:15]	RW	Reserved	6'b1
CLKDIV_MPEGPCLK	[14:9]	RW	Divide value to create the clock of HC MPEGPCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1
CLKDIV_MPEGBCLK	[8:3]	RW	Divide value to create the clock of MPEGBCLK. For "N" clock divide, enter an [N-1] value. Register Set value 000001 to 111111 → actual Divide Value = 2 to 64 Ex) For eight clock divide, set this register to 000111b For three clock divide, set this register to 000010b	6'b1

Name	Bit	Type	Description	Reset Value
CLKSEL_MPEGBCLK	[2:0]	RW	Select a clock source. If this bits is N, then PLL[N] is selected as clock source.	3'b0

4.9.1.1.12 PLLSETREG0_SSCG

- Base Address: 0xC001_0000
- Address = Base Address + 0048h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
K	[31: 16]	RW	Value of 16-bit DSM.	16'b0
MFR	[15:8]	RW	Modulation frequency control	8'b0
MRR	[7:2]	RW	Modulation rate control	6'b0
SEL_PF	[1:0]	RW	Modulation method 00 = Down spread 01 = Up spread 1x = Center spread	2'b0

NOTE: This register is applied only for dithered-type PLL.

4.9.1.1.13 PLLSETREG1_SSCG

- Base Address: 0xC001_0000
- Address = Base Address + 004Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
K	[31: 16]	RW	Value of 16-bit DSM.	16'b0
MFR	[15:8]	RW	Modulation frequency control	8'b0
MRR	[7:2]	RW	Modulation rate control	6'b0
SEL_PF	[1:0]	RW	Modulation method 00 = Down spread 01 = Up spread 1x = Center spread	2'b0

NOTE: This register is applied only for dithered-type PLL.

4.9.1.1.14 PLLSETREG2_SSCG

- Base Address: 0xC001_0000
- Address = Base Address + 0050h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
K	[31: 16]	RW	Value of 16-bit DSM.	16'b0
MFR	[15:8]	RW	Modulation frequency control	8'b0
MRR	[7:2]	RW	Modulation rate control	6'b0
SEL_PF	[1:0]	RW	Modulation method 00 = Down spread 01 = Up spread 1x = Center spread	2'b0

NOTE: This register is applied only for dithered-type PLL.

4.9.1.1.15 PLLSETREG3_SSCG

- Base Address: 0xC001_0000
- Address = Base Address + 0054h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
K	[31: 16]	RW	Value of 16-bit DSM.	16'b0
MFR	[15:8]	RW	Modulation frequency control	8'b0
MRR	[7:2]	RW	Modulation rate control	6'b0
SEL_PF	[1:0]	RW	Modulation method 00 = Down spread 01 = Up spread 1x = Center spread	2'b0

NOTE: This register is applied only for dithered-type PLL.

4.9.1.1.16 GPIOWAKEUPRISEENB

- Base Address: 0xC001_0000
- Address = Base Address + 0200h, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
RSVD	[31: 15]	–	Reserved	17'b0
RISEWKSRC14	[14]	RW	Wakeup source (USB20OTG.SUSPEND) Rising Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
RISEWKSRC13	[13]	RW	Wakeup source (USB20OTG.SLEEP) Rising Edge Detect Enable This bit enables wakeup form power down modes, when USB2.0 OTG's Sleep pin toggles. 0 = Disable 1 = Enable	1'b0
RISEWKSRC12	[12]	RW	Reserved. This bit must be set to "1'b0"	1'b0
RISEWKSRC11	[11]	RW	Reserved. This bit must be set to "1'b0"	1'b0
RISEWKSRC10	[10]	RW	Wakeup source (UART[3].RX) Rising Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
RISEWKSRC9	[9]	RW	Wakeup source (UART[2].RX) Rising Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
RISEWKSRC8	[8]	RW	Wakeup source (UART[1].RX) Rising Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
RISEWKSRC7	[7]	RW	Wakeup source (UART[0].RX) Rising Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0

Name	Bit	Type	Description	Reset Value
RISEWKSRC6	[6]	RW	Wakeup source (VDDPWRTOGGLE) Rising Edge Detect Enable This bit enables wakeup form power down modes, when user pushed VDDPWRTOGGLE PAD. 0 = Disable 1 = Enable	1'b0
RISEWKSRC5	[5]	RW	Wakeup Source (ALIVEGPIO5) Rising Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
RISEWKSRC4	[4]	RW	Wakeup Source (ALIVEGPIO4) Rising Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
RISEWKSRC3	[3]	RW	Wakeup Source (ALIVEGPIO3) Rising Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
RISEWKSRC2	[2]	RW	Wakeup Source (ALIVEGPIO2) Rising Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
RISEWKSRC1	[1]	RW	Wakeup Source (ALIVEGPIO1) Rising Edge Detect Enable 0 = Disable 1 = Enable	1'b 1
RISEWKSRC0	[0]	RW	Wakeup Source (ALIVEGPIO0) Rising Edge Detect Enable 0 = Disable 1 = Enable	1'b 1

4.9.1.1.17 GPIOWAKEUPFALLENB

- Base Address: 0xC001_0000
- Address = Base Address + 0204h, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
RSVD	[31 :15]	–	Reserved	17'b0
FALLWKSRC14	[14]	RW	Wakeup source (USB20OTG.SUSPEND)Falling Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin pin toggles. 0 = Disable 1 = Enable	1'b0
FALLWKSRC13	[13]	RW	Wakeup source (USB20OTG.SLEEP)Falling Edge Detect Enable This bit enables wakeup form power down modes, when USB2.0 OTG's Sleep pin toggles. 0 = Disable 1 = Enable	1'b0
FALLWKSRC12	[12]	RW	Reserved. This bit must be set to `1'b0'	1'b0
FALLWKSRC11	[11]	RW	Reserved. This bit must be set to `1'b0'	1'b0
FALLWKSRC10	[10]	R/W	Wakeup source (UART[3].RX)Falling Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
FALLWKSRC9	[9]	R/W	Wakeup source (UART[2].RX)Falling Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
FALLWKSRC8	[8]	R/W	Wakeup source (UART[1].RX)Falling Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
FALLWKSRC7	[7]	R/W	Wakeup source (UART[0].RX)Falling Edge Detect Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0

Name	Bit	Type	Description	Reset Value
FALLWKSRC6	[6]	RW	Wakeup source (VDDPWRTOGGLE) Falling Edge Detect Enable 0 = Disable 1 = Enable	1'b0
FALLWKSRC5	[5]	RW	Wakeup Source (ALIVEGPIO5) Falling Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
FALLWKSRC4	[4]	RW	Wakeup Source (ALIVEGPIO4) Falling Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
FALLWKSRC3	[3]	RW	Wakeup Source (ALIVEGPIO3) Falling Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
FALLWKSRC2	[2]	RW	Wakeup Source (ALIVEGPIO2) Falling Edge Detect Enable 0 = Disable 1 = Enable	1'b 0
FALLWKSRC1	[1]	RW	Wakeup Source (ALIVEGPIO1) Falling Edge Detect Enable 0 = Disable 1 = Enable	1'b 1
FALLWKSRC0	[0]	RW	Wakeup Source (ALIVEGPIO0) Falling Edge Detect Enable 0 = Disable 1 = Enable	1'b 1

4.9.1.1.18 GPIORSTENB

- Base Address: 0xC001_0000
- Address = Base Address + 0208h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31: 15]	RW	Reserved (These bits should always be "0")	17'b0
RSVD	[14:6]	RW	Reserved (These bits should always be "0")	1'b0
GPIO5RSTENB	[5]	RW	ALIVEGPIO5 Reset Source Enable 0 = Disable 1 = Enable	1'b0
GPIO4RSTENB	[4]	RW	ALIVEGPIO4 Reset Source Enable 0 = Disable 1 = Enable	1'b0
GPIO3RSTENB	[3]	RW	ALIVEGPIO3 Reset Source Enable 0 = Disable 1 = Enable	1'b0
GPIO2RSTENB	[2]	RW	ALIVEGPIO2 Reset Source Enable 0 = Disable 1 = Enable	1'b0
GPIO1RSTENB	[1]	RW	ALIVEGPIO1 Reset Source Enable 0 = Disable 1 = Enable	1'b0
GPIO0RSTENB	[0]	RW	ALIVEGPIO0 Reset Source Enable 0 = Disable 1 = Enable	1'b0

NOTE: Wake-up and Reset Enable are not allowed at the same time for the same ALIVEGPIO.

4.9.1.1.19 GPIOWKENB

- Base Address: 0xC001_0000
- Address = Base Address + 020Ch, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
RSVD	[31: 15]	RW	Reserved	17'b0
GPIO14WKENB	[14]	RW	Wakeup source (USB20OTG.SUSPEND) Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO13WKENB	[13]	RW	Wakeup source (USB20OTG.SLEEP) Enable This bit enables wakeup form power down modes, when USB2.0 OTG's Sleep pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO12WKENB	[12]	RW	Reserved. This bit must be set to "1'b0"	1'b0
GPIO11WKENB	[11]	RW	Reserved. This bit must be set to "1'b0"	1'b0
GPIO10WKENB	[10]	RW	Wakeup source (UART[3].RX) Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO9WKENB	[9]	RW	Wakeup source (UART[2].RX) Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO8WKENB	[8]	RW	Wakeup source (UART[1].RX) Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO7WKENB	[7]	RW	Wakeup source (UART[0].RX) Enable This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
VDDTOGGLEWKENB	[6]	RW	VDDPWRTOGGLE Wakeup Source Enable 0 = Disable 1 = Enable	1'b0
GPIO5WKENB	[5]	RW	ALIVEGPIO5 Wakeup Source Enable 0 = Disable	1'b0

Name	Bit	Type	Description	Reset Value
			1 = Enable	
GPIO4WKENB	[4]	RW	ALIVEGPIO4 Wakeup Source Enable 0 = Disable 1 = Enable	1'b0
GPIO3WKENB	[3]	RW	ALIVEGPIO3 Wakeup Source Enable 0 = Disable 1 = Enable	1'b0
GPIO2WKENB	[2]	RW	ALIVEGPIO2 Wakeup Source Enable 0 = Disable 1 = Enable	1'b0
GPIO1WKENB	[1]	RW	ALIVEGPIO1 Wakeup Source Enable 0 = Disable 1 = Enable	1'b1
GPIO0WKENB	[0]	RW	ALIVEGPIO0 Wakeup Source Enable 0 = Disable 1 = Enable	1'b1

NOTE: Wake-up and Reset Enable are not allowed at the same time for the same ALIVEGPIO.

4.9.1.1.20 INTENB

- Base Address: 0xC001_0000
- Address = Base Address + 0210h, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
RSVD	[31: 15]	–	Reserved	17'b0
GPIO14	[14]	RW	Wakeup source (USB20OTG.SUSPEND) Event Interrupt Enable This bit enables wakeup form power down modes, when UART RX pin pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO13	[13]	RW	Wakeup source (USB20OTG.SLEEP) Event Interrupt Enable This bit enables wakeup form power down modes, when USB2.0 OTG's Sleep pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO12	[12]	RW	Reserved. This bit must be set to "1'b0"	1'b0
GPIO11	[11]	RW	Reserved. This bit must be set to "1'b0"	1'b0
GPIO10	[10]	RW	Wakeup source (UART[3].RX) Event Interrupt Enable This bit enables wakeup form power down modes,	1'b0

Name	Bit	Type	Description	Reset Value
			when UART RX pin pin toggles. 0 = Disable 1 = Enable	
GPIO9	[9]	RW	Wakeup source (UART[2].RX) Event Interrupt Enable This bit enables wakeup form power down modes, when UART RX pin pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO8	[8]	RW	Wakeup source (UART[1].RX) Event Interrupt Enable This bit enables wakeup form power down modes, when UART RX pin pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO7	[7]	RW	Wakeup source (UART[0].RX) Event Interrupt Enable This bit enables wakeup form power down modes, when UART RX pin pin toggles. 0 = Disable 1 = Enable	1'b0
vddtoggle	[6]	RW	VDDPWRTOGGLE Event Interrupt Enable 0 = Disable 1 = Enable	1'b0
GPIO5	[5]	RW	ALIVEGPIO5 Event Interrupt Enable 0 = Disable 1 = Enable	1'b0
GPIO4	[4]	RW	ALIVEGPIO4 Event Interrupt Enable 0 = Disable 1 = Enable	1'b0
GPIO3	[3]	RW	ALIVEGPIO3 Event Interrupt Enable 0 = Disable 1 = Enable	1'b0
GPIO2	[2]	RW	ALIVEGPIO2 Event Interrupt Enable 0 = Disable 1 = Enable	1'b0
GPIO1	[1]	RW	ALIVEGPIO1 Event Interrupt Enable 0 = Disable 1 = Enable	1'b1
GPIO0	[0]	RW	ALIVEGPIO0 Event Interrupt Enable 0 = Disable 1 = Enable	1'b1

4.9.1.1.21 GPIOINTPEND

- Base Address: 0xC001_0000
- Address = Base Address + 0214h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
GPIO14PEND	[14]	RW	This bit is set as "1" when (USB20OTG. SUSPEND) Event occurs. And this bit is cleared by setting as "1" This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO13PEND	[13]	RW	This bit is set as "1" when (USB20OTG.SLEEP) Event occurs. And this bit is cleared by setting as "1" This bit enables wakeup form power down modes, when USB2.0 OTG's Sleep pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO12PEND	[12]	RW	Reserved. This bit must be set to "1'b0"	1'b0
GPIO11PEND	[11]	RW	Reserved. This bit must be set to "1'b0"	1'b0
GPIO10PEND	[10]	RW	This bit is set as "1" when (UART[3].RX) Event occurs. And this bit is cleared by setting as "1" This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO9PEND	[9]	RW	This bit is set as "1" when (UART[2].RX) Event occurs. And this bit is cleared by setting as "1" This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO8PEND	[8]	RW	This bit is set as "1" when (UART[1].RX) Event occurs. And this bit is cleared by setting as "1" This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0
GPIO7PEND	[7]	RW	This bit is set as "1" when (UART[0].RX) Event occurs. And this bit is cleared by setting as "1" This bit enables wakeup form power down modes, when UART RX pin toggles. 0 = Disable 1 = Enable	1'b0

Name	Bit	Type	Description	Reset Value
VDDTOGGLEPEND	[6]	RW	This bit is set as "1" when VDDPWRTOGGLE Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0
GPIO5PEND	[5]	RW	This bit is set as "1" when ALIVEGPIO5 Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0
GPIO4PEND	[4]	RW	This bit is set as "1" when ALIVEGPIO4 Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0
GPIO3PEND	[3]	RW	This bit is set as "1" when ALIVEGPIO3 Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0
GPIO2PEND	[2]	RW	This bit is set as "1" when ALIVEGPIO2 Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0
GPIO1PEND	[1]	RW	This bit is set as "1" when ALIVEGPIO1 Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear	1'b0

Name	Bit	Type	Description	Reset Value
			1 = Clear	
GPIO0PEND	[0]	RW	This bit is set as "1" when ALIVEGPIO0 Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0

4.9.1.1.22 RESETSTATUS

- Base Address: 0xC001_0000
- Address = Base Address + 0218h, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
RSVD	[31: 4]	–	Reserved	28'b0
SOFTWARERESET	[3]	R	Software Reset Status. This bit is cleared when other Reset occurs 0 = No Effect 1 = Software Reset	1'b0
WATCHDOGRESET	[2]	R	Watchdog Reset Status. This bit is cleared when other Reset occurs 0 = No Effect 1 = Watchdog Reset	1'b0
GPIORESET	[1]	R	GPIO Reset Status. This bit is cleared when other Reset occurs 0 = No Effect 1 = GPIO Reset	1'b0
POR	[0]	R	Power On Reset Status. This bit is cleared when other Reset occurs 0 = No Effect 1 = Power On Reset	1'b1

NOTE: The priority of Reset - POR > GPIO > Watchdog > Software

4.9.1.1.23 INTENABLE

- Base Address: 0xC001_0000
- Address = Base Address + 021Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31: 2]	–	Reserved	30'b0
BATF	[1]	RW	BATF(Battery Fault) Event Interrupt Enable Interrupt occurs when BATF is low level. 0 = Disable 1 = Enable	1'b0
RTC	[0]	RW	RTC Event Interrupt Enable Interrupt occurs when BATF is low level. 0 = Disable 1 = Enable	1'b0

4.9.1.1.24 INTPEND

- Base Address: 0xC001_0000
- Address = Base Address + 0220h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31: 2]	R-	Reserved	30'b0
BATFWAKEUP	[1]	RW	This bit is set as "1" when BATF (Battery Fault) Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0
RTCWAKEUP	[0]	RW	This bit is set as "1" when RTC Wakeup Event occurs. And this bit is cleared by setting as "1" Read 0 = None 1 = Interrupt Pended Write 0 = Not Clear 1 = Clear	1'b0

4.9.1.1.25 PWRCONT

- Base Address: 0xC001_0000
- Address = Base Address + 0224h, Reset Value = 0x0000_FF00

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
USE_WFI	[15:12]	RW	Use STANDBYWFI[n] signal as indicating signal to go into stop mode.	4'b1111
USE_WFE	[11:8]	RW	Use STANDBYWFE[n] signal as indicating signal to go into stop mode.	4'b1111
XTAL_PWRDN	[4]	RW	Xrystal power down mode selection This controls the power down of Xrystal-PAD in stop-mode. 0 = XTAL is powered down instop mode 1 = XTAL is not powered down in stop mode	1'b0
SWRSTENB	[3]	RW	Software Reset Enable. 0 = Disable 1 = Enable	1'b0
RESERVED	[2]	RW	Reserved (This bit always should be "0")	1'b0
RTCWKENB	[1]	RW	RTC Wake-up enable 0 = Disable 1 = Enable	1'b0
RESERVED	[0]	RW	Reserved (This bit always should be "0")	1'b0

4.9.1.1.26 PWRMODE

- Base Address: 0xC001_0000
- Address = Base Address + 0228h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	16'b0
chgpll	[15]	RW	Change PLL Value with new value defined in PLL Setting Register (PLL0set, PLL1set) in clock Controller. Read 0 = Stable 1 = PLL is Unstable Write 0 = None 1 = PLL Value Change	1'b0
RSVD	[14:13]		Reserved	2'b0
swrst	[12]	W	This bit is cleared after Software Reset 0 = Do Not Reset 1 = Go to Reset	1'b0

Name	Bit	Type	Description	Reset Value
RSVD	[11:6]	R	Reserved	6'b0
LASTPWRSTOP	[5]	R	Indicates that the chip has been in STOP Mode before in Normal state.(This bit is cleared in case of Reset in Normal state) 0 = None 1 = Stop mode	1'b0
LASTPWRIDLE	[4]	R	Indicates that the chip has been in STOP Mode before in Normal state.(This bit is cleared in case of Reset in Normal state) 0 = None 1 = Idle mode	1'b0
RSVD	[3]	RW	Reserved	1'b0
RSVD	[2]	RW	Reserved (This bit always should be `0')	1'b0
STOP	[1]	RW	Set New Power Mode STOP. The chip wakes up to be in Normal mode when RTC, GPIO occurs in STOP mode, and this bit is cleared. Read 0 = Normal 1 = Stop mode Write 0 = None 1 = go to stop mode	1'b0
IDLE	[0]	RW	Set New Power Mode IDLE. The chip wakes up to be in Normal mode when RTC, GPIO, Watchdog reset, and CPU interrupt occurs in STOP mode, and this bit is cleared. Read 0 = Normal 1 = Idle mode Write 0 = None 1 = go to Idle mode	1'b0

4.9.1.1.27 PADSTRENGTHGPIOAL

- Base Address : 0xC001_0000
- Address = Base Address + 0230h, 0234h, 0238h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SCRATCH	[31:0]	RW	Register is initialized only in case of CORE Power On Reset. (size: 8 byte)	0x0000_0000

4.9.1.1.28 SYSRSTCONFIG

- Base Address : 0xC001_0000

- Address = Base Address + 023Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
SCRATCH	[31:22]	R	Reserved	-
CfgICACHE	[21]	R	Indicates L1 Cache enable when (CfgBootMode ! = 4'hF) In the case of internal rom boot, use this register for CPU Instruction cache enable 0 = Disable 1 Enable	VID1_5
CfgDecrypt	[20]	R	Indicates AES ECB mode decrypt when (CfgBootMode ! = 4'hF) 0 = Not decrypt 1 = Decrypt	VID1_4
RSVD	[19]	R	Reserved	VID1_3
CfgNANDPage	[18]	R	Indicates External nand page size when (CfgBootMode == 4'h7). 0 = 2K or below 1 = 4K or above	VID1_2
CfgNANDType	[17:16]	R	Indicates External nand type when (CfgBootMode == 4'hF). 0 = Small Block 3 Address 1 = Small block 4 Address 2 = Large 4 Address 3 = Large 5 Address	2'b{VID1_1, VID1_0}
CfgBootMode	[15:12]	R	System boot mode. 4'bx000: Nor boot 4'bx011: Internal ROM UART boot 4'bx100: Internal ROM Serial flash boot 4'bx101: Internal ROM SD boot 4'bx110: Internal ROM USB boot 4'b0111: Internal ROM NAND boot 4'b1111: Internal ROM NANDEX boot	4'b{ DISD7, DISD6, DISD5, DISD4}
CfgSTBUSWIDTH	[11]	R	Static Memory BUS bit. Internal ROM boot fixed 0. 0 = 8-bit 1 = 16-bit	DISD3
CfgAlternative	[10]	R	Indicates eMMC Alternative Boot mode when (CfgBootMode == 4'bx101). 0 = Alternative Boot 1 = Normal Boot Indicates [1] bit of Serial flash memory address when (CfgBootMode == 4'bx100). Indicates UART Baudrate when (CfgBootMode == 4'bx011) 0 = 19200 bps 1 = 115200 bps Indicates Serial flash memory address width when	DISD2

Name	Bit	Type	Description	Reset Value
			(CfgBootMode == 4'bx100). (CfgAlternative, CfgPARTITION) == 2'b00:16-bit address (CfgAlternative, CfgPARTITION) == 2'b01:24-bit address (CfgAlternative, CfgPARTITION) == 2'b10:25-bit address	
CfgPARTITION	[9]	R	Indicates Boot Partition on eMMC when (CfgBootMode == 4'bx101) 0 = Default Partition 1 = Boot Partition (Partition#1) Used for [0] bit of Serial flash memory address when (CfgBootMode == 4'bx100).	DISD1
CfgLATADDR	[8]	R	Static Memory Latched Address. 0 = None 1 = Latched	DISD0
CfgeMMCBootMode	[7]	R	Indicates eMMC Boot mode when (CfgBootMode == 4'bx101). 0 = Normal SD Boot 1 = eMMC Boot	SD7
CfgOTGSessionCheck	[6]	R	Indicates USB OTG Session Check when (CfgBootMode == 4'bx110). 0 = not check 1 = check	SD6
CfgICACHE	[5]	R	Indicates L1 Cache enable when (CfgBootMode ! = F). Used for CPU Instruction cache enable in the case of internal rom boot. 0 = Disable 1 = Enable	SD5
CfgDecrypt	[4]	R	Indicates AES ECB mode decrypt when (CfgBootMode ! = F) 0 = Not decrypt 1 = Decrypt	SD4
CfgNANDSELCS	[3]	R	Select nand chip 0 or 1 when (CfgBootMode == 7). 0 = nNCS[0] 1 = nNCS[1] In the case of (CfgBootMode == 4'hF), CfgNANDSELCS is ignored and nNCS[1] can be used only	SD3
CfgNANDPage	[2]	R	Indicates External nand page size when (CfgBootMode == 7). 0 = 2K or below 1 = 4K or above	SD2
CfgNANDType	[1:0]	R	Indicates External nand type when (CfgBootMode ==	2'b{SD1, SD0}

Name	Bit	Type	Description	Reset Value
			7). 0 = Small Block 3 Address 1 = Small block 4 Address 2 = Large 4 Address 3 = Large 5 Address	

4.9.1.2 Tie Off

- Base Address: 0xC001_0000

Register	Offset	Description	Reset Value
TIEOFFREG00	1000	CPU Configuration 0 Register	0x00C0_0000
TIEOFFREG01	1004	CPU Configuration 1 Register	0x1E0D_800C
TIEOFFREG02	1008	DISPLAY Configuration 0 Register	0xFDB6_C78F
TIEOFFREG03	100C	DISPLAY Configuration 1/ MCU Configuration 0 Register	0x98C1_B6C6
TIEOFFREG04	1010	MCU Configuration 1/ UART Configuration 0 Register	0x0001_FFB7
TIEOFFREG05	1014	UART Configuration 1/ USBHOST Configuration 0 Register	0x0400_83C0
TIEOFFREG06	1018	USBHOST Configuration 1 Register	0x0000_0000
TIEOFFREG07	101C	USBHOST Configuration 2 Register	0x0000_0000
TIEOFFREG08	1020	USBHOST Configuration 3 Register	0xAC00_6D00
TIEOFFREG09	1024	USBHOST Configuration 4 Register	0x3E38_0200
TIEOFFREG10	1028	USBHOST Configuration 5 Register	0x3240_0153
TIEOFFREG11	102C	USBHOST Configuration 6 Register	0x0F3A_202B
TIEOFFREG12	1030	USBOTG Configuration 0 Register	0x0000_0001
TIEOFFREG13	1034	USBOTG Configuration 1 Register	0xA000_6D00
TIEOFFREG14	1038	USBOTG Configuration 2 Register	0x3E38_0200
TIEOFFREG15	103C	USBOTG Configuration 3 Register	0x3FC0_0153
TIEOFFREG16	1040	CODA Configuration 0 Register	0x00FF_FFFF
TIEOFFREG17	1044	CODA Configuration 1 Register	0x3FFF_FFFF
TIEOFFREG18	1048	CODA Configuration 2 Register	0xFFFF_FFFF
TIEOFFREG19	104C	CODA Configuration 3 Register	0x0FFF_FFFF
TIEOFFREG20	1050	CODA Configuration 4 Register	0x1B6D_BFFF
TIEOFFREG21	1054	CODA Configuration 5 Register	0x6C86_306C
TIEOFFREG22	1058	GPU Configuration 0 Register	0xFFFE_18DB
TIEOFFREG23	105C	GPU Configuration 1 Register	0x001F_FFFF
TIEOFFREG24	1060	GPU Configuration 2 Register	0x0000_0000
TIEOFFREG25	1064	GPU Configuration 3 Register	0xFFFF_FFFF
TIEOFFREG26	1068	GPU Configuration 4 Register	0x0000_0000
TIEOFFREG27	106C	GPU Configuration 5 Register	0xFFFF_FFFF
TIEOFFREG28	1070	GPU Configuration 6 Register	0x0000_0000
TIEOFFREG29	1074	GPU Configuration 7 Register	0xFFFF_FFFF
TIEOFFREG30	1078	GPU Configuration 8 Register	0xFFFF_FFFF
TIEOFFREG31	107C	GPU Configuration 9 Register	0xFFFF_FFFF
TIEOFFREG32	1080	BUS Configuration 0 Register	0x0000_0000

NOTE: SRAM EMA signals are for chip test only. Users don't need to control those registers for normal functions.
SRAM EMA: Extra Margin Adjustment
EMA: SRAM read/write margin
EMAW: SRAM write margin
EMAS: SRAM S/A pulse width

4.9.1.2.1 TIEOFFREG00

- Base Address: 0xC001_0000
- Address = Base Address + 1000, Reset Value = 0x00C0_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	0
CA9_L1EMAW	[30:29]	RW	Cortex-A9 L1 Cache EMAW value	0
CA9_TEINIT	[28:25]	RW	Individual Cortex-A9 Processor out-of-reset default exception handling state. When set to: 0 = ARM 1 = Thumb. This pin is only sampled during reset of the processor. It sets the initial value of SCTLR.TE.	0
CA9_L2EMA	[24:22]	RW	Cortex-A9 L2 Cache EMA value	3
CA9_VINITHI	[21:18]	RW	Individual Cortex-A9 Processor control of the location of the exception vectors at reset: 0 = Exception vectors start at address 0x00000000 1 = Exception vectors start at address 0xFFFF0000. This pin is only sampled during reset of the processor. It sets the initial value of SCTLR.V.	0
CA9_CLAMPL2_1	[17]	RW	Enables L2 cache way 8 to 15 memory clamp cells	0
CA9_CLAMPL2_0	[16]	RW	Enables L2 cache way 0~7 memory clamp cells	0
CA9_L2PGEN_1	[15]	RW	Power Down Enable for L2 cache way 8 to 15	0
CA9_L2PGEN_0	[14]	RW	Power Down Enable for L2 cache way 0 to 7	0
CA9_L2RET1N_1	[13]	RW	Retention mode enable1 for L2 cache way 8 to 15	0
CA9_L2RET1N_0	[12]	RW	Retention mode enable1 for L2 cache way 0 to 7	0
CA9_L1EMAS	[11]	RW	Cortex-A9 L1 Cache EMAS value	0
CA9_L2_CFGENDIAN	[10]	RW	For L2 cache controller, big-endian mode for accessing configuration registers out of reset	0
CA9_CPU3PWRDOWN	[9]	RW	Activates CPU3 power gating cells 0 = CPU3 Active 1 = CPU3 Power Down	0
CA9_CPU2PWRDOWN	[8]	RW	Activates CPU2 power gating cells 0 = CPU2 Active 1 = CPU2 Power Down	0
CA9_CPU1PWRDOWN	[7]	RW	Activates CPU1 power gating cells 0 = CPU1 Active 1 = CPU1 Power Down	0
CA9_CPU0PWRDOWN	[6]	RW	Activates CPU0 power gating cells 0 = CPU0 Active 1 = CPU0 Power Down	0
CA9_COREPWRDOWN	[5]	RW	Activates Cortex-A9 QAUD power gating cells	0

Name	Bit	Type	Description	Reset Value
			0 = Cortex-A9 Quad Active 1 = Cortex-A9 Quad Power Down	
CA9_CLAMPCPU3	[4]	RW	Enables CPU3 output port clamp cells	0
CA9_CLAMPCPU2	[3]	RW	Enables CPU3 output port clamp cells	0
CA9_CLAMPCPU1	[2]	RW	Enables CPU3 output port clamp cells	0
CA9_CLAMPCPU0	[1]	RW	Enables CPU3 output port clamp cells	0
CA9_CLAMPCOREOUT	[0]	RW	Enables the Cortex-A9 QAUD output port clamp cells	0

4.9.1.2.2 TIEOFFREG01

- Base Address: 0xC001_0000
- Address = Base Address + 1004, Reset Value = 0x1E0D_800C

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	RW	Reserved	0
RSVD	[29:27]	RW	Reserved	3
AXISRAM_NSLEEP	[26]	RW	AXISRAM SRAM retention (low active)	1
AXISRAM_NPOWERDOWN	[25]	RW	Reserved	1
AXISRAM_RA2W_EMAWB	[24:23]	RW	AXISRAM EMAWB value	0
AXISRAM_RA2W_EMAWA	[22:21]	RW	AXISRAM EMAWA value	0
AXISRAM_RA2W_EMAB	[20:18]	RW	AXISRAM EMAB value	3
AXISRAM_RA2W_EMAA	[17:15]	RW	AXISRAM EMAA value	3
CA9_PWRCTLI2	[14:13]	RW	Reset value for CPU2 status register [3:2]	0
CA9_PWRCTLI1	[12:11]	RW	Reset value for CPU1 status register [3:2]	0
CA9_PWRCTLI0	[10:9]	RW	Reset value for CPU0 status register [1:0]	0
CA9_CPUCLKOFF	[8:5]	RW	Activates individual processor clock gating cells 0 = Clock is enabled 1 = Clock is stopped	0
CA9_L1EMA	[4:2]	RW	Cortex-A9 L1 Cache EMA value	3
CA9_L2EMAW	[1:0]	RW	Cortex-A9 L2 Cache EMAW value	0

4.9.1.2.3 TIEOFFREG02

- Base Address: 0xC001_0000
- Address = Base Address + 1008, Reset Value = 0xFDB6_C78F

Name	Bit	Type	Description	Reset Value
HDMI_NSLEEP	[31:30]	RW	HDMI SRAM retention (low active)	3
RESERVED	[29:28]	RW		3
RESCONV_NSLEEP	[27]	RW	Resolution Converter SRAM retention (low active)	1
RESERVED	[26]	RW		1
DEINTER_RF2W_EMAB	[25:23]	RW	De-Interlacer RF2W SRAM EMAB value	3
DEINTER_RF2W_EMAA	[22:20]	RW	De-Interlacer RF2W SRAM EMAA value	3
DEINTER_RF2_EMAB	[19:17]	RW	De-Interlacer RF2 SRAM EMAB value	3
DEINTER_RF2_EMAA	[16:14]	RW	De-Interlacer RF2 SRAM EMAA value	3
DEINTER_RF1_EMAW	[13:12]	RW	De-Interlacer RF1 SRAM EMAW value	0
DEINTER_RF1_EMA	[11:9]	RW	De-Interlacer RF1 SRAM EMA value	3
RESERVED	[8]	RW		1
RESERVED	[7]	RW		1
RESERVED	[6:5]	RW		0
RESERVED	[4:2]	RW		3
RESERVED	[1]	RW		1
RESERVED	[0]	RW		1

4.9.1.2.4 TIEOFFREG03

- Base Address: 0xC001_0000
- Address = Base Address + 100C, Reset Value = 0x98C1_B6C6

Name	Bit	Type	Description	Reset Value
DREX_DFI_RESET_N_P0	[31]	RW	DFI reset signal. Reset value for dfi_reset_n_pN[1:0] are 1. These signals areonly required for DDR3 support. dfi_reset_n_p0/p1 is connected to io_reset_out.	1
DREX_CTRL_HCKE	[30]	RW	This signal decides the reset value of CKE and some signals. If this bit is set, reset value of io_cke_out is 1. Otherwise, reset value of them is 0.	0
DREX_PEREV_TRIGGER	[29]	RW	DERX Performance Event Trigger Enable bit 0x0 = disables all counters including CCNT 0x1 = enables all counters including CCNT When you read it, 1 means it's counting and 0 means it's idle(stop counting). You can write it only when the start mode is set to be 0(PPMU is started by CPU). At this time, you can write this bit by 1 to start counting	0

Name	Bit	Type	Description	Reset Value
			and write it by 0 to stop the counting. When the start mode is set to be 1(PPMU is started by SYSCON), you only can read it and get the status of the PPMU. At this time PPMU is controlled by external trigger. When external trigger is 1, counting starts, and when external trigger is 0, counting stops.	
DREX_PAUSE_REQ	[28]	RW	DREX-1 supports pause feature through external ports called "PAUSE_REQ" and "PAUSE_ACK". When PAUSE_ACK is set to low, DREX-1 guarantees that there will be no requests issued to the DRAM until the external port PAUSE_REQ is driven to high. This feature is used for switching the clock frequency of the memory interface. Clock frequency change of memory can be applied through this pause feature like below procedures. Pause request setting PAUSE_REQ to low. DREX-1 sets AxREADY to low. DREX-1 finishes memory access until queue empty. DREX-1 sets PAUSE_ACK to low. Clock frequency changes. Release pause request setting PAUSE_REQ to high. DREX-1 sets AxREADY and PAUSE_ACK to high. Master side of this protocol should not change PAUSE_REQ value before finishing previous handshaking. It means that PAUSE_REQ should be waiting for the PAUSE_ACK before change its value.	1
DREX_CSYSREQ	[27]	RW	AXI Low power interface Request signal.	1
DREX_CA_SWAP	[26]	RW	DREX-1 has an input signal named ca_swap. If this signal is driven to 1, the DFI interface's address signals will have its bit locations reversed. (addr[9] and addr[0] will be swapped, addr[8] and addr[1] will be swapped, etc) The purpose of this signal is for supporting different packaging solutions, so that the system level designer can choose among one of the modes depending on the routing requirement of the packaging or the PCB using the SoC with DREX-1. Please take care since driving the wrong ca_swap value may render the whole SoC unusable! The ca_swap feature is only valid on LPDDR2/LPDDR3 modes, and has no effect on DDR3 modes.	0
DREX_CKE_INIT	[25]	RW	DREX CKE signal initialization. It sets the state of CKE[MEMORY_CHIPS-1:0] when resetn is de-asserted. The default value is set by the state of cke_init, when resetn goes HIGH.	0
VROM_EMA	[24:22]	RW	ROM EMA value	3
DISPLAY_DPSRAM_EMA	[21:20]	RW	DISPLAY SRAM EMAWB value	0

Name	Bit	Type	Description	Reset Value
WB				
DISPLAY_DPSRAM_EMAWA	[19:18]	RW	DISPLAY SRAM EMAWA value	0
DISPLAY_DPSRAM_EMAB	[17:15]	RW	DISPLAY SRAM EMAB value	3
DISPLAY_DPSRAM_EMAA	[14:12]	RW	DISPLAY SRAM EMAA value	3
DISPLAY_DPSRAM_1R1W_EMAB	[11:9]	RW	DISPLAY SRAM EMAB value	3
DISPLAY_DPSRAM_1R1W_EMAA	[8:6]	RW	DISPLAY SRAM EMAA value	3
DISPLAY_SPSRAM_EMAW	[5:4]	RW	DISPLAY SRAM EMAW value	0
DISPLAY_SPSRAM_EMA	[3:1]	RW	DISPLAY SRAM EMA value	3
HDMI_PHY_REFCLK_SEL	[0]	RW	Reference Clock Selection. REFCLK_SEL is used for PHY reference clock selection. REFCLK_SEL = 1'b0: CLKI REFCLK_SEL = 1'b1: INT_CLK	0

4.9.1.2.5 TIEOFFREG04

- Base Address: 0xC001_0000
- Address = Base Address + 1010, Reset Value = 0x0001_FFB7

Name	Bit	Type	Description	Reset Value
UART3_SMCRXENB	[31]	RW	SmartCard Interface RX mode enable	0
UART3_SMCTXENB	[30]	RW	SmartCard Interface TX mode enable	0
UART3_USESMC	[29]	RW	Use UART for SmartCard Interface	0
UART2_SMCRXENB	[28]	RW	SmartCard Interface RX mode enable	0
UART2_SMCTXENB	[27]	RW	SmartCard Interface TX mode enable	0
UART2_USESMC	[26]	RW	Use UART for SmartCard Interface	0
UART1_SMCRXENB	[25]	RW	SmartCard Interface RX mode enable	0
UART1_SMCTXENB	[24]	RW	SmartCard Interface TX mode enable	0
UART1_USESMC	[23]	RW	Use UART for SmartCard Interface	0
UART0_SMCRXENB	[22]	RW	SmartCard Interface RX mode enable	0
UART0_SMCTXENB	[21]	RW	SmartCard Interface TX mode enable	0
UART0_USESMC	[20]	RW	Use UART for SmartCard Interface	0
SCALER_EMAW	[19:18]	RW	SCALER SRAM EMAW value	0
SCALER_EMA	[17:15]	RW	SCALER SRAM EMA value	3
MIPI_NSLEEP	[14:11]	RW	MIPI SRAM retention (low active)	F
RESERVED	[10:7]	RW		F
MIPI_DPSRAM_1R1W_EMAB	[6:4]	RW	MIPI SRAM EMAB value	3
MIPI_DPSRAM_1R1W_EMAA	[3:1]	RW	MIPI SRAM EMAA value	3
DREX_DFI_RESET_N_P1	[0]	RW	DFI reset signal. Reset value for dfi_reset_n_pN[1:0] are 1. These signals are only required for DDR3 support. dfi_reset_n_p0/p1 is connected to io_reset_out.	1

4.9.1.2.6 TIEOFFREG05

- Base Address: 0xC001_0000
- Address = Base Address + 1014, Reset Value = –

Name	Bit	Type	Description	Reset Value
HOST_phy_vstatus_0	[31:29]	RW	Vendor Status	0
HOST_SS_RESUME_UTMI_PLS_DIS	[28]	RW	Resume Disable Function: This signal is valid only if ss_utmi_backward_enb_i is tied low. ss_resume_utmi_pls_dis_i controls the Resume termination sequence. If ss_resume_utmi_pls_dis_i is tied low, then the EHCI simultaneously switches term_sel[1:0] to 2'b00 and xver_sel to 1'b0. This transition occurs if either of the following two conditions is satisfied: SE0 is detected online_state or 255 PHY clocks elapse after tx valid is de-asserted. Ifss_resume_utmi_pls_dis_i is tied high, at the end of resume, tx valid is de-asserted and term_sel[1:0] is switched simultaneously to 2'b00. At this point, xver_sel is still high. After line_state is SE0 or if 255 PHY clocks elapse after tx valid is de-asserted, xver_sel switches to 1'b0. NOTE: For interfacing with ULPI PHY or UTMI+ PHY set ss_resume_utmipls_dis_i == 0 Active State: High	0
HOST_SS_UTMI_BACKWARD_ENB	[27]	RW	UTMI Backward Enable Function: This signal controls the Resume termination sequence as follows: When this signal is tied high, term_sel is switched to high-speed when tx valid is de-asserted. Before the xver_sel signal is switched to high speed, one of the following two conditions should to be met: 2 us of SE0 is detected on line_state 255 PHY clocks elapse after txvalid is de-asserted When this signal is tied low, then it is used together with the strap signal ss_resume_utmi_pls_dis_i and the behavior of USB 2.0 Host is described in detail under strap signal ss_resume_utmi_pls_dis_i. The switching of term_sel is done first followed by xver_sel to create EOP as part of resume sequence. Since the term_sel which is xver_sel forUTMI+ PHY is switched during the last byte of transmit data (for sending resume, data is transmitted with bit stuff and NRZ disable) is coming on USB as garbage data and the device does not see a clean EOP for the resume sequence. NOTE: This signal is valid only if the USB 2.0 Host controller is interfaced to Synopsys PHY. If you use any third party PHY, then this signal needs to be tied	0

Name	Bit	Type	Description	Reset Value
			low. NOTE: For interfacing with ULPI PHY or UTMI+ PHY, set ss_utmi_backward_enb_i == 0 Active State: High	
HOST_SS_WORD_IF	[26]	RW	Word Interface Function: Selects the data width of the UTMI/UTMI+ PHY interface. 1'b1: 16 -bit interface 1'b0: 8-bit interface Note: In ULPI mode, unless the 16-bit ULPI adapter is selected, you cannot set ss_word_if_i interface to 16-bit mode. In 8-bit ULPI mode, ss_word_if_i must be tied to 0. In 16-bit ULPI mode, the ss_word_if_i must reflect same value asulpi_mode16_en_i on page 97. When ulpi_mode16_en_i is tied to 0, then ss_word_if_i must also be tied to 0. In 16-bit ULPI mode, when ulpi_mode16_en_i is tied to 1, then ss_word_if_i must also be tied to 1. Active State: High	1
HOST_SS_WORD_IF_ENB	[25]	RW	Use Tieoff register value instead of controller value	0
HOST_HSIC_480M_FROM_OTG_PHY	[24]	RW	Select HSIC PHY 480M clock 0 : PLL clock 1 : HOST PHY output clock	0
HOST_HSIC_FREE_CLOCK_ENB	[23]	RW	Select free clock of HSIC LINK. 0 : HOST PHY free clock 1 : HSIC PHY free clock	0
HOST_NHOSTHSICRESETSYNC	[22]	RW	Reset off HSIC LINK	0
HOST_NHOSTUTMIRESETSYNC	[21]	RW	Reset off UTMI clock of HOST LINK	0
HOST_NHOSTPHYRESETSYNC	[20]	RW	Reset off PHY clock of HOST LINK	0
HOST_NAUXWELLRESETSYNC	[19]	RW	Reset off Aux Well of HOST LINK	0
HOST_NRESETSYNC_OHCI	[18]	RW	Reset off OHCI of HOST LINK	0
HOST_NRESETSYNC	[17]	RW	Sleep off OTG RAM	0
HOST_HSIC_EN	[16:14]	RW	Description: HSIC into UTMI+ Interface Enable Function: This input pin exists only if the HSIC feature is enabled during core Consultant configuration. The width of this pin is 'UHC2_N_PORTS, the number of EHCI PHY ports in the host controller. Each pin is associated with its port number. 0 = When this pin is tied low, it indicates that the	2

Name	Bit	Type	Description	Reset Value
			associated port does not support HSIC. 1 = When this pin is tied high, it indicates that the associated port supports HSIC. The pin has to be tied to a valid value. This pin helps maintain backward compatibility of the controller for the HSIC feature per port. This pin is quasi static, that is, it doesn't change during a session and has to be tied to stable value (preferably) from power-on. If this pin is external to the core through registers, it must be stable before the enumeration of the port begins (before the AHB reset). This signal is implemented in one of two ways. • If heterogeneous ports is not selected during core Consultant configuration, this bussed input port should be driven to the same value homogeneously externally to the controller. • If heterogeneous ports is selected during core Consultant configuration, its width is still UHC2_N_PORTS, each bit is associated to a port in contiguous order, and each strap pin can independently and asynchronously enable HSIC per port. NOTE: This pin will be constrained as a false path from this input. It will be constrained from the AHB clock domain and end up being used in the UTMI+ clock domain. However, since the use model is quasi-static, this should not be an issue related to clock domain crossing. Active State: High	
HOST_SYS_INTERRUPT	[13]	RW	System Interrupt, system error indication to host controller only for non-AHB errors. Function: DWC_h20ahb detects an error condition on the AHB and takes the appropriate action. In addition to AHB error conditions, this signal is active when any fatal error occurs during a host system access involving the controller. In order for the host to detect this signal, the minimum signal duration is at least one AHB clock pulse (hclk_i). In PCI-based design, fatal (not recoverable) PCI bus errors are: Target Abort Address Parity Error Master Abort NOTE: That when the EHCI and OHCI Host Controllers sample this signal asserted, the controllers are halted to prevent further execution of the scheduled descriptors and send a host System Error	0

Name	Bit	Type	Description	Reset Value
			interrupt. The EHCI and OHCI Host Controllers do not process any lists until the corresponding Host Controller Driver clears the corresponding error Active State: High	
HOST_NX_RF1_EMAW	[12:11]	RW	USB2.0 HOST SRAM EMAW value	0
HOST_NX_RF1_EMA	[10:8]	RW	USB2.0 HOST SRAM EMA value	3
HOST_NSLEEP	[7]	RW	USB2.0 HOST SRAM retention (low active)	1
HOST_NPOWERDOWN	[6]	RW	Power Down off OTG RAM	1
RESERVED	[5]	RW		0
RESERVED	[4]	RW		0
RESERVED	[3]	RW		0
UART4_SMCRXENB	[2]	RW	SmartCard Interface RX mode enable	0
UART4_SMCTXENB	[1]	RW	SmartCard Interface TX mode enable	0
UART4_USESMC	[0]	RW	Use UART for SmartCard Interface	0

4.9.1.2.7 TIEOFFREG06

- Base Address: 0xC001_0000
- Address = Base Address + 1018, Reset Value = –

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	0
HOST_SS_SIMULATION_MODE	[30]	RW	Simulation Mode Function: When set to 1'b1, this bit sets the PHY in a non-driving mode so the EHCI can detect device connection. This signal is used only for simulation. Active State: High	0
HOST_APP_PRT_OVRCUR	[29:27]	RW	Port Over current Indication From Application Function: When asserted by the application, the corresponding port enters Disable state. This signal controls both EHCI and OHCI controller port state machines. Depending on ownership of the port, the corresponding EHCI or OHCI controller generates an Over current Detect interrupt. NOTE: That you must implement over current detection logic and provide input to the host. When an over current condition exists, port power remains on. Use the over current condition to control the port power. Active State: High	0
HOST_SS_NEXT_POWER_STATE	[26:25]	RW	Next Power Management State Function: Power management for the next state output from PCI.	0

Name	Bit	Type	Description	Reset Value
			Active State: High	
HOST_SS_POWER_STATE	[24:23]	RW	Power Management Function: Power management for the current state output from PCI. Active State: High	0
HOST_SS_NXT_POWER_STATE_VALID	[22]	RW	Next Power Management State Valid Function: Due to the difference between the host AHB and the PCI clocks, the ss_next_power_state_i may not be in the correct state when input to the host controller. Therefore, ss_nxt_power_state_valid_i is used (as asynchronization signal) to validate the ss_next_power_state_i signal. When this signal is asserted, the ss_next_power_state_i input is valid. Active State: High	0
HOST_SS_POWER_STATE_VALID	[21]	RW	Power State Valid Function: Active high input qualifier signal for ss_power_state_i. Active State: High	0
HOST_phy_vstatus_7	[20:18]	RW	Vendor Status	0
HOST_phy_vstatus_6	[17:15]	RW	Vendor Status	0
HOST_phy_vstatus_5	[14:12]	RW	Vendor Status	0
HOST_phy_vstatus_4	[11:9]	RW	Vendor Status	0
HOST_phy_vstatus_3	[8:6]	RW	Vendor Status	0
HOST_phy_vstatus_2	[5:3]	RW	Vendor Status	0
HOST_phy_vstatus_1	[2:0]	RW	Vendor Status	0

4.9.1.2.8 TIEOFFREG07

- Base Address: 0xC001_0000
- Address = Base Address + 101C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HOST_OHCI_0_APP_IRQ12	[31]	RW	External Interrupt 12 Function: This external keyboard controller interrupt 12 causes an emulation interrupt. Active State: High	0
HOST_OHCI_0_APP_IRQ1	[30]	RW	External Interrupt 1 Function: This external keyboard controller interrupt 1 causes an emulation interrupt. Active State: High	0
HOST_OHCI_0_CNTSEL_N	[29]	RW	Count Select Function: Selects the counter value for simulation or real time for 1ms.	0

Name	Bit	Type	Description	Reset Value
			1'b0: Count full 1 ms 1'b1: Simulation time Active State: Low	
HOST_SS_ENA_INCRX_ALIGN	[28]	RW	Burst Alignment Enable Function: Forces AHB master to start INCR4/8/16 busts only on burst boundaries. AHB requires that double word width burst be addressed aligned only to the double-word boundary. 1'b1: Start INCRX burst only on burst x-aligned addresses 1'b0: Normal AHB operation; start bursts on any double word boundary NOTE: When this function is enabled, the burst are started only when the lowest bits of haddr are: • INCR4: haddr[3:0] == 4'b0000 • INCR8: haddr[4:0] == 5'b00000 • INCR16: haddr[5:0] == 6'b000000 Active State: High	0
HOST_SS_ENA_INCR4	[27]	RW	AHB Burst Type INCR4 Enable Function: Enables the AHB master interface to utilize burst INCR8 when appropriate. 1'b1: Use INCR4 when appropriate 1'b0: Do not use INCR4; use other enabled INCRX bursts or un specified length burst INCR NOTE: The AHB INCRX enhancement must be enabled (during configuration) to utilize INCR4. If not, then this strap has no effect. The OHCI part of the controller only supports INCR4 or SINGLE. Active State: High	0
HOST_SS_ENA_INCR8	[26]	RW	AHB Burst Type INCR8 Enable Function: Enables the AHB master interface to utilize burst INCR8 when appropriate. 1'b1: Use INCR8 when appropriate 1'b0: Do not use INCR8; use other enabled INCRX bursts or un specified length burst INCR NOTE: The AHB INCRX enhancement must be enabled (during configuration) to utilize INCR8. If not, then this strap has no effect. The OHCI does not support INCR8. Active State: High	0
HOST_ss_ena_incr16	[25]	RW	AHB Burst Type INCR16 Enable Function: Enables the AHB master interface to utilize burst INCR16 when appropriate. 1'b1: Use INCR16 when appropriate 1'b0: Do not use INCR16; use other enabled INCRX bursts or unspecified length burst INCR	0

Name	Bit	Type	Description	Reset Value
			Note: The AHB INCRX enhancement must be enabled (during configuration) to utilize INCR16. If not, then this strap has no effect. The OHCI does not support INCR16. Active State: High	
HOST_SS_AUTOPPD_ON_OVERCUR_EN	[24]	RW	Auto Port Power Disable on Over current Function: This strap signal enables automatic port power disable in the host controller. When this signal is active, if an over-current condition is detected on a powered port and PPC is 1, the PP bit in each affected port is automatically transitioned by the host controller from a 1 to 0, removing power from the port. NOTE: If this strap signal is not high, then the software needs to disable port power when an over current condition occurs. Active State: High	0
HOST_SS_FLADJ_VAL_0	[23:21]	RW	Frame Length Adjustment Register for Port 0 Function: This feature adjusts the frame length of the micro frame per port. This value must be the same as that of ss_fladj_val_host_i, or the EHCI yields undefined results. See ss_fladj_val_host_i for the adjustment value. Active State: High	0
HOST_SS_FLADJ_VAL_1	[20:18]	RW	Frame Length Adjustment Register for Port 1 Function: This feature adjusts the frame length of the micro frame per port. This value must be the same as that of ss_fladj_val_host_i, or the EHCI yields undefined results. See ss_fladj_val_host_i for the adjustment value. Active State: High	0
HOST_SS_FLADJ_VAL_2	[17:15]	RW	Frame Length Adjustment Register for Port 2 Function: This feature adjusts the frame length of the micro frame per port. This value must be the same as that of ss_fladj_val_host_i, or the EHCI yields undefined results. See ss_fladj_val_host_i for the adjustment value. Active State: High	0
HOST_SS_FLADJ_VAL_3	[14:12]	RW	Frame Length Adjustment Register for Port 3 Function: This feature adjusts the frame length of the micro frame per port. This value must be the same as that of ss_fladj_val_host_i, or the EHCI yields undefined results. See ss_fladj_val_host_i for the adjustment value. Active State: High	0
HOST_SS_FLADJ_VAL_4	[11:9]	RW	Frame Length Adjustment Register for Port 4 Function: This feature adjusts the frame length of the micro frame per port. This value must be the same as	0

Name	Bit	Type	Description	Reset Value
			that of ss_fladj_val_host_i, or the EHCI yields undefined results. See ss_fladj_val_host_i for the adjustment value. Active State: High	
HOST_SS_FLADJ_VAL_5	[8:6]	RW	Frame Length Adjustment Register for Port 5 Function: This feature adjusts the frame length of the micro frame per port. This value must be the same as that of ss_fladj_val_host_i, or the EHCI yields undefined results. See ss_fladj_val_host_i for the adjustment value. Active State: High	0
HOST_SS_FLADJ_VAL_HOST	[5:0]	RW	Frame Length Adjustment Register Function: This feature adjusts any offset from the clock source that drives the µSOF counter. The µSOF cycle time (number of µSOF counter clock periods to generate a µSOF micro frame length) is equal to 59,488 plus this value. The default value is decimal 32 (0x20), which gives an SOF cycle time of 60,000 (each micro frame has 60,000 bit times). Frame Length (decimal) FLADJ Value (decimal) 59488 0 (0x00) 59504 1 (0x01) 59520 2 (0x02) … … 59984 31 (0x1F) 60000 32 (0x20) … … 60496 63 (0x3F) NOTE: That this register must be modified only when the HC Halted bit in the USBSTS register is set to 1; otherwise, the EHCI yields undefined results. The register must not be reprogrammed by the USB system software unless the default or BIOS programmed values are incorrect, or the system is restoring the register while returning from a suspended state. Connect this signal to value 0x20 (32 decimal) for no offset. Active State: High	0

4.9.1.2.9 TIEOFFREG08

- Base Address: 0xC001_0000
- Address = Base Address + 1020, Reset Value = 0xAC00_6D00

Name	Bit	Type	Description	Reset Value
HOST_SLEEPM	[31]	RW	Sleep Assertion Function: Asserting this signal places the USB 2.0 picoPHY in Sleep mode according to the USB 2.0 Link Power Management (LPM) addendum to the USB2.0 specification. In Sleep Mode, the transmitter is tri-stated and the USB 2.0picoPHY circuits are powered down except for the XO block If the reference clock isa crystal, the XO block remains powered when the USB 2.0 picoPHY is placed in Sleep mode. 0 = Sleep mode 1 = Normal operating mode If SUSPENDM0 is set to 1'b0, the USB 2.0 picoPHY will remain in Suspend mode irrespective of the SLEEPM0 setting. If the LPM function is not required, SLEEPM0 must be tied to DVDD. USB 2.0picoPHY Sleep mode can be overridden using the test interface. Voltage Range: 0 V-DVDD Active State: Low	1
HOST_SLEEPM_ENB	[30]	RW	Use Tieoff register value instead of controller value	0
HOST_SUSPENDM	[29]	RW	Suspend Assertion Function: Asserting this signal suspends the USB 2.0 picoPHY by tri-stating the transmitter and powering down the USB 2.0 picoPHY circuits. 0 = Suspend mode 1 = Normal operating mode USB 2.0 picoPHY power-down behavior can be overridden using the test interface. Voltage Range: 0 V-DVDD Active State: Low	1
HOST_SUSPENDM_ENB	[28]	RW	Use Tieoff register value instead of controller value	0
HOST_DMPULLDOWN	[27]	RW	D- Pull-Down Resistor Enable Function: This controller signal controls the pull-down resistance on the D- line. 0 = The pull-down resistance on D- is disabled 1 = The pull-down resistance on D- is enabled When an A/B device is acting as a host (downstream-facing port), DPPULLDOWN0 and DMPULLDOWN0 are enabled. NOTE: UTMI+/OTG-compliant controllers are not allowed to toggleDPPULLDOWN0 and	1

Name	Bit	Type	Description	Reset Value
			DMPULLDOWN0 during normal operation. Voltage Range: 0 V-DVDD Active State: High	
HOST_DPPULLDOWN	[26]	RW	D+ Pull-Down Resistor Enable Function: This controller signal controls the pull-down resistance on the D+ line. 0 = The pull-down resistance on D+ is disabled 1 = The pull-down resistance on D+ is enabled When an A/B device is acting as a host (downstream-facing port),DPPULLDOWN0 and DMPULLDOWN0 are enabled. Note: UTMI+/OTG-compliant controllers are not allowed to toggleDPPULLDOWN0 and DMPULLDOWN0 during normal operation. Voltage Range: 0 V-DVDD Active State: High	1
HOST_VBUSVLDEXTSEL	[25]	RW	External VBUS Valid Select Function: This signal selects either the VBUSVLDEXT0 input or the internal Session Valid comparator to generate the OTGSESSVLD0 output. To avoid potential glitches in DP0, VBUSVLDEXTSEL0 must be static prior to a power-on reset and remain static during normal operation. The OTGSESSVLD0 signal, in conjunction with XCVRSEL0[1:0],OPMODE0[1:0], TERMSEL0, DPPULLDOWN0, and DMPULLDOWN0,control the DP0 pull-up resistor. If VBUSVLDEXT0 and the internal Session Valid comparator output are asserted, and VBUSEXTSEL0changes, it is possible for OTGSESSVLD0 to glitch low, causing the DP0resistor to be temporarily disabled. 0 = The internal Session Valid comparator is used to generateOTGSESSVLD0 and assert the DP0 pull-up resistor. 1 = The VBUSVLDEXT0 input is used to generate OTGSESSVLD0 and assert the DP0 pull-up resistor This signal is not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: High	0
HOST_VBUSVLDEXT	[24]	RW	External VBUS Valid Indicator Function: This signal is valid in Device mode and only when theVBUSVLDEXTSEL0 signal is set to 1'b1. VBUSVLDEXT0 indicates whether the VBUS signal on the USB cable is valid. In addition, VBUSVLDEXT0	0

Name	Bit	Type	Description	Reset Value
			enables the pull-up resistor on the D+ line. 0 = The VBUS signal is not valid, and the pull-up resistor on D+ is disabled. 1 = The VBUS signal is valid, and the pull-up resistor on D+ is enabled In Host mode, this input is not used and can be tied to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	
HOST_ADPPRBENB	[23]	RW	ADP Probe Enable Function: Enables/disables the ADP Probe comparator. 0 = ADP Probe comparator is disabled 1 = ADP Probe comparator is enabled If this signal is not used, tie it to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_ADPDISCHRG	[22]	RW	VBUS Input ADP Discharge Enable Function: Controls discharging the VBUS input during ADP. 0 = Disables discharging VBUS during ADP. 1 = Enables discharging VBUS during ADP. If this signal is not used, tie it to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_ADPCHRG	[21]	RW	VBUS Input ADP Charge Enable Function: Controls charging the VBUS input during ADP. 0 = Disables charging VBUS during ADP. 1 = Enables charging VBUS during ADP. If this signal is not used, tie it to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_DRVVBUS	[20]	RW	Drive VBUS Function: This controller signal controls the VBUS Valid comparator. Thissignal drives 5 V on VBUS through an external charge pump. When OTGDISABLE0 is set to 1'b0 and DRVVBUS0 is asserted, theBandgap circuitry and VBUS Valid comparator are powered, even inSuspend or Sleep mode. 0 = The VBUS Valid comparator is disabled. 1 = The VBUS Valid comparator is enabled. Voltage Range: 0 V-DVDD Active State: High	0

Name	Bit	Type	Description	Reset Value
HOST_IDPULLUP	[19]	RW	Analog ID Input Sample Enable Function: This controller signal controls ID line sampling. 0 = ID pin sampling is disabled, and the IDDIG0 output is not valid. 1 = ID pin sampling is enabled, and the IDDIG0 output is valid. Voltage Range: 0 V-DVDD Active State: High	0
HOST_LOOPBACKENB	[18]	RW	Loopback Test Enable Function: This signal places the USB 2.0 picoPHY in Loopback mode, which enables the receive and transmit logic concurrently. 0 = During data transmission, the receive logic is disabled. 1 = During data transmission, the receive logic is enabled. NOTE: Loopback mode is for test purposes only; it cannot be used for normal operation. In normal operation, tie this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_OTGDISABLE	[17]	RW	OTG Block Disable Function: This signal powers down the VBUS Valid comparator, but not the Session Valid comparator, ADP probe and sense comparators, nor the ID detection circuitry. To save power, if the application does not use the OTG function, this input can be set high. 0 = The OTG block is powered up. 1 = The OTG block is powered down. Voltage Range: 0 V-DVDD Active State: High	0
HOST_PORTRESET	[16]	RW	Per-Port Reset Function: When asserted, this signal resets the corresponding port's transmit and receive logic without disabling the clocks within the USB 2.0 picoPHY. 0 = The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK0 cycles. 1 = The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. Asserting PORTRESET0 does not override any USB 2.0 picoPHY inputs that normally control the USB	0

Name	Bit	Type	Description	Reset Value
			state, nor does it cause any transient, illegal USB states. Within 100 ns of asserting PORTRESET0, the controller must set the inputs that control the USB to values that cause a safe state. A safe state for Host and Device modes is defined as follows: • Host mode: Non-driving (OPMODE0[1:0] = 2'b01) with the 15 kΩ pull-down resistors enabled (DPPULLDOWN0 and DMPULLDOWN0 = 1'b1) • Device mode: Non-driving (OPMODE0[1:0] = 2'b01) with the 1.5 kΩ pull-up resistor disabled Voltage Range: 0 V-DVDD Active State: High	
HOST_RESREQIN	[15]	RW	Reserved Function: Reserved. Tie this pin to 1'b0. Voltage Range: 0 V-DVDD	0
HOST_COMMONONN	[14]	RW	Common Block Power-Down Control Function: This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 picoPHY is in Suspend, or Sleep mode. 0 = In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered. 1 = In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. NOTE: 1. If COMMONONN is set low, CLK48MOHCI and CLK480M remain available in Suspend or UART/Auto resume mode. 2. If the reference clock source is a crystal, CLK12MOHCI remains available in Suspend or UART/Auto resume mode, only if COMMONONN is set to 1'b0. 3. If the reference clock source is either an external clock (connected to XO) or CLKCORE, CLK12MOHCI will continue to pulse in Suspend or UART/Auto resume mode, even when COMMONONN is set to 1'b1. 4. In Sleep mode, CLK48MOHCI and CLK12MOHCI	1

Name	Bit	Type	Description	Reset Value
			are always available, irrespective of COMMONONN. Voltage Range: 0 V-DVDD Active State: Low	
HOST_FSEL	[13:11]	RW	Reference Clock Frequency Select Function: Selects the USB 2.0 picoPHY reference clock frequency. 000 = 9.6 MHz 001 = 10 MHz 010 = 12 MHz 011 = 19.2 MHz 100 = 20 MHz 101 = 24 MHz 110 = Reserved 111 = 50 MHz Voltage Range: 0 V-DVDD Active State: N/A	5
HOST_REFCLKSEL	[10:9]	RW	Reference Clock Select for PLL Block Function: This signal selects the reference clock source for the PLL block. 00 = The XO block uses the clock from a crystal. 01 = The XO block uses an external, 1.8-V clock supplied on the XO pin. 10 = The PLL uses CLKCORE as reference. 11 = Reserved This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: N/A	2
HOST_POR	[8]	RW	Power-On Reset Function: This signal resets all test registers and state machines in the USB 2.0picoPHY. The POR signal must be asserted for a minimum of 10 µs. Voltage Range: 0 V-DVDD Active State: High	1
HOST_POR_ENB	[7]	RW	Use Tieoff register value instead of controller value	0
HOST_VATESTENB	[6:5]	RW	Analog Test Pin Select Function: Enables analog test voltages to be placed on either the ANALOGTEST or ID0 pin. 00 = Analog test voltages cannot be viewed or applied on either ANALOGTEST or ID0. 01 = Analog test voltages can be viewed or applied on	0

Name	Bit	Type	Description	Reset Value
			ID0. 10 = Analog test voltages can be viewed or applied on ANALOGTEST. 11 = Reserved. Invalid setting. If this bus is not used, tie these inputs low. Voltage Range: 0 V-DVDD Active State: N/A	
HOST_SIDDQ	[4]	RW	IDDQ Test Enable Function: This test signal enables you to perform IDDQ testing by powering downall analog blocks. Before asserting SIDDQ, ensure that VDATSRCENB0, VDATDETENB0, DCDENB0, BYPASSSEL0, ADPPRBENB0, and TESTBURNIN are set to 1'b0. 0 = The analog blocks are powered up. 1 = The analog blocks are powered down. If this signal is not used, tie it low. Voltage Range: 0 V-DVDD Active State: High	0
HOST_OHCI_SUSP_LGCY	[3]	RW	OHCI Clock control signal Function: This is a static strap signal. • When tied HIGH and the USB port is owned by OHCI, the signal utmi_suspend_o_n reflects the status of the USB port: (suspended or not suspended). • When tied LOW and the USB port is owned by OHCI, then utmi_suspend_o_n asserts (0) if all the OHCI ports are suspended, or if the OHCI is in global suspend state (HCFS = USBSUSOPEND). utmi_suspend_o_n de-asserts (1) if any of the OHCI ports are not suspended and OHCI is not in global suspend. Note: This strap must be tied low if the OHCI 48/12 MHz clocks must be suspended when the EHCI and OHCI controllers are not active. Active State: NA	0
HOST_APP_START_CLK	[2]	RW	OHCI Clock control signal Function: This is an asynchronous primary input to the host core. When the OHCI clocks are suspended, the system has to assert this signal to start the clocks (12 and 48 MHz). This should be de-asserted after the clocks are started and before the host is suspended again. (Host is suspended means HCFS = SUSPEND or all the OHCI ports are suspended). Active State: High	0

Name	Bit	Type	Description	Reset Value
HOST_SS_HUBSETUP_MIN	[1]	RW	Hub setup time control signal Function: This is static strap signal. Some FS devices down the hub do not recover properly after a pre-amble packet, directed at other LS device, if the hub setup time is four FS clocks. Four FS clocks just meet the specification. By adding one extra clock, these FS devices are made to work better. This strap selects four or five FS clocks as hub setup time for interoperability with the various devices. It is recommended to tie low, that is, for five FS clocks. • When tied HIGH, four FS clocks of hub setup time is used. • When tied LOW, five FS clocks of hub setup time is used. Active State: NA	0
HOST_OHCI_0_APP_IO_HIT	[0]	RW	Application I/O Hit Function: This signal indicates a PCI I/O cycle strobe. (This signal is relevant only when using a PCI controller.) Active State: High	0

4.9.1.2.10 TIEOFFREG09

- Base Address: 0xC001_0000
- Address = Base Address + 1024, Reset Value = 0x3E38_0200

Name	Bit	Type	Description	Reset Value
HOST_TXFSLSTUNE	[31:28]	RW	FS/LS Source Impedance Adjustment Function: This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 0000 = + 5 % 0001 = + 2.5 % 0011 = Design default 0111 = – 2.5 % 1111 = – 5 % All other bit settings are reserved. Voltage Range: 0 V-DVDD Active State: N/A	3
HOST_TXHSXVTUNE	[27:26]	RW	Transmitter High-Speed Crossover Adjustment Function: This bus adjusts the voltage at which the DP0 and DM0 signals cross while transmitting in HS mode. 00 = Reserved 01 = – 15 mV 10 = + 15 mV	3

Name	Bit	Type	Description	Reset Value
			11 = Default setting Voltage Range: 0 V-DVDD Active State: N/A	
HOST_OTGTUNE	[25:23]	RW	VBUS Valid Threshold Adjustment Function: This bus adjusts the voltage level for the VBUS Valid threshold. 000: – 12 % 001: – 9 % 010: – 6 % 011: – 3 % 100: Design default 101: + 3 % 110: + 6 % 111: + 9 % If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD Active State: N/A	4
HOST_SQRXTUNE	[22:20]	RW	Squelch Threshold Adjustment Function: This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 000: + 15 % 001: + 10 % 010: + 5 % 011: Design default 100: – 5 % 101: – 10 % 110: – 15 % 111: – 20 % Voltage Range: 0 V-DVDD Active State: N/A	3
HOST_COMPDISTUNE	[19:17]	RW	Disconnect Threshold Adjustment Function: This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 000: – 6 % 001: – 4.5 % 010: – 3 % 011: – 1.5 % 100: Design default 101: + 1.5 % 110: + 3 % 111: + 4.5 % If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD Active State: N/A	4
HOST_BYPASSSEL	[16]	RW	Transmitter Digital Bypass Select Function: Enables/disables Transmitter Digital Bypass	0

Name	Bit	Type	Description	Reset Value
			mode. 0 = Transmitter Digital Bypass mode is disabled. 1 = Transmitter Digital Bypass mode is enabled. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	
HOST_BYPASSDMEN	[15]	RW	DM0 Transmitter Digital Bypass Enable Function: Enables/disables the DM0 FS/LS driver in Transmitter Digital Bypass mode. 0 = DM0 FS/LS driver is disabled in Transmitter Digital Bypass mode. 1 = DM0 FS/LS driver is enabled and driven with the BYPASSDPDATA0 signal. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_BYPASSDPEN	[14]	RW	DP0 Transmitter Digital Bypass Enable Function: Enables/disables the DP0 FS/LS driver in Transmitter Digital Bypass mode. 0 = DP0 FS/LS driver is disabled in Transmitter Digital Bypass mode. 1 = DP0 FS/LS driver is enabled and driven with the BYPASSDPDATA0 signal. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_BYPASSDMDATA	[13]	RW	Data for DM0 Transmitter Digital Bypass Function: In Transmitter Digital Bypass mode, this signal provides the data that is transmitted on DM0. 0 = DM0 FS/LS driver drives to a low state. 1 = DM0 FS/LS driver drives to a high state. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
HOST_BYPASSDPDATA	[12]	RW	Data for DP0 Transmitter Digital Bypass Function: In Transmitter Digital Bypass mode, this signal provides the data that is transmitted on DP0. 0 = DP0 FS/LS driver drives to a low state. 1 = DP0 FS/LS driver drives to a high state. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0.	0

Name	Bit	Type	Description	Reset Value
			Voltage Range: 0 V-DVDD Active State: N/A	
HOST_TXBITSTUFFENH	[11]	RW	High-Byte Transmit Bit-Stuffing Enable Function: This controller signal controls bit stuffing on DATAINH0[7:0] whenOPMODE0[1:0] = 2'b11. 0 = Bit stuffing is disabled. 1 = Bit stuffing is enabled. Voltage Range: 0 V-DVDD Active State: High	0
HOST_TXBITSTUFFEN	[10]	RW	Low-Byte Transmit Bit-Stuffing Enable Function: This controller signal controls bit stuffing on DATAIN0[7:0] whenOPMODE0[1:0] = 2'b11. 0 = Bit stuffing is disabled. 1 = Bit stuffing is enabled. Voltage Range: 0 V-DVDD Active State: High	0
HOST_WORDINTERFACE	[9]	RW	UTMI+ Data Bus Width and Clock Select Function: This controller signal selects the data bus width of the UTMI+ data buses. 0 = 8-bit data interface (PHYCLOCK0 frequency is 60 MHz) 1 = 16-bit data interface (PHYCLOCK0 frequency is 30 MHz) The USB 2.0 picoPHY supports 8/16-bit data interfaces for all valid USB 2.0picoPHY speed modes. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: N/A	1
HOST_WORDINTERFACE_ENB	[8]	RW	Use Tieoff WORDINTERFACE instead of using USB2.0 HOST Controller signal	0
HOST_XCVRSEL	[7:6]	RW	Transceiver Select Function: This controller bus selects the HS, FS, or LS Transceiver. 00 = HS Transceiver 01 = FS Transceiver 10 = LS Transceiver 11 = Sends an LS packet on an FS bus or receives an LS packet. NOTE: Due to the power-up time required by the HS Transmitter, the controller must not transmit a high-speed packet within 1.6 µs after switching	0

Name	Bit	Type	Description	Reset Value
			XCVRSEL0[1:0] to HS Transceiver (from any other setting). Voltage Range: 0 V-DVDD Active State: N/A	
HOST_XCVRSEL_ENB	[5]	RW	Use Tieoff register value instead of controller value	0
HOST_TERMSEL	[4]	RW	USB Termination Select Function: This controller signal sets the USB 2.0 picoPHY's terminations to FS or HS. 0 = High-speed terminations are enabled. 1 = Full-speed terminations are enabled. NOTE: Four PHYCLOCK0 cycles are required for internal synchronous reset generation, and an additional six cycles are required to enable HS terminations inthe digital core. Therefore, the controller must not transmit a high-speed packet within 10 PHYCLOCK0 cycles after switching TERMSEL0 to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
HOST_TERMSEL_ENB	[3]	RW	Use Tieoff register value instead of controller value	0
HOST_OPMODE	[2:1]	RW	UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 00 = Normal 01 = Non-Driving 10 = Disable bit stuffing and NRZI encoding 11 = Normal operation without SYNC or EOP generation. If the XCVRSEL0[1:0]bus is not set to 2'b00 while OPMODE0[1:0] is set to 2'b11, USB 2.0 picoPHY behavior is undefined. NOTE: To perform battery charging, the USB 2.0 picoPHY must be placed in Non-Driving mode. Voltage Range: 0 V-DVDD Active State: N/A	0
HOST_OPMODE_ENB	[0]	RW	Use Tieoff register value instead of controller value	0

4.9.1.2.11 TIEOFFREG10

- Base Address: 0xC001_0000
- Address = Base Address + 1028, Reset Value = 0x3240_0153

Name	Bit	Type	Description	Reset Value
HOST_HSIC_LOOPBACKENB	[31]	RW	Loopback Test Enable Function: This signal places the USB 2.0 pico PHY in Loopback mode, which enables the receive and transmit logic concurrently. 0 = During data transmission, the receive logic is disabled. 1 = During data transmission, the receive logic is enabled. NOTE: Loopback mode is for test purposes only; it cannot be used for normal operation. In normal operation, tie this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_HSIC_PORTRESET	[30]	RW	Per-Port Reset Function: When asserted, this signal resets the corresponding port's transmit and receive logic without disabling the clocks within the USB 2.0 picoPHY. 0 = The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK0 cycles. 1 = The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. Asserting PORTRESET0 does not override any USB 2.0 picoPHY inputs that normally control the USB state, nor does it cause any transient, illegal USB states. Within 100 ns of asserting PORTRESET0, the controller must set the inputs that control the USB to values that cause a safe state. A safe state for Host and Device modes is defined as follows: • Host mode: Non-driving (OPMODE0[1:0] = 2'b01) with the 15 kΩ pull-down resistors enabled (DPPULLDOWN0 and DMPULLDOWN0 = 1'b1) • Device mode: Non-driving (OPMODE0[1:0] = 2'b01) with the 1.5 kΩ pull-up resistor disabled Voltage Range: 0 V-DVDD Active State: High	0
HOST_HSIC_COMMONONN	[29]	RW	Common Block Power-Down Control Function: This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0	1

Name	Bit	Type	Description	Reset Value
			picoPHY is in Suspend, or Sleep mode. 0 = In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered. 1 = In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. NOTE: 1. If COMMONONN is set low, CLK48MOHCI and CLK480M remain available in Suspend or UART/Auto resume mode. 2. If the reference clock source is a crystal, CLK12MOHCI remains available in Suspend or UART/Auto resume mode, only if COMMONONN is set to 1'b0. 3. If the reference clock source is either an external clock (connected to XO) or CLKCORE, CLK12MOHCI will continue to pulse in Suspend or UART/Auto resume mode, even when COMMONONN is set to 1'b1. 4. In Sleep mode, CLK48MOHCI and CLK12MOHCI are always available, irrespective of COMMONONN. Voltage Range: 0 V-DVDD Active State: Low	
HOST_HSIC_REFCLKSEL	[28:27]	RW	Reference Clock Select for PLL Block Function: This signal selects the reference clock source for the PLL block. 00 = The XO block uses the clock from a crystal. 01 = The XO block uses an external, 1.8-V clock supplied on the XO pin. 10 = The PLL uses CLKCORE as reference. 11 = Reserved This bus is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: N/A	2

Name	Bit	Type	Description	Reset Value
HOST_HSIC_REFCLKDIV	[26:20]	RW		0x24
HOST_HSIC_POR	[19]	RW	Power-On Reset Function: This signal resets all test registers and state machines in the USB 2.0picoPHY. The POR signal must be asserted for a minimum of 10 µs. Voltage Range: 0 V-DVDD Active State: High	0
HOST_HSIC_POR_ENB	[18]	RW	Use Tieoff register value instead of controller value	0
HOST_HSIC_SIDDQ	[17]	RW	IDDQ Test Enable Function: This test signal enables you to perform IDDQ testing by powering down all analog blocks. Before asserting SIDDQ, ensure that VDATSRCENB0,VDATDETENB0, DCDENB0, BYPASSSEL0, ADPPRBENB0, and TESTBURNIN are set to 1'b0. 0 = The analog blocks are powered up. 1 = The analog blocks are powered down. If this signal is not used, tie it low. Voltage Range: 0 V-DVDD Active State: High	0
HOST_HSIC_MSTRXCVR	[16]	RW		0
HOST_ACAENB	[15]	RW	ACA ID_OTG Pin Resistance Detection Enable Function: Enables detection of resistance on the ID_OTG pin of an ACA. 0 = Disables detection of resistance on the ID_OTG pin of an ACA. 1 = Enables detection of resistance on the ID_OTG pin of an ACA. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_DCDENB	[14]	RW	Data Contact Detection Enable Function: Enables current sourcing on the D+ line and pull-down resistance on the D- line for Data Contact Detect (DCD). 0 = IDP_SRC current is disabled, pull-down resistance on DM0 is disabled. 1 = IDP_SRC current is sourced onto DP0, pull-down resistance on DM0 is enabled. NOTE: During USB 2.0 picoPHY normal operation, set this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0

Name	Bit	Type	Description	Reset Value
HOST_VDATSRCENB	[13]	RW	Battery Charging Sourcing Select Function: Enables or disables sourcing for battery charging. 0 = Data source voltage (VDAT_SRC) is disabled. 1 = Data source voltage (VDAT_SRC) is enabled. During USB 2.0 picoPHY normal operation, set this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_VDATDETENB	[12]	RW	Battery Charging Attach/Connect Detection Enable Function: Enables or disables attach/connect detection. 0 = Data detect voltage (CHG_DET) is disabled. 1 = Data detect voltage (CHG_DET) is enabled. During USB 2.0 picoPHY normal operation, set this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
HOST_CHRGSEL	[11]	RW	Battery Charging Source Select Function: Determines whether current is sourced onto or sunk from DP0 or DM0. 0 = Data source voltage (VDAT_SRC) is sourced onto DP0 and sunk from DM0. 1 = Data source voltage (VDAT_SRC) is sourced onto DM0 and sunk from DP0. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
HOST_TXPREEMPPULSETUNE	[10]	RW	HS Transmitter Pre-Emphasis Duration Control Function: This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. The HS Transmitter pre-emphasis duration is defined in terms of unit amounts. One unit of pre-emphasis duration is approximately 580 ps and is defined as 1X pre-emphasis duration. This signal is valid only if either TXPREEMPAMPTUNE0[1] orTXPREEMPAMPTUNE0[0] is set to 1'b1. 0 (design default) = 2X, long pre-emphasis current duration 1 = 1X, short pre-emphasis current duration If TXPREEMPPULSETUNE0 is not used, set it to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0

Name	Bit	Type	Description	Reset Value
HOST_TXPREEMPAMPTUNE	[9:8]	RW	HS Transmitter Pre-Emphasis Current Control Function: This signal controls the amount of current sourced to DP0 andDM0 after a J-to-K or K-to-J transition. The HS Transmitter pre-emphasis current is defined in terms of unit amounts. One unit amount is approximately 600 µA and is defined as 1X pre-emphasis current. 00 = HS Transmitter pre-emphasis is disabled. 01 (design default) = HS Transmitter pre-emphasis circuit sources 1Xpre-emphasis current. 10 = HS Transmitter pre-emphasis circuit sources 2X pre-emphasis current. 11 = HS Transmitter pre-emphasis circuit sources 3X pre-emphasis current. If these signals are not used, set them to 2'b00. Voltage Range: 0 V-DVDD Active State: N/A	1
HOST_TXRESTUNE	[7:6]	RW	USB Source Impedance Adjustment Function: In some applications, there can be significant series resistance on the D+ and D- paths between the transceiver and cable. This bus adjusts the driver source impedance to compensate for added series resistance on the USB. NOTE: Any setting other than the default can result in source impedance variation across process, voltage, and temperature conditions that does not meet USB 2.0 specification limits. 00 = Source impedance is increased by approximately 1.5 Ω. 01 = Design default 10 = Source impedance is decreased by approximately 2 Ω. 11 = Source impedance is decreased by approximately 4 Ω. If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD Active State: N/A	1
HOST_TXRISETUNE	[5:4]	RW	HS Transmitter Rise/Fall Time Adjustment Function: This bus adjusts the rise/fall times of the high-speed waveform. 00 = – 10% 01 = – Design default 10 = + 15 11 = + 20% If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD	1

Name	Bit	Type	Description	Reset Value
			Active State: N/A	
HOST_TXVREFTUNE	[3:0]	RW	HS DC Voltage Level Adjustment Function: This bus adjusts the high-speed DC level voltage. 0000: – 6 % 0001: – 4 % 0010: – 2 % 0011: Design default 0100: + 2 % 0101: + 4 % 0101: + 4 % 0110: + 6 % 0111: + 8 % 1000: + 10 % 1001: + 12 % 1010: + 14 % 1011: + 16 % 1100: + 18 % 1101: + 20 % 1110: + 22 % 1111: + 24 % Voltage Range: 0 V-DVDD Active State: N/A	3

4.9.1.2.12 TIEOFFREG11

- Base Address: 0xC001_0000
- Address = Base Address + 102C, Reset Value = 0x0F3A_202B

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	0
OTG_NX_RF1_EMAW	[30:29]	RW	USB2.0 OTG SRAM EMAW value	0
OTG_NX_RF1_EMA	[28:26]	RW	USB2.0 OTG SRAM EMAW value	3
OTG_NSLEEP	[25]	RW	Sleep off OTG RAM	1
OTG_NPOWERDOWN	[24]	RW	Power down off OTG RAM	1
HOST_HSIC_TXSRTUNE	[23:20]	RW	TXSRTUNE value of HSIC PHY	3
HOST_HSIC_TXRPDTUNE	[19:18]	RW	TXRPDTUNE value of HSIC PHY	2
HOST_HSIC_TXRPUTUNE	[17:16]	RW	TXRPUTUNE value of HSIC PHY	2
HOST_HSIC_TXBITSTUFFENH	[15]	RW	High-Byte Transmit Bit-Stuffing Enable Function: This controller signal controls bit stuffing on DATAINH0[7:0] whenOPMODE0[1:0] = 2'b11. 0 = Bit stuffing is disabled.	0

Name	Bit	Type	Description	Reset Value
			1 = Bit stuffing is enabled. Voltage Range: 0 V-DVDD Active State: High	
HOST_HSIC_TXBITSTUFFEN	[14]	RW	Low-Byte Transmit Bit-Stuffing Enable Function: This controller signal controls bit stuffing on DATAIN0[7:0] whenOPMODE0[1:0] = 2'b11. 0 = Bit stuffing is disabled. 1 = Bit stuffing is enabled. Voltage Range: 0 V-DVDD Active State: High	0
HOST_HSIC_WORDINTERFACE	[13]	RW	UTMI+ Data Bus Width and Clock Select Function: This controller signal selects the data bus width of the UTMI+ data buses. 0 = 8-bit data interface (PHYCLOCK0 frequency is 60 MHz) 1 = 16-bit data interface (PHYCLOCK0 frequency is 30 MHz) The USB 2.0 picoPHY supports 8/16-bit data interfaces for all valid USB 2.0picoPHY speed modes. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: N/A	1
HOST_HSIC_WORDINTERFACE_ENB	[12]	RW	Use Tieoff register value instead of controller value	0
HOST_HSIC_XCVRSELECT	[11]	RW	XCVRSELECT value of HSIC PHY	0
HOST_HSIC_XCVRSELECT_ENB	[10]	RW	Enable HOST_HSIC_XCVRSELECT register	0
HOST_HSIC_OPMODE	[9:8]	RW	UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 00 = Normal 01 = Non-Driving 10 = Disable bit stuffing and NRZI encoding 11 = Normal operation without SYNC or EOP generation. If the XCVRSEL0[1:0]bus is not set to 2'b00 while OPMODE0[1:0] is set to 2'b11, USB 2.0 picoPHY behavior is undefined. NOTE: To perform battery charging, the USB 2.0 picoPHY must be placed in Non-Driving mode. Voltage Range: 0 V-DVDD	0

Name	Bit	Type	Description	Reset Value
			Active State: N/A	
HOST_HSIC_OPMODE_ENB	[7]	RW	Use Tieoff register value instead of controller value	0
HOST_HSIC_MSTRXOPU	[6]	RW	MSTRXOPU value of HSIC PHY	0
HOST_HSIC_SLEEPM	[5]	RW	Sleep Assertion Function: Asserting this signal places the USB 2.0 picoPHY in Sleep mode according to the USB 2.0 Link Power Management (LPM) addendum to the USB2.0 specification. In Sleep Mode, the transmitter is tri-stated and the USB 2.0picoPHY circuits are powered down except for the XO block If the reference clock is a crystal, the XO block remains powered when the USB 2.0 picoPHY is placed in Sleep mode. 0 = Sleep mode 1 = Normal operating mode If SUSPENDM0 is set to 1'b0, the USB 2.0 picoPHY will remain in Suspend mode irrespective of the SLEEPM0 setting. If the LPM function is not required, SLEEPM0 must be tied to DVDD. USB 2.0picoPHY Sleep mode can be overridden using the test interface. Voltage Range: 0 V-DVDD Active State: Low	1
HOST_HSIC_SLEEPM_ENB	[4]	RW	Use Tieoff register value instead of controller value	0
HOST_HSIC_SUSPENDM	[3]	RW	Suspend Assertion Function: Asserting this signal suspends the USB 2.0 picoPHY by tri-stating the transmitter and powering down the USB 2.0 picoPHY circuits. 0 = Suspend mode 1 = Normal operating mode USB 2.0 picoPHY power-down behavior can be overridden using the test interface. Voltage Range: 0 V-DVDD Active State: Low	1
HOST_HSIC_SUSPENDM_ENB	[2]	RW	Use Tieoff register value instead of controller value	0
HOST_HSIC_DMPULLDOWN	[1]	RW	D- Pull-Down Resistor Enable Function: This controller signal controls the pull-down resistance on the D- line. 0 = The pull-down resistance on D- is disabled. 1 = The pull-down resistance on D- is enabled. When an A/B device is acting as a host (downstream-facing port),DPPULLDOWN0 and DMPULLDOWN0 are enabled.	1

Name	Bit	Type	Description	Reset Value
			NOTE: UTMI+/OTG-compliant controllers are not allowed to toggleDPPULLDOWN0 and DMPULLDOWN0 during normal operation. Voltage Range: 0 V-DVDD Active State: High	
HOST_HSIC_DPPULLDOWN	[0]	RW	D+ Pull-Down Resistor Enable Function: This controller signal controls the pull-down resistance on the D+ line. 0 = The pull-down resistance on D+ is disabled. 1 = The pull-down resistance on D+ is enabled. When an A/B device is acting as a host (downstream-facing port),DPPULLDOWN0 and DMPULLDOWN0 are enabled. NOTE: UTMI+/OTG-compliant controllers are not allowed to toggleDPPULLDOWN0 and DMPULLDOWN0 during normal operation. Voltage Range: 0 V-DVDD Active State: High	1

4.9.1.2.13 TIEOFFREG12

- Base Address: 0xC001_0000
- Address = Base Address + 1030, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
OTG_SOF_COUNT	[31:18]	RW	SOF Input Count Function: Wireless USB Wire Adapter (DWA) application Values: • Wireless USB Device Wire Adapter (DWA) application: Input value to be loaded into Host Frame Number/Frame Time Remaining Register (HFNUM) field FrNum. • Non-Wireless USB application: Must be tied to 0. This signal is not present when parameter OTG_RM_OPT_FEATURES = Yes. Active State: High	0
OTG_GP_IN	[17:2]	RW	General Purpose Input Port Function: Can be used as general purpose inputs. This bus is not present when parameter OTG_RM_OPT_FEATURES = Yes. Active State: High	0
OTG_SS_SCALEDOWN_MODE	[1:0]	RW	Scale-Down Mode Function: • When this signal is enabled during simulation, the	1

Name	Bit	Type	Description	Reset Value
			core uses scaled-down timing values, resulting in faster simulations. • When it is disabled, actual timing values are used. NOTE: This signal must be disabled during synthesis. This strap signal is tied to one static value. Values: 2'b00: Disables all scale-downs. Actual timing values are used. Required for synthesis. 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include: Speed enumeration. HNP/SRP. Host mode suspend and resume. 2'b10: Enables scale-down of Device mode suspend and resume timing values only. 2'b11: Enables bit 0 and bit 1 scale-down timing values. Active State: N/A	

4.9.1.2.14 TIEOFFREG13

- Base Address: 0xC001_0000
- Address = Base Address + 1034, Reset Value = 0xA000_6D00

Name	Bit	Type	Description	Reset Value
OTG_SLEEPM	[31]	RW	Sleep Assertion Function: Asserting this signal places the USB 2.0 picoPHY in Sleep mode according to the USB 2.0 Link Power Management (LPM) addendum to the USB2.0 specification. In Sleep Mode, the transmitter is tri-stated and the USB 2.0picoPHY circuits are powered down except for the XO block If the reference clock is a crystal, the XO block remains powered when the USB 2.0 picoPHY is placed in Sleep mode. 0 = Sleep mode 1 = Normal operating mode If SUSPENDM0 is set to 1'b0, the USB 2.0 picoPHY will remain in Suspend mode irrespective of the SLEEPM0 setting. If the LPM function is not required, SLEEPM0 must be tied to DVDD. USB 2.0picoPHY Sleep mode can be overridden using the test interface. Voltage Range: 0 V-DVDD Active State: Low	1
OTG_SLEEPM_ENB	[30]	RW	Use Tieoff register value instead of controller value	0
OTG_SUSPENDM	[29]	RW	Suspend Assertion	1

Name	Bit	Type	Description	Reset Value
			Function: Asserting this signal suspends the USB 2.0 picoPHY by tri-stating the transmitter and powering down the USB 2.0 picoPHY circuits. 0 = Suspend mode 1 = Normal operating mode USB 2.0 picoPHY power-down behavior can be overridden using the test interface. Voltage Range: 0 V-DVDD Active State: Low	
OTG_SUSPENDM_ENB	[28]	RW	Use Tieoff register value instead of controller value	0
OTG_DMPULLDOWN	[27]	RW	D- Pull-Down Resistor Enable Function: This controller signal controls the pull-down resistance on the D- line. 0 = The pull-down resistance on D- is disabled. 1 = The pull-down resistance on D- is enabled. When an A/B device is acting as a host (downstream-facing port), DPPULLDOWN0 and DMPULLDOWN0 are enabled. NOTE: UTMI+/OTG-compliant controllers are not allowed to toggleDPPULLDOWN0 and DMPULLDOWN0 during normal operation. Voltage Range: 0 V-DVDD Active State: High	0
OTG_DPPULLDOWN	[26]	RW	D+ Pull-Down Resistor Enable Function: This controller signal controls the pull-down resistance on the D+ line. 0 = The pull-down resistance on D+ is disabled. 1 = The pull-down resistance on D+ is enabled. When an A/B device is acting as a host (downstream-facing port), DPPULLDOWN0 and DMPULLDOWN0 are enabled. NOTE: UTMI+/OTG-compliant controllers are not allowed to toggleDPPULLDOWN0 and DMPULLDOWN0 during normal operation. Voltage Range: 0 V-DVDD Active State: High	0
OTG_VBUSVLDEXTSEL	[25]	RW	External VBUS Valid Select Function: This signal selects either the VBUSVLDEXT0 input or the internal Session Valid comparator to generate the OTGSESSVLD0 output. To avoid potential glitches in DP0, VBUSVLDEXTSEL0 must be static prior to a power-on reset and remain static during normal operation. The OTGSESSVLD0 signal, in conjunction with XCVRSEL0[1:0],OPMODE0[1:0], TERMSEL0, DPPULLDOWN0, and DMPULLDOWN0,control the DP0 pull-up resistor. If VBUSVLDEXT0 and the	0

Name	Bit	Type	Description	Reset Value
			internal Session Valid comparator output are asserted, and VBUSEXTSEL0changes, it is possible for OTGSESSVLD0 to glitch low, causing the DP0resistor to be temporarily disabled. 0 = The internal Session Valid comparator is used to generateOTGSESSVLD0 and assert the DP0 pull-up resistor. 1 = The VBUSVLDEXT0 input is used to generate OTGSESSVLD0 and assert the DP0 pull-up resistor. This signal is not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: High	
OTG_VBUSVLDEXT	[24]	RW	External VBUS Valid Indicator Function: This signal is valid in Device mode and only when theVBUSVLDEXTSEL0 signal is set to 1'b1. VBUSVLDEXT0 indicates whether the VBUS signal on the USB cable is valid. In addition, VBUSVLDEXT0 enables the pull-up resistor on the D+ line. 0 = The VBUS signal is not valid, and the pull-up resistor on D+ is disabled. 1 = The VBUS signal is valid, and the pull-up resistor on D+ is enabled. In Host mode, this input is not used and can be tied to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_ADPPRBENB	[23]	RW	ADP Probe Enable Function: Enables/disables the ADP Probe comparator. 0 = ADP Probe comparator is disabled. 1 = ADP Probe comparator is enabled. If this signal is not used, tie it to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_ADPDISCHRG	[22]	RW	VBUS Input ADP Discharge Enable Function: Controls discharging the VBUS input during ADP. 0 = Disables discharging VBUS during ADP. 1 = Enables discharging VBUS during ADP. If this signal is not used, tie it to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_ADPCHRG	[21]	RW	VBUS Input ADP Charge Enable	0

Name	Bit	Type	Description	Reset Value
			Function: Controls charging the VBUS input during ADP. 0 = Disables charging VBUS during ADP. 1 = Enables charging VBUS during ADP. If this signal is not used, tie it to 1'b0. Voltage Range: 0 V-DVDD Active State: High	
OTG_DRVVBUS	[20]	RW	Drive VBUS Function: This controller signal controls the VBUS Valid comparator. This signal drives 5 V on VBUS through an external charge pump. When OTGDISABLE0 is set to 1'b0 and DRVVBUS0 is asserted, the Band gap circuitry and VBUS Valid comparator are powered, even in Suspend or Sleep mode. 0 = The VBUS Valid comparator is disabled. 1 = The VBUS Valid comparator is enabled. Voltage Range: 0 V-DVDD Active State: High	0
OTG_IDPULLUP	[19]	RW	Analog ID Input Sample Enable Function: This controller signal controls ID line sampling. 0 = ID pin sampling is disabled, and the IDDIG0 output is not valid. 1 = ID pin sampling is enabled, and the IDDIG0 output is valid. Voltage Range: 0 V-DVDD Active State: High	0
OTG_LOOPBACKENB	[18]	RW	Loopback Test Enable Function: This signal places the USB 2.0 picoPHY in Loopback mode, which enables the receive and transmit logic concurrently. 0 = During data transmission, the receive logic is disabled. 1: During data transmission, the receive logic is enabled. NOTE: Loopback mode is for test purposes only; it cannot be used for normal operation. In normal operation, tie this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_OTGDISABLE	[17]	RW	OTG Block Disable Function: This signal powers down the VBUS Valid comparator, but not the Session Valid comparator, ADP probe and sense comparators, nor the ID	0

Name	Bit	Type	Description	Reset Value
			detection circuitry. To save power, if the application does not use the OTG function, this input can be set high. 0 = The OTG block is powered up. 1 = The OTG block is powered down. Voltage Range: 0 V-DVDD Active State: High	
OTG_PORTRESET	[16]	RW	Per-Port Reset Function: When asserted, this signal resets the corresponding port's transmit and receive logic without disabling the clocks within the USB 2.0 picoPHY. 0 = The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK0 cycles. 1 = The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers. Asserting PORTRESET0 does not override any USB 2.0 picoPHY inputs that normally control the USB state, nor does it cause any transient, illegal USB states. Within 100 ns of asserting PORTRESET0, the controller must set the inputs that control the USB to values that cause a safe state. A safe state for Host and Device modes is defined as follows: • Host mode: Non-driving (OPMODE0[1:0] = 2'b01) with the 15 kΩ pull-down resistors enabled (DPPULLDOWN0 and DMPULLDOWN0 = 1'b1) • Device mode: Non-driving (OPMODE0[1:0] = 2'b01) with the 1.5 kΩ pull-up resistor disabled Voltage Range: 0 V-DVDD Active State: High	0
OTG_RESREQIN	[15]	RW	Reserved Function: Reserved. Tie this pin to 1'b0. Voltage Range: 0 V-DVDD	0
OTG_COMMONONN	[14]	RW	Common Block Power-Down Control Function: This signal controls the power-down signals in the XO, Bias, and PLL blocks when the USB 2.0 picoPHY is in Suspend, or Sleep mode. 0 = In Suspend mode, the XO, Bias, and PLL blocks remain powered in Suspend mode. In Sleep mode, if the reference clock is a crystal, the XO block remains powered. 1 = In Suspend mode, the XO, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL	1

Name	Bit	Type	Description	Reset Value
			blocks are powered down. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. NOTE: 1. If COMMONONN is set low, CLK48MOHCI and CLK480M remain available in Suspend or UART/Auto resume mode. 2. If the reference clock source is a crystal, CLK12MOHCI remains available in Suspend or UART/Auto resume mode, only if COMMONONN is set to 1'b0. 3. If the reference clock source is either an external clock (connected to XO) or CLKCORE, CLK12MOHCI will continue to pulse in Suspend or UART/Auto resume mode, even when COMMONONN is set to 1'b1. 4. In Sleep mode, CLK48MOHCI and CLK12MOHCI are always available, irrespective of COMMONONN. Voltage Range: 0 V-DVDD Active State: Low	
OTG_FSEL	[13:11]	RW	Reference Clock Frequency Select Function: Selects the USB 2.0 picoPHY reference clock frequency. 000 = 9.6 MHz 001 = 10 MHz 010 = 12 MHz 011 = 19.2 MHz 100 = 20 MHz 101 = 24 MHz 110 = Reserved 111 = 50 MHz Voltage Range: 0 V-DVDD Active State: N/A	5
OTG_REFCLKSEL	[10:9]	RW	Reference Clock Select for PLL Block Function: This signal selects the reference clock source for the PLL block. 00 = The XO block uses the clock from a crystal. 01 = The XO block uses an external, 1.8-V clock supplied on the XO pin. 10 = The PLL uses CLKCORE as reference. 11 = Reserved This bus is a strapping option that must be set prior to a power-on reset and remain static during normal	2

Name	Bit	Type	Description	Reset Value
			operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: N/A	
OTG_POR	[8]	RW	Power-On Reset Function: This signal resets all test registers and state machines in the USB 2.0picoPHY. The POR signal must be asserted for a minimum of 10 µs. Voltage Range: 0 V-DVDD Active State: High	1
OTG_POR_ENB	[7]	RW	Use Tieoff register value instead of controller value	0
OTG_VATESTENB	[6:5]	RW	Analog Test Pin Select Function: Enables analog test voltages to be placed on either the ANALOGTEST or ID0 pin. 00 = Analog test voltages cannot be viewed or applied on either ANALOGTEST or ID0. 01 = Analog test voltages can be viewed or applied on ID0. 10 = Analog test voltages can be viewed or applied on ANALOGTEST. 11 = Reserved. Invalid setting. If this bus is not used, tie these inputs low. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_SIDDQ	[4]	RW	IDDQ Test Enable Function: This test signal enables you to perform IDDQ testing by powering down all analog blocks. Before asserting SIDDQ, ensure that VDATSRCENB0, VDATDETENB0, DCDENB0, BYPASSSEL0, ADPPRBENB0, and TESTBURNIN are set to 1'b0. 0 = The analog blocks are powered up. 1 = The analog blocks are powered down. If this signal is not used, tie it low. Voltage Range: 0 V-DVDD Active State: High	0
OTG_NUTMIRESETSYNC	[3]	RW	Reset off utmi clock of OTG LINK	0
OTG_NRESETSYNC	[2]	RW	Reset off OTG LINK	0
OTG_IF_SELECT_HSIC	[1]	RW	HSIC Interface Select Function: Used to select the HSIC mode of operation. Indicates that the HSIC interface is selected. The core	0

Name	Bit	Type	Description	Reset Value
			starts to connect/operate in HSIC mode when the GLPMCFG. HSICCon is programmed to 1, if GLPMCFG. InvSelHsic = 0. Active State: High	
OTG_SYS_DMA_DONE	[0]	RW	System DMA Done Function: This signal should be asserted when the DATA write is completed in the System Memory. It should be asserted for one AHB clock cycle synchronous to hclk. The signal is valid only when RMS is enabled. Values: 0 = Data write not complete. 1 = Data Write complete in the system memory for the current DMA write-transferfrom HS OTG Active State: High	0

4.9.1.2.15 TIEOFFREG14

- Base Address: 0xC001_0000
- Address = Base Address + 1038, Reset Value = 0x3E38_0200

Name	Bit	Type	Description	Reset Value
OTG_TXFSLSTUNE	[31:28]	RW	FS/LS Source Impedance Adjustment Function: This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature. 0000 = +5 % 0001 = +2.5 % 0011 = Design default 0111 = –2.5 % 1111 = –5 % All other bit settings are reserved. Voltage Range: 0 V-DVDD Active State: N/A	3
OTG_TXHSXVTUNE	[27:26]	RW	Transmitter High-Speed Crossover Adjustment Function: This bus adjusts the voltage at which the DP0 and DM0 signals cross while transmitting in HS mode. 00 = Reserved 01 = –15 mV 10 = +15 mV 11 = Default setting Voltage Range: 0 V-DVDD Active State: N/A	3
OTG_OTGTUNE	[25:23]	RW	VBUS Valid Threshold Adjustment	4

Name	Bit	Type	Description	Reset Value
			Function = This bus adjusts the voltage level for the VBUS Valid threshold. 000 = –12 % 001 = –9 % 010 = –6 % 011 = –3 % 100 = Design default 101 = +3 % 110 = +6 % If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD Active State: N/A	
OTG_SQRXTUNE	[22:20]	RW	Squelch Threshold Adjustment Function = This bus adjusts the voltage level for the threshold used to detect valid high-speed data. 000 = +15 % 001 = +10 % 010 = +5 % 011 = Design default 100 = –5 % 101 = –10 % 110 = –15 % 111 = –20 % Voltage Range: 0 V-DVDD Active State: N/A	3
OTG_COMPDISTUNE	[19:17]	RW	Disconnect Threshold Adjustment Function = This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host. 000 = –6 % 001 = –4.5 % 010 = –3 % 011 = –1.5 % 100 = Design default 101 = +1.5 % 110 = +3 % 111 = +4.5 % If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD Active State: N/A	4
OTG_BYPASSSEL	[16]	RW	Transmitter Digital Bypass Select Function: Enables/disables Transmitter Digital Bypass mode. 0 = Transmitter Digital Bypass mode is disabled. 1 = Transmitter Digital Bypass mode is enabled. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0.	0

Name	Bit	Type	Description	Reset Value
			Voltage Range: 0 V-DVDD Active State: High	
OTG_BYPASSDMEN	[15]	RW	DM0 Transmitter Digital Bypass Enable Function: Enables/disables the DM0 FS/LS driver in Transmitter Digital Bypass mode. 0 = DM0 FS/LS driver is disabled in Transmitter Digital Bypass mode. 1 = DM0 FS/LS driver is enabled and driven with the BYPASSDPDATA0 signal. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_BYPASSDPEN	[14]	RW	DP0 Transmitter Digital Bypass Enable Function: Enables/disables the DP0 FS/LS driver in Transmitter Digital Bypass mode. 0 = DP0 FS/LS driver is disabled in Transmitter Digital Bypass mode. 1 = DP0 FS/LS driver is enabled and driven with the BYPASSDPDATA0 signal. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_BYPASSDMDATA	[13]	RW	Data for DM0 Transmitter Digital Bypass Function: In Transmitter Digital Bypass mode, this signal provides the data that is transmitted on DM0. 0 = DM0 FS/LS driver drives to a low state. 1 = DM0 FS/LS driver drives to a high state. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_BYPASSDPDATA	[12]	RW	Data for DP0 Transmitter Digital Bypass Function: In Transmitter Digital Bypass mode, this signal provides the data that is transmitted on DP0. 0 = DP0 FS/LS driver drives to a low state. 1 = DP0 FS/LS driver drives to a high state. If Transmitter Digital Bypass mode is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_TXBITSTUFFENH	[11]	RW	High-Byte Transmit Bit-Stuffing Enable Function: This controller signal controls bit stuffing on DATAINH0[7:0] whenOPMODE0[1:0] = 2'b11.	0

Name	Bit	Type	Description	Reset Value
			0 = Bit stuffing is disabled. 1 = Bit stuffing is enabled. Voltage Range: 0 V-DVDD Active State: High	
OTG_TXBITSTUFFEN	[10]	RW	Low-Byte Transmit Bit-Stuffing Enable Function: This controller signal controls bit stuffing on DATAIN0[7:0] whenOPMODE0[1:0] = 2'b11. 0 = Bit stuffing is disabled. 1 = Bit stuffing is enabled. Voltage Range: 0 V-DVDD Active State: High	0
OTG_WORDINTERFACE	[9]	RW	UTMI+ Data Bus Width and Clock Select Function: This controller signal selects the data bus width of the UTMI+ data buses. 0 = 8-bit data interface (PHYCLOCK0 frequency is 60 MHz) 1 = 16-bit data interface (PHYCLOCK0 frequency is 30 MHz) The USB 2.0 picoPHY supports 8/16-bit data interfaces for all valid USB 2.0picoPHY speed modes. This signal is a strapping option that must be set prior to a power-on reset and remain static during normal operation. Strapping options are not critical for STA, and any other timings or loading limits for the pin are specified in the .lib timing model included in the product deliverables. Voltage Range: 0 V-DVDD Active State: N/A	1
OTG_WORDINTERFACE_ENB	[8]	RW	Use Tieoff register value instead of controller value	0
OTG_XCVRSEL	[7:6]	RW	Transceiver Select Function: This controller bus selects the HS, FS, or LS Transceiver. 00 = HS Transceiver 01 = FS Transceiver 10 = LS Transceiver 11 = Sends an LS packet on an FS bus or receives an LS packet. NOTE: Due to the power-up time required by the HS Transmitter, the controller must not transmit a high-speed packet within 1.6 µs after switching XCVRSEL0[1:0] to HS Transceiver (from any other setting). Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_XCVRSEL_ENB	[5]	RW	Use Tieoff register value instead of controller value	0

Name	Bit	Type	Description	Reset Value
OTG_TERMSEL	[4]	RW	USB Termination Select Function: This controller signal sets the USB 2.0 picoPHY's terminations to FS orHS. 0 = High-speed terminations are enabled. 1 = Full-speed terminations are enabled. NOTE: Four PHYCLOCK0 cycles are required for internal synchronous reset generation, and an additional six cycles are required to enable HS terminations in the digital core. Therefore, the controller must not transmit a high-speed packet within 10 PHYCLOCK0 cycles after switching TERMSEL0 to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_TERMSEL_ENB	[3]	RW	Use Tieoff register value instead of controller value	0
OTG_OPMODE	[2:1]	RW	UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 00 = Normal 01 = Non-Driving 10 = Disable bit stuffing and NRZI encoding 11 = Normal operation without SYNC or EOP generation. If the XCVRSEL0[1:0]bus is not set to 2'b00 while OPMODE0[1:0] is set to 2'b11, USB 2.0 picoPHY behavior is undefined. NOTE: To perform battery charging, the USB 2.0 picoPHY must be placed in Non-Driving mode. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_OPMODE_ENB	[0]	RW	Use Tieoff register value instead of controller value	0

4.9.1.2.16 TIEOFFREG15

- Base Address: 0xC001_0000
- Address = Base Address + 103C, Reset Value = 0x3FC0_0153

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	–	Reserved	0
CODA960_NSLEEP00	[29:26]	RW	CODA960 SRAM group 0 retention (low active)	F
CODA960_NPWRDN00	[25:22]	RW	CODA960 SRAM group 0 Power Down	F
OTG_GLITCHLESSMUXCNTRL	[21]	RW	Select glitch less mux of OTG suspend clock	0
OTG_LPMCLKMUXCNTRL	[20]	RW		0
OTG_DRVVBUS_ENB	[19]	RW	Use Tieoff register value instead of controller value	0
OTG_DMPULLDOWN_ENB	[18]	RW	Use Tieoff register value instead of controller value	0
OTG_DPPULLDOWN_ENB	[17]	RW	Use Tieoff register value instead of controller value	0
OTG_IDPULLUP_ENB	[16]	RW	Use Tieoff register value instead of controller value	0
OTG_ACAENB	[15]	RW	ACA ID_OTG Pin Resistance Detection Enable Function: Enables detection of resistance on the ID_OTG pin of an ACA. 0 = Disables detection of resistance on the ID_OTG pin of an ACA. 1 = Enables detection of resistance on the ID_OTG pin of an ACA. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_DCDENB	[14]	RW	Data Contact Detection Enable Function: Enables current sourcing on the D+ line and pull-down resistance on the D- line for Data Contact Detect (DCD). 0 = IDP_SRC current is disabled, pull-down resistance on DM0 is disabled. 1 = IDP_SRC current is sourced onto DP0, pull-down resistance on DM0 is enabled. NOTE: During USB 2.0 picoPHY normal operation, set this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_VDATSRCENB	[13]	RW	Battery Charging Sourcing Select Function: Enables or disables sourcing for battery charging. 0 = Data source voltage (VDAT_SRC) is disabled.	0

Name	Bit	Type	Description	Reset Value
			1 = Data source voltage (VDAT_SRC) is enabled. During USB 2.0 picoPHY normal operation, set this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	
OTG_VDATDETENB	[12]	RW	Battery Charging Attach/Connect Detection Enable Function: Enables or disables attach/connect detection. 0 = Data detect voltage (CHG_DET) is disabled. 1 = Data detect voltage (CHG_DET) is enabled. During USB 2.0 picoPHY normal operation, set this signal low. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: High	0
OTG_CHRGSEL	[11]	RW	Battery Charging Source Select Function: Determines whether current is sourced onto or sunk from DP0 or DM0. 0 = Data source voltage (VDAT_SRC) is sourced onto DP0 and sunk from DM0. 1 = Data source voltage (VDAT_SRC) is sourced onto DM0 and sunk from DP0. If this signal is not used, tie this input to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_TXPREEMPPULSETUNE	[10]	RW	HS Transmitter Pre-Emphasis Duration Control Function: This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. The HS Transmitter pre-emphasis duration is defined in terms of unit amounts. One unit of pre-emphasis duration is approximately 580 ps and is defined as 1X pre-emphasis duration. This signal is valid only if either TXPREEMPAMPTUNE0[1] orTXPREEMPAMPTUNE0[0] is set to 1'b1. 0 (design default) = 2X, long pre-emphasis current duration 1 = 1X, short pre-emphasis current duration If TXPREEMPPULSETUNE0 is not used, set it to 1'b0. Voltage Range: 0 V-DVDD Active State: N/A	0
OTG_TXPREEMPAMPTUNE	[9:8]	RW	HS Transmitter Pre-Emphasis Current Control Function: This signal controls the amount of current sourced to DP0 andDM0 after a J-to-K or K-to-J transition. The HS Transmitter pre-emphasis current is	1

Name	Bit	Type	Description	Reset Value
			defined in terms of unit amounts. One unit amount is approximately 600µA and is defined as 1X pre-emphasis current. 00 = HS Transmitter pre-emphasis is disabled. 01 (design default) = HS Transmitter pre-emphasis circuit sources 1Xpre-emphasis current. 10 = HS Transmitter pre-emphasis circuit sources 2X pre-emphasis current. 11 = HS Transmitter pre-emphasis circuit sources 3X pre-emphasis current. If these signals are not used, set them to 2'b00. Voltage Range: 0 V-DVDD Active State: N/A	
OTG_TXRESTUNE	[7:6]	RW	USB Source Impedance Adjustment Function: In some applications, there can be significant series resistance on the D+ and D- paths between the transceiver and cable. This bus adjusts the driver source impedance to compensate for added series resistance on the USB. Note: Any setting other than the default can result in source impedance variation across process, voltage, and temperature conditions that does not meet USB 2.0 specification limits. 00 = Source impedance is increased by approximately 1.5 Ω. 01 = Design default 10 = Source impedance is decreased by approximately 2 Ω. 11 =: Source impedance is decreased by approximately 4 Ω. If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD Active State: N/A	1
OTG_TXRISETUNE	[5:4]	RW	HS Transmitter Rise/Fall Time Adjustment Function: This bus adjusts the rise/fall times of the high-speed waveform. 00 = –10 % 01 = –Design default 10 = + 15 % 11 = + 20 % If this bus is not used, leave it at the default setting. Voltage Range: 0 V-DVDD Active State: N/A	1
OTG_TXVREFTUNE	[3:0]	RW	HS DC Voltage Level Adjustment Function: This bus adjusts the high-speed DC level voltage.	3

Name	Bit	Type	Description	Reset Value
			0000 = –6 % 0001 = –4 % 0010 = –2 % 0011 = Design default 0100 = +2 % 0101 = +4 % 0110 = +6 % 0111 = +8 % 1000 = +10 % 1001 = +12 % 1010 = +14 % 1011 = +16 % 1100 = +18 % 1101 = +20 % 1110 = +22 % 1111 = +24 % Voltage Range: 0 V-DVDD Active State: N/A	

4.9.1.2.17 TIEOFFREG16

- Base Address: 0xC001_0000
- Address = Base Address + 0x1040, Reset Value = 0x00FF_FFFF

Name	Bit	Type	Description	Reset Value
RSGVD	[31:26]	–	Reserved	0
CODA960_nPWRDN02	[25:16]	RW	CODA960 SRAM group2 Power down(low active)	FF
CODA960_nSLEEP01	[15:8]	RW	CODA960 SRAM group 1 retention (low active)	FF
CODA960_nPWRDN01	[7:0]	RW	CODA960 SRAM group 1 power down(low active)	FF

4.9.1.2.18 TIEOFFREG17

- Base Address: 0xC001_0000
- Address = Base Address + 0x1044, Reset Value = 0x3FFF_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	–	Rserved	0
CODA960_nSLEEP04	[29:23]	RW	CODA960 SRAM group 4 retention (low active)	FF
CODA960_nPWRDN04	[21:14]	RW	CODA960 SRAM group 4 Power down(low active)	FF
CODA960_nSLEEP03	[13:12]	RW	CODA960 SRAM group 3 retention (low active)	3
CODA960_nPWRDN03	[11:10]	RW	CODA960 SRAM group 3 Power down(low active)	3
CODA960_nSLEEP02	[9:0]	RW	CODA960 SRAM group 2 retention (low active)	3FF

4.9.1.2.19 TIEOFFREG18

- Base Address: 0xC001_0000
- Address = Base Address + 0x1048, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
CODA960_nPWRDN07	[31:20]	RW	CODA960 SRAM group 7 power down(low active)	FFF
CODA960_nSLEEP06	[19:13]	RW	CODA960 SRAM group 6 retention (low active)	7F
CODA960_nPWRDN06	[12:6]	RW	CODA960 SRAM group 6 power down(low active)	7F
CODA960_nSLEEP05	[5:3]	RW	CODA960 SRAM group 5 retention (low active)	7
CODA960_nPWRDN05	[2:0]	RW	CODA960 SRAM group 5 power down(low active)	7

4.9.1.2.20 TIEOFFREG19

- Base Address: 0xC001_0000
- Address = Base Address + 0x104C, Reset Value = 0x0FFF_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	–		0
CODA960_nPWRDN10	[27:18]	RW	CODA960 SRAM group 10 power down (low active)	3FF
CODA960_nSLEEP09	[17:16]	RW	CODA960 SRAM group 9 retention (low active)	3
CODA960_nPWRDN09	[15:14]	RW	CODA960 SRAM group 9 power down (low active)	3
CODA960_nSLEEP08	[13]	RW	CODA960 SRAM group 8 retention (low active)	1
CODA960_nPWRDN08	[12]	RW	CODA960 SRAM group 8 power down (low active)	1
CODA960_nSLEEP07	[11:0]	RW	CODA960 SRAM group 7 retention (low active)	FFF

4.9.1.2.21 TIEOFFREG20

- Base Address: 0xC001_0000
- Address = Base Address + 0x1050, Reset Value = 0x1B6D_BFFF

Name	Bit	Type	Description	Reset Value
CODA960_ra2_EMAWA	[31:30]	RW	CODA960 SRAM EMAW value	0
CODA960_ra2_EMAB	[29:27]	RW	CODA960 SRAM EMAB value	3
CODA960_ra2_EMAA	[26:24]	RW	CODA960 SRAM EMAA value	3
CODA960_rf2w_EMAB	[23:21]	RW	CODA960 SRAM EMAB value	3
CODA960_rf2w_EMAA	[20:18]	RW	CODA960 SRAM EMAA value	3
CODA960_rf2_EMAB	[17:15]	RW	CODA960 SRAM EMAB value	3
CODA960_rf2_EMAA	[14:12]	RW	CODA960 SRAM EMAA value	3
CODA960_nSLEEP11	[11]	RW	CODA960 SRAM group 11 retention (low active)	1
CODA960_nPWRDN11	[10]	RW	CODA960 SRAM group 11 power down (low active)	1
CODA960_nSLEEP10	[9:0]	RW	CODA960 SRAM group 10 retention (low active)	3FF

4.9.1.2.22 TIEOFFREG21

- Base Address: 0xC001_0000
- Address = Base Address + 0x1054, Reset Value = 0x6C86_306C

Name	Bit	Type	Description	Reset Value
GMAC_RF2_EMAB	[31:29]	RW	GMAC SRAM EMAB value	3
GMAC_RF2_EMAA	[28:26]	RW	GMAC SRAM EMAA value	3
GMAC_PHY_INIF_SEL	[25:23]	RW	PHY Interface Select Function: These pins select on of the multiple PHY interface of MAC. This is sampled only during reset assertion and ignored after that. - 000 : GMII or MII - 001 : RGMII - 010 : SGMII - 011 : TBI - 100 : RMII - 101 : RTBL - 110 : SMLL - 111 : RevVII Synchronous to : CSR clock Caution : This chip supports only RGBMII	1
GMAC_SBD_FLOWCTL	[22]	RW	Side band Flow Control Function : When set high, instructs the MAC to transmit Pause frames in Full-Duplex mode, In half-duplex mode, the MAC enables the backpressure function until this signal is made low again Active State: High Registered: Yes Synchronous t0: Asynchronous	0
CODA960_rf1w_EMAW	[21:20]	RW	CODA960 SRAM EMAW value	0
CODA960_rf1w_EMA	[19:17]	RW	CODA960 SRAM EMA value	3
CODA960_rf1_EMAW	[16:15]	RW	CODA960 SRAM EMAW value	0
CODA960_rf1_EMA	[14:12]	RW	CODA960 SRAM EMA value	3
CODA960_ra2w_EMAWB	[11:10]	RW	CODA960 SRAM EMAWB value	0
CODA960_ra2w_EMAWA	[9:8]	RW	CODA960 SRAM EMAWA value	0
CODA960_ra2w_EMAB	[7:5]	RW	CODA960 SRAM EMAB value	3
CODA960_ra2w_EMAA	[4:2]	RW	CODA960 SRAM EMAA value	3
CODA960_ra2_EMAWB	[1:0]	RW	CODA960 SRAM EMAWB value	0

4.9.1.2.23 TIEOFFREG22

- Base Address: 0xC001_0000
- Address = Base Address + 0x1058, Reset Value = 0xFFFE_18DB

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	RW	Reserved	7FFF
RSVD	[16]	RW	Reserved	0
3D GPU_SPSRAM_BW_EMAW	[15:14]	RW	3D GPU SRAM EMAW value	0
3D GPU_SPSRAM_BW_EMA	[13:11]	RW	3D GPU SRAM EMA value	3
3D GPU_SPSRAM_EMAW	[10:9]	RW	3D GPU SRAM EMAW value	0
3D GPU_SPSRAM_EMA	[8:6]	RW	3D GPU SRAM EMA value	3
3D GPU_DPSRAM_1R1W_EMAB	[5:3]	RW	3D GPU SRAM EMAB value	3
3D GPU_DPSRAM_1R1W_EMAA	[2:0]	RW	3D GPU SRAM EMAA value	3

4.9.1.2.24 TIEOFFREG23

- Base Address: 0xC001_0000
- Address = Base Address + 105C, Reset Value = Reset Value = 0x001F_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	–	Reserved	0
3D GPU_L2_NSLEEP	[20:18]	RW	3D GPU L2 Cache SRAM retention (low active)	7
RSVD	[17:15]	RW	Reserved	7
3D GPU_GP_NSLEEP	[14:0]	RW	3D GPU GP SRAM retention (low active)	7FFF

4.9.1.2.25 TIEOFFREG24

- Base Address: 0xC001_0000
- Address = Base Address + 1060, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	0
ARQOS1	[15:12]	RW	DREX slave interface port 1 read channel QoS	0
AWQOS1	[11:8]	RW	DREX slave interface port 1 write channel QoS	0
ARQOS0	[7:4]	RW	DREX slave interface port 0 read channel QoS	0
AWQOS0	[3:0]	RW	DREX slave interface port 0 write channel QoS	0

4.9.1.2.26 TIEOFFREG25

- Base Address: 0xC001_0000
- Address = Base Address + 1064, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
3D GPU_PP0_NSLEEP	[31:0]	RW	3D GPU PP0 SRAM retention (low active)	FFFFFFFF

4.9.1.2.27 TIEOFFREG26

- Base Address: 0xC001_0000
- Address = Base Address + 1068, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TZPCDECPROT0m3	[31:24]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT1m3	[23:16]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
RSVD	[15:14]	RW	Reserved	0
TZPCDECPROT0m7	[13]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT1m7	[12]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT0m8	[11]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT1m8	[10]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT0m10	[9]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT1m10	[8]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT0m12	[7]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT1m12	[6]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT0m13	[5]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT1m13	[4]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT0m14	[3]	RW	Secure Transaction (Peri BUS) 0 = Secure	0

Name	Bit	Type	Description	Reset Value
			1 = Non-Secure	
TZPCDECPROT1m14	[2]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT0m16	[1]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0
TZPCDECPROT1m16	[0]	RW	Secure Transaction (Peri BUS) 0 = Secure 1 = Non-Secure	0

4.9.1.2.28 TIEOFFREG27

- Base Address: 0xC001_0000
- Address = Base Address + 106C, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
3D GPU_PP1_NSLEEP	[31:0]	RW	3D GPU PP1 SRAM retention (low active)	FFFFFFFF

4.9.1.2.29 TIEOFFREG28

- Base Address: 0xC001_0000
- Address = Base Address + 1070, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ACPARUSER_0	[31]	RW	ACP AR channel user value	0
ACPAWUSER_0	[30]	RW	ACP AW channel user value	0
RSVD	[29:26]	–	Reserved	0
CA9_PWRCTLI3	[25:24]	RW	Reset value for CPU3 status register [3:2]	0
MPEGTS_HPROT_3	[23]	RW	AXI Cacheable	0
MPEGTS_HPROT_2	[22]	RW	AXI Bufferable	0
SDMMC_HPROT_3	[21]	RW	AXI Cacheable	0
SDMMC_HPROT_2	[20]	RW	AXI Bufferable	0
TB0_AWCACHE1_VALUE	[19]	RW	TOP BUS m0 AWCACHE[1] value	0
TB0_ARCACHE1_VALUE	[18]	RW	TOP BUS m0 ARCACHE[1] value	0
TB0_AWCACHE1_CTRLEN	[17]	RW	TOP BUS m0 AWCACHE[1] control enable 0 = AWCACHE[1] bit control disable 1 = AWCACHE[1] bit control enable	0
TB0_ARCACHE1_CTRLEN	[16]	RW	TOP BUS m0 ARCACHE[1] control enable 0 = ARCACHE[1] bit control disble	0

Name	Bit	Type	Description	Reset Value
			1 = ARCACHE[1] bit control enable	
HOST_HPROT_3	[15]	RW	AXI Cacheable	0
HOST_HPROT_2	[14]	RW	AXI Bufferable	0
EHCI_HPROT_3	[13]	RW	AXI Cacheable	0
EHCI_HPROT_2	[12]	RW	AXI Bufferable	0
OTG_HPROT_3	[11]	RW	AXI Cacheable	0
OTG_HPROT_2	[10]	RW	AXI Bufferable	0
ACP_AxPROT	[9]	RW	Secure Transaction (AxPROT[1] between TOP bus <-> ARM) 0 = Secure 1 = Non-Secure	0
GMAC_AxPROT	[8]	RW	Secure Transaction (AxPROT[1] between GMAC <-> AXI) 0 = Secure 1 = Non-Secure	0
DISP_ARPROT	[7]	RW	Secure Transaction (Display0 & 1) 0 = Secure 1 = Non-Secure	0
VIP_AWPROT	[6]	RW	Secure Transaction (VIP0 & 1) 0 = Secure 1 = Non-Secure	0
SCALER_AxPROT	[5]	RW	Secure Transaction 0 = Secure 1 = Non-Secure	0
CODAS_AxPROT	[4]	RW	Secure Transaction 0 = Secure 1 = Non-Secure	0
CODAP_AxPROT	[3]	RW	Secure Transaction 0 = Secure 1 = Non-Secure	0
DEINT _AxPROT	[2]	RW	Secure Transaction 0 = Secure 1 = Non-Secure	0
T2B_AxPROT	[1]	RW	Secure Transaction 0 = Secure 1 = Non-Secure	0
MALI_AxPROT	[0]	RW	Secure Transaction1 0 = Secure 1 = Non-Secure	0

4.9.1.2.30 TIEOFFREG29

- Base Address: 0xC001_0000
- Address = Base Address + 1074, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
3D GPU_PP2_NSLEEP	[31:0]	RW	3D GPU PP2 SRAM retention (low active)	FFFFFFFF

4.9.1.2.31 TIEOFFREG30

- Base Address: 0xC001_0000
- Address = Base Address + 1078, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	RW	Reserved	FF
TZPROT_T_M1	[23]	RW	TrustZone Protection (TOP BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_T_M0	[22]	RW	TrustZone Protection (TOP BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M16	[21]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M15	[20]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M14	[19]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M13	[18]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M12	[17]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M11	[16]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M10	[15]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M9	[14]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1

Name	Bit	Type	Description	Reset Value
TZPROT_P_M8	[13]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M7	[12]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M6	[11]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M5	[10]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M4	[9]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M3	[8]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M2	[7]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M1	[6]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_P_M0	[5]	RW	TrustZone Protection (PERI BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_D_DREX	[4]	RW	TrustZone Protection (DISPLAY BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_B_AXISRAM	[3]	RW	TrustZone Protection (BOTTOM BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_B_PBUS	[2]	RW	TrustZone Protection (BOTTOM BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_B_DREX	[1]	RW	TrustZone Protection (BOTTOM BUS) 0 = Secure 1 = Non-Secure	1
TZPROT_B_MCUS	[0]	RW	TrustZone Protection (BOTTOM BUS) 0 = Secure 1 = Non-Secure	1

4.9.1.2.32 TIEOFFREG31

- Base Address: 0xC001_0000
- Address = Base Address + 0x107C, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
3D GPU_PP3_NSLEEP	[31:0]	RW	3D GPU PP3 SRAM retention (low active)	FFFFFFFF

4.9.1.2.33 TIEOFFREG32

- Base Address: 0xC001_0000
- Address = Base Address + 0x1080, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AXI_MASTER_BUS_REMAP	[4:3]	RW	TOP AXI BUS Remap Master Interface - 0 port: Bottom AXI BUS0 0x0000_0000 ~ 0x3FFF_FFFF 0xC000_0000 ~ 0xCFFF_FFFF 0xFFFF_0000 ~ 0xFFFF_FFFF AXI_MASTER_BUS_REMAP[3] 0 = 0x4000_0000 ~ 0xBFFF_FFFF 1 = 0xD000_0000 ~ 0xDFFF_FFFF Master Interface - 1 port: ARM Cortex-A9 ACP Port AXI_MASTER_BUS_REMAP[4] 0 = 0xD000_0000 ~ 0xDFFF_FFFF 1 = 0x4000_0000 ~ 0xBFFF_FFFF	0
AXI_PERI_BUS_SYNCMODEREQm16	[2]	RW	DREX & DDRPHY APB Interface clock synchronizer request	0
AXI_PERI_BUS_SYNCMODEREQm10	[1]	RW	CODA APB Interface clock synchronizer request	0
AXI_PERI_BUS_SYNCMODEREQm9	[0]	RW	3D GPU AXI (Peripheral interface) Interface clock synchronizer request	0

4.9.1.3 IP Reset

- Base Address: 0xC001_2000

Register	Offset	Description	Reset Value
IP RESET REGISTER 0	000h		0x0000_0000
IP RESET REGISTER 1	004h		0x0000_0000
IP RESET REGISTER 2	008h		0x0000_0000

4.9.1.3.1 IP RESET REGISTER 0

- Base Address: 0xC001_0000
- Address = Base Address + 2000h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MIPITOP_i_PHY_S_RESETN	[31]	RW	MIPI D-PHY Slave channel Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
MIPITOP_i_CSI_I_PRESETn	[30]	RW	MIPI CSI SlaveReset (Active Low) 0 = Reset 1 = No Reset	1'b0
MIPITOP_i_DSI_I_PRESETn	[29]	RW	MIPI DSI MasterReset (Active Low) 0 = Reset 1 = No Reset	1'b0
MIPITOP_i_nRST	[28]	RW	MIPI Register InterfaceReset (Active Low) 0 = Reset 1 = No Reset	1'b0
MCUYZTOP_nPRST	[27]	RW	Memory Controller Core Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
MCUYZTOP_ARESETn	[26]	RW	Memory Controller AXI Interface Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
MCUYZTOP_CRESETn	[25]	RW	Memory Controller APB Interface Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
I2S2_PRESETn	[24]	RW	I2S2 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
I2S1_PRESETn	[23]	RW	I2S1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
I2S0_PRESETn	[22]	RW	I2S0 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0

Name	Bit	Type	Description	Reset Value
I2C2_PRESETn	[21]	RW	I2C2 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
I2C1_PRESETn	[20]	RW	I2C1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
I2C0_PRESETn	[19]	RW	I2C0 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
DisplayTop_i_LVDS_nRST	[18]	RW	LVDS PHY Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
DisplayTop_i_HDMI_PHY_nRST	[17]	RW	HDMI PHY Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
DisplayTop_i_HDMI_TMDS_nRST	[16]	RW	HDMI LINK TMDS Block Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
DisplayTop_i_HDMI_SPDIF_nRST	[15]	RW	HDMI LINK SPDIF Block Reset (Active Low) 0: Reset 1: No Reset0 = Reset 1 = No Reset	1'b0
DisplayTop_i_HDMI_VIDEO_nRST	[14]	RW	HDMI LINK VIDEO Block Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
DisplayTop_i_HDMI_nRST	[13]	RW	HDMI LINK & CEC Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
RSVD	[12]	RW	**Caution:** This bit should be set to 1	1'b0
RSVD	[11]	RW	**Caution:** This bit should be set to 1	1'b0
DisplayTop_i_DualDisplay_nRST	[10]	RW	Dual Display(MLC & DPC) Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
DisplayTop_i_Top_nRST	[9]	RW	Display Block Total Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
DEINTERLACE_i_nRST	[8]	RW	Deinterlace Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
Crypto_i_nRST	[7]	RW	Crypto Engine Reset (Active Low)	1'b0

Name	Bit	Type	Description	Reset Value
			0 = Reset 1 = No Reset	
ARMTOP_nWDRESET3	[6]	RW	Watch Dog Timer 3 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
ARMTOP_nWDRESET2	[5]	RW	Watch Dog Timer 2 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
ARMTOP_nWDRESET1	[4]	RW	Watch Dog Timer 1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
ARMTOP_nCPURESET3	[3]	RW	CPU Core 3 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
ARMTOP_nCPURESET2	[2]	RW	CPU Core 2 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
ARMTOP_nCPURESET1	[1]	RW	CPU Core 1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
AC970_PRESETn	[0]	RW	AC97 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0

4.9.1.3.2 IP RESET REGISTER 1

- Base Address: 0xC001_0000
- Address = Base Address + 2004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
gmac0_aresetn_i	[31]	RW	GMAC Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
coda960_i_creset_n	[30]	RW	Multi-Format Video Codec CoreReset (Active Low) 0 = Reset 1 = No Reset	1'b0
coda960_i_preset_n	[29]	RW	Multi-Format Video Codec APB Interface Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
coda960_i_areset_n	[28]	RW	Multi-Format Video Codec AXI Interface Reset (Active Low) 0 = Reset 1 = No Reset	1'b0

Name	Bit	Type	Description	Reset Value
adc_nRST	[27]	RW	ADC Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
WDT00_nPOR	[26]	RW	nRSTOUT Initialization by POReset (Active Low) 0 = Reset 1 = No Reset	1'b0
WDT00_PRESETn	[25]	RW	WDT APB Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
USB20OTG0_i_nRST	[24]	RW	USB2.0 OTG Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
USB20HOST0_i_nRST	[23]	RW	USB2.0 Host Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
RSVD	[22]	RW	Reserved	1'b0
UART04_nUARTRST	[21]	RW	UART4 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
UART03_nUARTRST	[20]	RW	UART3 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
UART02_nUARTRST	[19]	RW	UART2 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
UART01_nUARTRST	[18]	RW	UART1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
UART00_nUARTRST	[17]	RW	UART0 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SSP2_nSSPRST	[16]	RW	SSP2 Core Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SSP2_PRESETn	[15]	RW	SSP2 APB Interface Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SSP1_nSSPRST	[14]	RW	SSP1 Core Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SSP1_PRESETn	[13]	RW	SSP1 APB Interface Reset (Active Low) 0 = Reset 1 = No Reset	1'b0

Name	Bit	Type	Description	Reset Value
SSP0_nSSPRST	[12]	RW	SSP0 Core Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SSP0_PRESETn	[11]	RW	SSP0 APB Interface Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SPDIFTX00_PRESETn	[10]	RW	SPDIFTX Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SPDIFRX00_PRESETn	[9]	RW	SPDIFRX Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SDMMC2_i_nRST	[8]	RW	SDMMC Controller 2 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SDMMC1_i_nRST	[7]	RW	SDMMC Controller 1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SDMMC0_i_nRST	[6]	RW	SDMMC Controller 0 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
SCALER_i_nRST	[5]	RW	Scaller Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
PWMTIMER1_PRESETn	[4]	RW	PWMTIMER1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
PWMTIMER0_PRESETn	[3]	RW	PWMTIMER0 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
PDM_i_nRST	[2]	RW	PDM Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
MPEGTSI00_i_nRST	[1]	RW	MPEG-TSI Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
MIPITOP_i_PHY_M_RESETN	[0]	RW	MIPI D-PHY Master Channel Reset (Active Low) 0 = Reset 1 = No Reset	1'b0

4.9.1.3.3 IP RESET REGISTER 2

- Base Address: 0xC001_0000
- Address = Base Address + 2008h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	28'b0
vip001_i_nRST	[3]	RW	VIP Controller 1 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
vip000_i_nRST	[2]	RW	VIP Controller 0 Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
ppm_i_nRST	[1]	RW	PPM Reset (Active Low) 0 = Reset 1 = No Reset	1'b0
3D GPU_nRST	[0]	RW	3D GPUReset (Active Low) 0 = Reset 1 = No Reset	1'b0

4.9.1.4 AXI BUS

- Bottom AXI BUS base address: 0xC0050000
- TOP AXI BUS base address: 0xC0052000
- DISPLAY AXI BUS base address: 0xC005E000

Offset	Type	Name	Description	Reset Value
0x400a	RW	QoS_tidemark_MI0	QoS tidemark for MI 0	0x00000000
0x404b	RW	QoS_control_MI0	QoS access control for MI 0	0x00000000
0x408c	RW	AR_arbitration_MI0	AR channel arbitration value for MI 0	Configured
0x40Cd	RW	AW_arbitration_MI0	AW channel arbitration value for MI 0	Configured

1. Address allocation for QoS tidemark Register is 0x400 + 0x20×N, where N is the number of the relevant MI.
2. Address allocation for QoS access control Register is 0x404 + 0x20×N, where N is the number of the relevant MI.
3. Address allocation for AR channel arbitration control registers is 0x408 + 0x20×N, where N is the number of the relevant MI.
4. Address allocation for AW channel arbitration control registers is 0x40C + 0x20×N, where N is the number of the relevant MI.

4.9.1.4.1 Programmable Quality of Service (ProgQoS)

- Address map

The register space for the MIs starts at 0x400 and extends to 0x7FC.
Each MI that is configured to support QoS filtering contains the registers at the following offsets:

- 0x0: QoS tidemark Register
- 0x4: QoS access control Register.

When more than one MI with QoS support is included then the MI number controls the register address offset for that MI.

- Qos tidemark Register

You can program this with the number of outstanding transactions that are permitted before the QoS scheme becomes active.

If a value is written to this register that is larger than the combined acceptance capability of the attached slave, then the QoS scheme never becomes active for this MI. If a value of 0 is written to this register, then the QoS scheme is turned off for this MI. This behavior ensures that it is impossible to block all transactions completely by accidental mis-programming.

If you access a QoS tidemark Register for an MI that has not been configured to support QoS then the HPM ignores writes and reads are undefined.

- Qos access control Register

A 1 in any bit of this register indicates that the SI corresponding to the bit position is permitted to use the reserved slots of the connected combined acceptance capability of the slaves.

The maximum value that you can write to this register is 2^<total number of SIs>^ -1.

NOTE: If you attempt to write a value containing 1s in positions that do not correspond to SIs, then these bits are ignored and are not set in the register.

Changes to these values occur on the first possible arbitration time after they are written.

If you access a QoS access control Register for an MI that has not been configured to support QoS then the HPM ignores writes and reads are undefined.

4.9.1.4.2 Arbitration control

The arbitration schemes for the AR channel and AW channel are set when you configure the HPM, and they control the arbitration scheme for these channels when the HPM exits from reset. However, the HPM enables you to change the AR channel and AW channel arbitration schemes by using the APB SI on the HPM to write to the arbitration control registers.

The HPM provides two arbitration control registers per MI, one for the AR channel and one for the AW channel. They operate and are programmed in the same way.

As the address map does not have sufficient space for each value to be addressable separately, some addressing information is encoded in the write data when updating values. When reading registers the extra addressing information is supplied by a preliminary write command before the read command.

NOTE: When a master interface has connections to only one slave interface its operation is much simpler and as a result the arbitration mechanism is removed. If you attempt to configure or interrogate the arbitration mechanism for such a master interface, all writes are ignored, and each read returns zero.

- Programmable RR arbitration scheme

The following sections describe how to program and read the values for the programmable RR arbitration scheme:

- Writing configuration values
- Reading configuration values

Writing configuration values

When the programmable RR scheme is selected for a master interface then each of its arbitration slots can have the slave interface associated with it changed.

Table 4-16 Bit Assignment for Writing Master Interface Channel Arbitration Values

Bit	Name	Description
[31:24]	slot_number	Arbitration slot number
[23:8]	reserved	Set to 0x0000
[7:0]	slave_interface_num	Slave interface number

NOTE: No protection is imposed when you program the slots in the programmable RR arbitration scheme. So it is possible for you to remove a slave interface from all the slots which would make that slave interface inaccessible. However, if the mechanism for programming the configuration registers uses the interconnect, it is possible to make the configuration mechanism itself inaccessible.

Reading configuration values

You must perform a write followed by a read operation to the same address. The write transfer sets the slot number to be read for that master interface. The following read operation returns the slave interface that is associated with that slot number.

Table 4-17 lists the bit assignments of the preliminary write operation.

Table 4-17 Preliminary write Bit Assignment for an Arbitration Register Read Operation

Bit	Name	Description
[31:24]	reserved	Set to 0xFF
[23:8]	reserved	Set to 0x0000
[7:0]	slot_number	These bits set the slot number for the following read operation

The format of the read data returned has the slave interface number associated with the addressed slot in bits [7:0]. All other bits are set to zero.

Table 4-18 lists the bit assignments of the arbitration read operation.

Table 4-18 Bit Assignment for an Arbitration Register Read Operation

Bit	Name	Description
[31:8]	reserved	These bits read as zero
[7:0]	interface_number	Slave interface number associated with the addressed slot number

5 Clock Generator

5.1 IP Clock Generator Overview

The IP Clock Generator can generate divided clock. Each IP have clocking scheme which requires several different division ratio simultaneously. Therefore, each of IP Clock Generator supplies required clock to each IP. These IP Clock Generators uses the PLL from SYSCTRL or External Clock from PAD. And it can divide required clock of each IP by 2-n divider.

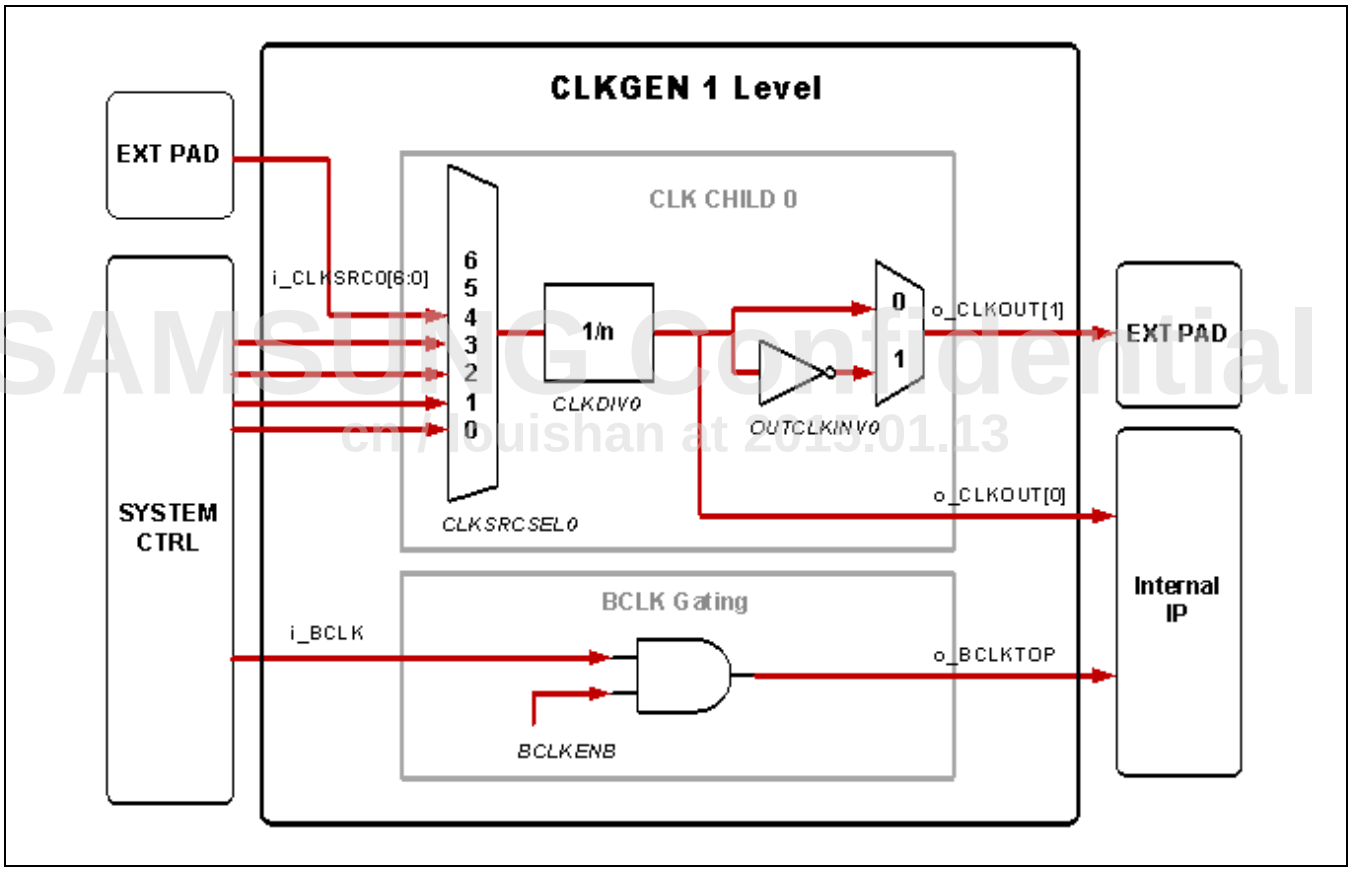


Figure 5-1 Interconnection Example of Clock Generator

5.1.1 Clock Generator Level 0

Clock Generator Level 0 does not have clock divider. It can only do clock gating. It uses PCLK or BCLK Gating.

- Following peripherals use Level 0 Clock Generator:
  - CODA960
  - Crypto
  - I2C
  - 3D GPU
  - MPEGTSI
  - PDM
  - SCALLER
  - DEINTERLACE
  - MLC

5.1.1.1 Block Diagram

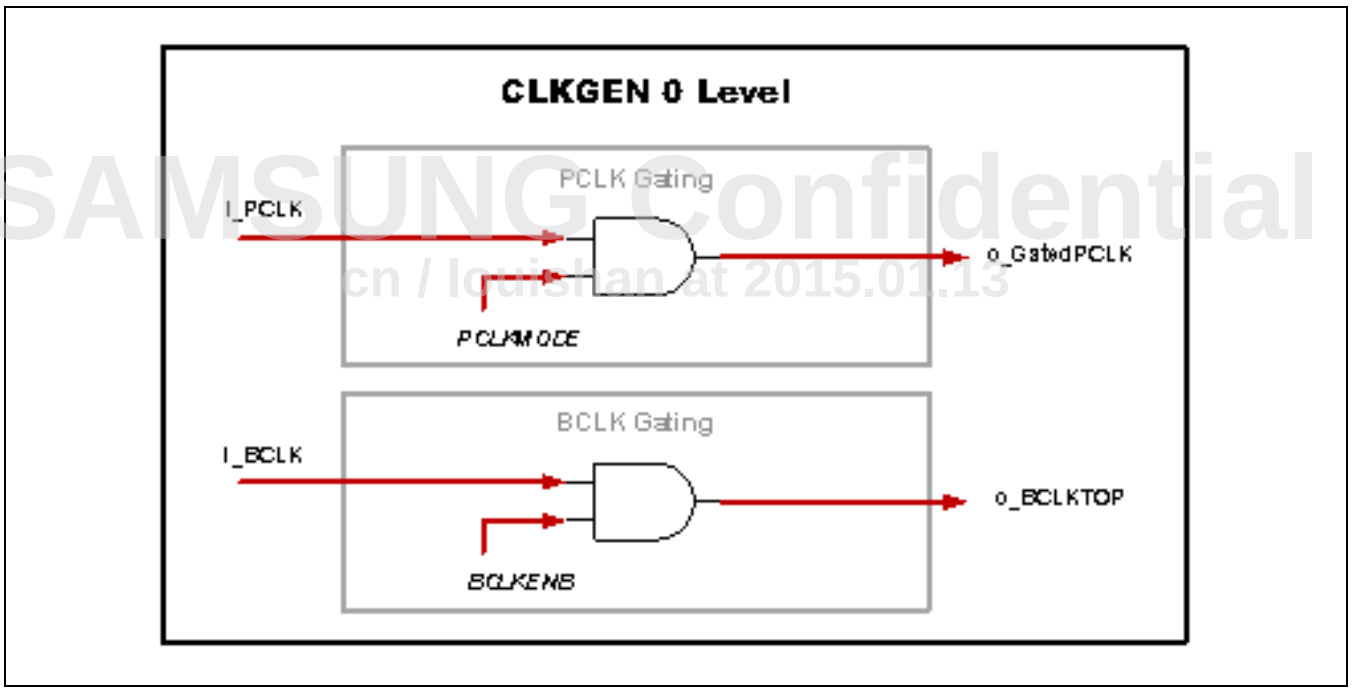


Figure 5-2 Block Diagram of Clock Generator Level 0

5.1.1.2 Register Map Summary

Register	Offset	Description	Reset Value
• Base Address: 0xC00C_0000			
CODA960CLKENB	0x7000	Clock Generator for CODA960 Enable Register	0x0000_0000
CRYPTOCLKENB	0x6000	Clock Generator for CRYPTO Enable Register	0x0000_0000
• Base Address: 0xC00A_0000 • Base Address: 0xC00B_0000			
I2CCLKENB	0xE000, 0xF000	Clock Generator for I2C ch0/1 Enable Register	0x0000_0000
	0x0000	Clock Generator for I2C ch2 Enable Register	0x0000_0000
• Base Address: 0xC00C_0000			
3D GPUCLKENB	0x3000	Clock Generator for 3D GPU Enable Register	0x0000_0000
MPEGTSICLKENB	0xB700	Clock Generator for MPEG-TS Enable Register	0x0000_0000
PDMCLKENB	0xB000	Clock Generator for PDM Enable Register	0x0000_0000
• Base Address: 0xC00B_0000			
SCALERCLKENB	0x6000	Clock Generator for SCALER Enable Register	0x0000_0000
DEINTERLACECLKENB	0x5000	Clock Generator for DEINTERLACE Enable Register	0x0000_0000
• Base Address: 0xC010_0000			
MLCCLKENB	0x23C0, 0x27C0	Clock Generator for MLC Enable Register	0x0000_0000

5.1.1.2.1 CODA960CLKENB

- Base Address: 0xC00C_7000
- Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
BCLKENB	[2:0]	R	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	2'b0

5.1.1.2.2 CRYPTOCLKENB

- Base Address: 0xC00C_6000
- Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
RSVD	[2:0]	R	Reserved	2'b0

5.1.1.2.3 I2CCLKENB

- Base Address: 0xC00A_E000, 0xC00A_F000
  Address = Base Address + 0x00, 0x00, Reset Value = 0x0000_0000
- Base Address: 0xC00B_0000
  Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
RSVD	[3:0]	R	Reserved	3'b0

5.1.1.2.4 3D GPUCLKENB

- Base Address: 0xC00C_3000
- Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved	30'b0
BCLKENB	[1:0]	R	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	2'b0

5.1.1.2.5 MPEGTSICLKENB

- Base Address: 0xC00C_B000
- Address = Base Address + 0x700, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved	30'b0
BCLKENB	[1:0]	R	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	2'b0

5.1.1.2.6 PDMCLKENB

- Base Address: 0xC00C_B000
- Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Reserved	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
BCLKENB	[2:0]	R	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	3'b0

5.1.1.2.7 SCALERCLKENB

- Base Address: 0xC00B_6000
- Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved	30'b0
BCLKENB	[1:0]	R	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	2'b0

5.1.1.2.8 DEINTERLACECLKENB

- Base Address: 0xC00B_5000
- Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved	30'b0
BCLKENB	[1:0]	R	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	2'b0

5.1.1.2.9 MLCCLKENB

- Base Address: 0xC010_2000
- Address = Base Address + 0x3C0, 0x7C0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
RSVD	[2]	R	Reserved	1'b0
BCLKENB	[1:0]	R	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	2'b0

5.1.2 Clock Generator Level 1

The Clock Generator Level-1 has one clock divider. Clock Divider has 8-bit divide registers. Divide registers can reach to 256 levels and it can divide up to 256 levels.

- Following peripherals use Level 1 Clock Generator:
  - MIPICSI
  - PPM
  - PWMTIMER
  - SDMMC
  - SPDIFTX
  - SSP
  - UART
  - VIP

5.1.2.1 Block Diagram

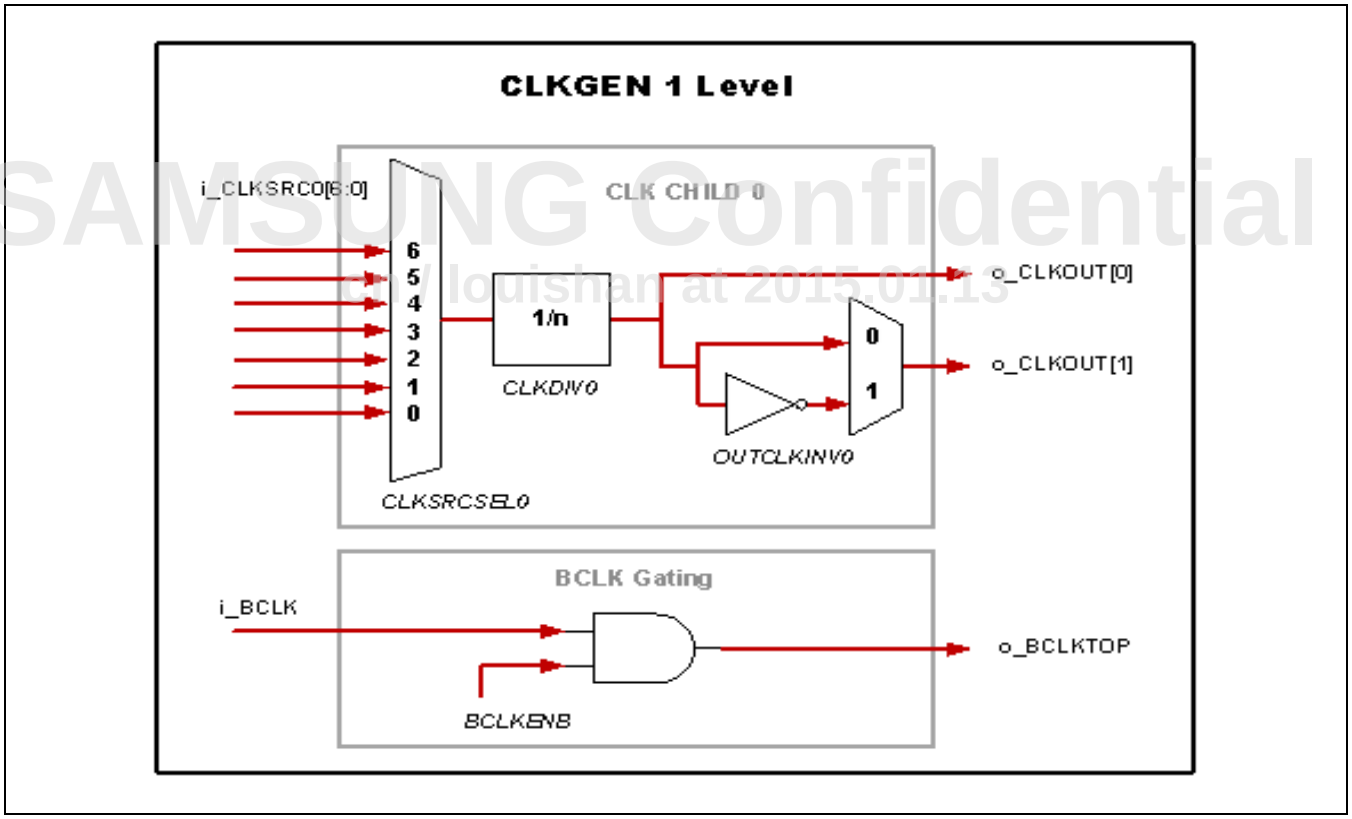


Figure 5-3 Block Diagram of Clock Generator Level 1

5.1.2.2 Register Map Summary

Register	Offset	Description	Reset Value
• Base Address: 0xC00C_0000			
MIPICSICLKENB	0xA000	Clock Generator Enable Register for MIPI CSI	0x0000_0000
MIPICSICLKGEN0L	0xA004	Clock Generator Control 0 Low Register for MIPI CSI	0x0000_0000
PPMCLKENB	0x4000	Clock Generator Enable Register for PPM	0x0000_0000
PPMCLKGEN0L	0x4004	Clock Generator Control 0 Low Register for PPM	0x0000_0000
• Base Address: 0xC00B_0000 (PWM, TIMER) • Base Address: 0xC00C_0000 (PWM)			
PWMTIMERCLKENB (PWM)	0xA000, 0xE000, 0xF000 0xC00C_0000	Clock Generator Enable Register for PWM	0x0000_0000
PWMTIMERCLKENB (TIMER)	0x9000, 0xB000, 0xC000, 0xD000	Clock Generator Enable Register for TIMER	0x0000_0000
PWMTIMERCLKGEN0L (PWM)	0xA004, 0xE004, 0xF004 0xC00C_0004	Clock Generator Control 0 Low Register for PWM	0x0000_0000
PWMTIMERCLKGEN0L (TIMER)	0x9004, 0xB004, 0xC004, 0xD004	Clock Generator Control 0 Low Register for TIMER	0x0000_0000
• Base Address: 0xC00C_0000			
SDMMCCLKENB	0x5000, 0xC000, 0xD000	Clock Generator Control 0 Low Register for SDMMC	0x0000_0000
SDMMCCLKGEN0L	0x5004, 0xC004, 0xD004	Clock Generator Control 0 Low Register for SDMMC	0x0000_0000
• Base Address: 0xC00B_0000			
SPDIFTXCLKENB	0x8000	Clock Generator Control 0 Low Register for SPDIF	0x0000_0000
SPDIFTXCLKGEN0L	0x8004	Clock Generator Control 0 Low Register for SPDIF	0x0000_0000
• Base Address: 0xC00A_0000			
SSPCLKENB	0xC000, 0xD000, 0x7000	Clock Generator Control 0 Low Register for SSP	0x0000_0000
SSPCLKGEN0L	0xC004, 0xD004,	Clock Generator Control 0 Low Register for SSP	0x0000_0000

Register	Offset	Description	Reset Value
	0x7004		
• Base Address: 0xC00A_0000 • Base Address: 0xC006_0000 • Base Address: 0xC008_0000			
UARTCLKENB	0x9000, 0x8000, 0xA000, 0xB000	Clock Generator Control 0 Low Register for UART	0x0000_0000
	0xE000		
	0x4000		
UARTCLKGEN0L	0x9004, 0x8004, 0xA004, 0xB004	Clock Generator Control 0 Low Register for UART	0x0000_0000
	0xE004		
	0x4004		
• Base Address: 0xC00C_0000			
VIPCLKENB	0x1000, 0x2000,	Clock Generator Control 0 Low Register for VIP	0x0000_0000
VIPCLKGEN0L	0x1004, 0x2004,	Clock Generator Control 0 Low Register for VIP	0x0000_0000

5.1.2.2.1 MIPICSICLKENB

- Base Address: 0xC00C_0000
- Address = Base Address + 0xA000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.2.2.2 MIPICSICLKGEN0L

- Base Address: 0xC00C_0000
- Address = Base Address + 0xA004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.2.2.3 PPMCLKENB

- Base Address: 0xC00C_0000
- Address = Base Address + 0x4000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.2.2.4 PPMCLKGEN0L

- Base Address: 0xC00C_0000
- Address = Base Address + 0x4004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.2.2.5 PWMTIMERCLKENB

- Base Address: 0xC00B_0000 (PWM, TIMER)
- Base Address: 0xC00C_0000 (PWM)
- Address = Base Address + 0xA000, 0xE000, 0xF000, 0xC00C_0000 (PWM), Reset Value = 0x0000_0000
- Address = Base Address + 0x9000, 0xB000, 0xC000, 0xD000 (TIMER), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.2.2.6 PWMTIMERCLKGEN0L

- Base Address: 0xC00B_0000 (PWM, TIMER)
- Base Address: 0xC00C_0000 (PWM)
- Address = Base Address + 0xA004, 0xE004, 0xF004, 0xC00C_0004 (PWM), Reset Value = 0x0000_0000
- Address = Base Address + 0x9004, 0xB004, 0xC004, 0xD004 (TIMER), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to `0')	1'b0

5.1.2.2.7 SDMMCCLKENB

- Base Address: 0xC00C_0000
- Address = Base Address + 0x5000, 0xC000, 0xD000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.2.2.8 SDMMCCLKGEN0L

- Base Address: 0xC00C_0000
- Address = Base Address + 0x5004, 0xC004, 0xD004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to `0')	1'b0

5.1.2.2.9 SPDIFTXCLKENB

- Base Address: 0xC00B_0000
- Address = Base Address + 0x8000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.2.2.10 SPDIFTXCLKGEN0L

- Base Address: 0xC00B_0000
- Address = Base Address + 0x8004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to `0')	1'b0

5.1.2.2.11 SSPCLKENB

- Base Address: 0xC00A_0000
- Address = Base Address + 0xC000, 0xD000, 0x7000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.2.2.12 SSPCLKGEN0L

- Base Address: 0xC00A_0000
- Address = Base Address + 0xC004, 0xD004, 0x7004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to `0')	1'b0

5.1.2.2.13 UARTCLKENB

- Base Address: 0xC00A_0000
  Address = Base Address + 0x9000, 0x8000, 0xA000, 0xB000, Reset Value = 0x0000_0000
- Base Address: 0xC006_0000
  Address = Base Address + 0xE000, Reset Value = 0x0000_0000
- Base Address: 0xC008_0000
  Address = Base Address + 0x4000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.2.2.14 UARTCLKGEN0L

- Base Address: 0xC00A_0000
  Address = Base Address + 0x9004, 0x8004, 0xA004, 0xB004, Reset Value = 0x0000_0000
- Base Address: 0xC006_0000
  Address = Base Address + 0xE004, Reset Value = 0x0000_0000
- Base Address: 0xC008_0000
  Address = Base Address + 0x4004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to `0')	1'b0

5.1.2.2.15 VIPCLKENB

- Base Address: 0xC00C_0000
- Address = Base Address + 0x1000, 0x2000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
BCLKENB	[1:0]	RW	BCLK Enable 0 = Disable 1 = Reserved 2 = Reserved 3 = Always	2'b0

5.1.2.2.16 VIPCLKGEN0L

- Base Address: 0xC00C_0000
- Address = Base Address + 0x1004, 0x2004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = CIS External Clock 0 5 = CIS External Clock 1	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to `0')	1'b0

5.1.3 Clock Generator Level 2

The Clock Generator Level2 has two clock dividers. Clock Divider has 8-bit divide registers. And each divide registers can reach to 256 levels and it can divide up to 256 levels. The two clock divider is serialized. Therefore Clock Generator Level-2 can divide up to 65,536.

- Following peripherals use Level 2 Clock Generator:
  - GMAC
  - I2S
  - USBHOSTOTG
  - DPC
  - LVDS
  - HDMI
  - MIPIDSI

5.1.3.1 Block Diagram

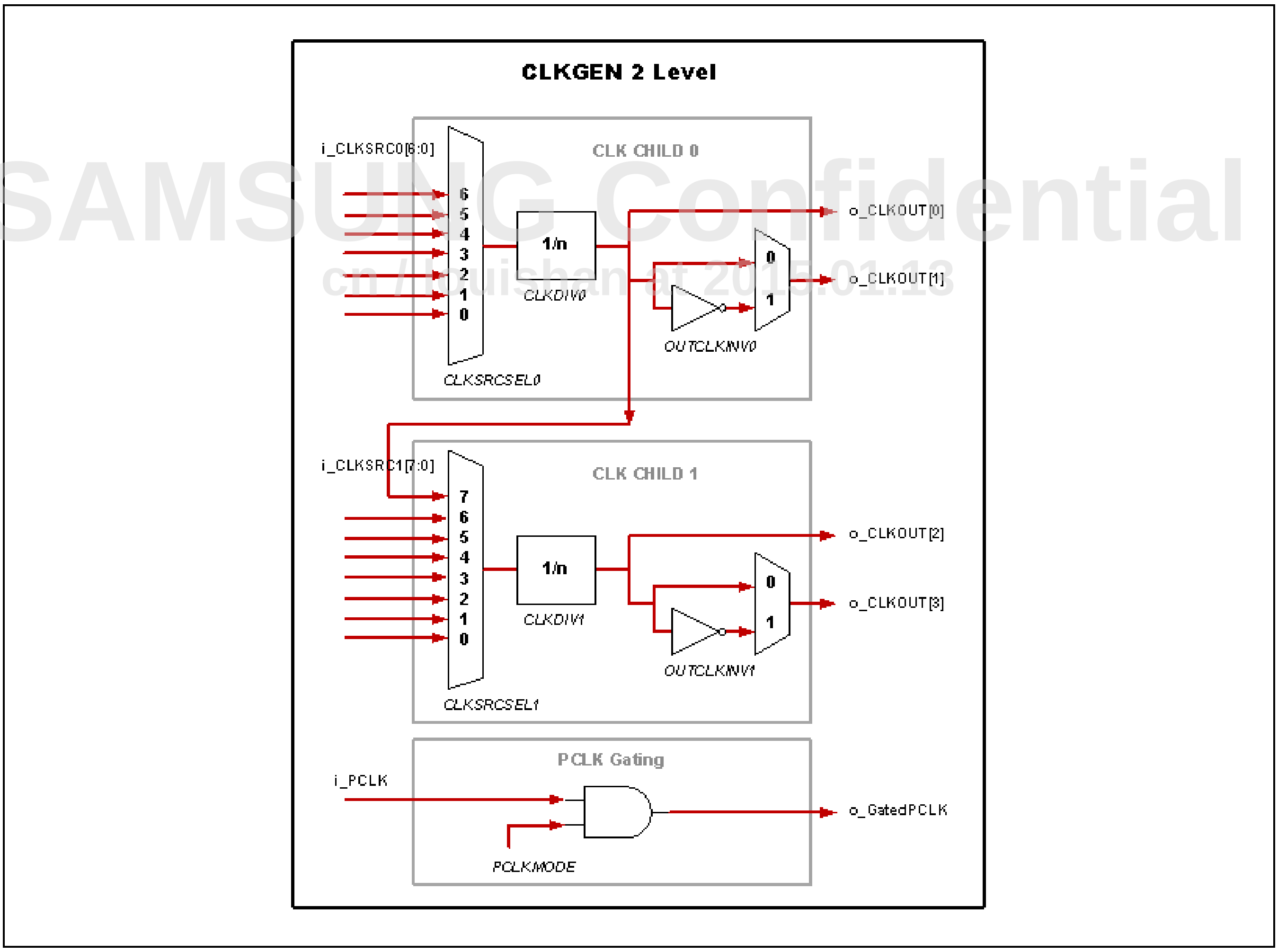


Figure 5-4 Block Diagram of Clock Generator Level 2

5.1.3.2 Register Map Summary

Register	Offset	Description	Reset Value
• Base Address: 0xC00C_0000			
GMACCLKENB	0x8000	Clock Generator Enable Register for GMAC	0x0000_0000
GMACCLKGEN0L	0x8004	Clock Generator Control 0 Low Register for GMAC	0x0000_0000
RSVD	0x8008	Reserved	0x0000_0000
GMACCLKGEN1L	0x800C	Clock Generator Control 1 Low Register for GMAC	0x0000_0000
• Base Address: 0xC00B_0000			
I2SCLKENB	0x2000, 0x3000, 0x4000,	Clock Generator Enable Register for I2S	0x0000_0000
I2SCLKGEN0L	0x2004, 0x3004, 0x4004,	Clock Generator Control 0 Low Register for I2S	0x0000_0000
RSVD	0x2008, 0x3008, 0x4008,	Reserved	0x0000_0000
I2SCLKGEN1L	0x200C, 0x300C, 0x400C,	Clock Generator Control 1 Low Register for I2S	0x0000_0000
• Base Address: 0xC006_0000			
USBHOSTOTGCLKENB	0xB000	Clock Generator Enable Register for USBHOSTOTG	0x0000_0000
USBHOSTOTGCLKGEN0L	0xB004	Clock Generator Control 0 Low Register for USBHOSTOTG	0x0000_0000
RSVD	0xB008		0x0000_0000
USBHOSTOTGCLKGEN1L	0xB00C	Clock Generator Control 1 Low Register for USBHOSTOTG	0x0000_0000
• Base Address: 0xC010_0000			
DPCCLKENB	0x2BC0, 0x2FC0	Clock Generator Enable Register for DPC	0x0000_0000
DPCCLKGEN0L	0x2BC4, 0x2FC4	Clock Generator Control 0 Low Register for DPC	0x0000_0000
RSVD	0x2BC8, 0x2FC8	Reserved	0x0000_0000
DPCCLKGEN1L	0x2BCC, 0x2FCC	Clock Generator Control 1 Low Register for DPC	0x0000_0000
LVDSCLKENB	0x8000	Clock Generator Enable Register for LVDS	0x0000_0000
LVDSCLKGEN0L	0x8004	Clock Generator Control 0 Low Register for LVDS	0x0000_0000
RSVD	0x8008	Reserved	0x0000_0000
LVDSCLKGEN1L	0x800C	Clock Generator Control 1 Low Register for LVDS	0x0000_0000
HDMICLKENB	0x9000	Clock Generator Enable Register for HDMI	0x0000_0000

Register	Offset	Description	Reset Value
HDMICLKGEN0L	0x9004	Clock Generator Control 0 Low Register for HDMI	0x0000_0000
RSVD	0x9008	Reserved	0x0000_0000
HDMICLKGEN1L	0x900C	Clock Generator Control 1 Low Register for HDMI	0x0000_0000
MIPIDSICLKENB	0x5000	Clock Generator Enable Register for MIPI	0x0000_0000
MIPIDSICLKGEN0L	0x5004	Clock Generator Control 0 Low Register for MIPI	0x0000_0000
RSVD	0x5008	Reserved	0x0000_0000
MIPIDSICLKGEN1L	0x500C	Clock Generator Control 1 Low Register for MIPI	0x0000_0000

5.1.3.2.1 GMACCLKENB

- Base Address: 0xC00C_0000
- Address = Base Address + 0x8000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.3.2.2 GMACCLKGEN0L

- Base Address: 0xC00C_0000
- Address = Base Address + 0x8004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = External RX Clock	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.3.2.3 GMACCLKGEN1L

- Base Address: 0xC00C_0000
- Address = Base Address + 0x800C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	0 = Reserved 1 = Reserved 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Divided Clock from Divider 0	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
OUTCLKSEL	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number 0; Bypass 1 source clock/2 ns	1'b0

5.1.3.2.4 I2SCLKENB

- Base Address: 0xC00B_0000
- Address = Base Address + 0x2000, 0x3000, 0x4000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.3.2.5 I2SCLKGEN0L

- Base Address: 0xC00B_0000
- Address = Base Address + 0x2004, 0x3004, 0x4004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = External I2S Codec Clock 2	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to `0')	1'b0

5.1.3.2.6 I2SCLKGEN1L

- Base Address: 0xC00B_0000
- Address = Base Address + 0x200C, 0x300C, 0x400C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	0 = Reserved 1 = Reserved 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = Divided Clock from Divider 0	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
OUTCLKSEL	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number	1'b0

Name	Bit	Type	Description	Reset Value
			0; Bypass 1 source clock/2 ns	

5.1.3.2.7 USBHOSTOTGCLKENB

- Base Address: 0xC006_0000
- Address = Base Address + 0xB000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.3.2.8 USBHOSTOTGCLKGEN0L

- Base Address: 0xC006_0000
- Address = Base Address + 0xB004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.3.2.9 USBHOSTOTGCLKGEN1L

- Base Address: 0xC006_0000
- Address = Base Address + 0xB00C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = External XTI 5 = Reserved 6 = Reserved 7 = Divided Clock from Divider 0	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
OUTCLKSEL	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number 0; Bypass 1 source clock/2 ns	1'b0

5.1.3.2.10 DPCCLKENB

- Base Address: 0xC010_0000
- Address = Base Address + 0x2BC0, 0x2FC0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Reserved	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
Reserved	[1:0]	R	Reserved	2'b0

5.1.3.2.11 DPCCLKGEN0L

- Base Address: 0xC010_0000
- Address = Base Address + 0x2BC4, 0x2FC4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable (Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = Reserved 4 = HDMI PLL Clock 5 = Reserved 6 = PLL[3]	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.3.2.12 DPCCLKGEN1L

- Base Address: 0xC010_0000
- Address = Base Address + 0x2BCC, 0x2FCC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = Reserved 4 = HDMI PLL Clock 5 = Reserved 6 = PLL[3] 7 = Divided Clock from Divider 0	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0

Name	Bit	Type	Description	Reset Value
OUTCLKSEL	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number 0; Bypass 1 source clock/2 ns	1'b0

5.1.3.2.13 LVDSCLKENB

- Base Address: 0xC010_0000
- Address = Base Address + 0x8000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.3.2.14 LVDSCLKGEN0L

- Base Address: 0xC010_0000
- Address = Base Address + 0x8004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable (Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = HDMI PLL Clock 5 = Reserved 6 = Reserved	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0

Name	Bit	Type	Description	Reset Value
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.3.2.15 LVDSCLKGEN1L

- Base Address: 0xC010_0000
- Address = Base Address + 0x800C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Reserved	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = HDMI PLL Clock 5 = Reserved 6 = Reserved 7 = Divided Clock from Divider 0	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
OUTCLKSEL	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number 0; Bypass 1 source clock/2 ns	1'b0

5.1.3.2.16 HDMICLKENB

- Base Address: 0xC010_0000
- Address = Base Address + 0x9000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.3.2.17 HDMICLKGEN0L

- Base Address: 0xC010_0000
- Address = Base Address + 0x9004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable (Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = Reserved 5 = Reserved 6 = Reserved	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.3.2.18 HDMICLKGEN1L

- Base Address: 0xC010_0000
- Address = Base Address + 0x900C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = Reserved 5 = Reserved 6 = Reserved 7 = Divided Clock from Divider 0	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
OUTCLKSEL	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number 0; Bypass 1 source clock/2 ns	1'b0

5.1.3.2.19 MIPIDSICLKENB

- Base Address: 0xC010_0000
- Address = Base Address + 0x5000, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

5.1.3.2.20 MIPIDSICLKGEN0L

- Base Address: 0xC010_0000
- Address = Base Address + 0x5004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable(Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = HDMI PLL Clock 5 = Reserved 6 = Reserved	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

5.1.3.2.21 MIPIDSICLKGEN1L

- Base Address: 0xC010_0000
- Address = Base Address + 0x500C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	0 = PLL[0] 1 = PLL[1] 2 = PLL[2] 3 = PLL[3] 4 = HDMI PLL Clock 5 = Reserved 6 = Reserved 7 = Divided Clock from Divider 0	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0

Name	Bit	Type	Description	Reset Value
OUTCLKSEL	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number 0; Bypass 1 source clock/2 ns	1'b0

6 System L2 Cache (PL-310 L2C)

6.1 Overview

The addition of an on-chip secondary cache, also referred to as a Level 2 or L2 cache, is a recognized method of improving the performance of ARM-based systems when significant memory traffic is generated by the processor. By definition a secondary cache assumes the presence of a Level 1 or primary cache, closely coupled or internal to the processor.

Memory access is fastest to L1 cache, followed closely by L2 cache. Memory access is typically significantly slower with L3 main memory.

6.2 Features

The cache controller features:

- Slave and master AMBA AXI interfaces designed for high performance systems.
- Lockdown format C supported, for data and instructions.
- Lockdown by line supported.
- Lockdown by master ID supported.
- L2 cache available size can be 16 KB to 8 MB, depending on configuration and the use of the lockdown registers.
- Fixed line length of 32 bytes, eight words or 256 bits.
- Interface to data RAM is byte writable.
- Supports all of the AXI cache modes:
  - Write-through and write-back
  - Read allocate, write allocate, read and write allocate.
- Force write allocate option to always have cacheable writes allocated to L2 cache, for processors not supporting this mode.
- Normal memory non-cacheable shared reads are treated as cacheable non-allocatable. Normal memory non-cacheable shared writes are treated as cacheable write-through no write-allocate. There is an option, Shared Override, to override this behavior.
- Critical word first line fill supported.
- Pseudo-Random, or round-robin victim selection policy. You can make this deterministic with use of lockdown registers.
- Four 256-bit Line Fill Buffers (LFBs), shared by the master ports. These buffers capture line fill data from main memory, waiting for a complete line before writing to L2 cache memory.
- Two 256-bit Line Read Buffers (LRBs) for each slave port. These buffers hold a line from the L2 memory for a cache hit.
- Three 256-bit Eviction Buffers (EBs). These buffers hold evicted lines from the L2 cache, to be written back to main memory.
- Three 256-bit Store Buffers (STBs). These buffers hold bufferable writes before their draining to main memory, or the L2 cache. They enable multiple writes to the same line to be merged.
- Software option to enable exclusive cache configuration.
- Configuration registers accessible using address decoding in the slave ports.
- Address filtering in the master ports enabling redirection of a certain address range to one master port while all other addresses are redirected to the other one.

6.3 Block Diagram

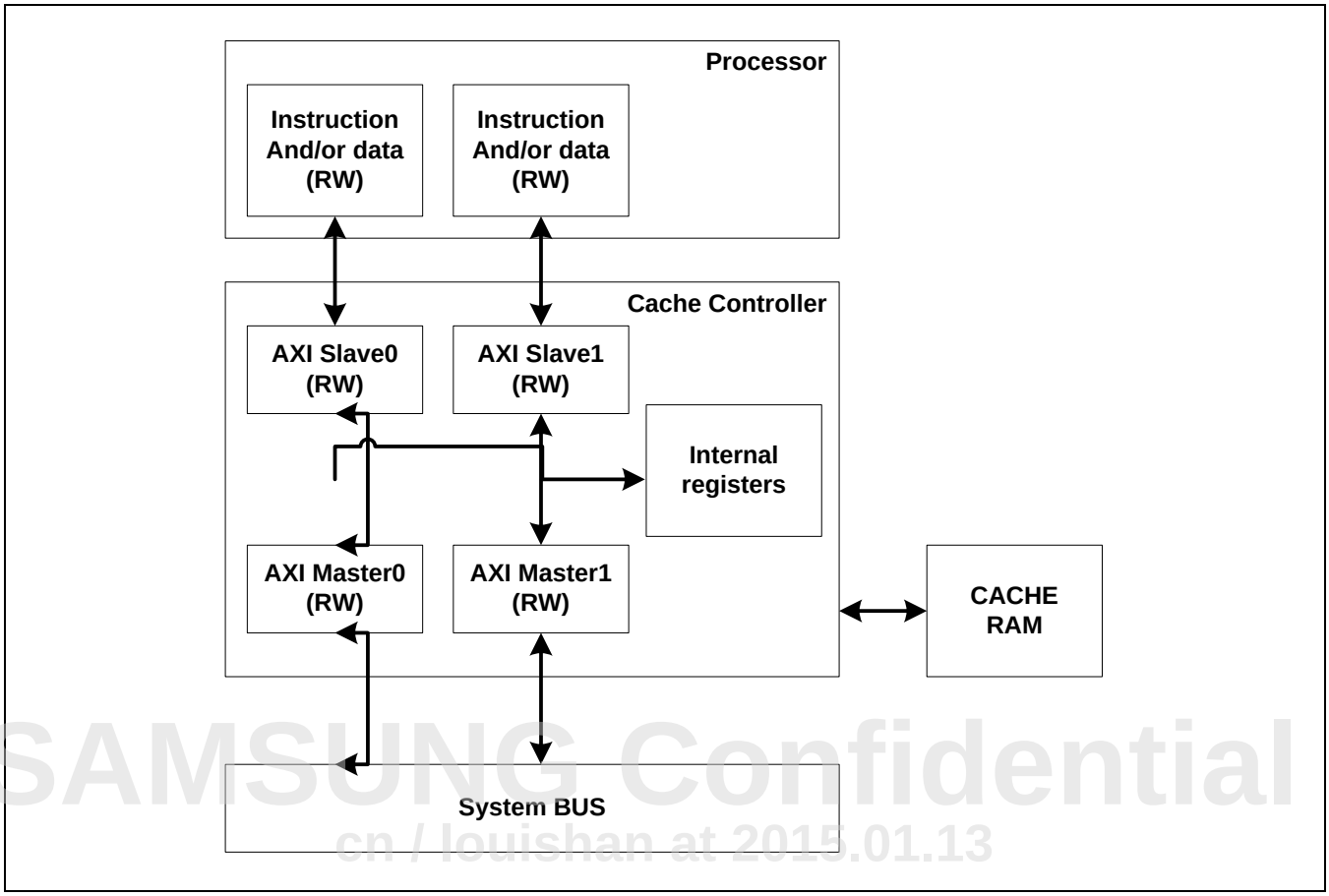


Figure 6-1 System L2 Cache Block Diagram

6.4 Functional Description

6.4.1 L2 Cache User Configure

- System L2 Cache Base Address: Base Address: 0xCF000000
- Turn off and Turn on L2C:
  - Turn off offset 0x100 (Base Address + 0x100) set to 0
  - Turn on offset 0x100 (Base Address + 0x100) set to 1
- Early Write Response:

  The AXI protocol specifies that the write response can only be sent back to an AXI master when the last write data has been accepted. This optimization enables the L2C-310 to send the write response of certain write transactions as soon as the store buffer accepts the write address. This behavior is not compatible with the AXI protocol and is disabled by default. You enable this optimization by setting the Early BRESP Enable bit in the Auxiliary Control Register, bit[30]. The L2C-310 slave ports then send an early write response only if the input signal AWUSERSx[11], x = 0 or 1, is set to 1'b1 for the corresponding write transaction.

6.4.2 Initialization Sequence

As an example, a typical cache controller start-up programming sequence consists of the following register operations:

1. Write to the Auxiliary, Tag RAM Latency, Data RAM Latency, Pre-fetch, and Power Control registers using a read-modify-write to set up global configurations:

- Associativity, Way Size
- latencies for RAM accesses
- allocation policy
- Pre-fetch and power capabilities.

2. Secure write to the Invalidate by Way, offset 0x77C, to invalidate all entries in cache:

- Write 0xFFFF to 0x77C
- Poll cache maintenance register until invalidate operation is complete.

3. Write to the Lockdown D and Lockdown I Register 9 if required.
4. Write to interrupt clear register to clear any residual raw interrupts set.
5. Write to the Interrupt Mask Register if you want to enable interrupts.
6. Write to Control Register 1 with the LSB set to 1 to enable the cache.

If you write to the Auxiliary, Tag RAM Latency, or Data RAM Latency Control Register with the L2 cache enabled, this results in a SLVERR. You must disable the L2 cache by writing to the Control Register 1 before Writing to the Auxiliary, Tag RAM Latency, or Data RAM Latency Control Register.

6.5 Register Description

The base address of the Cache controller is 0xCF000000.

6.5.1.1 Register Map Summary

- Base Address: 0xCF00_0000

Register	Offset	Description	Reset Value
REG0_CACHE_ID	0000h	Cache ID and type Register	0x4100_C4C8
REG0_CACHE_TYPE	0004h	CACHE Type register	0x1A34_0340
REG1_CONTROL	0100h	control register	0x0000_0000
AUX_CONTROL	0104h	aux control register	0x0207_0000
REG1_TAG_RAM_CONTROL/ REG1_DATA_RAM_CONTROL	0108h to 010Ch	tag and data ram control register	0x0000_0777
REG2_EV_COUNTER_CTRL	0200h	event counter control register	0x0000_0000
REG2_EV_COUNTER1_CFG/ REG2_EV_COUNTER0_CFG	0204h to 0208h	event counter configuration register 1, 0	0x0000_0000
REG2_EV_COUNTER1/ REG2_EV_COUNTER0	020Ch to 0210h	event counter registers 1, 0	0x0000_0000
REG2_INT_MASK	0214h	Interrupt mask register	0x0000_0000
REG2_INT_MASK_STATUS	0218h	Interrupt mask STATUS register	0x0000_0000
REG2_INT_RAW_STATUS	021Ch	Interrupt RAW STATUS register	0x0000_0000
REG2_INT_CLEAR	0220h	Interrupt CLEAR register	0x0000_0000
REG7_CACHE_SYNC	0730h	CACHE SYNC	0x0000_0000
REG7_INV_PA	0770h	INVALIDATE line by pa	0x0000_0000
REG7_INV_WAY	077Ch	invalidate by way	0x0000_0000
REG7_CLEAN_PA	07B0h	clean line by pa	0x0000_0000
REG7_CLEAN_INDEX	07B8h	clean line by set/way	0x0000_0000
REG7_CLEAN_WAY	07BCh	clean by way	0x0000_0000
REG7_CLEAN_INV_PA	07F0h	clean and invalidate line by pa	0x0000_0000
REG7_CLEAN_INV_INDEX	07F8h	clean and 07F8h line by set/way	0x0000_0000
REG7_CLEAN_INV_WAY	07FCh	clean and invalidate by way	0x0000_0000
REG9_D_LOCKDOWN0~7	0900h, 0908h, 0910h, 0918h, 0920h, 0928h,	DATA Lockdown 0 to 7	0x0000_0000

Register	Offset	Description	Reset Value
	0930h, 0938h		
REG9_I_LOCKDOWN0~7	0904h, 090Ch, 0914h, 091Ch, 0924h, 092Ch, 0934h, 093Ch	Instruction Lockdown 0 to 7	0x0000_0000
REG9_LOCK_LINE_EN	0950h	lock down by line enable	0x0000_0000
REG9_UNLOCK_WAY	0954h	Unlock lines by way	0x0000_0000
REG12_ADDR_FILTERING_START	0C00h	address filtering start	0x0000_0000
REG12_ADDR_FILTERING_END	0C04h	address filtering end	0x0000_0000
REG15_DEBUG_CTRL	0F40h	debug ctrl	0x0000_0000
REG15_PREFETCH_CTRL	0F60h	prefetch ctrl	0x0000_0004
REG15_POWER_CTRL	0F80h	power ctrl	0x0000_0000

6.5.1.1.1 REG0_CACHE_ID

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0000h, Reset Value = 0x4100_C4C8

Name	Bit	Type	Description	Reset Value
Implementer	[31:24]	R	ARM	0x4100_C4C8
RSVD	[23:16]	R	Reserved	
CACHE ID	[15:10]	R	Cache Controller ID	
Partnum	[9:6]	R	Part number 0x3 denotes Core Link Level 2 Cache Controller L2C-310	
RTL RELEASE	[5:0]	R	RTL release 0x8 denotes r3p2 code of the cache controller.	

6.5.1.1.2 REG0_CACHE_TYPE

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0004h, Reset Value = 0x1A34_0340

Name	Bit	Type	Description	Reset Value
data bank	[31]	R	0 = Data banking not implemented 1 = Data banking implemented	0x1A34_0340
RSVD	[30:29]	R	Reserved	
ctype	[28:25]	R	4'b11xy x=1 if pl310_LOCKDOWN_BY_MASTER is defined, otherwise 0 y=1 if pl310_LOCKDOWN_BY_LINE is defined, otherwise 0	
H	[24]	R	0 = unified 1 = Havard	
dsize	[23:19]	R	[23] SBZ/RAZ [19] SBZ/RAZ	
L2 associativity	[18]	R	Read from Auxiliary Control Register[16]	
RSVD	[17:14]	R	Reserved	
L2 cache line length	[13:12]	R	00 to 32 bytes	
isize	[11:7]	R	[11] SBZ/RAZ [7] SBZ/RAZ	
l2 associativity	[6]	R	Read from Auxiliary Control Register[16]	
reserved	[5:2]	R	Reserved	
L2 cache line length	[1:0]	R	00 to 32 bytes	

6.5.1.1.3 REG1_CONTROL

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0100h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	R	Reserved	0x0000_0000
Enb	[0]	RW	0 = L2 Cache disabled. Default 1 = L2 Cache Enabled	

6.5.1.1.4 AUX_CONTROL

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0104h, Reset Value = 0x0207_0000B

Name	Bit	Type	Description	Reset Value
RSVD	[31]	RW	Reserved	0x0207_0000B
early bresp	[30]	RW	0 = Early BRESP disabled. This is the default. 1 = Early BRESP enabled.	
instruction prefetch enable	[29]	RW	0 = Instruction pre-fetching disabled. This is the default. 1 = Instruction pre-fetching enabled.	
data prefetch enable	[28]	RW	0 = Data pre-fetching disabled. This is the default. 1 = Data pre-fetching enabled.	
ns interrupt access control	[27]	RW	0 = Interrupt Clear, 0x220, and Interrupt Mask, 0x214, can only be modified or read with secure accesses. This is the default. 1 = Interrupt Clear, 0x220, and Interrupt Mask, 0x214, can be modified or read with secure or non-secure accesses.	
ns lockdown	[26]	RW	0 = Lockdown registers cannot be modified using non-secure. This is the default. 1 = Non-secure accesses can write to the lockdown registers.	
cache replacement policy	[25]	RW	0 = Pseudo-random replacement using lfsr. 1 = Round-robin replacement. This is the default.	
force write allocate	[24:23]	RW	0b00 = Use AWCACHE attributes for WA. This is the default. 0b01 = Force no allocate, set WA bit always 0. 0b10 = Override *AWCACHE *attributes, set WA bit always 1, all cacheable write misses become write allocated. 0b11 = Internally mapped to 00.	
shared attribute override enable	[22]	RW	0 = Treats shared accesses. This is the default. 1 = Shared attribute internally ignored.	
parity enable	[21]	RW	0 = Disabled. This is the default.	

Name	Bit	Type	Description	Reset Value
			1 = Enabled.	
event monitor bus enable	[20]	RW	0 = Disabled. This is the default. 1 = Enabled.	
way-size	[19:17]	RW	0b000 = Reserved, internally mapped to 16 KB 0b001 = 16 KB 0b010 = 32 KB 0b011 = 64 KB 0b100 = 128 KB 0b101 = 256 KB 0b110 = 512 KB 0b111 = Reserved, internally mapped to 512 KB	
associativity	[16]	RW	0 = 8-way 1 = 16-way.	
RSVD	[15:14]	RW	SBZ/RAZ	
shared attribute invalidate enable	[13]	RW	0 = Shared invalidate behavior disabled. This is the default. 1 = Shared invalidate behavior enabled, if Shared Attribute Override Enable bit not set.	
exclusive cache configuration	[12]	RW	0 = Disabled. This is the default. 1 = Enabled.	
store buffer device limitation enable	[11]	RW	0 = Store buffer device limitation disabled. Device writes can take all slots in store buffer. This is the default. 1 = Store buffer device limitation enabled. Device writes cannot take all slots in store buffer when connected to the Cortex-A9 MPCore There is always one available slot to service Normal Memory.	
high priority for so and dev reads enable	[10]	RW	0 = Strongly Ordered and Device reads have lower priority than cacheable accesses when arbitrated in the L2CC L2C-310 master This is the default. 1 = Strongly Ordered and Device reads get the highest priority when arbitrated in the L2C-310 master ports.	
RSVD	[9:1]	RW	SBZ/RAZ	
full line of zero enable	[0]	RW	0 = Full line of write zero behavior disabled. This is the default. 1 = Full line of write zero behavior Enabled.	

6.5.1.1.5 REG1_TAG_RAM_CONTROL/ REG1_DATA_RAM_CONTROL

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0108h, 0x010Ch, Reset Value = 0x0000_0777

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	RW	Reserved	0x0000_0777
ram write access latency	[10:8]	RW	Default value depends on the value of pl310_TAG_WRITE_LAT for reg1_tag_ram_control or pl310_DATA_WRITE_LAT for reg1_data_ram_control. 0b000 = 1 cycle of latency, there is no additional latency 0b001 = 2 cycles of latency 0b010 = 3 cycles of latency 0b011 = 4 cycles of latency 0b100 = 5 cycles of latency 0b101 = 6 cycles of latency 0b110 = 7 cycles of latency 0b111 = 8 cycles of latency	
RSVD	[7]	RW	Reserved	
ram read access latency	[6:4]	RW	0b000 = 1 cycle of latency, there is no additional latency 0b001 = 2 cycles of latency 0b010 = 3 cycles of latency 0b011 = 4 cycles of latency 0b100 = 5 cycles of latency 0b101 = 6 cycles of latency 0b110 = 7 cycles of latency 0b111 = 8 cycles of latency	
RSVD	[3]	RW	SBZ/RAZ	
ram setup latency	[2:0]	RW	0b000 = 1 cycle of latency, there is no additional latency 0b001 = 2 cycles of latency 0b010 = 3 cycles of latency 0b011 = 4 cycles of latency 0b100 = 5 cycles of latency 0b101 = 6 cycles of latency 0b110 = 7 cycles of latency 0b111 = 8 cycles of latency	

6.5.1.1.6 REG2_EV_COUNTER_CTRL

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0200h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	RW	SBZ/RAZ	0x0000_0000
counter reset	[2:1]	RW	Always Read as zero. The following counters are reset when a 1 is written to the following bits: bit[2] = Event Counter1 reset bit[1] = Event Counter0 reset.	
event counter enable	[0]	RW	0 = Event Counting Disable. This is the default. 1 = Event Counting Enable.	

6.5.1.1.7 REG2_EV_COUNTER1_CFG/ REG2_EV_COUNTER0_CFG

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0204h, 0x0208h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:6]	RW	Reserved	26'b0
counter event source	[5:2]	RW	Event Encoding Counter Disabled: 0b'0000 CO: 0b'0001 DRHIT: 0b'0010 DRREQ: 0b'0011 DWHIT: 0b'0100 DWREQ: 0b'0101 DWTREQ: 0b'0110 IRHIT: 0b'0111 IRREQ: 0b'1000 WA: 0b'1001 IPFALLOC: 0b'1010 EPFHIT: 0b'1011 EPFALLOC: 0b'1100 SRRCVD: 0b'1101 SRCONF: 0b'1110 EPFRCVD: 0b'1111	4'b0
event counter interrupt generation	[1:0]	RW	0b00 = Disabled. This is the default. 0b01 = Enabled: Increment condition. 0b10 = Enabled: Overflow condition. 0b11 = Interrupt generation is disabled.	2'b0

6.5.1.1.8 REG2_EV_COUNTER1/ REG2_EV_COUNTER0

- Base Address: 0xCF00_0000
- Address = Base Address + 020Ch, 0x0210h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Counter	[31:0]	RW	Total of the event selected. If a counter reaches its maximum value, it saturates at that value until it is reset.	0x0000_0000

6.5.1.1.9 REG2_INT_MASK

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0214h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	RW	Reserved	0x0000_0000
DECERR	[8]	RW	DECERR from L3 0 = Masked, Default 1 = Enabled.	
SLVERR	[7]	RW	SLVERR from L3 0 = Masked, Default 1 = Enabled.	
ERRRD	[6]	RW	Error on L2 data RAM, Read 0 = Masked, Default 1 = Enabled.	
ERRRT	[5]	RW	Error on L2 tag RAM, Read 0 = Masked, Default 1 = Enabled.	
ERRWD	[4]	RW	Error on L2 data RAM, Write 0 = Masked, Default 1 = Enabled.	
ERRWT	[3]	RW	Error on L2 tag RAM, Write 0 = Masked, Default 1 = Enabled.	
PARRD	[2]	RW	Parity Error on L2 data RAM, Read 0 = Masked, Default 1 = Enabled.	
PARRT	[1]	RW	Parity Error on L2 tag RAM, Read 0 = Masked, Default 1 = Enabled.	
ECNTR	[0]	RW	Even Counter1 and Event Counter 0 Overflow Increment 0 = Masked, Default 1 = Enabled.	

6.5.1.1.10 REG2_INT_MASK_STATUS

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0218h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	R	Reserved	0x0000_0000
DECERR	[8]	R	DECERR from L3 HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	
SLVERR	[7]	R	SLVERR from L3 HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	
ERRRD	[6]	R	Error on L2 data RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	
ERRRT	[5]	R	Error on L2 tag RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	
ERRWD	[4]	R	Error on L2 data RAM, Write HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	
ERRWT	[3]	R	Error on L2 tag RAM, Write HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	
PARRD	[2]	R	Parity Error on L2 data RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	
PARRT	[1]	R	Parity Error on L2 tag RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has	

Name	Bit	Type	Description	Reset Value
			been generated, or the interrupt is masked.	
ECNTR	[0]	R	Even Counter1 and Event Counter 0 Overflow Increment HIGH: If the bits read HIGH, they reflect the status of the input lines triggering an interrupt. LOW: If the bits read LOW, either no interrupt has been generated, or the interrupt is masked.	

6.5.1.1.11 REG2_INT_RAW_STATUS

- Base Address: 0xCF00_0000
- Address = Base Address + 0x021Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	R	Reserved	0x0000_0000
DECERR	[8]	R	DECERR from L3 HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	
SLVERR	[7]	R	SLVERR from L3 HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	
ERRRD	[6]	R	Error on L2 data RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	
ERRRT	[5]	R	Error on L2 tag RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	
ERRWD	[4]	R	Error on L2 data RAM, Write HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	
ERRWT	[3]	R	Error on L2 tag RAM, Write HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	

Name	Bit	Type	Description	Reset Value
PARRD	[2]	R	Parity Error on L2 data RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	
PARRT	[1]	R	Parity Error on L2 tag RAM, Read HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	
ECNTR	[0]	R	Even Counter1 and Event Counter 0 Overflow Increment HIGH: If the bits read HIGH, they reflect the status of the input lines riggering an interrupt. LOW: If the bits read LOW, no interrupt has been generated.	

6.5.1.1.12 REG2_INT_CLEAR

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0220h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	W	Reserved	0x0000_0000
DECERR	[8]	W	DECERR from L3 When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
SLVERR	[7]	W	SLVERR from L3 When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
ERRRD	[6]	W	Error on L2 data RAM, Read When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
ERRRT	[5]	W	Error on L2 tag RAM, Read When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
ERRWD	[4]	W	Error on L2 data RAM, Write When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
ERRWT	[3]	W	Error on L2 tag RAM, Write	

Name	Bit	Type	Description	Reset Value
			When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
PARRD	[2]	W	Parity Error on L2 data RAM, Read When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
PARRT	[1]	W	Parity Error on L2 tag RAM, Read When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	
ECNTR	[0]	W	Even Counter1 and Event Counter 0 Overflow Increment When a bit is written as 1, it clears the corresponding bit in the Raw Interrupt Status Register. When a bit is written as 0, it has no effect.	

6.5.1.1.13 REG7_CACHE_SYNC

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0730h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	RW	Reserved	0x0000_0000
cachesync	[0]	RW	Cache SYNC	

6.5.1.1.14 REG7_INV_PA

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0770h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TAG	[31:12]	RW	Tag	0x0000_0000
INDEX	[11:5]	RW	Index	
RSVD	[4:1]	RW	Reserved	
Clean	[0]	RW	Invalidate 0 = Idle 1 = Enable Invalidate	

6.5.1.1.15 REG7_INV_WAY

- Base Address: 0xCF00_0000
- Address = Base Address + 0x077Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
way	[31:28]	RW	Way	0x0000_0000
RSVD	[27:12]	RW	Reserved	
INDEX	[11:5]	RW	Index	
RSVD	[4:1]	RW	Reserved	
Clean	[0]	RW	Invalidate 0 = Idle 1 = Enable Invalidate	

6.5.1.1.16 REG7_CLEAN_PA

- Base Address: 0xCF00_0000
- Address = Base Address + 0x07B0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TAG	[31:12]	RW	Tag	0x0000_0000
INDEX	[11:5]	RW	Index	
RSVD	[4:1]	RW	Reserved	
Clean	[0]	RW	Invalidate 0 = Idle 1 = Enable Invalidate	

6.5.1.1.17 REG7_CLEAN_INDEX

- Base Address: 0xCF00_0000
- Address = Base Address + 0x07B8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
way	[31:28]	RW	Way	0x0000_0000
RSVD	[27:12]	RW	Reserved	
INDEX	[11:5]	RW	Index	
reserved	[4:1]	RW	Reserved	

6.5.1.1.18 REG7_CLEAN_WAY

- Base Address: 0xCF00_0000
- Address = Base Address + 0x07BCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	0x0000_0000
WAY Bits	[15:0]	RW	Way Bits 8WAY: 0xFF 16WAY: 0xFFFF	

6.5.1.1.19 REG7_CLEAN_INV_PA

- Base Address: 0xCF00_0000
- Address = Base Address + 0x07F0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TAG	[31:12]	RW	Tag	0x0000_0000
INDEX	[11:5]	RW	Index	
RSVD	[4:1]	RW	Reserved	
Clean	[0]	RW	Invalidate 0 = Idle 1 = Enable Invalidate	

6.5.1.1.20 REG7_CLEAN_INV_INDEX

- Base Address: 0xCF00_0000
- Address = Base Address + 0x07F8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
way	[31:28]	RW	Way	0x0000_0000
RSVD	[27:12]	RW	Reserved	
INDEX	[11:5]	RW	Index	
RSVD	[4:1]	RW	Reserved	

6.5.1.1.21 REG7_CLEAN_INV_WAY

- Base Address: 0xCF00_0000
- Address = Base Address + 0x07FCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	0x0000_0000
WAY Bits	[15:0]	RW	Way Bits 8WAY: 0xFF 16WAY: 0xFFFF	

6.5.1.1.22 REG9_D_LOCKDOWN 0~7

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0900h, 0x0908h, 0x0910h, 0x0918h, 0x0920h, 0x0928h, 0x0930h, 0x0938h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	0x0000_0000
DATALOCK	[15:0]	RW	Way Bits 8WAY: 0xFF 16WAY: 0xFFFF	

6.5.1.1.23 REG9_I_LOCKDOWN 0~7

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0904h, 0x090Ch, 0x0914h, 0x091Ch, 0x0924h, 0x092Ch, 0x0934h, 0x093Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	0x0000_0000
INSTRLOCK	[15:0]	RW	Way Bits 8WAY: 0xFF 16WAY: 0xFFFF	

6.5.1.1.24 REG9_LOCK_LINE_EN

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0950h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSCD	[31:1]	RW	Reserved	0x0000_0000
LOCKDOWN by LINE ENB	[0]	RW	0 = Lockdown by line disabled. This is default 1 = Lockdown by line enabled	

6.5.1.1.25 REG9_UNLOCK_WAY

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0954h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	0x0000_0000
UNlock all lines by way	[15:0]	RW	For all bits: 0 = Unlock all lines disabled. This is the default 1 = Unlock all lines operation in progress for the corresponding way	

6.5.1.1.26 REG12_ADDR_FILTERING_START

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0C00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
filtering start	[31:20]	RW	Address filtering start address for bits[31:20] of the filtering address	0x0000_0000
RSVD	[19:1]	RW	SBZ/RAZ	
filter enb	[0]	RW	Address filter enable	

6.5.1.1.27 REG12_ADDR_FILTERING_END

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0C04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
filtering start	[31:20]	RW	Address filtering start address for bits[31:20] of the filtering address	0x0000_0000
RSVD	[19:0]	RW	SBZ/RAZ	

6.5.1.1.28 REG15_DEBUG_CTRL

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0F40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	RW	Reserved	0x0000_0000
SPNIDEN	[2]	RW	Reads value of SPNIDEN Input.	
DWB	[1]	RW	Disable Write-back force WT 0 = Enable write-back behavior. This is the default. 1 = Force write-through behavior	
DCL	[0]	RW	Disable cache line fill 0 = Enable cache line fills. This is the default 1 = Disable cache line fills	

6.5.1.1.29 REG15_PREFETCH_CTRL

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0F60h, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
RSVD	[31]	RW	Reserved	0x0000_0004
Double line fill enable	[30]	RW	You can set the following options for this register bit: 0 = The L2CC always issues 4x64-bit read bursts to L3 on reads that miss in the L2cache. This is the default. 1 = The L2CC issues 8x64-bit read bursts to L3 on reads that miss in the L2 cache.	
Instruction prefetch enable	[29]	RW	You can set the following options for this register bit: 0 =: Instruction pre-fetching disabled. This is the default. 1 =: Instruction pre-fetching enabled.	
Data prefetch enable	[28]	RW	You can set the following options for this register bit: 0 = Data pre-fetching disabled. This is the default. 1 = Data pre-fetching enabled.	

Name	Bit	Type	Description	Reset Value
Double line fill on wrap read disable	[27]	RW	You can set the following options for this register bit: 0 = Double line fill on WRAP read enabled. This is the default. 1 = Double line fill on wrap read disabled.	
RSVD	[26:25]	RW	SBZ/RAZ	
prefetch drop enable	[24]	RW	You can set the following options for this register bit: 0 = The L2CC does not discard pre-fetch reads issued to L3. This is default 1 = The L2CC discards pre-fetch reads issued to L3 when there is a resource conflict with explicit reads.	
incr double linefill enable	[23]	RW	0 = The L2CC does not issue INCR 8x64-bit read bursts to L3 on reads that miss in the L2 cache. This is the default. 1 = The L2CC can issue INCR 8x64-bit read bursts to L3 on reads that miss in the L2cache.	
RSVD	[22]	RW	SBZ/RAZ	
Not same ID on exclusive sequence enable	[21]	RW	You can set following options for this register bit: 0 = Read and write portions of a non cacheable exclusive sequence have the same AXI ID when issued to L3. This is the default. 1 = Read and write portions of a non cacheable exclusive sequence do not have the same AXI ID when issued to L3.	
RSVD	[20:5]	RW	SBZ/RAZ	
prefetch offset	[4:0]	RW	Default value = 0b00000 You must only use the pre-fetch offset values of 0-7, 15, 23, and 31 for these bits. The L2C-310 does not support the other values.	

6.5.1.1.30 REG15_POWER_CTRL

- Base Address: 0xCF00_0000
- Address = Base Address + 0x0F80h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	RW	Reserved	0x0000_0000
dynamic_clk_gating	[1]	RW	Dynamic Clock gating Enable. 0 = Disabled. This is the default 1 = Enabled	
stanby mode en	[0]	RW	Standby mode enable. 0 = Disabled. This is the default 1 = Enabled	

7 Secure JTAG

7.1 Overview

The Secure JTAG consists of an Authentication & Authorization module an Access Provider. Secure JTAG Device support protection by user password can be unlocked by providing the correct password. Secure JTAG Connected with CoreSight at AHB AP. To activate the password unlock mechanism, the password exchange request must be applied to the AHB AP of CoreSight.

7.2 Features

The Secure JTAG features: Authentication & Authorization Debug Module.

7.3 Block Diagram

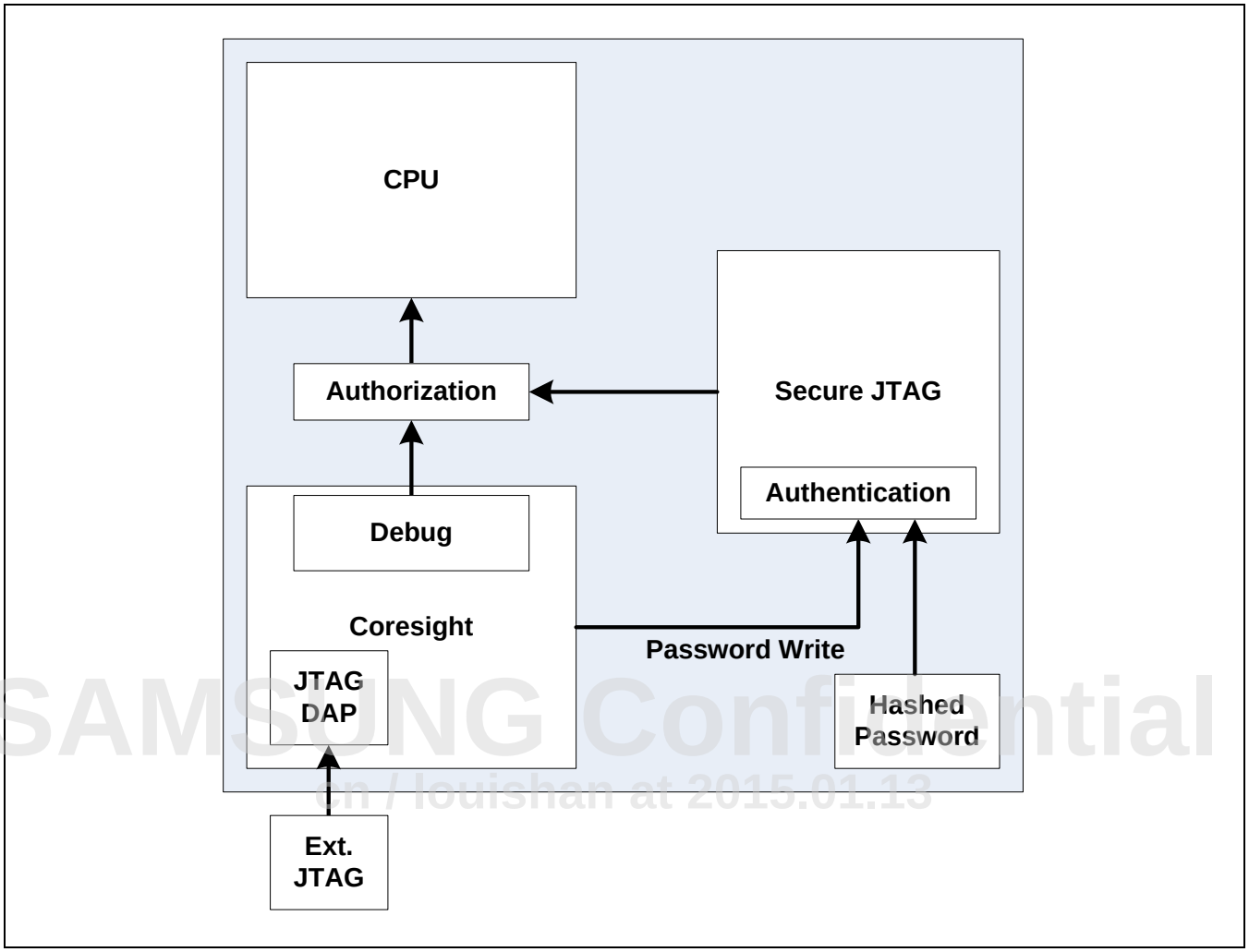


Figure 7-1 Secure JTAG Block Diagram

7.4 Secure JTAG User Configure

System L2 Cache Base Address: JTAG AHB-AP BASE Address 0x00000000

8 DMA

8.1 Overview

The DMA Controller (DMAC) is an Advanced Microcontroller Bus Architecture (AMBA) block that connects to the Advanced High-performance Bus (AHB). There is an AHB slave interface for programming the DMAC and 2 AHB masters for data transfer. There are two DMAC in S5P4418 and each DMAC has eight channels, which can buffer up to 4 words each. Each channel can transfer data through either of the AHB Master interfaces with the programmed data width and endianness. The DMAC supports 16 DMA requestors, and generates individually maskable interrupts for Terminal count and transfer error for each channel.

8.2 Features

- 16 DMA channels. Each channel can support a unidirectional transfer.
- 16 DMA requests. The DMAC provides 16 peripheral DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMAC can assert either a burst DMA request or a single DMA request. You set the DMA burst size by programming the DMAC.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA support through the use of linked lists.
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 7 has the lowest priority. If requests from two channels become active at the same time, the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. You program the DMAC by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. Use these interfaces to transfer data when a DMA request goes active.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. You can program the DMA burst size to transfer data more efficiently. The burst size is usually set to half the size of the FIFO in the peripheral.
- Internal four word FIFO per channel.
- Supports eight, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMAC defaults to little-endian mode on reset.
- Separate and combined DMA error and DMA count interrupt requests. You can generate an interrupt to the processor on a DMA error or when a DMA count has reached 0. This is usually used to indicate that a transfer has finished. There are three interrupt request signals to do this:
  - DMACINTTC signals when a transfer has completed.
  - DMACINTERR signals when an error has occurred.
  - DMACINTR combines both the DMACINTTC and DMACINTERR interrupt request signals. You can use the DMACINTR interrupt request in systems that have few interrupt controller request inputs.
- Interrupt masking. You can mask the DMA error and DMA terminal count interrupt requests.
- Raw interrupt status. You can read the DMA error and DMA count raw interrupt status prior to masking.
- Test registers for use in block and integration system level testing.
- Identification registers that uniquely identify the DMAC. An operating system can use these to automatically configure itself.

8.3 Block Diagram

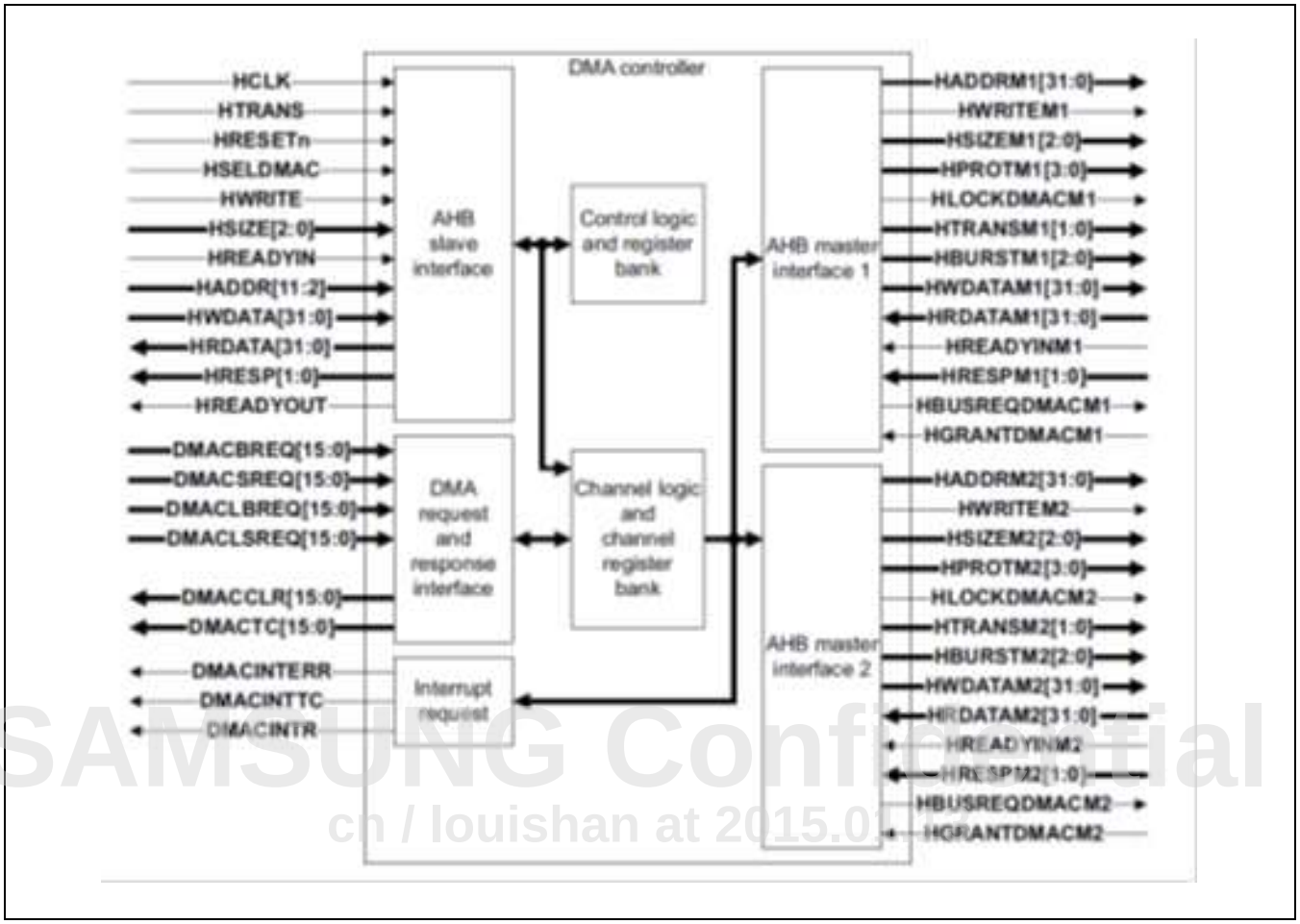


Figure 8-1 DMAC Block Diagram

8.4 Functional Description

8.4.1 Software Considerations

You must take into account the following software considerations when programming the DMAC:

- There must not be any write-operation to Channel registers in an active channel after the channel enable is made HIGH. If you must reprogram any DMAC channel parameters, you must reprogram after disabling the DMAC channel.
- If the source width is less than the destination width, the TransferSize value multiplied by the source width must be an integral multiple of the destination width.
- When the source peripheral is the flow controller and the source width is less than the destination width, the number of transfers that the source peripheral performs, before asserting a DMACLSREQ *or *DMACLBREQ, must be so that the number of transfers multiplied by the source width is an integral multiple of the destination width. If this case is violated, the data can get stuck and lost in the FIFO causing UNPREDICTABLE results. You can abort the transfer by disabling the relevant DMAC channel.
- You must not program the SrcPeripheral and DestPeripheral bit fields in the DMACCxConfig Register with any value greater than 15. See Channel Configuration Registers.
- The SWidth and DWidth bit fields in the DMACCxControl Register must not indicate more than a 32-bit wide peripheral. See Channel Control Registers.
- After the software disables a channel by clearing the Channel Enable bit in the DMACCxConfig Register, see Channel Configuration Registers, it must re-enable the bit only after it has polled a 0 in the corresponding DMACEnbldChns Register bit, see 'Enabled Channel Register. This is because the actual disabling does not immediately happen with the clearing of Channel Enable bit. You must accommodate the latency of the on going AHBburst.
- The LLI field in the DMACCxLLIReg Register must not indicate an address greater than 0xFFFFFFF0, otherwise the four-word LLI burst wraps over at 0x00000000 and the LLI data structure is not in contiguous memory locations. See Channel Linked List Item Registers.
- When the transfer size programmed in the DMAC is greater than the depth of the FIFO in a source or destination peripheral, you must only program the DMAC for non-incrementing address generation.
- A peripheral is expected to deassert any DMACSREQ, DMACBREQ, DMACLSREQ, or DMACLBREQ signals on receiving the DMACCLR signal irrespective of the request the DMACCLR was asserted in response to. This is because DMACCLR is not specific to a single-request signal, DMACSREQ, or burst-request signal, DMACSBEQ. The handshaking of DMACCLR is achieved with a logical OR of all the DMA requests in the DMAC.

NOTE: It is illegal for a peripheral to give a new DMACSREQ or DMACBREQ signal while DMACCLR is HIGH.

- If you program the TransferSize field in the DMACCxControl Register, see Channel Control Registers, as zero, and the DMAC is the flow controller, the TransferSize field has no meaning in other flow-control modes, then the channel does not initiate any transfers. It is your responsibility to disable the channel by writing into the channel enable bit of the DMACCxConfig Register and reprogramming the channel again.
- You must not run the normal read-write tests on the DMACCxControl Register, see Channel Control Registers, because the TransferSize field is not a typical write and read-back register field. While writing, the TransferSize bit-field is like a control register because it determines how many transfers the DMAC performs. However, during read-back, TransferSize behaves like a status register because it returns the number of remaining transfers in terms of source width. So when TransferSize is read back, it returns the number of destination-transfer-completed stored in a separate counter called TrfSizeDst multiplied by a factor. The same physical register is not being written into and read from, and normal write and read-back tests are not applicable.
- In the destination flow control mode, with peripheral-to-peripheral transfer, if sufficient data is present in the channel FIFO to service a DMACLSREQ or DMACLBREQ request raised by a destination peripheral without requiring data to be fetched from the source peripheral, then the source peripheral is issued a *DMACTC.
- For destination flow controlled case, peripheral-to-peripheral transfer, with DWidth < SWidth, the number of data bytes requested by the destination peripheral must be an integral multiple of Swidth expressed in bytes. If you do not ensure this, then the DMAC might fetch more data from the source peripheral than is required. This can result in data loss.
- At the end of accesses corresponding to low-priority channels, an IDLE cycle is inserted on the AHB bus to enable other masters to access the bus. This ensures that a low-priority channel does not monopolize the bus. It does, however, mean that the bus might be occupied by transactions corresponding to a low priority for up to 16 cycles in the worst case. This applies to all transfer configurations, including memory-to-memory transfers.

8.4.2 Programmer's Model

8.4.2.1 About the programmer's Model

The DMAC enables the following types of transactions:

- memory-to-memory
- memory-to-peripheral
- peripheral-to-memory
- peripheral-to-peripheral.

Each DMA stream is configured to provide unidirectional DMA transfers for a single source and destination.

For example, a bidirectional serial port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and you can access them through the same AHB master, or one area by each master.

The base address of the DMAC is not fixed, and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

Register fields

The following applies to the registers that the DMAC uses:

- You must not access reserved or unused address locations because this can result in unpredictable behavior of the device.
- You must write reserved or unused bits of registers as zero, and ignore them on read unless otherwise stated in the relevant text.
- A system or power-on reset resets all register bits to logic 0 unless otherwise stated in the relevant text.
- All registers support read and write accesses unless otherwise stated in the relevant text. A write updates the contents of a register, and a read returns the contents of the register.
- You can only access registers defined in this document using word reads and word writes, unless otherwise stated in the relevant text.

8.4.2.2 Programming the DMAC

Enabling the DMAC

Enable the DMAC by setting the DMA Enable, E, bit in the DMAC Configuration Register. See Configuration Register.

Disabling DMAC

To disable the DMAC:

1. Read the DMACEnbldChns Register and ensure that you have disabled all the DMA channels. If any channels are active, see disabling a DMA channel.
2. Disable the DMAC by writing 0 to the DMA Enable bit in the DMAC Configuration Register. See 'Configuration Register.

Enabling a DMA channel

Enable the DMA channel by setting the Channel Enable bit in the relevant DMA channel Configuration Register. See Channel Configuration Registers.

NOTE: You must fully initialize the channel before you enable it. Additionally, you must set the Enable bit of the DMAC before you enable any channels.

Disabling a DMA channel

You can disable a DMA channel in the following ways:

1. Write directly to the Channel Enable bit.

NOTE: You lose any outstanding data in the FIFOs if you use this method.

2. Use the Active and Halt bits in conjunction with the Channel Enable bit.
3. Wait until the transfer completes. The channel is then automatically disabled.

Disabling a DMA channel and losing data in the FIFO

Clear the relevant Channel Enable bit in the relevant channel Configuration Register.

See Channel Configuration Registers. The current AHB transfer, if one is in progress, completes and the channel is disabled.

NOTE: You lose any data in the FIFO.

Disabling a DMA channel without losing data in the FIFO

To disable a DMA channel without losing data in the FIFO:

1. Set the Halt bit in the relevant channel Configuration Register. See Channel Configuration Registers. This causes any subsequent DMA requests to be ignored.
2. Poll the Active bit in the relevant channel Configuration Register until it reaches0. This bit indicates whether there is any data in the channel that has to be transferred.
3. Clear the Channel Enable bit in the relevant channel Configuration Register.

Setting up a new DMA transfer

To set up a new DMA transfer:

1. If the channel is not set aside for the DMA transaction:
   - Read the DMACEnbldChns Register and determine the channels that are inactive. See Enabled Channel Register.
   - Choose an inactive channel that has the necessary priority.
2. Program the DMAC.

Halting a DMA channel

Set the Halt bit in the relevant DMA channel Configuration Register. The current source request is serviced. Any subsequent source DMA requests are ignored until the Halt bitis cleared.

Programming a DMA channel

To program a DMA channel:

1. Choose a free DMA channel with the necessary priority. DMA channel 0 has the highest priority and DMA channel 7 has the lowest priority.
2. Clear any pending interrupts on the channel you want to use by writing to the DMAC IntTCClear and DMAC IntErrClr Registers. See Interrupt Terminal Count Clear Register and Interrupt Error Clear Register. The previous channel operation might have left interrupts active.
3. Write the source address into the DMACCxSrcAddr Register. See Channel Source Address Registers.
4. Write the destination address into the DMAC CxDestAddr Register. See Channel Destination Address Registers.
5. Write the address of the next LLI into the DMACCxLLI Register. See Channel Linked List Item Registers. If the transfer consists of a single packet of data, you must write 0 into this register.
6. Write the control information into the DMACCxControl Register. See ChannelControl Registers.
7. Write the channel configuration information into the DMACCxConfiguration Register. See 'Channel Configuration Registers. If the Enable bit is set, then the DMA channel is automatically enabled.

8.4.2.3 Register Name Description

Table 8-1 DMAC0 Register Summary

- Base Address: 0xC000_0000

Name	Offset	Description	Reset value
DMACIntStatus	0x0000	Interrupt Status Register	0x00
DMACIntTCStatus	0x0004	Interrupt Terminal Count Status Register	0x00
DMACIntTCClear	0x0008	Interrupt Terminal Count Clear Register	–
DMACIntErrorStatus	0x000C	Interrupt Error Status Register	0x00
DMACIntErrClr	0x0010	Interrupt Error Clear Register	–
DMACRawIntTCStatus	0x0014	Raw Interrupt Terminal Count Status Register	–
DMACRawIntErrorStatus	0x0018	Raw Error Interrupt Status Register	–
DMACEnbldChns	0x001C	Enabled Channel Register	0x00
DMACSoftBReq	0x0020	Software Burst Request Register	0x0000
DMACSoftSReq	0x0024	Software Single Request Register	0x0000
DMACSoftLBReq	0x0028	Software Last Burst Request Register	0x0000
DMACSoftLSReq	0x002C	Software Last Single Request Register	0x0000
DMACConfiguration	0x0030	Configuration Register	0b000
DMACSync	0x0034	Synchronization Register	0x0000
DMACC0SrcAddr	0x0100	Channel Source Address Registers	0x00000000
DMACC0DestAddr	0x0104	Channel Destination Address Registers	0x00000000
DMACC0LLI	0x0108	Channel Linked List Item Registers	0x00000000
DMACC0Control	0x010C	Channel Control Registers	0x00000000
DMACC0Configuration	0x0110	Channel Configuration Registers	0x0000
DMACC1SrcAddr	0x0120	Channel Source Address Registers	0x00000000
DMACC1DestAddr	0x0124	Channel Destination Address Registers	0x00000000
DMACC1LLI	0x0128	Channel Linked List Item Registers	0x00000000
DMACC1Control	0x012C	Channel Control Registers	0x00000000
DMACC1Configuration	0x0130	Channel Configuration Registers	0x0000
DMACC2SrcAddr	0x0140	Channel Source Address Registers	0x00000000
DMACC2DestAddr	0x0144	Channel Destination Address Registers	0x00000000
DMACC2LLI	0x0148	Channel Linked List Item Registers	0x00000000
DMACC2Control	0x014C	Channel Control Registers	0x00000000
DMACC2Configuration	0x0150	Channel Configuration Registers	0x0000
DMACC3SrcAddr	0x0160	Channel Source Address Registers	0x00000000
DMACC3DestAddr	0x0164	Channel Destination Address Registers	0x00000000
DMACC3LLI	0x0168	Channel Linked List Item Registers	0x00000000
DMACC3Control	0x016C	Channel Control Registers	0x00000000

Name	Offset	Description	Reset value
DMACC3Configuration	0x0170	Channel Configuration Registers	0x0000
DMACC4SrcAddr	0x0180	Channel Source Address Registers	0x00000000
DMACC4DestAddr	0x0184	Channel Destination Address Registers	0x00000000
DMACC4LLI	0x0188	Channel Linked List Item Registers	0x00000000
DMACC4Control	0x018C	Channel Control Registers	0x00000000
DMACC4Configuration	0x0190	Channel Configuration Registers	0x0000
DMACC5SrcAddr	0x01A0	Channel Source Address Registers	0x00000000
DMACC5DestAddr	0x01A4	Channel Destination Address Registers	0x00000000
DMACC5LLI	0x01A8	Channel Linked List Item Registers	0x00000000
DMACC5Control	0x01AC	Channel Control Registers	0x00000000
DMACC5Configuration	0x01B0	Channel Configuration Registers	0x0000
DMACC6SrcAddr	0x01C0	Channel Source Address Registers	0x00000000
DMACC6DestAddr	0x01C4	Channel Destination Address Registers	0x00000000
DMACC6LLI	0x01C8	Channel Linked List Item Registers	0x00000000
DMACC6Control	0x01CC	Channel Control Registers	0x00000000
DMACC6Configuration	0x01D0	Channel Configuration Registers	0x0000
DMACC7SrcAddr	0x01E0	Channel Source Address Registers	0x00000000
DMACC7DestAddr	0x01E4	Channel Destination Address Registers	0x00000000
DMACC7LLI	0x01E8	Channel Linked List Item Registers	0x00000000
DMACC7Control	0x01EC	Channel Control Registers	0x00000000
DMACC7Configuration	0x01F0	Channel Configuration Registers	0x0000

Table 8-2 DMAC1 Register Summary

- Base Address: 0xC000_1000

Name	Offset	Description	Reset value
DMACIntStatus	0x0000	Interrupt Status Register	0x00
DMACIntTCStatus	0x0004	Interrupt Terminal Count Status Register	0x00
DMACIntTCClear	0x0008	Interrupt Terminal Count Clear Register	–
DMACIntErrorStatus	0x000C	Interrupt Error Status Register	0x00
DMACIntErrClr	0x0010	Interrupt Error Clear Register	–
DMACRawIntTCStatus	0x0014	Raw Interrupt Terminal Count Status Register	–
DMACRawIntErrorStatus	0x0018	Raw Error Interrupt Status Register	–
DMACEnbldChns	0x001C	Enabled Channel Register	0x00
DMACSoftBReq	0x0020	Software Burst Request Register	0x0000
DMACSoftSReq	0x0024	Software Single Request Register	0x0000
DMACSoftLBReq	0x0028	Software Last Burst Request Register	0x0000
DMACSoftLSReq	0x002C	Software Last Single Request Register	0x0000
DMACConfiguration	0x0030	Configuration Register	0b000
DMACSync	0x0034	Synchronization Register	0x0000
DMACC0SrcAddr	0x0100	Channel Source Address Registers	0x00000000
DMACC0DestAddr	0x0104	Channel Destination Address Registers	0x00000000
DMACC0LLI	0x0108	Channel Linked List Item Registers	0x00000000
DMACC0Control	0x010C	Channel Control Registers	0x00000000
DMACC0Configuration	0x0110	Channel Configuration Registers	0x0000
DMACC1SrcAddr	0x0120	Channel Source Address Registers	0x00000000
DMACC1DestAddr	0x0124	Channel Destination Address Registers	0x00000000
DMACC1LLI	0x0128	Channel Linked List Item Registers	0x00000000
DMACC1Control	0x012C	Channel Control Registers	0x00000000
DMACC1Configuration	0x0130	Channel Configuration Registers	0x0000
DMACC2SrcAddr	0x0140	Channel Source Address Registers	0x00000000
DMACC2DestAddr	0x0144	Channel Destination Address Registers	0x00000000
DMACC2LLI	0x0148	Channel Linked List Item Registers	0x00000000
DMACC2Control	0x014C	Channel Control Registers	0x00000000
DMACC2Configuration	0x0150	Channel Configuration Registers	0x0000
DMACC3SrcAddr	0x0160	Channel Source Address Registers	0x00000000
DMACC3DestAddr	0x0164	Channel Destination Address Registers	0x00000000
DMACC3LLI	0x0168	Channel Linked List Item Registers	0x00000000
DMACC3Control	0x016C	Channel Control Registers	0x00000000
DMACC3Configuration	0x0170	Channel Configuration Registers	0x0000
DMACC4SrcAddr	0x0180	Channel Source Address Registers	0x00000000

Name	Offset	Description	Reset value
DMACC4DestAddr	0x0184	Channel Destination Address Registers	0x00000000
DMACC4LLI	0x0188	Channel Linked List Item Registers	0x00000000
DMACC4Control	0x018C	Channel Control Registers	0x00000000
DMACC4Configuration	0x0190	Channel Configuration Registers	0x0000
DMACC5SrcAddr	0x01A0	Channel Source Address Registers	0x00000000
DMACC5DestAddr	0x01A4	Channel Destination Address Registers	0x00000000
DMACC5LLI	0x01A8	Channel Linked List Item Registers	0x00000000
DMACC5Control	0x01AC	Channel Control Registers	0x00000000
DMACC5Configuration	0x01B0	Channel Configuration Registers	0x0000
DMACC6SrcAddr	0x01C0	Channel Source Address Registers	0x00000000
DMACC6DestAddr	0x01C4	Channel Destination Address Registers	0x00000000
DMACC6LLI	0x01C8	Channel Linked List Item Registers	0x00000000
DMACC6Control	0x01CC	Channel Control Registers	0x00000000
DMACC6Configuration	0x01D0	Channel Configuration Registers	0x0000
DMACC7SrcAddr	0x01E0	Channel Source Address Registers	0x00000000
DMACC7DestAddr	0x01E4	Channel Destination Address Registers	0x00000000
DMACC7LLI	0x01E8	Channel Linked List Item Registers	0x00000000
DMACC7Control	0x01EC	Channel Control Registers	0x00000000
DMACC7Configuration	0x01F0	Channel Configuration Registers	0x0000

8.4.2.4 Peripheral DMA Request ID

Table 8-3 Peripheral DMA Request ID

Index	Description	Index	Description
0	UART1 Tx	16	I2S2 Tx
1	UART1 Rx	17	I2S2 Rx
2	UART0 Tx	18	AC97 PCMOUT
3	UART0 Rx	19	AC97 PCMIN
4	UART2 Tx	20	AC97 MICIN
5	UART2 Rx	21	SPDIF RX
6	SSP0 Tx	22	SPDIF TX
7	SSP0 Rx	23	MPEGTSI0
8	SSP1 Tx	24	MPEGTSI1
9	SSP1 Rx	25	MPEGTSI2
10	SSP2 Tx	26	MPEGTSI4
11	SSP2 Rx	27	CRYPTO BR
12	I2S0 Tx	28	CRYPTO BW
13	I2S0 Rx	29	CRYPTO HR
14	I2S1 Tx	30	Reserved
15	I2S1 Rx	31	Reserved

8.4.2.5 Address Generation

Address generation can be either incrementing or non-incrementing.

NOTE: Address wrapping is not supported.

Bursts do not cross the 1 KB address boundary.

8.4.2.6 Scatter/gather

Scatter/gather is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas in memory. You must set the DMACCxLLI Register to 0 if you do not require scatter/gather. For more information about scatter/gather DMA, see Appendix B DMA Interface.

Linked list items

An LLI consists of four words. These words are organized in the following order:

1. DMACCxSrcAddr
2. DMACCxDestAddr
3. DMACCxLLI
4. DMACCxControl

NOTE: The DMACCx Configuration Channel Configuration Register is not part of the LLI.

Programming the DMAC for scatter/gather DMA

To program the DMAC for scatter/gather DMA:

1. Write the LLIs for the complete DMA transfer to memory. Each LLI contains four words:
   - source address
   - destination address
   - pointer to next LLI
   - control word.

The last LLI has its linked list word pointer set to 0.

1. Choose a free DMA channel with the required priority. DMA channel 0 has the highest priority and DMA channel 7 the lowest priority.
2. Write the first LLI, previously written to memory, to the relevant channel in the DMAC.
3. Write the channel configuration information to the channel configuration register and set the Channel Enable bit. The DMAC then transfers the first and then subsequent packets of data as each LLI are loaded.
4. An interrupt can be generated at the end of each LLI depending on the Terminal Count bit in the DMACCxControl Register. If this bit is set, an interrupt is generated at the end of the relevant LLI. You must then service the interrupt request, and you must set the relevant bit in the DMACIntTCClear Register to clear the interrupt. If so, you must service this interrupt request and you must set the relevant IntTCClear bit in the DMACIntTCClr Register to clear the interrupt request interrupt.

Scatter/gather through linked list operation.

A series of linked lists define the source and destination data areas. Each LLI controls the transfer of one block of data, and then optionally loads another LLI to continue the DMA operation, or stops the DMA stream. The first LLI is programmed into the DMAC.

The data to be transferred described by an LLI, referred to as the packet of data, usually requires one or more DMA bursts, to each of the source and destination.

Figure 8-2 shows an example of an LLI. A rectangle of memory must be transferred to a peripheral. The addresses of each line of data are given, in hexadecimal, at the left-hand side of the figure. The LLIs describing the transfer are to be stored contiguously from address 0x20000.

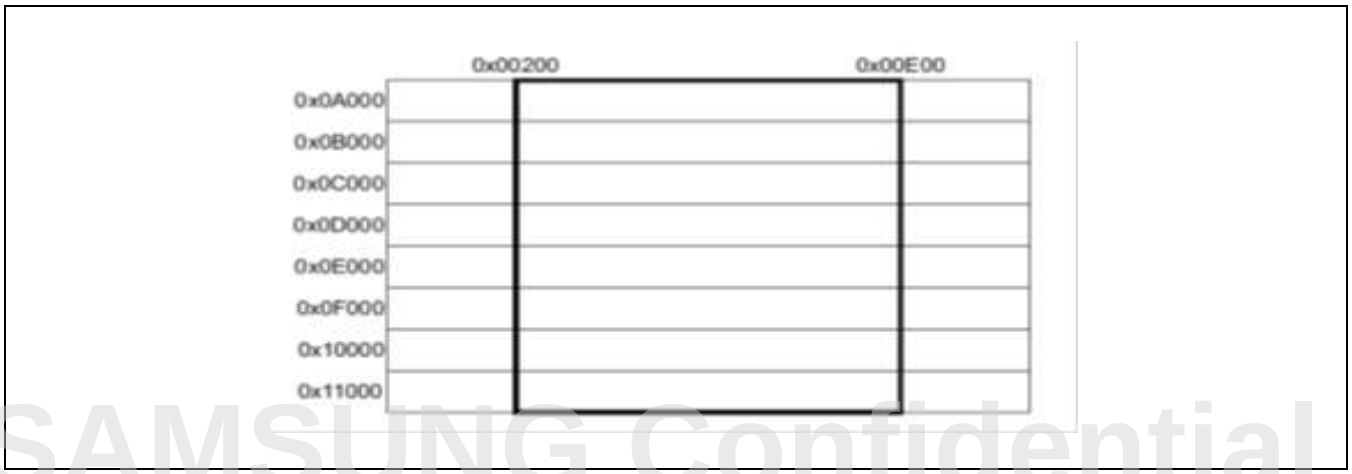


Figure 8-2 LLI Example

The first LLI, stored at 0x20000, defines the first block of data to be transferred. This is the data stored between addresses 0x0A200 and 0x0AE00:

- source start address 0x0A200
- destination address set to the destination peripheral address
- transfer width, word, 32-bit
- transfer size, 3072 bytes, 0xC00
- source and destination burst sizes, 16 transfers
- next LLI address, 0x20010.

The second LLI, stored at 0x20010, defines the next block of data to be transferred:

- source start address 0x0B200
- destination address set to the destination peripheral address
- transfer width, word, 32-bit
- transfer size, 3072 bytes, 0xC00
- source and destination burst sizes, 16 transfers
- next LLI address, 0x20020.

A chain of descriptors is built up, each one pointing to the next in the series. To initialize the DMA stream, the first LLI, 0x20000, is programmed into the DMAC. When the first packet of data has been transferred, the next LLI is automatically loaded.

The final LLI is stored at 0x20070 and contains:

- source start address 0x11200
- destination address set to the destination peripheral address
- transfer width, word, 32-bit
- transfer size, 3072 bytes, 0xC00
- source and destination burst sizes, 16 transfers
- next LLI address, 0x0.

Because the next LLI address is set to zero, this is the last descriptor, and the DMA channel is disabled after transferring the last item of data. The channel is probably set to generate an interrupt at this point to indicate to the ARM processor that the channel can be reprogrammed.

8.4.2.7 Interrupt requests

Interrupt requests can be generated when an AHB error is encountered, or at the end of a transfer, terminal count, after all the data corresponding to the current LLI has been transferred to the destination. The interrupts can be masked by programming the relevant bits on the relevant DMACCxControl and DMACCxConfiguration Channel Registers.

Interrupt Status Registers are provided. They group the interrupt requests from all the DMA channels prior to interrupt masking, DMACRawIntTCStatus, DMACRawIntErrorStatus, and after interrupt masking, DMACIntTCStatus, DMACIntErrorStatus.

The DMACIntStatus Register combines both the DMACIntTCStatus and DMACIntErrorStatus requests into a single register to enable the source of an interrupt to be found quickly. Writing to the DMACIntTCClear or the DMACIntErrClr Registers with a bit set HIGH enables selective clearing of interrupts.

The DMAC provides two interrupt request connection schemes. See Interrupt controller connectivity. The simplest connection scheme has a combined error and end of transfer complete interrupt request. To find the source of an interrupt, you must read both the DMACIntStatus and DMACIntTCStatus Registers.

For faster interrupt response, you can use an alternate connection scheme. This scheme uses separate interrupt requests for the error and transfer complete requests. Read either the DMACIntTCStatus or DMACIntErrorStatus Registers to find the source of an interrupt.

Combined terminal count and error interrupt sequence flow

When you use the *DMACINTR *interrupt request:

1. You must wait until the combined interrupt request from the DMAC goes active. Assuming the interrupt is enabled in the interrupt controller and in the processor, the processor branches to the interrupt vector address and enters the interrupt service routine.
2. You must read the interrupt controller Status Register and determine whether the source of the request was the DMAC.
3. You must read the DMACIntStatus Register to determine the channel that generated the interrupt. If more than one request is active, it is recommended that you check the highest priority channels first.
4. You must read the DMACIntTCStatus Register to determine whether the interrupt was generated because of the end of the transfer, terminal count, or because an error occurred. A HIGH bit indicates that the transfer completed.
5. You must read the DMACIntErrorStatus Register to determine whether the interrupt was generated because of the end of the transfer, terminal count, or because an error occurred. A HIGH bit indicates that an error occurred.
6. You must write a 1 to the relevant bit in the DMACIntTCClear, orDMACIntErrClr, Register to clear the interrupt request.

Terminal count interrupt sequence flow

When the separate, DMACINTTC and DMACINTERR, interrupt requests are used:

1. You must wait until the terminal count DMA interrupt request goes active. Assuming the interrupt is enabled in the interrupt controller and in the processor, the processor branches to the interrupt vector address and enters the interrupt service routine.
2. You must read the interrupt controller Status Register to determine if the source of the interrupt request was the DMAC asserting the DMACINTTC signal.
6. You must read the DMACIntTCStatus Register to determine the channel that generated the interrupt. If more than one request is active, it is recommended that you service the highest priority channel first.
4. You must service the interrupt request.
5. You must write a 1 to the relevant bit in the DMACIntTCClear Register to clear the interrupt request.

Error interrupt sequence flow

When the separate interrupt requests, DMACINTTC and DMACINTERR, are used:

1. You must wait until the interrupt request goes active because of a DMA channel error. Assuming the interrupt is enabled in the interrupt controller and in the processor, the processor branches to the interrupt vector address and enters the interrupt service routine.
2. You must read the Interrupt Controllers Status Register to determine if the source of the request was the DMAC asserting the DMACINTERR signal.
3. You must read the DMACIntErrorStatus Register to determine the channel that generated the interrupt. If more than one request is active it is recommended that you check the highest priority channels first.
4. You must service the interrupt request.
5. You must write a 1 to the relevant bit in the DMACIntErrClr Register to clear the interrupt request.

Interrupt polling sequence flow

The DMAC interrupt request signal is masked out, disabled in the interrupt controller, or disabled in the processor. When polling the DMAC, you must:

1. Read the DMACIntStatus Register. If none of the bits are HIGH repeat this step, otherwise, go to step 2. If more than one request is active, it is recommended that you check the highest priority channels first.
2. Read the DMACIntTCStatus Register to determine if the interrupt was generated because of the end of the transfer, terminal count, or because of error occurred. A HIGH bit indicates that the transfer completed.
3. Service the interrupt request.
4. For an error interrupt, write a 1 to the relevant bit of the DMACIntErrClr Register to clear the interrupt request. For a terminal count interrupt, write a 1 to the relevant bit of the DMACIntTCClrRegister.

8.4.2.8 DMAC Data Flow

Memory-to-memory DMA flow

For a memory-to-memory DMA flow:

1. Program and enable the DMA channel.
2. Transfer data whenever the DMA channel has the highest pending priority and the DMAC gains bus master ship of the AHB bus.
3. If an error occurs while transferring the data, generate an error interrupt and disable the DMA stream.
4. Decrement the transfer count.
5. If the count has reached zero:
   - Generate a terminal count interrupt. You can mask the interrupt.
   - If the DMACCxLLI Register is not 0, then reload the following registers and go to back to step 2:
     - DMACCxSrcAddr
     - DMACCxDestAddr
     - DMACCxLLI
     - DMACCxControl.
     - However, if DMACCxLLI is 0, the DMA stream is disabled and the flow sequence ends.

Memory-to-peripheral, or peripheral-to-memory DMA flow

For a peripheral-to-memory or memory-to-peripheral DMA flow:

1. Program and enable the DMA channel.
2. Wait for a DMA request.
3. The DMAC then starts transferring data when:
   - The DMA request goes active.
   - The DMA stream has the highest pending priority.
   - The DMAC is the bus master of the AHB bus.
4. If an error occurs while transferring the data, an error interrupt is generated and the DMA stream is disabled, and the flow sequence ends.
5. Decrement the transfer count if the DMAC is controlling the flow control.

6. If the transfer has completed, indicated by the transfer count reaching 0 if the DMAC is performing flow control, or by the peripheral setting the DMACLBREQ or DMACLSREQ signals if the peripheral is performing flow control:
   - The DMAC asserts the DMACTC signal.
   - The terminal count interrupt is generated. You can mask this interrupt.
   - If the DMACCxLLI Register is not 0, then reload the following registers and go to back to step 2:
     - DMACCxSrcAddr
     - DMACCxDestAddr
     - DMACCxLLI
     - DMACCxControl.
     - However, if DMACCxLLI is 0, the DMA stream is disabled and the flow sequence ends.

Peripheral-to-peripheral DMA flow

For a peripheral-to-peripheral DMA flow:

1. Program and enable the DMA channel.
2. Wait for a source DMA request.
3. The DMAC then starts transferring data when:
   - The DMA request goes active.
   - The DMA stream has the highest pending priority.
   - The DMAC is the bus master of the AHB bus.
4. If an error occurs while transferring the data, an error interrupt is generated, then finishes.
5. Decrement the transfer count if the DMAC is controlling the flow control.
6. If the transfer has completed, indicated by the transfer count reaching 0 if the DMAC is performing flow control, or by the peripheral setting the DMACLBREQ or DMACLSREQ signals if the peripheral is performing flow control:
   - The DMAC asserts the DMACTC signal to the source peripheral.
   - Subsequent source DMA requests are ignored.
7. When the destination DMA request goes active and there is data in the DMACFIFO, transfer data into the destination peripheral.
8. If an error occurs while transferring the data, an error interrupt is generated and the DMA stream is disabled, and the flow sequence ends.

9. If the transfer has completed, it is indicated by the transfer count reaching 0 if the DMAC is performing flow control, or by the peripheral setting the DMACLBREQ or DMACLSREQ signals if the peripheral is performing flow control.

   The following happens:

   - The DMAC asserts the DMACTC signal to the destination peripheral.
   - The terminal count interrupt is generated. You can mask this interrupt.
   - If the DMACCxLLI Register is not 0, then reload the following registers and go to back to step 2:
     - DMACCxSrcAddr
     - DMACCxDestAddr
     - DMACCxLLI
     - DMACCxControl.
     - However, if DMACCxLLI is 0, the DMA stream is disabled and the flow sequence ends.

8.5 Register Description

8.5.1 Register Map Summary

This section describes the DMAC0/1 registers.

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000

Register	Offset	Description	Reset Value
Interrupt Status Register	0x00	The read-only DMACIntStatus Register, with address offset of 0x000, shows the status of the interrupts after masking. A HIGH bit indicates that a specific DMA channel interrupt request is active. You can generate the request from either the error or terminal count interrupt requests.	0x0
Interrupt Terminal Count Status Register	0x04	The read-only DMACIntTCStatus Register, with address offset of 0x004, indicates the status of the terminal count after masking. You must use this register in conjunction with the DMACIntStatus Register if you use the combined interrupt request, DMACINTR, to request interrupts. If you use the DMACINTTC interrupt request, then you only have to read the DMACIntTCStatus Register to ascertain the source of the interrupt request.	0x0
Interrupt Terminal Count Clear Register	0x08	The write-only DMACIntTCClear Register, with address offset of 0x008, clears a terminal count interrupt request. When writing to this register, each data bit that is set HIGH causes the corresponding bit in the Status Register to be cleared. Data bits that are LOW have no effect on the corresponding bit in the register.	–
Interrupt Error Status Register	0x0C	The read-only DMACIntErrorStatus Register, with address offset of 0x00C, indicates the status of the error request after masking. You must use this register in conjunction with the DMACIntStatus Register if you use the combined interrupt request, DMACINTR, to request interrupts. If you use the DMACINTERR interrupt request, then only read the DMACIntErrorStatus Register.	0x0
Interrupt Error Clear Register	0x10	The write-only DMACIntErrClr Register, with address offset of 0x010, clears the error interrupt requests. When writing to this register, each data bit that is HIGH causes the corresponding bit in the Status Register to be cleared. Data bits that are LOW have no effect on the corresponding bit in the register.	–
Raw Interrupt Terminal Count Status Register	0x14	The read-only DMACRawIntTCStatus Register, with address offset of 0x014, indicates the DMA channels that are requesting a transfer complete, terminal count interrupt, prior to masking. A HIGH bit indicates that the terminal count interrupt request is active prior to masking.	–
Raw Error Interrupt Status Register	0x18	The read-only DMACRawIntErrorStatus Register, with address offset of 0x018, indicates the DMA channels that are requesting an error interrupt prior to masking. A HIGH	–

Register	Offset	Description	Reset Value
		bit indicates that the error interrupt request is active prior to masking.	
Enabled Channel Register	0x1C	The read-only DMACEnbldChns Register, with address offset of 0x01C, indicates the DMA channels that are enabled, as indicated by the Enable bit in the DMACCxConfiguration Register. A HIGH bit indicates that a DMA channel is enabled. A bit is cleared on completion of the DMA transfer.	0x0
Software Burst Request Register.	0x20	The read/write DMACSoftBReq Register, with address offset of 0x020, enables DMA burst requests to be generated by software. You can generate a DMA request for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Writing 0 to this register has no effect. Reading the register indicates the sources that are requesting DMA burst transfers. You can generate a request from either a peripheral or the software request register.	0x0
Software Single Request Register.	0x24	The read/write DMACSoftSReq Register, with address offset of 0x024, enables DMA single requests to be generated by software. You can generate a DMA request for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Writing 0 to this register has no effect. Reading the register indicates the sources that are requesting single DMA transfers. You can generate a request from either a peripheral or the software request register.	0x0
Software Last Burst Request Register	0x28	The read/write DMACSoftLBReq Register, with address offset of 0x028, enables software to generate DMA last burst requests. You can generate a DMA request for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Writing 0 to this register has no effect. Reading the register indicates the sources that are requesting last burst DMA transfers. You can generate a request from either a peripheral or the software request register.	0x0
Software Last Single Request Register	0x2C	The read/write DMACSoftLSReq Register, with address offset of 0x02C, enables software to generate DMA last single requests. You can generate a DMA request for each source by writing a 1 to the corresponding register bit. A register bit is cleared when the transaction has completed. Writing 0 to this register has no effect. Reading the register indicates the sources that are requesting last single DMA transfers. You can generate a request from either a peripheral or the software request register.	0x0
Configuration Register	0x30	The read/write DMACConfiguration Register, with address offset of 0x030, configures the operation of the DMAC. You can alter the endianness of the individual AHB master interfaces by writing to the M1 and M2 bits of this register. The M1 bit enables you to alter the endianness of AHB	0x0

Register	Offset	Description	Reset Value
		master interface 1. The M2 bit enables you to alter the endianness of AHB master interface 2. The AHB master interface 2. The AHB master interfaces are set to little-endian mode on reset.	
Synchronization Register	0x34	The read/write DMACSync Register, with address offset of 0x034, enables or disables synchronization logic for the DMA request signals. The DMA request signals consist of: • DMACBREQ[15:0] • DMACSREQ[15:0] • DMACLBREQ[15:0] • DMACLSREQ[15:0]. A bit set to 0 enables the synchronization logic for a particular group of DMA requests. A bit set to 1 disables the synchronization logic for a particular group of DMA requests. This register is reset to 0, and synchronization logic enabled. NOTE: It is illegal for a peripheral to give a new DMACSREQ or DMACBREQ signal while DMACCLR is HIGH. NOTE: You must use synchronization logic when the peripheral generating the DMA request runs on a different clock to the DMAC. For peripherals running on the same clock as the DMAC, disabling the synchronization logic improves the DMA request response time. If necessary, synchronize the DMA response signals, DMACCLR and DMACTC, in the peripheral.	0x0
Channel registers The channel registers are for programming a DMA channel. These registers consist of: • eight DMACCxSrcAddr Registers • eight DMACCxDestAddr Registers • eight DMACCxLLI Registers • eight DMACCxControl Registers • eight DMACCxConfiguration Registers. When performing scatter/gather DMA, the first four registers are automatically updated. NOTE: Unpredictable behavior can result if you update the channel registers when a transfer is taking place. If you want to change the channel configurations, you must disable the channel first and then reconfigure the relevant register.			
Channel Source Address Registers	0x100, 0x120, 0x140, 0x160, 0x180, 0x1A0, 0x1C0, 0x1E0	The eight read/write DMACCxSrcAddr Registers, with address offsets of 0x100, 0x120, 0x140, 0x160, 0x180, 0x1A0, 0x1C0, and 0x1E0 respectively, contain the current source address, byte-aligned, of the data to be transferred. Software programs each register directly before the appropriate channel is enabled. When the DMA channel is enabled, this register is updated: • as the source address is incremented • by following the linked list when a complete packet of	0x0

Register	Offset	Description	Reset Value
		data has been transferred. Reading the register when the channel is active does not provide useful information. This is because by the time the software has processed the value read, the channel might have progressed. It is intended to be read-only when the channel has stopped, and in such case, it shows the source address of the last item read. NOTE: You must align source and destination addresses to the source and destination widths.	
Channel Destination Address Register	0x104, 0x124, 0x144, 0x164, 0x184, 0x1A4, 0x1C4, 0x1E4	Channel Destination Address Registers. The eight read/write DMACCxDestAddr Registers, with address offsets of 0x104, 0x124, 0x144, 0x164, 0x184, 0x1A4, 0x1C4, and 0x1E4 respectively, contain the current destination address, byte-aligned, of the data to be transferred. Software programs each register directly before the channel is enabled. When the DMA channel is enabled, the register is updated as the destination address is incremented and by following the linked list when a complete packet of data has been transferred. Reading the register when the channel is active does not provide useful information. This is because by the time the software has processed the value read, the channel might have progressed. It is intended to be read-only when a channel has stopped. In this case, it shows the destination address of the last item read.	0x0
Channel Linked List Item Registers	0x108, 0x128, 0x148, 0x168, 0x188, 0x1A8, 0x1C8, 0x1E8	Channel Linked List Item Register. The eight read/write DMACCxLLI Registers, with address offsets of 0x108, 0x128, 0x148, 0x168, 0x188, 0x1A8, 0x1C8, and 0x1E8 respectively, contain a word-aligned address of the next LLI. If the LLI is 0, then the current LLI is the last in the chain, and the DMA channel is disabled after all DMA transfers associated with it are completed. NOTE: 1. Programming this register when the DMA channel is enabled has unpredictable results. 2. To make loading the LLIs more efficient for some systems, you can make the LLI data structures 4-word aligned.	0x0
Channel Control Registers	0x10C, 0x12C, 0x14C, 0x16C, 0x18C, 0x1AC, 0x1CC, 0x1EC	Refer to below description. The eight read/write DMACCxControl Registers, with address offsets of 0x010C, 0x12C, 0x14C, 0x16C, 0x18C, 0x1AC, 0x1CC, and 0x1EC respectively, contain DMA channel control information such as the transfer size, burst size, and transfer width. Software programs each register directly before the DMA channel is enabled. When the channel is enabled, the register is updated by	0x0

<table>
<tr><th>Register</th><th>Offset</th><th>Description</th><th>Reset Value</th></tr>
<tr><td></td><td></td><td>following the linked list when a complete packet of data has been transferred. Reading the register while the channel is active does not give useful information. This is because by the time that software has processed the value read, the channel might have progressed. It is intended to be read-only when a channel has stopped.
Below Table lists the values of the DBSize or SBSsize bits and their corresponding burst sizes.
Below Table Source or destination burst size
<table>
<tr><th>Bit value of DBSize or SBSize</th><th>Source or Destination Burst Transfer Request Size</th></tr>
<tr><td>0b000</td><td>1</td></tr>
<tr><td>0b001</td><td>4</td></tr>
<tr><td>0b010</td><td>8</td></tr>
<tr><td>0b011</td><td>16</td></tr>
<tr><td>0b100</td><td>32</td></tr>
<tr><td>0b101</td><td>64</td></tr>
<tr><td>0b110</td><td>128</td></tr>
<tr><td>0b111</td><td>256</td></tr>
</table>

Below Table lists the value of the SWidth or DWidth bits and their corresponding widths.
Below Table lists the value of the SWidth or DWidth bits and their corresponding widths.
<table>
<tr><th>Bit value of SWidth or DWidth</th><th>Source or Destination Width</th></tr>
<tr><td>0b000</td><td>Byte, 8-bit</td></tr>
<tr><td>0b001</td><td>Halfword, 16-bit</td></tr>
<tr><td>0b010</td><td>Word, 32-bit</td></tr>
<tr><td>0b011</td><td>Reserved</td></tr>
<tr><td>0b100</td><td>Reserved</td></tr>
<tr><td>0b101</td><td>Reserved</td></tr>
<tr><td>0b110</td><td>Reserved</td></tr>
<tr><td>0b111</td><td>Reserved</td></tr>
</table>
Protection and access information
AHB access information is provided to the source and destination peripherals when a transfer occurs. The transfer information is provided by programming the DMA channel, the Prot bit of the DMACCxControl Register, and the Lock bit of the DMACCxConfiguration Register. Software programs these bits, and peripherals can use this</td><td></td></tr>
</table>

<table>
<tr><th>Register</th><th>Offset</th><th>Description</th><th>Reset Value</th></tr>
<tr><td></td><td></td><td>information if necessary. Three bits of information are provided. Below Table lists the purposes of the three protection bits.
Below Table Protection bits
<table>
<tr><th>Bit</th><th>Description</th><th>Purpose</th></tr>
<tr><td>[2]</td><td>Cacheable or Non-cacheable</td><td>Indicates whether or not the access can be cached:
0 = non-cacheable
1 = cacheable.
This bit indicates whether or not the access is cacheable. For example, you can use this bit to indicate to an AMBA bridge that when it saw the first read of a burst of eight it can transfer the whole burst of eight reads on the destination bus, rather than pass the transactions through one at a time. This bit controls the AHB HPROT[3] signal.</td></tr>
<tr><td>[1]</td><td>Bufferable or Non-bufferable</td><td>Indicates whether or not the access can be buffered:
0 = non-bufferable
1 = bufferable.
This bit indicates whether or not the access is bufferable. For example, you can use this bit to indicate to an AMBA bridge that the read can complete in zero wait states on the source bus without waiting for it to arbitrate for the destination bus and for the slave to accept the data. This bit controls the AHB HPROT[2] signal.</td></tr>
<tr><td>[0]</td><td>Privileged or User</td><td>Indicates whether the access is in User, or Privileged mode:
0 = user mode
1 = privileged mode.
This bit controls the AHB HPROT[1] signal.</td></tr>
</table></td><td></td></tr>
<tr><td>Channel Configuration Registers</td><td>0x110, 0x130, 0x150, 0x170, 0x190, 0x1B0, 0x1D0, 0x1F0</td><td>The eight DMACCxConfiguration Registers, with address offsets of 0x110, 0x130, 0x150, 0x170, 0x190, 0x1B0, 0x1D0, and 0x1F0 respectively, are read/write and configure the DMA channel. The registers are not updated when a new LLI is requested.
Below Table lists the bit values of the three flow control and transfer type bits.
Below Table Flow control and transfer type bits</td><td>0x0</td></tr>
</table>

8.5.1.1 Interrupt Status Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SesReqScs	[31:8]	R	Read undefined	0x0
IntStatus	[7:0]	R	Status of the DMA interrupts after masking	0x0

8.5.1.2 Interrupt Terminal Count Status Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x04, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Read undefined	0x0
IntTCStatus	[7:0]	R	Interrupt terminal count request status	0x0

8.5.1.3 Interrupt Terminal Count Clear Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x08, Reset Value = x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	W	Undefined. Write as zero.	0x0
IntTCClear	[7:0]	W	Terminal count request clear.	0x0

8.5.1.4 Interrupt Error Status Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x0C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Read undefined	0x0
IntErrorStatus	[7:0]	R	Interrupt error status	0x0

8.5.1.5 Interrupt Error Clear Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x10, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	W	Undefined. Write as zero.	0x0
IntErrClr	[7:0]	W	IntErrClr Interrupt error clear.	0x0

8.5.1.6 Raw Interrupt Terminal Count Status Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x14, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Read undefined	0x0
RawIntTCStatus	[7:0]	R	Status of the terminal count interrupt prior to masking	0x0

8.5.1.7 Raw Error Interrupt Status Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x18, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Read undefined	0x0
RawIntErrorStatus	[7:0]	R	Status of the error interrupt prior to masking	0x0

8.5.1.8 Enabled Channel Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x1C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Read undefined	0x0
EnabledChannels	[7:0]	R	Channel enable status	0x0

8.5.1.9 Software Burst Request Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Read undefined. Write as zero.	0x0
SoftBReq	[15:0]	RW	Software burst request.	0x0

8.5.1.10 Software Single Request Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x24, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Read undefined. Write as zero.	0x0
SoftSReq	[15:0]	RW	Software single request.	0x0

8.5.1.11 Software Last Burst Request Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x28, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Read undefined. Write as zero.	0x0
SoftLBReq	[15:0]	RW	Software last burst request.	0x0

8.5.1.12 Software Last Single Request Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x2C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Read undefined. Write as zero.	0x0
SoftLSReq	[15:0]	RW	Software last single request.	0x0

8.5.1.13 Configuration Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x30, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	RW	Read undefined. Write as zero.	-
M2	[2]	RW	AHB Master 2 endianness configuration: 0 = little-endian mode 1 = big-endian mode This bit is reset to 0.	1'b0
M1	[1]	RW	AHB Master 1 endianness configuration: 0 = little-endian mode 1 = big-endian mode This bit is reset to 0.	1'b0
E	[0]	RW	DMAC enable: 0 = disabled 1 = enabled This bit is reset to 0. Disabling the DMAC reduces power consumption.	1'b0

8.5.1.14 Synchronization Register

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x34, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Read undefined. Write as zero.	-
DMACSync	[15:0]	RW	DMA synchronization logic for DMA request signals enabled or disabled. A LOW bit indicates that the synchronization logic for the request signals is enabled. A HIGH bit indicates that the synchronization logic is disabled.	0x0000

8.5.1.15 Channel Source Address Registers_n (n = 0 to 7)

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x100, 0x120, 0x140, 0x160, 0x180, 0x1A0, 0x1C0, 0x1E0,
  Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SrcAddr	[31:0]	RW	DMA source address	0x0000_0000

8.5.1.16 Channel Destination Address Registers_n (n = 0 to 7)

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x104, 0x124, 0x144, 0x164, 0x184, 0x1A4, 0x1C4, 0x1E4,
  Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DestAddr	[31:0]	RW	DMA destination address	0x0000_0000

8.5.1.17 Channel Linked List Item Registers_n (n = 0 to 7)

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x108, 0x128, 0x148, 0x168, 0x188, 0x1A8, 0x1C8, 0x1E8,
  Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LLI	[31:2]	–	Linked list item. Bits [31:2] of the address for the next LLI. Address bits [1:0] are 0.	0x0000_0000
RSVD	[1]	RW	Read undefined. Write as zero.	1'b0
LM	[0]	–	AHB master select for loading the next LLI 0 = AHB Master 1 1 = AHB Master 2.	1'b0

8.5.1.18 Channel Control Registers_n (n = 0 to 7)

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x10C, 0x12C, 0x14C, 0x16C, 0x18C, 0x1AC, 0x1CC, 0x1EC,
  Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
I	[31]	R	"Terminal count" interrupt enable bit. It controls whether the current LLI is expected to trigger the terminal count interrupt.	1'b0
Prot	[30:28]	RW	Protection.	3'b0
DI	[27]	R	Destination increment. When set, the destination address is incremented after each transfer.	1'b0
SI	[26]	R	Source increment. When set, the source address is incremented after each transfer.	1'b0
D	[25]	RW	Destination AHB master select: 0 = AHB master 1 selected for the destination transfer 1 = AHB master 2 selected for the destination transfer	1'b0
S	[24]	RW	Source AHB master select: 0 = AHB master 1 selected for the source transfer 1 = AHB master 2 selected for the source transfer	1'b0
DWidth	[23:21]	RW	Destination transfer width. Transfers wider than the AHB master bus width are illegal. The source and destination widths can be different from each other. The hardware automatically packs and unpacks the data when required.	3'b0
SWidth	[20:18]	RW	Source transfer width. Transfers wider than the AHB master bus width are illegal. The source and destination widths can be different from each other. The hardware automatically packs and unpacks the data when required.	3'b0
DBSize	[17:15]	RW	Destination burst size. Indicates the number of transfers that make up a destination burst transfer request. You must set this value to the burst size of the destination peripheral, or if the destination is memory, to the memory boundary size. The burst size is the amount of data that is transferred when the DMACxBREQ signal goes active in the destination peripheral. The burst size is not related to the AHB HBURST signal.	3'b0
SBSize	[14:12]	RW	Source burst size. Indicates the number of transfers that make up a source burst. You must set this value to the burst size of the source peripheral, or if the source is memory, to the memory boundary size. The burst size is the amount of data that is transferred when the DMACxBREQ signal goes active in the source peripheral. The burst size is not related to the	3'b0

Name	Bit	Type	Description	Reset Value
			AHB HBURST signal.	
TransferSize	[11:0]	RW	Transfer size. A write to this field sets the size of the transfer when the DMAC is the flow controller. This value counts down from the original value to zero, and so its value indicates the number of transfers left to complete. A read from this field provides the number of transfers still to be completed on the destination bus. Reading the register when the channel is active does not give useful information because by the time the software has processed the value read, the channel might have progressed. Only use it when a channel is enabled, and then disabled. Program the transfer size value to zero if the DMAC is not the flow controller. If you program the TransferSize to a non-zero value, the DMAC might attempt to use this value instead of ignoring the TransferSize.	11'b0

8.5.1.19 Channel Configuration Registers_n (n = 0 to 7)

- Base Address: 0xC000_0000
- Base Address: 0xC000_1000
- Address = Base Address + 0x110, 0x130, 0x150, 0x170, 0x190, 0x1B0, 0x1D0, 0x1F0,
  Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:19]	–	Read undefined. Write as zero.	-
H	[18]	RW	Halt: 0 = Enable DMA requests 1 = Ignore extra source DMA requests. The contents of the channels FIFO are drained. You can use this value with the Active and Channel Enable bits to cleanly disable a DMA channel.	1'b0
A	[17]	R	Active: 0 = There is no data in the FIFO of the channel 1 = The FIFO of the channel has data. You can use this value with the Halt and Channel Enable bits to cleanly disable a DMA channel.	1'b0
L	[16]	RW	Lock. When set, this bit enables locked transfers.	1'b0
ITC	[15]	RW	Terminal count interrupt mask. When cleared, this bit masks out the terminal count interrupt of the relevant channel.	1'b0
IE	[14]	RW	Interrupt error mask. When cleared, this bit masks out the error interrupt of the relevant channel.	1'b0
FlowCntrl	[13:11]	RW	Flow control and transfer type. This value indicates the flow controller and transfer type. The flow controller can be the DMAC, the source peripheral, or	3'b0

Name	Bit	Type	Description	Reset Value
			the destination peripheral. The transfer type can be memory-to-memory, memory-to-peripheral, peripheral-to-memory, or peripheral-to-peripheral.	
RSVD	[10]	–	Read undefined. Write as zero.	1'b0
DestPeripherala	[9:6]	RW	Destination peripheral. This value selects the DMA destination request This field is ignored if the destination of the transfer is to memory.	4'b0
RSVD	[5]	–	Read undefined. Write as zero.	-
SrcPeripherala	[4:1]	RW	Source peripheral. This value selects the DMA source request peripheral. This field is ignored if the source of the transfer is from memory.	4'b0
E	[0]	RW	Channel enable. Reading this bit indicates whether a channel is currently enabled or disabled: 0 = Channel disabled 1 = Channel enabled You can also determine the Channel Enable bit status by reading the DMACEnbldChns register. You enable a channel by setting this bit. You can disable a channel by clearing the Enable bit. This causes the current AHB transfer, if one is in progress, to complete, and the channel is then disabled. Any data in the channel's FIFO is lost. Restarting the channel by setting the Channel Enable bit has unpredictable effects and you must fully re-initialize the channel. The channel is also disabled, and the Channel Enable bit cleared, when the last LLI is reached, or if a channel error is encountered. If a channel has to be disabled without losing data in a channel's FIFO, you must set the Halt bit so that subsequent DMA requests are ignored. The Active bit must then be polled until it reaches 0, indicating that there is no data left in the channel's FIFO. Finally, you can clear the Channel Enable bit.	1'b0

9 Interrupt Controller

9.1 Overview

64 interrupt sources from internal peripherals, including the DMA controller, UART, I2C and GPIO, etc. supply requests to an Interrupt Controller.

An FIQ or an IRQ (interrupt requests) are signaled by the Interrupt Controller to CPU. After arbitrating multiple requests from internal peripherals and GPIO, the Controller requests an interrupt.

The hardware arbitration logic decides the interrupt arbitration process and the results are recorded in the interrupt pending registers.

9.2 Features

The interrupt controller is responsible for:

- support for 64 IRQ interrupts
- 2 channels, each channel processes 32 IRQ interrupts and has each AHB bus.
- IRQ and FIQ generation
- AHB mapped for faster interrupt response
- software interrupt generation
- raw interrupt status
- interrupt request status

9.3 Block Diagram

The interrupt controller has two channels. Each channel has 32 interrupt sources. The interrupt request logic receives the interrupt requests from the peripheral and combines them with the software interrupt requests. It then masks out the interrupt requests which are not enabled, and routes the enabled interrupt requests to either IRQ Status or FIQ Status. *Figure 9-1* shows a block diagram of the interrupt request logic in each channel.

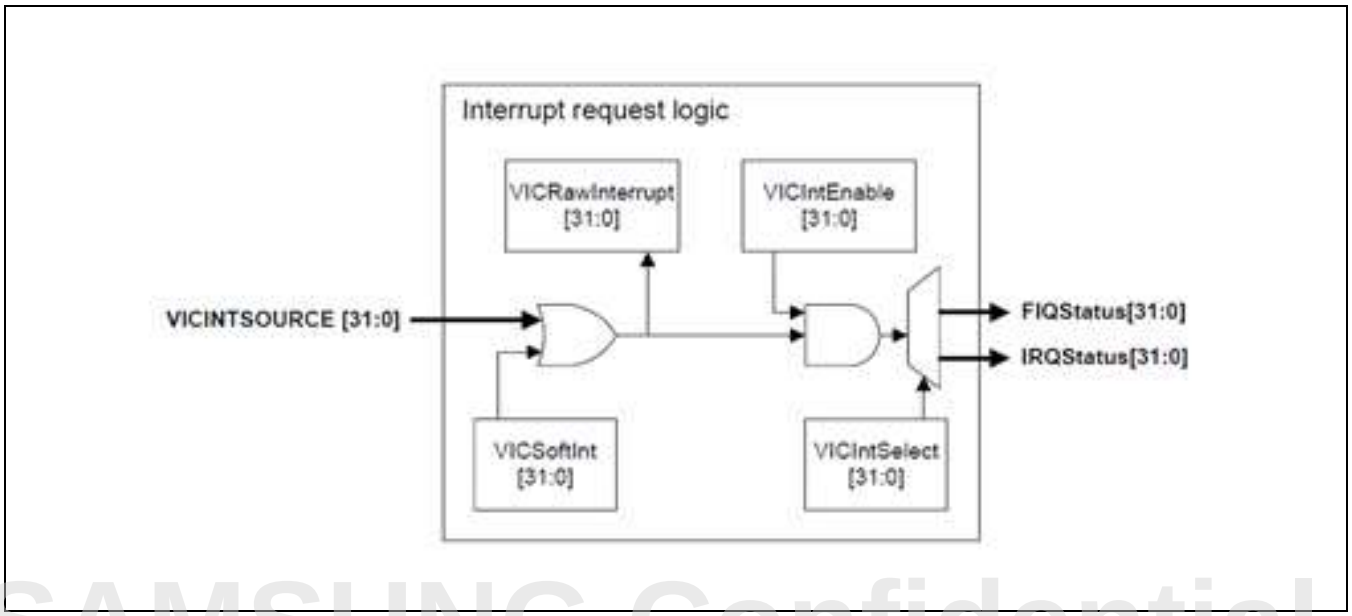


Figure 9-1 Interrupt Request Logic in 1 Channel

The FIQ interrupt logic generates the FIQ interrupt signal by FIQ interrupt requests in the interrupt controller. *Figure 9-2* shows a block diagram of the FIQ interrupt logic in each channel.

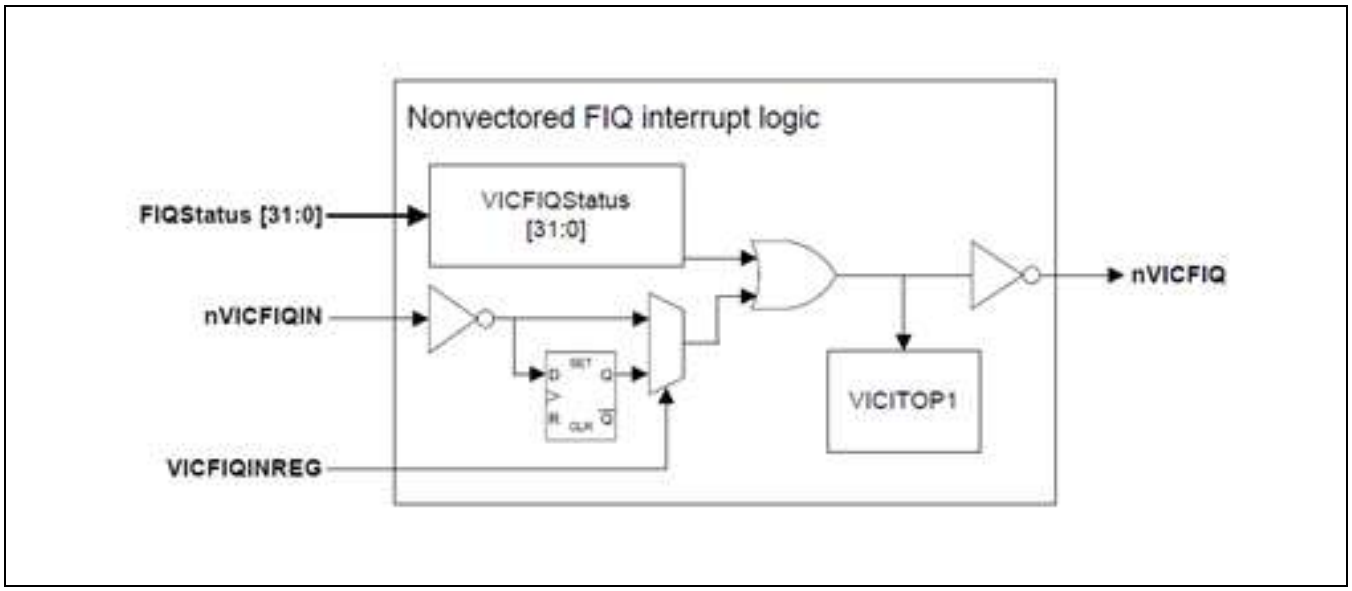


Figure 9-2 FIQ Interrupt Logic in 1 Channel

9.4 Programming sequence

9.4.1 Interrupt Flow Sequence Using AHB

The following procedure shows the sequence for the IRQ interrupt flow:

- An IRQ interrupt occurs.
- The ARM processor branches to the IRQ interrupt vector
- Stack the workspace so that IRQ interrupts can be re-enabled later.
- Perform a dummy read to the VICADDRESS Register to set up priority status control in the VIC.
- Read the VICIRQSTATUS Register and determine which interrupt sources have to be service.
- Execute the ISR. At the beginning of the ISR, the interrupt of the processor can be re-enabled so that a higher priority interrupt can be serviced.
- Clear the requesting interrupt in the peripheral, or write to the VICSOFTINTCLEAR Register if the request was generated by a software interrupt.
- Disable the interrupt on the processor and restore the workspace.
- Write to the VICADDRESS Register. This clears the respective interrupt in the internal interrupt priority hardware.
- Return from the interrupt. This re-enables the interrupts.

9.4.2 FIQ Interrupt Flow Sequence

The following procedure shows the sequence for the FIQ interrupt flow.

- An FIQ interrupt occurs.
- The ARM processor branches to the FIQ interrupt vector.
- Branch to the ISR.
- Execute the ISR.
- Clear the requesting interrupt in the peripheral, or write to the VICSOFTINTCLEAR Register if the request was generated by a software interrupt.
- Disable the interrupts and restore the workspace.
- Return from the interrupt. This re-enables the interrupts

9.4.3 Internal GIC

Cortex A9 MP Core has included internal Generic Interrupt Controller (GIC). Some interrupt signals are connected with this internal GIC. Internal GIC should be enable for using these interrupt. Refer to Cortex A9 MP Core Technical Reference Manual for how to use.

9.5 Interrupt Source

Table 9-1 Interrupt Sources Description Table

Interrupt Number	Source	Description
0	MCUSTOP	MCUSTOP interrupt
1	DMA0	DMA0 interrupt
2	DMA1	DMA1 interrupt
3	CLKPWR0	CLKPWRPWR interrupt
4	CLKPWR1	CLKPWRALIVE interrupt
5	CLKPWR2	CLKPWRRTC interrupt
6	UART1	UART1 interrupt
7	UART0	UART0 interrupt
8	UART2	UART2 interrupt
9	UART3	UART3 interrupt
10	UART4	UART4 interrupt
11	RESERVED	–
12	SSP0	SSP0 interrupt
13	SSP1	SSP1 interrupt
14	SSP2	SSP2 interrupt
15	I2C0	I2C0 interrupt
16	I2C1	I2C1 interrupt
17	I2C2	I2C2 interrupt
18	DEINTERLACE	DEINTERLACE interrupt
19	SCALER	SCALER interrupt
20	AC97	AC97 interrupt
21	SPDIFRX	SPDIFRX interrupt
22	SPDIFTX	SPDIFTX interrupt
23	TIMER0	TIMER0 interrupt
24	TIMER1	TIMER1 interrupt
25	TIMER2	TIMER2 interrupt
26	TIMER3	TIMER3 interrupt
27	PWM0	PWM0 interrupt
28	PWM1	PWM1 interrupt
29	PWM2	PWM2 interrupt
30	PWM3	PWM3 interrupt
31	WDT	WDT interrupt
32	MPEGTSI	MPEGTSI interrupt
33	DISPLAYTOP0	DISPLAYDUALDISPLAYPRIM interrupt

Interrupt Number	Source	Description
34	DISPLAYTOP1	DISPLAYDUALDISPLAYSECOND interrupt
35	DISPLAYTOP2	DISPLAYRESCONV interrupt
36	DISPLAYTOP3	DISPLAYHDMI interrupt
37	VIP0	VIP0 interrupt
38	VIP1	VIP1 interrupt
39	MIPI	MIPI interrupt
40	3D GPU	3D GPU interrupt
41	ADC	ADC interrupt
42	PPM	PPM interrupt
43	SDMMC0	SDMMC0 interrupt
44	SDMMC1	SDMMC1 interrupt
45	SDMMC2	SDMMC2 interrupt
46	CODA9600	CODA960HOST interrupt
47	CODA9601	CODA960JPG interrupt
48	GMAC	GMAC interrupt
49	USB20OTG	USB20OTG interrupt
50	USB20HOST	USB20HOST interrupt
51	N/A	N/A
52	N/A	N/A
53	GPIOA	GPIOA interrupt
54	GPIOB	GPIOB interrupt
55	GPIOC	GPIOC interrupt
56	GPIOD	GPIOD interrupt
57	GPIOE	GPIOE interrupt
58	CRYPTO	CRYPTO interrupt
59	PDM	PDM interrupt
60	N/A	N/A
61	N/A	N/A
62	N/A	N/A
63	N/A	N/A

9.6 Internal GIC Interrupt Source

Table 9-2 GIC Interrupt Sources Description Table

Interrupt Number	Source	Description
0	CPU0 PMU	CPU0 PMU interrupt
1	CPU1 PMU	CPU1 PMU interrupt
2	CPU2 PMU	CPU2 PMU interrupt
3	CPU3 PMU	CPU3 PMU interrupt
4	L2CCINTR	L2 cache interrupt
5	MCUINTR	MCU interrupt

9.7 Register Summary

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Channel 0 programs 0 to 31 IRQ.
- Channel 1 programs 32 to 63 IRQ.

Register	Offset	Description	Reset Value
VICIRQSTATUS	0x00 (CH0) 0x00 (CH1)	IRQ Status Register	0x0
VICFIQSTATUS	0x04 (CH0) 0x04 (CH1)	FIQ Status Register	0x0
VICRAWINTR	0x08 (CH0) 0x08 (CH1)	RAW Interrupt Status Register	–
VICINTSELECT	0x0C (CH0) 0x0C (CH1)	Interrupt Select Register	0x0
VICINTENABLE	0x10 (CH0) 0x10 (CH1)	Interrupt Enable Register	0x0
VICINTENCLEAR	0x14 (CH0) 0x14 (CH1)	Interrupt Enable Clear Register	–
VICSOFTINT	0x18 (CH0) 0x18 (CH1)	Software Interrupt Register	0x0
VICSOFTINTCLEAR	0x1C (CH0) 0x1C (CH1)	Software Interrupt Clear Register	–
VICPROTECTION	0x20 (CH0) 0x20 (CH1)	Protection Enable Register	0x0
VICSWPRIORITYMASK	0x24 (CH0) 0x24 (CH1)	Software Priority Mask Register	16'hFFFF
VICVECTPRIORITYDAISY	0x28 (CH0) 0x28 (CH1)	Vector Priority Register For Daisy Chain	4'b1111
VICVECTADDR0	0x100 (CH0) 0x100 (CH1)	Vector Address 0 Registers	0x0
VICVECTADDR1	0x104 (CH0) 0x104 (CH1)	Vector Address 1 Registers	0x0
VICVECTADDR2	0x108 (CH0) 0x108 (CH1)	Vector Address 2 Registers	0x0
VICVECTADDR3	0x10C (CH0) 0x10C (CH1)	Vector Address 3 Registers	0x0
VICVECTADDR4	0x110 (CH0) 0x110 (CH1)	Vector Address 4 Registers	0x0
VICVECTADDR5	0x114 (CH0) 0x114 (CH1)	Vector Address 5 Registers	0x0
VICVECTADDR6	0x118 (CH0) 0x118 (CH1)	Vector Address 6 Registers	0x0

Register	Offset	Description	Reset Value
VICVECTADDR7	0x11C (CH0) 0x11C (CH1)	Vector Address 7 Registers	0x0
VICVECTADDR8	0x120 (CH0) 0x120 (CH1)	Vector Address 8 Registers	0x0
VICVECTADDR9	0x124 (CH0) 0x124 (CH1)	Vector Address 9 Registers	0x0
VICVECTADDR10	0x128 (CH0) 0x128 (CH1)	Vector Address 10 Registers	0x0
VICVECTADDR11	0x12C (CH0) 0x12C (CH1)	Vector Address 11 Registers	0x0
VICVECTADDR12	0x130 (CH0) 0x130 (CH1)	Vector Address 12 Registers	0x0
VICVECTADDR13	0x134 (CH0) 0x134 (CH1)	Vector Address 13 Registers	0x0
VICVECTADDR14	0x138 (CH0) 0x138 (CH1)	Vector Address 14 Registers	0x0
VICVECTADDR15	0x13C (CH0) 0x13C (CH1)	Vector Address 15 Registers	0x0
VICVECTADDR16	0x140 (CH0) 0x140 (CH1)	Vector Address 16 Registers	0x0
VICVECTADDR17	0x144 (CH0) 0x144 (CH1)	Vector Address 17 Registers	0x0
VICVECTADDR18	0x148 (CH0) 0x148 (CH1)	Vector Address 18 Registers	0x0
VICVECTADDR19	0x14C (CH0) 0x14C (CH1)	Vector Address 19 Registers	0x0
VICVECTADDR20	0x150 (CH0) 0x150 (CH1)	Vector Address 20 Registers	0x0
VICVECTADDR21	0x154 (CH0) 0x154 (CH1)	Vector Address 21 Registers	0x0
VICVECTADDR22	0x158 (CH0) 0x158 (CH1)	Vector Address 22 Registers	0x0
VICVECTADDR23	0x15C (CH0) 0x15C (CH1)	Vector Address 23 Registers	0x0
VICVECTADDR24	0x160 (CH0) 0x160 (CH1)	Vector Address 24 Registers	0x0
VICVECTADDR25	0x164 (CH0) 0x164 (CH1)	Vector Address 25 Registers	0x0
VICVECTADDR26	0x168 (CH0) 0x168 (CH1)	Vector Address 26 Registers	0x0
VICVECTADDR27	0x16C (CH0) 0x16C (CH1)	Vector Address 27 Registers	0x0
VICVECTADDR28	0x170 (CH0)	Vector Address 28 Registers	0x0

Register	Offset	Description	Reset Value
	0x170 (CH1)		
VICVECTADDR29	0x174 (CH0) 0x174 (CH1)	Vector Address 29 Registers	0x0
VICVECTADDR30	0x178 (CH0) 0x178 (CH1)	Vector Address 30 Registers	0x0
VICVECTADDR31	0x17C (CH0) 0x17C (CH1)	Vector Address 31 Registers	0x0
VICVECTPRIORITY0	0x200 (CH0) 0x200 (CH1)	Vector Priority 0 register	4'b1111
VICVECTPRIORITY1	0x204 (CH0) 0x204 (CH1)	Vector Priority 1 register	4'b1111
VICVECTPRIORITY2	0x208 (CH0) 0x208 (CH1)	Vector Priority 2 register	4'b1111
VICVECTPRIORITY3	0x20C (CH0) 0x20C (CH1)	Vector Priority 3 register	4'b1111
VICVECTPRIORITY4	0x210 (CH0) 0x210 (CH1)	Vector Priority 4 register	4'b1111
VICVECTPRIORITY5	0x214 (CH0) 0x214 (CH1)	Vector Priority 5 register	4'b1111
VICVECTPRIORITY6	0x218 (CH0) 0x218 (CH1)	Vector Priority 6 register	4'b1111
VICVECTPRIORITY7	0x21C (CH0) 0x21C (CH1)	Vector Priority 7 register	4'b1111
VICVECTPRIORITY8	0x220 (CH0) 0x220 (CH1)	Vector Priority 8 register	4'b1111
VICVECTPRIORITY9	0x224 (CH0) 0x224 (CH1)	Vector Priority 9 register	4'b1111
VICVECTPRIORITY10	0x228 (CH0) 0x228 (CH1)	Vector Priority 10 register	4'b1111
VICVECTPRIORITY11	0x22C (CH0) 0x22C (CH1)	Vector Priority 11 register	4'b1111
VICVECTPRIORITY12	0x230 (CH0) 0x230 (CH1)	Vector Priority 12 register	4'b1111
VICVECTPRIORITY13	0x234 (CH0) 0x234 (CH1)	Vector Priority 13 register	4'b1111
VICVECTPRIORITY14	0x238 (CH0) 0x238 (CH1)	Vector Priority 14 register	4'b1111
VICVECTPRIORITY15	0x23C (CH0) 0x23C (CH1)	Vector Priority 15 register	4'b1111
VICVECTPRIORITY16	0x240 (CH0) 0x240 (CH1)	Vector Priority 16 register	4'b1111
VICVECTPRIORITY17	0x244 (CH0) 0x244 (CH1)	Vector Priority 17 register	4'b1111

Register	Offset	Description	Reset Value
VICVECTPRIORITY18	0x248 (CH0) 0x248 (CH1)	Vector Priority 18 register	4'b1111
VICVECTPRIORITY19	0x24C (CH0) 0x24C (CH1)	Vector Priority 19 register	4'b1111
VICVECTPRIORITY20	0x250 (CH0) 0x250 (CH1)	Vector Priority 20 register	4'b1111
VICVECTPRIORITY21	0x254 (CH0) 0x254 (CH1)	Vector Priority 21 register	4'b1111
VICVECTPRIORITY22	0x258 (CH0) 0x258 (CH1)	Vector Priority 22 register	4'b1111
VICVECTPRIORITY23	0x25C (CH0) 0x25C (CH1)	Vector Priority 23 register	4'b1111
VICVECTPRIORITY24	0x260 (CH0) 0x260 (CH1)	Vector Priority 24 register	4'b1111
VICVECTPRIORITY25	0x264 (CH0) 0x264 (CH1)	Vector Priority 25 register	4'b1111
VICVECTPRIORITY26	0x268 (CH0) 0x268 (CH1)	Vector Priority 26 register	4'b1111
VICVECTPRIORITY27	0x26C (CH0) 0x26C (CH1)	Vector Priority 27 register	4'b1111
VICVECTPRIORITY28	0x270 (CH0) 0x270 (CH1)	Vector Priority 28 register	4'b1111
VICVECTPRIORITY29	0x274 (CH0) 0x274 (CH1)	Vector Priority 29 register	4'b1111
VICVECTPRIORITY30	0x278 (CH0) 0x278 (CH1)	Vector Priority 30 register	4'b1111
VICVECTPRIORITY31	0x27C (CH0) 0x27C (CH1)	Vector Priority 31 register	4'b1111
VICADDRESS	0xF00 (CH0) 0xF00 (CH1)	Vector address register	0x0
VICPERIPHID0	0xFE0 (CH0) 0xFE0 (CH1)	Peripheral Identification Register Bits 7:0	8'h92
VICPERIPHID1	0xFE4 (CH0) 0xFE4 (CH1)	Peripheral Identification Register Bits 15:8	8'h11
VICPERIPHID2	0xFE8 (CH0) 0xFE8 (CH1)	Peripheral Identification Register Bits 23:16	4'b0100
VICPERIPHID3	0xFEC (CH0) 0xFEC (CH1)	Peripheral Identification Register Bits 31:24	0x0
VICPCELLID0	0xFF0 (CH0) 0xFF0 (CH1)	Prime cell Identification Register Bits 7:0	8'h0D
VICPCELLID1	0xFF4 (CH0) 0xFF4 (CH1)	Prime cell Identification Register Bits 15:8	8'hF0
VICPCELLID2	0xFF8 (CH0)	Prime cell Identification Register Bits 23:16	8'h05

Register	Offset	Description	Reset Value
	0xFF8 (CH1)		
VICPCELLID3	0xFFC (CH0) 0xFFC (CH1)	Prime cell Identification Register Bits 31:24	8'hB1

9.7.1.1 VICIRQSTATUS

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x00 (CH0), 0x00 (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VICIRQSTATUS	[31:0]	R	Shows the status of the interrupts after masking by the VICINTENABLE andVICINTSELECT Registers: 0 = Interrupt is inactive (reset) 1 = Interrupt is active There is one bit of the register for each interrupt source.	0x0000_0000

9.7.1.2 VICFIQSTATUS

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x04 (CH0), 0x04 (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VICFIQSTATUS	[31:0]	R	Shows the status of the FIQ interrupts after masking by the VICINTENABLE and VICINTSELECT Registers: 0 = Interrupt is inactive (reset) 1 = Interrupt is active There is one bit of the register for each interrupt source.	0x0000_0000

9.7.1.3 VICRAWINTR

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x08 (CH0), 0x08 (CH1), Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
VICRAWINTR	[31:0]	R	Shows the status of the interrupts before masking by the Enable Registers: 0 = Interrupt is inactive before masking 1 = Interrupt is active before masking Because this register provides a direct view of the raw interrupt inputs, the reset value is unknown. There is one bit of the register for each interrupt source.	–

9.7.1.4 VICINTSELECT

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x0C (CH0), 0x0C (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VICINTSELECT	[31:0]	RW	Selects type of interrupt for interrupt request: 0 = IRQ interrupt (reset) 1 = FIQ interrupt. There is one bit of the register for each interrupt source	0x0000_0000

9.7.1.5 VICINTENABLE

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x10 (CH0), 0x10 (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VICINTENABLE	[31:0]	RW	Enables the interrupt request lines, which allow the interrupts to reach the processor. Read: 0 = Interrupt disabled (reset) 1 = Interrupt enabled The interrupt enable can only be set using this register. The VICINTENCLEAR Register must be used to disable the interrupt enable. Write: 0 = No effect 1 = Interrupt enabled On reset, all interrupts are disabled. There is one bit of the register for each interrupt source.	0x0000_0000

9.7.1.6 VICINTENCLEAR

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x14 (CH0), 0x14 (CH1), Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
VICINTENCLEAR	[31:0]	W	Clears corresponding bits in the VICINTENABLE Register: 0 = No effect 1 = Interrupt disabled in VICINTENABLE Register There is one bit of the register for each interrupt source	–

9.7.1.7 VICSOFTINT

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x18 (CH0), 0x18 (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VICSOFTINT	[31:0]	RW	Setting a bit HIGH generates a software interrupt for the selected source before interrupt masking. Read: 0 = Software interrupt inactive (reset) 1 = Software interrupt active Write: 0 = No effect 1 = Software interrupt enabled There is one bit of the register for each interrupt source.	0x0000_0000

9.7.1.8 VICSOFTINTCLEAR

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x1C (CH0), 0x1C (CH1), Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
VICSOFTINTCLEAR	[31:0]	W	Clears corresponding bits in the VICSOFTINT Register: 0 = No effect 1 = Software interrupt disabled in the VICSOFTINT Register There is one bit of the register for each interrupt source.	–

9.7.1.9 VICPROTECTION

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x20 (CH0), 0x20 (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	–
VICPROTECTION	[0]	RW	Enables or disables protected register access: 0 = Protection mode disabled (reset) 1 = Protection mode enabled When enabled, only privileged mode accesses (reads and writes) can access the interrupt controller registers, that is, when HPROT[1] is set HIGH for the current transfer. When disabled, both user mode and privileged mode can access the registers. This register can only be accessed in privileged mode, even when protection mode is disabled.	1'b0

9.7.1.10 VICSWPRIORITYMASK

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x24 (CH0), 0x24 (CH1), Reset Value = 0x0000_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
VICSWPRIORITYMASK	[15:0]	RW	Controls software masking of the 16 interrupt priority levels: 0 = Interrupt priority level is masked 1 = Interrupt priority level is not masked (reset) Each bit of the register is applied to each of the 16 interrupt priority levels.	0xFFFF

9.7.1.11 VICVECTPRIORITYDAISY

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x28 (CH0), 0x28 (CH1), Reset Value = 0x0000_000F

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	-
VECTPRIORITY	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 - 15. 15 is the lowest.	4'b1111

9.7.1.12 VICVECTADDR0

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x100 (CH0), 0x100 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR0	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.13 VICVECTADDR1

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x104 (CH0), 0x104 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR1	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.14 VICVECTADDR2

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x108 (CH0), 0x108 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR2	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.15 VICVECTADDR3

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x10C (CH0), 0x10C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR3	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.16 VICVECTADDR4

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x110 (CH0), 0x110 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR4	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.17 VICVECTADDR5

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x114 (CH0), 0x114 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR5	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.18 VICVECTADDR6

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x118 (CH0), 0x118 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR6	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.19 VICVECTADDR7

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x11C (CH0), 0x11C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR7	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.20 VICVECTADDR8

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x120 (CH0), 0x120 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR8	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.21 VICVECTADDR9

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x124 (CH0), 0x124 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR9	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.22 VICVECTADDR10

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x128 (CH0), 0x128 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR10	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.23 VICVECTADDR11

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x12C (CH0), 0x12C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR11	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.24 VICVECTADDR12

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x130 (CH0), 0x130 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR12	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.25 VICVECTADDR13

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x134 (CH0), 0x134 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR13	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.26 VICVECTADDR14

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x138 (CH0), 0x138 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR14	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.27 VICVECTADDR15

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x13C (CH0), 0x13C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR15	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.28 VICVECTADDR16

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x140 (CH0), 0x140 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR16	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.29 VICVECTADDR17

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x144 (CH0), 0x144 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR17	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.30 VICVECTADDR18

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x148 (CH0), 0x148 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR18	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.31 VICVECTADDR19

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x14C (CH0), 0x14C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR19	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.32 VICVECTADDR20

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x150 (CH0), 0x150 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR20	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.33 VICVECTADDR21

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x154 (CH0), 0x154 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR21	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.34 VICVECTADDR22

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x158 (CH0), 0x158 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR22	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.35 VICVECTADDR23

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x15C (CH0), 0x15C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR23	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.36 VICVECTADDR24

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x160 (CH0), 0x160 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR24	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.37 VICVECTADDR25

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x164 (CH0), 0x164 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR25	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.38 VICVECTADDR26

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x168 (CH0), 0x168 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR26	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.39 VICVECTADDR27

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x16C (CH0), 0x16C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR27	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.40 VICVECTADDR28

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x170 (CH0), 0x170 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR28	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.41 VICVECTADDR29

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x174 (CH0), 0x174 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR29	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.42 VICVECTADDR30

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x178 (CH0), 0x178 (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR30	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.43 VICVECTADDR31

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x17C (CH0), 0x17C (CH1), Reset Value = 32'h0000_0000

Name	Bit	Type	Description	Reset Value
VICVECTADDR31	[31:0]	RW	Contains ISR vector addresses. This register can be accessed with one wait state. This register must only be updated when the relevant interrupts are disabled. Receiving an interrupt while the vector address is being written to can result in unpredictable behavior. If the system does not support interrupt vector addresses, the VICVECTADDR registers can be programmed with the numbers of the interrupt source ports they relate to, so that the source of the active interrupt can be easily determined.	0x0000_0000

9.7.1.44 VICVECTPRIORITY0

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x200 (CH0), 0x200 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY0	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.45 VICVECTPRIORITY1

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x204 (CH0), 0x204 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY1	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.46 VICVECTPRIORITY2

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x208 (CH0), 0x208 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY2	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.47 VICVECTPRIORITY3

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x20C (CH0), 0x20C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY3	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.48 VICVECTPRIORITY4

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x210 (CH0), 0x210 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY4	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.49 VICVECTPRIORITY5

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x214 (CH0), 0x214 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY5	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.50 VICVECTPRIORITY6

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x218 (CH0), 0x218 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY6	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.51 VICVECTPRIORITY7

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x21C (CH0), 0x21C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY7	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.52 VICVECTPRIORITY8

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x220 (CH0), 0x220 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY8	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.53 VICVECTPRIORITY9

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x224 (CH0), 0x224 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY9	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.54 VICVECTPRIORITY10

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x228 (CH0), 0x228 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY10	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.55 VICVECTPRIORITY11

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x22C (CH0), 0x22C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY11	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.56 VICVECTPRIORITY12

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x230 (CH0), 0x230 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY12	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.57 VICVECTPRIORITY13

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x234 (CH0), 0x234 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY13	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.58 VICVECTPRIORITY14

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x238 (CH0), 0x238 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY14	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.59 VICVECTPRIORITY15

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x23C (CH0), 0x23C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY15	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.60 VICVECTPRIORITY16

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x240 (CH0), 0x240 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY16	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.61 VICVECTPRIORITY17

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x244 (CH0), 0x244 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY17	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.62 VICVECTPRIORITY18

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x248 (CH0), 0x248 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY18	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.63 VICVECTPRIORITY19

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x24C (CH0), 0x24C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY19	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.64 VICVECTPRIORITY20

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x250 (CH0), 0x250 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY20	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.65 VICVECTPRIORITY21

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x254 (CH0), 0x254 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY21	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.66 VICVECTPRIORITY22

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x258 (CH0), 0x258 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY22	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.67 VICVECTPRIORITY23

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x25C (CH0), 0x25C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY23	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.68 VICVECTPRIORITY24

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x260 (CH0), 0x260 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY24	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.69 VICVECTPRIORITY25

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x264 (CH0), 0x264 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY25	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.70 VICVECTPRIORITY26

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x268 (CH0), 0x268 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY26	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.71 VICVECTPRIORITY27

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x26C (CH0), 0x26C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY27	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.72 VICVECTPRIORITY28

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x270 (CH0), 0x270 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY28	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.73 VICVECTPRIORITY29

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x274 (CH0), 0x274 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY29	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.74 VICVECTPRIORITY30

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x278 (CH0), 0x278 (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY30	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.75 VICVECTPRIORITY31

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0x27C (CH0), 0x27C (CH1), Reset Value = 4'b1111

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
VECTPRIORITY31	[3:0]	RW	Selects vectored interrupt priority level. User can select any of the 16 vectored interrupt priority levels by programming the register with the hexadecimal value of the priority level required, from 0 to 15. 15 is the lowest.	4'b1111

9.7.1.76 VICADDRESS

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xF00 (CH0), 0xF00 (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
vectaddr	[31:0]	RW	Contains the address of the currently active ISR, with reset value 0x00000000. A read of this register returns the address of the ISR and sets the current interrupt as being serviced. A read must only be performed while there is an active interrupt. A write of any value to this register clears the current interrupt. A write must only be performed at the end of an interrupt service routine.	0x0000_0000

9.7.1.77 VICPERIPHID0

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFE0 (CH0), 0xFE0 (CH1), Reset Value = 0x0000_0092

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
partnumber0	[7:0]	R	These bits read back as 0x92	8'h92

9.7.1.78 VICPERIPHID1

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFE4 (CH0), 0xFE4 (CH1), Reset Value = 0x0000_0011

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
designer0	[7:4]	R	These bits read back as 0x1.	4'b0001
partnumber1	[3:0]	R	These bits read back as 0x1.	4'b0001

9.7.1.79 VICPERIPHID2

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFE8 (CH0), 0xFE8 (CH1), Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
revision	[7:4]	R	These bits read back as the revision number, which can be between 0 and 15.	4'b0000
designer1	[3:0]	R	These bits read back as 0x4.	4'b0100

9.7.1.80 VICPERIPHID3

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFEC (CH0), 0xFEC (CH1), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
configuration	[7:2]	R	These bits read back as 0x0.	6'b000000
configuration	[1:0]	R	Indicates the number of interrupts supported: 00 = 32 (default) 01 = 64 10 = 128 11 = 256	2'b00

9.7.1.81 VICPCELLID0

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFF0 (CH0), 0xFF0 (CH1), Reset Value = 0x0000_000D

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
VICPCELLID0	[7:0]	R	These bits read back as 0x0d	8'h0D

9.7.1.82 VICPCELLID1

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFF4 (CH0), 0xFF4 (CH1), Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
VICPCELLID1	[7:0]	R	These bits read back as 0xF0	8'hF0

9.7.1.83 VICPCELLID2

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFF8 (CH0), 0xFF8 (CH1), Reset Value = 0x0000_0005

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
VICPCELLID2	[7:0]	R	These bits read back as 0x05	8'h05

9.7.1.84 VICPCELLID3

- Base Address: 0xC000_2000
- Base Address: 0xC000_3000
- Address = Base Address + 0xFFC (CH0), 0xFFC (CH1), Reset Value = 0x0000_00B1

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
VICPCELLID3	[7:0]	R	These bits read back as 0xB1	8'hB1

10 Watch Dog Timer

10.1 Overview

Watchdog timer is used to resume the controller operation whenever it is disturbed by malfunction such as noise and system error. It can be used as normal 16bit interval timer to request interrupt service. The watchdog timer generates the reset signal.

Difference in usage WDT compared with PWM timer is that WDT generates the reset signal.

10.2 Features

Features of WDT are:

- Normal interval timer mode with interrupt request
- Internal reset signal is activated when the timer count value reaches 0 (time-out).
- Level-triggered interrupt mechanism

10.3 Functional Description

10.3.1 Watchdog Timer Operation

Figure 10-1 shows the functional block diagram of the watchdog timer. The watchdog timer uses only PCLK as its source clock. The PCLK frequency is prescaled to generate the corresponding watchdog timer clock, and the resulting frequency is divided again.

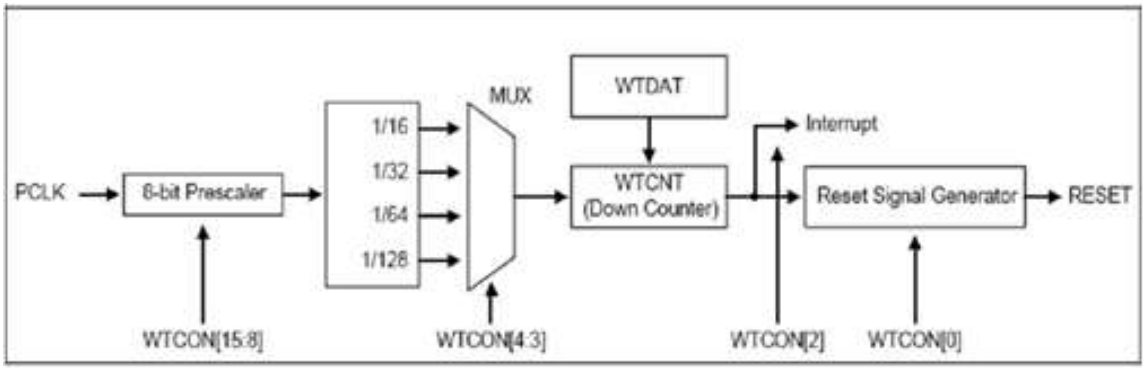


Figure 10-1 Watchdog Timer Block Diagram

The prescaler value and the frequency division factor are specified in the watchdog timer control (WDTCON) register. Valid prescaler values range from 0 to 2^8-1. The frequency division factor can be selected as 16, 32, 64 or 128.

Use the following equation to calculate the watchdog timer clock frequency and the duration of each timer clock cycle:

t_watchdog = 1/(PCLK/(Prescaler value + 1)/Division_factor)

10.3.2 WTDAT & WTCNT

Once the watchdog timer is enabled, the value of watchdog timer data (WTDAT) register cannot be automatically reloaded into the timer counter (WTCNT). In this reason, an initial value must be written to the watchdog timer count (WTCNT) register, before the watchdog timer starts.

10.3.3 Consideration of Debugging Environment

When the MDIRAC-III is in debug mode Embedded ICE, the watchdog timer must not operate. The watchdog timer can determine whether or not it is currently in the debug mode from the CPU core signal (DBGACK signal). Once the DBGACK signal is asserted, the reset output of the watchdog timer is not activated as the watchdog timer is expired.

10.3.4 Special Function Register

10.3.4.1 Memory map

Register	Type	Description	Reset Value
WTCON	RW	Watchdog timer control register	0x8021
WTDAT	RW	Watchdog timer data register	0x8000
WTCNT	RW	Watchdog timer count register	0x8000
WTCLRINT	W	Watchdog timer interrupt register	–

10.3.4.2 Watchdog Timer Control (WTCON) Register

The WTCON register allows the user to enable/disable the watchdog timer, select the clock signal from 4 different sources, enable/disable interrupts, and enable/disable the watchdog timer output.

The Watchdog timer is used to resume restart in mal-function after its power on, if controller restart is not desired, the Watchdog timer should be disabled.

If the user wants to use the normal timer provided by the Watchdog timer, enable the interrupt and disable the Watchdog timer.

10.3.4.3 Watchdog Timer Data (WTDAT) Register

The WTDAT register is used to specify the time-out duration. The content of WTDAT cannot be automatically loaded into the timer counter at initial watchdog timer operation. However, using 0x8000(initial value) will drive the first time_out. In this case, the value of WTDAT will be automatically reloaded into WTCNT.

10.3.4.4 Watchdog Timer Count (WTCNT) Register

The WTCNT register contains the current count values for the watchdog timer during normal operation. Note that the content of WTDAT register cannot be automatically loaded into the timer count register when the watchdog timer is enabled initially, so the WTCNT register must be set to initial value before enabling it.

10.3.4.5 Watchdog Timer Interrupt (WTCLRINT) Register

The WTCLRINT register is used to clear the interrupt. Interrupt service routine is responsible for clearing the relevant interrupt after the interrupt service is completed. Writing any values on this register clears the interrupt. Reading this register is not allowed.

10.4 Register Description

10.4.1 Register Map Summary

- Base Address: 0xC001_9000h

Register	Offset	Description	Reset Value
WTCON	0x00h	Watchdog Timer Control register	0x8021
WTDAT	0x04h	Watchdog Timer Data register	0x8000
WTCNT	0x08h	Watchdog Timer Count register	0x8000
WTCLRINT	0x0Ch	Watchdog Timer Interrupt register	–

10.4.1.1 WTCON

- Base Address: 0xC001_9000h
- Address = Base Address + 0x00h, Reset Value = 0x0000_8021

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
prescaler value	[15:8]	RW	Prescaler value. The valid range is from 0 to (28-1).	0x80
RSVD	[7:6]	–	Reserved	–
watchdog timer	[5]	RW	Enable or disable bit of Watchdog timer. 0 = Disable 1 = Enable	1'b1
clock select	[4:3]	RW	Determine the clock division factor. 00 = 16 01 = 32 10 = 64 11 = 128	2'b0
interrupt generation	[2]	RW	Enable or disable bit of the interrupt. 0 = Disable 1 = Enable	1'b0
RSVD	[1]	–	Reserved	–
Reset enable/disable	[0]	RW	Enable or disable bit of Watchdog timer output for reset signal. 0 = Disable the reset function of the watchdog timer. 1 = Assert reset signal of the NXP4330Q at watchdog time-out.	1'b0

10.4.1.2 WTDAT

- Base Address: 0xC001_9000h
- Address = Base Address + 0x04h, Reset Value = 0x0000_8000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
wtdat	[15:0]	RW	Watchdog timer count value for reload.	0x8000

10.4.1.3 WTCNT

- Base Address: 0xC001_9000h
- Address = Base Address + 0x08h, Reset Value = 0x0000_8000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
WTCNT	[15:0]	RW	The current value of the watchdog timer	0x8000

10.4.1.4 WTCLRINT

- Base Address: 0xC001_9000h
- Address = Base Address + 0x0Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
WTCLRINT	[31:0]	W	Write any values clears the interrupt	–

11 RTC

11.1 Overview

The Real Time Clock (RTC) block can be operated by the Backup Battery while the system power is off. The RTC block is composed of 32-bit free counter register and works with an external 32.768 kHz Crystal and also can perform the alarm function.

11.2 Features

- 32-bit Counter
- Alarm Function : Alarm Interrupt or Wake Up from Power Down Mode
- Independent power pin (VDD_RTC)
- Supports 1 Hz Time interrupt for Power Down Mode
- Generates Power Management Reset signal

11.3 Block Diagram

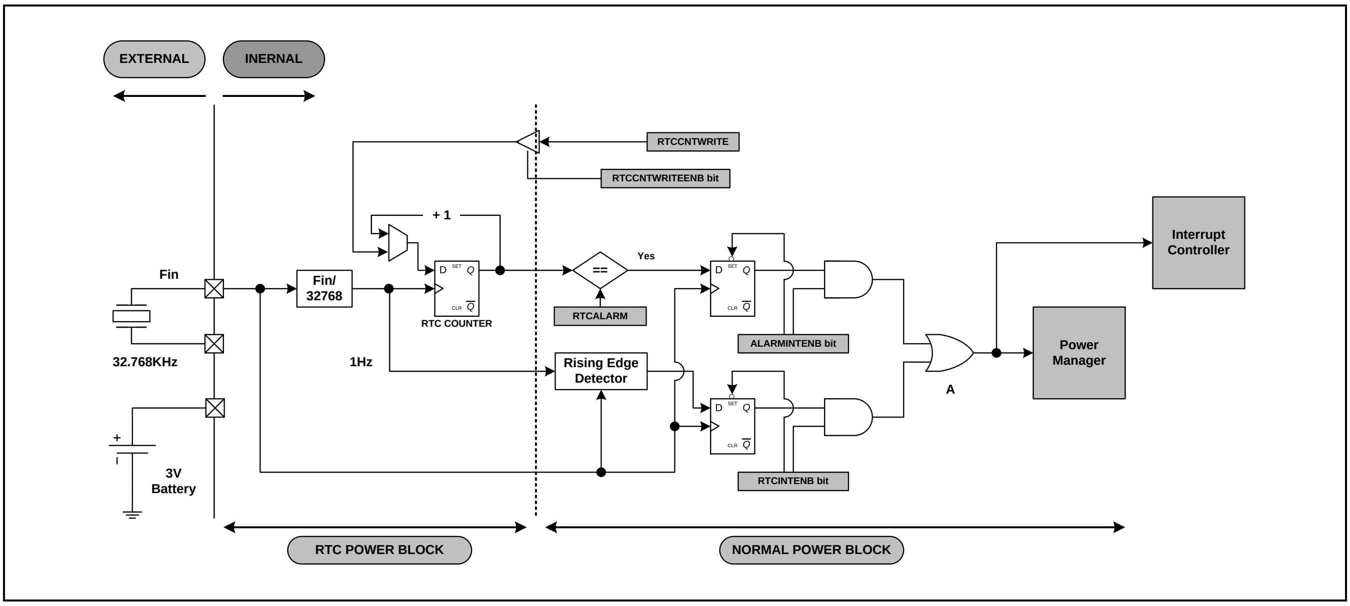


Figure 11-1 RTC Block Diagram

Figure 11-1 shows the RTC block diagram. The RTC block receives an external clock of 32.768 kHz and divides it into 1 Hz with 32.768 kHz. The RTC Counter operates depending on the external clock.

NOTE: As shown in *Figure 11-1*, the left and right parts of the central dotted line use RTC Power and Normal Power, separately. The RTC Power Block uses a mercury battery, but the block actually using the mercury battery is the RTC Counter in the RTC Power Block. The battery life is about five years.

In *Figure 11-1*, the output in point [A] is applied to the Power Manager or the Interrupt Controller. The output is applied to the Interrupt Controller in Normal mode and applied to the Power Manager in Power mode.

NOTE: Even if RTC is not used, RTC power and RTC clock should be supplied.

11.4 Functional Description

11.4.1 Backup Battery Operation

As shown in *Figure 11-1*, since the RTC block uses a separate power source (Coin Battery), the RTC block operates even when the external power is turned off.

The RTC Logic can be driven by the Backup Battery, which supplies the power through the VDD_RTC pin into the RTC Block, even if the system power is off. When the system power is off, the interfaces of the CPU and RTC logic should be blocked and the backup battery only drives the oscillation circuit and the internal 32-bit RTC counter to minimize power dissipation. In other words, the RTC block can be used as the Wake-Up Source when the S5P4418 is converted into Power Down mode.

The use of the RTC block as a Wake-Up source requires that the RTCCTRL.ACCESSENB bit is set as "0" before the system enters Power Down mode. Setting it as "0" is performed to use the RTC as the Wake-Up source even when the system enters the Power Down Mode. (For detailed information on the Power Down Mode, refer to Section 4.)

Even if the RTC block is not used, the RTC Clock must be connected to S5P4418 because the RTC clock is used as the clock for power management operation.

11.4.2 RTC Operation

The RTC generates an alarm signal at a specified time in the Power Down Mode or Normal Operation Mode. In Normal Operation Mode, the Alarm Interrupt is activated. In Power Down Mode, the Power Management Wake Up Signal is activated as well as the RTCALARM. The ALARM Time Set register (RTCALARM) determines the condition of the alarm time setting and the RTCINTENB.ALARMINTENB bit determines the alarm enable/disable status.

The procedure to generate an alarm interrupt is as follows:

First, write a counter value to the RTCCNTWRITE register. (To this end, the busy status of the RTCCTRL.RTCCNTWAIT should be checked in advance. The written value is applied to the register after two 32.768 kHz clock cycles.) After that, write the value of the point at which you wish to generate an interrupt to the RTCALARM register. The RTC counter increases the counter value at intervals of 1 Hz. If the values of the two registers (RTCCNTWRITE and RTCAKARM registers) become equal when the RTCINTENB.ALARMINTENB bit is set as "1", an interrupt occurs.

In a similar way, the RTC interrupt is detected in a rising edge of 1 Hz. In this case, the interrupt is generated by setting the RTCINTENB.RTCINTENB bit as "1".

In addition, The RTCINTENB register contains the Pending Clear function and the Pending Clear is performed by writing "0".

11.4.3 Accessing the RTC Time Counter Setting/Read Register

To access RTC Time Count Read Register (RTCCNTREAD) and RTC Time Count Setting Register (RTCCNTWRITE), the RTCCTRL.RTCCNTWRITEENB bit is set to "1" before accessing these register. When the CPU completes to access these register, the CPU should set the RTCCTRL.RTCCNTWRITEENB bit to "0" to protect the content of RTC counter from unknown problem in abnormal state. The RTCCNTWRITEENB bit determines the reflection of the RCCNTWRITE register value to the RTC counter.

11.4.4 Interrupt Pending Register

Only the "READ" function is available for the RTCINTPND register of the S5P4418, but the current pending status can be read.

Since the RTCINTPND register only has a "READ" function, the Pending Clear function is controlled by the RTCINTENB register. The Interrupt Pending status is cleared by disabling the relevant interrupt. Therefore, if the corresponding bit of the RTCINTENB register is set as "1", the relevant interrupt is enabled. If the corresponding bit is set as "0", the interrupt is disabled and the pending bit is also cleared.

11.4.5 Power Manager Reset Time Control

RTC controls the time when nPWRMANRST (Power Manager Reset) releases from CorePOR. Refer to RTCCORERSTIMESEL Register for setting the time when nPWRMANRST releases.

11.5 Register Description

11.5.1 Register Map Description

- Base Address: 0xC001_0C00h

Register	Offset	Description	Reset Value
RTCCNTWRITE	0x00h	RTC time count setting register	–
RTCCNTREAD	0x04h	RTC time count read register	–
RTCALARM	0x08h	Alarm time count set register	0x0000_0000
RTCCTRL	0x0Ch	RTC control register	0x0000_0000
RTCINTENB	0x10h	RTC interrupt enable register	0x0000_0000
RTCINTPND	0x14h	RTC interrupt pending register	0x0000_0000
RTCCORERSTIMESEL	0x18h	RTC core por time select register	0x0000_0000
RTCSCRATCH	0x1Ch	RTC scratch register	0x0000_0000

11.5.1.1 RTCCNTWRITE

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x00h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
rtccntwrite	[31:0]	W	Set RTC Counter Value. (Unit : 1Hz) The RTCCNTWAIT bit of the RTCCONTROL register should be checked before a value is written in this bit. If the RTCCNTWAIT bit is "1", this written value is not reflected. The written value is reflected to this register at least two cycles of 32768 Hz after it is changed to "0". To write a value to this register, the RTCCNTWRITEENB bit should be set as "1"'.	-

NOTE: RTC reset to unknown values. If RTC power is first applied

11.5.1.2 RTCCNTREAD

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x04h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
rtccntread	[31 : 0]	R	Read Current RTC Counter Value. (Unit: 1 Hz) The value of the RTC counter is continuously changed.	-

11.5.1.3 RTCALARM

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
rtcalarm	[31 : 0]	RW	ALARM Time Set Register. (Unit: 1 Hz) The ALARMCNTWAIT bit of the RTCCONTROL register should be checked before a value is written in this bit. If the RTCCNTWAIT bit is "1", this written value is not reflected. The written value is reflected to this register at least two cycles of 32768 Hz after it is changed to "0".	32'b0

11.5.1.4 RTCCTRL

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31 : 5]	-	Reserved	27'b0
RTCCNTWAIT	[4]	R	RTCCNTWAIT: Register to check if the previously requested "WRITE" is completed when writing a value to the RTCCNTWRITE register. The bit below indicates the status of the RTCCNTWRITE*register. 0 = IDLE 1 = Busy	1'b0
ALARMCNTWAIT	[3]	R	ALARMCNTWAIT: Register to check if the previously requested "WRITE" is completed when writing a value to the RTCALARM*register. The bit below indicates the status of the RTCALARMWRITE*register 0 = IDLE 1 = Busy	1'b0
RSVD	[2]	-	Reserved	1'b0
RSVD	[1]	-	Reserved. However, `0' should be written.	1'b0
RTCCNTWRITEENB	[0]	RW	RTCCNTWRITEENB: Control Power isolation and connection of RTC block. This bit should be "0" before Power Down Mode for normal operation of RTC in Power Down Mode. 0 = Disable (Power Isolation) 1 = Enable (Power Connection) To access the RTCCNTREAD and RTCCNTWRITE registers, this bit should be set as "1".	1'b0

11.5.1.5 RTCINTENB

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	30'b0
ALARMINTENB	[1]	RW	ALARMINTENB: Set ALARM Interrupt On/Off and Pending Clear/Interrupt Enable READ 0 = Interrupt Disable 1 = Interrupt Enable WRITE 0 = Pending Clear & Interrupt Disable 1 = Interrupt Enable	1'b0
RTCINTENB	[0]	RW	RTCINTENB : Set RTC (1 Hz Only) Interrupt On/Off and Pending Clear/Interrupt Enable READ 0 = Interrupt Disable 1 = Interrupt Enable WRITE 0 = Pending Clear & Interrupt Disable 1 = Interrupt Enable	1'b0

11.5.1.6 RTCINTPND

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	30'b0
ALARMINTPEND	[1]	R	ALARMINTEPND: ALARM Interrupt Pending bit. 0 = None 1 = Interrupt Pended	1'b0
RTCINTPEND	[0]	R	RTCINTPEND: Set RTC (1 Hz Only) Interrupt Pending bit. 0 = None 1 = Interrupt Pended	1'b0

11.5.1.7 RTCCORERSTIMESEL

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x18h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31 : 2]	–	Reserved	30'b0
COREPORtimeSEL6	[6:0]	RW	CORE POR (Power On Reset) releases with the delay of about 186 ms after CORE VDD Power is turned on. 0 = None 1 = Select	1'b0
COREPORTimeSEL5	[5]	RW	CORE POR (Power On Reset) releases with the delay of about 155 ms after CORE VDD Power is turned on. 0 = None 1 = Select	1'b0
COREPORtimeSEL4	[4]	RW	CORE POR (Power On Reset) releases with the delay of about 124 ms after CORE VDD Power is turned on. 0 = None 1 = Select	1'b0
COREPORtimeSEL3	[3]	RW	CORE POR (Power On Reset) releases with the delay of about 93 ms after CORE VDD Power is turned on. 0 = None 1 = Select	1'b0
COREPORtimeSEL2	[2]	RW	CORE POR (Power On Reset) releases with the delay of about 62 ms after CORE VDD Power is turned on. 0 = None 1 = Select	1'b0
COREPORtimeSEL1	[1]	RW	CORE POR (Power On Reset) releases with the delay of about 31 ms after CORE VDD Power is turned on. 0 = None 1 = Select	1'b0
COREPORtimeSEL0	[0]	RW	CORE POR (Power On Reset) releases without delay after CORE VDD Power is turned on. 0 = None 1 = Select	1'b0

NOTE: CORE POR releases about 210 ms after CORE VDD Power is turned on when RTCCOREPORIMESEL[6:0] == 7'b0

11.5.1.8 WTCON

- Base Address: 0xC001_0C00h
- Address = Base Address + 0x1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RTCscratch	[31:0]	RW	RTC scratch register.	32'b0

12 Alive

12.1 Overview

In the status with eliminating core power supply of S5P4418, some PAD need power supply continuously and should keep driving PAD with certain value.

For example a bit that controlling STN LCD should keep driving PAD with low in the status with eliminating core power supply. 32-bit value can be saved in Scratch Register and the saved value maintains in the case of core power off.

User could on/off the system power by pressing toggle switch and ALIVE performs the necessary functions in these momentary power controls.

12.2 Features

Alive GPIO PADs are all in/output PAD.

- The value of ALIVE Block maintains even in power off of Core Power.
- Alive Block does not use clock. To change the control register value, need to program set/reset pin of SR-flipflop directly.
- Chip sleep mode wake-up source (AliveGPIO, VDDToggle, RTCIRQ)
- Power IC Enable.
- Supports the PAD Hold function

Scan chain is not inserted to Alive GPIO.

12.3 Power Isolation

12.3.1 Core Power Off

In the case of power off of CoreVDD, Alive Registers maintains its value since Alive VDD keep supplied. Pull-down register connected to nPowerGating performs the function of maintaining control bit of Alive Registers securely in the interval of core power off or unstable.

12.3.2 Power Gating

The value of set/reset should be kept as low to maintains the value of Alive Registers securely in the case of power off of CoreVDD. Therefore, it's designed to maintain low value in the case of core power off since nPowerGating register is connected to pull-down register.

12.4 Alive Registers

All of the Registers except nPowerGating/AliveDetectPending Register of Alive block maintains the value written in Register when Core power turns off, and are reset when Alive Power turns off. Alive Registers do not have their own Clock, and these can be read and written when nPowerGating register is "1" (nPowerGating = 1). And especially, in write mode, Alive Registers can be written by SET/RST (reset) Register. The following is the example of the Register function according to Register SET/RST.

Alive Registers remains as the former state when Regiser_nameSET == 0, Regiser_nameRST=0
Alive Registers are written as "1" when Regiser_nameSET == 1, Regiser_nameRST=0
Alive Registers are written as "0" write "0" when Regiser_nameSET == 0, Regiser_nameRST=1
Alive Registers are written as "1" when Regiser_nameSET == 1, Regiser_nameRST=1

12.4.1 Alive GPIO Detect Registers

For Alive GPIO input, Alive GPIO Detect Registers can be used as Core Power on, Alive Interrupt, Sleep mode wakeup source in case of Asynchronous/synchronous detecting mode. And when those events are detected, ALIVEGPIODETECTPENDREG[n] Register is set to "1". The following are the operating examples according to Detecting modes.

Ex1) Asynchronous Low Level Detecting
Alive GPIO Detect Registers detect the event when ALIVEGPIOLOWASYNCDETECTMODEREADREG [n] = "1", ALIVEGPIODETECTENBREADREG[n] = "1", and AliveGPIO ==0

Ex2) Asynchronous High Level Detecting
Alive GPIO Detect Registers detect the event when ALIVEGPIOHIGHASYNCDETECTMODEREADREG [n] = "1", ALIVEGPIODETECTENBREADREG[n] = "1", and AliveGPIO[n] == "1"

Ex3) Synchronous Low Level Detecting
Alive GPIO Detect Registers detect the event when ALIVEGPIOLOWSYNCDETECTMODEREADREG [n] = "1", ALIVEGPIODETECTENBREADREG[n] = "1", AliveGPIO[n] == "0"

Ex4) Synchronous High Level Detecting
Alive GPIO Detect Registers detect the event when ALIVEGPIOHIGHSYNCDETECTMODEREADREG [n] = "1", ALIVEGPIODETECTENBREADREG[n] = "1", AliveGPIO[n] == "1"

Ex5) Synchronous Falling Edge Detecting
Alive GPIO Detect Registers detect the event when ALIVEGPIOFALLDETECTMODEREADREG[n] = "1", ALIVEGPIODETECTENBREADREG[n] = "1", and AliveGPIO[n] bit changes from "1" to "0"

Ex6) Synchronous Rising Edge Detecting
Alive GPIO Detect Registers detect the event when ALIVEGPIORISEDETECTMODEREADREG [n] = "1", ALIVEGPIODETECTENBREADREG[n] = "1", and AliveGPIO[n] bit changes from "0" to "1"

12.4.2 Scratch Register

Programmer could save any 32bit value in Scratch Register. The value of Scratch Register maintains in the case of power off of CoreVDD.

12.4.3 Alive GPIO Control Registers

Alive GPIO is controlled through Alive Block regardless of GPIO block.

Control Register has AliveGPIO in/out mode enable, pull-up, and AliveGPIOPADOut.

12.5 Momentary Power Control

12.5.1 CoreVDD Powering On

The Core Power can be changed from off-state to on-state by the VDDPWRTOGGLE switch, AliveGPIO Detecting, RTC interrupt. And in case of Power on, VDDPWRTOGGLE switch, AliveGPIO Detecting, and RTC interrupt can be processed, after system booting, by setting VDDPWRON_DDR/VDDPWRON Bit. (Power On is not allowed when Battery Fault occurs.).

12.5.2 CoreVDD Powering Off

The Core Power can be changed from off-state to on-state by clearing VDDPWRON_DDR/VDDPWRON Bit.

Core Block and Alive Block are connected through PowerGating Register, which makes it possible for Alive Registers to safely sustain their own values even after Core Power turns off with VDDPWRON_DDR/VDDPWRON Bit cleared.

The following is the example of Chip Power sequence

1. Do not hold the initial Pad state. (nPadHold = 1)
2. Hold the Pad before you turn off the Power. (nPadHold Register = 0)
3. Turn off VDDPWRON
4. Non-Alive POR is set low after power turns off
5. Power starts to be supplied by pressing toggle switch
6. PAD releases from the hold state when internal POR turns on (which provides the stability for preventing pad hold from releasing after power turns on)
7. VDDPWRON and PadHold Register should be released simultaneously after system booting.
8. VDDPOWRON should be released.

nPadHoldEnb Register should be set as "0" except Power On Reset.

12.6 SLEEP Mode

S5P4418 supports two SLEEP Modes (SleepMode1, SleepMode2). Core power turns off in SLEEP Mode, and the Chip wakes up from SLEEP Mode by Wake-up sources such as AliveGPIO Detecting, RTC Interrupt, and nVDDPWRTOGGLE Switch push.(And, No wake-up is possible in case of battery fault)

- Alive GPIO Detect Pending Register Clear
- Hold the Pad before user turns off Power. (SleepMode1: nPadHold[2:1] = 2'b00, SleepMode2: nPadHold[2:0] == 3'b000)
- VDDPWRON Register Clear
- nPowerGating Register Clear
- S5P4418 STOP Mode Set(Refer to Clock and Power management Section)

12.7 PMU (Power management Unit)

12.7.1 Overview

PMU is a block inside of ALIVE. It controls internal power switch of sub-blocks in chip.

PMU can controls the power up and down of these blocks:

- GPU (graphic processing unit)
- MFC (multi function codec)

12.7.2 Power Mode Table

MODE		PD_RTC	PD_ALIVE	PD_TOP	PD_DREX	PD_CODEC	PD_GR3D	PD_CPU
Num.	Name							
1	POWER ON RESET	ON	ON	ON	ON	ON	ON	ON
2	NORMAL	ON	ON	ON	ON	ON	ON	ON
3	SUB SLEEP - 0	ON	ON	ON	ON	OFF	ON	ON
4	SUB SLEEP - 1	ON	ON	ON	ON	ON	OFF	ON
5	SUB SLEEP - ALL	ON	ON	ON	ON	OFF	OFF	ON
6	DEEP IDLE	ON	ON	ON	ON	OFF	OFF	OFF
7	TOP SLEEP	ON	ON	OFF	OFF	OFF	OFF	OFF
8	RTC ONLY	ON	OFF	OFF	OFF	OFF	OFF	OFF

12.7.3 Power Switch Control Sequence

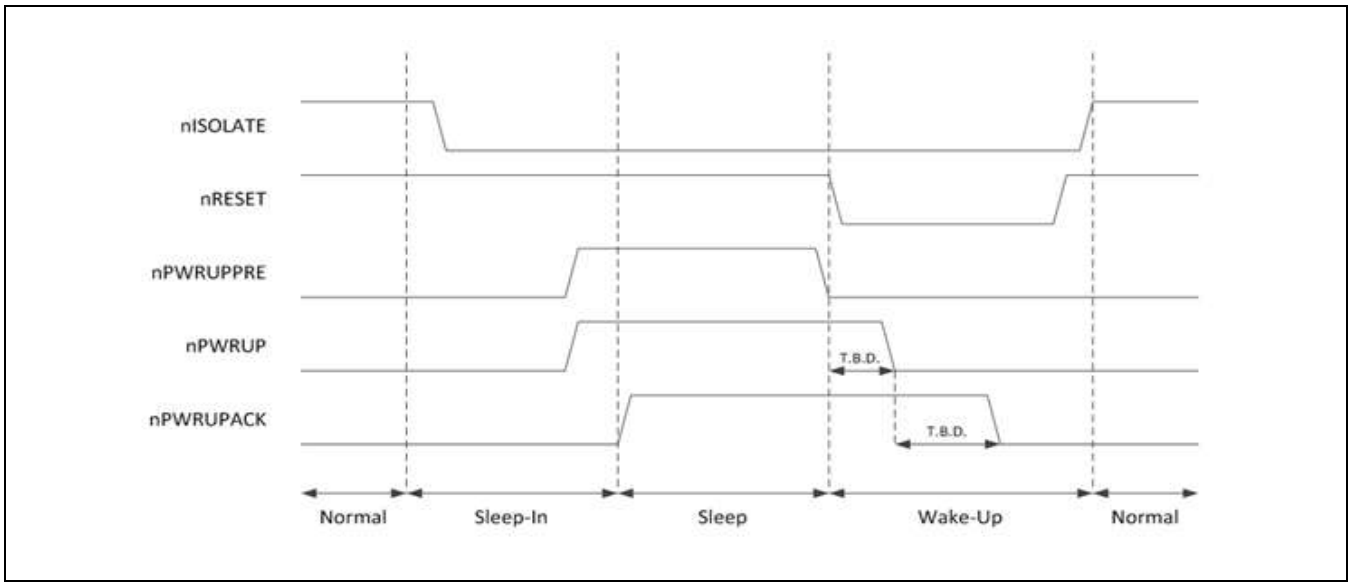


Figure 12-1 Power Switch Control Sequence

12.8 Register Description

12.8.1 Register Map Summary

- Base Address:C001_0000h

Register	Offset	Description	Reset Value
ALIVEPWRGATEREG	0800h	Alive Power Gating Register	0x0000_0000
ALIVEGPIOASYNCDETECTMODERSTREG0	0804h	Alive GPIO ASync Detect Mode Reset Register 0	0x0000_0000
ALIVEGPIOASYNCDETECTMODERSTREG1	0810h	Alive GPIO ASync Detect Mode Reset Register 1	0x0000_0000
ALIVEGPIOASYNCDETECTMODESETREG0	0808h	Alive GPIO ASync Detect Mode Set Register 0	0x0000_0000
ALIVEGPIOASYNCDETECTMODESETREG1	0814h	Alive GPIO ASync Detect Mode Set Register 1	0x0000_0000
ALIVEGPIOLOWASYNCDETECTMODEREADREG	080Ch	Alive GPIO Low Level Async Detect Mode Read Register	0x0000_0000
ALIVEGPIOHIGHASYNCDETECTMODEREADREG	0818h	Alive GPIO High Level Async Detect Mode Read Register	0x0000_0000
ALIVEGPIODETECTMODERSTREG0	081Ch	Alive GPIO Detect Mode Reset Register 0	0x0000_0000
ALIVEGPIODETECTMODERSTREG1	0828h	Alive GPIO Detect Mode Reset Register 1	0x0000_0000
ALIVEGPIODETECTMODERSTREG2	0834h	Alive GPIO Detect Mode Reset Register 2	0x0000_0000
ALIVEGPIODETECTMODERSTREG3	0840h	Alive GPIO Detect Mode Reset Register 3	0x0000_0000
ALIVEGPIODETECTMODESETREG0	0820h	Alive GPIO Detect Mode Set Register 0	0x0000_0000
ALIVEGPIODETECTMODESETREG1	082Ch	Alive GPIO Detect Mode Set Register 1	0x0000_0000
ALIVEGPIODETECTMODESETREG2	0838h	Alive GPIO Detect Mode Set Register 2	0x0000_0000
ALIVEGPIODETECTMODESETREG3	0844h	Alive GPIO Detect Mode Set Register 3	0x0000_0000
ALIVEGPIOFALLDETECTMODEREADREG	0824h	Alive GPIO Falling Edge Detect Mode Read Register	0x0000_0000
ALIVEGPIORISEDETECTMODEREADREG	0830h	Alive GPIO Rising Edge Detect Mode Read Register	0x0000_0000
ALIVEGPIOLOWDETECTMODEREADREG	083Ch	Alive GPIO Low Level Detect Mode Read Register	0x0000_0000
ALIVEGPIOHIGHDETECTMODEREADREG	0848h	Alive GPIO High Level Detect Mode Read Register	0x0000_0000
ALIVEGPIODETECTENBRSTREG	084Ch	Alive GPIO Detect Enable Reset Register	0x0000_0000

Register	Offset	Description	Reset Value
ALIVEGPIODETECTENBSETREG	0850h	Alive GPIO Detect Enable Set Register	0x0000_0000
ALIVEGPIODETECTENBREADREG	0854h	Alive GPIO Detect Enable Read Register	0x0000_0000
ALIVEGPIOINTENBRSTREG	0858h	Alive GPIO Interrupt Enable Reset Register	0x0000_0000
ALIVEGPIODETECTENABLESETREG	085Ch	Alive GPIO Detect Enable Set Register	0x0000_0000
ALIVEGPIOINTENBREADREG	0860h	Alive GPIO Interrupt Enable Read Register	0x0000_0000
ALIVEGPIODETECTPENDREG	0864h	Alive GPIO Detect Pending Register	0x0000_0000
ALIVESCRATCHRSTREG	0868h	Alive Scratch Reset Register	0x0000_0000
ALIVESCRATCHSETREG	086Ch	Alive Scratch Set Register	0x0000_0000
ALIVESCRATCHREADREG	0870h	Alive Scratch Read Register	0x0000_0000
ALIVEGPIOPADOUTENBRSTREG	0874h	Alive GPIO PAD Out Enable Reset Register	0x0000_0000
ALIVEGPIOPADOUTENBSETREG	0878h	Alive GPIO PAD Out Enable Set Register	0x0000_0000
ALIVEGPIOPADOUTENBREADREG	087Ch	Alive GPIO PAD Out Enable Read Register	0x0000_0000
ALIVEGPIOPADPULLUPRSTREG	0880h	Alive GPIO PAD Pullup Reset Register	0x0000_0000
ALIVEGPIOPADPULLUPSETREG	0884h	Alive GPIO PAD Pullup Set Register	0x0000_0000
ALIVEGPIOPADPULLUPREADREG	0888h	Alive GPIO PAD Pullup Read Register	0x0000_00FF
ALIVEGPIOPADOUTRSTREG	088Ch	Alive GPIO PAD Out Reset Register	0x0000_0000
ALIVEGPIOPADOUTSETREG	0890h	Alive GPIO PAD Out Set Register	0x0000_0000
ALIVEGPIOPADOUTREADREG	0894h	Alive GPIO PAD Out Read Register	0x0000_0000
VDDCTRLRSTREG	0898h	VDD Control reset Register	0x0000_0000
VDDCTRLSETREG	089Ch	VDD Control set Register	0x0000_0000
VDDCTRLREADREG	08A0h	VDD Control Read Register	0x0000_03FF
ALIVECLEARWAKEUPSTATUSREGISTER	08A4h	Alive Clear Wakeup Status Register	0x0000_0000
ALIVESLEEPWAKEUPSTATUSREGISTER	08A8h	Alive Sleep Wakeup Status Register	0x0000_0000
ALIVESCRATCHRSTREG1	08ACh	Alive Scratch Reset Register1	0x0000_0000
ALIVESCRATCHRSTREG2	08B8h	Alive Scratch Reset Register2	0x0000_0000
ALIVESCRATCHRSTREG3	08C4h	Alive Scratch Reset Register3	0x0000_0000
ALIVESCRATCHRSTREG4	08D0h	alive scratch reset register4	0x0000_0000
ALIVESCRATCHRSTREG5	08DCh	Alive Scratch Reset Register5	0x0000_0000
ALIVESCRATCHRSTREG6	08E8h	Alive Scratch Reset Register6	0x0000_0000
ALIVESCRATCHRSTREG7	08F4h	Alive Scratch Reset Register7	0x0000_0000
ALIVESCRATCHRSTREG8	0900h	Alive Scratch Reset Register8	0x0000_0000
ALIVESCRATCHSETREG1	08B0h	Alive Scratch Set Register1	0x0000_0000

Register	Offset	Description	Reset Value
ALIVESCRATCHSETREG2	08BCh	Alive Scratch Set Register2	0x0000_0000
ALIVESCRATCHSETREG3	08C8h	Alive Scratch Set Register3	0x0000_0000
ALIVESCRATCHSETREG4	08D4h	Alive Scratch Set Register4	0x0000_0000
ALIVESCRATCHSETREG5	08E0h	Alive Scratch Set Register5	0x0000_0000
ALIVESCRATCHSETREG6	08ECh	Alive Scratch Set Register6	0x0000_0000
ALIVESCRATCHSETREG7	08F8h	Alive Scratch Set Register7	0x0000_0000
ALIVESCRATCHSETREG8	0904h	Alive Scratch Set Register8	0x0000_0000
ALIVESCRATCHREADREG1	08B4h	Alive Scratch Read Register1	0x0000_0000
ALIVESCRATCHREADREG2	08C0h	Alive Scratch Read Register2	0x0000_0000
ALIVESCRATCHREADREG3	08CCh	Alive Scratch Read Register3	0x0000_0000
ALIVESCRATCHREADREG4	08D8h	Alive Scratch Read Register4	0x0000_0000
ALIVESCRATCHREADREG5	08E4h	Alive Scratch Read Register5	0x0000_0000
ALIVESCRATCHREADREG6	08F0h	Alive Scratch Read Register6	0x0000_0000
ALIVESCRATCHREADREG7	08FCh	Alive Scratch Read Register7	0x0000_0000
ALIVESCRATCHREADREG8	0908h	Alive Scratch Read Register8	0x0000_0000
VDDOFFDELAYRSTREGISTER	090Ch	VDD Off Delay Reset Register	0x0000_0000
VDDOFFDELAYSETREGISTER	0910h	VDD Off Delay Set Register	0x0000_0000
VDDOFFDELAYVALUEREGISTER	0914h	VDD Off Delay Value Register	0x0000_0000
VDDOFFDELAYTIMEREGISTER	0918h	VDD Off Delay Time Register	0x0000_0000
ALIVEGPIOINPUTVALUE	091Ch	Alive GPIO Input Value Read Register	0x0000_0000
RSVD	~ 0BFFh	Reserved	-
RTC	0C00h ~ 0CFFh	See RTC section	-
PMUNISOLATE	0D00h	PMU nISOLATE Register	0x0000_0003
PMUNPWRUPPRE	0D04h	PMU nPOWER Up Precharge Register	0x0000_0000
PMUNPWRUP	0D08h	PMU nPOWER Up Register	0x0000_0000
PMUNPWRUPACK	0D0Ch	PMU nPOWER Up ACK Register	0x0000_0000

12.8.1.1 ALIVEPWRGATEREG

- Base Address: C001_0000h
- Address = Base Address + 0800h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	0
NPOWERGATING	[0]	RW	nPowerGating (negative active Power Gating). The default value is 0, disabling writing to Alive Registers, in order to keep the values of Alive Registers when Core Power 1.0V is off. 0 = Disable writing data to Alive Register 1 = Enable writing data to Alive Register	1'b0

12.8.1.2 ALIVEGPIOASYNCDETECTMODERSTREG0

- Base Address: C001_0000h
- Address = Base Address + 0804h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ASyncdetectmoderST0_7	[7]	RW	Alive GPIO7 Low Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetectmoderST0_6	[6]	RW	Alive GPIO6 Low Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetectmoderST0_5	[5]	RW	Alive GPIO5 Low Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetectmoderST0_4	[4]	RW	Alive GPIO4 Low Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetectmoderST0_3	[3]	RW	Alive GPIO3 Low Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetectmoderST0_2	[2]	RW	Alive GPIO2 Low Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetectmoderST0_1	[1]	RW	Alive GPIO1 Low Level Async detect mode Register	1'b0

Name	Bit	Type	Description	Reset Value
			Reset. 0 = None 1 = Reset	
ASyncdetectmoderST0_0	[0]	RW	Alive GPIO0 Low Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.3 ALIVEGPIOASYNCDETECTMODERSTREG1

- Base Address: C001_0000h
- Address = Base Address + 0810h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ASyncdetecTMODERST1_7	[7]	RW	Alive GPIO7 High Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetecTMODERST1_6	[6]	RW	Alive GPIO6 High Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetecTMODERST1_5	[5]	RW	Alive GPIO5 High Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetecTMODERST1_4	[4]	RW	Alive GPIO4 High Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetecTMODERST1_3	[3]	RW	Alive GPIO3 High Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetecTMODERST1_2	[2]	RW	Alive GPIO2 High Level Async detect enable Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetecTMODERST1_1	[1]	RW	Alive GPIO1 High Level Async detect mode Register Reset. 0 = None 1 = Reset	1'b0
ASyncdetecTMODERST1_0	[0]	RW	Alive GPIO0 High Level Async detect mode Register Reset.	1'b0

Name	Bit	Type	Description	Reset Value
			0 = None 1 = Reset	

12.8.1.4 ALIVEGPIOASYNCDETECTMODESETREG0

- Base Address: C001_0000h
- Address = Base Address + 0808h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ASyncdetectMODEset0_7	[7]	RW	Alive GPIO7 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectMODEset0_6	[6]	RW	Alive GPIO6 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectMODEset0_5	[5]	RW	Alive GPIO5 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectMODEset0_4	[4]	RW	Alive GPIO4 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectMODEset0_3	[3]	RW	Alive GPIO3 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectMODEset0_2	[2]	RW	Alive GPIO2 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectMODEset0_1	[1]	RW	Alive GPIO1 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectMODEset0_0	[0]	RW	Alive GPIO0 Low Level Async detect mode Register Set. 0 = None 1 = Set	1'b0

12.8.1.5 ALIVEGPIOASYNCDETECTMODESETREG1

- Base Address: C001_0000h
- Address = Base Address + 0814h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ASyncdetectmodeset1_7	[7]	RW	Alive GPIO7 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectmodeset1_6	[6]	RW	Alive GPIO6 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectmodeset1_5	[5]	RW	Alive GPIO5 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectmodeset1_4	[4]	RW	Alive GPIO4 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectmodeset1_3	[3]	RW	Alive GPIO3 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetecenbset1_2	[2]	RW	Alive GPIO2 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectmodeset1_1	[1]	RW	Alive GPIO1 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0
ASyncdetectmodeset1_0	[0]	RW	Alive GPIO0 High Level Async detect mode Register Set. 0 = None 1 = Set	1'b0

12.8.1.6 ALIVEGPIOLOWASYNCDETECTMODEREADREG

- Base Address: C001_0000h
- Address = Base Address + 080Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpiolowasyncdetectMODE7	[7]	R	Alive GPIO7 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpiolowasyncdetectMODE6	[6]	R	Alive GPIO6 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpiolowasyncdetectMODE5	[5]	R	Alive GPIO5 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpiolowasyncdetectMODE4	[4]	R	Alive GPIO4 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpiolowasyncdetectMODE3	[3]	R	Alive GPIO3 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpiolowasyncdetectMODE2	[2]	R	Alive GPIO2 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpiolowasyncdetectMODE1	[1]	R	Alive GPIO1 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpiolowasyncdetectMODE0	[0]	R	Alive GPIO0 Low level Async detect mode register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIOLOWASYNCDETECTMODE(n) Register operates as follows
It remains as the former state in case of {ASYNCDETECTENBRST0_(n), ASYNCDETECTENBSET0_(n)} = 2'b00
It is set as "1" in case of {ASYNCDETECTENBRST0_(n), ASYNCDETECTENBSET0_(n)} = 2'b01
It is set as "0" in case of {ASYNCDETECTENBRST0_(n), ASYNCDETECTENBSET0_(n)} = 2'b10
It is set as "1" in case of {ASYNCDETECTENBRST0_(n), ASYNCDETECTENBSET0_(n)} = 2'b11

12.8.1.7 ALIVEGPIOHIGHASYNCDETECTMODEREADREG

- Base Address: C001_0000h
- Address = Base Address + 0818h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpiohighasyncdetect Mode7	[7]	R	Alive GPIO7 High level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHighasyncdetect mode6	[6]	R	Alive GPIO6 High level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHighasyncdetect mode5	[5]	R	Alive GPIO5 High level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHighasyncdetect mode4	[4]	R	Alive GPIO4 High level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHighasyncdetect mode3	[3]	R	Alive GPIO3 High level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHighasyncdetect mode2	[2]	R	Alive GPIO2 High level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHighasyncdetect mode1	[1]	R	Alive GPIO1 High level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHighasyncdetect mode0	[0]	R	Alive GPIO0 High level Async detect mode register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIOHIGHASYNCDETECTMODE(n) Register operates as follows
It remains as the former state in case of {ASYNCDETECTMODERST1_(n), ASYNCDETECTMODESET1_(n)} = 2'b00
It is set as "1" in case of {ASYNCDETECTMODERST1_(n), ASYNCDETECTMODESET1_(n)} = 2'b01
It is set as "0" in case of {ASYNCDETECTMODERST1_(n), ASYNCDETECTMODESET1_(n)} = 2'b10
It is set as "1" in case of {ASYNCDETECTMODERST1_(n), ASYNCDETECTMODESET1_(n)} = 2'b11

12.8.1.8 ALIVEGPIODETECTMODERSTREG0

- Base Address: C001_0000h
- Address = Base Address + 081Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTMODERST0_7	[7]	RW	Alive GPIO7 Falling Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST0_6	[6]	RW	Alive GPIO6 Falling Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST0_5	[5]	RW	Alive GPIO5 Falling Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST0_4	[4]	RW	Alive GPIO4 Falling Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST0_3	[3]	RW	Alive GPIO3 Falling Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST0_2	[2]	RW	Alive GPIO2 Falling Edge detect enable Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST0_1	[1]	RW	Alive GPIO1 Falling Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST0_0	[0]	RW	Alive GPIO0 Falling Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.9 ALIVEGPIODETECTMODERSTREG1

- Base Address: C001_0000h
- Address = Base Address + 0828h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTMODERST1_7	[7]	RW	Alive GPIO7 Rising Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST1_6	[6]	RW	Alive GPIO6 Rising Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST1_5	[5]	RW	Alive GPIO5 Rising Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST1_4	[4]	RW	Alive GPIO4 Rising Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST1_3	[3]	RW	Alive GPIO3 Rising Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST1_2	[2]	RW	Alive GPIO2 Rising Edge detect enable Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST1_1	[1]	RW	Alive GPIO1 Rising Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST1_0	[0]	RW	Alive GPIO0 Rising Edge detect mode Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.10 ALIVEGPIODETECTMODERSTREG2

- Base Address: C001_0000h
- Address = Base Address + 0834h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTMODERST2_7	[7]	RW	Alive GPIO7 Low Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST2_6	[6]	RW	Alive GPIO6 Low Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST2_5	[5]	RW	Alive GPIO5 Low Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST2_4	[4]	RW	Alive GPIO4 Low Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST2_3	[3]	RW	Alive GPIO3 Low Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST2_2	[2]	RW	Alive GPIO2 Low Level detect enable Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST2_1	[1]	RW	Alive GPIO1 Low Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST2_0	[0]	RW	Alive GPIO0 Low Level detect mode Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.11 ALIVEGPIODETECTMODERSTREG3

- Base Address: C001_0000h
- Address = Base Address + 0840h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTMODERST3_7	[7]	RW	Alive GPIO7 High Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST3_6	[6]	RW	Alive GPIO6 High Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST3_5	[5]	RW	Alive GPIO5 High Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST3_4	[4]	RW	Alive GPIO4 High Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST3_3	[3]	RW	Alive GPIO3 High Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST3_2	[2]	RW	Alive GPIO2 High Level detect enable Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST3_1	[1]	RW	Alive GPIO1 High Level detect mode Register Reset. 0 = None 1 = Reset	1'b0
detecTMODERST3_0	[0]	RW	Alive GPIO0 High Level detect mode Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.12 ALIVEGPIODETECTMODESETREG0

- Base Address: C001_0000h
- Address = Base Address + 0820h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detectmodeset0_7	[7]	RW	Alive GPIO7 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detectmodeset0_6	[6]	RW	Alive GPIO6 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detectmodeset0_5	[5]	RW	Alive GPIO5 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detectmodeset0_4	[4]	RW	Alive GPIO4 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detectmodeset0_3	[3]	RW	Alive GPIO3 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detectmodeset0_2	[2]	RW	Alive GPIO2 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detectmodeset0_1	[1]	RW	Alive GPIO1 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detectmodeset0_0	[0]	RW	Alive GPIO0 Falling Edge detect mode Register Set. 0 = None 1 = Set	1'b0

12.8.1.13 ALIVEGPIODETECTMODESETREG1

- Base Address: C001_0000h
- Address = Base Address + 082Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTMODESET1_7	[7]	RW	Alive GPIO7 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET1_6	[6]	RW	Alive GPIO6 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET1_5	[5]	RW	Alive GPIO5 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET1_4	[4]	RW	Alive GPIO4 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET1_3	[3]	RW	Alive GPIO3 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET1_2	[2]	RW	Alive GPIO2 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET1_1	[1]	RW	Alive GPIO1 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET1_0	[0]	RW	Alive GPIO0 Rising Edge detect mode Register Set. 0 = None 1 = Set	1'b0

12.8.1.14 ALIVEGPIODETECTMODESETREG2

- Base Address: C001_0000h
- Address = Base Address + 0838h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTMODESET2_7	[7]	RW	Alive GPIO7 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET2_6	[6]	RW	Alive GPIO6 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET2_5	[5]	RW	Alive GPIO5 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET2_4	[4]	RW	Alive GPIO4 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET2_3	[3]	RW	Alive GPIO3 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET2_2	[2]	RW	Alive GPIO2 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET2_1	[1]	RW	Alive GPIO1 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET2_0	[0]	RW	Alive GPIO0 Low Level detect mode Register Set. 0 = None 1 = Set	1'b0

12.8.1.15 ALIVEGPIODETECTMODESETREG3

- Base Address: C001_0000h
- Address = Base Address + 0844h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTMODESET3_7	[7]	RW	Alive GPIO7 High Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET3_6	[6]	RW	Alive GPIO6 High Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET3_5	[5]	RW	Alive GPIO5 High Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET3_4	[4]	RW	Alive GPIO4 High Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET3_3	[3]	RW	Alive GPIO3 High Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET3_2	[2]	RW	Alive GPIO2 High Level detect mode Register Set. 0 = None 1 = Set 0 : none 1: Set	1'b0
detecTMODESET3_1	[1]	RW	Alive GPIO1 High Level detect mode Register Set. 0 = None 1 = Set	1'b0
detecTMODESET3_0	[0]	RW	Alive GPIO0 High Level detect mode Register Set. 0 = None 1 = Set	1'b0

12.8.1.16 ALIVEGPIOFALLDETECTMODEREADREG

- Base Address: C001_0000h
- Address = Base Address + 0824h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioFALLdetectMode7	[7]	R	Alive GPIO7 Falling Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioFALLdetectMode6	[6]	R	Alive GPIO6 Falling Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioFALLdetectMode5	[5]	R	Alive GPIO5 Falling Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioFALLdetectMode4	[4]	R	Alive GPIO4 Falling Edge Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioFALLdetectMode3	[3]	R	Alive GPIO3 Falling Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioFALLdetectMode2	[2]	R	Alive GPIO2 Falling Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioFALLdetectMode1	[1]	R	Alive GPIO1 Falling Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioFALLdetectMode0	[0]	R	Alive GPIO0 Falling Edge detect mode register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIOFALLDETECTMODE(n) Register operates as follows
It remains as the former state in case of {DETECTMODERST0_(n), DETECTMODESET0_(n)} = 2'b00
It is set as "1" in case of {DETECTMODERST0_(n), DETECTMODESET0_(n)} = 2'b01
It is set as "0" in case of {DETECTMODERST0_(n), DETECTMODESET0_(n)} = 2'b10
It is set as "1" in case of {DETECTMODERST0_(n), DETECTMODESET0_(n)} = 2'b11

12.8.1.17 ALIVEGPIORISEDETECTMODEREADREG

- Base Address: C001_0000h
- Address = Base Address + 8030h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioRISEdetectMode7	[7]	R	Alive GPIO7 Rising Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioRISEdetectMode6	[6]	R	Alive GPIO6 Rising Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioRISEdetectMode5	[5]	R	Alive GPIO5 Rising Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioRISEdetectMode4	[4]	R	Alive GPIO4 Rising Edge Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioRISEdetectMode3	[3]	R	Alive GPIO3 Rising Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioRISEdetectMode2	[2]	R	Alive GPIO2 Rising Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioRISEdetectMode1	[1]	R	Alive GPIO1 Rising Edge detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioRISEdetectMode0	[0]	R	Alive GPIO0 Rising Edge detect mode register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIORISEDETECTMODE(n) Register operates as follows
It remains as the former state in case of {DETECTMODERST1_(n), DETECTMODESET1_(n)} = 2'b00
It is set as "1" in case of {DETECTMODERST1_(n), DETECTMODESET1_(n)} = 2'b01
It is set as "0" in case of {DETECTMODERST1_(n), DETECTMODESET1_(n)} = 2'b10
It is set as "1" in case of {DETECTMODERST1_(n), DETECTMODESET1_(n)} = 2'b11

12.8.1.18 ALIVEGPIOLOWDETECTMODEREADREG

- Base Address: C001_0000h
- Address = Base Address + 083Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioLOWdetectMode7	[7]	R	Alive GPIO7 Low Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioLOWdetectMode6	[6]	R	Alive GPIO6 Low Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioLOWdetectMode5	[5]	R	Alive GPIO5 Low Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioLOWdetectMode4	[4]	R	Alive GPIO4 Low Level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioLOWdetectMode3	[3]	R	Alive GPIO3 Low Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioLOWdetectMode2	[2]	R	Alive GPIO2 Low Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioLOWdetectMode1	[1]	R	Alive GPIO1 Low Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioLOWdetectMode0	[0]	R	Alive GPIO0 Low Level detect mode register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIOLOWDETECTMODE(n) Register operates as follows
It remains as the former state in case of {DETECTMODERST2_(n), DETECTMODESET2_(n)} = 2'b00
It is set as "1" in case of {DETECTMODERST2_(n), DETECTMODESET2_(n)} = 2'b01
It is set as "0" in case of {DETECTMODERST2_(n), DETECTMODESET2_(n)} = 2'b10
It is set as "1" in case of {DETECTMODERST2_(n), DETECTMODESET2_(n)} = 2'b11

12.8.1.19 ALIVEGPIOHIGHDETECTMODEREADREG

- Base Address: C001_0000h
- Address = Base Address + 0848h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioHIGHdetectMode7	[7]	R	Alive GPIO7 High Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHIGHdetectMode6	[6]	R	Alive GPIO6 High Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHIGHdetectMode5	[5]	R	Alive GPIO5 High Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHIGHdetectMode4	[4]	R	Alive GPIO4 High Level Async detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHIGHdetectMode3	[3]	R	Alive GPIO3 High Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHIGHdetectMode2	[2]	R	Alive GPIO2 High Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHIGHdetectMode1	[1]	R	Alive GPIO1 High Level detect mode register 0 = Disable 1 = Enable	1'b0
alivegpioHIGHdetectMode0	[0]	R	Alive GPIO0 High Level detect mode register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIOHIGHTDETECTMODE(n) Register operates as follows
It remains as the former state in case of {DETECTMODERST3_(n), DETECTMODESET3_(n)} = 2'b00
It is set as "1" in case of {DETECTMODERST3_(n), DETECTMODESET3_(n)} = 2'b01
It is set as "0" in case of {DETECTMODERST3_(n), DETECTMODESET3_(n)} = 2'b10
It is set as "1" in case of {DETECTMODERST3_(n), DETECTMODESET3_(n)} = 2'b11

12.8.1.20 ALIVEGPIODETECTENBRSTREG

- Base Address: C001_0000h
- Address = Base Address + 084Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTENBRST7	[7]	RW	Alive GPIO7 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0
detecTENBRST6	[6]	RW	Alive GPIO6 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0
detecTENBRST5	[5]	RW	Alive GPIO5 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0
detecTENBRST4	[4]	RW	Alive GPIO4 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0
detecTENBRST3	[3]	RW	Alive GPIO3 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0
detecTENBRST2	[2]	RW	Alive GPIO2 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0
detecTENBRST1	[1]	RW	Alive GPIO1 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0
detecTENBRST0	[0]	RW	Alive GPIO0 Detect Enable Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.21 ALIVEGPIODETECTENBSETREG

- Base Address: C001_0000h
- Address = Base Address + 0850h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
detecTENBSET7	[7]	RW	Alive GPIO7 Detect Enable Register Set. 0 = None 1 = Set	1'b0
detecTenbSET6	[6]	RW	Alive GPIO6 Detect Enable Register Set. 0 = None 1 = Set	1'b0
detecTenbSET5	[5]	RW	Alive GPIO5 Detect Enable Register Set. 0 = None 1 = Set	1'b0
detecTenbSET4	[4]	RW	Alive GPIO4 Detect Enable Register Set. 0 = None 1 = Set	1'b0
detecTenbSET3	[3]	RW	Alive GPIO3 Detect Enable Register Set. 0 = None 1 = Set	1'b0
detecTenbSET2	[2]	RW	Alive GPIO2 Detect Enable Register Set. 0 = None 1 = Set	1'b0
detecTenbSET1	[1]	RW	Alive GPIO1 Detect Enable Register Set. 0 = None 1 = Set	1'b0
detecTenbSET0	[0]	RW	Alive GPIO0 Detect Enable Register Set. 0 = None 1 = Set	1'b0

12.8.1.22 ALIVEGPIODETECTENBREADREG

- Base Address: C001_0000h
- Address = Base Address + 0854h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpiodetectENB7	[7]	R	Alive GPIO7 Detect Enable register 0 = Disable 1 = Enable	1'b0
alivegpiodetectENB6	[6]	R	Alive GPIO6 Detect Enable register 0 = Disable 1 = Enable	1'b0
alivegpiodetectENB5	[5]	R	Alive GPIO5 Detect Enable register 0 = Disable 1 = Enable	1'b0
alivegpiodetectENB4	[4]	R	Alive GPIO4 Detect Enable register 0 = Disable 1 = Enable	1'b0
alivegpiodetectENB3	[3]	R	Alive GPIO3 Detect Enable register 0 = Disable 1 = Enable	1'b0
alivegpiodetectENB2	[2]	R	Alive GPIO2 Detect Enable register 0 = Disable 1 = Enable	1'b0
alivegpiodetectENB1	[1]	R	Alive GPIO1 Detect Enable register 0 = Disable 1 = Enable	1'b0
alivegpiodetectENB0	[0]	R	Alive GPIO0 Detect Enable register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIODETECTENB (n) Register operates as follows
It remains as the former state in case of {DETECTENBRST(n), DETECTENBSET(n)} = 2'b00
It is set as "1" in case of {DETECTENBRST(n), DETECTENBSET(n)} = 2'b01
It is set as "0" in case of {DETECTENBRST(n), DETECTENBSET(n)} = 2'b10
It is set as "1" in case of {DETECTENBRST(n), DETECTENBSET(n)} = 2'b11

12.8.1.23 ALIVEGPIOINTENBRSTREG

- Base Address: C001_0000h
- Address = Base Address + 0858h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOINTENBRST7	[7]	RW	Alive GPIO7 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOINTENBRST6	[6]	RW	Alive GPIO6 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOINTENBRST5	[5]	RW	Alive GPIO5 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOINTENBRST4	[4]	RW	Alive GPIO4 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOINTENBRST3	[3]	RW	Alive GPIO3 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOINTENBRST2	[2]	RW	Alive GPIO2 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOINTENBRST1	[1]	RW	Alive GPIO1 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOINTENBRST0	[0]	RW	Alive GPIO0 Interrupt Enable Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.24 ALIVEGPIODETECTENABLESETREG

- Base Address: C001_0000h
- Address = Base Address + 085Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOINTENBSET7	[7]	RW	Alive GPIO7 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOINTENBSET6	[6]	RW	Alive GPIO6 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOINTENBSET5	[5]	RW	Alive GPIO5 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOINTENBSET4	[4]	RW	Alive GPIO4 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOINTENBSET3	[3]	RW	Alive GPIO3 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOINTENBSET2	[2]	RW	Alive GPIO2 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOINTENBSET1	[1]	RW	Alive GPIO1 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOINTENBSET0	[0]	RW	Alive GPIO0 Interrupt Enable Register Set. 0 = None 1 = Set	1'b0

12.8.1.25 ALIVEGPIOINTENBREADREG

- Base Address: C001_0000h
- Address = Base Address + 0860h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioINTENB7	[7]	R	Alive GPIO7 Interrupt Enable register 0 = Disable 1 = Enable	1'b0
alivegpioINTENB6	[6]	R	Alive GPIO6 Interrupt Enable register 0 = Disable 1 = Enable	1'b0
alivegpioINTENB5	[5]	R	Alive GPIO5 Interrupt Enable register 0 = Disable 1 = Enable	1'b0
alivegpioINTENB4	[4]	R	Alive GPIO4 Interrupt Enable register 0 = Disable 1 = Enable	1'b0
alivegpioINTENB3	[3]	R	Alive GPIO3 Interrupt Enable register 0 = Disable 1 = Enable	1'b0
alivegpioINTENB2	[2]	R	Alive GPIO2 Interrupt Enable register 0 = Disable 1 = Enable	1'b0
alivegpioINTENB1	[1]	R	Alive GPIO1 Interrupt Enable register 0 = Disable 1 = Enable	1'b0
alivegpioINTENB0	[0]	R	Alive GPIO0 Interrupt Enable register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIOINTENB (n) Register operates as follows
It remains as the former state in case of {ALIVEGPIOENBRST(n), ALIVEGPIOENBSET(n)} = 2'b00
It is set as "1" in case of {ALIVEGPIOENBRST(n), ALIVEGPIOENBSET (n)} = 2'b01
It is set as "0" in case of {ALIVEGPIOENBRST(n), ALIVEGPIOENBSET (n)} = 2'b10
It is set as "1" in case of {ALIVEGPIOENBRST(n), ALIVEGPIOENBSET (n)} = 2'b11

12.8.1.26 ALIVEGPIODETECTPENDREG

- Base Address: C001_0000h
- Address = Base Address + 0864h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioDETECTPEND7	[7]	R	Alive GPIO7 Detect Pending Read 0 = None 1 = Interrupt Pending Write 0 = None 1 = Clear	1'b0
alivegpioDETECTPEND6	[6]	R	Alive GPIO6 Detect Pending Read 0 = None 1 = Interrupt Pending Write 0 = None 1 = Clear	1'b0
alivegpioDETECTPEND5	[5]	R	Alive GPIO5 Detect Pending Read 0 = None 1 = Interrupt Pending Write 0 = None 1 = Clear	1'b0
alivegpioDETECTPEND4	[4]	R	Alive GPIO4 Detect Pending Read 0 = None 1 = Interrupt Pending Write 0 = None 1 = Clear	1'b0
alivegpioDETECTPEND3	[3]	R	Alive GPIO3 Detect Pending Read 0 = None 1 = Interrupt Pending Write 0 = None 1 = Clear	1'b0
alivegpioDETECTPEND2	[2]	R	Alive GPIO2 Detect Pending Read 0 = None 1 = Interrupt Pending	1'b0

Name	Bit	Type	Description	Reset Value
			Write 0 = None 1 = Clear	
alivegpioDETECTPEND1	[1]	R	Alive GPIO1 Detect Pending Read 0 = None 1 = Interrupt Pending Write 0 = None 1 = Clear	1'b0
alivegpioDETECTPEND0	[0]	R	Alive GPIO0 Detect Pending Read 0 = None 1 = Interrupt Pending Write 0 = None 1 = Clear	1'b0

12.8.1.27 ALIVESCRATCHRSTREG

- Base Address: C001_0000h
- Address = Base Address + 0868h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST drives Scratch Register's reset pin.	32'b0

12.8.1.28 ALIVESCRATCHSETREG

- Base Address: C001_0000h
- Address = Base Address + 086Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET drives Scratch Register's set pin	32'b0

12.8.1.29 ALIVESCRATCHREADREG

- Base Address: C001_0000h
- Address = Base Address + 0870h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.30 ALIVEGPIOPADOUTENBRSTREG

- Base Address: C001_0000h
- Address = Base Address + 0874h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOPADOUTENBRST7	[7]	RW	Alive GPIO7 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTENBRST6	[6]	RW	Alive GPIO6 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTENBRST5	[5]	RW	Alive GPIO5 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTENBRST4	[4]	RW	Alive GPIO4 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTENBRST3	[3]	RW	Alive GPIO3 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTENBRST2	[2]	RW	Alive GPIO2 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTENBRST1	[1]	RW	Alive GPIO1 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTENBRST0	[0]	RW	Alive GPIO0 PAD Out Enable Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.31 ALIVEGPIOPADOUTENBSETREG

- Base Address: C001_0000h
- Address = Base Address + 0878h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOPADOUTENBSET7	[7]	RW	Alive GPIO7 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTENBSET6	[6]	RW	Alive GPIO6 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTENBSET5	[5]	RW	Alive GPIO5 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTENBSET4	[4]	RW	Alive GPIO4 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTENBSET3	[3]	RW	Alive GPIO3 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTENBSET2	[2]	RW	Alive GPIO2 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTENBSET1	[1]	RW	Alive GPIO1 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTENBSET0	[0]	RW	Alive GPIO0 PAD Out Enable Register Set. 0 = None 1 = Set	1'b0

12.8.1.32 ALIVEGPIOPADOUTENBREADREG

- Base Address: C001_0000h
- Address = Base Address + 087Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioPADOUTENB7	[7]	R	Alive GPIO7 PAD Out Enable register 0 = Disable 1 = Enable	1'b0
alivegpioPADOUTENB6	[6]	R	Alive GPIO6 PAD Out Enable register 0 = Disable 1 = Enable	1'b0
alivegpioPADOUTENB5	[5]	R	Alive GPIO5 PAD Out Enable register 0 = Disable 1 = Enable	1'b0
alivegpioPADOUTENB4	[4]	R	Alive GPIO4 PAD Out Enable register 0 = Disable 1 = Enable	1'b0
alivegpioPADOUTENB3	[3]	R	Alive GPIO3 PAD Out Enable register 0 = Disable 1 = Enable	1'b0
alivegpioPADOUTENB2	[2]	R	Alive GPIO2 PAD Out Enable register 0 = Disable 1 = Enable	1'b0
alivegpioPADOUTENB1	[1]	R	Alive GPIO1 PAD Out Enable register 0 = Disable 1 = Enable	1'b0
alivegpioPADOUTENB0	[0]	R	Alive GPIO0 PAD Out Enable register 0 = Disable 1 = Enable	1'b0

NOTE: ALIVEGPIOPADOUTENB(n) Register operates as follows
It remains as the former state in case of {ALIVEGPIOPADOUTENBRST(n), ALIVEGPIOPADOUTENBSET(n)} = 2'b00
It is set as "1" in case of {ALIVEGPIOPADOUTENBRST(n), ALIVEGPIOPADOUTENBSET(n)} = 2'b01
It is set as "0" in case of {ALIVEGPIOPADOUTENBRST(n), ALIVEGPIOPADOUTENBSET(n)} = 2'b10
It is set as "1" in case of {ALIVEGPIOPADOUTENBRST(n), ALIVEGPIOPADOUTENBSET(n)} = 2'b11

12.8.1.33 ALIVEGPIOPADPULLUPRSTREG

- Base Address: C001_0000h
- Address = Base Address + 0880h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOPADPULLUPRST7	[7]	RW	Alive GPIO7 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADPULLUPRST6	[6]	RW	Alive GPIO6 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADPULLUPRST5	[5]	RW	Alive GPIO5 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADPULLUPRST4	[4]	RW	Alive GPIO4 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADPULLUPRST3	[3]	RW	Alive GPIO3 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADPULLUPRST2	[2]	RW	Alive GPIO2 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADPULLUPRST1	[1]	RW	Alive GPIO1 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADPULLUPRST0	[0]	RW	Alive GPIO0 PAD Pullup Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.34 ALIVEGPIOPADPULLUPSETREG

- Base Address: C001_0000h
- Address = Base Address + 0884h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOPADPULLUPSET7	[7]	RW	Alive GPIO7 PAD Pullup Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADPULLUPSET6	[6]	RW	Alive GPIO6 PAD Pullup Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADPULLUPSET5	[5]	RW	Alive GPIO5 PAD Pullup Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADPULLUPSET4	[4]	RW	Alive GPIO4 PAD Pullup Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADPULLUPSET3	[3]	RW	Alive GPIO3 PAD Pullup Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADPULLUPSET2	[2]	RW	Alive GPIO2 PAD Pullup Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADPULLUPSET1	[1]	RW	Alive GPIO1 PAD Pullup Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADPULLUPSET0	[0]	RW	Alive GPIO0 PAD Pullup Register Set. 0 = None 1 = Set	1'b0

12.8.1.35 ALIVEGPIOPADPULLUPREADREG

- Base Address: C001_0000h
- Address = Base Address + 0888h, Reset Value = 0x0000_00FF

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioPADPULLUP7	[7]	R	Alive GPIO7 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1
alivegpioPADPULLUP6	[6]	R	Alive GPIO6 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1
alivegpioPADPULLUP5	[5]	R	Alive GPIO5 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1
alivegpioPADPULLUP4	[4]	R	Alive GPIO4 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1
alivegpioPADPULLUP3	[3]	R	Alive GPIO3 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1
alivegpioPADPULLUP2	[2]	R	Alive GPIO2 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1
alivegpioPADPULLUP1	[1]	R	Alive GPIO1 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1
alivegpioPADPULLUP0	[0]	R	Alive GPIO0 PAD Pullup register 0 = Pull-down 1 = Pull-up	1'b1

NOTE: ALIVEGPIOPADPULLUP (n) Register operates as follows
It remains as the former state in case of {ALIVEGPIOPADPULLUPRST(n), ALIVEGPIOPADPULLUPSET(n)} = 2'b00
It is set as "1" in case of {ALIVEGPIOPADOPULLUPRST(n), ALIVEGPIOPADPULLUPSET(n)} = 2'b01
It is set as "0" in case of {ALIVEGPIOPADOPULLUPRST(n), ALIVEGPIOPADPULLUPSET(n)} = 2'b10
It is set as "1" in case of {ALIVEGPIOPADOPULLUPRST(n), ALIVEGPIOPADPULLUPSET(n)} = 2'b11

12.8.1.36 ALIVEGPIOPADOUTRSTREG

- Base Address: C001_0000h
- Address = Base Address + 088Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOPADOUTRST7	[7]	RW	Alive GPIO7 PAD Out Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTRST6	[6]	RW	Alive GPIO6 PAD Out Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTRST5	[5]	RW	Alive GPIO5 PAD Out Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTRST4	[4]	RW	Alive GPIO4 PAD Out Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTRST3	[3]	RW	Alive GPIO3 PAD Out Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTRST2	[2]	RW	Alive GPIO2 PAD Out Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTRST1	[1]	RW	Alive GPIO1 PAD Out Register Reset. 0 = None 1 = Reset	1'b0
ALIVEGPIOPADOUTRST0	[0]	RW	Alive GPIO0 PAD Out Register Reset. 0 = None 1 = Reset	1'b0

12.8.1.37 ALIVEGPIOPADOUTSETREG

- Base Address: C001_0000h
- Address = Base Address + 0890h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
ALIVEGPIOPADOUTSET7	[7]	RW	Alive GPIO7 PAD Out Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTSET6	[6]	RW	Alive GPIO6 PAD Out Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTSET5	[5]	RW	Alive GPIO5 PAD Out Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTSET4	[4]	RW	Alive GPIO4 PAD Out Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTSET3	[3]	RW	Alive GPIO3 PAD Out Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTSET2	[2]	RW	Alive GPIO2 PAD Out Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTSET1	[1]	RW	Alive GPIO1 PAD Out Register Set. 0 = None 1 = Set	1'b0
ALIVEGPIOPADOUTSET0	[0]	RW	Alive GPIO0 PAD Out Register Set. 0 = None 1 = Set	1'b0

12.8.1.38 ALIVEGPIOPADOUTREADREG

- Base Address: C001_0000h
- Address = Base Address + 0894h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0
alivegpioPADOUT7	[7]	R	Alive GPIO7 PAD Out register	1'b0
alivegpioPADOUT6	[6]	R	Alive GPIO6 PAD Out register	1'b0
alivegpioPADOUT5	[5]	R	Alive GPIO5 PAD Out register	1'b0
alivegpioPADOUT4	[4]	R	Alive GPIO4 PAD Out register	1'b0
alivegpioPADOUT3	[3]	R	Alive GPIO3 PAD Out register	1'b0
alivegpioPADOUT2	[2]	R	Alive GPIO2 PAD Out register	1'b0
alivegpioPADOUT1	[1]	R	Alive GPIO1 PAD Out register	1'b0
alivegpioPADOUT0	[0]	R	Alive GPIO0 PAD Out register	1'b0

NOTE: ALIVEGPIOPADOUT(n) Register operates as follows
It remains as the former state in case of {ALIVEGPIOPADOUTRST(n), ALIVEGPIOPADOUTSET(n)} = 2'b00
It is set as "1" in case of {ALIVEGPIOPADOUTRST(n), ALIVEGPIOPADOUTSET(n)} = 2'b01
It is set as "0" in case of {ALIVEGPIOPADOUTRST(n), ALIVEGPIOPADOUTSET(n)} = 2'b10
It is set as "1" in case of {ALIVEGPIOPADOUTRST(n), ALIVEGPIOPADOUTSET(n)} = 2'b11

12.8.1.39 VDDCTRLRSTREG

- Base Address: C001_0000h
- Address = Base Address + 0898h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	–	Reserved	0
padholdENBrst3	[9]	RW	nPADHOLDENB3 Reset This register is not used in current version. Write to this register does not affect anything. 0 = None 1 = Set	1'b0
padholdENBrst2	[8]	RW	nPADHOLDENB2 Reset 0 = None 1 = Set	1'b0
padholdENBrst1	[7]	RW	nPADHOLDENB1 Reset 0 = None 1 = Set	1'b0
padholdENBrst0	[6]	RW	nPADHOLDENB0 Reset 0 = None 1 = Set	1'b0
padholdrst3	[5]	RW	nPADHOLD3 Reset This register is not used in current version. Write to this register does not affect anything. 0 = None 1 = Set	1'b0
padholdrst2	[4]	RW	nPADHOLD2 Reset 0 = None 1 = Set	1'b0
padholdrst1	[3]	RW	nPADHOLD1 Reset 0 = None 1 = Set	1'b0
padholdRST0	[2]	RW	nPADHOLD0 Reset 0 = None 1 = Set	1'b0
vddPWRONRST_DDR	[1]	RW	DRAM VDD Power ON Reset 0 = None 1 = Set	1'b0
vddPWRONRST	[0]	RW	Core VDD Power ON Reset 0 = None 1 = Set	1'b0

12.8.1.40 VDDCTRLSETREG

- Base Address: C001_0000h
- Address = Base Address + 089Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	–	Reserved	0
padholdENBset3	[9]	RW	nPADHOLDENB3 Set This register is not used in current version. Write to this register does not affect anything. 0 = None 1 = Set	1'b0
padholdENBset2	[8]	RW	nPADHOLDENB2 Set 0 = None 1 = Set	1'b0
padholdENBset1	[7]	RW	nPADHOLDENB1 Set 0 = None 1 = Set	1'b0
padholdENBset0	[6]	RW	nPADHOLDENB0 Set 0 = None 1 = Set	1'b0
padholdset3	[5]	RW	nPADHOLD3 Set This register is not used in current version. Write to this register does not affect anything. 0 = None 1 = Set	1'b0
padholdset2	[4]	RW	nPADHOLD2 Set 0 = None 1 = Set	1'b0
padholdset1	[3]	RW	nPADHOLD1 Set 0 = None 1 = Set	1'b0
padholdset0	[2]	RW	nPADHOLD0 Set 0 = None 1 = Set	1'b0
vddPWRonset_DDr	[1]	RW	DRAM VDD Power ON Set 0 = None 1 = Set	1'b0
vddpwronset	[0]	RW	Core VDD Power ON Set 0 = None 1 = Set	1'b0

12.8.1.41 VDDCTRLREADREG

- Base Address: C001_0000h
- Address = Base Address + 08A0h, Reset Value = 0x0000_03FF

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	0
VDDPWRTOGGLE	[10]	R	Read VDDPWRTOGGLE PAD status 0 = User does not pushed VDDPWRTOGGLE PAD 1 = User pushed VDDPWRTOGGLE PAD	-
npadholdENB3	[9]	R	Read nPADHOLDENB3 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
npadholdENB2	[8]	R	Read nPADHOLDENB2 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
npadholdENB1	[7]	R	Read nPADHOLDENB1 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
npadholdENB0	[6]	R	Read nPADHOLDENB0 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
npadhold2	[5]	R	Read nPADHOLD3 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
npadhold2	[4]	R	Read nPADHOLD2 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
npadhold1	[3]	R	Read nPADHOLD1 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
npadhold0	[2]	R	Read nPADHOLD0 Register 0 = Pad Retention Enable 1 = Pad Retention Disable	1'b1
vddpwron_ddr	[1]	R	Read DRAM Vdd Power On Register 0 = DRAM Power Off 1 = CORE DRAM On	1'b1
vddpwron	[0]	R	Read CORE Vdd Power On Register 0 = CORE Power Off 1 = CORE Power On	1'b1

NOTE:

1. Each bit of VDDCTRLREADREG is set or reset by each bit of VDDCTRLSETREG/VDDCTRLRSTREG
2. The Pad Retention of nPadHod and nPadHoldEnb operate as follows.
   Pad Retention Disable if nPadHod == "1", nPadHoldEnb == "1" when Core Power turns off
   Pad Retention Disable if nPadHod == "0", nPadHoldEnb == "1" when Core Power turns off
   Pad Retention Enable if nPadHod == "1", nPadHoldEnb == "0" when Core Power turns off
   Pad Retention Enable if nPadHod == "0", nPadHoldEnb == "0" when Core Power turns off
   Pad Retention Disable if nPadHod == "1", nPadHoldEnb == "1" when Core Power turns on
   Pad Retention Disable if nPadHod == "0", nPadHoldEnb == "1" when Core Power turns on
   Pad Retention Disable if nPadHod == "1", nPadHoldEnb == "0" when Core Power turns on
   Pad Retention Enable if nPadHod == "0", nPadHoldEnb == "0" when Core Power turns on

12.8.1.42 ALIVECLEARWAKEUPSTATUSREGISTER

- Base Address: C001_0000h
- Address = Base Address + 08A4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	R	reserved	31'h0
CLRWAKEUP	[0]	W	Clear is wakeup status register 0 = None 1 = Clear	1'b0

12.8.1.43 ALIVESLEEPWAKEUPSTATUSREGISTER

- Base Address: C001_0000h
- Address = Base Address + 08A8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	R	reserved	22'b0
alivegpio7	[9]	R	0 = none 1 = wkeup is ALIVEGPIO[7]	1'b0
alivegpio6	[8]	R	0 = none 1 = wkeup is ALIVEGPIO[6]	1'b0
alivegpio5	[7]	R	0 = none 1 = wkeup is ALIVEGPIO[5]	1'b0
alivegpio4	[6]	R	0 = none 1 = wkeup is ALIVEGPIO[4]	1'b0
alivegpio3	[5]	R	0 = none 1 = wkeup is ALIVEGPIO[3]	1'b0
alivegpio2	[4]	R	0 = none 1 = wkeup is ALIVEGPIO[2]	1'b0
alivegpio1	[3]	R	0 = none 1 = wkeup is ALIVEGPIO[1]	1'b0
alivegpio0	[2]	R	0 = none 1 = wkeup is ALIVEGPIO[0]	1'b0
rtcinterrupt	[1]	R	0 = none 1 = wkeup is rtc interrupt	1'b0
nVDDpwrtoggle	[0]	R	0 = none 1 = wkeup is vddpwrtoggle	1'b0

12.8.1.44 ALIVESCRATCHRSTREG1

- Base Address: C001_0000h
- Address = Base Address + 08ACh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST1	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST1 drives Scratch Register's reset pin.	32'b0

12.8.1.45 ALIVESCRATCHRSTREG2

- Base Address: C001_0000h
- Address = Base Address + 08B8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST2	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST2 drives Scratch Register's reset pin.	32'b0

12.8.1.46 ALIVESCRATCHRSTREG3

- Base Address: C001_0000h
- Address = Base Address + 08C4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST3	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST3 drives Scratch Register's reset pin.	32'b0

12.8.1.47 ALIVESCRATCHRSTREG4

- Base Address: C001_0000h
- Address = Base Address + 08D0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST4	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST4 drives Scratch Register's reset pin.	32'b0

12.8.1.48 ALIVESCRATCHRSTREG5

- Base Address: C001_0000h
- Address = Base Address + 08DCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST5	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST5 drives Scratch Register's reset pin.	32'b0

12.8.1.49 ALIVESCRATCHRSTREG6

- Base Address: C001_0000h
- Address = Base Address + 08E8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST6	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST6 drives Scratch Register's reset pin.	32'b0

12.8.1.50 ALIVESCRATCHRSTREG7

- Base Address: C001_0000h
- Address = Base Address + 08F4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST7	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST7 drives Scratch Register's reset pin.	32'b0

12.8.1.51 ALIVESCRATCHRSTREG8

- Base Address: C001_0000h
- Address = Base Address + 0900h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHRST8	[31:0]	RW	Reset Alive Scratch Register Each bit of ALIVESCRATCHRST3 drives Scratch Register's reset pin.	32'b0

12.8.1.52 ALIVESCRATCHSETREG1

- Base Address: C001_0000h
- Address = Base Address + 08B0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET1	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET1 drives Scratch Register's set pin.	32'b0

12.8.1.53 ALIVESCRATCHSETREG2

- Base Address: C001_0000h
- Address = Base Address + 08BCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET2	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET2 drives Scratch Register's set pin.	32'b0

12.8.1.54 ALIVESCRATCHSETREG3

- Base Address: C001_0000h
- Address = Base Address + 08C8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET3	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET3 drives Scratch Register's set pin.	32'b0

12.8.1.55 ALIVESCRATCHSETREG4

- Base Address: C001_0000h
- Address = Base Address + 08D4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET4	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET4 drives Scratch Register's set pin.	32'b0

12.8.1.56 ALIVESCRATCHSETREG5

- Base Address: C001_0000h
- Address = Base Address + 08E0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET5	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET5 drives Scratch Register's set pin.	32'b0

12.8.1.57 ALIVESCRATCHSETREG6

- Base Address: C001_0000h
- Address = Base Address + 08ECh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET6	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET6 drives Scratch Register's set pin.	32'b0

12.8.1.58 ALIVESCRATCHSETREG7

- Base Address: C001_0000h
- Address = Base Address + 08F8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET7	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET7 drives Scratch Register's set pin.	32'b0

12.8.1.59 ALIVESCRATCHSETREG8

- Base Address: C001_0000h
- Address = Base Address + 0904h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHSET8	[31:0]	RW	Set Alive Scratch Register Each bit of ALIVESCRATCHSET8 drives Scratch Register's set pin.	32'b0

12.8.1.60 ALIVESCRATCHREADREG1

- Base Address: C001_0000h
- Address = Base Address + 08B4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD1	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.61 ALIVESCRATCHREADREG2

- Base Address: C001_0000h
- Address = Base Address + 08C0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD2	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.62 ALIVESCRATCHREADREG3

- Base Address: C001_0000h
- Address = Base Address + 08CCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD3	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.63 ALIVESCRATCHREADREG4

- Base Address: C001_0000h
- Address = Base Address + 08D8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD4	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.64 ALIVESCRATCHREADREG5

- Base Address: C001_0000h
- Address = Base Address + 08E4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD5	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.65 ALIVESCRATCHREADREG6

- Base Address: C001_0000h
- Address = Base Address + 08F0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD6	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.66 ALIVESCRATCHREADREG7

- Base Address: C001_0000h
- Address = Base Address + 08FCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD7	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.67 ALIVESCRATCHREADREG8

- Base Address: C001_0000h
- Address = Base Address + 0908h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVESCRATCHREAD8	[31:0]	R	Read Alive Scratch Register	32'b0

12.8.1.68 VDDOFFDELAYRSTREGISTER

- Base Address: C001_0000h
- Address = Base Address + 090Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VDDOFFDELAYRST	[31:0]	RW	ResetVDD Off delay value register Each bit of vddoffdelayrst drives Vdd off delay value Register's reset pin.	32'b0

12.8.1.69 VDDOFFDELAYSETREGISTER

- Base Address: C001_0000h
- Address = Base Address + 0910h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VDDOFFDELAYSET	[31:0]	RW	SetVDD Off delay value register Each bit of vddoffdelayset drives Vdd off delay value Register's set pin.	32'b0

12.8.1.70 VDDOFFDELAYVALUEREGISTER

- Base Address: C001_0000h
- Address = Base Address + 0914h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VDDOFFDELAYVALUE	[31:0]	R	VDD OFF DELAY VALUE (unit: RTC clock)	32'b0

12.8.1.71 VDDOFFDELAYTIMEREGISTER

- Base Address: C001_0000h
- Address = Base Address + 0918h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VDDOFFDELAYTIME	[31:0]	R	VDD OFF DELAY TIME (unit: RTC clock) clear is vddoffdelayrst/set register write	32'b0

12.8.1.72 ALIVEGPIOINPUTVALUE

- Base Address: C001_0000h
- Address = Base Address + 091Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALIVEGPIOINPUTVALUE	[31:0]	R	Nth bit of this register show the value of AliveGPIO[N].	32'b0

12.8.1.73 PMUNISOLATE

- Base Address: C001_0000h
- Address = Base Address + 0D00h, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	0
NISOLATE_MFC	[1]	RW	Power isolation (low active Power Isolation) for MFC block The default value is 1 (all blocks are connected normally) Sub-block must be isolatioted in order to power off the sub-block 0 = Isolate (ready-to-power-off) 1 = normal mode	0x1
NISOLATE_GPU	[0]	RW	Power isolation (low active Power Isolation) for GPU block The default value is 1 (all blocks are connected normally) Sub-block must be isolatioted in order to power off the sub-blocks 0 = Isolate (ready-to-power-off) 1 = normal mode	0x1

12.8.1.74 PMUNPWRUPPRE

- Base Address: C001_0000h
- Address = Base Address + 0D04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	0
nPWRUPPRE_MFC	[1]	RW	Power up precharge for MFC block Sub-block must be precharged before powering up all power switches. 0 = Power up precharge 1 = Power down precharge	0x0
nPWRUPPRE_GPU	[0]	RW	Power up precharge for GPU block Sub-block must be precharged before powering up all power switches. 0 = Power up precharge 1 = Power down precharge	0x0

12.8.1.75 PMUNPWRUP

- Base Address: C001_0000h
- Address = Base Address + 0D08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	0
nPWRUP_MFC	[1]	RW	Power up for MFC block Sub-blocks must be powered up all switches before normal operation. 0 = Power up 1 = Power down	0x0
nPWRUP_GPU	[0]	RW	Power up for GPU block Sub-blocks must be powered up all switches before normal operation. 0 = Power up 1 = Power down	0x0

12.8.1.76 PMUNPWRUPACK

- Base Address: C001_0000h
- Address = Base Address + 0D0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	0
nPWRUPACK_MFC	[1]	R	Power up acknowledge for MFC block This register must be checked after NPWRUP_MFC register is set to power up. 0 = Power On (Powering Up Sequence is finished) 1 = Power Off	0
nPWRUPACK_GPU	[0]	R	Power up acknowledge for GPU block This register must be checked after NPWRUP_GPU register is set to power up. 0 = Power On (Powering Up Sequence is finished) 1 = Power Off	0

13 ID Register

13.1 Overview

ECID module of the S5P4418 stores the 128-bit DIEID information on a e-fuse ROM. Each Chip will have its own DIEID to identify it.

13.2 Features

- Support 128-bit Die ID
- Support 128-bit Secure Boot ID
- Support 128-bit Secure JTAG ID
- Support 128-bit Backdoor JTAG ID
- Programmable Secure Boot ID, Secure JTAG ID, Backdoor JTAG ID

13.3 Functional Description

13.3.1 AC Timing

Table 13-1 AC Timing Table

[Unit: ns]

Symbol	Description	Symbol	Description
Program Mode			
tPCS	CS to PROG setup time (setup rising, rist constraint)	tPCH	CS to PROG hold time (hold falling, fall constraint)
tFSRCS	FSOURCE to PROG setup time (setup rising, rise constraint)	tFSRCH	FSOURCE to PROG hold time (hold falling, fall constraint)
tPRW	PROG pulse width high (rising edge)	tSCW	SCK pulse width high (rising edge)
tPSS	SCK to PROG setup time (setup rising, fall constraint)	tPSH	SCK to PROG hold time (hold falling, rise constraint)
tSIS	SDI to SCK setup time (setup falling, rise/fall constraint)	tSIH	SDI to SCK hold time (hold falling, rise/fall constraint)
tSAS	SDI to A0 setup time (setup rising, rise constraint)	tSAH	SDI to A0 hold time (hold falling, fall constraint)
tAAS	A2, A1 to A0 setup time (setup rising, rising constraint)	tAAH	A2, A1 to A0 hold time (hold falling, fall constraint)
tAWH	A0 pulse width high	tAWL	A0 pulse width low
tPAS	A0 to PROG setup time (setup rising, fall constraint)	tPAH	A0 to PROG hold time (hold falling, rise constraint)
Sense Mode			
tSCS	CS to FSET setup time (setup rising, rise constraint)	tSCH	CS to FSET hold time (hold falling, fall constraint)
tAS	ADDR[] to FSET setup time (setup rising, rise/fall constraint)	tAH	ADDR[] to PRCHG hold time (hold falling, rise/fall constraint)
tPRS	PRCHG to FSET setup time (setup rising, rise constraint)	tPRH	PRCHG to SIGDEV hold time (hold rising, rise constraint)
			PRCHG to SIGDEV hold time (hold falling, fall constraint)
tSDS	SIGDEV to FSET setup time (setup rising, rise constraint)	tSDH	SIGDEV to FSET hold time (hold rising, fall constraint)
tACC	DOUT[] access time after SIGDEV fall (falling edge)	tFSH	FSET to PRCHG hold time (hold falling, fall constraint)
Scan Mode			
tDCS	CS to SCK setup time (setup rising, rise constraint)	tDCH	CS to SCK hold time (hold falling, fall constraint)
tPACC	DOUT[] access time after SCK fall (falling edge)	tSACC	SDOUT access time after SCK rise (rising edge)

- Blue : It will use each program mode and scan mode
- Red : It will use each program mode and sense mode
- tFSRCS, tFSRCH = 1000ns, All other timing arcs = 2ns
- tPRW = 10000ns ± 100ns (Not allowed out of tPRW range. Must need approval from PTE/DT team if any change)

13.3.2 Sense Mode Timing

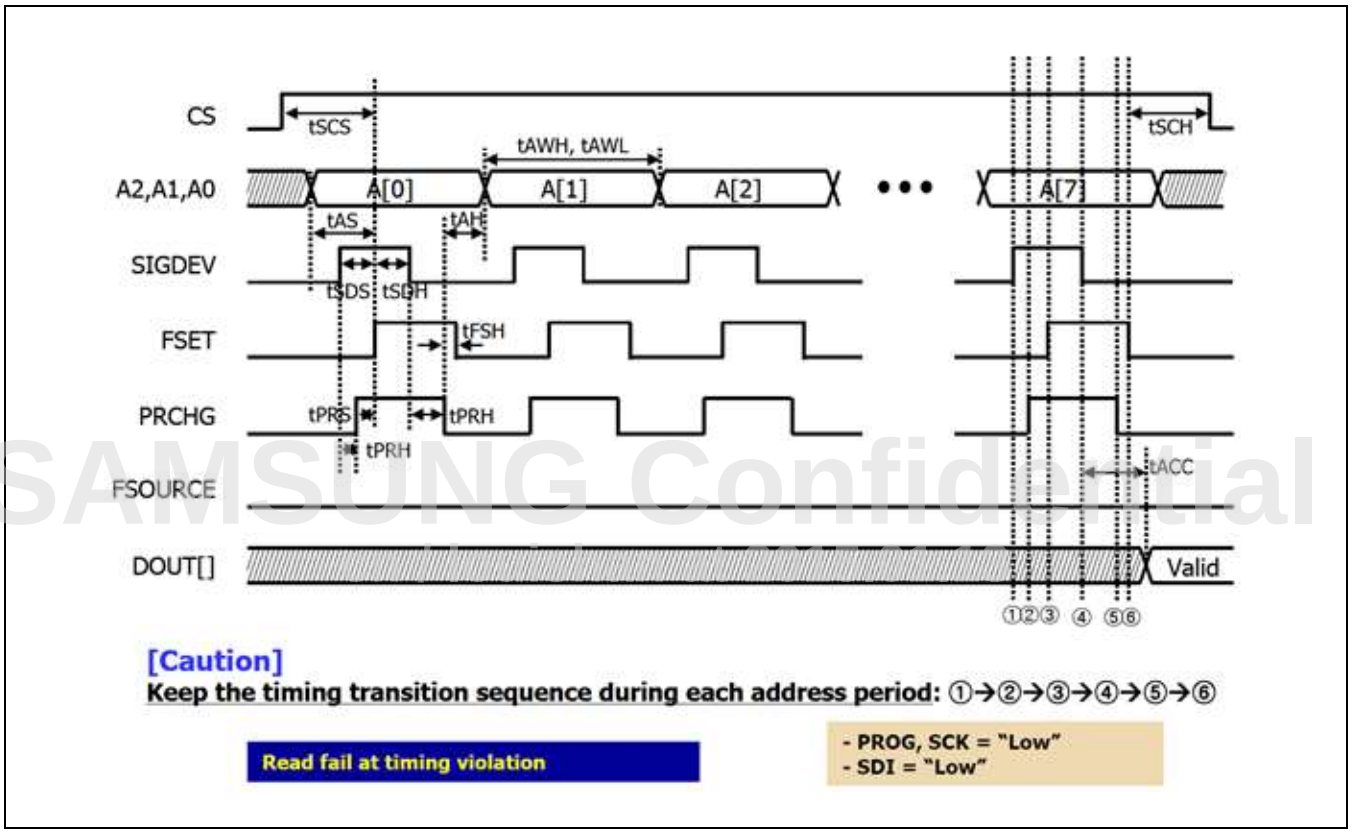


Figure 13-1 Sense Mode Timing

- When SIGDEV is enabled ("H"), sensing current is occurred. So you should reduce SIGDEV pulse width high period for power saving.
- CS should be set high (enable) and A2, A1, A0 states should be set properly before first SIGDEV rising in sense mode.
- After sense operation, DOUT[] have "0" for un-blown fuse cell and "1" for blown fuse cell.
- Sense (read) operation would be performed correctly with timing diagram above. The user who want to have different timing sequence must have a prior consultation with effuse designer.

13.3.3 Scan-latch Mode Timing

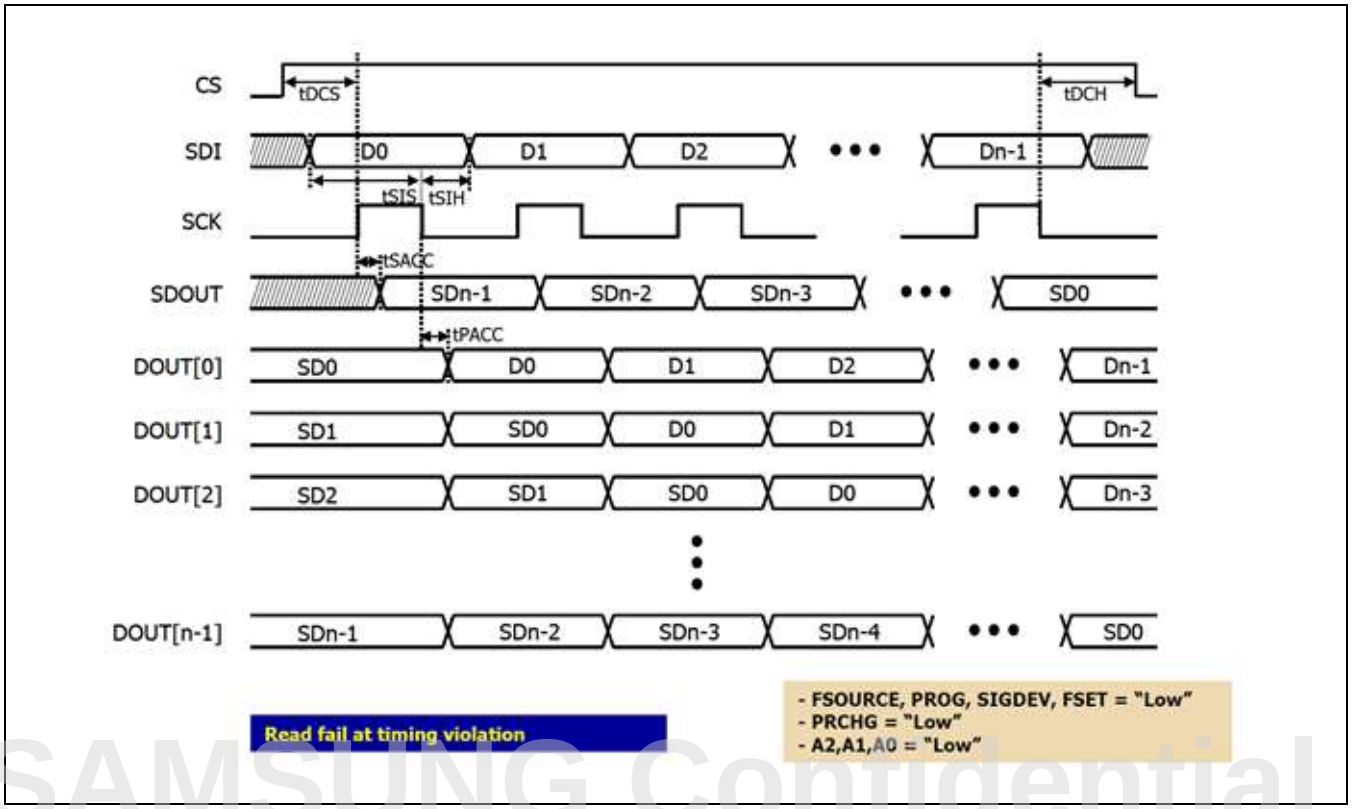


Figure 13-2 Scan-Latch Mode Timing

- After sense mode, cell's data is shifted to SDOUT by SCK in Scan-latch mode
- Scan-latch operation would be performed correctly with timing diagram above. The user who want to have different timing sequence must have a prior consultation with effuse designer.

13.3.4 Stand-by Mode Timing

- CS pin should be set to ground (=0.0v) to reduce unnecessary leakage current.
- Other control pins: don't care.

13.3.5 Program Mode Timing

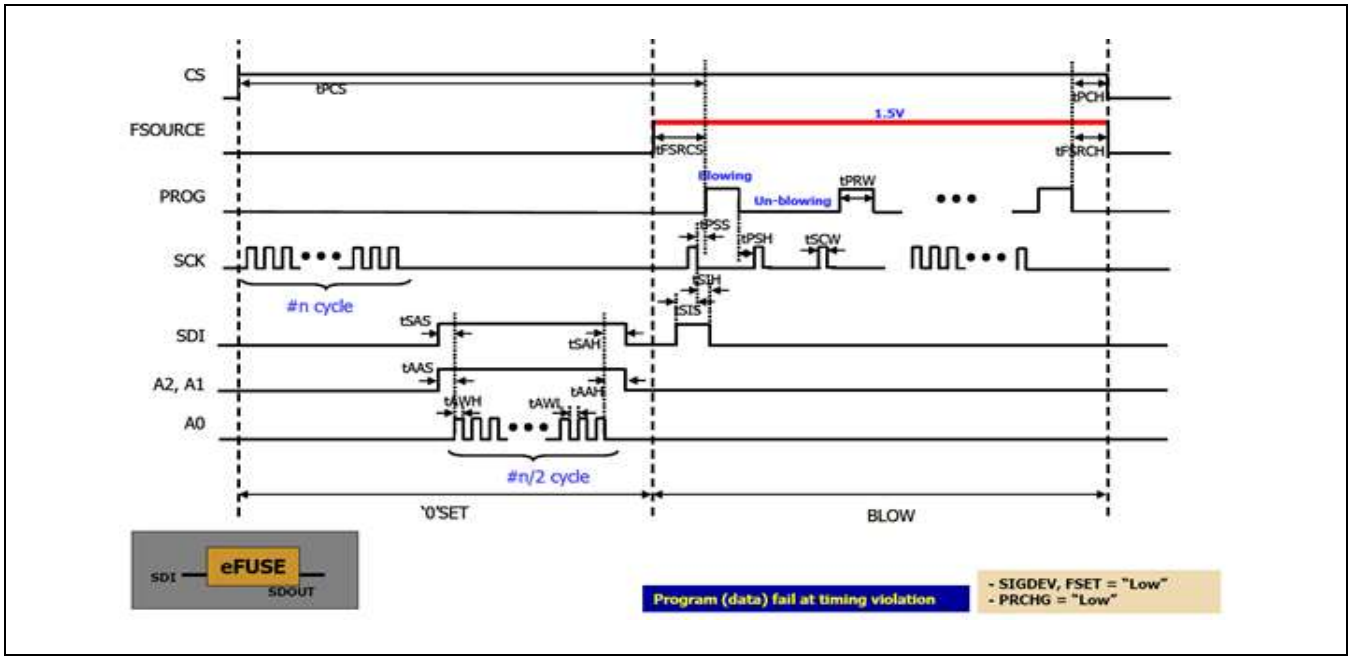


Figure 13-3 Fuse Programming Operation Using Single Macro

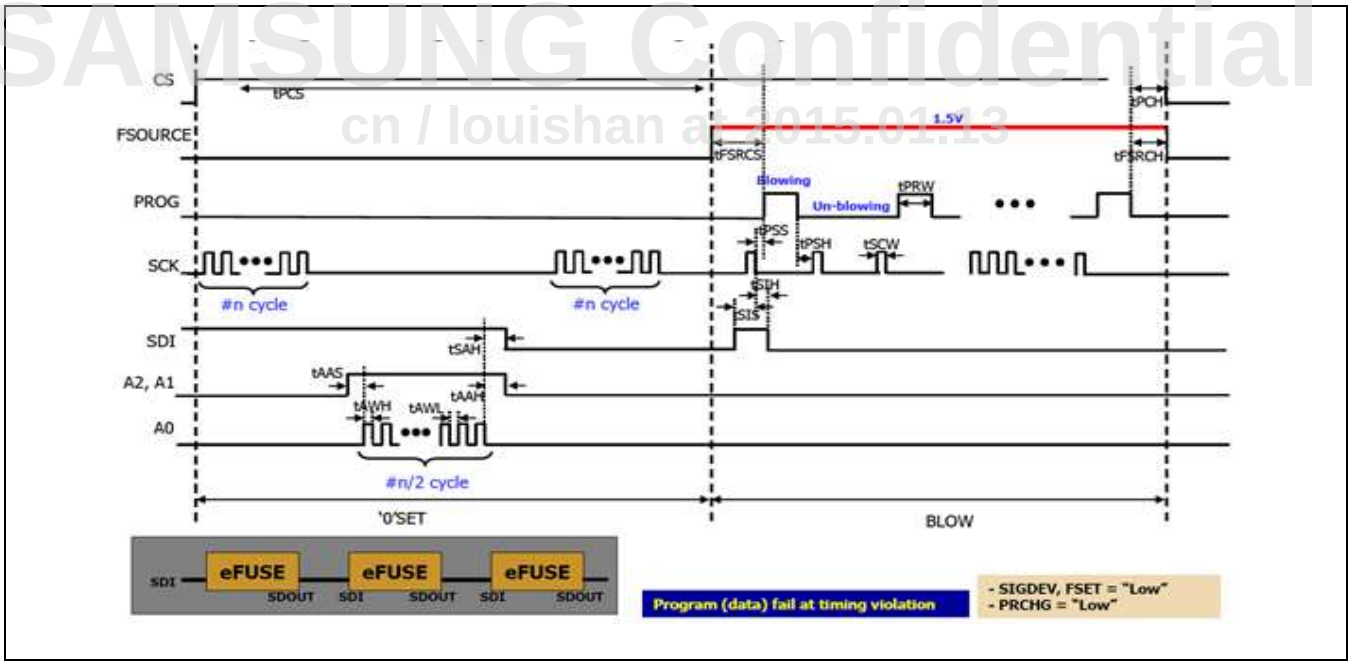


Figure 13-4 Fuse Programming Operation Using Single Macro

- Apply tFSRCS > 1 μs because of prevention leakage current from FSORUCE to ESD protection diode.
- Fuse program operation would be performed correctly with timing diagram above. The user who want to have different timing sequence must have a prior consultation with effuse designer.

13.4 Register Description

13.4.1 Register Map Summary

- Base Address: C006_7000h

Register	Offset	Description	Reset Value
ECID0	0x00h	128-bit ECID Register 0	–
ECID1	0x04h	128-bit ECID Register 1	–
ECID2	0x08h	128-bit ECID Register 2	–
ECID3	0x0Ch	128-bit ECID Register 3	–
CHIP_NAME_03_00	0x10h	Chip Name Register 03_00	–
CHIP_NAME_07_04	0x14h	Chip Name Register 07_04	–
CHIP_NAME_11_08	0x18h	Chip Name Register 11_08	–
CHIP_NAME_15_12	0x1Ch	Chip Name Register 15_12	–
CHIP_NAME_19_16	0x20h	Chip Name Register 19_16	–
CHIP_NAME_23_20	0x24h	Chip Name Register 23_20	–
CHIP_NAME_27_24	0x28h	Chip Name Register 27_24	–
CHIP_NAME_31_28	0x2Ch	Chip Name Register 31_28	–
CHIP_NAME_35_32	0x30h	Chip Name Register 35_32	–
CHIP_NAME_39_36	0x34h	Chip Name Register 39_36	–
CHIP_NAME_43_40	0x38h	Chip Name Register 43_40	–
CHIP_NAME_47_44	0x3Ch	Chip Name Register 47_44	–
RSVD	0x40h	Reserved	–
GUID0	0x44h	GUID0	–
GUID1_2	0x48h	GUID1_2	–
GUID3_0	0x4Ch	GUID3_0	–
GUID3_1	0x50h	GUID3_1	–
EC0	0x54h	ECID Control Register 0	0x0000_0000
EC1	0x58h	ECID Control Register 1	0x0000_0000
EC2	0x5Ch	ECID Control Register 2	0x0000_0000

13.4.1.1 ECID0

- Base Address: C006_7000h
- Address = Base Address + 0x00h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
ECID0	[31:0]	R	128-bit ECID Register [31:0]	–

13.4.1.2 ECID1

- Base Address: C006_7000h
- Address = Base Address + 0x04h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
ECID1	[31:0]	R	128-bit ECID Register [63:32]	–

13.4.1.3 ECID2

- Base Address: C006_7000h
- Address = Base Address + 0x08h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
ECID2	[31:0]	R	128-bit ECID Register [95:64]	–

13.4.1.4 ECID3

- Base Address: C006_7000h
- Address = Base Address + 0x0Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
ECID3	[31:0]	R	128-bit ECID Register [127:96]	–

13.4.1.5 CHIP_NAME_03_00

- Base Address: C006_7000h
- Address = Base Address + 0x10h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_3	[31:24]	R	Chip name character 3	–
chip_name_2	[23:16]	R	Chip name character 2	–
chip_name_1	[15:8]	R	Chip name character 1	–
chip_name_0	[7:0]	R	Chip name character 0	–

13.4.1.6 CHIP_NAME_07_04

- Base Address: C006_7000h
- Address = Base Address + 0x14h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_7	[31:24]	R	Chip name character 7	–
chip_name_6	[23:16]	R	Chip name character 6	–
chip_name_5	[15:8]	R	Chip name character 5	–
chip_name_4	[7:0]	R	Chip name character 4	–

13.4.1.7 CHIP_NAME_11_08

- Base Address: C006_7000h
- Address = Base Address + 0x18h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_11	[31:24]	R	Chip name character 11	–
chip_name_10	[23:16]	R	Chip name character 10	–
chip_name_9	[15:8]	R	Chip name character 9	–
chip_name_8	[7:0]	R	Chip name character 8	–

13.4.1.8 CHIP_NAME_15_12

- Base Address: C006_7000h
- Address = Base Address + 0x1Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_15	[31:24]	R	Chip name character 15	–
chip_name_14	[23:16]	R	Chip name character 14	–
chip_name_13	[15:8]	R	Chip name character 13	–
chip_name_12	[7:0]	R	Chip name character 12	–

13.4.1.9 CHIP_NAME_19_16

- Base Address: C006_7000h
- Address = Base Address + 0x20h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_19	[31:24]	R	Chip name character 19	–
chip_name_18	[23:16]	R	Chip name character 18	–
chip_name_17	[15:8]	R	Chip name character 17	–
chip_name_16	[7:0]	R	Chip name character 16	–

13.4.1.10 CHIP_NAME_23_20

- Base Address: C006_7000h
- Address = Base Address + 0x24h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_23	[31:24]	R	Chip name character 23	–
chip_name_22	[23:16]	R	Chip name character 22	–
chip_name_21	[15:8]	R	Chip name character 21	–
chip_name_20	[7:0]	R	Chip name character 20	–

13.4.1.11 CHIP_NAME_27_24

- Base Address: C006_7000h
- Address = Base Address + 0x28h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_27	[31:24]	R	Chip name character 27	–
chip_name_26	[23:16]	R	Chip name character 26	–
chip_name_25	[15:8]	R	Chip name character 25	–
chip_name_24	[7:0]	R	Chip name character 24	–

13.4.1.12 CHIP_NAME_31_28

- Base Address: C006_7000h
- Address = Base Address + 0x2Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_31	[31:24]	R	Chip name character 31	–
chip_name_30	[23:16]	R	Chip name character 30	–
chip_name_29	[15:8]	R	Chip name character 29	–
chip_name_28	[7:0]	R	Chip name character 28	–

13.4.1.13 CHIP_NAME_35_32

- Base Address: C006_7000h
- Address = Base Address + 0x30h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_35	[31:24]	R	Chip name character 35	–
chip_name_34	[23:16]	R	Chip name character 34	–
chip_name_33	[15:8]	R	Chip name character 33	–
chip_name_32	[7:0]	R	Chip name character 32	–

13.4.1.14 CHIP_NAME_39_36

- Base Address: C006_7000h
- Address = Base Address + 0x34h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_39	[31:24]	R	Chip name character 39	–
chip_name_38	[23:16]	R	Chip name character 38	–
chip_name_37	[15:8]	R	Chip name character 37	–
chip_name_36	[7:0]	R	Chip name character 36	–

13.4.1.15 CHIP_NAME_43_40

- Base Address: C006_7000h
- Address = Base Address + 0x38h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_43	[31:24]	R	Chip name character 43	–
chip_name_42	[23:16]	R	Chip name character 42	–
chip_name_41	[15:8]	R	Chip name character 41	–
chip_name_40	[7:0]	R	Chip name character 40	–

13.4.1.16 CHIP_NAME_47_44

- Base Address: C006_7000h
- Address = Base Address + 0x3Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
chip_name_47	[31:24]	R	Chip name character 47	–
chip_name_46	[23:16]	R	Chip name character 46	–
chip_name_45	[15:8]	R	Chip name character 45	–
chip_name_44	[7:0]	R	Chip name character 44	–

13.4.1.17 GUID0

- Base Address: C006_7000h
- Address = Base Address + 0x44h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
guid0	[31:0]	R	GUID 0	–

13.4.1.18 GUID1_2

- Base Address: C006_7000h
- Address = Base Address +0x48h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
guid2	[31:16]	R	GUID 2	–
guid1	[15:0]	R	GUID 1	–

13.4.1.19 GUID3_0

- Base Address: C006_7000h
- Address = Base Address + 0x4Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
guid3_3	[31:24]	R	GUID 3_3	–
guid3_2	[23:16]	R	GUID 3_2	–
guid3_1	[15:8]	R	GUID 3_1	–
guid3_0	[7:0]	R	GUID 3_0	–

13.4.1.20 GUID3_1

- Base Address: C006_7000h
- Address = Base Address + 0x50h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
guid3_7	[31:24]	R	GUID 3_7	–
guid3_6	[23:16]	R	GUID 3_6	–
guid3_5	[15:8]	R	GUID 3_5	–
guid3_4	[7:0]	R	GUID 3_4	–

13.4.1.21 EC0

- Base Address: C006_7000h
- Address = Base Address + 0x54h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	–	Reserved	–
A_FF	[9:7]	RW	Programmable A	3'b0
CS_FF	[6]	RW	Programmable CS	1'b0
sigdev_ff	[5]	RW	Programmable SIGDEV	1'b0
FSET_ff	[4]	RW	Programmable FSET	1'b0
prchg_ff	[3]	RW	Programmable PRCHG	1'b0
bonding_id	[2:0]	R	Boinding ID	–

13.4.1.22 EC1

- Base Address: C006_7000h
- Address = Base Address + 0x58h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	–	Reserved	–
prog_FF	[2]	RW	Programmable PROG	1'b0
sck_FF	[1]	RW	Programmable SCK	1'b0
sdi_ff	[0]	RW	Programmable SDI	1'b0

13.4.1.23 EC2

- Base Address: C006_7000h
- Address = Base Address + 0x5Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
hw_done	[15]	R	ECID initialize done	1'b0
RSVD	[14:5]	–	Reserved	–
hdcp_efuse_sel	[4]	RW	HDCP Key select 0 = Secure Boot 1 = Secure JTAG	1'b0
RSVD	[3:2]	–	Reserved	–
sel_bank	[1:0]	RW	eFUSE select 0 = ECID 1 = Secure Boot 2 = Secure JTAG 3 = Backdoor JTAG	2'b0

13.5 Application Notes

- Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in EFROM_LP is permitted without any restrictions over Metal-4 layer.
- Incomming power bus should be adjusted to guarantee NOT more than 5 % voltage drop at typical-case current levels.
- Reduce resistance (<3 Ω) between PAD and FSOURCE pin of EFROM_LP.
- Connect routing signal to all of the FSOURCE pins.

When using two or more e-fuse sets, FSOURCE line can be shared among e-fuse sets, but program-mode operation should be applied sequentially. (For example, at first, operate e-fuse0 and then operate e-fuse1 for program-mode) It applies same during sense-mode, but there is a guideline for multi-sensing, only sense-mode.Keep the below rules. Refer to integration guide document for further information.

Allowed maximum resistance can be obtained by 3 Ω/# of 128-bit efuse box.

If customer wants to run multi-sensing,

→ 3 Ω: 128-bit × 1 ea, 1.5 Ω: 128-bit × 2 ea, 1 Ω: 128-bit × 3 ea, 0.5 Ω: 128-bit × 6 ea

14 Memory Controller

14.1 Overview

The S5P4418 Memory Controller is based on a Unified Memory Architecture (UMA). This Controller consists of two control units: MCU-A, MCU-S. Each unit has dedicated control pins.

14.1.1 Unified Memory Architecture (UMA)

- Two Separate Memory Controller:
  - MCU-A: DDR3/LVDDR3(Low Voltage DDR3)/LPDDR3/LPDDR2
  - MCU-S: Static Memory

- MCU-A features:
  - MCU-A is organized DREX and DDRPHY
  - Supports DDR3/LVDDR3(Low Voltage DDR3)/LPDDR3/LPDDR2 memory
  - Supports 8/16/32-bit SDRAM of 2GByte
  - Single Bank of Memory (32-bit data bus width)
  - Supports Power down mode
  - Supports Self Refresh mode

- MCU-S features:
  - Static memory
  - Two Static Memory Chip Selects
  - NAND Flash Interface
  - 23-bit address supports using latch address
  - SLC NAND, MLC NAND with ECC (Supports BCH-algorithm)
  - Static Memory Map Shadow

14.2 Block Diagram

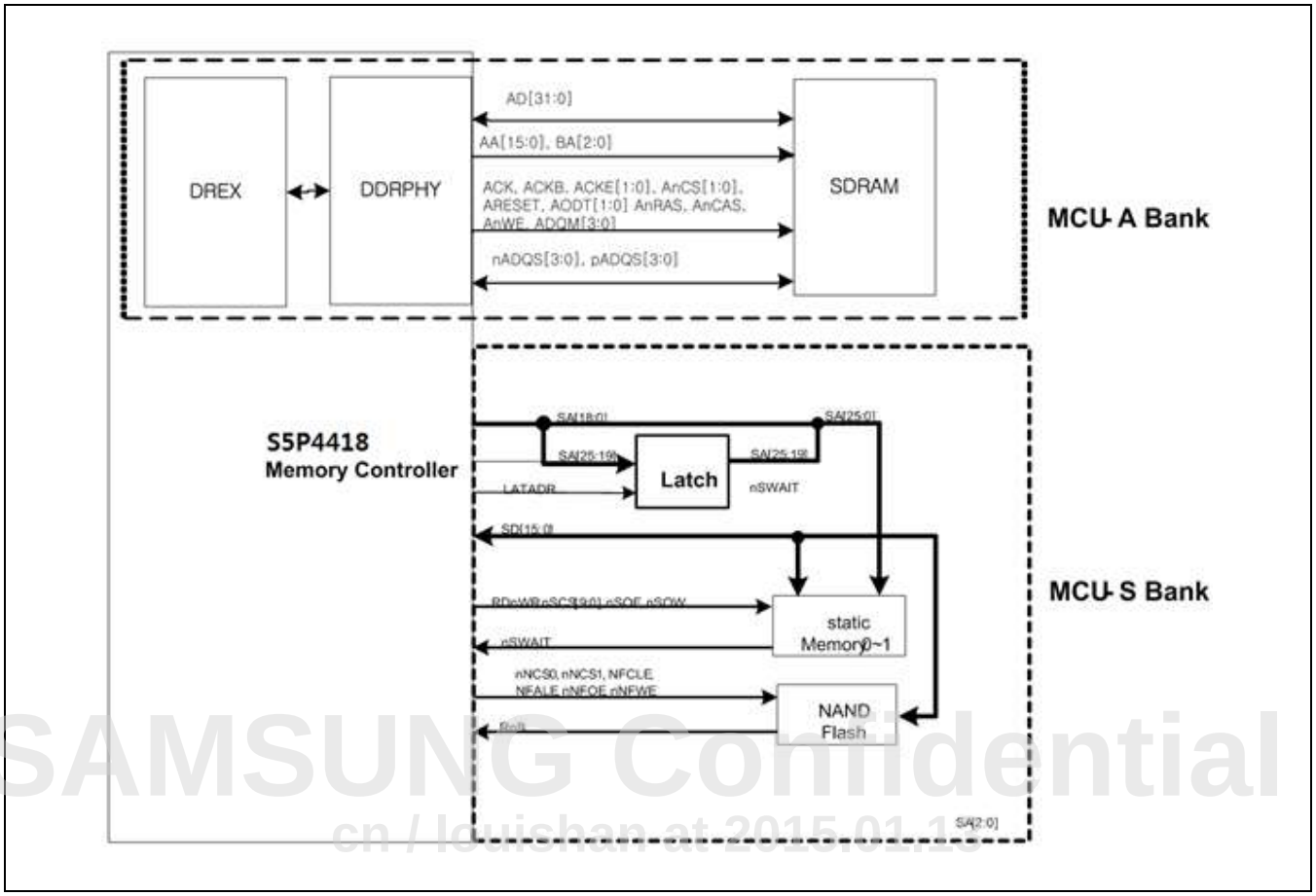


Figure 14-1 Memory Controller Block Diagram

14.3 Functional Description

The memory controller area of the S5P4418 is divided into an MCU-A and MCU-S bank. The MCU-A bank is connected to DDR3/LVDDR3 (Low Voltage DDR3)/LPDDR3/LPDDR2 which is the main memory of the S5P4418 and 32-bit data bus width.

The MCU-S bank is the static bank and can be connected to Static Memory/Device, NAND (Refer to *Figure 14-2*)

14.3.1 MCU-A Bank Feature

- Compatible with JEDEC standard LPDDR2-S4/LPDDR3/LVDDR3(Low Voltage DDR3)/DDR3 SDRAMs
- Supports 1:2 synchronous operation between bus clock and Memory clock
- Supports up to two memory ranks (chip selects) and 4/8 banks per memory chips
- Supports 512Mb, 1Gb, 2Gb, 4Gb, 8Gbit and 16Gbit density per a chip select
- Supports outstanding exclusive accesses
- Supports bank selective pre-charge policy
- DREX Clock: MBCLK (400 MHz)
- DDRPHY Clock: MCLK (800 MHz), MDCLK (800 MHz)
- MBCLK: MCLK = 1: MBCLKx2
  - MDCLK: MDCLK 0° phase Master DLL clock (400 to 800 MHz). This clock should be the same frequency clock with clk2x in normal mode and generated from the same PLL which MCLK is using. But Master DLL is not able to lock under 400MHz. if MCLK is under 400 MHz, the double frequency of clk2x can be used for locking Master DLL for the low frequency operation

14.3.2 MCU-S Bank Feature

- Latched Addressing
  The number of pins that are connected to the outside is ADDR[18:0]. Since, however, the total address of the MCU-S Bank is 26-bit. ADDR[8:2] and ADDR[25:19] are allotted to the same pin, the system has a structure in which addresses are output two times. If the system uses ADDR[19] or more, the setting of higher address (ADDR[25:19]) is possible via System Configuration Pin (CfgSTLATADD). In this event, ADDR[25:19] which is configured by using external Latch IC first should be latched.

- 16-bit data bus width
  Static memory register except NAND flash (8 bits) has bus width select registers

- Static memory Controller
  Normal static memory (SRAM and ROM) or static devices are connected.
  Up to two Static Chip Select signals exist.

- NAND Flash Controller
  It supports both the small and large block NAND flash memories.
  Up to two NAND flash memories can be connected.
  Supports both SLC and MLC NAND flash memories.
  Up to 4/8/16/24/40/60-bit error correction/(1024 or 512 byte) using Binary-BCH coding

14.3.3 Memory Map

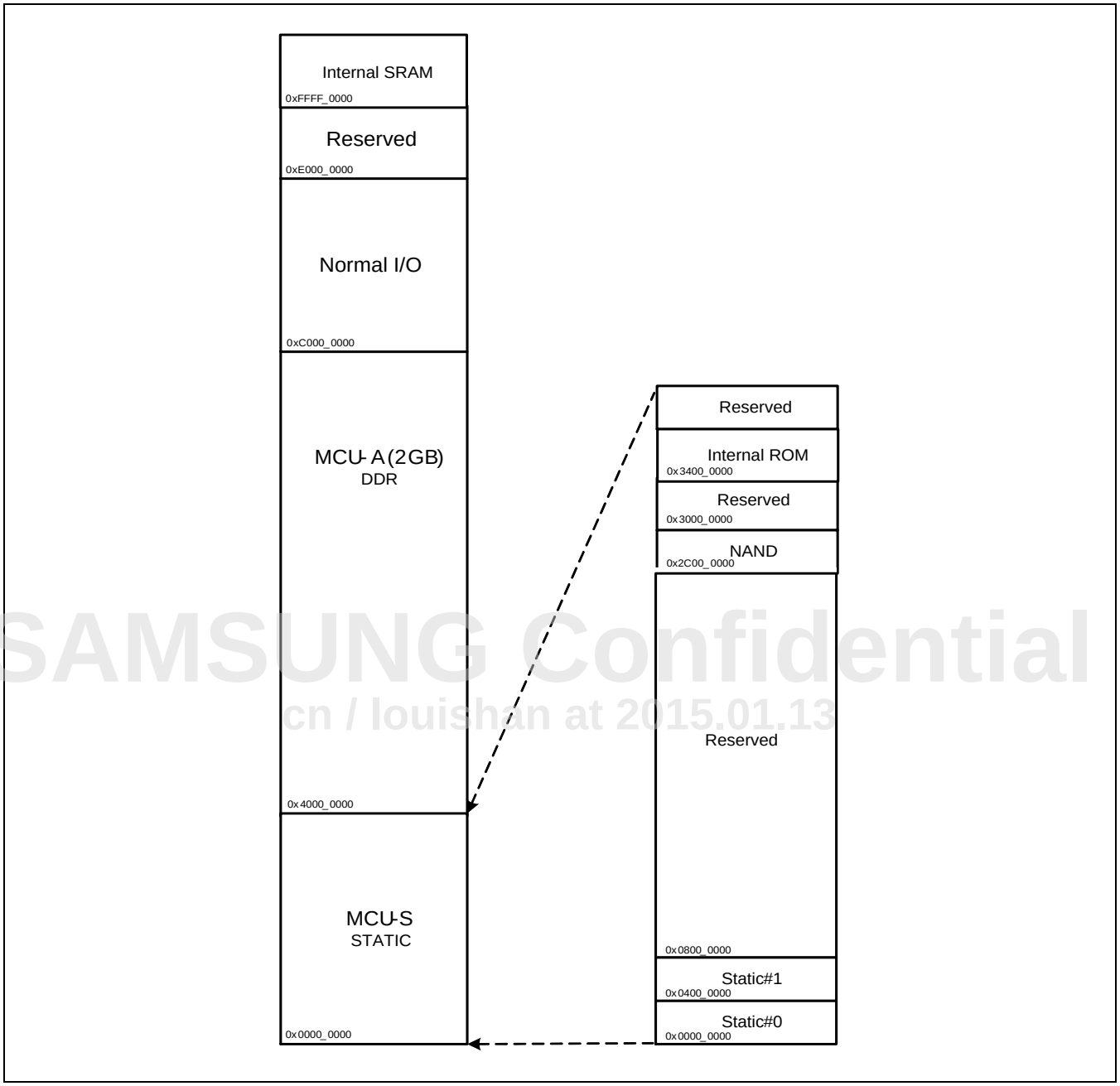


Figure 14-2 Memory Map

The memory map is roughly divided into one SDRAM Bank (MCU-A) and one static bank (MCU-S). The static bank consists of NAND Flash controller, Static Memory controller. The MCU-A bank consist of a Linear Array area and Display Array area.

14.3.4 MCU-A Address Mapping

DREX modifies the address of the AXI transaction coming from the AXI slave port into a memory address - chip select, bank address, row address, column address and memory data width.

To map chip select of memory device to a specific area of the address map, the chip_base and chip_mask bit-fields of the MemConfig0 register needs to be set (Refer to Register Descriptions). If chip1 of the memory device exists, the MemConfig1 register must also be set. Then, the AXI address requested by AXI Masters is divided into the AXI base address and AXI offset address. The AXI base address activates the appropriate memory chip select and the AXI offset address is mapped to a memory address according to the bank, row, column number, and data width set by the MemConfig0/1 and MemControl register.

There are two ways to map the AXI offset address as shown below: 14.2.4.1 linear mapping, 14.2.4.2 interleaved mapping

14.3.4.1 Linear Mapping

As shown in *Figure 14-3* the linear mapping method maps the AXI address in the order of bank, row, column and width. Since the bank address does not change for at least one bank size, applications that use linear address mapping have a high possibility to access the same bank.

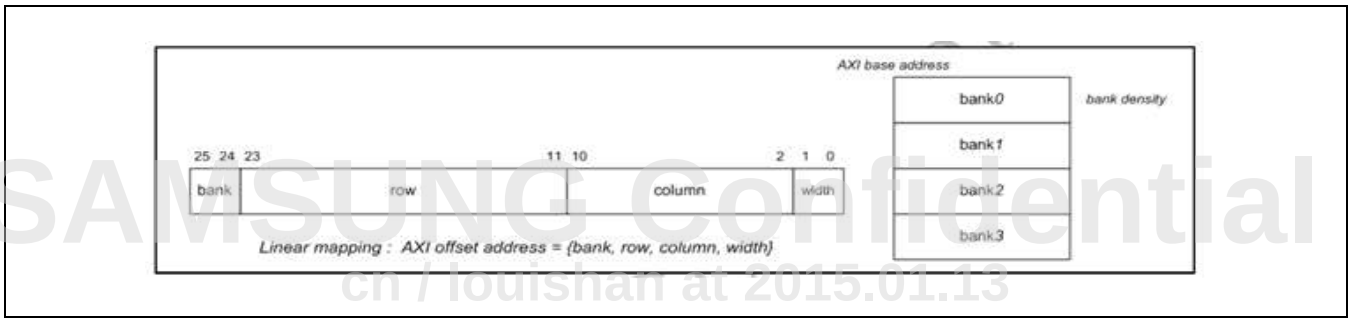


Figure 14-3 Linear Address Mapping

14.3.4.2 Interleaved Mapping

As shown in *Figure 14-4* the interleaved mapping method maps the AXI address in the order of row, bank, column and width. The difference between above two methods is that the bank and row order is different. For accesses beyond a row size, interleaved mapping accesses a different bank. Therefore, applications that use interleaved mapping access numerous banks. It causes better performance but more power consumption Command Arbiter.

Command Arbiter re-arbitrates with the result of Fast Arbiter and Slow Arbiter. In this case, Fast Arbiter is always processed ahead with fixed method.

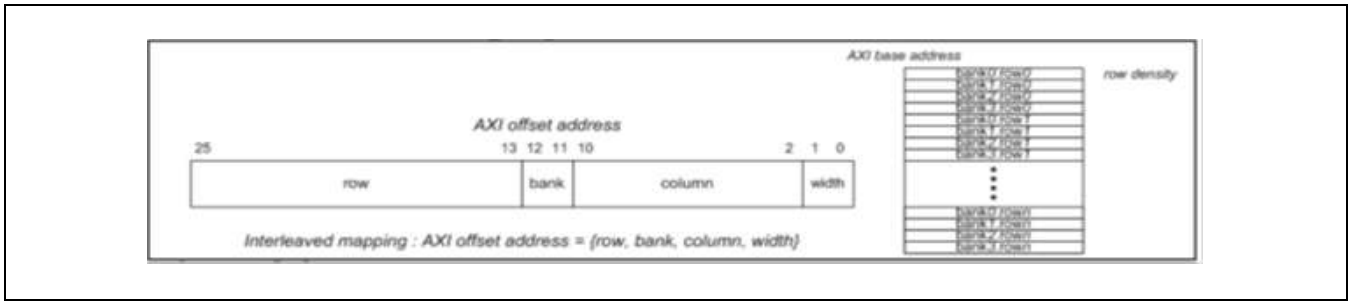


Figure 14-4 Linear Address Mapping

14.3.5 Low Power Operation

The controller executes a low power memory operation in five ways as described below. Each feature is independent of each other and executed at the same time.

14.3.5.1 AXI Low Power Channel

The controller has an AXI low power channel interface to communicate with low power management units such as the system controller, which makes the memory device go into self refresh mode.

14.3.5.2 Dynamic Power Down

An SDRAM device has an active/pre-charge power down mode. This mode is triggered by de-asserting CKE to LOW. When any of the banks is open, it enters active power down mode. Otherwise, it enters pre-charge power down mode.

When the request buffers remain empty for certain number of cycles (PwrdnConfig.dpwrdn_cyc register), DREX-1 changes the memory devices state to active/pre-charge power down automatically. The memory device enters Active/pre-charge power down mode or Forced pre-charge power down mode according to the SFR setting. The description of the two power down modes are as follows:

1. Active/pre-charge power down mode: Enter power down w/o considering whether there is a row open or not.
2. Forced pre-charge power down mode: Enter power down after closing all banks.

When DREX-1 receives a new AXI transaction while memory device is in power down mode, it automatically wakes up the memory device from power down state and executes in a normal operation state.

14.3.5.3 Dynamic Self Refresh

Similarly to the dynamic power down feature, if the request buffers remain empty for certain number of cycles (PwrdnConfig.dsref_cyc register), DREX-1 changes the memory device's state to self-refresh mode. Since exiting power down mode requires many cycles, a longer idle cycle threshold is recommended for dynamic self-refresh entry than the threshold for dynamic power down.

14.3.5.4 Clock Stop

To reduce the I/O power of the memory device and the controller, it is possible to stop the clock if the LPDDR / LPDDR2-S4 is in idle mode, or self refresh mode and DDR3 is in self refresh mode. If this feature is enabled, the controller automatically executes the clock stop feature. In DDR3, clock stop feature must be turn-on and off considering tCKSRX/tCKSRE/tCKESR timing by software.

14.3.5.5 Direct Command

Use the direct command feature to send a memory command directly to the memory device through the APB3 port. This way, it is possible to force the memory device to enter active/pre-charge power down, self-refresh or deep power down mode

14.3.6 MCU-A APPLICATION NOTE

14.3.6.1 DREX Initialization

14.3.6.1.1 LPDDR2/3

The following sequence should be used to initialize LPDDR2 devices. Unless specified otherwise, these steps are mandatory.

1. To provide stable power for memory device, DREX-1 must assert and hold CKE to a logic low level. Then apply stable clock.
2. Set the right value to PHY control register0 for LPDDR2/3 operation mode. If read leveling is needed, check LPDDR2/3 IO calibration MRR data and match it to PHY control register1's ctrl_rlvl_rdata_adj field. (Refer to PHY manual)
3. Set the PHY for dqs pull down mode. (Refer to PHY manual, PHY control register 14)
4. Set the ConControl. At this moment, assert the dfi_init_start field to high but the aref_en field should be off.
5. Wait for the PhyStatus0.dfi_init_complete field to change to [1[.
6. Set the ConControl. At this moment, de-assert the dfi_init_start field to low and the aref_en field should be off.
7. Set the PhyControl0.fp_resync bit-field to [1] to update DLL information for at least one MPCLK cycle.
8. Set the PhyControl0.fp_resync bit-field to [0].
9. Set the MemControl and PhyControl0. At this moment, all power down modes including sl_dll_dyn_con should be off.
10. Set the MemBaseConfig0 register. If there are two external memory chips, set the MemBaseConfig1 register.
11. Set the MemConfig0 register. If there are two external memory chips, also set the MemConfig1 register.
12. Set the PrechConfig and PwrdnConfig registers.
13. Set the TimingAref, TimingRow, TimingData and TimingPower registers according to memory AC parameters.
14. If QoS scheme is required, set the QosControl0 to 15 and QosConfig0 to 15 registers.
15. Set the PHY for LPDDR2/3 initialization. LPDDR2/3 initialization clock period is 18ns to 100ns. If LPDDR2/3 initialization clock period is 20ns, then follow below steps 16 to 22(refer to PHY manual).
16. Set the PHY ctrl_offsetr0 to 3 and ctrl_offsetw0 to 3 value to 0x7F
17. Set the PHY ctrl_offsetd value to 0x7F.
18. Set the PHY ctrl_force value to 0x7F.
19. Set the PHY ctrl_dll_on to low.
20. Wait for 10 MPCLK cycles.
21. Set the PhyControl0.fp_resync bit-field to [1] to update DLL information.
22. Set the PhyControl0.fp_resync bit-field to [0].

23. Confirm that CKE has been as a logic low level at least 100ns after power on
24. Issue a NOP command using the DirectCmd register to assert and to hold CKE to a logic high level.
25. Wait for minimum 200 us.
26. Issue a MRS command using the DirectCmd register to reset memory devices and program the operating parameters.
27. Wait for minimum 10 us.
28. Issue proper lpddr2 initialization commands according to specification such as IO calibration (MR #10), device feature1, 2 (MR #1, #2). Refer to LPDDR2/3 specification for details.
29. If there are two external memory chips, perform steps 24 to 28 for chip1 memory device.
30. Set the PHY ctrl_offsetr0 to 3 and ctrl_offsetw0 to 3 value to 0x0
31. Set the PHY ctrl_offsetd value to 0x0
32. Set the PHY ctrl_dll_on enable
33. Wait for 10 MPCLK cycles.
34. Set the PHY ctrl_start value to 0.
35. Set the PHY ctrl_start value to 1.
36. Wait for 10 MPCLK cycles.
37. Wait for the PhyStatus0.dfi_init_complete field to change to "1".
38. Set the PhyControl0.fp_resync bit-field to '1' to update DLL information.
39. Set the PhyControl0.fp_resync bit-field to '0'.
40. If any leveling/training is needed, disable ctrl_dll_on and set ctrl_force value. (Refer to PHY manual)
41. If write leveling for LPDDR3 is not needed, skip this procedure. If write leveling is needed, set LPDDR3 into write leveling mode using MRS command, set ODT pin high and tWLO using WRLVL_CONFIG0 register (offset = 0x120) and set the related PHY SFR fields through PHY APB Interface (Refer to PHY manual). To generate 1 cycle pulse of dfi_wrdata_en_p0, write 0x1 to WRLVL_CONFIG1 register (Offset addr = 0x124). To read the value of memory data, use CTRL_IO_RDATA (offset = 0x150). If write leveling is finished, then set ODT pin low and disable write leveling mode of LPDDR3
42. If CA calibration for LPDDR3 is not needed, skip this procedure. If CA calibration is needed, set the related PHY SFR fields through PHY APB Interface (Refer to PHY manual). Set LPDDR3 into CA calibration mode through MR41. For CKE assertion, de-assertion, CA value and tADDR setting, use CACAL_CONFIG0 (offset = 0x160). For Generation 1 cycle pulse of dfi_csn_p0, use CACAL_CONFIG1 (offset = 0x164). To read the value of memory data, use CTRL_IO_RDATA_CH0/CH1 (offset = 0x150, 0x154). Note that CKE pin should be asserted when MR41/48/42 command is issued and CKE pin should be de-asserted during CA calibration. Also note that because CA SDLL code updating needs some cycles to complete, 10 MPCLK cycles are needed before issuing next command.

43. If read leveling is not needed, skip 44 to 48 and set proper value to PHY control register #2. If read leveling is needed, set the related PHY SFR fields through PHY APB Interface. The related register is PHY control register #1 and #2 (mpr value, ctrl_rdlvl_gate_en and ctrl_rdlvl_en register, refer to PHY manual).
44. Set the RdlvlConfig.ctrl_rdlvl_data_en bit-field to 1'b1. Gate training is not supported.
45. Wait for the PhyStatus0.read_level_complete field to change to [1].
46. Disable the RdlvlConfig.ctrl_rdlvl_gate_en and ctrl_rdlvl_data_en.
47. Set the PhyControl0.fp_resync bit-field to [1] to update DLL information.
48. Set the PhyControl0.fp_resync bit-field to [0].
49. If write training is not needed, skip 50 to 55. If write training is nedded, set the related PHY SFR fields through PHY APB Interface. The related register is PHY control register #2 and #26, refer to PHY manual)
50. Set write latency of PHY control register #26.
51. Enable WrtraConfig.write_training_en to issue ACT command. Refer to this register definition for row and bank address.
52. Wait for 10 MPCLK cycles.
53. Enable write de-skewing of PHY control register #2.
54. Wait for the PhyStatus0.read_level_complete field to change to ?1?.
55. Disable write de-skewing of PHY control register #2.
56. After all leveling/training are completed, enable ctrl_dll_on. (Refer to PHY manual)
57. Set the PhyControl0.fp_resync bit-field to [1] to update DLL information.
58. Set the PhyControl0.fp_resync bit-field to [0].
59. Disable PHY gating control through PHY APB Interface (ctrl_atgate, see PHY manual).
60. If power down modes are required, set the MemControl register.
61. Set the ConControl to turn on an auto refresh counter.

14.3.6.1.2 DDR3

The following sequence should be used to initialize DDR3 devices. Unless specified otherwise, these steps are mandatory.

1. Apply power. RESET# pin of memory needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" any time before RESET# being de-asserted (Min. time 10ns)
2. Set the PHY for DDR3 operation mode. If read leveling is needed, check DDR3 MPR data and match it to PHY control register1's ctrl_rlvl_rdata_adj field. (Refer to PHY manual)
3. Set the PHY for dqs pull down mode. (Refer to PHY manual, PHY control register 14)
4. If on die termination is required, enable PhyControl0.mem_term_en, PhyControl0.phy_term_en.
5. Set the ConControl. At this moment, assert the dfi_init_start field to high but the aref_en field should be off.
6. Wait for the PhyStatus0.dfi_init_complete field to change to [1].
7. Set the ConControl. At this moment, de-assert the dfi_init_start field to low and the aref_en field should be off.
8. Set the PhyControl0.fp_resync bit-field to [1] to update DLL information.
9. Set the PhyControl0.fp_resync bit-field to [0].
10. Set the MemControl and PhyControl0. At this moment, all power down modes including sl_dll_dyn_con and periodic ZQ (pzq_en) should be off.
11. Set the MemBaseConfig0 register. If there are two external memory chips, set the MemBaseConfig1 register.
12. Set the MemConfig0 register. If there are two external memory chips, also set the MemConfig1 register.
13. Set the PrechConfig and PwrdnConfig registers.
14. Set the TimingAref, TimingRow, TimingData and TimingPower registers according to memory AC parameters.
15. If QoS scheme is required, set the QosControl0 to 15 and QosConfig0 to 15 registers.
16. Confirm that after RESET# is de-asserted, 500 us have passed before CKE becomes active.
17. Confirm that clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active.
18. Issue a NOP command using the DirectCmd register to assert and to hold CKE to a logic high level.
19. Wait for Txpr (Max. (5nCK,tRFC(min)+10ns)) or set tXP to tXPR value before step 17. If the system set tXP to tXPR, then the system must set tXP to proper value before normal memory operation.
20. Issue an EMRS2 command using the DirectCmd register to program the operating parameters. Dynamic ODT should be disabled. A10 and A9 should be low.
21. Issue an EMRS3 command using the DirectCmd register to program the operating parameters.
22. Issue an EMRS command using the DirectCmd register to enable the memory DLL.
23. Issue a MRS command using the DirectCmd register to reset the memory DLL.

24. Issues a MRS command using the DirectCmd register to program the operating parameters without resetting the memory DLL.
25. Issues a ZQINIT commands using the DirectCmd register.
26. If there are two external memory chips, perform steps 18 to 25 procedures for chip1 memory device.
27. If any leveling/training is needed, disable ctrl_dll_on and set ctrl_force value. (Refer to PHY manual)
28. If write leveling is not needed, skip this procedure. If write leveling is needed, set DDR3 into write leveling mode using MRS command, set ODT pin high and tWLO using WRLVL_CONFIG0 register (offset = 0x120) and set the related PHY SFR fields through PHY APB Interface (Refer to PHY manual). To generate 1 cycle pulse of dfi_wrdata_en_p0, write 0x1 to WRLVL_CONFIG1 register (Offset addr = 0x124). If write leveling is finished, then set ODT pin low and disable write leveling mode of DDR3
29. If gate leveling is not needed, skip 30 to 33. Gate leveling is only supported DDR3 over 667 MHz.
    If gate leveling is needed, set the related PHY SFR fields through PHY APB Interface. The related register is PHY control register #0, #1 and #2 (Refer to PHY manual)
30. Set the RdlvlConfig.ctrl_rdlvl_gate_en bit-field to 1'b1.
31. Wait for the PhyStatus0.read_level_complete field to change to [1].
32. Disable DQS pull down mode. (Refer to PHY manual)
33. Disable the RdlvlConfig.ctrl_rdlvl_gate_en and ctrl_rdlvl_data_en.
34. If read leveling is not needed, skip 35 to 39 and set proper value to PHY control register #2.
    If read leveling is needed, set the related PHY SFR fields through PHY APB Interface. The related register is PHY control register #1 and #2 (mpr value, ctrl_rdlvl_gate_en and ctrl_rdlvl_en register, refer to PHY manual).
35. Set the ctrl_rdlvl_data_en bit-field to 1'b1.
36. Wait for the PhyStatus0.read_level_complete field to change to [1]
37. Disable the RdlvlConfig.ctrl_rdlvl_gate_en and ctrl_rdlvl_data_en.
38. Set the PhyControl0.fp_resync bit-field to [1] to update DLL information.
39. Set the PhyControl0.fp_resync bit-field to [0].
40. If write training is not needed, skip 41 to 46. If write training is needed, set the related PHY SFR fields through PHY APB Interface. The related register is PHY control register #2 and #26, refer to PHY manual)
41. Set write latency of PHY control register #26.
42. Enable WrtraConfig.write_training_en to issue ACT command. Refer to this register definition for row and bank address.
43. Wait for 10 MPCLK cycles.
44. Enable write de-skewing of PHY control register #2.
45. Wait for the PhyStatus0.read_level_complete field to change to [1].
46. Disable write de-skewing of PHY control register #2.

47. After all leveling/training are completed, enable ctrl_dll_on. (Refer to PHY manual)
48. Set the PhyControl0.fp_resync bit-field to [1] to update DLL information.
49. Set the PhyControl0.fp_resync bit-field to [0].
50. Disable PHY gating control through PHY APB Interface (ctrl_atgate, refer to PHY manual).
51. If power down modes or periodic ZQ (pzq_en) are required, set the MemControl register.
52. Set the ConControl to turn on an auto refresh counter.

14.3.6.2 DDRPHY Initialization

After power-up and system PLL locking time, system reset (rst_n) is released.

1. Select Memory Type (=PHY_CON0[12:11]).
   - ctrl_ddr_mode = 2'b11 (LPDDR3)
   - ctrl_ddr_mode = 2'b10 (LDDR2)
   - ctrl_ddr_mode = 2'b01 (DDR3)

NOTE: If ctrl_ddr_mode[1] = 1'b1, lpddr2_cmd = 14'h000E(=PHY_CON25[13:0]), cmd_default = 14'h000F(=PHY_CON26[13:0])

2. ZQ Calibration (Please refer to "8.5 ZQ I/O CONTROL PROCEDURE" for more details)
   - Set Drive Strength (=zq_mode_dds or PHY_CON39[27:0]) properly (Please refer to p56, p63).- Please don't use default value (=0x0)
   - Enable and Disable "zq_clk_div_en" in PHY_CON16[18]
   - Enable "zq_manual_str" in PHY_CON16[1]
   - Wait until "zq_cal_done" (=PHY_CON17[0]) is enabled.
   - Disable "zq_manual_str" (=PHY_CON16[1])

3. Memory Controller should assert "dfi_init_start" from LOW to HIGH.

4. Memory Controller should wait until "dfi_init_complete" is set
   - DLL lock will be processed.
   - If the frequency of "MDCLK" is changed during operation, "ctrl_start" should be clear and set to lock again.

5. Enable DQS pull down mode

6. Memory Controller should assert "dfi_ctrlupd_req" after "dfi_init_complete" is set.

7. Start Memory Initialization.

8. Skip the following steps if Leveling and Training are not required.
   - Constraints during Leveling
     - Support BL=4 or 8 during Leveling. (Don't use BL=16)
     - Not support Memory ODT (On-Die-Termination) during Write DQ Calibration.
   - Enable "ctrl_atgate" in PHY_CON0[6].
   - Enable "p0_cmd_en" in PHY_CON0[14].
   - Enable "InitDeskewEn" in PHY_CON2[6].
   - Enable "byte_rdlvl_en" in PHY_CON0[13].
   - Set "rdlvl_pass_adj = 4'h6" in PHY_CON1[19:16].
   - Set "ddr3_cmd = 14'h105E" as default value (=PHY_CON25[29:16)
   - Set "lpddr2_cmd = 14'h107E" as default value (=PHY_CON25[13:0])
     - Set "cmd_default = 16'h000F(LPDDR2, LPDDR3), 16'h107F(DDR2, DDR3)" as default value (=PHY_CON26[13:0])
   - Recommend that "rdlvl_incr_adj=7'h01" for the best margin.
     - Calibration time can be shorter by adjusting "rdlvl_incr_adj" in PHY_CON2[22:16].
   - Disable "ctrl_dll_on" in PHY_CON12[5] before Leveling.
     - Read "ctrl_lock_value[8:2]" in PHY_CON13[16:10].
     - Update "ctrl_force[6:0]" in PHY_CON12[14:8] by the value of "ctrl_lock_value[9:2]".
   - Write Leveling (refer to 8.1.1)
   - CA Calibration (refer to 8.1.2)
   - Gate Leveling (refer to 8.1.3)
     - It should be used only for DDR3 (800 MHz). Please don't use under 800MHz.
   - Read DQ Calibration(=Read Leveling) (refer to 8.1.4)
   - After Read DQ Calibration, refer to "T_rddata_en" to know where "dfi_rddata_en_p0/p1" is enabled.
     - Read "T_rddata_en" timing parameters in PHY_CON18 after Read DQ Calibration.
   - Write DQ Calibration (refer to 8.1.5)
   - Enable "ctrl_dll_on" in PHY_CON12[5].
   - Disable "ctrl_atgate" in PHY_CON0[6] if controller controls "ctrl_gate_p0/p1" and "ctrl_read_p0/p1" directly.
   - Enable "DLLDeskewEn" (=PHY_CON2[12]) to compensate Voltage, Temperature variation during operation.

9. Controller should assert "dfi_ctrlupd_req" to make sure All SDLL is updated.
   - If "ca_swap_mode" is enabled, please don't use "ctrl_atgate=1" during normal operation.

NOTE: The goal of data eye training (=Read, Write DQ Calibration) is to identify the delay at which the read DQS rising edge aligns with the beginning and end transitions of the associated DQ data eye. By identifying these delays, the system can calculate the midpoint between the delays and accurately center the read DQS within the DQ data eye.

14.3.6.2.1 Write Leveling

Write Leveling compensates for the additional flight time skew delay introduced by the package, board and on-chip with respect to strobe (=DQS) and clock. The flight time skew between DQS and clock should be under 240ps to be compensated properly and suppose that the clock will be delayed than DQS

1. Memory Controller should configure Memory (DDR3, LPDDR3) in Write Level mode.
   - Memory Controller should assert "ODT[1:0]" signals(=dfi_odt_p0/p1) during Write Leveling.

2. Configure PHY in Write Level mode.
   - Enable "wrlvl_mode" in PHY_CON0[16].
   - "NOP" (CS HIGH at the clock rising edge N) should be used during "wrlvl_mode"=1 (Refer to p105).

3. To find out the optimal Write Level De-skew DLL code for the alignment between CK and DQS
   - Set each DLL code (PHY_CON30[6:0], PHY_CON[14:8], PHY_CON[23:17], PHY_CON[30:24]). (1)
     - The start code value should be 0x8. (0x8 to 0x38)
     - PHY_CON30[6:0] (= "DQS[0]" SDLL code)
     - PHY_CON30[14:8] (= "DQS[1]" SDLL code)
     - PHY_CON30[23:17] (= "DQS[2]" SDLL code)
     - PHY_CON30[30:24] (= "DQS[3]" SDLL code)
   - Update SDLL code(PHY_CON30[16]). (2)
     - Enable "ctrl_wrlvl_resync" in PHY_CON30[16]
     - Disable " ctrl_wrlvl_resync" in PHY_CON30[16]
   - Memory Controller should generate 1 cycle pulse of "dfi_wrdata_en_p0". (3)
   - Memory Controller should read the value of "ctrl_io_rdata[0]" which is output of PHY. (4)
     - If it is zero, Increment "DQS[0]" SDLL code by "1" and then go to "2" to update "DQS[0]" SDLL code.
     - If it is one, the previous "DQS[0]" SDLL code ("The current SDLL code - 1") will be the optimal SDLL code.
   - Memory Controller should read the value of "ctrl_io_rdata[8]" which is output of PHY. (5)
     - If it is zero, Increment "DQS[1]" SDLL code by "1" and then go to "2" to update "DQS[1]" SDLL code.
     - If it is one, the previous "DQS[1]" SDLL code ("The current SDLL code - 1") will be the optimal SDLL code.
   - Memory Controller should read the value of "ctrl_io_rdata[16]" which is output of PHY. (6)
     - If it is zero, Increment "DQS[2]" SDLL code by "1" and then go to "2" to update "DQS[2]" SDLL code.
     - If it is one, the previous "DQS[2]" SDLL code ("The current SDLL code - 1") will be the optimal SDLL code.
   - Memory Controller should read the value of "ctrl_io_rdata[31]" which is output of PHY. (7)
     - If it is zero, Increment "DQS[3]" SDLL code by "1" and then go to "2" to update "DQS[3]" SDLL code.
     - If it is one, the previous "DQS[3]" SDLL code ("The current SDLL code - 1") will be the optimal SDLL code.

4. Configure PHY in normal mode after 4 to 7 are finished. (8)
   - Disable "wrlvl_mode" in PHY_CON0[16].

5. Memory Controller should configure Memory (DDR3, LPDDR3) in normal mode. (9)

14.3.6.2.2 CA Calibration

1. Controller should configure Memory (LPDDR3) in CA Calibration mode.

2. Configure PHY in CA Calibration mode.
   - Enable "wrlvl_mode" in PHY_CON0[16].
   - Enable "ca_cal_mode" in PHY_CON2[23].

3. How to find the optimal CA SDLL code. (=PHY_CON10[7:0])
   - Change CA SDLL code in PHY_CON10[7:0]. (1)
     - The start code value should be 0x8.
   - Update CA SDLL code in PHY_CON10[7:0]. (2)
     - Enable "ctrl_resync" in PHY_CON10[24]
     - Disable " ctrl_resync" in PHY_CON10[24]
   - CA to DQ mapping change to calibrate CA[3:0], CA[8:5]. (3)
     - Mode Register Write to MR#41 by Controller.
     - Memory Controller should disable "dfi_cke_p0" and "dfi_cke_p1". (dfi_cke_p0/p1=0)
   - Memory Controller should generate 1 cycle pulse of "dfi_cs_n_p0" with "dfi_address_p0 = 20'h3FF.
   - Memory Controller should read and save the value of "ctrl_io_rddata[15:0]" which is output of PHY.
     - CA[3:0] at rising edge CK (=CA_L[3:0]) is equal to
     - CA[8:5] at rising edge CK (=CA_L[8:5]) is equal to {ctrl_io_rdata[14], ctrl_io_rdata[12], ctrl_io_rdata[10], ctrl_io_rdata[8]}.
     - CA[3:0] at falling edge CK (=CA_H[3:0]) is equal to {ctrl_io_rdata[7], ctrl_io_rdata[5], ctrl_io_rdata[3], ctrl_io_rdata[1]}.
     - CA[8:5] at falling edge CK (=CA_H[8:5]) is equal to {ctrl_io_rdata[15], ctrl_io_rdata[13], ctrl_io_rdata[11], ctrl_io_rdata[9]}.
   - CA to DQ mapping change to calibrate CA[4], CA[9]. (4)
     - Memory Controller should enable "dfi_cke_p0" and "dfi_cke_p1". (dfi_cke_p0/p1=1)
     - Mode Register Write to MR#48 by Controller.
     - Memory Controller should disable "dfi_cke_p0" and "dfi_cke_p1". (dfi_cke_p0/p1=0)
   - Memory Controller should generate 1 cycle pulse of "dfi_cs_n_p0" with "dfi_address_p0 = 20'h3FF.
   - Memory Controller read and save the value of "ctrl_io_rddata[1:0]" and "ctrl_io_rddata[8:9]" which is output of PHY.
     - CA[4] at rising edge CK (=CA_L[4]) is equal to "ctrl_io_rddata[0]"
     - CA[9] at rising edge CK (=CA_L[9]) is equal to "ctrl_io_rddata[8]"
     - CA[4] at falling edge CK (=CA_H[4]) is equal to "ctrl_io_rddata[1]"
     - CA[9] at falling edge CK (=CA_H[9]) is equal to "ctrl_io_rddata[9]"

       - Check if "CA_L = 10'h3FF" and "CA_H = 10'h000" or not. (5)

- If not equaled,
  - Go to "6" until it searches for the leftmost code value. (7)
  - If it already saved the leftmost code value, save the current SDLL code by the rightmost code value (=VWMR). Go to "11". (10)
- If equaled,
  - If it is matched for the first time, save the current SDLL code by the leftmost code value (=VWML). Go to "6". (8)
  - Go to "6" until it searches for the rightmost code value. (9)
- Increment SDLL code by "1" and then go to "2" to update SDLL code. (6)

4. Calculate the optimal CA SDLL code (=PHY_CON10[7:0]). (11)
   - Calculate the optimal CA SDLL code (=VWMC) by the following formula.
   - VWMC = VWML + (VWMR - VWML)/2
   - Update CA SDLL code by using "VWMC".

5. Configure PHY in normal mode.
   - Disable "wrlvl_mode" in PHY_CON0[16].

6. Memory Controller should configure Memory (LPDDR3) in normal mode.

14.3.6.2.3 Gate Leveling

The goal of gate training is to locate the delay at which the initial read DQS rising edge aligns with the rising edge of the read DQS gate (=ctrl_gate_p0/p1). Once this point is identified, the read DQS gate can be adjusted prior to the DQS, to the approximate midpoint of the read DQS preamble. You can use "GATE Leveling" when using "DDR3 memory" over 800 MHz.

1. Controller should configure Memory (DDR3) in MPR mode. (Please refer to JEDEC Standard.)

2. Set "lpddr2_addr=20'h208" (=PHY_CON22[19:0]) to issue MR32 during GATE Leveling (LPDDR2/3)
   - In case of CA swap mode, lpddr2_addr=20'h041 to issue MR32 during GATE Leveling

3. Set Gate Leveling Mode.(1)
   - Enable "gate_cal_mode" in PHY_CON2[24]
   - Enable "ctrl_shgate" in PHY_CON0[8]
   - Set "ctrl_gateduradj[3:0] (=PHY_CON1[23:20]) in the following way.
     - 4'b0000" (DDR3, DDR2)
     - 4'b1011" (LPDDR3)
     - 4'b1001" (LPDDR2)

4. Memory Controller should assert "dfi_rdlvl_en" and "dfi_rdlvl_gate_en" to do read leveling. (2)

5. Memory Controller should wait until "dfi_rdlvl_resp" is set. (3)
   - The maximum waiting time will be 20 us. If the any command (the refresh or pre-charge command) is required within 20 us, please issue those commands before "(1)".

6. Memory Controller should deassert "dfi_rdlvl_en" and "dfi_rdlvl_gate_en" after "dfi_rdlvl_resp" is disabled.

7. Disable DQS pull down mode. (4)

8. Memory Controller should configure Memory (DDR3) in normal mode.

14.3.6.2.4 Read DQ Calibration (=Read Leveling, Read De-skewing)

Read DQ Calibration adjusts for the delays introduced by the package, board and on-chip that impact the read cycle.

1. In case of using DDR3 Memory,
   - Memory Controller should configure Memory in MPR mode. (Please refer to JEDEC Standard)
   - Set "PHY_CON1[15:0]" by "0xFF00" if "Pre-defined Data Pattern" is "[0x0000_0000, 0x0101_0101, 0x0000_0000, 0x0101_0101]" (byte_rdlvl_en=1)
   - Set "PHY_CON1[15:0]" by "0x0100" if "Pre-defined Data Pattern" is "[0x0000_0000, 0xFFFF_FFFF, 0x0000_0000, 0xFFFF_FFFF]" in MPR mode. (byte_rdlvl_en=1)

NOTE: Read DQ Calibration with "byte_rdlvl_en=0" should be done after Write DQ Calibration. Set "PHY_CON1[15:0]" by "0xFF00". "MPR Data Pattern" should be "[0x0000_0000, 0xFFFF_FFFF, 0x0000_0000, 0xFFFF_FFFF]".

2. In case of using LPDDR3 or LPDDR2 Memory,
   - Set "PHY_CON1[15:0]" by "0x00FF" if "MRR32 DQ Pattern" is "[0x0101_0101, 0x0000_0000, 0x0101_0101, 0x0000_0000]" (byte_rdlvl_en=1)
   - Set "PHY_CON1[15:0]" by "0x0001" if "MRR32 DQ Pattern" is "[0xFFFF_FFFF, 0x0000_0000, 0xFFFF_FFFF, 0x0000_0000]". (byte_rdlvl_en=1)

NOTE: Read DQ Calibration with "byte_rdlvl_en=0" should be done after Write DQ Calibration. Set "PHY_CON1[15:0]" by "0x00FF". "MRR32 DQ Pattern" should be "[0xFFFF_FFFF, 0x0000_0000, 0xFFFF_FFFF, 0x0000_0000]".

3. Set "lpddr2_addr=20'h208"(=PHY_CON22[19:0]) to issue MR32 during Calibration (LPDDR2/3)
   - In case of CA swap mode, lpddr2_addr=20'h041 to issue MR32 during Calibration.
     - Set Read Leveling Mode.(1)

4. Enable "rd_cal_mode" in PHY_CON2[25]
   - Memory Controller should assert "dfi_rdlvl_en" to do read leveling. (2)
   - Memory Controller should wait until "dfi_rdlvl_resp" is set. (3)

5. The maximum waiting time will be 20 us. If the any command (the refresh or pre-charge command) is required within 20 us, please issue those commands before "(1)".
   - Memory Controller should deassert "dfi_rdlvl_en" after "dfi_rdlvl_resp" is enabled. (4)
   - Memory Controller should configure Memory (DDR3) in normal mode.

14.3.6.2.5 Write DQ Calibration (=Write Deskewing)

Write DQ Calibration adjusts for the delays introduced by the package, board and on-chip that impact the write cycle.

1. Set Write Latency (WL) before Write Training(1)
   - Set "T_wrdata_en" by "WL" in PHY_CON26[20:16].
     - WL is defined as clock cycles between the write command and the first valid rising edge of DQS

2. Memory Controller should issue "Active Command".

3. PHY will keep writing and reading the pattern in "PHY_CON1[15:0]" for Write DQ Calibration according to the following settings.(2)
   - The column address should be defined in "lpddr2_addr" in PHY_CON22[19:0](LPDDR2, LPDDR3).
     - "lpddr2_addr[9:0]" correspond to CA[9:0] at the rising edge of CK, and "lpddr2_addr[19:10]" to CA[19:10] at the falling edge of CK.
     - It should be the "READ" command. For example, lpddr2_addr = 20'h5 if the column address is 11'h0 and bank address is 3'b000. In case of CA swap mode, lpddr2_addr = 20'h204 if the column address is 11'h0 and bank address is 3'b000.
   - The column address should be defined in "ddr3_addr" in PHY_CON24[15:0] (DDR3)
     - For example, if the column address (=ddr3_addr) is "0x0", PHY will write and read the pre-defined pattern (=PHY_CON1[15:0]) at 0x0, 0x4, 0x8 and 0xC for DQ Calibration. (BL=4)
   - In case of using LPDDR2 or LPDDR3 memory,
     - Set "PHY_CON1[15:0] = 0x0001" and "byte_rdlvl_en = 1"(=PHY_CON0[13])
     - Set "PHY_CON1[15:0] = 0x00FF" and "byte_rdlvl_en = 0"(=PHY_CON0[13]) for Deskewing.
   - In case of using DDR3 memory,
     - Set "PHY_CON1[15:0] = 0x0100" and "byte_rdlvl_en = 1"(=PHY_CON0[13])
     - Set "PHY_CON1[15:0] = 0xFF00" and "byte_rdlvl_en = 0"(=PHY_CON0[13]) for Deskewing.

4. Enable "p0_cmd_en" in PHY_CON[14].

5. Set Write Training Mode (3)
   - Enable "wr_cal_mode" in PHY_CON2[26].

6. Enable "wr_cal_start" in PHY_CON2[27] to do Write DQ Calibration. (4)

7. Memory Controller should wait until "dfi_rdlvl_resp" is set. (5)
   - The maximum waiting time will be 50us. If the any command (the refresh or pre-charge command) is required within 50us, please issue those commands before "(3)".

8. Disable "wr_cal_start" in PHY_CON2[27] after "dfi_rdlvl_resp" is enabled. (6)

14.3.7 DLL Lock and ZQ I/O Calibration

DLL Lock and ZQ I/O calibration should be done prior to the initialization of MCUA Bank Memory following System Power on.

14.3.7.1 Static Memory Map Shadow

Figure 14-5 Static Memory is composed of Static#0 to #1 (External Static Memory), Static#13 (Internal ROM) and NAND as Figure.

However, base address of internal ROM, and nSCS[0] is changed according to system boot mode. In internal ROM Boot Mode, base address of internal ROM is supposed to be exchanged with that of nSCS[0].

The previous Base Address remains in case of External Static Boot.

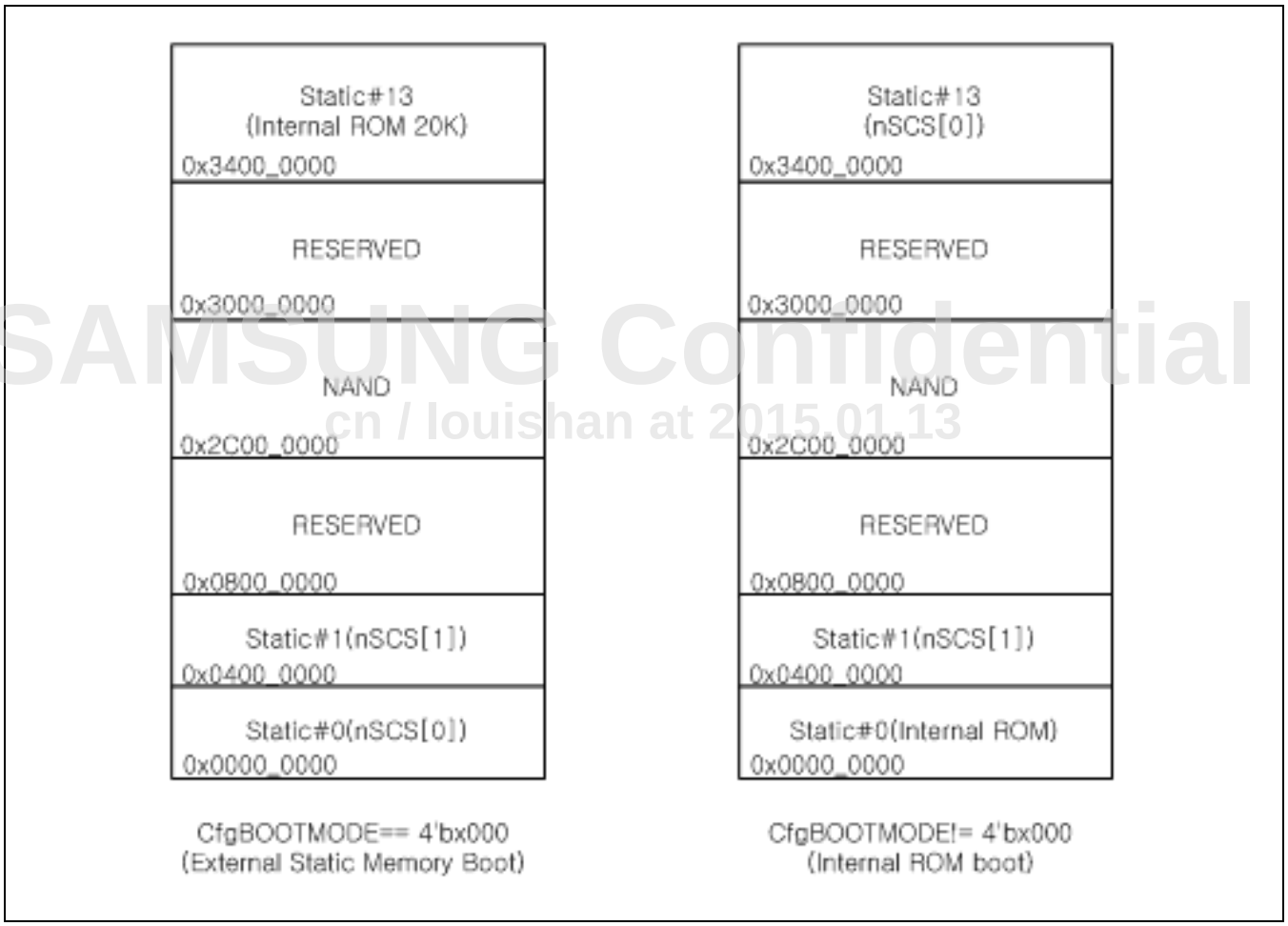


Figure 14-5 Static Memory Map Shadow

14.3.7.2 Interface

32-bit Data bus width SDRAM Interface of MCU-A Bank

MCU-A supports 32-bit data bus-width to CS[0] and CS[1] respectively.

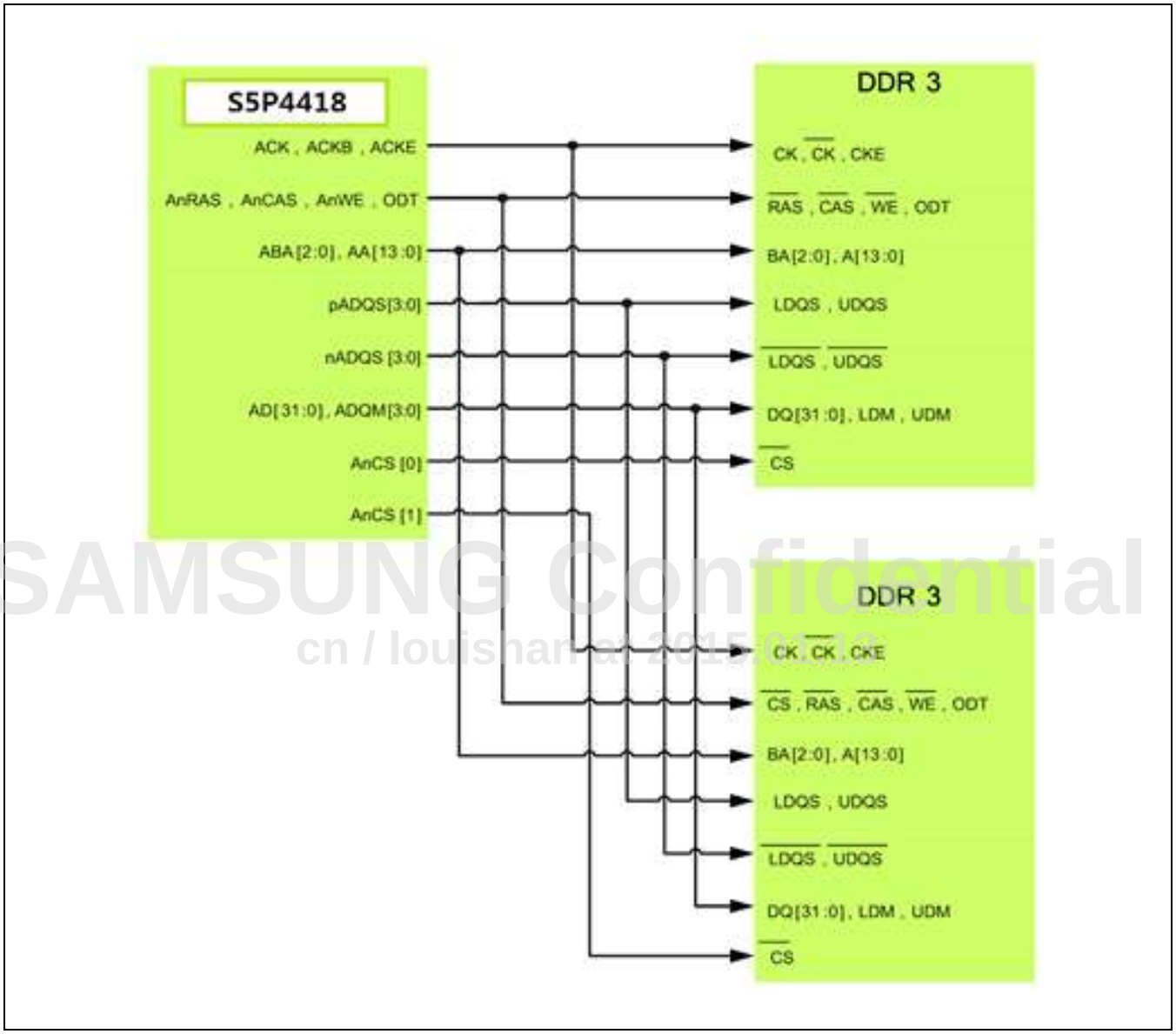


Figure 14-6 16-bit Data Bus width SDRAM Interface

16-bit Data bus width SDRAM Interface of MCU-A Bank

16-bit DDR3 SDRAM can add each two Memory to CS[0] and CS[1] respectively, which total four.

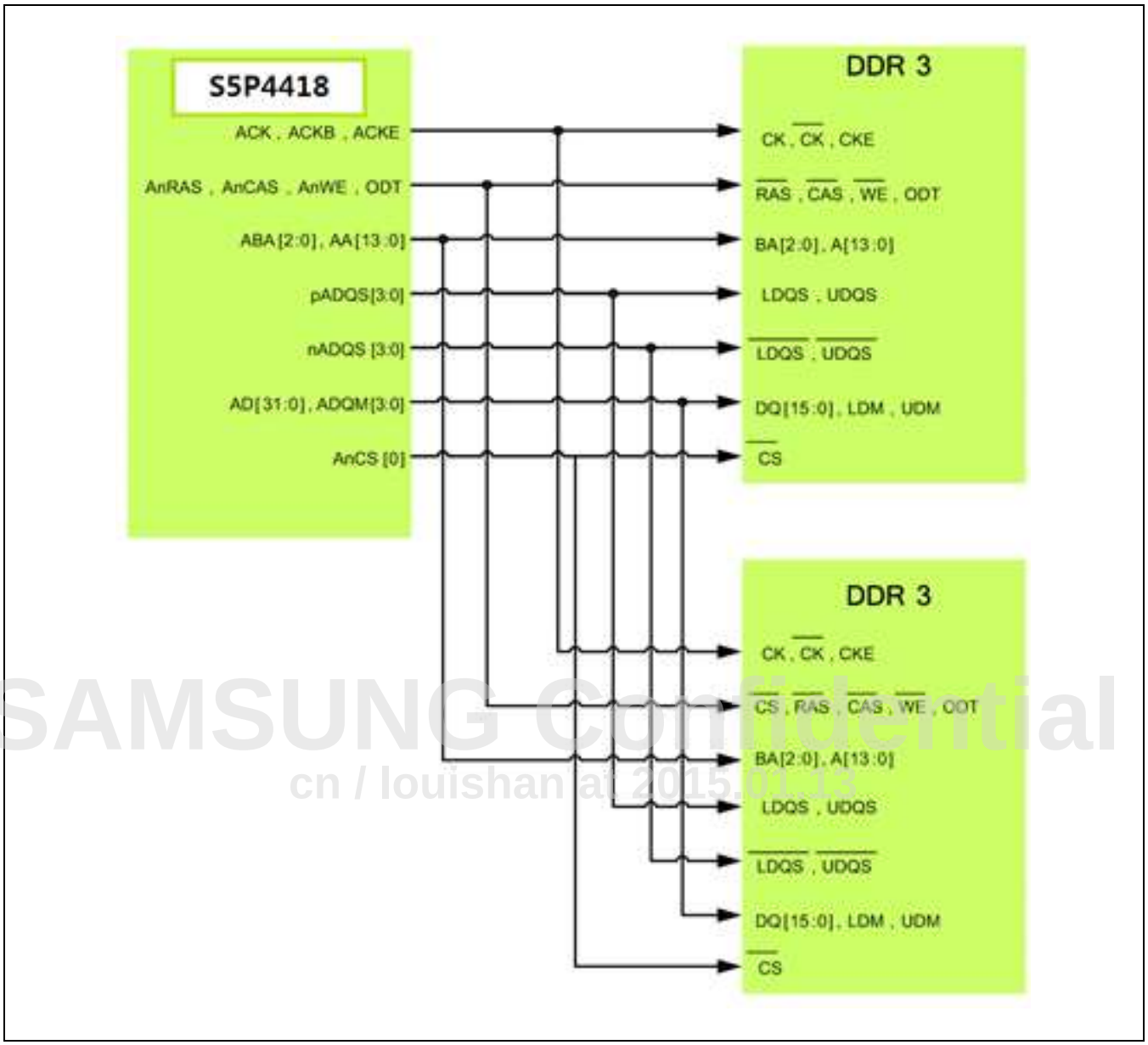


Figure 14-7 16-bit Data Bus width SDRAM Interface

14.3.8 NAND Overview

14.3.8.1 Normal Access Sequence

Read Cycle

- Write NAND Flash Command at NFCMD Register.
- Write Address to NFADDR Register with respect to NAND Flash Address Type. (Refer to NAND Flash data book)
- Check IRQPEND bit.
- Read ECC Data from NAND Flash Spare Array and Write ORGECC Register.
- Read Data (512/1024 byte) from NAND Flash Main Array.
- Check NFDecECCDone Register
- Check NFCheckError Register

Write Cycle

- Write NAND Flash Command to NFCMD Register. (Refer to NAND Flash data book)
- Access address of memory which tries to access to NFADDR Register by 3 to 5 time according to the sort of NAND Flash. (Refer to NAND Flash data book)
- Write data (512/1024 byte) through NFDATA Register.
- Check NFEncECCDone Register.
- Read the result of ECC through NFECC Register. (Small block only)
- Write NAND Flash Command to NFCMD Register. (Refer to NAND Flash data book)
- Check whether NAND Flash is ready or not by reading NFCONTROL.IRQPEND bit. (For the exact sequence of NAND Flash, Please refer to NAND Flash data book)

14.3.8.2 ECC (BCH)

Feature

- Hardware ECC generation, detection and indication (software correction) 4/8/16/24/40/60 bit error correction and detection
- Error Detection Code/Error Correction Code (EDC/ECC)
  NAND-based MLC flash has error weakness therefore error handling method is required. S5P4418 can perform EDC (error detecting codes) and ECC (error correction codes) and both based on BCH (Bose-Chadhuri-Hocquenghem) algorithm.EDC is run by hardware to reduce CPU overload and increase the CPU performance. In contrast, ECC is run by software. Parity bit is calculated on every 512/1024 byte page. Syndrome is calculated when each data is read from NAND flash and the value is used in error correction operation.
- Hardware ECC generation reset
  - This reset is asserted when NAND address or command register is written by any value.
  - This reset is also asserted when ECCRST bit (NFCONTROL register [11] bit) register is set to 1
  - This reset initializes NFECCL, NFECCH, NFCNT, NFECCSTATUS, NFSYNDRONE0 to 7 Registers.

14.4 Register Description

14.4.1 Register Map Summary

- Base Address: 0xC00E_0000 (DREX)

Register	Offset	Description	Reset Value
DREX			
ConControl	0x0000	Controller control register	0x0FFF_1100
MemControl	0x0004	Memory control register	0x0020_2601
MemConfig0	0x0008	Memory chip0 configuration register	0x0000_1312
MemConfig1	0x000C	Memory chip1 configuration register	0x0000_1312
DirectCmd	0x0010	Memory direct command register	0x0000_0000
PrechConfig	0x0014	Pre-charge policy configuration register	0xFF00_0000
PhyControl0	0x0018	PHY control0 register	0x0000_0000
RSVD	0x001C to 0x0024	Reserved	0x0000_0000
PwrdnConfig	0x0028	Dynamic power down configuration register	oxFFFF_00FF
TimingPZQ	0x002C	AC timing register for periodic ZQ(ZQCS) of memory	0x0000_4084
TimingAref	0x0030	AC timing register for auto refresh of memory	0x0000_005D
TimingRow	0x0034	AC timing register for the row of memory	0x1F23_3286
TimingData	0x0038	AC timing register for the data of memory	0x1230_360C
TimingPower	0x003C	AC timing register for the power modes of memory	0x381B_0422
PhyStatus	0x0040	PHY status register	0x0000_0000
RSVD	0x0044	Reserved	0x0000_0000
ChipStatus	0x0048	Memory chipstatus register	0x0000_0000
RSVD	0x004C to 0x0050	Reserved	0x0000_0000
MrStatus	0x0054	Memory mode registers status register	0x0000_0000
RSVD	0x0058 to 0x005C	Reserved	0x0000_0000
QosControl n	0x0060 to 0x00D8	Quality of service control register n	0x0000_0FFF
RSVD	0x00DC to 0x00F0	Reserved	0x0000_0000
WrTraConfig	0x00F4	Write training configuration register	0x0000_0000
RdlvlConfig	0x00F8	Read leveling configuration register	0x0000_0000
RSVD	0x00FC	Reserved	0x0000_0000

Register	Offset	Description	Reset Value
BRBRSVCONTROL	0x0100	BRB reservation control register	0x0000_0000
BRBRSVCONFIG	0x0104	BRB reservation configuration register	0x8888_8888
BRBQOSCONFIG	0x0108	BRB QoS configuration register	0x0000_0010
MemBaseConfig0	0x010C	Memory chip0 base configuration register	0x0020_07F8
MemBaseConfig1	0x0110	Memory chip1 base configuration register	0x0020_07F8
RSVD	0x0114 to 0x011C	Reserved	0x0000_0000
WRLVLCONFIG0	0x0120	Write leveling configuration register0	0x0000_0010
WRLVLCONFIG1	0x0124	Write leveling configuration register1	0x0000_0000
WRLVLSTATUS	0x0128	Write leveling status register	0x0000_0000
RSVD	0x012C to 0x014C	Reserved	0x0000_0000
CTRL_IO_RDATA	0x0150	CTRL_IO_RDATA register	0x0000_0000
RSVD	0x0154 to 0x015C	Reserved	0x0000_0000
CACAL_CONFIG0	0x0160	CA calibration configuration register0	0x003F_F010
CACAL_CONFIG1	0x0164	CA calibration configuration register1	0x0000_0000
CACAL_STATUS	0x0168	CA calibration status register	0x0000_0000

- Base Address: 0xC00E_1000 (DDRPHY)

Register	Offset	Description	Reset Value
DDRPHY			
PHY_CON0	0x1000	PHY Control Register 0	0x1702_0240
PHY_CON1	0x1004	PHY Control Register 1	0x0921_0100
PHY_CON2	0x1008	PHY Control Register 2	0x0001_0000
PHY_CON3	0x100C	GATE SDLL Code Control Register 0	0x0001_0842
PHY_CON4	0x1010	READ SDLL Code Control Register 0	0x0808_0808
PHY_CON5	0x1014	READ Mode Control Register	0x0000_0000
PHY_CON6	0x1018	WRITE SDLL Code Control Register 0	0x0808_0808
RSVD	0x101C	Reserved	0x0000_0000
PHY_CON8	0x1020	GATE SDLL Code Control Register 1	0x0000_0000
PHY_CON9	0x1024	GATE SDLL Code Control Register 2	0x0000_0000
PHY_CON10	0x1028	CMD SDLL Code Control Register	0x0000_0008
RSVD	0x102C	Reserved	0x0000_0000
PHY_CON12	0x1030	MDLL Control Register 0	0x1010_0070
PHY_CON13	0x1034	MDLL Control Register 1	-
PHY_CON14	0x1038	Low Power Control Register	0x001F_0000
PHY_CON15	0x103C	Feedback Test Control Register	0x0000_0000
PHY_CON16	0x1040	ZQ Control Register	0x0800_0304
PHY_CON17	0x1048	ZQ Status Register	-
PHY_CON18	0x104C	Read Leveling Status Register 0	0x0055_5555
PHY_CON19	0x1050	Read Leveling Status Register 1	-
PHY_CON20	0x1054	Read Leveling Status Register 2	-
PHY_CON21	0x1058	Read Leveling Status Register 3	-
PHY_CON22	0x105C	Read Leveling Control Register 0	0x0000_0208
PHY_CON23	0x1060	Read Leveling Control Register 1	0x0000_03FF
PHY_CON24	0x1064	Read Leveling Control Register 2	0x0000_0000
PHY_CON25	0x1068	Read Leveling Control Register 3	0x105E_107E
PHY_CON26	0x106C	Read Leveling Control Register 4	0x0008_107F
PHY_CON27	0x1070	PHY Control Register 27	-
PHY_CON28	0x1074	Read Leveling Status Register 4	-
PHY_CON29	0x1078	Version Information Register	0x0501_0203
PHY_CON30	0x107C	Write Leveling Control Register	0x0000_0000
PHY_CON31	0x1080	CA De-skew Control Register 0	0x0000_0000
PHY_CON32	0x1084	CA De-skew Control Register 1	0x0000_0000
PHY_CON33	0x1088	CA De-skew Control Register 2	0x0000_0000
PHY_CON34	0x108C	CA De-skew Control Register 3	0x0000_0000

Register	Offset	Description	Reset Value
RSVD	0x1090 to 0x1094	Reserved	0x0000_0000
PHY_CON37	0x1098	CMD De-skew Control Register 1	0x0000_0000
RSVD	0x109C	Reserved	0x0000_0000
PHY_CON39	0x10A0	Driver Strength Control Register	0x0000_0000
PHY_CON40	0x10A4	ZQ Divider Control Register	0x0000_0007
PHY_CON41	0x10A8	ZQ Timer Control Register	0x0000_00F0
PHY_CON42	0x10AC	PHY Control Register 3	0x0000_0000

- Base Address: 0xC005_1000 (MCUS_ADDR)

Register	Offset	Description	Reset Value
MCUS_ADDR			
MEMBW	0x1000	Memory bus width register	Note
MEMTIMEACSL	0x1004	Memory timing for TACS low register	Note
MEMTIMEACSH	0x1008	Memory timing for TACS high register	0x0000_0000
MEMTIMECOSL	0x100C	Memory timing for TCOS low register	Note
MEMTIMECOSH	0x1010	Memory timing for TCOS high register	0x0000_0000
MEMTIMEACC0	0x1014	Memory timing for TACC 0 register	Note
RSVD	0x1018	Reserved	-
RSVD	0x101C	Reserved	-
MEMTIMEACC3	0x1020	Memory timing for TACC 3 register	0x0000_0000
MEMTIMESACC0	0x1024	Memory timing for TSACC 0 register	0x0000_0000
RSVD	0x1028	Reserved	-
RSVD	0x102C	Reserved	-
MEMTIMESACC3	0x1030	Memory timing for TSACC 3 register	0x0000_0000
RSVD	0x1034 to 0x1040	Reserved	0x0000_0000
MEMTIMECOHL	0x1044	MEMORY TIMING FOR TCOH low register	Note
MEMTIMECOHH	0x1048	MEMORY timing for TCOH high register	0x0000_0000
MEMTIMECAHL	0x104C	MEMORY timing for TCAH low register	Note
MEMTIMECAHH	0x1050	MEMORY timing for TCAH high register	0x0000_0000
MEMBURSTL	0x1054	MEMORY burst control low register	0x0000_0010
RSVD	0x1058	Reserved	-
MEMWAIT	0x105C	Memory wait control register	0x0000_0000
RSVD	0x1060 to 0x1084	Reserved	-
NFCONTROL	0x1088	NAND flash control register	Note
NFECCTRL	0x108C	NAND ECC control register	0x0000_0000
NFCNT	0x1090	NAND flash data count register	0x0000_0000
NFECCSTATUS	0x1094	NAND flash ECC status register	0x0000_0000
NFTIMEACS	0x1098	NAND timing for TACS register	0x0000_0007
NFTIMECOS	0x109C	NAND timing for TCOS register	0x0000_0007
NFTIMEACC0	0x10A0	NAND timing for TACC0 register	0x0000_000F
RSVD	0x10A4	Reserved	-
NFTIMEOCH	0x10A8	NAND timing for TOCH register	0x0000_0007

Register	Offset	Description	Reset Value
NFTIMECAH	0x10AC	NAND timing for TCAH register	0x0000_0007
NFECC0 ~ NFECC26	0x10B0 to 0x1118	NAND flash ECC 0 ~ 26 register	0x0000_0000
NFORGECC0 ~ NFORGECC26	0x111C to 0x1184	NAND flash origin ECC 0~26 register	0x0000_0000
NFSYNDROME0 ~ NFSYNDROME29	0x1188 to 0x11FC	NAND flash ECC syndrome value 0~29 register	0x0000_0000
NFELP0 ~ NFELP59	0x1200 to 0x1274	NAND flash ECC ELP value 0 ~ 59 register	-
NFERRORLOCATION0 ~ NFERRORLOCATION59	0x1278 to 0x12EC	NAND flash error location 0 ~ 59 register	-
AUTOSYND	0x12F0	AUTO SYNDROM REGISTER	0x0000_0000
NFWSYNDRONE0 ~ NFWSYNDRONE29	0x12F4 to 0x1368	NAND flash ECC write syndrome value 0~29 register	0x0000_0000

- Base Address: 0x2C00_0000 (MCUS_ADDR)

Register	Offset	Description	Reset Value
NFDATA	0x0000	NAND flash data register	–
NFCMD	0x0010	NAND flash command register	–
NFADDR	0x0018	NAND flash address register	–

14.4.1.1 DREX Register

14.4.1.1.1 ConControl

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0000, Reset Value = 0x0FFF_1100

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	–	Reserved (Should be zero)	0x0
dfi_init_start	[28]	RW	DFI PHY initialization start This field is used to initialize DFI PHY. Set this field to 1 to initialize DFI PHY and set this field to 0 after received dfi_init_complete of PhyStatus register.	0x0
timeout_level0	[27:16]	RW	Default Timeout Cycles This counter prevents transactions in the AXI request FIFO from starvation. This counter starts if a new AXI transaction comes into the request FIFO. If the counter becomes zero, the corresponding FIFO has the highest priority during BRB arbitration. Refer to Section 1.7. Quality of Service for de-tailed information	0xFFF
RSVD	[15]	–	Reserved (Should be zero)	0x0
rd_fetch	[14:12]	RW	Read Data Fetch Cycles 0xn = n MBCLK cycles (MBCLK : DREX-1 core clock) The recommended value of this field is 0x2 for LPDDR3 800 MHz memory clock and other cases are 0x1. This register is for the unpredictable latency of read data coming from memory devices by tDQSCK variation or the board flying time. The read fetch delay of PHY read FIFO must be controlled by this parameter. The controller will fetch read data from PHY after read_latency + n MBCLK cycles. Refer to Section 1.3 for detailed information.	0x1
RSVD	[11:9]	–	Reserved (Should be zero)	0x0
empty	[8]	R	Empty Status 0x0 = Not Empty, 0x1 = Empty There is no AXI transaction in memory controller.	0x1
RSVD	[7:6]	–	Reserved (Should be zero)	0x0
aref_en	[5]	RW	Auto Refresh Counter 0x0 = Disable, 0x1 = Enable Enable this to decrease the auto refresh counter by 1 at the rising edge of the MPCLK	0x0
RSVD	[4]	–	Reserved (Should be zero)	0x0
io_pd_con	[3]	RW	I/O Power down Control in Low Power Mode(through LPI) 0x0 : Use programmed ctrl_pd and pull down control 0x1 : Automatic control for ctrl_pd and pull down control	0x0

Name	Bit	Type	Description	Reset Value
			If this value is set to 0x1 and in low power mode through LPI, DREX-1 automatically sets power down enable for input buffer of I/O and pull down disable for dq and dqs in power down mode If this value is set to 0x0, DREX-1 only sends programmed ctrl_pd value and pull down control.	
clk_ratio	[2:1]	RW	Clock Ratio of Bus Clock to Memory Clock 0x0 = freq.(MBCLK): freq.(MBCLK) = 1: 1, 0x1 to 0x3 = Reserved	0x0
RSVD	[0]	–	Reserved (Should be zero)	0x0

14.4.1.1.2 MemControl

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0004, Reset Value = 0x00202601

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	–	Reserved (Should be zero)	0x0
mrr_byte	[26:25]	RW	Mode Register Read byte lane location 0x0 = memory dq[7:0] 0x1 = memory dq[15:8] 0x2 = memory dq[23:16] 0x3 = memory dq[31:24]	0x0
pzq_en	[24]	RW	DDR3 periodic ZQ (ZQCS) enable NOTE: That after exit from self refresh, ZQ function is required by the software. The controller does not support ZQ calibration command to be issued in parallel to DLL lock time when coming out of self refresh. Turn-on only when using DDR3. The periodic ZQ interval is defined by t_pzq in TIMINGPZQ register.	0x0
RSVD	[23]	–	Reserved (Should be zero)	0x0
bl	[22:20]	RW	Memory Burst Length 0x0 to 1 = Reserved, 0x2 = 4, 0x3 = 8, 0x4 to 0x7 = Reserved In case of LPDDR2-S4, the controller only supports burst length 4. In case of DDR3 and LPDDR3, the controller only supports burst length 8.	0x2
num_chip	[19:16]	RW	Number of Memory Chips 0x0 = 1 chip, 0x1 = 2 chips, 0x2 to 0xf = Reserved	0x0
mem_width	[15:12]	RW	Width of Memory Data Bus 0x0 to 0x1 = Reserved, 0x2 = 32-bit, 0x3 to 0xf= Reserved	0x2
mem_type	[11:8]	RW	Type of Memory 0x0 to 0x4 = Reserved, 0x5 = LPDDR2-S4, 0x6 = DDR3, 0x7 = LPDDR3, 0x8 to 0xf = Reserved	0x6
add_lat_pall	[7:6]	RW	Additional Latency for PALL in MBCLK cycle 0x0 = 0 cycle,	0x0

Name	Bit	Type	Description	Reset Value
			0x1 = 1 cycle 0x2 = 2 cycle, 0x3 = Reserved If all banks pre-charge command is issued, the latency of pre-charging will be tRP + add_lat_pall	
dsref_en	[5]	RW	Dynamic Self Refresh 0x0 = Disable, 0x1 = Enable Refer to Section 1.5.2. Dynamic power down for detailed information. In DDR3, this feature is not supported. This feature must be turn-off when using DDR3.	0x0
tp_en	[4]	RW	Timeout Pre-charge 0x0 = Disable, 0x1 = Enable If tp_en is enabled, it automatically pre-charges an open bank after a specified amount of mclk cycles (if no access has been made in between the cycles) in an open page policy. If Prech-Config.tp_cnt bit-field is set, it specifies the amount of mclk cycles to wait until timeout pre-charge pre-charges the open bank. Refer to Section 1.6.2. Timeout pre-charge for detailed information.	0x0
dpwrdn_type	[3:2]	RW	Type of Dynamic Power Down 0x0 = Active/pre-charge power down, 0x1 = Forced pre-charge power down 0x2 to 0x3 = Reserved Refer to Section 1.5.2. Dynamic power down for detailed information.	0x0
dpwrdn_en	[1]	RW	Dynamic Power Down 0x0 = Disable, 0x1 = Enable	0x0
clk_stop_en	[0]	RW	Dynamic Clock Control 0x0 = Always running, 0x1 = Stops during idle periods This feature is only supported with LPDDR2/LPDDR3. Refer to Section 1.5.4. Clock stop for detailed information.	0x1

14.4.1.1.3 MemConfig0

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0008, Reset Value = 0x0000_1312

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved (Should be zero)	0x0
chip_map	[15:12]	RW	Address Mapping Method (AXI to Memory) 0x0 = Linear ({bank, row, column, width}), 0x1 = Interleaved ({row, bank, column, width}), 0x2 to 0xf = Reserved	0x1
chip_col	[11:8]	RW	Number of Column Address Bits 0x0 = Reserved, 0x1 = Reserved, 0x2 = 9 bits, 0x3 = 10 bits, 0x4 = Reserved, 0x5 to 0xf = Reserved	0x3
chip_row	[7:4]	RW	Number of Row Address Bits 0x0 = 12 bits, 0x1 = 13 bits, 0x2 = 14 bits, 0x3 = 15 bits, 0x4 = 16 bits, 0x5 to 0xf = Reserved	0x1
chip_bank	[3:0]	RW	Number of Banks 0x0 = Reserved, 0x1 = Reserved, 0x2 = 4 banks, 0x3 = 8 banks, 0x4 to 0xf = Reserved	0x2

14.4.1.1.4 MemConfig1

- Base Address: 0xC00E_0000
- Address = Base Address + 0x000C, Reset Value = 0x0000_1312

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved (Should be zero)	0x0
chip_map	[15:12]	RW	Address Mapping Method (AXI to Memory) 0x0 = Linear ({bank, row, column, width}), 0x1 = Interleaved ({row, bank, column, width}), 0x2 to 0xf = Reserved	0x1
chip_col	[11:8]	RW	Number of Column Address Bits 0x0 = Reserved, 0x1 = Reserved, 0x2 = 9 bits, 0x3 = 10 bits, 0x4 = Reserved, 0x5 to 0xf = Reserved	0x3
chip_row	[7:4]	RW	Number of Row Address Bits 0x0 = 12 bits, 0x1 = 13 bits, 0x2 = 14 bits, 0x3 = 15 bits, 0x4 = 16 bits, 0x5 to 0xf = Reserved	0x1
chip_bank	[3:0]	RW	Number of Banks 0x0 = Reserved, 0x1 = Reserved, 0x2 = 4 banks, 0x3 = 8 banks, 0x4 to 0xf = Reserved	0x2

14.4.1.1.5 DirectCmd

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0010, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	–	Reserved (Should be zero)	0x0
cmd_type	[27:24]	RW	Type of Direct Command 0x0 = MRS/EMRS (mode register setting), 0x1 = PALL (all banks pre-charge), 0x2 = PRE (per bank pre-charge), 0x3 = DPD (deep power down), 0x4 = REFS (self refresh), 0x5 = REFA (auto refresh), 0x6 = CKEL (active/pre-charge power down), 0x7 = NOP (exit from active/pre-charge power down or deep power down, 0x8 = REFSX (exit from self refresh), 0x9 = MRR (mode register reading), 0xa = ZQINIT (ZQ calibration init.) 0xb = ZQOPER (ZQ calibration long) 0xc = ZQCS (ZQ calibration short) 0xd to 0xf = Reserved When a direct command is issued, AXI masters must not access memory. It is strongly recommended to check the command queue's state by ConControl.chip0/1_empty and the chip FSM in the ChipStatus register before issuing a direct command. The chip status must be checked before issuing a direct command. And clk_stop_en, dynamic power down, dynamic self refresh, force pre-charge function (MemControl register) and sl_dll_dyn_con (PhyControl0 register) must be disabled. MRS/EMRS or MRR commands should be issued if all banks are in idle state. If MRS/EMRS or MRR is issued to LPDDR2-S4/LPDDR3, the CA pins must be mapped as follows. MA[7:0] = {cmd_addr[1:0], cmd_bank[2:0], cmd_addr[12:10]}, OP[7:0] = cmd_addr[9:2] In DDR3, self refresh related timing such as tCKESR/tCKSRE/tCKSRX should be check by software. NOTE: That do not write reserved value to this field.	0x0
Reserved	[23:21]	–	Reserved (Should be zero)	0x0
cmd_chip	[20]	RW	Chip Number to send the direct command to 0 = Chip 0 1 = Chip 1	0x0

Name	Bit	Type	Description	Reset Value
RSVD	[19]	–	Reserved (Should be zero)	0x0
cmd_bank	[18:16]	RW	Related Bank Address when issuing a direct command To send a direct command to a chip, additional information such as the bank address is required. This register is used in such situations	0x0
cmd_addr	[15:0]	RW	Related Address value when issuing a direct command To send a direct command to a chip, additional information such as the address is required. This register is used in such situations.	0x0

14.4.1.1.6 PrechConfig

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0014, Reset Value = 0xFF00_0000

Name	Bit	Type	Description	Reset Value
tp_cnt	[31:24]	RW	Timeout Pre-charge Cycles 0xn = n MBCLK cycles, The minimum vlaue of this field is 0x2 If the timeout pre-charge function (MemControl.tp_en) is enabled and the timeout pre-charge counter becomes zero, the controller forces the activated memory bank into the pre-charged state. Refer to Section 1.6.2 .Timeout pre-charge for detailed information.	0xFF
RSVD	[23:16]	–	Reserved (Should be zero)	0x0
chip1_policy	[15:8]	RW	Memory Chip1 Pre-charge Bank Selective Policy 0x0 = Open page policy, 0x1 = Close page (auto pre-charge) policy chip1_policy[n], n is the bank number of chip1. Open Page Policy: After a READ or WRITE, the row that was accessed is left open. Close Page (Auto Pre-charge) Policy: Right after a READ or WRITE command, memory devices automatically pre-charges the bank. This is a bank selective pre-charge policy. For example, if chip1_policy[2] is 0x0, bank2 of chip1 has an open page policy and if chip1_policy[6] is 0x1, bank6 of chip1 has a close page policy. Refer to Section 1.6.1. Bank Selective Pre-charge for detailed information.	0x0
chip0_policy	[7:0]	RW	Memory Chip0 Pre-charge Bank Selective Policy 0x0 = Open page policy, 0x1 = Close page (auto pre-charge) policy Chip0_policy[n], n is the bank number of chip0. This is for memory chip0.	0x0

14.4.1.1.7 PhyControl0

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
mem_term_en	[31]	RW	Termination Enable for Memory At high-speed memory operation, it can be necessary to turn on termination resistance in memory devices. This register control s an ODT pin of a memory device.	0x0
phy_term_en	[30]	RW	Termination Enable for PHY At high-speed memory operation, it can be necessary to turn on termination resistance in the PHY.	0x0
ctrl_shgate	[29]	–	Duration of DQS Gating Signal This field controls the gate control signal In LPDDR2-S4/LPDDRD3, this field should be 1"b0 regard-less of clock frequency. In DDR3, according to memory clock, set the value like be-low. 1"b0 = (gate signal length = "burst length / 2" (<= 200MHz)) 1"b1 = (gate signal length = "burst length / 2" - 1 (> 200MHz))	0x0
ctrl_pd	[28:24]	RW	Input Gate for Power Down If this field is set, input buffer is off for power down. This field should be 0 for normal operation. Ctrl_pd[3:0] = for each data slice, Ctrl_pd[4] = for control slice.	0x0
RSVD	[23:7]	–	Reserved (Should be zero)	0x0
dqs_delay	[6:4]	RW	Delay Cycles for DQS Cleaning This register is to enable PHY to clean incoming DQS signals delayed by external circumstances. If DQS is coming with read latency plus n memory clock cycles, this registers must be set to n memory clock cycles.	0x0
fp_resync	[3]	RW	Force DLL Re-synchronization	0x0
RSVD	[2]	–	Reserved (Should be zero)	0x0
sl_dll_dyn_con	[1]	RW	Turn On PHY Slave DLL Dynamically 0 = Disable, 1 = Enable	0x0
mem_term_chips	[0]	RW	Memory termination between chips 0 = Disable, 1 = Enable This field is only valid when num_chip is 0x1(2 chips) in MemControl register and DDR3.	0x0

14.4.1.1.8 PwrdnConfig

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0028, Reset Value = 0xFFFF_00FF

Name	Bit	Type	Description	Reset Value
dsref_cyc	[31:16]	RW	Number of Cycles for dynamic self refresh entry 0xn = n MBCLK cycles, The minimum value of this field is 0x2. If the command queue is empty for n+1 cycles, the controller forces memory devices into self refresh state. Refer to Section 1.5.3. Dynamic self refresh for detailed information.	0xFFFF
RSVD	[15:8]	–	Reserved (Should be zero)	0x0
dpwrdn_cyc	[7:0]	RW	Number of Cycles for dynamic power down entry 0xn = n MBCLK cycles, The minimum value of this field is 0x2. If the command queue is empty for n+1 cycles, the controller forces the memory device into active/pre-charge power down state. Refer to Section 1.5.2. Dynamic power down for detailed information.	0xFF

14.4.1.1.9 TimingPZQ

- Base Address: 0xC00E_0000
- Address = Base Address + 0x002C, Reset Value = 0x0000_4084

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved (Should be zero)	0x0
t_pzq	[23:0]	RW	Average Periodic ZQ Interval(Only in DDR3) tREFI(t_refi T(MPCLK)) t_pzq should be less than or equal to the minimum value of memory periodic ZQ interval, for example, if MPCLK frequency is 12 MHz, t_refi is set to 93 and ZQ interval is 128ms then the following value should be programmed into it: 128 ms * 12 MHz / 93 = 16516 The minimum value is 2.	0x4084

14.4.1.1.10 TimingAref

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0030, Reset Value = 0x0000_005D

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved (Should be zero)	0x0
t_refi	[15:0]	RW	Average Periodic Refresh Interval t_refi * T(MPCLK) should be less than or equal to the minimum value of memory tREFI (all bank), for example, for the all bank refresh period of 7.8us, and an MPCLK frequency of 12 MHz, the following value should be programmed into it: 7.8 us * 12 MHz = 93	0x5D

14.4.1.1.11 TimingRow

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0034, Reset Value = 0x1F23_3286

Name	Bit	Type	Description	Reset Value
t_rfc	[31:24]	RW	Auto refresh to Active / Auto refresh command period, in MBCLK cycles t_rfc * T(MBCLK) should be greater than or equal to the minimum value of memory tRFC and the minimum value is 17 if PHY is running with dll on. In FPGA with low frequency and dll is off, the minimum value is 3.	0x1F
t_rrd	[23:20]	RW	Active bank A to Active bank B delay, in MBCLK cycles t_rrd * T(MBCLK) should be greater than or equal to the minimum value of memory tRRD. The minimum value is 2.	0x2
t_rp	[19:16]	RW	Pre-charge command period, in MBCLK cycles t_rp * T(MBCLK) should be greater than or equal to the minimum value of memory tRP. The minimum value is 2.	0x3
t_rcd	[15:12]	RW	Active to Read or Write delay, in MBCLK cycles t_rcd * T(MBCLK) should be greater than or equal to the minimum value of memory tRCD + T(MBCLK)/2. For example, tRCD in memory specification is 13.75ns and MBCLK is 3.0ns, t_rcd * 3ns >= 13.75ns + 1.5ns The right value for t_rcd is 6. The minimum value is 2.	0x3
t_rc	[11:6]	RW	Active to Active period, in MBCLK cycles t_rc * T(MBCLK) should be greater than or equal to the minimum value of memory tRC. The minimum value is 2.	0xA

Name	Bit	Type	Description	Reset Value
t_ras	[5:0]	RW	Active to Pre-charge command period, in MBCLK cycles t_ras * T(MBCLK) should be greater than or equal to the minimum value of memory tRAS + T(MBCLK)/2. For example, tRAS in memory specification is 35ns and MBCLK is 3.0ns. t_ras * 3ns >= 35ns + 1.5ns The right value for t_ras is 13. The minimum value is 2.	0x6

14.4.1.1.12 TimingData

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0038, Reset Value = 0x1230_360C

Name	Bit	Type	Description	Reset Value
t_wtr	[31:28]	RW	Internal write to Read command delay, in MBCLK cycles t_wtr * T(MBCLK) should be greater than or equal to the minimum value of memory tWTR In LPDDR2-S4/LPDDR3 t_wtr is max(2tCK, tWTR) andIn DDR3 t_wtr is max(4tCK, tWTR). And then this value should be changed in MBCLK cycles. The minimum value is 2.	0x1
t_wr	[27:24]	RW	Write recovery time, in MBCLK cycles t_wr * T(MBCLK) should be greater than or equal to the minimum value of memory tWR. The minimum value is 2.	0x2
t_rtp	[23:20]	RW	Internal read to Pre-charge command delay, in MBCLK cycles t_rtp * T(MBCLK) should be greater than or equal to the minimum value of memory tRTP. The minimum value is 2.	0x3
RSVD	[19:17]	RW	Reserved (Should be zero)	0x0
t_w2w_c2c	[16]	RW	Additional Write to Write delay in chip to chip case in MBCLK cycles. If mem_term_en of PhyControl0 register (offset addr = 0x18) is enabled, then this value will be set to 1 automatically.	0x0
t_r2r_c2c	[15]	RW	Additional Read to Read delay in chip to chip case in MBCLK cycles. If mem_term_chips of PhyControl0 register (offset addr = 0x18) is enabled, then this value will be set to 1 automatically.	0x0
dqsck	[14:12]	–	tDQSCK in memory clock cycles In DDR3, this field should set to 0. In LPDDR2/3, this field should be set to RU (tDQSCK max/tCK). tDQSCK max is 5.5ns in LPDDR2/3.	0x3
wl	[11:8]	RW	Write data latency (for LPDDR2-S4/LPDDR3/DDR3), in memory clock cycles wl should be greater than or equal to the minimum value of memory WL. There is no restriction with LPDDR2-S4 but there is restriction with LPDDR3 and DDR3 like below. In LPDDR3, the minimum wl is 5 and in DDR3, the minimum wl is 6.	0x6
RSVD	[7:4]	–	Reserved (Should be zero)	0x0

Name	Bit	Type	Description	Reset Value
rl	[3:0]	RW	Read data latency (for LPDDR2-S4/LPDDR3/DDR3), in memory clock cycles rl should be greater than or equal to the minimum value of memory RL	0xC

14.4.1.1.13 TimingPower

- Base Address: 0xC00E_0000
- Address = Base Address + 0x003C, Reset Value = 0x381B_0422

Name	Bit	Type	Description	Reset Value
t_faw	[31:26]	RW	Four Active Window(for LPDDR2-S4/LPDDR3/DDR3) t_faw * T(MBCLK) should be greater than or equal to the minimum value of memory tFAW. The minimum value is 2.	0xE
t_xsr	[25:16]	RW	Self refresh exit power down to next valid command delay, in cycles t_xsr * T(MBCLK) should be greater than or equal to the minimum value of memory tXSR. In DDR3, this value should be set to tXSDLL. The minimum value is 2.	0x1B
t_xp	[15:8]	RW	Exit power down to next valid command delay, in cycles t_xp * T(MBCLK) should be greater than or equal to the minimum value of memory tXP In DDR3, this value should set to tXPDLL. In DDR3 even though “fast exit” is programmed in MRS, tXPDLL is applied. In DDR3, tXPDLL is likely Max. (10nCK, 24ns). So note that t_xp should set to Max. (5nMBCLK, 24ns/MBCLK period). The minimum value is 2.	0x4
t_cke	[7:4]	RW	CKE minimum pulse width (minimum power down mode duration), in cycles t_cke should be greater than or equal to the minimum value of memory tCKE. The minimum value is 2.	0x2
t_mrd	[3:0]	RW	Mode Register Set command period, in cycles t_mrd should be greater than or equal to the minimum value of memory tMRD In DDR3, this parameter should be set to tMOD value. The minimum value is 2.	0x2

14.4.1.1.14 PhyStatus

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0040, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved (Should be zero)	0x0
rdlvl_complete	[14]	R	Read Level Completion	0x0
RSVD	[13:4]	R	Reserved (Should be zero)	0x0
dfi_init_complete	[3]	R	DFI PHY initialization complete 0 = Initialization has not been finished 1 = Initialization has been finished	0x0
RSVD	[2:0]	R	Reserved (Should be zero)	0x0

14.4.1.1.15 ChipStatus

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0048, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved (Should be zero)	0x0
chip_dpd_state	[15:12]	R	Chip is in the deep power down state	0x0
chip_sref_state	[11:8]	R	Chip is in the self-refresh state	0x0
chip_pd_state	[7:4]	R	Chip is in the power down state	0x0
chip_busy_state	[3:0]	R	Chip is in the busy state [0] = chip0 busy state [1] = chip1 busy state [2] = chip2 busy state [3] = chip3 busy state	0x0

14.4.1.1.16 MrStatus

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0054, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved (Should be zero)	0x0
mr_status	[7:0]	R	Mode Registers Status	0x0

14.4.1.1.17 QosControl n (n = 0 to 15)

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0060, + 0x0068, + 0x0070, + 0x0078, + 0x0080, + 0x0088, + 0x0090, + 0x0098, + 0x00A0, + 0x00A8, + 0x00B0, + 0x00B8, + 0x00C0, + 0x00C8, + 0x00D0, + 0x00D8
- Reset Value = 0x0000_0FFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	RW	Reserved (Should be zero)	0x0
cfg_qos	[11:0]	RW	QoS Cycles 0xn = n MBCLK cycles The matched ARID uses this value for its timeout counters instead of ConControl.timeout_cnt.	0xFFF

14.4.1.1.18 WrTraConfig

- Base Address: 0xC00E_0000
- Address = Base Address + 0x00F4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
row_addr	[31:16]	RW	Row Address for Write Training	0x0
RSVD	[15:4]	–	Reserved (Should be zero)	0x0
bank	[3:1]	RW	Bank Address for Write Training	0x0
write_training_en	[0]	RW	Write Training Enable Use this field to issue ACT command. Before setting this field, below things should be finished. Please see PHY manual. • Set write latency before write training(PHY's control register 26) • Set write training mode(PHY's control register 2) 0x0 = Disable, 0x1 = Enable (Issue ACT command)	0x0

14.4.1.1.19 RdlvlConfig

- Base Address: 0xC00E_0000
- Address = Base Address + 0x00F8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved (Should be zero)	0x0
ctrl_rdlvl_data_en	[1]	RW	Data eye training enable	0x0
ctrl_rdlvl_gate_en	[0]	RW	Gate training enable This is only valid for DDR3 case. If LPDDR2-S4/LPDDR3 is used, this field must be set to 0x0. When ctrl_rdlvl_en = 1, Read leveling offset values will be used instead of ctrl_offsetr*. If read leveling is used, this value should be high during operation. This field should be set after dfi_init_complete is asserted. 0x0 = Disable, 0x1 = Enable	0x0

14.4.1.1.20 BRBRSVCONTROL

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0100, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved (Should be zero)	0x0
brb_rsv_en_w3	[7]	RW	Enable Write-BRB reservation for AXI port 3	0x0
brb_rsv_en_w2	[6]	RW	Enable Write-BRB reservation for AXI port 2	0x0
brb_rsv_en_w1	[5]	RW	Enable Write-BRB reservation for AXI port 1	0x0
brb_rsv_en_w0	[4]	RW	Enable Write-BRB reservation for AXI port 0	0x0
brb_rsv_en_r3	[3]	RW	Enable Read-BRB reservation for AXI port 3	0x0
brb_rsv_en_r2	[2]	RW	Enable Read-BRB reservation for AXI port 2	0x0
brb_rsv_en_r1	[1]	RW	Enable Read-BRB reservation for AXI port 1	0x0
brb_rsv_en_r0	[0]	RW	Enable Read-BRB reservation for AXI port 0	0x0

14.4.1.1.21 BRBRSVCONFIG

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0104, Reset Value = 0x8888_8888

Name	Bit	Type	Description	Reset Value
brb_rsv_th_w3	[31:28]	RW	Write-BRB reservation threshold for AXI port 3 Write request from AXI port3 does not serviced when Write-BRB reservation is enabled for AXI port 3 and the occupancy of corresponding Write-BRB exceeds brb_rsv_th_w3.	0x8
brb_rsv_th_w2	[27:24]	RW	Enable Write-BRB reservation for AXI port 2 Write request from AXI port2 does not serviced when Write-BRB reservation is enabled for AXI port 2 and the occupancy of corresponding Write-BRB exceeds brb_rsv_th_w2.	0x8
brb_rsv_th_w1	[23:20]	RW	Enable Write-BRB reservation for AXI port 1 Write request from AXI port1 does not serviced when Write-BRB reservation is enabled for AXI port 1 and the occupancy of corresponding Write-BRB exceeds brb_rsv_th_w1.	0x8
brb_rsv_th_w0	[19:16]	RW	Enable Write-BRB reservation for AXI port 0 Write request from AXI port0 does not serviced when Write-BRB reservation is enabled for AXI port 0 and the occupancy of corresponding Write-BRB exceeds brb_rsv_th_w0.	0x8
brb_rsv_th_r3	[15:12]	RW	Enable Read-BRB reservation for AXI port 3 Read request from AXI port3 does not serviced when Read-BRB reservation is enabled for AXI port 3 and the occupancy of corresponding Read-BRB exceeds brb_rsv_th_w3.	0x8
brb_rsv_th_r2	[11:8]	RW	Enable Read-BRB reservation for AXI port 2 Read request from AXI port2 does not serviced when Read-BRB reservation is enabled for AXI port 2 and the occupancy of corresponding Read-BRB exceeds brb_rsv_th_w2.	0x8
brb_rsv_th_r1	[7:4]	RW	Enable Read-BRB reservation for AXI port 1 Read request from AXI port1 does not serviced when Read-BRB reservation is enabled for AXI port 1 and the occupancy of corresponding Read-BRB exceeds brb_rsv_th_w1.	0x8
brb_rsv_th_r0	[3:0]	RW	Enable Read-BRB reservation for AXI port 0 Read request from AXI port0 does not serviced when Read-BRB reservation is enabled for AXI port 0 and the occupancy of corresponding Read-BRB exceeds brb_rsv_th_w0.	0x8

14.4.1.1.22 BRBQOSCONFIG

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0108, Reset Value = 0x0000_0010

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved (Should be zero)	0x0
brb_qos_timer_dec	[11:0]	RW	BRB timer decrementing size for QoS. The timer for request in BRB decreases by brb_qos_timer_dec for the following cases. • When the BRB is full • When the request is from the AXI port whose data buffer is full.	0x10

14.4.1.1.23 MemBaseConfig0

- Base Address: 0xC00E_0000
- Address = Base Address + 0x010C, Reset Value = 0x0020_07F8

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	–	Reserved (Should be zero)	0x0
chip_base	[26:16]	RW	AXI Base Address AXI base address [34:24] = chip_base, For example, if chip_base = 0x20, then AXI base address of memory chip0 becomes 0x2000_0000.	0x20
RSVD	[15:11]	–	Reserved (Should be zero)	0x0
chip_mask	[10:0]	RW	AXI Base Address Mask Upper address bit mask to determine AXI offset address of memory chip0. 0 = Corresponding address bit is not to be used for comparison 1 = Corresponding address bit is to be used for comparison For example, if chip_mask = 0x7F8, then AXI offset address be-comes 0x0000_0000 ~ 0x07FF_FFFF. If AXI base address of memory chip0 is 0x2000_0000, then memory chip0 has an ad-dress range of 0x2000_0000 ~ 0x27FF_FFFF.	0x7F8

NOTE: DRAM Start Address: 0x0000_0000
DRAM End Address: 0x7FFF_FFFF

14.4.1.1.24 MemBaseConfig1

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0110, Reset Value = 0x0020_07F8

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	–	Reserved (Should be zero)	0x0
chip_base	[26:16]	RW	AXI Base Address AXI base address [34:24] = chip_base, For example, if chip_base = 0x20, then AXI base address of memory chip0 becomes 0x2000_0000.	0x20
RSVD	[15:11]	–	Reserved (Should be zero)	0x0
chip_mask	[10:0]	RW	AXI Base Address Mask Upper address bit mask to determine AXI offset address of memory chip0. 0 = Corresponding address bit is not to be used for comparison 1 = Corresponding address bit is to be used for comparison For example, if chip_mask = 0x7F8, then AXI offset address be-comes 0x0000_0000 ~ 0x07FF_FFFF. If AXI base address of memory chip0 is 0x2000_0000, then memory chip0 has an ad-dress range of 0x2000_0000 ~ 0x27FF_FFFF.	0x7F8

14.4.1.1.25 WRLVLCONFIG0

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0120, Reset Value = 0x0000_0010

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved (Should be zero)	0x0
t_wlo	[7:4]	RW	Write Leveling Ouput Delay t_wlo * T(MPCLK) should be greater than or equal to the minimum value of memory tWLO and the minimum value is 1.	0x1
RSVD	[3:1]	–	Reserved (Should be zero)	0x0
odt_on	[0]	RW	Turn On ODT for Write Leveling 0x0 = ODT Turn off 0x1 = ODT Turn on, This field is only for write leveling. Turn on before write leveling and turn off after write leveling is finished. Write leveling procedure is MRS for Write leveling - ODT on - wrlvl_wrdata_en - Read ctrl_io_rdata - Change SDLL code of PHY. Refer to PHY manual for details.	0x0

14.4.1.1.26 WRLVLCONFIG1

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0124, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved (Should be zero)	0x0
wrlvl_wrdata_en	[0]	RW	Generate dfi_wrdata_en_p0 for Write Leveling Generate 1cycle pulse of dfi_wrdata_en_p0 for write leveling. Write leveling is supported in DDR3 and LPDDR3. NOTE: That if S/W write this field to 1 then, 1 cycle pulse of dfi_wrdata_en_p0 would be generated. Refer to PHY manual for write leveling.	0x0

14.4.1.1.27 WRLVLSTATUS

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0128, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:5]	RW	Reserved (Should be zero)	0x0
wrlvl_fsm	[4:0]	R	Write Leveling Status 5'b0_0001: FSM IDLE 5'b0_0010: FSM_SETUP 5'b0_0100: FSM_ACCESS 5'b0_1000: FSM_DONE 5'b1_0000: FSM_TWLO wrlvl_eq is valid only when wrlvl_fsm is FSM_IDLE. Refer to PHY manual for write leveling.	0x0

14.4.1.1.28 CTRL_IO_RDATA

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0150, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ctrl_io_rdata	[31:0]	R	ctrl_io_rdata from PHY	0x0

14.4.1.1.29 CACAL_CONFIG0

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0160, Reset Value = 0x003F_F010

Name	Bit	Type	Description	Reset Value
dfi_address_p0	[31:12]	RW	dfi_address_p0 value for CA Calibration This value would be the expected value for comparing the address pattern received from memory.	0x3FF
RSVD	[11:8]	RW	Reserved (Should be zero)	0x0
t_adr	[7:4]	RW	CSN Low to Data Output Delay t_adr * T(MPCLK) should be greater than or equal to the min-imum value of memory tADR and the minimum value is 1.	0x1
RSVD	[3:1]	–	Reserved (Should be zero)	0x0
deassert_cke	[0]	RW	Deassert CKE for CA Calibration 0x0 = Put CKE pin to normal operation 0x1 = Put CKE pin to low This field is only for CA calibration. De-assert CKE before CA calibration and put to normal operation after CA calibration is finished. CA calibration procedure is MRS for CA calibration - De-assert CKE - cacal_csn - Read ctrl_io_rdata - Change SDLL code of PHY. Refer to PHY manual for details.	0x0

14.4.1.1.30 CACAL_CONFIG1

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0164, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	RW	Reserved (Should be zero)	0x0
cacal_csn	[0]	RW	Generate dfi_csn_p0 for CA Calibration Generate 1cycle pulse of dfi_csn_p0 for CA calibration. CA calibration is supported in LPDDR3. NOTE: That if S/W writes this field to 1 then, 1 cycle pulse of dfi_csn_p0 would be generated. Refer to PHY manual for CA calibration.	0x0

14.4.1.1.31 CACAL_STATUS

- Base Address: 0xC00E_0000
- Address = Base Address + 0x0168, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:5]	R	Should be zero	0x0
cacal_fsm	[4:0]	R	Write Leveling Status 5'b0_0001: FSM IDLE 5'b0_0010: FSM_SETUP 5'b0_0100: FSM_ACCESS 5'b0_1000: FSM_DONE 5'b1_0000: FSM_TADR CTRL_IO_RDATA are valid only when wrlvl_fsm is FSM_IDLE. Refer to PHY manual for CA calibration.	0x0

14.4.1.2 DDRPHY Register

14.4.1.2.1 PHY_CON0

- Base Address: 0xC00E_1000
- Address = Base Address + 0x00, Reset Value = 0x1702_0240

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	R	Reserved for future use. This Value has no affect at current system	0
T_WrWrCmd	[28:24]	RW	It controls the interval between Write and Write during DQ Calibration. This value should be always kept by 5'h17. It will be used for debug purpose	5'h17
RSVD	[23:22]	RW	Reserved for future use. This Value has no affect at current system	2'b00
ctrl_upd_range	[21:20]	RW	It decides how many differences between the new lock value and the current lock value which is used in Slave-DLL is needed for updating lock value. 2'b00 = To update always 2'b01 = To ignore the lower 1 bit in ctrl_lock_value 2'b10 = To ignore the lower 2 bits in ctrl_lock_value 2'b11 = To ignore the lower 3 bits in ctrl_lock_value	2'b00
T_WrRdCmd	[19:17]	RW	It controls the interval between Write and Read by cycle unit during Write Calibration. It will be used for debug purpose. 3'b110 = tWTR = 4 cycles 3'b111 = tWTR = 6 cycles	3'b001
ctrl_wrlvl_en (=wrlvl_mode)	[16]	RW	Write Leveling Enable	1'b0
RSVD	[15]	RW	Reserved for future use. This Value has no affect at current system	1'b0
p0_cmd_en	[14]	RW	1'b0 = Issue Phase1 Read Command during read leveling 1'b1 = Issue Phase0 Read Command during read leveling	1'b0
byte_rdlvl_en	[13]	RW	Byte Read Leveling enable. It should be set if memory supports toggling only 1 DQ bit except for other 7 bits during read leveling	1'b0
ctrl_ddr_mode	[12:11]	RW	2'b00 = DDR2 and LPDDR1 2'b01 = DDR3 2'b10 = LPDDR2 2'b11 = LPDDR3	1'b0
RSVD	[10]	RW	Reserved for future use. This Value has no affect at current system	1'b0
ctrl_dfdqs	[9]	RW	1'b0 = Single-ended DQS 1'b1 = Differential DQS	1'b1
ctrl_shgate	[8]	RW	This field controls the gate control signal 1'b0 = Gate signal length = “burst length / 2” + N (DQS	1'b0

Name	Bit	Type	Description	Reset Value
			Pull-Down mode, ctrl_pulld_dqs[3:0] == 4'b1111, N = 0,1,2…) 1'b1 = Gate signal length = “burst length / 2” - 1	
ctrl_ckdis	[7]	RW	This field controls the CK/CKB 1'b0 = Clock output is enabled 1'b1 = Clock output is disabled	1'b0
ctrl_atgate	[6]	RW	If ctrl_atgate=0, Controller should generate ctrl_gate_p*, ctrl_read_p*. If ctrl_atgate=1, PHY will generate ctrl_gate_p*, ctrl_read_p*, but it has some constraints. This setting can be supported only over RL=4, BL and RL should be properly set to operate with ctrl_atgate=1.	1'b1
ctrl_read_disable	[5]	RW	Read ODT (On-Die-Termination) Disable Signal. This signal should be one in LPDDR2 or LPDDR3 mode. 1'b0 = drive ctrl_read_p* normally 1'b1 = drive ctrl_read_p* to 0. (If using LPDDR2 or LPDDR3, ctrl_read_p* will be always 0 by enabling this field.)	1'b0
ctrl_cmosrcv	[4]	RW	This field controls the input mode of I/O 1'b0 = Differential receiver mode for high speed operation 1'b1 = CMOS receiver mode for low speed operation (< 200 MHz)	1'b0
ctrl_read_width	[3]	RW	The default is 1'b0. We strongly recommend that it should have one more idle cycle between read and write because the variation of data arrival time during read can be greater than 1 cycle. If it is 1'b1, the package and board should be carefully optimized with a short length and it should be used at the low frequency. 1'b0 = Termination on period is (BL/2+1.5) cycle (Default) 1'b1 = Termination on period is (B/2+1) cycle(Not recommended)	1'b0
ctrl_fnc_fb	[2:0]	RW	Valid only when {mode_phy, mode_nand, mode_scan, mode_mux} is 4'b00000. For normal operation 3'b000 = Normal operation mode. For ATE test purpose 3'b010 = External FNC read feedback test mode. 3'b011 = Internal FNC read feedback test mode. For Board test purpose 3'b100 = External PHY read feedback test mode. When memory is not attached on the board 3'b101 = Internal PHY read feedback test mode. mode_highz should be set. 3'b110 = Internal PHY write feedback test mode.	3'b000

Name	Bit	Type	Description	Reset Value
			mode_highz should be set. For Power Down 3'b111 = Power Down Mode for SSTL I/O	

14.4.1.2.2 PHY_CON1

- Base Address: 0xC00E_1000
- Address = Base Address + 0x04, Reset Value = 0x0921_0100

Name	Bit	Type	Description	Reset Value
ctrl_gateadj	[31:28]	RW	It adjusts the enable time of "ctrl_gate" on a clock cycle base. MSB (bit[3]) controls direction: 1'b1(subtract delay), 1'b0(add delay), Bit[2:0] set delay value	4'h0
ctrl_readadj	[27:24]	RW	It adjusts the enable time of "ctrl_read" on a clock cycle base. MSB (bit[3]) controls direction: 1'b1(subtract delay), 1'b0(add delay), Bit[2:0] set delay value	4'h9
ctrl_gateduradj	[23:20]	RW	It adjusts the duration cycle of "ctrl_gate" on a clock cycle base. MSB (bit[3]) controls direction: 1'b1(subtract delay), 1'b0(add delay), Bit[2:0] set delay value	4'h2
rdlvl_pass_adj	[19:16]	RW	This field controls how many times "Read" should be operated well to determine if it goes into VWP (Valid Window Period) or not. (default: 4'h1)	4'h1
rdlvl_rddata_adj	[15:0]	RW	It decides the pattern to be read during read or write calibration. (default: 16'h0100) 16'h0100 = DDR3 ("byte_rdlvl_en=1") 16'h0001 = LPDDR3 ("byte_rdlvl_en=1")	16'h0100

14.4.1.2.3 PHY_CON2

- Base Address: 0xC00E_1000
- Address = Base Address + 0x08, Reset Value = 0x0001_0004

Name	Bit	Type	Description	Reset Value
ctrl_readduradj	[31:28]	RW	It adjusts the duration cycle of "ctrl_read" on a clock cycle base. MSB(bit3) controls direction: 1'b1(subtract delay), 1'b0(add delay), Bit[2:0] set delay value	0
wr_deskew_en	[27]	RW	DQ Calibration Start Signal to align DQ, DM during write	1'b0
wr_deskew_con	[26]	RW	If it is enabled, PHY will use "Write Slave DLL Code" which has got during Read Leveling.	1'b0
rdlvl_en	[25]	RW	When rd_cal_mode=1, Read leveling offset values will be used instead of ctrl_offsetr*. If read leveling is used, this value should be high during operation.	1'b0
rdlvl_gate_en	[24]	RW	When gate_cal_mode=1, Gate leveling offset value will be used instead of ctrl_shiftc*. If gate leveling is used, this value should be high during operation	1'b0
rdlvl_ca_en	[23]	RW	When ca_cal_mode=1, CA Calibration offset value will be used and updated	1'b0
rdlvl_incr_adj	[22:16]	RW	It decides the step value of delay line to increase during read leveling (default: 7'h1, fine step delay). It should be smaller than 7'hf [22:21]=2'b00 : The step value will be "rdlvl_incr_adj[20:16]" [22:21]=2'b01 : The step value will be "T/16" [22:21]=2'b10 : The step value will be "T/32" [22:21]=2'b11 : The step value will be "T/64"	7'b1
RSVD	[15]	R	Reserved (Should be zero)	–
WrDeskew_clear	[14]	RW	Clear WrDeSkewCode after Write De-skewing	1'b0
RdDeskew_clear	[13]	RW	Clear RdDeSkewCode after Read De-skewing	1'b0
DLLDeskewEn	[12]	RW	Deskew Code is updated with the latest Master DLL lock value whenever "dfi_ctrlupd_req" is issued from controller during DLLDeskewEn=1. It is required to compensate On-chip VT variation	1'b0
rdlvl_start_adj	[11:8]	RW	It decides the most left-shifted point when read leveling is started and the most right-shifted point when read leveling is ended. [9:8]=2'b00 : The most left-shifted code is 8'h00 [9:8]=2'b01 : The most left-shifted code is T/8 [9:8]=2'b10 : The most left-shifted code is T/8+T/16 [9:8]=2'b11 : The most left-shifted code is T/8-T/16 [11:10]=2'b00 : The most right-shifted Code is 8'hFF [11:10]=2'b01 : The most right-shifted Code is T/2+T/8 [11:10]=2'b10 : The most right-shifted Code is T/2+T/8+T/16	4'h0

Name	Bit	Type	Description	Reset Value
			[11:10]=2'b11 : The most right-shifted Code is T/2+T/8-T/16	
RSVD	[7]	RW	Reserved (Should be zero)	–
InitDeskewEn	[6]	RW	This field should be enabled before DQ Calibration is started	1'b0
RSVD	[5:2]	R	Reserved (Should be zero)	–
rdlvl_gateadj	[1:0]	RW	It determines how much earlier ctrl_gate* is asserted than RDQS when the transition of RDQS is detected. [1:0]=2'b00 : T/2(default) [1:0]=2'b01 : T/4 [1:0]=2'b10 : T/8 [1:0]=2'b11 : T/16	2'b0

14.4.1.2.4 PHY_CON3

- Base Address: 0xC00E_1000
- Address = Base Address + 0x0C, Reset Value = 0x0021_0842

Name	Bit	Type	Description	Reset Value
RSVD	[31:18]	R	Reserved (Should be zero)	-
ctrl_shiftc3	[17:15]	RW	GATEin signal delay amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. GATEin signal will be delayed by T/16 whenever it increases one. 000 = 0 (0° shift), 001 = T (365° shift), 010 = T/2 (180° shift), 011 = T/4 (90° shift) 100 = T/8 (45° shift), 101 = T/16 (22.5° shift)	3'b010
RSVD	[14:13]	R	Reserved (Should be zero)	-
ctrl_shiftc2	[12:10]	RW	GATEin signal delay amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. GATEin signal will be delayed by T/16 whenever it increases one. 000 = 0 (0° shift), 001 = T (365° shift), 010 = T/2 (180° shift), 011 = T/4 (90° shift) 100 = T/8 (45° shift), 101 = T/16 (22.5° shift)	3'b010
RSVD	[9:8]	R	Reserved (Should be zero)	-
ctrl_shiftc1	[7:5]	RW	GATEin signal delay amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. GATEin signal will be delayed by T/16 whenever it increases one. 000 = 0 (0° shift), 001 = T (365° shift), 010 = T/2 (180° shift), 011 = T/4 (90° shift) 100 = T/8 (45° shift), 101 = T/16 (22.5° shift)	3'b010
RSVD	[4:3]	R	Reserved (Should be zero)	-

Name	Bit	Type	Description	Reset Value
ctrl_shiftc0	[2:0]	RW	GATEin signal delay amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. This value is limited by the half of the maximum delay in Master Delay Line. GATEin signal will be delayed by T/16 whenever it increases one. 000 = 0 (0° shift), 001 = T (365° shift), 010 = T/2 (180° shift), 011 = T/4 (90° shift) 100 = T/8 (45° shift), 101 = T/16 (22.5° shift)	3'b010

14.4.1.2.5 PHY_CON4

- Base Address: 0xC00E_1000
- Address = Base Address + 0x10, Reset Value = 0x0808_0808

Name	Bit	Type	Description	Reset Value
ctrl_offsetr3	[31:24]	RW	This field can be used to give offset to read DQS. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Read DQS offset amount: • ctrl_offsetr3[7] = 1: (tFS: fine step delay) • Read DQS 90° delay amount - ctrl_offsetr3[6:0] × tFS • ctrl_offsetr3[7] = 0: (tFS: fine step delay) • Read DQS 90° delay amount + ctrl_offsetr3[6:0] × tFS	8'h8
ctrl_offsetr2	[23:16]	RW	This field can be used to give offset to read DQS. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Read DQS offset amount: • ctrl_offsetr2[7] = 1: (tFS: fine step delay) • Read DQS 90° delay amount - ctrl_offsetr2[6:0] × tFS • ctrl_offsetr2[7] = 0: (tFS: fine step delay) • Read DQS 90° delay amount + ctrl_offsetr2[6:0] × tFS	8'h8
ctrl_offsetr1	[15:8]	RW	This field can be used to give offset to read DQS. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Read DQS offset amount: • ctrl_offsetr1[7] = 1: (tFS: fine step delay) • Read DQS 90° delay amount - ctrl_offsetr1[6:0] × tFS • ctrl_offsetr1[7] = 0: (tFS: fine step delay) • Read DQS 90° delay amount + ctrl_offsetr1[6:0] × tFS	8'h8
ctrl_offsetr0	[7:0]	RW	This field can be used to give offset to read DQS. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Read DQS offset amount: • ctrl_offsetr0[7] = 1: (tFS: fine step delay) • Read DQS 90° delay amount - ctrl_offsetr0[6:0] × tFS • ctrl_offsetr0[7] = 0: (tFS: fine step delay) • Read DQS 90° delay amount + ctrl_offsetr0[6:0] × tFS	8'h8

14.4.1.2.6 PHY_CON5

- Base Address: 0xC00E_1000
- Address = Base Address + 0x14, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved (Should be zero)	2'h0
readmodecon	[7:0]	RW	Read Register Mode Control After Gate Leveling, • When ReadModeCon[7:0]='hD, Check "Gate Cycle"(0x50) • When ReadModeCon[7:0]='hE, Check "Gate Code"(0x50) • After Read Calibration, • When ReadModeCon[7:0]='h05, Check "VWML"(0x50) • When ReadModeCon[7:0]='h06, Check "VWMR"(0x50) • When ReadModeCon[7:0]='h07, Check "VWMC"(0x50) • When ReadModeCon[7:0]='h08, Check "VWMC"(0x50) • When ReadModeCon[7:0]='h01, Check "De-skew Code"(0x50) • After Write Calibration, • When ReadModeCon[7:0]='h05, Check "VWML"(0x50) • When ReadModeCon[7:0]='h06, Check "VWMR"(0x50) • When ReadModeCon[7:0]='h07, Check "VWMC"(0x50) • When ReadModeCon[7:0]='h09, Check "VWMC"(0x50) • When ReadModeCon[7:0]='h03, Check "De-skew Code"(0x50) NOTE: The result of VWM* will be over-written after each calibration. Check PHY_CON18 (=0x50) according to ReadModeCon[7:0].	8'h0

14.4.1.2.7 PHY_CON6

- Base Address: 0xC00E_1000
- Address = Base Address + 0x18, Reset Value = 0x0808_0808

Name	Bit	Type	Description	Reset Value
ctrl_offsetw3	[31:24]	RW	This field can be used to give offset to write DQ. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Write DQ offset amount : • ctrl_offsetw3[7] = 1 : (tFS: fine step delay) • Write DQ 270° delay amount - ctrl_offsetw3[6:0] × tFS • ctrl_offsetw3[7] = 0 : (tFS: fine step delay) • Write DQ 270° delay amount + ctrl_offsetw3[6:0] x tFS	0x8
ctrl_offsetw2	[23:16]	RW	This field can be used to give offset to write DQ. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Write DQ offset amount : • ctrl_offsetw2[7] = 1 : (tFS: fine step delay) • Write DQ 270° delay amount - ctrl_offsetw2[6:0] × tFS • ctrl_offsetw2[7] = 0 : (tFS: fine step delay) • Write DQ 270° delay amount + ctrl_offsetw2[6:0] x tFS	0x8
ctrl_offsetw1	[15:8]	RW	This field can be used to give offset to write DQ. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Write DQ offset amount : • ctrl_offsetw1[7] = 1 : (tFS: fine step delay) • Write DQ 270° delay amount - ctrl_offsetw1[6:0] × tFS • ctrl_offsetw1[7] = 0 : (tFS: fine step delay) • Write DQ 270° delay amount + ctrl_offsetw1[6:0] x tFS	0x8
ctrl_offsetw0	[7:0]	RW	This field can be used to give offset to write DQ. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. Write DQ offset amount : • ctrl_offsetw0[7] = 1 : (tFS: fine step delay) • Write DQ 270° delay amount - ctrl_offsetw0[6:0] × tFS • ctrl_offsetw0[7] = 0 : (tFS: fine step delay) • Write DQ 270° delay amount + ctrl_offsetw0[6:0] x tFS	0x8

14.4.1.2.8 PHY_CON8

- Base Address: 0xC00E_1000
- Address = Base Address + 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ctrl_offsetc3	[31:24]	RW	Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. ctrl_offsetc [7] = 1 : (tFS: fine step delay) GATEout delay amount - ctrl_offsetc [6:0] x tFS ctrl_offsetc [7] = 0 : (tFS: fine step delay) GATEout delay amount + ctrl_offsetc [6:0] x tFS	0x0
ctrl_offsetc2	[23:16]	RW	Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. ctrl_offsetc [7] = 1 : (tFS: fine step delay) GATEout delay amount - ctrl_offsetc [6:0] x tFS ctrl_offsetc [7] = 0 : (tFS: fine step delay) GATEout delay amount + ctrl_offsetc [6:0] x tFS	0x0
ctrl_offsetc1	[15:8]	RW	Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. ctrl_offsetc [7] = 1 : (tFS: fine step delay) GATEout delay amount - ctrl_offsetc [6:0] x tFS ctrl_offsetc [7] = 0 : (tFS: fine step delay) GATEout delay amount + ctrl_offsetc [6:0] x tFS	0x0
ctrl_offsetc0	[7:0]	RW	Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. ctrl_offsetc [7] = 1 : (tFS: fine step delay) GATEout delay amount - ctrl_offsetc [6:0] x tFS ctrl_offsetc [7] = 0 : (tFS: fine step delay) GATEout delay amount + ctrl_offsetc [6:0] x tFS	0x0

14.4.1.2.9 PHY_CON9

- Base Address: 0xC00E_1000
- Address = Base Address + 0x24, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved (Should be zero)	0x0
ctrl_offsetc4 (40-bit)	[7:0]	RW	Gate offset amount for DDR. If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. ctrl_offsetc [7] = 1 : (tFS: fine step delay) GATEout delay amount - ctrl_offsetc [6:0] x tFS ctrl_offsetc [7] = 0 : (tFS: fine step delay) GATEout delay amount + ctrl_offsetc [6:0] x tFS	0x0

14.4.1.2.10 PHY_CON10

- Base Address: 0xC00E_1000
- Address = Base Address + 0x28, Reset Value = 0x0000_0008

Name	Bit	Type	Description	Reset Value
RSVD	[31:25]	–	Reserved (Should be zero)	0x0
ctrl_resync	[24]	RW	Active RISIG-EDGE signal. This signal should become LOW after set HIGH for normal operation. When this bit transits from LOW to HIGH, pointers of FIFO and DLL information is updated. In general, this bit should be set during initialization and refresh cycles. Refer to "MC-Initiated Update"(p105) to use ctrl_resync.	0x0
RSVD	[23:8]	–	Reserved (Should be zero)	0x0
ctrl_offsetd	[7:0]	RW	This field is for debug purpose. (For LPDDR2) If this field is fixed, this should not be changed during operation. This value is valid only after dfi_ctrlupd_req becomes HIGH and LOW. The right-shifted value is limited by the quarter of the maximum delay in Master Delay Line. offset amount for 270° clock generation: ctrl_offsetd[7] = 1 : (tFS: fine step delay) 270° delay amount - ctrl_offsetd[6:0] x tFS ctrl_offsetd[7] = 0 : 270° delay amount + ctrl_offsetd[6:0] x tFS	0x8

14.4.1.2.11 PHY_CON12

- Base Address: 0xC00E_1000
- Address = Base Address + 0x30, Reset Value = 0x1010_0070

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved (Should be zero)	0x0
ctrl_start_point	[30:24]	RW	Initial DLL lock start point. This is the number of delay cells and is the start point where "DLL" start tracing to be locked. Initial delay time is calculated by multiplying the unit delay of delay cell and this value.	7'h10
RSVD	[23]	–	Reserved (Should be zero)	0x0
ctrl_inc	[22:16]	RW	Increase amount of start point	7'h10
ctrl_force	[14:8]	RW	This field is used instead of ctrl_lock_value[9:2] found by the DLL only when ctrl_dll_on is LOW ,i.e. If the DLL is off, this field is used to generate 270° clock and shift DQS by 90°.	0x0
ctrl_start	[6]	RW	This field is used to start DLL locking.	0'b1
ctrl_dll_on	[5]	RW	HIGH active start signal to turn on the DLL. This signal should be kept HIGH for normal operation. If this signal becomes LOW, DLL is turned off. This bit should be kept set before ctrl_start is set to turn on the DLL.	0'b1
ctrl_ref	[4:1]	RW	This field determines the period of time when ctrl_locked is cleared. 4'b0000 = Don't use. 4'b0001 = ctrl_flock is de-asserted during 16 clock cycles, ctrl_locked is deasserted. 4'b0010 = ctrl_flock is de-asserted during 24 clock cycles, ctrl_locked is deasserted. ~ 4'b1110 = ctrl_flock is de-asserted during 120 clock cycles, ctrl_locked is deasserted. 4'b1111 = Once ctrl_locked and dfi_init_complete are asserted, those won't be deasserted until rst_n is asserted.	4'h8
RSVD	[0]	–	Reserved (Should be zero)	0x0

14.4.1.2.12 PHY_CON13

- Base Address: 0xC00E_1000
- Address = Base Address + 0x34, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	R	Reserved (Should be zero)	–
ctrl_lock_value	[16:8]	RW	Locked delay line encoding value. ctrl_lock_value[8:2] : number of delay cells for coarse lock. ctrl_lock_value[1:0] : control value for fine lock. From ctrl_lock_value[8:0], tFS(fine step delay) can be calculated. tFS = tCK / ctrl_lock_value[9:0].	–
ctrl_clock	[2]	R	Coarse lock information. According to clock jitter, ctrl_clock can be de-asserted.	–
ctrl_flock	[1]	R	Fine lock information. According to clock jitter, ctrl_flock can be de-asserted.	–
ctrl_locked	[0]	R	DLL stable lock information. This field is set after ctrl_flock is set. This field is cleared when ctrl_flock is de-asserted for some period of time specified by ctrl_ref[3:0] value. This field is required for stable lock status check.	–

14.4.1.2.13 PHY_CON14

- Base Address: 0xC00E_1000
- Address = Base Address + 0x38, Reset Value = 0x001F_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved (Should be zero)	–
ctrl_pulld_dq	[11:8]	RW	Active HIGH signal to down DQ signals. For normal operation this field should be zero. When bus is idle, it can be set to pull-down or up the bus not to make bus high-z state.	4'h0
ctrl_pulld_dqs	[3:0]	RW	Active HIGH signal to pull-up or down PDQS/NDQS signals. When using Gate Leveling in DDR3, this field can be zero. When bus is idle, it can be set to pull-down or up the bus not to make bus high-z state (PDQS/NDQS is pulled-down/up). For LPDDR2/LPDDR3 mode, this field should be always set for normal operation to make P/NDQS signals pull-down/up.	4'h0

14.4.1.2.14 PHY_CON15

- Base Address: 0xC00E_1000
- Address = Base Address + 0x3C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	R	Reserved (Should be zero)	–
ctrl_fb_err	[20:16]	R	Feedback test stop with error for each slice. Ctrl_fb_err[0]: error of data channel0. Ctrl_fb_err[1]: error of data channel1. Ctrl_fb_err[2]: error of data channel2 for 32-bit PHY. Error of control for 16-bit PHY. Ctrl_fb_err[3]: error of data channel3 for 32-bit PHY. Ctrl_fb_err[4]: error of control channel for 32-bit PHY.	5'h0
ctrl_fb_okay	[12:8]	R	Feedback test completion without error for each slice. Ctrl_fb_oky[0]: okay of data channel0. Ctrl_fb_oky[1]: okay of data channel1. Ctrl_fb_oky[2]: okay of data channel2 for 32-bit PHY. Okay of control channel for 16-bit PHY. Ctrl_fb_oky[3]: okay of data channel3 for 32-bit PHY. Ctrl_fb_oky[4]: okay of control channel for 32-bit PHY.	5'h0
ctrl_fb_start	[4:0]	RW	Feedback test start signal for each slice. Ctrl_fb_start[0]: start of data channel0 ctrl_fb_start[1]: start of data channel1 ctrl_fb_start[2]: start of data channel2 for 32-bit PHY start of control channel for 16-bit PHY ctrl_fb_start[3]: start of data channel3 for 32-bit PHY. Ctrl_fb_start[4]: start of control channel for 32-bit PHY. For this test, mode_highz should be set when memory is on the board	5'h0

14.4.1.2.15 PHY_CON16

- Base Address: 0xC00E_1000
- Address = Base Address + 0x40, Reset Value = 0x0800_0304

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	RW	Reserved (Should be zero)	0x0
zq_clk_en	[27]	RW	ZQ I/O Clock enable	1'b1
zq_mode_dds	[26:24]	RW	Driver strength selection. It recommends one of the following settings instead of 3'h0. 3'b100 = 48Ω Impedance output driver 3'b101 = 40Ω Impedance output driver 3'b110 = 34Ω Impedance output driver 3'b111 = 30Ω Impedance output driver	3'h0
zq_mode_term	[23:21]	RW	On-die-termination(ODT) resistor value selection. "pblpddr3_dds" and "pblpddr3_dqs_dds" don't support ODT. 3'b001 = 120Ω Receiver termination 3'b010 = 60Ω Receiver termination 3'b011 = 40Ω Receiver termination 3'b100 = 30Ω Receiver termination	3'h0
zq_rgddr3	[20]	RW	GDDR3 mode enable signal(High: GDDR3 mode)	1'b0
zq_mode_noterm	[19]	RW	Termination disable selection. 0 = Termination enable. 1 = Termination disable. DDR : 1'b1 DDR2/DDR3 : 1'b0(recommended) or 1'b1(when termination is not used) LPDDR2/LPDDR3 : 1'b1 gDDR3 : 1'b0	1'b0
zq_clk_div_en	[18]	RW	Clock dividing enable	1'b0
zq_force_impn	[17:15]	RW	Immediate control code for pull-down.	3'h0
zq_force_impp	[14:12]	RW	Immediate control code for pull-up.	3'h0
zq_udt_dly	[11:4]	RW	ZQ I/O clock enable duration for auto calibration mode.	8'h30
zq_manual_mode	[3:2]	RW	Manual calibration mode selection 2'b00 = Force calibration 2'b01 = Long calibration 2;b10 = Short calibration	2'b01
zq_manual_str	[1]	RW	Manual calibration start	1'b0
zq_auto_en	[0]	RW	Auto calibration enable	1'b0

14.4.1.2.16 PHY_CON17

- Base Address: 0xC00E_1000
- Address = Base Address + 0x48, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	RW	Reserved (Should be zero)	0x0
zq_pmon	[8:6]	R	Control code found by auto calibration for pull-up.	–
zq_nmon	[5:3]	R	Control code found by auto calibration for pull-down.	–
zq_error	[2]	R	Calibration fail indication (High: calibration failed)	–
zq_pending	[1]	R	Auto calibration enable status	–
zq_done	[0]	R	ZQ Calibration is finished.	1'b0

14.4.1.2.17 PHY_CON18

- Base Address: 0xC00E_1000
- Address = Base Address + 0x4C, Reset Value = 0x0055_5555

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved (Should be zero)	0x0
dm_fail_status	[27:24]	R	It will be enabled if there is no pass period after DM Calibration. It should be read by zero if Calibration is done normally. Please refer to ReadModeCon (=PHY_CON5) to read.	0x0
T3_rddata_en	[23:18]	R	Trddata_en timing parameter for data slice 3. Please refer to ReadModeCon (=PHY_CON5) to read.	0x15
T2_rddata_en	[17:12]	R	Trddata_en timing parameter for data slice 2. Please refer to ReadModeCon (=PHY_CON5) to read.	0x15
T1_rddata_en	[11:6]	R	Trddata_en timing parameter for data slice 1. Please refer to ReadModeCon (=PHY_CON5) to read.	0x15
T0_rddata_en	[5:0]	R	Trddata_en timing parameter for data slice 0. Please refer to ReadModeCon (=PHY_CON5) to read.	0x15

14.4.1.2.18 PHY_CON19

- Base Address: 0xC00E_1000
- Address = Base Address + 0x50, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
rdlvl_offsetr3	[31:24]	R	DQ Calibration SDLL code for data slice 3. Please refer to ReadModeCon(=PHY_CON5) to read.	–
rdlvl_offsetr2	[23:16]	R	DQ Calibration SDLL code for data slice 2. Please refer to ReadModeCon(=PHY_CON5) to read.	–
rdlvl_offsetr1	[15:8]	R	DQ Calibration SDLL code for data slice 1. Please refer to ReadModeCon(=PHY_CON5) to read.	–
rdlvl_offsetr0	[7:0]	R	DQ Calibration SDLL code for data slice 0. Please refer to ReadModeCon(=PHY_CON5) to read.	–

14.4.1.2.19 PHY_CON20

- Base Address: 0xC00E_1000
- Address = Base Address + 0x54, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
rdlvl_offsetc3	[31:24]	R	Gate Training SDLL code for data slice 3. Please refer to ReadModeCon(=PHY_CON5) to read.	–
rdlvl_offsetc2	[23:16]	R	Gate Training SDLL code for data slice 2. Please refer to ReadModeCon(=PHY_CON5) to read.	–
rdlvl_offsetc1	[15:8]	R	Gate Training SDLL code for data slice 1. Please refer to ReadModeCon(=PHY_CON5) to read.	–
rdlvl_offsetc0	[7:0]	R	Gate Training SDLL code for data slice 0. Please refer to ReadModeCon(=PHY_CON5) to read.	–

14.4.1.2.20 PHY_CON21

- Base Address: 0xC00E_1000
- Address = Base Address + 0x58, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
vwm_fail_status	[31:0]	R	It will be enabled if there is no pass period after DQ Calibration. It should be read by zero if Calibration is done normally. Please refer to ReadModeCon (=PHY_CON5) to read.	0x0

14.4.1.2.21 PHY_CON22

- Base Address: 0xC00E_1000
- Address = Base Address + 0x5C, Reset Value = 0x0000_0208

Name	Bit	Type	Description	Reset Value
RSVD	[31:20]	R	Reserved (Should be zero)	–
lpddr2_addr	[19:0]	RW	LPDDR2/LPDDR3 Address. Default value (=0x208) is Mode Register Reads to DQ Calibration registers MR32. Reads to MR32 return DQ Calibration Pattern "1111-0000-1111-0000" on DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. When doing Write Training, This field should be set by READ command. For example, lpddr2_addr2 will be 20'h5 if the column address is 11'h0 and bank address is 3'b000. According to READ Command definition in LPDDR2 or LPDDR3 lpddr2_addr[19:0] = "C11-C10-C9-C8-C7-C6-C5-C4-C3-AP-BA2-BA1-BA0-C2-C1-R-R-H-L-H" (C means Column Address, BA means Bank Address, R means Reserved) In case of CA swap mode, lpddr2_addr=20'h41 for Read Training and lpddr2_addr=20'h204 for Write Training if the column address is 11'h0 and bank address is 3'b000. lpddr2_addr[19:0] = "AP-C3-C9-C5-C6-C7-C8-C4-C10-C11-H-L-BA0-R-R-C1-C2-H-B1-B2"(CA swap mode)	0x208

14.4.1.2.22 PHY_CON23

- Base Address: 0xC00E_1000
- Address = Base Address + 0x60, Reset Value = 0x0000_03FF

Name	Bit	Type	Description	Reset Value
RSVD	[31:20]	R	Reserved (Should be zero)	–
lpddr2_default	[19:0]	RW	LPDDR2/LPDDR3 Default Address	0x3ff

14.4.1.2.23 PHY_CON24

- Base Address: 0xC00E_1000
- Address = Base Address + 0x64, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ddr3_default	[31:16]	RW	DDR3 Default Address	0x0
ddr3_addr	[15:0]	RW	DDR3 Address	0x0
ca_swap_mode	[0]	RW	If ctrl_ddr_mode[1]=1 and ca_swap_mode=1, PHY will be in "CA swap mode" for POP. In "CA swap mode", CA[9:0] will be swapped in the following way. CA[0] CA[9] CA[1] CA[8] CA[2] CA[7] CA[3] CA[6] CA[4] CA[5] CA[5] CA[4] CA[6] CA[3] CA[7] CA[2] CA[8] CA[1] CA[9] CA[0] NOTE: Don't use "ctrl_atgate=1" in normal operation when ca_swap_mode = 1. "ctrl_atgate" can be enabled only during calibration.	0x0

14.4.1.2.24 PHY_CON25

- Base Address: 0xC00E_1000
- Address = Base Address + 0x68, Reset Value = 0x105E_107E

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved (Should be zero)	–
ddr3_cmd	[29:16]	RW	DDR3 Command	0x105E
RSVD	[15:14]	R	Reserved (Should be zero)	–
lpddr2_cmd	[13:0]	RW	LPDDR2/3 Command. This field should be "16'h000E" using LPDDR2 or LPDDR3.	0x107E

14.4.1.2.25 PHY_CON26

- Base Address: 0xC00E_1000
- Address = Base Address + 0x6C, Reset Value = 0x0008_107F

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	R	Reserved (Should be zero)	–
T_wrdata_en	[20:16]	RW	Clock cycles between write command and the first edge of DQS which can capture the first valid DQ. For example, if WL is 6, It should be set as 7(=WL+1) in LPDDR3, 6(=WL) in DDR3.	0x8
cmd_default	[13:0]	RW	Default Command 16'h000F(LPDDR2, LPDDR3) 16'h107F(DDR2, DDR3)	0x107F

14.4.1.2.26 PHY_CON27

- Base Address: 0xC00E_1000
- Address = Base Address + 0x70, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
rlvl_vwml3	[31:24]	R	Left Code Value in Read Valid Window Margin for Data Slice3. Please refer to ReadModeCon (=PHY_CON5) to read.	–
rlvl_vwml2	[23:16]	R	Left Code Value in Read Valid Window Margin for Data Slice2. Please refer to ReadModeCon (=PHY_CON5) to read.	–
rlvl_vwml1	[15:8]	R	Left Code Value in Read Valid Window Margin for Data Slice1. Please refer to ReadModeCon (=PHY_CON5) to read.	–
rlvl_vwml0	[7:0]	R	Left Code Value in Read Valid Window Margin for Data Slice0. Please refer to ReadModeCon (=PHY_CON5) to read.	–

14.4.1.2.27 PHY_CON28

- Base Address: 0xC00E_1000
- Address = Base Address + 0x74, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
rlvl_vwmr3	[31:24]	R	Right Code Value in Read Valid Window Margin for Data Slice3. Please refer to ReadModeCon (=PHY_CON5) to read	–
rlvl_vwmr2	[23:16]	R	Right Code Value in Read Valid Window Margin for Data Slice2. Please refer to ReadModeCon (=PHY_CON5) to read.	–
rlvl_vwmr1	[15:8]	R	Right Code Value in Read Valid Window Margin for Data Slice1. Please refer to ReadModeCon (=PHY_CON5) to read.	–
rlvl_vwmr0	[7:0]	R	Right Code Value in Read Valid Window Margin for Data Slice0. Please refer to ReadModeCon (=PHY_CON5) to read.	–

14.4.1.2.28 PHY_CON29

- Base Address: 0xC00E_1000
- Address = Base Address + 0x78, Reset Value = 0x0501_0203

Name	Bit	Type	Description	Reset Value
Version_Info	[31:0]	R	Version Information	0x0501_0203

14.4.1.2.29 PHY_CON30

- Base Address: 0xC00E_1000
- Address = Base Address + 0x7C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ctrl_wrlvl3_code	[30:24]	RW	Write Level Slave DLL Code Value for Data_Slice 3 (0x8 to 0x38)	0x0
ctrl_wrlvl2_code	[23:17]	RW	Write Level Slave DLL Code Value for Data_Slice 2 (0x8 to 0x38)	0x0
ctrl_wrlvl	[16]	RW	Write Level Enable	0x0
RSVD	[15]	R	Reserved (Should be zero)	–
ctrl_wrlvl1_code	[14:8]	RW	Write Level Slave DLL Code Value for Data_Slice 1 (0x8 to 0x38)	0x0
RSVD	[7]	R	Reserved (Should be zero)	–
ctrl_wrlvl0_code	[6:0]	RW	Write Level Slave DLL Code Value for Data_Slice 0 (0x8 to 0x38)	0x0

14.4.1.2.30 PHY_CON31

- Base Address: 0xC00E_1000
- Address = Base Address + 0x80, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CA4DeSkewCode	[31:28]	RW	DeSkew Code for CA[4] (0x8 to 0x60)	0x0
CA3DeSkewCode	[27:21]	RW	DeSkew Code for CA[3] (0x8 to 0x60)	0x0
CA2DeSkewCode	[20:14]	RW	DeSkew Code for CA[2] (0x8 to 0x60)	0x0
CA1DeSkewCode	[13:7]	RW	DeSkew Code for CA[1] (0x8 to 0x60)	0x0
CA0DeSkewCode	[6:0]	RW	DeSkew Code for CA[0] (0x8 to 0x60)	0x0

14.4.1.2.31 PHY_CON32

- Base Address: 0xC00E_1000
- Address = Base Address + 0x84, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CA9DeSkewCode	[31]	RW	DeSkew Code for CA[9] (0x8 to 0x60)	0x0
CA8DeSkewCode	[30:24]	RW	DeSkew Code for CA[8] (0x8 to 0x60)	0x0
CA7DeSkewCode	[23:17]	RW	DeSkew Code for CA[7] (0x8 to 0x60)	0x0
CA6DeSkewCode	[16:10]	RW	DeSkew Code for CA[6] (0x8 to 0x60)	0x0
CA5DeSkewCode	[9:3]	RW	DeSkew Code for CA[5] (0x8 to 0x60)	0x0
CA4DeSkewCode	[2:0]	RW	DeSkew Code for CA[4] (0x8 to 0x60)	0x0

14.4.1.2.32 PHY_CON33

- Base Address: 0xC00E_1000
- Address = Base Address + 0x88, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CKE0DeSkewCode	[31:27]	RW	DeSkew Code for CKE[0], (0x8~0x60)	0x0
CS1DeSkewCode	[26:20]	RW	DeSkew Code for CS[1] (0x8~0x60)	0x0
CS0DeSkewCode	[19:13]	RW	DeSkew Code for CS[0] (0x8~0x60)	0x0
CKDeSkewCode	[12:6]	RW	DeSkew Code for CK, (0x8~0x60)	0x0
CA9DeSkewCode	[5:0]	RW	DeSkew Code for CA[9] (0x8~0x60)	0x0

14.4.1.2.33 PHY_CON34

- Base Address: 0xC00E_1000
- Address = Base Address + 0x8C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	R	Reserved (Should be zero)	–
CKE1DeSkewCode	[8:2]	RW	DeSkew Code for CKE[1] (0x8~0x60)	0x0
CKE0DeSkewCode	[1:0]	RW	DeSkew Code for CKE[0] (0x8~0x60)	0x0

14.4.1.2.34 PHY_CON37

- Base Address: 0xC00E_1000
- Address = Base Address + 0x98, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:6]	R	Reserved (Should be zero)	–
RSTDeSkewCode	[5:0]	RW	DeSkew Code for Reset (0x8~0x38)	0x0

14.4.1.2.35 PHY_CON39

- Base Address: 0xC00E_1000
- Address = Base Address + 0xA0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved (Should be zero)	–
Da3DS	[27:25]	RW	Driver Strength Selection for Data Slice 3	0x0
Da2DS	[24:22]	RW	Driver Strength Selection for Data Slice 2	0x0
Da1DS	[21:19]	RW	Driver Strength Selection for Data Slice 1	0x0
Da0DS	[18:16]	RW	Driver Strength Selection for Data Slice 0	0x0
CaCkDrvrDS	[11:9]	RW	Driver Strength Selection for CK	0x0
CaCkeDrvrDS	[8:6]	RW	Driver Strength Selection for Cke[1:0]	0x0
CaCSDrvrDS	[5:3]	RW	Driver Strength Selection for CS[1:0]	0x0
CaAdrDrvrDS	[2:0]	RW	Driver Strength Selection for ADCT[15:0].	0x0

14.4.1.2.36 PHY_CON40

- Base Address: 0xC00E_1000
- Address = Base Address + 0xA4, Reset Value = 0x0000_0007

Name	Bit	Type	Description	Reset Value
ctrl_zq_clk_div	[31:0]	RW	ZQ Clock divider setting value	0x7

14.4.1.2.37 PHY_CON41

- Base Address: 0xC00E_1000
- Address = Base Address + 0xA8, Reset Value = 0x0000_00F0

Name	Bit	Type	Description	Reset Value
ctrl_zq_timer	[31:0]	RW	It controls the interval between each ZQ calibration	0xF0

14.4.1.2.38 PHY_CON42

- Base Address: 0xC00E_1000
- Address = Base Address + 0xAC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved (Should be zero)	–
ctrl_bstlen	[12:8]	RW	Burst Length(BL)	5'h0
RSVD	[7:5]	RW	Reserved (Should be zero)	–
ctrl_rdlat	[4:0]	RW	Read Latency(RL)	5'h0

14.4.1.3 MCUS Memory Control Register

14.4.1.3.1 MEMBW

- Base Address: 0xC005_1000
- Address = Base Address + 0x00, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31]	RW	Reserved (Should be zero)	1'b0
IntSramShadow1	[30]	RW	Base Address of Internal ROM 0 = Bass address = 0x0000_0000 1 = Bass address = 0x3400_0000	CfgBootMode
RSVD	[29:2]	RW	Reserved	1'b0
SR1BW	[1]	RW	Set data bus width of static #1 0 = Byte (8-bit) 1 = Half-word (16-bit)	1'b0
SR0BW	[0]	RW	Set data bus width of static #0 0 = Byte (8-bit) 1 = Half-word (16-bit)	CfgSTBUSWidth

14.4.1.3.2 MEMTIMEACSL

- Base Address: 0xC005_1000
- Address = Base Address + 0x04, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	RW	Reserved (Should be zero)	24'b0
TAcs1	[7:4]	RW	tACS of static #1 tACS = TACS + 1	4'b11
TAcs0	[3:0]	RW	tACS of static #0 tACS = TACS + 1 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	CfgBootMode

14.4.1.3.3 MEMTIMEACSH

- Base Address: 0xC005_1000
- Address = Base Address + 0x08, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	RW	Reserved (Should be zero)	8'b0
TAcs13	[23:19]	RW	tACS of static #13 tACS = TACS + 1 (Unit : BCLK)	4'b0
RSVD	[19:0]	RW	Reserved (Should be zero)	-

14.4.1.3.4 MEMTIMECOSL

- Base Address: 0xC005_1000
- Address = Base Address + 0x0C, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:8	RW	Reserved (Should be zero)	-
tCOS1	[7:4]	RW	tCOS of static #1 tCOS = TCOS + 1 (Unit : BCLK)	4'b11
tCOS0	[3:0]	RW	tCOS of static #0 tCOS = TCOS + 1 (Unit : BCLK) 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	CfgBootMode

14.4.1.3.5 MEMTIMECOSH

- Base Address: 0xC005_1000
- Address = Base Address + 0x10, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	RW	Reserved (Should be zero)	-
tCOS13	[23:20]	RW	tCOS of static #13 t COS = TCOS + 1 (Unit : BCLK)	4'b0
tCOS8	[19]	RW	tCOS of static #8 tCOS = TCOS + 1 (Unit : BCLK)	-

14.4.1.3.6 MEMTIMEACC0

- Base Address: 0xC005_1000
- Address = Base Address + 0x14, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved (Should be zero)	-
tACC1	[15:8]	RW	tACC of static #1	8'b01000
tACC0	[7:0]	RW	tACC of static #0	CfgBootMode

14.4.1.3.7 MEMTIMEACC1

- Base Address: 0xC005_1000
- Address = Base Address + 0x18, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:0]	RW	Reserved (Should be zero)	0x0000_0000

14.4.1.3.8 MEMTIMEACC2

- Base Address: 0xC005_1000
- Address = Base Address + 0x1C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:0]	RW	Reserved (Should be zero)	0x0000_0000

14.4.1.3.9 MEMTIMEACC3

- Base Address: 0xC005_1000
- Address = Base Address + 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16	RW	Reserved (Should be zero)	16'b0
tACC13	[15:8]	RW	tACC of static #13	8'b0
RSVD	[7:0]	RW	Reserved (Should be zero)	8'b0

14.4.1.3.10 MEMTIMESACC0

- Base Address: 0xC005_1000
- Address = Base Address + 0x24, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved (Should be zero)	16/b0
tSACC1	[15:8]	RW	tSACC of static #1	8'b0
tSACC0	[7:0]	RW	tSACC of static #0	8'b0

14.4.1.3.11 MEMTIMESACC1

- Base Address: 0xC005_1000
- Address = Base Address + 0x28, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:0]	RW	Reserved (Should be zero)	0x0000_0000

14.4.1.3.12 MEMTIMESACC2

- Base Address: 0xC005_1000
- Address = Base Address + 0x2C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:0]	RW	Reserved (Should be zero)	0x0000_0000

14.4.1.3.13 MEMTIMESACC3

- Base Address: 0xC005_1000
- Address = Base Address + 0x30, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	RW	Reserved (Should be zero)	16'b0
tSACC13	[15:8]	RW	tSACC of static #13	8'b0
RSVD	[7:0]	RW	Reserved (Should be zero)	8'b0

14.4.1.3.14 MEMTIMECOHL

- Base Address: 0xC005_1000
- Address = Base Address + 0x44, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	RW	Reserved (Should be zero)	24'b0
tCOH1	[7:4]	RW	tCOH of static #1	4'b11
tCOH0	[3:0]	RW	tCOH of static #0 tCOH = TCOH + 1 (Unit : BCLK) 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	CfgBootMode

14.4.1.3.15 MEMTIMECOHH

- Base Address: 0xC005_1000
- Address = Base Address + 0x48, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31::24]	RW	Reserved (Should be zero)	8'b0
tCOH13	[23:20]	RW	tCOH of static #13.	4'b0
RSVD	[19:0]	RW	Reserved	20'b0

14.4.1.3.16 MEMTIMECAHL

- Base Address: 0xC005_1000
- Address = Base Address + 0x4C, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	RW	Reserved (Should be zero)	24'b0
tCAH1	[7:4]	RW	tCAH of static #1	4'b11
tCAH0	[3:0]	RW	tCAH of static #0 tCAH = TCAH + 1 (Unit : BCLK) 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	CfgBootMode

14.4.1.3.17 MEMTIMECAHH

- Base Address: 0xC005_1000
- Address = Base Address + 0x50, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	RW	Reserved (Should be zero)	8'b0
tCAH13	[23:20]	RW	tCAH of static #13	4'b0
RSVD	[19:0]	RW	Reserved	20'b0

14.4.1.3.18 MEMBURSTL

- Base Address: 0xC005_1000
- Address = Base Address + 0x54, Reset Value = 0x0000_0008

Name	Bit	Type	Description	Reset Value
RSVD	[9:8]	RW	Reserved (Should be zero)	2'b0
BWRITE1	[7:6]	RW	Write Access Control of static #1 00 = Disable 01 = 4 byte burst Access 10 = 8 byte burst Access 11 = 16 byte burst Access	2'b00
BREAD1	[5:4]	RW	Read Access Control of static #1 00 = Disable 01 = 4 byte burst Access 10 = 8 byte burst Access 11 = 16 byte burst Access	2'b01
BWRITE0	[3:2]	RW	Write Access Control of static #0 00 = Disable 01 = 4 byte burst Access 10 = 8 byte burst Access 11 = 16 byte burst Access	2'b00
BREAD0	[1:0]	RW	Read Access Control of static #0 00 = Disable 01 = 4 byte burst Access 10 = 8 byte burst Access 11 = 16 byte burst Access	2'b00

14.4.1.3.19 MEMWAIT

- Base Address: 0xC005_1000
- Address = Base Address + 0x5C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	RW	Reserved (Should be zero)	'b0
WAITENB1	[3]	RW	Wait Enable control of static #1 0 = Disable Wait Control 1 = Enable Wait Control	1'b0
WAITPOL1	[2]	RW	Wait Polarity control of static #1 If it is set to low active wait signal, the wait is enabled when the input signal is low. If it is set to high active wait signal, the wait is enabled when the input signal is high. 0 = High active wait signal 1 = Low active wait signal	1'b0
WAITENB0	[1]	RW	Wait Enable control of static #0 0 = Disable Wait Control 1 = Enable Wait Control	1'b0
WAITPOL0	[0]	RW	Wait Polarity control of static #0 If it is set to low active wait signal, the wait is enabled when the input signal is low. If it is set to high active wait signal, the wait is enabled when the input signal is high. 0 = High active wait signal 1 = Low active wait signal	1'b0

14.4.1.3.20 NFCONTROL

- Base Address: 0xC005_1000
- Address = Base Address + 0x1088, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
NCSENB	[31]	RW	nNCS Enable 0 = Disable 1 = Enable	1'b0
NFECCAUTORSTENB	[30]	RW	0 = Auto Reset Disable 1 = Auto Reset Enable	1'b1
NFECCMode	[29:27]	RW	Number of Error correction bit 0 = 4-bit 1 = 8-bit 2 = 12-bit 3 = 16-bit 4 = 24-bit (Only data Size 1024 byte) 5 = 24 bits 6 = 40 bits (Only data Size 1024 byte) 7 = 60 bits (Only data Size 1024 byte)	3'b000
RSVD	[26:16]	R	Reserved (Should be zero)	11'b0
IRQPEND	[15]	RW	Interrupt pending bit of RnB signal detect. Read: 0 = Not pended 1 = Pended Writ: 0 = No affect 1 = Clear	1'bx
ECCIRQPEND	[14]	RW	Interrupt pending bit of ECC Done signal detect. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'bx
RSVD	[14:12]	R	Reserved (Should be zero)	3'h0
ECCrst	[11]	W	HW ECC block reset NFECCL, NFECCH, NFCNT, NFECCSTATUS, NFSYNDRONE31/75 Registers Reset	1'b0
RSVD	[10]	R	Reserved (Should be zero)	1'bx
RnB	[9]	R	Ready/Busy check of NAND Flash operation. 0 = Busy 1 = Ready	1'bx
IRQENB	[8]	RW	Set interrupt enable/disable at the rising edge of RnB	1'b0

Name	Bit	Type	Description	Reset Value
			signal of NAND Flash. 0 = Disable 1 = Enable	
ECCIRQENB	[7]	RW	Set interrupt enable/disable ECC done signal of NAND Flash controller. 0 = Disable 1 = Enable	1'b0
NFCartrideENB	[6:5]	RW	Set NAND Flash Cartridge Enable Used SDEX bus of NAND access. Write 00 = Disable 01 = Enable Read 00 = Disable 10 = Enable	1'b0
NFTYPE	[4:3]	RW	Set NAND Flash Type for NAND Booting. 00 = Small block 3 address NAND 01 = Small block 4 address NAND 10 = Large block 4 address NAND 11 = Large block 5 address NAND	CfgNFType
RSVD	[2]	RW	Reserved (Should be zero)	1'b0
NFBANK	[1:0]	RW	Set NAND Flash bank for access. This bit determines which one will be selected out of nNCS[2:0]. Selected nNCS applied after NFBANK is changed and static memory is accessed. 0 = nNCS[0] 1 = nNCS[1] 2 = nNCS[2] 3 = Reserved	2'b00

14.4.1.3.21 NFECCTRL

- Base Address: 0xC005_1000
- Address = Base Address + 0x108C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	R	Reserved (Should be zero)	–
ERROR	[28]	R	Result of Decode 0 = No Error 1 = Error	1'b0
NUMBEROFERROR	[28]	W	Number Of Error	5'h0
DECMODE	[24]	RW	0 = Encoder 1 = Decoder	1'b0
Loadelp	[27]	W	Load ELP Register	–
DECMODE	[26]	W	0 = Encoder 1 = Decoder	1'b0
RSVD	[25]	RW	Reserved (Must be zero)	–
NUMBEROFELP	[24:18]	RW	Number Of ELP When NFECCMODE Register = 0 then 4 When NFECCMODE Register = 1 then 8 When NFECCMODE Register = 2 then 12 When NFECCMODE Register = 3 then 16 When NFECCMODE Register = 4 then 24	5'h0
PARITYCONUT	[17:10]	RW	Number of Parity byte When NFECCMODE Register = 0 then 5 When NFECCMODE Register = 1 then 12 When NFECCMODE Register = 2 then 18 When NFECCMODE Register = 3 then 25 When NFECCMODE Register = 4 then 41	6'h0
NFCOUNTVALUE	[9:0]	RW	Number of NAND Read and Write data When NFECCMODE Register = 0 to 3 then 512 When NFECCMODE Register = 4 then 1024	10'h0

14.4.1.3.22 NFCNT

- Base Address: 0xC005_1000
- Address = Base Address + 0x90, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	R	Reserved (Should be zero)	6'h0
nfwrcnt	[25:16]	R	NAND Flash Write Data Count	–
RSVD	[15:10]	R	Reserved (Should be zero)	6'h0
NFRDCNT	[9:0]	R	NAND Flash Read Data Count	–

14.4.1.3.23 NFECCSTATUS

- Base Address: 0xC005_1000
- Address = Base Address + 0x94, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:22]	R	Reserved (Should be zero)	10'h0
NUMELPERROR	[21:16]	R	Number of ELP Error	6'b
RSVD	[15:12]	R	Reserved (Should be zero)	4'h0
NFERRFLAG	[11]	R	If ECC check data error occurs, SYNDROMERROR is set as "1" When reading ECC Register Data, it's cleared. 0 = No Error 1 = Error	1'b0
NUMECCERROR	[10:4]	R	Number of ECC Error	7'b0
SYNDROMERROR	[3]	R	If Syndrom check data error occurs, SYNDROMERROR is set as "1" When reading ECC Register Data, it's cleared. 0 = No Error 1 = Error	1'b0
NFCHECKERROR	[2]	R	When completing NAND Read operating, error check on Read Data. If Read Data Error occurs, NFCHECKERROR is set as "1". Then NAND Address/Command wirites, the register is cleared. 0 = No Error 1 =Data Error	1'b0
NFECCDECDONe	[1]	R	When reading NAND Data with 512 byte plus 51 Cycles (BCLK), NFECCDECDONE is set as "1". When NAND Address/Command wirites, it's cleared. 0 = IDLE or RUN 1 = End	1'b0

Name	Bit	Type	Description	Reset Value
NFECCENCDONE	[0]	R	After writing NAND DATA with 512 byte, NFECCENCDONE is set as "1". When reading ECC Register Data, it's cleared. 0 = IDLE or RUN 1 = End	1'b0

14.4.1.3.24 NFTIMEACS

- Base Address: 0xC005_1000
- Address = Base Address + 0x98, Reset Value = 0x0000_0007

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	RW	Reserved (Should be zero)	20'b0
tnfacs2	[11:8]	RW	NAND tNFACS of Nand Bank 2	4'h0
tnfacs1	[7:4]	RW	NAND tNFACS of Nand Bank 1	4'h0
tnfacs0	[3:0]	RW	NAND tNFACS of Nand Bank 0 tNFACS = TNFACS + 1 (Unit : BCLK) 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	4'h7

14.4.1.3.25 NFTIMECOS

- Base Address: 0xC005_1000
- Address = Base Address + 0x9C, Reset Value = 0x0000_0007

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	RW	Reserved (Should be zero)	20'b0
tnfcos2	[11:8]	RW	NAND tNFCOS of Nand Bank 2	4'h0
tnfcos1	[7:4]	RW	NAND tNFCOS of Nand Bank 1	4'h0
tnfcos0	[3:0]	RW	NAND tNFCOS of Nand Bank 0 tNFCOS = TNFCOS + 1 (Unit : BCLK) 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	4'h7

14.4.1.3.26 NFTIMEACC0

- Base Address: 0xC005_1000
- Address = Base Address + 0xA0, Reset Value = 0x0000_000F

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	RW	Reserved (Should be zero)	8'b0
tNFacc2	[23:16]	RW	tANFCC of NAND Bank 2	8'h00
tNFacc1	[15:8]	RW	tANFCC of NAND Bank 1	8'h00
tNFacc0	[7:0]	RW	tANFCC of NAND Bank 0 tNFACC = TNFACC +1 Cycle	8'h0f

14.4.1.3.27 NFTIMEOCH

- Base Address: 0xC005_1000
- Address = Base Address + 0xA8, Reset Value = 0x0000_0007

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	RW	Reserved (Should be zero)	20'b0
tnfOCH2	[11:8]	RW	NAND tNFOCH of Nand Bank 2	4'h0
tnfOCH1	[7:4]	RW	NAND tNFOCH of Nand Bank 1	4'h0
tnfOCH0	[3:0]	RW	NAND tNFOCH of Nand Bank 0 tNFOCH = TNFOCH + 1 (Unit : BCLK) 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	4'h7

14.4.1.3.28 NFTIMECAH

- Base Address: 0xC005_1000
- Address = Base Address + 0xAC, Reset Value = 0x0000_0007

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	RW	Reserved (Should be zero)	20'b0
tnfcAH2	[11:8]	RW	NAND tNFCOS of Nand Bank 2	4'h0
tnfcAH1	[7:4]	RW	NAND tNFCOS of Nand Bank 1	4'h0
tnfcAH0	[3:0]	RW	NAND tNFCAH of Nand Bank 0 tNFCAH = TNFCAH + 1 (Unit : BCLK) 0000 = 1 cycle 0001 = 2 cycle 0010 = 3 cycle 0011 = 4 cycle 0100 = 5 cycle 0101 = 6 cycle 0110 = 7 cycle 0111 = 8 cycle 1000 = 9 cycle 1001 = 10 cycle 1010 = 11 cycle 1011 = 12 cycle 1100 = 13 cycle 1101 = 14 cycle 1110 = 15 cycle 1111 = 0 cycle	4'h7

14.4.1.3.29 NFECCn (n = 0 to 26)

- Base Address: 0xC005_1000
- Address = Base Address + 0x10B0, + 0x10B4, + 0x10B8, + 0x10BC, + 0x10C0, + 0x10C4, + 0x10C8, + 0x10CC, + 0x10D0, + 0x10D4, + 0x10D8, + 0x10DC, + 0x10E0, + 0x10E4, + 0x10E8, + 0x10EC, + 0x10F0, + 0x10F4, + 0x10F8, + 0x10FC, + 0x1100, + 0x1104, + 0x1108, + 0x110C, + 0x1110, + 0x1114, + 0x1118, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ECC[n]	[31:0]	R	Represents 512/1024 byte ECC parity code during Write operation by H/W ECC generation block	32'h0

14.4.1.3.30 NFORGECCn (n = 0 to 26)

- Base Address: 0xC005_1000
- Address = Base Address + 0x111C, + 0x1120, + 0x1124, + 0x1128, + 0x112C, + 0x1130, + 0x1134, + 0x1138, + 0x113C, + 0x1140, + 0x1144, + 0x1148, + 0x114C, + 0x1150, + 0x1154, + 0x1158, + 0x115C, + 0x1160, + 0x1164, + 0x1168, + 0x116C, + 0x1170, + 0x1174, + 0x1178, + 0x117C, + 0x1180, + 0x1184, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ORGECC[n]	[31:0]	RW	When NAND Read operates, firstly read Original ECC Data already saved in the NAND Spare area and then wrties in Register.	32'h0

14.4.1.3.31 NFSYNDROMEn (n = 0 to 29)

- Base Address: 0xC005_1000
- Address = Base Address + 0x1188, + 0x118C, + 0x1190, + 0x1194, + 0x1198, + 0x119C, + 0x11A0, + 0x11A4, + 0x11A8, + 0x11AC, + 0x11B0, + 0x11B4, + 0x11B8, + 0x11BC, + 0x11C0, + 0x11C4, + 0x11C8, + 0x11CC, + 0x11D0, + 0x11D4, + 0x11D8 + 0x11DC, + 0x11E0, + 0x11E4, + 0x11E8, + 0x11EC, + 0x11F0, + 0x11F4, + 0x11F8, + 0x11FC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved (Should be zero)	2'b0
SYNDROM [3+(nx4)]	[29:16]	R	ECC Decoder Result Odd Syndrome Data3 (offset n x4)	14'h0
RSVD	[15:14]	R	Reserved (Should be zero)	2'b0
SYNDROM [1+(nx4)]	[13:0]	R	ECC Decoder Result Odd Syndrome Data1 (offset n x4)	14'h0

14.4.1.3.32 NFELPn (n = 0 to 59)

- Base Address: 0xC005_1000
- Address = Base Address + 0x1200, 0x1204, 0x1208, 0x120C, 0x1210, 0x1214, 0x1218, 0x121C, 0x1220, 0x1224, 0x1228, 0x122C, 0x1230, 0x1234, 0x1238, 0x123C, 0x1240, 0x1244, 0x1248, 0x124C, 0x1250, 0x1254, 0x1258, 0x125C, 0x1260, 0x1264, 0x1268, 0x126C, 0x1270 0x1274, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	RW	Reserved (Should be zero)	–
ELP[2+(nx2)	[27:14]	RW	2nd ELP (Error locator polynomial) register	–
ELP[1+(nx2)]	[13:0]	RW	1st t ELP (Error locator polynomial) register	–

14.4.1.3.33 NFERRORLOCATIONn (n = 0 to 59)

- Base Address: 0xC005_1000
- Address = Base Address + 0x1278, 0x127C, 0x1280, 0x1284, 0x1288, 0x128C, 0x1290, 0x1294, 0x1298, 0x129C, 0x12A0, 0x12A4, 0x12A8, 0x12AC, 0x12B0, 0x12B4, 0x12B8, 0x12BC, 0x12C0, 0x12C4, 0x12C8, 0x12CC, 0x12D0, 0x12D4, 0x12D8, 0x12DC, 0x12E0, 0x12E4, 0x12E8, 0x12EC, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved (Should be zero)	–
Error[2+(nx2)]	[27:14]	R	2nd location of error	–
Error[1+(nx2)]	[13:0]	R	1st location of error	–

14.4.1.3.34 AUTO SYNDROM REGISTER(AUTOSYND)

- Base Address: 0xC005_1000
- Address = Base Address + 0x12F0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved (Should be zero)	–
CPUSYND	[1]	W	User can write the SYNDROM value or auto SYNDROM value. 0 = Auto 1 = User write	1'b0
CPUELP	[0]	W	User can write the ELP value or auto ELP value. 0 = Auto 1 = User write	1'b0

14.4.1.3.35 NFWSYNDRONEn (n = 0 to 29)

- Base Address: 0xC005_1000
- Address = Base Address + 0x12F4, 0x12F8, 0x12FC, 0x1300, 0x1304, 0x1308, 0x130C, 0x1310, 0x1314, 0x1318, 0x131C, 0x1320, 0x1324, 0x1328, 0x132C, 0x1330, 0x1334, 0x1338, 0x133C, 0x1340, 0x1344, 0x1348, 0x134C, 0x1350, 0x1354, 0x1358, 0x135C, 0x1360, 0x1364, 0x1368, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved (Should be zero)	2'b0
SYNDROM [3+(nx4)]	[29:16]	W	ECC Decoder Result Odd Syndrome Data3 (offset n x4)	14'h0
RSVD	[15:14]	R	Reserved	2'b0
SYNDROM [1+(nx4)]	[13:0]	W	ECC Decoder Result Odd Syndrome Data1 (offset n x4)	14'h0

14.4.1.4 MCUS Memory Control Register

14.4.1.4.1 NFDATA

- Base Address: 0x2C00_0000
- Address = Base Address + 0x0000, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
NFDATA	[31:0]	RW	NAND flash data register. In case of 16-bit access on this register, it generates 8-bit access cycle in twice automatically. In case of 32-bit access on this register, it also generates four 8-bit access cycles automatically.	–

14.4.1.4.2 NFCMD

- Base Address: 0x2C00_0000
- Address = Base Address + 0x0010, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[15:8]	–	Reserved (Should be zero)	8'h0
NFCMD	[7:0]	W	NAND flash command register. Writing on this register generates a command cycle with CLE signal and transfers this value on data bus automatically. You have to write only 8-bit data on this register. Do not access this register with 16/32-bit data.	8'hx

14.4.1.4.3 NFADDR

- Base Address: 0x2C00_0000

- Address = Base Address + 0x0018, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[15:8]	–	Reserved (Should be zero)	8'hx
NFADDR	[7:0]	W	NAND flash address register. Writing on this register generates an address cycle with ALE signal and transfers this value on data bus automatically. You have to write only 8-bit data on this register. Do not access this register with 16/32-bit access. Only byte access is available.	8'hx

15 GPIO Controller

15.1 Overview

15.1.1 Features

- Programmable Pull-Up Control
- Edge/Level Detect
- Supports programmable Pull-Up resistance.
- Supports four event detection modes
  - Rising Edge Detection
  - Falling Edge Detection
  - Low Level Detection
  - High Level Detection
- The number of GPIOs: 160

15.2 Block Diagram

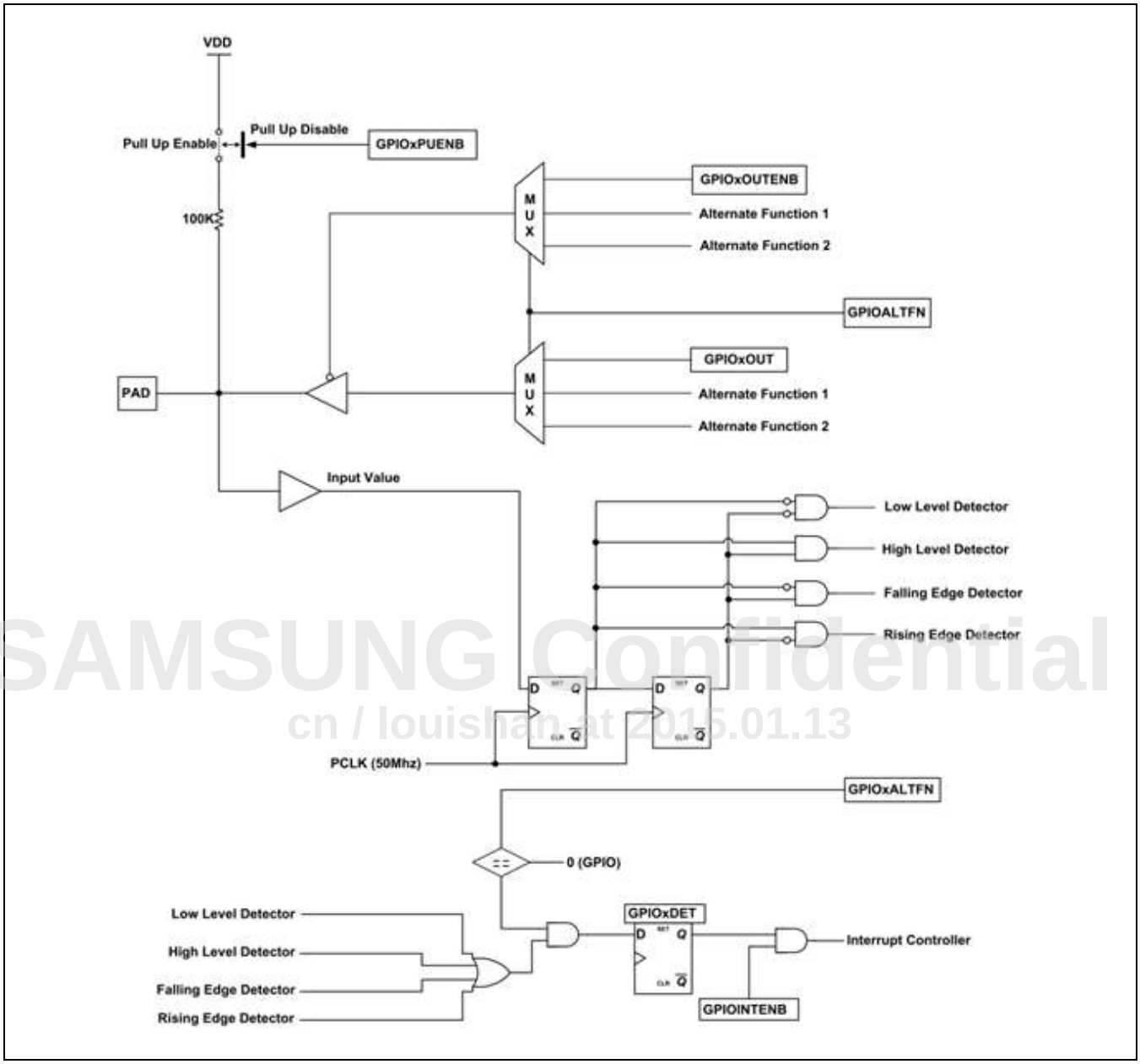


Figure 15-1 GPIO Block Diagram

15.3 Functional Description

S5P4418 GPIO Pins have an internal pull-up resistance of 100 kΩ.

The current of the pull-up resistance (for VDD = 3.3 V and V (PAD) = 0 V) is listed in the table below:

Pull Up	Min.	Typ.	Max.	Unit
ENABLE	10	33	72	uA
DISABLE	–	–	0.1	uA

Most S5P4418 GPIO ports contain the Alternate function (some ports supports up to Alternate Function2). All GPIO ports should be set as GPIO function or Alternate Function suitable for the user's purposes and this setting can easily be performed with GPIO registers. In addition, all GPIO pull-up resistances are enabled/ disabled. This setting operates when the system is fully booted and does not affect the system in initial booting. If there is a value which needs to be determined in system booting, the value is given by inserting a pull up/down resistance from outside.

15.3.1 Input Operation

To use GPIO for input, the GPIO function should be selected by setting the relevant bit of the GPIO Alternate Function Select register as b'00 to select the GPIO function. In addition, the GPIO Input mode should be, also, selected by the GPIOx Output Enable register (GPIOxOUTENB) as “0”.

An input signal is detected by selecting a desired detection type with the GPIOx Event Detect Mode register. Four types of input signal can be detected: Low Level, High Level, Falling edge and Rising edge. The GPIOx Event Detect Mode registers consist of GPIOx Event Detect Mode register0 (GPIOxDETMODE0) and GPIOx Event Detect Moderegister1 (GPIOxDETMODE1).

To use interrupt, set the GPIOx Interrupt Enable Register (GPIOxINTENB) as “1”.

The GPIOx Event Detect Register (GPIOxDET) enables checking the generation of an event via GPIO and may be used as the Pending Clear function when an interrupt occurs.

When the GPIOx PAD Status Register (GPIOxPAD) is set as GPIO Input mode, the levelof the relevant GPIOx PAD can be checked.

The Open drain pins (GPIOB[7:4] and GPIOC[8]) operate in Input mode only when the GPIOx Output register (GPIOxOUT) is set as “1”. The Open drain pins are operated by the GPIOx Output Register (GPIOxOUT) even if the GPIOx Output Enable register (GPIOxOUTENB) is set as Input mode.

15.3.2 Output Operation

To use GPIO for output, the GPIO function should be selected by setting the relevant bit of the GPIOx. Alternate Function Select register should be set as b'00 to select the GPIO function. In addition, the GPIOx Output mode should also be selected by setting the GPIOx Output Enable register as "1".

If you set a desired output value (low level: "0", high level: "1") with the GPIOx Output Register (GPIOxOUT), the value is reflected to the corresponding bit.

The Open drain pins (GPIOB[7:4] and GPIOC[8]) operate in output mode only when the GPIOx Output register (GPIOxOUT) is set as "0". The Open drain pins are operated by the GPIOx Output Register (GPIOxOUT) even if the GPIOx Output Enable register(GPIOxOUTENB) is set as Input mode.

15.3.3 Alternate Function Operation

Among the 151 GPIO pins of the S5P4418, most GPIO pins have an Alternate function. However, the Alternate function and the GPIO function should not be used simultaneously. Therefore, Alternate Function1 and Alternate Function2 are operated by setting the corresponding bits of the GPIOx Alternate Function Select register as b'01 and b'10, respectively.

15.4 Register Description

15.4.1 Register Map Summary

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)

Register	Offset	Description	Reset Value
GPIOxOUT	A000h, B000h, C000h, D000h, E000h	GPIOx output register	32'h0
GPIOxOUTENB	A004h, B004h, C004h, D004h, E004h	GPIOx output enable register	32'h0
GPIOxDETMODE0	A008h, B008h, C008h, D008h, E008h	GPIOx event detect mode register 0	2'b00
GPIOxDETMODE1	A00Ch, B00Ch, C00Ch, D00Ch, E00Ch	GPIOx event detect mode register 1	2'b00
GPIOxINTENB	A010h, B010h, C010h, D010h, E010h	GPIOx interrupt enable register	32'h0
GPIOxDET	A014h, B014h, C014h, D014h, E014h	GPIOx event detect register	32'h0
GPIOxPAD	A018h, B018h, C018h, D018h, E018h	GPIOx PAD status register	32'h0
RSVD	A01Ch, B01Ch,C	Reserved	Undefined

Register	Offset	Description	Reset Value
	01Ch,D01Ch,E01Ch		
GPIOxALTFN0	A020h, B020h, C020h, D020h, E020h	GPIOx alternate function select register 0	2'b00
GPIOxALTFN1	A024h, B024h, C024h, D024h, E024h	GPIOx alternate function select register 1	2'b00
GPIOxDETMODEEX	A028h, B028h, C028h, D028h, E028h	GPIOx event detect mode extended register	1'b0
GPIOxDETENB	A03Ch, B03Ch, C03Ch, D03Ch, E03Ch	GPIOx detect enable register	32'h0
GPIOx_SLEW	A040h, B040h, C040h, D040h, E040h	GPIOx slew register	32'hffffffff
GPIOx_SLEW_DISABLE_DEFAULT	A044h, B044h, C044h, D044h, E044h	GPIOx slew disable default register	32'hffffffff
GPIOx_DRV1	A048h, B048h, C048h, D048h, E048h	GPIOx DRV1 register	32'h0
GPIOx_DRV1_DISABLE_DEFAULT	A04Ch, B04Ch, C04Ch, D04Ch, E04Ch	GPIOx DRV1 disable default register	32'hffffffff
GPIOx_DRV0	A050h, B050h, C050h, D050h,	GPIOx DRV0 register	32'h0

Register	Offset	Description	Reset Value
	E050h		
GPIOx_DRV0_DISABLE_DEFAULT	A054h, B054h, C054h, D054h, E054h	GPIOx DRV0 disable default register	32'hffffffff
GPIOx_PULLSEL	A058h, B058h, C058h, D058h, E058h	GPIOx PULLSEL register	32'h0
GPIOx_PULLSEL_DISABLE_DEFAULT	A05Ch, B05Ch, C05Ch, D05Ch, E05Ch	GPIOx PULLSEL disable default register	32'h0
GPIOx_PULLENB	A060h, B060h, C060h, D060h, E060h	GPIOx PULLENB register	32'h0
GPIOx_PULLENB_DISABLE_DEFAULT	A064h, B064h, C064h, D064h, E064h	GPIOx PULLENB disable default register	32'h0

NOTE: "GPIOx Register (x = A, B, C, D, E)

15.4.1.1 GPIOxOUT

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A000h, + B000h, + C000h, + D000h, + E000h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOXOUT	[31:0]	RW	GPIOx[31:0]: Specifies the output value in GPIOx output mode. NOTE: This bit should be set as "1" (Input mode) or "0" (Output mode) to use the Open drain pins in Input/Output mode. 0 = Low Level 1 = High Level	32'h0

15.4.1.2 GPIOxOUTENB

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A004h, + B004h, + C004h, + D004h, + E004h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOXOUTENB	[31:0]	RW	GPIOx[31:0]: Specifies GPIOx In/Out mode. NOTE: The Open drain pins are operated in Input/Output mode by the GPIOxOUTPUT register (GPIOxOUT) and not by this bit. 0 = Input Mode 1 = Output Mode	32'h0

15.4.1.3 GPIOxDETMODE0

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A008h, + B008h, + C008h, + D008h, + E008h, Reset Value = 2'b00

Name	Bit	Type	Description	Reset Value
GPIOXDETMODE0_15	[31:30]	RW	Specifies Detect mode when GPIOx15 is in Input mode. It is configured the combination of GPIOXDET_EX15 (1-bit) + GPIOXDETMODE0_15 (2-bit). Considers GPIOXDET_EX15 as well as GPIOXDETMODE0_15. NOTE: First bit is GPIOXDET_EX15 Second and third bit is GPIOXDETMODE0_15 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_14	[29:28]	RW	Specifies Detect mode when GPIOx14 is in Input mode. It is configured the combination of GPIOXDET_EX14 (1-bit) + GPIOXDETMODE0_14 (2-bit). Considers GPIOXDET_EX14 as well as GPIOXDETMODE0_14. NOTE: First bit is GPIOXDET_EX14 Second and third bit is GPIOXDETMODE0_14 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_13	[27:26]	RW	Specifies Detect mode when GPIOx13 is in Input mode. It is configured the combination of GPIOXDET_EX13 (1-bit) + GPIOXDETMODE0_13 (2-bit). Considers GPIOXDET_EX13 as well as GPIOXDETMODE0_13. NOTE: First bit is GPIOXDET_EX13	2'b00

Name	Bit	Type	Description	Reset Value
			Second and third bit is GPIOXDETMODE0_13 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDETMODE0_12	[25:24]	RW	Specifies Detect mode when GPIOx12 is in Input mode. It is configured the combination of GPIOXDET_EX12 (1-bit) + GPIOXDETMODE0_12 (2-bit). Considers GPIOXDET_EX12 as well as GPIOXDETMODE0_12. NOTE: First bit is GPIOXDET_EX12 Second and third bit is GPIOXDETMODE0_12 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_11	[23:22]	RW	Specifies Detect mode when GPIOx11 is in Input mode. It is configured the combination of GPIOXDET_EX11 (1-bit) + GPIOXDETMODE0_11 (2-bit). Considers GPIOXDET_EX11 as well as GPIOXDETMODE0_11. NOTE: First bit is GPIOXDET_EX11 Second and third bit is GPIOXDETMODE0_11 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_10	[21:20]	RW	Specifies Detect mode when GPIOx10 is in Input mode. It is configured the combination of GPIOXDET_EX10 (1-bit) + GPIOXDETMODE0_10 (2-bit). Considers GPIOXDET_EX10 as well as GPIOXDETMODE0_10. NOTE: First bit is GPIOXDET_EX10 Second and third bit is GPIOXDETMODE0_10 000 = Low Level	2'b00

Name	Bit	Type	Description	Reset Value
			001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDETMODE0_9	[19:18]	RW	Specifies Detect mode when GPIOx9 is in Input mode. It is configured the combination of GPIOXDET_EX9 (1-bit) + GPIOXDETMODE0_9 (2-bit). Considers GPIOXDET_EX9 as well as GPIOXDETMODE0_9. NOTE: First bit is GPIOXDET_EX9 Second and third bit is GPIOXDETMODE0_9 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_8	[17:16]	RW	Specifies Detect mode when GPIOx8 is in Input mode. It is configured the combination of GPIOXDET_EX8 (1-bit) + GPIOXDETMODE0_8 (2-bit.). Considers GPIOXDET_EX8 as well as GPIOXDETMODE0_8. NOTE: First bit is GPIOXDET_EX8 Second and third bit is GPIOXDETMODE0_8 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_7	[15:14]	RW	Specifies Detect mode when GPIOx7 is in Input mode. It is configured the combination of GPIOXDET_EX7 (1-bit) + GPIOXDETMODE0_7 (2-bit). Considers GPIOXDET_EX7 as well as GPIOXDETMODE0_7. NOTE: First bit is GPIOXDET_EX7 Second and third bit is GPIOXDETMODE0_7 000 = Low Level 001 = High Level 010 = Falling Edge	2'b00

Name	Bit	Type	Description	Reset Value
			011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDETMODE0_6	[13:12]	RW	Specifies Detect mode when GPIOx6 is in Input mode. It is configured the combination of GPIOXDET_EX6 (1-bit) + GPIOXDETMODE0_6 (2-bit). Considers GPIOXDET_EX6 as well as GPIOXDETMODE0_6. NOTE: First bit is GPIOXDET_EX6 Second and third bit is GPIOXDETMODE0_6 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_5	[11:10]	RW	Specifies Detect mode when GPIOx5 is in Input mode. It is configured the combination of GPIOXDET_EX5 (1-bit) + GPIOXDETMODE0_5 (2-bit). Considers GPIOXDET_EX5 as well as GPIOXDETMODE0_5. NOTE: First bit is GPIOXDET_EX5 Second and third bit is GPIOXDETMODE0_5 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_4	[9:8]	RW	Specifies Detect mode when GPIOx4 is in Input mode. It is configured the combination of GPIOXDET_EX4 (1-bit) + GPIOXDETMODE0_4 (2-bit). Considers GPIOXDET_EX4 as well as GPIOXDETMODE0_4. NOTE: First bit is GPIOXDET_EX4 Second and third bit is GPIOXDETMODE0_4 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge	2'b00

Name	Bit	Type	Description	Reset Value
			101 to 111 = Reserved	
GPIOXDETMODE0_3	[7:6]	RW	Specifies Detect mode when GPIOx3 is in Input mode. It is configured the combination of GPIOXDET_EX3 (1-bit) + GPIOXDETMODE0_3 (2-bit). Considers GPIOXDET_EX3 as well as GPIOXDETMODE0_3. NOTE: First bit is GPIOXDET_EX3 Second and third bit is GPIOXDETMODE0_3 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_2	[5:4]	RW	Specifies Detect mode when GPIOx2 is in Input mode. It is configured the combination of GPIOXDET_EX2 (1-bit) + GPIOXDETMODE0_2 (2-bit). Considers GPIOXDET_EX2 as well as GPIOXDETMODE0_2. NOTE: First bit is GPIOXDET_EX2 Second and third bit is GPIOXDETMODE0_2 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_1	[3:2]	RW	Specifies Detect mode when GPIOx1 is in Input mode. It is configured the combination of GPIOXDET_EX1 (1-bit) + GPIOXDETMODE0_1 (2-bit). Considers GPIOXDET_EX1 as well as GPIOXDETMODE0_1. NOTE: First bit is GPIOXDET_EX1 Second and third bit is GPIOXDETMODE0_1 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE0_	[1:0]	RW	Specifies Detect mode when GPIOx0 is in Input mode.	2'b00

Name	Bit	Type	Description	Reset Value
0			It is configured the combination of GPIOXDET_EX0 (1-bit) + GPIOXDETMODE0_0 (2-bit). Considers GPIOXDET_EX0 as well as GPIOXDETMODE0_0. NOTE: First bit is GPIOXDET_EX0 Second and third bit is GPIOXDETMODE0_0 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	

15.4.1.4 GPIOxDETMODE1

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A00Ch, + B00Ch, + C00Ch, + D00Ch, + E00Ch, Reset Value = 2'b00

Name	Bit	Type	Description	Reset Value
GPIOXDETMODE1_31	[31:30]	RW	Specifies Detect mode when GPIOx31 is in Input mode. It is configured the combination of GPIOXDET_EX31 (1-bit) + GPIOXDETMODE1_31 (2-bit). Considers GPIOXDET_EX31 as well as GPIOXDETMODE1_31. NOTE: First bit is GPIOXDET_EX31 Second and third bit is GPIOXDETMODE1_31 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_30	[29:28]	RW	Specifies Detect mode when GPIOx30 is in Input mode. It is configured the combination of GPIOXDET_EX30 (1-bit) + GPIOXDETMODE1_30 (2-bit). Considers GPIOXDET_EX30 as well as GPIOXDETMODE1_30. NOTE: First bit is GPIOXDET_EX30 Second and third bit is GPIOXDETMODE1_30 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_29	[27:26]	RW	Specifies Detect mode when GPIOx29 is in Input mode. It is configured the combination of GPIOXDET_EX29 (1-bit) + GPIOXDETMODE1_29 (2-bit). Considers GPIOXDET_EX29 as well as GPIOXDETMODE1_29. NOTE: First bit is GPIOXDET_EX29	2'b00

Name	Bit	Type	Description	Reset Value
			Second and third bit is GPIOXDETMODE1_29 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDETMODE1_28	[25:24]	RW	Specifies Detect mode when GPIOx28 is in Input mode. It is configured the combination of GPIOXDET_EX28 (1-bit) + GPIOXDETMODE1_28 (2-bit). Considers GPIOXDET_EX28 as well as GPIOXDETMODE1_28. NOTE: First bit is GPIOXDET_EX28 Second and third bit is GPIOXDETMODE1_28 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_27	[23:22]	RW	Specifies Detect mode when GPIOx27 is in Input mode. It is configured the combination of GPIOXDET_EX27 (1-bit) + GPIOXDETMODE1_27 (2-bit). Considers GPIOXDET_EX27 as well as GPIOXDETMODE1_27. NOTE: First bit is GPIOXDET_EX27 Second and third bit is GPIOXDETMODE1_27 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_26	[21:20]	RW	Specifies Detect mode when GPIOx26 is in Input mode. It is configured the combination of GPIOXDET_EX26 (1-bit) + GPIOXDETMODE1_26 (2-bit). Considers GPIOXDET_EX26 as well as GPIOXDETMODE1_26. NOTE: First bit is GPIOXDET_EX26 Second and third bit is GPIOXDETMODE1_26 000 = Low Level	2'b00

Name	Bit	Type	Description	Reset Value
			001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDETMODE1_25	[19:18]	RW	Specifies Detect mode when GPIOx25 is in Input mode. It is configured the combination of GPIOXDET_EX25 (1-bit) + GPIOXDETMODE1_25 (2-bit). Considers GPIOXDET_EX25 as well as GPIOXDETMODE1_25. NOTE: First bit is GPIOXDET_EX25 Second and third bit is GPIOXDETMODE1_25 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_24	[17:16]	RW	Specifies Detect mode when GPIOx24 is in Input mode. It is configured the combination of GPIOXDET_EX24 (1-bit) + GPIOXDETMODE1_24 (2-bit). Considers GPIOXDET_EX24 as well as GPIOXDETMODE1_24. NOTE: First bit is GPIOXDET_EX24 Second and third bit is GPIOXDETMODE1_24 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_23	[15:14]	RW	Specifies Detect mode when GPIOx23 is in Input mode. It is configured the combination of GPIOXDET_EX23 (1-bit) + GPIOXDETMODE1_23 (2-bit). Considers GPIOXDET_EX23 as well as GPIOXDETMODE1_23. NOTE: First bit is GPIOXDET_EX23 Second and third bit is GPIOXDETMODE1_23 000 = Low Level 001 = High Level 010 = Falling Edge	2'b00

Name	Bit	Type	Description	Reset Value
			011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDETMODE1_22	[13:12]	RW	Specifies Detect mode when GPIOx22 is in Input mode. It is configured the combination of GPIOXDET_EX22 (1-bit) + GPIOXDETMODE1_22 (2-bit). Considers GPIOXDET_EX22 as well as GPIOXDETMODE1_22. NOTE: First bit is GPIOXDET_EX22 Second and third bit is GPIOXDETMODE1_22 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_21	[11:10]	RW	Specifies Detect mode when GPIOx21 is in Input mode. It is configured the combination of GPIOXDET_EX21 (1-bit) + GPIOXDETMODE1_21 (2-bit). Considers GPIOXDET_EX21 as well as GPIOXDETMODE1_21. NOTE: First bit is GPIOXDET_EX21 Second and third bit is GPIOXDETMODE1_21 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_20	[9:8]	RW	Specifies Detect mode when GPIOx20 is in Input mode. It is configured the combination of GPIOXDET_EX20 (1-bit) + GPIOXDETMODE1_20 (2-bit). Considers GPIOXDET_EX20 as well as GPIOXDETMODE1_20. NOTE: First bit is GPIOXDET_EX20 Second and third bit is GPIOXDETMODE1_20 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge	2'b00

Name	Bit	Type	Description	Reset Value
			101 to 111 = Reserved	
GPIOXDETMODE1_19	[7:6]	RW	Specifies Detect mode when GPIOx19 is in Input mode. It is configured the combination of GPIOXDET_EX19 (1-bit) + GPIOXDETMODE1_19 (2-bit). Considers GPIOXDET_EX19 as well as GPIOXDETMODE1_19. NOTE: First bit is GPIOXDET_EX19 Second and third bit is GPIOXDETMODE1_19 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_18	[5:4]	RW	Specifies Detect mode when GPIOx18 is in Input mode. It is configured the combination of GPIOXDET_EX18 (1-bit) + GPIOXDETMODE1_18 (2-bit). Considers GPIOXDET_EX18 as well as GPIOXDETMODE1_18. NOTE: First bit is GPIOXDET_EX18 Second and third bit is GPIOXDETMODE1_18 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_17	[3:2]	RW	Specifies Detect mode when GPIOx17 is in Input mode. It is configured the combination of GPIOXDET_EX17 (1-bit) + GPIOXDETMODE1_17 (2-bit). Considers GPIOXDET_EX17 as well as GPIOXDETMODE1_17. NOTE: First bit is GPIOXDET_EX17 Second and third bit is GPIOXDETMODE1_17 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	2'b00
GPIOXDETMODE1_	[1:0]	RW	Specifies Detect mode when GPIOx16 is in Input mode.	2'b00

Name	Bit	Type	Description	Reset Value
16			It is configured the combination of GPIOXDET_EX16 (1-bit) + GPIOXDETMODE1_16 (2-bit). Considers GPIOXDET_EX16 as well as GPIOXDETMODE1_16. NOTE: First bit is GPIOXDET_EX16 Second and third bit is GPIOXDETMODE1_16 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	

15.4.1.5 GPIOxINTENB

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A010h, + B010h, + C010h, + D010h, + E010h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOXINTENB	[31:0]	RW	GPIOx[31:0]: Specifies the use of an interrupt when a GPIOx Event occurs. The events specified in GPIOxDETMODE0 and GPIOxDETMODE1 are used. 0 = Disable 1 = Enable	32'h0

15.4.1.6 GPIOxDET

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A014h, + B014h, + C014h, + D014h, + E014h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOXDET	[31:0]	RW	GPIOx[31:0]: Shows if an event is detected in accordance with Event Detect mode in GPIOx Input Mode. Set "1" to clear the relevant bit. GPIOx[31:0] is used as a Pending register when an interrupt occurs. Read: 0 = Not Detect 1 = Detected Write: 0 = Not Clear 1 = Clear	32'h0

15.4.1.7 GPIOxPAD

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A018h, + B018h, + C018h, + D018h, + E018h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOXPAD	[31:0]	R	GPIOx[31:0]: Can read the level pf PAD in GPIOx Input mode. The data read in this register is the data not passing a filter and reflects the PAD status itself. 0 = Low Level 1 = High Level	32'h0

15.4.1.8 GPIOxALTFN0

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A020h, + B020h, + C020h, + D020h, + E020h, Reset Value = 2'b00

Name	Bit	Type	Description	Reset Value
GPIOXALTFN0_15	[31:30]	RW	GPIOx[15]: Selects the function of GPIOx 15pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_14	[29:28]	RW	GPIOx[14]: Selects the function of GPIOx 14pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_13	[27:26]	RW	GPIOx[13]: Selects the function of GPIOx 13pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_12	[25:24]	RW	GPIOx[12]: Selects the function of GPIOx 12pin. 00 = ALT Function0	2'b00

Name	Bit	Type	Description	Reset Value
			01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	
GPIOXALTFN0_11	[23:22]	RW	GPIOx[11]: Selects the function of GPIOx 11pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_10	[21:20]	RW	GPIOx[10]: Selects the function of GPIOx 10pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_9	[19:18]	RW	GPIOx[9]: Selects the function of GPIOx 9pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_8	[17:16]	RW	GPIOx[8]: Selects the function of GPIOx 8pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_7	[15:14]	RW	GPIOx[7]: Selects the function of GPIOx 7pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_6	[13:12]	RW	GPIOx[6]: Selects the function of GPIOx 6pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_5	[11:10]	RW	GPIOx[5]: Selects the function of GPIOx 5pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_4	[9:8]	RW	GPIOx[4]: Selects the function of GPIOx 4pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2	2'b00

Name	Bit	Type	Description	Reset Value
			11 = ALT Function3	
GPIOXALTFN0_3	[7:6]	RW	GPIOx[3]: Selects the function of GPIOx 3pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_2	[5:4]	RW	GPIOx[2]: Selects the function of GPIOx 2pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_1	[3:2]	RW	GPIOx[1]: Selects the function of GPIOx 1pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN0_0	[1:0]	RW	GPIOx[0]: Selects the function of GPIOx 0pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00

15.4.1.9 GPIOxALTFN1

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A024h, + B024h, + C024h, + D024h, + E024h, Reset Value = 2'b00

Name	Bit	Type	Description	Reset Value
GPIOXALTFN1_31	[31:30]	RW	GPIOx[31]: Selects the function of GPIOx 31pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_30	[29:28]	RW	GPIOx[30]: Selects the function of GPIOx 30pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_29	[27:26]	RW	GPIOx[29]: Selects the function of GPIOx 29pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_28	[25:24]	RW	GPIOx[28]: Selects the function of GPIOx 28pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_27	[23:22]	RW	GPIOx[27]: Selects the function of GPIOx 27pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_26	[21:20]	RW	GPIOx[26]: Selects the function of GPIOx 26pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_25	[19:18]	RW	GPIOx[25]: Selects the function of GPIOx 25pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2	2'b00

Name	Bit	Type	Description	Reset Value
			11 = ALT Function3	
GPIOXALTFN1_24	[17:16]	RW	GPIOx[24]: Selects the function of GPIOx 24pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_23	[15:14]	RW	GPIOx[23]: Selects the function of GPIOx 23pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_22	[13:12]	RW	GPIOx[22]: Selects the function of GPIOx 22pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_21	[11:10]	RW	GPIOx[21]: Selects the function of GPIOx 21pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_20	[9:8]	RW	GPIOx[20]: Selects the function of GPIOx 20pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_19	[7:6]	RW	GPIOx[19]: Selects the function of GPIOx 19pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_18	[5:4]	RW	GPIOx[18]: Selects the function of GPIOx 18pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_17	[3:2]	RW	GPIOx[17]: Selects the function of GPIOx 17pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b00
GPIOXALTFN1_16	[1:0]	RW	GPIOx[16]: Selects the function of GPIOx 16pin.	2'b00

Name	Bit	Type	Description	Reset Value
			00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	

15.4.1.10 GPIOxDETMODEEX

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A028h, + B028h, + C028h, + D028h, + E028h, Reset Value = 1'b0

Name	Bit	Type	Description	Reset Value
GPIOXDET_EX31	[31]	RW	Specifies Detect mode when GPIOx31 is in Input mode. It is configured the combination of GPIOXDET_EX31 (1-bit) + GPIOXDETMODE1_31 (2-bit). Considers GPIOXDET_EX31 as well as GPIOXDETMODE1_31. NOTE: First bit is GPIOXDET_EX31 Second and third bit is GPIOXDETMODE1_31 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX30	[30]	RW	Specifies Detect mode when GPIOx30 is in Input mode. It is configured the combination of GPIOXDET_EX30 (1-bit) + GPIOXDETMODE1_30 (2-bit). Considers GPIOXDET_EX30 as well as GPIOXDETMODE1_30. NOTE: First bit is GPIOXDET_EX30 Second and third bit is GPIOXDETMODE1_30 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX29	[29]	RW	Specifies Detect mode when GPIOx29 is in Input mode. It is configured the combination of GPIOXDET_EX29 (1-bit) + GPIOXDETMODE1_29 (2-bit). Considers GPIOXDET_EX29 as well as GPIOXDETMODE1_29. NOTE: First bit is GPIOXDET_EX29	1'b0

Name	Bit	Type	Description	Reset Value
			Second and third bit is GPIOXDETMODE1_29 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX28	[28]	RW	Specifies Detect mode when GPIOx28 is in Input mode. It is configured the combination of GPIOXDET_EX28 (1-bit) + GPIOXDETMODE1_28 (2-bit). Considers GPIOXDET_EX28 as well as GPIOXDETMODE1_28. NOTE: First bit is GPIOXDET_EX28 Second and third bit is GPIOXDETMODE1_28 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX27	[27]	RW	Specifies Detect mode when GPIOx27 is in Input mode. It is configured the combination of GPIOXDET_EX27 (1-bit) + GPIOXDETMODE1_27 (2-bit). Considers GPIOXDET_EX27 as well as GPIOXDETMODE1_27. NOTE: First bit is GPIOXDET_EX27 Second and third bit is GPIOXDETMODE1_27 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX26	[26]	RW	Specifies Detect mode when GPIOx26 is in Input mode. It is configured the combination of GPIOXDET_EX26 (1-bit) + GPIOXDETMODE1_26 (2-bit). Considers GPIOXDET_EX26 as well as GPIOXDETMODE1_26. NOTE: First bit is GPIOXDET_EX26 Second and third bit is GPIOXDETMODE1_26 000 = Low Level	1'b0

Name	Bit	Type	Description	Reset Value
			001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX25	[25]	RW	Specifies Detect mode when GPIOx25 is in Input mode. It is configured the combination of GPIOXDET_EX25 (1-bit) + GPIOXDETMODE1_25 (2-bit). Considers GPIOXDET_EX25 as well as GPIOXDETMODE1_25. NOTE: First bit is GPIOXDET_EX25 Second and third bit is GPIOXDETMODE1_25 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX24	[24]	RW	Specifies Detect mode when GPIOx24 is in Input mode. It is configured the combination of GPIOXDET_EX24 (1-bit) + GPIOXDETMODE1_24 (2-bit). Considers GPIOXDET_EX24 as well as GPIOXDETMODE1_24. NOTE: First bit is GPIOXDET_EX24 Second and third bit is GPIOXDETMODE1_24 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX23	[23]	RW	Specifies Detect mode when GPIOx23 is in Input mode. It is configured the combination of GPIOXDET_EX23 (1-bit) + GPIOXDETMODE1_23 (2-bit). Considers GPIOXDET_EX23 as well as GPIOXDETMODE1_23. NOTE: First bit is GPIOXDET_EX23 Second and third bit is GPIOXDETMODE1_23 000 = Low Level 001 = High Level 010 = Falling Edge	1'b0

Name	Bit	Type	Description	Reset Value
			011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX22	[22]	RW	Specifies Detect mode when GPIOx22 is in Input mode. It is configured the combination of GPIOXDET_EX22 (1-bit) + GPIOXDETMODE1_22 (2-bit). Considers GPIOXDET_EX22 as well as GPIOXDETMODE1_22. NOTE: First bit is GPIOXDET_EX22 Second and third bit is GPIOXDETMODE1_22 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX21	[21]	RW	Specifies Detect mode when GPIOx21 is in Input mode. It is configured the combination of GPIOXDET_EX21 (1-bit) + GPIOXDETMODE1_21 (2-bit). Considers GPIOXDET_EX21 as well as GPIOXDETMODE1_21. NOTE: First bit is GPIOXDET_EX21 Second and third bit is GPIOXDETMODE1_21 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX20	[20]	RW	Specifies Detect mode when GPIOx20 is in Input mode. It is configured the combination of GPIOXDET_EX20 (1-bit) + GPIOXDETMODE1_20 (2-bit). Considers GPIOXDET_EX20 as well as GPIOXDETMODE1_20. NOTE: First bit is GPIOXDET_EX20 Second and third bit is GPIOXDETMODE1_20 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge	1'b0

Name	Bit	Type	Description	Reset Value
			101 to 111 = Reserved	
GPIOXDET_EX19	[19]	RW	Specifies Detect mode when GPIOx19 is in Input mode. It is configured the combination of GPIOXDET_EX19 (1-bit) + GPIOXDETMODE1_19 (2-bit). Considers GPIOXDET_EX19 as well as GPIOXDETMODE1_19. NOTE: First bit is GPIOXDET_EX19 Second and third bit is GPIOXDETMODE1_19 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX18	[18]	RW	Specifies Detect mode when GPIOx18 is in Input mode. It is configured the combination of GPIOXDET_EX18 (1-bit) + GPIOXDETMODE1_18 (2-bit). Considers GPIOXDET_EX18 as well as GPIOXDETMODE1_18. NOTE: First bit is GPIOXDET_EX18 Second and third bit is GPIOXDETMODE1_18 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX17	[17]	RW	Specifies Detect mode when GPIOx17 is in Input mode. It is configured the combination of GPIOXDET_EX17 (1-bit) + GPIOXDETMODE1_17 (2-bit). Considers GPIOXDET_EX17 as well as GPIOXDETMODE1_17. NOTE: First bit is GPIOXDET_EX17 Second and third bit is GPIOXDETMODE1_17 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX16	[16]	RW	Specifies Detect mode when GPIOx16 is in Input mode.	1'b0

Name	Bit	Type	Description	Reset Value
			It is configured the combination of GPIOXDET_EX16 (1-bit) + GPIOXDETMODE1_16 (2-bit). Considers GPIOXDET_EX16 as well as GPIOXDETMODE1_16. NOTE: First bit is GPIOXDET_EX16 Second and third bit is GPIOXDETMODE1_16 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX15	[15]	RW	Specifies Detect mode when GPIOx15 is in Input mode. It is configured the combination of GPIOXDET_EX15 (1-bit) + GPIOXDETMODE0_15 (2-bit). Considers GPIOXDET_EX15 as well as GPIOXDETMODE0_15. NOTE: First bit is GPIOXDET_EX15 Second and third bit is GPIOXDETMODE0_15 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX14	[14]	RW	Specifies Detect mode when GPIOx14 is in Input mode. It is configured the combination of GPIOXDET_EX14 (1-bit) + GPIOXDETMODE0_14 (2-bit). Considers GPIOXDET_EX14 as well as GPIOXDETMODE0_14. NOTE: First bit is GPIOXDET_EX14 Second and third bit is GPIOXDETMODE0_14 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX13	[13]	RW	Specifies Detect mode when GPIOx13 is in Input mode. It is configured the combination of GPIOXDET_EX13 (1-bit) + GPIOXDETMODE0_13 (2-bit).	1'b0

Name	Bit	Type	Description	Reset Value
			Considers GPIOXDET_EX13 as well as GPIOXDETMODE0_13. NOTE: First bit is GPIOXDET_EX13 Second and third bit is GPIOXDETMODE0_13 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX12	[12]	RW	Specifies Detect mode when GPIOx12 is in Input mode. It is configured the combination of GPIOXDET_EX12 (1-bit) + GPIOXDETMODE0_12 (2-bit). Considers GPIOXDET_EX12 as well as GPIOXDETMODE0_12. NOTE: First bit is GPIOXDET_EX12 Second and third bit is GPIOXDETMODE0_12 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX11	[11]	RW	Specifies Detect mode when GPIOx11 is in Input mode. It is configured the combination of GPIOXDET_EX11 (1-bit) + GPIOXDETMODE0_11 (2-bit). Considers GPIOXDET_EX11 as well as GPIOXDETMODE0_11. NOTE: First bit is GPIOXDET_EX11 Second and third bit is GPIOXDETMODE0_11 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX10	[10]	RW	Specifies Detect mode when GPIOx10 is in Input mode. It is configured the combination of GPIOXDET_EX10 (1-bit) + GPIOXDETMODE0_10 (2-bit). Considers GPIOXDET_EX10 as well as GPIOXDETMODE0_10.	1'b0

Name	Bit	Type	Description	Reset Value
			NOTE: First bit is GPIOXDET_EX10 Second and third bit is GPIOXDETMODE0_10 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX9	[9]	RW	Specifies Detect mode when GPIOx9 is in Input mode. It is configured the combination of GPIOXDET_EX9 (1-bit) + GPIOXDETMODE0_9 (2-bit). Considers GPIOXDET_EX9 as well as GPIOXDETMODE0_9. NOTE: First bit is GPIOXDET_EX9 Second and third bit is GPIOXDETMODE0_9 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX8	[8]	RW	Specifies Detect mode when GPIOx8 is in Input mode. It is configured the combination of GPIOXDET_EX8 (1-bit) + GPIOXDETMODE0_8 (2-bit). Considers GPIOXDET_EX8 as well as GPIOXDETMODE0_8. NOTE: First bit is GPIOXDET_EX8 Second and third bit is GPIOXDETMODE0_8 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX7	[7]	RW	Specifies Detect mode when GPIOx7 is in Input mode. It is configured the combination of GPIOXDET_EX7 (1-bit) + GPIOXDETMODE0_7 (2-bit). Considers GPIOXDET_EX7 as well as GPIOXDETMODE0_7. NOTE: First bit is GPIOXDET_EX7	1'b0

Name	Bit	Type	Description	Reset Value
			Second and third bit is GPIOXDETMODE0_7 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX6	[6]	RW	Specifies Detect mode when GPIOx6 is in Input mode. It is configured the combination of GPIOXDET_EX6 (1-bit) + GPIOXDETMODE0_6 (2-bit). Considers GPIOXDET_EX6 as well as GPIOXDETMODE0_6. NOTE: First bit is GPIOXDET_EX6 Second and third bit is GPIOXDETMODE0_6 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX5	[5]	RW	Specifies Detect mode when GPIOx5 is in Input mode. It is configured the combination of GPIOXDET_EX5 (1-bit) + GPIOXDETMODE0_5 (2-bit). Considers GPIOXDET_EX5 as well as GPIOXDETMODE0_5. NOTE: First bit is GPIOXDET_EX5 Second and third bit is GPIOXDETMODE0_5 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX4	[4]	RW	Specifies Detect mode when GPIOx4 is in Input mode. It is configured the combination of GPIOXDET_EX4 (1-bit) + GPIOXDETMODE0_4 (2-bit). Considers GPIOXDET_EX4 as well as GPIOXDETMODE0_4. NOTE: First bit is GPIOXDET_EX4 Second and third bit is GPIOXDETMODE0_4 000 = Low Level	1'b0

Name	Bit	Type	Description	Reset Value
			001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX3	[3]	RW	Specifies Detect mode when GPIOx3 is in Input mode. It is configured the combination of GPIOXDET_EX3 (1-bit) + GPIOXDETMODE0_3 (2-bit). Considers GPIOXDET_EX3 as well as GPIOXDETMODE0_3. NOTE: First bit is GPIOXDET_EX3 Second and third bit is GPIOXDETMODE0_3 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX2	[2]	RW	Specifies Detect mode when GPIOx2 is in Input mode. It is configured the combination of GPIOXDET_EX2 (1-bit) + GPIOXDETMODE0_2 (2-bit). Considers GPIOXDET_EX2 as well as GPIOXDETMODE0_2. NOTE: First bit is GPIOXDET_EX2 Second and third bit is GPIOXDETMODE0_2 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0
GPIOXDET_EX1	[1]	RW	Specifies Detect mode when GPIOx1 is in Input mode. It is configured the combination of GPIOXDET_EX1 (1-bit) + GPIOXDETMODE0_1 (2-bit). Considers GPIOXDET_EX1 as well as GPIOXDETMODE0_1. NOTE: First bit is GPIOXDET_EX1 Second and third bit is GPIOXDETMODE0_1 000 = Low Level 001 = High Level 010 = Falling Edge	1'b0

Name	Bit	Type	Description	Reset Value
			011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	
GPIOXDET_EX0	[0]	RW	Specifies Detect mode when GPIOx0 is in Input mode. It is configured the combination of GPIOXDET_EX0 (1-bit) + GPIOXDETMODE0_0 (2-bit). Considers GPIOXDET_EX0 as well as GPIOXDETMODE0_0. NOTE: First bit is GPIOXDET_EX0 Second and third bit is GPIOXDETMODE0_0 000 = Low Level 001 = High Level 010 = Falling Edge 011 = Rising Edge 100 = Both(Rising & Falling) Edge 101 to 111 = Reserved	1'b0

15.4.1.11 GPIOxDETENB

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A03Ch, + B03Ch, + C03Ch, + D03Ch, + E03Ch, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOXDETENB	[31:0]	RW	GPIOx[31:0]: Decides the use of the detected mode of GPIOx PAD. 0 = Disable 1 = Enable	32'h0

15.4.1.12 GPIOx_SLEW

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A040h, + B040h, + C040h, + D040h, + E040h, Reset Value = 32'hffffffff

Name	Bit	Type	Description	Reset Value
GPIOX_SLEW	[31:0]	RW	GPIOx[31:0]: Decides the use of the Slew resistance of GPIOx PAD. 0 = Fast Slew 1 = Normal Slew	32'hffffffff

15.4.1.13 GPIOx_SLEW_DISABLE_DEFAULT

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A044h, + B044h, + C044h, + D044h, + E044h, Reset Value = 32'hffffffff

Name	Bit	Type	Description	Reset Value
GPIOX_SLEW_DISABLE_DEFAULT	[31:0]	RW	GPIOx[31:0]: Decides the use of the Slew resistance of GPIOx PAD. 0 = Use Default Slew 1 = Use GPIOx_Slew Value	32'hffffffff

15.4.1.14 GPIOx_DRV1

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A048h, + B048h, + C048h, + D048h, + E048h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOX_DRV1	[31:0]	RW	GPIOx[31:0]: Decides the use of the Drive Strength1 resistance of GPIOx PAD. 0 = Drive Strength0 to 0 1 = Drive Strength0 to 1	32'h0

15.4.1.15 GPIOx_DRV1_DISABLE_DEFAULT

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A04Ch, + B04Ch, + C04Ch, + D04Ch, + E04Ch, Reset Value = 32'hffffffff

Name	Bit	Type	Description	Reset Value
GPIOX_DRV1_DISABLE_DEFAULT	[31:0]	RW	GPIOx[31:0]: Decides the use of the Drive Strength1 resistance of GPIOx PAD. 0 = Use Default Drive Strength 1 = Use GPIOx_DRV1 Value	32'hffffffff

15.4.1.16 GPIOx_DRV0

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A050h, + B050h, + C050h, + D050h, + E050h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOX_DRV0	[31:0]	RW	GPIOx[31:0]: Decides the use of the Drive Strength0 resistance of GPIOx PAD. 0 = Drive Strength1 to 0 1 = Drive Strength1 to 1 DC current of output driver (DS : Drive Strength)	32'h0

15.4.1.17 GPIOx_DRV0_DISABLE_DEFAULT

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A054h, + B054h, + C054h, + D054h, + E054h, Reset Value = 32'hffffffff

Name	Bit	Type	Description	Reset Value
GPIOX_DRV0_DISABLE_DEFAULT	[31:0]	RW	GPIOx[31:0]: Decides the use of the Drive Strength0 resistance of GPIOx PAD. 0 = Use Default Drive Strength 1 = Use GPIOx_DRV0 Value	32'hffffffff

15.4.1.18 GPIOx_PULLSEL

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A058h, + B058h, + C058h, + D058h, + E058h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOX_PULLSEL	[31:0]	RW	GPIOx[31:0]: Decides the Pull-up or Pull-down of GPIOx PAD. 0 = Pull-Down 1 = Pull-Up	32'h0

15.4.1.19 GPIOx_PULLSEL_DISABLE_DEFAULT

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A05Ch, + B05Ch, + C05Ch, + D05Ch, + E05Ch, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOX_PULLSEL_DISABLE_DEFAULT	[31:0]	RW	GPIOx[31:0]: Decides the use of the PullSel resistance of GPIOx PAD. 0 = Use Default Pull Sel 1 = Use GPIOx_PULLSEL Value	32'h0

15.4.1.20 GPIOx_PULLENB

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A060h, + B060h, + C060h, + D060h, + E060h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOX_PULLENB	[31:0]	RW	GPIOx[31:0]: Decides the use of the Pull-up resistance (100 kΩ) of GPIOx PAD. 0 = Pull-Up Disable 1 = Pull-Up Enable	32'h0

15.4.1.21 GPIOx_PULLENB_DISABLE_DEFAULT

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A064h, + B064h, + C064h, + D064h, + E064h, Reset Value = 32'h0

Name	Bit	Type	Description	Reset Value
GPIOX_PULLENB_DISABLE_DEFAULT	[31:0]	RW	GPIOx[31:0]: Decides the use of the PullEnb resistance of GPIOx PAD.	32'h0

Name	Bit	Type	Description	Reset Value
			0 = Use Default Pull Enb 1 = Use GPIOx_PULLENB Value	

16 Ethernet MAC

16.1 Overview

The GMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE802.3-2008 standard.

EMAC supports 10/100/1000Mbps data transfer rates, and it has Reduced Gigabit Media Independent Interface (RGMII) with External PHY chip.

16.1.1 MAC Core Features

- Supports 10/100/1000 Mbps data transfer rates with the following phy interfaces:
  - RGMII interface to communicate with an external gigabit PHY
- Supports both full-duplex and half-duplex operation
- Automatic CRC and pad generation controllable on receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16KB
- Programmable Inter Frame Gap (40-96 bit times in steps of 8)
- Support a variety of flexible address filtering mode
- Separate transmission, reception, and control interface to the Application9
- MDIO Master Interface for PHY device configuration and management
- Compliant to the following standards:
  - IEEE 802.3 - 2002 for Ethernet MAC
  - IEEE 1588 - 2002 standard for precision networked clock synchronization
  - RGMII specification version 2.0 from HP/Marvell.

16.1.2 DMA Block Features

- 32/64/128-bit data transfer
- Single-channel Transmit and Receive engines
- Optimization for packet-oriented DMA transfers with frame delimiters
- Byte-aligned addressing for data buffer support
- Descriptor architectures, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 8 KB of data
- Individual programmable burst size for Transmit and Receive DMA Engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-frame Transmit/Receive complete interrupt control
- Round-robin or fixed-priority arbitration between Receive and Transmit Engines
- Start/Stop mode
- Separate port for host CSR (Control and Status Register) access and host data interface

16.2 Block Diagram

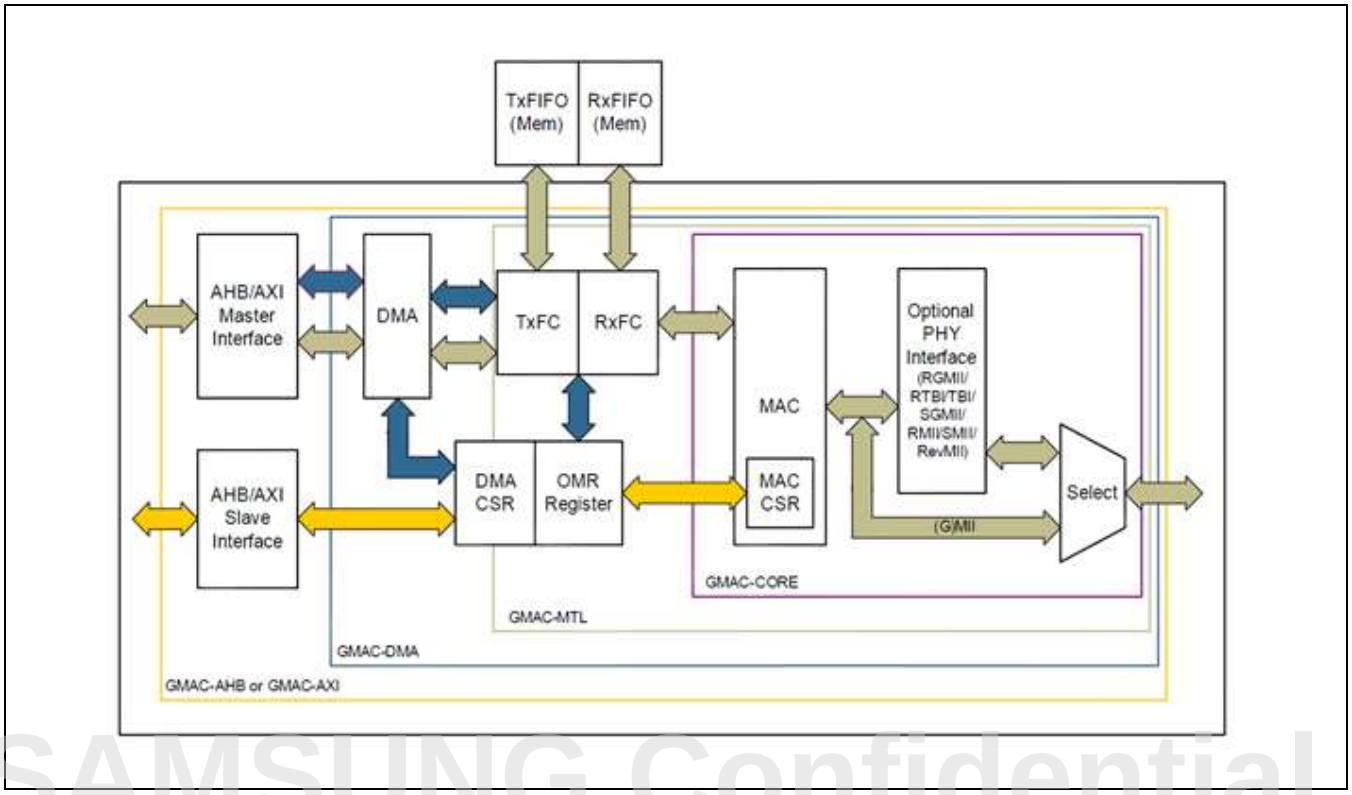


Figure 16-1 Block Diagram of the Ethernet MAC

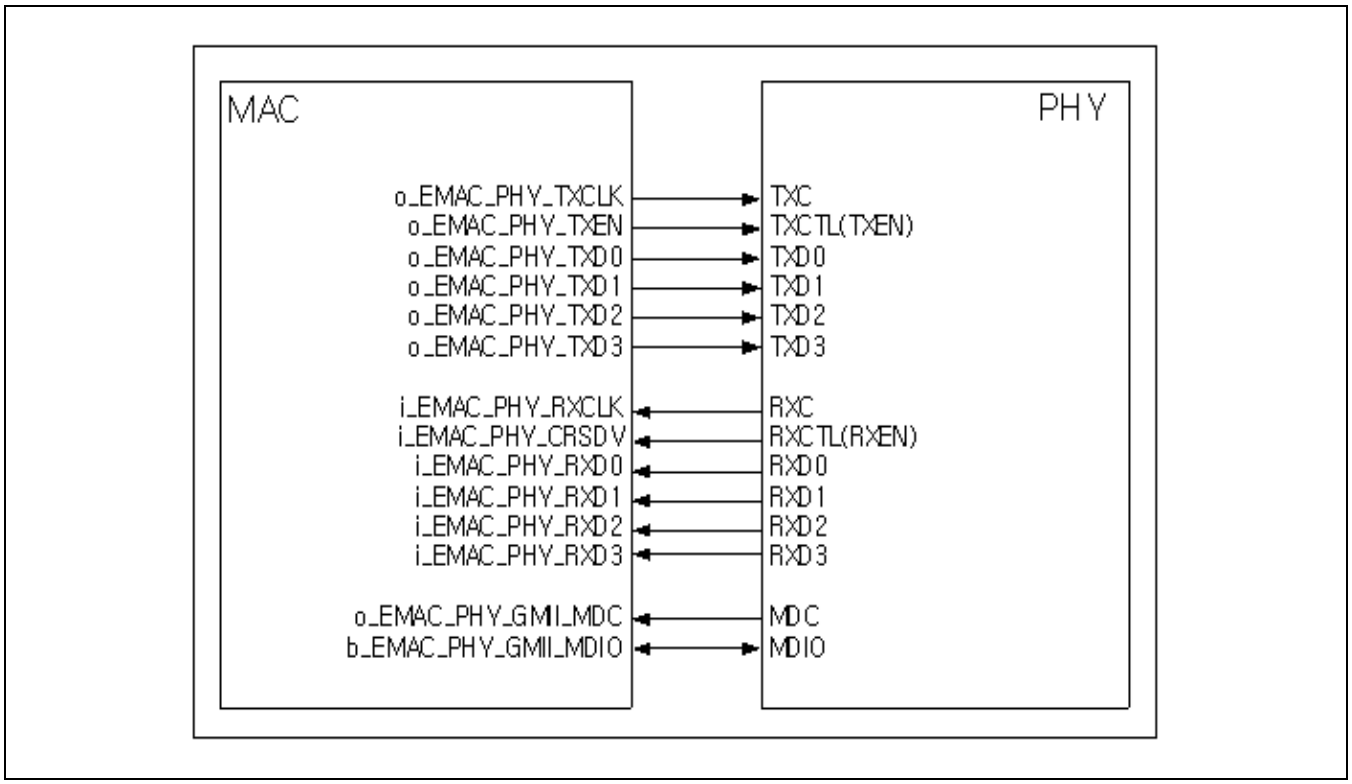


Figure 16-2 RGMII Interface between MAC and Gigabit Ethernet PHY

16.3 Register Description

16.3.1 Register Map Summary

- Base Address: C006_1000h (MAC DMA)

Register	Offset	Description	Reset Value
MAC DMA			
Ethernet MAC DMA register 0	0x00h	Bus Mode Register	0x0000_0101
Ethernet MAC DMA register 1	0x04h	Transmit Poll Demand Register	0x0000_0000
Ethernet MAC DMA register 2	0x08h	Receive Poll Demand Register	0x0000_0000
Ethernet MAC DMA register 3	0x0Ch	Receive Descriptor List Address Register	0x0000_0000
Ethernet MAC DMA register 4	0x10h	Transmit Descriptor List Address Register	0x0000_0000
Ethernet MAC DMA register 5	0x14h	Status Register	0x0000_0000
Ethernet MAC DMA register 6	0x18h	Operation Mode Register	0x0000_0000
Ethernet MAC DMA register 7	0x1Ch	Interrupt Enable Register	0x0000_0000
Ethernet MAC DMA register 8	0x20h	Missed Frame and Buffer Overflow Control Register	0x0000_0000
RSVD	0x24h to 0x44h	Reserved	–
Ethernet MAC DMA register 18	0x48h	Current Host Transmit Descriptor Register	0x0000_0000
Ethernet MAC DMA register 19	0x4Ch	Current Host Receive Descriptor Register	0x0000_0000
Ethernet MAC DMA register 20	0x50h	Current Host Transmit Buffer Address Register	0x0000_0000
Ethernet MAC DMA register 21	0x54h	Current Host Receive Buffer Address Register	0x0000_0000

- Base Address: C006_0000h (MAC Core)

Register	Offset	Description	Reset Value
MAC Core			
Ethernet MAC Register 0	0x00h	MAC Configuration Register	0x0000_0000
Ethernet MAC Register 1	0x04h	MAC Frame Filter Register	0x0000_0000
Ethernet MAC Register 2	0x08h	Hash Table High Register	0x0000_0000
Ethernet MAC Register 3	0x0Ch	Hash Table Low Register	0x0000_0000
Ethernet MAC Register 4	0x10h	GMII Address Register	0x0000_0000
Ethernet MAC Register 5	0x14h	GMII Data Register	0x0000_0000
Ethernet MAC Register 6	0x18h	Flow Control Register	0x0000_0000
Ethernet MAC Register 7	0x1Ch	VALN Tag Register	0x0000_0000
Ethernet MAC Register 8	0x20h	Version Register	0x0000_0037
Ethernet MAC Register 9	0x24h	Debug Register	0x0000_0000
RSVD	0x28h to 0x34h	Reserved	–
Ethernet MAC Register 14	0x38h	Interrupt Status Register	0x0000_0000
Ethernet MAC Register 15	0x3Ch	Interrupt Mask Register	0x0000_0000
Ethernet MAC Register 16	0x40h	MAC Address0 High Register	0x0000_FFFF
Ethernet MAC Register 17	0x44h	MAC Address0 Low Register	0xFFFF_FFFF
Ethernet MAC Register 18	0x48h	MAC Address1 High Register	0x0000_FFFF
Ethernet MAC Register 19	0x4Ch	MAC Address1 Low Register	0xFFFF_FFFF
Ethernet Mac Register 20 ~ 47	0x50h to 0xBCh	MAC Address1 High Register MAC Address1 Low Register	0x0000_FFFF 0xFFFF_FFFF
Ethernet MAC Register 48	0xC0h	AN Control Register	0x0000_0000
Ethernet MAC Register 49	0xC4h	AN Status Register	0x0000_0000
Ethernet MAC Register 50	0xC8h	Auto-Negotiation Advertisement Register	0x0000_0000
Ethernet MAC Register 51	0xCCh	Auto-Negotiation Link Partner Ability Register	0x0000_0000
Ethernet MAC Register 52	0xD0h	Auto-Negotiation Expansion Register	0x0000_0000
Ethernet MAC Register 53	0xD4h	TBI Extended Status Register	0x0000_0000
Ethernet MAC Register 54	0xD8h	SGMII/RGMII/SMII Control and Status Register	0x0000_0000
RSVD	0xE0h to 0x6FCh	Reserved	–
Ethernet MAC Register 448	0x700h	Time Stamp Control Register	0x0000_0000
Ethernet MAC Register 449	0x704h	Sub-Second Increment Register	0x0000_0000
Ethernet MAC Register 450	0x708h	System Time - Second Register	0x0000_0000
Ethernet MAC Register 451	0x70Ch	System Time - Nano second Register	0x0000_0000
Ethernet MAC Register 452	0x710h	System Time - Second Update	0x0000_0000
Ethernet MAC Register 453	0x714h	System Time - Nano Second Update Register	0x0000_0000

Register	Offset	Description	Reset Value
Ethernet MAC Register 454	0x718h	Timestamp Addend Register	0x0000_0000
Ethernet MAC Register 455	0x71Ch	Target Time Second Register	0x0000_0000
Ethernet MAC Register 456	0x720h	Target Time Nano Second Register	0x0000_0000
Ethernet MAC Register 457	0x724h	System Time - Higher Word Seconds Register	0x0000_0000
Ethernet MAC Register 458	0x728h	Timestamp Status Register	0x0000_0000
RSVD	0x72Ch to 0x7FCh	Reserved	–
Ethernet MAC Register 512 ~ 543	0x800h to 0x87Ch	MAC Address1 High Register MAC Address1 Low Register	0x0000_FFFF 0xFFFF_FFFF

16.3.1.1 MAC DMA Register

16.3.1.1.1 Ethernet MAC DMA Register 0

- Base Address: C006_1000h
- Address = Base Address + 0x00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RIB	[31]	RW	Rebuild INCRx Burst When this bit is set high and the AHB master gets an EBT (Retry, Split, or Losing bus grant), the AHB master interface rebuilds the pending beats of any burst transfer initiated with INCRx. The AHB master interface rebuilds the beats with a combination of specified bursts with INCRx and SINGLE. By default, the AHB master interface rebuilds pending beats of an EBT with an unspecified (INCR) burst. This bit is valid only in the GMAC-AHB configuration. It is reserved in all other configuration.	1'b0
RSVD	[30]	–	Reserved	1'b0
PRWG	[29:28]	RW	Channel Priority Weights This field sets the priority weights for Channel 0 during the round-robin arbitration between the DMA channels for the system bus. 00 = The priority weight is 1. 01 = The priority weight is 2. 10 = The priority weight is 3. 11 = The priority weight is 4. This field is present in all DWC_GMAC configurations except GMAC-AXI when you select the AV feature. Otherwise, this field is reserved and read-only (RO).	2'b0
TXPR	[27]	RW	Transmit Priority When set, this bit indicates that the transmit DMA has higher priority than the receive DMA during arbitration for the system-side bus. In the GMAC-AXI configuration, this bit is reserved and read-only (RO).	1'b0
MB	[26]	RW	Mixed Burst When this bit is set high and the FB bit is low, the AHB master interface starts all bursts of length more than 16 with INCR (undefined burst), whereas it reverts to fixed burst transfers (INCRx and SINGLE) for burst length of 16 and less.	1'b0
AAL	[25]	RW	Address-Aligned Beats When this bit is set high and the FB bit is equal to 1, the AHB or AXI interface generates all bursts aligned to the start address LS bits. If the FB bit is equal to 0, the first burst (accessing the start address of data buffer) is not aligned, but subsequent bursts are aligned to the address.	1'b0

Name	Bit	Type	Description	Reset Value
PBLX8	[24]	RW	PBLx8 Mode When set high, this bit multiplies the programmed PBL value (Bits [22:17] and Bits[13:8]) eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64,128, and 256 beats depending on the PBL value.	1'b0
USP	[23]	RW	Use Separate PBL When set high, this bit configures the Rx DMA to use the value configured in Bits[22:17] as PBL. The PBL value in Bits [13:8] is applicable only to the Tx DMA operations. When reset to low, the PBL value in Bits [13:8] is applicable for both DMA engines.	1'b0
RPBL	[22:17]	RW	Rx DMA PBL This field indicates the maximum number of beats to be transferred in one RxDMA transaction. This is the maximum value that is used in a single block Read or Write. The Rx DMA always attempts to burst as specified in the RPBL bit each time it starts a Burst transfer on the host bus. You can program RPBL with values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. This field is valid and applicable only when USP is set high.	6'h10
FB	[16]	RW	Fixed Burst This bit controls whether the AHB or AXI master interface performs fixed burst transfers or not. When set, the AHB interface uses only SINGLE, INCR4, INCR8,or INCR16 during start of the normal burst transfers. When reset, the AHB or AXI interface uses SINGLE and INCR burst transfer operations. For more information, see Bit 0 (UNDEF) of the AXI Bus Mode register in the GMAC-AXI configuration.	1'b0
PR	[15:14]	RW	Priority Ratio These bits control the priority ratio in the weighted round-robin arbitration between the Rx DMA and Tx DMA. These bits are valid only when Bit 1 (DA) is reset. The priority ratio is Rx:Tx or Tx:Rx depending on whether Bit 27 (TXPR) is reset or set. 00 = The Priority Ratio is 1:1. 01 = The Priority Ratio is 2:1. 10 = The Priority Ratio is 3:1. 11 = The Priority Ratio is 4:1. In the GMAC-AXI configuration, these bits are reserved and read-only (RO).	2'b0
PBL	[13:8]	RW	Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This is the maximum value that is used in a single block Read or Write. The	6'h01

Name	Bit	Type	Description	Reset Value
			DMA always attempts to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value results in undefined behavior. When USP is set high, this PBL value is applicable only for Tx DMA transactions. If the number of beats to be transferred is more than 32, then perform the following steps: Set the PBLx8 mode. Set the PBL. For example, if the maximum number of beats to be transferred is 64, then first set PBLx8 to 1 and then set PBL to 8. The PBL values have the following limitation: The maximum number of possible beats (PBL) is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified.	
ATDS	[7]	RW	Alternate Descriptor Size When set, the size of the alternate descriptor increases to 32 bytes (8 DWORDS). This is required when the Advanced Timestamp feature or the IPC Full Checksum Offload Engine (Type 2) is enabled in the receiver. The enhanced descriptor is not required if the Advanced Timestamp and IPC Full Checksum Offload Engine (Type 2) features are not enabled. In such case, you can use the 16 bytes descriptor to save 4 bytes of memory. This bit is present only when you select the Alternate Descriptor feature and anyone of the following features during core configuration: • Advanced Timestamp feature • IPC Full Checksum Offload Engine (Type 2) feature Otherwise, this bit is reserved and is read-only. When reset, the descriptor size reverts back to 4 DWORDs (16 bytes). This bit preserves the backward compatibility for the descriptor size. In versions prior to 3.50a, the descriptor size is 16 bytes for both normal and enhanced descriptors. In version 3.50a, descriptor size is increased to 32 bytes because of the Advanced Timestamp and IPC Full Checksum Offload Engine (Type 2) features.	1'b0
DSL	[6:2]	RW	Descriptor Skip Length This bit specifies the number of Word, Dword, or Lword (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When the DSL value is equal to zero, the descriptor table is taken as contiguous by the DMA in Ring	5'b0

Name	Bit	Type	Description	Reset Value
			mode.	
DA	[1]	RW	DMA Arbitration Scheme This bit specifies the arbitration scheme between the transmit and receive paths of Channel 0. 0 = Weighted round-robin with Rx:Tx or Tx:Rx - The priority between the paths is according to the priority specified in Bits[15:14] (PR) and priority weights specified in Bit[27] (TXPR). 1 = Fixed priority - The transmit path has priority over receive path when Bit 27 (TXPR) is set. Otherwise, receive path has priority over the transmit path. In the GMAC-AXI configuration, these bits are reserved and are read-only (RO).	1'b0
SWR	[0]	RW	Software Reset When this bit is set, the MAC DMA Controller resets the logic and all internal registers of the MAC. It is cleared automatically after the reset operation is complete in all of the DWC_GMAC clock domains. Before reprogramming any register of the DWC_GMAC, you should read a zero (0) value in this bit. NOTE: • The Software reset function is driven only by this bit. Bit[0] of Register 64 (Channel 1 Bus Mode Register) or Register 128 (Channel 2 Bus Mode Register) has no impact on the Software reset function. • The reset operation is completed only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for the software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.	1'b1

16.3.1.1.2 Ethernet MAC DMA Register 1

- Base Address: C006_1000h
- Address = Base Address + 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TPD	[31:0]	RW	Transmit Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 18 (Current Host Transmit Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the transmission returns to the Suspend state and Bit 2 (TU) of Register 5 (Status Register) is asserted. If the descriptor is available, the transmission resumes. When this register is read, it always returns zero.	32'b0

16.3.1.1.3 Ethernet MAC DMA Register 2

- Base Address: C006_1000h
- Address = Base Address + 0x08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RPD	[31:0]	RW	Receive Poll Demand When these bits are written with any value, the DMA reads the current descriptor to which the Register 19 (Current Host Receive Descriptor Register) is pointing. If that descriptor is not available (owned by the Host), the reception returns to the Suspended state and Bit 7 (RU) of Register 5 (Status Register) is asserted. If the descriptor is available, the Rx DMA returns to the active state. When this register is read, it always returns zero.	32'b0

16.3.1.1.4 Ethernet MAC DMA Register 3

- Base Address: C006_1000h
- Address = Base Address + 0x0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RDESLA	[31:0]	RW	Start of Receive List This field contains the base address of the first descriptor in the Receive Descriptor list. The LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	32'b0

16.3.1.1.5 Ethernet MAC DMA Register 4

- Base Address: C006_1000h
- Address = Base Address + 0x10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TDESLA	[31:0]	RW	Start of Transmit List This field contains the base address of the first descriptor in the Transmit Descriptor list. The LSB bits (1:0, 2:0, 3:0) for 32-bit, 64-bit, or 128-bit bus width are ignored and are internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO).	32'b0

16.3.1.1.6 Ethernet MAC DMA Register 5

- Base Address: C006_1000h
- Address = Base Address + 0x14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
GLPII/GTMSI	[30]	R	GLPII: GMAC LPI Interrupt (for Channel 0) This bit indicates an interrupt event in the LPI logic of the MAC. To reset this bit to 1'b0, the software must read the corresponding registers in the DWC_GMAC to get the exact cause of the interrupt and clear its source. NOTE: GLPII status is given only in Channel 0 DMA register and is applicable only when the Energy Efficient Ethernet feature is enabled. Otherwise, this bit is reserved. When this bit is high, the interrupt signal from the MAC (sbd_intr_o) is high. -or- GTMSI: GMAC TMS Interrupt (for Channel 1 and Channel 2) This bit indicates an interrupt event in the traffic manager and scheduler logic of DWC_GMAC. To reset this bit, the software must read the corresponding registers (Channel Status Register) to get the exact cause of the interrupt and clear its source. NOTE: GTMSI status is given only in Channel 1 and Channel 2 DMA register when the AV feature is enabled and corresponding additional transmit channels are present. Otherwise, this bit is reserved. When this bit is high, the interrupt signal from the MAC (sbd_intr_o) is high.	1'b0
TTI	[29]	R	Timestamp Trigger Interrupt This bit indicates an interrupt event in the Timestamp Generator block of the DWC_GMAC. The software must read the corresponding registers in the DWC_GMAC to get the exact cause of the interrupt and clear its source to reset this bit to 1'b0. When this bit is high, the interrupt signal from the DWC_GMAC subsystem (sbd_intr_o) is high. This bit is applicable only when the IEEE 1588 Timestamp feature is enabled. Otherwise, this bit is reserved.	1'b0
GPI	[28]	R	GMAC PMT Interrupt This bit indicates an interrupt event in the PMT module of the DWC_GMAC. The software must read the PMT Control and Status Register in the MAC to get the exact cause of interrupt and clear its source to reset this bit to 1'b0. The interrupt signal from the DWC_GMAC subsystem (sbd_intr_o) is high when this bit is high. This bit is applicable only when the Power Management feature is enabled. Otherwise, this bit is reserved. NOTE: The GPI and pmt_intr_o interrupts are generated in	1'b0

Name	Bit	Type	Description	Reset Value
			different clock domains.	
GMI	[27]	R	GMAC MMC Interrupt This bit reflects an interrupt event in the MMC module of the DWC_GMAC. The software must read the corresponding registers in the DWC_GMAC to get the exact cause of the interrupt and clear the source of interrupt to make this bit as1'b0. The interrupt signal from the DWC_GMAC subsystem (sbd_intr_o) is high when this bit is high. This bit is applicable only when the MAC Management Counters (MMC) are enabled. Otherwise, this bit is reserved.	1'b0
GLI	[26]	R	GMAC Line Interface Interrupt When set, this bit reflects any of the following interrupt events in the DWC_GMAC interfaces (if present and enabled in your configuration): • PCS (TBI, RTBI, or SGMII): Link change or auto-negotiation complete event • SMII or RGMII: Link change event • General Purpose Input Status (GPIS): Any LL or LH event on the gpi_i input ports To identify the exact cause of the interrupt, the software must first read Bit 11and Bits[2:0] of Register 14 (Interrupt Status Register) and then to clear the source of interrupt (which also clears the GLI interrupt), read any of the following corresponding registers: • PCS (TBI, RTBI, or SGMII): Register 49 (AN Status Register) • SMII or RGMII: Register 54 (SGMII/RGMII/SMII Control and Status Register) • General Purpose Input (GPI): Register 56 (General Purpose IO Register) The interrupt signal from the DWC_GMAC subsystem (sbd_intr_o) is high when this bit is high.	1'b0
EB	[25:23]	R	Error Bits This field indicates the type of error that caused a Bus Error, for example, error response on the AHB or AXI interface. This field is valid only when Bit 13 (FBI)is set. This field does not generate an interrupt. 0 0 0: Error during Rx DMA Write Data Transfer 0 1 1: Error during Tx DMA Read Data Transfer 1 0 0: Error during Rx DMA Descriptor Write Access 1 0 1: Error during Tx DMA Descriptor Write Access 1 1 0: Error during Rx DMA Descriptor Read Access 1 1 1: Error during Tx DMA Descriptor Read Access NOTE: 001 and 010 are reserved.	3'b0
TS	[22:20]	R	Transmit Process State This field indicates the Transmit DMA FSM state. This field	3'b0

Name	Bit	Type	Description	Reset Value
			does not generate an interrupt. 3'b000: Stopped; Reset or Stop Transmit Command issued 3'b001: Running; Fetching Transmit Transfer Descriptor 3'b010: Running; Waiting for status 3'b011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO) 3'b100: TIME_STAMP write state 3'b101: Reserved for future use 3'b110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow 3'b111: Running; Closing Transmit Descriptor	
RS	[19:17]	R	Receive Process State This field indicates the Receive DMA FSM state. This field does not generate an interrupt. 3'b000: Stopped: Reset or Stop Receive Command issued 3'b001: Running: Fetching Receive Transfer Descriptor 3'b010: Reserved for future use 3'b011: Running: Waiting for receive packet 3'b100: Suspended: Receive Descriptor Unavailable 3'b101: Running: Closing Receive Descriptor 3'b110: TIME_STAMP write state 3'b111: Running: Transferring the receive packet data from receive buffer to host memory	3'b0
NIS	[16]	RW	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): • Register 5[0]: Transmit Interrupt • Register 5[2]: Transmit Buffer Unavailable • Register 5[6]: Receive Interrupt • Register 5[14]: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in Register 7) affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes NIS to be set, is cleared.	1'b0
AIS	[15]	RW	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register 7 (Interrupt Enable Register): • Register 5[1]: Transmit Process Stopped • Register 5[3]: Transmit Jabber Timeout • Register 5[4]: Receive FIFO Overflow • Register 5[5]: Transmit Underflow • Register 5[7]: Receive Buffer Unavailable	1'b0

Name	Bit	Type	Description	Reset Value
			• Register 5[8]: Receive Process Stopped • Register 5[9]: Receive Watchdog Timeout • Register 5[10]: Early Transmit Interrupt • Register 5[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.	
ERI	[14]	RW	Early Receive Interrupt This bit indicates that the DMA filled the first data buffer of the packet. This bit is cleared when the software writes 1 to this bit or Bit 6 (RI) of this register is set (whichever occurs earlier).	1'b0
TBI	[13]	RW	Fatal Bus Error Interrupt This bit indicates that a bus error occurred, as described in Bits [25:23]. When this bit is set, the corresponding DMA engine disables all of its bus accesses.	1'b0
RSVD	[12:11]	–	Reserved	2'b0
ETI	[10]	RW	Early Transmit Interrupt This bit indicates that the frame to be transmitted is fully transferred to the MTL Transmit FIFO.	1'b0
RWT	[9]	RW	Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer expired while receiving the current frame and the current frame is truncated after the watchdog timeout.	1'b0
RPS	[8]	RW	Receive Process Stopped This bit is asserted when the Receive Process enters the Stopped state.	1'b0
RU	[7]	RW	Receive Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Receive List and the DMA cannot acquire it. The Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, the Receive Process resumes when the next recognized incoming frame is received. This bit is set only when the previous Receive Descriptor is owned by the DMA.	1'b0
RI	[6]	RW	Receive Interrupt This bit indicates that the frame reception is complete. When reception is complete, the Bit 31 of RDES1 (Disable Interrupt on Completion) is reset in the last Descriptor, and the specific frame status information is updated in the descriptor. The reception remains in the Running state.	1'b0

Name	Bit	Type	Description	Reset Value
UNF	[5]	RW	Transmit Underflow This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.	1'b0
OVF	[4]	RW	Receive Overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to the application, the overflow status is set in RDES0[11].	1'b0
TJT	[3]	RW	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired, which happens when the frame size exceeds 2,048 (10,240 bytes when the Jumbo frame is enabled).When the Jabber Timeout occurs, the transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert.	1'b0
TU	[2]	RW	Transmit Buffer Unavailable This bit indicates that the host owns the Next Descriptor in the Transmit List and the DMA cannot acquire it. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing Transmit descriptors, the host should change the ownership of the descriptor by setting TDES0[31] and then issue a Transmit Poll Demand command.	1'b0

16.3.1.1.7 Ethernet MAC DMA Register 6

- Base Address: C006_1000h
- Address = Base Address + 0x18h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	–	Reserved	5'b0
DT	[26]	RW	Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the MAC does not drop the frames which only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors only in the encapsulated payload. When this bit is reset, all error frames are dropped if the FEF bit is reset. If the IPC Full Checksum Offload Engine (Type 2) is disabled, this bit is reserved (RO with value 1'b0).	1'b0
RSF	[25]	RW	Receive Store and Forward When this bit is set, the MTL reads a frame from the Rx FIFO only after the complete frame has been written to it, ignoring the RTC bits. When this bit is reset, the Rx FIFO operates in the cut-through mode, subject to the threshold specified by the RTC bits.	1'b0
DFF	[24]	RW	Disable Flushing of Received Frames When this bit is set, the Rx DMA does not flush any frames because of the unavailability of receive descriptors or buffers as it does normally when this bit is reset. This bit is reserved (and RO) in the GMAC-MTL configuration.	1'b0
RFA_2	[23]	RW	MSB of Threshold for Activating Flow Control If the DWC_GMAC is configured for an Rx FIFO size of 8 KB or more, this bit (when set) provides additional threshold levels for activating the flow control in both half duplex and full-duplex modes. This bit (as Most Significant Bit), along with the RFA (Bits [10:9]), gives the following thresholds for activating flow control: 100 = Full minus 5 KB, that is, FULL - 5 KB 101 = Full minus 6 KB, that is, FULL - 6 KB 110 = Full minus 7 KB, that is, FULL - 7 KB 111 = Reserved This bit is reserved (and RO) if the Rx FIFO is 4 KB or less deep.	1'b0
RFD_2	[22]	RW	MSB of Threshold for Deactivating Flow Control If the DWC_GMAC is configured for Rx FIFO size of 8 KB or more, this bit (when set) provides additional threshold levels for deactivating the flow control in both half-duplex and full-duplex modes. This bit (as Most Significant Bit) along with the RFD (Bits [12:11]) gives the following thresholds for deactivating flow control: 100 = Full minus 5 KB, that is, FULL - 5 KB	1'b0

Name	Bit	Type	Description	Reset Value
			101 = Full minus 6 KB, that is, FULL - 6 KB 110 = Full minus 7 KB, that is, FULL - 7 KB 111 = Reserved This bit is reserved (and RO) if the Rx FIFO is 4 KB or less deep.	
TSF	[21]	RW	Transmit Store and Forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in Bits [16:14] are ignored. This bit should be changed only when the transmission is stopped.	1'b0
TFT	[20]	RW	Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost or flushed. This bit is cleared internally when the flushing operation is complete. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt frame transmission. NOTE: The flush operation is complete only when the Tx FIFO is emptied of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock (clk_tx_i) is required to be active.	1'b0
RSVD	[19:17]	–	Reserved	3'b0
TTC	[16:14]	RW	Transmit Threshold Control These bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the In addition, full frames with a length less than the threshold are also These bits are used only when Bit 21 (TSF) is reset. 000 = 64 001 = 128 010 = 192 011 = 256 100 = 40 101 = 32 110 = 24 111 = 16	3'b0
ST	[13]	RW	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is	1'b0

Name	Bit	Type	Description	Reset Value
			the Transmit List Base Address set by Register 4 (Transmit Descriptor List Address Register), or from the position retained when transmission was stopped previously. If the DMA does not own the current descriptor, transmission enters the Suspended state and Bit 2 (Transmit Buffer Unavailable) of Register 5(Status Register) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting Register 4(Transmit Descriptor List Address Register), then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and it becomes the current position when transmission is restarted. To change the list address, you need to program Register 4 (Transmit Descriptor List Address Register) with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current frame is complete or the transmission is in the Suspended state.	
RFD	[12:11]	RW	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill-level of Rx FIFO) at which the flow control is de-asserted after activation. 00 = Full minus 1 KB, that is, FULL - 1 KB 01 = Full minus 2 KB, that is, FULL - 2 KB 10 = Full minus 3 KB, that is, FULL - 3 KB 11 = Full minus 4 KB, that is, FULL - 4 KB The de-assertion is effective only after flow control is asserted. If the Rx FIFO is 8KB or more, an additional Bit (RFD_2) is used for more threshold levels as described in Bit 22. These bits are reserved and read-only when the Rx FIFO depth is less than 4 KB. NOTE: For proper flow control, the value programmed in the "RFD_2, RFD" fields should be equal to or more than the value programmed in the "RFA_2, RFA" fields.	2'b0
RFA	[10:9]	RW	Threshold for Activating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (Fill level of Rx FIFO) at which the flow control is activated. 00 = Full minus 1 KB, that is, FULL-1KB. 01 = Full minus 2 KB, that is, FULL-2KB. 10 = Full minus 3 KB, that is, FULL-3KB. 11 = Full minus 4 KB, that is, FULL-4KB. These values are applicable only to Rx FIFOs of 4 KB or more and when Bit 8(EFC) is set high. If the Rx FIFO is 8 KB	2'b0

Name	Bit	Type	Description	Reset Value
			or more, an additional Bit (RFA_2) is used for more threshold levels as described in Bit 23. These bits are reserved and read-only when the depth of Rx FIFO is less than 4 KB. NOTE: When FIFO size is exactly 4 KB, although the DWC_GMAC allows you to program the value of these bits to 11, the software should not program these bits to 2'b11. The value 2'b11 means flow control on FIFO empty condition.	
EFC	[8]	RW	Enable HW Flow Control When this bit is set, the flow control signal operation based on the fill-level of RxFIFO is enabled. When reset, the flow control operation is disabled. This bit is not used (reserved and always reset) when the Rx FIFO is less than 4 KB.	1'b0
FEF	[7]	RW	Forward Error Frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, or overflow). However, if the start byte (write) pointer of a frame is already transferred to the read controller side (in Threshold mode), then the frame is not dropped. In the GMAC-MTL configuration in which the Frame Length FIFO is also enabled during core configuration, the Rx FIFO drops the error frames if that frame's start byte is not transferred (output) on the ARI bus. When the FEF bit is set, all frames except runt error frames are forwarded to the DMA. If the Bit 25 (RSF) is set and the Rx FIFO overflows when a partial frame is written, then the frame is dropped irrespective of the FEF bit setting. However, if the Bit 25 (RSF) is reset and the Rx FIFO overflows when a partial frame is written, then a partial frame may be forwarded to the DMA. NOTE: When FEF bit is reset, the giant frames are dropped if the giant frame status is given in Rx Status in the following configurations: • The IP checksum engine (Type 1) and full checksum offload engine (Type 2) are not selected. • The advanced timestamp feature is not selected but the extended status is selected. The extended status is available with the following features: L3-L4 filter in GMAC-CORE or GMAC-MTL configurations Full checksum offload engine (Type 2) with enhanced descriptor format in the GMAC-DMA, GMAC-AHB, or GMAC-AXI configurations.	1'b0
FUF	[6]	RW	Forward Undersized Good Frames When set, the Rx FIFO forwards Undersized frames (that is, frames with no Error and length less than 64 bytes) including pad-bytes and CRC. When reset, the Rx FIFO drops all frames of less than 64 bytes, unless a frame is already transferred because of the	1'b0

Name	Bit	Type	Description	Reset Value
			lower value of Receive Threshold, for example, RTC = 01.	
DGF	[5]	RW	Drop Giant Frames When set, the MAC drops the received giant frames in the Rx FIFO, that is, frames that are larger than the computed giant frame limit. When reset, the MAC does not drop the giant frames in the Rx FIFO. NOTE: This bit is available in the following configurations in which the giant frame status is not provided in Rx status and giant frames are not dropped by default: • Configurations in which IP Checksum Offload (Type 1) is selected in Rx • Configurations in which the IPC Full Checksum Offload Engine (Type 2) is selected in Rx with normal descriptor format • Configurations in which the Advanced Timestamp feature is selected In all other configurations, this bit is not used (reserved and always reset).	1'b0
RTC	[4:3]	RW	Threshold Control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with length less than the threshold are automatically transferred. The value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. 00 = 64 01 = 32 10 = 96 11 = 128	2'b0
OSF	[2]	RW	Operate on Second Frame When this bit is set, it instructs the DMA to process the second frame of the Transmit data even before the status for the first frame is obtained.	2'b0
SR	[1]	RW	Start or Stop Receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes the incoming frames. The descriptor acquisition is attempted from the current position in the list, which is the address set by the Register 3 (Receive Descriptor List Address Register) or the position retained when the Receive process was previously stopped. If the DMA does not own the descriptor, reception is suspended and Bit 7 (Receive Buffer Unavailable) of Register 5 (Status Register) is set. The Start Receive command is effective only	2'b0

Name	Bit	Type	Description	Reset Value
			when the reception has stopped. If the command is issued before setting Register 3 (Receive Descriptor List Address Register), the DMA behavior is unpredictable. When this bit is cleared, the Rx DMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is effective only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state.	
RSVD	[0]	–	Reserved	1'b0

16.3.1.1.8 Ethernet MAC DMA Register 7

- Base Address: C006_1000h
- Address = Base Address + 0x1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
NIE	[16]	RW	Normal Interrupt Summary Enable When this bit is set, normal interrupt summary is enabled. When this bit is reset, normal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): Register 5[0]: Transmit Interrupt Register 5[2]: Transmit Buffer Unavailable Register 5[6]: Receive Interrupt Register 5[14]: Early Receive Interrupt	1'b0
AIE	[15]	RW	Abnormal Interrupt Summary Enable When this bit is set, abnormal interrupt summary is enabled. When this bit is reset, the abnormal interrupt summary is disabled. This bit enables the following interrupts in Register 5 (Status Register): Register 5[1]: Transmit Process Stopped Register 5[3]: Transmit Jabber Timeout Register 5[4]: Receive Overflow Register 5[5]: Transmit Underflow Register 5[7]: Receive Buffer Unavailable Register 5[8]: Receive Process Stopped Register 5[9]: Receive Watchdog Timeout Register 5[10]: Early Transmit Interrupt Register 5[13]: Fatal Bus Error	1'b0
ERE	[14]	RW	Early Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Early Receive Interrupt is enabled. When this bit is reset, the Early Receive Interrupt is disabled.	1'b0
FBE	[13]	RW	Fatal Bus Error Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Fatal Bus Error Interrupt is enabled. When this bit is reset, the Fatal Bus Error Enable Interrupt is disabled.	1'b0
RSVD	[12:11]	–	Reserved	2'b0
ETE	[10]	RW	Early Transmit Interrupt Enable When this bit is set with an Abnormal Interrupt Summary Enable (Bit 15), the Early Transmit Interrupt is enabled. When this bit is reset, the Early Transmit Interrupt is disabled.	1'b0
RWE	[9]	RW	Receive Watchdog Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Watchdog Timeout Interrupt is enabled.	1'b0

Name	Bit	Type	Description	Reset Value
			When this bit is reset, the Receive Watchdog Timeout Interrupt is disabled.	
RSE	[8]	RW	Receive Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped Interrupt is disabled.	1'b0
RUE	[7]	RW	Receive Buffer Unavailable Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled.	1'b0
RIE	[6]	RW	Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.	1'b0
UNE	[5]	RW	Underflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Underflow Interrupt is enabled. When this bit is reset, the Underflow Interrupt is disabled.	1'b0
OVE	[4]	RW	Overflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Receive Overflow Interrupt is enabled. When this bit is reset, the Overflow Interrupt is disabled.	1'b0
THE	[3]	RW	Transmit Jabber Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, the Transmit Jabber Timeout Interrupt is disabled.	1'b0
TUE	[2]	RW	Transmit Buffer Unavailable Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable Interrupt is disabled.	1'b0
TSE	[1]	RW	Transmit Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (Bit 15), the Transmission Stopped Interrupt is enabled. When this bit is reset, the Transmission Stopped Interrupt is disabled.	1'b0
TIE	[0]	RW	Transmit Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (Bit 16), the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.	1'b0

16.3.1.1.9 Ethernet MAC DMA Register 8

- Base Address: C006_1000h
- Address = Base Address + 1020h, Reset Value =

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	–	Reserved	3'b0
OVFCNTOVF	[28]	RW	Overflow Bit for FIFO Overflow Counter This bit is set every time the Overflow Frame Counter (Bits[27:17])overflows, that is, the Rx FIFO overflows with the overflow frame counter at maximum value. In such a scenario, the overflow frame counter is reset to all-zeros and this bit indicates that the rollover happened.	1'b0
OVFFRMCNT	[27:17]	RW	Overflow Frame Counter This field indicates the number of frames missed by the application. This counter is incremented each time the MTL FIFO overflows. The counter is cleared when this register is read with mci_be_i[2] at 1'b1.	11'b0
MISCNTOVF	[16]	RW	Overflow Bit for Missed Frame Counter This bit is set every time Missed Frame Counter (Bits[15:0]) overflows, that is, the DMA discards an incoming frame because of the Host Receive Buffer being unavailable with the missed frame counter at maximum value. In such a scenario, the Missed frame counter is reset to all-zero sand this bit indicates that the rollover happened.	1'b0
MISFRMCNT	[15:0]	RW	Missed Frame Counter This field indicates the number of frames missed by the controller because of the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.	16'b0

16.3.1.1.10 Ethernet MAC DMA Register 18

- Base Address: C006_1000h
- Address = Base Address + 0x48h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CURTDESAPTR	[31:0]	RW	Host Transmit Descriptor Address Pointer Cleared on Reset. Pointer updated by the DMA during operation.	32'b0

16.3.1.1.11 Ethernet MAC DMA Register 19

- Base Address: C006_1000h
- Address = Base Address + 0x4Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CURRDESAPTR	[31:0]	RW	Host Receive Descriptor Address Pointer Cleared on Reset. Pointer updated by the DMA during operation.	32'b0

16.3.1.1.12 Ethernet MAC DMA Register 20

- Base Address: C006_1000h
- Address = Base Address + 0x50h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CURTBUFAPTR	[31:0]	RW	Host Transmit Buffer Address Pointer Cleared on Reset. Pointer updated by the DMA during operation.	32'b0

16.3.1.1.13 Ethernet MAC DMA Register 21

- Base Address: C006_1000h
- Address = Base Address + 0x54h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CURRBUFAPTR	[31:0]	RW	Host Receive Buffer Address Pointer Cleared on Reset. Pointer updated by the DMA during operation.	32'b0

16.3.1.2 MAC Core Register

16.3.1.2.1 Ethernet MAC Register 0

- Base Address: C006_0000h
- Address = Base Address + 0x00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
SARC	[30:28]	RW	Source Address Insertion or Replacement Control This field controls the source address insertion or replacement for all transmitted frames. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits [29:28]: 2'b0x: The input signals mti_sa_ctrl_i and ati_sa_ctrl_i control the SA field generation. 2'b10: If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0registers (registers 16 and 17) in the SA field of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC inserts the content of the MAC Address 1 registers (registers 18 and 19) in the SA field of all transmitted frames. 2'b11: If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0registers (registers 16 and 17) in the SA field of all transmitted frames. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected during core configuration, the MAC replaces the content of the MAC Address 1 registers (registers 18 and 19) in the SA field of all transmitted frames. NOTE: • Changes to this field take effect only on the start of a frame. If you write this register field when a frame is being transmitted, only the subsequent frame can use the updated value, that is, the current frame does not use the updated value. • These bits are reserved and RO when the Enable SA, VLAN, and CRC Insertion on TX feature is not selected during core configuration.	3'b0
TWOKPE	[27]	RW	IEEE 802.3as Support for 2K Packets When set, the MAC considers all frames, with up to 2,000 bytes length, as normal packets. When Bit 20 (JE) is not set, the MAC considers all received frames of size more than 2K bytes as Giant frames. When this bit is reset and Bit 20 (JE) is not set, the MAC considers all received frames of size more than 1,518 bytes (1,522bytes for tagged) as Giant frames.	1'b0

Name	Bit	Type	Description	Reset Value
			When Bit 20 is set, setting this bit has no effect on Giant Frame status.	
SFTERR	[26]	RW	SMII Force Transmit Error When set, this bit indicates to the PHY to force a transmit error in the SMII frame being transmitted. This bit is reserved if the SMII PHY port is not selected during core configuration.	1'b0
CST	[25]	RW	CRC Stripping for Type Frames When this bit is set, the last 4 bytes (FCS) of all frames of Ether type (Length/Type field greater than or equal to 1,536) are stripped and dropped before forwarding the frame to the application. This function is not valid when the IP Checksum Engine (Type 1) is enabled in the MAC receiver. This function is valid when Type 2 Checksum Offload Engine is enabled.	1'b0
TC	[24]	RW	Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and linkup or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. This bit is reserved (and RO) if the RGMII, SMII, or SGMII PHY port is not selected during core configuration.	1'b0
wd	[23]	RW	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive frames of up to 16,384 bytes. When this bit is reset, the MAC does not allow a receive frame which more than 2,048 bytes (10,240 if JE is set high) or the value programmed in Register 55(Watchdog Timeout Register). The MAC cuts off any bytes received after the watchdog limit number of bytes.	1'b0
JD	[22]	RW	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer frames of up to 16,384 bytes. When this bit is reset, the MAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.	1'b0
be	[21]	RW	Frame Burst Enable When this bit is set, the MAC allows frame bursting during transmission in the GMII half-duplex mode. This bit is reserved (and RO) in the 10/100 Mbps only or full-duplex-only configurations.	1'b0
JE	[20]	RW	Jumbo Frame Enable When this bit is set, the MAC allows Jumbo frames of 9,018 bytes (9,022 bytes for VLAN tagged frames) without	1'b0

Name	Bit	Type	Description	Reset Value
			reporting a giant frame error in the receive frame status.	
IFG	[19:17]	RW	Inter-Frame Gap These bits control the minimum IFG between frames during transmission. 000 = 96-bit times 001 = 88-bit times 010 = 80-bit times … 111 = 40-bit times In the half-duplex mode, the minimum IFG can be configured only for 64 bit times (IFG = 100). Lower values are not considered. In the 1000-Mbps mode, the minimum IFG supported is 64 bit times (and above) in the GMAC-CORE configuration and 80 bit times (and above) in other configurations.	3'b0
DCRS	[16]	RW	Disable Carrier Sense During Transmission When set high, this bit makes the MAC transmitter ignore the (G) MII CRS signal during frame transmission in the half-duplex mode. This request results in no errors generated because of Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC transmitter generates such errors because of Carrier Sense and can even abort the transmissions. This bit is reserved (and RO) in the full-duplex-only configurations.	1'b0
PS	[15]	RW	Port Select This bit selects the Ethernet line speed. 0 = For 1000 Mbps operations 1 = For 10 or 100 Mbps operations In 10 or 100 Mbps operations, this bit, along with FES bit, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only with the appropriate value. In default10/100/1000 Mbps configuration, this bit is R_W. The mac_portselect_o ormac_speed_o[1] signal reflects the value of this bit.	1'b0
FES	[14]	RW	Speed This bit selects the speed in the MII, RMII, SMII, RGMII, SGMII, or RevMIIinterface: 0 = 10 Mbps 1 = 100 Mbps This bit is reserved (RO) by default and is enabled only when the parameter SPEED_SELECT = Enabled. This bit generates link speed encoding when Bit 24(TC) is set in the RGMII, SMII, or SGMII mode. This bit is always enabled for RGMII, SGMII, SMII, or RevMII interface. In configurations with RGMII, SGMII, SMII, or RevMII	1'b0

Name	Bit	Type	Description	Reset Value
			interface, this bit is driven as an output signal (mac_speed_o[0]) to reflect the value of this bit in the mac_speed_o signal. In configurations with RMII, MII, or GMII interface, you can optionally drive this bit as an output signal (mac_speed_o[0]) to reflect its value in the mac_speed_o signal.	
DO	[13]	RW	Disable Receive Own When this bit is set, the MAC disables the reception of frames when the phy_txen_o is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets that are given by the PHY while transmitting. This bit is not applicable if the MAC is operating in the full-duplex mode. This bit is reserved (RO with default value) if the MAC is configured for the full-duplex-only operation.	1'b0
LM	[12]	RW	Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G) MII Receive clock input (clk_rx_i) is required for the loopback to work properly, because the Transmit clock is not looped-back internally.	1'b0
DM	[11]	RW	Duplex Mode When this bit is set, the MAC operates in the full-duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configuration.	1'b0
IPC	[10]	RW	Checksum Offload When this bit is set, the MAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25-26 or 29-30 (VLAN tagged)of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The MAC also appends the 16-bitchecksum calculated for the IP header datagram payload (bytes after the IPv4header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits are always cleared. If the IP Checksum Offload feature is not enabled during core configuration, this bit is reserved (RO with default value).	1'b0
DR	[9]	RW	Disable Retry	1'b0

Name	Bit	Type	Description	Reset Value
			When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current frame transmission and reports a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the MAC attempts retries based on the settings of the BL field (Bits [6:5]). This bit is applicable only in the half-duplex mode and is reserved (RO with default value) in the full-duplex-only configuration.	
LUD	[8]	RW	Link Up or Down This bit indicates whether the link is up or down during the transmission of configuration in the RGMII, SGMII, or SMII interface: 0 = Link Down 1 = Link Up This bit is reserved (RO with default value) and is enabled when the RGMII, SGMII, or SMII interface is enabled during core configuration.	1'b0
ACS	[7]	RW	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming frames only if the value of the length field is less than 1,536 bytes. All received frames with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming frames, without modifying them, to the Host. Note: For information about how the settings of Bit 23 (CST) and this bit impact the frame length	1'b0
BL	[6:5]	RW	Back-Off Limit The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only in the half-duplex mode and is reserved (RO)in the full-duplex-only configuration. 00: k= min (n, 10) 01: k = min (n, 8) 10: k = min (n, 4) 11: k = min (n, 1) where n = retransmission attempt. The random integer r takes the value in the range $0 \le r < 2k$	2'b0
DC	[4]	RW	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status, when the transmit state machine is deferred for more than 24,288-bit times in the 10 or 100 Mbps	1'b0

Name	Bit	Type	Description	Reset Value
			mode. If the MAC is configured for 1000 Mbps operation or if the Jumbo frame mode is enabled in the 10 or 100 Mbps mode, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000bit times because the CRS signal is active and then the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0 and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode and is reserved (RO) in the full-duplex-only configuration.	
TE	[3]	RW	Transmitter Enable When this bit is set, the transmit state machine of the MAC is enabled for transmission on the GMII or MII. When this bit is reset, the MAC transmit state machine is disabled after the completion of the transmission of the current frame, and does not transmit any further frames.	1'b0
RE	[2]	RW	Receiver Enable When this bit is set, the receiver state machine of the MAC is enabled for receiving frames from the GMII or MII. When this bit is reset, the MAC receive state machine is disabled after the completion of the reception of the current frame, and does not receive any further frames from the GMII or MII.	1'b0
PRELEN	[1:0]	RW	Preamble Length for Transmit frames These bits control the number of preamble bytes that are added to the beginning of every Transmit frame. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 2'b00 = 7 bytes of preamble 2'b01 = 5 bytes of preamble 2'b10 = 3 bytes of preamble 2'b11 = Reserved	2'b0

16.3.1.2.2 Ethernet MAC Register 1

- Base Address: C006_0000h
- Address = Base Address + 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RA	[31]	RW	Receive All When this bit is set, the MAC Receiver module passes all received frames, irrespective of whether they pass the address filter or not, to the Application. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes only those frames to the Application that pass the SA or DA address filter.	1'b0
RSVD	[30:22]	–	Reserved	9'b0
DNTU	[21]	RW	Drop non-TCP/UDP over IP Frames When set, this bit enables the MAC to drop the non-TCP or UDP over IP frames. The MAC forward only those frames that are processed by the Layer 4 filter. When reset, this bit enables the MAC to forward all non-TCP or UDP over IP frames. If the Layer 3 and Layer 4 Filtering feature is not selected during core configuration, this bit is reserved (RO with default value).	1'b0
IPFE	[20]	RW	Layer 3 and Layer 4 Filter Enable When set, this bit enables the MAC to drop frames that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When reset, the MAC forwards all frames irrespective of the match status of the Layer 3 and Layer 4 fields. If the Layer 3 and Layer 4 Filtering feature is not selected during core configuration, this bit is reserved (RO with default value).	1'b0
RSVD	[19:17]	–	Reserved	3'b0
VTFE	[16]	RW	VLAN Tag Filter Enable When set, this bit enables the MAC to drop VLAN tagged frames that do not match the VLAN Tag comparison. When reset, the MAC forwards all frames irrespective of the match status of the VLAN Tag.	1'b0
RSVD	[15:11]	–	Reserved	5'b0
HPF	[10]	RW	Hash or Perfect Filter When this bit is set, it configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by the HMC or HUC bits. When this bit is low and the HUC or HMC bit is set, the frame is passed only if it matches the Hash filter. This bit	1'b0

Name	Bit	Type	Description	Reset Value
			is reserved (and RO) if the Hash filter is not selected during core configuration.	
SAF	[9]	RW	Source Address Filter Enable When this bit is set, the MAC compares the SA field of the received frames with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the frame. When this bit is reset, the MAC forwards the received frame to the application with updated SAF bit of the Rx Status depending on the SA address comparison. NOTE: According to the IEEE specification, Bit 47 of the SA is reserved and set to 0.However, in DWC_GMAC, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.	1'b0
SAIF	[8]	RW	SA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers are marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers are marked as failing the SA Address filter.	1'b0
PCF	[7:6]	RW	Pass Control Frames These bits control the forwarding of all control frames (including uni-cast and multicast Pause frames). 00 = MAC filters all control frames from reaching the application. 01 = MAC forwards all control frames except Pause frames to application even if they fail the Address filter. 10 = MAC forwards all control frames to application even if they fail the Address Filter. 11 = MAC forwards control frames that pass the Address Filter. The following conditions should be true for the Pause frames processing: • Condition 1: The MAC is in the full-duplex mode and flow control is enabled by setting Bit 2 (RFE) of Register 6 (Flow Control Register) to 1. • Condition 2: The destination address (DA) of the received frame matches the special multicast address or the MAC Address 0 when Bit 3 (UP) of the Register6 (Flow Control Register) is set. • Condition 3: The Type field of the received frame is 0x8808 and the OPCODE Field is 0x0001. NOTE: This field should be set to 01 only when the Condition 1 is true, that is, the MAC is programmed to operate in the full-duplex mode and the RFE bit is enabled. Otherwise, the Pause frame filtering may be	2'b0

Name	Bit	Type	Description	Reset Value
			inconsistent. When Condition 1 is false, the Pause frames are considered as generic control frames. Therefore, to pass all control frames (including Pause frames) when the full-duplex mode and flow control is not enabled, you should set the PCF field to 10 or 11 (as required by the application).	
DBF	[5]	RW	Disable Broadcast Frames When this bit is set, the AFM module blocks all incoming broadcast frames. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast frames.	1'b0
PM	[4]	RW	Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address field is 1) are passed. When reset, filtering of multicast frame depends on HMC bit.	1'b0
DAIF	[3]	RW	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.	1'b0
HMC	[2]	RW	Hash Multicast When set, MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA field with the values programmed in DA registers. If Hash Filter is not selected during core configuration, this bit is reserved (and RO).	1'b0
HUC	[1]	RW	Hash Unicast When set, MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA field with the values programmed in DA registers. If Hash Filter is not selected during core configuration, this bit is reserved (and RO).	1'b0
PR	[0]	RW	Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frame sir respective of the destination or source address. The SA or DA Filter Fails status bits of the Receive Status Word are always cleared when PR is set.	1'b0

16.3.1.2.3 Ethernet MAC Register 2

- Base Address: C006_0000h
- Address = Base Address + 0x08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HTH	[31:0]	RW	Hash Table High. This field contains the upper 32 bits of the Hash table.	32'b0

16.3.1.2.4 Ethernet MAC Register 3

- Base Address: C006_0000h
- Address = Base Address + 0x0Ch, Reset Value =

Name	Bit	Type	Description	Reset Value
HTL	[31:0]	RW	Hash Table Low. This field contains the lower 32 bits of the Hash table.	32'b0

16.3.1.2.5 Ethernet MAC Register 4

- Base Address: C006_0000h
- Address = Base Address + 0010h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	16'b0
PA	[15:11]	RW	Physical Layer Address This field indicates which of the 32 possible PHY devices are being accessed. For RevMII, this field gives the PHY Address of the RevMII module.	5'b0
GR	[10:6]	RW	GMII Register These bits select the desired GMII register in the selected PHY device. For RevMII, these bits select the desired CSR register in the RevMII Registers set.	5'b0
CR	[5:2]	RW	CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design. The CSR clock corresponding to different GMAC configurations. The suggested range of CSR clock frequency applicable for each value (when Bit[5]= 0) ensures that the MDC clock is approximately between the frequency range1.0 MHz-2.5MHz. 0000 = The CSR clock frequency is 60-100 MHz and the MDC clock frequency is CSR clock/42. 0001 = The CSR clock frequency is 100-150 MHz and the MDC clock frequency is CSR clock/62. 0010 = The CSR clock frequency is 20-35 MHz and the MDC clock frequency is CSR clock/16.	4'b0

Name	Bit	Type	Description	Reset Value
			0011 = The CSR clock frequency is 35-60 MHz and the MDC clock frequency is CSR clock/26. 0100 = The CSR clock frequency is 150-250 MHz and the MDC clock frequency is CSR clock/102. 0101 = The CSR clock frequency is 250-300 MHz and the MDC clock is CSR clock/124. 0110, 0111 = Reserved When Bit 5 is set, you can achieve higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE Std 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, then the resultant MDC clock is of 12.5 MHz which is outside the limit of IEEE 802.3 specified range. Program the following values only if the interfacing chips support faster MDC clocks. 1000 = CSR clock/4 1001 = CSR clock/6 1010 = CSR clock/8 1011 = CSR clock/10 1100 = CSR clock/12 1101 = CSR clock/14 1110 = CSR clock/16 1111 = CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface.	
GW	[1]	RW	GMII Write When set, this bit indicates to the PHY or RevMII that this is a Write operation using the GMII Data register. If this bit is not set, it indicates that this is a Read operation, that is, placing the data in the GMII Data register.	1'b0
GB	[0]	RW	GMII Busy This bit should read logic 0 before writing to Register 4 and Register 5. During a PHY or RevMII register access, the software sets this bit to 1'b1 to indicate that a Read or Write access is in progress. Register 5 is invalid until this bit is cleared by the MAC. Therefore, Register 5 (GMII Data) should be kept valid until the MAC clears this bit during a PHY Write operation. Similarly for a read operation, the contents of Register 5 are not valid until this bit is cleared. The subsequent read or write operation should happen only after the previous operation is complete. Because there is no acknowledgment from the PHY to MAC after a read or write operation is completed, there is no change in the functionality of this bit even when the PHY is not present.	1'b0

16.3.1.2.6 Ethernet MAC Register 5

- Base Address: C006_0000h
- Address = Base Address + 0x14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	16'b0
GD	[15:0]	RW	GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.	16'b0

16.3.1.2.7 Ethernet MAC Register 6

- Base Address: C006_0000h
- Address = Base Address + 0018h, Reset Value =

Name	Bit	Type	Description	Reset Value
PT	[31:16]	RW	Pause Time This field holds the value to be used in the Pause Time field in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain	16'b0
RSVD	[15:8]	–	Reserved	8'b0
DZQP	[7]	RW	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the Zero-Quanta Pause frames on the de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signals bd_flowctrl_i/mti_flowctrl_i). When this bit is reset, normal operation with automatic Zero-Quanta Pause frame generation is enabled.	1'b0
RSVD	[6]	–	Reserved	1'b0
PLT	[5:4]	RW	Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second Pause frame is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256 - 28) slot times after the first Pause frame is transmitted. The following list provides the threshold values for different values:	2'b0

Name	Bit	Type	Description	Reset Value
			00 = The threshold is Pause time minus 4 slot times (PT - 4 slot times). 01 = The threshold is Pause time minus 28 slot times (PT - 28 slot times). 10 = The threshold is Pause time minus 144 slot times (PT - 144 slot times). 11 = The threshold is Pause time minus 256 slot times (PT - 256 slot times). The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface.	
UP	[3]	RW	Unicast Pause Frame Detect A pause frame is processed when it has the unique multicast address specified in the IEEE Std 802.3. When this bit is set, the MAC can also detect Pause frames with unicast address of the station. This unicast address should be as specified in the MAC Address0 High Register and MAC Address0 Low Register. When this bit is reset, the MAC only detects Pause frames with unique multicast address. NOTE: The MAC does not process a Pause frame if the multicast address of received frame is different from the unique multicast address.	1'b0
PFE	[2]	RW	Receive Flow Control Enable When this bit is set, the MAC decodes the received Pause frame and disables its transmitter for a specified (Pause) time. When this bit is reset, the decode function of the Pause frame is disabled.	1'b0
TFE	[1]	RW	Transmit Flow Control Enable In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause frames. In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled.	1'b0
FCP_BPA	[0]	RW	Flow Control Busy or Backpressure Activate This bit initiates a Pause frame in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. In the full-duplex mode, this bit should be read as 1'b0 before writing to the Flow Control register. To initiate a Pause frame, the Application must set this bit to 1'b1. During a transfer of the Control Frame, this bit continues to be set to signify that a frame transmission is in progress. After the completion of Pause frame transmission, the MAC resets this bit to 1'b0. The Flow Control register should not be written to until this bit is	1'b0

Name	Bit	Type	Description	Reset Value
			cleared. In the half-duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the MAC. During backpressure, when the MAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically O Red with the mti_flowctrl_iinput signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled.	

16.3.1.2.8 Ethernet MAC Register 7

- Base Address: C006_0000h
- Address = Base Address + 0x1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:20]	–	Reserved	12'b0
VTHM	[19]	RW	VLAN Tag Hash Table Match Enable When set, the most significant four bits of the VLAN tag's CRC are used to index the content of Register 354 (VLAN Hash Table Register). A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the frame matched the VLAN hash table. When Bit 16 (ETV) is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison whereas when ETV is reset, the CRC of the 16-bit VLAN tag is used for comparison. When reset, the VLAN Hash Match operation is not performed. If the VLAN Hash feature is not enabled during core configuration, this bit is reserved (RO with default value).	1'b0
ESVL	[18]	RW	Enable S-VLAN When this bit is set, the MAC transmitter and receiver also consider the S-VLAN(Type = 0x88A8) frames as valid VLAN tagged frames.	1'b0
VTIM	[17]	RW	VLAN Tag Inverse Match Enable When set, this bit enables the VLAN Tag inverse matching. The frames that do not have matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The frames with matched VLAN Tag are marked as matched.	1'b0
ETV	[16]	RW	Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged frame. Similarly, when enabled, only 12 bits of the VLAN tag in the received frame are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN frame are used for comparison and VLAN hash filtering.	1'b0
VL	[15:0]	RW	VLAN Tag Identifier for Receive Frames This field contains the 802.1Q VLAN tag to identify the VLAN frames and is compared to the 15th and 16th bytes of the frames being received for VLAN frames. The following list describes the bits of this field: Bits [15:13]: User Priority	16'b0

Name	Bit	Type	Description	Reset Value
			Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits[11:0]: VLAN tag's VLAN Identifier (VID) field When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the MAC does not check the fifteenth and16th bytes for VLAN tag comparison, and declares all frames with a Type field value of 0x8100 or 0x88a8 as VLAN frames.	

16.3.1.2.9 Ethernet MAC Register 8

- Base Address: C006_0000h
- Address = Base Address + 0x20h, Reset Value = 0x0000_0037

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	16'b0
USERVER	[15:8]	R	User-defined Version (configured with core Consultant)	8'bxx
SNPSVER	[7:0]	R	MAC Version (3.7)	8'h37

16.3.1.2.10 Ethernet MAC Register 9

- Base Address: C006_0000h
- Address = Base Address + 0x24h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	6'b0
TXSTSFSTS	[25]	R	MTL TxStatus FIFO Full Status When high, this bit indicates that the MTL TxStatus FIFO is full. Therefore, the MTL cannot accept any more frames for transmission. This bit is reserved in the GMAC-AHB and GMAC-DMA configurations.	1'b0
TXFSTS	[24]	R	MTL Tx FIFO Not Empty Status When high, this bit indicates that the MTL Tx FIFO is not empty and some data is left for transmission.	1'b0
RSVD	[23]	–	Reserved	1'b0
TWCSTS	[22]	R	MTL Tx FIFO Write Controller Status When high, this bit indicates that the MTL Tx FIFO Write Controller is active and is transferring data to the Tx FIFO.	1'b0
TRCSTS	[21:20]	R	MTL Tx FIFO Read Controller Status This field indicates the state of the Tx FIFO Read Controller: 00 = IDLE state 01 = READ state (transferring data to the MAC transmitter) 10 = Waiting for TxStatus from the MAC transmitter 11 = Writing the received TxStatus or flushing the Tx FIFO	2'b0
TXPAUSED	[19]	R	MAC Transmitter in Pause When high, this bit indicates that the MAC transmitter is in the Pause condition (in the full-duplex-only mode) and hence does not schedule any frame for transmission.	1'b0
TFCSTS	[18:17]	R	MAC Transmit Frame Controller Status This field indicates the state of the MAC Transmit Frame Controller module: 00 = IDLE state 01 = Waiting for status of previous frame or IFG or back off period to be over 10 = Generating and transmitting a Pause frame (in the full-duplex mode) 11 = Transferring input frame for transmission	2'b0
TPESTS	[16]	R	MAC GMII or MII Transmit Protocol Engine Status When high, this bit indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data and is not in the IDLE state.	1'b0
RSVD	[15:0]	–	Reserved	16'b0

16.3.1.2.11 Ethernet MAC Register 14

- Base Address: C006_0000h
- Address = Base Address + 0x38h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	20'b0
GPIIS	[11]	R	GPI Interrupt Status When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field (Bits [3:0]) of Register 56 (General Purpose IO Register) and the corresponding GPIE bit is enabled. This bit is cleared on reading lane 0 (GPIS) of Register 56 (General Purpose IO Register). When the GPIO feature is not enabled, this bit is reserved.	1'b0
LPIIS	[10]	R	LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared on reading Bit 0 of Register 12 (LPI Control and Status Register). In all other modes, this bit is reserved.	1'b0
TSIS	[9]	R	Timestamp Interrupt Status When the Advanced Timestamp feature is enabled, this bit is set when any of the following conditions is true: • The system time value equals or exceeds the value specified in the Target Time High and Low registers. • There is an overflow in the seconds register. • The Auxiliary snapshot trigger is asserted. This bit is cleared on reading Bit 0 of Register 458 (Timestamp Status Register). If default Time stamping is enabled, when set, this bit indicates that the system time value is equal to or exceeds the value specified in the Target Time registers. In this mode, this bit is cleared after the completion of the read of this bit. In all other modes, this bit is reserved.	1'b0
RSVD	[8]	–	Reserved	1'b0
MMCRXIPIS	[7]	R	MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is valid only when you select the optional MMC module and Checksum Offload Engine (Type 2) during core configuration.	1'b0
MMCTXIS	[6]	R	MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is valid only when you select the optional MMC module during core configuration.	1'b0

Name	Bit	Type	Description	Reset Value
MMCRXIS	[5]	R	MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is valid only when you select the optional MMC module during core configuration.	1'b0
MMCIS	[4]	R	MMC Interrupt Status This bit is set high when any of the Bits [7:5] is set high and cleared only when all of these bits are low. This bit is valid only when you select the optional MMC module during core configuration.	1'b0
PMTIS	[3]	R	PMT Interrupt Status This bit is set when a magic packet or remote wake-up frame is received in the power-down mode (see Bits 5 and 6 in the PMT Control and Status Register). This bit is cleared when both Bits[6:5] are cleared because of a read operation to the PMT Control and Status register. This bit is valid only when you select the optional PMT module during core configuration.	1'b0
PCSANCIS	[2]	R	PCS Auto-Negotiation Complete This bit is set when the Auto-negotiation is completed in the TBI, RTBI, or SGMII PHY interface (Bit 5 in Register 49 (AN Status Register)). This bit is cleared when you perform a read operation to the AN Status register. This bit is valid only when you select the optional TBI, RTBI, or SGMIIPHY interface during core configuration and operation	1'b0
PCSLCHGIS	[1]	R	PCS Link Status Changed This bit is set because of any change in Link Status in the TBI, RTBI, or SGMII PHY interface (Bit 2 in Register 49 (AN Status Register)). This bit is cleared when you perform a read operation on the AN Status register. This bit is valid only when you select the optional TBI, RTBI, or SGMIIPHY interface during core configuration and operation.	1'b0
RGSMIIIS	[0]	R	RGMII or SMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII or SMII interface (Bit 3 in Register 54 (SGMII/RGMII/SMII Control and Status Register)). This bit is cleared when you perform a read operation on the SGMII/RGMII/SMII Control and Status Register. This bit is valid only when you select the optional RGMII or SMII PHY interface during core configuration and operation.	1'b0

16.3.1.2.12 Ethernet MAC Register 15

- Base Address: C006_0000h
- Address = Base Address + 0x3Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	21'b0
LPIIM	[10]	R	LPI Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the LPI Interrupt Status bit in Register 14 (Interrupt Status Register). This bit is valid only when you select the Energy Efficient Ethernet feature during core configuration. In all other modes, this bit is reserved.	1'b0
TSIM	[9]	R	Timestamp Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of Timestamp Interrupt Status bit in Register 14 (Interrupt Status Register). This bit is valid only when IEEE1588 time stamping is enabled. In all other modes, this bit is reserved.	1'b0
RSVD	[8:4]	–	Reserved	5'b0
PMTIM	[3]	R	PMT Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PMT Interrupt Status bit in Register 14 (Interrupt Status Register).	1'b0
PCSANCIM	[2]	R	PCS AN Completion Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of PCS Auto-negotiation complete bit in Register 14 (Interrupt Status Register).	1'b0
PCSLCHGIM	[1]	R	PCS Link Status Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the PCS Link-status changed bit in Register 14 (Interrupt Status Register).	1'b0
RGSMIIIM	[0]	R	RGMII or SMII Interrupt Mask When set, this bit disables the assertion of the interrupt signal because of the setting of the RGMII or SMII Interrupt Status bit in Register 14 (Interrupt Status Register).	1'b0

16.3.1.2.13 Ethernet MAC Register 16

- Base Address: C006_0000h
- Address = Base Address + 0x40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AE	[31]	R	Address Enable This bit is always set to 1.	1'b0
RSVD	[30:16]	–	Reserved	15'b0
ADDRHI	[15:0]	RW	MAC Address0 [47:32] This field contains the upper 16 bits (47:32) of the first 6-byte MAC address. The MAC uses this field for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames.	16'hFFFF

16.3.1.2.14 Ethernet MAC Register 17

- Base Address: C006_0000h
- Address = Base Address + 0x44h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDRLO	[31:0]	RW	MAC Address0 [31:0] This field contains the lower 32 bits of the first 6-byte MAC address. This is used by the MAC for filtering the received frames and inserting the MAC address in the Transmit Flow Control (Pause) Frames.	32'hFFFFFFFF

16.3.1.2.15 Ethernet MAC Register 18

- Base Address: C006_0000h
- Address = Base Address + 0x48h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
AE	[31]	R	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.	1'b0
SA	[30]	R	Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received frame. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received frame.	1'b0
MBC	[29:24]	R	Mask Byte Control These bits are mask control bits for comparison of each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: Register 18[15:8] Bit 28: Register 18[7:0] Bit 27: Register 19[31:24] … Bit 24: Register 19[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.	6'b0
RSVD	[23:16]	–	Reserved	8'b0
ADDRHI	[15:0]	RW	MAC Address1 [47:32] This field contains the upper 16 bits (47:32) of the second 6-byte MAC address.	16'hFFFF

16.3.1.2.16 Ethernet MAC Register 19

- Base Address: C006_0000h
- Address = Base Address + 0x4Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDRLO	[31:0]	RW	MAC Address1 [31:0] This field contains the lower 32 bits of the second 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.	32'hFFFFFFFF

16.3.1.2.17 Ethernet MAC Register 20 ~ 47

- Base Address: C006_0000h
- Address = Base Address + 0050h to 00BCh, Reset Value = –

The descriptions for registers 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, and 46 (MAC Address2 High Register through MAC Address15 High Register) are the same as for the Register 18 (MAC Address1 High Register).

The descriptions for registers 21, 23, 25, 27, 29, 31, 33, 35, 37, 38, 41, 43, 45, and 47 (MAC Address2 Low Register through MAC Address15 Low Register) are the same as for the Register 19 (MAC Address1 Low Register).

16.3.1.2.18 Ethernet MAC Register 48

- Base Address: C006_0000h
- Address = Base Address + 0xC0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:19]	–	Reserved	13'b0
SGMRAL	[18]	RW	SGMII RAL Control When set, this bit forces the SGMII RAL block to operate in the speed configured in the Speed and Port Select bits of the MAC Configuration register. This is useful when the SGMII interface is used in a direct MAC to MAC connection (without a PHY) and any MAC must reconfigure the speed. When reset, the SGMII RAL block operates according to the link speed status received on SGMII (from the PHY). This bit is reserved (and RO) if the SGMII PHY interface is not selected during core configuration.	1'b0
LR	[17]	RW	Lock to Reference When set, this bit enables the PHY to lock its PLL to the 125 MHz reference clock. This bit controls the pcs_lck_ref_o signal on the TBI, RTBI, or SGMII interface.	1'b0
ECD	[16]	RW	Enable Comma Detect When set, this bit enables the PHY for comma detection and word resynchronization. This bit controls the pcs_en_cdet_o signal on the TBI, RTBI or SGMII interface.	1'b0
RSVD	[15]	–	Reserved	1'b0
ELE	[14]	RW	External Loopback Enable When set, this bit causes the PHY to loopback the transmit data into the receive path. The pcs_ewrap _o signal is asserted high when this bit is set.	1'b0
RSVD	[13]	–	Reserved	1'b0
ANE	[12]	RW	External Loopback Enable When set, this bit causes the PHY to loopback the transmit data into the receive path. The pcs_ewrap _o signal is asserted high when this bit is set.	1'b0
RSVD	[11:10]	–	Reserved	2'b0
RAN	[9]	RW	Restart Auto-Negotiation When set, this bit causes auto-negotiation to restart if Bit 12 (ANE) is set. This bit is self-clearing after auto-negotiation starts. This bit should be cleared for normal operation.	1'b0
RSVD	[8:0]	–	Reserved	9'b0

16.3.1.2.19 Ethernet MAC Register 49

- Base Address: C006_0000h
- Address = Base Address + 0xC4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	–	Reserved	23'b0
SGMRAL	[8]	R	Extended Status This bit is tied to high if the TBI or RTBI interface is selected during core configuration indicating that the MAC supports extended status information in Register 53 (TBI Extended Status Register). This bit is tied to low if the SGMII interface is selected and the TBI or RTBI interface is not selected during core configuration indicating that Register 53 is not present.	1'b0
RSVD	[7:6]	–	Reserved	2'b0
ANC	[5]	R	Auto-Negotiation Complete When set, this bit indicates that the auto-negotiation process is complete. This bit is cleared when auto-negotiation is reinitiated.	1'b0
RSVD	[4]	–	Reserved	1'b0
ANA	[3]	R	Auto-Negotiation Ability This bit is always high because the MAC supports auto negotiation.	1'b0
LS	[2]	R	Link Status When set, this bit indicates that the link is up between the MAC and the TBI, RTBI, or SGMII interface. When cleared, this bit indicates that the link is down between the MAC and the TBI, RTBI, or SGMII interface.	1'b0
RSVD	[1:0]	–	Reserved	2'b0

16.3.1.2.20 Ethernet MAC Register 50

- Base Address: C006_0000h
- Address = Base Address + 0xC8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	16'b0
NP	[15]	R	Next Page Support This bit is always low because the MAC does not support the next page.	1'b0
RSVD	[14]	–	Reserved	1'b0
RFE	[13:12]	RW	Remote Fault Encoding These bits provide a remote fault encoding, indicating to a link partner that a fault or error condition has occurred. The encoding of these bits is defined in IEEE802.3z, Section 37.2.1.5.	2'b0
RSVD	[11:9]	–	Reserved	3'b0
PSE	[8:7]	RW	Pause Encoding These bits provide an encoding for the Pause bits, indicating that the MAC is capable of configuring the Pause function as defined in IEEE 802.3x. The encoding of these bits is defined in IEEE 802.3z, Section 37.2.1.4.	2'b0
HD	[6]	RW	Half-Duplex When set high, this bit indicates that the MAC supports the half-duplex mode. This bit is always low (and RO) when the MAC is configured for the full-duplex-only mode.	1'b0
FD	[5]	RW	Full-Duplex When set high, this bit indicates that the MAC supports the full-duplex mode	1'b0
RSVD	[4:0]	–	Reserved	5'b0

16.3.1.2.21 Ethernet MAC Register 51

- Base Address: C006_0000h
- Address = Base Address + 0xCCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	16'b0
NO	[15]	R	Next Page Support When set, this bit indicates that more next page information is available. When cleared, this bit indicates that next page exchange is not desired.	1'b0
ACK	[14]	R	Acknowledge When set, the auto-negotiation function uses this bit to indicate that the link partner has successfully received the base page of the MAC. When cleared, it indicates that the link partner did not successfully receive the base page of the MAC.	1'b0
RFE	[13:12]	R	Remote Fault Encoding These bits provide a remote fault encoding, indicating a fault or error condition of the link partner. The encoding of these bits is defined in IEEE 802.3z, Section37.2.1.5.	2'b0
RSVD	[11:9]	–	Reserved	3'b0
PSE	[8:7]	R	Pause Encoding These bits provide an encoding for the Pause bits, indicating that the link partner's capability of configuring the Pause function as defined in the IEEE 802.3xspecification. The encoding of these bits is defined in IEEE 802.3z, Section37.2.1.4.	2'b0
HD	[6]	R	Half-Duplex When set, this bit indicates that the link partner has the ability to operate in the half-duplex mode. When cleared, this bit indicates that the link partner does not have the ability to operate in the half-duplex mode.	1'b0
FD	[5]	R	Full-Duplex When set, this bit indicates that the link partner has the ability to operate in the full duplex mode. When cleared, this bit indicates that the link partner does not have the ability to operate in the full-duplex mode.	1'b0
RSVD	[4:0]	–	Reserved	5'b0

16.3.1.2.22 Ethernet MAC Register 52

- Base Address: C006_0000h
- Address = Base Address + 0xD0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	–	Reserved	29'b0
NPA	[2]	R	Next Page Ability This bit is always low because the MAC does not support the next page function.	1'b0
NPR	[1]	R	New Page Received When set, this bit indicates that the MAC has received a new page. This bit is cleared when read.	1'b0
RSVD	[0]	–	Reserved	1'b0

16.3.1.2.23 Ethernet MAC Register 53

- Base Address: C006_0000h
- Address = Base Address + 0xD4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	29'b0
gfd	[15]	R	1000BASE-X Full-Duplex Capable This bit indicates that the MAC is able to perform the full-duplex and1000BASE-X operations.	1'b0
ghd	[14]	R	1000BASE-X Half-Duplex Capable This bit indicates that the MAC is able to perform the half-duplex and1000BASE-X operations. This bit is always low when the MAC is configured for the full-duplex-only operation during core configuration.	1'b0
RSVD	[13:0]	–	Reserved	29'b0

16.3.1.2.24 Ethernet MAC Register 54

- Base Address: C006_0000h
- Address = Base Address + 0xD8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
SMIDRXS	[16]	RW	Delay SMII RX Data Sampling with respect to the SMII SYNC Signal When set, the first bit of the SMII RX data is sampled one cycle after the SMII SYNC signal. When reset, the first bit of the SMII RX data is sampled along with the SMII SYNC signal. If the SMII PHY Interface with source synchronous mode is selected during core configuration, this bit is reserved (RO with default value).	1'b0
RSVD	[15:6]	–	Reserved	10'b0
FALSCARDET	[5]	R	False Carrier Detected This bit indicates whether the SMII PHY detected false carrier (1'b1). This bit is reserved when the MAC is configured for the SGMII or RGMII PHY interface.	1'b0
JABTO	[4]	R	Jabber Timeout This bit indicates whether there is jabber timeout error (1'b1) in the received frame. This bit is reserved when the MAC is configured for the SGMII or RGMII PHY interface.	1'b0
LNKSTS	[3]	R	Link Status When set, this bit indicates that the link is up between the local PHY and the remote PHY. When cleared, this bit indicates that the link is down between the local PHY and the remote PHY.	1'b0
LNKSPEED	[2:1]	R	Link Speed This bit indicates the current speed of the link: 00 = 2.5 MHz 01 = 25 MHz 10 = 125 MHz Bit 2 is reserved when the MAC is configured for the SMII PHY interface.	1'b0
LNKMOD	[0]	R	Link Mode This bit indicates the current mode of operation of the link: 1'b0 = Half-duplex mode 1'b1 = Full-duplex mode	1'b0

16.3.1.2.25 Ethernet MAC Register 448

- Base Address: C006_0000h
- Address = Base Address + 0x700h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	–	Reserved	3'b0
ATSEN3	[28]	RW	Auxiliary Snapshot 3 Enable This field controls capturing the Auxiliary Snapshot Trigger 3. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[3] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration or the selected number in the Number of IEEE 1588 Auxiliary Snapshot Inputs option is less than four.	1'b0
ATSEN2	[27]	RW	Auxiliary Snapshot 2 Enable This field controls capturing the Auxiliary Snapshot Trigger 2. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[2] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration or the selected number in the Number of IEEE 1588 Auxiliary Snapshot Inputs option is less than three.	16'b0
ATSEN1	[26]	RW	Auxiliary Snapshot 1 Enable This field controls capturing the Auxiliary Snapshot Trigger 1. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration or the selected number in the Number of IEEE 1588 Auxiliary Snapshot Inputs option is less than two.	1'b0
ATSEN0	[25]	RW	Auxiliary Snapshot 0 Enable This field controls capturing the Auxiliary Snapshot Trigger 0. When this bit is set, the Auxiliary snapshot of event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration.	1'b0
ATSFC	[24]	RW	Auxiliary Snapshot FIFO Clear When set, it resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, auxiliary snapshots get stored in the FIFO. This bit is reserved when the Add IEEE 1588 Auxiliary Snapshot option is not selected during core configuration.	1'b0

Name	Bit	Type	Description	Reset Value
RSVD	[23:19]	–	Reserved	3'b0
TSENMACADDR	[18]	RW	Enable MAC address for PTP Frame Filtering When set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP frames when PTP is directly sent over Ethernet.	1'b0
SNAPTYPSEL	[17:16]	RW	Select PTP packets for Taking Snapshots These bits along with Bits 15 and 14 decide the set of PTP packet types for which snapshot needs to be taken.	2'b0
TSMSTRENA	[15]	RW	Enable Snapshot for Messages Relevant to Master When set, the snapshot is taken only for the messages relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node.	1'b0
TSEVNTENA	[14]	RW	Enable Timestamp Snapshot for Event Messages When set, the timestamp snapshot is taken only for event messages(SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When reset, the snapshot is taken for all messages except Announce, Management, and Signaling.	1'b0
TSIPV4ENA	[13]	RW	Enable Processing of PTP Frames Sent over IPv4-UDP When set, the MAC receiver processes the PTP packets encapsulated in UDP over IPv4 packets. When this bit is clear, the MAC ignores the PTP transported over UDP-IPv4 packets. This bit is set by default.	1'b0
TSIPV6ENA	[12]	RW	Enable Processing of PTP Frames Sent over IPv6-UDP When set, the MAC receiver processes PTP packets encapsulated in UDP over IPv6 packets. When this bit is clear, the MAC ignores the PTP transported over UDP-IPv6 packets.	1'b0
TSIPENA	[11]	RW	Enable Processing of PTP over Ethernet Frames When set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet frames. When this bit is clear, the MAC ignores the PTP over Ethernet packets.	1'b0
TSVER2ENA	[10]	RW	Enable PTP packet Processing for Version 2 Format When set, the PTP packets are processed using the 1588 version 2format. Otherwise, the PTP packets are processed using the version 1format.	1'b0
TSCTRLSSR	[9]	RW	Timestamp Digital or Binary Rollover Control When set, the Timestamp Low register rolls over after 0x3B9A_C9FFvalue (that is, 1 nanosecond accuracy) and increments the timestamp(High) seconds. When reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment has to be programmed correctly depending on the PTP reference clock frequency and the value of this bit.	1'b0
TSENALL	[8]	RW	Enable Timestamp for All Frames When set, the timestamp snapshot is enabled for all	1'b0

Name	Bit	Type	Description	Reset Value
			frames received by the MAC.	
RSVD	[7:6]	–	Reserved	2'b0
TSADDREG	[5]	RW	Addend Reg Update When set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This is cleared when the update is completed. This register bit should be zero before setting it.	1'b0
TSTRIG	[4]	RW	Timestamp Interrupt Trigger Enable When set, the timestamp interrupt is generated when the System Time becomes greater than the value written in the Target Time register. This bit is reset after the generation of the Timestamp Trigger Interrupt.	1'b0
TSUPDT	[3]	RW	Timestamp Update When set, the system time is updated (added or subtracted) with the value specified in Register 452 (System Time - Seconds Update Register) and Register 453 (System Time - Nanoseconds Update Register). This bit should be read zero before updating it. This bit is reset when the update is completed in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated.	1'b0
TSINIT	[2]	RW	Timestamp Initialize When set, the system time is initialized (overwritten) with the value specified in the Register 452 (System Time - Seconds Update Register) and Register 453 (System Time - Nanoseconds Update Register). This bit should be read zero before updating it. This bit is reset when the initialization is complete. The "Timestamp Higher Word" register (if enabled during core configuration) can only be initialized.	1'b0
TSCFUPDT	[1]	RW	Timestamp Fine or Coarse Update When set, this bit indicates that the system time update should be done using the fine update method. When reset, it indicates the system timestamp update should be done using the Coarse method.	1'b0
TSENA	[0]	RW	Timestamp Enable When set, the timestamp is added for the transmit and receive frames. When disabled, timestamp is not added for the transmit and receive frames and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the receive side, the MAC processes the 1588 frames only if this bit is set.	1'b0

16.3.1.2.26 Ethernet MAC Register 449

- Base Address: C006_0000h
- Address = Base Address + 0x704h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	24'b0
SSINC	[7:0]	RW	Sub-second Increment Value The value programmed in this field is accumulated every clock cycle (ofclk_ptp_i) with the contents of the sub-second register. For example, when PTP clock is 50 MHz (period is 20 ns), you should program 20(0x14) when the System Time- Nanoseconds register has an accuracy of1 ns [Bit 9 (TSCTRLSSR) is set in Register 448 (Timestamp Control Register)]. When TSCTRLSSR is clear, the Nanoseconds register has are solution of ~ 0.465ns. In this case, you should program a value of 43(0x2B) that is derived by 20ns/0.465.	8'b0

16.3.1.2.27 Ethernet MAC Register 450

- Base Address: C006_0000h
- Address = Base Address + 0x708h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TSS	[31:0]	R	Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC.	32'b0

16.3.1.2.28 Ethernet MAC Register 451

- Base Address: C006_0000h
- Address = Base Address + 0x70Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
TSSS	[30:0]	R	Timestamp Sub Seconds The value in this field has the sub second representation of time, with an accuracy of 0.46 ns. When Bit 9 (TSCTRLSSR) is set in Register 448(Timestamp Control Register), each bit represents 1 ns and the maximum value is 0x3B9A_C9FF, after which it rolls-over to zero.	31'b0

16.3.1.2.29 Ethernet MAC Register 452

- Base Address: C006_0000h
- Address = Base Address + 0x710h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TSS	[31:0]	RW	Timestamp Second The value in this field indicates the time in seconds to be initialized or added to the system time.	32'b0

16.3.1.2.30 Ethernet MAC Register 453

- Base Address: C006_0000h
- Address = Base Address + 0x714h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDSUB	[31]	RW	Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register.	1'b0
TSSS	[30:0]	RW	Timestamp Sub Seconds The value in this field has the sub second representation of time, with an accuracy of 0.46 ns. When Bit 9 (TSCTRLSSR) is set in Register 448(Timestamp Control Register), each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF.	31'b0

16.3.1.2.31 Ethernet MAC Register 454

- Base Address: C006_0000h
- Address = Base Address + 0x718h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TSAR	[31:0]	RW	Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.	32'b0

16.3.1.2.32 Ethernet MAC Register 455

- Base Address: C006_0000h
- Address = Base Address + 0x71Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TSTR	[31:0]	RW	Target Time Seconds Register This register stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, then based on Bits[6:5] of Register 459 (PPS Control Register), the MAC starts or stops the PPS signal output and generates an interrupt (if enabled).	32'b0

16.3.1.2.33 Ethernet MAC Register 456

- Base Address: C006_0000h
- Address = Base Address + 0x720h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TRGTBUSY	[31]	RW	Target Time Register Busy The MAC sets this bit when the PPSCMD field (Bit [3:0]) in Register459 (PPS Control Register) is programmed to 010 or 011.Programming the PPSCMD field to 010 or 011, instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted. This bit is reserved when the Enable Flexible Pulse-Per-Second Output feature is not selected.	1'b0
TTSLO	[30:0]	RW	Target Timestamp Low Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the both Target Timestamp registers, then based on the TRGTMODSEL0 field (Bits [6:5]) in Register 459 (PPSControl Register), the MAC starts or stops the PPS signal output and generates an interrupt (if enabled). This value should not exceed 0x3B9A_C9FF when Bit 9(TSCTRLSSR) is set in Register 448 (Timestamp Control Register).The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value.	31'b0

16.3.1.2.34 Ethernet MAC Register 457

- Base Address: C006_0000h
- Address = Base Address + 0x724h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	16'b0
TSHWR	[15:0]	RW	Timestamp Higher Word Register This field contains the most significant 16 bits of the timestamp seconds value. This register is optional and can be selected using the Enable IEEE1588 Higher Word Register option during core configuration. The register is directly written to initialize the value. This register is incremented when there is an overflow from the 32 bits of the System Time - Seconds register.	16'b0

16.3.1.2.35 Ethernet MAC Register 458

- Base Address: C006_0000h
- Address = Base Address + 0x728h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	–	Reserved	2'b0
ATSNS	[29:25]	R	Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected during core configuration.	5'b0
ATSSTM	[24]	R	Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected during core configuration.	1'b0
RSVD	[23:20]	–	Reserved	4'b0
ATSSTN	[19:16]	R	Auxiliary Timestamp Snapshot Trigger Identifier These bits identify the Auxiliary trigger inputs for which the time stamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: Bit 16: Auxiliary trigger 0	4'b0

Name	Bit	Type	Description	Reset Value
			Bit 17: Auxiliary trigger 1 Bit 18: Auxiliary trigger 2 Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken.	
RSVD	[15:10]	–	Reserved	6'b0
TSTRGTERR3	[9]	R	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 496and Register 497, is already elapsed. This bit is cleared when read by the application.	1'b0
TSTARGT3	[8]	R	Timestamp Target Time Reached for Target Time PPS3 When set, this bit indicates that the value of system time is greater than or equal to the value specified in Register 496 (PPS3 Target Time High Register) and Register 497 (PPS3 Target Time Low Register).	1'b0
TSTRGTERR2	[7]	R	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 488and Register 489, is already elapsed. This bit is cleared when read by the application.	1'b0
TSTARGT2	[6]	R	Timestamp Target Time Reached for Target Time PPS2 When set, this bit indicates that the value of system time is greater than or equal to the value specified in Register 488 (PPS2 Target Time High Register) and Register 489 (PPS2 Target Time Low Register).	1'b0
TSTRGTERR1	[5]	R	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 480and Register 481, is already elapsed. This bit is cleared when read by the application.	1'b0
TSTARGT1	[4]	R	Timestamp Target Time Reached for Target Time PPS1 When set, this bit indicates that the value of system time is greater than or equal to the value specified in Register 480 (PPS1 Target Time High Register) and Register 481 (PPS1 Target Time Low Register).	1'b0
TSTRGTERR	[3]	R	Timestamp Target Time Error This bit is set when the target time, being programmed in Register 455and Register 456, is already elapsed. This bit is cleared when read by the application.	1'b0
AUXTSTRIG	[2]	R	Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Enable IEEE 1588 Auxiliary Snapshot feature is selected.	1'b0
TSTARGT	[1]	R	Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the Register 455 (Target Time Seconds Register) and Register 456	1'b0

Name	Bit	Type	Description	Reset Value
			(Target Time Nanoseconds Register).	
TSSOVF	[0]	R	Timestamp Seconds Overflow When set, this bit indicates that the seconds value of the timestamp(when supporting version 2 format) has overflowed beyond32'hFFFF_FFFF.	1'b0

16.3.1.2.36 Ethernet MAC Register 512 ~ 543

- Base Address: C006_0000h
- Address = Base Address + 0800h to 087Ch, Reset Value =

The descriptions for registers 512, 514, 516, 518, 520, 522, 524, 526, 528, 530, 532, 534, 536, 538, 540, and 542 (MAC Address16 High Register through MAC Address31 High Register) are the same as for the Register 18 (MAC Address1 High Register).

The descriptions for registers 513, 515, 517, 519, 521, 523, 525, 527, 529, 531, 533, 535, 537, 539, 541, and 543 (MAC Address16 Low Register through MAC Address31 Low Register) are the same as for the Register 19 (MAC Address1 Low Register).

17 SD/MMC Controller

17.1 Overview

This Section describes Secure Digital (SD/SDIO), Multimedia Card (MMC), CT-ATA host controller and related register that S5P4418 supports. The Mobile Storage Host is an interface between system and SD/MMC card.

17.1.1 Features

- Compatible with the Multi-Media Card System Specification, (MMC 4.41, eMMC 4.5)
- Compatible with the Secure Digital memory Specification, (SD 3.0)
- Compatible with the Secure Digital I/O Specification, (SDIO 3.0)
- Supports clock speeds up to 50 MHz
- Contains an Internal Clock Pre-Scaler
- Contains 32 Bytes of FIFO for data Receive/Transmit
- 3 Channel of SD/MMC

17.1.1.1 Features of Mobile Storage Host

- The following are features of the Mobile Storage Host:
  - Supports Secure Digital memory protocol commands
  - Supports Secure Digital I/O protocol commands
  - Supports Multimedia Card protocol commands
  - Supports CE-ATA digital protocol commands
  - Supports Command Completion signal and interrupt to host processor
  - Command Completion Signal disable feature
- The following features of MMC4.41 are supported:
  - DDR in 4-bit mode
  - GO_PRE_IDLE_STATE command (CMD with argument 0xF0F0F0F0)
  - New EXTCSD registers
  - Hardware Reset as supported by MMC 4.41
- The following IP-specific features of eMMC 4.5 are supported:
  - HS200 Mode (4 bits)
  - Packed Commands, CMD21, CMD49
  - Support for 1.2/1.8/3.3V of operation control
  - START bit behavior change for DDR modes
- The following IP-specific features of MMC 4.41 are not supported:
  - Boot in DDR mode

17.2 Block Diagram

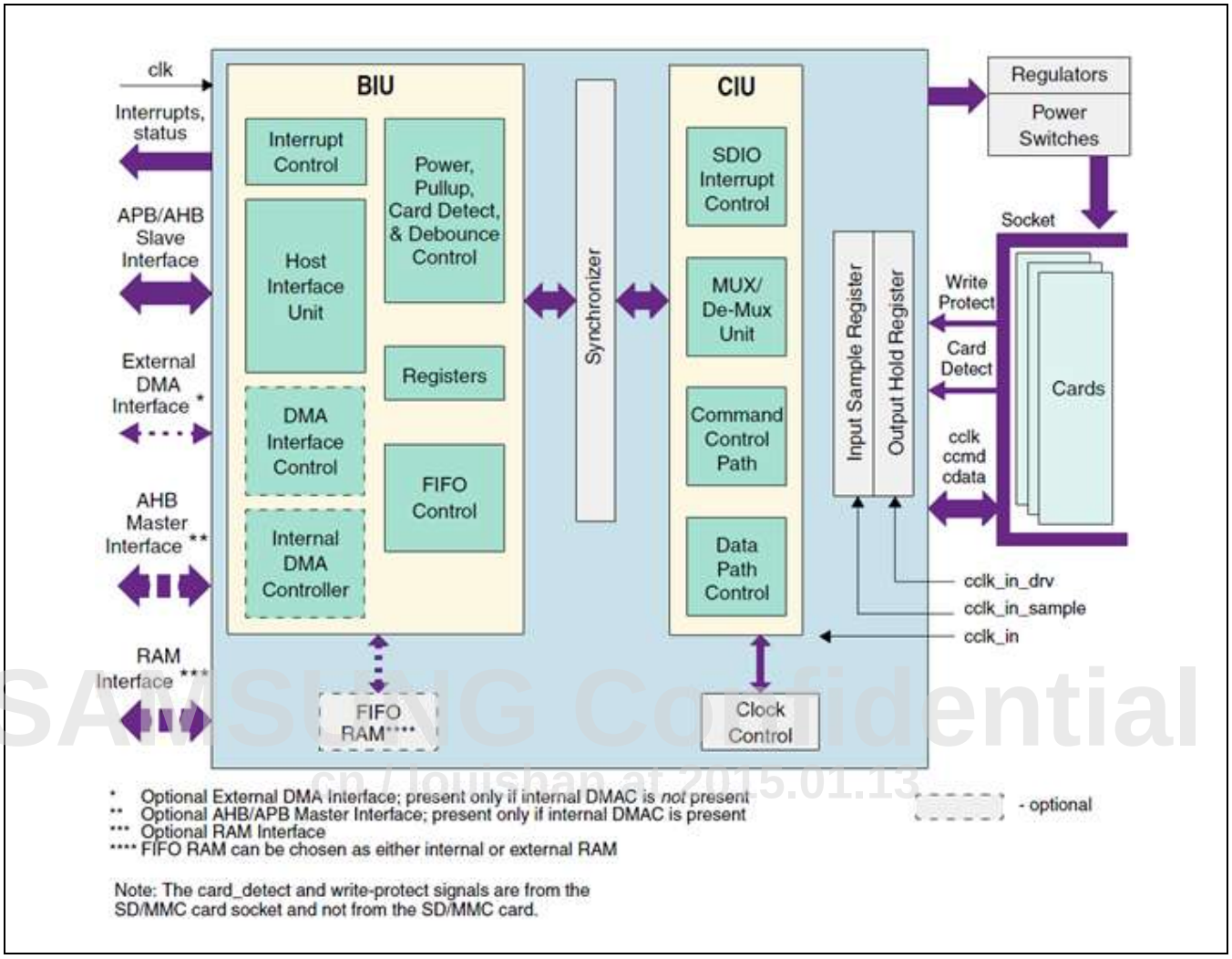


Figure 17-1 Block Diagram of Mobile Storage Host

Figure 17-1 illustrates the block diagram of Mobile Storage Host.

- Bus Interface Unit (BIU): Provides AMBA AHB/APB and DMA interfaces for register and data read/writes
- Card Interface Unit (CIU): Takes care of SD_MMC_CEATA protocols and provides clock management.

The BIU provides the host interface to the registers. It also provides the data FIFO through the Host Interface Unit (HIU). Additionally, it provides independent data FIFO access through a DMA interface. You can configure host interface as an AMBA APB slave interface.

The IDMAC is responsible for exchanging data between FIFO and the host memory. A set of IDMAC registers is accessible by host for controlling the IDMAC operation through the AMBA APB slave interface.

The Mobile Storage CIU controls the card-specific protocols. Within CIU, the command path control unit and data path control unit interface with the controller to the command and data ports of the SD_MMC_CEATA cards. The CIU alos provides clock control.

17.2.1.1 Clock Phase Shifter

SD/MMC card receives DATA/CMD with card clock from the host controller. To synchronize the clock and DATA/CMD, it is required that the clock delay is inserted to the Tx/Rx clock path. For this to happen, the logic is added to the design as illustrated in the *Figure 17-2*. And clock selection can be done with CLKSEL register at the end of this Section.

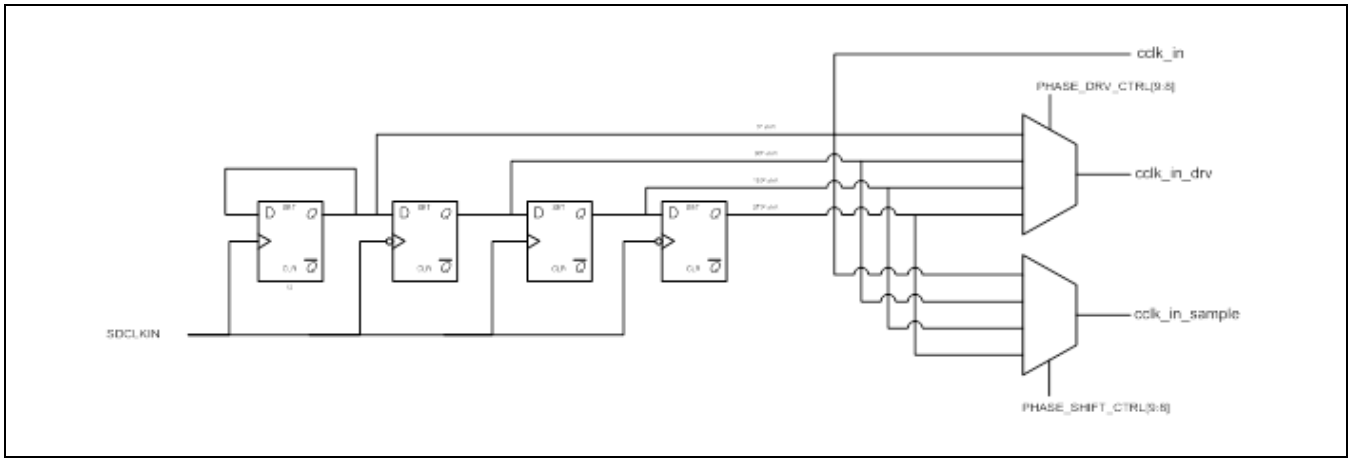


Figure 17-2 Block Diagram of Mobile Storage Host

This clock phase shifter makes 0, 90, 180, 270 phase shifted clocks for Tx/Rx respectively. To make 50 MHz phase shifted clock, SDCLKIN should be 100 MHz.

17.3 Register Description

17.3.1 Register Map Summary

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)

Register	Offset	Description	Reset Value
CTRL	00h, 00h, 00h	SD/MMC control register	0x1000_0000
POWER_ENABLE	04h, 04h, 04h	SD/MMC power enable register	0x0000_0000
CLKDIV	08h, 08h, 08h	SD/MMC clock divider register	0x0000_0000
CLK_SOURCE	0Ch, 0Ch, 0Ch	SD/MMC clock source register	0x0000_0000
CLKENA	10h, 10h, 10h	SD/MMC clock enable register	0x0000_0000
TMOUT	14h, 14h, 14h	SD/MMC timeout register	0xFFFF_FF40
CTYPE	18h, 18h, 18h	SD/MMC card type register	0x0000_0000
BLKSIZ	1Ch, 1Ch, 1Ch	SDMMC block size register	0x0000_0000
BYTCNT	20h, 20h, 20h	SD/MMC byte count register	0x0000_0200
INTMASK	24h, 24h, 24h	SD/MMC interrupt mask register	0x0000_0000
CMDARG	28h, 28h 28h	SD/MMC command argument register	0x0000_0000
CMD	2Ch, 2Ch,	SD/MMC command register	0x2000_0000

Register	Offset	Description	Reset Value
	2Ch		
RESP0	30h, 30h, 30h	SD/MMC response register 0	0x0000_0000
RESP1	34h, 34h, 34h	SD/MMC response register 1	0x0000_0000
RESP2	38h, 38h, 38h	SD/MMC response register 2	0x0000_0000
RESP3	3Ch, 3Ch, 3Ch	SD/MMC response register 3	0x0000_0000
MINTSTS	40h, 40h, 40h	SD/MMC masked interrupt status register	0x0000_0000
RINTSTS	44h, 44h, 44h	SD/MMC raw interrupt status register	0x0000_0000
STATUS	48h, 48h, 48h	SD/MMC status register	0x0000_0006
FIFOTH	4Ch, 4Ch, 4Ch	SD/MMC FIFO threshold watermark register	0x0000_0000
CDETECT	50h, 50h, 50h	SD/MMC card detect register	0x0000_0000
WRTPRT	54h, 54h, 54h	SD/MMC card write protect register	0x0000_0000
RSVD	58h, 58h, 58h	Reserved	0x0000_0000
TCBCNT	5Ch, 5Ch, 5Ch	SD/MMC transferred CIU card byte count register	0x0000_0000
TBBCNT	60h, 60h, 60h	SD/MMC transferred host to BIU-FIFO byte count register	0x0000_0000
DEBNCE	64h,	SD/MMC de-bounce count register	0x00FF_FFFF

Register	Offset	Description	Reset Value
	64h, 64h		
USRID	68h, 68h, 68h	SD/MMC user ID register	0x0000_0000
VERID	6Ch, 6Ch, 6Ch	SD/MMC version ID register	0x5342_240A
RSVD	70h, 70h, 70h	Reserved	0x0000_0000
UHS_REG	74h, 74h, 74h	SD/MMC UHS-1 register	0x0000_0000
RST_n	78h, 78h, 78h	SD/MMC H/W reset	0x0000_0000
BMODE	80h, 80h, 80h	SD/MMC bus mode register	0x0000_0000
PLDMND	84h, 84h, 84h	SD/MMC poll demand register	0x0000_0000
DBADDR	88h, 88h, 88h	SD/MMC descriptor list base address register	0x0000_0000
IDSTS	8Ch, 8Ch, 8Ch	SD/MMC internal DMAC status register	0x0000_0000
IDINTEN	90h, 90h, 90h	SD/MMC internal DMAC interrupt enable register	0x0000_0000
DSCADDR	94h, 94h, 94h	SD/MMC current host descriptor address register	0x0000_0000
BUFADDR	98h, 98h, 98h	SD/MMC current buffer descriptor address register	0x0000_0000
RSVD	9Ch, 9Ch, 9Ch	Reserved	0x0000_0000

Register	Offset	Description	Reset Value
CARDTHRCTL	100h, 100h, 100h	SD/MMC card threshold control register	0x0000_0000
BACK_END_POWER	104h, 104h, 104h	SD/MMC back-end power register	0x0000_0000
RSVD	108h, 108h, 108h	Reserved	0x0000_0000
EMMC_DDR_REG	10Ch, 10Ch, 10Ch	SD/MMC eMMC 4.5 DDR start bit detection control register	0x0000_0000
RSVD	110h, 110h, 110h	Reserved	0x0000_0000
EMMC_DDR_REG	114h, 114h, 114h	SD/MMC enable phase shift register	0x0000_0000
RSVD	118h to 1FFh, 110h to 1FFh, 110h	Reserved	0x0000_0000
Data	200h, 200h, 200h	SD/MMC data register	Undefine

17.3.1.1 CTRL

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 00h, + 00h, + 00h, Reset Value = 0x1000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	6'b0
use_internal_dmac	[25]	RW	Present only for the Internal DMAC configuration; else, it is reserved. 0 = The host performs data transfers through the slave interface 1 = Internal DMAC used for data transfer	1'b0
enable_od_pullup	[24]	RW	External open-drain pull up: 0 = Disable 1 = Enable Inverted value of this bit is output to ccmd_od_pullup_en_n port. When bit is set, command output always driven in open-drive mode; that is,DWC_mobile_storage drives either 0 or high impedance, and does not drive hard 1.	1'b1
Card_voltage_b	[23:20]	RW	Card regulator-B voltage setting; output to card_volt_b port. Optional feature; ports can be used as general-purpose outputs.	4'b0
Card_voltage_a	[19:16]	RW	Card regulator-A voltage setting; output to card_volt_a port. Optional feature; ports can be used as general-purpose outputs.	4'b0
RSVD	[15:12]	RW	Reserved	3'b0
ceata_device_interrupt_status	[11]	RW	0 = Interrupts not enabled in CE-ATA device (nIEN = 1 in ATA control register) 1 = Interrupts are enabled in CE-ATA device (nIEN = 0 in ATA control register) Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled (nIEN = 1). If the host enables CE-ATA device interrupt, then software should set this bit.	1'b0
send_auto_stop_ccsd	[10]	RW	0 = Clear bit if DWC_mobile_storage does not reset the bit. 1 = Send internally generated STOP after sending CCSD to CE-ATA device. NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together; send_auto_stop_ccsd should not be set independent of send_ccsd. When set,	1'b0

Name	Bit	Type	Description	Reset Value
			DWC_Mobile_Storage automatically sends internally generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, DWC_mobile_storage automatically clears send_auto_stop_ccsd bit.	
send_ccsd	[9]	RW	0 = Clear bit if DWC_mobile_storage does not reset the bit. 1 = Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, DWC_mobile_storage sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, DWC_mobile_storage automatically clears send_ccsd bit. It also sets Command Done (CD) bi tin RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signaled CCS.	1'b0
abort_read_data	[8]	RW	0 = No change 1 = After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.	1'b0
send_irq_response	[7]	RW	0 = No change 1 = Send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, host issues CMD40, and DWC_mobile_storage waits for interrupt response from MMC card(s). In meantime, if host wants DWC_mobile_storage to exit waiting for interrupt state, it can set this bit, at which time DWC_mobile_storage command state-machine sends CMD40 response on bus and returns to idle state.	1'b0
read_wait	[6]	RW	For sending read-wait to SDIO cards. 0 = Clear read wait 1 = Assert read wait	1'b0
RSVD	[5]	–	Reserved	–

Name	Bit	Type	Description	Reset Value
int_enable	[4]	RW	Global interrupt enable/disable bit 0 = Disable interrupt 1 = Enable interrupt The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.	1'b0
RSVD	[3]	RW	Reserved.	1'b0
dma_reset	[2]	RW	0 = No change 1 = Reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.	1'b0
FIFO_Reset	[1]	RW	0 = No change 1 = Reset to data FIFO To reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.	1'b0
controller_reset	[0]	RW	0 = No change 1 = Reset DWC_mobile_storage controller To reset controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: • BIU/CIU interface • CIU and state machines • abort_read_data, send_irq_response, and read_wait bits of Control register • start_cmd bit of Command register Does not affect any registers or DMA interface, or FIFO or host interrupts	1'b0

17.3.1.2 POWER_ENABLE

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 04h, + 04h, + 04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	–
power_enable	[0]	RW	Power on/off switch for up to 16 cards; for example, bit[0] controls card 0.Once power is turned on, firmware should wait for regulator/switch ramp-uptime before trying to initialize card. 0 = Power off 1 = Power on Only NUM_CARDS number of bits are implemented. Bit values output to card_power_en port. Optional feature; ports can be used as general-purpose outputs.	1'b0

17.3.1.3 CLKDIV

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 08h, + 08h, + 08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
clk_divider3	[31:24]	RW	Clock divider-3 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), a value of 1 means divide by 2*1 = 2, a value of "ff" means divide by 2*255 = 510, and so on.	8'b0
clk_divider2	[23:16]	RW	Clock divider-2 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), a value of 1 means divide by 2*1 = 2, a value of "ff" means divide by 2*255 = 510, and so on.	8'b0
clk_divider1	[15:8]	RW	Clock divider-1 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), a value of 1 means divide by 2*1 = 2, a value of "ff" means divide by 2*255 = 510, and so on.	8'b0
clk_divider0	[7:0]	RW	Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), a value of 1 means divide by 2*1 = 2, a value of "ff" means divide by 2*255 = 510, and so on.	8'b0

17.3.1.4 CLK_SOURCE

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 0Ch, + 0Ch, + 0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	–
CLK_Source	[1:0]	RW	Clock divider source 00 = Clock divider 0 01 = Clock divider 1 10 = Clock divider 2 11 = Clock divider 3	32'b0

17.3.1.5 CLKENA

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 10h, + 10h, + 10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
cclk_low_power	[16]	RW	Low power control. If enabled, stop clock when card in idle status. 0 = Low power disable 1 = Low power enable	1'b0
RSVD	[15:1]	RW	Reserved	15'b0
cclk_enable	[0]	RW	Clock enable control 0 = Disable sd clock 1 = Enable sd clock	1'b0

17.3.1.6 TMOUT

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 14h, + 14h, + 14h, Reset Value = 0xFFFF_FF40

Name	Bit	Type	Description	Reset Value
data_timeout	[31:8]	RW	Value for card Data Read Timeout; same value also used for Data Starvation by Host timeout. The timeout counter is started only after the card clock is stopped. Value is in number of card output clocks - cclk_out of selected card.	24'hFF_FFFF
response_timeout	[7:0]	RW	Response timeout value. Value is in number of card output clocks - cclk_out.	8'h40

17.3.1.7 CTYPE

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 18h, + 18h, + 18h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
card_width	[16]	RW	8-bit interface mode. In S5P4418, this bit must be 0.	1'b0
RSVD	[15:1]	–	Reserved.	15'b0
card_width	[0]	RW	Card bus width. 0 = 1-bit mode 1 = 4-bit mode	1'b0

17.3.1.8 BLKSIZ

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 1Ch, + 1Ch, + 1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	16'b0
blksize	[15:0]	RW	Block size in bytes.	16'h200

17.3.1.9 BYTCNT

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 20h, + 20h, + 20h, Reset Value = 0x0000_0200

Name	Bit	Type	Description	Reset Value
byte_count	[31:0]	RW	Number of bytes to be transferred; should be integer multiple of Block Size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.	32'h200

17.3.1.10 INTMASK

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 24h, + 24h, + 24h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
sdio_int_mask	[16]	RW	SDIO interrupt mask. 0 = Masked 1 = Enabled	1'b0
mAsk_ebe	[15]	RW	End bit error (read), Write no CRC (write) interrupt mask.	1'b0
mAsk_acd	[14]	RW	Auto command done interrupt mask.	1'b0
mAsk_sbe	[13]	RW	Start bit error / Busy Complete interrupt mask	1'b0
mAsk_hle	[12]	RW	Hardware locked write error interrupt mask	1'b0
mAsk_frun	[11]	RW	FIFO under run/overrun error interrupt mask	1'b0
mAsk_hto	[10]	RW	Data starvation by host timeout/Volt_switch_int interrupt mask	1'b0
mAsk_drto	[9]	RW	Data read timeout interrupt mask	1'b0
mAsk_rto	[8]	RW	Response timeout interrupt mask	1'b0
mAsk_dcrc	[7]	RW	Data CRC error interrupt mask	1'b0
mAsk_rcrc	[6]	RW	Response CRC error interrupt mask	1'b0
mAsk_rxdr	[5]	RW	Receive FIFO data request interrupt mask	1'b0
mAsk_txdr	[4]	RW	Transmit FIFO data request interrupt mask	1'b0
mAsk_dto	[3]	RW	Data transfer over interrupt mask	1'b0
mAsk_cd	[2]	RW	Command done interrupt mask	1'b0
mAsk_re	[1]	RW	Response error interrupt mask	1'b0
MASK_CD	[0]	W	This bit must be "0"	1'b0

17.3.1.11 CMDARG

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 28h, + 28h, + 28h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
cmdarg	[31:0]	RW	Value indicates command argument to be passed to card.	32'b0

17.3.1.12 CMD

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 2Ch, + 2Ch, + 2Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
start_cmd	[31]	RW	Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD_MMC_CEATA cards, Command Done bit is set in raw interrupt register.	1'b0
RSVD	[30]	–	Reserved	1'b0
use_hold_reg	[29]	RW	Use Hold Register 0 = CMD and DATA sent to card bypassing HOLD Register 1 = CMD and DATA sent to card through the HOLD Register	1'b1
volt_switch	[28]	RW	Voltage switch bit 0 = No voltage switching 1 = Voltage switching enabled; must be set for CMD11 only	1'b0
boot_mode	[27]	RW	Boot Mode 0 = Mandatory Boot operation 1 = Alternate Boot operation	1'b0
disable_boot	[26]	RW	Disable Boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do NOT set disable_boot and enable_boot together.	1'b0
expect_boot_ack	[25]	RW	Expect Boot Acknowledge. When Software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0from the selected card.	1'b0

Name	Bit	Type	Description	Reset Value
enable_boot	[24]	RW	Enable Boot-this bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do NOT set disable_boot and enable_boot together	1'b0
ccs_expected	[23]	RW	0 = Interrupts are not enabled in CE-ATA device (nIEN = 1 inATA control register), or command does not expect CCS from device 1 = Interrupts are enabled in CE-ATA device (nIEN = 0), and RW_BLK command expects command completion signal from CE-ATA device If the command expects Command Completion Signal (CCS) from the CE-ATA device, the software should set this control bit. DWC_mobile_storage sets Data Transfer Over (DTO) bit in RINTSTS register and generates interrupt to host if Data Transfer Over interrupt is not masked.	1'b0
read_ceata_device	[22]	RW	0 = Host is not performing read access (RW_REG or RW_BLK)towards CE-ATA device 1 = Host is performing read access (RW_REG or RW_BLK)towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than10 seconds. DWC_mobile_storage should not indicate read data timeout while waiting for data from CE-ATA device.	1'b0
update_clock_register_only	[21]	RW	0 = Normal command sequence 1 = Do not send commands, just update clock register value into card clock domain Following register values transferred into card clock domain:CLKDIV, CLRSRC, CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_registers_only = 0, following control registers are transferred from BIU to CIU: CMD, CMDARG, TMOUT, CTYPE, BLKSIZ, BYTCNT. CIU uses new register values for new command sequence to card(s). When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.	1'b0
card_number	[20:16]	RW	Card number in use. In S5P4418, this value must be 0.	5'b0
send_initialization	[15]	RW	After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit	1'b0

Name	Bit	Type	Description	Reset Value
			should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory). 0 = Do not send initialization sequence before sending command 1 = Send initialization sequence before sending command	
stop_abort_cmd	[14]	RW	0 = Neither stop nor abort command to stop current data transferrin progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1 = Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along withCMD[26] = disable_boot.	1'b0
wait_prvdata_complete	[13]	RW	0 = Send command at once, even if previous data transfer has not completed 1 = Wait for previous data transfer completion before sending command The wait_prvdata_complete = 0 option typically used to query status of card during data transfer or to stop current data transfer;card_number should be same as in previous command.	1'b0
send_auto_stop	[12]	RW	0 = No stop command sent at end of data transfer 1 = Send stop command at end of data transfer When set, mobile_storage sends stop command toSD_MMC_CEATA cards at end of data transfer when send_auto_stop bit should be set, since some data transfers do not need explicit stop commands open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume - suspended memory access of SD-Combo card - bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.	1'b0
transfer_mode	[11]	RW	Transfer mode. Don't care if no data expected. 0 = Block data transfer mode 1 = Stream data transfer mode	1'b0
read/write	[10]	RW	Read/Write mode selection. Don't care if no data expected. 0 = Read from card	1'b0

Name	Bit	Type	Description	Reset Value
			1 = Write to card	
data_expected	[9]	RW	Data transfer expected flag. 0 = No data transfer expected 1 = Data transfer expected	1'b0
check_response_crc	[8]	RW	0 = Do not check response CRC 1 = Check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.	1'b0
response_length	[7]	RW	Response length selection. 0 = Short response 1 = Long response	1'b0
response_expect	[6]	RW	Response expected flag. 0 = No response expected 1 = Response expected	1'b0
cmd_index	[5:0]	RW	Command index.	6'b0

17.3.1.13 RESP0

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 30h, + 30h, + 30h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
response0	[31:0]	R	Bit[31:0] of response	32'b0

17.3.1.14 RESP1

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 34h, + 34h, + 34h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Response1	[31:0]	R	Bit[63:32] of long response.	32'b0

17.3.1.15 RESP2

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 38h, + 38h, + 38h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Response2	[31:0]	R	Bit[95:64] of long response.	32'b0

17.3.1.16 RESP3

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 3Ch, + 3Ch, + 3Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Response3	[31:0]	R	Bit[127:96] of long response.	32'b0

17.3.1.17 MINTSTS

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 40h, + 40h, + 40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
SDIO_iNTerrupt	[16]	R	Interrupt from SDIO card; SDIO interrupt for card enabled only if corresponding sdio_int_mask bit is set in Interrupt mask register (mask bit 1enables interrupt; 0 masks interrupt). 0 = No SDIO interrupt from card 1 = SDIO interrupt from card.	1'b0
ebeint	[15]	R	End bit error (read), Write no CRC (write) interrupt.	1'b0
acdint	[14]	R	Auto command done interrupt.	1'b0
sbeint	[13]	R	Start bit error interrupt(SBE), Busy Complete Interrupt (BCI)	1'b0
hleint	[12]	R	Hardware locked write error interrupt	1'b0
frunint	[11]	R	FIFO under run/overrun error interrupt	1'b0
htoint	[10]	R	Data starvation by host timeout interrupt (HTO), Volt_switch_int	1'b0
drtoint	[9]	R	Data read timeout interrupt	1'b0
rtoint	[8]	R	Response timeout interrupt	1'b0
dcrcint	[7]	R	Data CRC error interrupt	1'b0
rcrcint	[6]	R	Response CRC error interrupt	1'b0
rxdrint	[5]	R	Receive FIFO data request interrupt	1'b0
txdrint	[4]	R	Transmit FIFO data request interrupt	1'b0
dtoint	[3]	R	Data transfer over interrupt	1'b0
cdint	[2]	R	Command done interrupt	1'b0
reint	[1]	R	Response error interrupt	1'b0
CDINT	[0]	R	Card detect	1'b0

17.3.1.18 RINTSTS

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 44h, + 44h, + 44h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
sdio_interrupt	[16]	RW	SDIO interrupt from card	1'b0
ebe	[15]	RW	End bit error (read), Write no CRC (write) interrupt.	1'b0
acd	[14]	RW	Auto command done interrupt.	1'b0
sbe	[13]	RW	Start bit error interrupt(SBE), Busy Complete Interrupt (BCI)	1'b0
hle	[12]	RW	Hardware locked write error interrupt	1'b0
frun	[11]	RW	FIFO under run/overrun error interrupt	1'b0
hto	[10]	RW	Data starvation by host timeout interrupt (HTO), Volt_switch_int	1'b0
drto	[9]	RW	Data read timeout interrupt	1'b0
rto	[8]	RW	Response timeout interrupt	1'b0
dcrc	[7]	RW	Data CRC error interrupt	1'b0
rcrc	[6]	RW	Response CRC error interrupt	1'b0
rxdr	[5]	RW	Receive FIFO data request interrupt	1'b0
txdr	[4]	RW	Transmit FIFO data request interrupt	1'b0
dto	[3]	RW	Data transfer over interrupt	1'b0
cd	[2]	RW	Command done interrupt	1'b0
re	[1]	RW	Response error interrupt	1'b0
CDINT	[0]	R	Card detect	1'b0

17.3.1.19 STATUS

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 48h, + 48h, + 48h, Reset Value = 0x0000_0006

Name	Bit	Type	Description	Reset Value
DMA_REQ	[31]	R	DMA request signal state	1'b0
dma_ack	[30]	R	DMA acknowledge signal state	1'b0
fifocount	[29:17]	R	Number of filled locations in FIFO	13'b0
response_index	[16:11]	R	Index of previous response, including any auto-stop sent by core	6'b0
data_state_mc_busy	[10]	R	Data transmit or receive state-machine is busy	1'b0
data_busy	[9]	R	Selected card data busy 0 = Card data not busy 1 = Card data busy	1'bx
data_3_status	[8]	R	Checks whether card is present 0 = Card not present 1 = Card present	1'bx
command fsm states	[7:4]	R	Command FSM states. 0 = Idle 1 = Send init sequence 2 = Tx cmd start bit 3 = Tx cmd tx bit 4 = Tx cmd index + arg 5 = Tx cmd crc7 6 = Tx cmd end bit 7 = Rx resp start bit 8 = Rx resp IRQ response 9 = Rx resp tx bit 10 = Rx resp cmd idx 11 = Rx resp data 12 = Rx resp crc7 13 = Rx resp end bit 14 = Cmd path with NCC 15 = Wait NOTE: The command FSM state is represented using 19 bits. The STATUS Register (7:4) has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the STATUS (7:4) register. The three states that are not represented in the STATUS Register(7:4) are:	4'b0

Name	Bit	Type	Description	Reset Value
			Bit[16] - Wait for CCS Bit[17] - Send CCSD Bit[18] - Boot Mode Due to this, while command FSM is in "Wait for CCS state" or` `Send CCSD" or "Boot Mode", the Status register indicates status as 0 for the bit field 7:4.	
fifo_full	[3]	R	FIFO is full	1'b0
fifo_empty	[2]	R	FIFO is empty	1'b1
fifo_tx_watermark	[1]	R	FIFO reached transmit watermark level. Not qualified with data transfer.	1'b1
fifo_rx_watermark	[0]	R	FIFO reached receives watermark level. Not qualified with data transfer.	1'b0

17.3.1.20 FIFOTH

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 4Ch, + 4Ch, + 4Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	1'b0
dma_multiple_transaction_size	[30:28]	RW	Burst size of multiple transaction; should be programmed same as DW-DMA controller multiple-transaction-size SRC/DEST_MSIZE. 000 = 1 transfers 001 = 4 010 = 8 011 = 16 100 = 32 101 = 64 110 = 128 111 = 256 The units for transfers is the H_DATA_WIDTH parameter. A single transfer (dw_dma_single assertion in case of Non DW DMA interface) would be signaled based on this value. Value should be sub-multiple of (RX_WMark + 1)*(F_DATA_WIDTH/H_DATA_WIDTH) and (FIFO_DEPTH - TX_WMark)* (F_DATA_WIDTH/H_DATA_WIDTH) For example, if FIFO_DEPTH = 16, FDATA_WIDTH == H_DATA_WIDTH Allowed combinations for MSize and TX_WMark are: MSize = 1, TX_WMARK = 1-15 MSize = 4, TX_WMark = 8 MSize = 4, TX_WMark = 4 MSize = 4, TX_WMark = 12 MSize = 8, TX_WMark = 8 MSize = 8, TX_WMark = 4 Allowed combinations for MSize and RX_WMark are: MSize = 1, RX_WMARK = 0-14 MSize = 4, RX_WMark = 3 MSize = 4, RX_WMark = 7 MSize = 4, RX_WMark = 11 MSize = 8, RX_WMark = 7 Recommended: MSize = 8, TX_WMark = 8, RX_WMark = 7	3'b0
rx_wmark	[27:16]	RW	FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this	12'b0

Name	Bit	Type	Description	Reset Value
			number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits - 1-bit less than FIFO-count of status register, which is 13 bits. Limitation: RX_WMark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than(FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.	
RSVD	[15:12]	–	Reserved	4'b0
tx_wmark	[11:0]	RW	FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits - 1-bit less than FIFO-count of status register, which is 13 bits. Limitation: TX_WMark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)	12'b0

17.3.1.21 CDETECT

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 50h, + 50h, + 50h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	32'b0
card_detect_n	[0]	R	Value on card_detect_n input ports.	32'b0

17.3.1.22 WRTPRT

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 54h, + 54h, + 54h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	32'b0
write_protect	[0]	R	Value on card_write_prt input ports	32'b0

17.3.1.23 TCBCNT

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 5Ch, + 5Ch, + 5Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
trans_card_byte_count	[31:0]	R	Number of bytes transferred by CIU unit to card.	32'b0

17.3.1.24 TBBCNT

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 60h, + 60h, + 60h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
trans_fifo_byte_count	[31:0]	R	Number of bytes transferred between host/DMA memory and BIU FIFO	32'b0

17.3.1.25 DEBNCE

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 64h, + 64h, + 64h, Reset Value = 0x00FF_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	8'b0
debounce_count	[23:0]	RW	Number of host clocks (clk) used by de-bounce filter logic; typical de-bounce time is 5-25ms.	24'hFFFFFF

17.3.1.26 USRID

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 68h, + 68h, + 68h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
USRID	[31:0]	RW	User identification register; value set by user	32'b0

17.3.1.27 VERID

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 6Ch, + 6Ch, + 6Ch, Reset Value = 0x5342_240A

Name	Bit	Type	Description	Reset Value
verid	[31:0]	RW	Version identification register	32'h5342240a

17.3.1.28 UHS_REG

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 74h, + 74h, + 74h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
ddr_reg	[16]	RW	DDR mode. Determines the voltage fed to the buffers by an external voltage regulator. 0 = Non-DDR mode 1 = DDR mode	1'b0
RSVD	[15:1]	–	Reserved	15'b0
volt_reg	[0]	RW	High Voltage mode. Determines the voltage fed to the buffers by an external voltage regulator. 0 = Buffers supplied with 3.3 V VDD 1 = Buffers supplied with 1.8 V VDD	1'b0

17.3.1.29 RST_n

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 78h, + 78h, + 78h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	31'b0
card_reset	[0]	RW	Hardware reset. 0 = Reset 1 = Active mode These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.	1'b0

17.3.1.30 BMODE

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 80h, + 80h, + 80h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	21'b0
pbl	[10:8]	RW	Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows. 000 = 1 transfers 001 = 4 transfers 010 = 8 transfers 011 = 16 transfers 100 = 32 transfers 101 = 64 transfers 110 = 128 transfers 111 = 256 transfers Transfer unit is either 16, 32, or 64 bits, based on HDATA_WIDTH. PBL is a read-only value and is applicable only for Data Access; it does not apply to descriptor accesses.	3'b0
DE	[7]	RW	IDMAC Enable. When set, the IDMAC is enabled.DE is read/write.	1'b0
DSL	[6:2]	RW	Descriptor Skip Length. Specifies the number of HWord/Word/Dword (depending on 16/32/64-bit bus) to skip between two unchained descriptors. This is applicable only for dual buffer structure. DSL is read/write.	5'b0
fb	[1]	RW	Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 orINCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations. FB is read/write.	1'b0
swr	[0]	RW	Software Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.	1'b0

17.3.1.31 PLDMND

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 84h, + 84h, + 84h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
pd	[31:0]	W	Poll Demand. If the OWN bit of a descriptor is not set, the FSM goes to the Suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation. This is a write only register. PD bit is write-only.	32'b0

17.3.1.32 DBADDR

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 88h, + 88h, + 88h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
sdl	[31:0]	RW	Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [0/1/2:0] for 16/32/64-bit bus-width) are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.	32'b0

17.3.1.33 IDSTS

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 8Ch, + 8Ch, + 8Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	15'b0
fsm	[16:13]	R	DMAC FSM present state. 0 = DMA_IDLE 1 = DMA_SUSPEND 2 = DESC_RD 3 = DESC_CHK 4 = DMA_RD_REQ_WAIT 5 = DMA_WR_REQ_WAIT 6 = DMA_RD 7 = DMA_WR 8 = DESC_CLOSE This bit is read-only.	4'b0
eb	[12:10]	R	Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 3'b001 = Host Abort received during transmission 3'b010 = Host Abort received during reception Others = Reserved EB is read-only.	3'b0
ais	[9]	RW	Abnormal Interrupt Summary. Logical OR of the following: • IDSTS[2] - Fatal Bus Interrupt • IDSTS[4] - DU bit Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.	1'b0
NIS	[8]	RW	Normal Interrupt Summary. Logical OR of the following: • IDSTS[0] - Transmit Interrupt • IDSTS[1] - Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.	1'b0
RSVD	[7:6]	–	Reserved	2'b0
ces	[5]	RW	Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits:	1'b0

Name	Bit	Type	Description	Reset Value
			• EBE - End Bit Error • RTO - Response Timeout/Boot ACK Timeout • RCRC - Response CRC • SBE - Start Bit Error • DRTO - Data Read Timeout/BDS timeout • DCRC - Data CRC for Receive • RE - Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a “response error”; however, it will not abort if the CES bit is cleared.	
DU	[4]	RW	Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.	1'b0
RSVD	[3]	–	Reserved	1'b0
fbe	[2]	RW	Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.	1'b0
ri	[1]	RW	Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a1 clears this bit.	1'b0
ti	[0]	RW	Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a "1" clears this bit.	1'b0

17.3.1.34 IDINTEN

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 90h, + 90h, + 90h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	–	Reserved	22'b0
ai	[9]	RW	Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: • IDINTEN[2] : Fatal Bus Error Interrupt • IDINTEN[4] : DU Interrupt	1'b0
NI	[8]	RW	Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: • IDINTEN[0] : Transmit Interrupt • IDINTEN[1] : Receive Interrupt	1'b0
RSVD	[7:6]	–	Reserved	2'b0
ces	[5]	RW	Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.	1'b0
du	[4]	RW	Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled.	1'b0
RSVD	[3]	–	Reserved	1'b0
fbe	[2]	RW	Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.	1'b0
Ri	[1]	RW	Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.	1'b0
Ti	[0]	RW	Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.	1'b0

17.3.1.35 DSCADDR

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 94h, + 94h, + 94h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HDA	[31:0]	R	Host Descriptor Address Pointer. Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC.	32'b0

17.3.1.36 BUFADDR

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 98h, + 98h, + 98h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HBA	[31:0]	R	Host Buffer Address Pointer. Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC.	32'b0

17.3.1.37 CARDTHRCTL

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 100h, + 100h, + 100h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	–	Reserved	5'b0
card_rd_threshold	[26:16]	RW	Card Read Threshold size; N depends on the FIFO size.	11'b0
RSVD	[15:2]	–	Reserved	14'b0
bsy_clr_inten	[1]	RW	Busy Clear Interrupt generation: 0 = Busy Clear Interrupt disabled 1 = Busy Clear Interrupt enabled NOTE: The application can disable this feature if it does not want to wait for a Busy Clear Interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.	1'b0
card_rd_thren	[0]	RW	Card Read Threshold Enable 1'b0 = Card Read Threshold disabled 1'b1 = Card Read Threshold enabled. Host Controller initiates Read Transfer only if Card Rd Threshold amount of space is available in receives FIFO.	1'b0

17.3.1.38 BACK_END_POWER

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 104h, + 104h, + 104h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	31'b0
back_end_power	[0]	RW	Back end power 1'b0 = Off; Reset 1'b1 = Back-end Power supplied to card application; one pin per card	1'b0

17.3.1.39 EMMC_DDR_REG

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 10Ch, + 10Ch, + 10Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	31'b0
half_start_bit	[0]	RW	Control for start bit detection mechanism inside DWC_mobile_storage based on duration of start bit; each bit refers to one slot. For eMMC 4.5, start bit can be: • Full cycle (HALF_START_BIT = 0) • Less than one full cycle (HALF_START_BIT = 1) Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.	1'b0

17.3.1.40 EMMC_DDR_REG

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 114h, + 114h, + 114h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	6'b0
phase_shift_sample	[25:24]	RW	Sample clock phase shift 0 = 0 1 = 90	2'b0

Name	Bit	Type	Description	Reset Value
			2 = 180 3 = 270	
RSVD	[23:18]	–	Reserved	6'b0
phase_shift_drive	[17:16]	RW	Drive clock phase shift 0 = 0 1 = 90 2 = 180 3 = 270	2'b0
DELAY_sample	[15:8]	RW	Sample clock delay	8'b0
delay_drive	[7:0]	RW	Drive clock delay	8'b0

17.3.1.41 Data

- Base Address: C006_2000h (SD0)
- Base Address: C006_8000h (SD1)
- Base Address: C006_9000h (SD2)
- Address = Base Address + 114h, + 114h, + 114h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
data	[31:0]	RW	Data write to or read from FIFO	32'bx

18 Pulse Period Measurement (PPM)

18.1 Overview

The Pulse Period Measurement (PPM) measures the period of the high level and the low level of a 1-bit Signal entered from the outside.

18.1.1 Features

The PPM provides:

- 16-bit Pulse Period Measurement Counter
- Overflow Check
- Control Input Polarity
- PPM Clock generator

18.1.2 Block Diagram

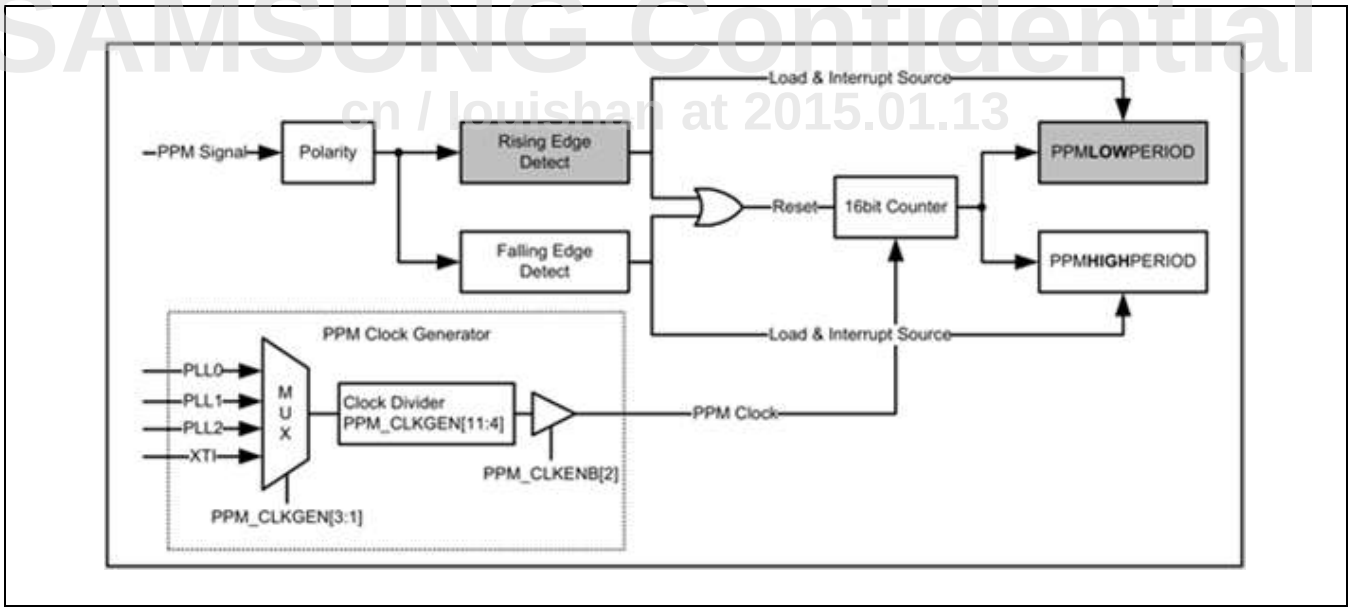


Figure 18-1 PPM Block Diagram

- PPMLOWPERIOD: PPM Low Period Register: If PPM Signal is changed from Low to High (rising edge detect), the count value of 16-bit Counter is stored at PPMLOWPERIOD Register and 16-bit Counter is reset.
- PPMHIGHPERIOD: PPM High Period Register: If PPM Signal is changed from High to Low (falling edge detect), the count value of 16-bit Counter is stored at PPMHIGHPERIOD Register and 16-bit Counter is reset.
- If the high or low period is too long to be measured by the 16-bit Counter, Overflow interrupt occurs.

18.2 Functional Description

When a PPM signal rising edge or a falling edge is detected, the 16-bit counter is reset after storing the 16-bit counter value to the PPMLOWPERIOD register or the PPMHIGHPERIOD register. If a falling edge is detected, the counter value is stored at the PPMHIGHPERIOD register and then the counter is reset. If a rising edge is detected, the counter value is stored at the PPMLOWPERIOD register and then the counter is reset. If the high or the low period is too long to be measured by the 16-bit Counter, an Overflow interrupt occurs. Therefore the IP-Remo on input signal should be checked and an appreciate PPL clock value should be specified to prevent the occurrence of Overflow interrupts.

18.2.1 IR Remote Protocol Example

Figure 18-2 shows a representative waveform of an IP Remote signal being passed IR-Receiver Module.

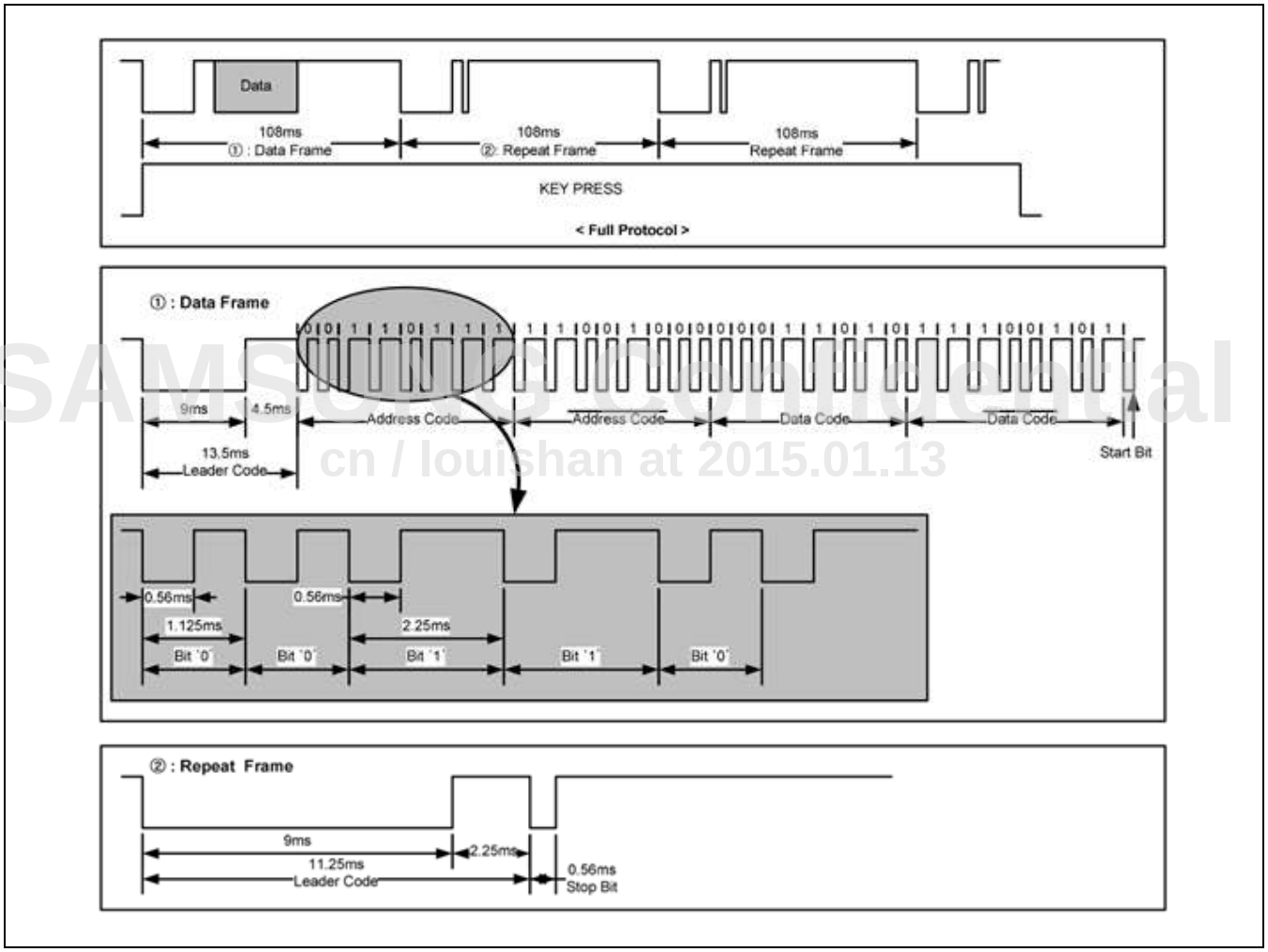


Figure 18-2 IR Remote Example Protocol

The PPM clock between 850 kHz and 6.75 MHz is suitable to prevent the occurrence of an Overflow interrupt.

The PPM clock can be selected in the range of 843,750 Hz to 13,500,000 Hz via the Clock Divider setting. (1 to 31)

18.2.2 Timing

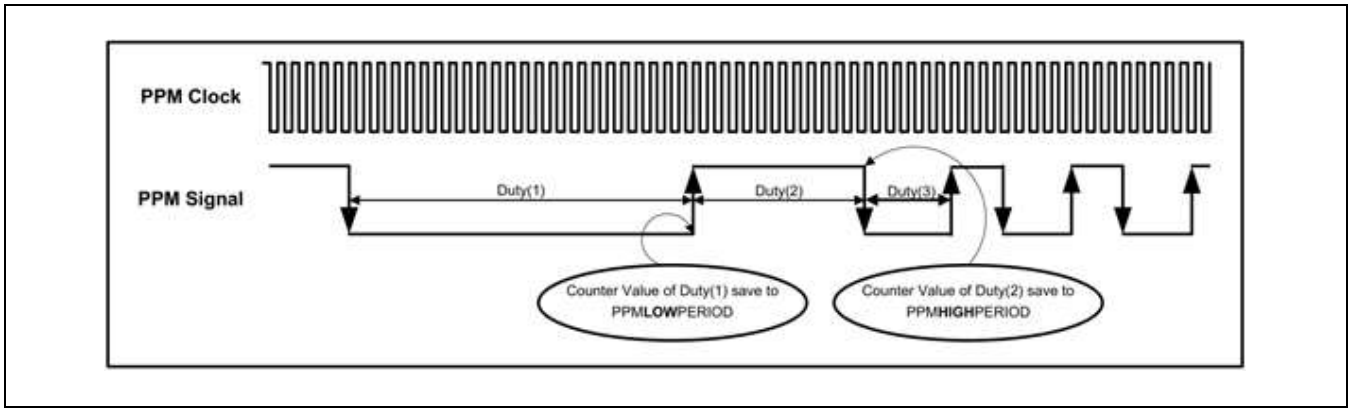


Figure 18-3 PPM Timing

18.2.3 Flowchart

Figure 18-4 shows an example of a flowchart for checking IR-Remote signals.

Initialization Procedure for PPM:

1. Set GPIO
2. Clock Source Select (XTI)
3. Clock Divider (1 to 31)
4. Set Polarity
5. Set Interrupt mode (Falling Edge, Rising Edge and Overflow)
6. Initialize the PPM Status Register.
7. Enable Interrupt

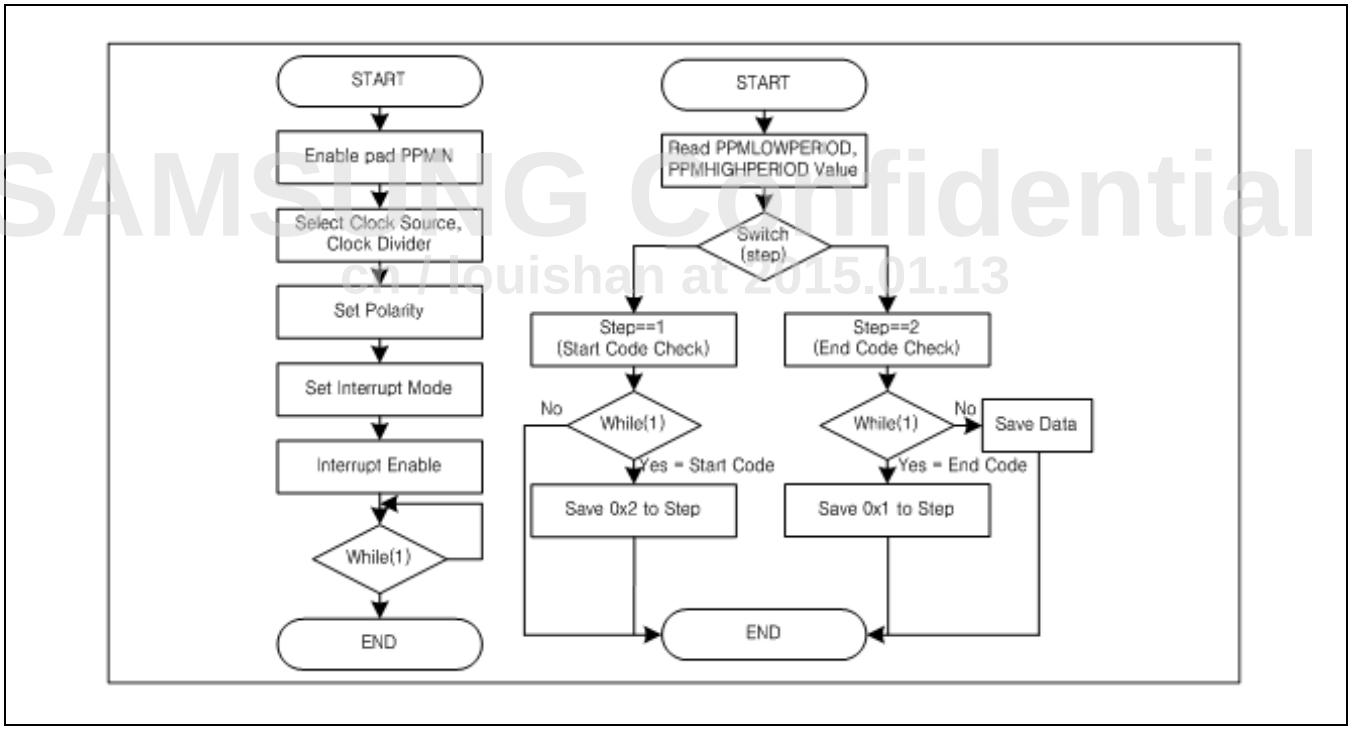


Figure 18-4 IR Remote Receiver Flowchart

18.3 Register Description

18.3.1 Register Map Summary

- Base Address: C005_4000h

Register	Offset	Description	Reset Value
PPMCTRL	00h	PPM control register	0x0000_4000
PPMSTATUS	04h	PPM status register	0x0000_0000
PPMLOWPERIOD	06h	PPM low period register	0x0000_0000
PPMHIGHPERIOD	08h	PPM high period register	0x0000_0000

18.3.1.1 PPMCTRL

- Base Address: C005_4000h
- Address = Base Address + 00h, Reset Value = 0x0000_4000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
PPMENB	[15]	RW	PPM Module Enable 0 = Disable 1 = Enable	1'b0
PPMINPOL	[14]	RW	Control Polarity of PPM Input Signal 0 = Invert 1 = Bypass	1'b1
RSVD	[31:16]	–	Reserved	–
PPMIRQO	[2]	RW	Overflow Interrupt Enable 0 = Disable 1 = Enable	1'b0
PPMIRQF	[1]	RW	Falling Edge Detect Interrupt Enable 0 = Disable 1 = Enable	1'b0
PPMIRQR	[0]	RW	Rising Edge Detect Interrupt Enable 0 = Disable 1 = Enable	1'b0

18.3.1.2 PPMSTATUS

- Base Address: C005_4000h
- Address = Base Address + 04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVSD	[31:5]	–	Reserved	–
PPMOVERLOW	[4]	R	Indicate Overflow in Low 0 = Normal 1 = Overflow	1'b0
PPMOVERHIGH	[3]	R	Indicate Overflow in High 0 = Normal 1 = Overflow	1'b0
PPMPENDO	[2]	RW	Overflow Interrupt Pending Bit. Set to 1 to clear this bit 0 = None 1 = Detected	1'b0
PPMPENDF	[1]	RW	Falling Edge Detect Interrupt Pending Bit. Set to 1 to clear this bit 0 = None 1 = Detected	1'b0
PPMPENDR	[0]	RW	Rising Edge Detect Interrupt Pending Bit. Set to 1 to clear this bit 0 = None 1 = Detected	1'b0

18.3.1.3 PPMLOWPERIOD

- Base Address: C005_4000h
- Address = Base Address + 06h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVSD	[31:16]	–	Reserved	–
PPMLOWPERIOD	[15:0]	R	Read Counter Value of Low	16'h0

18.3.1.4 PPMHIGHPERIOD

- Base Address: C005_4000h
- Address = Base Address + 08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVSD	[31:16]	–	Reserved	–
PPMHIGHPERIOD	[15:0]	R	Read Counter Value of High	16'h0

19 Pulse Width Modulation (PWM) Timer

19.1 Overview

These timers can be used to generate internal interrupts to the ARM subsystem. In addition, Timers 0, 1, 2, and 3 include a PWM function (Pulse Width Modulation) which can drive an external I/O signal. The PWM for timer 0 has a optional dead-zone generator capability, which can be utilized to support a large current device. Timer 4 is only an internal timer with no output pins.

The Timers are normally clocked off of a divided version of the APB-PCLK. Timers 0 and 1 share a programmable 8-bit prescaler that provides the first level of division for the PCLK. Timer 2, 3, and 4 share a different 8-bit prescaler. Each timer has its own, private clock-divider that provides a second level of clock division (prescaler divided by 2, 4, 8, or 16). Alternatively, the Timers can also select a clock source from an external pin, except Timer 4. Timers 0 and 1 can select the external clock TCLK0. Timers 2 and 3 can select the external clock TCLK1. Timer 4 operates with APB-PCLK only.

Each timer has its own 32-bit down-counter which is driven by the timer clock. The down-counter is initially loaded from the Timer Count Buffer register (TCNTBn). When the down-counter reaches zero, the timer interrupt request is generated to inform the CPU that the timer operation is completed. When the timer down-counter reaches zero, the value of corresponding TCNTBn can be automatically reloaded into the down-counter to start the next cycle. However, if the timer stops, for example, by clearing the timer enable bit of TCONn during the timer running mode, the value of TCNTBn will not be reloaded into the counter.

The Pulse Width Modulation function (PWM) uses the value of the TCMPBn register. The timer control logic changes the output level when the down-counter value matches the value of the compare register in the timer control logic. Therefore, the compare register determines the turn-on time (or turn-off time) of a PWM output.

The TCNTBn and TCMPBn registers are double buffered to allow the timer parameters to be updated in the middle of a cycle. The new values will not take effect until the current timer cycle completes.

A simple example of a PWM cycle is shown in the figure below.

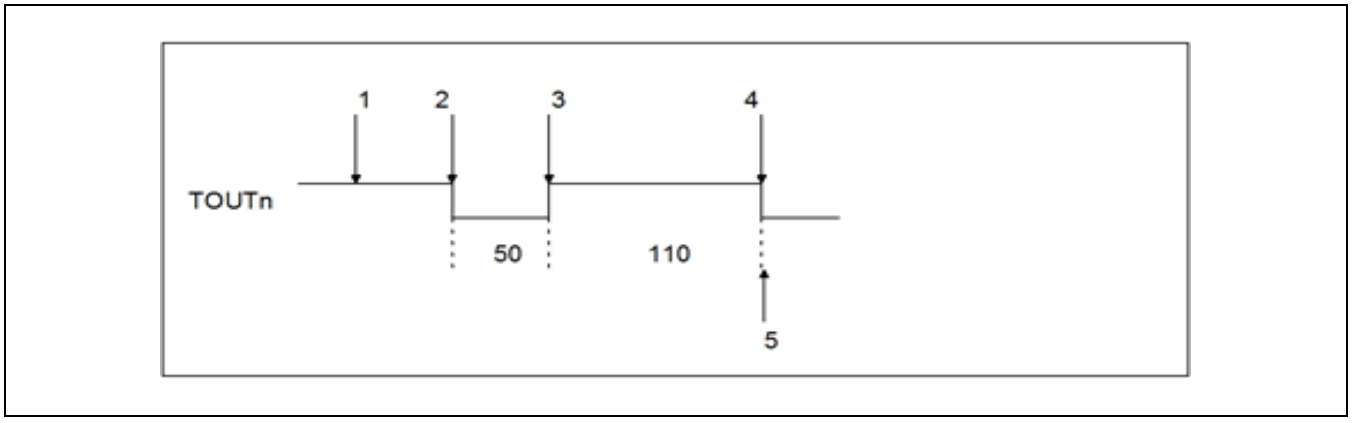


Figure 19-1 Simple Example of PWM Cycle

1. Initialize the TCNTBn with 160 (50+110) and the TCMPBn with 110.
2. Start Timer by setting the start bit and manual update bit off. The TCNTBn value of 160 is loaded into the down counter, the output is driven low.
3. When down counter counts down to the value in the TCMPBn register (110), the output is changed from low to high
4. When the down counter reaches 0, the interrupt request is generated.
5. At the same time the down counter is automatically reloaded with TCNTBn, which restarts the cycle.

19.2 Features

- The Features supported by the PWM are:
  - Five 32-bit Timers.
  - Two 8-bit Clock Prescalers providing first level of division for the PCLK, Five Clock Dividers and Multiplexers providing second level of division for the Prescaler clock and Two External Clocks.
  - Programmable Clock Select Logic for individual PWM Channels.
  - Four Independent PWM Channels with Programmable Duty Control and Polarity.
  - Static Configuration: PWM is stopped.
  - Dynamic Configuration: PWM is running.
  - Supports Auto-Reload Mode and One-Shot Pulse Mode.
  - Supports for two external inputs to start PWM.
  - Dead Zone Generator on two PWM Outputs.
  - Supports DMA Transfers.
  - Optional Pulse or Level Interrupt Generation.

- The PWM has two operation modes:
  - Auto-Reload Mode:
  - Continuous PWM pulses are generated based on programmed duty cycle and polarity.
  - One-Shot Pulse Mode:
  - Only one PWM pulse is generated based on programmed duty cycle and polarity.
  - To control the functionality of PWM, 18 special function registers are provided. The PWM is a programmable output, dual clock input AMBA slave module and connects to the Advanced Peripheral Bus (APB). The 18 special function registers within PWM are accessed via APB transactions.

19.3 Block Diagram

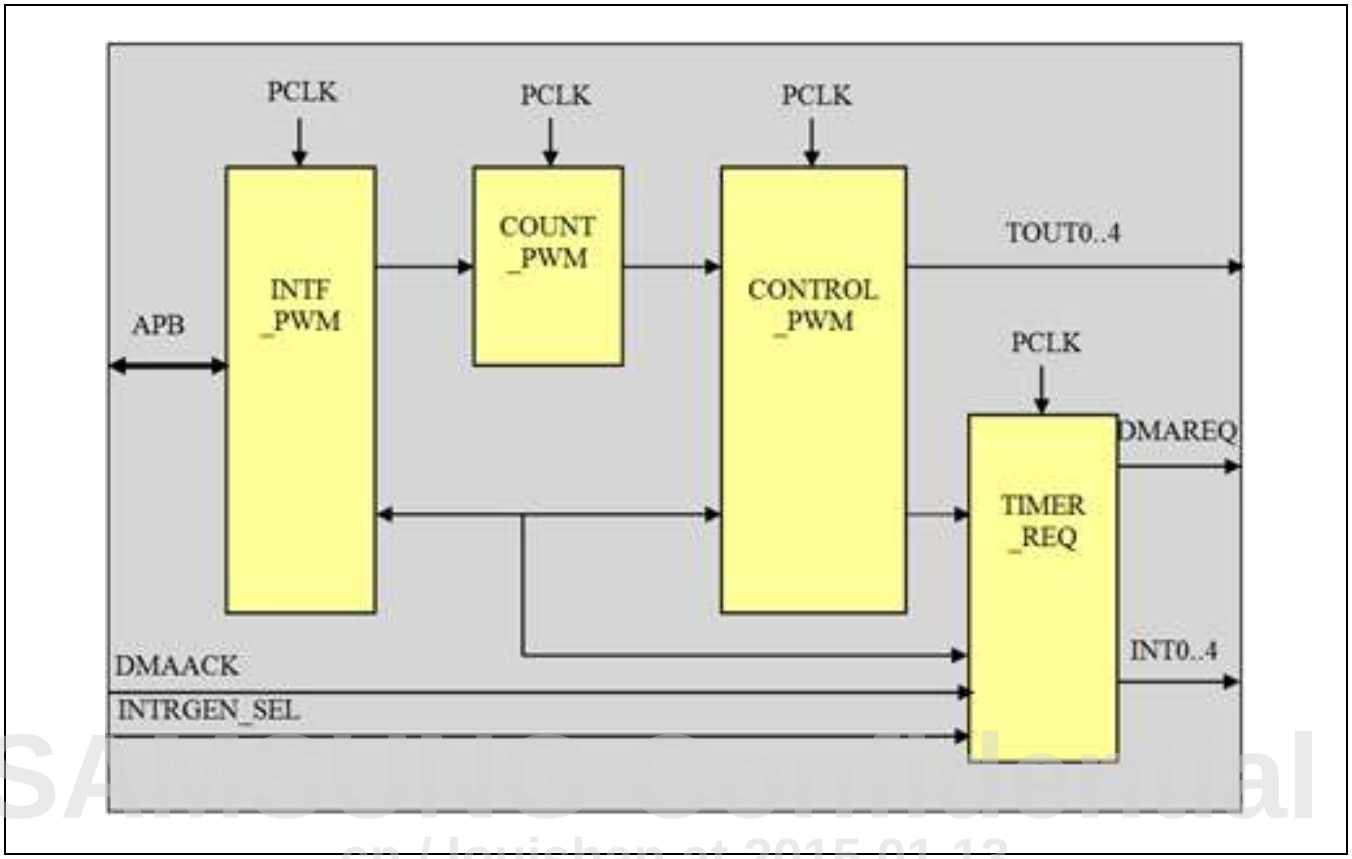


Figure 19-2 PWMTIMER Block Diagram

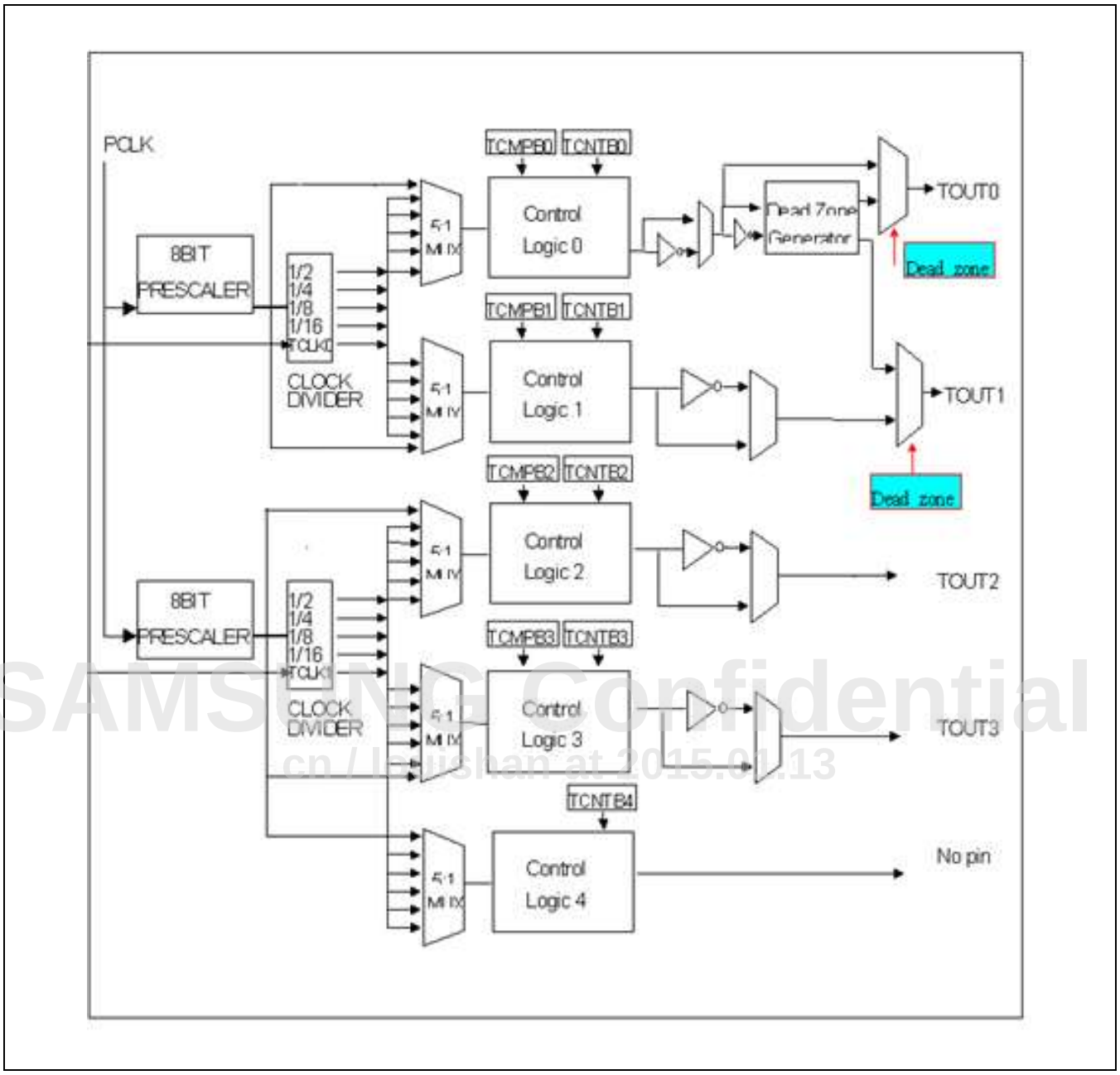


Figure 19-3 PWMTIMER Clock Tree Diagram

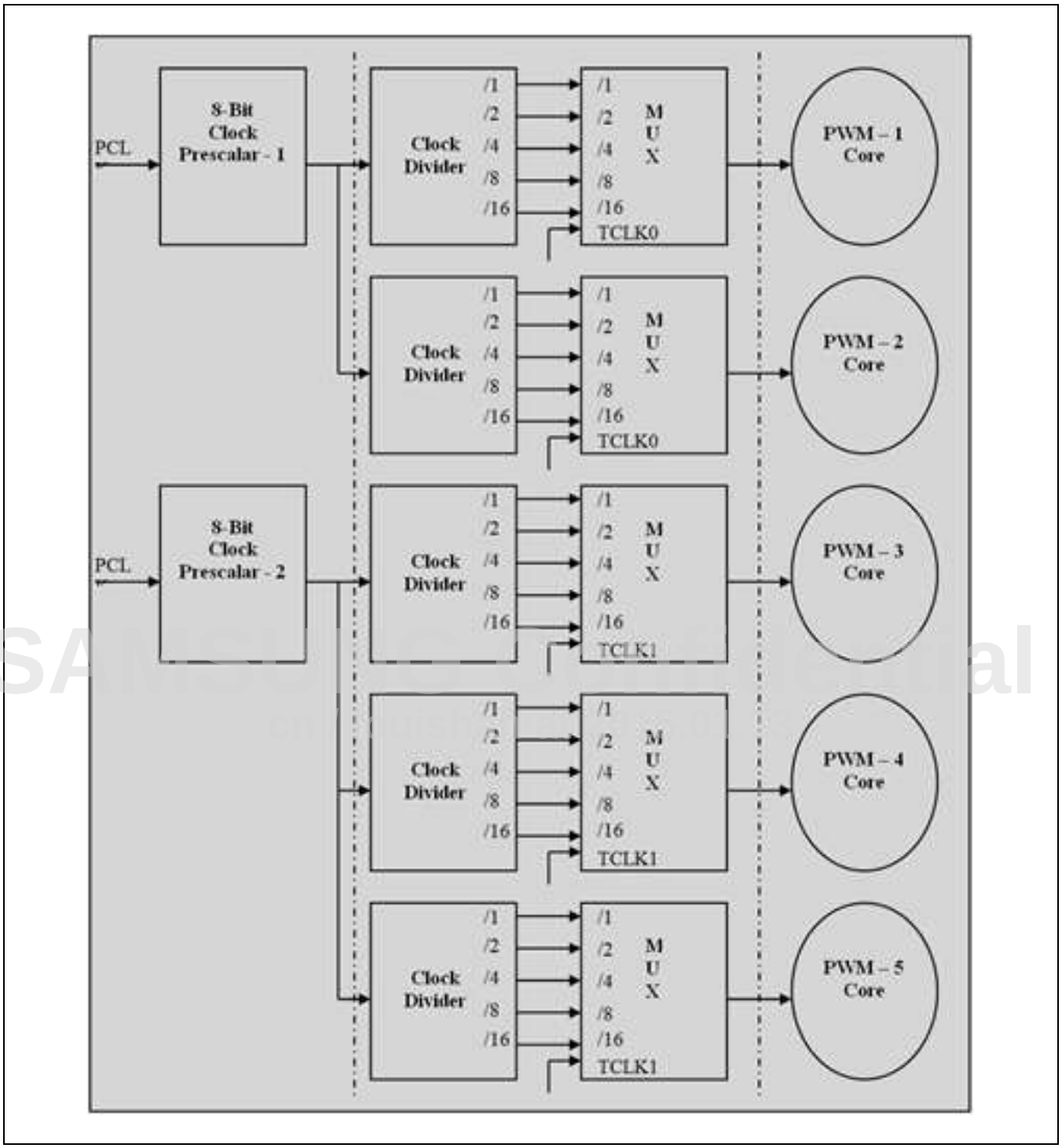


Figure 19-4 PWMTIMER Detailed Clock Tree Diagram

19.4 Functional Description

19.4.1 Prescaler & Divider

8-bit prescaler and 3-bit divider make the following output frequencies:

Table 19-1 Min. and Max. Resolution based on Prescaler and Clock Divider Values

4-bit Divider Settings	Minimum Resolution (prescaler=0)	Maximum Resolution (prescaler=255)	Maximum Interval (TCNTBn=65535)
1/1 (PCLK=66 MHz)	0.015 us (66.0 MHz)	3.87 us (258 kHz)	0.25s
1/2 (PCLK=66 MHz)	0.030 us (33.0 MHz)	7.75 us (129 kHz)	0.50s
1/4 (PCLK=66 MHz)	0.060 us (16.5 MHz)	15.5 us (64.5 kHz)	1.02s
1/8 (PCLK=66 MHz)	0.121 us (8.25 MHz)	31.0 us (32.2 kHz)	2.03s
1/16 (PCLK=66 MHz)	0.242 us (4.13 MHz)	62.1 us (16.1 kHz)	4.07s

19.4.2 Basic Timer Operation

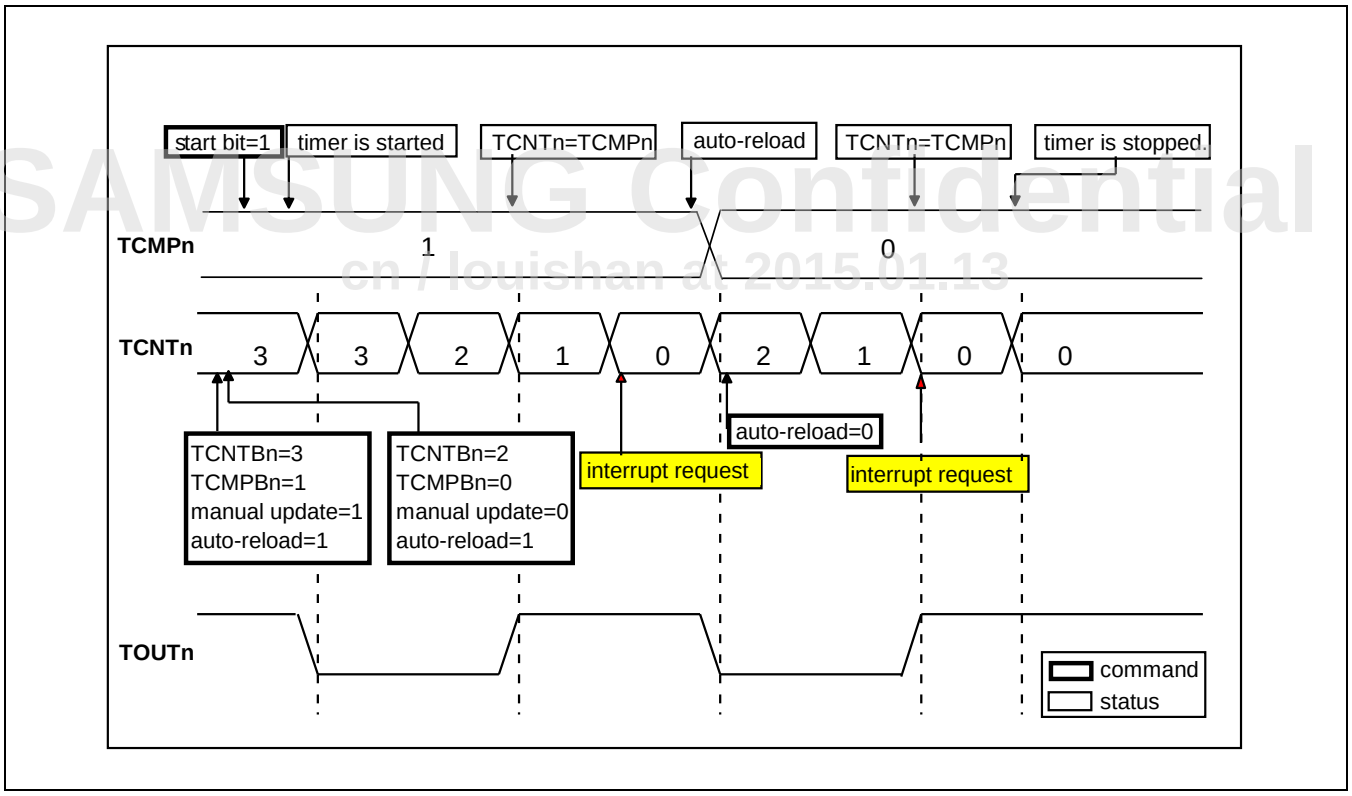


Figure 19-5 Timer Operations

A timer (except the timer channel 5) has TCNTBn, TCNTn, TCMPBn and TCMPn. TCNTBn and TCMPBn are loaded into TCNTn and TCMPn when the timer reaches 0. When TCNTn reaches 0, the interrupt request will occur if the interrupt is enabled. (TCNTn and TCMPn are the names of the internal registers. The TCNTn register can be read from the TCNTOn register)

19.4.3 Auto-Reload and Double Buffering

The Timers have a double buffering feature, which can change the reload value for the next timer operation without stopping the current timer operation. So, although the new timer value is set, a current timer operation is completed successfully.

The timer value can be written into TCNTBn (Timer Count Buffer register) and the current counter value of the timer can be read from TCNTOn (Timer Count Observation register). If TCNTBn is read, the read value is not the current state of the counter but the reload value for the next timer duration.

The auto-reload is the operation, which copies the TCNTBn into TCNTn when TCNTn reaches 0. The value, written into TCNTBn, is loaded to TCNTn only when the TCNTn reaches to 0 and auto-reload is enabled. If the TCNTn is 0 and the auto-reload bit is 0, the TCNTn does not operate any further.

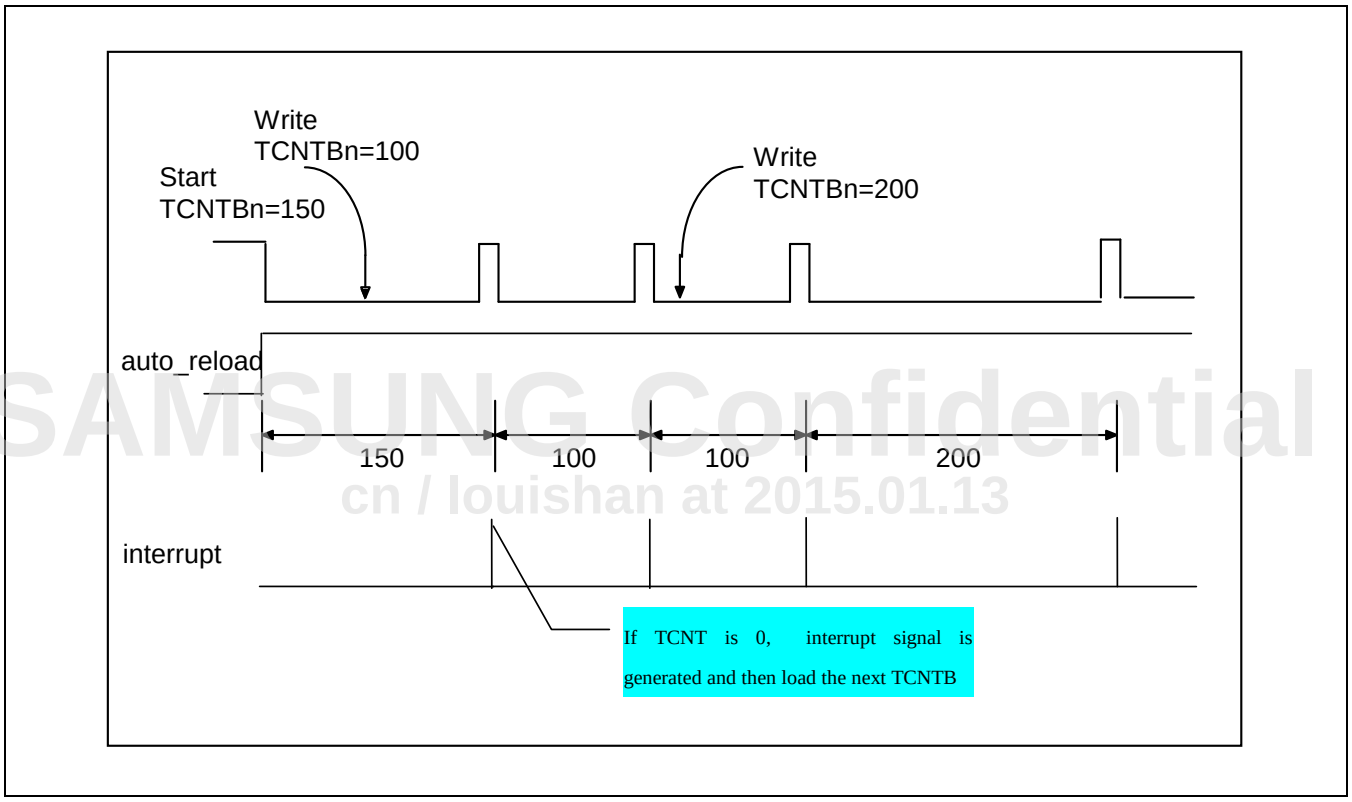


Figure 19-6 Example of Double Buffering Feature

The result of the following procedure is shown in *Figure 19-7*.

1. Enable the auto-reload feature. Set the TCNTBn as 160(50+110) and the TCMPBn as 110. Set the manual update bit and inverter bit(on/off). The manual update bit makes the TCNTn, TCMPn set to the value of TCNTBn, TCMPBn. And then, set TCNTBn, TCMPBn as 80(40+40), 40 to determine the next reload value.
2. Start Timer by setting the start bit and manual updata bit off.
3. When TCNTn has the same value with TCMPn, the logic level of TOUTn is changed from low to high
4. When TCNTn reaches to 0, TCNTn is reloaded automatically with TCNTBn. At the same time, the interrupt request is generated.
5. In the ISR (interrupt service routine), the TCNTBn and TCMPBn is set as 80(20+60) and 60, which is used for next duration.
6. When TCNTn has the same value with TCMPn, the logic level of TOUTn is changed from low to high
7. When TCNTn reaches to 0, TCNTn is reloaded automatically with TCNTBn. At the same time, the interrupt request is generated.
8. In the ISR (interrupt service routine), auto-reload and interrupt request are disabled to stop the timer.
9. When TCNTn has the same value with TCMPn, the logic level of TOUTn is changed from low to high
10. Even when TCNTn reaches to 0, TCNTn is not any more reloaded and the timer is stopped because auto-reload is disabled.
11. No interrupt request is generated.

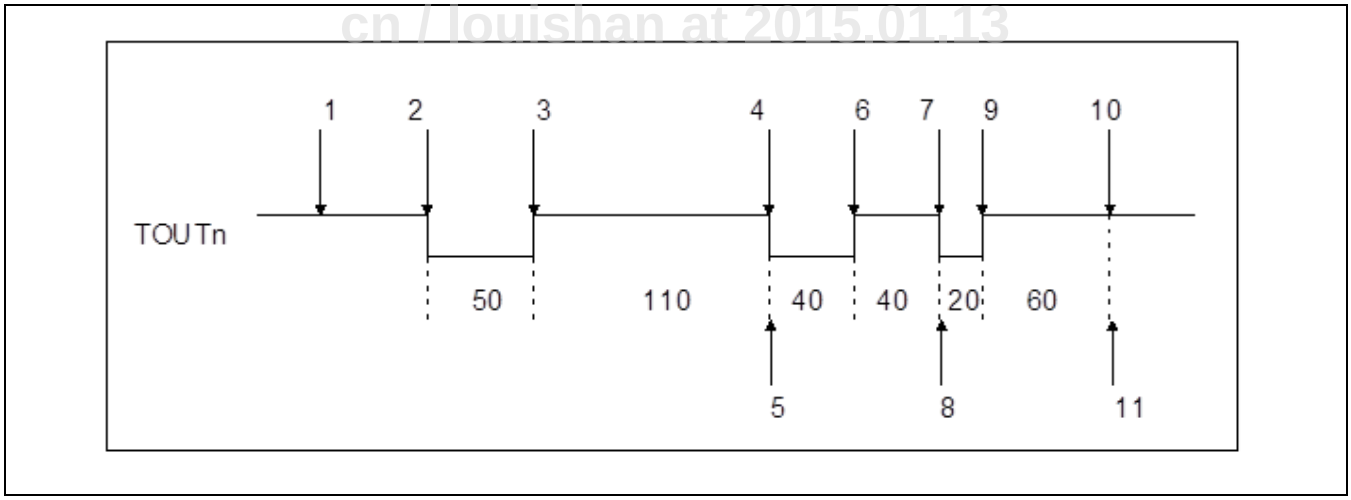


Figure 19-7 Example of Timer Operation

19.4.4 Initialize Timer (Setting Manual-Up Data and Inverter)

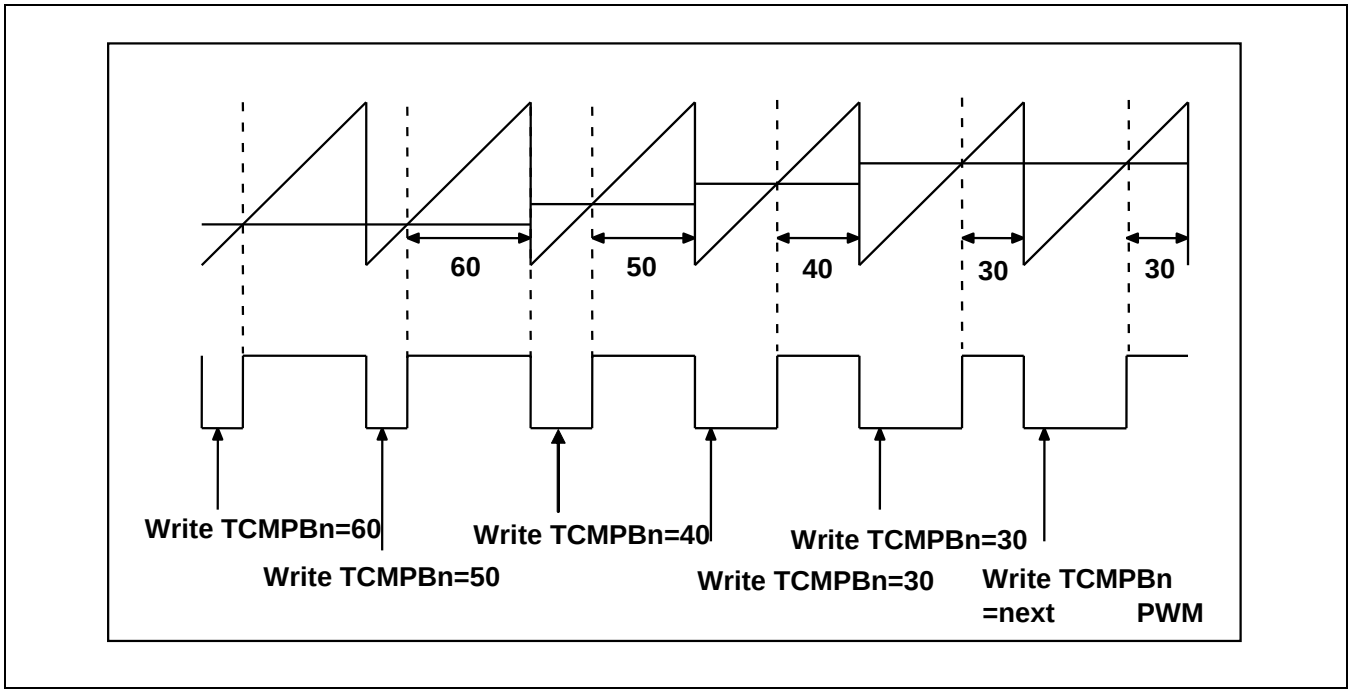


Figure 19-8 Example of PWM

PWM feature can implement by using the TCMPBn. PWM frequency is determined by TCNTBn. A PWM value is determined by TCMPBn in the *Figure 19-8*.

For higher PWM value, decrease TCMPBn value. For lower PWM value, increase TCMPBn value. If output inverter is enabled, the increment/decrement may be opposite.

Because of double buffering feature, TCMPBn, for a next PWM cycle, can be written in any point of current PWM cycle by ISR.

19.4.5 Output Level Control

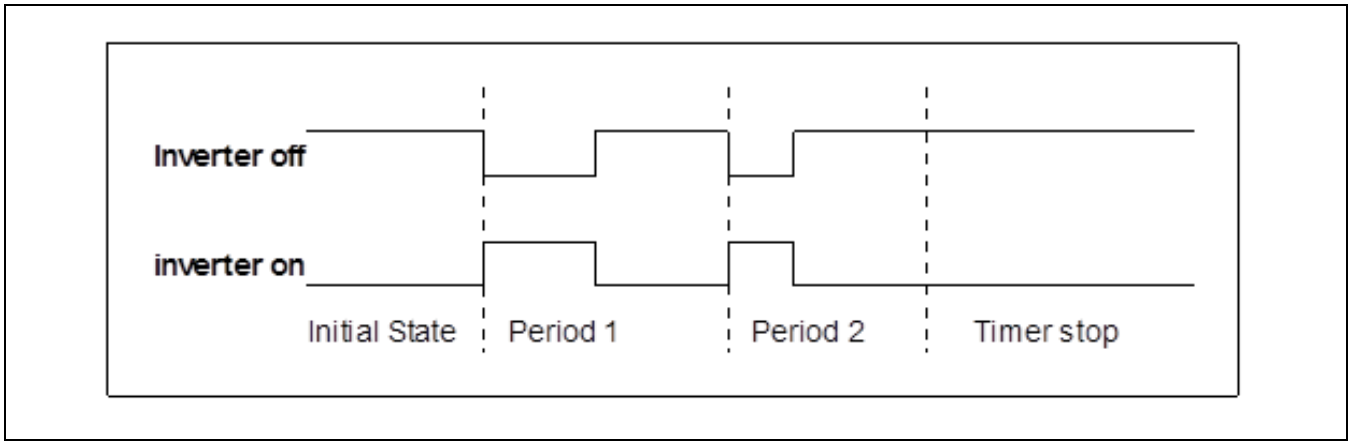


Figure 19-9 Inverter On/Off

The following methods can be used to maintain TOUT as high or low. (Assume the inverter is off)

Turn off the auto-reload bit. And then, TOUTn goes to high level and the timer is stopped after TCNTn reaches to 0. This method is recommended.

Stop the timer by clearing the timer start/stop bit to 0. If TCNTn <= TCMPn, the ouput level is high. If TCNTn >TCMPn, the output level is low

TOUTn can be inverted by the inverter on/off bit in TCON. The inverter removes the additional circuit to adjust the output level.

19.4.6 Dead Zone Generator

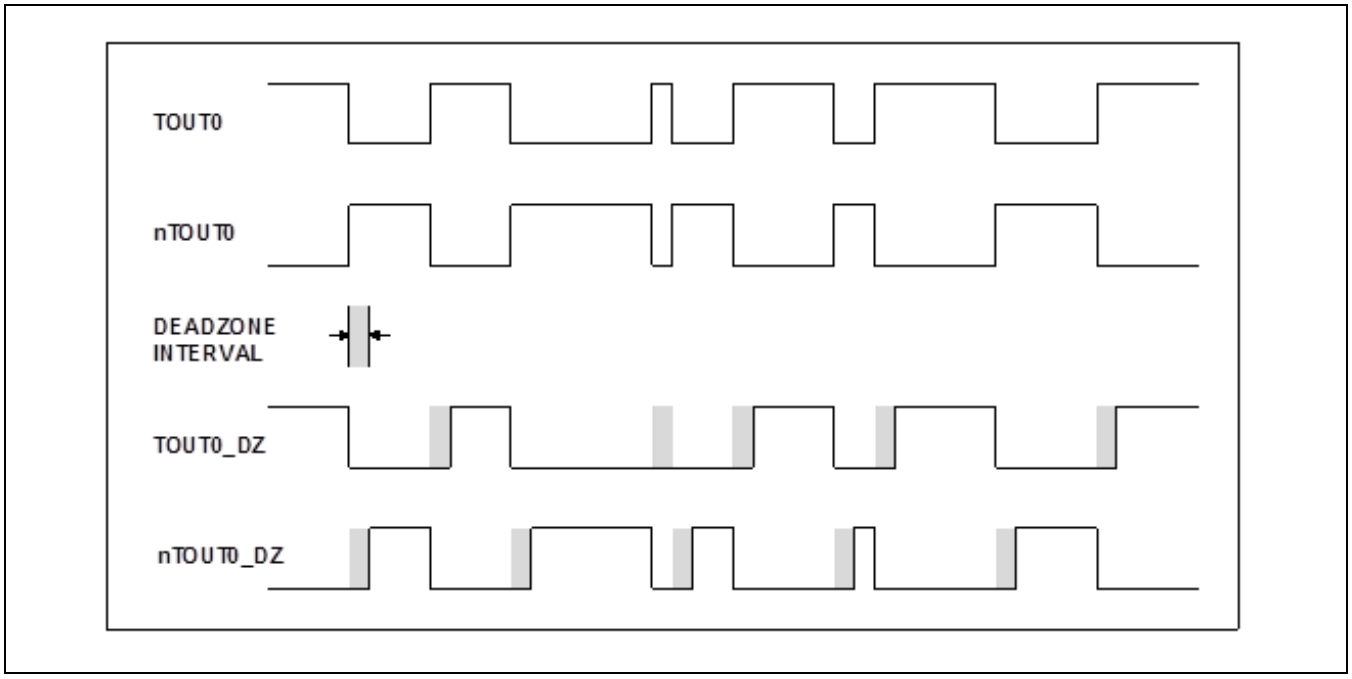


Figure 19-10 The Waveform when a Dead Zone Feature is Enabled

The dead zone is for the PWM control of power devices. This feature is used to insert the time gap between a turn-off of a switching device and a turn on of the other switching device. This time gap prohibit the two switching device turning on simultaneously even for a very short time.

TOUT0 is the PWM output. nTOUT0 is the inversion of the TOUT0. If the dead-zone is enabled, the output wave-form of TOUT0,nTOUT0 will be TOUT0_DZ and nTOUT0_DZ. TOUT0_DZ and nTOUT0_DZ never can be turned on simultaneously by the dead zone interval. For functional correctness, the dead zone length must be set smaller than compare counter value.

19.4.7 Timer Interrupt Generation

The PWMTIMER provides flexibility to generate Pulse and Level Interrupts by controlling the "INTRGEN_SEL" port status. When the port "INTRGEN_SEL" is tied to logic 1, optional level interrupts will be, generated else optional pulse interrupts will be generated. The interrupt generation is controlled by writing specific values to the "TINT_CSTAT" register within PWMTIMER. Also, interrupt generations is optional based on programmed value in "TINT_CSTAT" register.

19.5 Register Description

19.5.1 Register Map Summary

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)

Register	Offset	Description	Reset Value
TCFG0	0x00h 0x00h	Clock-Prescalar and dead-zone configurations	0x0000_0101
TCFG1	0x04h 0x04h	Clock multiplexers and DMA mode select	0x0000_0000
TCON	0x08h 0x08h	Timer control register	0x0000_0000
TCNTB0	0x0Ch 0x0Ch	Timer 0 count buffer register	0x0000_0000
TCMPB0	0x10h 0x10h	Timer 0 compare buffer register	0x0000_0000
TCNTO0	0x14h 0x14h	Timer 0 count observation register	0x0000_0000
TCNTB1	0x18h 0x18h	Timer 1 count buffer register	0x0000_0000
TCMPB1	0x1Ch 0x1Ch	Timer 1 compare buffer register	0x0000_0000
TCNTO1	0x20h 0x20h	Timer 1 count observation register	0x0000_0000
TCNTB2	0x24h 0x24h	Timer 2 count buffer register	0x0000_0000
TCMPB2	0x28h 0x28h	Timer 2 compare buffer register	0x0000_0000
TCNTO2	0x2Ch 0x2Ch	Timer 2 count observation register	0x0000_0000
TCNTB3	0x30h 0x30h	Timer 3 count buffer register	0x0000_0000
TCMPB3	0x34h 0x34h	Timer 3 compare buffer register	0x0000_0000
TCNTO3	0x38h 0x38h	Timer 3 count observation register	0x0000_0000
TCNTB4	0x3Ch 0x3Ch	Timer 4 count buffer register	0x0000_0000
TCNTO4	0x40h 0x40h	Timer 4 count observation register	0x0000_0000
TINT_CSTAT	0x44h 0x44h	Timer interrupt control and status register	0x0000_0000

19.5.1.1 TCFG0

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x00h, 0x00h, Reset Value = 0x0000_0101

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	–
Dead zone length	[23:16]	RW	Dead zone length	8'b0
Prescaler 1	[15:8]	RW	Prescaler 1 value for Timer 2, 3 and 4	8'b1
Prescaler 0	[7:0]	RW	Prescaler 0 value for timer 0 & 1	8'b1

19.5.1.2 TCFG1

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x04h, 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	–
DMA mode	[23:20]	RW	Select DMA Request Channel Select Bit 0000 = No select 0001 = INT0 0010 = INT1 0011 = INT2 0100 = INT3 0101 = INT4 0110 = No select 0111 = No select	4'b0
Divider MUX4	[19:16]	RW	Select Mux input for PWM Timer 4 0000 =1/1 0001 =1/2 0010 =1/4 0011 =1/8 0100 = 1/16 0101 = External TCLK1 0110 = External TCLK1 0111 = External TCLK1	4'b0
Divider MUX3	[15:12]	RW	Select Mux input for PWM Timer 3 0000 =1/1 0001 =1/2 0010 =1/4 0011 =1/8 0100 = 1/16 0101 = External TCLK1 0110 = External TCLK1	4'b0

Name	Bit	Type	Description	Reset Value
			0111 = External TCLK1	
Divider MUX2	[11:8]	RW	Select Mux input for PWM Timer 2 0000 =1/1 0001 =1/2 0010 =1/4 0011 =1/8 0100 = 1/16 0101 = External TCLK1 0110 = External TCLK1 0111 = External TCLK1	4'b0
Divider MUX1	[7:4]	RW	Select Mux input for PWM Timer 1 0000 =1/1 0001 =1/2 0010 =1/4 0011 =1/8 0100 = 1/16 0101 = External TCLK1 0110 = External TCLK1 0111 = External TCLK1	4'b0
Divider MUX0	[3:0]	RW	Select Mux input for PWM Timer 0 0000 =1/1 0001 =1/2 0010 =1/4 0011 =1/8 0100 = 1/16 0101 = External TCLK1 0110 = External TCLK1 0111 = External TCLK1	4'b0

19.5.1.3 TCON

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x08h, 0x08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:23]	–	Reserved	–
Timer 4 Auto Reload on/off	[22]	RW	0 = One-Shot 1 = Interval Mode(Auto-Reload)	1'b0
Timer 4 Manual Update	[21]	RW	0 = No Operation 1 = Update TCNTB4	1'b0
Timer 4 Start/Stop	[20]	RW	0 = Stop 1 = Start Timer 4	1'b0
Timer 3 Auto Reload on/off	[19]	RW	0 = One-Shot 1 = Interval Mode(Auto-Reload)	1'b0
Timer 3 Output Inverter on/off	[18]	RW	0 = Inverter Off 1 = TOUT3 Inverter-On	1'b0
Timer 3 Manual Update	[17]	RW	0 = No Operation 1 = Update TCNTB3,TCMPB3	1'b0
Timer 3 Start/Stop	[16]	RW	0 = Stop 1 = Start Timer 3	1'b0
Timer 2 Auto Reload on/off	[15]	RW	0 = One-Shot 1 = Interval Mode(Auto-Reload)	1'b0
Timer 2 Output Inverter on/off	[14]	RW	0 = Inverter Off 1 = TOUT2 Inverter-On	1'b0
Timer 2 Manual Update	[13]	RW	0 = No Operation 1 = Update TCNTB2,TCMPB2	1'b0
Timer 2 Start/Stop	[12]	RW	0 = Stop 1 = Start Timer 2	1'b0
Timer 1 Auto Reload on/off	[11]	RW	0 = One-Shot 1 = Interval Mode(Auto-Reload)	1'b0
Timer 1 Output Inverter on/off	[10]	RW	0 = Inverter Off 1 = TOUT1 Inverter-On	1'b0
Timer 1 Manual Update	[9]	RW	0 = No Operation 1 = Update TCNTB1,TCMPB1	1'b0
Timer 1 Start/Stop	[8]	RW	0 = Stop 1 = Start Timer 1	1'b0
RSVD	[7:5]	–	Reserved	-
Dead zone enable/disable	[4]	RW	Dead zone Generator Enable/Disable	1'b0
Timer 0 Auto Reload on/off	[3]	RW	0 = One-Shot 1 = Interval Mode(Auto-Reload)	1'b0
Timer 0 Output	[2]	RW	0 = Inverter Off	1'b0

Name	Bit	Type	Description	Reset Value
Inverter on/off			1 = TOUT0 Inverter-On	
Timer 0 Manual Update	[1]	RW	0 = No Operation 1 = Update TCNTB0,TCMPB0	1'b0
Timer 0 Start/Stop	[0]	RW	0 = Stop 1 = Start Timer 0	1'b0

19.5.1.4 TCNTB0

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x0Ch, 0x0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 0 Count Buffer	[31:0]	RW	Timer 0 Count Buffer Register	32'b0

19.5.1.5 TCMPB0

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x10h, 0x10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 0 Compare Buffer	[31:0]	RW	Timer 0 Compare Buffer Register	32'b0

19.5.1.6 TCNTO0

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x14h, 0x14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 0 Count Observation	[31:0]	R	Timer 0 Count Observation Register	32'b0

19.5.1.7 TCNTB1

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x18h, 0x18h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 1 Count Buffer	[31:0]	RW	Timer 1 Count Buffer Register	32'b0

19.5.1.8 TCMPB1

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x1Ch, 0x1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 1 Compare Buffer	[31:0]	RW	Timer 1 Compare Buffer Register	32'b0

19.5.1.9 TCNTO1

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x20h, 0x20h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 1 Count Observation	[31:0]	R	Timer 1 Count Observation Register	32'b0

19.5.1.10 TCNTB2

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x24h, 0x24h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 2 Count Buffer	[31:0]	RW	Timer 2 Count Buffer Register	32'b0

19.5.1.11 TCMPB2

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x28h, 0x28h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 2 Compare Buffer	[31:0]	RW	Timer 2 Compare Buffer Register	32'b0

19.5.1.12 TCNTO2

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x2Ch, 0x2Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 2 Count Observation	[31:0]	R	Timer 2 Count Observation Register	32'b0

19.5.1.13 TCNTB3

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x30h, 0x30h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 3 Count Buffer	[31:0]	RW	Timer 3 Count Buffer Register	32'b0

19.5.1.14 TCMPB3

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x34h, 0x34h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 3 Compare Buffer	[31:0]	RW	Timer 3 Compare Buffer Register	32'b0

19.5.1.15 TCNTO3

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x38h, 0x38h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 3 Count Observation	[31:0]	R	Timer 3 Count Observation Register	32'b0

19.5.1.16 TCNTB4

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x3Ch, 0x3Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 4 Count Buffer	[31:0]	RW	Timer 4 Count Buffer Register	32'b0

19.5.1.17 TCNTO4

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x40h, 0x40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Timer 4 Count Observation	[31:0]	R	Timer 4 Count Observation Register	32'b0

19.5.1.18 TINT_CSTAT

- Base Address: C001_7000h (TIMER)
- Base Address: C001_8000h (PWM)
- Address = Base Address + 0x44h, 0x44h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	–	Reserved	–
Timer 4 interrupt Status	[9]	RW	Timer 4 Interrupt Status Bit. Clears by writing "1" on this bit.	1'b0
Timer 3 interrupt Status	[8]	RW	Timer 3 Interrupt Status Bit. Clears by writing "1" on this bit.	1'b0
Timer 2 interrupt Status	[7]	RW	Timer 2 Interrupt Status Bit. Clears by writing "1" on this bit.	1'b0
Timer 1 interrupt Status	[6]	RW	Timer 1 Interrupt Status Bit. Clears by writing "1" on this bit.	1'b0
Timer 0 interrupt Status	[5]	RW	Timer 0 Interrupt Status Bit. Clears by writing "1" on this bit.	1'b0
Timer 4 interrupt Enable	[4]	RW	Timer 4 Interrupt Enable. 0 = Disabled 1 = Enabled	1'b0
Timer 3 interrupt Enable	[3]	RW	Timer 3 Interrupt Enable. 0 = Disabled 1 = Enabled	1'b0
Timer 2 interrupt Enable	[2]	RW	Timer 2 Interrupt Enable. 0 = Disabled 1 = Enabled	1'b0
Timer 1 interrupt Enable	[1]	RW	Timer 1 Interrupt Enable. 0 = Disabled 1 = Enabled	1'b0
Timer 0 interrupt Enable	[0]	RW	Timer 0 Interrupt Enable. 0 = Disabled 1 = Enabled	1'b0

20 Analog Digital Converter (ADC)

20.1 Overview

The ADC2802A is a 28 nm CMOS 1.8 V 12-bit analog-to-digital converter (ADC) with 16-ch analog input MUX and level-shifters for low-voltage digital interface. It converts single-ended analog input signal to 12-bit digital output codes at a maximum conversion rate of 1MSPS.

The device is a cyclic type monolithic ADC, which provides an on-chip sample-and-hold and power down mode.

20.2 Features

- 28 nm Low Power CMOS Process
- Resolution: 12-bit
- Conversion rate (Fs): 1 MSPS
- Power consumption:
  - 1.0 mW (Fs = 1 MSPS) @ Normal operation mode Typ.
  - 0.005 mW @ Power down mode Typ.
- Input range: 0 to AVDD18 (Normally 1.8 V)
- Input frequency: up to 100 kHz
- Digital output: CMOS Level (0 to AVDD10)
- Operation temperature range (ambient): –25 °C to 85 °C

20.3 Block Diagram

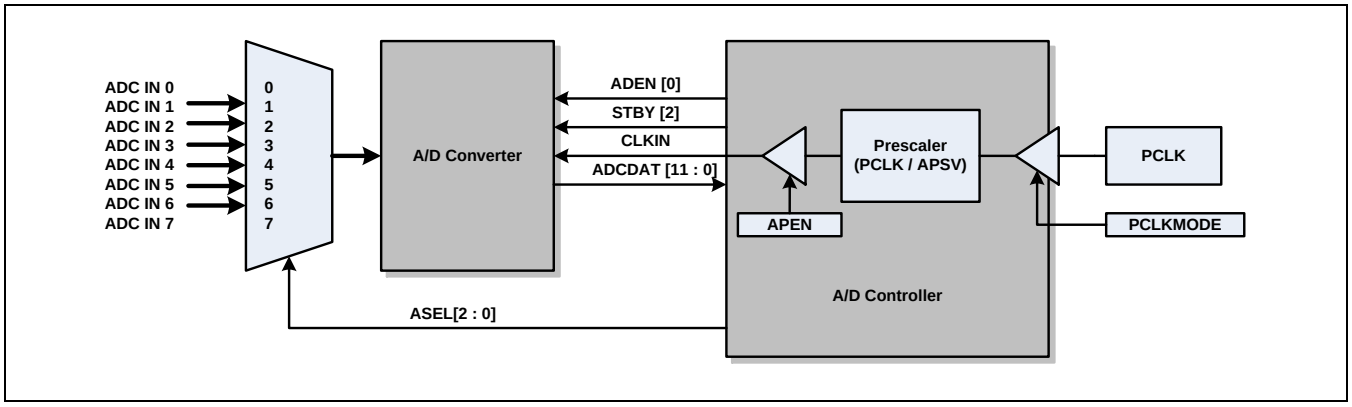


Figure 20-1 ADC Block Diagram

20.4 Functional Description

The S5P4418 can receive eight ADC inputs and select one of the ADC inputs by using ADCCON.ASEL[2:0]. The sizes of the eight ADC inputs depend on the size of VREF.

The ADC controller uses PCLK and the PCLK is divided in the Prescaler and applied to the ADC. At this time, the ADCCON.APEN bit is used for the application of CLKIN. Clock divide values by the Prescaler are available from 20 to 256. (Actually, since the register input value is [Clock Divide Value - 1], smaller divide values make the sampling more detailed. The clock divide value is determined by *ADCCON.APSV*bit.

If the ADC block continuously accepts after power is applied, it consumes current unnecessarily. In this case, it is better to power down the A/D converter by using the ADCCON.STBY bit. The ADCCON.STBY bit determines the power input for the ADC block. If the ADCCON.STBY bit is "0", the ADC block waits for ADC input after power on. After that, if the ADCCON.ADEN bit is set as "1" to accept ADC input, the ADC operation is actually performed. On the other hand, if the ADCCON.STBY bit is "1", the ADC block goes to power down status, that is, power is not applied. This is called Standby mode. (In Standby mode, only about 20 uA current is consumed.

If the ADC block is not used, set the ADCCON.STBY bit as "1" and power off the ADC block. In this way, unnecessary power consumption by the ADC block can be reduced. In addition, since the supply of the clock can be determined by using the ADCCON.APEN bit, power consumption can be reduced further by stopping the clock supply when supply is unnecessary.

20.4.1 I/O Chart

Table 20-1 I/O Chart

Index	ADC Input (V)	Digital Output	
0	~ 0.00322	00_0000_0000	1LSB = 3.22 mV V_{REF} = 3.3 V AGND = 0.0 V
1	0.00322 ~ 0.00644	00_0000_0001	
2	0.00644 ~ 0.00967	00_0000_0010	
~	~	~	
511	1.64678 ~ 1.65000	01_1111_1111	
512	1.65000 ~ 1.65322	10_0000_0000	
513	1.65322 ~ 1.65644	10_0000_0001	
~	~	~	
1021	3.29033 ~ 3.29355	11_1111_1101	
1022	3.29355 ~ 3.29678	11_1111_1110	
1023	3.29678 ~	11_1111_1111	

20.4.2 Timing

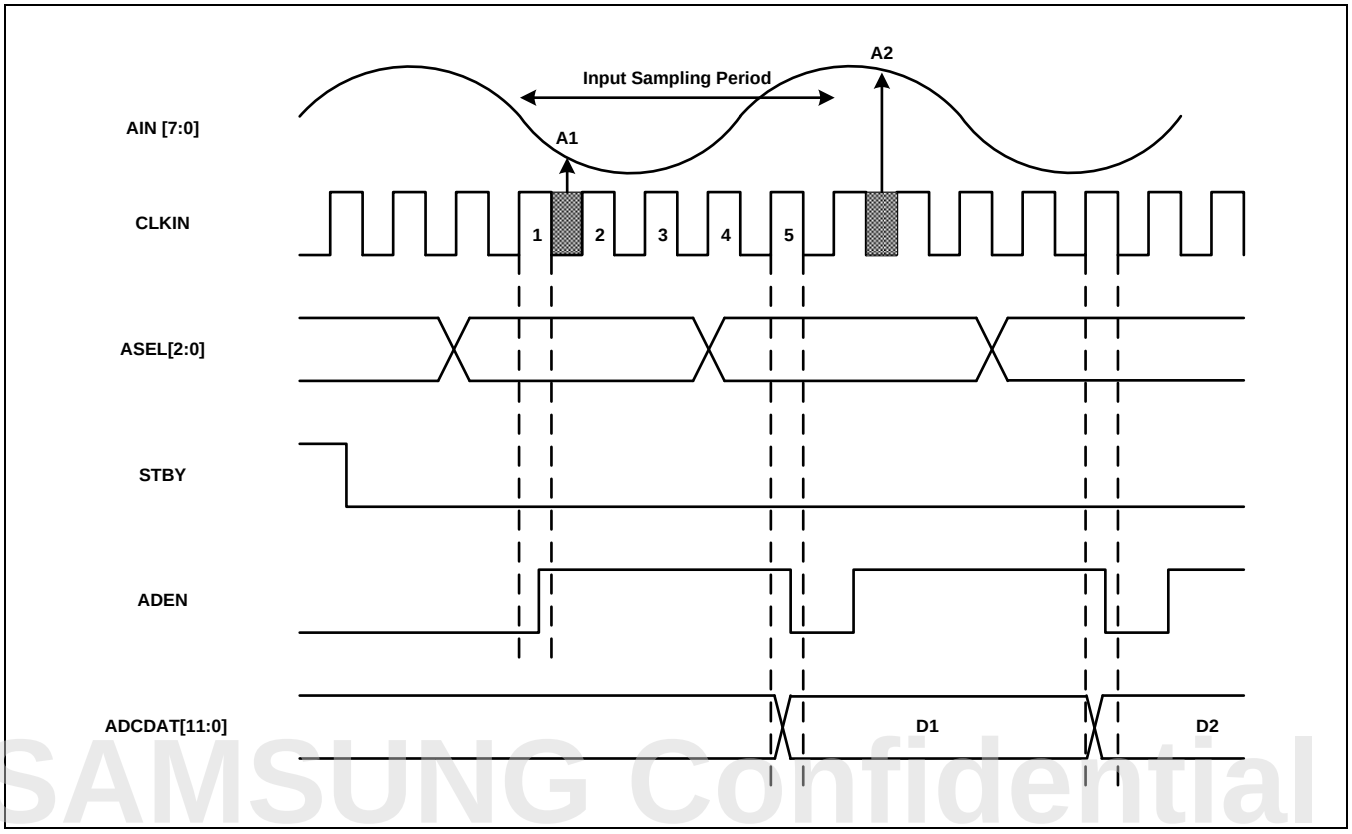


Figure 20-2 Main Waveform

Figure 20-2 shows the timing chart for the ADC. AIN[7:0] is continuously input from the outside and CLKIN is supplied via the ADCCON.APEN bit. After AIN[7:0] is selected, by using ASEL[2:0], the ADCCON.STBY bit is set as "0" to supply power to the ADC block. Finally, A/D conversion is progressed by setting the ADCCON.ADEN bit as "1".After the conversion is completed, EDO occurs and the ADCCON.ADEN bit is automatically cleared to "0". After that, A/D Converted Data (D1) can be read through ADCDAT.ADCDAT. Since it always takes 5-cycles for 10-bit conversion, the maximum conversion rate of the S5P4418 is 1MSPS.Set the ADCCON.ADEN bit as "1" to operate the ADC again.

20.4.3 Analog Input Selection Table

Table 20-2 Analog Input Selection Table

CHANNEL	ASEL[2]	ASEL[1]	ASEL[0]
Analog Input [0]	0	0	0
Analog Input [1]	0	0	1
Analog Input [2]	0	1	0
Analog Input [3]	0	1	1
Analog Input [4]	1	0	0
Analog Input [5]	1	0	1
Analog Input [6]	1	1	0
Analog Input [7]	1	1	1

20.4.4 Flowchart

- PCLK Supply: CLKENB.PCLKMODE = 1
- Analog Input Select: ADCCON.ASEL
- ADC Power On: ADCCON.STBY = 0
- CLKIN Divide Value: ADCCON.APSV
- CLKIN On: ADCCON.APEN
- ADC Enable: ADCCON.ADEN
- A/D Conversion Process
- Read ADCDAT.ADCDAT
- CLKIN Off
- ADC Power Off

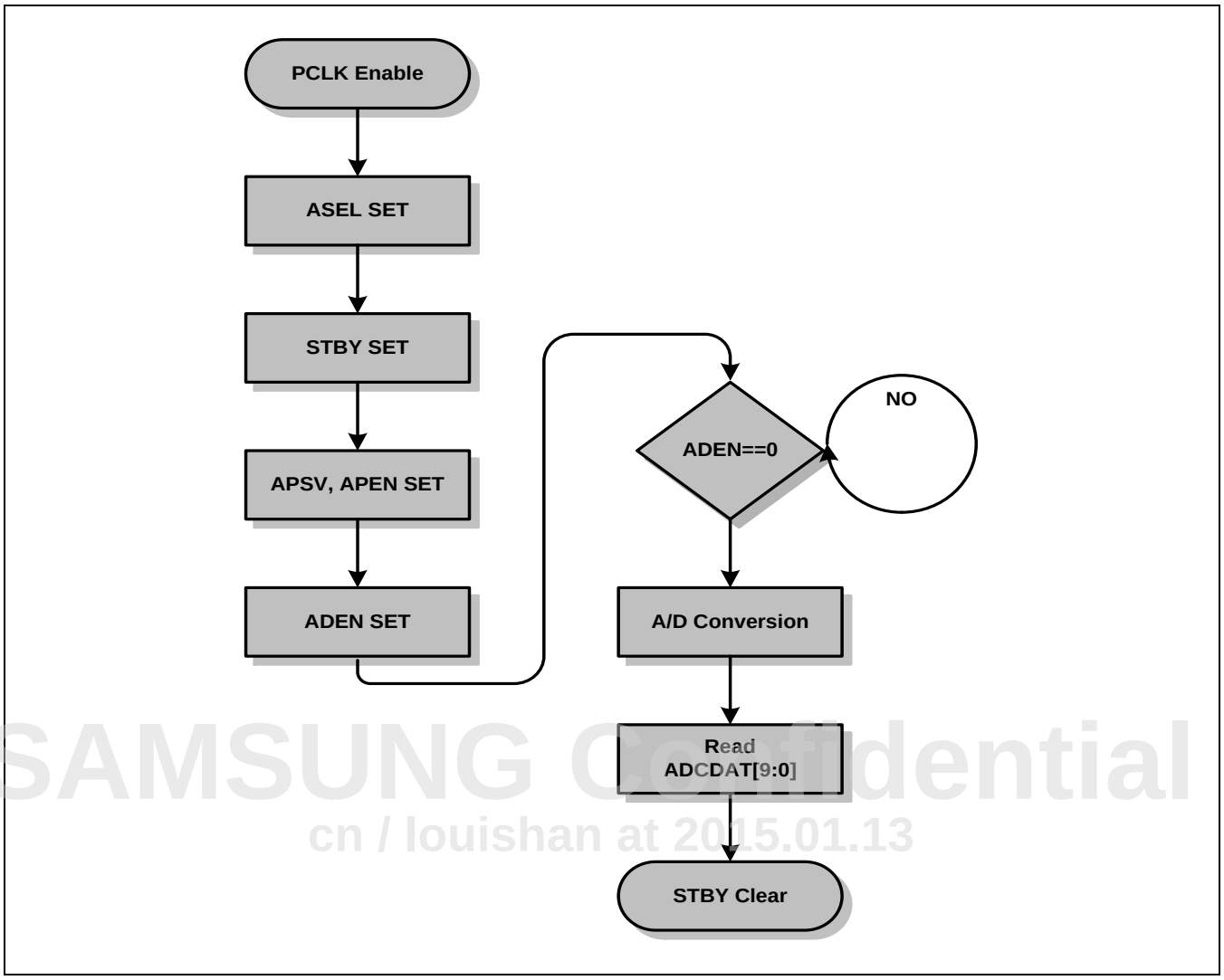


Figure 20-3 ADC Sequence Flowchart

20.5 Register Description

20.5.1 Register Map Summary

- Base Address: C005_3000h

Register	Offset	Description	Reset Value
ADCCON	0x00h	ADC control register	0x0000_BFC4
ADCDAT	0x04h	ADC output data register	0x0000_0000
ADCINTENB	0x08h	ADC interrupt enable register	0x0000_0000
ADCINTCLR	0x0Ch	ADC interrupt pending and clear register	0x0000_0000

20.5.1.1 ADCCON

- Base Address: C005_3000h
- Address = Base Address + 0x00h, Reset Value = 0x0000_BFC4

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b1
APEN	[14]	RW	Prescaler Enable. This bit determines the supply of the clock divided by the APSV register for the A/D converter. Before the APEN bit is enabled, the APSV register should be set. 0 = Disable 1 = Enable	1'b0
APSV	[13:6]	RW	A/D Converter Clock Prescaler Value (8bit) To write a value to this bit, APEN should be `0'. The maximum value of the ADC CLK divided by the APSV value is 2.5 MHz (400 ns) (where PCLK is 50 MHz). The minimum and the maximum value for the APSV bit are 19 and 255, respectively. (In effect, the range of the clock divide value is from 20 to 256). Input Value = Clock Divide Value -1. For divide-by-20 and divide-by-100, (20-1) = 19 and (100-1) = 99 are input to APSV, respectively.	8'hFF
ASEL	[5:3]	RW	These bits select ADCIN. NXP4330Q has four ADCINs and can select one of them. 000 = ADCIN_0 001 = ADCIN_1 010 = ADCIN_2 011 = ADCIN_3 100 = ADCIN_4 101 = ADCIN_5 110 = ADCIN_6 111 = ADCIN_7	3'b0
STBY	[2]	RW	A/D Converter Standby Mode. If this bit is set as `0', power is actually applied to the A/D converter. 0 = ADC Power On 1 = ADC Power Off(Standby)	1'b1
RSVD	[1]	–	Reserved	1'b0
ADEN	[0]	RW	A/D Conversion Start When the A/D conversion ends, this bit is cleared to "0". Read > Check the A/D conversion operation. 0 = Idle 1 = Busy Write > Start the A/D conversion. 0 = None 1 = Start A/D conversion	1'b0

20.5.1.2 ADCDAT

- Base Address: C005_3000h
- Address = Base Address + 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	20'b0
ADCDAT	[11:0]	R	These bits are 12-bit data converted via the ADC.	12'b0

20.5.1.3 ADCINTENB

- Base Address: C005_3000h
- Address = Base Address + 0x08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	31'b0
ADCINTENB	[0]	RW	ADC Interrupt Enable. (This bit determines the generation of an interrupt when EOC occurs.) This bit determines if interrupt occurs when the ADEN bit is "0". 0 = Interrupt Disable 1 = Interrupt Enable	1'b0

20.5.1.4 ADCINTCLR

- Base Address: C005_3000h
- Address = Base Address + 0x0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	31'b0
ADCINTCLR	[0]	RW	EOC Interrupt Pending and Clear Read > 0 = None 1 = Interrupt Pended Write > 0 = None 1 = Pending Clear	1'b0

21 I2C Controller

21.1 Overview

The S5P4418 application processor can support a multi-master I2C-bus serial interface. A dedicated serial data line (SDA) and a serial clock line (SCL) carry information between bus masters and peripheral devices which are connected to the I2C-bus. The SDA and SCL lines are bi-directional. Devices communicating with each other on a serial bus must have some form of protocol that avoids all possibilities of confusion, data loss and blockage of information. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible.

In multi-master I2C-bus mode, multiple microprocessor can receive or transmit serial data to or from slave devices. The master that initiates a data transfer over the I2C-bus is responsible for terminating the transfer.

21.2 Features

- Compliance to the AMBA specification onwards for easy integration into SoC implementation
- Only 2 bus lines are required; a serial data line (SDA) and a serial clock line (SCL). The simple 2-wire serial I2C-bus minimizes interconnections so ICs have fewer pins.
- The completely integrated I2C-bus protocol eliminates the need for address decoders and other glue logic.
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; master can operate as master-transmitter or as master-receiver.
- It is a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer.
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.
- System bus asynchronous reset is not supported.
- Every operation command used in I2C-bus needs delays of minimum 3 Cycles (PCLK) between them.
- High speed mode, combined format, 10-bit address are not supported

21.3 Functional Description

21.3.1 The Concept of the I2C-Bus

The I2C-bus interface has four operation modes:

- Master transmitter mode
- Master receiver mode
- Slave transmitter mode
- Slave receiver mode

Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address (whether it's a microcontroller, LCD driver, memory or keyboard interface) and operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfer. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave. *Table 21-1* shows the basic terminology of I2C-bus.

Table 21-1 I/O I2C-Bus Terminology Definition

Term	Definition
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Term	Definition
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Multi-Master	More than one master can attempt to control the bus at the same time without corruption the message
Slave	The device addressed by a master
Arbitration	Procedure to ensure that, if more that one master simultaneously tires to control the bus, only one is allowed to do so and the winning message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

21.3.2 IC Protocol

Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a current-source or pull-up resistor. *Figure 21-1* shows the hardware layout of the I2C-bus. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode or up to 400 kbit/s in the Fast-mode.

Figure 21-2 shows additional information of I2C-bus pad structure.

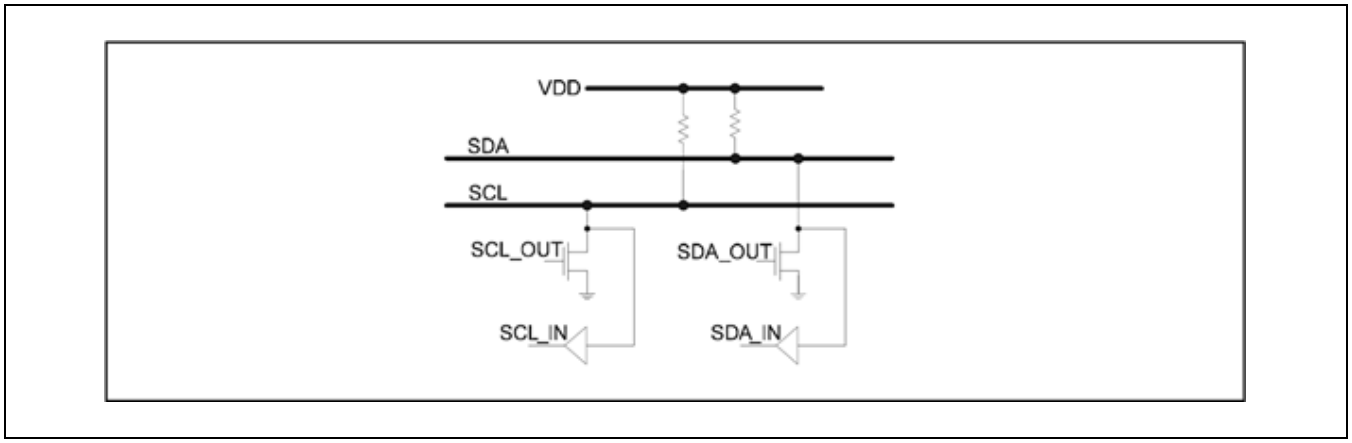


Figure 21-1 Connection of Devices to the I2C-Bus

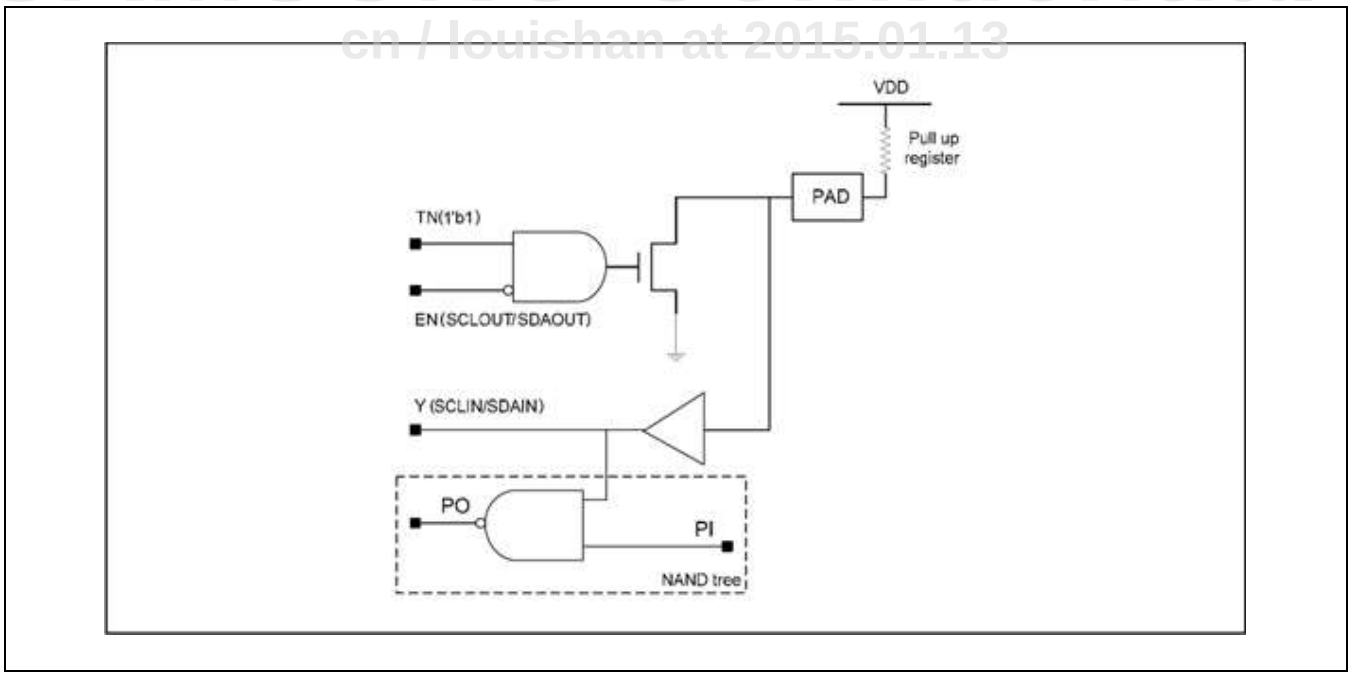


Figure 21-2 Bi-Direction PAD Structure of the I2C-Bus

21.3.3 Start/Stop Operation

Within the procedure of the I2C-bus, unique situations arise which are defined as START (S) and STOP (P) condition. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP condition are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

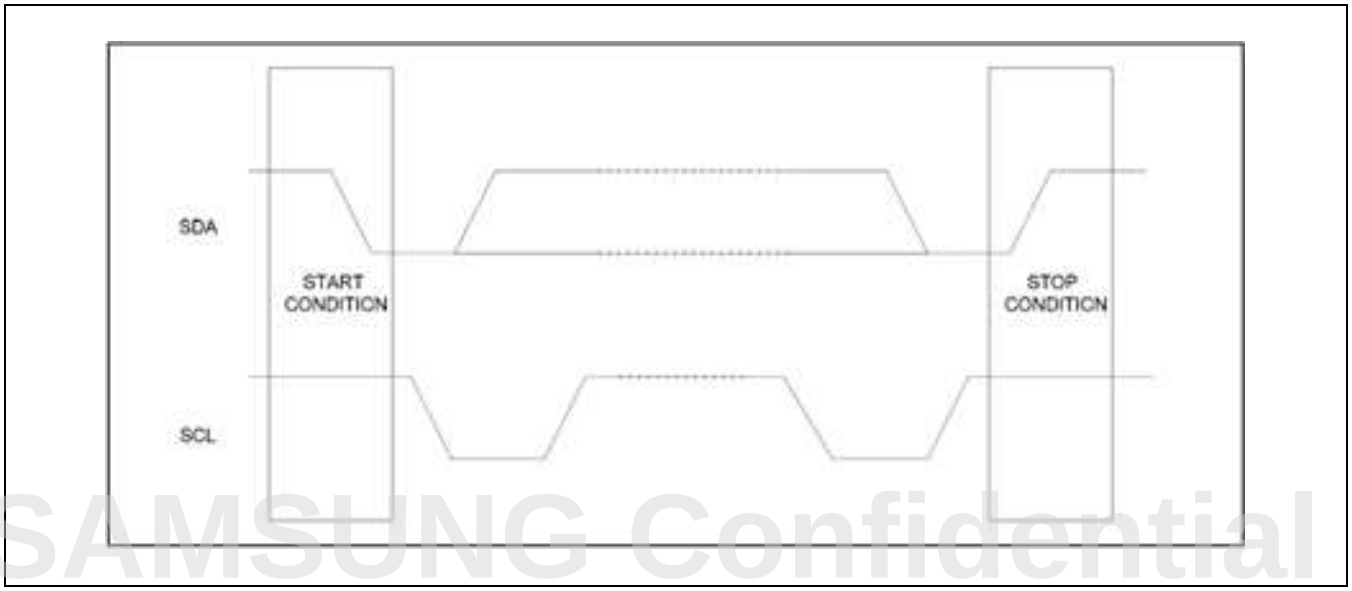


Figure 21-3 Start/Stop Condition of I2C-Bus

21.3.4 Data Format

The first seven bits of the first byte make up the slave address. The eighth bit is the LSB (Least Significant Bit). It determines the direction of the message. A zero in the least significant position of the first byte means that the master will write information to a selected slave. A one in this position means that the master will read information from the slave. A data transfer is always terminated by a STOP condition (P) generated by the master. The first acknowledge is generated by the slave. But the acknowledge of data is generated by the receiver. *Figure 21-4* shows the 7-bit data format.

Possible data transfer formats are:

- Master-transfer transmits to slave receiver.
- Master reads slave immediately after first byte. At the moment of the first acknowledge, the master-transfer becomes a master-receiver and the slave-receiver becomes a slave-transfer.
- Combined format is not supported.

NOTE: A START condition immediately followed by a STOP condition (void message) is an illegal format.

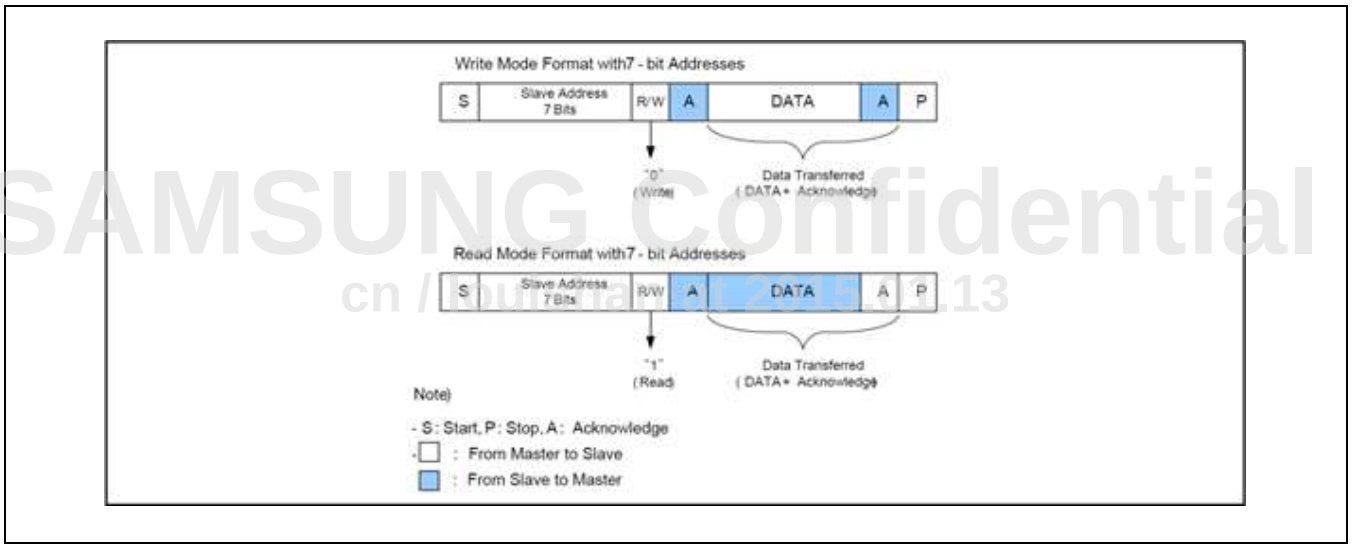


Figure 21-4 I2C-Bus Data Format

21.3.5 Data Transfer

Every byte put on the SDA line must be eight bits long. The number of bytes which can be transmitted per transfer is unrestricted. The address byte is transmitted by the master when the I2C-bus is operating in master mode. When a master initiates a start condition, it sends its slave address onto the bus. The address byte consists of a 7-bit address and a 1-bit transfer direction indicator (that is, write or read). If bit 8 is "0", a transmit operation (write) is indicated; if bit 8 is "1", a request for data (read) is indicated.

The master ends the indicated transfer operation by transmitting a stop condition. If the master wants to continue sending data over the bus, it can generate another start condition and another slave address. Each byte must be followed by an acknowledge (ACK) bit. Serial data and addresses are transferred with the most significant bit (MSB) first. In this way, read-write operations can be performed in various formats. *Figure 21-5* shows the sequence of data transmission.

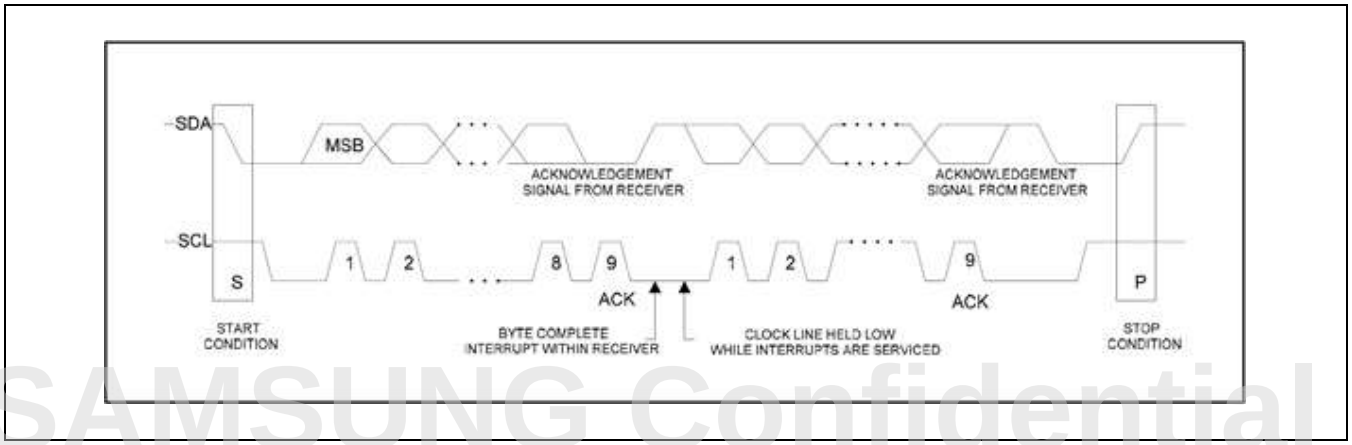


Figure 21-5 Data Transfer on the I2C-Bus

21.3.6 Arbitration

Arbitration takes place on the SDA line to prevent contention on the bus between two masters, while the SCL line is at the HIGH level. If a master with a SDA High level detects another master with a SDA Low level, it will not initiate a data transfer because the current level on the bus dose not correspond to its own. The master that loses the arbitration can generate clock pulses until the end of the last-transmitted data byte. The arbitration procedure can continue while data continues to be transferred over the bus. *Figure 21-6* shows the arbitration.

The first stage of arbitration is the comparison of address bits. If a master loses the arbitration during the addressing stage of a data transfer, it is possible that the master which won the arbitration is attempting to address the master which lost. In this case, the losing master must immediately switch to the slave receiver mode.

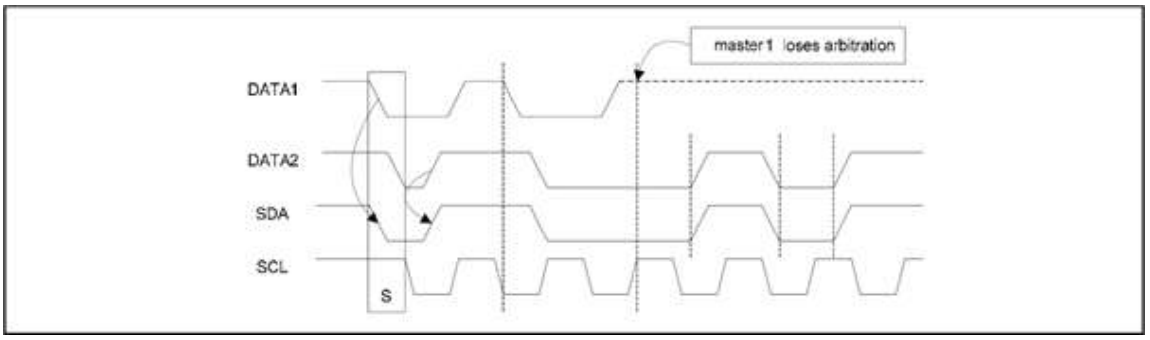


Figure 21-6 Arbitration Procedure between Two Masters

21.3.7 Synchronization

Clock synchronization is performed using the wired-AND connection of I2C-bus interface to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and, once a device clock has gone LOW, it will hold SCL line in that state until the clock HIGH state is reached. However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. In this way, a synchronized SCL clock is generated with its LOW period determined by the device with the longest clock LOW period and its HIGH period determined by the one with the shortest clock HIGH period. Devices with shorter LOW periods enter a HIGH wait-state during this time. *Figure 21-7* shows the procedure of SCL generation.

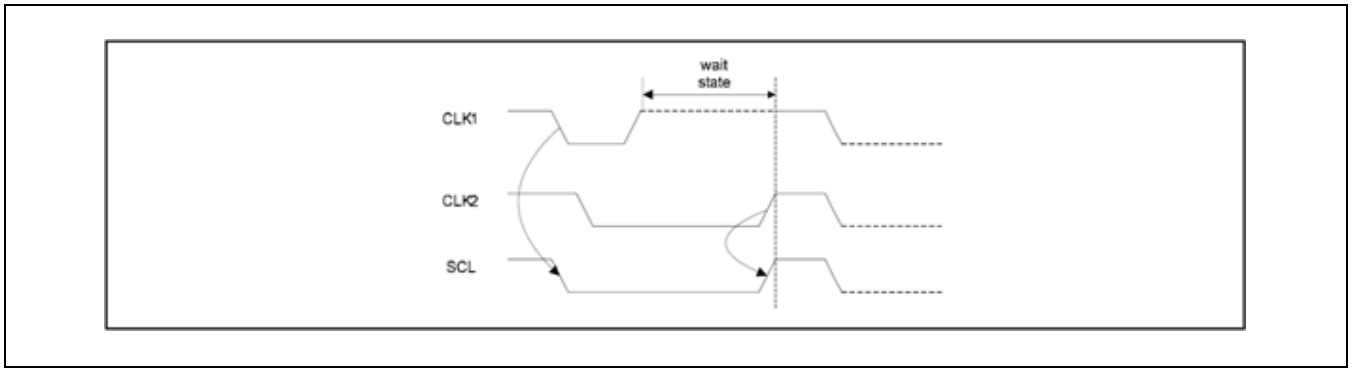


Figure 21-7 Clock Synchronization

21.3.8 Acknowledge

Data transfer with acknowledge is obligatory. To complete one-byte transfer operation, the receiver must send an ACK bit to the transmitter. The ACK pulse occurs at the ninth clock of the SCL line (eight clocks are required to complete the one-byte transfer).

The transmitter releases the SDA line (that is, it sends the SDA line High) when the ACK clock pulse is received. The receiver must drive the SDA line Low during the ACK clock pulse so that SDA is Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enable and disabled by software (ICCR[7]). *Figure 21-8* shows data transfer with acknowledge signal.

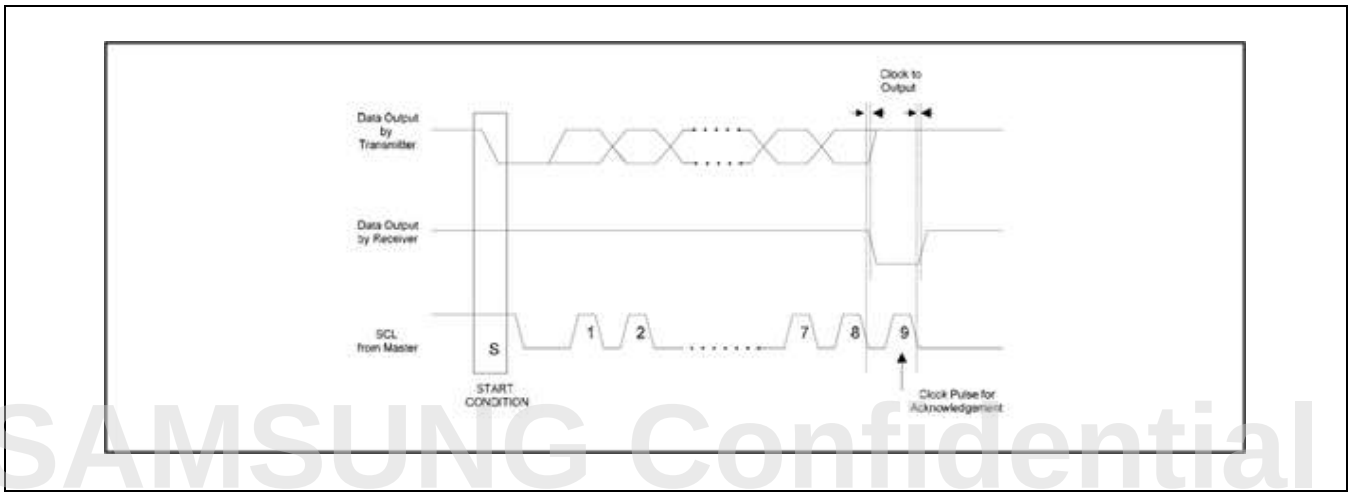


Figure 21-8 Acknowledge on the I2C-Bus

21.3.9 Read/Write Operation

When operating in transmitter mode, the I2C-bus interface interrupt routine waits for the master to write a data byte into the I2C-bus data shift register (IDSR). To do this, it holds the SCL line Low prior to transmission. In receive mode, the I2C-bus interface waits for the master to read the byte from the I2C-bus data shift register (IDSR). It does this by holding the SCL line Low following the complete reception of a data byte.

21.3.10 Configuration I2C-Bus

Data transfer with acknowledge is obligatory. To complete one-byte transfer operation, the receiver must send an ACK bit to the transmitter. The ACK to control the frequency of the serial clock (SCL), user has to program the 4-bit prescaler value in the ICCR register.

Timing of the SCL and SDA

- Standard mode: fscl = Max. 100 kHz (Period: 10 us)
- Fast mode: fscl = Max. 400 kHz (period: 2.5 us)

Table 21-2 Characteristics of the SDA and SCL Bus Lines for Standard and Fast Mode I2S-Bus

Parameter	Symbol	STANDARD MODE		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{scl}	0	100	0	400	kHz
Hold time Start condition. After this period, the first clock pulse is generated	$t_{hold:start}$	4.0	–	0.6	–	µs
Low period of SCL clock	t_{LOW}	4.7	–	1.3	–	µs
High period of SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Data hold time	$t_{hold:DATA}$	0	3.45	0	0.9	µs
Data setup time	$t_{setup:DATA}$	250	–	100	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	20+0.1Cb	300	ns
Setup time for Stop condition	$tS_{etup:STOP}$	4.0	–	0.6	–	µs
Captive load for each bus line	C_b	–	400	–	400	pF
Bus free time between a Stop and Start condition	$t_{BUSfree}$	4.7	–	1.3	–	µs

NOTE: * Cb is total capacitance of one bus line in pF

Timing spec for SCL does not affect slave mode devices. (EG. High/Low SCL period, Start/Stop data hold time)

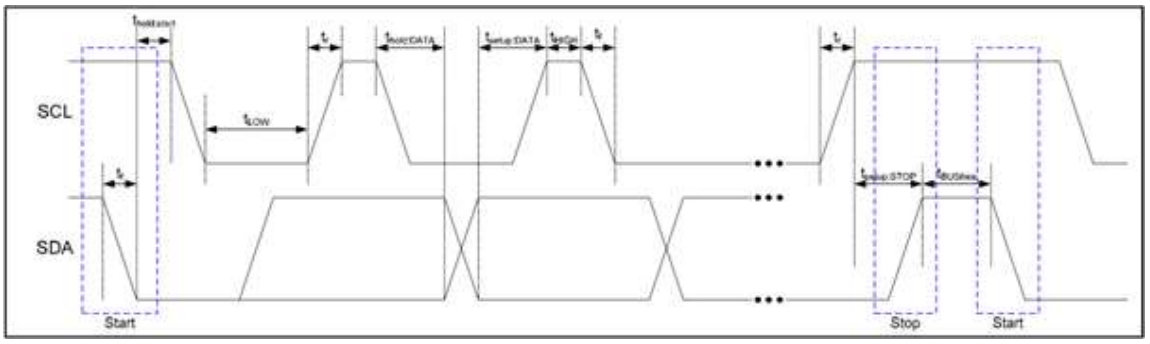


Figure 21-9 Timing on the SCL and SDA

21.3.11 Operations

To control multi-master I2C-bus operations, user has to write values to the following registers:

- Multi-master I2C-bus control register, ICCR
- Multi-master I2C-bus control-status register, ICSR
- Multi-master I2C-bus Tx/Rx data shift register, IDSR
- Multi-master I2C-bus address register, IAR
- Multi-master I2C-bus stop control register, STOPCON

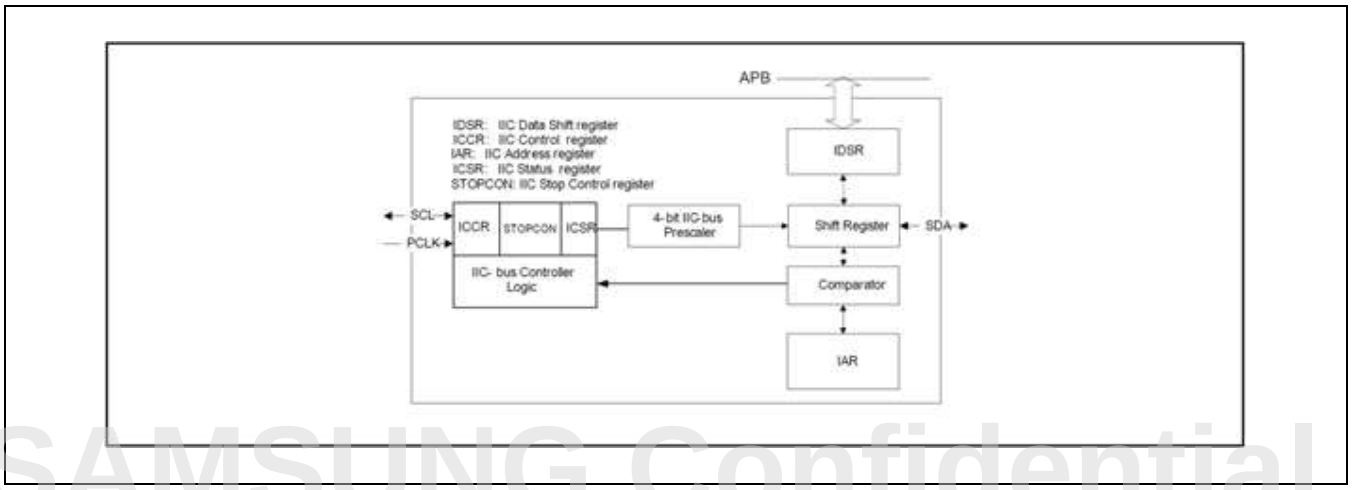


Figure 21-10 Functional Block Diagram of I2C-Bus

21.3.12 Interrupt Generation

When one byte transmission or reception, appointed as slave and a loss of the bus arbitration, this block requests interrupt to external interrupt controller. To enable the I2C-bus interrupt, the ICCR[5] bit should be set to 1. When the I2C-bus interrupt is enabled, the interrupt signal generates request signal to CPU.

21.3.13 System Bus Reset

The I2C-bus was designed for system bus clock synchronous reset scheme. Asynchronous reset scheme is forbidden.

21.4 Programming Guide

21.4.1 I2C-Bus Initialize

The initialization sequence in this section is used for I2C-bus controller.

1. Provide a clock and Release a reset this signals are propagated all of the I2C-bus controller internal registers and logic.
2. Enable pad select alt-function of I2C

21.4.2 Commands

Following diagram shows I2C-bus operation command examples.

21.4.2.1 Master Transmitter Mode (M/Tx)

In this mode, master-transmitter addresses slave, sends data to slave-receiver, and terminates the transfer.

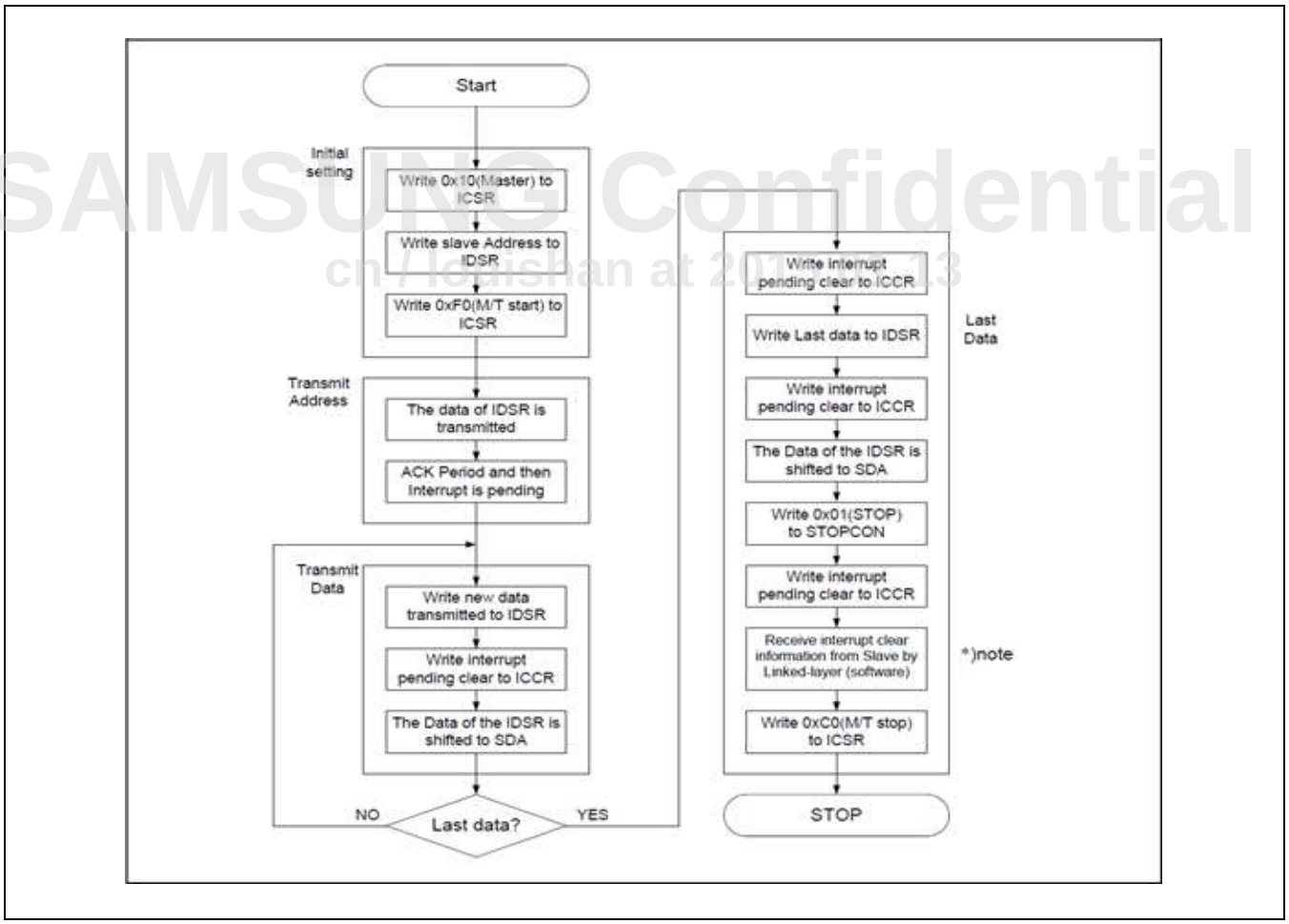


Figure 21-11 Master Transmitter Mode Operation

21.4.2.2 Master Receiver Mode (M/Rx)

In this mode, master-receiver addresses slave, receives data from slave-transmitter, and terminates the transfer.

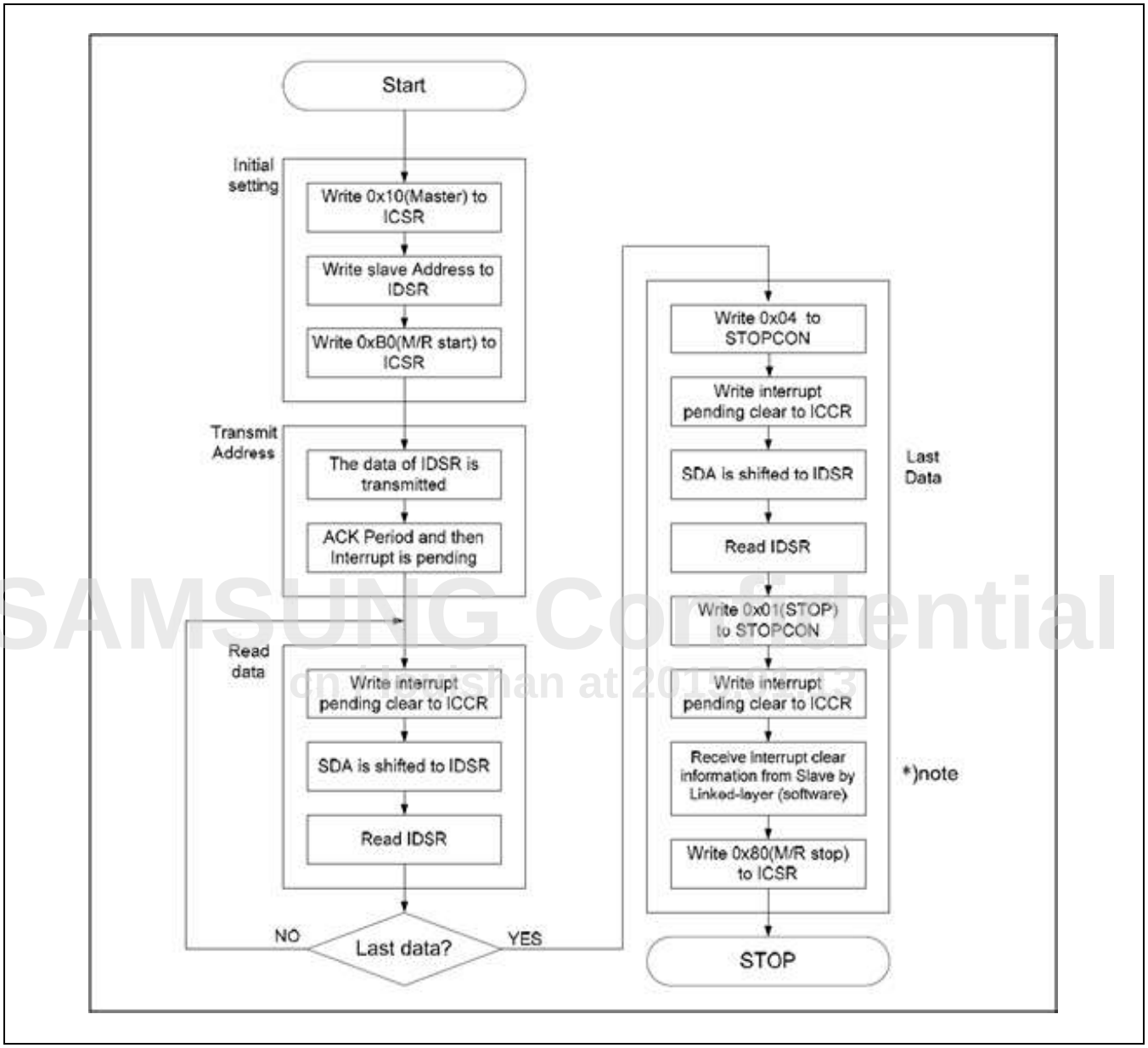


Figure 21-12 Master Receiver Mode Operation

21.4.2.3 Slave Transmitter Mode (S/Tx)

In this mode, received address is compared with IAR register value. If the current I2C-bus interface selected, slave-transmitter transfers data to master-receiver.

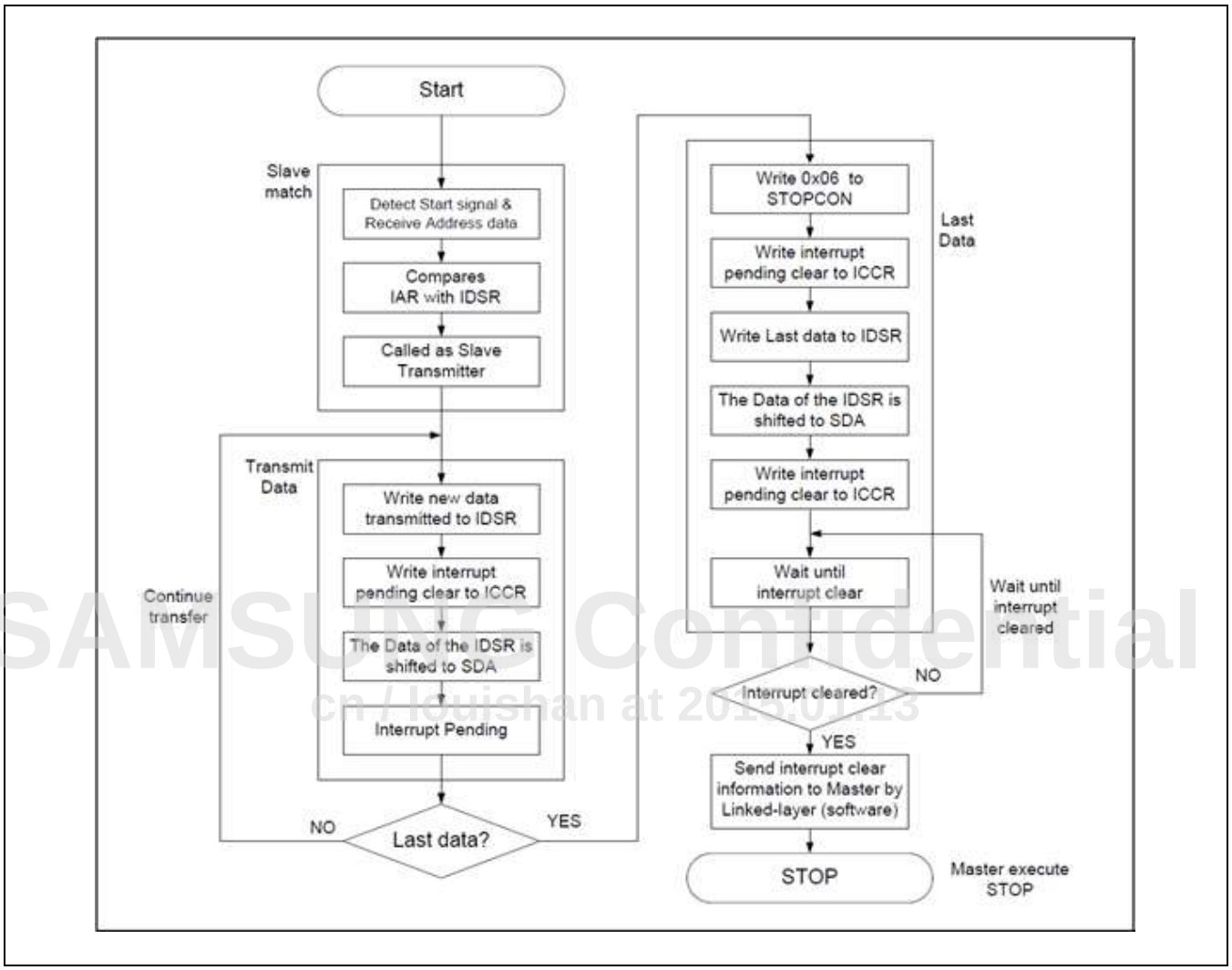


Figure 21-13 Slave Transmitter Mode Operation

21.4.2.4 Slave Receiver Mode (S/Rx)

In this mode, received address is compared with IAR register value. If the current I2C-bus interface selected, slave-receiver receives data from master-transmitter.

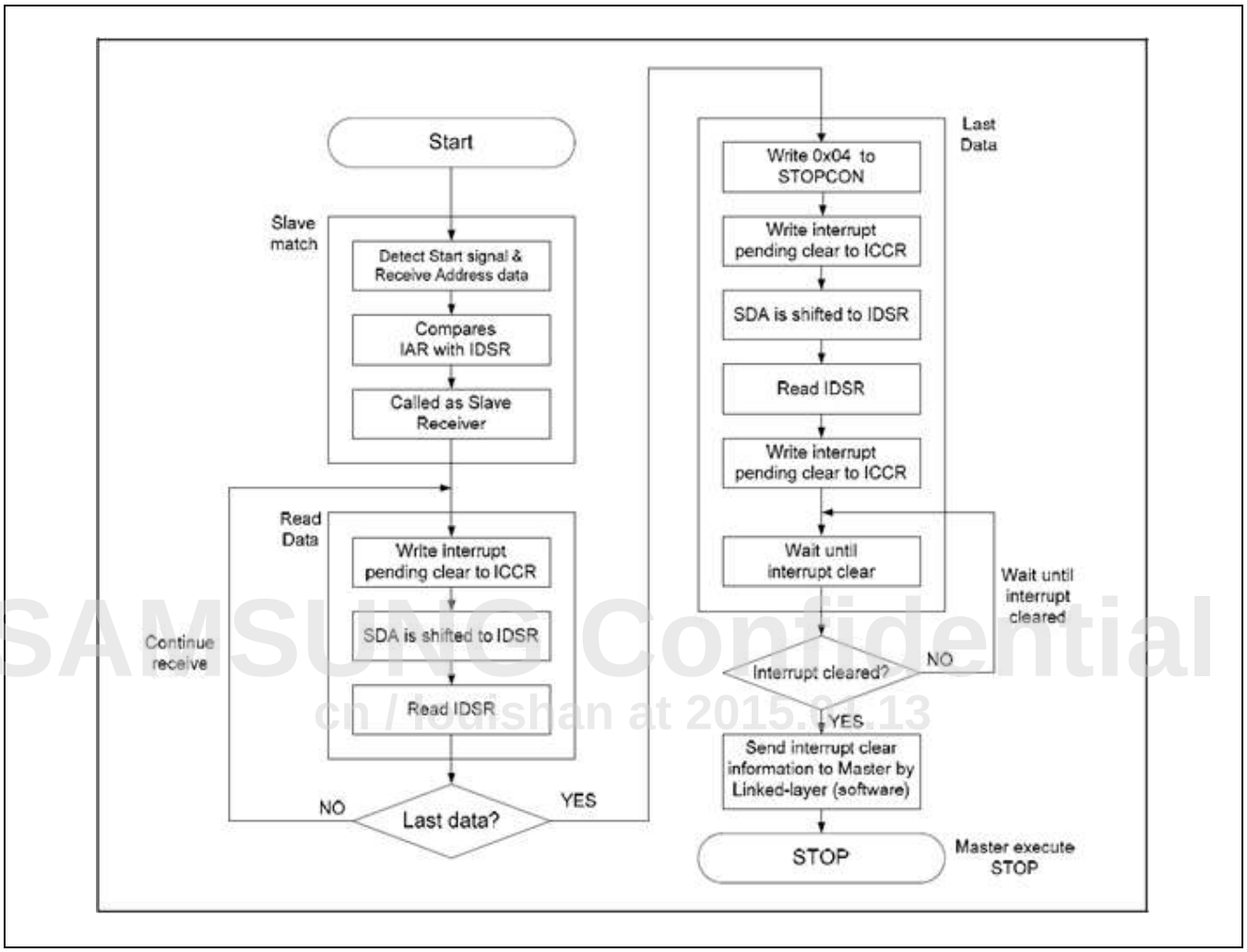


Figure 21-14 Slave Receiver Mode Operation

21.5 Design Issues

21.5.1 Software Layer

This I2C-bus module needs linked-layer (software) to control both module operations. For example, STOP sequence of I2C-bus operation needs the status of both I2C-bus modules. *Figure 21-15* shows a simple example how to deal with a STOP sequence of I2C-bus by linked-layer (by software).

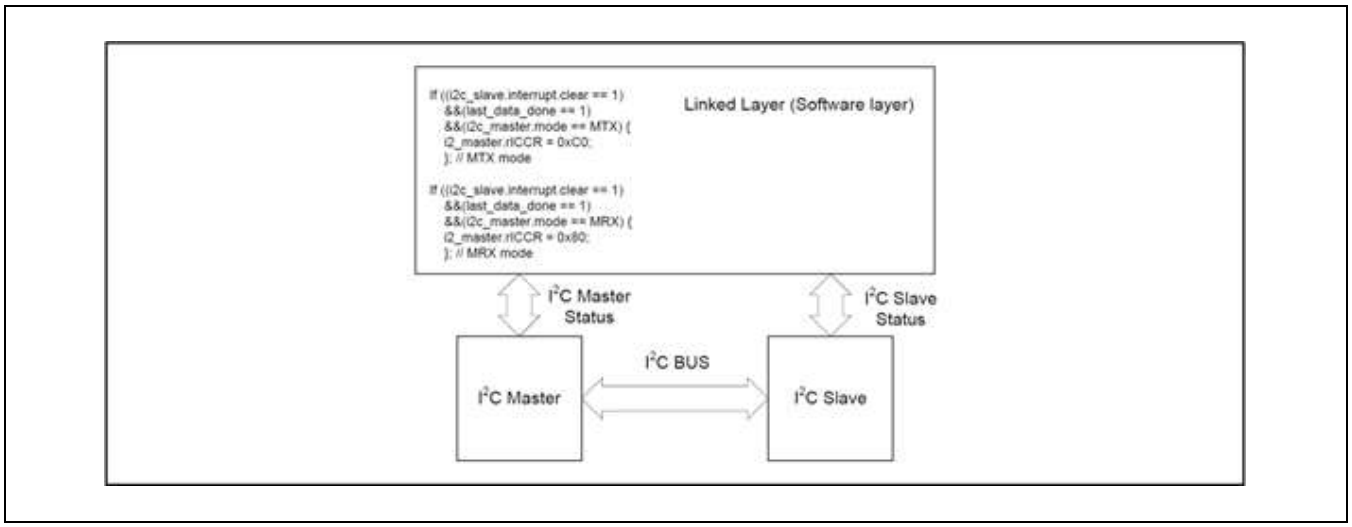


Figure 21-15 Linked Layer of the I2C-Bus

21.5.2 Delays between I2C-Bus Commands

This I2C-bus module needs 3-cycle delays between every register setting operations. For example, delay operation must be inserted between the Tx data write command (IDSR) and the interrupt clear command (ICCR).

Figure 21-16 shows a simple example how to deal with delays between each register setting operation.

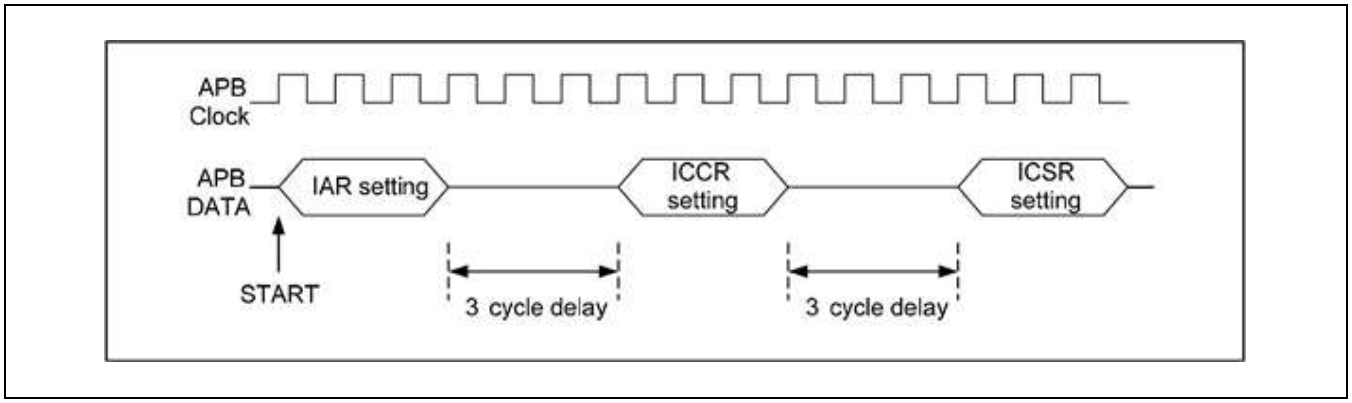


Figure 21-16 Delays between the I2C-Bus Commands

21.6 Register Description

21.6.1 Register Map Summary

- Base Address: C00A_4000h (I2C0)
- Base Address: C00A_5000h (I2C1)
- Base Address: C00A_6000h (I2C2)

Register	Offset	Description	Reset Value
ICCR	0x00h 0x00h 0x00h	I2C-bus control register	0x0000_0000
ICSR	0x04h 0x04h 0x04h	I2C-bus Control-Status Register	0x0000_0000
IAR	0x08h 0x08h 0x08h	I2C-bus Address Register	–
IDSR	0x0Ch 0x0Ch 0x0Ch	I2C-bus Transmit-Receive Data Shift Register	–
STOPCON	0x10h 0x10h 0x10h	I2C-bus Stop Control Register	0x0000_0000

21.6.1.1 ICCR

- Base Address: C00A_4000h (I2C0)
- Base Address: C00A_5000h (I2C1)
- Base Address: C00A_6000h (I2C2)
- Address = Base Address + 0x00h, 0x00h, 0x00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Interrupt clear	[8]	RW	I2C-bus Interrupt clear bit 0 = No Interrupt (when read) 1 = Interrupt is cleared (when write)	1'b0
Acknowledge enable	[7]	RW	I2C-bus acknowledge enable bit 0 = Disable ACK generation 1 = Enable ACK generation	1'b0
TX clock source selection	[6]	RW	Source clock of I2C-bus transmit clock prescaler selection bit 0 = I2C CCLK = fPCLK/16 1 = I2C CCLK = fPCLK/256	1'b0
TX/RX interrupt enalbe	[5]	RW	I2C-bus Tx/Rx interrupt enable/disable bit 0 = Disable interrupt 1 = Enable interrupt	1'b0
Interrupt pending flag	[4]	RW	I2C-bus Tx/Rx interrupts pending flag. Writing "1" is impossible 0 = No interrupt pending (when read), This bit is cleared (when write) 1 = Interrupt is pending (when read), No effect. Namely "1" doesn't be written to this bit NOTE: A I2C-bus interrupt occurs 1. When an 1-byte transmit or receive operation is terminated 2. When a general call or a slave address match occurs 3. If bus arbitration fails	1'b0
transmit clock value	[3:0]	RW	I2C-bus transmit clock prescaler. I2C-bus transmit clock frequency is determined by this 4-bit prescaler value, according to the following formula: Tx clock = I2C CLK/(ICCR[3:0]+1) NOTE: 1. I2CCLK is determined by ICCR[6] 2. Tx clock can vary by SCL transition time 3. When ICCR[6] = 0, "ICCR[3:0] = 0x0 or 0x1" is not available	4'bXXXX

21.6.1.2 ICSR

- Base Address: C00A_4000h (I2C0)
- Base Address: C00A_5000h (I2C1)
- Base Address: C00A_6000h (I2C2)
- Address = Base Address + 0x04h, 0x04h, 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Mode selection	[7:6]	RW	I2C-bus master-slave Tx/Rx mode select bits: 00 = Slave receive mode 01 = Slave transmit mode 10 = Master receive mode 11 = Master receive mode	2'b0
busy signal status	[5]	RW	I2C-bus busy signal status bit: 0 = I2C-bus not busy (when read), I2C-bus interface STOP signal generation (when write) 1 = I2C-bus busy (when read), I2C-bus interface START signal generation (when write)	1'b0
serail output enable	[4]	RW	I2C-bus data output enable/disable bit: 0 = Disable Rx/Tx 1 = Enable Rx/Tx	1'b0
arbitration status flag	[3]	R	I2C-bus arbitration procedure status flag bit 0 = Bus arbitration status okay 1 = Bus arbitration failed during serial I/O	1'b0
address-as-slave status flag	[2]	R	I2C-bus address-as-slave status flag bit: 0 = START/STOP condition was generated 1 = Received salve address matches the address value in the IAR	1'b0
address zero status flag	[1]	R	I2C-bus address zero status flag bit: 0 = START/STOP condition was generated 1 = Received slave address is "0x00"	1'b0
last-received bit status falg	[0]	R	I2C-bus last-received bit status flag bit 0 = Last-received bit si "0" (ACK was received) 1 = Last-received bit is "1" (ACK was not received)	1'b0

21.6.1.3 IAR

- Base Address: C00A_4000h (I2C0)
- Base Address: C00A_5000h (I2C1)
- Base Address: C00A_6000h (I2C2)
- Address = Base Address + 0x08h, 0x08h, 0x08h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
slave address	[7:1]	RW	7-bit slave address, latched from the I2C-bus: When serial output enable=0 in the ICSR, IAR is write-enable. You can read the IAR value at any time, regardless of the current serial output enable bit (ICSR[4]) setting Slave address = [7:1] Not mapped = [0]	–

21.6.1.4 IDSR

- Base Address: C00A_4000h (I2C0)
- Base Address: C00A_5000h (I2C1)
- Base Address: C00A_6000h (I2C2)
- Address = Base Address + 0x0Ch, 0x0Ch, 0x0Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
data shift	[7:0]	RW	8-bit data shift register for I2C-bus Tx/Rx operation: When serial output enable=1 in the ICSR, IDSR is write-enabled. You can read the IDSR value at any time, regardless of the current serial output enable bit (ICSR[4]) setting	–

21.6.1.5 STOPCON

- Base Address: C00A_4000h (I2C0)
- Base Address: C00A_5000h (I2C1)
- Base Address: C00A_6000h (I2C2)
- Address = Base Address + 0x10h, 0x10h, 0x10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
not-acknowledge generation data shift control	[2]	RW	I2C-nout acknowledge generation and data shift control bit 0 = Normal operation 1 = Master will generate not-acknowledge for the last byte received in master-receive mode. Or I2C will not shift the data shift register IDSR after the stop.	1'b0
data line release	[1]	RW	I2C-data bus release setting bit 0 = Normal operation 1 = Slave will release data bus line in Transfer mode after transmitting the last byte. NOTE: This bit can be only used in slave-transmit mode	1'b0
clock line release	[0]	RW	I2C-clock bus release setting bit 0 = Normal operation 1 = Master will release clock bus line for the stop condition after completing the transfer. NOTE: This bit can be only used in Master-transmit mode or Master-receive mode.	1'b0

NOTE: Writing 0x00 or 0x03 or 0x07 on the STOPCON register are not permitted

22 SPI/SSP

22.1 Overview

The SPI/SSP is a full-duplex synchronous serial interface. It supports Serial Peripheral Interface (SPI) and Synchronous Serial Protocol (SSP). It can connect to a variety of external converter, serial memory and many other device which use serial protocols for transferring data.

There are 4 I/O pin signals associated with SPI/SSP transfers: The SSPCLK, the SSPRXD data receive line, the SSPTXD data transfer line, SSPFSS (Chip Select in SPI mode, Frame Indicator in SSP mode).

The S5P4418 has three SPI/SSP port and it can operate in Master and Slave mode.

22.2 Features

- SPI Protocol, SSP Protocol, Microwire Protocol
- 16-bit wide, 8-location deep transmit/receive FIFO
- Master & Slave mode
- DMA request servicing of the transmit and receive FIFO
- Inform the system that a receive FIFO over-run has occurred
- Inform the system that data is present in the receive FIFO after an idle period has expired
- Programmable clock bit rate and prescale
- Only support DMA burst length 4
- Maximum SSP CLKGEN's frequency is 100 MHz
- SSP Receive Timeout Period: 64 cycle of SSP CLKGEN's clock
- Max Operation Frequency
  - Master Mode: 50 MHz (Receive Data is 20 MHz)
  - Slave Mode: 8 MHz

22.3 Block Diagram

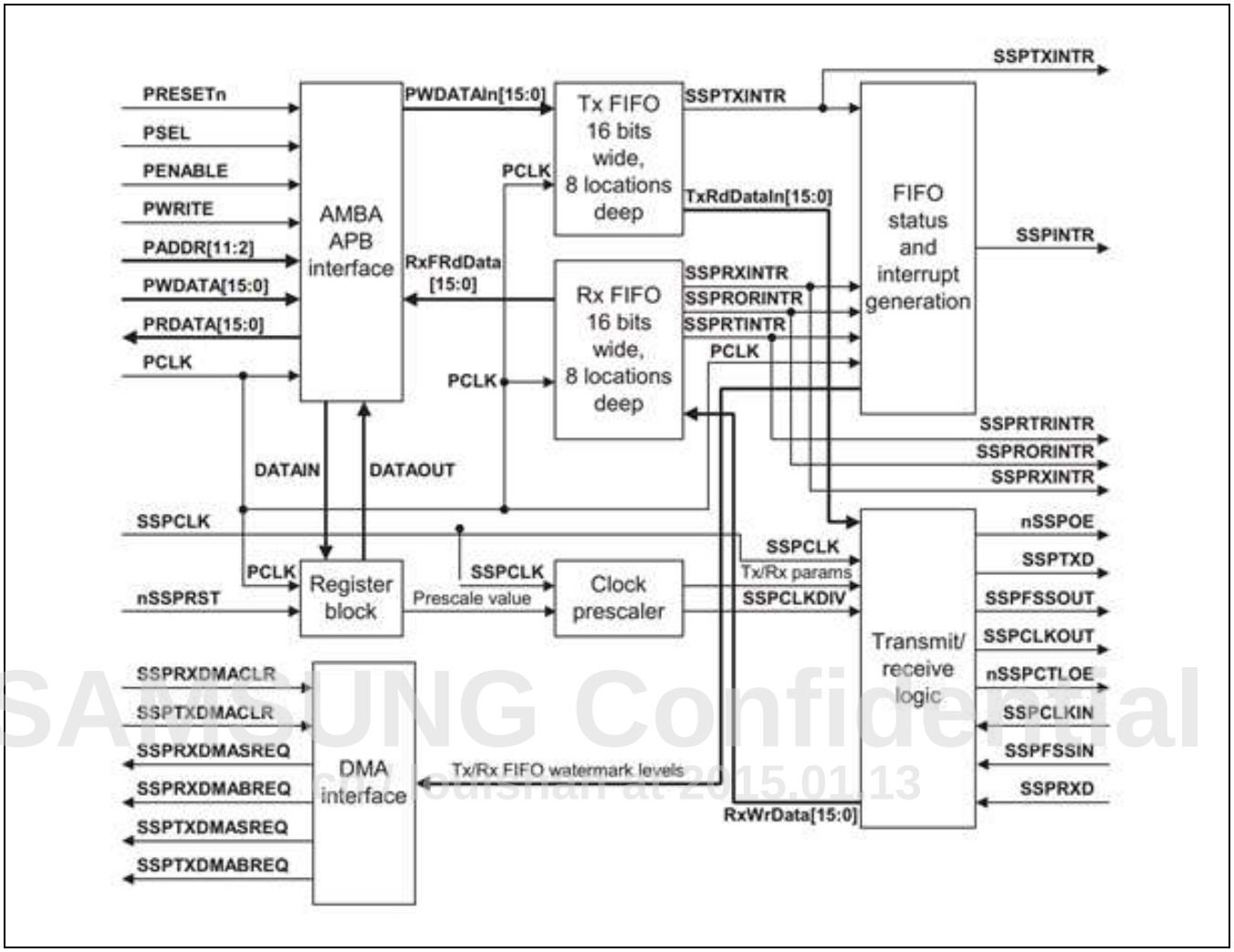


Figure 22-1 SPI/SSP Block Diagram

22.4 Functional Description

22.4.1 Clock Generation Configuration

SPI/SSP operates by using the PCLK and the SSPCLK. The PCLK is used when the CPU accesses the registers of the SPI/SSP. And, users can adjust the PCLK for the SPI/SSP by setting the PCLKMODE parameters according to their purpose. The PCLK is generated by Clock Generator of the SPI/SSP.

The SSPCLK is used when the SPI/SSP transmit or receive SPI/SSP Protocol. SSPCLK is generated by Clock Generator of the SPI/SSP. Each SPI/SSP has own Clock Generator. Therefore, users must set up the SPI/SSP Clock Generator before the SPI configuration stage.

22.4.2 Clock Ratios

There is a constraint on the ratio of the frequencies of PCLK to SSPCLK. The frequency of SSPCLK must be less than or equal to that of PCLK. This ensures that control signals from the SSPCLK domain to the PCLK domain are certain to get synchronized before one frame duration:

$F_{SSPCLK} <= F_{PCLK}.(F_{SSPCLK} <= 100\ MHz)$

In the slave mode of operation, the SSPCLKIN signal from the external master is double synchronized and then delayed to detect an edge. It takes three SSPCLKs to detect an edge on SSPCLKIN. SSPTXD has less setup time to the falling edge of SSPCLKIN on which the master is sampling the line. The setup and hold times on SSPRXD with reference to SSPCLKIN must be more conservative to ensure that it is at the right value when the actual sampling occurs within the SSPMS. To ensure correct device operation, SSPCLK must be at least 12 times faster than the maximum expected frequency of SSPCLKIN.

The frequency selected for SSPCLK must accommodate the desired range of bit clock rates. The ratio of minimum SSPCLK frequency to SSPCLKOUT maximum frequency in the case of the slave mode is 12 and for the master mode it is two.

To generate a maximum bit rate of 1.8432 Mbps in the Master mode, the frequency of SSPCLK must be at least 3.6864 MHz. With an SSPCLK frequency of 3.6864 MHz, the SSPCPSR register has to be programmed with a value of two and the SCR[7:0] field in the SSPCR0 register needs to be programmed as zero.

To work with a maximum bit rate of 1.8432 Mbps in the slave mode, the frequency of SSPCLK must be at least 22.12 MHz. With an SSPCLK frequency of 22.12 MHz, the SSPCPSR register can be programmed with a value of 12 and the SCR[7:0] field in the SSPCR0 register can be programmed as zero. Similarly the ratio of SSPCLK maximum frequency to SSPCLKOUT minimum frequency is 254 × 256.

The minimum frequency of SSPCLK is governed by the following equations, both of which have to be satisfied:

$F_{SSPCLK}(Min.) => 2 \times F_{SSPCLKOUT}(Max.)$ [for master mode]
$F_{SSPCLK}(Min.) => 12 \times F_{SSPCLKIN}(Max.)$ [for slave mode].

The maximum frequency of SSPCLK is governed by the following equations, both of which have to be satisfied:

$F_{SSPCLK}(Max.) <= 254 \times 256 \times F_{SSPCLKOUT}(Min.)$ [for master mode]
$F_{SSPCLK}(Max.) <= 254 \times 256 \times F_{SSPCLKIN}(Min.)$ [for slave mode]

22.4.2.1 Programming the Serial Clock Rate

SSPCR0 register is used to

- Program the serial clock rate
- Select one of the three protocols
- Select the data word size (where applicable)

SSPCPSR register is used to

- Program the serial clock prescale divisor

The serial bit rate is derived by dividing down the input clock SSPCLK. The clock is first divided by an even prescale value CPSDVSR from 2 to 254, which is programmed in SSPCPSR. The clock is further divided by a value from 1 to 256, which is 1 + SCR, where SCR is the value programmed in SSPCR0.

The frequency of the output signal bit clock SSPCLKOUT is defined below:

$$F_{SSPCLKOUT} = \frac{F_{SSPCLK}}{CPSDVR \times (1+SCR)}$$

For example, if SSPCLK is 3.6864 MHz, and CPSDVSR = 2, then SSPCLKOUT has a frequency range from 7.2 kHz to 1.8432 MHz.

22.4.3 Operation

The SPI/SSP Block transfers Serial Data from/to External device via FIFO in the SPI/SSP Block. The transfer operation is initiated by CPU, using the programmed I/O system or the DMA, to/from the system memory. The SPI/SSP Data transfer is performed in full duplex.

When the SPI/SSP sends Data to the PIO mode, the transfer operation is completed by Reading "Read FIFO" or Writing to "Write FIFO" by means of a program.

In the case of communication with DMA mode, For DMA transfer mode, user must set up the DMA configuration and set as "1" 'the SSPDMACR.TXDMAE bit and the SSPDMACR.RXDMAE bit in the SPI/SSP to enable the DMA transfer Request from SPI/SSP. RX Request occurs when Receive FIFO has 4 more than data, TX Request occurs when Transmit FIFO has 4 less than data. User can't adjust this configuration.

22.4.3.1 Transmit and Receive Operation

When configured as a master, the clock to the attached slaves is derived from a divided down version of SSPCLK through the prescaler operations described previously. The master transmit logic successively reads a value from its transmit FIFO and performs

Parallel to serial conversion on it. Then the serial data stream and frame control signal, synchronized to SSPCLKOUT, are output through the SSPTXD pin to the attached slaves. The master receive logic performs serial to parallel conversion on the incoming

Synchronous SSPRXD data stream, extracting and storing values into its receive FIFO, for subsequent reading through the APB interface.

NOTE: SSPRXD data is only valid when FSSPCLKOUT (Frequency of SSPCLKOUT) is lower than 20 MHz. This Constraint may be changed by exterior device's specification.

When configured as a slave, the SSPCLKIN clock is provided by an attached master and used to time its transmission and reception sequences. The slave transmit logic, under control of the master clock, successively reads a value from its transmit FIFO, performs parallel to serial conversion, then output the serial data stream and frame control signal through the slave SSPTXD pin. The slave receive logic performs serial to parallel conversion on the incoming SSPRXD data stream, extracting and storing values into its receive FIFO, for subsequent reading through the APB interface.

22.4.3.2 Reset Operation

The SPI/SSP is reset by the global reset signal PRESETn and a block-specific reset signal nSSPRST. An external reset controller must use PRESETn to assert nSSPRST asynchronously and negate it synchronously to SSPCLK. PRESETn must be asserted LOW for a period long enough to reset the slowest block in the on-chip system, and then taken HIGH again. The SPI/SSP requires PRESETn to be asserted LOW for at least one period of PCLK.

In S5P4418, PRESETn and nSSPRST is controlled by Reset Controller. User can set up SPI/SSP reset signals by CPU.

22.4.3.3 Interrupts

There are 4 maskable interrupts generated in the SPI/SSP. These are combined to produce one interrupt outputs.

- Receive overrun interrupt
- Receive timeout interrupt
- Receive FIFO interrupt (half full)
- Transmit FIFO interrupt (half empty)

22.4.4 Frame Format

Each data frame is between 4 and 16 bits long depending on the size of data programmed, and is transmitted starting with the MSB. There are three basic frame types that can be selected:

- Texas Instruments synchronous serial
- Motorola SPI
- National Semiconductor Microwire.

For all three formats, the serial clock (SSPCLKOUT) is held inactive while the SPI/SSP is idle, and transitions at the programmed frequency only during active transmission or reception of data. The idle state of SSPCLKOUT is utilized to provide a receive timeout indication that occurs when the receive FIFO still contains data after a timeout period.

For Motorola SPI and National Semiconductor Microwire frame formats, the serial frame (SSPFSSOUT) pin is active LOW, and is asserted (pulled down) during the entire transmission of the frame.

For Texas Instruments synchronous serial frame format, the SSPFSSOUT pin is pulsed for one serial clock period starting at its rising edge, prior to the transmission of each frame. For this frame format, both the SPI/SSP and the off-chip slave device drive their output data on the rising edge of SSPCLKOUT, and latch data from the other device on the falling edge.

Unlike the full-duplex transmission of the other two frame formats, the National Semiconductor Microwire format uses a special master-slave messaging technique, which operates at half-duplex. In this mode, when a frame begins, an 8-bit control message is transmitted to the off-chip slave. During this transmit, no incoming data is received by the SSP. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the requested data. The returned data can be 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

22.4.4.1 Texas Instruments Synchronous Serial Frame Format

Figure 22-2 shows the Texas Instruments synchronous serial frame format for a single transmitted frame.

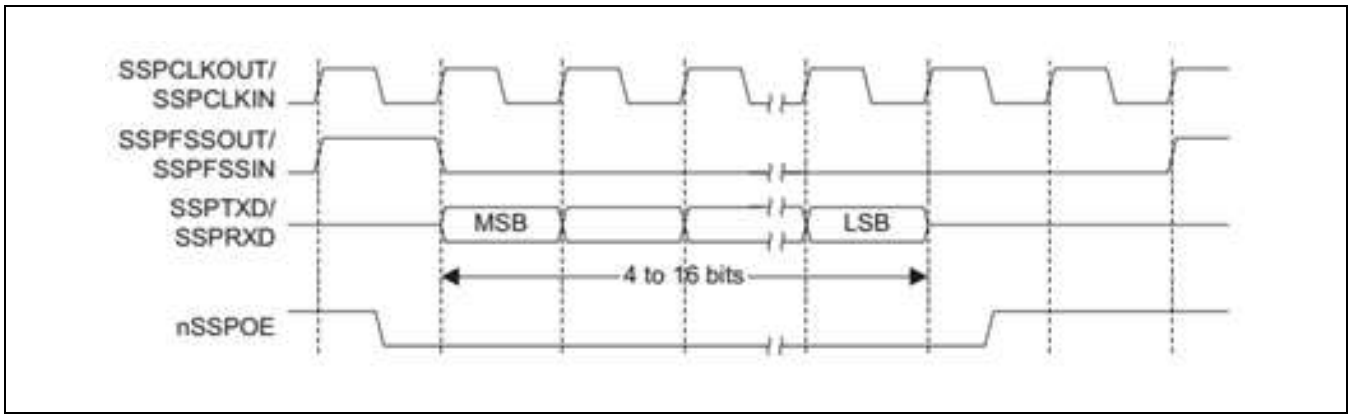


Figure 22-2 Texas Instruments Synchronous Serial Frame Format (Single Transfer)

In this mode, SSPCLKOUT and SSPFSSOUT are forced LOW, and the transmit data line SSPTXD is tri-stated whenever the SPI/SSP is idle. Once the bottom entry of the transmit FIFO contains data, SSPFSSOUT is pulsed HIGH for one SSPCLKOUT period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the transmit logic. On the next rising edge of SSPCLKOUT, the MSB of the 4 to 16-bit data frame is shifted out on the SSPTXD pin. Likewise, the MSB of the received data is shifted onto the SSPRXD pin by the off-chip serial slave device.

Both the SPI/SSP and the off-chip serial slave device then clock each data bit into their serial shifter on the falling edge of each SSPCLKOUT. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of SSPCLKOUT after the LSB has been latched.

Figure 22-3 shows the Texas Instruments synchronous serial frame format when back-to-back frames are transmitted.

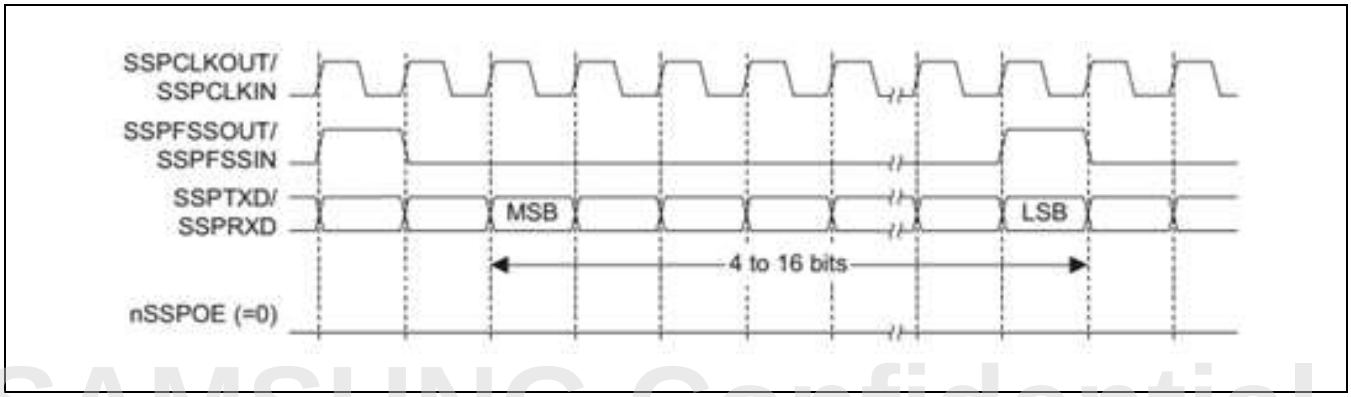


Figure 22-3 TI Synchronous Serial Frame Format (Continuous Transfer)

22.4.4.2 Motorola SPI Frame Format

The Motorola SPI interface is a four-wire interface where the SSPFSSOUT signal behaves as a slave select. The main feature of the Motorola SPI format is that the inactive state and phase of the SSPCLKOUT signal are programmable through the SPO and SPH bits within the SSPSCR0 control register.

SPO, clock polarity

When the SPO clock polarity control bit is LOW, it produces a steady state low value on the SSPCLKOUT pin. If the SPO clock polarity control bit is HIGH, a steady state high value is placed on the SSPCLKOUT pin when data is not being transferred.

SPH, clock phase

The SPH control bit selects the clock edge that captures data and allows it to change state. It has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge.

When the SPH phase control bit is LOW, data is captured on the first clock edge transition. If the SPH clock phase control bit is HIGH, data is captured on the second clock edge transition.

22.4.4.3 Motorola SPI Format with SPO = 0, SPH = 0

Single and continuous transmission signal sequences for Motorola SPI format with SPO = 0, SPH = 0 are shown in *Figure 22-4* and *Figure 22-5*.

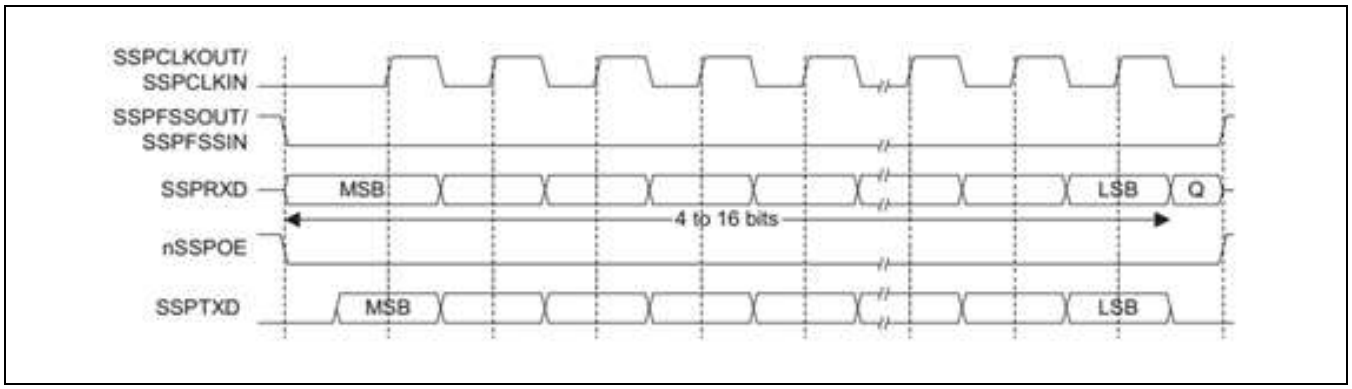


Figure 22-4 Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 0

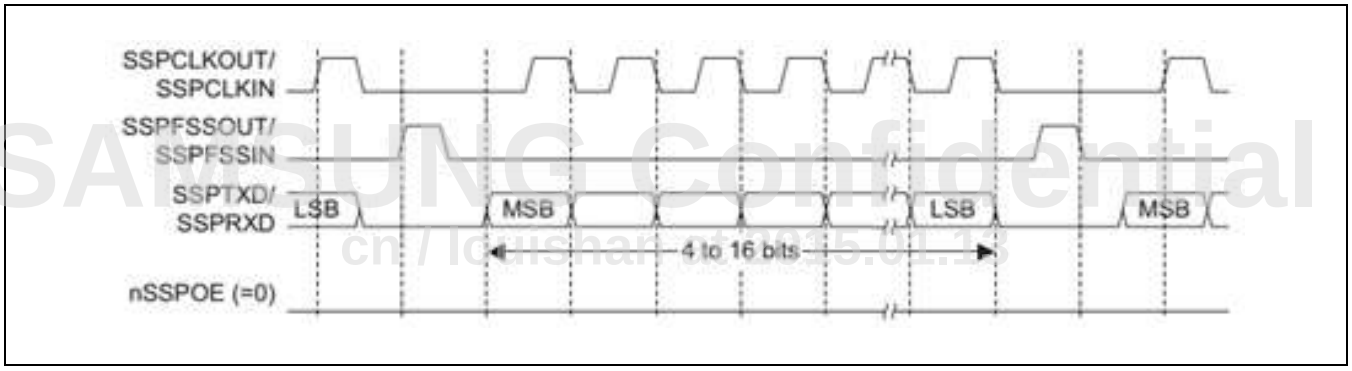


Figure 22-5 Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 0

In this configuration, during idle periods:

- The SSPCLKOUT signal is forced LOW
- SSPFSSOUT is forced HIGH
- The transmit data line SSPTXD is arbitrarily forced LOW

If the SPI/SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW. This causes slave data to be enabled onto the SSPRXD input line of the master. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad.

One half SSPCLKOUT period later, valid master data is transferred to the SSPTXD pin. Now that both the master and slave data have been set, the SSPCLKOUT master clock pin goes HIGH after one further half SSPCLKOUT period.

The data is now captured on the rising and propagated on the falling edges of the SSPCLKOUT signal.

In the case of a single word transmission, after all bits of the data word have been transferred, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSPFSSOUT signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the SPH bit is logic zero. Therefore the master device must raise the SSPFSSIN pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSPFSSOUT pin is returned to its idle state one SSPCLKOUT period after the last bit has been captured.

22.4.4.4 Motorola SPI Format with SPO = 0, SPH = 1

The transfer signal sequence for Motorola SPI format with SPO = 0, SPH = 1 is shown in *Figure 22-6*, which covers both single and continuous transfers.

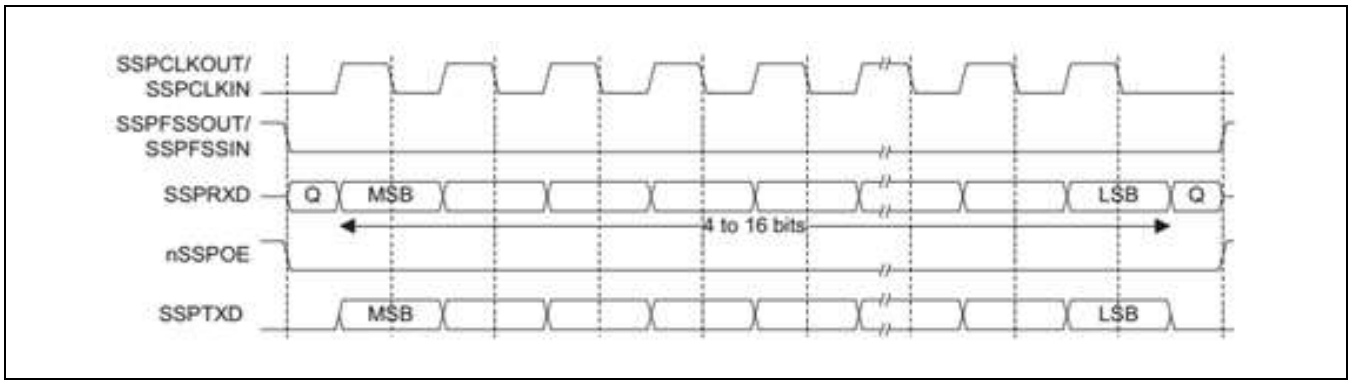


Figure 22-6 Motorola SPI Frame Format with SPO = 0 and SPH = 1

In this configuration, during idle periods:

- The SSPCLKOUT signal is forced LOW
- SSPFSSOUT is forced HIGH
- The transmit data line SSPTXD is arbitrarily forced LOW

If the SPI/SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad. After a further one half SSPCLKOUT period, both master and slave valid data is enabled onto their respective transmission lines. At the same time, the SSPCLKOUT is enabled with a rising edge transition.

Data is then captured on the falling edges and propagated on the rising edges of the SSPCLKOUT signal.

In the case of a single word transfer, after all bits have been transferred, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

For continuous back-to-back transfers, the SSPFSSOUT pin is held LOW between successive data words and termination is the same as that of the single word transfer.

22.4.4.5 Motorola SPI Format with SPO = 1, SPH = 0

Single and continuous transmission signal sequences for Motorola SPI format with SPO = 1, SPH = 0 are shown in Figure 22-7 and *Figure 22-8*.

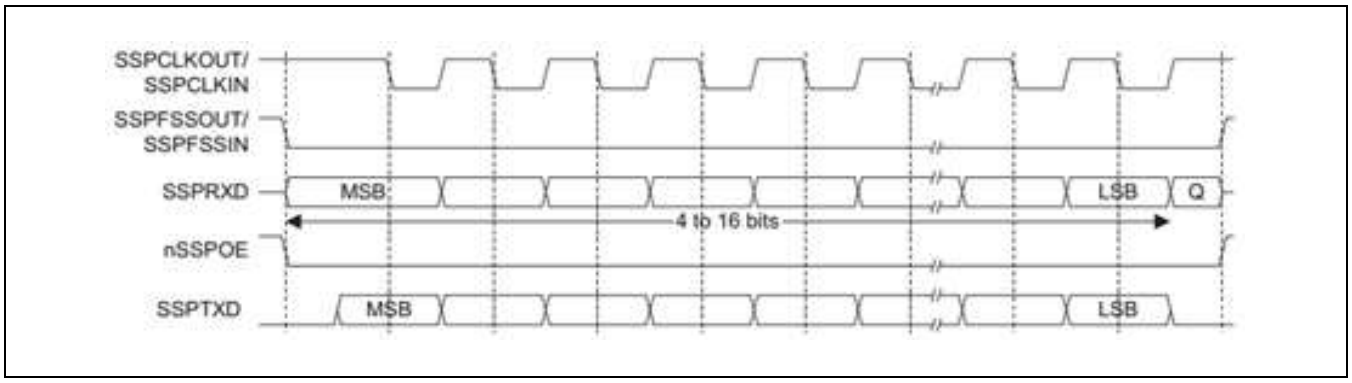


Figure 22-7 Motorola SPI Frame Format (Single Transfer) with SPO = 1 and SPH = 0

NOTE: In *Figure 22-7*, Q is an undefined signal

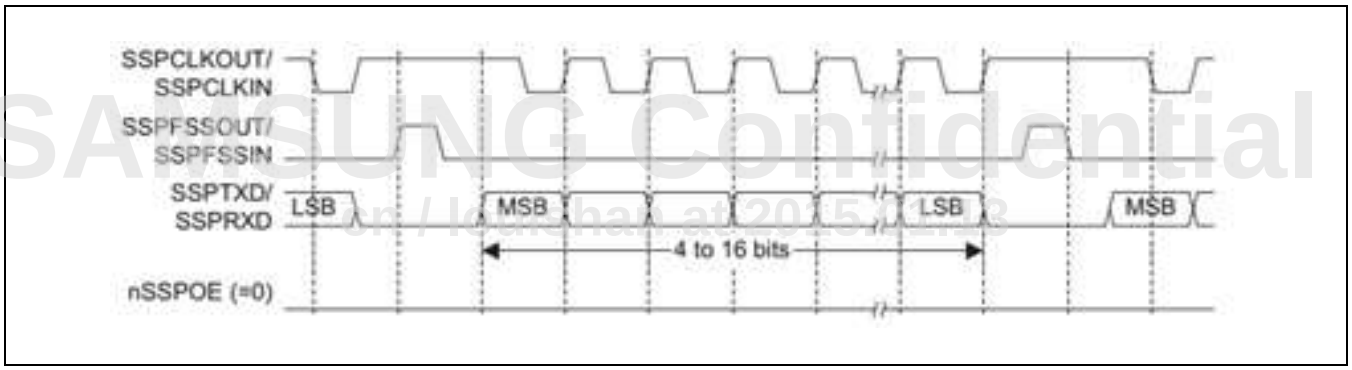


Figure 22-8 Motorola SPI Frame Format (Continuous Transfer) with SPO = 1 and SPH = 0

In this configuration, during idle periods:

- The SSPCLKOUT signal is forced HIGH
- SSPFSSOUT is forced HIGH
- The transmit data line SSPTXD is arbitrarily forced LOW

If the SPI/SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW, which causes slave data to be immediately transferred onto the SSPRXD line of the master. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad.

One half period later, valid master data is transferred to the SSPTXD line. Now that both the master and slave data have been set, the SSPCLKOUT master clock pin becomes LOW after one further half SSPCLKOUT period. This means that data is captured on the falling edges and be propagated on the rising edges of the SSPCLKOUT signal.

In the case of a single word transmission, after all bits of the data word are transferred, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSPFSSOUT signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the SPH bit is logic zero. Therefore the master device must raise the SSPFSSIN pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSPFSSOUT pin is returned to its idle state one SSPCLKOUT period after the last bit has been captured.

22.4.4.6 Motorola SPI Format with SPO = 1, SPH = 1

The transfer signal sequence for Motorola SPI format with SPO = 1, SPH = 1 is shown in *Figure 22-9*, which covers both single and continuous transfers.

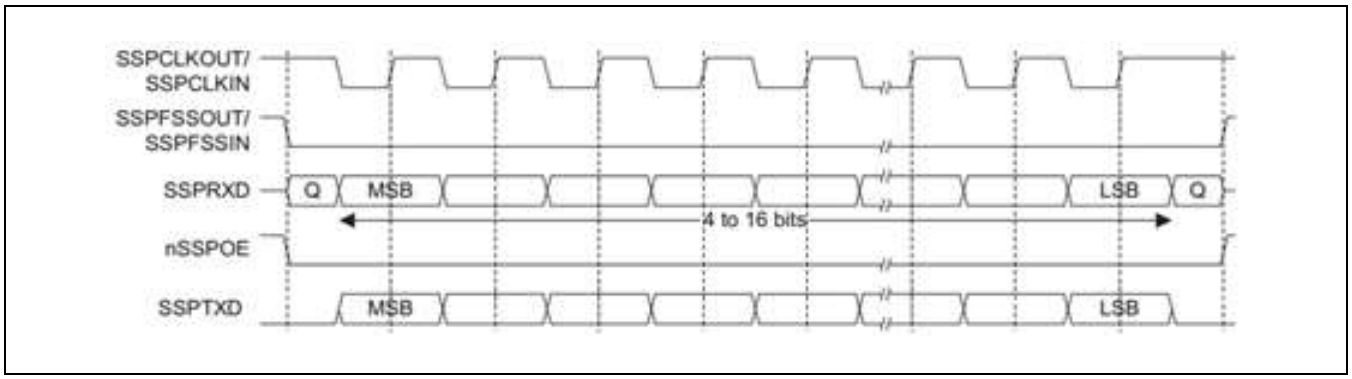


Figure 22-9 Motorola SPI Frame Format with SPO = 1 and SPH = 1

NOTE: In *Figure 22-9*, Q is an undefined signal

In this configuration, during idle periods:

- The SSPCLKOUT signal is forced HIGH
- SSPFSSOUT is forced HIGH
- The transmit data line SSPTXD is arbitrarily forced LOW

If the SPI/SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the SSPFSSOUT master signal being driven LOW. The nSSPOE line is driven LOW, enabling the master SSPTXD output pad. After a further one half SSPCLKOUT period, both master and slave data are enabled onto their respective transmission lines. At the same time, the SSPCLKOUT is enabled with a falling edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SSPCLKOUT signal.

After all bits have been transferred, in the case of a single word transmission, the SSPFSSOUT line is returned to its idle HIGH state one SSPCLKOUT period after the last bit has been captured.

For continuous back-to-back transmissions, the SSPFSSOUT pins remains in its active LOW state, until the final bit of the last word has been captured, and then returns to its idle state as described above.

For continuous back-to-back transfers, the SSPFSSOUT pin is held LOW between successive data words and termination is the same as that of the single word transfer.

22.4.4.7 National Semiconductor Microwire Frame Format

Figure 22-10 shows the National Semiconductor Microwire frame format, again for a single frame. *Figure 22-11* shows the same format when back to back frames are transmitted.

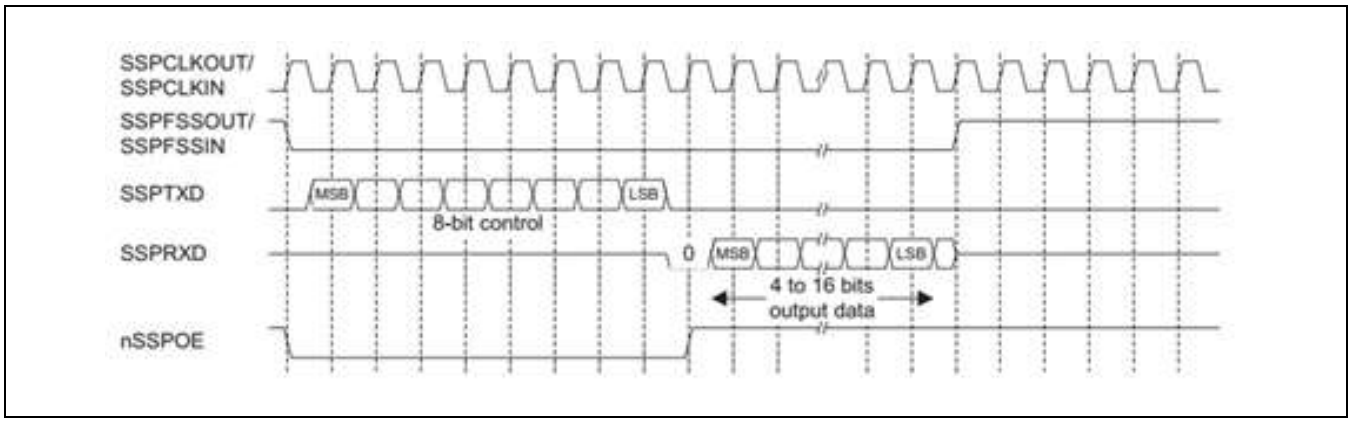


Figure 22-10 Microwire frame format (single transfer)

Microwire format is very similar to SPI format, except that transmission is half-duplex instead of full-duplex, using a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SPI/SSP to the off-chip slave device. During this transmission, no incoming data is received by the SPI/SSP. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the required data. The returned data is 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

In this configuration, during idle periods:

- The SSPCLKOUT signal is forced LOW
- SSPFSSOUT is forced HIGH
- The transmit data line SSPTXD is arbitrarily forced LOW

A transmission is triggered by writing a control byte to the transmit FIFO. The falling edge of SSPFSSOUT causes the value contained in the bottom entry of the transmit FIFO to be transferred to the serial shift register of the transmit logic, and the MSB of the 8-bit control frame to be shifted out onto the SSPTXD pin. SSPFSSOUT remains LOW for the duration of the frame transmission. The SSPRXD pin remains tri-stated during this transmission.

The off-chip serial slave device latches each control bit into its serial shifter on the rising edge of each SSPCLKOUT. After the last bit is latched by the slave device, the control byte is decoded during a one clock wait-state, and the slave responds by transmitting data back to the SPI/SSP. Each bit is driven onto SSPRXD line on the falling edge of SSPCLKOUT. The SPI/SSP in turn latches each bit on the rising edge of SSPCLKOUT. At the end of the frame, for single transfers, the SSPFSSOUT signal is pulled HIGH one clock period after the last bit has been latched in the receive serial shifter, that causes the data to be transferred to the receive FIFO.

NOTE: The off-chip slave device can tri-state the receive line either on the falling edge of SSPCLKOUT after the LSB has been latched by the receive shifter, or when the SSPFSSOUT pin goes HIGH.

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the SSPFSSOUT line is continuously asserted (held LOW) and transmission of data occurs back to back. The control byte of the next frame follows directly after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge SSPCLKOUT, after the LSB of the frame has been latched into the SPI/SSP.

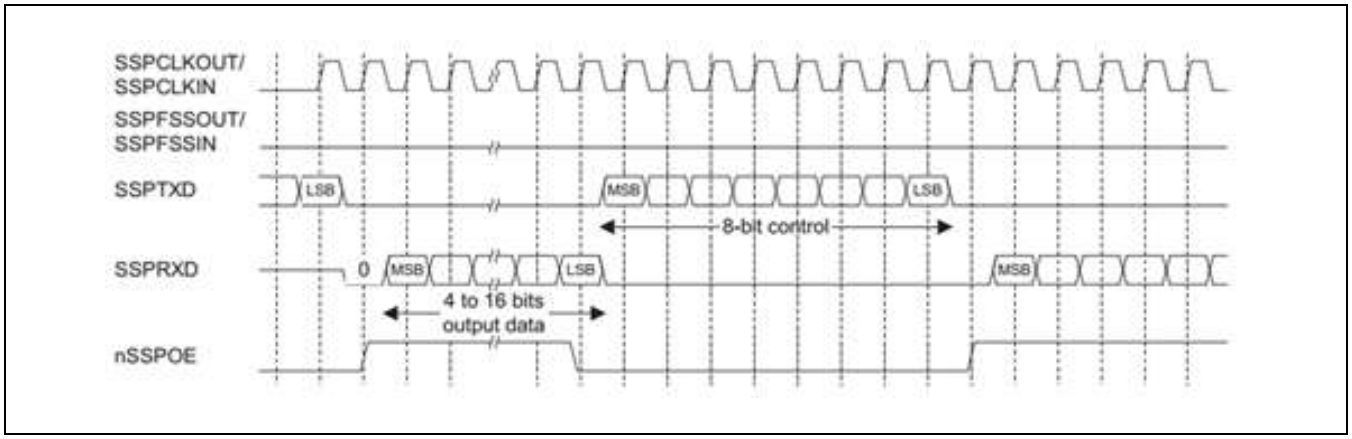


Figure 22-11 Microwire Frame Format (Continuous Transfers)

Setup and hold time requirements on SSPFSSIN with respect to SSPCLKIN in Microwire mode

In the Microwire mode, the SPI/SSP slave samples the first bit of receive data on the rising edge of SSPCLKIN after SSPFSSIN has gone LOW. Masters that drive a free-running SSPCKLIN must ensure that the SSPFSSIN signal has sufficient setup and hold margins with respect to the rising edge of SSPCLKIN.

Figure 22-12 illustrates these setup and hold time requirements. With respect to the SSPCLKIN rising edge on which the first bit of receive data is to be sampled by the SPI/SSP slave, SSPFSSIN must have a setup of at least two times the period of SSPCLKIN on which the SPI/SSP operates. With respect to the SSPCLKIN rising edge previous to this edge, SSPFSSIN must have a hold of at least one SSPCLKIN period.

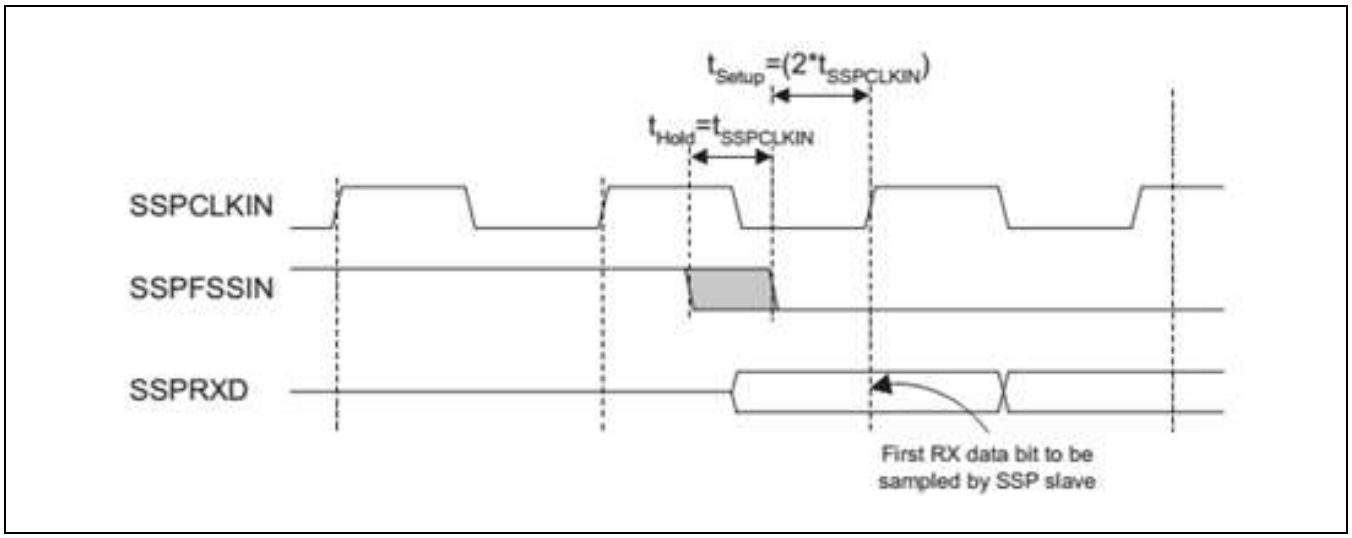


Figure 22-12 Microwire Frame Format, SSPFSSIN Input Setup and Hold Requirements

22.5 Register Description

22.5.1 Register Map Summary

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)

Register	Offset	Description	Reset Value
SSPCR0	0x00h 0x00h 0x00h	SPI/SSP control register 0	0x0000_0000
SSPCR1	0x04h 0x04h 0x04h	SPI/SSP control register 1	0x0000_0000
SSPDR	0x08h 0x08h 0x08h	SPI/SSP data register	0x0000_
SSPSR	0x0Ch 0x0Ch 0x0Ch	SPI/SSP status register	0x0000_0003
SSPCPSR	0x10h 0x10h 0x10h	SPI/SSP clock prescaler register	0x0000_0000
SSPIMSC	0x14h 0x14h 0x14h	SPI/SSP interrupt mask set or clear register	0x0000_0000
SSPRIS	0x18h 0x18h 0x18h	SPI/SSP raw interrupt status register	0x0000_0000
SSPMIS	0x1Ch 0x1Ch 0x1Ch	SPI/SSP masked interrupt status register	0x0000_0000
SSPICR	0x20h 0x20h 0x20h	SPI/SSP interrupt clear register	0x0000_
SSPDMACR	0x24h 0x24h 0x24h	SPI/SSP DMA control register	0x0000_0000

22.5.1.1 SSPCR0

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x00h, 0x00h, 0x00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
SCR	[15:8]	RW	Serial clock rate. The value SCR is used to generate the transmit and receive bit rate of + the SPI/SSP. The bit rate is where CPSDVSR is an even value from 2 to 254, programmed through the SSPCPSR register and SCR is a value from 0 to 255.	8'b0
SPH	[7]	RW	SSPCLKOUT phase (applicable to Motorola SPI frame format only)	1'b0
SPO	[6]	RW	SSPCLKOUT polarity (applicable to Motorola SPI frame format only)	1'b0
FRF	[5:4]	RW	Frame format: 0 = Motorola SPI frame format 1 = TI synchronous serial frame format 2 = National Microwire frame format 3 = Reserved, undefined operation	1'b0
DSS	[3:0]	RW	Data Size Select 0 to 2 = Reserved, undefined operation 3 = 4-bit data 4 = 5-bit data 5 = 6-bit data 6 = 7-bit data 7 = 8-bit data 8 = 9-bit data 9 = 10-bit data 10 = 11-bit data 11 = 12-bit data 12 = 13-bit data 13 = 14-bit data 14 = 15-bit data 15 = 16-bit data	1'b0

22.5.1.2 SSPCR1

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x04h, 0x04h, 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
SOD	[3]	RW	Slave-mode output disable. This bit is relevant only in the slave mode (MS = 1). In multiple-slave systems, it is possible for an SPI/SSP master to broadcast a message to all slaves in the system while ensuring that only one slave drives data onto its serial output line. In such systems the RXD lines from multiple slaves could be tied together. To operate in such systems, the SOD bit can be set if the SPI/SSP slave is not supposed to drive the SSPTXD line. 0 = SSP can drive the SSPTXD output in slave mode. 1 = SSP must not drive the SSPTXD output in slave mode.	1'b0
MS	[2]	RW	Master or slave mode select. This bit can be modified only when the SPI/SSP is disabled (SSE = 0): 0 = Device configured as master (default) 1 = Device configured as slave.	1'b0
SSE	[1]	RW	Synchronous serial port enable: 0 = SSP operation disabled 1 = SSP operation enabled.	1'b0
LBM	[0]	RW	Loop back mode: 0 = Normal serial port operation enabled 1 = Output of transmit serial shifter is connected to input of receive serial shifter internally.	1'b0

22.5.1.3 SSPDR

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x08h, 0x08h, 0x08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
DATA	[15:0]	RW	Transmit/Receive FIFO: Read: Receive FIFO Write: Transmit FIFO. You must right-justify data when the SPI/SSP is programmed for a data size that is less than 16 bits. Unused bits at the top are ignored by transmit logic. The receive logic automatically right-justifies.	16'b0

22.5.1.4 SSPSR

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x0Ch, 0x0Ch, 0x0Ch, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
RSVD	[31:5]	R	Reserved	27'b0
BSY	[4]	R	SPI/SSP busy flag (read-only): 0 = SSP is idle 1 = SSP is currently transmitting and/or receiving a frame or the transmit FIFO is not empty.	1'b0
RFF	[3]	R	Receive FIFO full (read-only): 0 = Receive FIFO is not full 1 = Receive FIFO is full.	1'b0
RNE	[2]	R	Receive FIFO not empty (read-only): 0 = Receive FIFO is empty 1 = Receive FIFO is not empty.	1'b0
TNF	[1]	R	Transmit FIFO not full (read-only): 0 = Transmit FIFO is full 1 = Transmit FIFO is not full.	1'b1
TFE	[0]	R	Transmit FIFO empty (read-only): 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty.	1'b1

22.5.1.5 SSPCPSR

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x10h, 0x10h, 0x10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
CPSDVSR	[7:0]	RW	Clock prescale divisor. Must be an even number from 2 to 254, depending on the frequency of SSPCLK. The least significant bit always returns zero on reads	8'b0

22.5.1.6 SSPIMSC

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x14h, 0x14h, 0x14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
TXIM	[3]	RW	Transmit FIFO interrupt mask: 0 = Tx FIFO half empty or less condition interrupt is masked 1 = Tx FIFO half empty or less condition interrupt is not masked.	1'b0
RXIM	[2]	RW	Receive FIFO interrupt mask: 0 = Rx FIFO half full or less condition interrupt is masked 1 = Rx FIFO half full or less condition interrupt is not masked.	1'b0
RTIM	[1]	RW	Receive timeout interrupt mask: 0 = RxFIFO not empty and no read prior to timeout period interrupt is masked 1 = RxFIFO not empty and no read prior to timeout period interrupt is not masked.	1'b0
RORIM	[0]	RW	Receive overrun interrupt mask: 0 = RxFIFO written to while full condition interrupt is masked 1 = RxFIFO written to while full condition interrupt is not masked.	1'b0

22.5.1.7 SSPRIS

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x18h, 0x18h, 0x18h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
TXRIS	[3]	R	Gives the raw interrupt state (prior to masking) of the SSPTXINTR interrupt	1'b0
RXRIS	[2]	R	Gives the raw interrupt state (prior to masking) of the SSPRXINTR interrupt	1'b0
RTRIS	[1]	R	Gives the raw interrupt state (prior to masking) of the SSPRTINTR interrupt	1'b0
RORRIS	[0]	R	Gives the raw interrupt state (prior to masking) of the SSPRORINTR interrupt	1'b0

22.5.1.8 SSPMIS

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x1Ch, 0x1Ch, 0x1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
TXMIS	[3]	R	Gives the transmit FIFO masked interrupt state (after masking) of the SSPTXINTR Interrupt	1'b0
RXMIS	[2]	R	Gives the receive FIFO masked interrupt state (after masking) of the SSPRXINTR interrupt	1'b0
RTMIS	[1]	R	Gives the receive timeout masked interrupt state (after masking) of the SSPRTINTR Interrupt	1'b0
RORMIS	[0]	R	Gives the receive over run masked interrupt status (after masking) of the SSPRORINTR Interrupt	1'b0

22.5.1.9 SSPICR

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x20h, 0x20h, 0x20h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved	30'b0
RTIC	[1]	W	Clears the SSPRTINTR interrupt	-
RORIC	[0]	W	Clears the SSPRORINTR interrupt	-

22.5.1.10 SSPDMACR

- Base Address: C005_B000h (SPISSP0)
- Base Address: C005_C000h (SPISSP1)
- Base Address: C005_F000h (SPISSP2)
- Address = Base Address + 0x24h, 0x24h, 0x24h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved	30'b0
TXDMAE	[1]	RW	If this bit is set to 1, DMA for the transmit FIFO is enabled	1'b0
RXDMAE	[0]	RW	If this bit is set to 1, DMA for the receive FIFO is enabled	1'b0

23 MPEG-TS Interface

23.1 Overview

The MPEG I/F block receives the output of the MPEG transport decoder chip and then Store the transmitted data the Main Memory using the Fast-DMA of the S5P4418.

23.2 Features

- Supports 1-bit/8-bit Modes
- Supports External/Internal DMA
- Supports AES/CAS Encoding & Decoding
- Supports 2 channel MPEG TS interface input
- Supports 1 channel MPEG TS interface output

23.3 Functional Description

23.3.1 Timing

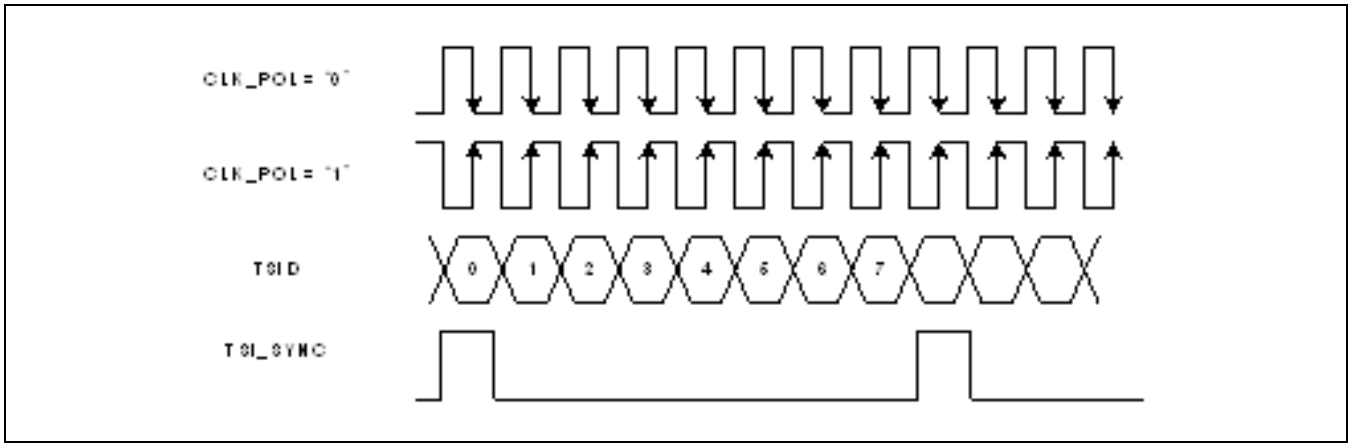


Figure 23-1 Basic Transfer Timing Diagram

Figure 23-1 shows the timing chart in which the S5P4418 reads data when an external device sends data via the MPEG TS interface. If the external device sends data on the rising edge, the S5P4418 actually reads the data on the falling edge

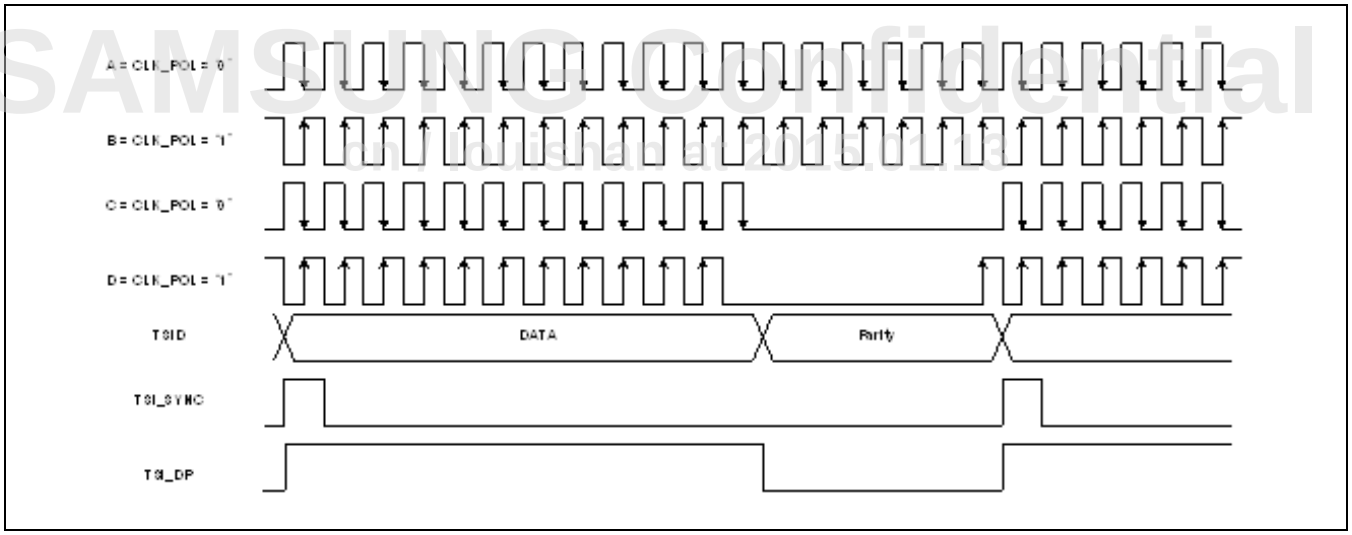


Figure 23-2 MPEG TS Timing at Serial Mode

External devices can provide clocks as well as MPEG TS timing. *Figure 23-2* shows the types of clock that can be provided by external devices. The clock types are determined by the point at which the external devices output data.

- A type devices output data on the rising edge. The value of the CAP_CTRL.CAP_CLK_POL bit is "0", and the MPEG TSP reads data on the point of the falling edge as above described.
- B type devices output data on the falling edge. The value of the CAP_CTRL.CAP_CLK_POL bit is "1".
- C type Devices very similar to the A type device are used. The point of difference from an A type device is that these devices do not check Parity.
- D type Devices very similar to the B type device are used. The point of difference from a B type device is that these devices do not check Parity.

If the value of TSI_DP is "1", the value indicates Data. If the value is "0", the value indicates Parity. However, the value may have the opposite meaning depending on device properties. In this case, its polarity can be changed by setting the MPEGIFCONT.DP_POL bit as "1".

23.4 Register Description

23.4.1 Register Map Summary

- Base Address: C005_D000h

Register	Offset	Description	Reset Value
CAP_CTRL0	0x00h	MPEG TSP Capture 0 Control Register 0	0x0000_0000
CAP_CTRL1	0x04h	MPEG TSP Capture 1 Control Register 0	0x0000_0000
CAP_WR_PID_VAL	0x08h	MPEG TSP Write PID Value Register	0x0000_0000
CAP_WR_PID_ADDR	0x0Ch	MPEG TSP Write PID Address Register	0x0000_0000
CAP0_CAPDATA	0x10h	MPEG TSP Capture 0 Capture Data	0x0000_0000
CAP1_CAPDATA	0x14h	MPEG TSP Capture 1 Capture Data	0x0000_0000
CORE_TRDATA	0x1Ch	MPEG TSP Transfer Data	0x0000_0000
CORE_CTRL	0x20h	MPEG TSP Core Control Register	0x0000_0000
IDMA_STATUS	0x24h	MPEG TSP IDMA Status Register	0x0000_0000
IDMA_CON	0x28h	MPEG TSP IDMA Control Register	0x0000_0000
IDMA_INT	0x2Ch	MPEG TSP IDMA Interrupt Register	0x0000_0000
IDMA0_ADDR	0x30h	MPEG TSP Internal DMA0 Base Address Register	0x0000_0000
IDMA1_ADDR	0x34h	MPEG TSP Internal DMA1 Base Address Register	0x0000_0000
IDMA2_AD	0x38h	MPEG TSP Internal DMA2 Base Address Register	0x0000_0000
IDMA3_ADDR	0x3Ch	MPEG TSP Internal DMA3 Base Address Register	0x0000_0000
IDMA0_LEN	0x40h	MPEG TSP Internal DMA0 Data Length Register	0x0000_0000
IDMA1_LEN	0x44h	MPEG TSP Internal DMA1 Data Length Register	0x0000_0000
IDMA2_LEN	0x48h	MPEG TSP Internal DMA2 Data Length Register	0x0000_0000
IDMA3_LEN	0x4Ch	MPEG TSP Internal DMA3 Data Length Register	0x0000_0000

23.4.1.1 CAP_CTRL0

- Base Address: C005_D000h
- Address = Base Address + 0x00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CAP0_DATA_DUMP_ENABLE	[31]	RW	MPEG TSI Data dump enable 0 = Dump only matched data 1 = Dump all input data	1'b0
RSVD	[30:28]	–	Reserved	3'b0
cap0_lock_int_pend	[27]	RW	MPEG TS Interface capture 0 interrupt pending R: 0 = Interrupt not pended 1 = Interrupt pended W: 0 = Not work 1 = Interrupt clear	1'b0
cap0_lock_INT_mask	[26]	RW	MPEG TS Interface capture 0 interrupt mask 0 = Interrupt masking enabled 1 = Interrupt masking disabled	1'b0
cap0_lock_int_enb	[25]	RW	MPEG TS Interface capture 0 interrupt enabled 0 = Interrupt disabled 1 = Interrupt enabled	1'b0
cap0_lock_mode	[24]	RW	MPEG TS Interface capture 0 lock mode 0 = Unlock (Header not detect) 1 = lock (Header detect)	1'b0
RSVD	[23:10]	–	Reserved	24'b0
cap0_sram_pwr_enb	[9]	RW	MPEG TS Interface capture 0 SRAM power enable 0 = Power disabled 1 = Power enabled	1'b0
cap0_sram_sleep	[8]	RW	MPEG TS Interface capture 0 SRAM sleep mode 0 = Sleep 1 = Awake	1'b0
cap0_err_pol	[7]	RW	MPEG TS Interface capture 0 ERR polling mode 0 = Neg-edge capture 1 = Pos-edge capture	1'b0
cap0_sync_pol	[6]	RW	MPEG TS Interface capture 0 SYNC polling mode 0 = Neg-edge capture 1 = Pos-edge capture	1'b0
cap0_dp_pol	[5]	RW	MPEG TS Interface capture 0 DP polling mode 0 = Neg-edge capture 1 = Pos-edge capture	1'b0
cap0_clk_pol	[4]	RW	MPEG TS Interface capture 0 CLK polling mode 0 = Neg-edge capture 1 = Pos-edge capture	1'b0

Name	Bit	Type	Description	Reset Value
RSVD	[3:2]	–	Reserved	2'b0
cap0_cap_mode	[1]	RW	MPEG TS Interface capture 0 capture mode 0 = Byte mode 1 = Serial Mode	1'b0
cap0_cap_enb	[0]	RW	MPEG TS Interface capture 0 capture enable 0 = Disable 1 = Enable	1'b0

23.4.1.2 CAP_CTRL1

- Base Address: C005_D000h
- Address = Base Address + 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CAP1_DATA_DUMP_ENABLE	[31]	RW	MPEG TSI Data dump enable 0 = Dump only matched data 1 = Dump all input data	1'b0
RSVD	[30:28]	–	Reserved	3'b0
cap1_lock_int_pend	[27]	R	MPEG TS Interface capture 1 interrupt pending R: 0 = Interrupt not pended 1 = Interrupt pended W: 0 = Not work 1 = Interrupt clear	1'b0
cap1_lock_INT_mask	[26]	RW	MPEG TS Interface capture 1 interrupt mask 0 = Interrupt masking enabled 1 = Interrupt masking disabled	1'b0
cap1_lock_int_enb	[25]	RW	MPEG TS Interface capture 1 interrupt enabled 0 = Interrupt disabled 1 = Interrupt enabled	1'b0
cap1_lock_mode	[24]	RW	MPEG TS Interface capture 1 lock mode 0 = Unlock (Header not detect) 1 = lock (Header detect)	1'b0
RSVD	[23:18]	–	Reserved	24'b0
CAP1_OUTCLK_POL	[17]	RW	MPEG TS Interface capture 1 output CLK polling mode 0 = neg-edge capture 1 = pos-edge capture	1'b0
CAP1_OUTENB	[16]	RW	MPEG TS Interface capture 1 direction 0 = Input 1 = Output	1'b0
RSVD	[15:10]	–	Reserved	24'b0
cap1_sram_pwr	[9]	RW	MPEG TS Interface capture 1 SRAM power enable 0 = Power disabled 1 = Power enabled	1'b0
cap1_sram_sleep	[8]	RW	MPEG TS Interface capture 1 SRAM sleep mode 0 = Sleep 1 = Awake	1'b0
cap1_err_pol	[7]	RW	MPEG TS Interface capture 1 ERR polling mode 0 = Active low 1 = Active high	1'b0
cap1_sync_pol	[6]	RW	MPEG TS Interface capture 1 SYNC polling mode 0 = Active low	1'b0

Name	Bit	Type	Description	Reset Value
			1 = Active high	
cap1_dp_pol	[5]	RW	MPEG TS Interface capture 1 DP polling mode 0 = Active low 1 = Active high	1'b0
cap1_clk_pol	[4]	RW	MPEG TS Interface capture 1 CLK polling mode 0 = neg-edge capture 1 = pos-edge capture	1'b0
RSVD	[3:2]	–	Reserved	2'b0
cap1_cap_mode	[1]	RW	MPEG TS Interface capture 1 capture mode 0 = Byte mode 1 = Serial Mode	1'b0
cap1_cap_enb	[0]	RW	MPEG TS Interface capture 1 capture enable 0 = Disable 1 = Enable	1'b0

23.4.1.3 CAP_WR_PID_VAL

- Base Address: C005_D000h
- Address = Base Address + 0x08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PID_VALUE	[31:0]	RW	MPEG TSP PID value	32'b0

23.4.1.4 CAP_WR_PID_ADDR

- Base Address: C005_D000h
- Address = Base Address + 0x0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	21'b0
PID_WR_SEL	[10:9]	RW	PID write module select 0 = MPEG TSP Capture 0 1 = MPEG TSP Capture 1 2 = MPEG TSP Core module	2'b0
PID_WR_ADDR	[8:0]	RW	PID Write Address	9'b0

23.4.1.5 CAP0_CAPDATA

- Base Address: C005_D000h
- Address = Base Address + 0x10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
cap0_capdata	[31:0]	R	MPEG TS Interface capture data	32'b0

23.4.1.6 CAP1_CAPDATA

- Base Address: C005_D000h
- Address = Base Address + 0x14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
cap1_capdata	[31:0]	R	MPEG TS Interface capture data	32'b0

23.4.1.7 CORE_TRDATA

- Base Address: C005_D000h
- Address = Base Address + 0x1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CORE_TRdata	[31:0]	R	MPEG TS Interface transfer data	32'b0

23.4.1.8 CORE_CTRL

- Base Address: C005_D000h
- Address = Base Address + 0x20h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:19]	–	Reserved	13'b0
CORE_INT_PEND	[18]	R	MPEG TS Core interrupt pending R: 0 = Interrupt not pended 1 = Interrupt pended W: 0 = Not work 1 = Interrupt clear	1'b0
CORE_int_mask	[17]	RW	MPEG TS Core interrupt mask	1'b0
CORE_int_enb	[16]	RW	MPEG TS Core interrupt enable	1'b0
RSVD	[15:8]	–	Reserved	8'b0
CORE_SRAM_PWR	[7]	RW	MPEG TS Core SRAM power	1'b0
CORE_sram_sleep	[6]	RW	MPEG TS Core SRAM sleep mode	1'b0
RSVD	[5:2]	–	Reserved	4'b0
CORE_encr_mode	[1]	RW	MPEG TS Core Encryption mode 0 = Decoding 1 = Encoding	1'b0
CORE_enb	[0]	RW	MPEG TS Core Enable	1'b0

23.4.1.9 IDMA_STATUS

- Base Address: C005_D000h
- Address = Base Address + 0x24h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:20]	–	Reserved	12'b0
idma3_busy	[19]	R	Internal DMA3 busy	1'b0
idma2_busy	[18]	R	Internal DMA2 busy	1'b0
idma1_busy	[17]	R	Internal DMA1 busy	1'b0
idma0_busy	[16]	R	Internal DMA0 busy	1'b0
RSVD	[15:4]	–	Reserved	12'b0
Idma3_enb	[3]	RW	Internal DMA3 Enable	1'b0
Idma2_enb	[2]	RW	Internal DMA2 Enable	1'b0
Idma1_enb	[1]	RW	Internal DMA1 Enable	1'b0
Idma0_enb	[0]	RW	Internal DMA0 Enable	1'b0

23.4.1.10 IDMA_CON

- Base Address: C005_D000h
- Address = Base Address + 0x28h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:20]	–	Reserved	12'b0
idma3_stop	[19]	W	Internal DMA3 stop	1'b0
idma2_stop	[18]	W	Internal DMA2 stop	1'b0
idma1_stop	[17]	W	Internal DMA1 stop	1'b0
idma0_stop	[16]	W	Internal DMA0 stop	1'b0
RSVD	[15:4]	–	Reserved	12'b0
Idma3_run	[3]	W	0 = Internal DMA3 Initialize 1 = Internal DMA3 run	1'b0
Idma2_run	[2]	W	0 = Internal DMA2 Initialize 1 = Internal DMA2 run	1'b0
Idma1_run	[1]	W	0 = Internal DMA1 Initialize 1 = Internal DMA1 run	1'b0
Idma0_run	[0]	W	0 = Internal DMA0 Initialize 1 = Internal DMA0 run	1'b0

23.4.1.11 IDMA_INT

- Base Address: C005_D000h
- Address = Base Address + 0x2Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	–	Reserved	4'b0
idma3_int_enb	[27]	RW	Internal DMA3 interrupt enable	1'b0
idma2_int_enb	[26]	RW	Internal DMA2 interrupt enable	1'b0
idma1_int_enb	[25]	RW	Internal DMA1 interrupt enable	1'b0
idma0_int_enb	[24]	RW	Internal DMA0 interrupt enable	1'b0
RSVD	[23:20]	–	Reserved	4'b0
Idma3_int_mask	[19]	RW	Internal DMA3 interrupt mask 0 = Mask 1 = UnMask	1'b0
Idma2_int_mask	[18]	RW	Internal DMA2 interrupt mask 0 = Mask 1 = UnMask	1'b0
Idma2_int_mask	[17]	RW	Internal DMA1 interrupt mask 0 = Mask 1 = UnMask	1'b0
Idma0_int_mask	[16]	RW	Internal DMA0 interrupt mask 0 = Mask 1 = UnMask	1'b0
RSVD	[15:12]	–	Reserved	4'b0
Idma3_int_pend	[11]	RW	Internal DMA3 interrupt pending	1'b0
Idma2_int_pend	[10]	RW	Internal DMA2 interrupt pending	1'b0
Idma2_int_pend	[9]	RW	Internal DMA1 interrupt pending	1'b0
Idma0_int_pend	[8]	RW	Internal DMA0 interrupt pending	1'b0
RSVD	[7:4]	–	Reserved	4'b0
Idma3_int_clr	[3]	W	Internal DMA3 interrupt pending clear	1'b0
Idma2_int_clr	[2]	W	Internal DMA2 interrupt pending clear	1'b0
Idma2_int_clr	[1]	W	Internal DMA1 interrupt pending clear	1'b0
Idma0_int_clr	[0]	W	Internal DMA0 interrupt pending clear	1'b0

23.4.1.12 IDMA0_ADDR

- Base Address: C005_D000h
- Address = Base Address + 0x30h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma0_addr	[31:0]	RW	Internal DMA0 Base Addr	32'b0

23.4.1.13 IDMA1_ADDR

- Base Address: C005_D000h
- Address = Base Address + 0x34h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma1_addr	[31:0]	RW	Internal DMA1 Base Addr	32'b0

23.4.1.14 IDMA2_ADDR

- Base Address: C005_D000h
- Address = Base Address + 0x38h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma2_Addr	[31:0]	RW	Internal DMA2 Base Addr	32'b0

23.4.1.15 IDMA3_ADDR

- Base Address: C005_D000h
- Address = Base Address + 0x3Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma3_addr	[31:0]	RW	Internal DMA3 Base Addr	32'b0

23.4.1.16 IDMA0_LEN

- Base Address: C005_D000h
- Address = Base Address + 0x40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma0_LEN	[31:0]	RW	Internal DMA0 Data Length	32'b0

23.4.1.17 IDMA1_LEN

- Base Address: C005_D000h
- Address = Base Address + 0x44h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma1_LEN	[31:0]	RW	Internal DMA1 Data Length	32'b0

23.4.1.18 IDMA2_LEN

- Base Address: C005_D000h
- Address = Base Address + 0x48h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma2_LEN	[31:0]	RW	Internal DMA2 Data Length	32'b0

23.4.1.19 IDMA3_LEN

- Base Address: C005_D000h
- Address = Base Address + 0x4Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
idma3_LEN	[31:0]	RW	Internal DMA3 Data Length	32'b0

23.5 PID Filter Data Structure

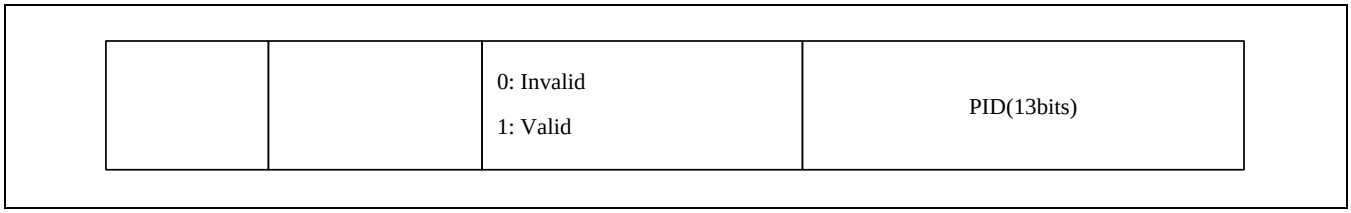


Figure 23-3 Capture I/F PID Structure

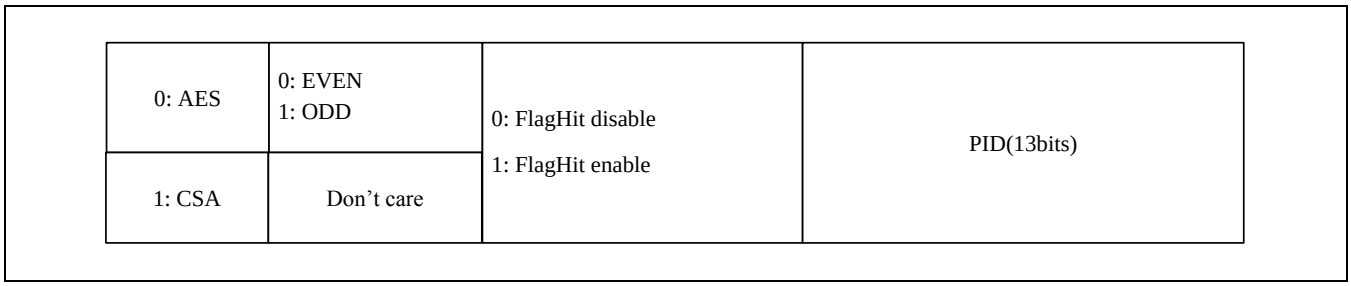


Figure 23-4 Basic AES/CSA PID Structure

24 UART_ISO7816

24.1 Overview

The UART performs:

- Serial-to-parallel conversion on data received from a peripheral device
- Parallel-to-serial conversion on data transmitted to the peripheral device.

The CPU reads and writes data and control/status information through the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories enabling up to 32 bytes to be stored independently in both transmit and receive modes.

The UART:

- Includes a programmable baud rate generator that generates a common transmit and receive internal clock from the UART internal reference clock input, UARTCLK
- Offers similar functionality to the industry-standard 16C650 UART device
- Supports the following maximum baud rates:
  - 921600 bps, in UART mode
  - 460800 bps, in IrDA mode
  - 115200 bps, in low-power IrDA mode.

The UART operation and baud rate values are controlled by the Line Control Register, UARTLCR_H and the baud rate divisor registers (Integer Baud Rate Register, UARTIBRD and Fractional Baud Rate Register, UARTFBRD.

The UART can generate:

- Individually-maskable interrupts from the receive (including timeout), transmit, modem status and error conditions
- A single combined interrupt so that the output is asserted if any of the individual interrupts are asserted, and unmasked
- DMA request signals for interfacing with a Direct Memory Access (DMA) controller.

If a framing, parity, or break error occurs during reception, the appropriate error bit is set, and is stored in the FIFO. If an overrun condition occurs, the overrun register bit is set immediately and FIFO data is prevented from being overwritten.

You can program the FIFOs to be 1 byte deep providing a conventional double-buffered UART interface.

The modem status input signals Clear to Send (CTS), Data Carrier Detect (DCD), Data Set Ready (DSR), and Ring Indicator (RI) are supported. The output modem control lines, Request to Send (RTS), and Data Terminal Ready (DTR) are also supported.

There is a programmable hardware flow control feature that uses the nUARTCTS input and the nUARTRTS output to automatically control the serial data flow.

The device is a cyclic type monolithic ADC, which provides an on-chip sample-and-hold and power down mode.

IrDA SIR block

The IrDA Serial Infra-Red (SIR) block contains an IrDA SIR protocol ENDEC. The SIR protocol ENDEC can be enabled for serial communication through signals nSIROUT and SIRIN to an infrared transducer instead of using the UART signals UARTTXD and UARTRXD.

If the SIR protocol ENDEC is enabled, the UARTTXD line is held in the passive state (HIGH) and transitions of the modem status, or the UARTRXD line have no effect. The SIR protocol ENDEC can receive and transmit, but it is half-duplex only, so it cannot receive while transmitting, or transmit while receiving.

The IrDA SIR physical layer specifies a minimum 10 ms delay between transmission and reception.

24.2 Features

The UART provides:

- Compliance to the AMBA Specification (Rev 2.0) onwards for easy integration into SoC implementation.
- Programmable use of UART or IrDA SIR input/output.
- Separate 32 × 8 transmit and 32 × 12 receive First-In, First-Out (FIFO) memory buffers to reduce CPU interrupts.
- Programmable FIFO disabling for 1 byte depth.
- Programmable baud rate generator. This enables division of the reference clock by (1 × 16) to (65535 × 16) and generates an internal ×16 clock. The divisor can be a fractional number enabling you to use any clock with a frequency > 3.6864 MHz as the reference clock.
- Standard asynchronous communication bits (start, stop and parity). These are added prior to transmission and removed on reception.
- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts.
- Support for Direct Memory Access (DMA): UART0, UART1, and UART2 only
- False start bit detection.
- Line break generation and detection.
- Support of the modem control functions CTS, DCD, DSR, RTS, DTR, and RI: UART1 only
- Programmable hardware flow control.
- Fully-programmable serial interface characteristics:
  - Data can be 5, 6, 7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Baud rate generation, dc up to UARTCLK/16
- IrDA SIR ENDEC block providing:
  - Programmable use of IrDA SIR or UART input/output
  - Support of IrDA SIR ENDEC functions for data rates up to 115200 bps half-duplex
  - Support of normal 3/16 and low-power (1.41-2.23 µs) bit durations
  - Programmable division of the UARTCLK reference clock to generate the appropriate bit duration for low-power IrDA mode.
- Support of the ISO-7816.
- Identification registers that uniquely identify the UART. These can be used by an operating system to automatically configure itself.

24.3 Block Diagram

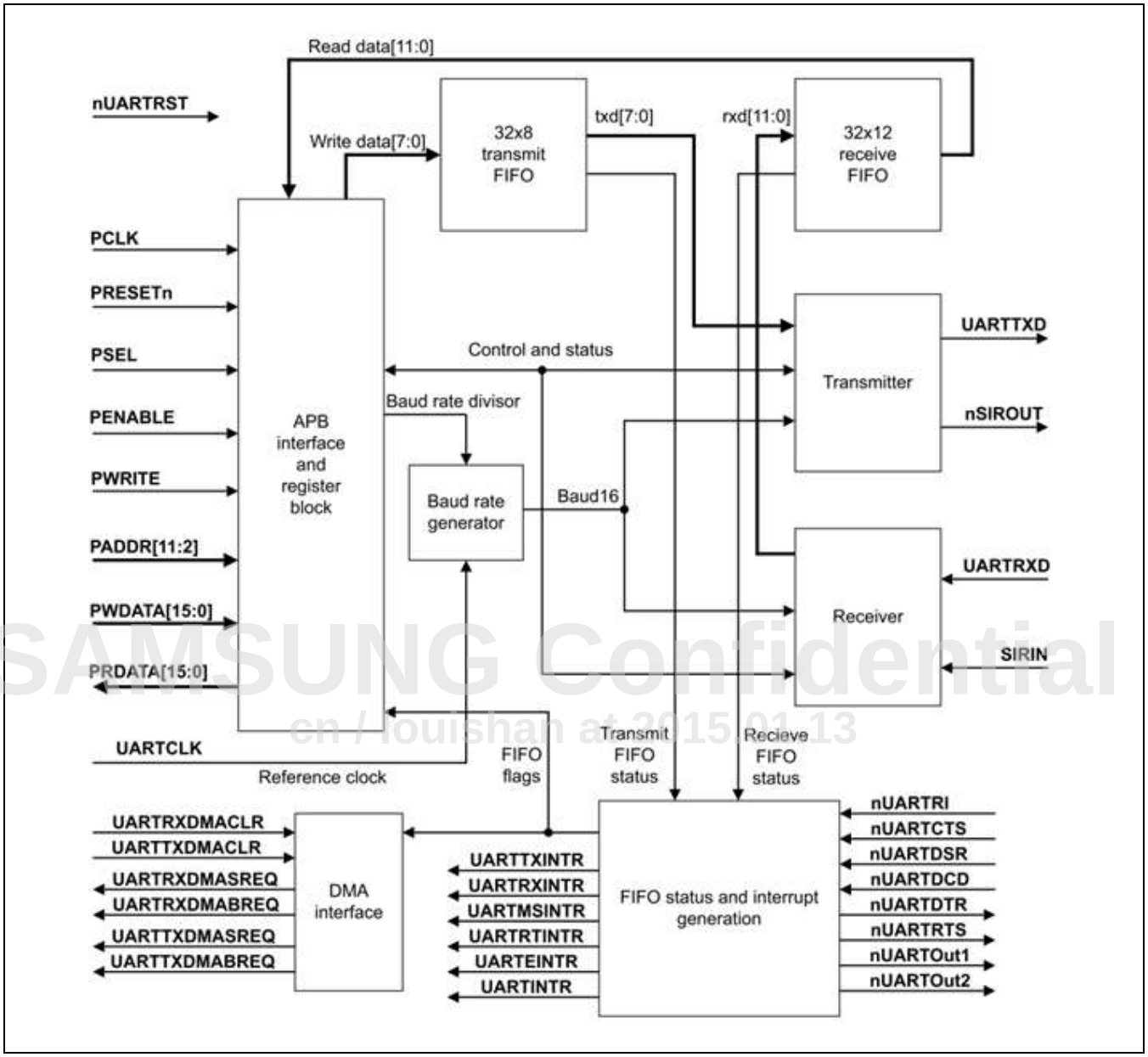


Figure 24-1 UART Block Diagram

AMBA APB interface

The AMBA APB interface generates read and write decodes for accesses to status/control registers, and the transmit and receive FIFOs.

Register block

The register block stores data written, or to be read across the AMBA APB interface.

Baud rate generator

The baud rate generator contains free-running counters that generate the internal × 16 clocks, Baud16 and IrLPBaud16 signals. Baud16 provides timing information for UART transmit and receive control. Baud16 is a stream of pulses with a width of one UARTCLK clock period and a frequency of 16 times the baud rate. IrLPBaud16provides timing information to generate the pulse width of the IrDA encoded transmit bit stream when in low-power IrDA mode.

Transmit FIFO

The transmit FIFO is an 8-bit wide, 32 location deep, FIFO memory buffer. CPU data written across the APB interface is stored in the FIFO until read out by the transmit logic. You can disable the transmit FIFO to act like a one-byte holding register. The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. Overrun, parity, frame error checking, and line break detection are also performed, and their status accompanies the data that is written to the receive FIFO.

Receive FIFO

The receive FIFO is a 12-bit wide, 32 location deep, FIFO memory buffer. Received data and corresponding error bits, are stored in the receive FIFO by the receive logic until read out by the CPU across the APB interface. The receive FIFO can be disabled to act like a one-byte holding register.

Transmit logic

The transmit logic performs parallel-to-serial conversion on the data read from the transmit FIFO. Control logic outputs the serial bit stream beginning with a start bit, data bits with the Least Significant Bit (LSB) first, followed by the parity bit, and then the stop bits according to the programmed configuration in control registers.

Receive logic

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. Overrun, parity, frame error checking, and line break detection are also performed, and their status accompanies the data that is written to the receive FIFO.

Interrupt generation logic

Individual mask-able active HIGH interrupts are generated by the UART. A combined interrupt output is also generated as an OR function of the individual interrupt requests. You can use the single combined interrupt with a system interrupt controller that provides another level of masking on a per-peripheral basis. This enables you to use modular device drivers that always know where to find the interrupt source control register bits.

You can also use the individual interrupt requests with a system interrupt controller that provides masking for the outputs of each peripheral. In this way, a global interrupt service routine can read the entire set of sources from one wide register in the system interrupt controller. This is attractive where the time to read from the peripheral registers is significant compared to the CPU clock speed in a real-time system.

DMA interface

The UART provides an interface to connect to the DMA controller.

Synchronizing registers and logic

The UART supports both asynchronous and synchronous operation of the clocks, PCLK and UARTCLK. Synchronization registers and handshaking logic have been implemented, and are active at all times. This has a minimal impact on performance or area. Synchronization of control signals is performed on both directions of data flow, that is from the PCLK to the UARTCLK domain, and from the UARTCLK to the PCLK domain.

24.3.1 IrDA SIR ENDEC Functional Description

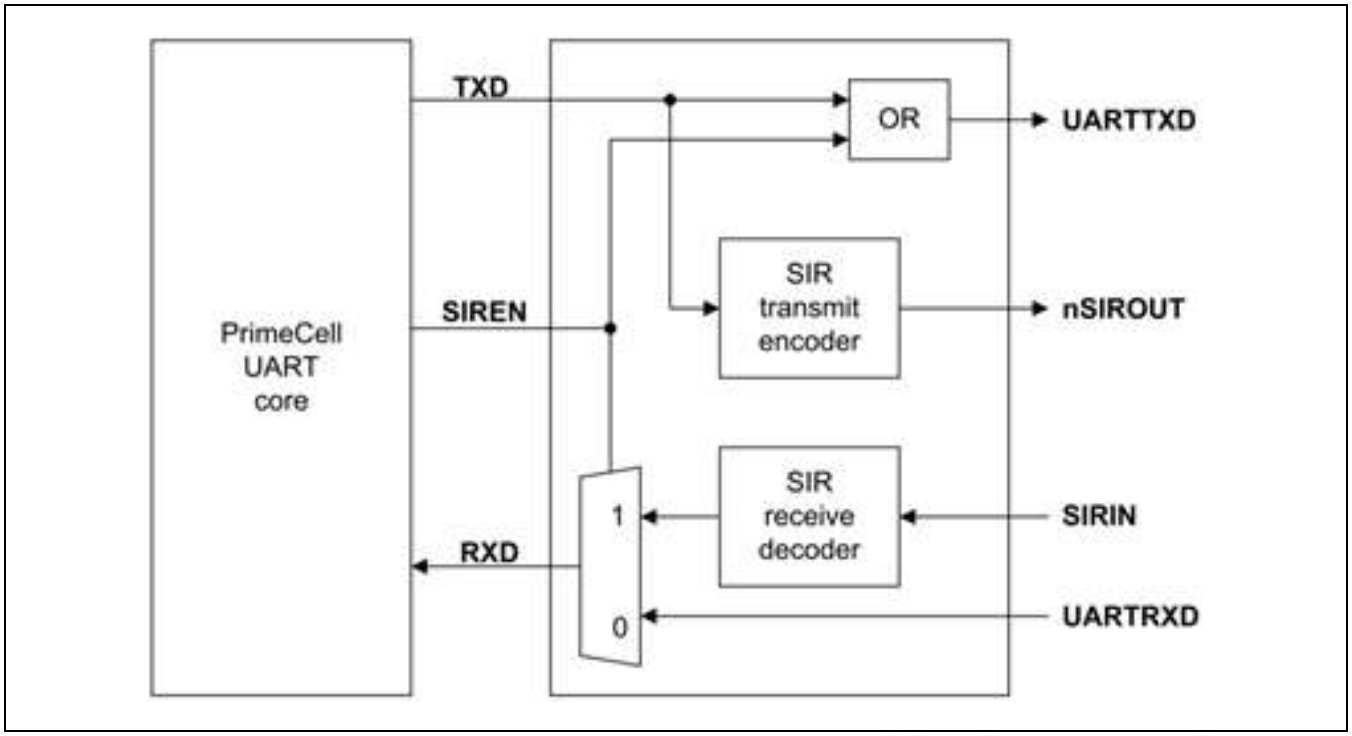


Figure 24-2 IrDA SIR RNDEC Block Diagram

24.3.1.1 IrDA SIR Transmit Encoder

The SIR transmit encoder modulates the Non Return-to-Zero (NRZ) transmit bit stream output from the UART. The IrDA SIR physical layer specifies use of a Return to Zero, Inverted (RZI) modulation scheme that represents logic 0 as an infrared light pulse. The modulated output pulse stream is transmitted to an external output driver and infrared Light Emitting Diode (LED).

In IrDA mode the transmitted pulse width is specified as three times the period of the internal × 16 clock (Baud16), that is, 3/16 of a bit period.

In low-power IrDA mode the transmit pulse width is specified as 3/16 of a 115200 bps bit period. This is implemented as three times the period of a nominal 1.8432 MHz clock (IrLPBaud16) derived from dividing down of UARTCLK clock. The frequency ofIrLPBaud16 is set up by writing the appropriate divisor value to the IrDA Low-Power Counter Register, UARTILPR.

The active low encoder output is normally LOW for the marking state (no light pulse).The encoder outputs a high pulse to generate an infrared light pulse representing a logic 0 or spacing state.

In normal and low-power IrDA modes, when the fractional baud rate divider is used, the transmitted SIR pulse stream includes an increased amount of jitter. This jitter is because the Baud16 pulses cannot be generated at regular intervals when fractional division is used. That is, the Baud16 cycles have a different number of UARTCLK cycles. It can be shown that the worst case jitter in the SIR pulse stream can be up to three UARTCLK cycles. This is within the limits of the SIR IrDA Specification where the maximum amount of jitter permitted is 13 %, provided the UARTCLK is > 3.6864 MHz and the maximum baud rate used for IrDA mode is ≤ 115200 bps. With these conditions, the jitter is less than 9 %.

24.3.1.2 IrDA SIR Receive Decoder

The SIR receive decoder demodulates the return-to-zero bit stream from the infrared detector and outputs the received NRZ serial bit stream to the UART received data input. The decoder input is normally HIGH (marking state) in the idle state. The transmit encoder output has the opposite polarity to the decoder input.

A start bit is detected when the decoder input is LOW.

NOTE: To prevent the UART from responding to glitches on the received data input then it ignores SIRIN pulses that are less than:
3/16 of Baud16, in IrDA mode
3/16 of IrLPBaud16, in low-power IrDA mode.

24.4 Operation

24.4.1 Interface Reset

The UART and IrDA SIR ENDEC are reset by the global reset signal PRESETn and a block-specific reset signal nUARTRST. An external reset controller must use PRESETn to assert nUARTRST asynchronously and negate it synchronously to UARTCLK. PRESETn must be asserted LOW for a period long enough to reset the slowest block in the on-chip system, and then be taken HIGH again. The UART requires PRESETn to be asserted LOW for at least one period of PCLK.

24.4.2 Clock Signals

The frequency selected for UARTCLK must accommodate the required range of baud rates:

- FUARTCLK (Min.) ≥ 16 × baud-rate (Max.)
- FUARTCLK (Max.) ≤ 16 × 65535 × baud-rate (Min.)

For example, for a range of baud rates from 110 baud to 460800 baud the UARTCLK frequency must be between 7.3728 MHz to 115.34 MHz.

The frequency of UARTCLK must also be within the required error limits for all baud rates to be used.

There is also a constraint on the ratio of clock frequencies for PCLK to UARTCLK. The frequency of UARTCLK must be no more than 5/3 times faster than the frequency of PCLK:

- FUARTCLK ≤ 5/3 × FPCLK

For example, in UART mode, to generate 921600 baud when UARTCLK is14.7456 MHz then PCLK must be greater than or equal to 8.85276 MHz. This ensures that the UART has sufficient time to write the received data to the receive FIFO.

24.4.3 UART Operation

Control data is written to the UART Line Control Register, UARTLCR. This register is 30 bits wide internally, but is externally accessed through the APB interface by writes to the following registers:

UARTLCR_H Defines the:

- Transmission parameters
- Word length
- Buffer mode
- Number of transmitted stop bits
- Parity mode
- Break generation.

UARTIBRD defines the integer baud rate divider

UARTFBRD defines the fractional baud rate divider

Fractional baud rate divider

The baud rate divisor is a 22-bit number consisting of a 16-bit integer and a 6-bit fractional part. This is used by the baud rate generator to determine the bit period. The fractional baud rate divider enables the use of any clock with a frequency > 3.6864 MHz to act as UARTCLK, while it is still possible to generate all the standard baud rates.

The 16-bit integer is written to the Integer Baud Rate Register, UARTIBRD. The 6-bit fractional part is written to the Fractional Baud Rate Register, UARTFBRD. The Baud Rate Divisor has the following relationship to UARTCLK:

- Baud Rate Divisor = UARTCLK/(16 × Baud Rate) = BRDI + BRDF

Where BRDI is the integer part and BRDF is the fractional part separated by a decimal point as *Figure 24-3* shows.

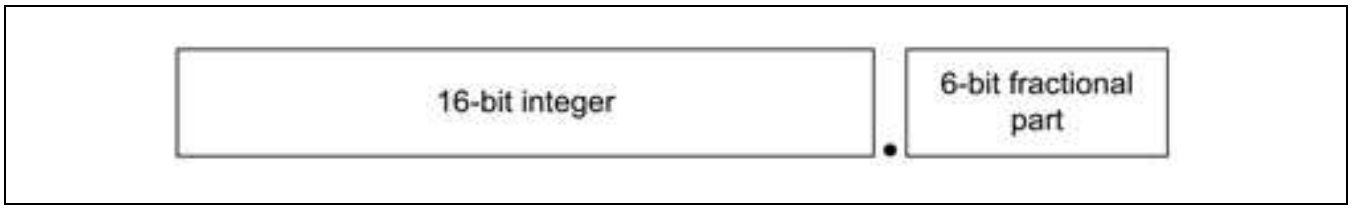


Figure 24-3 Baud rate divisor

You can calculate the 6-bit number (m) by taking the fractional part of the required baud rate divisor and multiplying it by 64 (that is, 2n, where n is the width of the UARTFBRD Register) and adding 0.5 to account for rounding errors:

- m = integer(BRDF × 2n + 0.5)

An internal clock enable signal, Baud16, is generated, and is a stream of one UARTCLK wide pulses with an average frequency of 16 times the required baud rate. This signal is then divided by 16 to give the transmit clock. A low number in the baud rate divisor gives a short bit period, and a high number in the baud rate divisor gives along bit period.

Data transmission or reception

Data received or transmitted is stored in two 32 byte FIFOs, though the receive FIFO has an extra four bits per character for status information.

For transmission, data is written into the transmit FIFO. If the UART is enabled, it causes a data frame to start transmitting with the parameters indicated in the Line Control Register, UARTLCR_H. Data continues to be transmitted until there is no data left in the transmit FIFO. The BUSY signal goes HIGH as soon as data is written to the transmit FIFO (that is, the FIFO is non-empty) and remains asserted HIGH while data is being transmitted. BUSY is negated only when the transmit FIFO is empty, and the last character has been transmitted from the shift register, including the stop bits. BUSY can be asserted HIGH even though the UART might no longer be enabled.

For each sample of data, three readings are taken and the majority value is kept. In the following paragraphs the middle sampling point is defined, and one sample is take neither side of it.

When the receiver is idle (UARTRXD continuously 1, in the marking state) and a LOW is detected on the data input (a start bit has been received), the receive counter, with the clock enabled by Baud16, begins running and data is sampled on the eighth cycle of that counter in UART mode, or the fourth cycle of the counter in SIR mode to allow for the shorter logic 0 pulses (half way through a bit period).

The start bit is valid if UARTRXD is still LOW on the eighth cycle of Baud16, otherwise a false start bit is detected and it is ignored.

If the start bit was valid, successive data bits are sampled on every 16th cycle of Baud16 (that is, one bit period later) according to the programmed length of the data characters. The parity bit is then checked if parity mode was enabled.

Lastly, a valid stop bit is confirmed if UARTRXD is HIGH, otherwise a framing error has occurred. When a full word is received, the data is stored in the receive FIFO, with any error bits associated with that word.

Error bits

Three error bits are stored in bits[10:8] of the receive FIFO, and are associated with a particular character. There is an additional error that indicates an overrun error and this is stored in bit 11 of the receive FIFO.

Overrun bit

The overrun bit is not associated with the character in the receive FIFO. The overrun error is set when the FIFO is full, and the next character is completely received in the shift register. The data in the shift register is overwritten, but it is not written into the FIFO. When an empty location is available in the receive FIFO, and another character is received, the state of the overrun bit is copied into the receive FIFO along with the received character. The overrun state is then cleared. *Table 24-1* lists the bit functions of the receive FIFO.

Table 24-1 Receive FIFO Bit Functions

FIFO bit	Function
11	Overrun indicator
10	Break error
9	Parity error
8	Framing error
7:0	Received data

Disabling the FIFOs

Additionally, you can disable the FIFOs. In this case, the transmit and receive sides of the UART have 1-byte holding registers (the bottom entry of the FIFOs). The overrun bit is set when a word has been received, and the previous one was not yet read. In this implementation, the FIFOs are not physically disabled, but the flags are manipulated to give the illusion of a 1-byte register. When the FIFOs are disabled, a write to the data register bypasses the holding register unless the transmit shift register is already in use.

System and diagnostic loopback testing

You can perform loopback testing for UART data by setting the Loop Back Enable (LBE) bit to 1 in the Control Register, UARTCR.

Data transmitted on UARTTXD is received on the UARTRXD input.

IrDA SIR operation

The IrDA SIR ENDEC provides functionality that converts between an asynchronous UART data stream, and half-duplex serial SIR interface. No analog processing is performed on-chip. The role of the SIR ENDEC is to provide a digital encoded output, and decoded input to the UART. There are two modes of operation:

- In IrDA mode, a zero logic level is transmitted as high pulse of 3/16th duration of the selected baud rate bit period on the nSIROUT signal, while logic one levels are transmitted as a static LOW signal. These levels control the driver of an infrared transmitter, sending a pulse of light for each zero. On the reception side, the incoming light pulses energize the photo transistor base of the receiver, pulling its output LOW. This drives the SIRIN signal LOW.
- In low-power IrDA mode, the width of the transmitted infrared pulse is set to three times the period of the internally generated IrLPBaud16 signal (1.63µs, assuming a nominal 1.8432MHz frequency) by setting the SIRLP bit in the Control Register, UARTCR.

In normal and low-power IrDA modes:

- During transmission, the UART data bit is used as the base for encoding
- During reception, the decoded bits are transferred to the UART receive logic

The IrDA SIR physical layer specifies a half-duplex communication link, with a minimum 10 ms delay between transmission and reception. This delay must be generated by software because it is not supported by the UART. The delay is required because the Infrared receiver electronics might become biased, or even saturated from the optical power coupled from the adjacent transmitter LED. This delay is known as latency, or receiver setup time.

The IrLPBaud16 signal is generated by dividing down the UARTCLK signal according to the low-power divisor value written to the IrDA Low-Power Counter Register, UARTILPR.

The low-power divisor value is calculated as:

- Low-power divisor = ($F_{UARTCLK}/F_{IrLPBaud16}$)

where $F_{IrLPBaud16}$ is nominally 1.8432 MHz

The divisor must be chosen so that 1.42 MHz < $F_{IrLPBaud16}$< 2.12 MHz.

System and diagnostic loopback testing

It is possible to perform loopback testing for SIR data by:

Setting the LBE bit to 1 in the Control Register, UARTCR.

Setting the SIRTEST bit to 1 in the Test Control Register, UARTTCR.

Data transmitted on nSIROUT is received on the SIRIN input.

NOTE: This is the only occasion that a test register is accessed during normal operation.

24.4.4 UART Character Frame

Figure 24-4 shows the UART character frame.

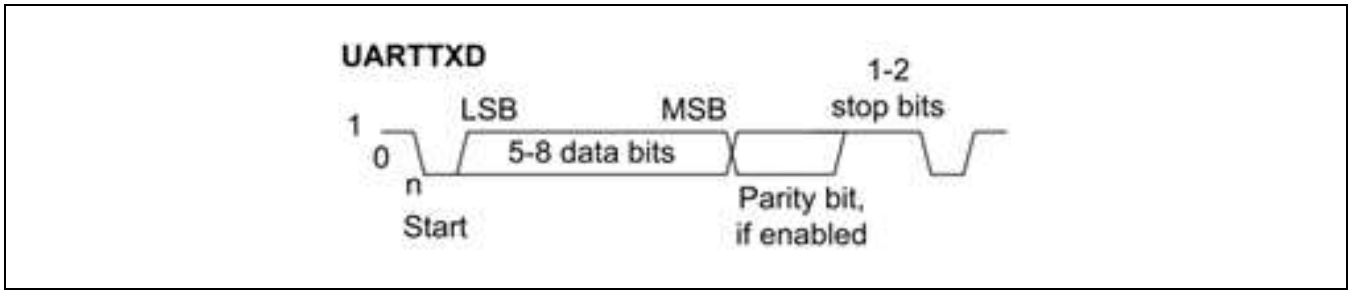


Figure 24-4 UART Character Frame

24.4.5 IrDA Data Modulation

Figure 24-5 shows the effect of IrDA 3/16 data modulation.

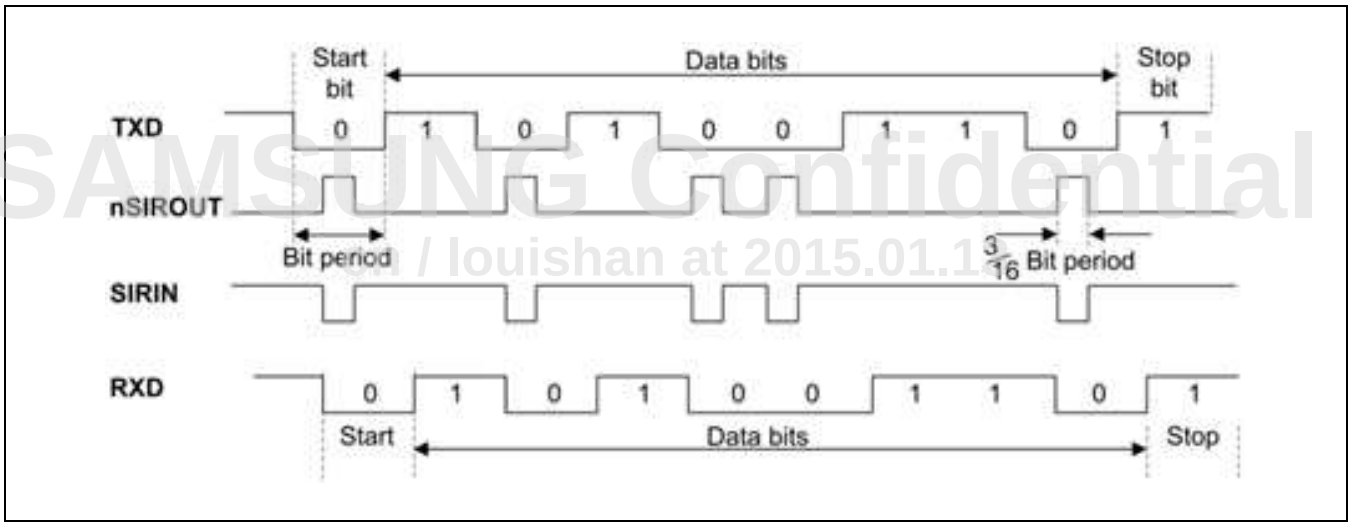


Figure 24-5 IrDA Data Modulation (3/16)

24.4.6 UART Modem Operation

You can use the UART to support both the Data Terminal Equipment (DTE) and Data Communication Equipment (DCE) modes of operation.

Table 24-2 Function of the Modem Input/Output Signals in DTE and DCE Modes

Signal	Function	
	DTE	DCE
nUARTCTS	Clear to send	Request to send
nUARTDSR	Data set ready	Data terminal ready
nUARTDCD	Data carrier detect	–
nUARTRI	Ring indicator	–
nUARTRTS	Request to send	Clear to send
nUARTDTR	Data terminal ready	Data set ready
nUARTOUT1	–	Data carrier detect
nUARTOUT2	–	Ring indicator

24.4.7 UART DMA Interface

The UART provides an interface to connect to a DMA controller. The DMA operation of the UART is controlled using the DMA Control Register, UARTDMACR. The DMA interface includes the following signals:

For receive:

- UARTRXDMASREQ

Single character DMA transfer request, asserted by the UART. For receive, one character consists of up to 12 bits. This signal is asserted when the receive FIFO contains at least one character.

- UARTRXDMABREQ

Burst DMA transfer request, asserted by the UART. This signal is asserted when the receive FIFO contains more characters than the programmed watermark level. You can program the watermark level for each FIFO using the Interrupt FIFO Level Select Register, UARTIFLS.

- UARTRXDMACLR

DMA request clear, asserted by a DMA controller to clear the receive request signals. If DMA burst transfer is requested, the clear signal is asserted during the transfer of the last data in the burst.

For transmit:

- UARTTXDMASREQ

Single character DMA transfer request, asserted by the UART. For transmit one character consists of up to eight bits. This signal is asserted when there is at least one empty location in the transmit FIFO.

- UARTTXDMABREQ

Burst DMA transfer request, asserted by the UART. This signal is asserted when the transmit FIFO contains less characters than the watermark level. You can program the watermark level for each FIFO using the Interrupt FIFO Level Select Register, UARTIFLS.

- UARTTXDMACLR

DMA request clear, asserted by a DMA controller to clear the transmit request signals. If DMA burst transfer is requested, the clear signal is asserted during the transfer of the last data in the burst.

The burst transfer and single transfer request signals are not mutually exclusive, they can both be asserted at the same time. For example, when there is more data than the watermark level in the receive FIFO, the burst transfer request and the single transfer request are asserted. When the amount of data left in the receive FIFO is less than the watermark level, the single request only is asserted. This is useful for situations where the number of characters left to be received in the stream is less than a burst.

For example, if 19 characters have to be received and the watermark level is programmed to be four. The DMA controller then transfers four bursts of four characters and three single transfers to complete the stream.

NOTE: For the remaining three characters the UART cannot assert the burst request.

Each request signal remains asserted until the relevant DMACLR signal is asserted. After the request clear signal is de-asserted, a request signal can become active again, depending on the conditions described previously. All request signals are de-asserted if the UART is disabled or the relevant DMA enable bit, TXDMAE or RXDMAE, in the DMA Control Register, UARTDMACR is cleared.

If you disable the FIFOs in the UART then it operates in character mode and only the DMA single transfer mode can operate, because only one character can be transferred to, or from the FIFOs at any time. UARTRXDMASREQ and UARTTXDMASREQ are the only request signals that can be asserted. See the Line Control Register, UARTLCR_H for information about disabling the FIFOs.

When the UART is in the FIFO enabled mode, data transfers can be made by either single or burst transfers depending on the programmed watermark level and the amount of data in the FIFO. *Table 24-3* lists the trigger points for UARTRXDMABREQ and UARTTXDMABREQ depending on the watermark level, for the transmit and receive FIFOs.

Table 24-3 DMA Trigger Points for the Transmit and Receive FIFOs

Watermark Level	Burst length	
	Transmit (Number of Empty Locations)	Receive (Number of Filled Locations)
1/8	28	4
1/4	24	8
1/2	16	16
3/4	8	24
7/8	4	28

In addition, the DMAONERR bit in the DMA Control Register, UARTDMACR supports the use of the receive error interrupt, UARTEINTR. It enables the DMA receive request outputs, UARTRXDMASREQ or UARTRXDMABREQ, to be masked out when the UART error interrupt, UARTEINTR, is asserted. The DMA receive request outputs remain inactive until the UARTEINTR is cleared. The DMA transmit request outputs are unaffected.

Figure 24-6 shows the timing diagram for both a single transfer request and a burst transfer request with the appropriate DMACLR signal. The signals are all synchronous to PCLK. For the sake of clarity it is assumed that there is no synchronization of the request signals in the DMA controller.

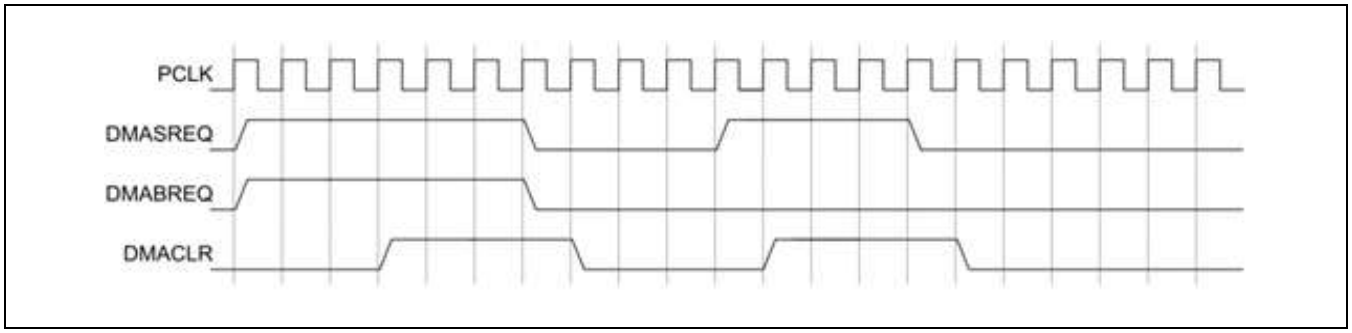


Figure 24-6 DMA Transfer Waveforms

24.4.8 Interrupts

There are eleven mask-able interrupts generated in the UART. These are combined to produce five individual interrupt outputs and one that is the OR of the individual outputs:

- UARTRXINTR
- UARTTXINTR
- UARTRTINTR
- UARTMSINTR, that can be caused by:
  - UARTRIINTR, because of a change in the nUARTRI modem status
  - UARTCTSINTR, because of a change in the nUARTCTS modem status
  - UARTDCDINTR, because of a change in the nUARTDCD modem status
  - UARTDSRINTR, because of a change in the nUARTDSR modem status.
- UARTEINTR, that can be caused by:
  - UARTOEINTR, because of an overrun error
  - UARTBEINTR, because of a break in the reception
  - UARTPEINTR, because of a parity error in the received character
  - UARTFEINTR, because of a framing error in the received character.
- UARTINTR, this is an OR function of the five individual masked outputs.

You can enable or disable the individual interrupts by changing the mask bits in the Interrupt Mask Set/Clear Register, UARTIMSC. Setting the appropriate mask bit HIGH enables the interrupt.

Provision of individual outputs and the combined interrupt output, enables you to use either a global interrupt service routine, or modular device drivers to handle interrupts.

The transmit and receive dataflow interrupts UARTRXINTR and UARTTXINTR *have been separated from the status interrupts. This enables you to use *UARTRXINTR* and *UARTTXINTR so that data can be read or written in response to the FIFO trigger levels.

The error interrupt, UARTEINTR, can be triggered when there is an error in the reception of data. A number of error conditions are possible.

The modem status interrupt, UARTMSINTR, is a combined interrupt of all the individual modem status signals.

The status of the individual interrupt sources can be read either from the Raw Interrupt Status Register, UARTRIS or from the Masked Interrupt Status Register, UARTMIS.

UARTMSINTR

The modem status interrupt is asserted if any of the modem status signals (nUARTCTS, nUARTDCD, nUARTDSR, and nUARTRI) change. It is cleared by writing a 1 to the corresponding bit(s) in the Interrupt Clear Register, UARTICR, depending on the modem status signals that generated the interrupt.

UARTRXINTR

The receive interrupt changes state when one of the following events occurs:

- If the FIFOs are enabled and the receive FIFO reaches the programmed trigger level. When this happens, the receive interrupt is asserted HIGH. The receive interrupt is cleared by reading data from the receive FIFO until it becomes less than the trigger level, or by clearing the interrupt.
- If the FIFOs are disabled (have a depth of one location) and data is received thereby filling the location, the receive interrupt is asserted HIGH. The receive interrupt is cleared by performing a single read of the receive FIFO, or by clearing the interrupt.

UARTTXINTR

The transmit interrupt changes state when one of the following events occurs:

- If the FIFOs are enabled and the transmit FIFO is equal to or lower than the programmed trigger level then the transmit interrupt is asserted HIGH. The transmit interrupt is cleared by writing data to the transmit FIFO until it becomes greater than the trigger level, or by clearing the interrupt.
- If the FIFOs are disabled (have a depth of one location) and there is no data present in the transmitters single location, the transmit interrupt is asserted HIGH. It is cleared by performing a single write to the transmit FIFO, or by clearing the interrupt.

To update the transmit FIFO you must:

- Write data to the transmit FIFO, either prior to enabling the UART and the interrupts, or after enabling the UART and interrupts.

NOTE: The transmit interrupt is based on a transition through a level, rather than on the level itself. When the interrupt and the UART is enabled before any data is written to the transmit FIFO the interrupt is not set. The interrupt is only set, after written data leaves the single location of the transmit FIFO and it becomes empty.

UARTRTINTR

The receive timeout interrupt is asserted when the receive FIFO is not empty, and no more data is received during a 32-bit period. The receive timeout interrupt is cleared either when the FIFO becomes empty through reading all the data (or by reading the holding register), or when a 1 is written to the corresponding bit of the Interrupt Clear Register, UARTICR.

UARTEINTR

The error interrupt is asserted when an error occurs in the reception of data by the UART. The interrupt can be caused by a number of different error conditions:

- framing
- parity
- break
- overrun

You can determine the cause of the interrupt by reading the Raw Interrupt Status Register, UARTRIS or the Masked Interrupt Status Register, UARTMIS. It can be cleared by writing to the relevant bits of the Interrupt Clear Register, UARTICR (bits 7 to 10 are the error clear bits).

UARTINTR

The interrupts are also combined into a single output, that is an OR function of the individual masked sources. You can connect this output to a system interrupt controller to provide another level of masking on a individual peripheral basis.

The combined UART interrupt is asserted if any of the individual interrupts are asserted and enabled.

24.4.9 ISO-7816

Figure 24-7 represents ISO-7816 interface. UARTTXD and UARTRXD signals are connected to external pads through Smart card Adapter block. Users can select whether to use ISO-7816 through USESMC, SMCTXENB, SMCRXENB signals, which are controllable by register.

In the case of communicating through ISO-7816 interface, SMC pads are controlled by PAD interface of NXOpenDrainAdapter.

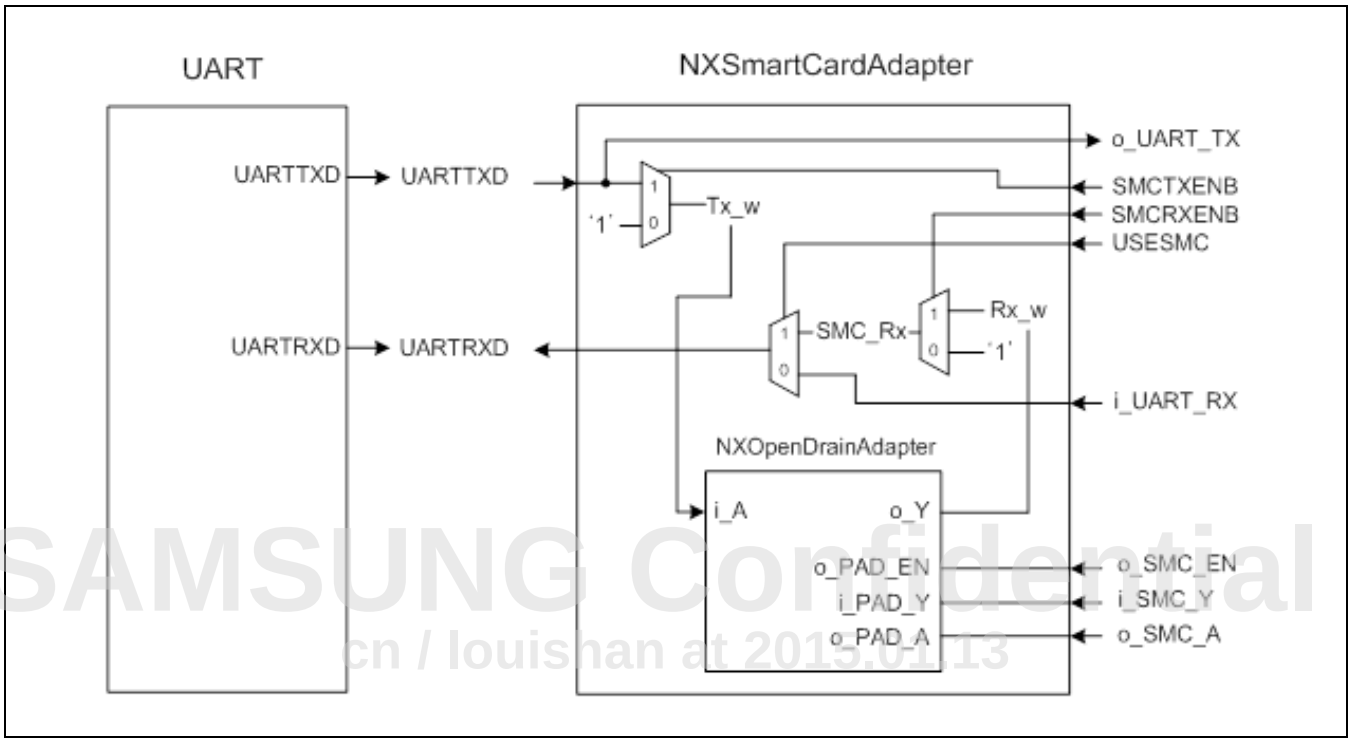


Figure 24-7 Smart Card Adepter Interface

24.5 Register Description

24.5.1 Register Map Summary

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)

Register	Offset	Description	Reset Value
UARTDR	0x00 0x00 0x00 0x00 0x00	Data register	0x0000_0000
UARTRSR/UARTECR	0x04 0x04 0x04 0x04 0x04	Receive status register/error clear register	0x0000_0000
RSVD	0x08 to 0x14 0x08 to 0x14 0x08 to 0x14 0x08 to 0x14 0x08 to 0x14	Reserved	Undefined
UARTFR	0x18 0x18 0x18 0x18 0x18	Flag register	Undefined
RSVD	0x1C 0x1C 0x1C 0x1C 0x1C	Reserved	Undefined
UARTILPR	0x20 0x20 0x20 0x20 0x20	IrDA Low-power counter register	0x0000_0000
UARTIBRD	0x24 0x24 0x24	Integer baud rate register	0x0000_0000

Register	Offset	Description	Reset Value
	0x24 0x24		
UARTFBRD	0x28 0x28 0x28 0x28 0x28	Fractional baud rate register	0x0000_0000
UARTLCR_H	0x2C 0x2C 0x2C 0x2C 0x2C	Line control register	0x0000_0000
UARTCR	0x30 0x30 0x30 0x30 0x30	Control register	0x0000_0180
UARTIFLS	0x34 0x34 0x34 0x34 0x34	Interrupt FIFO level select register	0x0000_0012
UARTIMSC	0x38 0x38 0x38 0x38 0x38	Interrupt mask set/clear register	0x0000_0000
UARTRIS	0x3C 0x3C 0x3C 0x3C 0x3C	Interrupt status register	0x0000_0000
UARTMIS	0x40 0x40 0x40 0x40 0x40	Interrupt status register	0x0000_0000
UARTICR	0x44 0x44 0x44 0x44 0x44	Interrupt clear register	Undefined

Register	Offset	Description	Reset Value
UARTDMACR	0x48 0x48 0x48 0x48 0x48	DMA control register	0x0000_0000

24.5.1.1 UARTDR

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x00, 0x00, 0x00, 0x00, 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	–
OE	[11]	R	Overrun error. This bit is set to 1 if data is received and the receive FIFO is already full. This is cleared to 0 once there is an empty space in the FIFO and a new character can be written to it.	1'b0
BE	[10]	R	Break error. This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits). In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a 1 (marking state), and the next valid start bit is received.	1'b0
PE	[9]	R	Parity error. When set to 1, it indicates that the parity of the received data character does not match the parity that the EPS and SPS bits in the Line Control Register, UARTLCR_H select. In FIFO mode, this error is associated with the character at the top of the FIFO.	1'b0
FE	[8]	R	Framing error. When set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is 1). In FIFO mode, this error is associated with the character at the top of the FIFO.	1'b0
DATA	[7:0]	RW	Receive (read) data character. Transmit (write) data character.	8'b0

The UARTDR Register is the data register.

For words to be transmitted:

- If the FIFOs are enabled, data written to this location is pushed onto the transmit FIFO
- If the FIFOs are not enabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO).
- The write operation initiates transmission from the UART. The data is prefixed with a start bit, appended with the appropriate parity bit (if parity is enabled), and a stop bit. The resultant word is then transmitted.

For received words:

- If the FIFOs are enabled, the data byte and the 4-bit status (break, frame, parity, and overrun) is pushed onto the 12-bit wide receive FIFO
- If the FIFOs are not enabled, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO).

24.5.1.2 UARTRSR/UARTECR

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x04, 0x04, 0x04, 0x04, 0x04, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	–	Reserved	–
-	[7:0]	W	A write to this register clears the framing, parity, break, and overrun errors. The data value is not important.	–
RSVD	[31:4]	–	Reserved	–
OE	[3]	R	Overrun error. This bit is set to 1 if data is received and the FIFO is already full. This bit is cleared to 0 by a write to UARTECR. The FIFO contents remain valid because no more data is written when the FIFO is full, only the contents of the shift register are overwritten. The CPU must now read the data, to empty the FIFO.	1'b0
BE	[2]	R	Break error. This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time (defined as start, data, parity, and stop bits).This bit is cleared to 0 after a write to UARTECR. In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a 1 (marking state) and the next valid start bit is received.	1'b0
PE	[1]	R	Parity error. When set to 1, it indicates that the parity of the received data character does not match the parity that the EPS and SPS bits in the Line Control Register, UARTLCR_H select. This bit is cleared to 0 by a write to UARTECR. In FIFO mode, this error is associated with the character at the top of the FIFO.	1'b0
FE	[0]	R	Framing error. When set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is 1). This bit is cleared to 0 by a write to UARTECR. In FIFO mode, this error is associated with the character at the top of the FIFO.	1'b0

The UARTRSR/UARTECR Register is the receive status register/error clear register.

Receive status can also be read from the UARTRSR Register. If the status is read from this register, then the status information for break, framing and parity corresponds to the data character read from the Data Register, UARTDR prior to reading the UARTRSR Register. The status information for overrun is set immediately when an overrun condition occurs.

A write to the UARTECR Register clears the framing, parity, break, and overrun errors. All the bits are cleared to 0 on reset.

24.5.1.3 UARTFR

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x18, 0x18, 0x18, 0x18, 0x18, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	–	Reserved	–
RI	[8]	R	Ring indicator. This bit is the complement of the UART ring indicator, nUARTRI, modem status input. That is, the bit is 1 when nUARTRI is LOW.	–
TXFF	[7]	R	Transmit FIFO empty. The meaning of this bit depends on the state of the FEN bit in the Line Control Register, UARTLCR_H. If the FIFO is disabled, this bit is set when the transmit holding register is empty. If the FIFO is enabled, the TXFE bit is set when the transmit FIFO is empty. This bit does not indicate if there is data in the transmit shift register.	–
RXFF	[6]	R	Receive FIFO full. The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H Register. If the FIFO is disabled, this bit is set when the receive holding register is full. If the FIFO is enabled, the RXFF bit is set when the receive FIFO is full.	–
TXFE	[5]	R	Transmit FIFO full. The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H Register. If the FIFO is disabled, this bit is set when the transmit holding register is full. If the FIFO is enabled, the TXFF bit is set when the transmit FIFO is full.	–
RXFE	[4]	R	Receive FIFO empty. The meaning of this bit depends on the state of the FEN bit in the UARTLCR_H Register. If the FIFO is disabled, this bit is set when the receive holding register is empty. If the FIFO is enabled, the RXFE bit is set when the receive FIFO is empty.	–
BUSY	[3]	R	UART busy. If this bit is set to 1, the UART is busy transmitting data. This bit remains set until the complete byte, including all the stop bits, has been sent from the shift register. This bit is set as soon as the transmit FIFO becomes non-	–

Name	Bit	Type	Description	Reset Value
			empty, regardless of whether the UART is enabled or not.	
DSD	[2]	R	Data carrier detect. This bit is the complement of the UART data carrier detect, nUARTDCD, modem status input. That is, the bit is 1 when nUARTDCD is LOW.	–
DSR	[1]	R	Data set ready. This bit is the complement of the UART data set ready, nUARTDSR, modem status input. That is, the bit is 1 when nUARTDSR is LOW.	–
CTS	[0]	R	Clear to send. This bit is the complement of the UART clear to send, nUARTCTS, modem status input. That is, the bit is 1 when nUARTCTS is LOW.	–

24.5.1.4 UARTILPR

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x20, 0x20, 0x20, 0x20, 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
ILPDVSR	[7:0]	RW	8-bit low-power divisor value. These bits are cleared to 0 at reset.	8'b0

The UARTILPR Register is the IrDA low-power counter register. This is an 8-bit read/write register that stores the low-power counter divisor value used to generate theIrLPBaud16 signal by dividing down of UARTCLK.

The IrLPBaud16 signal is generated by dividing down the UARTCLK signal according to the low-power divisor value written to the UARTILPR Register.

The low-power divisor value is calculated as follows:

- low-power divisor (ILPDVSR) = ($F_{UARTCLK}/F_{IrLPBaud16}$)

where $F_{IrLPBaud16}$ is nominally 1.8432 MHz.

You must select the divisor so that 1.42 MHz < $F_{IrLPBaud16}$ < 2.12 MHz, results in a low-power pulse duration of 1.41-2.11 µs (three times the period of IrLPBaud16).

24.5.1.5 UARTIBRD

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x24, 0x24, 0x24, 0x24, 0x24, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
BAUD DIVINT	[15:0]	RW	The integer baud rate divisor. These bits are cleared to 0 on reset.	16'b0

The UARTIBRD Register is the integer part of the baud rate divisor value.

24.5.1.6 UARTFBRD

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x28, 0x28, 0x28, 0x28, 0x28, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:6]	–	Reserved	–
BAUD DIVFRAC	[5:0]	RW	The integer baud rate divisor. These bits are cleared to 0 on reset.	6'b0

The UARTFBRD Register is the fractional part of the baud rate divisor value.

The baud rate divisor is calculated as follows:

- Baud rate divisor BAUDDIV = ($F_{UARTCLK}$/(16 × Baud rate))

where $F_{UARTCLK}$ is the UART reference clock frequency.

The BAUDDIV is comprised of the integer value (BAUD DIVINT) and the fractional value (BAUD DIVFRAC).

24.5.1.7 UARTLCR_H

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x2C, 0x2C, 0x2C, 0x2C, 0x2C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
SPS	[7]	RW	Stick parity select. 0 = Stick parity is disabled 1 = Either: • if the EPS bit is 0 then the parity bit is transmitted and checked as a 1 • if the EPS bit is 1 then the parity bit is transmitted and checked as a 0. This bit has no effect when the PEN bit disables parity checking and generation.	1'b0
WLEN	[6:5]	RW	Word length. These bits indicate the number of data bits transmitted or received in a frame as follows: b11 = 8 bits b10 = 7 bits b01 = 6 bits b00 = 5 bits.	2'b0
FEN	[4]	RW	Enable FIFOs: 0 = FIFOs are disabled (character mode) that is, the FIFOs become 1-byte-deep holding registers 1 = transmit and receive FIFO buffers are enabled (FIFO mode).	1'b0
STP2	[3]	RW	Two stop bits select. If this bit is set to 1, two stop bits are transmitted at the end of the frame. The receive logic does not check for two stop bits being received.	1'b0
EPS	[2]	RW	Even parity select. Controls the type of parity the UART uses during transmission and reception: 0 = Odd parity. The UART generates or checks for an odd number of 1s in the data and parity bits. 1 = Even parity. The UART generates or checks for an even number of 1s in the data and parity bits. This bit has no effect when the PEN bit disables parity checking and generation.	1'b0
PEN	[1]	RW	Parity enable: 0 = Parity is disabled and no parity bit added to the data frame 1 = Parity checking and generation is enabled.	1'b0

Name	Bit	Type	Description	Reset Value
BRK	[0]	RW	Send break. If this bit is set to 1, a low-level is continually output on the UARTTXD output, after completing transmission of the current character. For the proper execution of the break command, the software must set this bit for at least two complete frames. For normal use, this bit must be cleared to 0.	1'b0

The UARTLCR_H Register is the line control register. This register accesses bits 29 to 22 of the UART Line Control Register, UARTLCR.

All the bits are cleared to 0 when reset.

The UARTLCR_H, UARTIBRD, and UARTFBRD registers form the single 30-bit wide UARTLCR Register that is updated on a single write strobe generated by aUARTLCR_H write. So, to internally update the contents of UARTIBRD or UARTFBRD, a UARTLCR_H write must always be performed at the end.

To update the three registers there are two possible sequences:

- UARTIBRD write, UARTFBRD write, and UARTLCR_H write
- UARTFBRD write, UARTIBRD write, and UARTLCR_H write.

To update UARTIBRD or UARTFBRD only:

- UARTIBRD write, or UARTFBRD write, and UARTLCR_H write.

24.5.1.8 UARTCR

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x30, 0x30, 0x30, 0x30, 0x30, Reset Value = 0x0000_0180

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
CTSEN	[15]	RW	CTS hardware flow control enable. If this bit is set to 1, CTS hardware flow control is enabled. Data is only transmitted when the nUARTCTS signal is asserted.	1'b0
RTSEN	[14]	RW	RTS hardware flow control enable. If this bit is set to 1, RTS hardware flow control is enabled. Data is only requested when there is space in the receive FIFO for it to be received.	1'b0
OUT2	[13]	RW	This bit is the complement of the UART Out2 (nUARTOut2) modem status output. That is, when the bit is programmed to a 1, the output is 0. For DTE this can be used as Ring Indicator (RI).	1'b0
OUT1	[12]	RW	This bit is the complement of the UART Out1 (nUARTOut1) modem status output. That is, when the bit is programmed to a 1 the output is 0. For DTE this can be used as Data Carrier Detect (DCD).	1'b0
RTS	[11]	RW	Request to send. This bit is the complement of the UART request to send, nUARTRTS, modem status output. That is, when the bit is programmed to a 1 then nUARTRTS is LOW.	1'b0
DTR	[10]	RW	Data transmit ready. This bit is the complement of the UART data transmit ready, nUARTDTR, modem status output. That is, when the bit is programmed to a 1 then nUARTDTR is LOW.	1'b0
RXE	[9]	RW	Receive enable. If this bit is set to 1, the receive section of the UART is enabled. Data reception occurs for either UART signals or SIR signals depending on the setting of the SIREN bit. When the UART is disabled in the middle of reception, it completes the current character before stopping.	1'b0
TXE	[8]	RW	Transmit enable. If this bit is set to 1, the transmit section of the UART is enabled. Data transmission occurs for either UART signals, or SIR signals depending on the setting of the SIREN bit. When the UART is disabled in the middle of transmission, it completes the current character before stopping.	1'b1
LBE	[7]	RW	Loopback enable. If this bit is set to 1 and the SIREN bit is	1'b1

Name	Bit	Type	Description	Reset Value
			set to 1 and the SIRTEST bit in the Test Control Register, UARTTCR is set to 1, then the nSIROUT path is inverted, and fed through to the SIRIN path. The SIRTEST bit in the test register must be set to 1 to override the normal half-duplex SIR operation. This must be the requirement for accessing the test registers during normal operation, and SIRTEST must be cleared to 0 when loopback testing is finished. This feature reduces the amount of external coupling required during system test. If this bit is set to 1, and the SIRTEST bit is set to 0, the UARTTXD path is fed through to the UARTRXD path. In either SIR mode or UART mode, when this bit is set, the modem outputs are also fed through to the modem inputs. This bit is cleared to 0 on reset, to disable loopback.	
RSVD	[6:3]	–	Reserved	–
SIRLP	[2]	RW	SIR low-power IrDA mode. This bit selects the IrDA encoding mode. If this bit is cleared to 0,low-level bits are transmitted as an active high pulse with a width of 3/16th of the bit period. If this bit is set to 1, low-level bits are transmitted with a pulse width that is 3 times the period of theIrLPBaud16 input signal, regardless of the selected bit rate. Setting this bit uses less power, but might reduce transmission distances.	1'b0
siren	[1]	RW	SIR enable: 0 = IrDA SIR ENDEC is disabled. nSIROUT remains LOW (no light pulse generated), and signal transitions on SIRIN have no effect. 1 = IrDA SIR ENDEC is enabled. Data is transmitted and received on nSIROUT and SIRIN. UARTTXD remains HIGH, in the marking state. Signal transitions on UARTRXD or modem status inputs have no effect. This bit has no effect if the UARTEN bit disables the UART.	1'b0
UARTEN	[0]	RW	UART enable: 0 = UART is disabled. If the UART is disabled in the middle of transmission or reception, it completes the current character before stopping. 1 = The UART is enabled. Data transmission and reception occurs for either UART signals or SIR signals depending on the setting of the SIREN bit.	1'b0

The UARTCR Register is the control register. All the bits are cleared to 0 on reset except for bits 9 and 8 that are set to 1.

24.5.1.9 UARTIFLS

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x34, 0x34, 0x34, 0x34, 0x34, Reset Value = 0x0000_0012

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	–	Reserved	–
RXIFLSEL	[5:3]	RW	Receive interrupt FIFO level select. The trigger points for the receive interrupt are as follows: b000 = Receive FIFO becomes ≥ 1/8 full b001 = Receive FIFO becomes ≥ 1/4 full b010 = Receive FIFO becomes ≥ 1/2 full b011 = Receive FIFO becomes ≥ 3/4 full b100 = Receive FIFO becomes ≥ 7/8 full b101-b111 = Reserved.	3'b010
TXIFLSEL	[2:0]	RW	Transmit interrupt FIFO level select. The trigger points for the transmit interrupt are as follows: b000 = Transmit FIFO becomes ≤ 1/8 full b001 = Transmit FIFO becomes ≤ 1/4 full b010 = Transmit FIFO becomes ≤ 1/2 full b011 = Transmit FIFO becomes ≤ 3/4 full b100 = Transmit FIFO becomes ≤ 7/8 full b101-b111 = Reserved.	3'b010

The UARTIFLS Register is the interrupt FIFO level select register. You can use this register to define the FIFO level that triggers the assertion of UARTTXINTR and UARTRXINTR.

The interrupts are generated based on a transition through a level rather than being based on the level. That is, the interrupts are generated when the fill level progresses through the trigger level.

The bits are reset so that the trigger level is when the FIFOs are at the half-way mark.

24.5.1.10 UARTIMSC

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x38, 0x38, 0x38, 0x38, 0x38, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	–
OEIM	[10]	RW	Overrun error interrupt mask. A read returns the current mask for the UARTOEINTR interrupt. On a write of 1, the mask of the UARTOEINTR interrupt is set. A write of 0 clears the mask.	1'b0
BEIM	[9]	RW	Break error interrupt mask. A read returns the current mask for the UARTBEINTR interrupt. On a write of 1, the mask of the UARTBEINTR interrupt is set. A write of 0 clears the mask.	1'b0
PEIM	[8]	RW	Parity error interrupt mask. A read returns the current mask for the UARTPEINTR interrupt. On a write of 1, the mask of the UARTPEINTR interrupt is set. A write of 0 clears the mask.	1'b0
FEIM	[7]	RW	Framing error interrupt mask. A read returns the current mask for the UARTFEINTR interrupt. On a write of 1, the mask of the UARTFEINTR interrupt is set. A write of 0 clears the mask.	1'b0
RTIM	[6]	RW	Receive timeout interrupt mask. A read returns the current mask for the UARTRTINTR interrupt. On a write of 1, the mask of the UARTRTINTR interrupt is set. A write of 0 clears the mask.	1'b0
TXIM	[5]	RW	Transmit interrupt mask. A read returns the current mask for the UARTTXINTR interrupt. On a write of 1, the mask of the UARTTXINTR interrupt is set. A write of 0 clears the mask.	1'b0
RXIM	[4]	RW	Receive interrupt mask. A read returns the current mask for the UARTRXINTR interrupt. On a write of 1, the mask of the UARTRXINTR interrupt is set. A write of 0 clears the mask.	1'b0
DSRMIM	[3]	RW	nUARTDSR modem interrupt mask. A read returns the current mask for the UARTDSRINTR interrupt. On a write of 1, the mask of the UARTDSRINTR interrupt is set. A write of 0 clears the mask.	1'b0
DCDMIM	[2]	RW	nUARTDCD modem interrupt mask. A read returns the current mask for the UARTDCDINTR interrupt. On a write of 1, the mask of the UARTDCDINTR interrupt	1'b0

Name	Bit	Type	Description	Reset Value
			is set. A write of 0 clears the mask.	
CTSMIM	[1]	RW	nUARTCTS modem interrupt mask. A read returns the current mask for the UARTCTSINTR interrupt. On a write of 1, the mask of the UARTCTSINTR interrupt is set. A write of 0 clears the mask.	1'b0
RIMIM	[0]	RW	nUARTRI modem interrupt mask. A read returns the current mask for the UARTRIINTR interrupt. On a write of 1, the mask of the UARTRIINTR interrupt is set. A write of 0 clears the mask.	1'b0

The UARTIMSC Register is the interrupt mask set/clear register. It is a read/write register.

On a read this register returns the current value of the mask on the relevant interrupt. On a write of 1 to the particular bit, it sets the corresponding mask of that interrupt. A write of 0 clears the corresponding mask.

All the bits are cleared to 0 when reset.

24.5.1.11 UARTRIS

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x3C, 0x3C, 0x3C, 0x3C, 0x3C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	–
OERIS	[10]	R	Overrun error interrupt status. Returns the raw interrupt state of the UARTOEINTR interrupt.	1'b0
BERIS	[9]	R	Break error interrupt status. Returns the raw interrupt state of the UARTBEINTR interrupt.	1'b0
PERIS	[8]	R	Parity error interrupt status. Returns the raw interrupt state of the UARTPEINTR interrupt.	1'b0
FERIS	[7]	R	Framing error interrupt status. Returns the raw interrupt state of the UARTFEINTR interrupt.	1'b0
RTRIS	[6]	R	Receive timeout interrupt status. Returns the raw interrupt state of the UARTRTINTR interrupt. In this case the raw interrupt cannot be set unless the mask is set, this is because the mask acts as an enable for power saving. That is, the same status can be read from UARTMIS and UARTRIS for the receive timeout interrupt.	1'b0
TXRIS	[5]	R	Transmit interrupt status. Returns the raw interrupt state of the UARTTXINTR interrupt.	1'b0
RXRIS	[4]	R	Receive interrupt status. Returns the raw interrupt state of the UARTRXINTR interrupt.	1'b0
DSRRMIS	[3]	R	nUARTDSR modem interrupt status. Returns the raw interrupt state of the UARTDSRINTR interrupt.	1'b0
DCDRMIS	[2]	R	nUARTDCD modem interrupt status. Returns the raw interrupt state of the UARTDCDINTR interrupt.	1'b0
CTSRMIS	[1]	R	nUARTCTS modem interrupt status. Returns the raw interrupt state of the UARTCTSINTR interrupt.	1'b0
RIRMIS	[0]	R	nUARTRI modem interrupt status. Returns the raw interrupt state of the UARTRIINTR interrupt.	1'b0

The UARTRIS Register is the raw interrupt status register. It is a read-only register. This register returns the current raw status value, prior to masking, of the corresponding interrupt. A write has no effect.

All the bits, except for the modem status interrupt bits (bits 3 to 0), are cleared to 0 when reset. The modem status interrupt bits are undefined after reset.

24.5.1.12 UARTMIS

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x40, 0x40, 0x40, 0x40, 0x40, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	–
OEMIS	[10]	R	Overrun error masked interrupt status. Returns the masked interrupt state of the UARTOEINTR interrupt.	1'b0
BEMIS	[9]	R	Break error masked interrupt status. Returns the masked interrupt state of the UARTBEINTR interrupt.	1'b0
PEMIS	[8]	R	Parity error masked interrupt status. Returns the masked interrupt state of the UARTPEINTR interrupt.	1'b0
FEMIS	[7]	R	Framing error masked interrupt status. Returns the masked interrupt state of the UARTFEINTR interrupt.	1'b0
RTMIS	[6]	R	Framing error masked interrupt status. Returns the masked interrupt state of the UARTFEINTR interrupt.	1'b0
TXMIS	[5]	R	Transmit masked interrupt status. Returns the masked interrupt state of the UARTTXINTR interrupt.	1'b0
RXMIS	[4]	R	Receive masked interrupt status. Returns the masked interrupt state of the UARTRXINTR interrupt.	1'b0
DSRMMI	[3]	R	nUARTDSR modem masked interrupt status. Returns the masked interrupt state of the UARTDSRINTR interrupt.	1'b0
DCDMM	[2]	R	nUARTDCD modem masked interrupt status. Returns the masked interrupt state of the UARTDCDINTR interrupt.	1'b0
CTSMMIS	[1]	R	nUARTCTS modem masked interrupt status. Returns the masked interrupt state of the UARTCTSINTR interrupt.	1'b0
RIMMIS	[0]	R	nUARTRI modem masked interrupt status. Returns the masked interrupt state of the UARTRIINTR interrupt.	1'b0

The UARTMIS Register is the masked interrupt status register. It is a read-only register. This register returns the current masked status value of the corresponding interrupt. A write has no effect.

All the bits except for the modem status interrupt bits (bits 3 to 0) are cleared to 0 when reset. The modem status interrupt bits are undefined after reset.

24.5.1.13 UARTICR

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x44, 0x44, 0x44, 0x44, 0x44, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	–	Reserved	–
OEIC	[10]	W	Overrun error interrupt clear. Clears the UARTOEINTR interrupt.	–
BEIC	[9]	W	Break error interrupt clear. Clears the UARTBEINTR interrupt.	–
PEIC	[8]	W	Parity error interrupt clear. Clears the UARTPEINTR interrupt.	–
FEIC	[7]	W	Framing error interrupt clear. Clears the UARTFEINTR interrupt.	–
RTIC	[6]	W	Receive timeout interrupt clear. Clears the UARTRTINTR interrupt.	–
TXIC	[5]	W	Transmit interrupt clear. Clears the UARTTXINTR interrupt.	–
RXIC	[4]	W	Receive interrupt clear. Clears the UARTRXINTR interrupt.	–
DSRMIC	[3]	W	nUARTDSR modem interrupt clear. Clears the UARTDSRINTR interrupt.	–
DCDMIC	[2]	W	nUARTDCD modem interrupt clear. Clears the UARTDCDINTR interrupt.	–
CTSMIC	[1]	W	nUARTCTS modem interrupt clear. Clears the UARTCTSINTR interrupt.	–
RIMIC	[0]	W	nUARTRI modem interrupt clear. Clears the UARTRIINTR interrupt.	–

The UARTICR Register is the interrupt clear register and is write-only. On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.

24.5.1.14 UARTDMACR

- Base Address: C00A_1000 (UART0)
- Base Address: C00A_0000 (UART1)
- Base Address: C00A_2000 (UART2)
- Base Address: C00A_3000 (UART3)
- Base Address: C006_D000 (UART4)
- Address = Base Address + 0x48, 0x48, 0x48, 0x48, 0x48, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	–	Reserved	–
DMAONERR	[2]	RW	DMA on error. If this bit is set to 1, the DMA receive request outputs, UARTRXDMASREQ or UARTRXDMABREQ, are disabled when the UART error interrupt is asserted.	1'b0
TXDMAE	[1]	RW	Transmit DMA enable. If this bit is set to 1, DMA for the transmit FIFO is enabled.	1'b0
RXDMAE	[0]	RW	Receive DMA enable. If this bit is set to 1, DMA for the receive FIFO is enabled.	1'b0

The UARTDMACR Register is the DMA control register. It is a read/write register. All the bits are cleared to 0 on reset.

25 USB2.0 OTG

25.1 Overview

USB On-The-Go (OTG) is a Dual-Role Device (DRD) controller, which supports both device and host functions. It is fully compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a. It supports high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps, Host only) transfers. HS OTG can be configured as a Host-only or Device-only controller.

25.2 Features

The USB2.0 HS OTG features include the following:

- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.3a)
- Operates in High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps, Host only) modes
- Supports UTMI+ Level 3 interface (Revision 1.0)
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- Supports only 32-bit data on the AHB
- 1 Control Endpoint 0 for control transfer
- 16 Device Mode Endpoints including Control Endpoint 0
- Programmable endpoint type: Bulk, Isochronous, or Interrupt
- Programmable IN/ OUT direction
- Supports 16 Host channels

25.3 Block Diagram

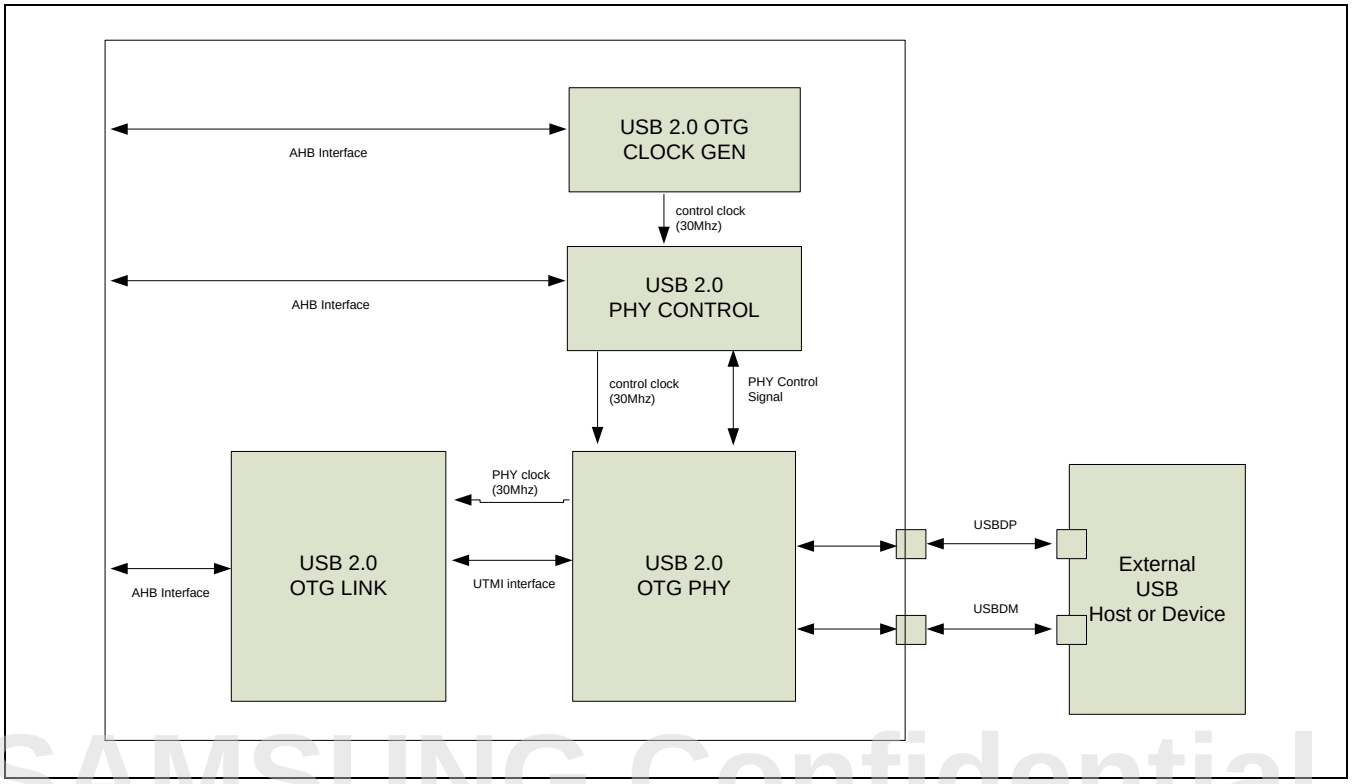


Figure 25-1 USB 2.0 OTG Block Diagram

The blocks in the USB 2.0 OTG controller are comprising as follows:

- USB 2.0 CLOCK GEN
- USB 2.0 PHY Control
- USB 2.0 PHY Link

Each has an AHB Slave, which provides CPU with read and write access to Control and Status Registers. The OTG Link has an AHB Master to transfer data on the AHB.

The USB system shown in *Figure 25-1* supports the port:

- USB 2.0 OTG 1 Port

25.4 I/O Pin Description

Table 25-1 USB OTG I/O Pin Description

Pin Name	GPIO No.	GPIO Function	Type	Description
USB 2.0 OTG Controller				
USBDP	–	–	I/O	Data Plus Signal from the USB Cable
USBDM	–	–	I/O	Data Minus Signal from the USB Cable
USBREXT	–	–	I	Connection to the external 200 Ω (± 1%) resistor. The signal must not go though a series resistance in the pad (an ESD resistance is included in the macro). The pad should have ESD, PMOS and NMOS clamp devices. The 200 Ω (±1%) resistor must be referenced to the VSSA33C ground supply and placed as close as possible to the chip. Total capacitance should be less than 8pF, including board traces.
USBVBUSIO	–	–	I	USB 5 V Power detection This VBUS indicator signal indicates that the VBUS signal on the USB cable is active. For the serial interface, this signal controls the Pull-Up resistance on the D+ line in Device mode only. 0 = Pull-Up resistance on the D+ line is disable. 1 = Pull-Up resistance on the D+ line is enabled based on the speed of operation.
USBVBUS	–	–	I	Logic Level VBUS Detect. When VBUSVLDEXTSEL of USB PHY register is set to 1, USBVBUS is used instead of USBVBUSIO. This pin is legacy mode.
USBID	*	*	IO	USB Mini-Receptacle Identifier. This signal differentiates a mini-A from a mini-B plug. The ID line is sampled only when the PULLUP signal is high. After sampling the ID line, It indicates whether a mini-A or mini-B cable is connected. • Low: Mini-A connected • High: Mini-B connected If this signal is not used, internal resistance pulls the signal's voltage level up to 2.5 V.
USBDRVVBUS	GPIOC[11]	Alt3	O	This controller signal enables or disablesexternal charge pump in host mode.

25.5 Functional Description

25.5.1 End Point Packet Size

USB OTG of this chip supports 8 end-points. In device mode, maximum packet size per each EP (Endpoint) is as follows:

Table 25-2 Maximum Packet Size per Endpoint

EP Number	Max Packet Size (bytes)
EP[0]	64
EP[1]	512
EP[2]	512
EP[3]	1024
EP[4]	1024
EP[5]	512
EP[6]	512
EP[7]	512
EP[9]	512
EP[9]	512
EP[10]	512
EP[11]	64
EP[12]	64
EP[13]	64
EP[14]	64
EP[15]	64

25.5.2 USB 5V Power Detection

You can select one of two VBUS by VBUSVLDEXTSEL of USB PHY register.

VBUS Pin	Description
USBVBUSIO	USB2.0 OTG module can operate in device mode when the voltage on USBVBUSIO is valid. To be valid in device mode, the voltage on USBVBUSIO is required to be between 4.75 V and 5.25 V.
USBVBUS	When VBUSVLDEXTSEL of USB PHY register is set to 1, USBVBUS is used instead of USBVBUSIO. The USBVBUS pad is a logic-level input. When the USB2 PHY is operating as a device, The USBVBUS acts as a gating signal for many of the internal USB2 PHY modules. Therefore, it is important that transitions on the USBVBUS are clean and well-defined.

25.5.3 Force Power Down

To reduce power consumption, all analog circuits of the USB 2.0 OTG block can be power downed.

See the following table for setting registers to force power down and power up.

Table 25-3 Force Power down configurations

Operation	Register Setting	Description
Power Up	PHYCTRL.PHYPOR = 0x0237; PHYCTRL.TESTPARM4 = 0x0000;	Power up USB PHY.
Power Down	PHYCTRL.PHYPOR = 0x023C; PHYCTRL.TESTPARM4 = 0x0030;	Power Down USB PHY including: • VBUS valid comparator(Bias and Bandgap circuits) • PLL • XO In power down mode, VBUS signal is gated. And USB PHY does not communicate with external Host/Device regardless of VBUS.

25.5.4 External Charge Pump

The USB 2.0 PHY requires an off-chip charge pump to provide power to the USB 2.0 OTG PHY VBUS pin.

Figure 25-2 shows the charge pump connection to the USB 2.0 PHY.

The charge pump's output is connected directly to VBUS on the device board. The USB 2.0 PHY's VBUS pin VBUS pin is also connected to VBUS. The charge pump's DRVVBUS input is an output of the OTG HNP finitestate machine and an input to the USB 2.0 PHY.

The VBUS presents a worst-case core-side load of 500pF. This worst-case load is a small addition to the overall capacitance budget that includes the external capacitive load due to routing, pads, package, board traces, and receivers

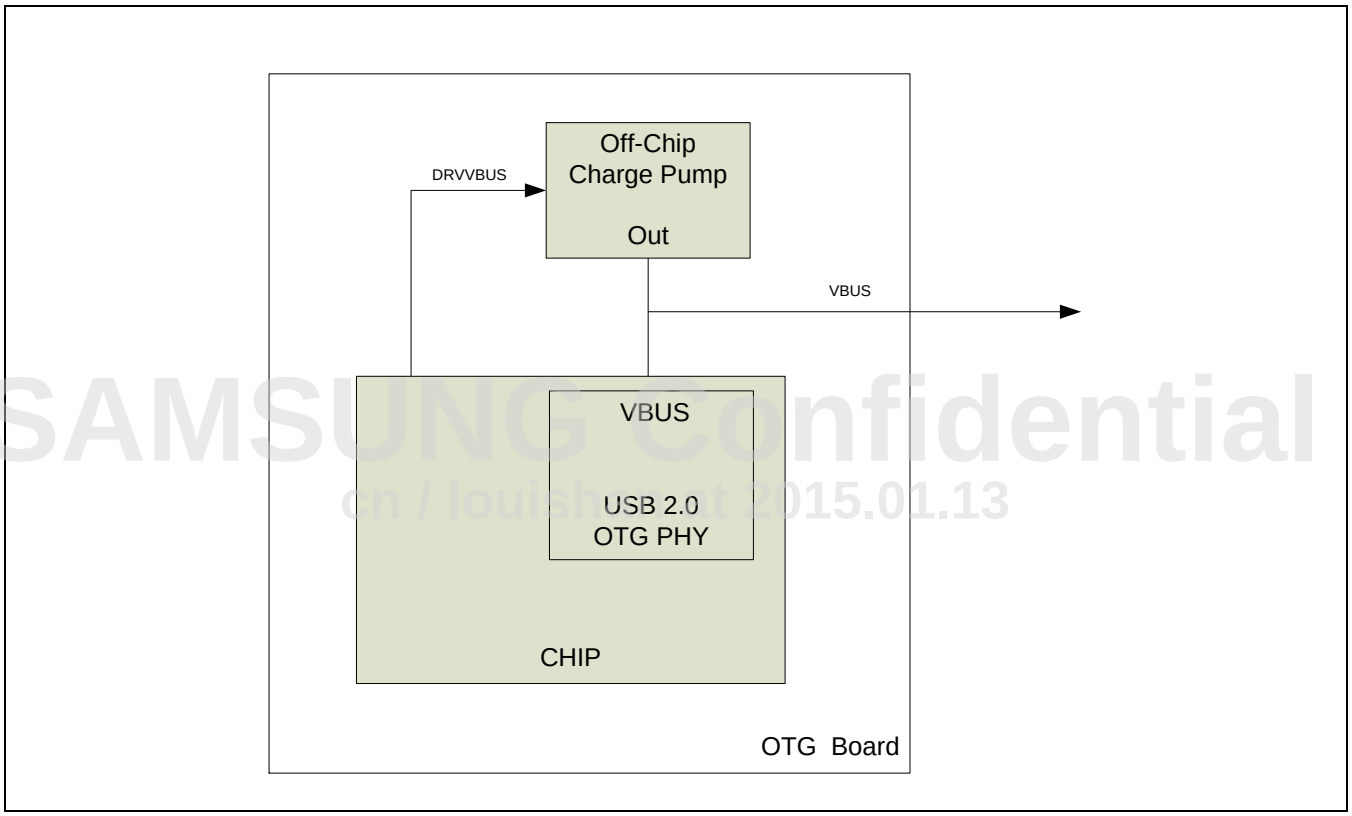


Figure 25-2 Charge Pump Connection

25.5.5 Modes of Operation

The application operates the Link either in DMA mode or in Slave mode. The application cannot operate the core using DMA and Slave modes simultaneously.

- DMA Mode

  USB OTG host uses the AHB Master interface to transmit packet data fetch (AHB to USB) and receive data update (USB to AHB). The AHB master uses the programmed DMA address (HCDMAn register in Host mode and DIEPDMAn/DOEPDMAn register in Device mode) to access the data buffers.

- Slave Mode

  USB OTG can operate either in transaction-level operation or in pipelined transaction-level operation. The application handles one data packet at a time per channel/endpoint in transaction-level operations. In pipelined transaction-level operation, the application programs the OTG to perform multiple transactions. The advantage of pipelined operation is that the application is not interrupted on packet basis.

25.6 Programming User Configure of PHY and OTG LINK

1. Release otg common reset
   - Program RSTCON1[25] (address: 0xC0012004) to 1'b1
2. Program scale mode to real mode
   - Program TIEOFFREG12[1:0] (address: 0xC0011030) to 2'b00
3. Select word interface and enable word interface selection
   - 8-bit word interface: Program TIEOFFREG14[9:8] (address: 0xC0011038) to 2'b01
   - 16-bit word interface: Program TIEOFFREG14[9:8] (address: 0xC0011038) to 2'b11
4. Select VBUS
   - Analog 5V USBVBUSIO: program TIEOFFREG13[25:24] (address: 0xC0011034) to 2'b00
   - Digital USBVBUS: program TIEOFFREG13[25:24] (address: 0xC0011034) to 2'b11
5. POR (Power On Reset) of PHY
   - Program TIEOFFREG13[8:7] (address: 0xC0011034) to 2'b01
6. Wait clock of PHY: About 40 micro seconds
7. Release utmi reset
   - Program TIEOFFREG13[3] (address: 0xC0011034) to 1'b1
8. Release ahb reset
   - Program TIEOFFREG13[2] (address: 0xC0011034) to 1'b1

25.7 Register Description

The OTG Link registers are classified as follows:

- Core Global Registers
- Host Mode Registers
  - Host Global Registers
  - Host Port CSRs
  - Host Channel-Specific Registers
- Device Mode Registers
  - Device Global Registers
  - Device Endpoint-Specific Registers

USB 2.0 OTG Register Map Groups

Register	Address	Description
Base address: USB_OTG_BASE = 0xC004_0000H		
USBOTG_GCSR	0xC004_0000	Core Global CSRs (1 KB)
USBOTG_HMCSR	0xC004_0400	Host Mode CSRs (1 KB)
USBOTG_DMCSR	0xC004_0800	Device Mode CSRs (1.5 KB)
USBOTG_PCGCCTL	0xC004_0E00	Power and Clock Gating CSRs (0.5 KB)
USBOTG_EPFIFO0	0xC004_1000	Device EP 0/Host Channel 0 FIFO (4 KB)
USBOTG_EPFIFO1	0xC004_2000	Device EP 1/Host Channel 1 FIFO (4 KB)
USBOTG_EPFIFO2	0xC004_3000	Device EP 2/Host Channel 2 FIFO (4 KB)
USBOTG_EPFIFO3	0xC004_4000	Device EP 3/Host Channel 3 FIFO (4 KB)
USBOTG_EPFIFO4	0xC004_5000	Device EP 4/Host Channel 4 FIFO (4 KB)
USBOTG_EPFIFO5	0xC004_6000	Device EP 5/Host Channel 5 FIFO (4 KB)
USBOTG_EPFIFO6	0xC004_7000	Device EP 6/Host Channel 6 FIFO (4 KB)
USBOTG_EPFIFO7	0xC004_8000	Device EP 7/Host Channel 7 FIFO (4 KB)
USBOTG_EPFIFO8	0xC004_9000	Device EP 8/Host Channel 8 FIFO (4 KB)
USBOTG_EPFIFO9	0xC004_A000	Device EP 9/Host Channel 9 FIFO (4 KB)
USBOTG_EPFIFO10	0xC004_B000	Device EP 10/Host Channel 10 FIFO (4 KB)
USBOTG_EPFIFO11	0xC004_C000	Device EP 11/Host Channel 11 FIFO (4 KB)
USBOTG_EPFIFO12	0xC004_D000	Device EP 12/Host Channel 12 FIFO (4 KB)
USBOTG_EPFIFO13	0xC004_E000	Device EP 13/Host Channel 13 FIFO (4 KB)
USBOTG_EPFIFO14	0xC004_F000	Device EP 14/Host Channel 14 FIFO (4 KB)
USBOTG_EPFIFO15	0xC005_0000	Device EP 15/Host Channel 15 FIFO (4 KB)
RSVD	0xC005_1000	Reserved
DFIFO_RAM	0xC006_0000	Direct Access to Data FIFO RAM for Debugging (128 KB)

25.7.1 Register Map Summary

- Base Address: 0xC004_0000

Register	Offset	Description	Reset Value
Core Global Registers			
GOTGCTL	0x0000	OTG Control and Status Register	0x0001_0000
GOTGINT	0x0004	OTG Interrupt Register	0x0000_0000
GAHBCFG	0x0008	Core AHB Configuration Register	0x0000_0000
GUSBCFG	0x000C	Core USB Configuration Register	0x0000_1400
GRSTCTL	0x0010	Core Reset Register	0x8000_0000
GINTSTS	0x0014	Core Interrupt Register	0x0400_1020
GINTMSK	0x0018	Core Interrupt Mask Register	0x0000_0000
GRXSTSR	0x001C	Receive Status Debug Read Register	–
GRXSTSP	0x0020	Receive Status Read/Pop Register	–
GRXFSIZ	0x_0024	Receive FIFO Size Register	0x0000_1800
GNPTXFSIZ	0x_0028	Non-Periodic Transmit FIFO Size Register	0x1800_1800
GNPTXSTS	0x_002C	Non-Periodic Transmit FIFO/Queue Status Register	0x0008_1800
HPTXFSIZ	0x_0100	Host Periodic Transmit FIFO Size Register	0x0300_5A00
DPTXFSIZ1	0x_0104	Device Periodic Transmit FIFO-1 Size Register	0x0300_1000
DPTXFSIZ2	0x_0108	Device Periodic Transmit FIFO-2 Size Register	0x0300_3300
DPTXFSIZ3	0x_010C	Device Periodic Transmit FIFO-3 Size Register	0x0300_3600
DPTXFSIZ4	0x_0110	Device Periodic Transmit FIFO-4 Size Register	0x0300_3900
DPTXFSIZ5	0x_0114	Device Periodic Transmit FIFO-5 Size Register	0x0300_3C00
DPTXFSIZ6	0x_0118	Device Periodic Transmit FIFO-6 Size Register	0x0300_3F00
DPTXFSIZ7	0x_011C	Device Periodic Transmit FIFO-7 Size Register	0x0300_4200
DPTXFSIZ8	0x_0120	Device Periodic Transmit FIFO-8 Size Register	0x0300_4500
DPTXFSIZ9	0x_0124	Device Periodic Transmit FIFO-9 Size Register	0x0300_4800
DPTXFSIZ10	0x_0128	Device Periodic Transmit FIFO-10 Size Register	0x0300_4B00
DPTXFSIZ11	0x_012C	Device Periodic Transmit FIFO-11 Size Register	0x0300_4E00
DPTXFSIZ12	0x_0130	Device Periodic Transmit FIFO-12 Size Register	0x0300_5100
DPTXFSIZ13	0x_0134	Device Periodic Transmit FIFO-13 Size Register	0x0300_5400
DPTXFSIZ14	0x_0138	Device Periodic Transmit FIFO-14 Size Register	0x0300_5700
DPTXFSIZ15	0x_013C	Device Periodic Transmit FIFO-15 Size Register	0x0300_5A00
Host Mode Registers			
Host Global Registers			
HCFG	0x_0400	Host Configuration Register	0x0020_0000
HFIR	0x_0404	Host Frame Interval Register	0x0000_17D7
HFNUM	0x_0408	Host Frame Number/Frame Time Remaining Register	0x0000_0000

Register	Offset	Description	Reset Value
HPTXSTS	0x_0410	Host Periodic Transmit FIFO/Queue Status Register	0x0008_0100
HAINT	0x_0414	Host All Channels Interrupt Register	0x0000_0000
HAINTMSK	0x_0418	Host All Channels Interrupt Mask Register	0x0000_0000
Host Port Control and Status Registers			
HPRT	0x_0440	Host Port Control and Status Register	0x0000_0000
Host Channel-Specific Registers			
HCCHAR0	0x_0500	Host Channel 0 Characteristics Register	0x0000_0000
HCSPLT0	0x_0504	Host Channel 0 Spilt Control Register	0x0000_0000
HCINT0	0x_0508	Host Channel 0 Interrupt Register	0x0000_0000
HCINTMSK0	0x_050C	Host Channel 0 Interrupt Mask Register	0x0000_0000
HCTSIZ0	0x_0510	Host Channel 0 Transfer Size Register	0x0000_0000
HCDMA0	0x_0514	Host Channel 0 DMA Address Register	0x0000_0000
HCCHAR1	0x_0520	Host Channel 1 Characteristics Register	0x0000_0000
HCSPLT1	0x_0524	Host Channel 1 Spilt Control Register	0x0000_0000
HCINT1	0x_0528	Host Channel 1 Interrupt Register	0x0000_0000
HCINTMSK1	0x_052C	Host Channel 1 Interrupt Mask Register	0x0000_0000
HCTSIZ1	0x_0530	Host Channel 1 Transfer Size Register	0x0000_0000
HCDMA1	0x_0534	Host Channel 1 DMA Address Register	0x0000_0000
HCCHAR2	0x_0540	Host Channel 2 Characteristics Register	0x0000_0000
HCSPLT2	0x_0544	Host Channel 2 Spilt Control Register	0x0000_0000
HCINT2	0x_0548	Host Channel 2 Interrupt Register	0x0000_0000
HCINTMSK2	0x_054C	Host Channel 2 Interrupt Mask Register	0x0000_0000
HCTSIZ2	0x_0550	Host Channel 2 Transfer Size Register	0x0000_0000
HCDMA2	0x_0554	Host Channel 2 DMA Address Register	0x0000_0000
HCCHAR3	0x_0560	Host Channel 3 Characteristics Register	0x0000_0000
HCSPLT3	0x_0564	Host Channel 3 Spilt Control Register	0x0000_0000
HCINT3	0x_0568	Host Channel 3 Interrupt Register	0x0000_0000
HCINTMSK3	0x_056C	Host Channel 3 Interrupt Mask Register	0x0000_0000
HCTSIZ3	0x_0570	Host Channel 3 Transfer Size Register	0x0000_0000
HCDMA3	0x_0574	Host Channel 3 DMA Address Register	0x0000_0000
HCCHAR4	0x_0580	Host Channel 4 Characteristics Register	0x0000_0000
HCSPLT4	0x_0584	Host Channel 4 Spilt Control Register	0x0000_0000
HCINT4	0x_0588	Host Channel 4 Interrupt Register	0x0000_0000
HCINTMSK4	0x_058C	Host Channel 4 Interrupt Mask Register	0x0000_0000
HCTSIZ4	0x_0580	Host Channel 4 Transfer Size Register	0x0000_0000
HCDMA4	0x_0584	Host Channel 4 DMA Address Register	0x0000_0000
HCCHAR5	0x_05A0	Host Channel 5 Characteristics Register	0x0000_0000

Register	Offset	Description	Reset Value
HCSPLT5	0x_05A4	Host Channel 5 Spilt Control Register	0x0000_0000
HCINT5	0x_05A8	Host Channel 5 Interrupt Register	0x0000_0000
HCINTMSK5	0x_05AC	Host Channel 5 Interrupt Mask Register	0x0000_0000
HCTSIZ5	0x_05B0	Host Channel 5 Transfer Size Register	0x0000_0000
HCDMA5	0x_05B4	Host Channel 5 DMA Address Register	0x0000_0000
HCCHAR6	0x_05C0	Host Channel 6 Characteristics Register	0x0000_0000
HCSPLT6	0x_05C4	Host Channel 6 Spilt Control Register	0x0000_0000
HCINT6	0x_05C8	Host Channel 6 Interrupt Register	0x0000_0000
HCINTMSK6	0x_05CC	Host Channel 6 Interrupt Mask Register	0x0000_0000
HCTSIZ6	0x_05D0	Host Channel 6 Transfer Size Register	0x0000_0000
HCDMA6	0x_05D4	Host Channel 6 DMA Address Register	0x0000_0000
HCCHAR7	0x_05E0	Host Channel 7 Characteristics Register	0x0000_0000
HCSPLT7	0x_05E4	Host Channel 7 Spilt Control Register	0x0000_0000
HCINT7	0x_05E8	Host Channel 7 Interrupt Register	0x0000_0000
HCINTMSK7	0x_05EC	Host Channel 7 Interrupt Mask Register	0x0000_0000
HCTSIZ7	0x_05F0	Host Channel 7 Transfer Size Register	0x0000_0000
HCDMA7	0x_05F4	Host Channel 7 DMA Address Register	0x0000_0000
HCCHAR8	0x_0600	Host Channel 8 Characteristics Register	0x0000_0000
HCSPLT8	0x_0604	Host Channel 8 Spilt Control Register	0x0000_0000
HCINT8	0x_0608	Host Channel 8 Interrupt Register	0x0000_0000
HCINTMSK8	0x_060C	Host Channel 8 Interrupt Mask Register	0x0000_0000
HCTSIZ8	0x_0610	Host Channel 8 Transfer Size Register	0x0000_0000
HCDMA8	0x_0614	Host Channel 8 DMA Address Register	0x0000_0000
HCCHAR9	0x_0620	Host Channel 9 Characteristics Register	0x0000_0000
HCSPLT9	0x_0624	Host Channel 9 Spilt Control Register	0x0000_0000
HCINT9	0x_0628	Host Channel 9 Interrupt Register	0x0000_0000
HCINTMSK9	0x_062C	Host Channel 10 Interrupt Mask Register	0x0000_0000
HCTSIZ9	0x_0630	Host Channel 10 Transfer Size Register	0x0000_0000
HCDMA9	0x_0634	Host Channel 10 DMA Address Register	0x0000_0000
HCCHAR10	0x_0640	Host Channel 10 Characteristics Register	0x0000_0000
HCSPLT10	0x_0644	Host Channel 10 Spilt Control Register	0x0000_0000
HCINT10	0x_0648	Host Channel 10 Interrupt Register	0x0000_0000
HCINTMSK10	0x_064C	Host Channel 10 Interrupt Mask Register	0x0000_0000
HCTSIZ10	0x_0650	Host Channel 10 Transfer Size Register	0x0000_0000
HCDMA10	0x_0654	Host Channel 10 DMA Address Register	0x0000_0000
HCCHAR11	0x_0660	Host Channel 11 Characteristics Register	0x0000_0000
HCSPLT11	0x_0664	Host Channel 11 Spilt Control Register	0x0000_0000

Register	Offset	Description	Reset Value
HCINT11	0x_0668	Host Channel 11 Interrupt Register	0x0000_0000
HCINTMSK11	0x_066C	Host Channel 11 Interrupt Mask Register	0x0000_0000
HCTSIZ11	0x_0670	Host Channel 11 Transfer Size Register	0x0000_0000
HCDMA11	0x_0674	Host Channel 11 DMA Address Register	0x0000_0000
HCCHAR12	0x_0680	Host Channel 12 Characteristics Register	0x0000_0000
HCSPLT12	0x_0684	Host Channel 12 Spilt Control Register	0x0000_0000
HCINT12	0x_0688	Host Channel 12 Interrupt Register	0x0000_0000
HCINTMSK12	0x_068C	Host Channel 12 Interrupt Mask Register	0x0000_0000
HCTSIZ12	0x_0690	Host Channel 12 Transfer Size Register	0x0000_0000
HCDMA12	0x_0694	Host Channel 12 DMA Address Register	0x0000_0000
HCCHAR13	0x_06A0	Host Channel 13 Characteristics Register	0x0000_0000
HCSPLT13	0x_06A4	Host Channel 13 Spilt Control Register	0x0000_0000
HCINT13	0x_06A8	Host Channel 13 Interrupt Register	0x0000_0000
HCINT6	0x_05C8	Host Channel 13 Interrupt Mask Register	0x0000_0000
HCINTMSK6	0x_05CC	Host Channel 13 Transfer Size Register	0x0000_0000
HCTSIZ6	0x_05D0	Host Channel 13 DMA Address Register	0x0000_0000
HCDMA6	0x_05D4	Host Channel 14 Characteristics Register	0x0000_0000
HCCHAR7	0x_05E0	Host Channel 14 Spilt Control Register	0x0000_0000
HCSPLT7	0x_05E4	Host Channel 14 Interrupt Register	0x0000_0000
HCINT7	0x_05E8	Host Channel 14 Interrupt Mask Register	0x0000_0000
HCINTMSK7	0x_05EC	Host Channel 14 Transfer Size Register	0x0000_0000
HCTSIZ7	0x_05F0	Host Channel 14 DMA Address Register	0x0000_0000
HCDMA7	0x_05F4	Host Channel 15 Characteristics Register	0x0000_0000
HCCHAR8	0x_0600	Host Channel 15 Spilt Control Register	0x0000_0000
HCSPLT8	0x_0604	Host Channel 15 Interrupt Register	0x0000_0000
HCINT8	0x_0608	Host Channel 15 Interrupt Mask Register	0x0000_0000
HCINTMSK8	0x_060C	Host Channel 15 Transfer Size Register	0x0000_0000
HCTSIZ8	0x_0610	Host Channel 15 DMA Address Register	0x0000_0000
HCDMA8	0x_0614	Host Channel 0 Characteristics Register	0x0000_0000
HCCHAR9	0x_0620	Host Channel 0 Spilt Control Register	0x0000_0000
HCSPLT9	0x_0624	Host Channel 0 Interrupt Register	0x0000_0000
HCINT9	0x_0628	Host Channel 0 Interrupt Mask Register	0x0000_0000
HCINTMSK9	0x_062C	Host Channel 0 Transfer Size Register	0x0000_0000
HCTSIZ9	0x_0630	Host Channel 0 DMA Address Register	0x0000_0000
HCDMA9	0x_0634	Host Channel 1 Characteristics Register	0x0000_0000
HCCHAR10	0x_0640	Host Channel 1 Spilt Control Register	0x0000_0000
HCSPLT10	0x_0644	Host Channel 1 Interrupt Register	0x0000_0000

Register	Offset	Description	Reset Value
HCINT10	0x_0648	Host Channel 1 Interrupt Mask Register	0x0000_0000
HCINTMSK10	0x_064C	Host Channel 1 Transfer Size Register	0x0000_0000
HCTSIZ10	0x_0650	Host Channel 1 DMA Address Register	0x0000_0000
HCDMA10	0x_0654	Host Channel 2 Characteristics Register	0x0000_0000
HCCHAR11	0x_0660	Host Channel 2 Spilt Control Register	0x0000_0000
HCSPLT11	0x_0664	Host Channel 2 Interrupt Register	0x0000_0000
HCINT11	0x_0668	Host Channel 2 Interrupt Mask Register	0x0000_0000
HCINTMSK11	0x_066C	Host Channel 2 Transfer Size Register	0x0000_0000
HCTSIZ11	0x_0670	Host Channel 2 DMA Address Register	0x0000_0000
HCDMA11	0x_0674	Host Channel 3 Characteristics Register	0x0000_0000
HCCHAR12	0x_0680	Host Channel 3 Spilt Control Register	0x0000_0000
HCSPLT12	0x_0684	Host Channel 3 Interrupt Register	0x0000_0000
HCINT12	0x_0688	Host Channel 3 Interrupt Mask Register	0x0000_0000
HCINTMSK12	0x_068C	Host Channel 3 Transfer Size Register	0x0000_0000
HCTSIZ12	0x_0690	Host Channel 3 DMA Address Register	0x0000_0000
HCDMA12	0x_0694	Host Channel 4 Characteristics Register	0x0000_0000
HCCHAR13	0x_06A0	Host Channel 4 Spilt Control Register	0x0000_0000
HCSPLT13	0x_06A4	Host Channel 4 Interrupt Register	0x0000_0000
HCINT13	0x_06A8	Host Channel 4 Interrupt Mask Register	0x0000_0000
HCINTMSK13	0x_06AC	Host Channel 4 Transfer Size Register	0x0000_0000
HCTSIZ13	0x_06B0	Host Channel 4 DMA Address Register	0x0000_0000
HCDMA13	0x_06B4	Host Channel 5 Characteristics Register	0x0000_0000
HCCHAR14	0x_06C0	Host Channel 5 Spilt Control Register	0x0000_0000
HCSPLT14	0x_06C4	Host Channel 5 Interrupt Register	0x0000_0000
HCINT14	0x_06C8	Host Channel 5 Interrupt Mask Register	0x0000_0000
HCINTMSK14	0x_06CC	Host Channel 5 Transfer Size Register	0x0000_0000
HCTSIZ14	0x_06D0	Host Channel 5 DMA Address Register	0x0000_0000
HCDMA14	0x_06D4	Host Channel 6 Characteristics Register	0x0000_0000
HCCHAR15	0x_06E0	Host Channel 6 Spilt Control Register	0x0000_0000
HCSPLT15	0x_06E4	Host Channel 6 Interrupt Register	0x0000_0000
HCINT15	0x_06E8	Host Channel 6 Interrupt Mask Register	0x0000_0000
HCINTMSK15	0x_06EC	Host Channel 6 Transfer Size Register	0x0000_0000
HCTSIZ15	0x_06F0	Host Channel 6 DMA Address Register	0x0000_0000
HCDMA15	0x_06F4	Host Channel 7 Characteristics Register	0x0000_0000
Device Mode Registers			
Device Global Registers			
DCFG	0x_0800	R/W Device Configuration Register	0x0020_0000

Register	Offset	Description	Reset Value
DCTL	0x_0804	Device Control Register	0x0000_0000
DSTS	0x_0808	Device Status Register	0x0000_0002
DIEPMSK	0x_0810	Device IN Endpoint Common Interrupt Mask Register	0x0000_0000
DOEPMSK	0x_0814	Device OUT Endpoint Common Interrupt Mask Register	0x0000_0000
DAINT	0x_0818	Device ALL Endpoints Interrupt Register	0x0000_0000
DAINTMSK	0x_081C	Device ALL Endpoints Interrupt Mask Register	0x0000_0000
DTKNQR1	0x_0820	Device IN Token Sequence Learning Queue Read Register 1	0x0000_0000
DTKNQR2	0x_0824	Device IN Token Sequence Learning Queue Read Register 2	0x0000_0000
DVBUSDIS	0x_0828	Device VBUS Discharge Time Register	0x0000_17D7
DVBUSPULSE	0x_082C	Device VBUS Pulsing Time Register	0x0000_05B8
DTKNQR3	0x_0830	Device IN Token Sequence Learning Queue Read Register 3	0x0000_0000
DTKNQR4	0x_0834	Device IN Token Sequence Learning Queue Read Register 4	0x0000_0000
Device Logical IN Endpoint-Specific Registers			
DIEPCTL0	0x_0900	Device Control IN Endpoint 0 Control Register	0x0000_8000
DIEPINT0	0x_0908	Device IN Endpoint 0 Interrupt Register	0x0000_0000
DIEPTSIZ0	0x_0910	Device IN Endpoint 0 Transfer Size Register	0x0000_0000
DIEPDMA0	0x_0914	Device IN Endpoint 0 DMA Address Register	0x0000_0000
DIEPCTL1	0x_0920	Device Control IN Endpoint 1 Control Register	0x0000_0000
DIEPINT1	0x_0928	Device IN Endpoint 1 Interrupt Register	0x0000_0080
DIEPTSIZ1	0x_0930	Device IN Endpoint 1 Transfer Size Register	0x0000_0000
DIEPDMA1	0x_0934	Device IN Endpoint 1 DMA Address Register	0x0000_0000
DIEPCTL2	0x_0940	Device Control IN Endpoint 2 Control Register	0x0000_0000
DIEPINT2	0x_0948	Device IN Endpoint 2 Interrupt Register	0x0000_0080
DIEPTSIZ2	0x_0950	Device IN Endpoint 2 Transfer Size Register	0x0000_0000
DIEPDMA2	0x_0954	Device IN Endpoint 2 DMA Address Register	0x0000_0000
DIEPCTL3	0x_0960	Device Control IN Endpoint 3 Control Register	0x0000_0000
DIEPINT3	0x_0968	Device IN Endpoint 3 Interrupt Register	0x0000_0080
DIEPTSIZ3	0x_0970	Device IN Endpoint 3 Transfer Size Register	0x0000_0000
DIEPDMA3	0x_0974	Device IN Endpoint 3 DMA Address Register	0x0000_0000
DIEPCTL4	0x_0980	Device Control IN Endpoint 4 Control Register	0x0000_0000
DIEPINT4	0x_0988	Device IN Endpoint 4 Interrupt Register	0x0000_0080
DIEPTSIZ4	0x_0990	Device IN Endpoint 4 Transfer Size Register	0x0000_0000
DIEPDMA4	0x_0994	Device IN Endpoint 4 DMA Address Register	0x0000_0000
DIEPCTL5	0x_09A0	Device Control IN Endpoint 5 Control Register	0x0000_0000

Register	Offset	Description	Reset Value
DIEPINT5	0x_09A8	Device IN Endpoint 5 Interrupt Register	0x0000_0080
DIEPTSIZ5	0x_09B0	Device IN Endpoint 5 Transfer Size Register	0x0000_0000
DIEPDMA5	0x_09B4	Device IN Endpoint 5 DMA Address Register	0x0000_0000
DIEPCTL6	0x_09C0	Device Control IN Endpoint 6 Control Register	0x0000_0000
DIEPINT6	0x_09C8	Device IN Endpoint 6 Interrupt Register	0x0000_0080
DIEPTSIZ6	0x_09D0	Device IN Endpoint 6 Transfer Size Register	0x0000_0000
DIEPDMA6	0x_09D4	Device IN Endpoint 6 DMA Address Register	0x0000_0000
DIEPCTL7	0x_09E0	Device Control IN Endpoint 7 Control Register	0x0000_0000
DIEPINT7	0x_09E8	Device IN Endpoint 7 Interrupt Register	0x0000_0080
DIEPTSIZ7	0x_09F0	Device IN Endpoint 7 Transfer Size Register	0x0000_0000
DIEPDMA7	0x_09F4	Device IN Endpoint 7 DMA Address Register	0x0000_0000
Device Logical OUT Endpoint-Specific Registers			
DOEPCTL0	0x_0B00	Device Control OUT Endpoint 0 Control Register	0x0000_8000
DOEPINT0	0x_0B08	Device OUT Endpoint 0 Interrupt Register	0x0000_0000
DOEPTSIZ0	0x_0B10	Device OUT Endpoint 0 Transfer Size Register	0x0000_0000
DOEPDMA0	0x_0B14	Device OUT Endpoint 0 DMA Address Register	0x0000_0000
DOEPCTL1	0x_0B00	Device Control OUT Endpoint 1 Control Register	0x0000_0000
DOEPINT1	0x_0B08	Device OUT Endpoint 1 Interrupt Register	0x0000_0000
DOEPTSIZ1	0x_0B10	Device OUT Endpoint 1 Transfer Size Register	0x0000_0000
DOEPDMA1	0x_0B14	Device OUT Endpoint 1 DMA Address Register	0x0000_0000
DOEPCTL2	0x_0B00	Device Control OUT Endpoint 2 Control Register	0x0000_0000
DOEPINT2	0x_0B08	Device OUT Endpoint 2 Interrupt Register	0x0000_0000
DOEPTSIZ2	0x_0B10	Device OUT Endpoint 2 Transfer Size Register	0x0000_0000
DOEPDMA2	0x_0B14	Device OUT Endpoint 2 DMA Address Register	0x0000_0000
DOEPCTL3	0x_0B00	Device Control OUT Endpoint 3 Control Register	0x0000_0000
DOEPINT3	0x_0B08	Device OUT Endpoint 3 Interrupt Register	0x0000_0000
DOEPTSIZ3	0x_0B10	Device OUT Endpoint 3 Transfer Size Register	0x0000_0000
DOEPDMA3	0x_0B14	Device OUT Endpoint 3 DMA Address Register	0x0000_0000
DOEPCTL4	0x_0B00	Device Control OUT Endpoint 4 Control Register	0x0000_0000
DOEPINT4	0x_0B08	Device OUT Endpoint 4 Interrupt Register	0x0000_0000
DOEPTSIZ4	0x_0B10	Device OUT Endpoint 4 Transfer Size Register	0x0000_0000
DOEPDMA4	0x_0B14	Device OUT Endpoint 4 DMA Address Register	0x0000_0000
DOEPCTL5	0x_0B00	Device Control OUT Endpoint 5 Control Register	0x0000_0000
DOEPINT5	0x_0B08	Device OUT Endpoint 5 Interrupt Register	0x0000_0000
DOEPTSIZ5	0x_0B10	Device OUT Endpoint 5 Transfer Size Register	0x0000_0000
DOEPDMA5	0x_0B14	Device OUT Endpoint 5 DMA Address Register	0x0000_0000
DOEPCTL6	0x_0B00	Device Control OUT Endpoint 6 Control Register	0x0000_0000

Register	Offset	Description	Reset Value
DOEPINT6	0x_0B08	Device OUT Endpoint 6 Interrupt Register	0x0000_0000
DOEPTSIZ6	0x_0B10	Device OUT Endpoint 6 Transfer Size Register	0x0000_0000
DOEPDMA6	0x_0B14	Device OUT Endpoint 6 DMA Address Register	0x0000_0000
DOEPCTL7	0x_0B00	Device Control OUT Endpoint 7 Control Register	0x0000_0000
DOEPINT7	0x_0B08	Device OUT Endpoint 7 Interrupt Register	0x0000_0000
DOEPTSIZ7	0x_0B10	Device OUT Endpoint 7 Transfer Size Register	0x0000_0000
DOEPDMA7	0x_0B14	Device OUT Endpoint 7 DMA Address Register	0x0000_0000
Power and Clock Gating Register			
PCGCCTL	0x_0E00	Power and Clock Gating Control Register	0x0000_0000

25.7.1.1 Core Global Registers (USB_OTG_GCSR)

25.7.1.1.1 GOTGCTL

- Base Address: 0xC004_0000
- Address = Base Address + 0x0000, Reset Value = 0x0001_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	–	Reserved	–
OTGVer	[20]	RW	OTG Version Indicates the OTG revision. 1'b0 = OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP. 1'b1 = OTG Version 2.0. In this version the core supports only Data line pulsing for SRP.	0x0
BSesVld	[19]	RW	B-Session Valid Indicates the Device mode transceiver status. 0 = B-session is not valid 1 = B-session is valid	0x0
ASesVld	[18]	R	A-Session Valid Indicates the Host mode transceiver status. 0 = A-session is not valid 1 = A-session is valid	0x0
DbncTime	[17]	R	Long/ Short Debounce Time Indicates the Debounce time of a detected connection. 0 = Long Debounce time, used for physical connections 1 = Short Debounce time, used for soft connections	0x0
ConIDSts	[16]	R	Connector ID Status Indicates the connector ID status. 0 = The OTG core is in A-device mode 1 = The OTG core is in B-device mode	0x1
RSVD	[15:12]	–	Reserved	-
DevHNPEn	[11]	RW	Device HNP Enable The application sets the bit if it successfully receives a Set Feature. 0 = HNP is not enabled in the application 1 = HNP is enabled in the application	0x0
HstSetHNPEn	[10]	RW	Host Set HNP Enable The application sets this bit if it has successfully enabled HNP on the connected device. 0 = Host Set HNP is not enabled 1 = Host Set HNP is enabled	0x0
HNPReq	[9]	RW	HNP Request The application sets this bit to initiate an HNP request to the connected USB host. The core clears this bit if the HstNegSucStsChng bit is cleared.	0x0

Name	Bit	Type	Description	Reset Value
			0 = No HNP request 1 = HNP request	
HstNegScs	[8]	R	Host Negotiation Success The core sets this bit if host negotiation is successful. The core clears this bit if the HNP Request (HNPReq) bit in this register isset. 0 = Host negotiation failure 1 = Host negotiation success	0x0
BvalidOvVal	[7]	RW	B-Peripheral Session Valid Override Value This bit is used to set the Override value for Bvalid signal when GOTGCTL.BvalidOvEn is set. 1'b0 = Bvalid value is 1'b0 when GOTGCTL.BvalidOvEn = 1. 1'b1 = Bvalid value is 1'b1 when GOTGCTL.BvalidOvEn = 1.	0x0-
BvalidOvEn	[6]	RW	B-Peripheral Session Valid Override Enable This bit is used to enable/disable the software to override the Bvalid signal using the GOTGCTL.BvalidOvVal. 1'b1 = Internally Bvalid received from the PHY is overridden with GOTGCTL.BvalidOvVal. 1'b0 = Override is disabled and Bvalid signal from the respective PHY selected is used internally by the core.	0x0
AvalidOvVal	[5]	RW	A-Peripheral Session Valid Override Value This bit is used to set the Override value for Avalid signal when GOTGCTL.AvalidOvEn is set. 1'b0 = Avalid value is 1'b0 when GOTGCTL.AvalidOvEn = 1. 1'b1 = Avalid value is 1'b1 when GOTGCTL.AvalidOvEn = 1.	0x0
AvalidOvEn	[4]	RW	A-Peripheral Session Valid Override Enable This bit is used to enable/disable the software to override the Avalid signal using the GOTGCTL.AvalidOvVal. 1'b1 = Internally Avalid received from the PHY is overridden with GOTGCTL.AvalidOvVal. 1'b0 = Override is disabled and Avalid signal from the respective PHYis used internally by the core.	0x0
VbvalidOvVal	[3]	RW	VBUS Valid Override Value This bit is used to set the Override value for vbus valid signal when GOTGCTL.VbusvalidOvEn is set. 1'b0 = vbus valid value is 1'b0 when OTGCTL.VbvalidOvEn = 1. 1'b1 = vbus valid value is 1'b1 when OTGCTL.VbvalidOvEn = 1.	0x0
VbvalidOvEn	[2]	RW	VBUS Valid Override Enable (VbvalidOvEn) This bit is used to enable/disable the software to override the vbus-valid signal using the GOTGCTL.vbvalidOvVal. 1'b1 = The vbus-valid signal received from the PHY is overridden with GOTGCTL.vbvalidOvVal. 1'b0 = Override is disabled and avalid signal from the	0x0

Name	Bit	Type	Description	Reset Value
			respective PHY is used internally by the core.	
SesReq	[1]	RW	Session Request The application sets this bit to initiate a session request on the USB. The core clears this bit if the HstNegSucStsChng bit is cleared. 0 = No session request 1 = Session request	0x0
SesReqScs	[0]	R-	Session Request Success The core sets this bit if a session request initiation is successful. 0 = Session request failure 1 = Session request success	0x0

25.7.1.1.2 GOTGINT

- Base Address: 0xC004_0000
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:20]	–	Reserved	–
DbnceDone	[19]	RW	Debounce Done The core sets this bit if the debounce is complete after the device connects. This bit is only valid if the HNP Capable or SRP Capable bit is set in the Core USB Configuration register.	0x0
ADevTOUTChg	[18]	RW	A-Device Timeout Change The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.	0x0
HstNegDet	[17]	RW	Host Negotiation Detected. The core sets this bit if it detects a host negotiation request on the USB.	0x0
RSVD	[16:10]	–	Reserved	–
HstnegSucStsChng	[9]	RW	Host Negotiation Success Status Change The core sets this bit on the success or failure of a USB host negotiation request.	0x0
SesReqSucStsChng	[8]	RW	Session Request Success Status Change The core sets this bit on the success or failure of a session request.	0x0
RSVD	[7:3]	–	Reserved	–
SesEndDet	[2]	RW	Session End Detected The core sets this bit if the b_valid signal is de-asserted.	0x0
RSVD	[1:0]	–	Reserved	–

25.7.1.1.3 GAHBCFG

- Base Address: 0xC004_0000
- Address = Base Address + 0x0008, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	–	Reserved	–
PTxFEmpLvl	[8]	RW	Periodic TxFIFO Empty Level Indicates if the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt registers (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode. 0 = GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty. 1 = GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty.	0x0
NPTxFEmpLvl	[7]	RW	Non-Periodic TxFIFO Empty Level Indicates if the Non-Periodic TxFIFO Empty Interrupt bits in the Core Interrupt register (GINSTS.NPTxFEmp) is triggered. This bitis used only in Slave mode. 0 = GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty. 1 = GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty.	0x0
DMAEn	[5]	RW	DMA Enable 0 = Core operates in Slave mode 1 = Core operates in a DMA mode	0x0
HBstLen	[4:1]	RW	Burst Length/vType Internal DMA Mode - AHB Master burst type: 0 = Single 1 = INCR 3 = INCR4 5 = INCR8 7 = INCR16 Others = Reserved	0x0
GlblIntrMsk	[0]	RW	Global Interrupt Mask The application uses this bit to mask or unmask the interrupt line assertion to itself. 0 = Mask the interrupt assertion to the application 1 = Unmask the interrupt assertion to the application	0x0

25.7.1.1.4 GUSBCFG

- Base Address: 0xC004_0000
- Address = Base Address + 0x000C, Reset Value = 0x0000_1400

Name	Bit	Type	Description	Reset Value
RSVD	[316]	–	Reserved	–
ForceDevMode	[30]	RW	Force Device Mode Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. 1'b0 = Normal Mode 1'b1 = Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 µs is sufficient.	0x0
ForceHstMode	[29]	RW	Force Host Mode Writing a 1 to this bit forces the core to host mode irrespective ofutmiotg_iddig input pin. 1'b0 = Normal Mode 1'b1 = Force Host Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500µs is sufficient.	0x0
RSVD	[27:16]	–	Reserved	-
PHYLowPower ClockSelect	[15]	RW	PHY Low-Power Clock Select Selects either 480 MHz or 48 MHz (low-power) PHY mode. In FS and LS modes, the PHY usually operate on a 48 MHz clock to save power. 0 = 480 MHz Internal PLL clock 1 = 48 MHz External clock NOTE: This bit must be configured with OPHYPWR.pll_powerdown.	0x0
RSVD	[14:10]	–	Reserved	0x5
HNPCap	[9]	RW	HNP-Capable The application uses this bit to control the OTG cores's HNP capabilities. 0 = HNP capability is not enabled 1 = HNP capability is enabled	0x0
SRPCap	[8]	RW	SRP-Capable The application uses this bit to control the OTG core's SRP capabilities. 0 = SRP capability is not enabled 1 = SRP capability is enabled	0x0
RSVD	[7:4]	–	Reserved	–
PHYIf	[3]	RW	PHY Interface The application uses this bit to configure the core to support	0x0

Name	Bit	Type	Description	Reset Value
			a UTMI+ PHY with an 8- or 16-bit interface. Only 16-bit interface is supported. This bit must be set to 1. 0 = 8 bits 1 = 16 bits	
TOutCal	[2:0]	RW	HS/ FS Timeout Calibration Set this bit to 3'h7.	0x0

25.7.1.1.5 GRSTCTL

- Base Address: 0xC004_0000
- Address = Base Address + 0x0010, Reset Value = 0x8000_0000

Name	Bit	Type	Description	Reset Value
AHBIdle	[31]	R	AHB Master Idle Indicates that the AHB Master State Machine is in the IDLE condition.	0x1
DMAReq	[30]	R	DMA Request Signal Indicates that the DMA request is in progress. Used for debug.	0x0
RSVD	[29:11]	–	Reserved	–
TxFNum	[10:6]	RW	TxFIFO Number This is the FIFO number. Use TxFIFO Flush bit to flush FIFO number. This field must not be changed until the core clears the TxFIFO Flush bit. 0 = Non-Periodic TxFIFO flush 1 = Periodic TxFIFO 1 flush in Device mode for Periodic TxFIFO flush in Host mode 2 = Periodic TxFIFO 2 flush in Device mode 15 = Periodic TxFIFO 15 flush in Device mode 16 = Flush all the Periodic and Non-Periodic TxFIFOs in the core	0x0
TxFFlsh	[5]	RW	TxFIFO Flush This bit selectively flushes a single or all transmit FIFOs, but cannot flush if the core is in the middle of a transaction. The application must only write this bit after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. The application must wait until the core clears this bit before performing any operations. This bit takes 8 clocks to clear.	0x0
RxFFlsh	[4]	RW	RxFIFO Flush The application flushes the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO.The application must wait until the bit is cleared before performing any other operations. This	0x0

Name	Bit	Type	Description	Reset Value
			bit takes 8 clocks to clear.	
INTknQFlsh	[3]	RW	IN Token Sequence Learning Queue Flush The application writes this bit to flush the IN Token Sequence Learning Queue.	0x0
FrmCntrRst	[2]	RW	Host Frame Counter Reset The application writes this bit to reset the (micro) frame number counter inside the core. If the (micro) frame counter is reset, the subsequent SOF sent out by the core will have a (micro) frame number of 0.	0x0
HSftRst	[1]	RW	HClk Soft Reset The application uses this bit to flush the control logic in the AHB Clock domain. Only AHB Clock Domain pipelines are reset. FIFOs are not flushed with this bit. All state machines in the AHB clock Domain are reset to IDLE state after terminating the transactions on the AHB, following the protocol. Control bits in the CSRs that the AHB Clock domain state machines use are cleared. Status mask bits generated by the AHB Clock domain state machine that control the interrupt status, are cleared to clear the interrupt. Because interrupt status bits are not cleared, the application gets the status of any core events that occurred after this bit is set. This is a self-clearing bit that the core clears after all necessarylogic is reset in the core. This may take several clocks, depending on the core's current state.	0x0
CSftRst	[0]	RW	Core Soft Reset Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits: HCFG.FSLSPclkSel DCFG.DevSpd All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which may take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain.	0x0

Name	Bit	Type	Description	Reset Value
			Software must also check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and if you dynamically change the PHY selection bits in the USB configuration registers listed above. If you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.	

25.7.1.1.6 GINTSTS

- Base Address: 0xC004_0000
- Address = Base Address + 0x0014, Reset Value = 0x0400_1020

Name	Bit	Type	Description	Reset Value
WkUpInt	[31]	RW	Resume/ Remote Wakeup Detected Interrupt In Device mode, this interrupt is asserted if a resume is detected on the USB. In Host mode, this interrupt is asserted if a remote wakeup is detected on the USB.	0x0
SessReqInt	[30]	RW	Session Request/ New Session Detected Interrupt In Host mode, this interrupt is asserted if a session request is detected from the device. In Device mode, this interrupt is asserted if the b_valid signal goes high.	0x0
DisconnInt	[29]	RW	Disconnect Detected Interrupt Asserted when a device disconnect is detected.	0x0
ConIDStsChng	[28]	RW	Connector ID Status Change The core sets this bit if there is a change in connector ID status.	0x0
RSVD	[27]	–	Reserved	–
PTxFEmp	[26]	R	Periodic TxFIFO Empty Asserted if the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register.	0x0
HChInt	[25]	R	Host Channels Interrupt The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the	0x0

Name	Bit	Type	Description	Reset Value
			HCINTn register to clear this bit.	
PrtInt	[24]	R	Host Port Interrupt The core sets this bit to indicate a change in port status of one of the OTG core ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit.	0x0
RSVD	[23]	–	Reserved	–
FetSusp	[22]	RW	Data Fetch Suspended. This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: • Sets a global non-periodic IN NAK handshake • Disables In endpoints • Flushes the FIFO • Determines the token sequence from the IN Token Sequence Learning Queue • Re-enables the endpoints • Clears the global non-periodic IN NAK handshake If the global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token received: the core generates an "IN token received when FIFO empty" interrupt. The OTG then sends the host a NAK response. To avoid this scenario, the application checks the GINSTS. FetSusp interrupt, which ensures that the FIFO is full before clearing a global NAK handshake. Alternatively, the application masks the “IN token received when FIFO empty” interrupt if clearing a global IN NAK handshake.	0x0
incompIP	[21]	RW	Incomplete Periodic Transfer. In Host mode, the core sets this interrupt bit if there are incomplete periodic transactions still pending which are scheduled for the current micro frame.	0x0
incomplSOOUT			Incomplete Isochronous OUT Transfer. The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not complete in the current micro frame. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.	
Incomplete	[20]	RW	Isochronous IN Transfer. The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not	0x0

Name	Bit	Type	Description	Reset Value
			complete in the current micro frame. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.	
OEPInt	[19]	R	OUT Endpoints Interrupt. The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-n interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit inthe corresponding DOEPINTn register to clear this bit.	0x0
IEPInt	[18]	R	IN Endpoints Interrupt The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT)register to determine the exact number of the IN endpoint on which the interrupt occurred, and then read the corresponding Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.	0x0
EPMis	[17]	RW	Endpoint Mismatch Interrupt Indicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-Periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.	0x0
RSVD	[16]	–	Reserved	–
EOPF	[15]	RW	End of Periodic Frame Interrupt Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PerFrInt) has been reached in the current micro frame.	0x0
ISOutDrop	[14]	RW	Isochronous OUT Packet Dropped Interrupt The core sets this bit if it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.	0x0
EnumDone	[13]	RW	Enumeration Done The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.	0x0
USBRst	[12]	RW	USB Reset The core sets this bit to indicate that a reset is detected on	0x1

Name	Bit	Type	Description	Reset Value
			the USB.	
USBSusp	[11]	RW	USB Suspend The core sets this bit to indicate that a suspend was detected on the USB. The core enters the Suspended state if there is no activity on the line_state signal for an extended period of time.	0x0
ErlySusp	[10]	RW	Early Suspend The core sets this bit to indicate that an Idle state has been detected on the USB for 3ms.	0x0
RSVD	[9]	–	Reserved	–
RSVD	[8]	–	Reserved	–
GOUTNakEff	[7]	R	Global OUT NAK Effective Indicates that the Set Global OUT NAK bit in the Device Control register (DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit is cleared by writing the Clear Global OUT NAK bit in the Device Control register.	0x0
GINNakEff	[6]	R	Global IN Non-Periodic NAK Effective Indicates that the Set Global Non-Periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, has taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit is cleared by clearing the Clear Global Non-Periodic IN NAK bit setby the application. This bit is cleared by clearing the Clear Global Non-Periodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.	0x0
NPTxFEmp	[5]	R	Non-Periodic TxFIFO Empty This interrupt is asserted if the Non-Periodic TxFIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-Periodic Transmit Request Queue. The half or completely empty status is determined by the Non-Periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl).	0x1
RxFLvl	[4]	R	RxFIFO Non-Empty Indicates that there is at least one packet pending to be read from the RxFIFO.	0x0
Sof	[3]	RW	Start of (micro) Frame In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF (HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application reads the Device Status register to get the	0x0

Name	Bit	Type	Description	Reset Value
			current (micro) frame number. This interrupt is seen if the core is operating at either HS or FS.	
OTGInt	[2]	R	OTG Interrupt The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.	0x0
ModeMis	[1]	RW	Mode Mismatch Interrupt The core sets this bit if the application is trying to access: A Host mode register, if the core is operating in Device mode A Device mode register, if the core is operating in Host mode	0x0
CurMod	[0]	R	Current Mode Of Operation Indicates the current mode of operation. 0 = Device mode 1 = Host mode	0x0

25.7.1.1.7 GINTMSK

- Base Address: 0xC004_0000
- Address = Base Address + 0x0018, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
WkUpIntMsk	[31]	RW	Resume/ Remote Wakeup Detected Interrupt Mask	0x0
SessReqIntMsk	[30]	RW	Session Request/ New Session Detected Interrupt Mask	0x0
DisconnIntMsk	[29]	RW	Disconnect Detected Interrupt Mask	0x0
ConIDStsChngMsk	[28]	RW	Connector ID Status Change Mask	0x0
RSVD	[27]	–	Reserved	–
PTxFEmpMsk	[26]	RW	Periodic TxFIFO Empty Mask	0x0
HChIntMsk	[25]	RW	Host Channels Interrupt Mask	0x0
PrtIntMsk	[24]	RW	Host Port Interrupt Mask	0x0
RSVD	[23]	–	Reserved	–
FetSuspMsk	[22]	RW	Data Fetch Suspended Mask	0x0
incomplPMsk	[21]	RW	Incomplete Periodic Transfer Mask RW	0x0
incompISOOUTMsk			Incomplete Isochronous OUT Transfer Mask	
incompISOINMsk	[20]	RW	Incomplete Isochronous IN Transfer Mask	0x0
OEPIntMsk	[19]	RW	OUT Endpoints Interrupt Mask	0x0
INEPIntMsk	[18]	RW	IN Endpoints Interrupt Mask	0x0
EPMisMsk	[17]	RW	Endpoint Mismatch Interrupt Mask	0x0

Name	Bit	Type	Description	Reset Value
RSVD	[16]	–	Reserved	–
EOPFMsk	[15]	RW	End of Periodic Frame Interrupt Mask	0x0
ISOOutDropMsk	[14]	RW	Isochronous OUT Packet Dropped Interrupt Mask	0x0
EnumDoneMsk	[13]	RW	Enumeration Done Mask	0x0
USBRstMsk	[12]	RW	USB Reset Mask	0x0
USBSuspMsk	[11]	RW	USB Suspend Mask	0x0
ErlySuspMsk	[10]	RW	Early Suspend Mask	0x0
RSVD	[9]	–	Reserved	–
RSVD	[8]	–	Reserved	–
GOUTNakEffMsk	[7]	RW	Global OUT NAK Effective Mask	0x0
GINNakEffMsk	[6]	RW	Global Non-Periodic IN NAK Effective Mask	0x0
NPTxFEmpMsk	[5]	RW	Non-Periodic TxFIFO Empty Mask	0x0
RxFLvlMsk	[4]	RW	Receive FIFO Non-Empty Mask	0x0
SofMsk	[3]	RW	Start of (micro)Frame Mask	0x0
OTGIntMsk	[2]	RW	OTG Interrupt Mask	0x0
ModeMisMsk	[1]	RW	Mode Mismatch Interrupt Mask	0x0
RSVD	[0]	–	Reserved	–

25.7.1.1.8 GRXSTSR (Host Mode)

- Base Address: 0xC004_0000
- Address = Base Address + 0x001C, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	–	Reserved	–
PktSts	[20:17]	R	Packet Status Indicates the status of the received packet. 2 = IN data packet received 3 = IN transfer completed (triggers an interrupt) 5 = Data toggle error (triggers an interrupt) 7 = Channel halted (triggers an interrupt) others = Reserved	–
DPID	[16:15]	R	Data PID Indicates the Data PID of the received packet. 0 = DATA0 2 = DATA1 1 = DATA2 3 = MDATA	–
BCnt	[14:4]	R	Byte Count Indicates the byte count of the received IN data packet.	–
ChNum	[3:0]	R	Channel number Indicates the channel number to which the current receivedpacket belongs.	–

25.7.1.1.9 GRXSTSP (Device Mode)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0020, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:25]	–	Reserved	0x3F
FN	[24:21]	R	Frame Number This is the least significant 4 bits of the (micro) frame number in which the packet is received on the USB. This field is supported if isochronous OUT endpoints are supported.	0xF
PktSts	[20:17]	R	Packet Status Indicates the status of the received packet. 1 = Global OUT NAK (triggers an interrupt) 2 = OUT data packet received 3 = OUT transfer completed (triggers an interrupt) 4 = SETUP transaction completed (triggers an interrupt) 6 = SETUP data packet received others = Reserved	0xF
DPID	[16:15]	R	Data PID Indicates the Data PID of the received OUT data packet. 0 = DATA0 2 = DATA1 1 = DATA2 3 = MDATA	0x3
BCnt	[14:4]	R	Byte Count Indicates the byte count of the received data packet.	0x3FF
EPNum	[3:0]	R	Endpoint number Indicates the endpoint number to which the current received packet belongs.	0xF

25.7.1.1.10 GRXFSIZ

- Base Address: 0xC004_0000
- Address = Base Address + 0x0024, Reset Value = 0x0000_1800

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
RxFDep	[15:0]	RW	RxFIFO Depth This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 6144 The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. A new value must be written to this field. Programmed values must not exceed the power-on value set.	0x1800

25.7.1.1.11 GNPTXFSIZ

- Base Address: 0xC004_0000
- Address = Base Address + 0x0028, Reset Value = 0x1800_1800

Name	Bit	Type	Description	Reset Value
NPTxFDep	[31:16]	RW	Non-Periodic TxFIFO Depth This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32768 The power-on reset value of this register is specified as the Largest Non-Periodic Tx Data FIFO Depth (6144). A new value must be written to this field. Programmed values must not exceed the power-on value set.	0x1800
NPTxFStAddr	[15:0]	RW	Non-Periodic Transmit Start Address This field contains the memory start address for Non-Periodic Transmit FIFO RAM. The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth (6144). A new value must be written to this field. Programmed values must not exceed the power-on value set.	0x1800

25.7.1.1.12 GNPTXSTS

- Base Address: 0xC004_0000
- Address = Base Address + 0x002C, Reset Value = 0x0008_1800

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	–
NPTxQTop	[30:24]	R	Top of the Non-Periodic Transmit Request Queue. Entry in the Non-Periodic Tx Request Queue that is currently being processed by the MAC. Bits[30:27]: Channel/ endpoint number Bits[26:25]: 0 = IN/ OUT token 1 = Zero-length transmit packet (device IN/host OUT) 2 = PING/CSPLIT token 3 = Channel halt command Bit[24] = Terminate (last entry for selected channel/endpoint)	0x0
NPTxQSpcAvail	[23:16]	R	Non-Periodic Transmit Request Queue Space Available. Indicates the amount of free space available in the Non-Periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. 8'h0 = Non-Periodic Transmit Request Queue is full 8'h1 = 1 location available 8'h2 = 2 locations available : n locations available(0 ≤ n ≤ 8) Others = Reserved	0x8
NPTxFSpcAvail	[15:0]	R	Non-Periodic TxFIFO Space Available Indicates the amount of free space available in the Non-Periodic TxFIFO. Values are in terms of 32-bit words. 0 = Non-Periodic TxFIFO is full 1 = 1 word available 2 = 2 words available : n words available (where 0 ≤ n ≤ 32768) 0x8000 = 32768 words available Others = Reserved	0x1800

25.7.1.1.13 HPTXFSIZ

- Base Address: 0xC004_0000
- Address = Base Address + 0x0100, Reset Value = 0x0300_5A00

Name	Bit	Type	Description	Reset Value
PTxFSize	[31:16]	RW	Host Periodic TxFIFO Depth This value is in terms of 32-bit words Minimum value is 16 Maximum value is 6144 A new value must be written to this field. Programmed values must not exceed the Maximum value.	0x0300
PTxFStAddr	[15:0]	RW	Host Periodic TxFIFO Start Address The power-on reset value of this register is sum of the Largest Rx Data FIFO Depth and Largest Non -Periodic TxData FIFO Depth specified. If you have programmed new values for the RxFIFO or Non-Periodic TxFIFO, write their sum in this field. Programmed values must not exceed the power-on value.	0x5A00

25.7.1.1.14 DPTXFSIZn (DPTXFSIZ1, DPTXFSIZ2, …, DPTXFSIZ15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0104 + (n-1) × 0x4, Reset Value = 0x0300_1000, …, 0x0300_4800

Name	Bit	Type	Description	Reset Value
DPTxFSize	[31:16]	RW	Device Periodic TxFIFO Size This value is in terms of 32-bit words Minimum value is 4 Maximum value is 768 The power-on reset value of this register is the Largest Device Mode Periodic Tx Data FIFO-n Depth. Write a new value to this field.	n:1 (0x0300) n:2 (0x0300) n:3 (0x0300) n:4 (0x0300) n:5 (0x0300) n:6 (0x0300) n:7 (0x0300) n:8 (0x0300) n:9 (0x0300) n:10(0x0300) n:11(0x0300) n:12(0x0300) n:13(0x0300) n:14(0x0300) n:15(0x0300)
DPTxFStAddr	[15:0]	RW	Device Periodic TxFIFO RAM Start Address Holds the start address in the RAM for this periodic FIFO. The power-on reset value of this register is sum of the Largest Rx Data FIFO Depth, Largest Non-Periodic Tx Data FIFO Depth, and all lower numbered Largest Device Mode Periodic Tx Data FIFOn Depth specified. If you have programmed new values for the RxFIFO, Non-Periodic TxFIFO, or device Periodic TxFIFOs, write their sum in this field. Programmed values must not exceed the power-on value set.	n:1 (0x1000) n:2 (0x3300) n:3 (0x3600) n:4 (0x3900) n:5 (0x3C00) n:6 (0x3F00) n:7 (0x4200) n:8 (0x4500) n:9 (0x4800) n:10(0x4B00) n:11(0x4E00) n:12(0x5100) n:13(0x5400) n:14(0x5700) n:15(0x5A00)

25.7.1.2 Host Mode Registers (USB_OTG_HMCSR)

25.7.1.2.1 HCFG

- Base Address: 0xC004_0000
- Address = Base Address + 0x0400, Reset Value = 0x0020_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	–	Reserved	0x0040000
FSLSSupp	[2]	RW	FS- and LS- Only Support The application uses this bit to control the core's enumeration speed. Using this bit, the application makes the core enumerate as a FS host, even if the connected device supports HS traffic. Do not make changes to this field after initial programming. 0 = HS/FS/LS, based on the maximum speed supported by the connected device 1 = FS/LS -only, even if the connected device can support HS	0x0
FSLSPclkSel	[1:0]	RW	FS/ LS PHY Clock Select If the core is in FS Host mode 0 = PHY clock is 30/60 MHz 1 = PHY clock is 48 MHz Others = Reserved If the core is in LS Host mode 0 = PHY clock is 30/60 MHz 1 = PHY clock is 48 MHz 2 = PHY clock is 6 MHz 3 = Reserved	–

25.7.1.2.2 HFIR

- Base Address: 0xC004_0000
- Address = Base Address + 0x0404, Reset Value = 0x0000_17D7

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
FrInt	[15:0]	RW	Frame Interval The value that the application programs to this field specifies the interval between two consecutive SOFs (FS) or micro-SOFs (HS)or Keep-Alive tokens (HS). This field contains the number of PHY clocks that constitute the required frame interval. The default value set in this field for a FS operation if the PHY clock frequency is 60MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/ LS PHY Clock Select field of the Host Configuration register (HCFG.FSLSPclkSel). Do not change the value of this field after the initial configuration. 125µs × (PHY clock frequency for HS) 1 ms × (PHY clock frequency for FS/LS)	0x17D7

25.7.1.2.3 HFNUM

- Base Address: 0xC004_0000
- Address = Base Address + 0x0408, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FrRem	[31:16]	R	Frame Time Remaining Indicates the amount of time remaining in the current micro frame (HS) or frame (FS/ LS), in terms of PHY clocks. This field decrements on each PHY clock. If it reaches zero, this field is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB.	0x0
FrNum	[15:0]	R	Frame Number This field increment if a new SOF is transmitted on the USB, and is reset to 0 if it reaches 0x3FFF.	0x0

25.7.1.2.4 HPTXSTS

- Base Address: 0xC004_0000
- Address = Base Address + 0x0410, Reset Value = 0x0008_0100

Name	Bit	Type	Description	Reset Value
PTxQTop	[31:24]	R	Top of the Periodic Transmit Request Queue This indicates the entry in the Periodic Tx Request Queue that is currently being processes by the MAC. This register is used for debugging. Bit [31]: Odd/Even (micro) frame 0 = Send in even (micro) frame 1 = Send in odd (micro) frame Bits [30:27]: Channel/endpoint number Bits [26:25]: Type 0 = IN/OUT 1 = Zero-length packet 2 = CSPLIT 3 = Disable channel command Bit[24]: Terminate	0x0
PTxQSpcAvail	[23:16]	R	Periodic Transmit Request Queue Space Available Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests.	0x8

Name	Bit	Type	Description	Reset Value
			0 = Periodic Transmit Request Queue is full 1 = 1 location available 2 = 2 location available : n locations available (0 ≤ n ≤ 8) Others = Reserved	
PTxFSpcAvail	[15:0]	R	Periodic Transmit Data FIFO Space Available Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words 0 = Periodic TxFIFO is full 1 = 1 word available 2 = 2 words available n: n words available (0 ≤ n ≤ 8) Others = Reserved	0x0100

25.7.1.2.5 HAINT

- Base Address: 0xC004_0000
- Address = Base Address + 0x0414, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
HAINT	[15:0]	R	Channel Interrupts One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15	0x0

25.7.1.2.6 HAINTMSK

- Base Address: 0xC004_0000
- Address = Base Address + 0x0418, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
HAINTMsk	[15:0]	RW	Channel Interrupt Mask One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15	0x0

25.7.1.2.7 HPRT

- Base Address: 0xC004_0000
- Address = Base Address + 0x0440, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:19]	–	Reserved	–
PrtSpd	[18:17]	R	Port Speed Indicates the speed of the device attached to this port. 0 = High speed 1 = Full speed 2 = Low speed 3 = Reserved	0x0
PrtTstCtl	[16:13]	RW	Port Test Control The application writes a nonzero value to this field to put the port into a Test mode, and the corresponding pattern is signaled on the port. 0 = Test mode disabled 1 = Test_J mode 2 = Test_K mode 3 = Test_SE0_NAK mode 4 = Test_Packet mode 5 = Test_Force_Enable Others = Reserved	0x0
PrtPwr	[12]	RW	Port Power The application uses this field to control power to this port, and the core clears this bit on an over current condition. 0 = Power off 1 = Power on	0x0
PrtLnSts	[11:10]	R	Port Line Status Indicates the current logic level USB data lines Bit [10]: Logic level of D? Bit [11]: Logic level of D+	0x0
RSVD	[9]	–	Reserved	–
PrtRst	[8]	RW	Port Reset If the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. 0 = Port not in reset 1 = Port in reset The application must leave this bit set for at least a minimum duration mentioned	0x0

Name	Bit	Type	Description	Reset Value
			below to start a reset on the port. The application can leave it set for another 10ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit set by the USB standard. High speed: 50 ms Full speed/Low speed: 10 ms	
prtSusp	[7]	RW	Port Suspend The application sets this bit to put this port in Suspend mode. The core stops sending SOFs if this is set. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the suspend input pin of the PHY. The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register. 0 = Port not in Suspend mode 1 = Port in Suspend mode	0x0
PrtRes	[6]	RW	Port Resume The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/ Remote Wakeup Detected Interrupt bit of the Core Interrupt register, the core starts driving resume signaling without application intervention and clears this bit if it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. 0 = No resume driven 1 = Resume driven	0x0
PrtOvrCurrChng	[5]	RW	Port Over current Change The core sets this bit if the status of the Port Over current Active bit (bit 4) in this register changes.	0x0
PrtOvrCurrAct	[4]	R	Port Over current Active Indicates the over current condition of the	0x0

Name	Bit	Type	Description	Reset Value
			port. 0 = No over current condition 1 = Over current condition	
PrtEnChng	[3]	RW	Port Enable/Disable Change The core sets this bit if the status of the Port Enable bit[2] of this register changes.	0x0
PrtEna	[2]	RW	Port Enable A port is enabled by the core after a reset sequence, and is disabled by an over current condition, a disconnect condition, or by the application clearing this bit. The application cannot set this bit by a register write. It clears it to disable the port. This bit does not trigger any interrupt to the application. 0 = Port disabled 1 = Port enabled	0x0
PrtConnDet	[1]	RW	Port Connect Detected The core sets this bit if a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register. The application must write a 1 to this bit to clear the interrupt.	0x0
PrtConnSts	[0]	R	Port Connect Status 0 = No device is attached to the port 1 = A device is attached to the port	0x0

25.7.1.2.8 HCCHARn (0 ≤ n ≤ 15, HCCHAR0, HCCHAR1, …, HCCHAR15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0500 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ChEna	[31]	RW	Channel Enable This field is set by the application and cleared by the OTG host. 0 = Disables Channel 1 = Enables Channel	0x0
ChDis	[30]	RW	Channel Disable The application sets this bit to stop transmitting/ receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled.	0x0
OddFrm	[29]	RW	Odd Frame This field is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro) frame. This field is applicable for only periodic transactions. 0 = Even (micro)frame 1 = Odd (micro)frame	0x0
DevAddr	[28:22]	RW	Device Address This field selects the specific device serving as the data source or sink.	0x0
MC/EC	[21:20]	RW	Multi Count/Error Count If the Split Enable bit of the Host Channel-n Split Control register is reset (1'b0), this field indicates to the host the number of transactions that must be executed per micro frame for this endpoint. 0 = Reserved 1 = 1 transaction 2 = 2 transactions to be issued for this endpoint per micro frame 3 = 3 transactions to be issued for this endpoint per micro frame If HCSPLTn.SpltEna is set, this field indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This field must be set to at least 0x1.	0x0
EPType	[19:18]	RW	Endpoint Type Indicates the transfer type selected. 0 = Control	0x0

Name	Bit	Type	Description	Reset Value
			1 = Isochronous 2 = Bulk 3 = Interrupt	
LSpdDev	[17]	RW	Low-Speed Device This field is set by the application to indicate that this channel is communicating to a low-speed device.	0x0
RSVD	[16]	–	Reserved	–
EPDir	[15]	RW	Endpoint Direction Endpoint Type Indicates the transfer type selected. 0 = OUT 1 = IN	0x0
EPNum	[14:11]	RW	Endpoint Number Indicates the endpoint number on the device serving as the data source or sink.	0x0
MPS	[10:0]	RW	Maximum Packet Size Indicates the maximum packet size of the associated endpoint.	0x0

25.7.1.2.9 HCSPLTn (0 ≤ n ≤ 15, HCSPLT0, HCSPLT1, …, HCSPLT15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0504 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
SpltEna	[31]	RW	Split Enable The application sets this field to indicate that this channel is enabled to perform split transactions.	0x0
RSVD	[30:17]	–	Reserved	–
CompSplt	[16]	RW	Do Complete Split The application sets this field to request the OTG host to perform a complete split transaction.	0x0
XactPos	[15:14]	RW	Transaction Position This field is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. 3 = All. This is the entire data payload is of this transaction. 2 = Begin. This is the first data payload of this transaction. 0 = Mid. This is the middle payload of this transaction. 1 = End. This is the last payload of this	0x0

Name	Bit	Type	Description	Reset Value
			transaction.	
HubAddr	[13:7]	RW	Hub Address This field holds the device address of the transaction translator's hub.	0x0
PrtAddr	[6:0]	RW	Port Address This field is the port number of the recipient transaction translator.	0x0

25.7.1.2.10 HCINTn (0 ≤ n ≤ 15, HCINT0, HCINT1, …, HCINT15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0508 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	–
DataTglErr	[10]	RW	Data Toggle Error	0x0
FrmOvrun	[9]	RW	Frame Overrun	0x0
BblErr	[8]	RW	Babble Error	0x0
XactErr	[7]	RW	Transaction Error	0x0
NYET	[6]	RW	NYET Response Received Interrupt	0x0
ACK	[5]	RW	ACK Response Received Interrupt	0x0
NAK	[4]	RW	NAK Response Received Interrupt	0x0
STALL	[3]	RW	STALL Response Received Interrupt	0x0
AHBErr	[2]	RW	AHB Error This is generated only in Internal DMA mode if there is an AHB error during AHB read/ writes. The application reads the corresponding channel's DMA address register to get the error address.	0x0
ChHltd	[1]	RW	Channel Halted Indicates the incomplete transfer either because of any USB transaction error or in response to disable request by the application.	0x0
XferCompl	[0]	RW	Transfer Completed Transfer completed normally without any errors.	0x0

25.7.1.2.11 HCINTMSKn (0 ≤ n ≤ 15, HCINTMSK0, HCINTMSK1, …, HCINTMSK15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x050C + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	–	Reserved	–
DataTglErrMsk	[10]	RW	Data Toggle Error Mask	0x0
FrmOvrunMsk	[9]	RW	Frame Overrun Mask	0x0
BblErrMsk	[8]	RW	Babble Error Mask	0x0
XactErrMsk	[7]	RW	Transaction Error Mask	0x0
NyetMsk	[6]	RW	NYET Response Received Interrupt Mask	0x0
AckMsk	[5]	RW	ACK Response Received Interrupt Mask	0x0
NakMsk	[4]	RW	NAK Response Received Interrupt Mask	0x0
StallMsk	[3]	RW	STALL Response Received Interrupt Mask	0x0
AHBErrMsk	[2]	RW	AHB Error Mask	0x0
ChHltdMsk	[1]	RW	Channel Halted Mask	0x0
XferComplMsk	[0]	RW	Transfer Completed Mask	0x0

25.7.1.2.12 HCTSIZn (0 ≤ n ≤ 15, HCTSIZ0, HCTSIZ1, …, HCTSIZ15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0510 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DoPng	[31]	RW	Do Ping Setting this field to 1 directs the host to do PING protocol.	0x0
Pid	[30:29]	RW	PID The application programs this field with the type of PID to use for the initial transaction. The host maintains this field for the rest of the transfer. 0 = DATA0 1 = DATA1 2 = DATA2 3 = MDATA (non-control)/ SETUP(control)	0x0
PktCnt	[28:19]	RW	Packet Count This field is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN).The host decrements this count on every successful transmission or reception of an OUT/ IN packet. Once this	0x0

Name	Bit	Type	Description	Reset Value
			count reaches zero, the application is interrupted to indicate normal completion.	
XferSize	[18:0]	RW	Transfer Size For an OUT, this field is the number of data bytes the host sends during the transfer. For an IN, this field is the buffer size that the application has reserved for the transfer. The application is expected to program this field as an integer multiple of the maximum packet size for IN transactions.	0x0

25.7.1.2.13 HCDMAn (0 ≤ n ≤ 15, HCDMA0, HCDMA1, …, HCDMA15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0514 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DMAAddr	[31:0]	RW	DMA Address This field holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction.	0x0

25.7.1.3 Device Mode Registers (USB_OTG_DMCSR)

25.7.1.3.1 DCFG

- Base Address: 0xC004_0000
- Address = Base Address + 0x0800, Reset Value = 0x0020_0000

Name	Bit	Type	Description	Reset Value
ResValid	[31:26]	RW	Resume Validation Period This field controls the period when the core resumes from a suspend. When this bit is set, the core counts for the ResValid number of clock cycles to detect a valid resume. This field is effective only when DCFG.Ena32kHzSusp is set.	0x2
PerSchIntvl	[25:24]	RW	Periodic Scheduling Interval PerSchIntvl must be programmed only for Scatter/Gather DMA mode. Description: This field specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25, 50 or 75 % of (micro) frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data. When no periodic endpoints are active, then the internal DMA engine services non-periodic endpoints, ignoring this field. After the specified time within a (micro) frame, the DMA switches to fetching for non-periodic endpoints. 2'b00 = 25% of (micro) frame. 2'b01 = 50% of (micro) frame. 2'b10 = 75% of (micro) frame. 2'b11 = Reserved.	0x0
DescDMA	[23]	RW	Enable Scatter/Gather DMA in Device mode When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available	0x0

Name	Bit	Type	Description	Reset Value
			for programming: • GAHBCFG.DMAEn=0,DCFG.DescDMA=0 → Slave mode • GAHBCFG.DMAEn=0,DCFG.DescDMA=1 → Invalid • GAHBCFG.DMAEn=1,DCFG.DescDMA=0 → Buffered DMA mode • GAHBCFG.DMAEn=1,DCFG.DescDMA=1 → Scatter/Gather DMA mode	
EPMisCnt	[22:18]	RW	IN Endpoint Mismatch Count The application programs this field with a count that determines when the core generates an Endpoint Mismatch interrupt. The core loads this value into an internal counter and decrements it. The counter is reloaded whenever there is a match or if the counter expires. The width of this counter depends on the depth of the Token Queue.	0x8
RSVD	[17:13]	–	Reserved	–
PerFrInt	[12:11]	RW	Periodic Frame Interval Indicates the time within a (micro) frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro) frame is complete. 0 = 80% of the (micro) frame interval 1 = 85% 2 = 90% 3 = 95%	0x0
DevAddr	[10:4]	RW	Device Address The application must program this field after every Set Address control command.	0x0
Ena32KHzS	[3]	RW	Enable 32 kHz Suspend Mode When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48 MHz PHY clock to be switched to 32 kHz during a suspend. This bit can only be set if USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero.	0x0
NZStsOUTHShk	[2]	RW	Non-Zero-Length Status OUT Handshake The application can use this field to select	0x0

Name	Bit	Type	Description	Reset Value
			the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. 1'b1 = Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. 1'b0 = Send the received OUT packet to the application (zero-length or nonzero length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.	
DevSpd	[1:0]	RW	Device Speed. Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 2'b00 = High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b01 = Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b10 = Low speed (USB 1.1 FS transceiver clock is 48 MHz) 2'b11 = Full speed (USB 1.1 FS transceiver clock is 48 MHz)	0x0

25.7.1.3.2 DCTL

- Base Address: 0xC004_0000
- Address = Base Address + 0x0804, Reset Value = 0x0020_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	–
NakOnBble	[16]	RW	Set NAK automatically on babble The core sets NAK automatically for the endpoint on which babble is received.	0x0
IgnrFrmNum	[15]	RW	Ignore frame number for isochronous endpoints Slave Mode (GAHBCFG.DMAEn = 0): This bit is not valid in Slave mode and should not be programmed to 1. Non-Scatter/Gather DMA mode (GAHBCFG.DMAEn = 1,DCFG.DescDMA = 0): This bit is not used when Threshold mode is enabled and should not be programmed to 1. In non-Scatter/Gather DMA mode, the application receives transfer complete interrupt after transfers for multiple (micro) frames are completed. When Scatter/Gather DMA mode is disabled, this field is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple (micro) frames. 0 = Periodic transfer interrupt feature is disabled; the application must program transfers for periodic endpoints every (micro) frame 1 = Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. This field is also used by the application to enable periodic transfer interrupts. Scatter/Gather DMA Mode (GAHBCFG.DMAEn = 1,DCFG.DescDMA = 1): This bit is not applicable to high-speed, high-bandwidth transfers and should not be programmed to 1. In addition, this bit is not used when Threshold mode is enabled and should not be programmed to 1. 0 = The core transmits the packets only in the frame number in which they are intended to be transmitted. 1 = Packets are not flushed when an ISOC IN token is received for an elapsed frame. The core ignores the frame number, sending packets as soon as the packets are ready, and the corresponding token is received. When this bit is set, there must be only one packet per	0x0

Name	Bit	Type	Description	Reset Value
			descriptor.	
GMC	[14:13]	RW	Global Multi Count GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets tobe serviced for that end point before moving to the next end point. It is only for non periodic endpoints. 2'b00 = Invalid. 2'b01 = 1 packet. 2'b10 = 2 packets. 2'b11 = 3 packets. The value of this field automatically changes to 2'h1 when DCFG.DescDMA is set to 1. When Scatter/Gather DMA mode is disabled, this field is reserved and reads 2'b00.	0x0
RSVD	[12]	–	Reserved	–
PWROnPrgDone	[11]	RW	Power-On Programming Done The application uses this bit to indicate that register programming is complete after a wake-up from Power Down mode.	0x0
CGOUTNak	[10]	W	Clear Global OUT NAK A write to this field clears the Global OUT NAK.	0x0
SGOUTNak	[9]	W	Set Global OUT NAK A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set this bit after making sure that the Global OUT NAK Effective bit in Core Interrupt Register is cleared.	0x0
CGNPInNAK	[8]	W	lear Global Non-Periodic IN NAK A write to this field clears the Global Non-Periodic IN NAK.	0x0
SGNPInNAK	[7]	W	Set Global Non-Periodic IN NAK A write to this field sets the Global Non-Periodic IN NAK. The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core sets this bit if a timeout condition is detected on a non-periodic endpoint. The application must set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register is cleared.	0x0
TstCtl	[6:4]	RW	Test Control 0 = Test mode disabled 1 = Test_J mode 2 = Test_K mode 3 = Test_SE0_NAK mode 4 = Test_Packet mode 5 = Test_Force_Enable	0x0

Name	Bit	Type	Description	Reset Value
			Others = Reserved	
GOUTNakSts	[3]	R	Global OUT NAK Status 0 = A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1 = No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped.	0x0
GNPINNakSts	[2]	R	Global Non-Periodic IN NAK Status 0 = A handshake is sent based on the data availability in the transmit FIFO. 1 = A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.	0x0
SftDiscon	[1]	RW	Soft Disconnect The application uses this bit to signal the OTG core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device will not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. 0 = Normal operation. If this bit is cleared after a soft disconnect, the core drives the op mode signal on the UTMI+ to 0x0, which generates a device connect event to the USB host. If the device is reconnected, the USB host restarts device enumeration. 1 = The core drives the op mode signal on the UTMI+ to 0x1, which generates a device disconnect event to the USB host.	0x0
RmtWkUpSig	[0]	RW	Remote Wakeup Signaling If the application sets this bit, the core initiates remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1 to 15 ms after setting it.	0x0

25.7.1.3.3 DSTS

- Base Address: 0xC004_0000
- Address = Base Address + 0x0808, Reset Value = 0x0000_0002

Name	Bit	Type	Description	Reset Value
RSVD	[31:22]	–	Reserved	–
SOFFN	[21:8]	R	Frame or Micro frame Number of the Received SOF If the core is operating at high speed; this field contains a micro frame number. If the core is operating at full or low speed, this field contains a frame number.	0x0
RSVD	[7:4]	–	Reserved	–
ErrticErr	[3]	R	The core sets this bit to report any erratic errors seen on the UTMI+. Due to erratic errors, the OTG core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register. If the early suspend is asserted due to an erratic error, the application performs a soft disconnect recover.	0x0
EnumSpd	[2:1]	R	Enumerated Speed Indicates the speed at which the OTG core has come up after speed detection through a chirp sequence. 0 = High speed (PHY clock is 30 MHz or 60 MHz) 1 = Full speed (PHY clock is 30 MHz or 60 MHz) 2 = Low speed (PHY clock is 6 MHz). 3 = Full speed (PHY clock is 48 MHz). Low speed is not supported for devices using a UTMI+ PHY.	0x1
SuspSts	[0]	R	Suspend Status In device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state if there is no activity on the line_state signal for an extended period of time. The core comes out of the suspend: If there is any activity on the line_state signal If the application writes to the Remote Wakeup Signaling bit in the Device Control register.	0x0

25.7.1.3.4 DIEPMSK

- Base Address: 0xC004_0000
- Address = Base Address + 0x0810, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:14]	–	Reserved	–
NAKMsk	[13]	RW	NAK interrupt Mask	0x0
RSVD	[12:10]	–	Reserved	–
BNAInIntrMsk	[9]	RW	BNA Interrupt Mask This bit is valid only when Device Descriptor DMA is enabled.	0x0
TxfifoUndrnMsk	[8]	RW	Fifo Under run Mask	0x0
RSVD	[7]	–	Reserved	–
INEPNakEffMsk	[6]	RW	IN Endpoint NAK Effective Mask	0x0
INTknEPMisMsk	[5]	RW	IN Token received with EP Mismatch Mask	0x0
INTknTXFEmpMsk	[4]	RW	IN Token received with TxFIFO Empty mask	0x0
TimeOUTMsk	[3]	RW	Timeout Condition Mask	0x0
AHBErrMsk	[2]	RW	AHB Error Mask	0x0
EPDisbldMsk	[1]	RW	Endpoint Disabled Interrupt Mask	0x0
XferComplMsk	[0]	RW	Transfer Completed Interrupt Mask	0x0

25.7.1.3.5 DOEPMSK

- Base Address: 0xC004_0000
- Address = Base Address + 0x0814, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	–	Reserved	–
NYETMsk	[14]	RW	NYET Interrupt Mask	0x0
NAKMsk	[13]	RW	NAK Interrupt Mask	0x0
BbleErrMsk	[12]	RW	Babble Interrupt Mask	0x0
RSVD	[11:10]	–	Reserved	–
BnaOutIntrMsk	[9]	RW	BNA interrupt Mask	0x0
OutPktErrMsk	[8]	RW	OUT Packet Error Mask	0x0
RSVD	[7]	–	Reserved	–
Back2BackSETup	[6]	RW	Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only.	0x0
RSVD	[5]	–	Reserved	–
OUTTknEPdisMsk	[4]	RW	OUT Token Received When Endpoint Disabled Applies to control OUT endpoints only.	0x0
SetUPMsk	[3]	RW	SETUP Phase Done Mask Applies to control endpoints only.	0x0
AHBErrMsk	[2]	RW	AHB Error	0x0
EPDisbldMsk	[1]	RW	Endpoint Disabled Interrupt Mask	0x0
XferComplMsk	[0]	RW	Transfer Completed Interrupt Mask	0x0

25.7.1.3.6 DAINT

- Base Address: 0xC004_0000
- Address = Base Address + 0x0818, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
OutEPInt	[31:16]	R	OUT Endpoint Interrupt Bits One bit per OUT endpoint : Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15	0x0
InEpInt	[15:0]	R	IN Endpoint Interrupt Bits One bit per IN endpoint : Bit 0 for IN endpoint 0, bit 15 for endpoint 15	0x0

25.7.1.3.7 DAINTMSK

- Base Address: 0xC004_0000
- Address = Base Address + 0x081C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
OutEPMsk	[31:16]	RW	OUT EP Interrupt Mask Bits One bit per OUT endpoint : Bit 16 for OUT EP 0, bit 31 for OUT EP 15	0x0
InEpMsk	[15:0]	RW	IN EP Interrupt Mask Bits One bit per IN endpoint : Bit 0 for IN EP 0, bit 15 for IN EP 15	0x0

25.7.1.3.8 DTKNQR1

- Base Address: 0xC004_0000
- Address = Base Address + 0x0820, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EPTkn	[31:8]	R	Endpoint Token Four bits per token represent the endpoint number of the token: • Bits [31:28]: Endpoint number of Token 5 • Bits [27:24]: Endpoint number of Token 4 … • Bits [15:12]: Endpoint number of Token 1 • Bits [11:8]: Endpoint number of Token 0	0x0
WrapBit	[7]	R	Wrap Bit This bit is set if the write pointer wraps. It is cleared if the learning queue is cleared.	0x0
RSVD	[6:5]	–	Reserved	–
INTKnWPtr	[4:0]	R	IN Token QUEUE Write Pointer	0x0

25.7.1.3.9 DTKNQR2

- Base Address: 0xC004_0000
- Address = Base Address + 0x0824, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EPTkn	[31:0]	R	Endpoint Token Four bits per token represent the endpoint number of the token: • Bits [31:28]: Endpoint number of Token 13 • Bits [27:24]: Endpoint number of Token 12 .. • Bits [7:4]: Endpoint number of Token 7 • Bits [3:0]: Endpoint number of Token 6	0x0

25.7.1.3.10 DVBUSDIS

- Base Address: 0xC004_0000
- Address = Base Address + 0x0828, Reset Value = 0x0000_17D7

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
DVBUSDis	[15:0]	RW	Device VBUS Discharge Time Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals: • VBUS discharge time in PHY clocks /1,024	0x17D7

25.7.1.3.11 DVBUSPULSE

- Base Address: 0xC004_0000
- Address = Base Address + 0x082C, Reset Value = 0x0000_05B8

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
DVBUSPulse	[15:0]	RW	Device VBUS Pulsing Time Specifies the VBUS pulsing time during SRP. This value equals : • VBUS pulse time in PHY clocks /1,024	0x5B8

25.7.1.3.12 DTKNQR3

- Base Address: 0xC004_0000
- Address = Base Address + 0x0830, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EPTkn	[31:0]	R	Endpoint Token Four bits per token represent the endpoint number of the token: • Bits [31:28]: Endpoint number of Token 21 • Bits [27:24]: Endpoint number of Token 20 … • Bits [7:4]: Endpoint number of Token 15 • Bits [3:0]: Endpoint number of Token 14	0x0

25.7.1.3.13 DTKNQR4

- Base Address: 0xC004_0000
- Address = Base Address + 0x0834, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EPTkn	[31:0]	R	Endpoint Token Four bits per token represent the endpoint number of the token: • Bits [31:28]: Endpoint number of Token 29 • Bits [27:24]: Endpoint number of Token 28 … • Bits [7:4]: Endpoint number of Token 23 • Bits [3:0]: Endpoint number of Token 22	0x0

25.7.1.3.14 DIEPCTL0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0900, Reset Value = 0x0000_8000

Name	Bit	Type	Description	Reset Value
EPEna	[31]	RW	Endpoint Enable Indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting any of the following interrupts on this endpoint. Endpoint Disabled Transfer Completed	0x0
EPDis	[30]	RW	Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	0x0
RSVD	[29:28]	–	Reserved	–
SetNAK	[27]	W	Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application controls the transmission of NAK handshakes on an endpoint. The core also sets this bit for an endpoint after a SETUP packet is received on that endpoint.	0x0
CNAK	[26]	W	Clear NAK A write to this bit clears the NAK bit for the endpoint.	0x0
TxFNum	[25:22]	R	TxFIFO Number This value is always set to 0, indicating that control IN endpoint0 data is always written in the Non-Periodic Transmit FIFO.	0x0
stall	[21]	RW	STALL Handshake The application sets this bit, and the core clears it, if a SETUP token is received for this endpoint. If a NAK bit, Global Non-Periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.	0x0
RSVD	[20]	–	Reserved	–
EPType	[19:18]	R	Endpoint Type Hardcoded to 00 for control	0x0
NAKsts	[17]	R	NAK Status Indicates the following: 0 = The core is transmitting non-NAK handshakes	0x0

Name	Bit	Type	Description	Reset Value
			based on the FIFO status 1 = The core is transmitting NAK handshakes on this endpoint If this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	
RSVD	[16]	–	Reserved	–
USBActEP	[15]	R	USB Active Endpoint This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.	0x1
NextEp	[14:11]	RW	Next Endpoint Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core accesses this field, even if the Endpoint Enable bit is not set. This field is not valid in Slave mode operation.	0x0
RSVD	[10:2]	–	Reserved	–
MPS	[1:0]	RW	Maximum Packet Size The application must program this field with the maximum packet size for the current logical endpoint. 0 = 64 bytes 1 = 32 bytes 2 = 16 bytes 3 = 8 bytes	0x0

25.7.1.3.15 DIEPINT0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0908, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:7]	–	Reserved	–
INEPNakEff	[6]	R	IN Endpoint NAK Effective Applies to periodic IN endpoints only. Indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This bit is cleared if the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit This interrupt does not necessarily mean that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit.	0x0
INTknEPMis	[5]	RW	IN Token Received with EP Mismatch Applies to periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. For OUT endpoints, this bit is reserved.	0x0
INTknTXFEmp	[4]	RW	IN Token Received When TxFIFO is Empty Applies to non-periodic IN endpoints only. Indicates that an IN token was received when the associated TxFIFO was empty. This interrupt is asserted on the endpoint for which the IN token was received.	0x0
TimeOUT	[3]	RW	Timeout Condition Applies to non-isochronous IN endpoints only. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint.	0x0
AHBErr	[2]	RW	AHB Error This is generated only in Internal DMA mode if there is an AHB error during an AHB read/write. The application reads the corresponding endpoint DMA address register to get the error address.	0x0
EPDisbld	[1]	RW	Endpoint Disabled Interrupt This bit indicates that the endpoint is disabled per the application's request.	0x0
XferCompl	[0]	RW	Transfer Completed Interrupt Indicates that the programmed transfer is complete on	0x0

Name	Bit	Type	Description	Reset Value
			the AHB as well as on the USB, for this endpoint.	

25.7.1.3.16 DIEPTSIZ0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0910, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	–	Reserved	–
PktCnt	[20:19]	RW	Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet is read from the TxFIFO.	0x0
RSVD	[18:7]	–	Reserved	–
XferSize	[6:0]	RW	Transfer Size Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO.	0x0

25.7.1.3.17 DIEPDMA0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0914, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DMAAddr	[31:0]	RW	DMA Address Holds the start address of the external memory for storing or fetching endpoint data. This register is incremented on every AHB transaction. NOTE: For control endpoints, this address stores control OUT data packets as well as SETUP transaction data packets. If multiple SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten.	0x0

25.7.1.3.18 DIEPCTLn (1 ≤ n ≤ 15, DIEPCTL1, DIEPCTL2, …, DIEPCTL15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0900 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EPEna	[31]	RW	Endpoint Enable Applies to IN and OUT endpoints. For IN endpoint, this bit indicates that data is ready to be transmitted on the endpoint. For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: • SETUP Phase Done (OUT only) • Endpoint Disabled • Transfer Complete Transfer Completed NOTE: For control OUT endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.	0x0
EPDis	[30]	RW	Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	0x0
SetD1PID SetOddFr	[29]	W	Set DATA1 PID Applies to interrupt/ bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. Set Odd (micro) frame Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/ Odd (micro) frame field to odd (micro) frame.	0x0
SetD0PID SetEvenFr	[28]	W	Set DATA0 PID Applies to interrupt/ bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. Set Even (micro) frame Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/ Odd (micro) frame field to even (micro) frame.	0x0
SetNAK	[27]	W	Set NAK A write to this bit sets the NAK bit for the endpoint.	0x0

Name	Bit	Type	Description	Reset Value
			Using this bit, the application controls the transmission of NAK handshakes on an endpoint. The core also sets this bit for an endpoint after a SETUP packet is received on that endpoint.	
CNAK	[26]	W	Clear NAK A write to this bit clears the NAK bit for the endpoint.	0x0
TxFNum	[25:22]	RW	TxFIFO Number Applies to IN endpoints only. Non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 0 = Non-Periodic TxFIFO Others = Specified Periodic TxFIFO number NOTE: An interrupt IN endpoint could be configured as a non-periodic endpoint for applications like mass storage.	0x0
stall	[21]	RW	STALL Handshake Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-Periodic In NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application clears this bit, never the core. Applies to control endpoints only The application sets this bit, and the core clears it, if a SETUP token is received for this endpoint. If a NAK bit, Global Non-Periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	0x0
RSVD	[20]	–	Reserved	–
EPType	[19:18]	R	Endpoint Type This is the transfer type supported by this logical endpoint. 0 = Control 1 = Isochronous 2 = Bulk 3 = Interrupt	0x0
NAKsts	[17]	R	NAK Status Indicates the following: 0 = The core is transmitting non-NAK handshakes based on the FIFO status 1 = The core is transmitting NAK handshakes on this endpoint. If either the application or the core sets this bit: The core stops receiving any data on an OUT	0x0

Name	Bit	Type	Description	Reset Value
			endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	
DPID EO_FrNum	[16]	R	Endpoint Data PID Applies to interrupt/ bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. Applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. 0 = DATA0 1 = DATA1 Even/ Odd (Micro) Frame Applies to isochronous IN and OUT endpoints only. Indicates the (micro) frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/ odd (micro) frame number in which it intends to transmit/ receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. 0 = Even (micro) frame 1 = Odd (micro) frame	–
USBActEP	[15]	RW	USB Active Endpoint Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints after detecting a USB reset. After receiving the Set Configuration and Set Interface commands, the application must program endpoint registers accordingly and set this bit.	0x0
NextEp	[14:11]	RW	Next Endpoint Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core accesses this field, even if the Endpoint Enable bit is not set. This field is not valid in Slave mode operation.	0x0
MPS	[10:0]	RW	Maximum Packet Size The application must program this field with the	0x0

Name	Bit	Type	Description	Reset Value
			maximum packet size for the current logical endpoint. This value is in bytes.	

25.7.1.3.19 DIEPINTn (1 ≤ n ≤ 7, DIEPINT1, DIEPINT2, …, DIEPINT7)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0908 + n × 0x20, Reset Value = 0x0000_0080

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	–	Reserved	–
NYETIntrpt	[14]	R	NYET interrupt The core generates this interrupt when a NYET response is transmitted for a non-isochronous OUT endpoint.	0x0
NAKIntrpt	[13]	R	NAK interrupt The core generates this interrupt when a NAK is transmitted. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to unavailability of data in the TXFifo.	0x0
BbleErrIntrpt	[12]	R	BbleErr (Babble Error) interrupt The core generates this interrupt when babble is received for the endpoint.	0x0
PktDrpSts	[11]	R	Packet Dropped Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.	0x0
RSVD	[10]	–	Reserved	–
BNAIntr	[9]	R	PBNA (Buffer Not Available) Interrupt The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Dependency: This bit is valid only when Scatter/Gather DMA mode is enabled.	0x0
TxfifoUndrn	[8]	R	FIFO Under run Applies to IN endpoints only The core generates this interrupt when it detects a transmit FIFO under run condition for this endpoint. Dependency: This interrupt is valid only when both of the following conditions are true: • Parameter OTG_EN_DED_TX_FIFO=1 • Thresholding is enabled	0x0

Name	Bit	Type	Description	Reset Value
TxFEmp	[7]	R	Transmit FIFO Empty This bit is valid only for IN Endpoints This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).	0x0
INEPNakEff	[6]	R	IN Endpoint NAK Effective This bit should be cleared by writing a 1'b1 before writing a 1'b1 to corresponding DIEPCTLn.CNAK. The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled.	0x0
INTknEPMis	[5]	RW	IN Token Received with EP Mismatch Applies to periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received.	0x0
INTknTXFEmp	[4]	RW	IN Token Received When TxFIFO is Empty Indicates that an IN token was received when the associated TxFIFO (periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received.	0x0
TimeOUT	[3]	RW	Timeout Condition • In shared TX FIFO mode, applies to non-isochronous IN endpoints only. • In dedicated FIFO mode, applies only to Control IN endpoints. • In Scatter/Gather DMA mode, the Time OUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint.	0x0
AHBErr	[2]	RW	AHB Error Applies to IN and OUT endpoints. This is generated only in Internal DMA mode if there is an AHB error during an AHB read/write. The application reads the corresponding endpoint DMA address register to get the error address.	0x0
EPDisbld	[1]	RW	Endpoint Disabled Interrupt	0x0

Name	Bit	Type	Description	Reset Value
			Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.	
XferCompl	[0]	RW	Transfer Completed Interrupt Applies to IN and OUT endpoints. • When Scatter/Gather DMA mode is enabled • For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. • For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. • When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.	0x0

25.7.1.3.20 DIEPTSIZn (1 ≤ n ≤ 7, DIEPTSIZ1, DIEPTSIZ2, …, DIEPTSIZ7)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0910 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	–
MC	[30:29]	RW	Multi Count For periodic IN endpoints, this field indicates the number of packets that must be transmitted per micro frame on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. 1 = 1 packet 2 = 2 packets 3 = 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-nControl register	–
PktCnt	[28:19]	RW	Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for endpoint 0. This field is decremented every time a packet is read from the TxFIFO.	0x0
XferSize	[18:0]	RW	Transfer Size This field contains the transfer size in bytes for the current endpoint. The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size is set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet from the external memory is written to the TxFIFO.	0x0

25.7.1.3.21 DIEPDMAn (1 ≤ n ≤ 7, DIEPDMA1, DIEPDMA2, …, DIEPDMA7)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0914 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DMAAddr	[31:0]	RW	DMA Address Holds the start address of the external memory for storing or fetching endpoint data. This register is incremented on every AHB transaction. NOTE: For control endpoints, this address stores control OUT data packets as well as SETUP transaction data packets. If multiple SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten.	0x0

25.7.1.3.22 DOEPCTL0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B00, Reset Value = 0x0000_8000

Name	Bit	Type	Description	Reset Value
EPEna	[31]	RW	Endpoint Enable Indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint. SETUP Phase Done Endpoint Disabled Transfer Complete NOTE: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory. Transfer Completed	0x0
EPDis	[30]	RW	Endpoint Disable The application cannot disable control OUT endpoint 0.	0x0
RSVD	[29:28]	–	Reserved	–
SetNAK	[27]	W	Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application controls the transmission of NAK handshakes on an endpoint. The core also sets this bit for an endpoint after a SETUP packet is received on that endpoint.	0x0
CNAK	[26]	W	Clear NAK A write to this bit clears the NAK bit for the endpoint.	0x0
RSVD	[25:22]	–	Reserved	–
stall	[21]	RW	STALL Handshake	0x0

Name	Bit	Type	Description	Reset Value
			The application sets this bit, and the core clears it, if a SETUP token is received for this endpoint. If a NAK bit or Global OUTNAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	
Snp	[20]	RW	Snoop Mode This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	–
EPType	[19:18]	R	Endpoint Type Hardcoded to 00 for control	0x0
NAKsts	[17]	R	NAK Status Indicates the following: 0 = The core is transmitting non-NAK handshakes based on the FIFO status 1 = The core is transmitting NAK handshakes on this endpoint If this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	0x0
RSVD	[16]	–	Reserved	–
USBActEP	[15]	R	USB Active Endpoint This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.	0x1
RSVD	[14:2]	–	Reserved	–
MPS	[1:0]	R	Maximum Packet Size The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. 0 = 64 bytes 1 = 32 bytes 2 = 16 bytes 3 = 8 bytes	0x0

25.7.1.3.23 DOEPINT0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B08, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:7]	–	Reserved	0x1
Back2BackSETup	[6]	R	Back-to-Back SETUP Packets Received This bit indicates that core has received more than three back-to-back SETUP packets for this particular endpoint.	0x0
RSVD	[5]	–	Reserved	–
OUTTknEPdis	[4]	RW	Token Received When Endpoint Disabled Indicates that an OUT token is received if the endpoint is not enabled. This interrupt is asserted on the endpoint for which the OUT token was received.	0x0
SetUp	[3]	RW	SETUP Phase Done Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application decodes the received SETUP data packet.	0x0
AHBErr	[2]	RW	AHB Error This is generated only in Internal DMA mode if there is an AHB error during an AHB read/write. The application reads the corresponding endpoint DMA address register to get the error address.	0x0
EPDisbld	[1]	RW	Endpoint Disabled Interrupt This bit indicates that the endpoint is disabled per the application's request.	0x0
XferCompl	[0]	RW	Transfer Completed Interrupt Indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.	0x0

25.7.1.3.24 DOEPTSIZ0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B10, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	–
SUPCnt	[30:29]	RW	SETUP Packet Count This field specifies the number of back-to-back SETUP data packets the endpoint can receive. 1 = 1 packet 2 = 2 packets 3 = 3 packets	-
RSVD	[28:20]	–	Reserved	–
PktCnt	[19]	RW	Packet Count This field is decremented to zero after a packet is written into the RxFIFO.	0x0
RSVD	[18:7]	–	Reserved	–
XferSize	[6:0]	RW	Transfer Size Indicates the transfer size in bytes for endpoint 0. The core interrupts the application only after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. The core decrements this field every time a packet is read from RxFIFO and written to the external memory.	0x0

25.7.1.3.25 DOEPDMA0

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B14, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DMAAddr	[31:0]	RW	DMA Address Holds the start address of the external memory for storing or fetching endpoint data. This register is incremented on every AHB transaction. NOTE: For control endpoints, this address stores control OUT data packets as well as SETUP transaction data packets. If multiple SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten.	0x0

25.7.1.3.26 DOEPCTLn (1 ≤ n ≤ 15, DOEPCTL1, DOEPCTL2, …, DOEPCTL15)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B00 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EPEna	[31]	RW	Endpoint Enable For IN endpoint, this bit indicates that data is ready to be transmitted on the endpoint. For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: • SETUP Phase Done (OUT only) • Endpoint Disabled • Transfer Complete Transfer Completed NOTE: For control OUT endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.	0x0
EPDis	[30]	RW	Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.	0x0
SetD1PID SetOddFr	[29]	W	Set DATA1 PID Applies to interrupt/ bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1. Set Odd (micro) frame Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/ Odd (micro) frame field to odd (micro) frame.	0x0
SetD0PID SetEvenFr	[28]	W	Set DATA0 PID Applies to interrupt/ bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0. Set Even (micro) frame Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/ Odd (micro) frame field to even (micro) frame.	0x0
SetNAK	[27]	W	Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application controls the transmission of NAK handshakes on an endpoint. The core also	0x0

Name	Bit	Type	Description	Reset Value
			sets this bit for an endpoint after a SETUP packet is received on that endpoint.	
CNAK	[26]	W	Clear NAK A write to this bit clears the NAK bit for the endpoint.	0x0
RSVD	[25:22]	–	Reserved	–
stall	[21]	RW	STALL Handshake Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-Periodic In NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application clears this bit, never the core. Applies to control endpoints only The application sets this bit, and the core clears it, if a SETUP token is received for this endpoint. If a NAK bit, Global Non-Periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	0x0
Snp	[20]	RW	Snoop Mode This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.	–
EPType	[19:18]	R	Endpoint Type This is the transfer type supported by this logical endpoint. 0 = Control 1 = Isochronous 2 = Bulk 3 = Interrupt	0x0
NAKsts	[17]	R	NAK Status Indicates the following: 0 = The core is transmitting non-NAK handshakes based on the FIFO status 1 = The core is transmitting NAK handshakes on this endpoint. If either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in theTxFIFO. For isochronous IN endpoints: The core sends out a	0x0

Name	Bit	Type	Description	Reset Value
			zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.	
DPID EO_FrNum	[16]	R	Endpoint Data PID Applies to interrupt/ bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. Applications use the SetD1PID andSetD0PID fields of this register to program either DATA0 orDATA1 PID. 0 = DATA0 1 = DATA1 Even/ Odd (Micro) Frame Applies to isochronous IN and OUT endpoints only. Indicates the (micro) frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/ odd (micro) frame number in which it intends to transmit/ receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. 0 = Even (micro) frame 1 = Odd (micro) frame	–
USBActEP	[15]	RW	USB Active Endpoint Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints after detecting a USB reset. After receiving the Set Configuration and Set Interface commands, the application must program endpoint registers accordingly and set this bit.	0x0
RSVD	[14:11]	–	Reserved	–
MPS	[10:0]	RW	Maximum Packet Size The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.	0x0

25.7.1.3.27 DOEPINTn (1 ≤ n ≤ 7, DOEPINT1, DOEPINT2, …, DOEPINT7)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B08 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	–	Reserved	–
NYETIntrpt	[14]	R	NYET interrupt The core generates this interrupt when a NYET response is transmitted for a non-isochronous OUT endpoint.	0x0
NAKIntrpt	[13]	R	NAK interrupt The core generates this interrupt when a NAK is transmitted. In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to unavailability of data in the TXFifo.	0x0
BbleErrIntrpt	[12]	R	BbleErr (Babble Error) interrupt The core generates this interrupt when babble is received for the endpoint.	0x0
PktDrpSts	[11]	R	Packet Dropped Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.	0x0
RSVD	[10]	–	Reserved	–
BNAIntr	[9]	R	PBNA (Buffer Not Available) Interrupt The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Dependency: This bit is valid only when Scatter/Gather DMA mode is enabled.	0x0
OutPktErr	[8]	R	OUT Packet Error Applies to OUT endpoints only. This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. Dependency: This interrupt is valid only when both of the following conditions are true: • Parameter OTG_EN_DED_TX_FIFO=1 • Thresholding is enabled.	0x0
RSVD	[7]	–	Reserved	–
Back2BackSETup	[6]	R	Back-to-Back SETUP Packets Received This bit indicates that core has received more than three back-to-back SETUP packets for this particular endpoint.	0x0

Name	Bit	Type	Description	Reset Value
StsPhseRcvd	[5]	R	Status Phase Received For Control Write This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in case of Scatter Gather DMA mode.	0x0
OUTTknEPdis	[4]	RW	Token Received When Endpoint Disabled Indicates that an OUT token is received if the endpoint is not enabled. This interrupt is asserted on the endpoint for which the OUT token was received.	0x0
SetUp	[3]	RW	SETUP Phase Done Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application decodes the received SETUP data packet.	0x0
AHBErr	[2]	RW	AHB Error This is generated only in Internal DMA mode if there is an AHBerror during an AHB read/write. The application reads the corresponding endpoint DMA address register to get the error address.	0x0
EPDisbld	[1]	RW	Endpoint Disabled Interrupt This bit indicates that the endpoint is disabled per the application's request.	0x0
XferCompl	[0]	RW	Transfer Completed Interrupt Applies to IN and OUT endpoints. • When Scatter/Gather DMA mode is enabled • For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. • For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. • When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.	0x0

25.7.1.3.28 DOEPTSIZn (1 ≤ n ≤ 7, DOEPTSIZ1, DOEPTSIZ2, …, DOEPTSIZ7)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B10 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	–
RxDPID SUPCnt	[30:29]	RW	Received Data PID This is the data PID received in the last packet for this endpoint. 0 = DATA0 1 = DATA1 2 = DATA2 3 = MDATA SETUP Packet Count This field specifies the number of back-to-back SETUP data packets the endpoint can receive. 1 = 1 packet 2 = 2 packets 3 = 3 packets	–
PktCnt	[28:19]	RW	Packet Count Indicates the total number of USB packets that constitute theTransfer Size amount of data for endpoint 0. This field is decremented every time a packet is read from theTxFIFO.	0x0
XferSize	[18:0]	RW	Transfer Size This field contains the transfer size in bytes for the current endpoint. The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size is set to the maximum packet size of the endpoint, to be in terruptedat the end of each packet. The core decrements this field every time apacket from the external memory is written to the TxFIFO.	0x0

25.7.1.3.29 DOEPDMAn (1 ≤ n ≤ 7, DOEPDMA1, DOEPDMA2, …, DOEPDMA7)

- Base Address: 0xC004_0000
- Address = Base Address + 0x0B14 + n × 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
DMAAddr	[31:0]	RW	DMA Address Holds the start address of the external memory for storing or fetching endpoint data. This register is incremented on every AHB transaction. NOTE: For control endpoints, this address stores control OUT data packets as well as SETUP transaction data packets. If multiple SETUP packets are received back-to-back, theSETUP data packet in the memory is overwritten.	0x0

25.7.1.4 Power and Clock Gating Registers (USB_OTG_PCGCCTL)

25.7.1.4.1 PCGCCTL

- Base Address: 0xC004_0000
- Address = Base Address + 0x0E00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	–
StopPclk	[0]	RW	STOP Pclk The application sets this bit to stop the PHY clock if the USB iss uspended, the session is not valid, or the device isd isconnected. The application clears this bit if the USB isresumed or a new session starts.	–

26 USB2.0 HOST

26.1 Overview

The USB 2.0 EHCI Host Controller is fully compliant with the USB 2.0 specification and the Enhanced Host Controller Interface (EHCI) specification (revision 2.0). The controller supports high-speed, 480Mbps transfers (40 times faster than USB 1.1 full- speed mode) as well as companion controller integration with the USB 1.1OHCI Host Controller. The controller is designed to operate independently of the Bus Interface Unit (BIU) to the Application, shielding the complexities of the USB 2.0 Host Controller native protocol and providing easy integration of the EHCI Host Controller with an industry-standard AHB or PCI bus or with your target application. At the USB 2.0 physical interface, the EHCI Host Controller is designed with USB 2.0 Transceiver Macro cell Interface. Also the controller provides High-Speed Inter-Chip (HSIC) (version 1.0).

26.2 Features

The host controller is responsible for:

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices
- Controlling the association to either the Open Host Controller Interface or the Enhanced
- Host Controller via a Port Router
- Root Hub functionality to supports up/down stream port
- Support High-Speed Inter-Chip (HSIC), Version 1.0

26.3 Block Diagram

The architecture of the USB 2.0 EHCI Host Controller with BIU (Bus Interface Unit), along with the majorbuilding blocks and the companion controller (USB 1.1 OHCI Host Controller), is shown in *Figure 26-1*.

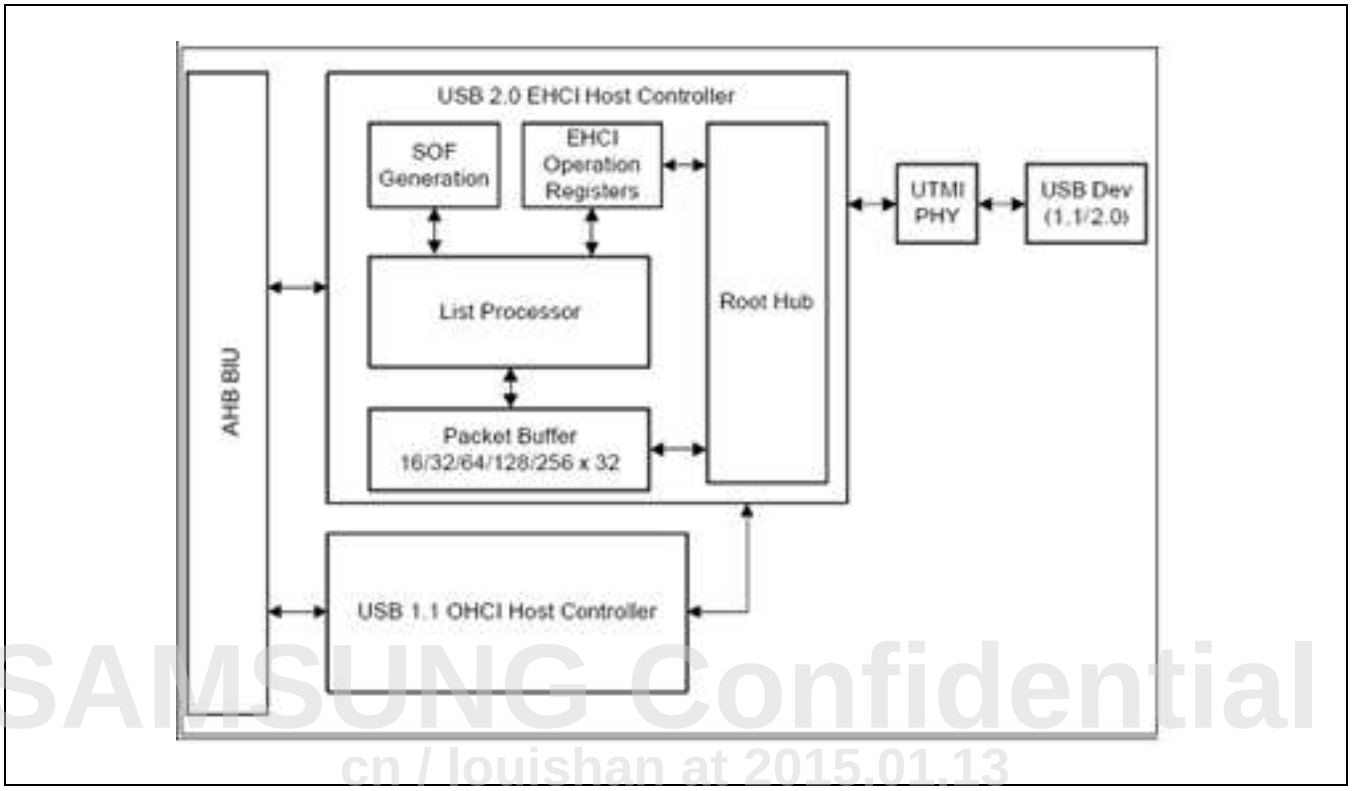


Figure 26-1 USB2.0 HOST Block Diagram

26.4 Functional Description

26.4.1 Programming User Configure of PHY and LINK in EHCI or OHCI

1. Release common reset of host controller
   - Program RSTCON1[24] (address: 0xC0012004) to 1'b1
2. Program AHB Burst type
   - SINGLE: default. TIEOFFREG7[27:25] (address: 0xC001101C) is 3'b000.
   - INCR16 (The OHCI does not support INCR16): program TIEOFFREG7[27:25] (address: 0xC001101C) to 3'b111 (recommended)
   - INCR8 (The OHCI does not support INCR8): program TIEOFFREG7[27:25] (address: 0xC001101C) to 3'b110
   - INCR4 (The OHCI part of the controller only supports INCR4 or SINGLE): program TIEOFFREG7[27:25] (address: 0xC001101C) to 3'b100
3. Select word interface and enable word interface selection
   - 8-bit word interface: program TIEOFFREG5[26:25] (address: 0xC0011014) to 2'b01 and TIEOFFREG9[10:9] (address: 0xC0011024) to 2'b01
   - 16-bit word interface: program TIEOFFREG5[26:25] (address: 0xC0011014) to 2'b11 and TIEOFFREG9[10:9] (address: 0xC0011024) to 2'b11

4. POR (Power On Reset) of PHY
   - Program TIEOFFREG8[8:7] (address: 0xC0011020) to 2'b01
5. Wait clock of PHY: About 40 micro seconds
6. Release utmi reset
   - Program TIEOFFREG5[21:20](address: 0xC0011014) to 2'b11
7. Release ahb reset of EHCI, OHCI
   - Program TIEOFFREG13[19:17] (address: 0xC0011034) to 3'b111

26.4.2 Programming User Configure of PHY and LINK in HSIC

1. Release common reset of host controller
   - Program RSTCON1[24] (address: 0xC0012004) to 1'b1
2. Program AHB Burst type
   - SINGLE: default. TIEOFFREG7[27:25] (address: 0xC001101C) is 3'b000.
   - INCR16 (The OHCI does not support INCR16): program TIEOFFREG7[27:25] (address: 0xC001101C) to 3'b111
   - INCR8 (The OHCI does not support INCR8): program TIEOFFREG7[27:25] (address: 0xC001101C) to 3'b110
   - INCR4 (The OHCI part of the controller only supports INCR4 or SINGLE): program TIEOFFREG7[27:25] (address: 0xC001101C) to 3'b100
3. Select word interface and enable word interface selection
   - 8-bit word interface: program TIEOFFREG5[26:25] (address: 0xC0011014) to 2'b01 and TIEOFFREG9[10:9] (address: 0xC0011024) to 2'b01 and TIEOFFREG11[13:12] (address: 0xC001102C) to 2'b01
   - 16-bit word interface: program TIEOFFREG5[26:25] (address: 0xC0011014) to 2'b11 and TIEOFFREG9[10:9] (address: 0xC0011024) to 2'b11 and TIEOFFREG11[13:12] (address: 0xC001102C) to 2'b11

4. POR (Power On Reset) of EHCI PHY
   - Program TIEOFFREG8[8:7] (address: 0xC0011020) to 2'b01
5. Wait clock of EHCI PHY: about 40 micro seconds
6. Program HSIC Mode
   - Program TIEOFFREG5[24:23] (address: 0xC0011014) to 2'b11
7. POR (Power On Reset) of HSIC PHY
   - Program TIEOFFREG10[19:18] (address: 0xC0011028) to 2'b01
8. Wait clock of HSIC PHY: About 40 micro seconds
9. Release utmi reset
   - Program TIEOFFREG5[20] (addr: 0xC0011014) to 1'b1 and TIEOFFREG5[22] (address: 0xC0011014) to 1'b1
10. Release ahb reset
    - Program TIEOFFREG5[19:17] (address: 0xC0011014) to 3'b111

26.4.3 Attention Point of HSIC Programming

Port Status Control Register:

- EHCI uses PORTSC_1 (address: 0xC0030054)
- HSIC uses PORTSC_2 (address: 0xC0030058)

How to enable the Port Power Control Switch:

- EHCI case: set PORTSC_1[12] (address: 0xC0030054) to 1'b1
- HSIC case: set INSNREG08[1] (address: 0x0xC00300B0) to 1'b1

26.5 Register Description

26.5.1 Register Map Summary

- Base Address: 0xC002_0000 (OHCI Controller)
- Base Address: 0xC003_0000 (EHCI Controller)

The USB2.0 Host controller implements all of the necessary EHCI registers. Consult the Enhanced Host Controller Interface Specification for USB for register details and programming considerations. Registers that differ from the EHCI specification are described below.

Register	Offset	Description	Reset Value
HCCAPBASE	0000h	Capability Register	0x0100_0010
HCSPARAMS	0004h	Structural Parameter Register	0x0000_1116
HCCPARAMS	0008h	Capability Parameter Register	0x0000_A010
RSVD	000Ch	Reserved	-
USBCMD	0010h	USB Command Register	0x0008_0000
USBSTS	0014h	USB Status Register	0x0000_1000
USBINTR	0018h	USB Interrupt Enable Register	0x0000_0000
FRINDEX	001Ch	USB Frame Index Register	0x0000_0000
CTRLDSSEGMEN	0020h	4G Segment Select Register	0x0000_0000
PERIODICLISTBASE	0024h	Periodic Frame List Base Address Register	0x0000_0000
ASYNCLISTADDR	0028h	Asynchronous List Address Register	0x0000_0000
RSVD	002Ch to 004Ch	Reserved	
CONFIGFLAG	0050h	Configure Flag Register	0x0000_0000
PORTSC_1 to 15	0054h to 008Ch	Port Status/Control Register	0x0000_2000
INSNREG00	0090H: WORD	Micro-Frame Counter Interface Register	0x0000_0000
INSNREG01	0094H: WORD	Packet Buffer In/Out Threshold Register	0x0020_0020
INSNREG02	0098H: WORD	Packet Buffer depth Register	0x0000_0080
INSNREG03	009CH: WORD	Transfer En/Disable Register	0x0000_0000
INSNREG04	00A0H: WORD	HCC Parameters Register	0x0000_0000
INSNREG05	00A4H: WORD	UTMI Configuration Control and Status Register	0x0000_1000
INSNREG06	00A8H: WORD	AHB Error Status Register	16'b0
INSNREG07	00ACH: WORD	AHB Master Error Address Register	16'b0
INSNREG08	00A4H: WORD	HSIC Enable/Disable Register	0x0000_0000

26.5.1.1 HCCAPBASE

- Base Address: 0xC003_0000
- Address = Base Address + 0000h, Reset Value = 0x0100_0010

Name	Bit	Type	Description	Reset Value
HCCAPBASE	[31:0]	RW	Capability Register	0x0100_0010

26.5.1.2 HCSPARAMS

- Base Address: 0xC003_0000
- Address = Base Address + 0004h, Reset Value = 0x0000_1116

Name	Bit	Type	Description	Reset Value
HCSPARAMS	[31:0]	RW	Structural Parameter Register	0x0000_1116

26.5.1.3 HCCPARAMS

- Base Address: 0xC003_0000
- Address = Base Address + 0008h, Reset Value = 0x0000_A010

Name	Bit	Type	Description	Reset Value
HCCPARAMS	[31:0]	RW	Capability Parameter Register NOTE: The Isochronous Scheduling Threshold value is set to 1 by default	0x0000_A010

26.5.1.4 USBCMD

- Base Address: 0xC003_0000
- Address = Base Address + 0010h, Reset Value = 0x0008_0000

Name	Bit	Type	Description	Reset Value
USBCMD	[31:0]	RW	USB Command	0x0008_0000

26.5.1.5 USBSTS

- Base Address: 0xC003_0000
- Address = Base Address + 0014h, Reset Value = 0x0008_0000

Name	Bit	Type	Description	Reset Value
USBCMD	[31:0]	RW	USBCMD	0x0008_0000

26.5.1.6 USBINTR

- Base Address: 0xC003_0000
- Address = Base Address + 0018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
USBINTR	[31:0]	RW	USB Interrupt Enable	0x0000_0000

26.5.1.7 FRINDEX

- Base Address: 0xC003_0000
- Address = Base Address + 001Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FRINDEX	[31:0]	RW	USB Frame Index	0x0000_0000

26.5.1.8 CTRLDSSEGMEN

- Base Address: 0xC003_0000
- Address = Base Address + 0020h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CTRLDSSEGMEN	[31:0]	RW	4G Segment Selector	0x0000_0000

26.5.1.9 PERIODICLISTBASE

- Base Address: 0xC003_0000
- Address = Base Address + 0024h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PERIODICLISTBASE	[31:0]	RW	Periodic Frame List Base Address Register	0x0000_0000

26.5.1.10 ASYNCLISTADDR

- Base Address: 0xC003_0000
- Address = Base Address + 0028h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ASYNCLISTADDR	[31:0]	RW	Asynchronous List Address Register	0x0000_0000

26.5.1.11 CONFIGFLAG

- Base Address: 0xC003_0000
- Address = Base Address + 0050h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CONFIGFLAG	[31:0]	RW	Configured Flag Register	0x0000_0000

26.5.1.12 PORTSC_1 to 15

- Base Address: 0xC003_0000
- Address = Base Address + 0054h to 008Ch, Reset Value = 0x0000_2000

Name	Bit	Type	Description	Reset Value
PORTSC_1 to 15	[31:0]	RW	Port Status/Control	0x0000_2000

26.5.1.13 INSNREG00

- Base Address: 0xC003_0000
- Address = Base Address + 0090H: WORD, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:14]	–	Reserved	0x0
BIT8	[13:12]	RW	This value is used as the 1-microframe counter with byte interface (8 bits)	2'b0
Bit16	[11:1]	RW	This value is used as the 1-microframe counter with byte interface (16 bits)	11'b0
WRENB	[0]	RW	Write Enable Register 0 = Disable 1 = Enable	1'b0

26.5.1.14 INSNREG01

- Base Address: 0xC003_0000
- Address = Base Address + 0094H: WORD, Reset Value = 0x0020_0020

Name	Bit	Type	Description	Reset Value
OUTTHRESHOLD	[31:16]	RW	Programmable Packet Buffer OUT Thresholds	0x0020
INTHRESHOLD	[15:0]	RW	Programmable Packet Buffer IN Threshold	0x0020

26.5.1.15 INSNREG02

- Base Address: 0xC003_0000
- Address = Base Address + 0098H: WORD, Reset Value = 0x0000_0080

Name	Bit	Type	Description	Reset Value
INSNREG02	[31:0]	RW	Programmable Packet Buffer Depth The value specified here is the number of DWORDs (32-bit entries)	0x0000_0080

26.5.1.16 INSNREG03

- Base Address: 0xC003_0000
- Address = Base Address + 009CH: WORD, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
INSNREG03	[31:0]	RW	Break Memory Transfer Used in conjunction with INSNREG01 to enable/disable breaking memory transactions into chunks once the OUT/IN threshold value is reached. 0 = Disable 1 = Enable	0x0000_0000

26.5.1.17 INSNREG04

- Base Address: 0xC003_0000
- Address = Base Address + 00A0H: WORD, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:5]	–	Reserved	0x0
NAK	[4]	RW	This value is used as the 1-microframe counter with byte interface (8 bits)	1'b0
RSVD	[3]	–	Reserved	1'b0
SCALESDOWN	[2]	RW	Scales down port enumeration time enable 0 = Disable 1 = Enable	1'b0
M_HCCPARAMS	[1]	RW	Makes the HCCPARAMS register Write Enable 0 = Disable 1 = Enable	1'b0
M_HCSPARAMS	[0]	RW	Makes the HCSPARAMS register Write Enable 0 = Disable 1 = Enable	1'b0

26.5.1.18 INSNREG05

- Base Address: 0xC003_0000
- Address = Base Address + 00A0H: WORD, Reset Value = 0x0000_1000

Name	Bit	Type	Description	Reset Value
RSVD	[31:18]	–	Reserved	0x0
VBUSY	[17]	RW	VBusy (Software RO). Hardware indicator that a write to this register has occurred and the hardware is currently processing the operation defined by the data written. When processing is finished, this bit is cleared.	1'b0
vport	[16:13]	RW	VPort (Software R/W)	1'b0
vcontrol_loadm	[12]	RW	VControl_LoadM 0 = Load 1 = NOP (Software RW)	1'b1
vcontrol	[11:8]	RW	VControl (Software RW)	4'b0
vstatus	[7:0]	RW	VStatus (Software RW)	8'b0

26.5.1.19 INSNREG06

- Base Address: 0xC003_0000
- Address = Base Address + 00A8H: WORD, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CAPTURED	[31]	R/W	AHB Error Captured Indicator that an AHB error was encountered and values were captured. To clear this field the application must write a '0' to it.	1'b0
RSVD	[30:12]	R	Reserved	19'b0
HBURST	[11:9]	R	HBURST value of the control phase at which the AHB error occurred.	3'b0
NUMBER	[8:4]	R	Number of beats expected in the burst at which the AHB error occurred. Valid values are '0' to '16'	5'b0
COMPLETED	[3:0]	R	Number of successfully-completed beats in the current burst before the AHB error occurred.	4'b0

26.5.1.20 INSNREG07

- Base Address: 0xC003_0000
- Address = Base Address + 00ACH: WORD, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ERROR	[31:0]	R/W	AHB address of the control phase at which the AHB error occurred	0x0000_0000

26.5.1.21 INSNREG08

- Base Address: 0xC003_0000
- Address = Base Address + 00A4H: WORD, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved for future use. You don't have to write any value except 0.	16'b0
HSIC_ENB	[15:0]	RW	This register has R/W access to the host driver and gives control to the host driver to enable/disable the HSIC interface per port. Each bit in this register controls the HSIC interface for a particular port. Bit 1 controls PORT 1, Bit 0 controls the HSIC interface for PORT 0, and so on. 0 = When HSIC support is selected, then a value of 0 on this control register bit will put the corresponding PORT in the HSIC Disabled state	16'b0

Name	Bit	Type	Description	Reset Value
			1 = When HSIC configuration is selected and a value of 1 in this control bit will put the corresponding port in HSIC Enabled state	

27 I2S

27.1 Overview

The I2S controller supports streaming serial audio data between the External I2S Codec (ADC/DAC) and the processor. It consists of one transmitter channel and one receive channel. Both the transmitting and receiving channels are independent of each other and can work simultaneously.

- The I2S controller interface can be configured to work in three modes by the IMS (Internal Master/Slave) Fields in the I2SMOD register.
  - Internal Master mode
  - In the Internal master mode the Clock source to the I2S controller is APB "PCLK". The Bit Clock "I2SBCLK"' and the word select signal "I2SLRCLK" is generated internally from PCLK.
  - External Master mode
  - In the External master mode, the Clock source to the I2S controller is External Codec Clock. The Bit Clock "I2SBCLK" and the word select signal "I2SLRCLK" is generated internally from PCLK.
  - Slave mode
  - In the Slave mode, the Clock source to the I2S controller is APB "PCLK". The Bit Clock "I2SBCLK" and the word select signal "I2SLRCLK" is also supplied to the I2S Controller from an External source.
- BLC bits in the I2SMOD register can be configured for 8-bit or 16-bit or 24-bit per channel.
- LRP bit in the I2S mod register can be configured to configure the left right word clock polarity.
- SDF in the I2SMOD register can be configured to change the data bit position
  - Internal Master mode
  - MSB (Left) Justified
  - LSB (Right) Justified
- TXR in the I2SMOD register can be configured for half duplex or full duplex transmission.
  - Transmit only mode
  - Receive only mode
  - Transmit receive simultaneous mode
  - No operation/reserved
- DMA transfer mode can be set by setting the TXDMACTIVE and RXDMACTIVE bits in the I2SCON register.

27.2 Features

- Single Transmit and Receive Channel.
- Supports 8/16/24-bit word length.
- Programmable left/right word clock polarity
- Programmable MSB justified (Left), I2S and LSB (Right justified) data bit position.
- Programmable Transmit/Receive mode and simultaneous transmit receive mode.
- DMA transfer mode.

27.3 Block Diagram

A high-level block diagram of the I2S Controller is shown in *Figure 27-1*.

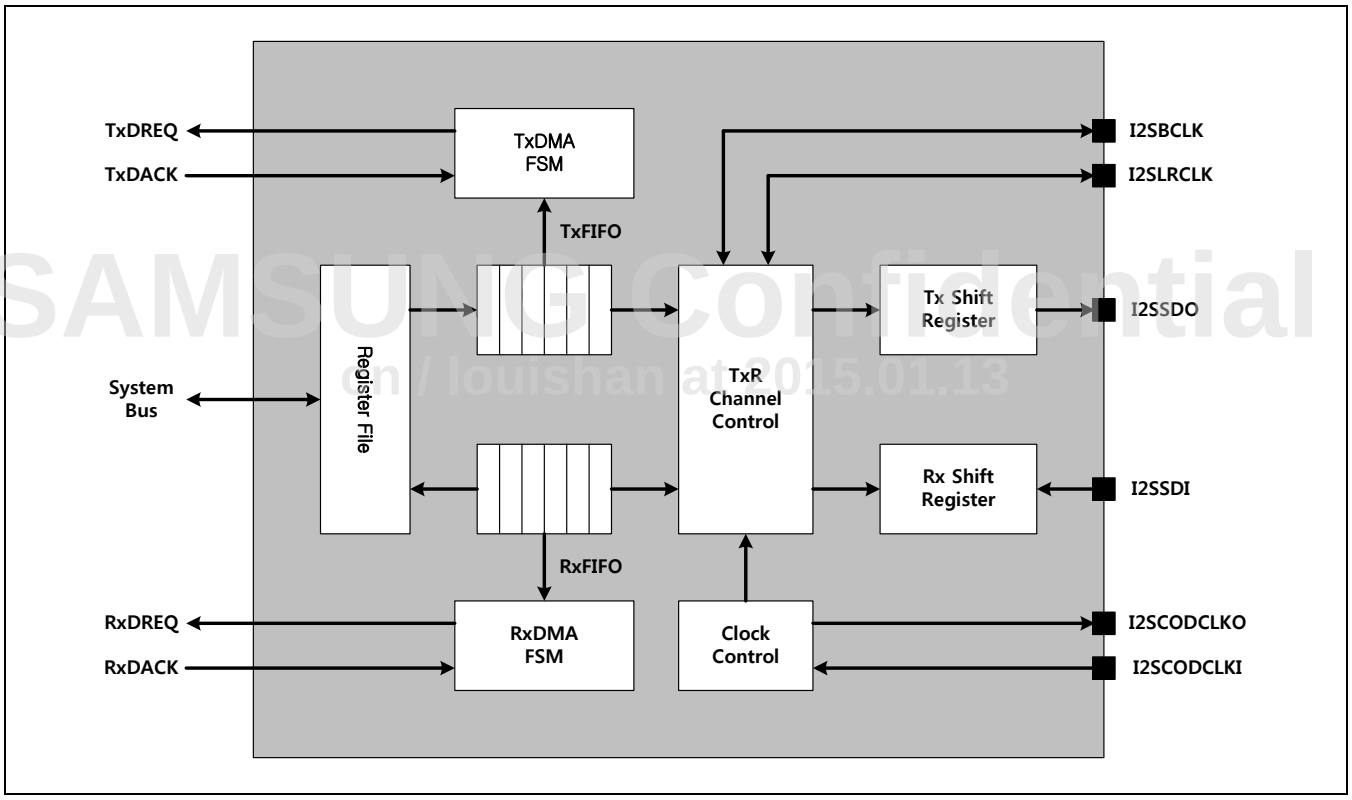


Figure 27-1 Block Diagram of the I2S Controller

27.4 Functional Description

The I2S Controller is very feature rich and works in slave only and External master and internal master mode as Transmitter or Receiver. In the Master mode, the Output Codec Clock to the External codec and the BCLKm is generated by the I2SLKCON block. The Audio Channel Clock is then derived from the BCLKm in the I2S Channel generator Block.

In the Slave Mode BITCLK and LRCLK is supplied from an external master.

The I2S controller after the power on reset needs to be configured for I2S Access. The Configuration block is I2SREG block. Here using the APB access the TX and Receive FIFO needs to be flushed before any valid I2S Transaction can occur. Then I2S Data is written using the PWRITE and PWDATA APB signals, which are written onto the TXFIFO block .For the I2S to transmit, the I2SACTIVE Signal should be activated for the TXFIFO block to transfer the data onto I2S Channel Generator Block.

The I2S Channel Generator Block then takes the BITCLK and generates the Channel Clock and the Parallel to serial load transfer control signals to the TX SFTR Block. The Holding Register inside the TX SFTR holds the incoming Parallel data and passes it onto I2SSDO bit by bit aligned with BITCLK. The Channel Clock LRCLK is also passed along with Channel Clock enable.

During the Receive phase, the change on Channel clock is interpreted as the incoming data on the I2SSDI line and is latched in on the positive edge of BCLK inside the RX SFTR.

The I2SACTIVE with the help of BCLK and LRCLK help generate the control signal, Serial to Parallel load in the Channel generator block. The Channel Generator block waits for the Left Channel data and the Right Channel data and passes it onto the RX FIFO Block where it is stored in subsequent locations .Any read from the APB is then provided the stored data.

The DMA Access to the I2S Controller can be activated by enabling the TXDMACTIVE/RXDMACTIVE bit in the I2SREG block. The TXDREQ is generated in the TXDMAFSM Block when TXDMACTIVE is high and the TXFIFO is not full .The RXDREQ is generated in the RXDMAFSM when the RXDMACTIVE is high and the RX FIFO is not empty. Both requests work on a Request -ACK mode.

27.4.1 Basic Clock Tree

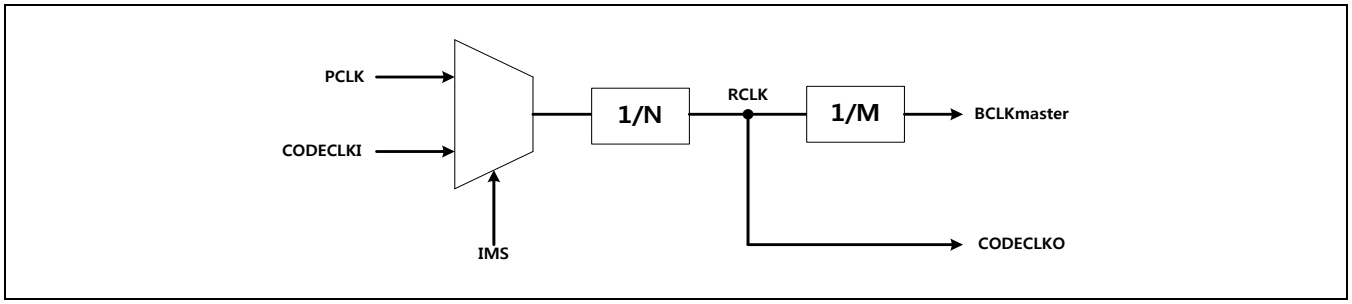


Figure 27-2 Basic Clock Tree

NOTE:

1. PSVALA is the value written to the prescaler division register.
2. PSVALC (internal register in I2SCLKCON) depends upon the RFS and BFS value combined to decide the division value.

For more information please refer to the I2SMOD register and I2S clock mapping table.

27.4.2 I2S-bus Format

The I2S bus has four lines including serial data input I2SSDI, serial data output I2SSDO, left/right channel select clock I2SLRCLK, and serial bit clock I2SBCLK; the device generating I2SLRCLK and I2SBCLK is the master.

Serial data is transmitted in 2's complement with the MSB first with a fixed position, whereas the position of the LSB depends on the word length. The transmitter sends the MSB of the next word at one clock period after the I2SLRCLK is changed. Serial data sent by the transmitter may be synchronized with either the trailing or the leading edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The LR channel select line indicates the channel being transmitted. I2SLRCLK may be changed on either a trailing or leading edge of the serial clock, but it does not need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The I2SLRCLK line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

- MSB (Left) Justified

  MSB-Justified (Left-Justified) format is similar to I2S bus format, except the in MSB-justified format, the transmitter always sends the MSB of the next word at the same time whenever the I2SLRCLK is changed.

- LSB (Right) Justified

  LSB-Justified (Right-Justified) format is opposite to the MSB-justified format. In other word, the transferring serial data is aligned with ending point of I2SLRCLK transition.

Formats show the audio serial format of I2S, MSB-justified, and LSB-justified. Note that in this figure, the word length is 16-bit and I2SLRCLK makes transition every 24 cycle of I2SBCLK (BFS is 48 fs, where fs is sampling frequency; I2SLRCLK frequency).

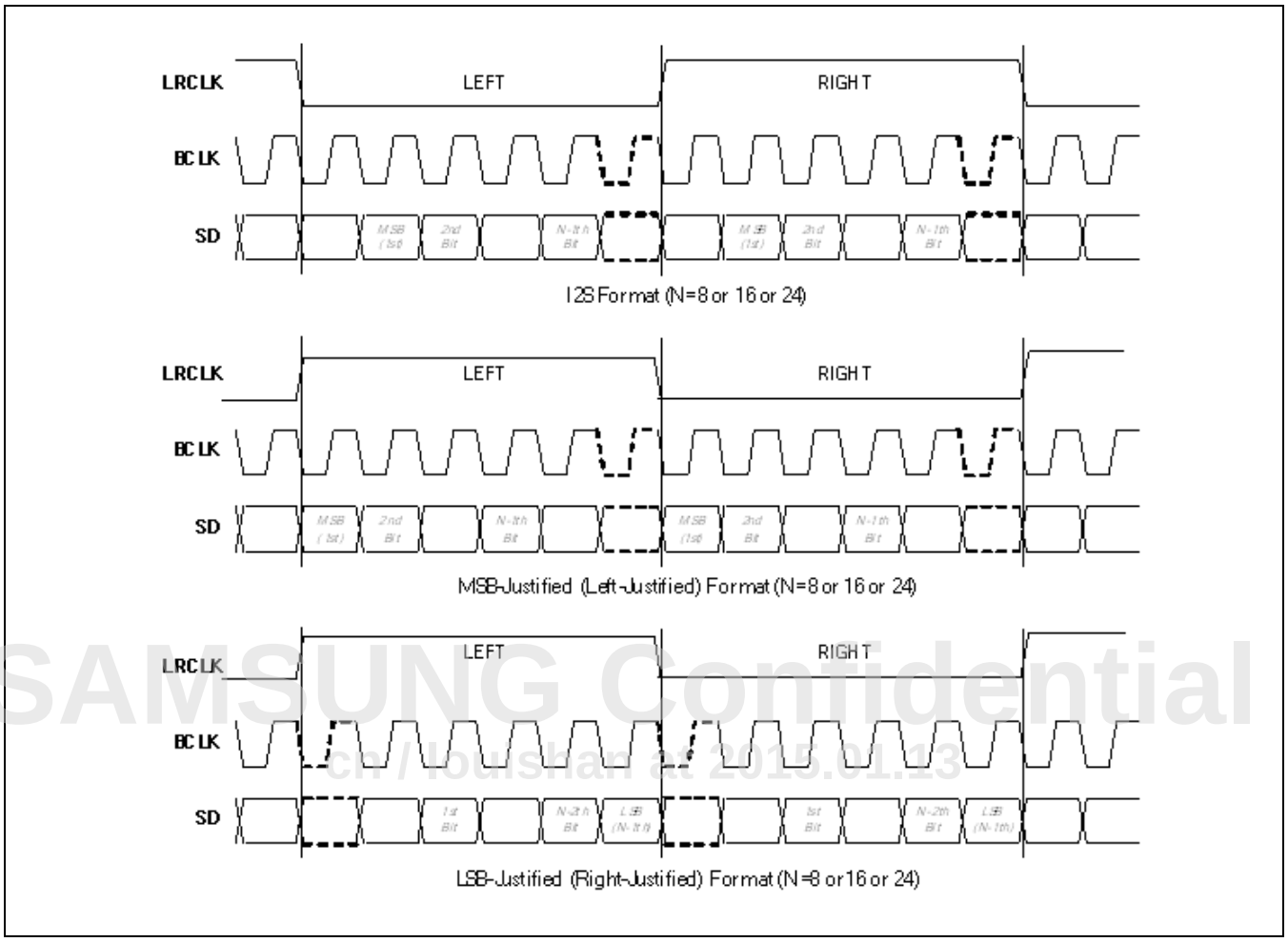


Figure 27-3 I2S Audio Serial Data Formats

27.4.3 Sampling Frequency and Master Clock

Master clock frequency (PCLK) can be selected by sampling frequency as shown in *Table 27-1*. Because PCLK is made by I2S prescaler, the prescaler value and PCLK type (256 or 384 fs) should be determined properly.

Table 27-1 I2S CODEC Clock (CODECLK = 256 or 384 fs)

I2SLRCLK (fs)	8.000 kHz	11.025 kHz	16.000 kHz	22.050 kHz	32.000 kHz	44.100 kHz	48.000 kHz	64.000 kHz	88.200 kHz	96.000 kHz
CODECLK (MHz)	256 fs									
	2.0480	2.8224	4.0960	5.6448	8.1920	11.2896	12.2880	16.3840	22.5792	24.5760
	384 fs									
	3.0720	4.2336	6.1440	8.4672	12.2880	16.9344	18.4320	24.5760	33.8688	36.8640

27.4.4 I2S Clock Mapping Table

On selecting BFS, RFS, and BLC bits of I2SMOD register, user should refer to the following table. *Table 27-2* shows the allowable clock frequency mapping relations.

Table 27-2 I2S Clock Mapping Table

Clock Frequency		RFS			
		256 fs (00B)	512 fs (01B)	384 fs (10B)	768 fs (11B)
BFS	16 fs (10B)	(a)	(a)	(a)	(a)
	24 fs (11B)	–	–	(a)	(a)
	32 fs (00B)	(a) (b)	(a) (b)	(a) (b)	(a) (b)
	48 fs (01B)	–	–	(a) (b) (c)	(a) (b) (c)
Description		(a) Allowed when BLC is 8-bit (b) Allowed when BLC is 16-bit (c) Allowed when BLC is 24-bit			

27.5 Programming Guide

27.5.1 Tx Channel

The I2S TX channel provides a single stereo compliant output. The transmit channel can operate in master or Slave mode. Data is transferred between the processor and the I2S controller via an APB access or a DMA access.

The processor must write words in multiples of two (i.e. for left and right audio sample). The words are serially shifted out timed with respect to the audio bit clock, BCLK and word select clock, LRCLK.

TX Channel has 16 × 32 bit wide FIFO where the processor or DMA can write up to 16 left/right data samples after enabling the channel for transmission.

An Example sequence is as the following.

Ensure the PCLK and CODCLKI are coming correctly to the I2S controller and FLUSH the TX FIFO using the TFLUSH bit in the I2SFIC Register (I2S FIFO Control Register).

Please ensure that I2S Controller is configured in one of the following modes.

- TX only mode
- TX/RX simultaneous mode.

This can be done by programming the TXR bit in the I2SMOD register (I2S mode register).

Then program the following parameters according the need.

- IMS
- SDF
- BFS
- BLC
- LRP

For programming, the above-mentioned fields please refer I2SMOD register (I2S mode register).

Once ensured that the input clocks for I2S controller are up and running and step 1 and 2 have been completed we can write to TX FIFO.

The write to the TX FIFO has to be carried out thorough the I2STXD Register (I2S TX FIFO Register). This 32-bit data will occupy position 0 of the FIFO and any further data will be written to position 2, 3 and so on.

The Data is aligned in the TX FIFO for 8 bits/channel or 16 bits/channel BLC as shown.

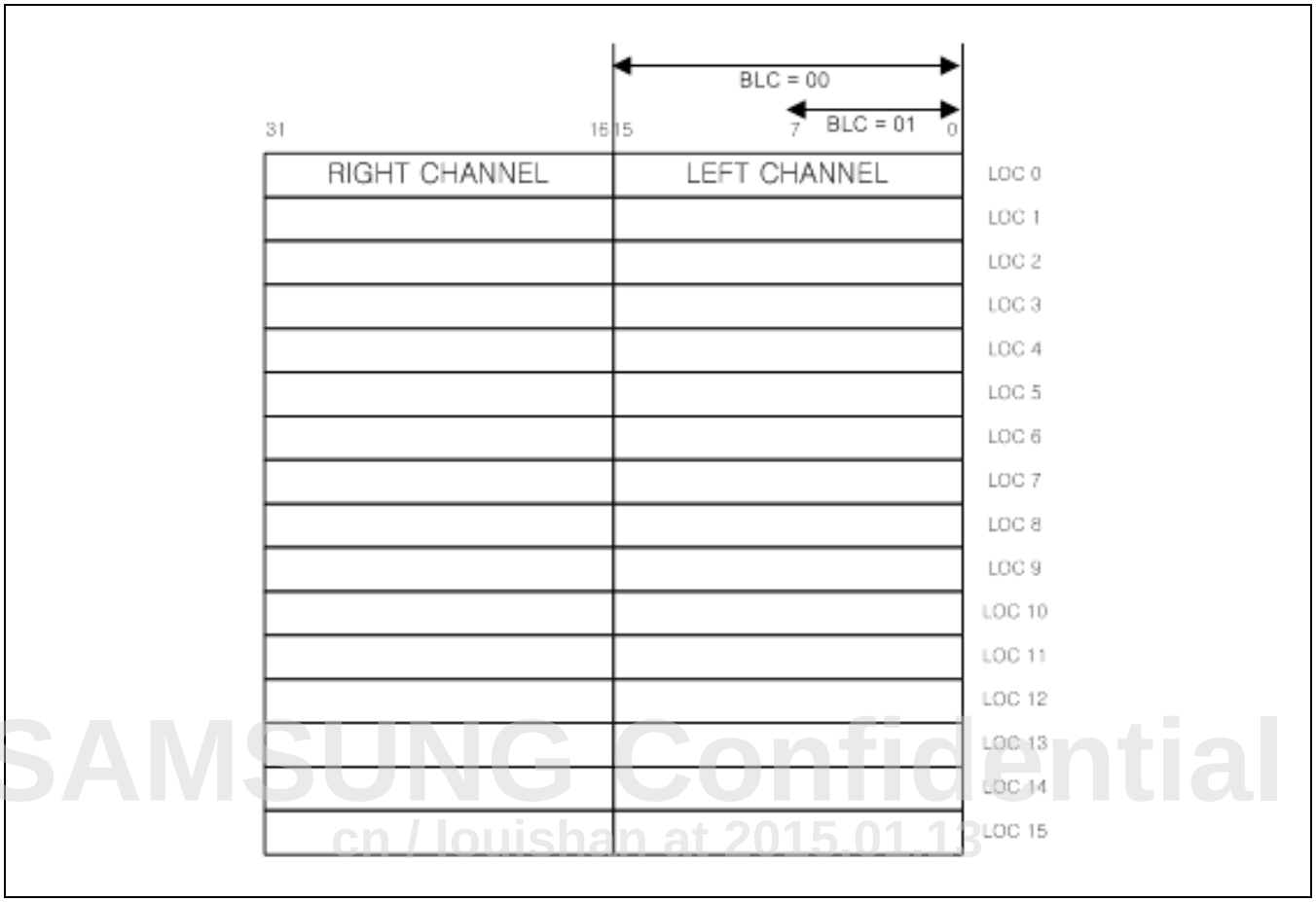


Figure 27-4 TX FIFO Structure for BLC = 00 or BLC = 01

The data is aligned in the TX FIFO for 24 bits/channel BLC as shown.

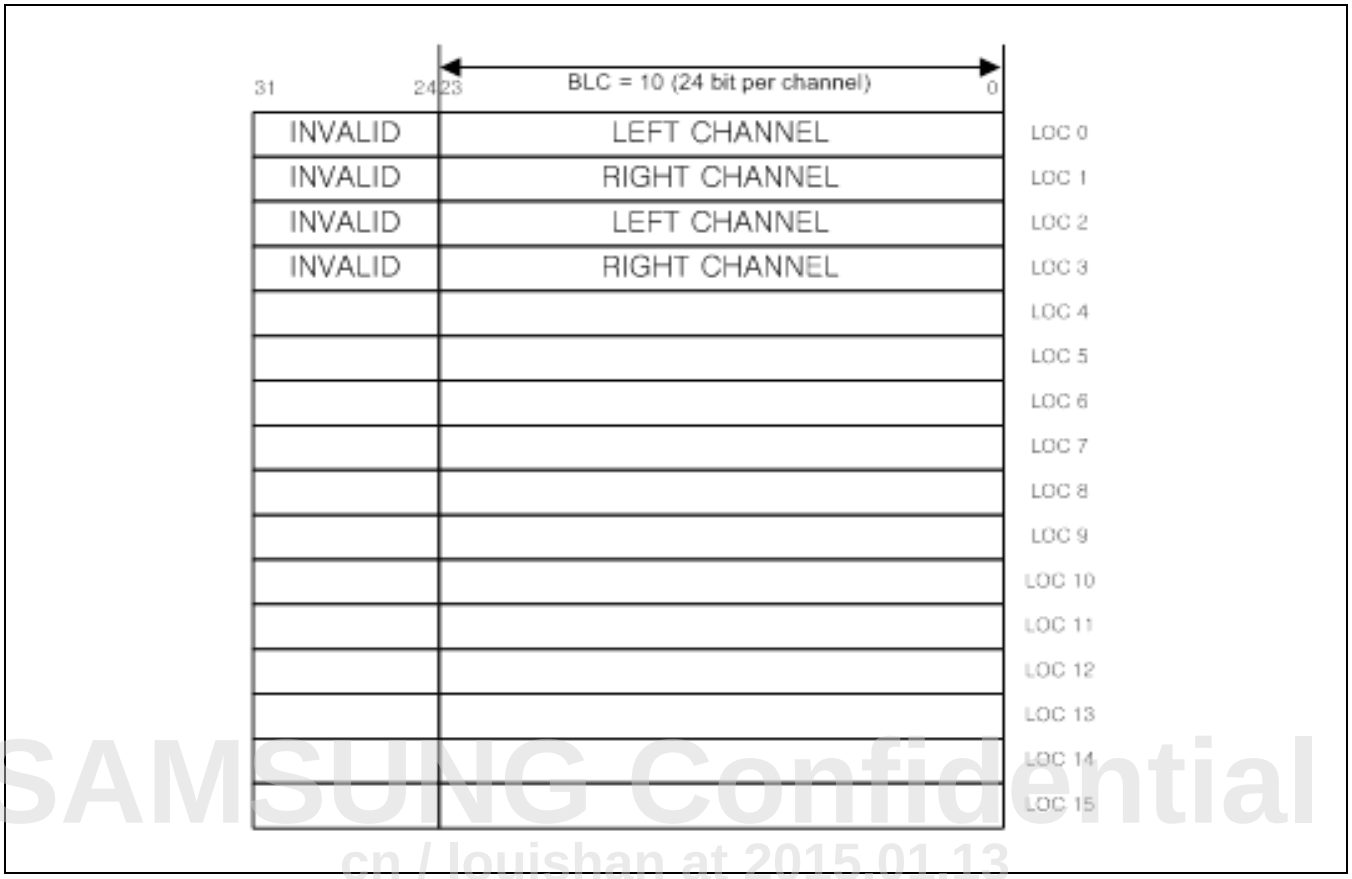


Figure 27-5 TX FIFO Structure for BLC = 10 (24 bits/channel)

Once the data is written to the TX FIFO the TX channel can be made active by enabling the I2SACTIVE bit in the I2SCON Register (I2S Control Register).The data is then serially shifted out with respect to the bit clock BCLK and word select clock LRCLK.

The TXCHPAUSE in the I2SCON Register (I2S Control Register) can stop the serial data transmission on the I2SSDO.The transmission is stopped once the current Left/Right channel is transmitted. If the control registers in the I2SCON Register (I2S Control Register) and I2SMOD Register (I2S Mode Register) are to be reprogrammed then it is advisable to disable the TX channel.

If the TX channel is enabled while the FIFO is empty, no samples are read from the FIFO. The Status of TX FIFO can be checked by checking the bits in the I2SFIC Register (I2S FIFO Control Register).

27.5.2 Rx Channel

The I2S RX channel provides a single stereo compliant output. The receive channel can operate in master or slave mode. Data is received from the input line and transferred into the RX FIFO. The processor can then read this data via an APB read or a DMA access can access this data.

RX Channel has a 16 × 32 bit wide RX FIFO where the processor or DMA can read up to 16 left/right data samples after enabling the channel for reception.

An Example sequence is as following.

Ensure the PCLK and CODCLKI are coming correctly to the I2S controller and FLUSH the RX FIFO using the RFLUSH bit in the I2SFIC Register (I2S FIFO Control Register) and the I2S controller is configured in any of the modes.

- Receive only.
- Receive/Transmit simultaneous mode.

This can be done by programming the TXR bit in the I2SMOD register (I2S mode register).

Then program the following parameters according to the need.

- IMS
- SDF
- BFS
- BLC
- LRP

For programming, the above mentioned fields please refer I2SMOD register. (I2S mode register).

Once ensured that the input clocks for I2S controller are up and running and step1 and 2 have been completed user must put the I2SACTIVE high to enable any reception of data, the I2S controller receives data on the LRCLK change.

The Data must be read from the RX FIFO using the I2SRXD Register (I2S RX FIFO Register) only after looking at the RX FIFO count in the I2SFIC Register (I2S FIFO Control Register). The count would only increment once the complete left channel and right have been received.

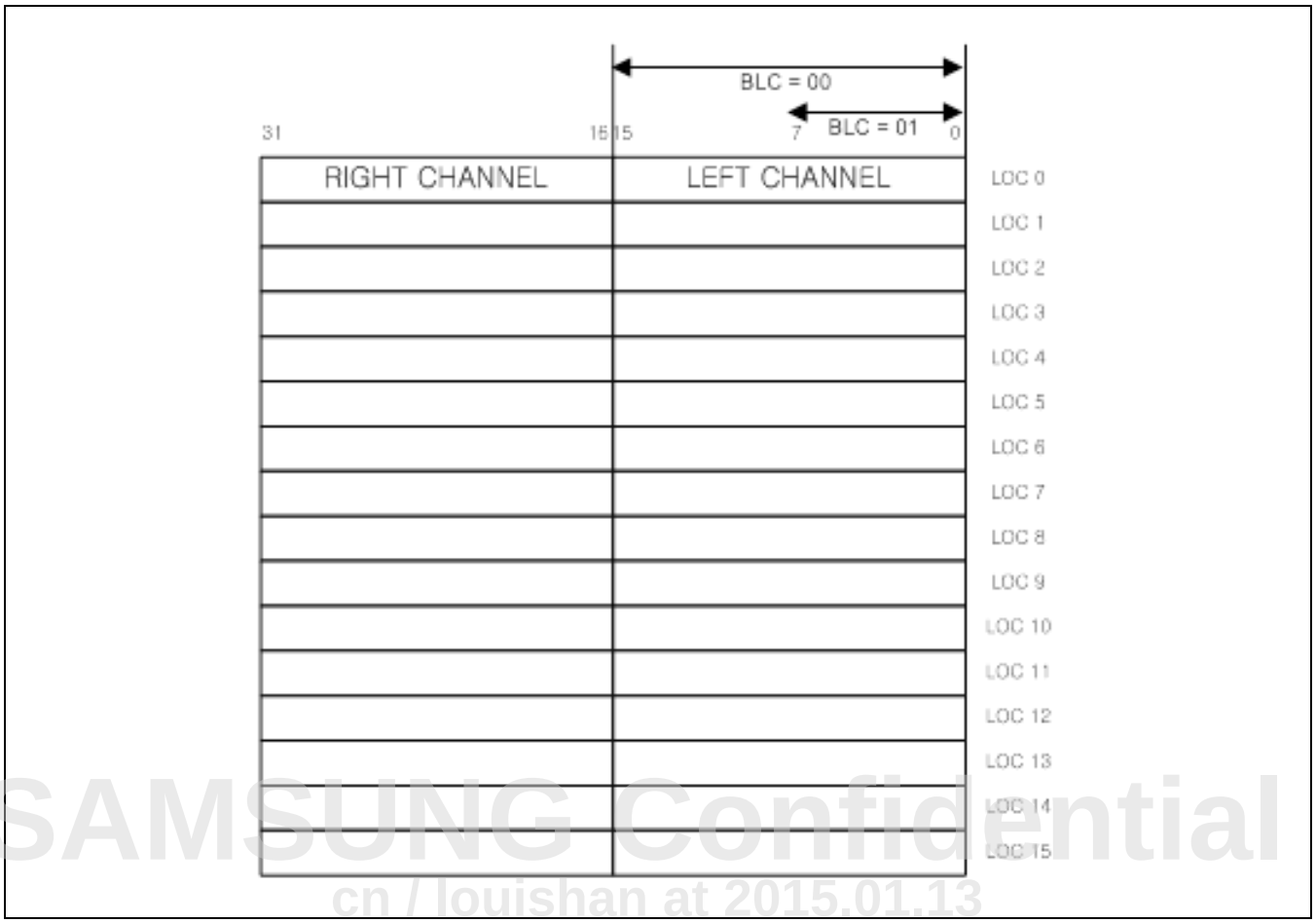


Figure 27-6 RX FIFO Structure for BLC = 00 or BLC = 01

The data is aligned in the RX FIFO for 24 bits/channel BLC as shown.

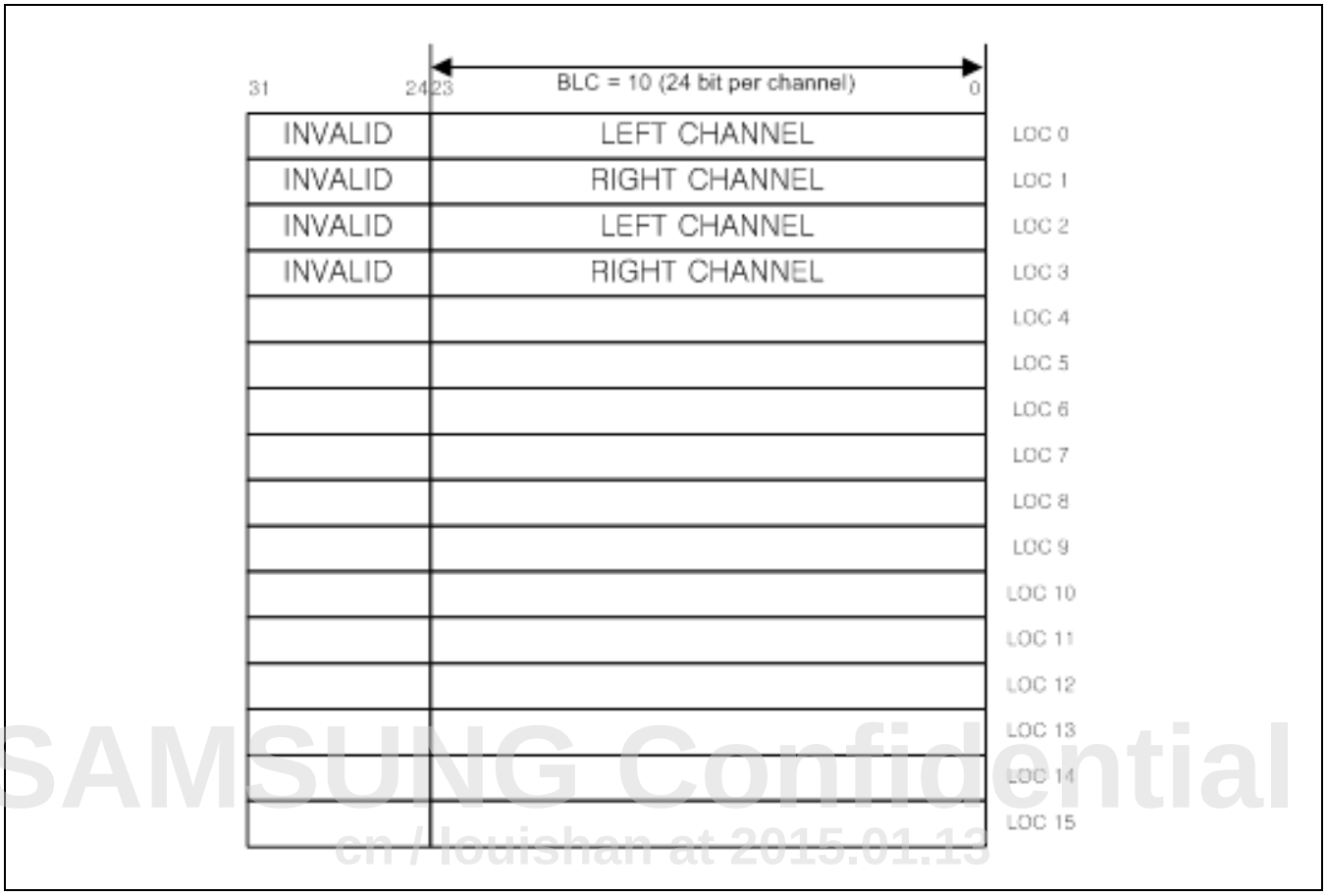


Figure 27-7 RX FIFO Structure for BLC = 10 (24 bits/channel)

The RXCHPAUSE in the I2SCON register can stop the serial data reception on the I2SSDI.The reception is stopped once the current Left/Right channel is received. If the control registers in the I2SCON Register (I2S Control Register) and I2SMOD Register (I2S Mode Register) are to be reprogrammed then it is advisable to disable the RX channel.

The Status of RX FIFO can be checked by checking the bits in the I2SFIC Register (I2S FIFO Control Register).

27.5.3 I2S-Controller Initialize

The initialization sequence in this section is used for I2S-bus controller.

- Provide a clock and Release a reset. This signals are propagated all of the I2S-bus controller internal registers and logic.
- Enable pad select alt-function of I2S

Following diagram shows I2S-controller operation command examples.

Example 27-1 Transmitter Mode

```
//to function in the TX mode

void activate_I2S_controller (void)

{

apbif_single_write   (SEND_TO_I2S, FIFO_CONTROL_REG,  0xFFFF_FFFF); //Flush the current FIFO

apbif_single_write   (SEND_TO_I2S, FIFO_CONTROL_REG,  0x0000_0000);  //Clear the Flush bit

apbif_multiple_write (SEND_TO_I2S, TX_REG, data_value);               //Data to be transmitted

apbif_single_write   (SEND_TO_I2S, MODE_REG, 0x0000_0000);           //Configure the mode register

apbif_single_write   (SEND_TO_I2S, CONTROL_REG,0x0000_0001);        //Initiate the transfer

wait_until_data_is_transmitted();                                    //wait for data to be
transmitted

apbif_single_write   (SEND_TO_I2S, CONTROL_REG,0x0000_0000);         //End the transfer

};
```


Example 27-2 Receiver Mode

```
void activate_I2S_controller (void)

{

apbif_single_write   (SEND_TO_I2S, FIFO_CONTROL_REG,  0xFFFF_FFFF);  //Flush the current FIFO

apbif_single_write   (SEND_TO_I2S, FIFO_CONTROL_REG,  0x0000_0000);  //Clear the Flush bit

apbif_single_write   (SEND_TO_I2S, MODE_REG,0x0001_0000);           //Configure the mode register

apbif_single_write   (SEND_TO_I2S, CONTROL_REG,0x0000_0001);        //Initiate the transfer

wait_until_data_is_received();                                      //wait for data to be
transmitted
```

```
apbif_single_write   (SEND_TO_I2S, CONTROL_REG,0x0000_0000);        //End the transfer

apbif_multiple_read (SEND_FROM_I2S, RX_REG);                          //Read data which is
received

};
```

27.5.4 Notes

While doing continuous change in mode such as a TX only mode/RX only mode/TX-RX mode in a single test kindly, ensure that the I2SACTIVE is only pulled low when a complete channel has been transmitted or in between the change of modes a system reset occurs.

The I2S controller should be supplied the BFS value according to the valid table even in the slave mode for correct functioning of the I2S unit.

The flush bit for the TX and RX FIFO should be given at the start of configuration of the I2S controller and not anywhere in between for correct functioning of the device.

Always keep LRP = 1 for MSB and LSB justified mode in both Slave and Master mode.

While doing changes in TXDMAACTIVE/RXDMAACTIVE/I2SACTIVE/TXDMA PAUSE/RXDMA PAUSE/TXCHANNEL PAUSE/RXCHANNEL PAUSE/TXR in 24-bit BLC configuration, ensure that Left and Right channel data is transmitted or received successfully. Successful transmission or reception of Left and Right channel data in 24-bit BLC configuration can be observed by polling LRI bit in I2SCON register.

27.6 Register Description

27.6.1 Register Map Summary

- Base Address: 0xC005_0000

Register	Offset	Description	Reset Value
I2SCON (I2S 0)	5000h	I2S interface control register	0x0000_0E00
I2SCON (I2S 1)	6000h		
I2SCON (I2S 2)	7000h		
ICSR (I2S 0)	5004h	I2C-bus Control-Status Register	0x0000_0000
ICSR (I2S 1)	6004h		
ICSR (I2S 2)	7004h		
I2SFIC (I2S 0)	5008h	I2S interface FIFO control register	0x0000_0000
I2SFIC (I2S 1)	6008h		
I2SFIC (I2S 2)	7008h		
I2SPSR (I2S 0)	500Ch	I2S interface clock divider control register	0x0000_0000
I2SPSR (I2S 1)	600Ch		
I2SPSR (I2S 2)	700Ch		
I2STXD (I2S 0)	5010h	I2S interface transmit data register	0x0000_0000
I2STXD (I2S 1)	6010h		
I2STXD (I2S 2)	7010h		
I2SRXD (I2S 0)	5014h	I2S interface receive data register	0x0000_0000
I2SRXD (I2S 1)	6014h		
I2SRXD (I2S 2)	7014h		

27.6.1.1 I2SCON

- Base Address: 0xC005_0000
- Address = Base Address + 5000h (I2S 0) + 6000h (I2S 1) + 7000h (I2S 2), Reset Value = 0x0000_0E00

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	RW	Reserved. Program to Zero	20'h0000
Lri	[11]	R	Left/right channel clock indication: LRI depends upon LRP bit of I2SMOD register and LRCLK. 0 = Left (when LRCLK is low and LRP is 0)/Right (when LRCLK is high and LRP is 0) 1 = Left (when LRCLK is high and LRP is 1)/Right (when LRCLK is low and LRP is 1)	1'b1
FTXEMPT	[10]	R	Tx FIFO empty status indication 0 = Tx FIFO is not empty (Ready to transmit data) 1 = Tx FIFO is empty (Not ready to transmit data)	1'b1
FRXDEMPT	[9]	R	Rx FIFO empty status indication 0 = Rx FIFO is not empty 1 = Rx FIFO is empty	1'b1
FTXFULL	[8]	R	Tx FIFO full status indication 0 = Tx FIFO is not full 1 = Tx FIFO is full	1'b0
FRXFULL	[7]	R	Rx FIFO full status indication 0 = Rx FIFO is not full (Ready to receive data) 1 = Rx FIFO is full (Not ready to receive data)	1'b0
TXDMAPAUSE	[6]	RW	Tx DMA operation pause command. DMA request will be halted after the current ongoing DMA transfer. 0 = No pause DMA operation 1 = Pause DMA operation	1'b0
RXDMAPAUSE	[5]	RW	Rx DMA operation pause command. DMA request will be halted after the current ongoing DMA transfer. 0 = No pause DMA operation 1 = Pause DMA operation	1'b0
TXCHPAUSE	[4]	RW	Tx channel operation pause command. Channel operation will be paused after LR channel data transmission is complete. 0 = No pause TX channel 1 = Pause TX channel	1'b0
RXCHPAUSE	[3]	RW	RX channel operation pause command. Channel operation will be paused after LR channel data reception is complete 0 = No pause RX channel 1 = Pause RX channel	1'b0

Name	Bit	Type	Description	Reset Value
TXDMACTIVE	[2]	RW	Tx DMA Active (start DMA request) when this bit is set from high to low DMA operation will be forced to stop immediately. 0 = INACTIVE 1 = ACTIVE	1'b0
RXDMACTIVE	[1]	RW	Rx DMA Active (start DMA request) when this bit is set from high to low DMA operation will be forced to stop immediately. 0 = INACTIVE 1 = ACTIVE	1'b0
I2SACTIVE	[0]	RW	I2S interface active (start I2S operation command) 0 = INACTIVE 1 = ACTIVE	1'b0

27.6.1.2 ICSR

- Base Address: 0xC005_0000
- Address = Base Address + 5004h (I2S 0) + 6004h (I2S 1) + 7004h (I2S 2), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	RW	Reserved. Program to Zero	17'h0
BLC	[14:13]	RW	Bit Length Control: Bit which decides transmission of 8/16 bits per audio channel 00 = 16 bits per channel 01 = 8 bits per channel 10 = 24 bits per channel 11 = Reserved	2'b0
CDCLKCON	[12]	RW	CODCLKOEN control 0 = CODCLKOEN is zero (I2SCODCLKO is output to the external codec) 1 = CODCLKOEN is one (No clock is given to the external codec)	1'b0
IMS	[11:10]	RW	I2S master (internal/external) or slave select mode 00 = Internal master (Divide mode): Input clock PCLK 01 = External master mode (Bypass mode): Input clock CODCLKI 10 = Slave mode: Input clock PCLK 11 = Slave mode: Input clock CODCLKI	2'b0
TXR	[9:8]	RW	Transmit or Receive mode select 00 = Transmit only 01 = Receive only 10 = Transmit and Receive simultaneous mode 11 = No operation/reserved	2'b0
LRP	[7]	RW	Left/Right channel clock polarity select 0 = Low for left channel and high for right channel. 1 = High for left channel and low for right channel.	1'b0
SDF	[6:5]	RW	Serial data format 00 = I2S format 01 = MSB-justified (Left-justified) format 10 = LSB-justified (Right-justified) format 11 = Reserved	2'b0
RFS	[4:3]	RW	I2S root clock (codec clock) frequency select Fs is sampling frequency. 00 = 256 fs 01 = 512 fs 10 = 384 fs 11 = 768 fs	2'b0
BFS	[2:1]	RW	Bit clock frequency select. Fs is sampling frequency. 00 = 32 fs 01 = 48 fs	2'b0

Name	Bit	Type	Description	Reset Value
			10 = 16 fs 11 = 24 fs	
RSVD	[0]	RW	Reserved. Program to Zero.	1'b0

NOTE: CODCLKOEN (active low) is used as a output pad enable for the I2SCODCLKO for various I2S audio codecs. Default condition of I2SMOD register has the I2SCODCLKO always enabled. Similarly I2SBCLKOEN and I2SLRCLKOEN is controlled by IMS bit when 00 and 01 only then both these output enables are zero (active) which validates the output clocks at the output pads.

27.6.1.3 I2SFIC

- Base Address: 0xC005_0000
- Address = Base Address + 5008h (I2S 0) + 6008h (I2S 1) + 7008h (I2S 2), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved. Program to Zero.	16'b0
tfulsh	[15]	RW	Tx FIFO flush command 0 = No flush 1 = Flush	1'b0
RSVD	[14:13]	RW	Reserved. Program to Zero.	2'b0
ftxcnt	[12:8]	R	Tx FIFO data count. FIFO has 16 depths, so value ranges from 0 to 15. N = Data count N of FIFO	5'b0
rflush	[7]	RW	Rx FIFO flush command 0 = No flush 1 = Flush	1'b0
RSVD	[6:5]	RW	Reserved. Program to Zero.	2'b0
frxcnt	[4:0]	R	Rx FIFO data count. FIFO has 16 depths, so value ranges from 0 to 15. N = Data count N of FIFO	5'b0

27.6.1.4 I2SPSR

- Base Address: 0xC005_0000
- Address = Base Address + 500Ch (I2S 0) + 600Ch (I2S 1) + 700Ch (I2S 2), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved. Program to Zero.	16'b0
psraen	[15]	RW	Prescaler (clock divider) A active 0 = Inactive 1 = Active	1'b0
RSVD	[14]	RW	Reserved. Program to Zero.	1'b0
psvala	[13:8]	RW	Prescaler (clock divider) A division value. N = Division factor is N+1	6'b0
RSVD	[7:0]	RW	Reserved. Program to Zero.	8'b0

27.6.1.5 I2STXD

- Base Address: 0xC005_0000
- Address = Base Address + 5010h (I2S 0) + 6010h (I2S 1) + 7010h (I2S 2), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
I2STXD	[31:0]	W	Tx FIFO write data. Note that the left/right channel data is allocated as the following bit fields R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC.	32'b0

27.6.1.6 I2SRXD

- Base Address: 0xC005_0000
- Address = Base Address + 5014h (I2S 0) + 6014h (I2S 1) + 7014h (I2S 2), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
I2SRXD	[31:0]	R	Rx FIFO read data. Note that the left/right channel data is allocated as the following bit fields. R[31:16], L[15:0] when 16-bit BLC R[23:16], L[7:0] when 8-bit BLC.	32'b0

28 AC97

28.1 Overview

The AC97 Controller Unit in the S5P4418 supports the features of AC97 revision 2.0. AC97 Controller uses audio controller link (AC-link) to communicate with AC97 Codec. Controller sends the stereo PCM data to Codec. The external digital-to-analog converter (DAC) in the Codec converts the audio sample to an analog audio waveform. Controller receives the stereo PCM data and the mono MIC data from Codec then store in memories. This Section describes the programming model for the AC97 Controller Unit. The prerequisite in this Section requires an understanding of the AC97 revision 2.0 specifications.

28.2 Features

The AC97 Controller includes the following features:

- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In.
- DMA-based operation and interrupt based operation.
- All of the channels support only 16-bit samples.
- Variable sampling rate AC97 Codec interface (48 kHz and below)
- 16-bit, 16 entry FIFOs per channel
- Only primary Codec support

28.3 Block Diagram

Figure 28-1 shows the functional block diagram of S5P4418 AC97 Controller. The AC97 signals from the AC-link are connected with external AC97 codec device. S5P4418 AC97 Controller supports full-duplex data transfers. All digital audio streams and command/status information are communicated via AC-link.

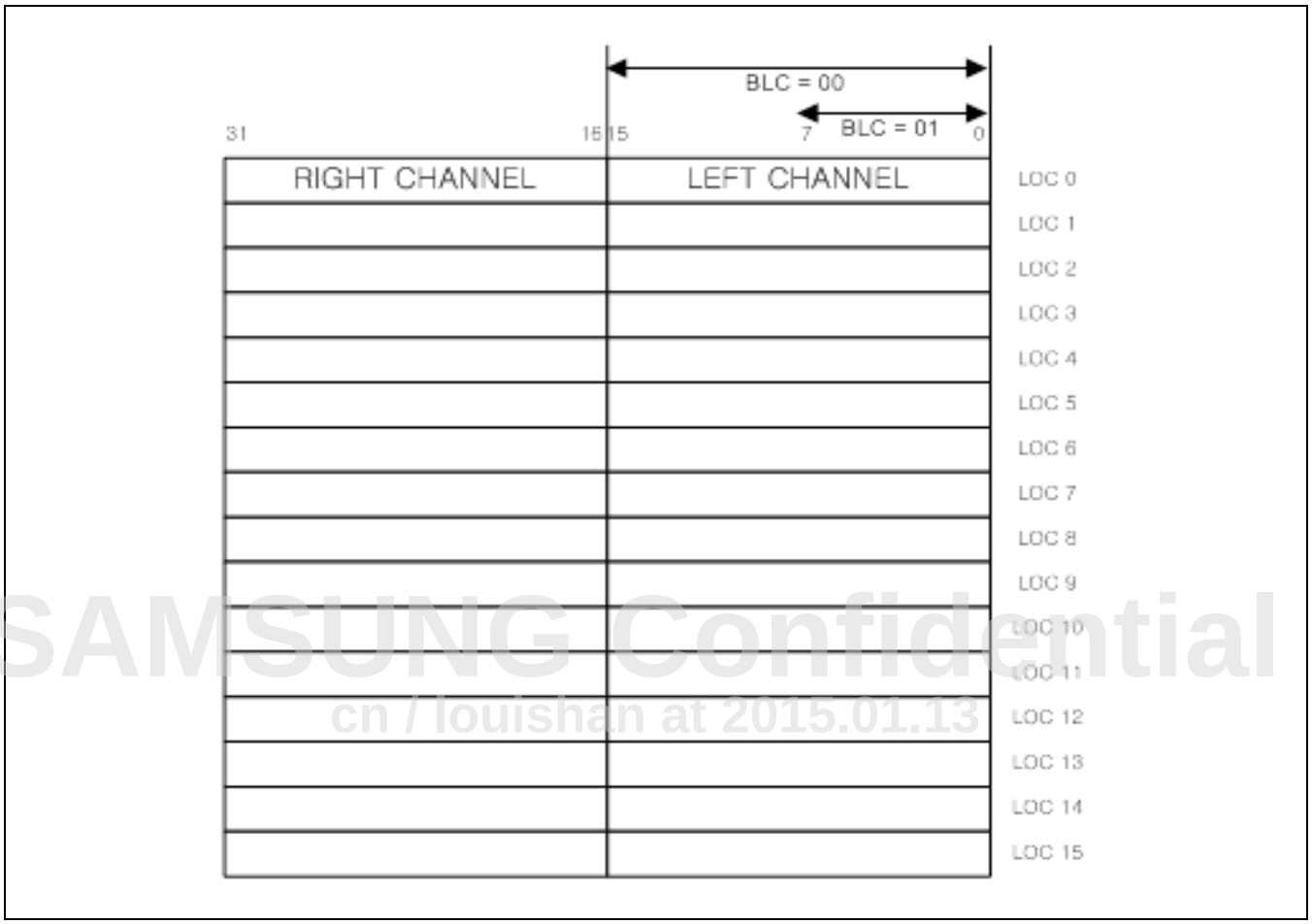


Figure 28-1 AC97 Block Diagram

28.4 Functional Description

This section explains the AC97 Controller operation, namely, AC-Link, Power-down sequence and Wake-up sequence.

28.4.1 Internal Data Path

Figure 28-2 shows the internal data path of S5P4418 AC97 Controller. It includes stereo Pulse Code Modulated (PCM) In, Stereo PCM Out and mono MIC-in buffers, which consist of 16-bit and 16 entries buffer. It also has 20-bit I/O shift register via AC-link.

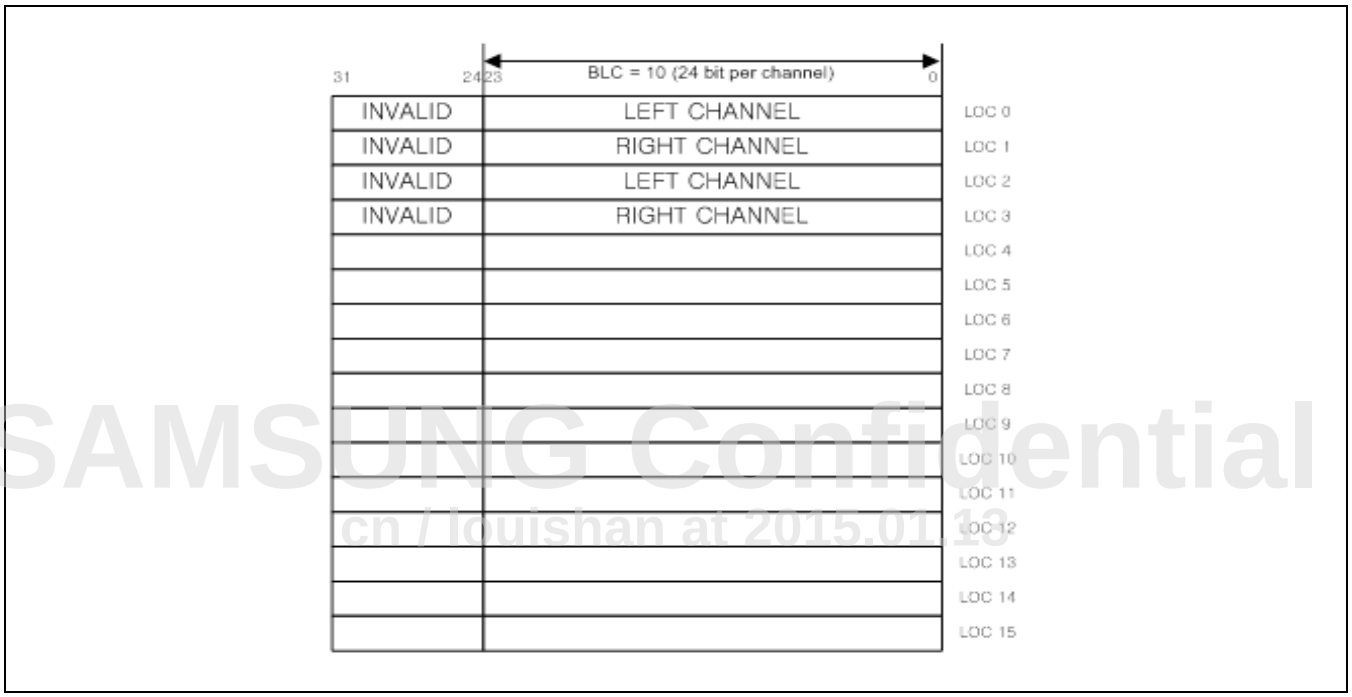


Figure 28-2 Internal Data Path

28.4.2 Operation Flow Chart

When you initialize the AC97 controller, you must assert system reset or cold reset, because the previous state of the external AC97 audio-codec is unknown. This assures that GPIO is already ready. Then you enable the codec ready interrupt. You can check codec ready interrupt by polling or interrupt. When interrupt occurs, you must de-assert codec ready interrupt. Use DMA or PIO (directly to write data to register) to transmit data from memory to register or from register to memory. If internal FIFOs (Tx FIFO or Rx FIFO) are not empty, then let data be transmitted.

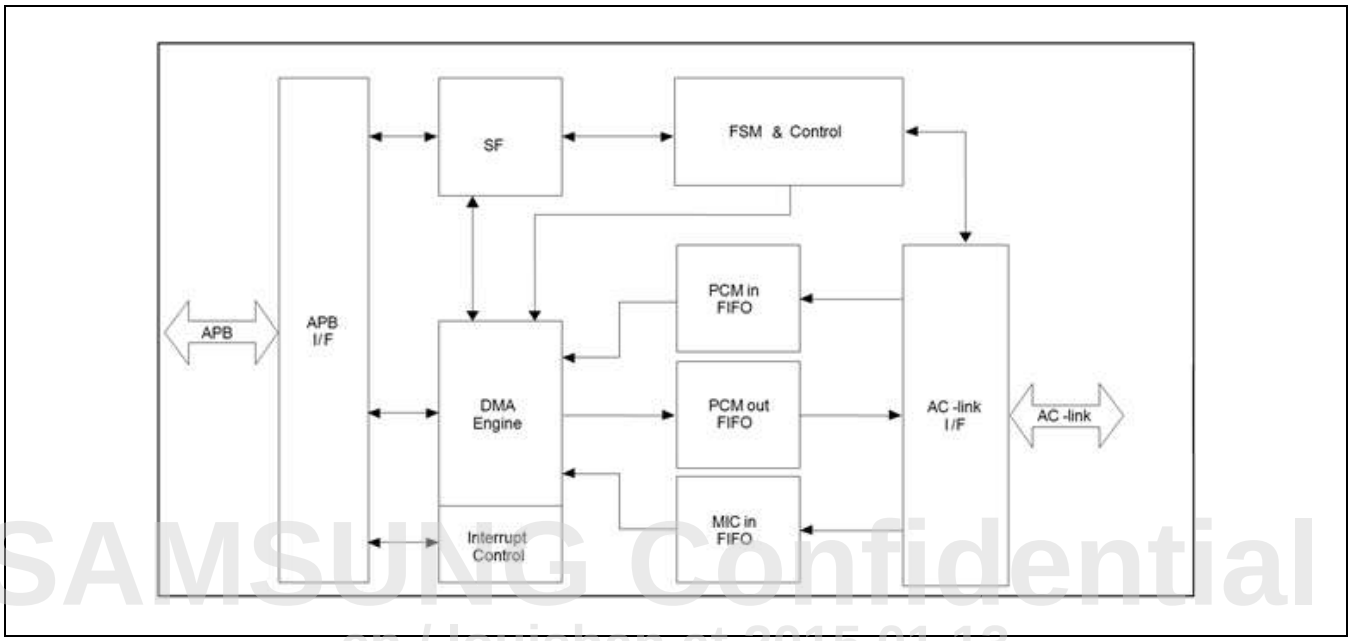


Figure 28-3 AC97 Operation Flow Chart

28.4.3 AC-link Digital Interface Protocol

Each AC97 Codec incorporates a five-pin digital serial interface that links it to the S5P4418 AC97 Controller. AC-link is a full-duplex, fixed-clock and PCM digital stream. It employs a time division multiplexed (TDM) scheme to handle control register accesses and multiple input and output audio streams. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams. Each stream has 20-bit sample resolution and requires a DAC and an analog-to-digital converter (ADC) with a minimum 16-bit resolution.

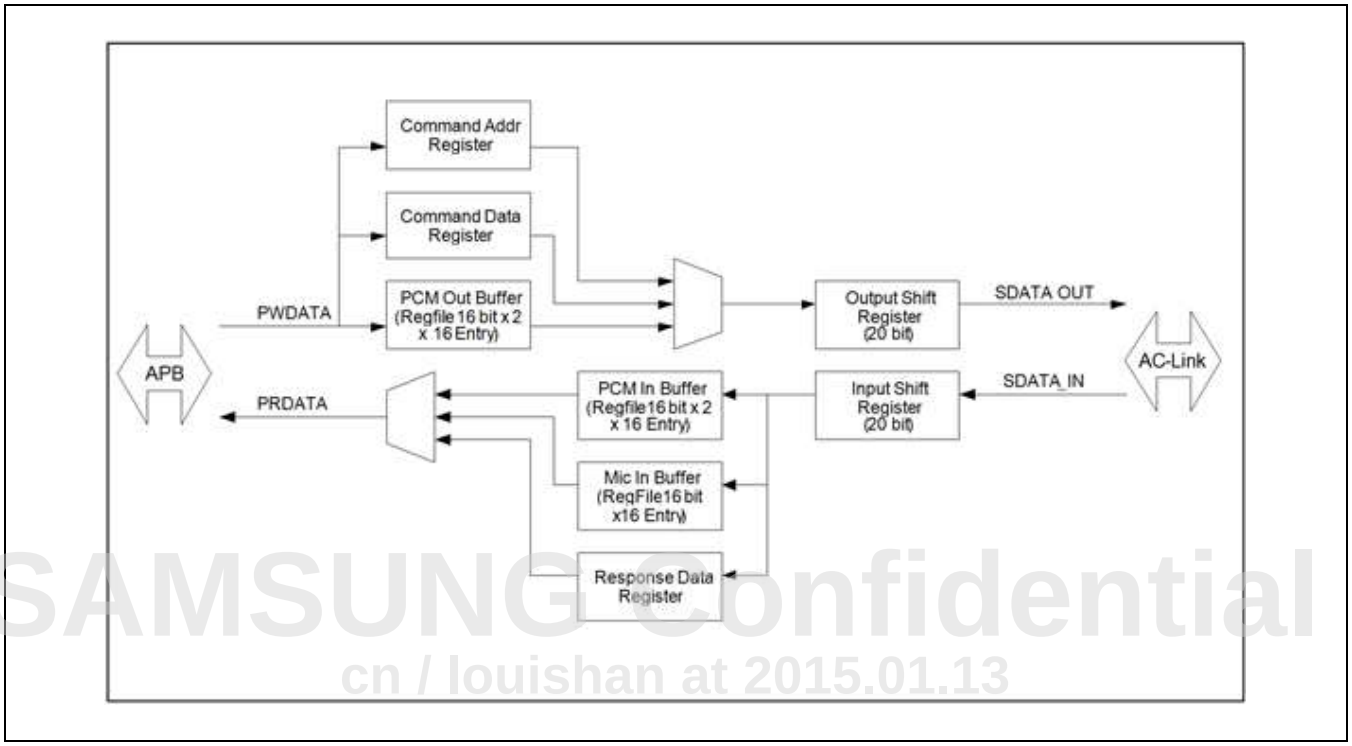


Figure 28-4 Bi-directional AC-link Frame with Slot Assignments

Figure 28-4 shows the slot definitions supported by S5P4418 AC97 Controller. The S5P4418 AC97 Controller provides synchronization for all data transaction on the AC-link.

A data transaction is made up of 256 bits of information broken into groups of 13 time slots and is called a frame. Time slot 0 is called the Tag Phase and it is 16 bits long. The other 12 time slots are called the Data Phase. The Tag Phase contains one bit that identifies a valid frame and 12 bits that identify the time slots in the Data Phase that contain valid data. Each time slot in the Data Phase is 20 bits long. A frame begins when SYNC goes high. The amount of time that SYNC is high corresponds to the Tag Phase. AC97 frames occur at fixed 48 kHz intervals and are synchronous to the 12.288 MHz bit rate clock, BITCLK.

The controller and the Codec use the SYNC and BITCLK to determine when to send transmit data and when to sample received data. A transmitter transfers the serial data stream on each rising edge of BITCLK and a receiver samples the serial data stream on falling edges of BITCLK. The transmitter must tag the valid slots in its serial data stream. The valid slots are tagged in slot 0. Serial data on the AC-link is ordered most significant bit (MSB) to least significant bit (LSB). The Tag Phase's first bit is bit[15] and the first bit of each slot in Data Phase is bit[19]. The last bit in any slot is bit[0].

28.4.3.1 AC-link Output Frame (SDATA_OUT)

Slot 0: Tag Phase

In slot 0, the first bit is a bit (SDATA_OUT, bit[15]) which represents the validity of the entire frame. If bit[15] is 1, the current frame contains at least a valid time slot. The next 12-bit positions correspond each 12 time slot contains valid data. Bits 0 and 1 of slot 0 are used as CODEC IO bits for I/O reads and writes to the CODEC registers as described in the next section. In this way, data streams of differing sample rate can be transmitted across AC-link at its fixed 48 kHz audio frame rate.

Slot 1: Command Address Port

In slot 1, it communicates control register address and write/read command information to the AC97 controller.

When software accesses the primary CODEC, the hardware configures the frame as follows:

- In slot 0, the valid bit for 1, 2 slots are set.
- In slot 1, bit[19] is set (read) or clear (write). Bits 18-12 (of slot 1) are configured to specify the index to the CODEC register. Others are filled with 0's (reserved).
- In slot 2, it configured with the data which is for writing because of output frame.

Slot 2: Command Data Port

In slot 2, this is the write data with 16-bit resolution ([19:4] is valid data)

Slot 3: PCM Playback Left channel*

Slot 3 is audio output frame is the composite digital audio left stream. If a sample has a resolution that is less than 16 bits, the AC97 controller fills all training non-valid bit positions in the slot with zeroes.

Slot 4: PCM Playback Right channel

Slot 4 which is audio output frame is the composite digital audio right stream. If a sample has a resolution that is less than 16 bits, the AC97 controller fills all training non-valid bit positions in the slot with zeroes.

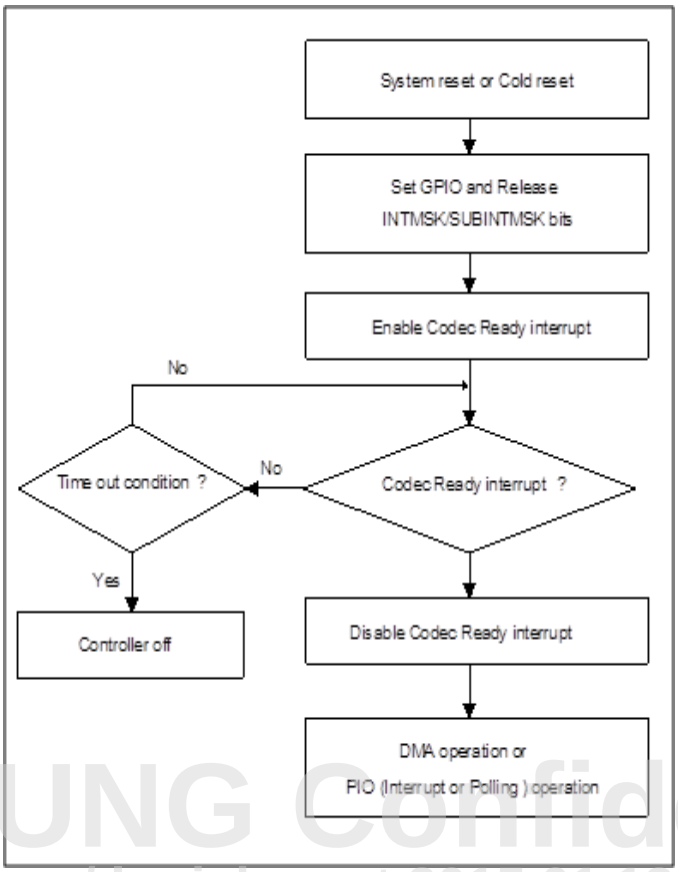


Figure 28-5 AC-link Output Frame

28.4.3.2 AC-link Input Frame (SDATA_IN)

Each AC97 Codec incorporates a five-pin digital serial interface that links it to the S5P4418 AC97 Controller. AC-link is a full-duplex, fixed-clock and PCM digital stream.

Slot 0: Tag Phase

In slot 0, the first bit (SDATA_OUT, bit[15]) indicates whether the AC97 controller is in the CODEC ready state. If the CODEC Ready bit is 0, it means that the AC97 controller is not ready for normal operation. This condition is normal after the power is de-asserted on reset and the AC97 controller voltage references are settling.

Slot 1: Status Address Port/SLOTREQ bits

The status port monitors the status of the AC97 controller functions. It is not limited to mixer settings and power management. Audio input frame slot 1s stream echoes the control register index for the data to be returned in slot 2, if the controller tags slots 1 and 2 as valid during slot 0. The controller only accepts status data if the accompanying status address matches the last valid command address issued during the most recent read command. For multiple sample rate output, the CODEC examines its sample-rate control registers, its FIFOs' states, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current audio input frame indicate which output slots require data from the controller in the next audio output frame. For fixed 48 kHz operation, the SLOTREQ bits are set active (low), and a sample is transferred in each frame. For multiple sample-rate input, the "tag" bit for each input slot indicates whether valid data is present.

Table 28-1 Input Slot 1-bit Definitions

Bit	Description
[19]	Reserved (Filled with zero)
[18:12]	Control register index (Filled with zeroes if AC97 tags is invalid)
[11]	Slot 3 request: PCM Left channel
[10]	Slot 4 request: PCM Right channel
[9]	Slot 5 request: NA
[8]	Slot 6 request: MIC channel
[7]	Slot 7 request: NA
[6]	Slot 8 request: NA
[5]	Slot 9 request: NA
[4]	Slot 10 request: NA
[3]	Slot 11 request: NA
[2]	Slot 12 request: NA
[1:0]	Reserved (Filled with zero)

Slot 2: Status Data Port

In slot 2, this is the status data with 16-bit resolution ([19:4] is valid data)

Slot 3: PCM Record Left channel

Slot 3 which is audio input frame is the left channel audio output of the AC97 Codec. If a sample has a resolution that is less than 16 bits, the AC97 Codec fills all training non-valid bit positions in the slot with zeroes.

Slot 4: PCM Record Right channel

Slot 4 which is audio input frame is the right channel audio output of the AC97 Codec. If a sample has a resolution that is less than 16 bits, the AC97 Codec fills all training non-valid bit positions in the slot with zeroes.

Slot 6: Microphone Record Data

The AC97 Controller supports 16-bit resolution for the MIC-in channel.

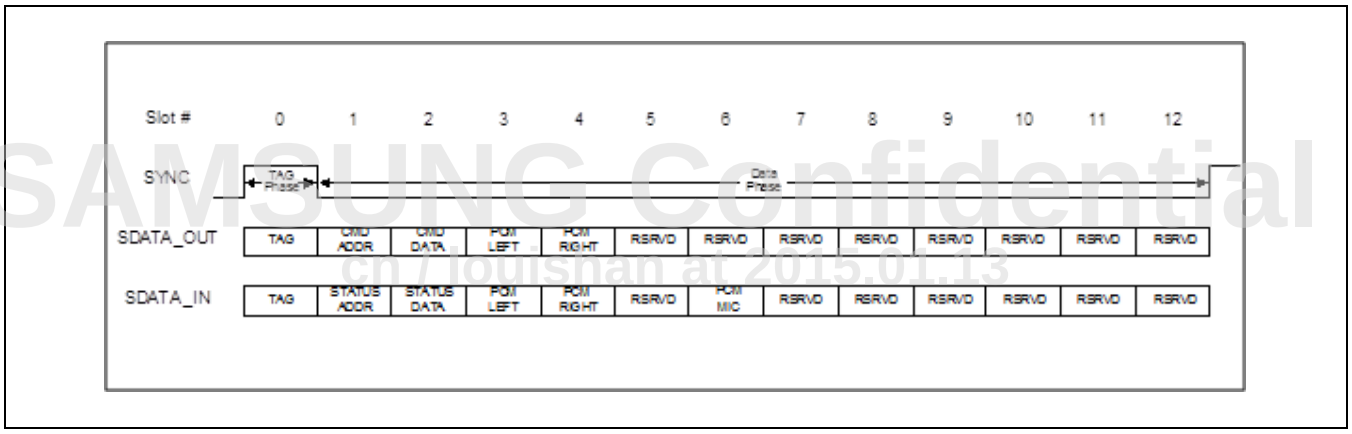


Figure 28-6 AC-Link Input Frame

28.4.4 AC97 Power-down

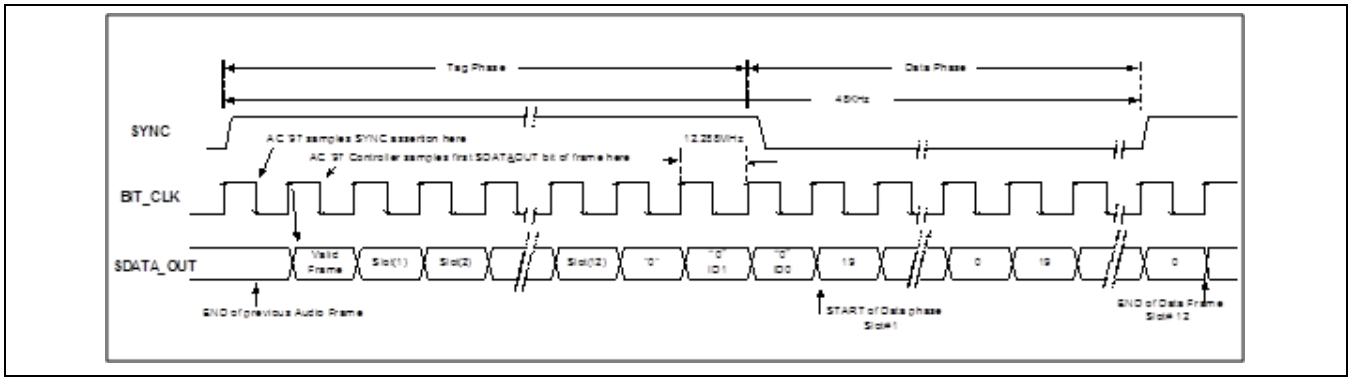


Figure 28-7 AC97 Power-Down Timing

28.4.4.1 Powering Down the AC-Link

The AC-link signals enter a low power mode when the AC97 Codec Power-down register (0x26) bit PR4 is set to 1 (by writing 0x1000). Then the Primary Codec drives both BITCLK and SDATA_IN to a logic low voltage level. The sequence follows the timing diagram as shown in *Figure 28-7*.

The AC97 Controller transmits the write to Power-down register (0x26) via AC-link. Set up the AC97 Controller so that it does not transmit data to slots 3-12 when it writes to the Power-down register bit PR4 (data 0x1000), and it does not require the Codec to process other data when it receives a power down request. When the Codec processes the request it immediately transfers BITCLK and SDATA_IN to a logic low level. The AC97 Controller drives SYNC and SDATA_OUT to a logic low level after programming the AC_GLBCTRL register.

28.4.4.2 Waking Up the AC-Link - Wake Up Triggered by the AC97 Controller

AC-link protocol provides a cold AC97 reset and a warm AC97 reset. The current power-down state ultimately dictates which AC97 reset is used. Registers must stay in the same state during all power-down modes unless a cold AC97 reset is performed. In a cold AC97 reset, the AC97 registers are initialized to their default values. After a power down, the AC-link must wait for a minimum of four audio frame times after the frame in which the power down occurred before it can be reactivated by reasserting the SYNC signal. When AC-link powers up, Codec ready bit (input slot 0, bit[15]) indicates that AC-link is ready for operation.

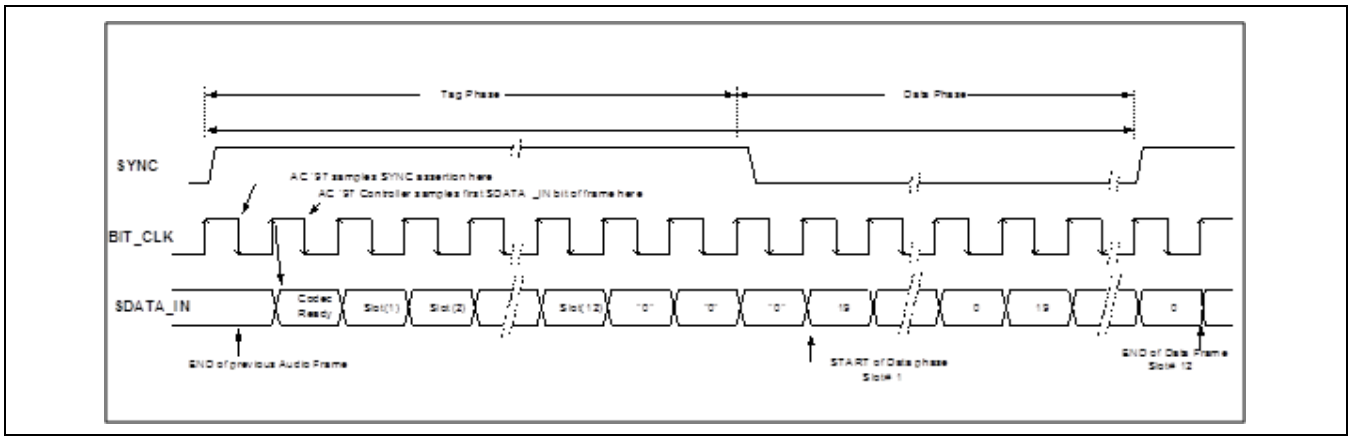


Figure 28-8 AC97 Power Down/Power Up Flow

28.4.4.3 Cold AC97 Reset

A cold reset is generated when the nRESET pin is asserted through the AC_GLBCTRL. Asserting and de-asserting nRESET activates BITCLK and SDATA_OUT. A cold reset initializes all of AC97 control registers. nRESET is an asynchronous AC97 input.

28.4.4.4 Warm AC97 Reset

A Warm AC97 reset reactivates the AC-link without altering the current AC97 register values. A warm reset is generated when BITCLK is absent and SYNC is driven high. In normal audio frames, SYNC is a synchronous AC97 input. When BITCLK is absent, SYNC is treated as an asynchronous input used to generate a warm reset to AC97.The AC97 Controller must not activate BITCLK until it samples SYNC low again. This prevents a new audio frame being falsely detected.

28.4.4.5 AC97 State Diagram

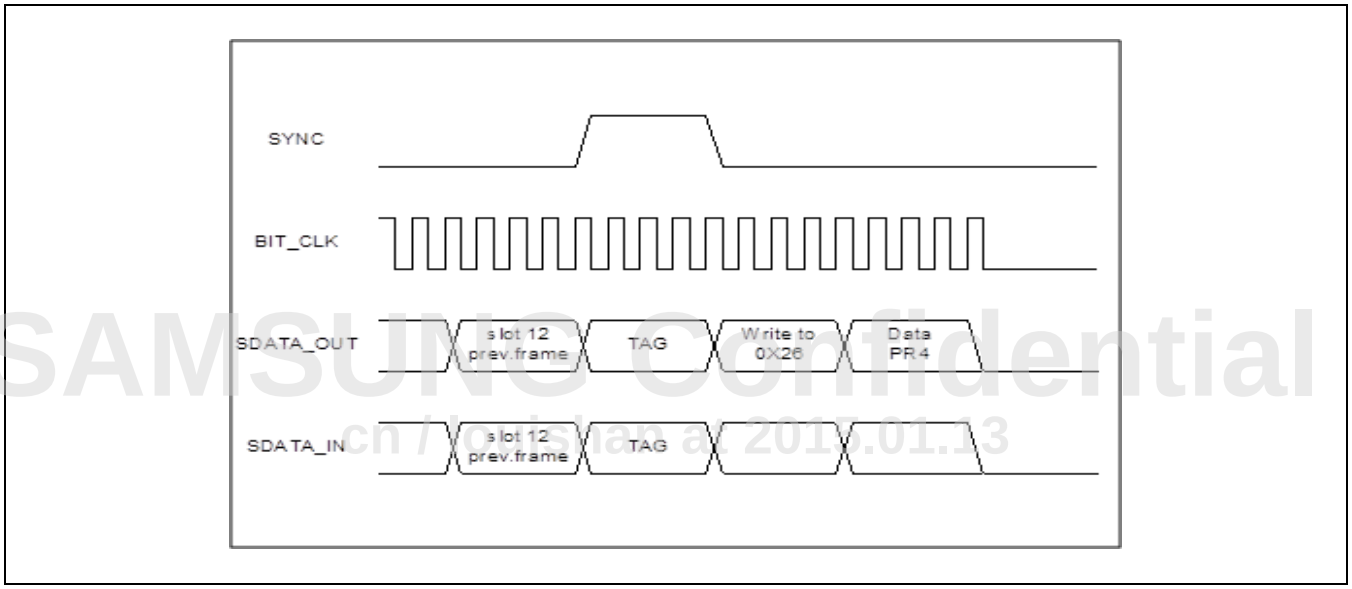


Figure 28-9 AC97 State Diagram

Figure 28-9 shows the state diagram of AC97 controller. It is useful to check AC97 controller state machine. State machine shown in above figure is synchronized by peripheral clock (PCLK). Use AC_GLBSTAT register to monitor state.

28.5 Register Description

28.5.1 Register Map Summary

- Base Address: 0xC005_0000

Register	Offset	Description	Reset Value
AC_GLBCTRL	8000h	AC97 global control register	0x0000_0000
AC_GLBSTAT	8004h	AC97 global status register	0x0000_0000
AC_CODEC_CMD	8008h	AC97 codec command register	0x0000_0000
AC_CODEC_STAT	800Ch	AC97 codec status register	0x0000_0000
AC_PCMADDR	8010h	AC97 PCM out/in channel FIFO address register	0x0000_0000
AC_MICADDR	8014h	AC97 MIC In channel FIFO address register	0x0000_0000
AC_PCMDATA	8018h	AC97 PCM out/in channel FIFO data register	0x0000_0000
AC_MICDATA	801Ch	AC97 MIC in channel FIFO data register	0x0000_0000

28.5.1.1 AC_GLBCTRL

- Base Address: 0xC005_0000
- Address = Base Address + 8000h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	–
Codec ready interrupt clear	[30]	RW	1 = Interrupt clear (write only)	1'b0
PCM out channel underrun interrupt clear	[29]	RW	1 = Interrupt clear (write only)	1'b0
PCM in channel overrun interrupt clear	[28]	RW	1 = Interrupt clear (write only)	1'b0
MIC in channel overrun interrupt clear	[27]	RW	1 = Interrupt clear (write only)	1'b0
PCM out channel threshold interrupt clear	[26]	RW	1 = Interrupt clear (write only)	1'b0
PCM in channel threshold interrupt clear	[25]	RW	1 = Interrupt clear (write only)	1'b0
MIC in channel threshold interrupt clear	[24]	RW	1 = Interrupt clear (write only)	1'b0
RSVD	[23]	–	Reserved	–
Codec ready interrupt enable	[22]	RW	0 = Disables 1 = Enables	1'b0
PCM out channel underrun interrupt enable	[21]	RW	0 = Disables 1 = Enables (FIFO is empty)	1'b0
PCM in channel overrun interrupt enable	[20]	RW	0 = Disables 1 = Enables (FIFO is full)	1'b0
Mic in channel overrun interrupt enable	[19]	RW	0 = Disables 1 = Enables (FIFO is full)	1'b0
PCM out channel threshold interrupt enable	[18]	RW	0 = Disables 1 = Enables (FIFO is half empty)	1'b0
PCM in channel threshold interrupt enable	[17]	RW	0 = Disables 1 = Enables (FIFO is half full)	1'b0
MIC in channel threshold interrupt enable	[16]	RW	0 = Disables 1 = Enables (FIFO is half full)	1'b0
RSVD	[15:14]	–	Reserved	–
PCM out channel transfer mode	[13:12]	RW	00 = Off 01 = PIO 10 = DMA 11 = Reserved	2'b0
PCM in channel transfer mode	[11:10]	RW	00 = Off 01 = PIO 10 = DMA 11 = Reserved	2'b0
MIC in channel transfer mode	[9:8]	RW	00 = Off 01 = PIO 10 = DMA	2'b0

Name	Bit	Type	Description	Reset Value
			11 = Reserved	
RSVD	[7:4]	–	Reserved	–
Transfer data enable using AC-link	[3]	RW	0 = Disables 1 = Enables	1'b0
AC-Link on	[2]	RW	0 = Off 1 = SYNC signal transfer to Codec	1'b0
Warm reset	[1]	RW	0 = Normal 1 = Wake up codec from power down	1'b0
Cold reset	[0]	RW	0 = Normal 1 = Reset Codec and Controller logic NOTE: # During Cold reset, writing to any AC97 Registers is not affected. When recovering from Cold reset, writing to any AC97 Registers is not affected. Example: For consecutive Cold reset and Warm reset, first set AC_GLBCTRL = 0x1 then set AC_GLBCTRL = 0x0. After recovering from cold reset set AC_GLBCTRL = 0x2 then AC_GLBCTRL = 0x0.	1'b0

28.5.1.2 AC_GLBSTAT

- Base Address: 0xC005_0000
- Address = Base Address + 8004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:23]	–	Reserved	–
Codec ready interrupt	[22]	R	0 = Not requested 1 = Requested	1'b0
PCM out channel underrun interrupt	[21]	R	0 = Not requested 1 = Requested	1'b0
PCM in channel overrun interrupt	[20]	R	0 = Not requested 1 = Requested	1'b0
MIC in channel overrun interrupt	[19]	R	0 = Not requested 1 = Requested	1'b0
PCM out channel threshold interrupt	[18]	R	0 = Not requested 1 = Requested	1'b0
PCM in channel threshold interrupt	[17]	R	0 = Not requested 1 = Requested	1'b0
MIC in channel threshold interrupt	[16]	R	0 = Not requested 1 = Requested	1'b0
RSVD	[15:3]	–	Reserved	–
Controller main state	[2:0]	R	000 = Idle 001 = Init 010 = Ready 011 = Active 100 = LP 101 = Warm	3'b0

28.5.1.3 AC_CODEC_CMD

- Base Address: 0xC005_0000
- Address = Base Address + 8008h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	–
Read enable	[23]	RW	0 = Command write 1 = Status read	1'b0
Address	[22:16]	RW	Codec command address	7'b0
Data	[15:0]	RW	Codec command data	16'b0

28.5.1.4 AC_CODEC_STAT

- Base Address: 0xC005_0000
- Address = Base Address + 800Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:23]	–	Reserved	–
Address	[22:16]	R	Codec command address	7'b0
Data	[15:0]	R	Codec command data	16'b0

28.5.1.5 AC_PCMADDR

- Base Address: 0xC005_0000
- Address = Base Address + 8010h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	–	Reserved	–
Out read address	[27:24]	R	PCM out channel FIFO read address	4'b0
RSVD	[23:20]	–	Reserved	–
In read address	[19:16]	R	PCM in channel FIFO read address	4'b0
RSVD	[15:12]	–	Reserved	–
Out write address	[11:8]	R	PCM out channel FIFO write address	4'b0
RSVD	[7:4]	–	Reserved	–
In write address	[3:0]	R	PCM in channel FIFO write address	4'b0

28.5.1.6 AC_MICADDR

- Address = Base Address + 8014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:20]	–	Reserved	–
Out write address	[19:16]	R	MIC in channel FIFO read address	4'b0
RSVD	[15:4]	–	Reserved	–
In write address	[3:0]	R	MIC in channel FIFO write address	4'b0

28.5.1.7 AC_PCMDATA

- Base Address: 0xC005_0000
- Address = Base Address + 8018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Right data	[31:16]	RW	PCM out/in right channel FIFO data Read = PCM in right channel Write = PCM out right channel	16'b0
Left data	[15:0]	RW	PCM out/in left channel FIFO data Read = PCM in left channel Write = PCM out left channel	16'b0

28.5.1.8 AC_MICDATA

- Base Address: 0xC005_0000
- Address = Base Address + 801Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	–
Mono data	[15:0]	RW	MIC in mono channel FIFO data	16'b0

29 SPDIF TX

29.1 Overview

The SPDIF transmitter is based on IEC60958. This Section describes a serial, unidirectional, self-clocking interface to interconnect digital audio equipment in consumer and professional applications.

When you use a consumer digital processing environment in SPDIF standard, the SPDIF interface is primarily intended to carry stereophonic programs, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.

When you use SPDIF in a broadcasting studio environment, the interface is primarily intended to carry monophonic or stereophonic programs, at a 48 kHz sampling frequency and with a resolution of up to 24 bits per sample; it can carry one or two signals sampled at 32 kHz.

In both cases, the clock references and auxiliary information are transmitted with the program. IEC60958 enables the interface to carry software related data.

29.2 Features

Features of SPDIF-TX are:

- SPDIFOUT module only supports the consumer application in S5P4418
- Supports linear PCM up to 24-bit per sample
- Supports Non-linear PCM formats such as AC3, MPEG1 and MPEG2
- 2 × 24-bit buffers which is alternately filled with data

29.3 Block Diagram

Figure 29-1 illustrates the block diagram of SPDIFOUT.

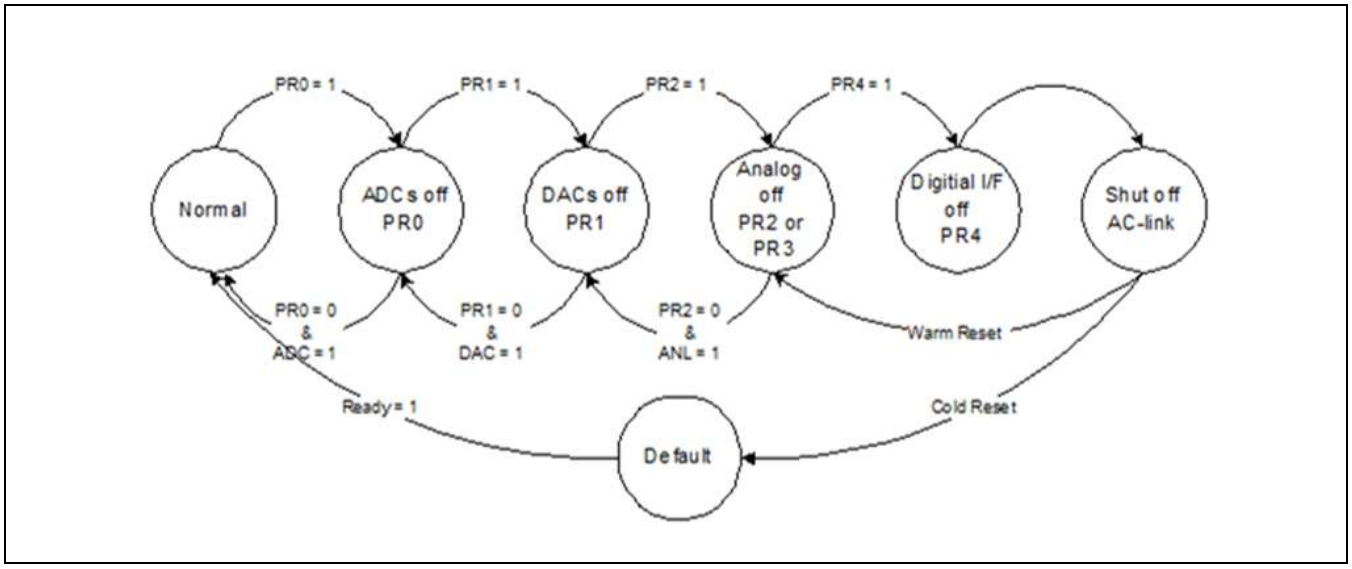


Figure 29-1 Block Diagram of SPDIFOUT

Components in SPDIF Transmitter:

- **APB interface block:** This block defines register banks to control the driving of SPDIFOUT module and data buffers to store linear or non-linear PCM data.
- **DMA interface block:** This block requests DMA service to IODMA that depends on the status of data buffer in APB Interface block.
- **Clock Generator block:** This block generates 128 fs (sampling frequency) clock that is used in out_spdif block from system audio clock (MCLK).
- **Audio_if_core block:** This block acts as an interface block between data buffer and out_spdif block. Finite-state machine controls the flow of PCM data.
- **spdif_tx block:** This block inserts burst preamble and executes zero-stuffing in the nonlinear PCM stream. The spdif_tx module bypasses the linear PCM data.
- **out_spdif block:** This block generates SPDIF format. It inserts 4-bit preamble, 16- or 20- or 24-bit data, user-data bit, validity bit, channel status bit, and parity bit into the appropriate position of 32-bit word. It modulates each bit to bi-phase format.

29.4 Functional Description

This section includes:

- Data Format of SPDIF
- Channel Coding
- Preamble
- Non-Linear PCM Encoded Source (IEC 61937)
- SPDIF Operation
- Shadowed Register

29.4.1 Data Format of SPDIF

This section includes:

- Frame Format
- Sub-frame Format (IEC 60958)

29.4.1.1 Frame Format

A frame is uniquely composed of two sub-frames. The transmission rate of frames corresponds exactly to the source sampling frequency.

In the 2-channel operation mode, the time multiplexing transmits samples taken from both channels in consecutive sub-frames.

The sub-frames related to channel 1 (left or "A" channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B after every 192 frame. This unit, which is composed of 192 frames, defines the block structure that is used to organize the channel status information. Sub-frames of channel 2 (right or "B" in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

In the single-channel operation mode in broadcasting studio environment, the frame format is identical to the 2-channel mode. Data is carried only in channel 1. In the sub-frames allocated to channel 2, time slot 28 (validity flag) should be set to logical "1" ("1" means not valid).

Figure 29-2 illustrates the format of SPDIF frame.

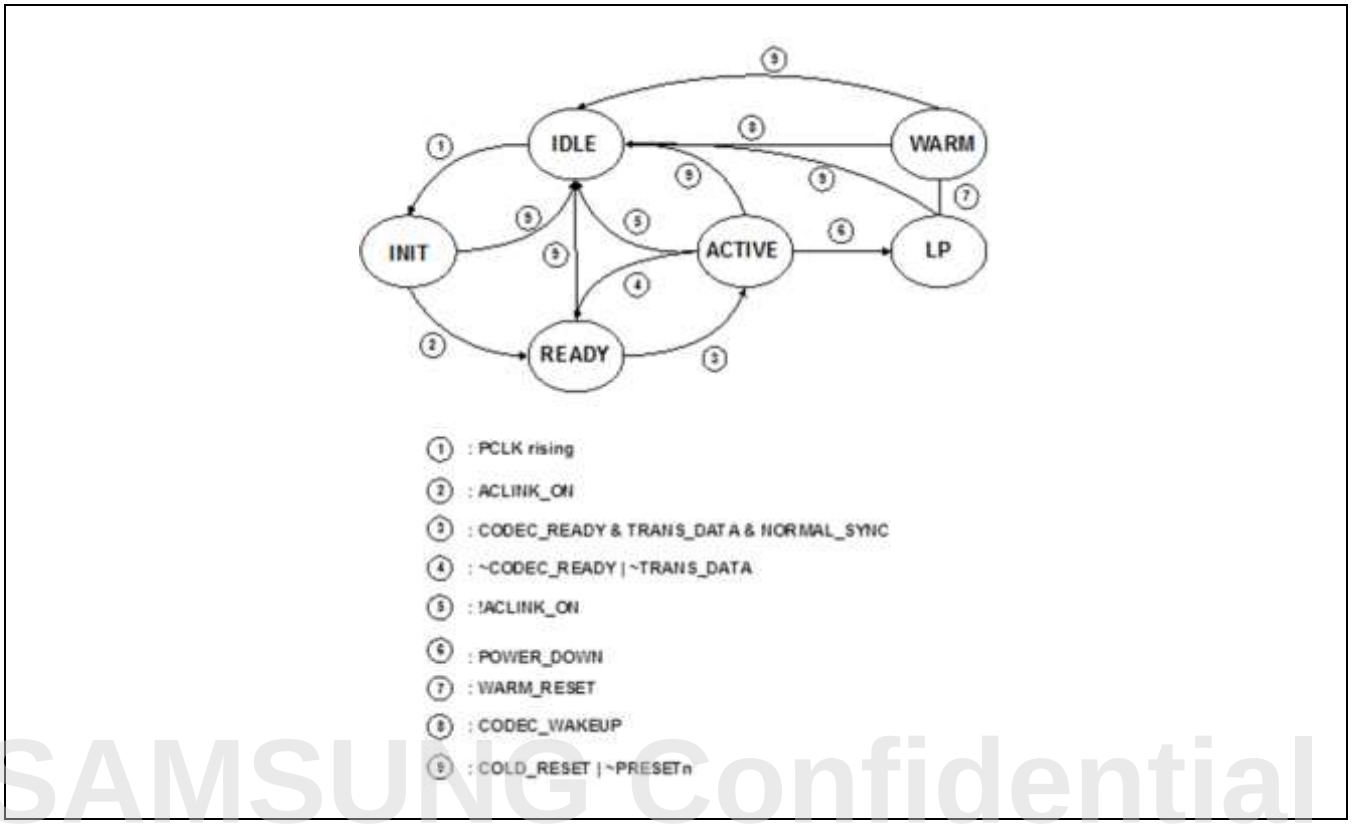


Figure 29-2 SPDIF Frame Format

29.4.1.2 Sub-frame Format (IEC 60958)

Each sub-frame is divided into 32 time slot, numbered from 0 to 31. Time slots 0 to 3 carry one of the three permitted preambles. These are used to affect synchronization of sub-frames, frames, and blocks. Time slots 4 to 27 carry the audio sample word in linear 2's complement representation. Time slot 27 carries the most significant bit. When a 24-bit coding range is used, the least significant bit is in time slot 4.

When a 20-bit coding range is sufficient, the least significant bit is in time slot 8. Time slots 4 to 7 may be used for other application. Under these circumstances, the bits in the time slots 4 to 7 are designated auxiliary sample bits.

If the source provides fewer bit than the interface allows (20 or 24 bits), the unused least significant bits shall be set to a logical "0". This procedure supports that SPDIF connect equipment by using different numbers of bits. Time slot 28 carries the validity flag associated with the audio sample word. This flag is set to logical "0" when the audio sample is reliable. Time slot 29 carries 1 bit of the user data associated with the audio channel that is transmitted in the same sub-frame. The default value of the user bit is logical "0".

Time slot 30 carries 1 bit of the channel status words associated with the audio channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that the time slots, including 4 to 31 carries an even number of ones and zeros.

Figure 29-3 illustrates format of SPDIF sub-frame.

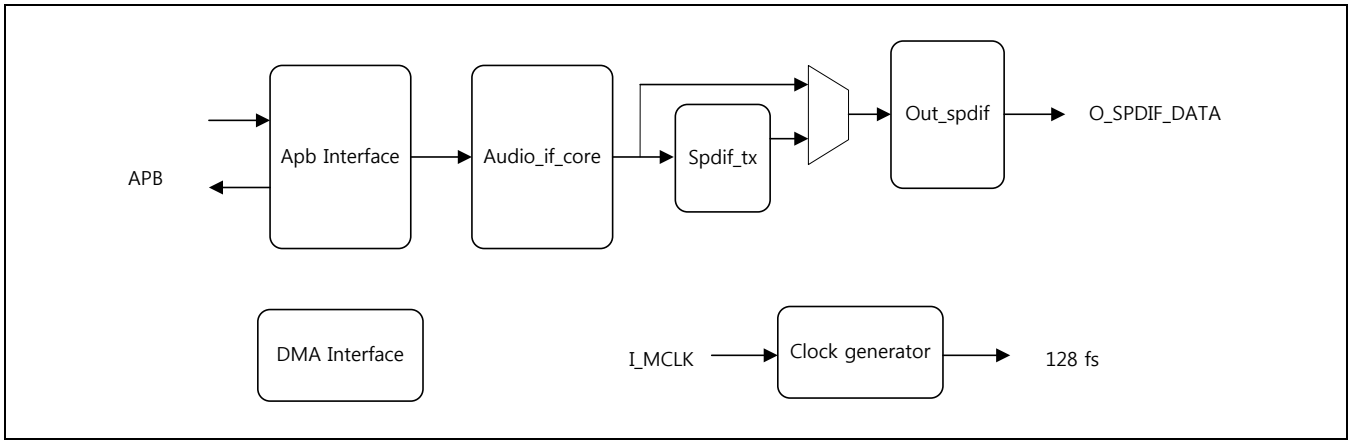


Figure 29-3 SPDIF Sub-frame Format

29.4.2 Channel Coding

Time slots 4 to 31 are encoded in biphase-mark to:

- Minimize the dc component on the transmission line
- Facilitate clock recovery from the data stream
- Make the interface insensitive to the polarity of connections

A symbol comprising two consecutive binary states represents each bit to be transmitted:

- The first state of a symbol is always different from the second state of the previous symbol.
- The second state of the symbol is identical to the first when the bit to be transmitted is logical "0" and is different from the first when the bit is logical "1".

Figure 29-4 illustrates channel coding.

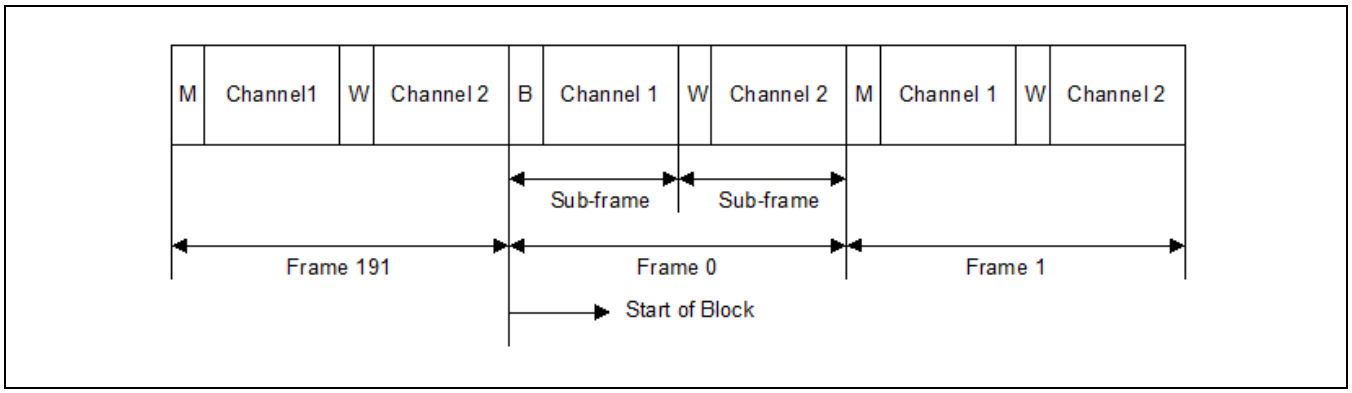


Figure 29-4 SPDIF Sub-frame Format

29.4.3 Preamble

Preambles are specific patterns that provide synchronization and identification of the sub-frames and blocks. A set of three preambles (M, B, and W) is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

Similar to bi-phase code, these preambles are dc free and provide clock recovery. They differ in minimum two states from any valid bi-phase sequence.

29.4.4 Non-Linear PCM Encoded Source (IEC 61937)

The non-linear PCM encoded audio bit stream is transferred by using the basic 16-bit data area of the IEC 60958 sub frames, that is, in time slots 12 to 27. Each IEC 60958 frame can transfer 32 bits of the non-PCM data in consumer application mode.

When the SPDIF bit stream conveys linear PCM audio, the symbol frequency is 64 times the PCM sampling frequency (32 time slots per two channels of PCM sample time). When a non-linear PCM encoded audio bit stream is transmitted by the interface, the symbol frequency shall be 64 times the sampling rate of the encoded audio within that bit stream. If a non-linear PCM encoded audio bit stream is transmitted by the interface containing audio with low sampling frequency, the symbol frequency shall be 128 times the sampling rate of the encoded audio within that bit stream.

Each data burst contains a burst-preamble consisting of four 16-bit words (Pa, Pb, Pc, and Pd), followed by the burst-payload, which contains data of an encoded audio frame.

The burst-preamble consists of four mandatory fields:

- Pa and Pb represent a synchronization word.
- Pc provides information about the type of data and some information/control for the receiver.
- Pd provides the length of the burst-payload, limited to 216 (= 65,535) bits.

The four preamble words are contained in two sequential SPDIF frames. The frame beginning the data-burst contains preamble word Pa in sub-frame 1 and Pb in sub-frame 2. The next frame contains Pc in sub-frame 1 and Pd in sub-frame 2. When placed into a SPDIF sub-frame, the MSB of a 16-bit burst-preamble is placed into time slot 27 and the LSB is placed into time slot 12.

Figure 29-5 illustrates format of Burst Payload.

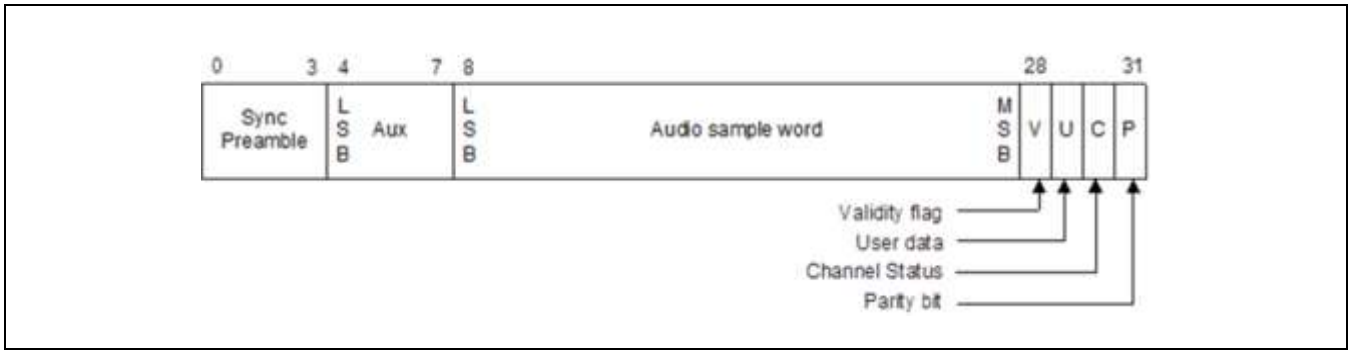


Figure 29-5 Format of Burst Payload

Table 29-1 lists the burst preamble words.

Table 29-1 Burst Preamble Words

Preamble Word	Length of Field	Contents	Value MSB LSB
Pa	16 bits	Sync word 1	0xF872
Pb	16 bits	Sync word 2	0x4E1F
Pc	16 bits	Burst-info	Refer to SPDBSTAS_SHD[15:0] for more information.
Pd	16 bits	Length-code	Refer to SPDBSTAS_SHD[31:16] for more information.

29.4.5 SPDIF Operation

The bit frequency of SPDIF is 128 fs (fs: sampling frequency). Therefore, divide audio main clock (MCLK) depending on the frequency of MCLK to make the main clock of SPDIF. You can divide MCLK by:

- 2 in case of 256 fs
- 3 in case of 384 fs
- 4 in case of 512 fs

The SPDIF module in Exynos5250 changes the audio sample data format to SPDIF. To change the format, SPDIF module inserts these into the appropriate time slots:

- Preamble data
- Channel status data
- User data
- Error check bit
- Parity bit

Preamble data are fixed in the module and inserted depending on sub-frame counter. Channel status data are set in the SPDCSTAS register and used by 1 bit per frame. User data always have zero values.

For non-linear PCM data, insert burst-preamble, which consists of Pa, Pb, Pc, and Pd before burst-payload and zero is padded from the end of burst-payload to the repetition count. Pa (= 16'hF872) and Pb (= 16'h4E1F) is fixed in the module and Pc and Pd is set in the register SPDBSTAS. To stuff zero, the end of burst-payload is calculated from Pd value and repetition count that depends on data type in the preamble Pc is acquired from register SPDCNT.

Audio data are justified to the LSB. 16-, 20- or 24-bit PCM data and 16-bit stream data are supported. The unoccupied upper bits of 32-bit word are ignored.

Data are fetched via DMA request. When one of two data buffers is empty, DMA service is requested. Audio data that are stored in the data buffers are transformed into SPDIF format and output to the port. For non-linear PCM data, interrupt is generated after audio data are output up to the value specified in the SPDCNT register. Interrupt sets the registers such as SPDBSTAS and SPDCNT to new values when the data type of new bit stream is different from the previous one.

29.4.6 Shadowed Register

Both SPDBSTAS_SHD and SPDCNT_SHD registers are shadowed registers that are related to SPDBSTAS and SPDCNT registers, respectively. They are updated from related registers at every stream end interrupt signal. The usage of shadowed register is as follows.

1. Set burst status and repetition count information to their respective registers.
2. Turn on SPDIF module, and stream end interrupt is asserted immediately.
3. With stream end interrupt, shadowed registers are updated from their related registers and SPDIF starts to transfer data.
4. The next stream information (burst status and repetition count) can be written to SPDBSTAS and SPDCNT register because the previous information is copied to their respective shadowed registers.
5. Set next stream information to SPDBSTAS and SPDCNT registers.
6. Wait for stream end interrupt that signals the end of the first stream.
7. With stream end interrupt, the second stream data will start to transfer.
8. Set third stream information to registers.

The usage of user bit registers is similar to stream information registers. However, these registers are not related to SPDIF end interrupt but to user data interrupt. As soon as SPDIF is on, the shadowed user bit registers are updated from their related registers and user bit starts to be shifted out with asserted user data interrupt. User can write the next user data to registers with this interrupt. After entire 96 user bits are shifted out, user data interrupt will be asserted again and 3rd user bits can be written to registers with second user bits going out.

29.5 Register Description

29.5.1 Register Map Summary

- Base Address: 0x0000_0000

Register	Offset	Description	Reset Value
SPDCLKCON	9000h	Clock control register	0x0000_0000
SPDCON	9004h	Control register	0x0000_0000
SPDBSTAS	9008h	Burst status register	0x0000_0000
SPDCSTAS	900Ch	Channel status register	0x0000_0000
SPDDAT	9010h	SPDIFOUT data buffer	0x0000_0000
SPDCNT	9014h	Repetition count register	0x0000_0000
SPDBSTAS_SHD	9018h	Shadowed burst status register	0x0000_0000
SPDCNT_SHD	901Ch	Shadowed repetition count register	0x0000_0000
USERBIT1	9020h	Sub-code Q1 to Q32	0x0000_0000
USERBIT2	9024h	Sub-code Q33 to Q64	0x0000_0000
USERBIT3	9028h	Sub-code Q65 to Q96	0x0000_0000
USERBIT1_SHD	902Ch	Shadowed register userbit1	0x0000_0000
USERBIT2_SHD	9030h	Shadowed register userbit2	0x0000_0000
USERBIT3_SHD	9034h	Shadowed register userbit3	0x0000_0000
VERSION_INFO	9038h	RTL version information	0x0000_0000

29.5.1.1 SPDCLKCON

- Base Address: 0x0000_0000
- Address = Base Address + 9000h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	–	Reserved	–
MCLK SEL	[3:2]	RW	Main audio clock selection 0 = Internal Clock (I_MCLK_INT) 1 = External Clock (I_MCLK_EXT0)	2'h0
SPDIFOUT Clock Down Ready	[1]	R	0 = Clock-down not ready 1 = Clock-down ready	1'h0
SPDIFOUT power on	[0]	RW	0 = Power off 1 = Power on	1'h0

29.5.1.2 SPDCON

- Base Address: 0x0000_0000
- Address = Base Address + 9004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	–	Reserved	–
FIFO level	[30:22]	R	FIFO Level Monitoring (Read Only) FIFO depth is 16 0 = Empty of FIFO Level 16 = Full of FIFO Level	5'h0
FIFO level threshold	[21:19]	RW	FIFO Threshold Level is controllable 000 = 0-FIFO Level 001 = 1-FIFO Level 010 = 4-FIFO Level 011 = 6-FIFO Level 100 = 10-FIFO Level 101 = 12-FIFO Level 110 = 14-FIFO Level 111 = 15-FIFO Level	3'h0
FIFO transfer mode	[18:17]	RW	00 = DMA transfer mode 01 = Polling mode 10 = Interrupt mode 11 = Reserved	2'h0
FIFO_level interrupt status	[16]	RW	Read Operation 0 = No interrupt pending 1 = Interrupt pending Write Operation 0 = No effect 1 = Clear this flag	1'h0
FIFO_level interrupt	[15]	RW	0 = Interrupt masked	1'h0

Name	Bit	Type	Description	Reset Value
enable			1 = Enable interruptv	
endian format	[14:13]	RW	00 = big endian • o_data = {in_data[23:0]} 01 = 4 byte swap • o_data={in_data[15:8], in_data[23:16], in_data[31:24]} 10 = 3 byte swap • o_data={in_data[7:0], in_data[15:8], in_data[23:16]} 11 = 2 byte swap • o_data={0x00,in_data[7:0], in_data[15:8]} NOTE: in_data: BUS → in port of SPDIF o_data: in port of SPDIF → Logic	2'h0
user_data_attach	[12]	RW	0 = User data is stored in USERBIT register. User data of sub-frame is out from USERBIT1, 2, 3 (96-bit) 1 = User data is stored in 23rd bit of audio data. User data is out in 23th bit of PCM data.	1'h0
User data interrupt status	[11]	RW	Read Operation 0 = No interrupt pending 1 = Interrupt pending when 96-bit of user data is out. Write Operation 0 = No effect 1 = Clear this flag	1'h0
User data interrupt enable	[10]	RW	0 = Interrupt masked 1 = Enables interrupt	1'h0
Buffer empty interrupt status	[9]	RW	Read Operation 0 = No interrupt pending 1 = Interrupt pending Write Operation 0 = No effect 1 = Clears this flag	1'h0
Buffer empty interrupt enable	[8]	RW	0 = Interrupt masked 1 = Enables interrupt	1'h0
Stream end interrupt status	[7]	RW	Read Operation 0 = No interrupt pending 1 = Interrupt pending when the number of output audio data reaches repetition count in SPDCNT register Write Operation 0 = No effect 1 = Clears this flag.	1'h0
Stream end interrupt	[6]	RW	0 = Interrupt masked	1'h0

Name	Bit	Type	Description	Reset Value
enable			1 = Enables interrupt	
software reset	[5]	RW	0 = Normal operation 1 = Software reset Software reset is 1-cycle pulse (auto clear) Enables I_MCLK before software reset assertion because SPDIF uses synchronous reset	1'h0
Main audio clock frequency	[4:3]	RW	00 = 256 fs 01 = 384 fs 10 = 512 fs 11 = Reserved If you want to use SPDIF on HDMI, select 512 fs because HDMI in Exynos5250 accepts only 512 fs or more frequency.	2'h0
PCM data size	[2:1]	RW	00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = Reserved	2'h0
PCM or stream	[0]	RW	0 = Stream 1 = PCM	1'h0

29.5.1.3 SPDBSTAS

- Base Address: 0x0000_0000
- Address = Base Address + 9008h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Burst data length bit	[31:16]	RW	ES size in bits (Burst Preamble Pd) ES size: Elementary Stream size This indicates Burst-payload length	16'h0
Bit stream number	[15:13]	RW	Bit_stream_number should be set to 0	3'h0
Data type dependent info	[12:8]	RW	Data type dependent information	5'h0
Error flag	[7]	RW	0 = Error flag indicates a valid burst_payload 1 = Error flag indicates that the burst payload may contain errors	1'h0
RSVD	[6:5]	–	Reserved	–
Compressed data type	[4:0]	RW	00000 = Null Data 00001 = AC-3 00010 = Reserved 00011 = Pause 00100 = MPEG1 (layer1) 00101 = MPEG1 (layer2, 3), MPEG2-bc 00110 = MPEG2-extension 00111 = Reserved 01000 = MPEG2 (layer1-lsf) 01001 = MPEG2 (layer2, layer3-lsf) Others = Reserved	5'h0

29.5.1.4 SPDCSTAS

- Base Address: 0x0000_0000
- Address = Base Address + 900Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	–	Reserved	–
Clock accuracy	[29:28]	RW	10 = Level I, ± 50 ppm 00 = Level II, ± 1000 ppm 01 = Level III, variable pitch shifted	2'h0
Sampling frequency	[27:24]	RW	0000 = 44.1 kHz 0010 = 48 kHz 0011 = 32 kHz 1010 = 96 kHz	4'h0
Channel number	[23:20]	RW	Bit[20] is LSB	4'h0
Source number	[19:16]	RW	Bit[16] is LSB	4'h0
Category code	[15:8]	RW	Equipment type • CD player = 0000_0001 • DAT player = L000_0011 • DCC player = L100_0011 • Mini disc = L100_1001 (L: Information about generation status of the material)	8'h0
Channel status mode	[7:6]	RW	00 = Mode 0 Others = Reserved	2'h0
Emphasis	[5:3]	RW	When bit[1] = 0, 000 = 2 Audio channels without pre-emphasis 001 = 2 Audio channels with 50 us/15 us pre-emphasis When bit[1] = 1, 000 = Default state	3'h0
Copyright assertion	[2]	RW	0 = Copyright 1 = No copyright	1'h0
Audio sample word	[1]	RW	0 = Linear PCM 1 = Non-linear PCM	1'h0
Channel status block	[0]	RW	0 = Consumer format 1 = Professional format	1'h0

29.5.1.5 SPDDAT

- Base Address: 0x0000_0000
- Address = Base Address + 9010h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	–
SPDIFOUT data	[23:0]	W	PCM or stream data	24'h0

29.5.1.6 SPDCNT

- Base Address: 0x0000_0000
- Address = Base Address + 9014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	–	Reserved	–
Stream repetition count	[12:0]	W	Repetition count according to data type. This bit is valid only for stream data.	13'h0

29.5.1.7 SPDBSTAS_SHD

- Base Address: 0x0000_0000
- Address = Base Address + 9018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Burst data length bit	[31:16]	R	ES size in bits (Burst Preamble Pd) ES size: Elementary Stream size This indicates Burst-payload length	16'h0
Bit stream number	[15:13]	R	Bit_stream_number should be set to 0	3'h0
Data type dependent info	[12:8]	R	Data type dependent information	5'h0
Error flag	[7]	R	0 = Error flag indicates a valid burst_payload 1 = Error flag indicates that the burst payload may contain errors	1'h0
RSVD	[6:5]	–	Reserved	–
Compressed data type	[4:0]	R	00000 = Null Data 00001 = AC-3 00010 = Reserved 00011 = Pause 00100 = MPEG1 (layer1) 00101 = MPEG1 (layer2, 3), MPEG2-bc 00110 = MPEG2-extension 00111 = Reserved 01000 = MPEG2 (layer1-lsf) 01001 = MPEG2 (layer2, layer3-lsf) Others = Reserved	5'h0

29.5.1.8 SPDCNT_SHD

- Base Address: 0x0000_0000
- Address = Base Address + 901Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	–	Reserved	–
Stream repetition count	[12:0]	R	Repetition count according to data type This bit is valid only for stream data.	13'h0

29.5.1.9 USERBIT1

- Base Address: 0x0000_0000
- Address = Base Address + 9020h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
User data bit (sub-code Q for CD)	[31:0]	RW	USERBIT1: Q1 to Q32 User Data Bit has the Digital Audio Track information (Track number, Play Time and so on). 1176 bits of these being taken out in a row.	32'h0

29.5.1.10 USERBIT2

- Base Address: 0x0000_0000
- Address = Base Address + 9024h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
User data bit (sub-code Q for CD)	[31:0]	RW	USERBIT2: Q33 to Q64 User Data Bit has the Digital Audio Track information (Track number, Play Time and so on). 1176 bits of these being taken out in a row.	32'h0

29.5.1.11 USERBIT3

- Base Address: 0x0000_0000
- Address = Base Address + 9028h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
User data bit (sub-code Q for CD)	[31:0]	RW	USERBIT3: Q65 to Q96 User Data Bit has the Digital Audio Track information (Track number, Play Time and so on). 1176 bits of these being taken out in a row.	32'h0

29.5.1.12 USERBIT1_SHD

- Base Address: 0x0000_0000
- Address = Base Address + 902Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
User data bit	[31:0]	R	USERBIT1_SHD: Q1 to Q32 User Data Bit has the Digital Audio Track information like (Track number, Play Time etc.). 1176 bits of these being taken out in a row.	32'h0

29.5.1.13 USERBIT2_SHD

- Base Address: 0x0000_0000
- Address = Base Address + 9030h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
User data bit	[31:0]	R	USERBIT2_SHD: Q33 to Q64 User Data Bit has the Digital Audio Track information like (Track number, Play Time etc.). 1176 bits of these being taken out in a row.	32'h0

29.5.1.14 USERBIT3_SHD

- Base Address: 0x0000_0000
- Address = Base Address + 9034h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
User data bit	[31:0]	R	USERBIT3_SHD: Q65 to Q96 User Data Bit has the Digital Audio Track information like (Track number, Play Time etc.). 1176 bits of these being taken out in a row.	32'h0

29.5.1.15 VERSION_INFO

- Base Address: 0x0000_0000
- Address = Base Address + 9038h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Version information	[31:0]	R	RTL Version Information	32'hD

30 SPDIF RX

30.1 Overview

SPDIF standard defines a serial interface for transferring digital audio data between various audio equipment like DVD/HD-DVD players, AVRs and amplifiers. When audio is transferred from a DVD player to an audio amplifier over an analogue link, noise is introduced. Filtering out this noise is a difficult task. This problem is overcome when audio data is transferred over a digital link instead of an analogue link. The data can be transferred between devices without having to convert it to an analogue signal. This is the biggest advantage of SPDIF.

30.2 Features

Features of SPDIF-RX are:

- Serial, unidirectional, self-clocking interface
- Single wire-single signal interface
- Easy to work because it is polarity independent

30.3 Block Diagram

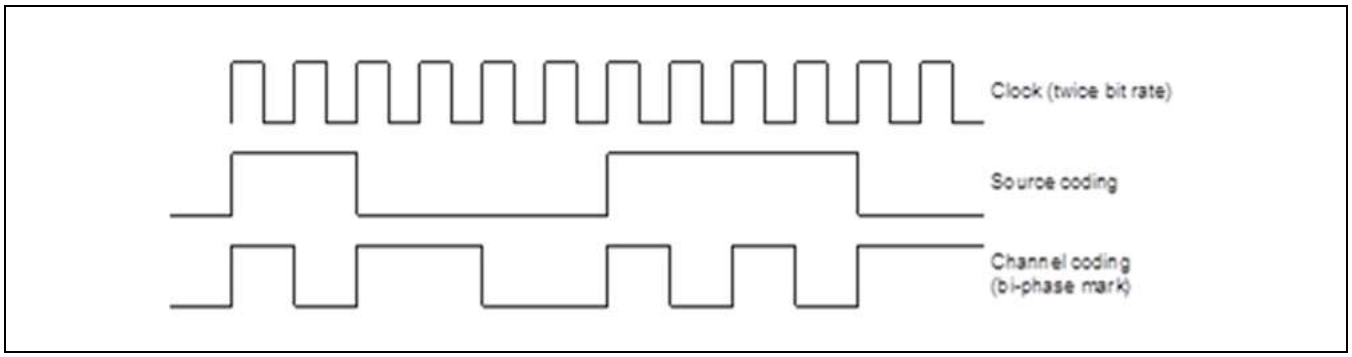


Figure 30-1 SPDIF-RX Block Diagram

30.4 Functional Description

SPDIF is a single wire serial interface and the clock is embedded within the data. The transmitted data is bi-phase mark encoded. The clock and frame sync is recovered at the receiver along with bi-phase decoded data stream. Each data bit in the stream has a time slot. The time slot begins with a transition and ends with a transition. If the transmitted data bit is "1" then additional transition is made in the middle of the time slot. Data bit "0" does not have extra transition. The shortest interval between the transitions is called the unit interval (UI).

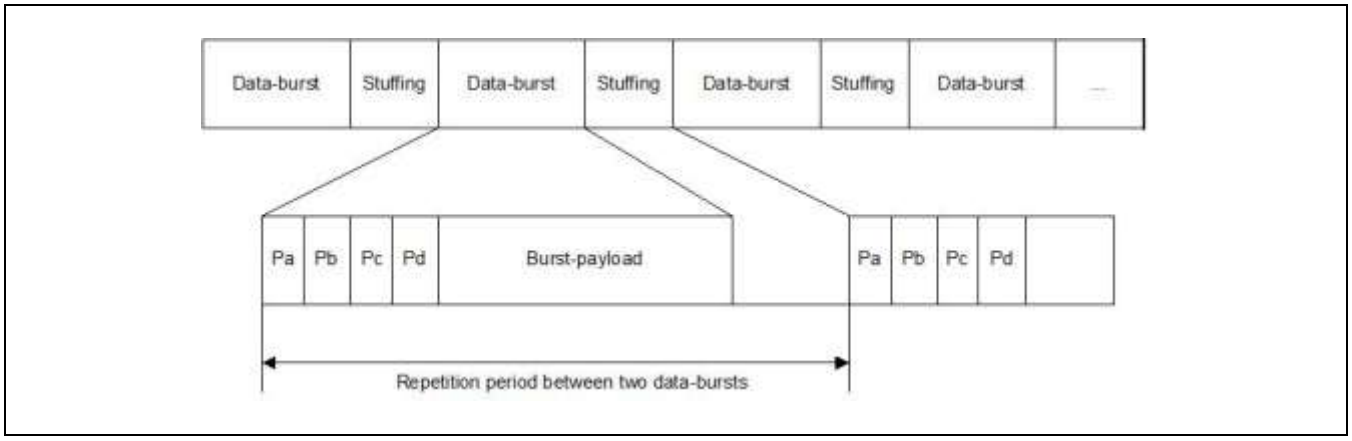


Figure 30-2 SPDIF Bi-phase Mark Encoded Stream

The least significant bit of the data is driven first. Each frame is 64 timeslots and has two sub-frames, which are 32 timeslots (*Figure 30-3*). The sub-frame starts with a preamble followed by 24 bits of data and ends with 4 bits which carry information such as user data and channel status. The first four time slots of a sub-frame, called preamble, is used to indicate sub-frame and block starts.

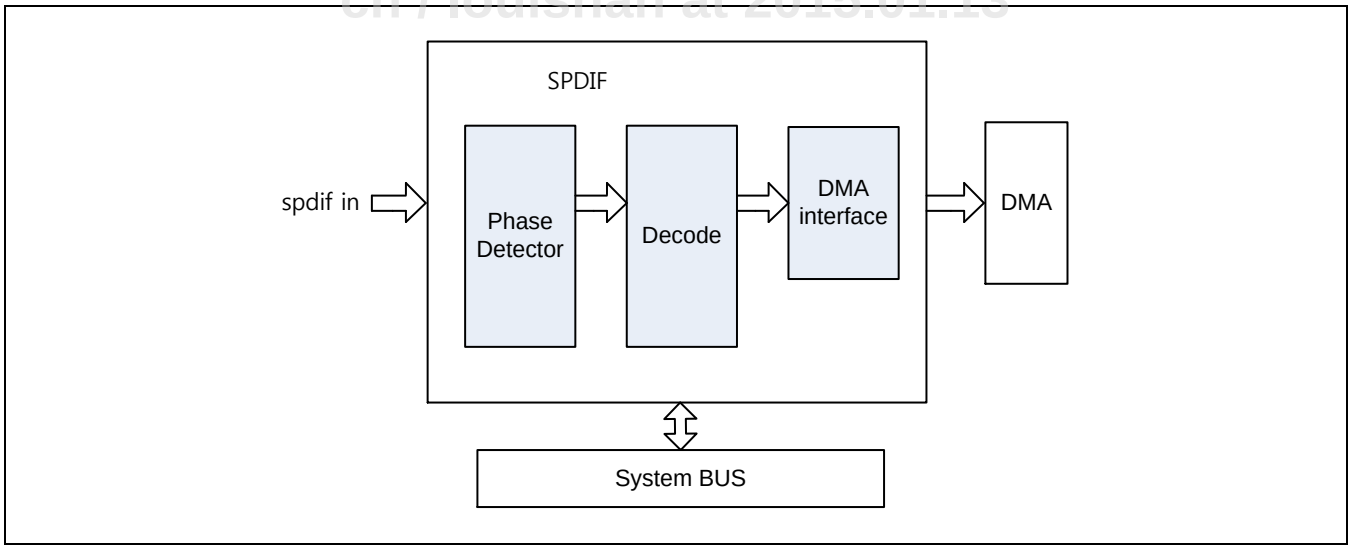


Figure 30-3 SPDIF Sub-frame Format

There are three preambles, each of which breaks the bi-phase coding rule by containing one or two pulses, which have duration of 3 UIs. This would mean that the pattern can't occur anywhere else in the stream. Each sub-frame begins with a 4-bit preamble. Start of a block is indicated by preamble "Z" and the start of sub-frame channel "A". Preamble "X" indicates the start of a channel "A" sub-frame when not at the start of a block while preamble "Y" indicates the start of a channel "B" sub-frame.

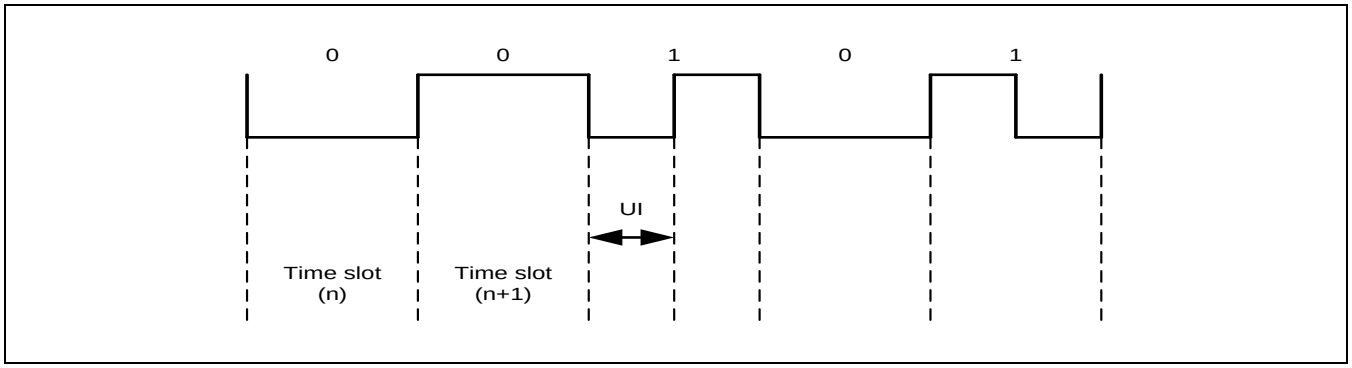


Figure 30-4 SPDIF Frame and Block Format

30.5 Register Description

30.5.1 Register Map Summary

- Base Address: 0xC005_0000

Register	Offset	Description	Reset Value
SPDIF_CTRL	A000h	SPDIF-RX Control Register	0x0000_0000
SPDIF_ENBIRQ	A004h	SPDIF-RX Interrupt Register	0x0000_0000
REGUSERA0	A008h	UserA Register[31:0]	0x0000_0000
REGUSERA1	A00Ch	UserA Register[63:32]	0x0000_0000
REGUSERA2	A010h	UserA Register[95:64]	0x0000_0000
REGUSERA3	A014h	UserA Register[127:96]	0x0000_0000
REGUSERA4	A018h	UserA Register[159:128]	0x0000_0000
REGUSERA5	A01Ch	UserA Register[191:160]	0x0000_0000
REGUSERB0	A020h	UserB Register[31:0]	0x0000_0000
REGUSERB1	A024h	UserB Register[63:32]	0x0000_0000
REGUSERB2	A028h	UserB Register[95:64]	0x0000_0000
REGUSERB3	A02Ch	UserB Register[127:96]	0x0000_0000
REGUSERB4	A030h	UserB Register[159:128]	0x0000_0000
REGUSERB5	A034h	UserB Register[191:160]	0x0000_0000
REGSTATA0	A038h	StatA Register[31:0]	0x0000_0000
REGSTATA1	A03Ch	StatA Register[63:32]	0x0000_0000
REGSTATA2	A040h	StatA Register[95:64]	0x0000_0000
REGSTATA3	A044h	StatA Register[127:96]	0x0000_0000
REGSTATA4	A048h	StatA Register[159:128]	0x0000_0000
REGSTATA5	A04Ch	StatA Register[191:160]	0x0000_0000
REGSTATB0	A050h	StatB Register[31:0]	0x0000_0000
REGSTATB1	A054h	StatB Register[63:32]	0x0000_0000
REGSTATB2	A058h	StatB Register[95:64]	0x0000_0000
REGSTATB3	A05Ch	StatB Register[127:96]	0x0000_0000
REGSTATB4	A060h	StatB Register[159:128]	0x0000_0000
REGSTATB5	A064h	StatB Register[191:160]	0x0000_0000

30.5.1.1 SPDIF_CTRL

- Base Address: 0xC005_0000
- Address = Base Address + A000h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	–
FillRegUserInv	[11]	RW	User Data filling order. 0 = Fill data from LSB to MSB 1 = Fill data from MSB to LSB	1'b0
lock	[10]	R	Lock to SPDIF input enable or disable. 0 = No-lock 1 = Lock	1'b0
Clr_FIFO	[9]	RW	DMA write/read count clear 0 = Enable 1 = Clear	1'b0
EnbPhaseDet	[8]	RW	Specifies whether the phase detector is enable or disable. 0 = Disable 1 = Enable	1'b0
Sample_OFFSET	[7:4]	RW	Specifies the valid sampling bit. 4'b0000 : 8 4'b0001 : 7 4'b0010 : 6 4'b0011 : 5 4'b0100 : 4 4'b0101 : 3 4'b0110 : 2 4'b0111 : 1 4'b1000 : 0	4'b0
EnbCapUserStat	[3]	RW	Capture User Data. When start-of-block pulse is TRUE, RegUserA, RegUserB, RegStatA, RegStatB, detected rx_data can be captured. 0 = Disable 1 = Enable	1'b0
DMA_DataOnly	[2]	RW	Specifies whether DMA transfer the data only 0 = Data & Status 1 = Data only	1'b0
DMA_Swap	[1]	RW	Specifies the order of ChannelA and ChannelB. 0 = ChannelA first 1 = ChannelB first	1'b0
DECODE_ENB	[0]	RW	Begin to decoder 0 = Disable 1 = Enable	1'b0

30.5.1.2 SPDIF_ENBIRQ

- Base Address: 0xC005_0000
- Address = Base Address + A004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	–
PendLock	[7]	RW	Interrupt pending bit of LOCK detect. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0
PendErr	[6]	RW	Interrupt pending bit of ERROR detect. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0
PendParity	[5]	RW	Interrupt pending bit of PARITY detect. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0
PendBlock	[4]	RW	Interrupt pending bit of BLOCK detect. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0
EnbIRQLock	[3]	RW	LOCK IRQ Enable 0 = Disable 1 = Enable	1'b0
EnbIRQErr	[2]	RW	ERROR IRQ Enable 0 = Disable 1 = Enable	1'b0
EnbIRQParity	[1]	RW	PARITY IRQ Enable 0 = Disable 1 = Enable	1'b0
EnbIRQBlock	[0]	RW	BLOCK IRQ Enable 0 = Disable	1'b0

Name	Bit	Type	Description	Reset Value
			1 = Enable	

30.5.1.3 REGUSERA0

- Base Address: 0xC005_0000
- Address = Base Address + A008h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserA[31:0]	[31:0]	R	Read UserA Register[31:0] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. A enable.	32'h0

30.5.1.4 REGUSERA1

- Base Address: 0xC005_0000
- Address = Base Address + A00Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserA[63:32]	[31:0]	R	Read UserA Register[63:32] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. A enable.	32'h0

30.5.1.5 REGUSERA2

- Base Address: 0xC005_0000
- Address = Base Address + A010h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserA[95:64]	[31:0]	R	Read UserA Register[95:64] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. A enable.	32'h0

30.5.1.6 REGUSERA3

- Base Address: 0xC005_0000
- Address = Base Address + A014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserA[127:96]	[31:0]	R	Read UserA Register[127:96] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. A enable.	32'h0

30.5.1.7 REGUSERA4

- Base Address: 0xC005_0000
- Address = Base Address + A018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserA[159:128]	[31:0]	R	Read UserA Register[159:128] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. A enable.	32'h0

30.5.1.8 REGUSERA5

- Base Address: 0xC005_0000
- Address = Base Address + A01Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserA[191:160]	[31:0]	R	Read UserA Register[191:160] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. A enable.	32'h0

30.5.1.9 REGUSERB0

- Base Address: 0xC005_0000
- Address = Base Address + A020h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserB[31:0]	[31:0]	R	Read UserB Register[31:0] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. B enable.	32'h0

30.5.1.10 REGUSERB1

- Base Address: 0xC005_0000
- Address = Base Address + A024h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserB[63:32]	[31:0]	R	Read UserB Register[63:32] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. B enable.	32'h0

30.5.1.11 REGUSERB2

- Base Address: 0xC005_0000
- Address = Base Address + A028h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserB[95:64]	[31:0]	R	Read UserB Register[95:64] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. B enable.	32'h0

30.5.1.12 REGUSERB3

- Base Address: 0xC005_0000
- Address = Base Address + A02Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserB[127:96]	[31:0]	R	Read UserB Register[127:96] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. B enable.	32'h0

30.5.1.13 REGUSERB4

- Base Address: 0xC005_0000
- Address = Base Address + A030h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserB[159:128]	[31:0]	R	Read UserB Register[159:128] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. B enable.	32'h0

30.5.1.14 REGUSERB5

- Base Address: 0xC005_0000
- Address = Base Address + A034h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegUserB[191:160]	[31:0]	R	Read UserB Register[191:160] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and user data ch. B enable.	32'h0

30.5.1.15 REGSTATA0

- Base Address: 0xC005_0000
- Address = Base Address + A038h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatA[31:0]	[31:0]	R	Read StatA Register[31:0] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. A enable.	32'h0

30.5.1.16 REGSTATA1

- Base Address: 0xC005_0000
- Address = Base Address + A03Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatA[63:32]	[31:0]	R	Read StatA Register[63:32] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. A enable.	32'h0

30.5.1.17 REGSTATA2

- Base Address: 0xC005_0000
- Address = Base Address + A040h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatA[95:64]	[31:0]	R	Read StatA Register[95:64] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. A enable.	32'h0

30.5.1.18 REGSTATA3

- Base Address: 0xC005_0000
- Address = Base Address + A044h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatA[127:96]	[31:0]	R	Read StatA Register[127:96] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. A enable.	32'h0

30.5.1.19 REGSTATA4

- Base Address: 0xC005_0000
- Address = Base Address + A048h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatA[159:128]	[31:0]	R	Read StatA Register[159:128] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. A enable.	32'h0

30.5.1.20 REGSTATA5

- Base Address: 0xC005_0000
- Address = Base Address + A04Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatA[191:160]	[31:0]	R	Read StatA Register[191:160] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. A enable.	32'h0

30.5.1.21 REGSTATB0

- Base Address: 0xC005_0000
- Address = Base Address + A050h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatB[31:0]	[31:0]	R	Read StatA Register[31:0] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. B enable.	32'h0

30.5.1.22 REGSTATB1

- Base Address: 0xC005_0000
- Address = Base Address + A054h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatB[63:32]	[31:0]	R	Read StatA Register[63:32] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. B enable.	32'h0

30.5.1.23 REGSTATB2

- Base Address: 0xC005_0000
- Address = Base Address + A058h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatB[95:64]	[31:0]	R	Read StatA Register[95:64] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. B enable.	32'h0

30.5.1.24 REGSTATB3

- Base Address: 0xC005_0000
- Address = Base Address + A05Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatB[127:96]	[31:0]	R	Read StatA Register[127:96] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. B enable.	32'h0

30.5.1.25 REGSTATB4

- Base Address: 0xC005_0000
- Address = Base Address + A060h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatB[159:128]	[31:0]	R	Read StatA Register[159:128] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. B enable.	32'h0

30.5.1.26 REGSTATB5

- Base Address: 0xC005_0000
- Address = Base Address + A064h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RegStatB[191:160]	[31:0]	R	Read StatA Register[191:160] when ENBCAPUSERSTAT is TRUE, start-of-block pulse is HIGH and channel status ch. B enable.	32'h0

31 PDM

31.1 Overview

Pulse-density modulation (hereafter, PDM) is a form of modulation used to represent an analog signal with digital data. In a PDM signal, specific amplitude values are not encoded into pulses of different size as they would be in PCM. Instead, it is the relative density of the pulses that corresponds to the analog signal's amplitude. The output of a 1-bit DAC is the same as the PDM encoding of the signal. The PDM in S5P4418 is a block that receives the PDM signals from an exterior digital Microphone (with 1-bit IO) and demodulates the 1-bit digital signals and returns original amplitude. The PDM supports DMA interface.

31.2 Features

- Supports receiving 2 channel audio data with 1 data pin
- 1 output clock pin
- 2 data pins (total 4 channel accepts available)
- Fixed output clock frequency
- Supports select of the timing of data capture
- Supports DMA interface
- Supports a user configuration of Coefficient. (Butterworth Low-pass Filter)

31.3 Block Diagram

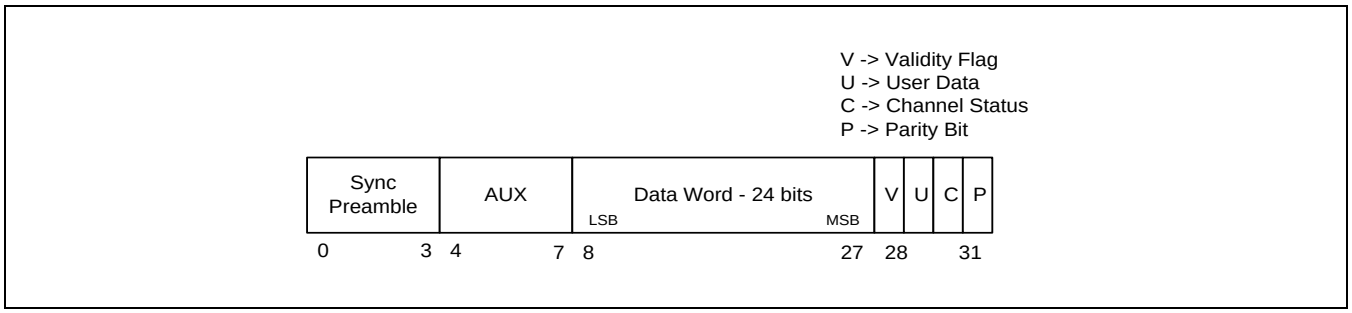


Figure 31-1 PDM Block Diagram

31.4 PDM Application Note

31.4.1 Butterworth Filter Configuration

The PDM has registers for the Butterworth Filter coefficients. Users can adjust filter coefficients and use own filter for PDM Input data.

Table 31-1 PDM Filter Configuration Example

Register Name	Bit	Symbol	Value
PDM_GAIN0	[31:16]	GAIN × (4)	276 (0x0114)
	[15:0]	GAIN × (2)	138 (0x008a)
PDM_GAIN1	[31:16]	GAIN × (-4)	–276 (0xfeec)
	[15:0]	GAIN × (-2)	–138 (0xff76)
PDM_COEFF	[31:16]	CPU_COEFF1	16194
	[15:0]	CPU_COEFF0	–8004

PDM Filter Configuration Example

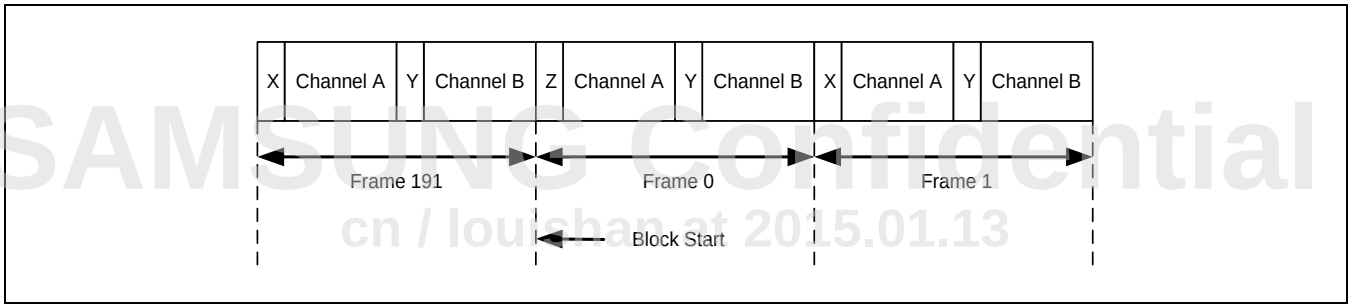


Figure 31-2 Filter Characteristics

31.5 Register Description

31.5.1 Register Map Summary

- Base Address: 0x0000_0000

Register	Offset	Description	Reset Value
PDM_CTRL	4000h	PDM Control register	0x0000_0000
PDM_gain0	4004h	PDM gain 0 register	0x0000_0000
PDM_gain1	4008h	PDM gain 1 register	0x0000_0000
PDM_coeff	400Ch	PDM coefficient register	0x0000_0000
PDM_data	4010h	PDM data register	–
PDM_ctrl1	4014h	PDM control register 1	0x0000_0000
PDM_irqctrl	4018h	PDM interrupt control register	–

31.5.1.1 PDM_CTRL

- Base Address: 0x0000_0000
- Address = Base Address + 4000h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:23]	R	Reserved	9'b0
CPU_OVERSAMPLE	[22:16]	RW	Specifies the value of over sampling.	7'b0
RSVD	[15:12]	R	Reserved	4'b0
CPU_SEL_SHIFT	[11:8]	RW	Specifies the position of shift strobe. (output clock position)	4'b0
RSVD	[7:3]	R	Reserved	5'b0
CPU_DMACHMODE	[2]	RW	Enable DMA Mode 0 = Disable 1 = Enable	1'b0
CPU_ENB	[1]	RW	Enable PDM 0 = Disable 1 = Enable	1'b0
CPU_INIT	[0]	RW	Software Reset	1'b0

31.5.1.2 PDM_gain0

- Base Address: 0x0000_0000
- Address = Base Address + 4004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
GAIN x (4)	[31:16]	RW	Specifies the value of Filter Gain x 4	16'b0
GAIN x (2)	[15:0]	RW	Specifies the value of Filter Gain x 2	16'b0

31.5.1.3 PDM_gain1

- Base Address: 0x0000_0000
- Address = Base Address + 4008h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
GAIN x (-4)	[31:16]	RW	Specifies the value of Filter Gain x (-4)	16'b0
GAIN X (-2)	[15:0]	RW	Specifies the value of Filter Gain x (-2)	16'b0

31.5.1.4 PDM_coeff

- Base Address: 0x0000_0000
- Address = Base Address + 400Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_COEFF1	[31:16]	RW	Specifies the value of Filter Coefficient 1	16'b0
CPU_COEFF0	[15:0]	RW	Specifies the value of Filter Coefficient 0	16'b0

31.5.1.5 PDM_data

- Base Address: 0x0000_0000
- Address = Base Address + 4010h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
PDM_DATA	[31:0]	R	Demodulated amplitude of input PDM signals Single Mode Dual Mode	–

31.5.1.6 PDM_ctrl1

- Base Address: 0x0000_0000
- Address = Base Address + 4014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:19]	R	Reserved	13'b0
CPU_NUM_SHIFT_CLOCK	[18:16]	RW	Specifies the number of output clock shift	3'b0
CPU_NUM_CLOCK	[15:8]	RW	Specifies the toggle position of output clock	8'b0
CPU_SAMPLE_POS	[7:0]	RW	Specifies the sampling position for PDM Input data	8'b0

31.5.1.7 PDM_irqctrl

- Base Address: 0x0000_0000
- Address = Base Address + 4018h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:7]	R	Reserved	25'b0
INTPEND	[6]	R	Interrupt Pending Bit	–
intpend_CLR	[5]	W	Write 1: Interrupt Pending Clear	–
IRQ_COUNT	[4:0]	RW	Specifies the count for PDM Interrupt. The interrupt is occurred by internal FIFO write counter. User must use this count only for PIO mode. 0 = Interrupt Disable	5'b0

32 Display Architecture

32.1 Overview

32.2 Features

- 2 Multi-layer Controller, 2 Display Controller
- 1 HDMI, 1 LVDS, 1 MIPI DSI
- Supports TFT/MPU LCD Interface, HDMI, LVDS, MIPI DSI output formats
- Supports that transmits the same image through different outputs at the same time.

32.3 Block Diagram

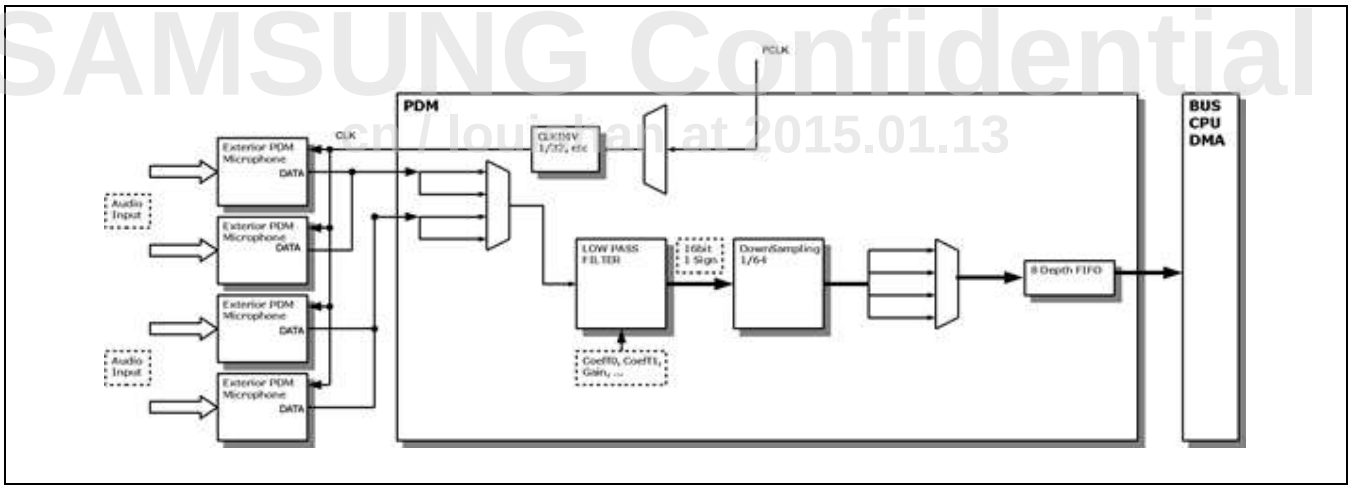


Figure 32-1 S5P4418 Display Architecture Block Diagram

32.4 TFT/MPU Interface

Things can be output through the LCD Interface as follows.

- Primary DPC (TFT Interface)
- Primary DPC (i80 MPU Interface)
- Secondary DPC (TFT Interface)

NOTE: There is no i80 MPU Interface in Secondary DPC

Users can select one of them by setting the TFT_MUXCTRL register.

32.5 Register Description

32.5.1 Register Map Summary

- Base Address: 0x0000_0000

Register	Offset	Description	Reset Value
HDMI_MUXCTRL	1004h	DISPLAYTOP HDMI MUX Control register	0x0000_0000
LVDS_MUXCTRL	100Ch	DISPLAYTOP LVDS MUX Control register	0x0000_0000
HDMI_SYNCCTRL0	1014h	DISPLAYTOP HDMI sync Control register 0	0x0000_0000
HDMI_SYNCCTRL1	1018h	DISPLAYTOP HDMI sync Control register 1	0x0000_0000
HDMI_SYNCCTRL2	101Ch	DISPLAYTOP HDMI sync Control register 2	0x0000_0000
HDMI_ SYNCCTRL3	1020h	DISPLAYTOP HDMI sync Control register 3	0x0000_0000
TFT_MUXCTRL	1024h	DISPLAYTOP TFT MUX Control register	0x0000_0000

32.5.1.1 HDMI_MUXCTRL

- Base Address: 0x0000_0000
- Address = Base Address + 1004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HDMI_MUXENB	[31]	RW	MUX Enable 0 = MUX Disable 1 = MUX Enable	1'b0
RSVD	[30:2]	RW	Reserved	29'b0
HDMI_MUXSEL	[1:0]	RW	MUX Select 0 = Primary DPC 1 = Secondary DPC 2-3 = Reserved	2'b0

32.5.1.2 LVDS_MUXCTRL

- Base Address: 0x0000_0000
- Address = Base Address + 100Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LVDS_MUXENB	[31]	RW	MUX Enable 0 = MUX Disable 1 = MUX Enable	1'b0
RSVD	[30:2]	RW	Reserved	29'b0
LVDS_MUXSEL	[1:0]	RW	MUX Select 0 = Primary DPC 1 = Secondary DPC 2-3 = Reserved	2'b0

32.5.1.3 HDMI_SYNCCTRL0

- Base Address: 0x0000_0000
- Address = Base Address + 1014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HDMI_vclk_sel	[31]	RW	Must set this value to 0 0 = HDMI PHY's pixel clock used for HDMI Operation 1 = Never set this value	1'b0
RSVD	[30:16]	RW	Reserved	15'b0
HDMI_Vsyncstart	[15:0]	RW	Specifies the start line of i_v_sync for the HDMI Link	16'b0

32.5.1.4 HDMI_SYNCCTRL1

- Base Address: 0x0000_0000
- Address = Base Address + 1018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	16'b0
HDMI_HActivestart	[15:0]	RW	Specifies the start position(h_line) of h_active for the HDMI Link	16'b0

32.5.1.5 HDMI_SYNCCTRL2

- Base Address: 0x0000_0000
- Address = Base Address + 101Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	16'b0
HDMI_HActiveend	[15:0]	RW	Specifies the end position of h_active for the HDMI Link	16'b0

32.5.1.6 HDMI_ SYNCCTRL3

- Base Address: 0x0000_0000
- Address = Base Address + 1020h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HDMI_VSYNCHSend	[31:16]	RW	Specifies the end position of i_v_sync for the HDMI Link	16'b0
HDMI_VSYNCHSStart	[15:0]	RW	Specifies the start position of i_v_sync for the HDMI Link	16'b0

32.5.1.7 TFT_MUXCTRL

- Base Address: 0x0000_0000
- Address = Base Address + 1024h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	RW	Reserved	30'b0
TFT_MUXSEL	[1:0]	RW	MUX Select 0 = Primary DPC (TFT) 1 = Primary DPC (i80 MPU) 2 = Secondary DPC (TFT) 3 = Reserved (Never use this value)	16'b0

33 Multi Layer Controller (MLC)

33.1 Overview

The user screen is composed of complex components - RGB pictures, moving pictures, etc. These individual components have unique formats and are stored in their own memory spaces. The Multi Layer Controller (hereinafter, MLC) of S5P4418 reads and compounds various screen components in terms of Hardware, to organize a desired screen and transmits the result to the Display controller.

Figure 33-1 Concept of Multi Layer Controller

33.2 Features

- Dual register-set architecture
- Two/One RGB layers and one Video layer
  (Primary Display: 2 RGB layer, Secondary Display: 1 RGB layer)
- RGB layers can be used as 3D layers.
- Various pixel formats
  - RGB layer: RGB/BGR 332, 444, 555, 565, 888 with/without Alpha
  - Video layer: 2D Separated YUV 4:4:4, 4:2:2, 4:2:0, Linear YUV 4:2:2(YUYV)
- Various blending effects between layers
  - Per-layer or Per-pixel Alpha blending, Transparency, Inverse color
- Free layer position and size in pixel units
- Hardware clipping
- Vertical flip
- Video layer priority
- Gamma Correction
- Configurable Burst Length (LOCKSIZE, RGB layer)
- Scale-up/down (Video layer only)
  - Bilinear interpolation, Nearest neighbor sampling scale-up/down
- Color control (Video layer only)
  - Brightness, Contrast, Hue, Saturation

33.3 Block Diagram

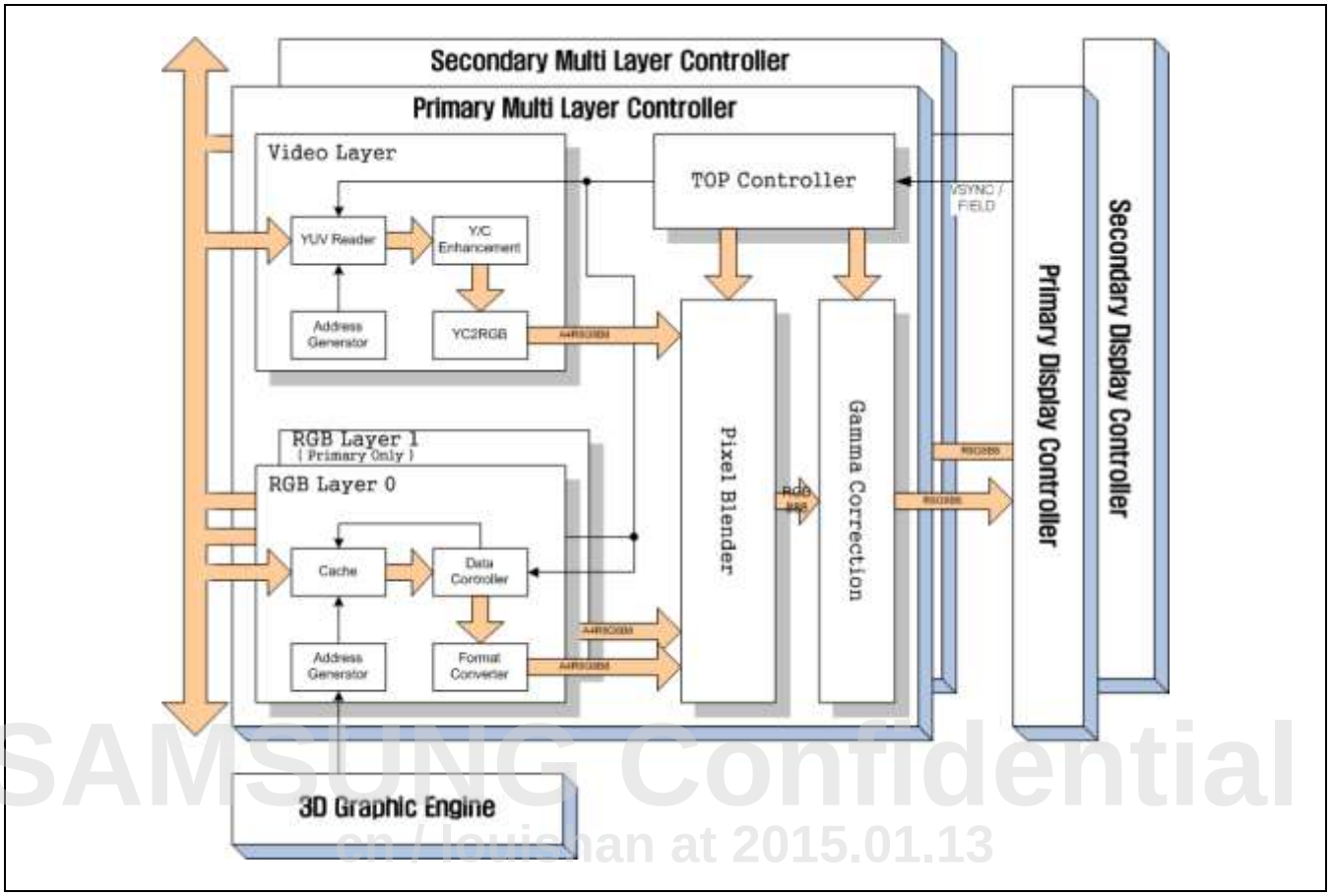


Figure 33-2 MLC Block Diagram

The MLC consists of three RGB layers and one Video layer. In the MLC, positions, pixel formats and various effects can be configured according to each layer. The Video layer supports the Scale function to display video images on various screen areas at certain sizes and various color control functions to provide optimal images.

33.4 Dual Register Set Architecture

The MLC of S5P4418 has dual register set architecture with a current working register group and a user side register group. All users can set registers via the user side register group. If the dirty flag is set as "1" after the user writes a desired setting to a register in the user side register group, the MLC copies the user side register group to the current working register group at the point when vertical sync occurs. Then the dirty flag is cleared to "0" and the user can continue to progress the next setting. In this way the changes in all registers are synchronized and applied to vertical sync so that the user can hide any abnormal screen, even if the user changes a register at any point.

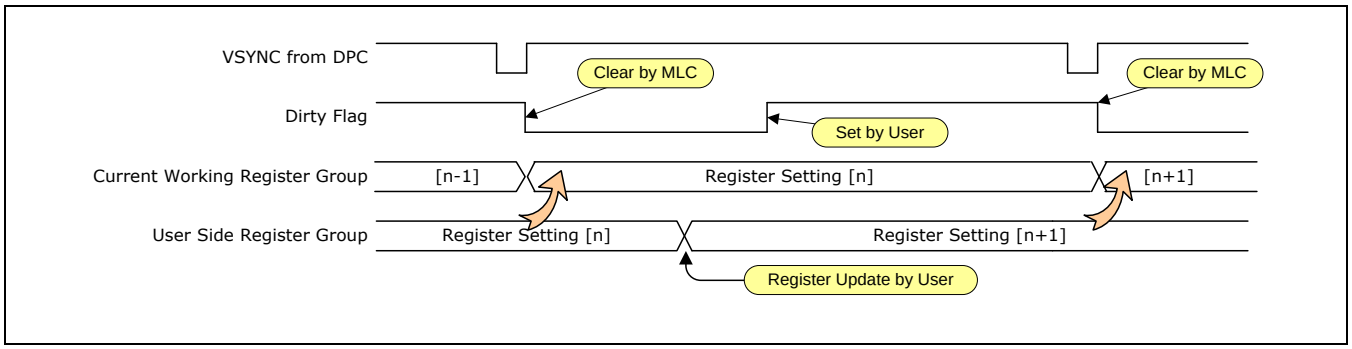


Figure 33-3 Dual Register Set Architecture

The Top controller and three layers of the MLC have separate dirty flag bits. Each dirty flag reflects the changes of the registers pertaining to the corresponding group.

Table 33-1 Dirty Flag

Dirty Flag	Numbers	Registers to be Affected
Top controller	1	MLCCONTROLT, MLCSCREENSIZE, MLCBGCOLOR
RGB layer	2	MLCLEFTRIGHTn, MLCTOPBOTTOMn, MLCCONTROLn, MLCHSTRIDEn, MLCVSTRIDEn, MLCTPCOLORn, MLCINVCOLORn, MLCADDRESSn, MLCLEFTRIGHTn_0, MLCTOPBOTTOMn_0, MLCLEFTRIGHTn_1, MLCTOPBOTTOMn_1
Video layer	1	MLCLEFTRIGHT2, MLCTOPBOTTOM2, MLCCONTROL2, MLCVSTRIDE2, MLCTPCOLOR2, MLCADDRESS2, MLCADDRESSCB, MLCADDRESSCR, MLCVSTRIDECB, MLCVSTRIDECR, MLCHSCALE, MLCVSCALE, MLCLUENH, MLCCHENH0, MLCCHENH1, MLCCHENH2, MLCCHENH3

33.5 MLC Global Parameters

This section describes how to set the global parameters of the MLC.

Table 33-2 Top Controller Registers

Function	Symbol	Bit width	Register	Brief Description
Priority	PRIORITY	2	MLCCONTROLT[9:8]	Specifies the priority of the Video layer.
Dual register set	DIRTYFLAGT	1	MLCCONTROLT[3]	Dirty Flag for MLC top controller.
Enable	MLCENB	1	MLCCONTROLT[1]	Specifies whether or not to enable MLC
Scan mode	FIEEDENB	1	MLCCONTROLT[0]	Specifies whether or not to enable Interlace mode
Screen size	SCREENWIDTH	12	MLCSCREENSIZE[11:0]	Specifies "the whole screen width - 1".
	SCREENHEIGHT	12	MLCSCREENSIZE[27:16]	Specifies "the whole screen height - 1".
Background color	BGCOLOR	24	MLCBGCOLOR[23:0]	Specifies the background color to be displayed on the screen in areas not covered by any of the layers
RGB Gamma	RGBGAMMAENB	1	MLCGAMMACONT[1]	Gamma Enable for the RGB region
Dithering	DITHERENB	1	MLCGAMMACONT[0]	Dithering Enable for the result of Gamma correction
Video Gamma	VIDEOGAMMAENB	1	MLCGAMMACONT[4]	Gamma Enable for the Video region
Alpha select	ALPAHASELECT	1	MLCGAMMACONT[5]	Allocate the Alpha blended region of RGB layer and Video layer to the Video region or the RGB region

33.5.1 Screen Size

The Screen size function enables users to specify the width and height of the whole screen to be displayed. The values of "the whole screen width - 1" and "the whole height - 1" are set to the SCREENWIDTH and SCREENHEIGHT, respectively. Since each of the SCREENWIDTH and SCREENHEIGHT has 12-bit size units, the maximum available resolution is 2048 × 2048 pixels. The screen size is determined by setting the size in frame units regardless of whether the display is progressive or interlace.

33.5.2 Priority

The MLC consists of three RGB layers and one Video layer. Among the RGB layers, Layer 0 has the highest priority and Layer 1 has the lowest priority. These priorities cannot be changed, but the priority of the Video layer can be adjusted via the PRIORITY parameter at the user's discretion.

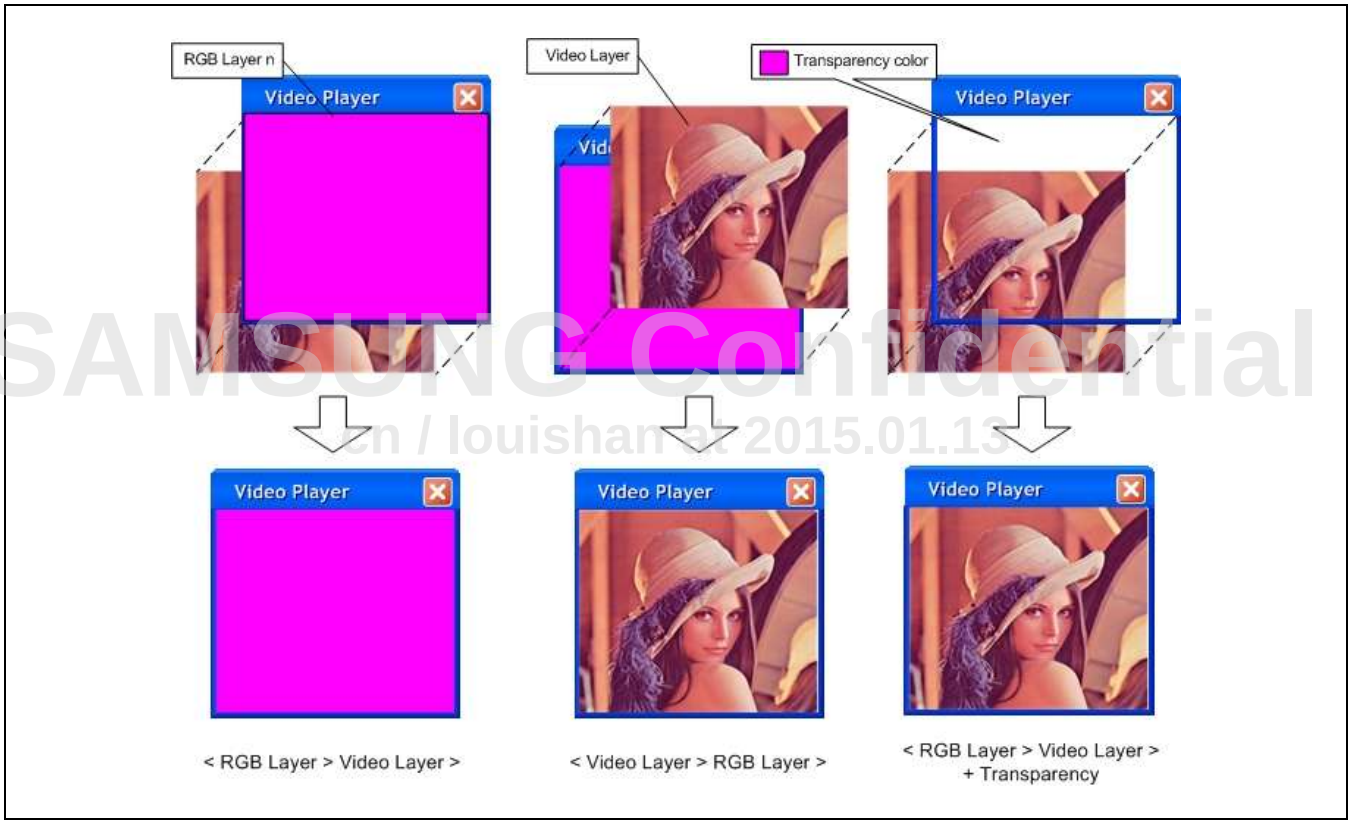


Figure 33-4 Layer Priority

33.5.3 Field Mode

The MLC of S5P4418 supports an interlace display as well as a progressive display. All registers of the MLC should be set in frame units. For the progressive display, the FIELDENB bit of the Top controller should be set as "0". For the interlace display, the FIELDENB bit of the Top controller should be set as "1". For example, a 720 × 480 progressive display and a 720 × 480 interlace display have the same settings, except for the setting of the FIELDENB bit.

33.5.4 Background Color

Each layer of the MLC can be positioned at any place on the screen. Therefore, it is possible for there to be an area not contained in any of the layers actually on the screen. The default color displayed in this area is called the background color and the background color is set to BGCOLOR. If all layers are disabled, only the background color is displayed on the screen.

The bpp of the BGCOLOR is 24 and has the following format:

Table 33-3 Background Color Format

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Background color	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

33.6 Per-layer Parameters

Table 33-4 RGB Layer Registers

Function	Symbol	Bit width	Register	Brief Description
Enable	LAYERENB	1	MLCCONTROLn[5]	Specifies whether or not to enable this layer.
Dual register set	DIRTYFLAG	1	MLCCONTROLn[4]	Dirty flag for this layer
Lock control	LOCKSIZE (1)	2	MLCCONTROLn[13:12]	Specifies lock size for memory access.
Position	LEFT	12	MLCLEFTRIGHTn[27:16]	Specifies x-coordinate of upper-left corner.
	TOP	12	MLCTOPBOTTOMn [27:16]	Specifies y-coordinate of upper-left corner.
	RIGHT	12	MLCLEFTRIGHTn [11:0]	Specifies x-coordinate of lower-right corner.
	BOTTOM	12	MLCTOPBOTTOMn[11:0]	Specifies y-coordinate of lower-right corner.
InValid Position0	INVLIDENB (1)	1	MLCLEFTRIGHTn_0[28]	InValid0 Area Enable
	LEFT (1)	12	MLCLEFTRIGHTn_0[26:16]	Specifies x-coordinate of upper-left corner.
	TOP (1)	12	MLCTOPBOTTOMn_0[26:16]	Specifies y-coordinate of upper-left corner.
	RIGHT (1)	12	MLCLEFTRIGHTn_0[10:0]	Specifies x-coordinate of lower-right corner.
	BOTTOM (1)	12	MLCTOPBOTTOMn_0[10:0]	Specifies y-coordinate of lower-right corner.
InValid Position1	INVLIDENB (1)	1	MLCLEFTRIGHTn_1[28]	InValid1 Area Enable
	LEFT (1)	12	MLCLEFTRIGHTn_1[26:16]	Specifies x-coordinate of upper-left corner.
	TOP (1)	12	MLCTOPBOTTOMn_1[26:16]	Specifies y-coordinate of upper-left corner.
	RIGHT (1)	12	MLCLEFTRIGHTn_1[10:0]	Specifies x-coordinate of lower-right corner.
	BOTTOM (1)	12	MLCTOPBOTTOMn_1[10:0]	Specifies y-coordinate of lower-right corner.
Alpha blending	BLENDENB	1	MLCCONTROLn[2]	Specifies whether or not to enable alpha blending.
	ALPHA	8	MLCTPCOLORn[31:24]	Specifies alpha blending factor.
Color inversion	INVENB (1)	1	MLCCONTROLn[1]	Specifies whether or not to enable color inversion.
	INVCOLOR (1)	24	MLCINVCOLOR[23:0]	Specifies the color to be used for color inversion.
Transparency	TPENB (1)	1	MLCCONTROLn[0]	Specifies whether or not to enable transparency.
	TPCOLOR (1)	24	MLCTPCOLORn[23:0]	Specifies the color to be used as transparency color.
Address generation	ADDRESS	32	MLCADDRESSn[31:0]	Specifies the base address of image buffer.

Function	Symbol	Bit width	Register	Brief Description
	HSTRIDE (1)	32	MLCHSTRIDEn[31:0]	Specifies the horizontal stride in bytes.
	VSTRIDE	32	MLCVSTRIDEn[31:0]	Specifies the vertical stride in bytes.
	ADDRESSCB (2)	32	MLCADDRESSCB[31:0]	Specifies the base address of Cb image buffer
	ADDRESSCR (2)	32	MLCADDRESSCR[31:0]	Specifies the base address of Cr image buffer.
	VSTRIDECB (2)	32	MLCVSTRIDECB[31:0]	Specifies the vertical stride in bytes for Cb image buffer.
	VSTRIDECR (2)	32	MLCVSTRIDECR[31:0]	Specifies the vertical stride in bytes for Cr image buffer.

NOTE:

1. Only exists in RGB layers
2. Only exists in Video layer

33.6.1 Enable

Each layer has a LAYERENB bit to enable/disable each layer of S5P4418 at a certain point. If the LAYERENB bit is set as "1", the relevant layer becomes on. If the LAYERENB bit is set as "0", the relevant layer becomes off and the other layer setting registers are not used. Since the setting of the LAYERENB bit is reflected by a dirty flag, the layer is toggled on/off in accordance with a VSYNC signal, even if the user controls the LAYERENB bit at a certain point.

33.6.2 Lock Control

Each RGB layer can adjust the data size to be read at any one time when a memory read is requested through the Lock control. The LOCKSIZE can specify 4, 8 or 16 and the unit size is 16 bytes. Therefore, if the LOCKSIZE is 4, the data size to be read at any one time is 64 bytes. For a resolution of 1280 × 1024 or higher, it is recommended to set the LOCKSIZE as 16.

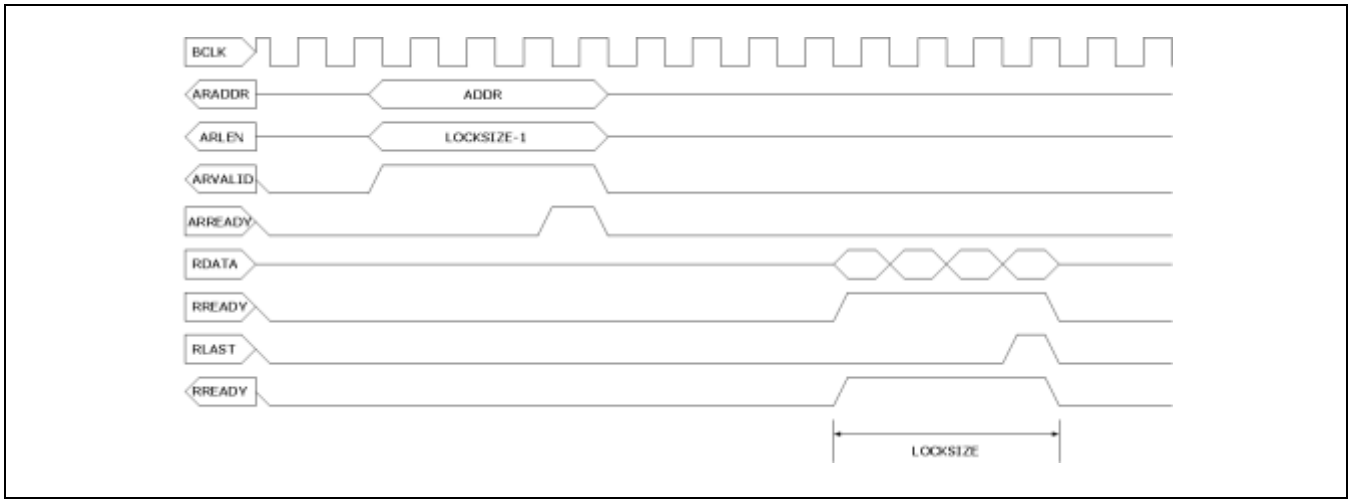


Figure 33-5 Lock Timing

33.6.3 Position

The Position function enables users to specify the top-left (LEFT*and*TOP) and the bottom-right (RIGHT and BOTTOM) coordinates. Each coordinate can be positioned at any point within the range from –2048 to 2047, but only the layer contained in the area from (0, 0) and (ScreenWidth – 1, ScreenHeight – 1) is displayed on the actual screen. The MLC of S5P4418 supports H/W clipping for any area outside of the screen area, so users do not need to carry out additional clipping processing. In addition, the MLC does not read the data in the clipped area and the area hidden by upper layer from memory for effective use of the memory bandwidth.

RGB Layer could appoint three invisible areas without using certain color. Appointed area is not read from Memory.

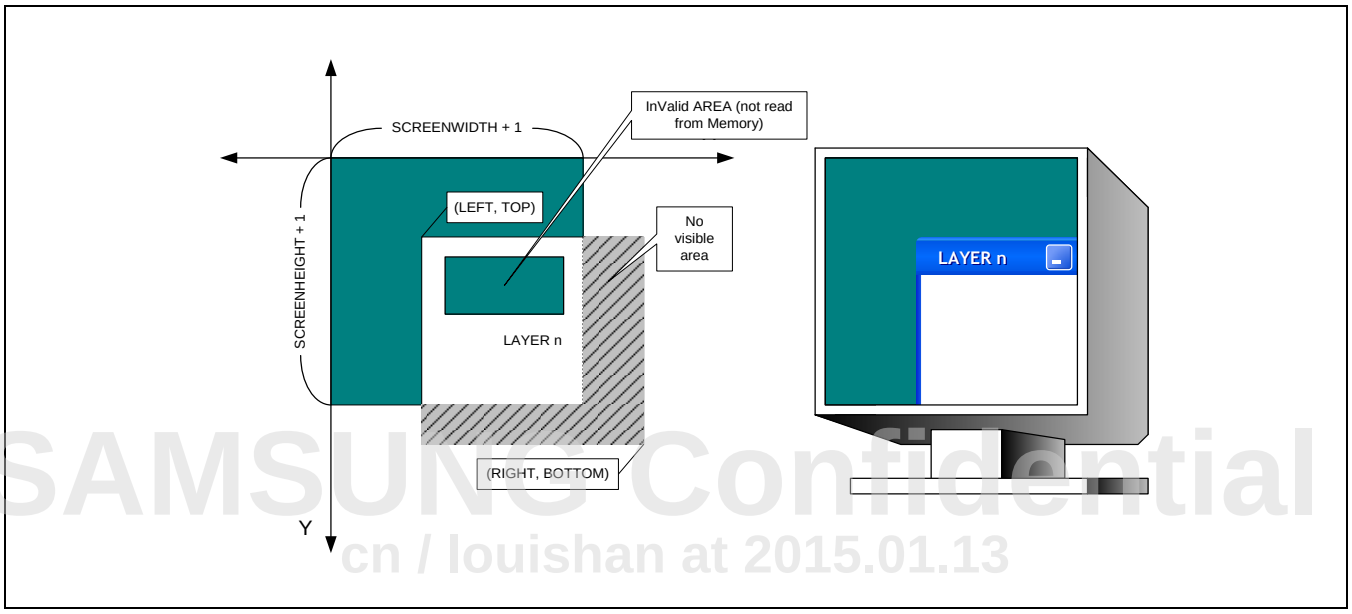


Figure 33-6 Layer Position

33.6.4 Pixel Format

33.6.4.1 RGB Layer Format

Each RGB layer supports various formats and the formats are listed in *Figure 33-5*.

- R: Red, G: Green, B: Blue, A: Alpha, X: Not used

Table 33-5 RGB Layer Format

Pixel format	FORMAT[15:0]	Bpp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5G6B5	4432h	16	R1[4:0]					G1[5:0]						B1[4:0]					R0[4:0]					G0[5:0]					B0[4:0]				
B5G6R5	C432h	16	B1[4:0]					G1[5:0]						R1[4:0]					B0[4:0]					G0[5:0]					R0[4:0]				
X1R5G5B5	4342h	16		R1[4:0]				G1[4:0]						B1[4:0]						R0[4:0]				G0[4:0]					B0[4:0]				
X1B5G5R5	C342h	16		B1[4:0]				G1[4:0]						R1[4:0]						B0[4:0]				G0[4:0]					R0[4:0]				
X4R4G4B4	4211h	16				R1[3:0]				G1[3:0]				B1[3:0]								R0[3:0]				G0[3:0]				B0[3:0]			
X4B4G4R4	C211h	16				B1[3:0]				G1[3:0]				R1[3:0]								B0[3:0]				G0[3:0]				R0[3:0]			
X8R3G3B2	4120h	16									R1[2:0]			G1[2:0]			B1[1:0]										R0[2:0]			G0[2:0]			B0[1:0]
X8B3G3R2	C120h	16									B1[2:0]			G1[2:0]			R1[1:0]										B0[2:0]			G0[2:0]			R0[1:0]
A1R5G5B5	3342h	16	A1		R1[4:0]				G1[4:0]					B1[4:0]					A0		R0[4:0]				G0[4:0]					B0[4 : 0]				
A1B5G5R5	B342h	16	A1		B1[4:0]				G1[4:0]					R1[4:0]					A0		B0[4:0]				G0[4:0]					R0[4 : 0]				
A4R4G4B4	2211h	16		A1[3:0]				R1[3:0]				G1[3:0]				B1[3:0]				A0[3:0]				R0[3:0]				G0[3:0]				B0[3:0]		
A4B4G4R4	A211h	16		A1[3:0]				B1[3:0]				G1[3:0]				R1[3:0]				A0[3:0]				B0[3:0]				G0[3:0]				R0[3:0]		
A8R3G3B2	1120h	16						A1[7:0]							R1[2:0]			G1[2:0]			B1[1:0]							A0[7:0]						
A8B3G3R2	9120h	16						A1[7:0]							B1[2:0]			G1[2:0]			R1[1:0]							A0[7:0]						
R8G8B8	4653h1)	24						B1[7:0]																					R0[7:0]					
B8G8R8	C653h1)	24						R1[7:0]																					B0[7:0]					
X8R8G	4653h1)	32																											R[7:0]					

Pixel format	FORMAT[15:0]	Bpp	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8B8																																		
X8B8G8R8	C653h1)	32									B[7:0]								G[7:0]								R[7:0]							
A8R8G8B8	0653h	32	A[7:0]								R[7:0]								G[7:0]								B[7:0]							
A8B8G8R8	8653h	32	A[7:0]								B[7:0]								G[7:0]								R[7:0]							

NOTE: The format settings for R8G8B8 & X8R8G8B8 and B8G8R8 & X8B8G8R8 are the same. However, the HSTRIDE*s for R8G8B8 and B8G8R8 should be set as "3" because they are in 24 bpp modes, while the HSTRIDE*s for X8R8G8B8 and X8B8G8R8 should be set as "4".

The above formats are converted into A8R8G8B8 and are managed in each RGB layer. Each color component is converted into 8-bit size. The color components with the size smaller than 8-bit are extended to 8-bit size from the highest bit repeatedly. For example, the color with 5-bit size is converted to {[4:0], [4:2]} and the color with 3-bit size is converted to {[2:0], [2:0], [2:1]}. Each layer compares the color component internally extended with TPCOLOR or INVCOLOR. Therefore, a user should set the color that each color format is extended in R8G8B8 in TPCOLOR and INVCOLOR.

33.6.4.2 Video Layer Format

The Video layer manages YUV data and supports the linear YUV format and the 2D block addressing separated YUV format.

Table 33-6 Video Layer Format

FORMAT[1:0]	Pack mode	Type	Y:UV	Addressing mode
0	Separate Y/U/V	YUV	4:2:0	2D Block
1	Separate Y/U/V	YUV	4:2:2	2D Block
2	Non-separate	YUV	4:2:2	Linear
3	Separate Y/U/V	YUV	4:4:4	2D Block
4	Separate Y/UV	YUV	4:2:2	2D Block
5	Separate Y/UV	YUV	4:2:0	2D Block

The MLC of S5P4418 uses the A4R8G8B8 format internally. Therefore, the Video layer also reads YUV data from the memory and converts into RGB data internally. The formulas with which the Video layer converts YUV data into RGB data are as follows:

The formula for YCbCr to RGB conversion

R = Y + (1.4020 × Cr)
G = Y - (0.34414 × Cb) + (0.71414 × Cr)
B = Y + (1.7720 × Cb)

- Linear YUV 422 Format

  The video layer supports the YUYV format as a linear YUV format whose Y data (luminance data) exists at every pixel, but Cb and Cr (chrominance) data exist separately over two pixels. Therefore two pixels share the same Cb/Cb data. Hence the Video layer has 2-pixel data per 32-bit and manages it in 2-pixel units.

Table 33-7 YUYV Format

Pixel Format	FORMAT [2:0]	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
YUYV	2	Cr[7:0]								Y1[7:0]								Cb[7:0]								Y0[7:0]							

- 2D Block Addressing Separated Y/U/V Format

  In the 2D block addressing separated Y/U/V format, each of Y, U and V exists at separate memory spaces. In addition, the format is divided into 444, 422 and 420 in proportion to U and V for Y. The 2D block addressing separated YUV format is the 2D block addressing format, and each component has a size of 64 × 32 and linearity in block units. These features provide S5P4418s unique memory format, to enhance the effectiveness of memory access when S5P4418 manages data in macro block units through an algorithm to compress/decompress images like MPEG files.

According to each format, Y, U and V correspond to 2 × 2 pixels as follows:

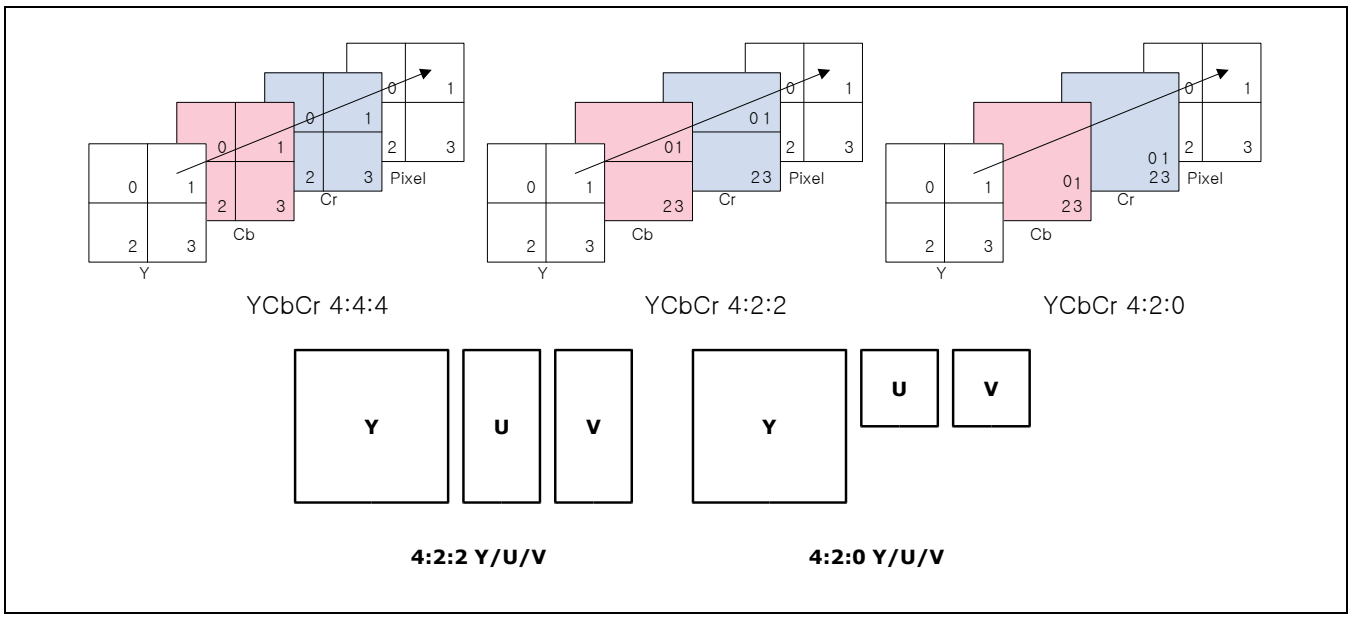


Figure 33-7 Separated YUV Format

In the memory, each of Y, U and V exists at separated memory space.

33.6.4.3 Layer Blending

MLC consists of three RGB layers and one Video layer. Each RGB layer supports Transparency, Color Inversion and Alpha Blending functions but the Video layer only supports Alpha Blending functions. The Color Inversion and the Alpha Blending functions are only applied to between layers and not to background.

The Transparency function enables users to specify a particular color and handle the color as a transparent color. Therefore, an area filled with a transparent color shows through the lower layer and shows the layer as it is. Like the Transparency function, the Color Inversion function shows through the lower layer and shows the layer as it is, but the function is different in that it inverts and projects the layer's color. The Transparency and Color Inversion functions are useful for the implementation of the Cursor layer as shown in the figure below:

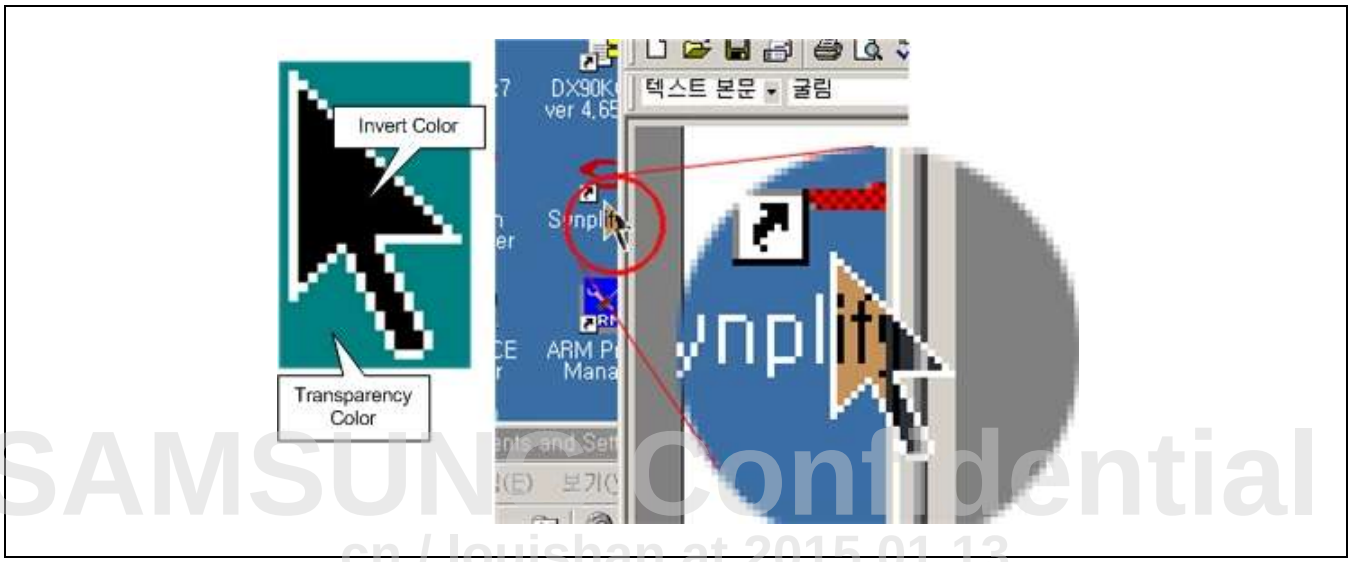


Figure 33-8 Transparency & Color Inversion

The Transparency and the Color Inversion effects are applied by setting each of the TPENB and the INVENB bits of an RGB Layer as "1". Both TPCOLOR and INVCOLOR have R8G8B8 formats.

Table 33-8 TPCOLOR & INVCOLOR Format

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPCOLOR / INVCOLOR	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

The Alpha Blending function enables users to adjust the transparency of a desired layer. The Alpha level is adjusted by ALPHA[7:0] and can be specified in the range between 0 and 255. If the Alpha level is 255, it means it is fully opaque. If the level is 0, it indicates full transparency. In addition, each RGB layer can use a pixel format including Alpha and is applied in Alpha per pixel units. In the Per-layer alpha or the Per-pixel Alpha formats, the Alpha Blending effect can only be applied by setting the BLENDENB bit as "1".

Only one layer can use the alpha blending function at the same time, and when the alpha blending function of one layer is enabled, the alpha blending function of the other layers must be disabled.

All layers use the A8R8G8B8 format internally and the formula for Alpha Blending is as follows:

The formula for Alpha blending function

If alpha is 0 then α is 0, else α is alpha + 1
Result color = this layer color α / 256 + lower layer color (256 - α) / 256
In the A4 format, α = alpha × 16 + alpha (0 ≤ alpha < 16)

Figure 33-9 Alpha Blending

33.6.5 Address Generation

33.6.5.1 RGB Layer Address Generation

The Address generation function enables users to specify the address and stride of the memory where images are stored.

Stride is divided into horizontal stride and vertical stride. The stride is the unit for increasing an address. The horizontal stride (HSTRIDE) is the value to be added to an address whenever its x-coordinate increases, while the vertical stride (VSTRIDE) is the value to be added to the address whenever its y-coordinate increases. In general, the horizontal stride is the number of the bytes per pixel and the vertical stride is the value that is the number of bytes per pixel multiplied by an image width. The vertical stride has 2's complement format. Thus a vertical flip function can be implemented by specifying the vertical stride as negative number.

The Image address (ADDRESS) usually specifies an address on the top left corner of the image. If the vertical stride for the vertical flip function has a negative number, the ADDRESS should specify an address on the bottom left corner of the image.

Table 33-9 RGB Layer Address & Flip

Vertical Flip	Vertical Stride	Base Address
Off	0	Address on the top left corner of the image
On	< 0	Address on the bottom left corner of the image

33.6.5.2 Video Layer Address Generation

In the Video layer, the horizontal stride is not separately specified and is fixed internally. In addition, the vertical stride should always be a positive number. Since the vertical stride is always positive number, the vertical flip function is not supported.

- Linear YUV 422 format (YUYV)

  In the linear YUV 422 format, an address can only be specified by setting its base address and vertical stride. The Base address (ADDRESS) specifies the base address in the YUYV image buffer and the vertical stride (VSTRIDE) specifies the increment of the address in proportion to the increase of the y-coordinate. The vertical stride should be a positive number.

- 2D block addressing separated YUV format

  In the separated format, each Y, U and V is stored in different addresses of the memory. Thus the address for the Y component is specified by the ADDRESS3 and the VSTRIDE3 registers and the address for the U (Cb) and V (Cr) components is separately specified by the ADDRESSCB & the VSTRIDECB registers and the ADDRESSCR& the VSTRIDECR registers. Since S5P4418 uses segments with 4096 × 4096 pixel sizes in the 2D block addressing format, the vertical stride should be specified as 4096. In addition, the ADDRESS3/CB/CR registers set the separate format for segment addresses and not for normal linear addresses. The segment addressing format is listed in *Table 33-10*.

Table 33-10 Segment Addressing Format

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address	0	0	1	Index of Segment					Y coordinate in segment [11:0]												X coordinate in segment [11:0]											

The display array area on the memory map should be specified as a setting Address[31:29] of 4'b001. In addition, the Memory controller should be enabled to use the display array area. See section "5.3.2. Display Array Area" for more detail.

33.6.6 Video Layer Specific Parameters

The Video layer provides the Scale and Color Control functions additionally.

Table 33-11 Video Layer Specific Parameters

Function	Symbol	Bit width	Register	Brief description
Scale	VFILTERENB	1	MLCVSCALE[28]	Specifies whether or not to vertical scale enable bilinear filter.(This is only applicable to the Y component)
	VFILTERENB_C	1	MLCVSCALE[29]	Specifies whether or not to vertical scale enable bilinear filter. (This is only applicable to the Cb, Cr components)
	HFILTERENB	1	MLCHSCALE[28]	Specifies whether or not to horizontal scale enable bilinear filter. (This is only applicable to the Y component)
	HFILTERENB_C	1	MLCHSCALE[29]	Specifies whether or not to horizontal scale enable bilinear filter. (This is only applicable to the Cb, Cr components)
	HSCALE	23	MLCHSCALE[22:0]	Specifies the horizontal scale ratio.
	VSCALE	23	MLCVSCALE[22:0]	Specifies the vertical scale ratio.
Color control	BRIGHTNESS	8	MLCLUENH[15:8]	Specifies the brightness value.
	CONTRAST	3	MLCLUENH[2:0]	Specifies the contrast value.
	HUECBnA	8	MLCCHENHn[7:0]	Specifies the cosine value for Cb component.
	HUECBnB	8	MLCCHENHn[15:8]	Specifies the sine value for Cb component.
	HUECRnA	8	MLCCHENHn[23:16]	Specifies the sine value for Cr component.
	HUECRnB	8	MLCCHENHn[31:24]	Specifies the cosine value for Cr component.

33.6.7 Scale Function

The scale-up and the scale-down of the Video layer are determined by the HSCALE and VSCALE parameters. Each parameter finds and sets the ratio between an input image size and an output image size. The setting formulae for the HSCALE and VSCALE parameters are as follows:

The formula for HSCALE and VSCALE
In case of the enlargement by using a Bilinear filter:

HSCALE = (source width-1) * (1<<11) / (destination width-1)
VSCALE = (source height-1) * (1<<11) / (destination height-1)

,else

HSCALE = source width * (1<<11) / destination width
VSCALE = source height * (1<<11) / destination height

Video Layer supports bilinear filtered scaling up and down. Nearest neighbor scaling is also supported. Filter enable signals are separately allocated for Y and C (Cb, Cr) components in case of scaling up/down (H/VFILTERENB, H/VFILTERENB_C)

When bilinear scaling up and down is used, H/VFILTERENB and H/VFILTERENB_C should be set to "1" for bilinear filtered scaling. When nearest neighbor scaling down is used, H/VFILTERENB and H/VFILTERENB_C* should be set to "0". The difference in images produced by the bilinear filter method is as shown in *Figure 33-10*.

Figure 33-10 Bilinear Filter

33.6.7.1 Color Control

The Video layer supports the Color Control function for output images. A user can adjust Brightness, Contrast, Hue and Saturation to compensate video data colors.

33.6.7.2 Luminance Enhancement

The Video layer can compensate luminance data by adjusting Brightness and Contrast.

The Brightness consists of 256 levels and is set by the BRIGHTNESS parameter. The BRIGHTNESS parameter has a 2's complement value and can be set between the -128 level and the +127 level. *Figure 33-11* shows the image change depending on the Brightness change.

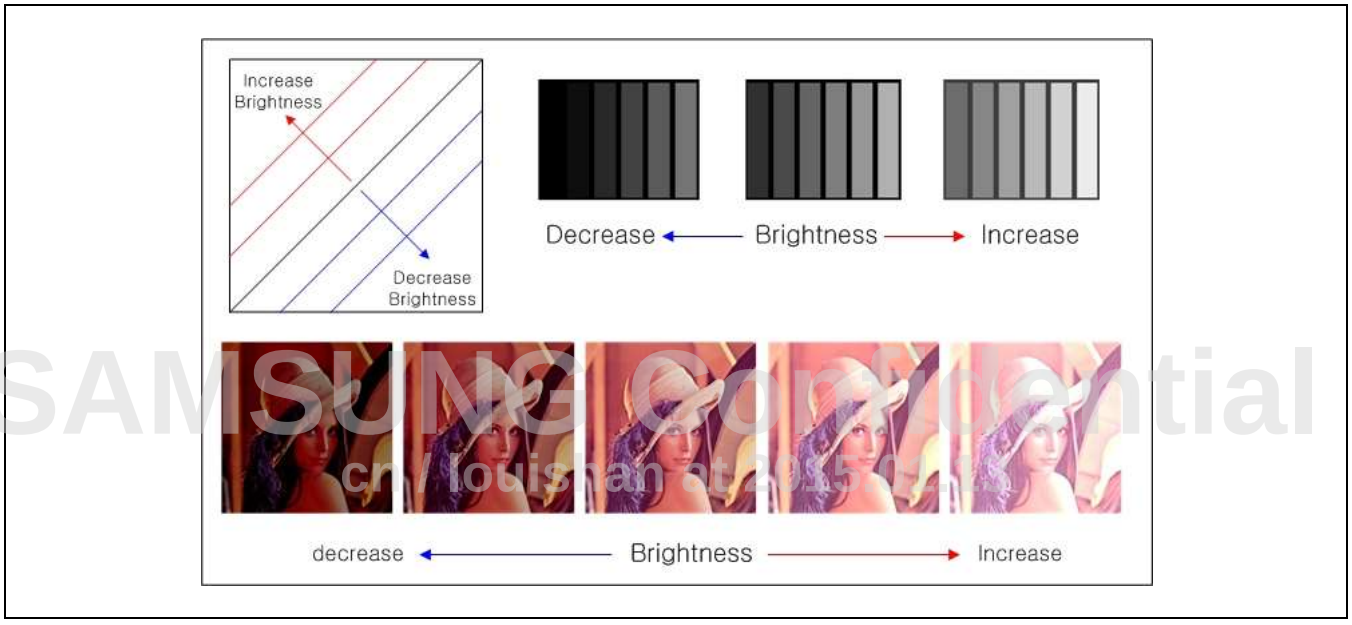


Figure 33-11 Brightness

The Contrast consists of 8 levels and is set by the CONTRAST parameter. The Video layer can adjust the contrast from 1.0 to 1.875 in increments of 0.125, but cannot reduce the contrast of the original image. *Table 33-12* lists the contrast values corresponding to the CONTRAST parameters.

Table 33-12 CONTRAST Parameter

CONTRAST	0	1	2	3	4	5	6	7
Contrast value	1.0	1.125	1.25	1.375	1.5	1.625	1.75	1.875

Figure 33-12 shows the image change depending on the contrast change. The following figure is originally intended to explain better about the contrast function as well as to show the effect of contrast reduction. Actually, the Video layer can increase the contrast, but not reduce it.

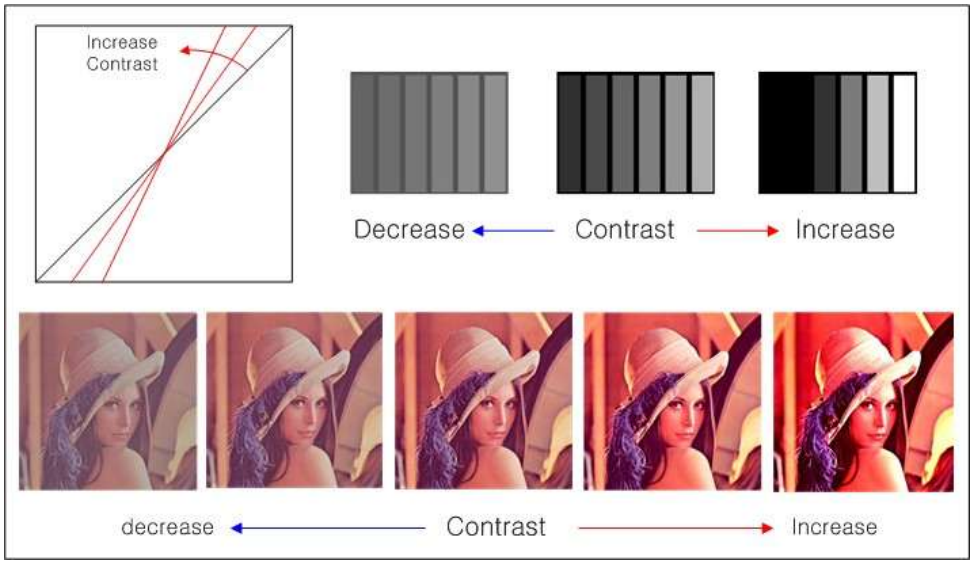


Figure 33-12 Contrast

33.6.7.3 Chrominance Enhancement

The Video layer can compensate Chrominance data by adjusting Hue and Saturation.

The Hue is adjusted by the following formulae:

(B-Y)' = (B-Y) Cos(θ) - (R-Y) Sin(θ)
(R-Y)' = (B-Y) Sin(θ) + (R-Y) Cos(θ)

The Saturation can be adjusted by multiplying a gain value by the above result value.

The Video layer can adjust the Hue and Saturation differently in each quadrant and has HUECBnA/B*and *HUECRnA/B parameters for each quadrant. Each parameter has the [S.1.6] format and is applied as follows:

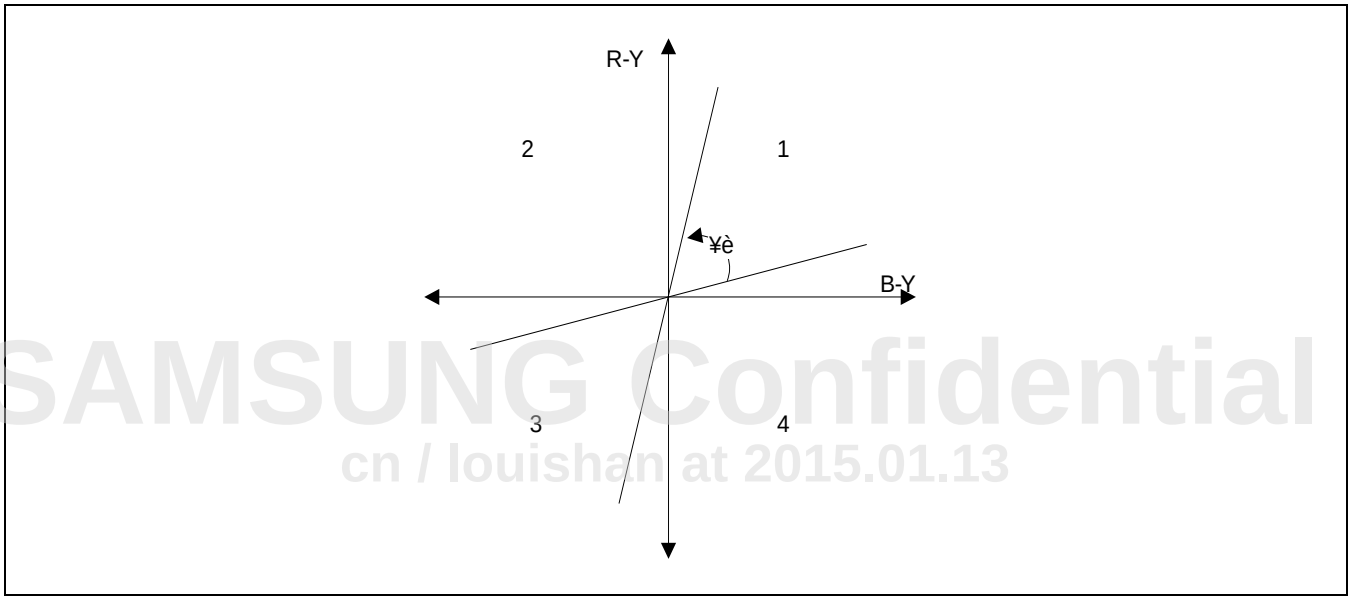


Figure 33-13 The Basic concept of Hue and Saturation Control

1. 1st quadrant: (B-Y) > 0 and (R-Y) > 0
(B-Y)' = (B-Y) HUECB1A + (R-Y) HUECB1B
(R-Y)' = (B-Y) HUECR1A + (R-Y) HUECR1B

2. 2nd quadrant: (B-Y) < 0 and (R-Y) > 0
(B-Y)' = (B-Y) HUECB2A + (R-Y) HUECB2B
(R-Y)' = (B-Y) HUECR2A + (R-Y) HUECR2B

3. 3rd quadrant: (B-Y) < 0 and (R-Y) < 0
(B-Y)' = (B-Y) HUECB3A + (R-Y) HUECB3B
(R-Y)' = (B-Y) HUECR3A + (R-Y) HUECR3B

4. 4th quadrant: (B-Y) < 0 and (R-Y) < 0
(B-Y)' = (B-Y) HUECB4A + (R-Y) HUECB4B
(R-Y)' = (B-Y) HUECR4A + (R-Y) HUECR4B

Therefore, each parameter can be calculated by using the following formulas:

The formula for Hue and Saturation parameters:

HUECBnA = cos(θ) * 64 * gain, HUECBnB = - sin(θ) * 64 * gain
HUECRnA = sin(θ) * 64 * gain, HUECRnB = cos(θ) * 64 * gain
, where θ is for hue and gain is for saturation from -2 to 1.99999X.

Figure 33-14 the image change depending on the changes to Hue and Saturation.

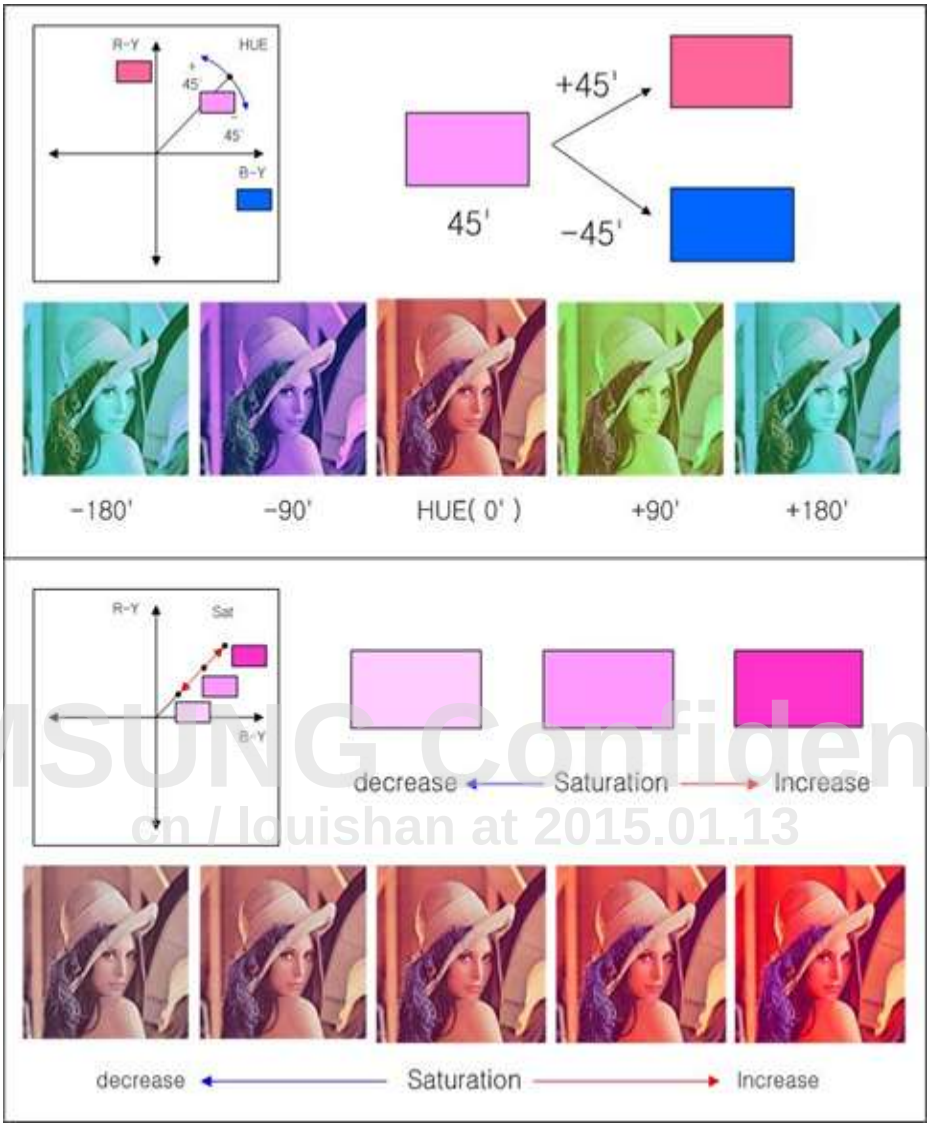


Figure 33-14 Hue and Saturation

33.6.8 Gamma Correction

MLC has three Gamma Table (256 × 10-bit) for Red, Green, and Blue colors. Gamma[9:0] consists of Gamma[9:2], which are the integers(0 to 255), and Gamma[1:0], which are decimals (0.0, 0.5, 0.25, 0.75). And, R10, G10, B10, as the result of Gamma correction, are transformed into R8, G8, B8, which then can be used as input pixel for Display block , and it is possible to apply dithering while 10-bit results is being transformed into 8-bit.

Gamma correction can choose any Gamma region according to 3 different modes (total layer, RGB layer, Video layer), and also can designate the Alpha-blended regions of Video layer and RGB layer as the region of RGB layer or Video layer.

Gamma Table R = (255 * (R / 255) ^ γ) << 2
Gamma Table G = (255 * (G / 255) ^ γ) << 2
Gamma Table B = (255 * (B / 255) ^ γ) << 2

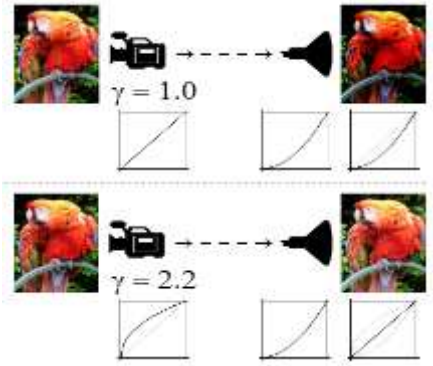


Figure 33-15 Gamma Correction

Register Set in case of Gamma correction

Example:

R,G,B Gamma Table Power On (MLCGAMMACONT Register R/G/BGAMMATABLE_PWD bit = "1")

Gamma Table SLEEP Mode Disable (MLCGAMMACONT Register R/G/BGAMMATABLE_SLD bit = "1")

Write the value of Gamma Table
(Table address: MLCR/G/BGAMMATABLEWRITE[31:24], table data: MLCR/G/BGAMMATABLEWRITE[9:0])

Gamma enable(Refer to MLCGAMMACONT Register)

MLC Enable

33.7 Clock Generation

The MLC operates by using the PCLK and the BCLK. The PCLK is used when the CPU accesses the registers of the MLC. The BCLK is used as an internal clock or when the MLC accesses the memory. The MLC provides various operation modes for the PCLK and the BCLK. Therefore, users can adjust the clock for the MLC by setting the PCLKMODE and the BCLKMODE parameters according to their purpose. Users must set Always Mode for using the MLC. (BCLK and PCLK both)

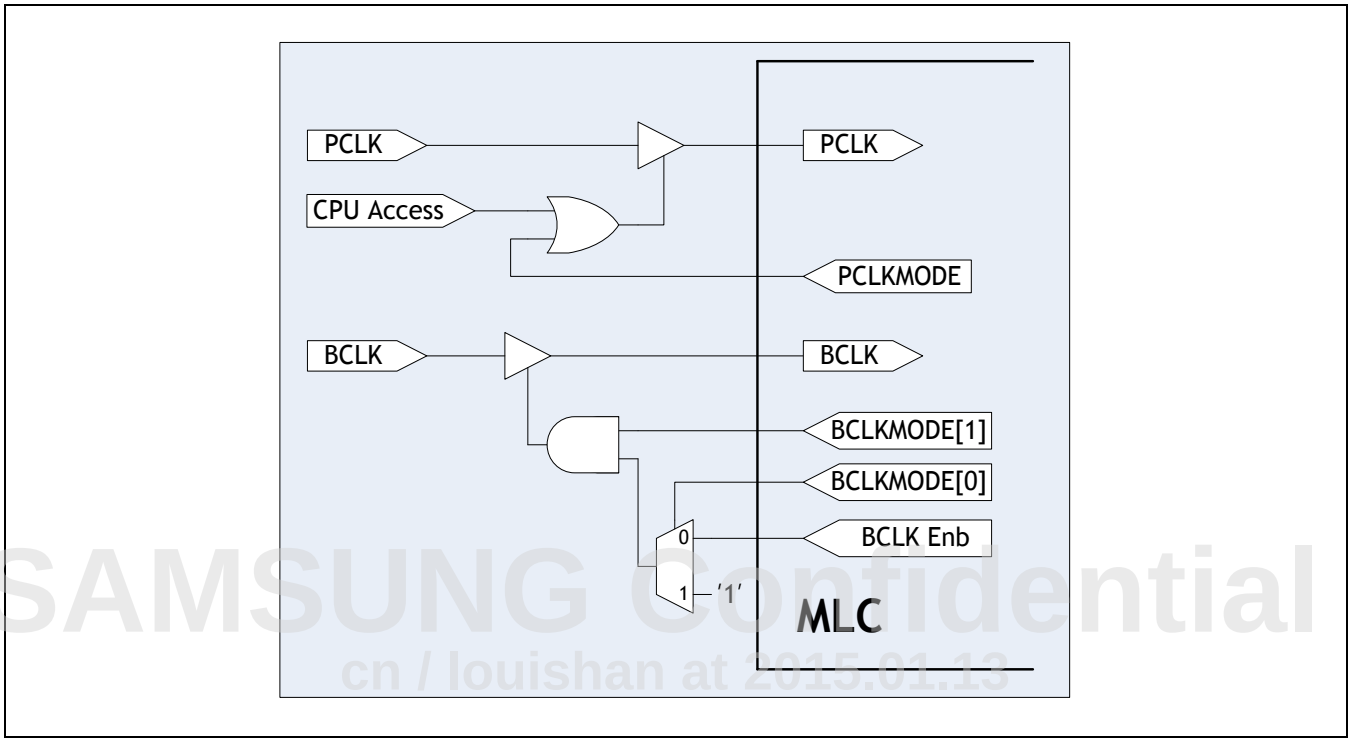


Figure 33-16 Clock Generation

Table 33-13 PCLK Mode

PCLKMODE	Brief Description
0	Always disabled
1	Always enabled.

Table 33-14 BCLK Mode

BLCKMODE		Brief Description
[1]	[0]	
0	0	Always disabled.
0	1	
1	0	
1	1	Always enabled.

33.8 Register Description

33.8.1 Register Map Summary

- Base Address: 0xC010_2000

Register	Offset	Description	Reset Value
MLCCONTROLT	0x000h (Primary), 0x400h (Secondary)	MLC TOP control Register	0x0000_0100
MLCSCREENSIZE	0x004h/0x404h	MLC screen size Register	0x0000_0000
MLCBGCOLOR	0x008h/0x408h	MLC BACKGROUND COLOR Register	0x0000_0000
MLCLEFTRIGHT0	0x00Ch/0x40Ch	MLC RGB Layer 0 LEFT right Register	0x0000_0000
MLCTOPBOTTOM0	0x010h/0x410h	MLC RGB Layer 0 top bottom Register	0x0000_0000
MLCLEFTRIGHT0_0	0x014h/0x414h	MLC RGB Layer 0 INVALID AREA 0 LEFT right Register	0x0000_0000
MLCTOPBOTTOM0_0	0x018h/0x418h	MLC RGB Layer 0 INVALID AREA 0 bottom top Register	0x0000_0000
MLCLEFTRIGHT0_1	0x01Ch/0x41Ch	MLC RGB Layer 0 INVALID AREA 1 LEFT right Register	0x0000_0000
MLCTOPBOTTOM0_1	0x020h/0x420h	MLC RGB Layer 0 INVALID AREA 1 bottom top Register	0x0000_0000
MLCCONTROL0	0x024h/0x424h	MLC RGB Layer 0 control Register	0x0000_0000
MLCHSTRIDE0	0x028h/0x428h	MLC RGB Layer 0 HORIZONTAL stride Register	0x0000_0000
MLCVSTRIDE0	0x02Ch/0x42Ch	MLC RGB Layer 0 VERTICAL stride Register	0x0000_0000
MLCTPCOLOR0	0x030h/0x430h	MLC RGB Layer 0 TRANSPARENCY Color Register	0x0000_0000
MLCINVCOLOR0	0x034h/0x434h	MLC RGB Layer 0 INVERSION Color Register	0x0000_0000
MLCADDRESS0	0x038h/0x438h	MLC RGB Layer 0 BASE Address Register	0x0000_0000
RSVD	0x03Ch/0x43Ch	Reserved	0x0000_0000
MLCLEFTright1	0x040h	MLC RGB Layer 1 left right Register	0x0000_0000
MLCTOPBOTTOM1	0x044h	MLC RGB Layer 1 top bottom Register	0x0000_0000
MLCLEFTRIGHT1_0	0x048h	MLC RGB Layer 1INVALID AREA 0 LEFT right Register	0x0000_0000
MLCTOPBOTTOM1_0	0x04Ch	MLC RGB Layer 1INVALID AREA 0 bottom top Register	0x0000_0000
MLCLEFTRIGHT1_1	0x050h	MLC RGB Layer 1INVALID AREA 1 LEFT right Register	0x0000_0000
MLCTOPBOTTOM1_1	0x054h	MLC RGB Layer 1INVALID AREA 1 bottom top Register	0x0000_0000
MLCCONTROL1	0x058h	MLC RGB Layer 1 control Register	0x0000_0000
MLCHSTRIDE1	0x05Ch	MLC RGB Layer 1 HORIZONTAL stride Register	0x0000_0000
MLCVSTRIDE1	0x060h	MLC RGB Layer 1 VERTICAL stride Register	0x0000_0000
MLCTPCOLOR1	0x064h	MLC RGB Layer 1 TRANSPARENCY Color Register	0x0000_0000
MLCINVCOLOR1	0x068h	MLC RGB Layer 1 INVERSION Color Register	0x0000_0000
MLCADDRESS1	0x06Ch	MLC RGB Layer 1 BASE Address Register	0x0000_0000
RSVD	0x070h	Reserved	0x0000_0000
MLCLEFright2	0x074h/0x474h	MLC VIDEO Layer left right Register	0x0000_0000
MLCtopBOTTOM2	0x078h/0x478h	MLC VIDEO Layer top bottom Register	0x0000_0000

Register	Offset	Description	Reset Value
MLCCONTROL2	0x07Ch / 0x47Ch	MLC VIDEO Layer control Register	0x0000_0000
MLCVSTRIDE3	0x080h/0x480h	MLC VIDEO Layer VERTICAL stride Register	0x0000_0000
MLCTPCOLOR3	0x084h/0x484h	MLC VIDEO Layer TRANSPARENCY Color Register	0x0000_0000
RSVD	0x088h/0x488h	Reserved	0x0000_0000
MLCADDRESS3	0x08Ch/0x48Ch	MLC VIDEO Layer BASE Address Register	0x0000_0000
MLCADDRESSCB	0x090h / 0x490h	MLC VIDEO Layer Cb BASE Address Register	0x0000_0000
MLCADDRESSCR	0x094h/0x494h	MLC VIDEO Layer Cr BASE Address Register	0x0000_0000
MLCVSTRIDECB	0x098h/0x498h	MLC VIDEO Layer Cb VERTICAL stride Register	0x0000_0000
MLCVSTRIDECR	0x09Ch/0x49Ch	MLC VIDEO Layer Cr VERTICAL stride Register	0x0000_0000
MLCHSCALE	0x0A0h/0x4A0h	MLC VIDEO Layer Horizontal Scale Register	0x0000_0000
MLCVSCALE	C010_00A4h/ C010_04A4h	MLC VIDEO Layer Vertical Scale Register	0x0000_0800
MLCLUENH	0x0A8h/0x4A8h	MLC VIDEO Layer Luminance Enhancement Control Register	0x0000_0000
MLCCHENH0	0x0ACh/0x4ACh	MLC VIDEO Layer Chrominance Enhancement Control 0 Register	0x0000_0000
MLCCHENH1	0x0B0h/0x4B0h	MLC VIDEO Layer Chrominance Enhancement Control 1 Register	0x0000_0000
MLCCHENH2	0x0B4h/0x4B4h	MLC VIDEO Layer Chrominance Enhancement Control 2 Register	0x0000_0000
MLCCHENH3	0x0B8h/0x4B8h	MLC VIDEO Layer Chrominance Enhancement Control 3 Register	0x0000_0000
MLCGAMMACONT	0x0ECh/0x4ECh	MLC GAMMA CONTROL Register	0x0000_0000
MLCRGAMMATABLEWRITE	0x0F0h/0x4F0h	MLC RED GAMMA TABLE WRITE	-
MLCGGAMMATABLEWRITE	0x0F4h/0x4F4h	MLC GREEN GAMMA TABLE WRITE	-
MLCBGAMMATABLEWRITE	0x0F8h/0x4F8h	MLC BLUE GAMMA TABLE WRITE	-
RSVD	0x0FCh to 0x3BC/ 0x4FCh to 0x7BC	Reserved	0x0000_0000
MLCCLKENB	0x3C0h/0x7C0h	MLC Clock Generation Enable Register	0x0000_0000

33.8.1.1 MLCCONTROLT

- Base Address: 0xC010_2000
- Address = Base Address + 0x000h (Primary), 0x400h (Secondary), Reset Value = 0x0000_0100

Name	Bit	Type	Description	Reset Value
RSVD	[31:14]	R	Reserved	18'b0
RSVD	[13:12]	RW	Reserved	2'b00
PIXELBUFFER_PWD	[11]	RW	MLC Pixel Buffer Power On/Off It should be "On" before MLC Enabled. 0 = Power Off 1 = Power On	1'b0
PIXELBUFFER_SLD	[10]	RW	MLC Pixel Buffer Sleep Mode It is usable only when Power On. 0 = Sleep Mode Enable 1 = Sleep Mode Disable	1'b0
PRIORITY	[9:8]	RW	Specifies the priority of the Video layer. 00 = video layer > layer0 > layer1 > layer2 01 = layer0 > video layer > layer1 > layer2 10 = layer0 > layer1 > video layer > layer2 11 = layer0 > layer1 > layer2 > video layer	2'b1
RSVD	[7:4]	R	Reserved	4'bx
DITTYFLAG	[3]	RW	Dirty Flag for MLC top controller. If this bit is set as "1", the register settings concerned with the Top controller in vertical sync mode are updated and this bit is cleared as "0" automatically. Read: 0 = Clean 1 = Dirty Write: 0 = No affect 1 = Apply modified settings	1'b0
RSVD	[2]	R	Reserved	1'b0
MLCENB	[1]	RW	Specifies whether or not to enable MLC Set when MLCENB Set/Clear together with set MLCCONTROLT DITTYFLAG. 0 = Disable 1 = Enable	1'b0
FIELDENB	[0]	RW	Specifies whether or not to enable Interlace mode. 0 = progressive mode 1 = Interlace mode	1'b0

33.8.1.2 MLCSCREENSIZE

- Base Address: 0xC010_2000
- Address = Base Address + 0x004h, 0x404h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved	4'b0
SCREENHEIGHT	[27:16]	RW	Specifies "the whole screen height - 1".	12'b0
RSVD	[15:12]	R	Reserved	4'b0
SCREENWIDTH	[11:0]	RW	Specifies "the whole screen width - 1".	12'b0

33.8.1.3 MLCBGCOLOR

- Base Address: 0xC010_2000
- Address = Base Address + 0x008h, 0x408h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	R	Reserved	8'b0
DEFAULTCOLOR	[23:0]	RW	Specifies the color to be displayed on the screen in areas not covered by any of the layers Specifies the R8G8B8 format in 24 bpp mode.	24'b0

33.8.1.4 MLCLEFTRIGHT0

- Base Address: 0xC010_2000
- Address = Base Address + 0x00Ch, 0x40Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved	4'b0
LEFT	[27:16]	RW	Specifies the x-coordinate of the upper-left corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0
RSVD	[15:12]	R	Reserved	4'b0
RIGHT	[11:0]	RW	Specifies the x-coordinate of the lower-right corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0

33.8.1.5 MLCTOPBOTTOM0

- Base Address: 0xC010_2000
- Address = Base Address + 0x010h, 0x410h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved	4'b0
TOP	[27:16]	RW	Specifies the y-coordinate of the upper-left corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0
RSVD	[15:12]	R	Reserved	4'b0
BOTTOM	[11:0]	RW	Specifies the y-coordinate of the lower-right corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0

33.8.1.6 MLCLEFTRIGHT0_0

- Base Address: 0xC010_2000
- Address = Base Address + 0x014h, 0x414h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	R	Reserved	3'b0
Invalidenb0	[28]	RW	Shows the status of disable/enable about 1st invisible area of RGB Layer0. 0 = Disable 1 = Enable	1'b0
RSVD	[27]	R	Reserved	1'b0
LEFT	[26:16]	RW	Notify left coordination of X axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
RIGHT	[10:0]	RW	Notify right coordination of X axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0

33.8.1.7 MLCTOPBOTTOM0_0

- Base Address: 0xC010_2000
- Address = Base Address + 0x018h, 0x418h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	R	Reserved	5'b0
TOP	[26:16]	RW	Notify upper coordination of Y axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
BOTTOM	[10:0]	RW	Notify lower coordination of Y axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0

33.8.1.8 MLCLEFTRIGHT0_1

- Base Address: 0xC010_2000
- Address = Base Address + 0x01Ch, 0x41Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	R	Reserved	3'b0
Invalidenb1	[28]	RW	Shows the status of disable/enable about 2nd invisible area of RGB Layer0. 0 = Disable 1 = Enable	1'b0
RSVD	[27]	R	Reserved	1'b0
LEFT	[26:16]	RW	Notify left coordination of X axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
RIGHT	[10:0]	RW	Notify right coordination of X axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0

33.8.1.9 MLCTOPBOTTOM0_1

- Base Address: 0xC010_2000
- Address = Base Address + 0x020h, 0x420h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	R	Reserved	5'b0
TOP	[26:16]	RW	Notify upper coordination of Y axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
BOTTOM	[10:0]	RW	Notify lower coordination of Y axis from the area to be invisible of RGB Layer0. Able to set coordination from 0 to 2047.	11'b0

33.8.1.10 MLCCONTROL0

- Base Address: 0xC010_2000
- Address = Base Address + 0x024h, 0x424h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FORMAT	[31:16]	RW	Specifies the RGB data format. For detailed information, refer to *Table 33-5*.	16'b0
RSVD	[15:14]	R	Reserved	2'b0
LOCKSIZE	[13:12]	RW	Adjusts the data size to be read at any one time when a memory read for RGB data is requested. For a resolution of 1280 × 1024, it is recommended to set it as 16. 0 = 4 1 = 8 2 = 16 3 = reserved	2'b0
RSVD	[11:9]	R	Reserved	3'b0
RSVD	[8]	RW	Reserved but it should be written "0"	1'b0
RSVD	[7:6]	R	Reserved	2'b0
LAYERENB	[5]	RW	Enables/disables this layer. 0 = Disable 1 = Enable	1'b0
DIRTYFLAG	[4]	RW	Dirty flag for this layer. If this bit is set as "1", the register settings concerned with this layer are updated in vertical sync mode and this bit is cleared as "0" automatically. Read: 0 = Clean 1 = Dirty Write:	1'b0

Name	Bit	Type	Description	Reset Value
			0 = No affect 1 = Apply modified settings	
RSVD	[3]	R	Reserved	1'b0
BLENDENB	[2]	RW	Enables/disables the Alpha Blending function in this layer. In addition, this bit should be set as "enable" to apply Alpha to a format with an Alpha channel. 0 = Disable 1 = Enable	1'b0
INVENB	[1]	RW	Enables/disables the Color Inversion function in this layer. 0 = Disable 1 = Enable	1'b0
TPENB	[0]	RW	Enables/disables the Transparency function in this layer. 0 = Disable 1 = Enable	1'b0

33.8.1.11 MLCHSTRIDE0

- Base Address: 0xC010_2000
- Address = Base Address + 0x028h, 0x428h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	RW	Reserved for future use. You have to write `0' only.	1'b0
HSTRIDE	[30:0]	RW	Specifies the horizontal stride in byte units. This value is the byte offset from the current pixel to the next unit and has the number of bytes per pixel in general.	31'b0

33.8.1.12 MLCVSTRIDE0

- Base Address: 0xC010_2000
- Address = Base Address + 0x02Ch, 0x42Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VSTRIDE	[31:0]	RW	Specifies the vertical stride in byte units. This value is the byte offset from the current line to the next line and has the number of bytes per line in general. This value has the 2's complement format and can be specified as a negative number for the Vertical Flip function.	32'b0

33.8.1.13 MLCTPCOLOR0

- Base Address: 0xC010_2000
- Address = Base Address + 0x030h, 0x430h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALPHA	[31:24]	RW	Specifies an Alpha Blending factor. This value is valid only for an RGB format without Alpha channels. The formula for Alpha Blending is as follows: • If ALPHA is 0 then a is 0, else a is ALPHA + 1. • color = this layer color a / 256 + lower layer color (256-a) / 256	8'b0
TPCOLOR	[23:0]	RW	Specifies the color for the Transparency. These bits have the R8G8B8 format in 24 bpp mode.	24'b0

33.8.1.14 MLCINVCOLOR0

- Base Address: 0xC010_2000
- Address = Base Address + 0x034h, 0x434h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	R	Reserved	8'b0
INVCOLOR	[23:0]	RW	Specifies the color to be inverted. These bits have the R8G8B8 format in 24 bpp mode.	24'b0

33.8.1.15 MLCADDRESS0

- Base Address: 0xC010_2000
- Address = Base Address + 0x038h, 0x438h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDRESS	[31:0]	RW	Specifies the memory address where RGB data is stored. In general, the address on the top left of the image is specified, but the address on the bottom left corner is specified for Vertical Flip.	32'b0

33.8.1.16 MLCLEFTright1

- Base Address: 0xC010_2000
- Address = Base Address + 0x040h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved	4'b0
LEFT	[11:0]	RW	Specifies the x-coordinate of the upper-left corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0
RSVD	[15:12]	R	Reserved	4'b0
RIGHT	[27:16]	RW	Specifies the x-coordinate of the lower-right corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0

33.8.1.17 MLCtopBOTTOM1

- Base Address: 0xC010_2000
- Address = Base Address + 0x044h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved	4'b0
TOP	[27:16]	RW	Specifies the y-coordinate of the upper-left corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0
RSVD	[15:12]	R	Reserved	4'b0
BOTTOM	[11:0]	RW	Specifies the y-coordinate of the lower-right corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0

33.8.1.18 MLCLEFTRIGHT1_0

- Base Address: 0xC010_2000
- Address = Base Address + 0x048h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	R	Reserved	3'b0
INvalidenb0	[28]	RW	Shows the status of disable/enable about 1st invisible area of RGB Layer1. 0 = Disable 1 = Enable	1'b0
RSVD	[27]	R	Reserved	1'b0
LEFT	[26:16]	RW	Notify left coordination of X axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
RIGHT	[10:0]	R/W	Notify right coordination of X axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0

33.8.1.19 MLCTOPBOTTOM1_0

- Base Address: 0xC010_2000
- Address = Base Address + 0x04Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	R	Reserved	5'b0
TOP	[26:16]	RW	Notify upper coordination of Y axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
BOTTOM	[10:0]	R/W	Notify lower coordination of Y axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0

33.8.1.20 MLCLEFTRIGHT1_1

- Base Address: 0xC010_2000
- Address = Base Address + 0x050h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	R	Reserved	3'b0
Invalidenb1	[28]	RW	Shows the status of disable/enable about 2nd invisible area of RGB Layer1. 0 = Disable 1 = Enable	1'b0
RSVD	[27]	R	Reserved	1'b0
LEFT	[26:16]	RW	Notify left coordination of X axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
RIGHT	[10:0]	RW	Notify right coordination of X axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0

33.8.1.21 MLCTOPBOTTOM1_1

- Base Address: 0xC010_2000
- Address = Base Address + 0x054h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:27]	R	Reserved	5'b0
TOP	[26:16]	RW	Notify upper coordination of Y axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0
RSVD	[15:11]	R	Reserved	5'b0
BOTTOM	[10:0]	RW	Notify lower coordination of Y axis from the area to be invisible of RGB Layer1. Able to set coordination from 0 to 2047.	11'b0

33.8.1.22 MLCCONTROL1

- Base Address: 0xC010_2000
- Address = Base Address + 0x058h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FORMAT	[31:16]	RW	Specifies the RGB data format. For detailed information, refer to *Table 33-5*.	16'b0
RSVD	[15:14]	R	Reserved	2'b0
LOCKSIZE	[13:12]	RW	Adjusts the data size to be read at any one time when a memory read for RGB data is requested. For a resolution of 1280 × 1024, it is recommended to set it as 16. 0 = 4 1 = 8 2 = 16 3 = reserved	2'b0
RSVD	[11:9]	R	Reserved	3'b0
RSVD	[8]	RW	Reserved but you have to write 0 only	1'b0
RSVD	[7:6]	R	Reserved	2'b0
LAYERENB	[5]	RW	Enables/disables this layer. 0 = Disable 1 = Enable	1'b0
DIRTYFLAG	[4]	RW	Dirty flag for this layer. If this bit is set as "1", the register settings concerned with this layer are updated in vertical sync mode and this bit is cleared as "0" automatically. Read: 0 = Clean 1 = Dirty Write: 0 = No affect 1 = Apply modified settings	1'b0
RSVD	[3]	R	Reserved	1'b0
BLENDENB	[2]	RW	Enables/disables the Alpha Blending function in this layer. In addition, this bit should be set as "enable" to apply Alpha to a format with Alpha channels. 0 = Disable 1 = Enable	1'b0
INVENB	[1]	RW	Enables/disables the Color Inversion function in this layer. 0 = Disable 1 = Enable	1'b0
TPENB	[0]	RW	Enables/disables the Transparency function in this layer. 0 = Disable 1 = Enable	1'b0

33.8.1.23 MLCHSTRIDE1

- Base Address: 0xC010_2000
- Address = Base Address + 0x05Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31]	RW	Reserved for future use. You have to write `0' only.	1'b0
HSTRIDE	[30:0]	RW	Specifies the horizontal stride in byte units. This value is the byte offset from the current pixel to the next unit and has the number of bytes per pixel in general.	31'b0

33.8.1.24 MLCVSTRIDE1

- Base Address: 0xC010_2000
- Address = Base Address + 0x060h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VSTRIDE	[31:0]	RW	Specifies the vertical stride in byte units. This value is the byte offset from the current line to the next line and has the number of bytes per line in general. This value has the 2's complement format and can be specified as a negative number for the Vertical Flip function.	32'b0

33.8.1.25 MLCTPCOLOR1

- Base Address: 0xC010_2000
- Address = Base Address + 0x064h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALPHA	[31:24]	RW	Specifies an Alpha Blending factor. This value is valid only for an RGB format without an Alpha channel. The formula for Alpha Blending is as follows: • If ALPHA is 0 then a is 0, else a is ALPHA + 1. • color = this layer color a / 256 + lower layer color (256-a) / 256	8'b0
TPCOLOR	[23:0]	RW	Specifies the color for the Transparency. These bits have the R8G8B8 format in 24 bpp mode.	24'b0

33.8.1.26 MLCINVCOLOR1

- Base Address: 0xC010_2000
- Address = Base Address + 0x068h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	R	Reserved	8'b0
INVCOLOR	[23:0]	RW	Specifies the color to be inverted. These bits have the R8G8B8 format in 24 bpp mode.	24'b0

33.8.1.27 MLCADDRESS1

- Base Address: 0xC010_2000
- Address = Base Address + 0x06Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDRESS	[31:0]	RW	Specifies the memory address where RGB data is stored. In general, the address on the top left end of the image is specified, but the address on the bottom left corner is specified for Vertical Flip.	32'b0

33.8.1.28 MLCLERight2

- Base Address: 0xC010_2000
- Address = Base Address + 0x074h, 0x474h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved	4'b0
LEFT	[27:16]	RW	Specifies the x-coordinate of the upper-left corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0
RSVD	[15:12]	R	Reserved	4'b0
RIGHT	[11:0]	RW	Specifies the x-coordinate of the lower-right corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0

33.8.1.29 MLCtopBOTTOM2

- Base Address: 0xC010_2000
- Address = Base Address + 0x078h, 0x478h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	R	Reserved	4'b0
TOP	[27:16]	RW	Specifies the y-coordinate of the upper-left corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0
RSVD	[15:12]	R	Reserved	4'b0
BOTTOM	[11:0]	RW	Specifies the y-coordinate of the lower-right corner of the layer. This value has 2's complement and from -2048 to 2047.	12'b0

33.8.1.30 MLCCONTROL2

- Base Address: 0xC010_2000
- Address = Base Address + 0x07Ch, 0x47Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:19]	R	Reserved	16'b0
FORMAT	[18:16]	RW	Specifies the YUV data format. 0 = 2D block addressing separated YUV 420 (each component has 8-bit data width) 1 = 2D block addressing separated YUV 422 (each component has 8-bit data width) 2 = Linear YUV 422 (YUYV) 3 = 2D block addressing separated YUV 444 (each component has 8-bit data width)	2'b00
lienbuffer_pwd	[15]	RW	Video Layer Line Buffer's Power On/Off 0 = Power Off 1 = Power On	1'b0
lienbuffer_slmd	[14]	RW	Video Layer Line Buffer's Sleep Mode. It is usable only when lien buffer_pwd = "1" 0 = Sleep Mode Enable 1 = Sleep Mode Disable	1'b0
LAYERENB	[5]	RW	Enables/disables this layer. 0 = Disable 1 = Enable	1'b0
DIRTYFLAG	[4]	RW	Dirty flag for this layer. If this bit is set as "1", the register settings concerned with this layer are updated in vertical sync mode and this bit is cleared as "0" automatically. Read: 0 = Clean	1'b0

Name	Bit	Type	Description	Reset Value
			1 = Dirty Write: 0 = No affect 1 = Apply modified settings	
RSVD	[3]	R	Reserved	1'b0
BLENDENB	[2]	RW	Enables/disables the Alpha Blending function in this layer. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	RW	Reserved for future use. You have to write "0" only.	2'b0

33.8.1.31 MLCVSTRIDE3

- Base Address: 0xC010_2000
- Address = Base Address + 0x080h, 0x480h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VSTRIDE	[31:0]	RW	Specifies the vertical stride in byte units. This value is the byte offset from the current line to the next line and has the number of bytes per line in general. In the 2D block addressing separated YUV format, this value only corresponds to the Y component and should be set as 4096 in general.	32'b0

33.8.1.32 MLCTPCOLOR3

- Base Address: 0xC010_2000
- Address = Base Address + 0x084h, 0x484h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ALPHA	[31:24]	RW	Specifies an Alpha Blending factor. The formula for Alpha Blending is as follows: • If ALPHA is 0 then a is 0, else a is ALPHA + 1. • color = this layer color a / 256 + lower layer color (256-a) / 256	8'b0
RSVD	[23:0]	R	Reserved	24'b0

33.8.1.33 MLCADDRESS3

- Base Address: 0xC010_2000
- Address = Base Address + 0x08Ch, 0x48Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDRESS	[31:0]	RW	Specifies the memory address where YUB data is stored. In the 2D block addressing separated YUV format, this value only corresponds to the Y component and should be set as follows: • ADDRESS[31:24]: the index of segment • ADDRESS[23:12]: y-coordinate in segment • ADDRESS[11:0]: x-coordinate in segment, ADDRESS[2:0] must be "0"	32'b0

33.8.1.34 MLCADDRESSCB

- Base Address: 0xC010_2000
- Address = Base Address + 0x090h, 0x490h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDRESSCB	[31:0]	RW	Specifies the memory address where Cb data is stored. These bits are valid only for the 2D block addressing separated YUV format and should be set as follows: • ADDRESS[31:24]: the index of segment • ADDRESS[23:12]: y-coordinate in segment • ADDRESS[11:0]: x-coordinate in segment, ADDRESS[2:0] must be "0"	32'b0

33.8.1.35 MLCADDRESSCR

- Base Address: 0xC010_2000
- Address = Base Address + 0x094h, 0x494h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
ADDRESSCR	[31:0]	RW	Specifies the memory address where Cr data is stored. These bits are valid only for the 2D block addressing separated YUV format and should be set as follows: • ADDRESS[31:24]: the index of segment • ADDRESS[23:12]: y-coordinate in segment • ADDRESS[11:0]: x-coordinate in segment, ADDRESS[2:0] must be "0"	32'b0

33.8.1.36 MLCVSTRIDECB

- Base Address: 0xC010_2000
- Address = Base Address + 0x098h, 0x498h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VSTRIDECB	[31:0]	RW	Specifies the vertical stride for Cr data in byte units. These bits are valid only for the 2D block addressing separated YUV format and should be set as 4096 in general.	32'b0

33.8.1.37 MLCVSTRIDECR

- Base Address: 0xC010_2000
- Address = Base Address + 0x09Ch, 0x49Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
VSTRIDECR	[31:0]	RW	Specifies the vertical stride for Cr data in byte units. These bits are valid only for the 2D block addressing separated YUV format and should be set as 4096 in general.	32'b0

33.8.1.38 MLCHScALE

- Base Address: 0xC010_2000
- Address = Base Address + 0x0A0h, 0x4A0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	2'b0
HFILTERENB_C	[29]	RW	Decides whether to use bilinear filter when Video Layer horizontal scale.(Chroma filter enable) 0 = Disable (point sample) 1 = Enable (bilinear filter)	1'b0
HFILTERENB	[28]	RW	Decides whether to use bilinear filter when Video Layer horizontal scale.(Luminance filter enable) 0 = Disable (point sample) 1 = Enable (bilinear filter)	1'b0
RSVD	[27:23]	R	Reserved	5'b0
HSCALE	[22:0]	RW	Specifies the ratio for the horizontal scale. The formula to calculate this value is as follows: When FILTERENB is 1 and the destination width is wider than the source width: • HSCALE = (source width-1) (1<<11) / (destination width-1) , else • HSCALE = source width (1<<11) / destination width	23'h800

33.8.1.39 MLCVSCALE

- Base Address: 0xC010_2000
- Address = Base Address + 0x0A4h, 0x4A4h, Reset Value = 0x0000_0800

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	2'b0
VFILTERENB_C	[29]	RW	Decides whether to use bilinear filter when Video Layer vertical scale.(Chroma filter enable) 0 = Disable (Nearest sample) 1 = Enable (bilinear filter)	1'b0
VFILTERENB	[28]	RW	Decides whether to use bilinear filter when Video Layer vertical scale.(Luminance filter enable) 0 = Disable (Nearest sample) 1 = Enable (bilinear filter)	1'b0
RSVD	[27:23]	R	Reserved	5'b0
VSCALE	[22:0]	RW	Specifies the ratio for the vertical scale. The formula to calculate this value is as follows: When FILTERENB is 1, the destination height is higher than the source height: • VSCALE = (source height-1) (1<<11) / (destination height-1) , else • VSCALE = source height (1<<11) / destination height	23'h800

33.8.1.40 MLCLUENH

- Base Address: 0xC010_2000
- Address = Base Address + 0x0A8h, 0x4A8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
BRIGHTNESS	[15:8]	RW	Specifies brightness values in 256 levels. These values are 2's complements and can be set between -128 and +127.	8'b0
RSVD	[7:3]	R	Reserved	5'b0
CONTRAST	[2:0]	RW	Specifies contrast levels with 8 levels. 0 = 1.0 1 = 1.125 2 = 1.25 3 = 1.375 4 = 1.5 5 = 1.625 6 = 1.75 7 = 1.875	3'b0

33.8.1.41 MLCCHENH0

- Base Address: 0xC010_2000
- Address = Base Address + 0x0ACh, 0x4ACh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HUECR1B	[31:24]	RW	Specifies the factors for Hue and Saturation for the first quadrant. Each value has the 2's complement format and the format is [S.1.6] (here, S means a sign bit).	8'h40
HUECR1A	[23:16]	RW		8'b0
HUECB1B	[15:8]	RW		8'b0
HUECB1A	[7:0]	RW	The Hues and Saturations for each quadrant are determined by the following formulae: • (B-Y) = (B-Y) HUECBnA + (R-Y) HUECBnB • (R-Y) = (B-Y) HUECRnA + (R-Y) HUECRnB The formulae for each factor are as follows: • HUECBnA = cos(θ) 64 gain • HUECBnB = -sin(θ) 64 gain • HUECRnA = sin(θ) 64 gain • HUECRnB = cos(θ) 64 gain Where the gain value is between 0 and 2.	8'h40

33.8.1.42 MLCCHENH1

- Base Address: 0xC010_2000
- Address = Base Address + 0x0B0h, 0x4B0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HUECR2B	[31:24]	RW	Specifies the factors for Hue and Saturation for the second quadrant. Each value has the 2's complement format and the format is [S.1.6] (here, S means a sign bit).	8'h40
HUECR2A	[23:16]	RW		8'b0
HUECB2B	[15:8]	RW		8'b0
HUECB2A	[7:0]	RW	The Hues and Saturations for each quadrant are determined by the following formulae: • (B-Y) = (B-Y) HUECBnA + (R-Y) HUECBnB • (R-Y) = (B-Y) HUECRnA + (R-Y) HUECRnB The formulae for each factor are as follows: • HUECBnA = cos(θ) 64 gain • HUECBnB = -sin(θ) 64 gain • HUECRnA = sin(θ) 64 gain • HUECRnB = cos(θ) 64 gain Where the gain value is between 0 and 2.	8'h40

33.8.1.43 MLCCHENH2

- Base Address: 0xC010_2000
- Address = Base Address + 0x0B4h, 0x4B4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HUECR3B	[31:24]	RW	Specifies the factors for Hue and Saturation for the third quadrant. Each value has the 2's complement format and the format is [S.1.6] (here, S means a sign bit).	8'h40
HUECR3A	[23:16]	RW		8'b0
HUECB3B	[15:8]	RW		8'b0
HUECB3A	[7:0]	RW	The Hues and Saturations for each quadrant are determined by the following formulae: • (B-Y) = (B-Y) HUECBnA + (R-Y) HUECBnB • (R-Y) = (B-Y) HUECRnA + (R-Y) HUECRnB The formulae for each factor are as follows: • HUECBnA = cos(θ) 64 gain • HUECBnB = -sin(θ) 64 gain • HUECRnA = sin(θ) 64 gain • HUECRnB = cos(θ) 64 gain Where the gain value is between 0 and 2.	8'h40

33.8.1.44 MLCCHENH3

- Base Address: 0xC010_2000
- Address = Base Address + 0x0B8h, 0x4B8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HUECR4B	[31:24]	RW	Specifies the factors for Hue and Saturation for the fourth quadrant. Each value has the 2's complement format and the format is [S.1.6] (here, S means a sign bit).	8'h40
HUECR4A	[23:16]	RW		8'b0
HUECB4B	[15:8]	RW		8'b0
HUECB4A	[7:0]	RW	The Hues and Saturations for each quadrant are determined by the following formulae: • (B-Y) = (B-Y) HUECBnA + (R-Y) HUECBnB • (R-Y) = (B-Y) HUECRnA + (R-Y) HUECRnB The formulae for each factor are as follows: • HUECBnA = cos(θ) 64 gain • HUECBnB = -sin(θ) 64 gain • HUECRnA = sin(θ) 64 gain • HUECRnB = cos(θ) 64 gain Where the gain value is between 0 and 2.	8'h40

33.8.1.45 MLCGAMMACONT

- Base Address: 0xC010_2000
- Address = Base Address + 0x0ECh, 0x4ECh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved	19'b0
BGAMMATABLE_PWD	[11]	RW	"Blue" Gamma Table Power On/Off It should be "On" before MLC GAMMA Enabled. 0 = Power Off 1 = Power On	1'b0
BGAMMATABLE_SLD	[10]	RW	"Blue" Gamma Table Sleep Mode It is usable only when Power On. 0 = Sleep Mode Enable 1 = Sleep Mode Disable	1'b0
GGAMMATABLE_PWD	[9]	RW	"Green" Gamma Table Power On/Off It should be `On' before MLC GAMMA Enabled. 0 = Power Off 1 = Power On	1'b0
GGAMMATABLE_SLD	[8]	RW	"Green" Gamma Table Sleep Mode It is usable only when Power On. 0 = Sleep Mode Enable 1 = Sleep Mode Disable	1'b0
RSVD	[7:6]	R	Reserved	2'b0
ALPHASELECT	[5]	RW	Determine whether the Alpha blended region with RGB layer, in Video layer, should be processed as Video layer or as RGB layer. 0 = RGB 1 = Video	1'b0
YUVGAMMAENB	[4]	RW	Gamma Enable for the Video region 0 = Disable 1 = Enable	1'b0
RGAMMATABLE_PWD	[3]	RW	"Red" Gamma Table Power On/Off It should be `On' before MLC GAMMA Enabled. 0 = Power Off 1 = Power On	1'b0
RGAMMATABLE_SLD	[2]	RW	"Red" Gamma Table Sleep Mode It is usable only when Power On. 0 = Sleep Mode Enable 1 = Sleep Mode Disable	1'b0
RGBGAMMAEMB	[1]	RW	Gamma Enable for the RGB region 0 = Disable 1 = Enable	1'b0
DitherEnb	[0]	RW	Dither Enable Enables/disables the dithering operation when 10-bit, as	1'b0

Name	Bit	Type	Description	Reset Value
			the result of Gamma correction, is transformed to 8-bit. 0 = Disable 1 = Enable	

33.8.1.46 MLCRGAMMATABLEWRITE

- Base Address: 0xC010_2000
- Address = Base Address + 0x0F0h, 0x4F0h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
Tableaddr	[31:24]	W	Table Write Address (Size: 10-bit × 256)	–
RSVD	[23:10]	–	Reserved	–
TABLEDATA	[9:0]	W	Table Write Data	–

33.8.1.47 MLCGGAMMATABLEWRITE

- Base Address: 0xC010_2000
- Address = Base Address + 0x0F4h, 0x4F4h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
Tableaddr	[31:24]	W	Table Write Address	–
RSVD	[23:10]	–	Reserved	–
TABLEDATA	[9:0]	W	Table Write Data	–

33.8.1.48 MLCBGAMMATABLEWRITE

- Base Address: 0xC010_2000
- Address = Base Address + 0x0F8h, 0x4F8h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
Tableaddr	[31:24]	W	Table Write Address	–
RSVD	[23:10]	–	Reserved	–
TABLEDATA	[9:0]	W	Table Write Data	–

33.8.1.49 MLCCLKENB

- Base Address: 0xC010_2000
- Address = Base Address + 0x7C0h, 0x4F8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is always disabled (can access CLKGEN only)	1'b0

Name	Bit	Type	Description	Reset Value
			1 = PCLK is always enabled	
RSVD	[2]	R	Reserved	1'b0
BCLKMODE	[1:0]	RW	Specifies BCLK operating mode. 0 = BCLK is always disabled 1 = Reserved (Never use this) 2 = Reserved (Never use this) 3 = BCLK is always enabled	2'b0

34 Display Controller (DPC)

34.1 Overview

The Display controller (hereinafter, DPC) is a block that generates the signals to interface with external display devices, such as a TFT-LCD, or video encoder. The DPC consists of a Sync generator. The Sync generator transmits control signals to the Multi-Layer Controller (MLC) and receives RGB data from the MLC. Then the Sync generator converts the received RGB data into a suitable format. In addition, the Sync generator can supports various types of LCD and video encoders adjusting various output formats and Sync signals.

34.2 Features

- Supports RGB, Multiplexed RGB (MRGB), ITU-R BT.601, ITU-R BT.656 and MPU Type (i80)
- Programmable HSYNC, VSYNC and DE (Data Enable)
- Programmable polarity for Sync signals
- Programmable delay for data, Sync signals and clock phase
- Supports UP-Scaler (Only Secondary Display)
- Supports RGB dithering
- VCLK (video clock) max frequency 150 MHz
- Max resolution 2048 × 2048

34.3 Block Diagram

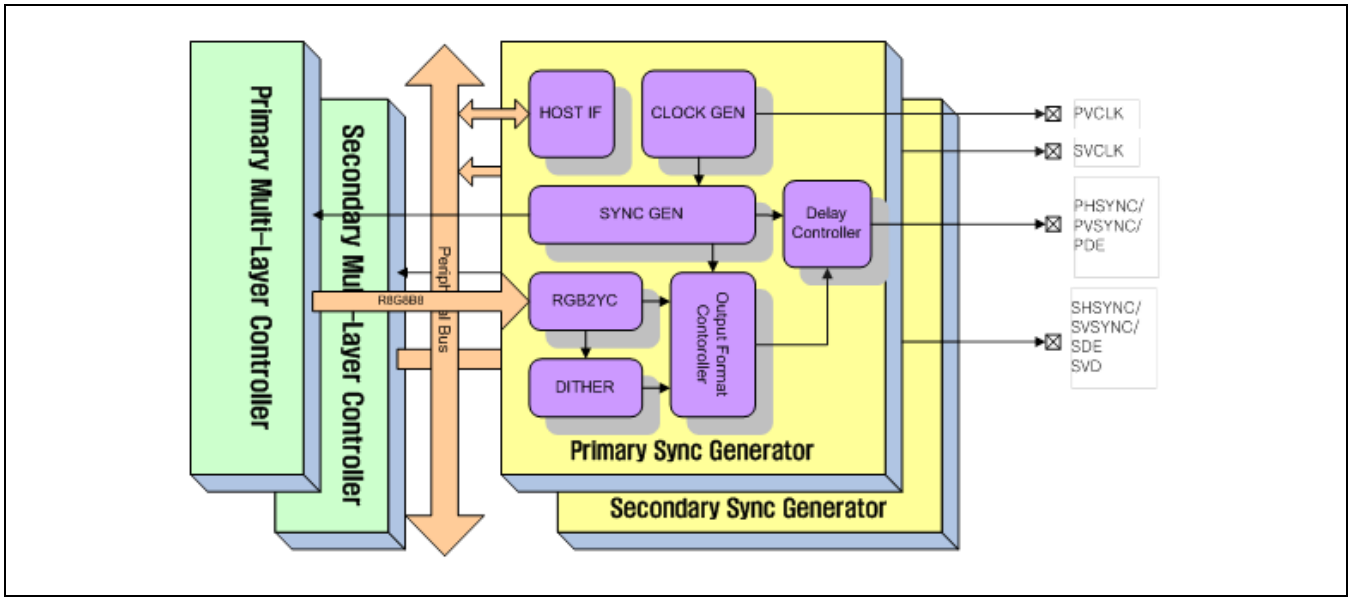


Figure 34-1 Display Controller

34.4 Sync Generator

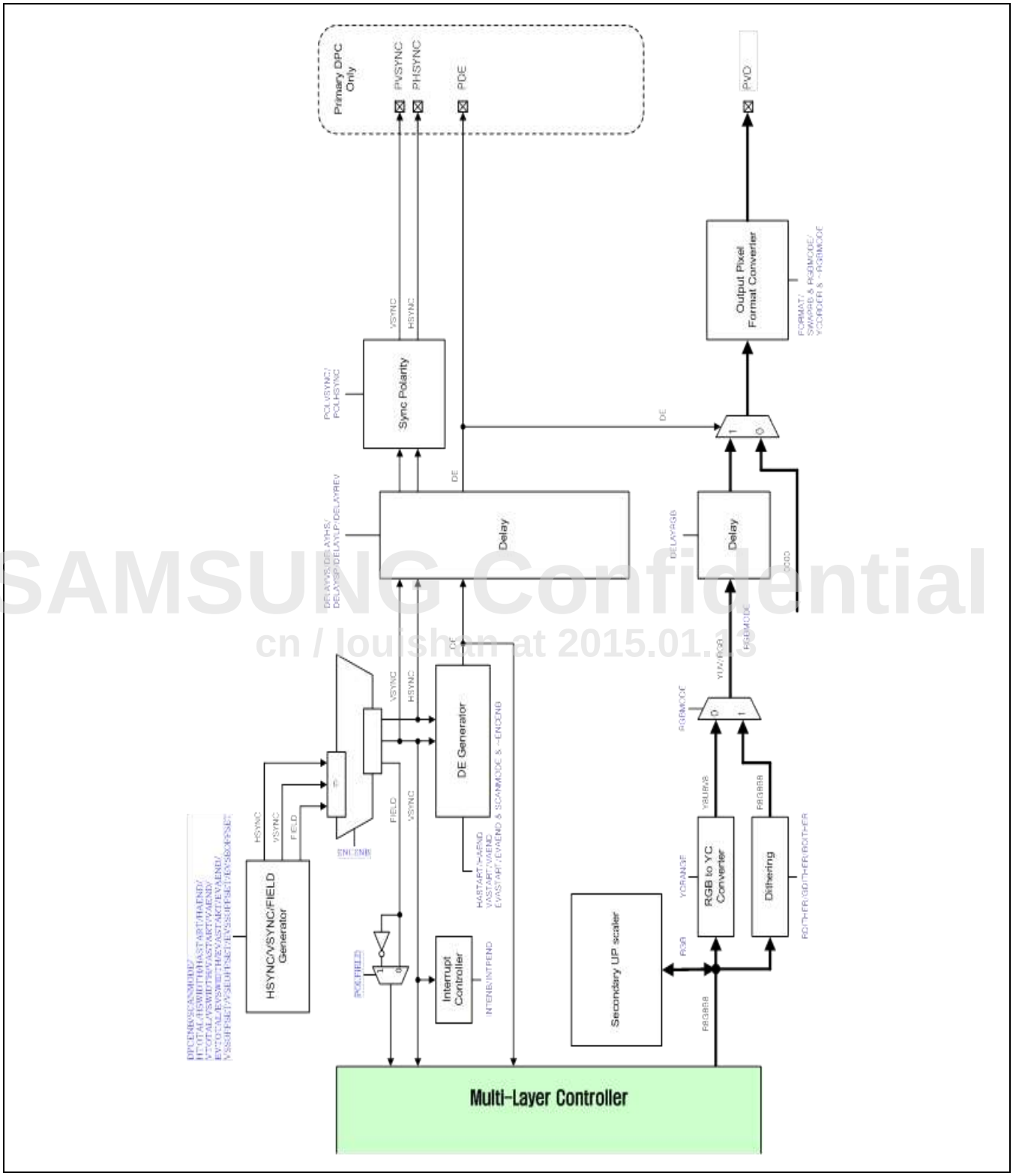


Figure 34-2 Sync Generator

34.4.1 Clock Generation

34.4.1.1 Peripheral Clock Generation

The PCLK is used when the CPU accesses the registers of the DPC. Users can adjust the DPC clock by setting the PCLKMODE for the user's purpose.

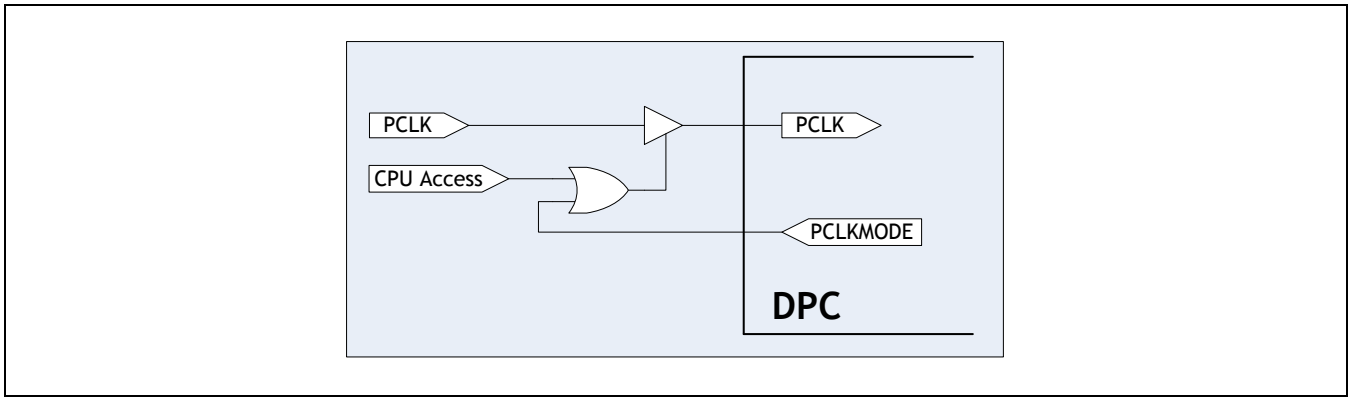


Figure 34-3 Peripheral Clock Generation

Table 34-1 PCLK Mode

PCLKMODE	Brief Description
0	Always Disable
1	Always enabled.

34.4.1.2 Video Clock Generation

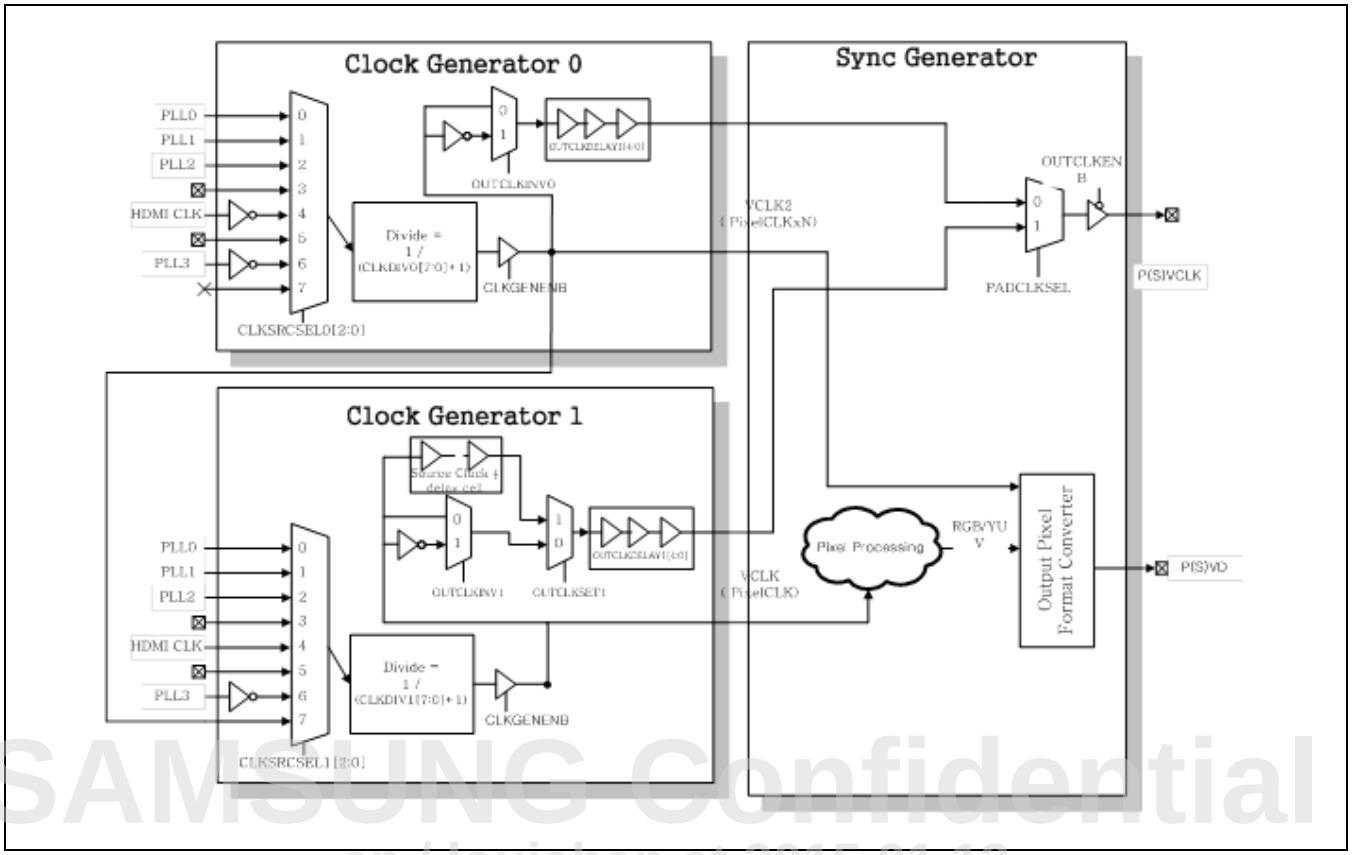


Figure 34-4 Video Clock Generation

The DPC can create an output clock via various clock sources. The clocks for creating an output clock are 2-PLL, PADCLK (P/SCLK, ACLK), etc.

The sync generator uses the VCLK and the VCLK2 as clock sources. The VCLK is a clock for the operation of a pixel unit. The VCLK2 is a clock for pixel output. Therefore, the VCLK is one clock per pixel and the VCLK2 is 1 to 6 clocks per pixel depending on the output format. In the RGB and ITU-R BT.601A formats, which output one pixel data per clock, the VCLK and the VCLK2 share the same clock. In the MRGB, the ITU-R BT.601B, the ITU-R BT.601 (8-bit) and the ITU-R BT.656 formats, which output one pixel data per two clocks, the VCLK should divide the VCLK2 by 2. Since the VCLK should divide the VCLK2 by 2, Clock Generator1 should use the output of Clock Generator0 as the clock source. Users can select the output source by using the PADCLKSEL. The selection of the PADCLKSEL is not related to the operation of the sync generator. In general, VCLK2 is used as the output clock. If, however, a display device using a dual edge is connected, the VCLK is used as the output clock.

Table 34-2 Recommend Clock Settings

Format	CLKSRCSEL0	CLKDIV0	CLKSRCSEL1	CLKDIV1	OUTCLKSEL1	PADCLKSEL
RGB, ITU-R BT.601A	0 to 6	0 to 256	7	0	0	1
MRGB, ITU-R BT.601B, 601 (8-bit), 656,MPU (i80)	0 to 6	0 to 256	7	1	0	1
MRGB (- Dual edge)	0 to 6	0 to 256	7	1	1	0
SRGB888	0 to 6	0 to 256	7	6	0	2
SRGBD8888	0 to 6	0 to 256	7	4	0	1

The DPC can adjust the polarity and phase of the output clock. The OUTCLKINV adjusts the polarity of the output clock and the OUTCLKDELAY, OUTCLKSEL adjusts the phase of the output clock.

Basically, the DPC outputs data to be fetched at the falling edge and the OUTCLKINV is set as "0". For a display device that fetches the clock at the rising edge, the OUTCLKINV should be set as "1" to invert the output clock.

Table 34-3 Clock Delay

OUTCLKDELAY	0	1	2	3	4	5	6	7
tDelay (ns)	TBD							

The output clock is changed by the OUTCLKINV and the OUTCLKDELAY as shown in *Figure 34-5*.

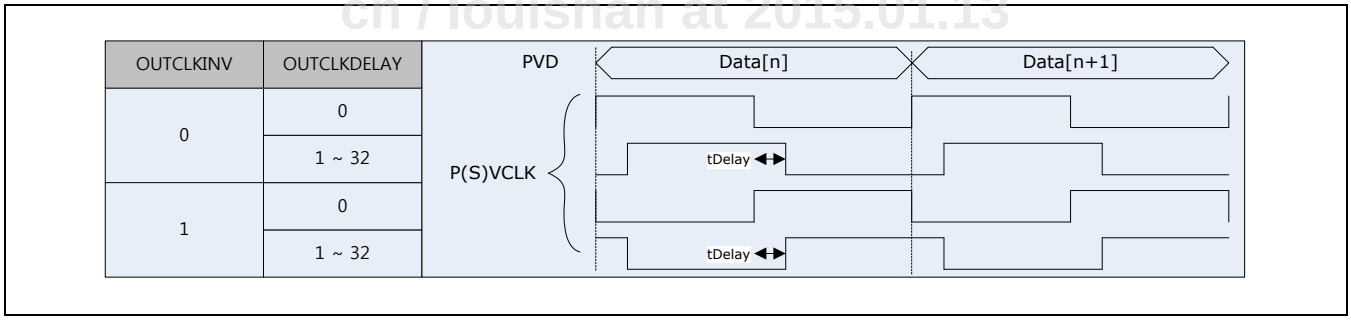


Figure 34-5 Clock Polarity and Delay

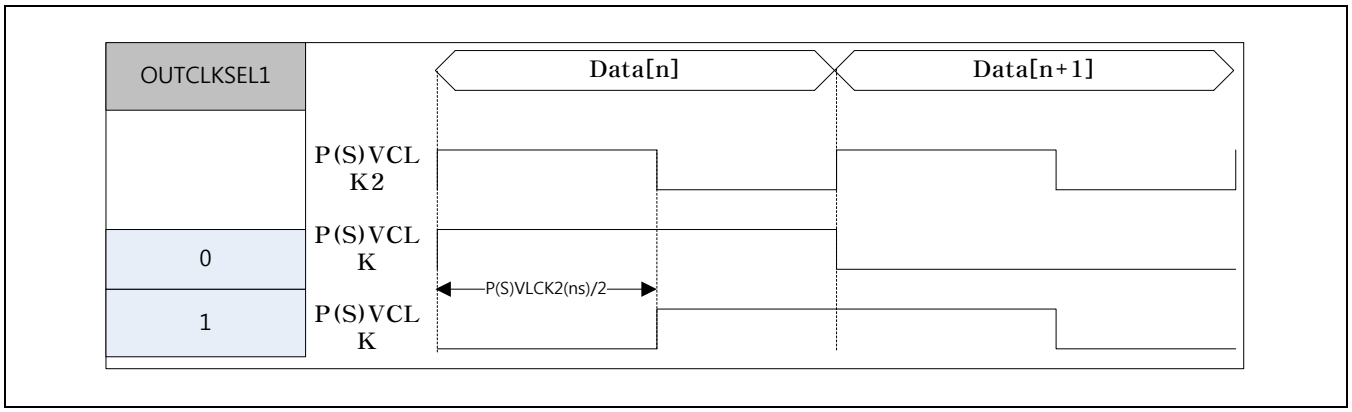


Figure 34-6 OUTCLK Delay

34.4.2 Format

The sync generator can receive RGB888 data from the MLC and display the data in various formats.

The formats that can be displayed by the primary sync generator are listed in *Table 34-4*.

Table 34-4 Data format for Primary Sync Generator

Output format	RGB MODE	FORMAT	CLK	PVD																							
				23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RGB555		0	-										R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
RGB565		1	-	R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0			
RGB666		2	-	R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0		
RGB888		3	-	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
MRGB555A	1	4	1st																	G2	G1	G0	B4	B3	B2	B1	B0
			2nd																		R4	R3	R2	R1	R0	G4	G3
MRGB555B		5	1st																	G2	G1	G0	B4	B3	B2	B1	B0
			2nd																	R4	R3	R2	R1	R0		G4	G3
MRGB565		6	1st																	G2	G1	G0	B4	B3	B2	B1	B0
			2nd																	R4	R3	R2	R1	R0	G5	G4	G3
MRGB666		7	1st																G2	G1	G0	B5	B4	B3	B2	B1	B0

Output format	RGB MODE	FORMAT	CLK	PVD																							
				23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			2nd																R5	R4	R3	R2	R1	R0	G5	G4	G3
MRGB888A		8	1st													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
			2nd													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
MRGB888B		9	1st													G4	G3	G2	B7	B6	B5	B4	B3	G0	B2	B1	B0
			2nd													R7	R6	R5	R4	R3	G7	G6	G5	R2	R1	R0	G1
ITU-R BT.656 BT.601(8bit)	0	10	1st									Cb7	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0								
			2nd									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								
			3rd									Cr7	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0								
			4th									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0								
ITU-R BT.601A		12	1st									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cb7	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0
			2nd									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cr7	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0
ITU-R BT.601B		13	1st									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cb7	Cb6	Cb5	Cb4	Cb3	Cb2	Cb1	Cb0
			2nd																	Cr7	Cr6	Cr5	Cr4	Cr3	Cr2	Cr1	Cr0
4096 Color	X	1	-																	R0	G0	B0	R1	B1	G1	R2	G2
16 Level Gray	X	3	-																	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7

Up to 24-bit data is available in the primary sync generator. If, however, the display format is not RGB666 or RGB888, the higher 8-bit is not used.

34.4.2.1 RGB Format

In the RGB format, data are displayed in the order of blue components, green components and red components based on the lower data. However, a user can swap the display of red components and blue components by setting the SWAPRB as "1".

In addition, the DPC supports the Dithering effect in RGB format. All RGB data transmitted from the MLC have 8-bit data width. Therefore, if the data width of each component is less than 8-bit, as in RGB565 and RGB666 display, the lower bits are discarded. In such cases, the display quality can be compensated by the Dithering effect.

When RGB images are displayed as RGB565, the dithered image shows the difference from the image displayed, as shown in *Figure 34-7*, after the unused lower bits are simply discarded.

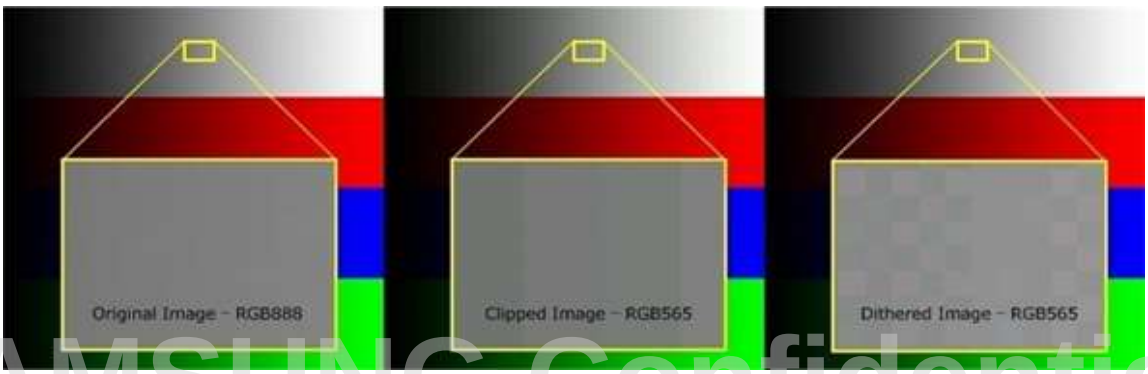


Figure 34-7 RGB Dithering

The RGB Dithering is set by RDITHER, GDITHER*and*BDITHER and the setting values by output formats are listed in *Table 34-5*.

Table 34-5 Recommend Setting for RGB Dithering

Output Format	RDITHER	GDITHER	BDITHER
RGB555, MRGB555A, MRGB555B	5-bit Dither	5-bit Dither	5-bit Dither
RGB565, MRGB565	5-bit Dither	6-bit Dither	5-bit Dither
RGB666, MRGB666	6-bit Dither	6-bit Dither	6-bit Dither
STN - 4096 Color, 16 Level Gray	4-bit Dither	4-bit Dither	4-bit Dither
RGB888, MRGB888A/B, ITU-R BT.656, ITU-R BT.601A/B	Bypass	Bypass	Bypass

34.4.2.2 YCbCr Format

Since the DPC only receives RGB data from the MLC, it outputs the data after converting the RGB data to YCbCr data for the ITU-R BT.656 display or the ITU-R BT.601 display.

The DPC converts RGB data to YCbCr data by using the following formulae:

The formula for RGB to YCbCr conversion

Y= 0.229 R + 0.587 G + 0.114 × B
Cb = – 0.169 × R – 0.331 × G + 0.5 × B
Cr = 0.5 × R – 0.419 × G – 0.081 × B

When ITU-R BT.601 B external display device is used, the user can change the data output order by adjusting the YCORDER. The output data for YCORDER can be changed as listed in *Table 34-6*.

Table 34-6 Output Order for ITU-R BT. 601 B

YCORDER	0		1	
CLK	1st	2nd	1st	2nd
VD[15]	Y[7]		Y[7]	
VD[14]	Y[6]		Y[6]	
VD[13]	Y[5]		Y[5]	
VD[12]	Y[4]		Y[4]	
VD[11]	Y[3]		Y[3]	
VD[10]	Y[2]		Y[2]	
VD[9]	Y[1]		Y[1]	
VD[8]	Y[0]		Y[0]	
VD[7]	Cr[7]	Cb[7]	Cb[7]	Cr[7]
VD[6]	Cr[6]	Cb[6]	Cb[6]	Cr[6]
VD[5]	Cr[5]	Cb[5]	Cb[5]	Cr[5]
VD[4]	Cr[4]	Cb[4]	Cb[4]	Cr[4]
VD[3]	Cr[3]	Cb[3]	Cb[3]	Cr[3]
VD[2]	Cr[2]	Cb[2]	Cb[2]	Cr[2]
VD[1]	Cr[1]	Cb[1]	Cb[1]	Cr[1]
VD[0]	Cr[0]	Cb[0]	Cb[0]	Cr[0]

34.4.3 Sync Signals

The sync generator creates sync signals with various timings. The primary sync generator transmits HSYNC, VSYNC and DE signals to the outside to provide timing interfaces for external display devices. Users can program each sync signal setting to create the timings required from external display devices.

34.4.3.1 Horizontal Timing Interface

HSYNC and DE signals are used for Horizontal Sync. The horizontal timing consists of tHSW, tHBP, tHFP and tAVW as shown in *Figure 34-8*.

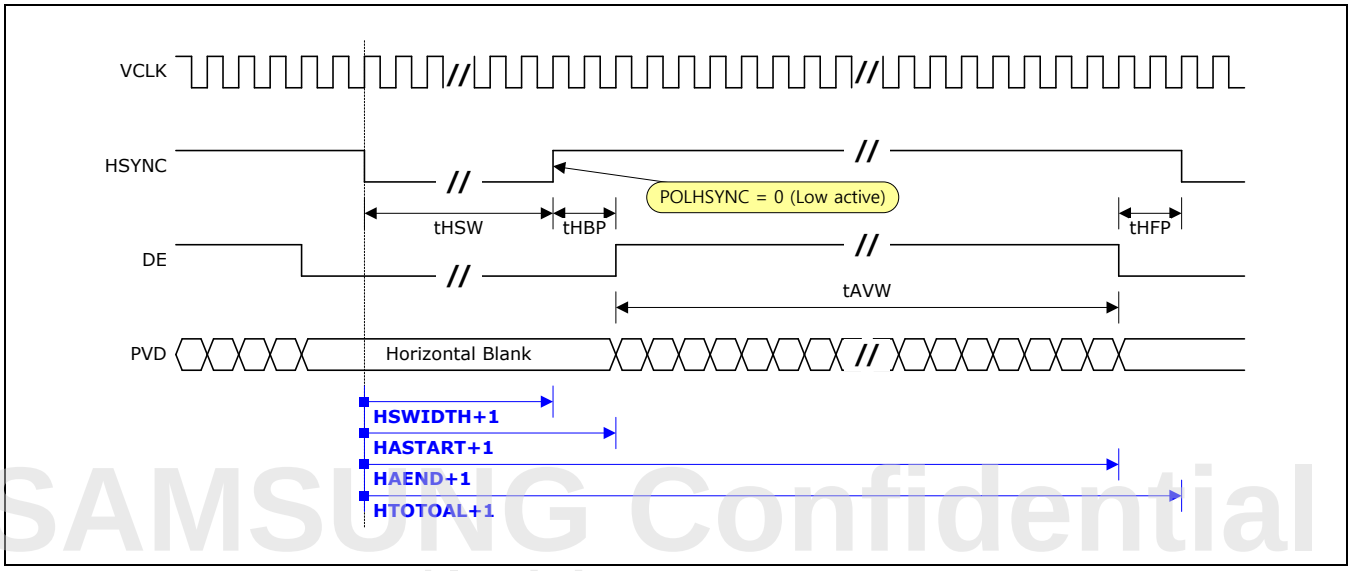


Figure 34-8 Horizontal Timing

Each symbol in the above figure is described in *Table 34-7*.

Table 34-7 Horizontal Timing Symbols

Symbol	Brief	Remark
tHSW	Horizontal Sync Width	Number of VCLKs in the section where the horizontal sync pulse is active
tHBP	Horizontal Back Porch	Number of VCLKs in a section from the end point of the horizontal sync pulse to the start point of the horizontal active
tHFP	Horizontal Front Porch	Number of VCLKs in a section from the end point of the horizontal active to the start point of the horizontal sync pulse
tAVW	Active Video Width	Number of VCLKs in a horizontal active section

The horizontal timing setting registers are HSWIDTH, HASTART, HAEND and HTOTAL and each register setting is described in *Table 34-8*. Each unit of the registers is based on VCLK and each value is set as "total number – 1".

Table 34-8 Horizontal Timing Registers

Register	Formula	Remark
HSWIDTH	tHSW – 1	Number of VCLKs in a section from the start point of the horizontal sync pulse to the end point of the horizontal sync pulse – 1
HASTART	tHSW + tHBP – 1	Number of VCLKs in a section from the start point of the horizontal sync pulse to the start point of the horizontal active – 1
HAEND	tHSW + tHBP + tAVW – 1	Number of VCLKs in a section from the start point of the horizontal sync pulse to the end point of the horizontal active – 1
HTOTAL	tHSW + tHBP + tAVW + tHFP – 1	Number of VCLKs in a section from the start point of the horizontal sync pulse to the start point of the next horizontal sync pulse – 1

The POLHSYNC is used to change the polarity of the HSYNC signal to be output to the outside. The horizontal sync pulse is low active when the POLHSYNC is "0", while the horizontal sync pulse is high active when the POLHSYNC is "1". The polarity of the Data Enable (DE) signal to be output to the outside cannot be changed and the section that outputs valid data comes into high state.

34.4.3.2 Vertical Timing Interface

The VSYNC signal is used for the Vertical Sync. The vertical timing consists of tVSW, tVBP, tVFP and tAVH as shown in *Figure 34-9*. In addition, the relation between the Vertical Sync and the Horizontal Sync is established by tVSSO and tVSEO.

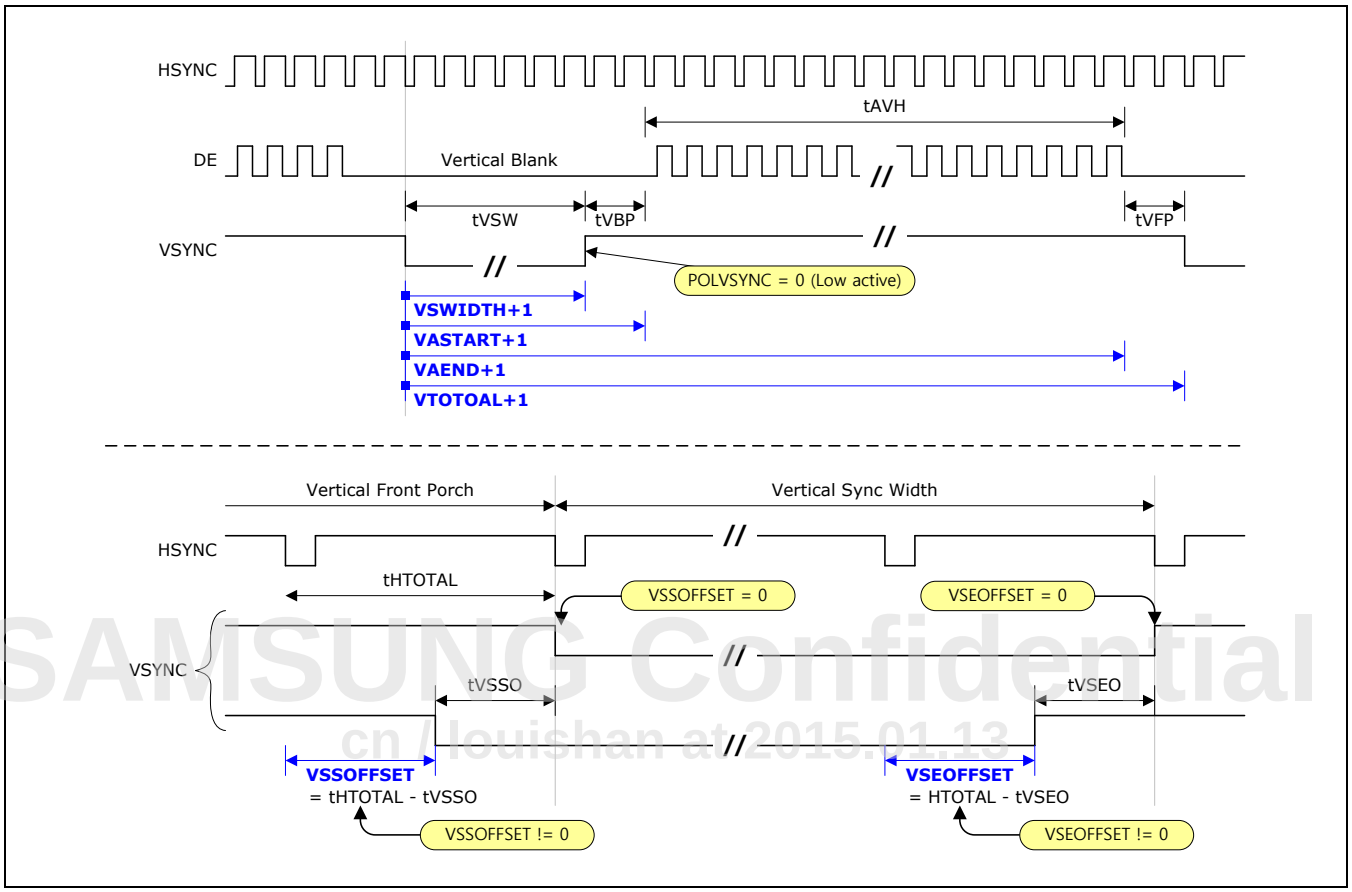


Figure 34-9 Vertical Timing

Each symbol in the above figure is described in *Table 34-9*.

Table 34-9 Vertical Timing Symbols

Symbol	Brief	Remark
tVSW	Vertical Sync Width	Number of lines in the section where the vertical sync pulse is active
tVBP	Vertical Back Porch	Number of lines in the section from the end point of the vertical sync pulse to the start point of the next vertical active
tVFP	Vertical Front Porch	Number of lines in the section from the end point of the vertical active to the start point of the vertical sync pulse
tAVH	Active Video Height	Number of lines in the vertical active section
tHTOTAL	Horizontal Total	Number of total VCLKs in a horizontal cycle where the horizontal active section and the horizontal blank section are added
tVSSO	Vertical Sync Start Offset	Number of VCLKs in a section from the start point of the vertical sync pulse to the start point of the horizontal sync pulse
tVSEO	Vertical Sync End Offset	Number of the VCLKs in a section from the end point of the horizontal sync pulse to the start point of the horizontal sync pulse

The vertical timing setting registers are VSWIDTH, VASTART, VAEND and VTOTAL and each register setting is described in *Table 34-10*. The units of VSWIDTH, VASTART, VAEND and VTOTAL are based on the horizontal lines and their values are set as total number – 1. The units of VSSOFFSET and VSEOFFSET are based on the VCLK.

Table 34-10 Vertical Timing Registers

Register	Formula	Remark
VSWIDTH	tVSW – 1	Number of lines in a section from the start point of the vertical sync pulse to the end point of the vertical sync pulse – 1
VASTART	tVSW + tVBP – 1	Number of VCLKs in a section from the start point of the vertical sync pulse to the start point of the vertical active – 1
VAEND	tVSW + tVBP + tAVH – 1	Number of lines in a section from the start point of the vertical sync pulse to the end point of the vertical active – 1
VTOTAL	tVSW + tVBP + tAVH + tVFP – 1	Number of lines in a section from the start point of the vertical sync pulse to the next point of the vertical sync pulse – 1
VSSOFFSET	If tVSSO is 0 then 0, else tHTOTAL – tVSSO	Number of VCLKs in a section from the start point of the last horizontal sync pulse in the Vertical Front Porch to the start point of the vertical sync pulse. If, however, VSSOFFSET is equal to tHTOTAL, the value is set as "0".
VSEOFFSET	If tVSEO is 0 then 0, else tHTOTAL – tVSEO	Number of VCLKs in a section from the start point of the last horizontal sync pulse in the Vertical Front Porch to the start point of the vertical sync pulse. If, however, VSEOFFSET is equal to tHTOTAL, the value is set as "0".

The*POLVSYNC* is used to change the polarity of the VSYNC signal to be output to the outside. The vertical sync pulse is low active when the POLVSYNC is "0", while the vertical sync pulse is high active when the POLVSYNC is "1".

34.4.3.3 AC Timing

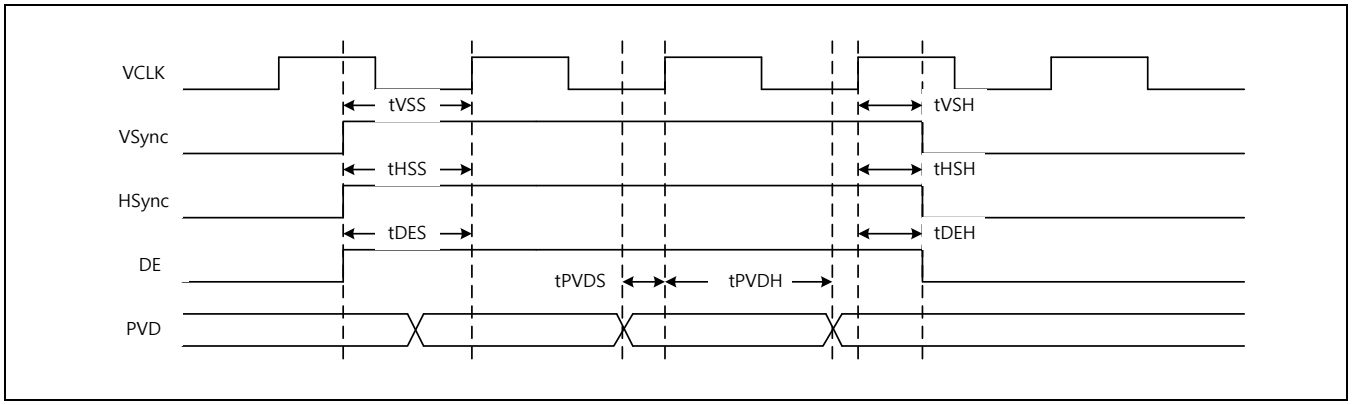


Figure 34-10 Vertical Timing

Condition: VCLK 40 MHz (25 ns)

Table 34-11 Sync Timing Symbols

Description	Symbol	Min	Max	Unit
VSync setup time	tVSS	12.13	–	ns
VSync hold time	tVSH	12.28	–	ns
HSync setup time	tHSS	12.27	–	ns
HSync hold time	tHSH	12.26	–	ns
DE setup time	tDES	12.1	–	ns
DE hols time	tDEH	12.4	–	ns
PVD setup time	tPVDS	8.8	–	ns
PVD hold time	tPVDH	12.87	–	ns

34.4.3.4 UPSCALER (Only Secondary Display)

UPSCALER performs the function of horizontal bilinear filter upscale MLC OUT Layer. It is selectable whether to scale with UPSCALEENB Setting.

UPSCALEENB Setting:

UPSCALE = (MLCScreenWidth – 1) × (1<<11) / (destination width – 1)

34.4.3.5 Embedded Sync

The ITU-R BT.656 output does not need the separate Sync Signal pin to transmit signals to the outside. The Sync information is transmitted along with data via a data pin. At this time, the Sync information is inserted as a separate code before the start point of the valid data (SAV) and after the end point of the valid data (EAV). The Sync information included in data is as shown in *Figure 34-11*.

CB359	Y718	CR359	Y719	FF	00	00	CODE	Blank	FF	00	00	CODE	CB0	Y0	CR0	Y1
				EAV					SAV							

Figure 34-11 Data stream format with SAV/EAV

The SAV and EAV consist of [FF, 00, 00, CODE]. Each of the SAV and EAV codes contains Field (F), VSYNC(V) and HSYNC(H) data and each code is composed as follows:

Table 34-12 Embedded Sync Code

Bit		7	6	5	4	3	2	1	0	Hex	Brief Description
Function		1	F	V	H	P3	P2	P1	P0		
(FVH)	0	1	0	0	0	0	0	0	0	80h	SAV of odd field
	1	1	0	0	1	1	1	0	1	9Dh	EAV of odd field
	2	1	0	1	0	1	0	1	1	ABh	SAV of odd blank
	3	1	0	1	1	0	1	1	0	B6h	EAV of odd blank
	4	1	1	0	0	0	1	1	1	C7h	SAV of even field
	5	1	1	0	1	1	0	1	0	DAh	EAV of even field
	6	1	1	1	0	1	1	0	0	ECh	SAV of even blank
	7	1	1	1	1	0	0	0	1	F1h	EAV of even blank

- F: Field select
  - 0 = odd field
  - 1 = even field
- V: Vertical blanking
  - 0 = Active
  - 1 = blank
- H: SAV/EAV
  - 0 = SAV
  - 1 = EAV
- Parity: P3 = V xor H, P2 = F xor H, P1 = F xor V, P0 = F xor V xor H

In the ITU-R BT.656 format, SAV/EAV codes are inserted in data by setting the SEAVENB as "1". However, since the SAV/EAV codes are transmitted via a data pin, the range of the data should be restricted, to distinguish the codes from the data. Users can restrict the data range by using YCRANGE. *Figure 34-12* shows that the result of the color space conversion changing RGB data to YCbCr data varies depending on YCRANGE.

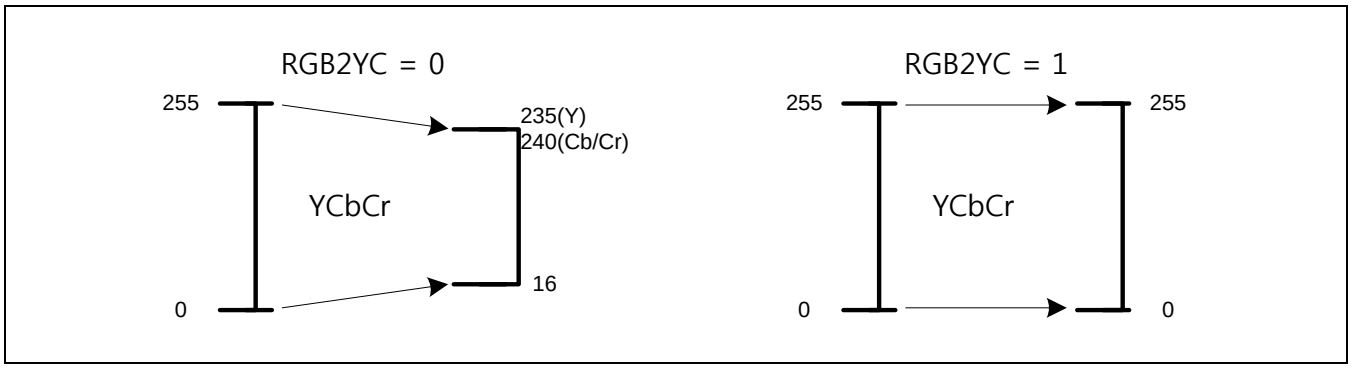


Figure 34-12 Y/C Clip

If YCRANGE is set as "0", a Y value between 0 and 15 is changed to 16 and a Y value between 236 and 255 is changed to 235. In a similar way, Cb/Cr values between 0 and 15 are changed to 16 and Cb/Cr values between 241 and 255 are changed to 240. If YCRANGE is set as "1", all Y/Cb/Cr values are bypassed.

34.4.4 Scan Mode

The sync generator supports interlace display as well as progressive display. The Scan mode is determined by SCANMODE. If SCANMODE is "0", the sync generator operates in progressive scan mode. If SCANMODE is "1", the sync generator operates in interlaced scan mode. In interlaced scan mode, the different vertical timing interfaces can be set in the odd and even fields separately. The odd field display and the progressive display share same registers and registers for the even field display exists separately. Registers to create vertical timing in accordance with the scan mode is listed in *Table 34-13*.

Table 34-13 Registers Relative to Scan Mode

SCANMODE	Scan Mode		Registers
0	Progressive		VTOTAL, VSWIDTH, VASTART, VAEND, VSSOFFSET, VSEOFFSET
1	Interlace	Odd field	
		Even field	EVTOTAL, EVSWIDTH, EVASTART, EVAEND, EVSSOFFSET, EVSEOFFSET

34.4.5 Delay

The pixel data is more delayed than the final output sync signal due to the processing in the sync generator. Therefore, users should delay Sync signal output to synchronize the Sync signals with the pixel data. When the Sync generator processes data, 4-clock is consumed for RGB data and 6-clock is consumed for YCbCr data. Therefore, for synchronization between Sync signals and data, the output of the Sync signals should be delayed. In RGB format and ITU-R BT.601A format with the same VCLK and VCLK2, delays of 4-clock and 6-clock should be set in each format, separately. In the MGRB and the ITU-R BT.656/601B formats, where the VCLK2 is twice the VCLK, delays of 8-clock and 12-clock should be set in each format, separately.

Table 34-14 Default Delay Value

Unit: VCLK2

Format	VCLK2 : VCLK	DELAYRGB	DELAYHS, DELAYVS, DELAYDE
RGB	1 : 1	0	Primary TFT:7 Primary STN: 8 Secondary: 7
MRGB	2 : 1	0	Primary TFT: 14 Secondary: 14
ITU-R BT.601A	1 : 1	0	6
ITU-R BT.656, ITU-R BT.601B	2 : 1	0	12

34.4.6 Interrupt

The DPC can generate an interrupt whenever VSYNC occurs.

Interrupt invokes each vertical Sync when TFT LCD Progressive operation. Interrupt invokes each 16 vertical sync when STN LCD Progressive operation. Interrupt invokes each EVEN field (2 vertical sync) when interlace operation. The DPC sets INTPEND as "1" if VSYNC occurs and notifies the interrupt generation to the Interrupt controller if the INTENB is "1". Therefore, users can acknowledge the generation of VSYNC via polling by using the status of the INTPEND regardless of the generation of interrupts. The INTPEND is cleared by writing "1" to it.

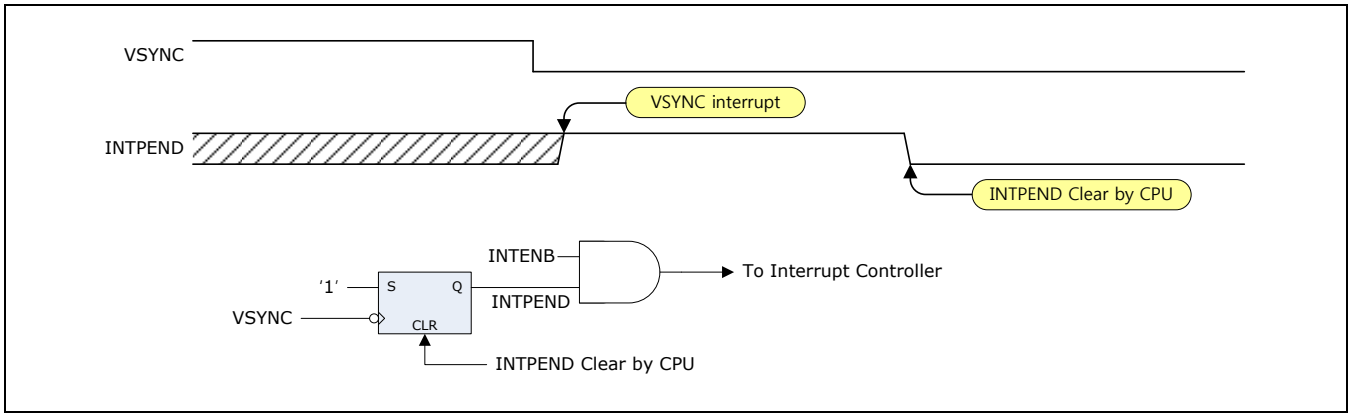


Figure 34-13 Interrupt Block Diagram and Timing

34.4.7 MPU (i80) Type Sync Signals

The sync generator can create signals for MPU LCD interface (i80). MPU LCD interface's signals are consists of nCS (Chip Select), RS (Register Select), nWR (Write), nRD(Read), and In/Out Data. MPU LCD interface has 4 types of accesses.

Table 34-15 i80 Access Types

Signals	Access Types	Description	Register Address
RS = 0 nWR	Address Write	Write index to IR	[15:0]: C010_2984 [23:16]: C010_2988
RS = 0 nRD	Status Read	Read Internal Status	[23:16]: C010_298C [15:0]: C010_2994
RS = 1 nWR	Data Write (or Graphic Data Write)	Write to Control Register and GRAM	[15:0]: C010_2984 [23:16]: C010_2990
RS = 1 nRD	Data Read	Read from GRAM	[23:16]: C010_2990 [15:0]: C010_2994

S5P4418 has register for communicating with external devices, and it supports 4 types of MPU interface format. In the case of "writing", lower 16 bits need to be written to C010_2984 address followed by writing upper 8 bits to C010_2990*address. In the case of "reading", upper 8 bits need to be read from *C010_298C address followed by reading lower 16 bits from C010_2994 address. Actual communication with external devices is occurred when writing to C010_2990*address and reading from *C010_298C address.

To satisfy setup/hold timing of external devices, setting appropriate parameters, which include setup counter, access counter and hold counter, need to be set in DPCMPUTIME0, DPCMPUTIME1registers. Following is the timing diagram of write operation.

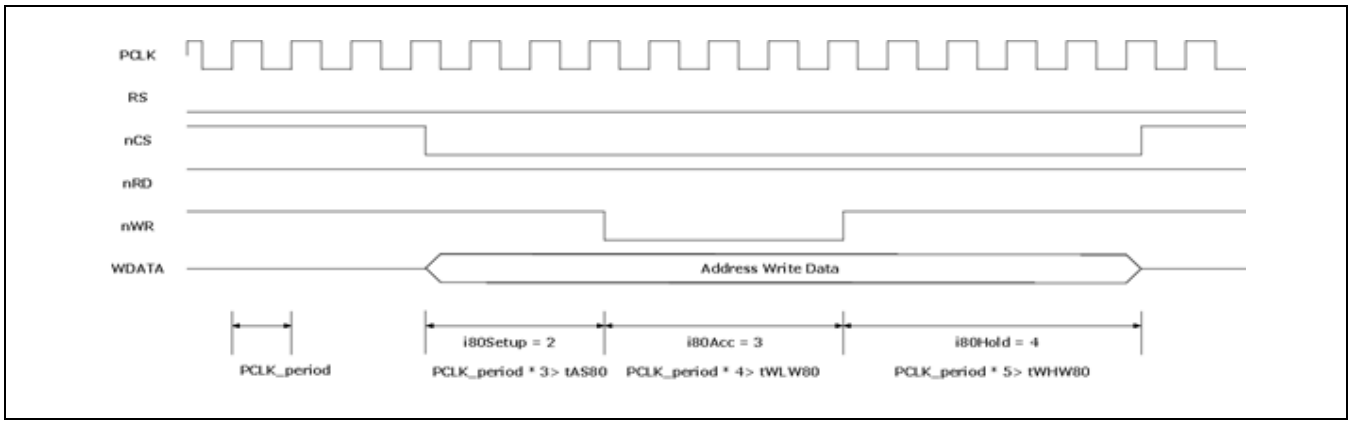


Figure 34-14 i80Address Write

S5P4418 can convert video sync signals to MPU i80 type by setting DPC to i80 mode. Note that VCLK_2 needs to be 2 times faster than VCLK for MPU i80. Following diagram describes video sync to MPU i80 conversion.

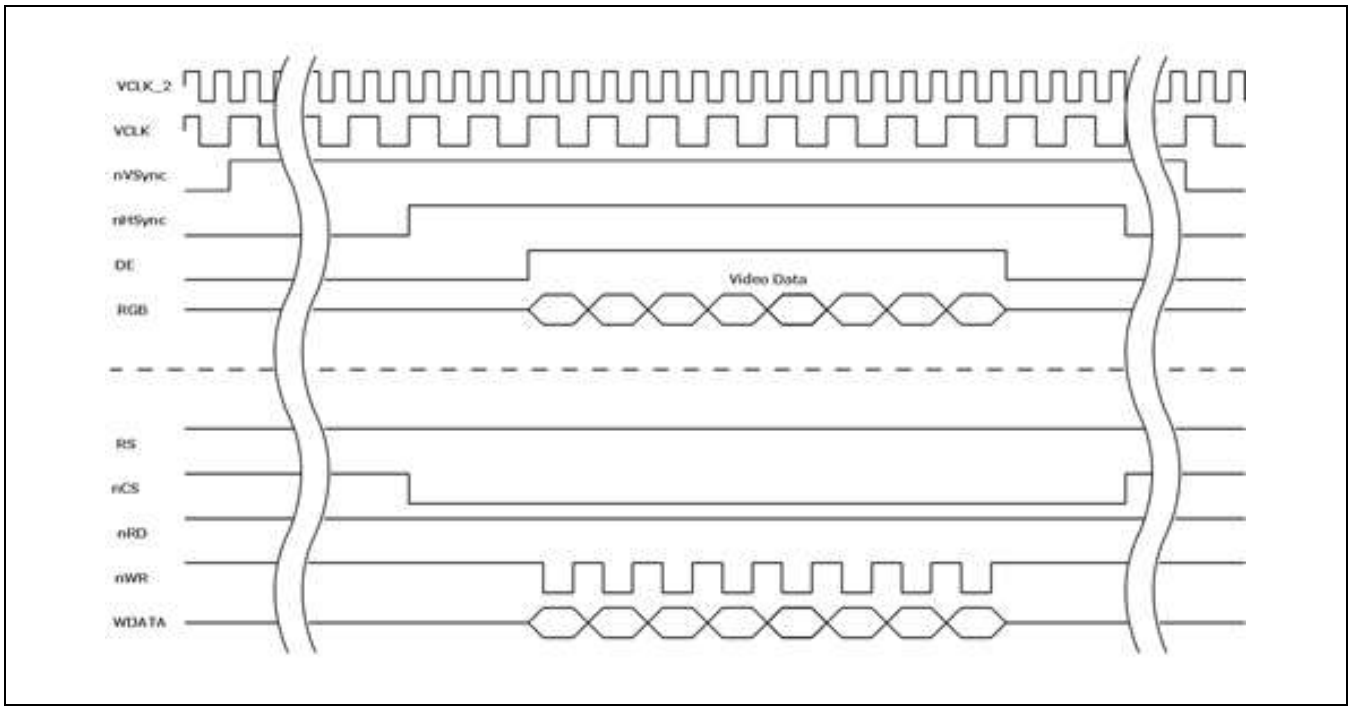


Figure 34-15 i80 Graphic Data Convert

S5P4418 has a "Command Buffer", which is used to send additional information during the VSYNC period.

34.4.8 Odd/Even Field Flag

S5P4418 DPC provides DPCRGBSHIFT.FIELDFLAG register which indicates whether currently being displayed frame is odd or even frame.

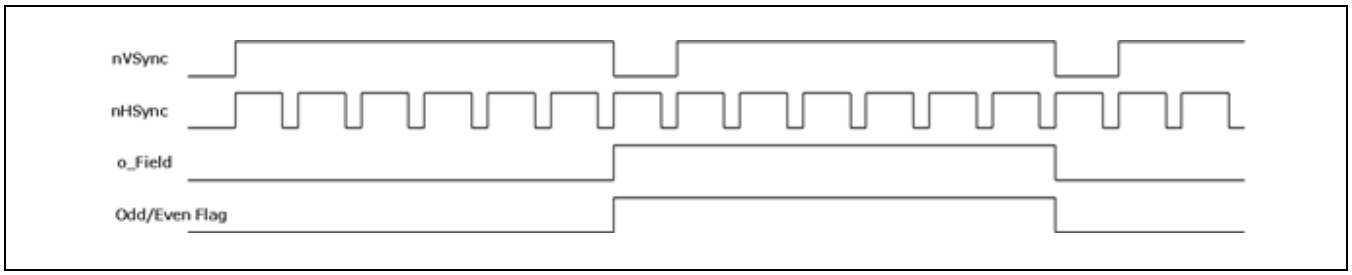


Figure 34-16 Odd/Even Flag

34.5 Register Description

34.5.1 Register Map Summary

- Base Address: 0xC010_2000

Register	Offset	Description	Reset Value
RSVD	0x800h to 0x8FFh/ 0xC70h to 0xCFFh	Reserved	0x0000_0000
DPCHTOTAL	0x8F8h/0xCF8h	DPC Horizontal Total Length Register	0x0000_0000
DPCHSWIDTH	0x8FCh/0xCFCh	DPC Horizontal Sync Width Register	0x0000_0000
DPCHASTART	0x900h/0xD00h	DPC Horizontal Active Video START Register	0x0000_0000
DPCHAEND	0x904h/0xD04h	DPC Horizontal Active Video End Register	0x0000_0000
DPCVTOTAL	0x908h/0xD08h	DPC Vertical Total Length Register	0x0000_0000
DPCVSWIDTH	0x90Ch/0xD0Ch	DPC Vertical Sync Width Register	0x0000_0000
DPCVASTART	0x910h/0xD10h	DPC Vertical Active Video START Register	0x0000_0000
DPCVAEND	0x914h/0xD14h	DPC Vertical Active Video End Register	0x0000_0000
DPCCTRL0	0x918h/0xD18h	DPC Control 0 Register	0x0000_0000
DPCCTRL1	0x91Ch/0xD1Ch	DPC Control 1 Register	0x0000_0000
DPCEVTOTAL	0x920h/0xD20h	DPC Even Field Vertical Total Length Register	0x0000_0000
DPCEVSWIDTH	0x924h/0xD24h	DPC Even Field Vertical Sync Width Register	0x0000_0000
DPCEVASTART	0x928h/0xD28h	DPC Even Field Vertical Active Video START Register	0x0000_0000
DPCEVAEND	0x92Ch/0xD2Ch	DPC Even Field Vertical Active Video End Register	0x0000_0000
DPCCTRL2	0x930h/0xD30h	DPC Control 2 Register	0x0000_0000
DPCVSEOFFSET	0x934h/0xD34h	DPC Vertical Sync End Offset Register	0x0000_0000
DPCVSSOFFSET	0x938h/0xD38h	DPC Vertical Sync START Offset Register	0x0000_0000
DPCEVSEOFFSET	0x93Ch/0xD3Ch	DPC Even Field Vertical Sync End Offset Register	0x0000_0000
DPCEVSSOFFSET	0x940h/0xD40h	DPC Even Field Vertical Sync START Offset Register	0x0000_0000
DPCDELAY0	0x944h/0xD44h	DPC Sync Delay 0 Register	0x0000_0000
DPUPSCALECON0	Not available/ 0xD48h	DPC Sync UPScale control register 0	0x0000_0000
DPUPSCALECON1	Not available/ 0xD4Ch	DPC Sync UPScale control register 1	0x0000_0000
RSVD	0x94Ch to 0x977h/ 0xD4Ch to 0xD77h	Reserved	0x0000_0000
DPCDELAY1	0x978h/0xD78h	DPC Sync DELAY CONTROL register 1	0x0000_0000
DPCmputime0	0x97Ch/0xD7Ch	DPC MPU i80 timing CONTROL register 0	0x0000_0000
DPCmputime1	0x980h/ Not available	DPC MPU i80 timing CONTROL register 1	0x0000_0000
dpcmpuwrdatal	0x984h/ Not available	DPC MPU i80 low bit Write data register	-
dpcmpuindex	0x988h/	DPC MPU i80 index Write data register	-

Register	Offset	Description	Reset Value
	Not available		
dpcmpustatus	0x98Ch/ Not available	DPC MPU i80 status read data register	0x0000_0000
dpcmPUDatah	0x990h/ Not available	DPC MPU i80 READ/WRITE data register	0x0000_0000
dpcmpurdatal	0x994h/ Not available	DPC MPU i80 low bit read data register	0x0000_0000
RSVD	0x998h to 0x99Bh/ 0xD98h to 0xD9Bh	Reserved	0x0000_0000
dpccmdbufferrdatal	0x99Ch/ Not available	DPC MPU i80 command buffer low bit data register	-
dpccmdbufferrdataH	0x9A0h/ Not available	DPC MPU i80 command buffer high bit data register	-
DPCmputime1	0x9A4h/0xDA4h	DPC MPU i80 timing CONTROL register 1	0x0000_0000
DPCpadposition0	0x9A8h/ Not available	DPC PAD LOCATION CONTROL register 0	0x0000_0000
DPCpadposition1	0x9ACh/ Not available	DPC PAD LOCATION CONTROL register 1	0x0000_0000
DPCpadposition2	0x9B0h/ Not available	DPC PAD LOCATION CONTROL register 2	0x0000_0000
DPCpadposition3	0x9B4h/ Not available	DPC PAD LOCATION CONTROL register 3	0x0000_0000
DPCpadposition4	0x9B8h/ Not available	DPC PAD LOCATION CONTROL register 4	0x0000_0000
DPCpadposition5	0x9BCh/ Not available	DPC PAD LOCATION CONTROL register 5	0x0000_0000
DPCpadposition6	0x9C0h/ Not available	DPC PAD LOCATION CONTROL register 6	0x0000_0000
DPCpadposition7	C010_0x9C4h/ Not available	DPC PAD LOCATION CONTROL register 7	0x0000_0000
DPCRGBMASK0	0x9C8h/Not available	DPC PAD LOCATION MASK register 0	0x0000_0000
DPCRGBMASK1	0x9CCh/ Not available	DPC PAD LOCATION MASK register 1	0x0000_0000
DPCRGBSHIFT	0x9D0h/ Not available	DPC RGB SHIFT CONTROL register	0x0000_0000
dpcdataflush	0x9D4h/ Not available	DPC MPU i80 command buffer FLUSH Control register	-
RSVD	0x9D8h to 0xBCFh/ 0xDD8h to 0xFCFh	Reserved	0x0000_0000
DPCCLKENB	0xBC0h/0xFC0h	DPC Clock Generation Enable Register	0x0000_0000
DPCCLKGEN0L	0xBC4h/0xFC4h	DPC Clock Generation Control 0 Low Register	0x0000_0000

Register	Offset	Description	Reset Value
DPCCLKGEN0h	0xBC8h/0xFC8h	DPC Clock Generation Control 0high Register	0x0000_0000
DPCCLKGEN1L	0xBCCh/0xFCCh	DPC Clock Generation Control 1 low Register	0x0000_0000
DPCCLKGEN1h	0xBD0h/0xFD0h	DPC Clock Generation Control 1high Register	0x0000_0000

34.5.1.1 DPCHTOTAL

- Base Address: 0xC010_2000
- Address = Base Address + 0x8F8h, 0xCF8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
HTOTAL	[15:0]	RW	Specifies the number of total VCLK clocks for a horizontal line. • TFT or Video Encoder: HTOTAL = tHSW + tHBP + tHFP + tAVW – 1 • Color STN: HTOTAL = CL1HW + CL1ToCL2DLY + {(tAVWx 3)/BitWidth} × CPLCYCx2} – 1 • Monochrome STN: HTOTAL = CL1HW + CL1ToCL2DLY + {(tAVWx 1)/BitWidth} × CL2CYCx2} – 1	16'b0

34.5.1.2 DPCHSWIDTH

- Base Address: 0xC010_2000
- Address = Base Address + 0x8FCh, 0xCFCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
HSWIDTH	[15:0]	RW	TFT or Video Encoder: Specifies the number of VCLK clocks for the horizontal sync width. This value must be less than HASTART. • HSWIDTH = tHSW – 1 STN: CL1 Height Width HSWIDTH = CL1HW – 1	16'b0

34.5.1.3 DPCHASTART

- Base Address: 0xC010_2000
- Address = Base Address + 0x900h, 0xD00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
HASTART	[15:0]	RW	TFT or Video Encoder: Specifies the number of VCLK clocks from start of the horizontal sync to start of the active video. This value must be less than HAEND. • HASTART = tHSW + tHBP – 1 STN: Delay Cycle from posedge active of CL1 signal to CL2 posedge active. • HASTART = CL1ToCL2DLY	16'b0

34.5.1.4 DPCHAEND

- Base Address: 0xC010_2000
- Address = Base Address + 0x904h, 0xD04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
HAEND	[15:0]	RW	TFT or Video Encoder: Specifies the number of VCLK clocks from start of the horizontal sync to end of the active video. This value must be less than HTOTAL. • HAEND = tHSW + tHBP + tAVW – 1 STN: Active Width • HAEND = tAVW – 1	16'b0

34.5.1.5 DPCVTOTAL

- Base Address: 0xC010_2000
- Address = Base Address + 0x908h, 0xD08h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
VTOTAL	[15:0]	RW	Specifies the number of total lines for a frame or field. • TFT or Video Encoder: VTOTAL = tVSW + tVBP + tVFP + tAVH – 1 • STN: VTOTAL = BLANKLINE + tAVH – 1	16'b0

34.5.1.6 DPCVSWIDTH

- Base Address: 0xC010_2000
- Address = Base Address + 0x90Ch, 0xD0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
VSWIDTH	[15:0]	RW	TFT or Video Encoder: Specifies the number of lines for the vertical sync width. This value must be less than VASTART. When interlace mode, this value is used for odd field. • VSWIDTH = tVSW – 1 STN: Blank Line Number • VSWIDTH = BLANKLINE – 1	16'b0

34.5.1.7 DPCVASTART

- Base Address: 0xC010_2000
- Address = Base Address + 0x910h, 0xD10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
VASTART	[15:0]	RW	Specifies the number of lines from start of the vertical sync to start of the active video. This value must be less than VAEND. When interlace mode, this value is used for odd field. • VASTART = tVSW + tVBP – 1	16'b0

34.5.1.8 DPCVAEND

- Base Address: 0xC010_2000
- Address = Base Address + 0x914h, 0xD14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
VAEND	[15:0]	RW	Specifies the number of lines from start of the vertical sync to end of the active video. This value must be less than VTOTAL. When interlace mode, this value is used for odd field. • VAEND = tVSW + tVBP + tAVH – 1	16'b0

34.5.1.9 DPCCTRL0

- Base Address: 0xC010_2000
- Address = Base Address + 0x918h, 0xD18h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
DPCENB	[15]	RW	Enable/Disable the display controller (DPC). 0 = Disable 1 = Enable	1'b0
RSVD	[14:13]	RW	Reserved	2'b0
RGBMODE	[12]	RW	Specifies the output pixel format. 0 = YCbCr 1 = RGB	1'b0
INTENB	[11]	RW	Enable/Disable the VSYNC interrupt. The VSYNC interrupt will be issued at start of the VSYNC pulse. Therefore an interrupt will be occurred at every frame in progressive mode or at every field in interlace mode. 0 = Disable 1 = Enable	1'b0
INTPEND	[10]	RW	Indicates whether the VSYNC interrupt is pended or not. This bit is always operated regardless of INTENB bit. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0
SCANMODE	[9]	RW	Determines whether scan mode is progressive or interlace. 0 = Progressive scan mode 1 = Interlaced scan mode	1'b0
SEAVENB	[8]	RW	Enable/Disable SAV/EAV signal into the data. This is used for ITU-R BT.656 format. 0 = Disable embedded sync 1 = Enable embedded sync	1'b0
DELAYRGB	[7:4]	RW	Specifies the delay for RGB PAD output. The unit is VCLK2. Generally this value has 0 for normal operation.	4'b0
RSVD	[3]	R	Reserved	1'b0
POLFIELD	[2]	RW	Specifies the polarity of the internal field signal. 0 = Normal (Low is odd field) 1 = Inversion (Low is even field)	1'b0
POLVSYNC	[1]	RW	Specifies the polarity of the vertical sync output. This bit is only valid in case of primary display controller. 0 = Low active 1 = High active	1'b0
POLHSYNC	[0]	RW	Specifies the polarity of the horizontal sync output. This bit	1'b0

Name	Bit	Type	Description	Reset Value
			is only valid in case of primary display controller. 0 = Low active 1 = High active	

34.5.1.10 DPCCTRL1

- Base Address: 0xC010_2000
- Address = Base Address + 0x91Ch, 0xD1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
SWAPRB	[15]	RW	Swap Red and Blue component. This value is only valid when the output is RGB. This bit is only valid in case of primary display controller. 0 = RGB 1 = BGR	1'b0
RSVD	[14]	R	Reserved	1'b0
YCRANGE	[13]	RW	Determines the YUV range for RGB to YUV conversion. Write 0 set of Video Encoder output 0 = Y = 16 to 235, Cb/Cr = 16 to 240 1 = Y/Cb/Cr = 0 to 255	1'b0
RSVD	[12]	R	Reserved	1'b0
FORMAT	[11:8]	RW	Specifies the data output format. TFT or Video Encoder : 0 = RGB555 1 = RGB565 2 = RGB666 3 = RGB888 4 = MRGB555A 5 = MRGB555B 6 = MRGB565 7 = MRGB666 8 = MRGB888A 9 = MRGB888B 10 = ITU-R BT.656 or 601(8bit) 11 = Reserved 12 = ITU-R BT.601A 13 = ITU-R BT.601B(set YCORDER bit as "1") 14 = Reserved 15 = Reserved STN: 0 = Reserved 1 = 4096 Color 2 = Reserved 3 = 16 Gray Level Other = Reserved	4'b0

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved but this bit should be set to `0'	1'b0
YCORDER	[6]	RW	Specifies the data output order in case of ITU-R BT. 601B. 0 = Cb Y Cr Y 1 = Cr Y CbY	1'b0
BDITHER	[5:4]	RW	Specifies the dithering method of Blue component. This value is only valid in case of primary display controller. 0 = Bypass 1 = 4-bit dither 2 = 5-bit dither 3 = 6-bit dither	2'b0
GDITHER	[3:2]	RW	Specifies the dithering method of Green component. This value is only valid in case of primary display controller. 0 = Bypass 1 = 4-bit dither 2 = 5-bit dither 3 = 6-bit dither	2'b0
RDITHER	[1:0]	RW	Specifies the dithering method of Red component. This value is only valid in case of primary display controller. 0 = Bypass 1 = 4-bit dither 2 = 5-bit dither 3 = 6-bit dither	2'b0

34.5.1.11 DPCEVTOTAL

- Base Address: 0xC010_2000
- Address = Base Address + 0x920h, 0xD20h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
EVTOTAL	[15:0]	RW	Specifies the number of total lines for even field. This register is only used when interlace mode. • EVTOTAL = tEVSW + tEVBP + tEVFP + tEAVH – 1	16'b0

34.5.1.12 DPCEVSWIDTH

- Base Address: 0xC010_2000
- Address = Base Address + 0x924h, 0xD24h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
EVSWIDTH	[15:0]	RW	Specifies the number of lines for the vertical sync width of even field. This value must be less than EVASTART. This register is only used when interlace mode. • EVSWIDTH = tEVSW – 1	16'b0

34.5.1.13 DPCEVASTART

- Base Address: 0xC010_2000
- Address = Base Address + 0x928h, 0xD28h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
EVASTART	[15:0]	RW	Specifies the number of lines from start of the vertical sync to start of the active video when even field. This value must be less than EVAEND. This register is only used when interlace mode. • EVASTART = tEVSW + tEVBP – 1	16'b0

34.5.1.14 DPCEVAEND

- Base Address: 0xC010_2000
- Address = Base Address + 0x92Ch, 0xD2Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
EVAEND	[15:0]	RW	Specifies the number of lines from start of the vertical sync to end of the active video when even field. This value must be less than EVTOTAL. This register is only used when interlace mode. • EVAEND = tEVSW + tEVBP + tEAVH – 1	16'b0

34.5.1.15 DPCCTRL2

- Base Address: 0xC010_2000
- Address = Base Address + 0x930h, 0xD30h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
CL2CYC	[15:12]	RW	Sets STN LCD CL2 (Shift clock) Cycle (Unit: VCLK) CL2CYC = CL2CYC – 1	4'b0
RSVD	[11:10]	R	Reserved	2'b0
STNLCDBITWIDTH	[9]	RW	STN LCD Data Bus Bit Width. 0 = Reserved 1 = 8-bit Scan mode is applicable with Dual view mode set.	1'b0
LCDTYPE	[8:7]	RW	Declares External Display Device Type 0 = TFT or Video Encoder 1 = STN LCD 2 = Dual View mode (TFT or Video Encoder) 3 = Reserved	2'b0
RSVD	[6:5]	R	Reserved	2'b0
I80ENABLE	[4]	RW	Enable MPU i80 Mode. 0 = No i80 Mode 1 = i80 Mode Enable	1'b0
RSVD	[3]	R	Reserved	1'b0
INITPADCLK	[2]	RW	Initial Value of VCLK2 div 2. (for SRGB888)	1'b0
PADCLKSEL	[1:0]	RW	Specifies the PAD output clock. 0 = VCLK 1 = VCLK2 2 = VCLK2 div 2 (for SRGB888) 3 = Reserved	2'b0

34.5.1.16 DPCVSEOFFSET

- Base Address: 0xC010_2000
- Address = Base Address + 0x934h, 0xD34h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
VSEOFFSET	[15:0]	RW	Specifies the number of clocks from start of the horizontal sync to end of the vertical sync, where the horizontal sync is last one in the vertical sync. If this value is 0 then end of the vertical sync synchronizes with start of the horizontal sync which is new one in the vertical back porch. This value has to be less than HTOTAL. When interlace mode, this value is used for odd field. • If tVSEO is 0 then VSEOFFSET = 0, else VSEOFFSET = HTOTAL – tVSEO	16'b0

34.5.1.17 DPCVSSOFFSET

- Base Address: 0xC010_2000
- Address = Base Address + 0x938h, 0xD38h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
VSSOFFSET	[15:0]	RW	Specifies the number of clocks from start of the horizontal sync to start of the vertical sync, where the horizontal sync is last one in the vertical front porch. If this value is 0 then start of the vertical sync synchronizes with start of the horizontal sync which is new one in the vertical sync. This value has to be less than HTOTAL. When interlace mode, this value is used for odd field. • If tVSSO is 0 then VSSOFFSET = 0, else VSSOFFSET = HTOTAL – tVSSO	16'b0

34.5.1.18 DPCEVSEOFFSET

- Base Address: 0xC010_2000
- Address = Base Address + 0x93Ch, 0xD3Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
EVSEOFFSET	[15:0]	RW	Specifies the number of clocks from start of the horizontal sync to end of the vertical sync, where the horizontal sync is last one in the vertical sync. If this value is 0 then end of the vertical sync synchronizes with start of the horizontal sync which is new one in the vertical back porch. This value has to be less than HTOTAL and is used for even field. • If tEVSEO is 0 then EVSEOFFSET = 0, else EVSEOFFSET = HTOTAL – tEVSEO	16'b0

34.5.1.19 DPCEVSSOFFSET

- Base Address: 0xC010_2000
- Address = Base Address + 0x940h, 0xD40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
EVSSOFFSET	[15:0]	RW	Specifies the number of clocks from start of the horizontal sync to start of the vertical sync, where the horizontal sync is last one in the vertical front porch. If this value is 0 then start of the vertical sync synchronizes with start of the horizontal sync which is new one in the vertical sync. This value has to be less than HTOTAL and is used for even field. • If tEVSSO is 0 then EVSSOFFSET = 0, else EVSSOFFSET = HTOTAL – tEVSSO	16'b0

34.5.1.20 DPCDELAY0

- Base Address: 0xC010_2000
- Address = Base Address + 0x944h, 0xD44h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved	20'b0
PADPOLFIELD	[15]	RW	Specifies the polarity of the PAD's field signal. 0 = Normal (Low is odd field) 1 = Inversion (Low is even field)	1'b0
RSVD	[14]	R	Reserved	1'b0
DELAYVS	[13:8]	RW	Specifies delay value of the vertical sync/FRM output. This value depends on the output format. The unit is VCLK2.	4'b0
DELAYHS	[5:0]	RW	Specifies delay value of the horizontal sync/CP1 output. This value depends on the output format. The unit is VCLK2.	4'b0

34.5.1.21 DPUPSCALECON0

- Base Address: 0xC010_2000
- Address = Base Address + Not available, 0xD48h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
UPSCALEL	[15:8]	RW	Specifies the ratio for the horizontal scale. The formula to calculate this value is as follows: When FILTERENB is 1 and the destination width is wider than the source width: • UPSCALE = (source width-1) × (1<<11) / (destination width – 1) • UPSCALEL = UPSCALE[7:0]	8'b0
RSVD	[7:1]	R	Reserved	7'b0
UPSCALERENB	[0]	RW	Decide whether to enlarge Source Image horizontal width. 0 = Scaler Disable 1 = Scaler Enable	1'b0

34.5.1.22 DPUPSCALECON1

- Base Address: 0xC010_2000
- Address = Base Address + Not available, 0xD4Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
UPSCALEH	[14:0]	RW	Specifies the ratio for the horizontal scale. The formula to calculate this value is as follows: When FILTERENB is 1 and the destination width is wider than the source width: • UPSCALE = (MLCScreenwidth-1) × (1<<11) / (destination width – 1) • UPSCALEH = UPSCALE[22:8]	15'b0

34.5.1.23 DPCDELAY1

- Base Address: 0xC010_2000
- Address = Base Address + 0x978h, 0xD78h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:6]	R	Reserved	26'b0
DELAYDE	[5:0]	RW	Specifies delay value of DE (data enable)/CP2 output. This value depends on the output format. The unit is VCLK2.	6'b0

34.5.1.24 DPCmputime0

- Base Address: 0xC010_2000
- Address = Base Address + 0x97Ch, 0xD7Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
i80holdtime	[15:8]	RW	Specifies value of MPU i80 hold time config. The unit is PCLK.	8'b0
i80setuptime	[7:0]	RW	Specifies value of MPU i80 setup time cconfig. The unit is PCLK.	8'b0

34.5.1.25 DPCmputime1

- Base Address: 0xC010_2000
- Address = Base Address + 0x980h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
i80acctime	[7:0]	RW	Specifies value of MPU i80 hold time config. The unit is PCLK.	8'b0

34.5.1.26 dpcmpuwrdatal

- Base Address: 0xC010_2000
- Address = Base Address + 0x984h, Not available, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
mpuwrdatal	[15:0]	W	Write low 16-bit write data for MPU i80. Users must write this register first for MPU i80 access via CPU.	-

34.5.1.27 dpcmpuindex

- Base Address: 0xC010_2000
- Address = Base Address + 0x988h, Not available, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	16'b0
mpuindex	[7:0]	W	Write high 8-bit write data for MPU i80 index access. (RS = 0)	-

34.5.1.28 dpcmpustatus

- Base Address: 0xC010_2000
- Address = Base Address + 0x98Ch, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	16'b0
mpustatus	[7:0]	R	Read high 8-bit write data1 for MPU i80 index access. (RS = 0)	16'b0

34.5.1.29 dpcmPUDatah

- Base Address: 0xC010_2000
- Address = Base Address + 0x990h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	16'b0
mpuDATAH	[7:0]	RW	Read/Write high 8-bit write data1 for MPU i80 data access. (RS = 1)	16'b0

34.5.1.30 dpcmpurdatal

- Base Address: 0xC010_2000
- Address = Base Address + 0x994h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
mpuwrdatal	[15:0]	R	Read low 16-bit write data for MPU i80. Users must read this register after reading DPCMPUSTATUS or DPCMPUDATAH for MPU i80 access via CPU.	16'b0

34.5.1.31 dpccmdbufferrdatal

- Base Address: 0xC010_2000
- Address = Base Address + 0x99Ch, Not available, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
MPUcmdbufl	[15:0]	W	Write low 16-bit write data for MPU i80. Users must write this register first for MPU i80 command buffer	-

34.5.1.32 dpccmdbufferrdataH

- Base Address: 0xC010_2000
- Address = Base Address + 0x9A0h, Not available, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
MPUcmdbufh	[7:0]	W	Write high 8-bit write data for MPU i80.	-

34.5.1.33 DPCmputime1

- Base Address: 0xC010_2000
- Address = Base Address + 0x9A4h, 0xDA4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:6]	R	Reserved	26'b0
POLDE	[5]	RW	Specifies the polarity of the Data Enable output. 0 = Normal (High is data enable) 1 = Inversion (High is data enable)	1'b0
POLnCS	[4]	RW	Specifies the polarity of the nCS signal. (MPU i80 type, primary only) 0 = Normal (Low is chip select) 1 = Inversion (High is chip select)	1'b0
POLnWR	[3]	RW	Specifies the polarity of the nWR signal. (MPU i80 type, primary only) 0 = Normal (neg-edge trigger) 1 = Inversion (pos-edge trigger)	1'b0
POLnRD	[2]	RW	Specifies the polarity of the nRD signal. (MPU i80 type, primary only) 0 = Normal (neg-edge trigger) 1 = Inversion (pos-edge trigger)	1'b0
POLRS	[1]	RW	Specifies the polarity of the RS signal. (MPU i80 type, primary only) 0 = Normal(Low is index access) 1 = Inversion (High is index access)	1'b0
RSVD	[0]	RW	Must be Set 1'b0	1'b0

34.5.1.34 DPCpadposition0

- Base Address: 0xC010_2000
- Address = Base Address + 0x9A8h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc2	[14:10]	RW	Select a location to go in the video data number 2 outputs. (active when i80 mode)	5'b 0
padloc1	[9:5]	RW	Select a location to go in the video data number 1 outputs. (active when i80 mode)	5'b 0
padloc0	[4:0]	RW	Select a location to go in the video data number 0 outputs. (active when i80 mode)	5'b 0

34.5.1.35 DPCpadposition1

- Base Address: 0xC010_2000
- Address = Base Address + 0x9ACh, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc5	[14:10]	RW	Select a location to go in the video data number 5 outputs. (active when i80 mode)	5'b 0
padloc4	[9:5]	RW	Select a location to go in the video data number 4 outputs. (active when i80 mode)	5'b 0
padloc3	[4:0]	RW	Select a location to go in the video data number 3 outputs. (active when i80 mode)	5'b 0

34.5.1.36 DPCpadposition2

- Base Address: 0xC010_2000
- Address = Base Address + 0x9B0h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc8	[14:10]	RW	Select a location to go in the video data number 8 outputs. (active when i80 mode)	5'b 0
padloc7	[9:5]	RW	Select a location to go in the video data number 7 outputs. (active when i80 mode)	5'b 0
padloc6	[4:0]	RW	Select a location to go in the video data number 6 outputs. (active when i80 mode)	5'b 0

34.5.1.37 DPCpadposition3

- Base Address: 0xC010_2000
- Address = Base Address + 0x9B4h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc11	[14:10]	RW	Select a location to go in the video data number 11 outputs. (active when i80 mode)	5'b 0
padloc10	[9:5]	RW	Select a location to go in the video data number 10 outputs. (active when i80 mode)	5'b 0
padloc9	[4:0]	RW	Select a location to go in the video data number 9 outputs. (active when i80 mode)	5'b 0

34.5.1.38 DPCpadposition4

- Base Address: 0xC010_2000
- Address = Base Address + 0x9B8h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc14	[14:10]	RW	Select a location to go in the video data number 14 outputs. (active when i80 mode)	5'b 0
padloc13	[9:5]	RW	Select a location to go in the video data number 13 outputs. (active when i80 mode)	5'b 0
padloc12	[4:0]	RW	Select a location to go in the video data number 12 outputs. (active when i80 mode)	5'b 0

34.5.1.39 DPCpadposition5

- Base Address: 0xC010_2000
- Address = Base Address + 0x9BCh, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc17	[14:10]	RW	Select a location to go in the video data number 17 outputs. (active when i80 mode)	5'b 0
padloc16	[9:5]	RW	Select a location to go in the video data number 16 outputs. (active when i80 mode)	5'b 0
padloc15	[4:0]	RW	Select a location to go in the video data number 15 outputs. (active when i80 mode)	5'b 0

34.5.1.40 DPCpadposition6

- Base Address: 0xC010_2000
- Address = Base Address +0x9C0h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc20	[14:10]	RW	Select a location to go in the video data number 20 outputs. (active when i80 mode)	5'b 0
padloc19	[9:5]	RW	Select a location to go in the video data number 19 outputs. (active when i80 mode)	5'b 0
padloc18	[4:0]	RW	Select a location to go in the video data number 18 outputs. (active when i80 mode)	5'b 0

34.5.1.41 DPCpadposition7

- Base Address: 0xC010_2000
- Address = Base Address +0x9C4h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:15]	R	Reserved	17'b0
padloc23	[14:10]	RW	Select a location to go in the video data number 23 outputs. (active when i80 mode)	5'b0
padloc22	[9:5]	RW	Select a location to go in the video data number 22 outputs. (active when i80 mode)	5'b0
padloc21	[4:0]	RW	Select a location to go in the video data number 21 outputs. (active when i80 mode)	5'b 0

34.5.1.42 DPCRGBMASK0

- Base Address: 0xC010_2000
- Address = Base Address + 0x9C8h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
RGBMASK[15:0]	[15:0]	RW	Specifies the mask of the video data output (active when i80 mode) 0 = Masked (output = 0) 1 = Enabled	16'b0

34.5.1.43 DPCRGBMASK1

- Base Address: 0xC010_2000
- Address = Base Address + 0x9CCh, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
RGBMASK[23:16]	[7:0]	RW	Specifies the mask of the video data output (active when i80 mode) 0 = Masked (output = 0) 1 = Enabled	8'b0

34.5.1.44 DPCRGBSHIFT

- Base Address: 0xC010_2000
- Address = Base Address + 0x9D0h, Not available, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:6]	R	Reserved	26'b0
FIELDFLAG	[5]	R	Specifies the field flag of the interlace mode 0 = Odd frame 1 = Even frame	1'b0
RGBSHIFT	[4:0]	RW	Specifies the shift number of the video data output (active when i80 mode) PAD video data[23:0] = video data[23:0]<<RGBSHIFT	5'b0

34.5.1.45 dpcdataflush

- Base Address: 0xC010_2000
- Address = Base Address + 0x9D4h, Not available, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
REGFLUSH	[4]	W	Register flush manualy (primary only)	-
cmdbuffull	[3]	R	MPU i80 command buffer's full flag 0 = Not full 1 = Full	1'b0
cmdbufempty	[2]	R	MPU i80 command buffer's empty flag 0 = Not empty 1 = Empty	1'b0
CMDBUFFLUSH	[1]	RW	Set the dirty flag for MPU i80 command buffer 1 = When vertical sync period, command buffer start to send data.	1'b0
cmdbufclr	[0]	W	Clear the MPU i80 command buffer	-

34.5.1.46 DPCCLKENB

- Base Address: 0xC010_2000
- Address = Base Address + 0xBC0h, 0xFC0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:4]	R	Reserved	28'b0
PCLKMODE	[3]	RW	Specifies PCLK operating mode. 0 = PCLK is only enabled when CPU accesses this module 1 = PCLK is always enabled	1'b0
CLKGENENB	[2]	RW	Enable/Disable to generate a clock. 0 = Disable 1 = Enable	1'b0
RSVD	[1:0]	R	Reserved	2'b0

34.5.1.47 DPCCLKGEN0L

- Base Address: 0xC010_2000
- Address = Base Address + 0xBC4h, 0xFC4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
OUTCLKENB	[15]	RW	Specifies the direction of the PADVCLK pad. This bit should be set when CLKSRCSEL0/1 is 3 or 4. 0 = Enable (Output) 1 = Reserved	1'b0
RSVD	[14:13]	R	Reserved	2'b0
CLKDIV0	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL0	[4:2]	RW	Specifies the source clock. 0 = PLL0 1 = PLL1 2 = PLL2 3 = none 4 = HDMI PLL Clock 5 = none 6 = PLL3 7 = Reserved	3'b0
OUTCLKINV0	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
RSVD	[0]	RW	Reserved (This bit should be set to "0")	1'b0

34.5.1.48 DPCCLKGEN0h

- Base Address: 0xC010_2000
- Address = Base Address + 0xBC8h, 0xFC8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:5]	RW	Reserved for future use. This bit should be set to "0"	27'b0
OUTCLKDELAY0	[4:0]	RW	Specifies delay value of the clock output. This value is needed to adjust clock skew with respect to data signal. TBD	5'b0

34.5.1.49 DPCCLKGEN1L

- Base Address: 0xC010_2000
- Address = Base Address + 0xBCCh, 0xFCCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:13]	R	Reserved	19'b0
CLKDIV1	[12:5]	RW	Specifies divider value of the source clock. Divider value = CLKDIV0 + 1	8'b0
CLKSRCSEL1	[4:2]	RW	Specifies the source clock. 0 = PLL0 1 = PLL1 2 = PLL2 3 = none 4 = HDMI PLL Clock 5 = none 6 = PLL3 7 = CLKGEN0 Clock	3'b0
OUTCLKINV1	[1]	RW	Specifies whether to invert the clock output. 0 = Normal (Falling Edge) 1 = Invert (Rising Edge)	1'b0
outclksel	[0]	RW	1/2 ns delay is applied to Out clock from source clock Can be used only in case of division by even number 0 = Bypass 1 source clock /2 ns	1'b0

34.5.1.50 DPCCLKGEN1h

- Base Address: 0xC010_2000
- Address = Base Address + 0xBD0h, 0xFD0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:5]	RW	Reserved for future use. You don't have to write any value except 0.	27'b0
OUTCLKDELAY1	[4:0]	RW	Specifies delay value of the clock output. This value is needed to adjust clock skew with respect to data signal.	5'b0

Name	Bit	Type	Description	Reset Value
			TBD	

35 Scaler

35.1 Overview

The Scaler is the block to change image sizes. The Scaler reads an image from the memory and writes the image to the memory after Up/Down Scaling and Low-pass Filtering. At this time, the Scaler changes the direction of the image by using the Flip or Rotation function.

35.2 Features

- Source/Destination Image
- Format: Separated YUV Format (420, 422, 444), Interleaved UV
- Size: (8 to 4096) × (8 to 4096) (Width is set as a multiple of eight).
- Upscale Ratio: 8 × 8 → 4096 × 4096
- Downscale Ratio: 4096 × 4096 → 8 × 8
- Lowpass filter available after Upscale or before Downscale.
- Horizontal 5-Tab Filter: Coefficients 64 Sets.
- Vertical 3-Tab Filter: Coefficients 32 Sets (For Frequency Response, refer to Operation Item).

35.3 Block Diagram

The Scaler consists of the blocks (SRC_ADDR_GEN, DEST_ADDR_GEN) to generate addresses, the Filter block, the FIFO block, and the blocks (CPUIF and POS_GEN2) to exchange data with bus.

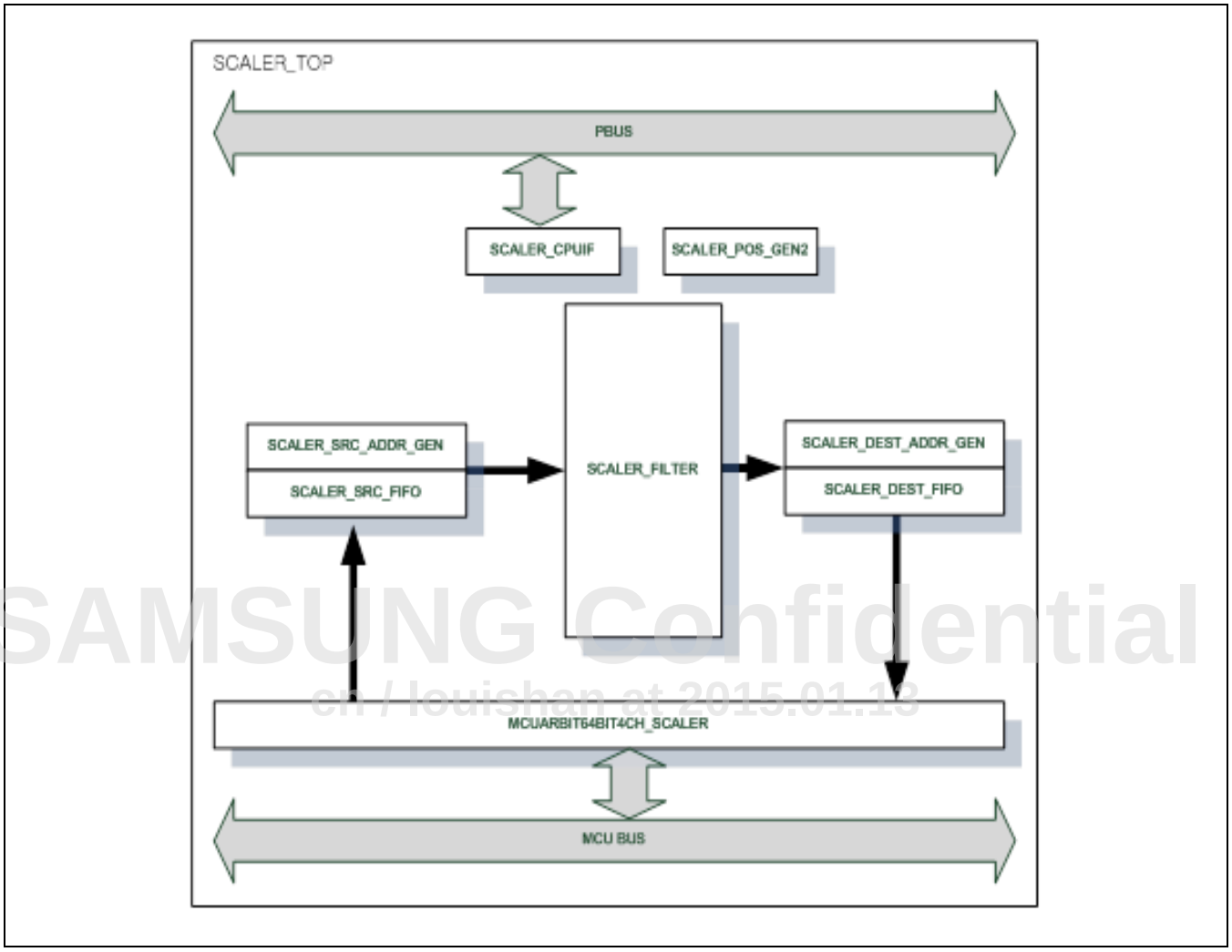


Figure 35-1 Fine Scaler Filter Block Diagram

35.4 Functional Description

The Scales enable a user to read a source image in memory, change the image size and store the image in the memory. The Scaler changes image sizes by using the setting values of the address, width and height of the source and destination images. A user can use the low-pass filter and rotate functions of the Scaler.

35.4.1 Digital Filter Characteristics

The low-pass filter of the Scaler has the horizontal filter of 5-tab and the vertical filter of 3-tab. The Scaler prevents image quality deterioration when an image is enlarged by using the low-pass filter.

35.4.1.1 Horizontal Filter (5-Tab FIR Filter) Frequency Response and Group Delay

Figure 35-2 shows the characteristics of the horizontal filter of the Scaler and the filter has the setting range between 0 and 63. The Scaler register, SCCFGREG.SC_HFILT_COEFF, is used for the setting.

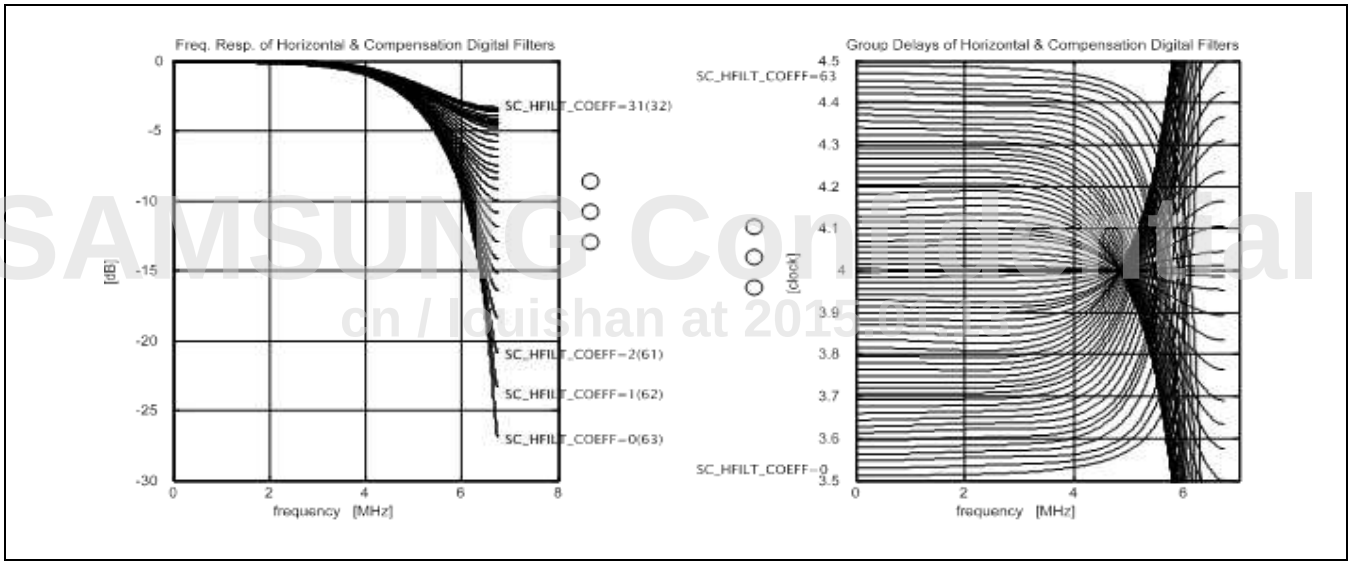


Figure 35-2 Horizontal Filter (5-Tab FIR Filter) Frequency Response and Group Delay

35.4.1.2 Vertical Filter (3-Tab FIR Filter) Frequency Response and Group Delay

Figure 35-3 shows the characteristics of the vertical filter of Scaler and the filter has the setting range between 0and 31. The Scaler register, SCCFGREG.SC_VFILT_COEFF, is used for the setting.

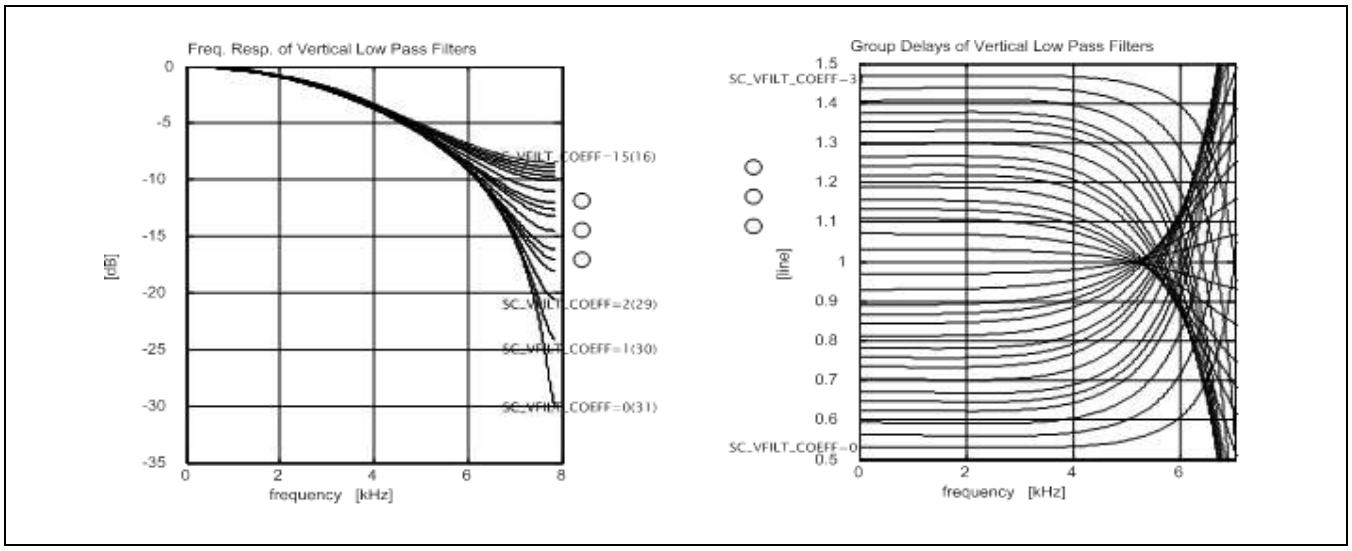


Figure 35-3 Vertical Filter (3-Tab FIR Filter) Frequency Response and Group Delay

35.5 Programming Guide

35.5.1 Configuration

1. Check the Scaler controller status: SCINTREG.SC_BUSY = 0
2. Set the source address and stride to the SCSRCADDR and SCSRCSTRIDE register respectively.
3. Set SCSRCSIZEREG.SC_SRC_WIDTH and SCSRCSIZEREG.SC_SRC_HEIGHT register. (the width is a multiple of 8).
4. Set the destination address and stride to the SCDESTADDR0 and SCDESTSTRIDE0 register respectively. If you need to scale UV interleaved image, set the destination address and stride to the SCDESTADDR1 and SCDESTSTRIDE1 register respectively.
5. Set SCDESTSIZEREG.SC_DEST_WIDTH and SCDESTSIZEREG.SC_DEST_HEIGHT register. (The width is a multiple of 8).
6. Delta Image setting: Set DELTAXREG and DELTAYREG register.
7. Soft setting: Set Horizontal/Vertical Set HVSOFTREG register.
8. Set the filter: Set the filter as On/Off by using SCCFGREG.SC_FILT_ENB. Select the Filter Coefficient Set by using SCCFGREG.SC_HFILT_COEFF and SCCFGREG.SC_VFILT_COEFF.
9. Set the interrupt: SCINTREG.SC_INT_ENB register.

35.5.2 RUN

1. Set the SCRUNREG.SC_RUN bit as "1".
2. Read the SCINTREG.SC_BUSY register to check the operation status.
3. If the SCRUNREG.SC_RUN bit is cleared when SCINTREG.SC_BUSY = 1, the operation halts immediately.

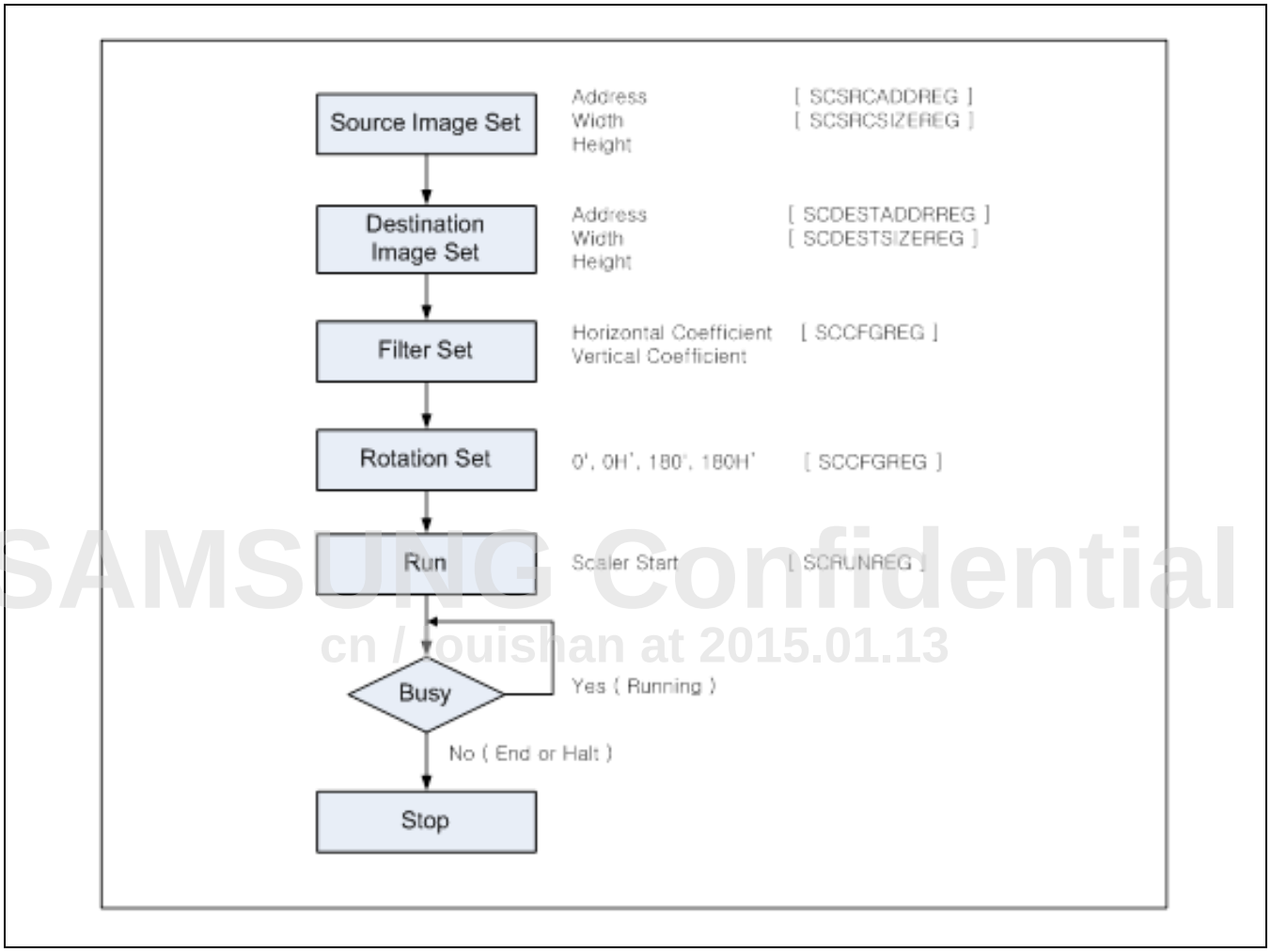


Figure 35-4 Scaler Operation Flow

35.6 Register Description

35.6.1 Register Map Summary

- Base Address: 0xC006_6000

Register	Offset	Description	Reset Value
SCRUNREG	0x000h	Scaler Run Register	0x0000_0000
SCCFGREG	0x004h	Scaler Configuration Register	0x0000_0000
SCINTREG	0x008h	Scaler Interrupt Register	0x0000_0000
SCSRCADDRREG	0x00Ch	Scaler Source Address Register	0x0000_0000
SCSRCADDRREG	0x010h	Scaler Source Stride Register	0x0000_0000
SCSRCSIZEREG	0x014h	Scaler Source Size Register	0x0000_0000
SCDESTADDR0	0x018h	Scaler Destination Address Register 0	–
SCDESTSTREDE0	0x01Ch	Scaler Destination Stride Register 0	–
SCDESTADDR1	0x020h	Scaler Destination Address Register1	–
SCDESTADDR1	0x024h	Scaler Destination Stride Register1	–
SCDESTSIZE	0x028h	Scaler Destination Size Register	0x0000_0000
DELTAXREG	0x02Ch	Scaler Horizontal Delta Register	0x0000_0000
DELTAYREG	0x030h	Scaler Vertical Delta Register	0x0000_0000
HVSOFTREG	0x034h	Scaler Ratio Reset Value Register	0x0000_0000
CMDBUFADDR	0x38h	Scaler Command Buffer Base Address Register	–
CMDBUFCON	0x03Ch	Scaler Command Buffer Control Register	0x0000_0000
YVFILTER[N]_00_03	0x040h (Filter1), 0x060h (Filter2), 0x080h (Filter3)	Scaler YV Filter[N] Value Table Register0	0x0000_0000
YVFILTER[N]_04_07	0x044h (Filter1), 0x064h (Filter2), 0x084h (Filter3)	Scaler YV Filter[N] Value Table Register1	0x0000_0000
YVFILTER[N]_04_07	0x044h (Filter1), 0x064h (Filter2), 0x084h (Filter3)	Scaler YV Filter[N] Value Table Register1	0x0000_0000
YVFILTER[N]_08_11	0x048h (Filter1), 0x068h (Filter2), 0x088h (Filter3)	Scaler YV Filter[N] Value Table Register2	0x0000_0000
YVFILTER[N]_12_15	0x04Ch (Filter1), 0x06Ch (Filter2), 0x08Ch (Filter3)	Scaler YV Filter[N] Value Table Register3	0x0000_0000
YVFILTER[N]_16_19	0x050h (Filter1), 0x070h (Filter2), 0x090h (Filter3)	Scaler YV Filter[N] Value Table Register4	0x0000_0000
YVFILTER[N]_20_23	0x054h (Filter1), 0x074h (Filter2), 0x094h (Filter3)	Scaler YV Filter[N] Value Table Register5	0x0000_0000

Register	Offset	Description	Reset Value
YVFILTER[N]_24_27	0x058h (Filter1), 0x078h (Filter2), 0x098h (Filter23)	Scaler YV Filter[N] Value Table Register6	0x0000_0000
YVFILTER[N]_28_31	0x05Ch (Filter1), 0x07Ch (Filter2), 0x09Ch (Filter23)	Scaler YV Filter[N] Value Table Register7	0x0000_0000
YVFILTER2_00_03	0x060h	Scaler YV Filter2 Value Table Register0	0x0000_0000
RSVD	0x0A0h to 0x0FC	Reserved	0x0000_0000
YHFILTER[N]_00_01	0x100h (Filter1), 0x140h (Filter2), 0x180h (Filter3), 0x1C0h (Filter4), 0x200h (Filter5)	Scaler YH Filter1 to 5 Value Table Register0	0x0000_0000
YHFILTER[N]_02_03	0x104h (Filter1), 0x144h (Filter2), 0x184h (Filter3), 0x1C4h (Filter4), 0x204h (Filter5)	Scaler YH Filter1 to 5 Value Table Register1	0x0000_0000
YHFILTER[N]_04_05	0x108h (Filter1), 0x148h (Filter2), 0x188h (Filter3), 0x1C8h (Filter4), 0x208h (Filter5)	Scaler YH Filter1 to 5 Value Table Register2	0x0000_0000
YHFILTER[N]_06_07	0x10Ch (Filter1), 0x14Ch (Filter2), 0x18Ch (Filter3), 0x1CCh (Filter4), 0x20Ch (Filter5)	Scaler YH Filter1 to 5 Value Table Register3	0x0000_0000
YHFILTER[N]_08_09	0x110h (Filter1), 0x150h (Filter2), 0x190h (Filter3), 0x1D0h (Filter4), 0x210h (Filter5)	Scaler YH Filter1 to 5 Value Table Register4	0x0000_0000
YHFILTER[N]_10_11	0x114h (Filter1), 0x154h (Filter2), 0x194h (Filter3), 0x1D4h (Filter4), 0x214h (Filter5)	Scaler YH Filter1 to 5 Value Table Register5	0x0000_0000
YHFILTER[N]_12_13	0x118h (Filter1), 0x158h (Filter2), 0x198h (Filter3), 0x1D8h (Filter4), 0x218h (Filter5)	Scaler YH Filter1 to 5 Value Table Register6	0x0000_0000
YHFILTER[N]_14_15	0x11Ch (Filter1), 0x15Ch (Filter2), 0x19Ch (Filter3), 0x1DCh (Filter4),	Scaler YH Filter1 to 5 Value Table Register7	0x0000_0000

Register	Offset	Description	Reset Value
	0x21Ch (Filter5)		
YHFILTER[N]_16_17	0x120h (Filter1), 0x160h (Filter2), 0x1A0h (Filter3), 0x1E0h (Filter4), 0x220h (Filter5)	Scaler YH Filter1 to 5 Value Table Register8	0x0000_0000
YHFILTER[N]_18_19	0x124h (Filter1), 0x164h (Filter2), 0x1A4h (Filter3), 0x1E4h (Filter4), 0x224h (Filter5)	Scaler YH Filter1 to 5 Value Table Register9	0x0000_0000
YHFILTER[N]_20_21	0x128h (Filter1), 0x168h (Filter2), 0x1A8h (Filter3), 0x1E8h (Filter4), 0x228h (Filter5)	Scaler YH Filter1 to 5 Value Table Register10	0x0000_0000
YHFILTER[N]_22_23	0x12Ch (Filter1), 0x16Ch (Filter2), 0x1ACh (Filter3), 0x1ECh (Filter4), 0x22Ch (Filter5)	Scaler YH Filter1 to 5 Value Table Register11	0x0000_0000
YHFILTER[N]_24_25	0x130h (Filter1), 0x170h (Filter2), 0x1B0h (Filter3), 0x1F0h (Filter4), 0x230h (Filter5)	Scaler YH Filter1 to 5 Value Table Register12	0x0000_0000
YHFILTER[N]_26_27	0x134h (Filter1), 0x174h (Filter2), 0x1B4h (Filter3), 0x1F4h (Filter4), 0x234h (Filter5)	Scaler YH Filter1 to 5 Value Table Register13	0x0000_0000
YHFILTER[N]_28_29	0x138h (Filter1), 0x178h (Filter2), 0x1B8h (Filter3), 0x1F8h (Filter4), 0x238h (Filter5)	Scaler YH Filter1 to 5 Value Table Register13	0x0000_0000
YHFILTER[N]_30_31	0x13Ch (Filter1), 0x17Ch (Filter2), 0x1BCh (Filter3), 0x1FCh (Filter4), 0x23Ch (Filter5)	Scaler YH Filter1 to 5 Value Table Register15	0x0000_0000

35.6.1.1 SCRUNREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x000h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	–	Reserved	31'b0
SC_RUN	[0]	RW	Scaler RUN bit. When the scaling process is finished, SCALER clears this bit automatically. While the scale process is running, it can be halted by clearing this bit. 0 = Stop 1 = Start (Auto Clear)	1'b0

35.6.1.2 SCCFGREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	–	Reserved	11'b0
sc_vfilt_coeff	[20:16]	RW	Vertical filter coefficient select. Range is 0 to 31. (See Frequency Response Graph)	5'bx
RSVD	[15:14]	–	Reserved	2'b0
sc_hfilt_coeff	[13:8]	RW	Horizontal filter coefficient select. Range is 0 to 63. (See Frequency Response Graph)	6'bx
RSVD	[7:2]	–	Reserved	6'b0
sc_filt_enb	[1:0]	RW	Fine scale filter enable. 00 = Filter Disable 01 = Reserved 10 = Reserved 11 = Filter Enable NOTE: This bit should be set as "00" or "11"	2'bx

35.6.1.3 SCINTREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x008h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:25]	–	Reserved	7'b0
sc_busy	[24]	R	Scaler Busy Check 0 = Scaler Idle 1 = Scaler Busy	1'b0
RSVD	[23:18]	–	Reserved	6'b0
cmd_proc_int_enb	[17]	RW	Internal Command Processor Interrupt Enable 0 = Disable 1 = Enable	1'b0
sc_int_enb	[16]	RW	Scaler Interrupt Enable 0 = Disable 1 = Enable	1'b0
RSVD	[15:10]	RW	Reserved	6'b0
cmd_proc_int_clr	[9]	W	Clear Internal Command Processor Interrupt Pending Bit 0 = None 1 = Clear Interrupt Pending	1'b0
sc_int_clr	[8]	W	Clear Internal Command Processor Interrupt Pending Bit 0 = None 1 = Clear Interrupt Pending	1'b0
RSVD	[7:2]	–	Reserved	6'b0
cmd_proc_int_pend	[1]	R	Command Processor Interrupt Pending Bit 0 = None 1 = Interrupt Pending	1'b0
sc_int_pend	[0]	R	Scaler Interrupt Pending Bit 0 = None 1 = Interrupt Pending	1'b0

35.6.1.4 SCSRCADDRREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x00Ch, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
SC_SRC_REG	[31:0]	RW	Source Base Address Register	-

35.6.1.5 SCSRCADDRREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x010h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
SC_SRC_STR	[31:0]	RW	Source Stride Register	-

35.6.1.6 SCSRCSIZEREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	–	Reserved	4'bx
sc_src_height	[27:16]	RW	Source Image Height. Height's range is 8 to 4096 (Source Height – 1)	12'b0
RSVD	[15:12]	–	Reserved	4'b0
sc_src_width	[11:0]	RW	Set Source Image Width. Width's range is 8 to 4096. Width must align to 8 (Source width – 1)	12'bx

35.6.1.7 SCDESTADDR0

- Base Address: 0xC006_6000
- Address = Base Address + 0x018h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
sc_dest_addr0	[31:0]	RW	Destination Base Address0	-

35.6.1.8 SCDESTSTREDE0

- Base Address: 0xC006_6000
- Address = Base Address + 0x01Ch, Reset Value =

Name	Bit	Type	Description	Reset Value
sc_dest_stride0	[31:0]	RW	Destination Stride	-

35.6.1.9 SCDESTADDR1

- Base Address: 0xC006_6000
- Address = Base Address + 0x020h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
sc_dest_addr1	[31:0]	RW	Destination Base Address1 NOTE: UV interleaved mode only	-

35.6.1.10 SCDESTADDR1

- Base Address: 0xC006_6000
- Address = Base Address + 0x024h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
sc_dest_stride1	[31:0]	RW	Destination Stride NOTE: UV interleaved mode only	-

35.6.1.11 SCDESTSIZE

- Base Address: 0xC006_6000
- Address = Base Address + 0x028h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	–	Reserved	4'b0
sc_dest_height	[27:16]	RW	Destination Image Height Height's range is 8 to 4096 (Destination Height -1)	-
RSVD	[15:12]	–	Reserved	4'b0
sc_dest_width	[11:0]	RW	Destination Image Width Image's range is 8 to 4096	-

35.6.1.12 DELTAXREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x02Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
deltaxreg	[31:0]	RW	Delta X of X-axis DELTA_X = (sc_src_width × h'10000) / (sc_dest_width-1)	32'b0

35.6.1.13 DELTAYREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x030h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
deltayreg	[31:0]	RW	Delta Y of Y-axis DELTA_Y = (sc_src_height × h'10000) / (sc_dest_height-1)	32'0

35.6.1.14 HVSOFTREG

- Base Address: 0xC006_6000
- Address = Base Address + 0x034h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:21]	–	Reserved	-
V_ratio	[20:16]	RW	Vertical Filter Ratio	5'b0
RSVD	[15:6]	–	Reserved	-
H_ratio	[5:0]	RW	Horizontal Filter Ratio	6'b0

35.6.1.15 CMDBUFADDR

- Base Address: 0xC006_6000
- Address = Base Address + 0x038h, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
cmdbufaddr	[31:0]	RW	Scaler Command Buffer Base Address Register	-

35.6.1.16 CMDBUFCON

- Base Address: 0xC006_6000
- Address = Base Address + 0x03Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	–	Reserved	-
cmdbuf_stop	[1]	RW	Scaler Command Buffer Stop Register 0 = No operation 1 = Stop	1'b0
cmdbuf_start	[0]	RW	Scaler Command Buffer Start Register 0 = No operation 1 = Start	1'b0

35.6.1.17 YVFILTER[N]_00_03

- Base Address: 0xC006_6000
- Address = Base Address + 0x040h (Filter1), 0x060h (Filter2), 0x080 (Filter3), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_03	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_02	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_01	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_00	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.18 YVFILTER[N]_04_07

- Base Address: 0xC006_6000
- Address = Base Address + 0x044h (Filter1), 0x064h (Filter2), 0x084 (Filter3), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_07	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_06	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_05	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_04	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.19 YVFILTER[N]_08_11

- Base Address: 0xC006_6000
- Address = Base Address + 0x048h (Filter1), 0x068h (Filter2), 0x088 (Filter3), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_11	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_10	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_09	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_08	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.20 YVFILTER[N]_12_15

- Base Address: 0xC006_6000
- Address = Base Address + 0x04Ch (Filter1), 0x06Ch (Filter2), 0x08C (Filter3), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_15	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_14	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_13	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_12	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.21 YVFILTER[N]_16_19

- Base Address: 0xC006_6000
- Address = Base Address + 0x050h (Filter1), 0x070h (Filter2), 0x090h (Filter3), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_19	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_18	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_17	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_16	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.22 YVFILTER[N]_20_23

- Base Address: 0xC006_6000
- Address = Base Address + 0x054h (Filter1), 0x074h (Filter2), 0x094h (Filter3), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_23	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_22	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_21	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_20	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.23 YVFILTER[N]_24_27

- Base Address: 0xC006_6000
- Address = Base Address + 0x058h (Filter1), 0x078h (Filter2), 0x098h (Filter23), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_27	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_26	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_25	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_24	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.24 YVFILTER[N]_28_31

- Base Address: 0xC006_6000
- Address = Base Address + 0x05Ch (Filter1), 0x07Ch (Filter2), 0x09Ch (Filter23), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF[N]_31	[31:24]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_30	[23:16]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_29	[15:8]	W	Scaler YVCOEF[N] value	8'b0
FILTER_YVCOEF[N]_28	[7:0]	W	Scaler YVCOEF[N] value	8'b0

35.6.1.25 YVFILTER2_00_03

- Base Address: 0xC006_6000
- Address = Base Address + 0x060h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
FILTER_YVCOEF2_03	[31:24]	W	Scaler YVCOEF2 value	8'b0
FILTER_YVCOEF2_02	[23:16]	W	Scaler YVCOEF2 value	8'b0
FILTER_YVCOEF2_01	[15:8]	W	Scaler YVCOEF2 value	8'b0
FILTER_YVCOEF2_00	[7:0]	W	Scaler YVCOEF2 value	8'b0

35.6.1.26 YHFILTER[N]_00_01

- Base Address: 0xC006_6000
- Address = Base Address + 0x100h (Filter1), 0x140 (Filter2), 0x180 (Filter3), 0x1C0 (Filter4), 0x200 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[N]_01	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_00	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.27 YHFILTER[N]_02_03

- Base Address: 0xC006_6000
- Address = Base Address + 0x104h (Filter1), 0x144 (Filter2), 0x184 (Filter3), 0x1C4 (Filter4), 0x204 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_03	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_02	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.28 YHFILTER[N]_04_05

- Base Address: 0xC006_6000
- Address = Base Address + 0x108h (Filter1), 0x148 (Filter2), 0x188 (Filter3), 0x1C8 (Filter4), 0x208 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_05	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_04	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.29 YHFILTER[N]_06_07

- Base Address: 0xC006_6000
- Address = Base Address + 0x10Ch (Filter1), 0x14C (Filter2), 0x18C (Filter3), 0x1CC (Filter4), 0x20C (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_07	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_06	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.30 YHFILTER[N]_08_09

- Base Address: 0xC006_6000
- Address = Base Address + 0x110h (Filter1), 0x150 (Filter2), 0x190 (Filter3), 0x1D0 (Filter4), 0x210 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_09	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_08	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.31 YHFILTER[N]_10_11

- Base Address: 0xC006_6000
- Address = Base Address + 0x114h (Filter1), 0x154 (Filter2), 0x194 (Filter3), 0x1D4 (Filter4), 0x214 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_11	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_10	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.32 YHFILTER[N]_12_13

- Base Address: 0xC006_6000
- Address = Base Address + 0x118h (Filter1), 0x158 (Filter2), 0x198 (Filter3), 0x1D8 (Filter4), 0x218 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_13	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_12	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.33 YHFILTER[N]_14_15

- Base Address: 0xC006_6000
- Address = Base Address + 0x11Ch (Filter1), 0x15C (Filter2), 0x19C (Filter3), 0x1DC (Filter4), 0x21C (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_15	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_14	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.34 YHFILTER[N]_16_17

- Base Address: 0xC006_6000
- Address = Base Address + 0x120h (Filter1), 0x160 (Filter2), 0x1A0 (Filter3), 0x1E0 (Filter4), 0x220 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_17	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_16	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.35 YHFILTER[N]_18_19

- Base Address: 0xC006_6000
- Address = Base Address + 0x124h (Filter1), 0x164 (Filter2), 0x1A4 (Filter3), 0x1E4 (Filter4), 0x224 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_19	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_18	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.36 YHFILTER[N]_20_21

- Base Address: 0xC006_6000
- Address = Base Address + 0x128h (Filter1), 0x168 (Filter2), 0x1A8 (Filter3), 0x1E8 (Filter4), 0x228 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_21	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_20	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.37 YHFILTER[N]_22_23

- Base Address: 0xC006_6000
- Address = Base Address + 0x12Ch (Filter1), 0x16C (Filter2), 0x1AC (Filter3), 0x1EC (Filter4), 0x22C (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_23	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_22	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.38 YHFILTER[N]_24_25

- Base Address: 0xC006_6000
- Address = Base Address + 0x130h (Filter1), 0x170 (Filter2), 0x1B0 (Filter3), 0x1F0 (Filter4), 0x230 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_25	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_24	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.39 YHFILTER[N]_26_27

- Base Address: 0xC006_6000
- Address = Base Address + 0x134h (Filter1), 0x174 (Filter2), 0x1B4 (Filter3), 0x1F4 (Filter4), 0x234 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_27	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_26	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.40 YHFILTER[N]_28_29

- Base Address: 0xC006_0000
- Address = Base Address + 0x138h (Filter1), 0x178 (Filter2), 0x1B8 (Filter3), 0x1F8 (Filter4), 0x238 (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-
FILTER_YHCOEF[n]_29	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_28	[9:0]	W	Scaler YHCOEF[N] value	10'b0

35.6.1.41 YHFILTER[N]_30_31

- Base Address: 0xC006_6000
- Address = Base Address + 0x13Ch (Filter1), 0x17C (Filter2), 0x1BC (Filter3), 0x1FC (Filter4), 0x23C (Filter5), Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	-

Name	Bit	Type	Description	Reset Value
FILTER_YHCOEF[n]_31	[25:16]	W	Scaler YHCOEF[N] value	10'b0
RSVD	[15:10]	–	Reserved	-
FILTER_YHCOEF[n]_30	[9:0]	W	Scaler YHCOEF[N] value	10'b0

36 LVDS

36.1 Overview

The LVDS (Low-Voltage differential signaling) is a block that generates the signals to interface with external LVDS display devices. The LVDS consists of a LVDS Controller and LVDS PHY block. The LVDS Controller receives RGB Video data from the DPC (or Resolution Converter) and converts RGB Video Data into a suitable LVDS data stream format and transmits converted RGB Video data to the LVDS PHY block. And the LVDS Controller transmits the control signals to the LVDS PHY block. The LVDS PHY block transmits received RGB Video Data from the LVDS Controller through 6 LVDS output channels.

36.2 Features

- Selectable Progressive RGB Video data (2 DPC)
- Supports JEIDA and VESA data packing for LVDS output
- Programmable data packing for LVDS output (configurable)
- Internal Input Video clock range: 30M to 90 MHz
- 6 LVDS output channels (5 data channels, 1 clock channel)
- 35:7 data channel compression up to 630Mbps on each LVDS channel
- Power down mode

36.3 Block Diagram

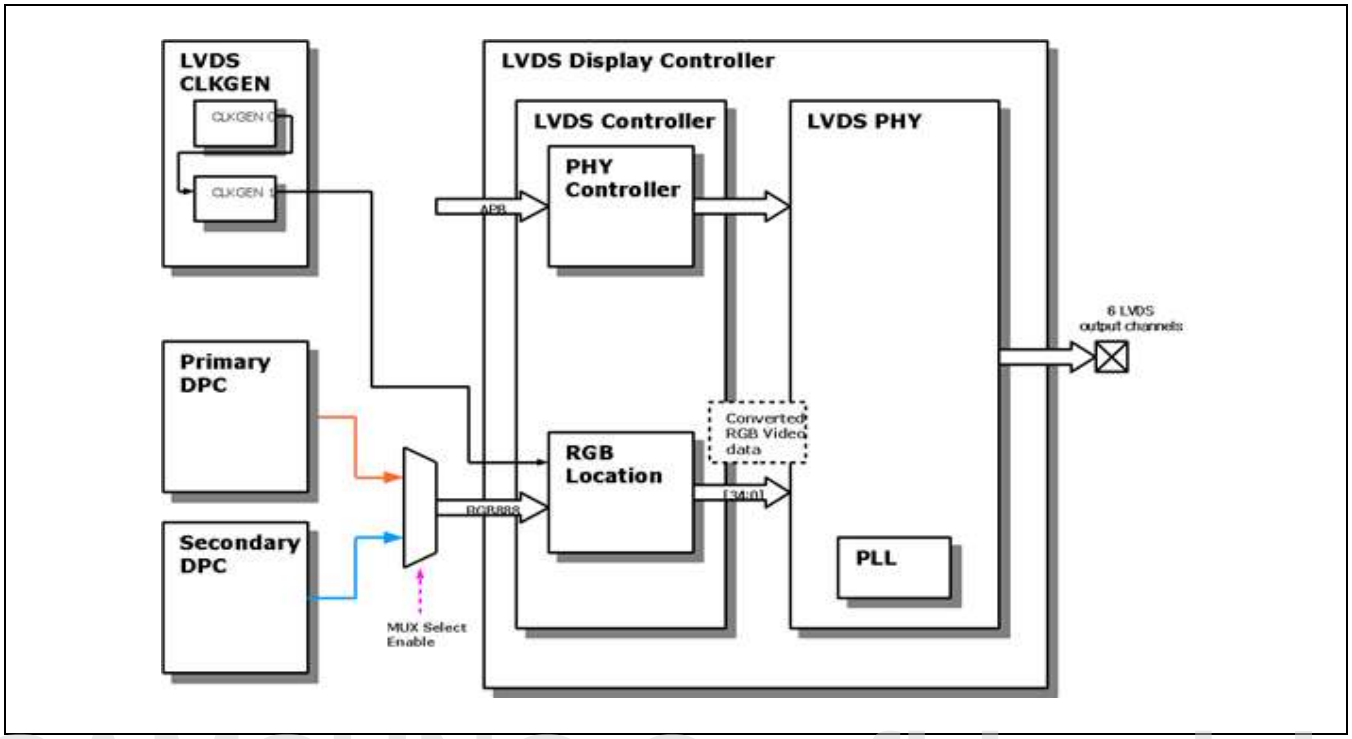


Figure 36-1 LVDS Block Diagram

36.4 Functional Description

36.4.1 LVDS Data Packing Format

The LVDS Controller converts received RGB Video Data from DPC into one of three data packing formats and transmits them to the LVDS PHY block. Following is supported LVDS data packing formats.

- VESA data packing format
- JEIDA data packing format
- User Programmable data packing format

In the VESA and JEIDA data packing formats, four of the five data channel is used for transmission.

Following is a format for each data packing format.

Table 36-1 VESA Data Packing Format

Channel	Bit Position						
	6	5	4	3	2	1	0
LVDS Channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS Channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS Channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS Channel D	Don't' care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6
LVDS Channel E	Not used	Not used	Not used	Not used	Not used	Not used	Not used

Table 36-2 JEIDA Data Packing Format

Channel	Bit Position						
	6	5	4	3	2	1	0
LVDS Channel A	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2
LVDS Channel B	bit 3	bit 2	bit 7	bit 6	bit 5	bit 4	bit 3
LVDS Channel C	DE	VSYNC	HSYNC	bit 7	bit 6	bit 5	bit 4
LVDS Channel D	Don't' care	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0
LVDS Channel E	Not used	Not used	Not used	Not used	Not used	Not used	Not used

When users set LCD_FORMAT bit of LVDSCTRL0 register to VESA data packing format, the outputs from the LVDS has a form of *Table 36-1*. Similarity, when users set them to JEIDA data packing format, the outputs has a form of *Table 36-2*.

In the User Programmable data packing format, users can set own data packing format for the LVDS output. Users determine for each bit of the channel, willing to output what signal. The signal can be a Hsync, Vsync, DE, or RGB Color bit. In the User Programmable data packing format, the setting value of the register means in *Table 36-3*.

Table 36-3 Location Setting Input Format

Bit Position							
[34:31]	[30:27]	[26]	[25]	[24]	[23:16]	[15: 8]	[7: 0]
4'b1111	4'b0000	VDEN	VSync	HSync	RED[7:0]	GREEN[7:0]	BLUE[7:0]

For examples, if users want to set 0'st bit of the LVDS Channel A to RED[2], users set the LOC_A0 bit of the LVDSLOC0 register to 17. (Note that 17'th bit position in *Table 36-3* is the RED[2]) If users want to set 5'th bit of the LVDS Channel D to VSync, users set the LOC_D5 bit of the LVDSLOC5 register to 25.

36.4.2 LVDS Application Note

In S5P4418, users can choose one of two RGB Video data.

- Primary DPC Video Data
- Secondary DPC Video Data

The following sequence should be used to use LVDS device. (Assuming that the sequence uses the Primary DPC Video Data)

1. Release the Reset of the DisplayTop and DualDisplay
2. Set the configuration of the Primary MLC and the Primary DPC. Set the Vertical, Horizontal Sync width of the DPC with the same width of the exterior LVSD Display Device's. Set the output format of the DPC to RGB888 format. Assuming that the DPC CLKGEN's clock source is PLL2 and clock divider is 2.
3. Set the LVDS CLKGEN's clock source is PLL2 and clock divider is 2 (same as the DPC CLKGEN). Recommend Configuration is the following.
   a. CLKGEN 0: SRC (PLL2), DIV (2)
   b. CLKGEN 1: SRC (7), DIV (2)
4. Set the LVDS_MUXSEL bit of the LVDS_MUXCTRL register to 0 (Using the Primary DPC), Set the LVDS_MUXENB bit of the LVDS_MUXCTRL register to 1 (Enable).
5. Set the LVDS data packing mode, set the configuration for LVDS Control Register. *Table 36-4* shows a example of using VESA data packing format.

Table 36-4 Recommend Configure for LVDS (VESA)

Register Name	Value
LVDSCTRL0	0x10036C70
LVDSCTRL1	0x000036DB
LVDSCTRL2	0x0000538E (High Speed, > 90MHz) 0x0000128A (Low Speed, < 90MHz)
LVDSCTRL3	0x00000333
LVDSCTRL4	0x003FFC20
LVDSTMODE0	0x00000080

6. Release the reset of the LVDS PHY block.

36.4.3 Skew Control between Output Data and Clock

The LVDS has the auto de-skew control function, If the LVDSCTRL0.I_AUTO_SEL and *LVDSCTRL4.AUTO_DSK_SEL*are high. The LVDS could operate the de-skewing function automatically. For the auto de-skewing, the signal which informs the vertical blank region is injected to the LVDS TX as like *Figure 36-2*.

If customer want to implement the auto de-skew function, RX have to support auto de-skew function.

In S5P4418, auto de-skew works only with Using the Primary DPC RGB Video.

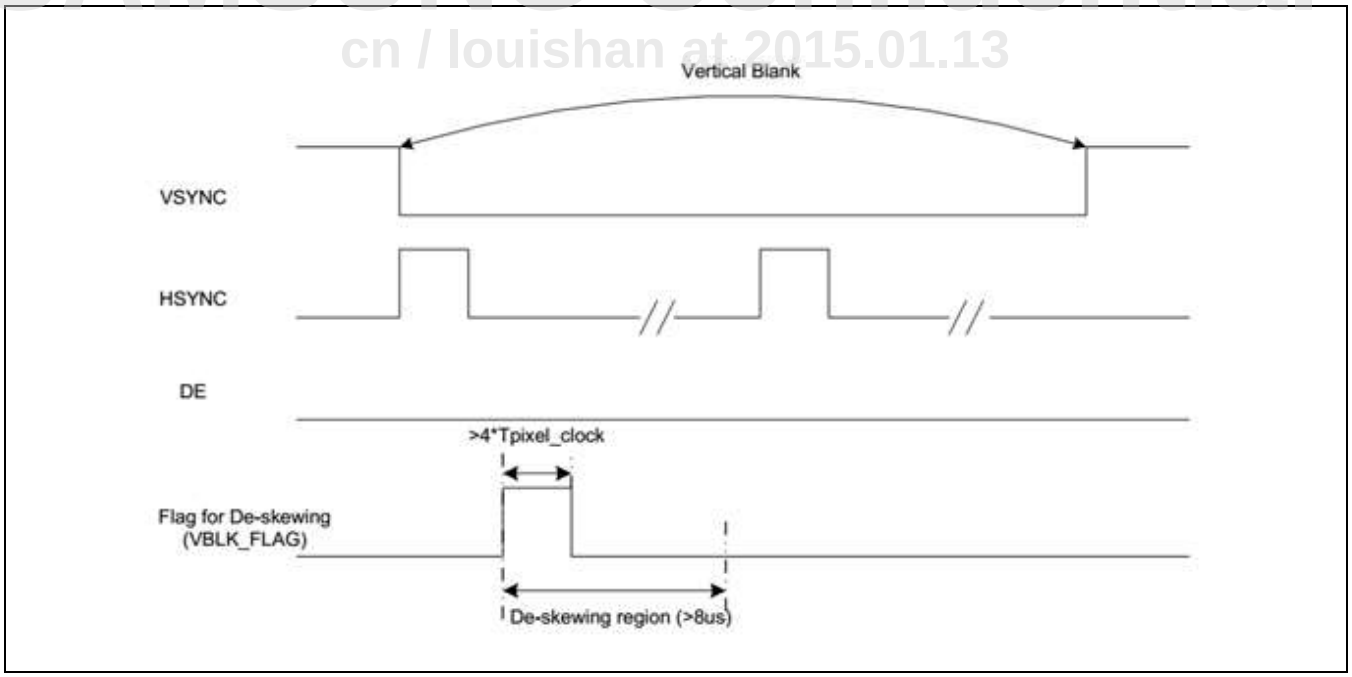


Figure 36-2 De-skewing Timing Diagram at Vertical blank

36.4.4 Electrical Characteristics

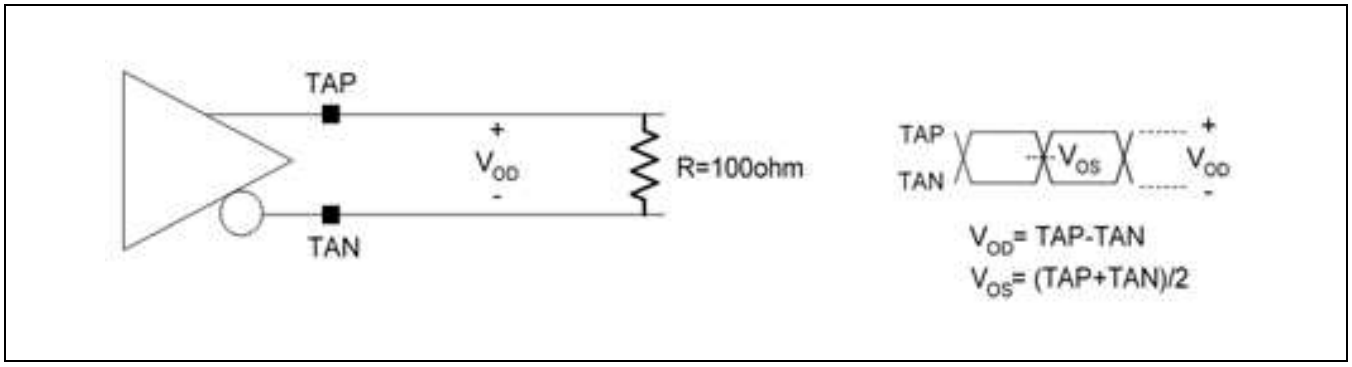


Figure 36-3 Output Common Mode Voltage and Differential Voltage

36.5 Register Description

36.5.1 Register Map Summary

- Base Address: 0xC010_A000

Register	Offset	Description	Reset Value
LVDSCTRL0	0x00h	LVDS Control register 0	0x0003_6C70
LVDSCTRL1	0x04h	LVDS Control register 1	0x0000_0000
LVDSCTRL2	0x08h	LVDS Control register 2	0x0000_028A
LVDSCTRL3	0x0Ch	LVDS Control register 3	0x0000_00C3
LVDSCTRL4	0x10h	LVDS Control register 4	0x003F_FC20
LVDSLOC0	0x20h	LVDS LOCATION register 0	0x0000_0000
LVDSLOC1	0x24h	LVDS LOCATION register 1	0x0000_0000
LVDSLOC2	0x28h	LVDS LOCATION register 2	0x0000_0000
LVDSLOC3	0x2Ch	LVDS LOCATION register 3	0x0000_0000
LVDSLOC4	0x30h	LVDS LOCATION register 4	0x0000_0000
LVDSLOC5	0x34h	LVDS LOCATION register 5	0x0000_0000
LVDSLOC6	0x38h	LVDS LOCATION register 6	0x0000_0000
LVDSLOCMASK0	0x40h	LVDS LOCATION MASK register 0	0x0000_0000
LVDSLOCMASK1	0x44h	LVDS LOCATION MASK register 1	0x0000_0000
LVDSLOCPOL0	0x48h	LVDS LOCATION PORALITY register 0	0x0000_0000
LVDSLOCPOL1	0x4Ch	LVDS LOCATION PORALITY register 1	0x0000_0000
LVDSTMODE0	0x50h	LVDS TEST MODE register 0	0x0000_0000
LVDSTMODE1	0x54h	LVDS TEST MODE register 1	0x0000_0004
DisplayTop Register Summary • Base Address : 0xC010_1000			
LVDS_MUXCTRL	0x0Ch	DISPLAYTOP LVDS MUX Control register	0x0000_0000

36.5.1.1 LVDSCTRL0

- Base Address: 0xC010_A000
- Address = Base Address + 0x00h, Reset Value = 0x0003_6C70

Name	Bit	Type	Description	Reset Value
RSVD	[31]	R	Reserved	1'b0
CPU_I_VBLK_FLAG_SEL	[30]	RW	Enable/Disable Using CPU_I_VBLK_FLAG (I_VBLK_FLAG used for de-skew) 0 = Using Input Video's VBLK 1 = Using CPU_I_VBLK	1'b0
CPU_I_VBLK_FLAG	[29]	RW	Specifies the CPU_I_VBLK_FLAG Value	1'b0
SKINI_BST	[28]	RW	Delay initial control pin for BIST 0 = Bypass 1 = Delay control	1'b0
DLYS_BST	[27]	RW	Delay control pin for BIST 0 = 25ps 1 = 50ps	1'b0
I_AUTO_SEL	[26]	RW	Auto de-skew selection pin 0 = Auto de-skew 1 = Not auto de-skew	1'b0
RSVD	[25:24]	R	Reserved	2'b0
DE_POL	[23]	RW	Specifies the polarity of the Data Enable (DE) (applicable to VESA and JEIDA data packing format only) 0 = High Active 1 = Low Active	1'b0
HSYNC_POL	[22]	RW	Specifies the polarity of the Horizontal Sync (HSync) (applicable to VESA and JEIDA data packing format only) - High Active means HSync is HIGH when Horizontal Sync Period 0 = High Active 1 = Low Active	1'b0
VSYNC_POL	[21]	RW	Specifies the polarity of the Vertical Sync (VSync) (applicable to VESA and JEIDA data packing format only) - High Active means VSync is HIGH when Vertical Sync Period 0 = High Active 1 = Low Active	1'b0
LCD_FORMAT	[20:19]	RW	Specifies the LVDS data packing format 0 = VESA data packing format 1 = JEIDA data packing format 2 = User Programmable data packing format 3 = Reserved (Undefined data packing format)	2'b0
I_LOCK_PPM_SET	[18:13]	RW	PPM setting for PLL lock	6'b011011
I_DESKEW_CNT_SET	[12:1]	RW	Adjust the period of de-skew region.	12'b0110_00

Name	Bit	Type	Description	Reset Value
				11_1000
I_AUTO_SEL	[0]	RW	Auto de-skew selection pin 0 = auto de-skew 1 = not auto de-skew	1'b0

36.5.1.2 LVDSCTRL1

- Base Address: 0xC010_A000
- Address = Base Address + 0x04h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
TX4010X_DUMMY	[31:29]	RW	Dummy Pin (for LVDS PHY self test)	3'b0
I_ATE_MODE	[28]	RW	Function or ATE 0 = Function 1 = ATE	1'b0
I_TEST_CON_MODE	[27]	RW	DA or I2C 0 = DA 1 = I2C	1'b0
I_TX4010X_DUMMY	[26:24]	RW	Dummy Pin (for LVDS PHY self test)	3'b0
RSVD	[23:18]	R	Reserved	6'b0
SKCCK	[17:15]	RW	TX output skew control pin at ODD clock ch.(Dft: 3'b011)	3'b000
SKC4	[14:12]	RW	TX output skew control pin at ODD ch4 (Dft: 3'b011)	3'b000
SKC3	[11:9]	RW	TX output skew control pin at ODD ch3 (Dft: 3'b011)	3'b000
SKC2	[8:6]	RW	TX output skew control pin at ODD ch2 (Dft: 3'b011)	3'b000
SKC1	[5:3]	RW	TX output skew control pin at ODD ch1 (Dft: 3'b011)	3'b000
SKC0	[2:0]	RW	TX output skew control pin at ODD ch0 (Dft: 3'b011)	3'b000

36.5.1.3 LVDSCTRL2

- Base Address: 0xC010_A000
- Address = Base Address + 0x08h, Reset Value = 0x0000_028A

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
CK_POL_SEL	[15]	RW	Input clock polarity selection pin 0 = Bypass 1 = Inversion	1'b0
VSEL	[14]	RW	VCO Frequency range selection pin 0 = Low speed (40MHz to 90MHz) 1 = High speed (90MHz to 160MHz)	1'b0
S	[13:12]	RW	Post-scaler control pin for PLL Recommend: Low speed: 2'b01, High speed: 2'b01	2'b00
M	[11:6]	RW	Main divider control pin for PLL Recommend: Low speed: 6'b001010, High speed: 6'b001110	6'b001010
P	[5:0]	RW	Pre-divider control pin for PLL Recommend: Low speed: 6'b001010, High speed: 6'b001110	6'b001010

36.5.1.4 LVDSCTRL3

- Base Address: 0xC010_A000
- Address = Base Address + 0x0Ch, Reset Value = 0x0000_00C3

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	R	Reserved	22'b0
SK_BIAS	[9:6]	RW	Bias current control pin for Skew	4'b0011
SKEWINI	[5]	RW	Skew selection pin 0 = Bypass 1 = Skew enable	1'b0
SKEW_EN_H	[4]	RW	Skew block power down 0 = Power down 1 = Operating	1'b0
CNTB_TDLY	[3]	RW	Delay control pin for each channel 0 = 25p 1 = 50ps	1'b0
SEL_DATABF	[2]	RW	Input clock 1/2 division control pin	1'b0
SKEW_REG_CUR	[1:0]	RW	Regulator bias current selection pin in SKEW block	2'b11

36.5.1.5 LVDSCTRL4

- Base Address: 0xC010_A000
- Address = Base Address + 0X10h, Reset Value = 0x003F_FC20

Name	Bit	Type	Description	Reset Value
RSVD	[31:29]	R	Reserved	3'b0
FLT_CNT	[28]	RW	Filter control pin for PLL	1'b0
VOD_ONLY_CNT	[27]	RW	The pre-emphasis's pre-driver control pin (VOD Only) 0 = Disable 1 = Enable	1'b0
CNNCT_MODE_SEL	[26]	RW	Connectivity mode selection pin 0 = TX operating 1 = Connectivity check.	1'b0
CNNCT_CNT	[25:24]	RW	Connectivity control pin 0 = TX operating 1 = Connectivity check 2, 3 = X (Don't care)	2'b00
VOD_HIGH_S	[23]	RW	VOD control pin 0 = Normal w/pre-emphasis 1 = Vod only	1'b0
SRC_TRH	[22]	RW	Source termination resistor selection pin 0 = Off 1 = Termination	1'b0
CNT_VOD_H	[21:14]	RW	TX driver output differential voltage level control pin	8'b11111111
CNT_PEN_H	[13:6]	RW	TX driver pre-emphasis level control (Dft: 8'b0000_0001)	8'b11110000
FC_CODE	[5:3]	RW	Vos control pin	3'b100
OUTCON	[2]	RW	TX Driver state selection pin 0 = Hi-z 1 = Low	1'b0
LOCK_CNT	[1]	RW	Lock signal selection pin 0 = Lock enable 1 = Lock disable	1'b0
AUTO_DSK_SEL	[0]	RW	Auto de-skew selection pin for analog 0 = Normal 1 = Auto-de-skew	1'b0

36.5.1.6 LVDSLOC0

- Base Address: 0xC010_A000
- Address = Base Address + 0x20h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	28'b0
LOC_A4	[29:24]	RW	Select a location to go in LVDS Channel A bit 4. (applicable to User Programmable data packing format only)	6'b0
LOC_A3	[23:18]	RW	Select a location to go in LVDS Channel A bit 3. (applicable to User Programmable data packing format only)	6'b0
LOC_A2	[17:12]	RW	Select a location to go in LVDS Channel A bit 2. (applicable to User Programmable data packing format only)	6'b0
LOC_A1	[11:6]	RW	Select a location to go in LVDS Channel A bit 1. (applicable to User Programmable data packing format only)	6'b0
LOC_A0	[5:0]	RW	Select a location to go in LVDS Channel A bit 0. (applicable to User Programmable data packing format only)	6'b0

36.5.1.7 LVDSLOC1

- Base Address: 0xC010_A000
- Address = Base Address + 0x24h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	28'b0
LOC_B2	[29:24]	RW	Select a location to go in LVDS Channel B bit 2. (applicable to User Programmable data packing format only)	6'b0
LOC_B1	[23:18]	RW	Select a location to go in LVDS Channel B bit 1. (applicable to User Programmable data packing format only)	6'b0
LOC_B0	[17:12]	RW	Select a location to go in LVDS Channel B bit 0. (applicable to User Programmable data packing format only)	6'b0
LOC_A6	[11:6]	RW	Select a location to go in LVDS Channel A bit 6. (applicable to User Programmable data packing format only)	6'b0
LOC_A5	[5:0]	RW	Select a location to go in LVDS Channel A bit 5. (applicable to User Programmable data packing format only)	6'b0

36.5.1.8 LVDSLOC2

- Base Address: 0xC010_A000
- Address = Base Address + 0x28h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	28'b0
LOC_C0	[29:24]	RW	Select a location to go in LVDS Channel C bit 0. (applicable to User Programmable data packing format only)	6'b0
LOC_B6	[23:18]	RW	Select a location to go in LVDS Channel B bit 6. (applicable to User Programmable data packing format only)	6'b0
LOC_B5	[17:12]	RW	Select a location to go in LVDS Channel B bit 5. (applicable to User Programmable data packing format only)	6'b0
LOC_B4	[11:6]	RW	Select a location to go in LVDS Channel B bit 4. (applicable to User Programmable data packing format only)	6'b0
LOC_B3	[5:0]	RW	Select a location to go in LVDS Channel B bit 3. (applicable to User Programmable data packing format only)	6'b0

36.5.1.9 LVDSLOC3

- Base Address: 0xC010_A000
- Address = Base Address + 0x2Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	28'b0
LOC_C5	[29:24]	RW	Select a location to go in LVDS Channel C bit 5. (applicable to User Programmable data packing format only)	6'b0
LOC_C4	[23:18]	RW	Select a location to go in LVDS Channel C bit 4. (applicable to User Programmable data packing format only)	6'b0
LOC_C3	[17:12]	RW	Select a location to go in LVDS Channel C bit 3. (applicable to User Programmable data packing format only)	6'b0
LOC_C2	[11:6]	RW	Select a location to go in LVDS Channel C bit 2. (applicable to User Programmable data packing format only)	6'b0
LOC_C1	[5:0]	RW	Select a location to go in LVDS Channel C bit 1. (applicable to User Programmable data packing format only)	6'b0

36.5.1.10 LVDSLOC4

- Base Address: 0xC010_A000
- Address = Base Address + 0x30h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	28'b0
LOC_D3	[29:24]	RW	Select a location to go in LVDS Channel D bit 3. (applicable to User Programmable data packing format only)	6'b0
LOC_D2	[23:18]	RW	Select a location to go in LVDS Channel D bit 2. (applicable to User Programmable data packing format only)	6'b0
LOC_D1	[17:12]	RW	Select a location to go in LVDS Channel D bit 1. (applicable to User Programmable data packing format only)	6'b0
LOC_D0	[11:6]	RW	Select a location to go in LVDS Channel D bit 0. (applicable to User Programmable data packing format only)	6'b0
LOC_C6	[5:0]	RW	Select a location to go in LVDS Channel C bit 6. (applicable to User Programmable data packing format only)	6'b0

36.5.1.11 LVDSLOC5

- Base Address: 0xC010_A000
- Address = Base Address + 0x34h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	28'b0
LOC_E1	[29:24]	RW	Select a location to go in LVDS Channel E bit 1. (applicable to User Programmable data packing format only)	6'b0
LOC_E0	[23:18]	RW	Select a location to go in LVDS Channel E bit 0. (applicable to User Programmable data packing format only)	6'b0
LOC_D6	[17:12]	RW	Select a location to go in LVDS Channel D bit 6. (applicable to User Programmable data packing format only)	6'b0
LOC_D5	[11:6]	RW	Select a location to go in LVDS Channel D bit 5. (applicable to User Programmable data packing format only)	6'b0
LOC_D4	[5:0]	RW	Select a location to go in LVDS Channel D bit 4. (applicable to User Programmable data packing format only)	6'b0

36.5.1.12 LVDSLOC6

- Base Address: 0xC010_A000
- Address = Base Address + 0x38h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	R	Reserved	28'b0
LOC_E6	[29:24]	RW	Select a location to go in LVDS Channel E bit 6. (applicable to User Programmable data packing format only)	6'b0
LOC_E5	[23:18]	RW	Select a location to go in LVDS Channel E bit 5. (applicable to User Programmable data packing format only)	6'b0
LOC_E4	[17:12]	RW	Select a location to go in LVDS Channel E bit 4. (applicable to User Programmable data packing format only)	6'b0
LOC_E3	[11:6]	RW	Select a location to go in LVDS Channel E bit 3. (applicable to User Programmable data packing format only)	6'b0
LOC_E2	[5:0]	RW	Select a location to go in LVDS Channel E bit 2. (applicable to User Programmable data packing format only)	6'b0

36.5.1.13 LVDSLOCMASK0

- Base Address: 0xC010_A000
- Address = Base Address + 0x40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LOCMASK0	[31:0]	RW	Specifies the mask of the LVDS Channel A0 to E3 output (applicable to User Programmable data packing format only) - Each bits (Users must set HIGH to use) 0 = Masked 1 = Output Enable	32'b0

36.5.1.14 LVDSLOCMASK1

- Base Address: 0xC010_A000
- Address = Base Address + 0x44h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
LOCMASK1	[2:0]	RW	Specifies the mask of the LVDS Channel E4 to E5 output (applicable to User Programmable data packing format only) - bits (Users must set HIGH to use) 0 = Masked 1 = Output Enable	3'b0

36.5.1.15 LVDSLOCPOL0

- Base Address: 0xC010_A000
- Address = Base Address + 0x48h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LOCPOL0	[31:0]	RW	Specifies the polarity of the LVDS Channel A0 to E3 output (applicable to User Programmable data packing format only) - Each bits 0 = Normal 1 = Inversed Bit	32'b0

36.5.1.16 LVDSLOCPOL1

- Base Address: 0xC010_A000
- Address = Base Address + 0x4Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved	29'b0
LOCPOL1	[2:0]	RW	Specifies the polarity of the LVDS Channel E4 to E6 output (applicable to User Programmable data packing format only) - Each bits 0 = Normal 1 = Inversed Bit	3'b0

36.5.1.17 LVDSTMODE0

- Base Address: 0xC010_A000
- Address = Base Address + 0x50h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:25]	R	Reserved	7'b0
I_BIST_RESETB	[24]	RW	Reset all BIST blocks 0 = Reset enable 1 = Reset disable	1'b0
I_BIST_EN	[23]	RW	Enable BIST operation 0 = BIST Disable 1 = BIST Enable	1'b0
I_BIST_PAT_SEL	[22:21]	RW	Select BIST pattern to perform. 0 = PRBS7 1 = User pat 2 = 1's0 + 1's1 3 = 7's0 + 7's1	2'b0
I_BIST_USER_PATTERN	[20:14]	RW	BIST user pattern setting	7'b0
I_BIST_FORCE_ERROR	[13]	RW	Inserted one error into BIST transmitted pattern	1'b0
I_BIST_SKEW_CTRL	[12:7]	RW	Used the manual skew setting during data comparing in BIST 5'th bit: 0 = Auto-skew, 1 = Manual skew control	6'b0
I_BIST_CLK_INV	[6:5]	RW	Inverted clock during BIST operation. Bit0 is for digital and bit1 is for Analog, respectively.	2'b0
I_BIST_DATA_INV	[4:3]	RW	Inverted the data order during BIST operation. Bit0 is for RX and bit1 is for TX, respectively.	2'b0
I_BIST_CH_SEL	[2:0]	RW	Select the channel for BIST operation	3'b0

36.5.1.18 LVDSTMODE1

- Base Address: 0xC010_A000
- Address = Base Address + 0x54h, Reset Value = 0x0000_0004

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
O_BIST_ERR_COUNT	[15:8]	R	ODD BIST error count value	8'b0
RSVD	[7:3]	R	Reserved	5'b0
MON_FOR_CNNCT	[2]	R	Monitor pin for connectivity check	1'b1
O_BIST_SYNC	[1]	R	ODD BIST found the expected pattern and started data comparing	1'b0
O_BIST_STATUS	[0]	R	ODD Indicated whether BIST error occurs	1'b0

36.5.1.19 DisplayTop Register Summary

User uses this register to select the RGB Video data between the Primary DPC and the Secondary DPC.

36.5.1.19.1 LVDS_MUXCTRL

- Base Address: 0xC010_1000
- Address = Base Address + 0x0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
LVDS_MUXENB	[31]	RW	MUX Enable 0 = MUX Disable 1 = MUX Enable	1'b0
RSVD	[30:2]	RW	Reserved	29'b0
LVDS_MUXSEL	[1:0]	RW	MUX Select 0 = Primary DPC 1 = Secondary DPC 2-3 = Reserved (Never use this value)	2'b0

37 HDMI

37.1 Overview

The HDMI (High Definition Multimedia Interface) is compatible with HDMI v1.4 spec and supports up to 1080p video resolution. It accepts RGB Video data from DPC and transmits them into HDMI cable with a serialized form.

The HDMI consists of a HDMI Link and HDMI PHY. The HDMI Link receives RGB Video data from DPC and translates them into a sequence of 10-bit signals compliant to HDMI v1.4 specification. The HDMI PHY receives a sequence of 10-bit signals from the HDMI Link and transmits them into HDMI cable with serialized form. And the HDMI PHY can generate both pixel clock and TMDS clock from the reference 24 MHz clock. So users can use the generated pixel clock from the HDMI PHY, instead of external divided PLL clock from CLKGEN.DPC (Display Controller) also can use the generated pixel clock from the HDMI PHY. All the pixel clock frequency specified in HDMI v1.4 spec can be generated by the HDMI PHY.

37.2 Features

- HDMI 1.4a, HDCP 1.4 Complaint
- Supports Video format
  - 480p @59.94 Hz/60 Hz, 576p@50 Hz
  - 720p @50 Hz/59.94 Hz/60 Hz
  - 1080p @50 Hz/59.94 Hz/60 Hz
    (not supports for interlace video format)
- Supports Color Format: 4:4:4 RGB
- Pixel Repetition: Up to x4
- Supports Bit Per Color: 8-bit
- HDMI CEC (Consumer Electronics Control)
- Supports: SPDIF 2Ch, I2C 2Ch, (left/right)
- Integrated HDCP Encryption Engine for Video/Audio content protection (Authentication procedure are controlled by S/W, not by H/W)
- Power down mode

NOTE: I2C for DDC channel is not including in the HDMI module, users must use one I2C module for DDC channel in S5P4418.

37.3 Block Diagram

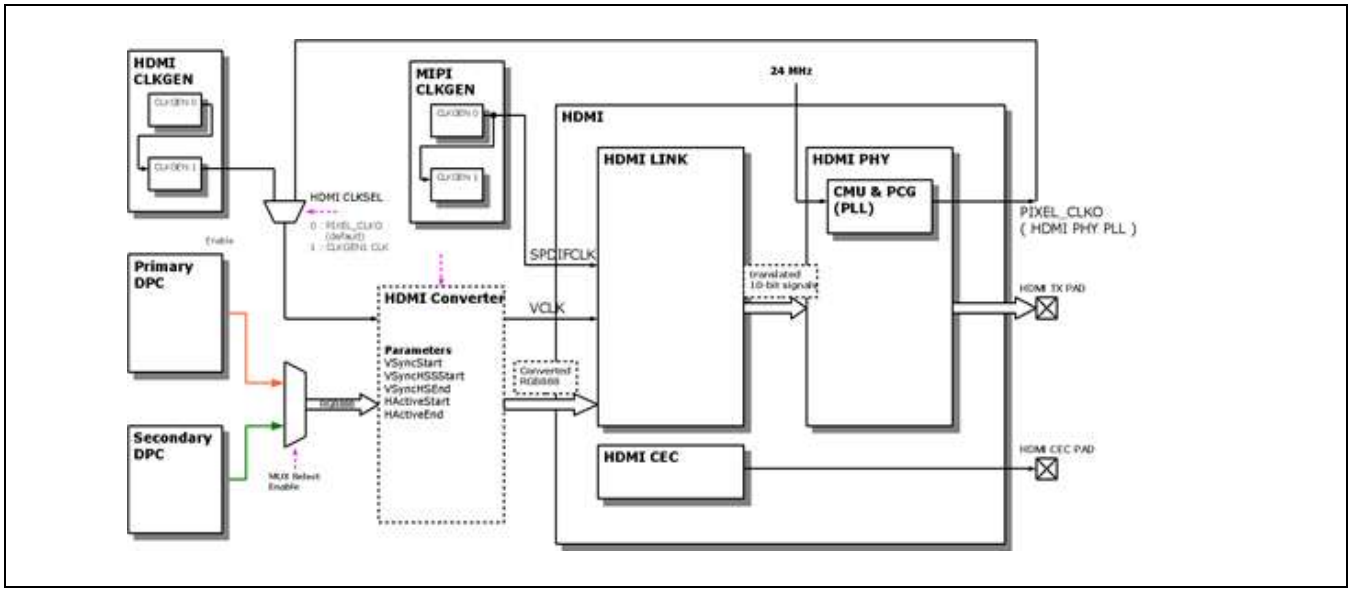


Figure 37-1 HDMI Block Diagram

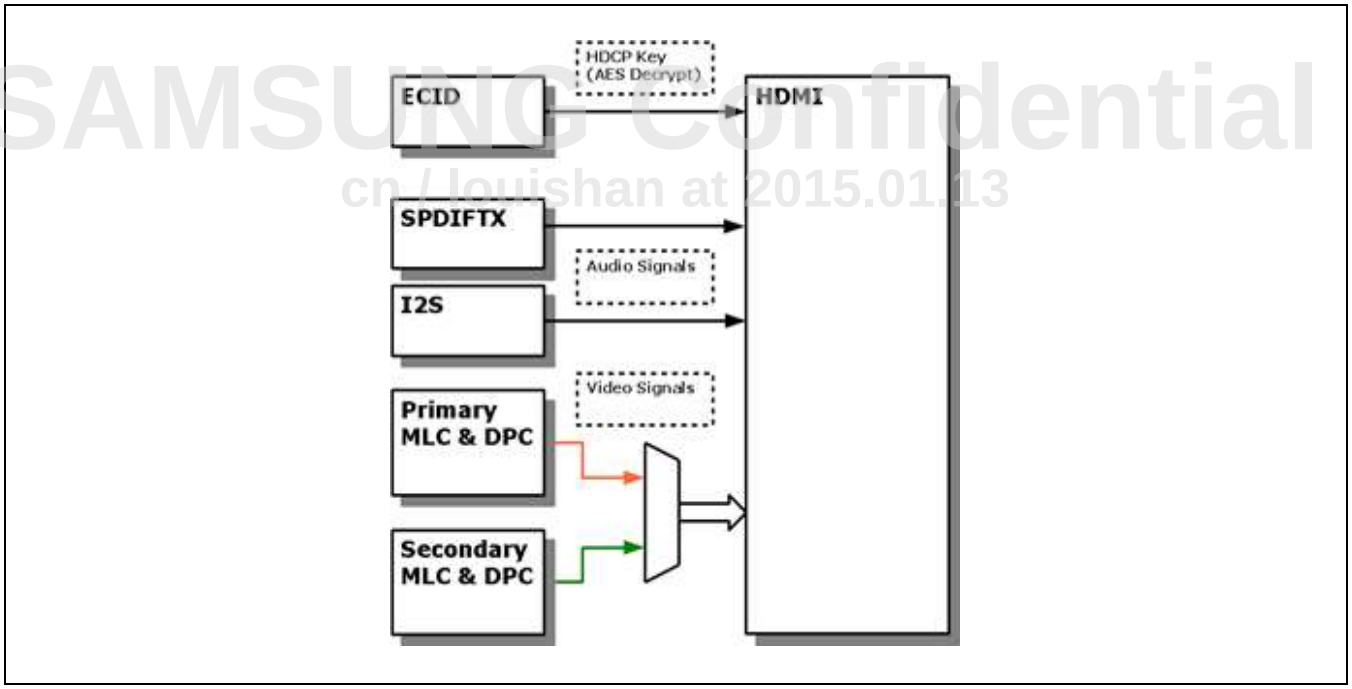


Figure 37-2 HDMI SYSTEM Block Diagram

NOTE: SPDIFCLK (*Figure 37-1*) is used to latch SDATA of I2S and SPDIFIN of SPDIFTX. SPDIFCLK frequency shall be eight times higher than that of SDATA and SPDIFIN. In SPDIF, SPDIFCLK must have higher frequency than fs × 512.

For example, SPDIF TX uses 48 kHz frequency sampling, and then SPDIFCLK must have 24.576MHz frequency. 48k × 512 = 24576k.

37.4 Functional Description

37.4.1 Select RGB Video data for HDMI

In S5P4418, users can choose one of two RGB Video data.

- Primary DPC Video Data
- Secondary DPC Video Data

When user want to use the Primary DPC Video Data for HDMI outputs, user set the HDMI_MUXSEL bit of the HDMI_MUXCTRL register with 0 and set the HDMI_MUXENB bit of the HDMI_MUXCTRL register with 1.

37.4.2 HDMI Converter

The HDMI Converter converts the RGB Video data from DPC into a suitable format for the HDMI Link. Users must set the HDMI Converter's parameters. The HDMI Converter consists of few registers. The configuration values for the registers are in following table. The *Figure 37-3* shows sync signal timing diagram.

NOTE: Since DPC makes sync signals, users must remember the sync information of current source video data. And users must calculate the values of V2_BLANK and V_SYNC_LINE_BEF, etc. (referred on *Figure 37-3*)

Table 37-1 The Configuration Values for the HDMI Converter

Register name	Bit	Symbol	Description (Refer *Figure 37-3*)
HDMI_SYNCCTRL0	[31]	HDMI_VCLK_SEL	This bit must be 0 (In *Figure 37-1*, HDMI_CLKSEL)
HDMI_SYNCCTRL0	[15:0]	HDMI_VSYNCSTART	V2_BLANK - V_SYNC_LINE_BEF_1 - 1
HDMI_SYNCCTRL1	[15:0]	HDMI_HACTIVESTART	H_BLANK - H_SYNC_START
HDMI_SYNCCTRL2	[15:0]	HDMI_HACTIVEEND	H_BLANK - H_SYNC_START + 1
HDMI_SYNCCTRL3	[31:16]	HDMI_VSYNCHSEND	H_BLANK - H_SYNC_START
HDMI_SYNCCTRL3	[15:0]	HDMI_VSYNCHSSTART	H_LINE - H_SYNC_START

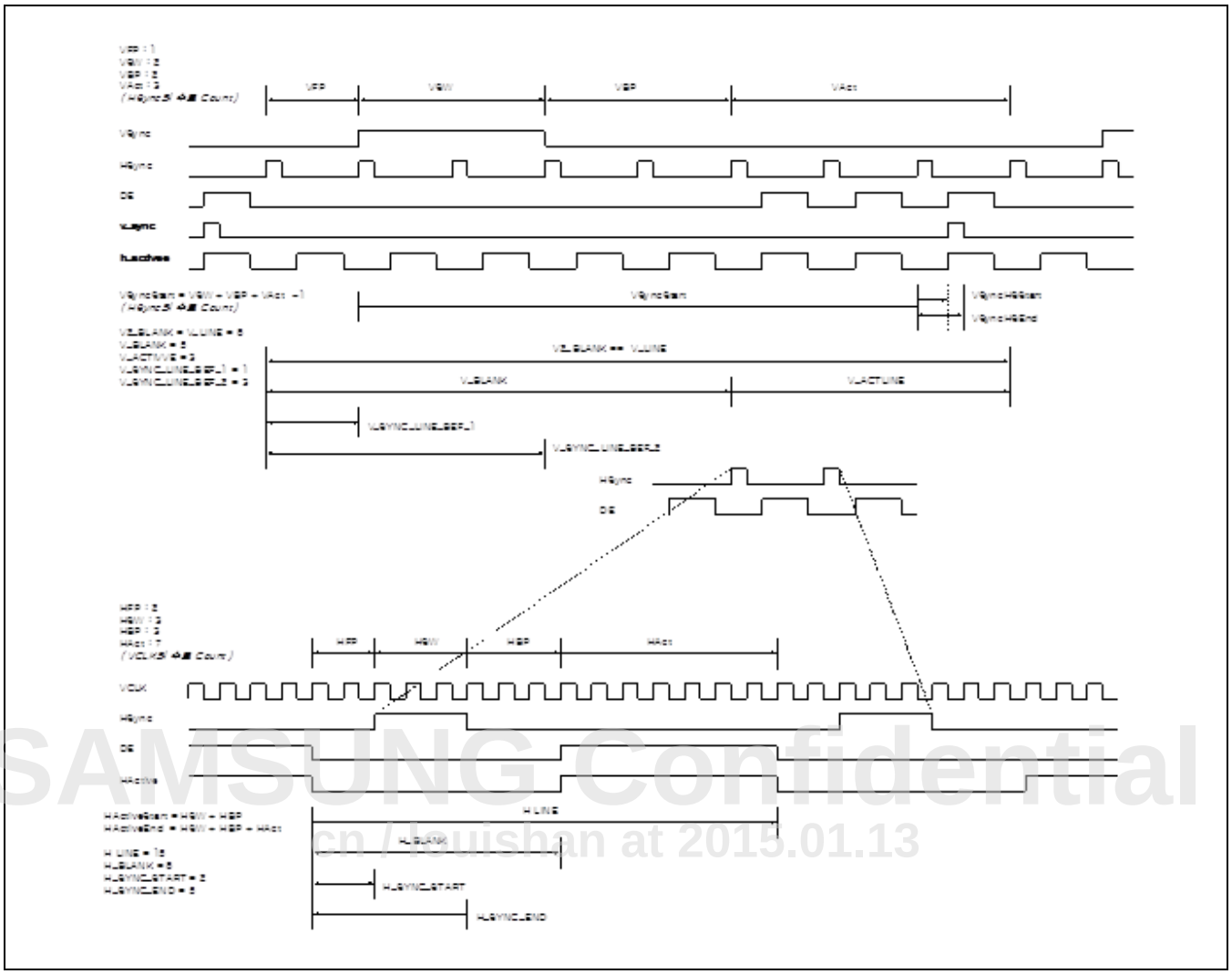


Figure 37-3 Video Sync Signal Timing Diagram

37.4.3 HDMI LINK

The HDMI Link receives a converted Video Data from the HDMI Converter. Also, the HDMI link receives an audio data from the SPDIFTX or I2S. The HDMI link translates them (video, audio) into a sequence of 10-bit signals compliant to HDMI v1.4 specification.

Users must set the configuration about video and audio.

37.4.3.1 Video Input Interface

Video input interface receives i_vsync, i_h_active, i_field and pixel data signals to identify the starting of a frame, the starting of a line and the starting of the top field in case of interlaced video formats. These signals, except for the pixel data, are different from VSYNC, HSYNC and DE signals in the CEA-861. Note that HSYNC and DE signal in CEA-861 are not used. Instead, actual vsync and hsync signals that are transferred to HDMI Rx side is generated inside hdmi_14tx_ss according to the register settings.

The i_vsync signal is activated only one cycle during active area period of the last line of the previous frame.i_h_active is always LOW as the blank period and HIGH during active period regardless of the video format. Note that i_h_active goes HIGH even in the vertical blank period. *Figure 37-4*, *Figure 37-5* show the timing diagrams for the three signals.

There are two sets of the registers related to video timing. One specifies the input timing and the other specifies the output timing. Video input/output timing with respect to the register values are also shown in *Figure 37-4*.Users must set the input-related registers in accordance with the input video timing. Users can use the output-related registers to control the video timing for display side, such as offset and display specific timing. Note that *Figure 37-4* and *Figure 37-5* is informative and is added to illustrate the relations between register values and video timing. It is recommended referring to register descriptions for exact timing.

Also, note that o_vsync, o_hsync and o_r/g/b in the figures are video timing signals described in CEA-861. These signals are generated inside hdmi_14tx_ss and is transferred to HDMI Rx.

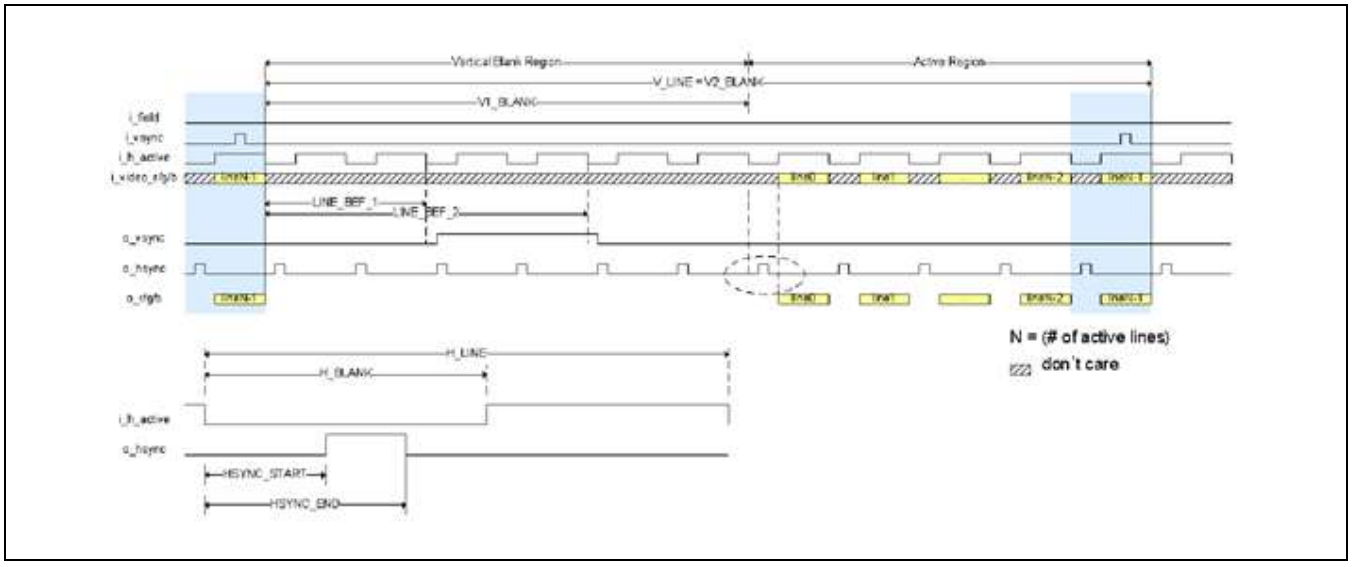


Figure 37-4 Video Timing with Respect to Register Values in Progressive Mode (Informative)

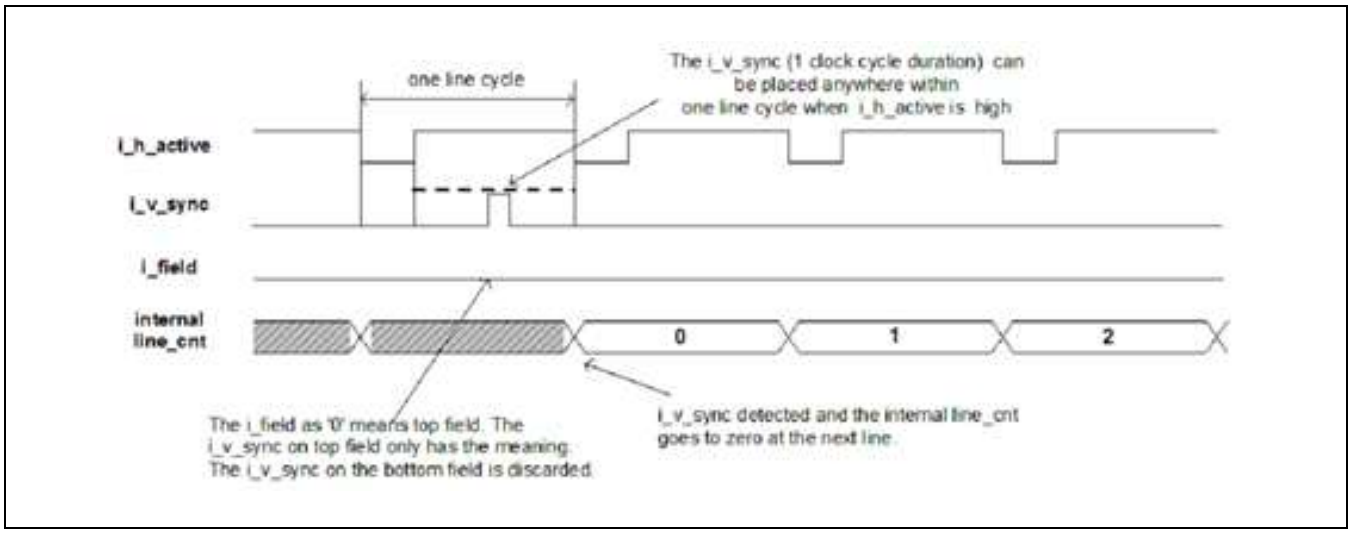


Figure 37-5 Video Input Interface timing

Below notations are used in the following explanations.

- o_h_sync is equal to o_hsync.
- o_v_sync is equal to o_vsync.
- v_line is equal to V_LINE.
- h_line is equal to H_LINE.
- h_sync_start is equal to HSYNC_START.
- h_sync_end is equal to HSYNC_END.
- h_blank is equal to H_BLANK.
- v1_blank is equal to V1_BLANK.
- v2_blank is equal to V2_BLANK.
- v_blank_f0 is equal to V_BLANK_F0.
- v_blank_f1 is equal to V_BLANK_F1.
- v_blank_f2 is equal to V_BLANK_F2.
- v_blank_f3 is equal to V_BLANK_F3.
- v_blank_f4 is equal to V_BLANK_F4.
- v_blank_f5 is equal to V_BLANK_F5.
- line_bef_1 is equal to LINE_BEF_1.
- line_bef_2 is equal to LINE_BEF_2.
- line_aft_1 is equal to LINE_AFT_1.
- line_aft_2 is equal to LINE_AFT_2.
- line_aft_3 is equal to LINE_AFT_3.
- line_aft_4 is equal to LINE_AFT_4.

- line_aft_pxl_1 is equal to LINE_AFT_PXL_1.
- line_aft_pxl_2 is equal to LINE_AFT_PXL_2.
- line_aft_pxl_3 is equal to LINE_AFT_PXL_3.
- line_aft_pxl_4 is equal to LINE_AFT_PXL_4.
- vact_space1 is equal to VACT_SPACE1.
- vact_space2 is equal to VACT_SPACE2.
- vact_space3 is equal to VACT_SPACE3.
- vact_space4 is equal to VACT_SPACE4.
- vact_space5 is equal to VACT_SPACE5.
- vact_space6 is equal to VACT_SPACE6.

Below figures indicate video timing per each mode.

In 2D Progressive mode, i_field and i_vsync input video signals indicate starting of image frame. When i_vsync input video signal is active, i_field should be low.

o_v_sync is generated by line_bef_1 and line_bef_2. o_v_sync goes high at h_sync_start pixel in line_bef_1 line and goes low at h_sync_start pixel in line_bef_2 line.

v2_blank should be equal to v_line.

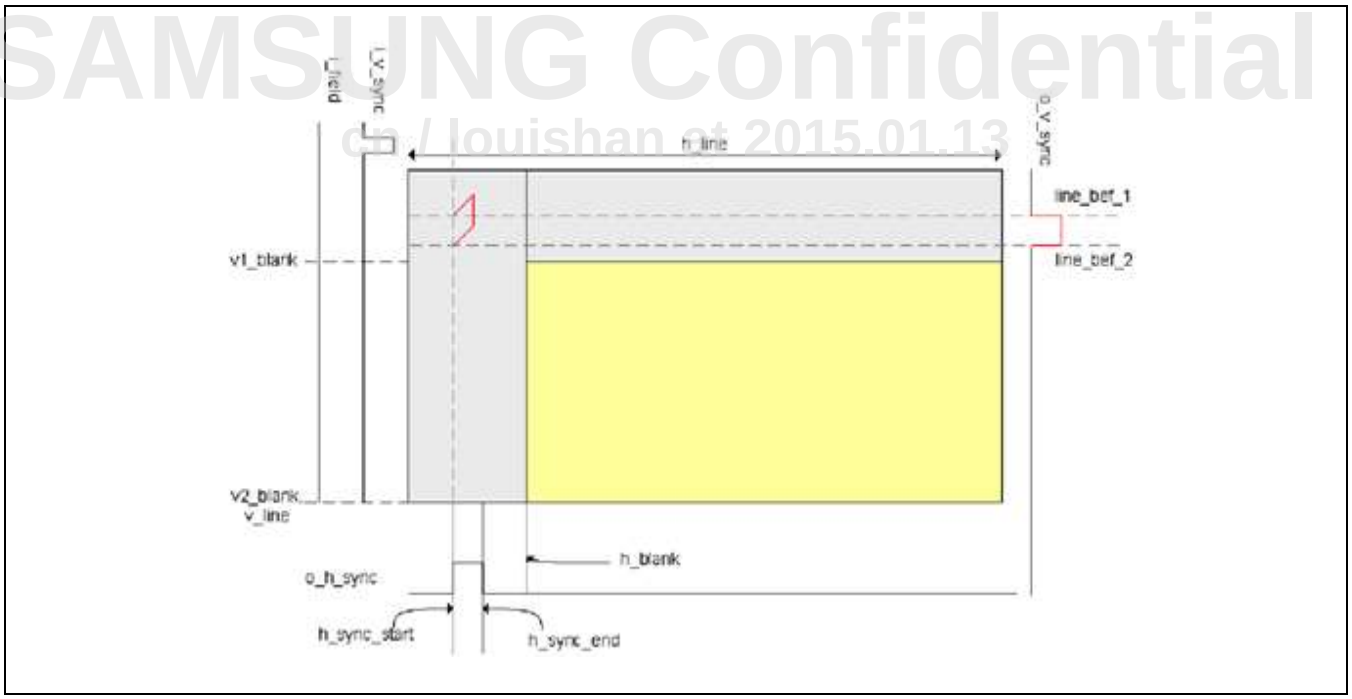


Figure 37-6 Progressive Video Timing

In 3D Frame Packing Progressive mode, i_field and i_vsync input video signals indicate starting of image frame.

When i_vsync input video signal is active, i_field should be low.

o_v_sync is generated by line_bef_1 and line_bef_2. o_v_sync is generated at h_sync_start in the lines.

Active space is indicated by vact_sapce1 line and vact_space2 line.

v2_blank should be equal to v_line.

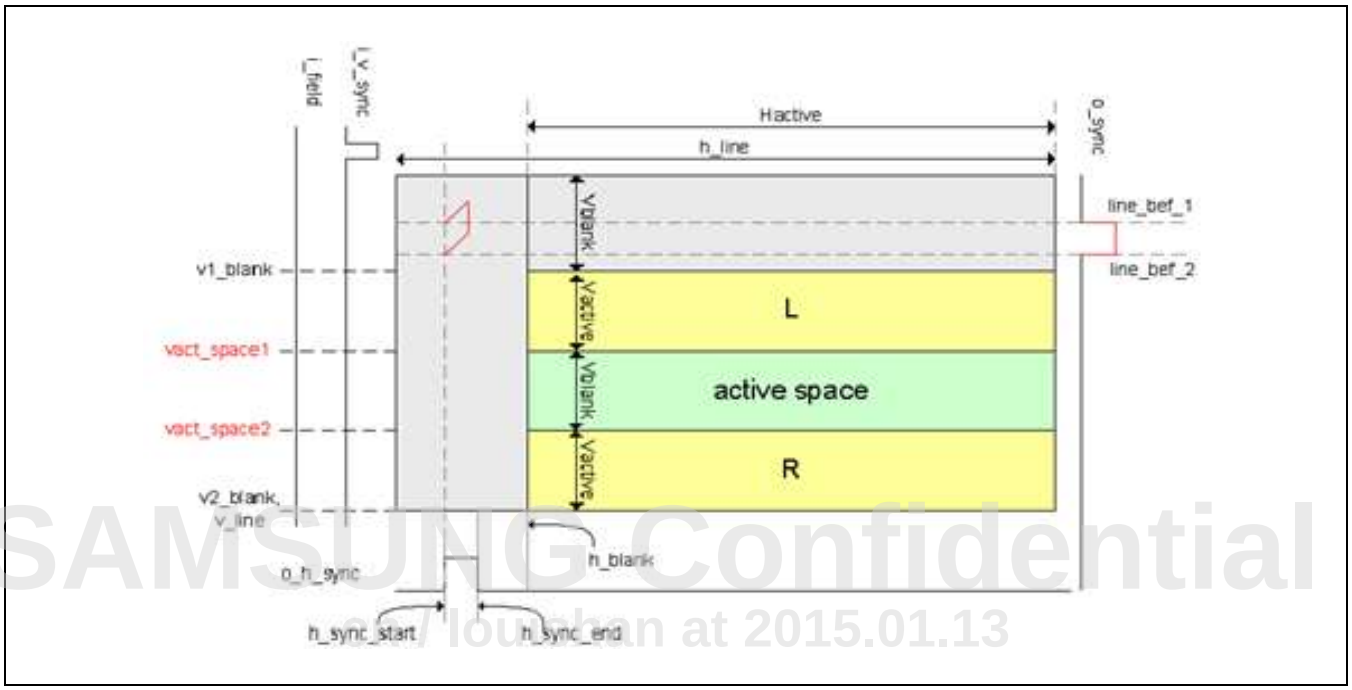


Figure 37-7 3D Frame Packing Progressive Video Timing

In 3D Side by side (half) Progressive mode, i_field and i_vsync input video signals indicate starting of image frame.

When i_vsync input video signal is active, i_field should be low.

o_v_sync is generated by line_bef_1 and line_bef_2. o_v_sync is generated at h_sync_start in the lines.

v2_blank should be equal to v_line.

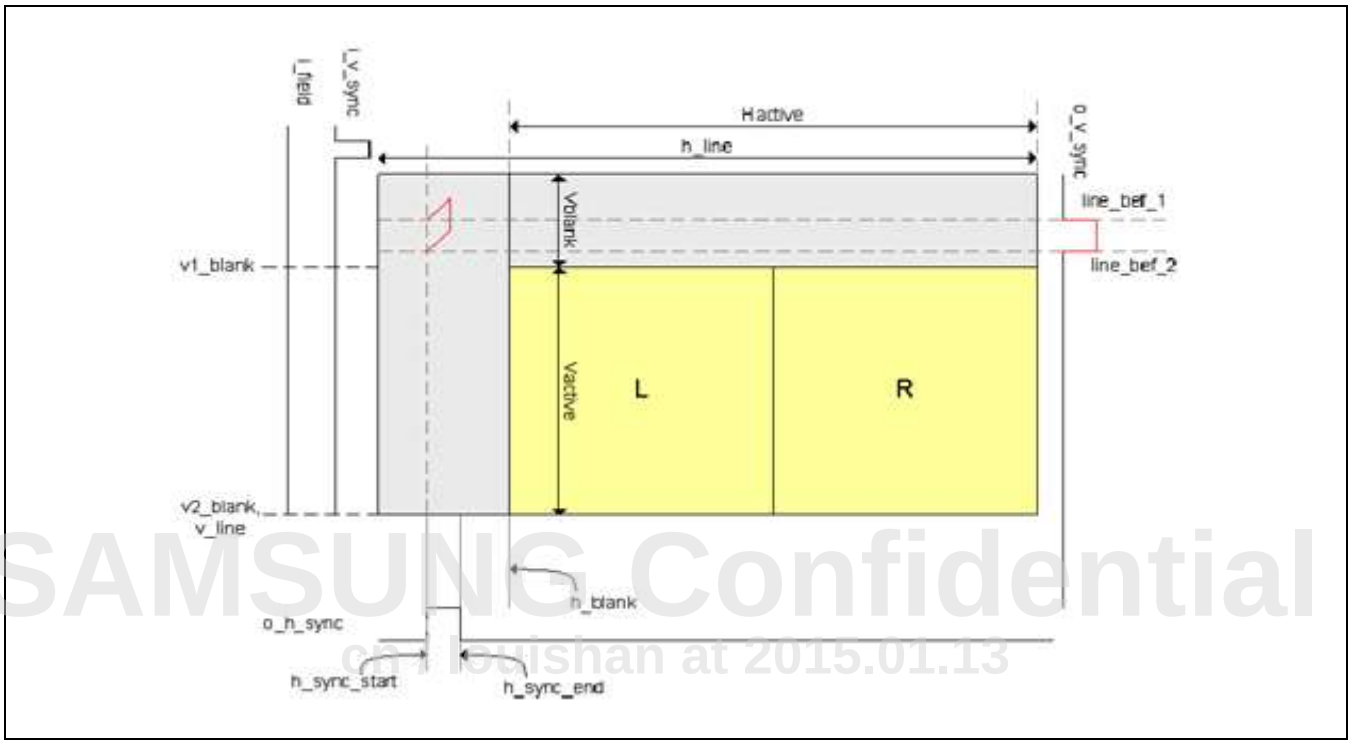


Figure 37-8 3D Side by Side (Half) Progressive Video Timing

In 3D Top and bottom Progressive mode, i_field and i_vsync input video signals indicate starting of image frame.

When i_vsync input video signal is active, i_field should be low.

o_v_sync is generated by line_bef_1 and line_bef_2. o_v_sync is generated at h_sync_start in the lines.

v2_blank should be equal to v_line.

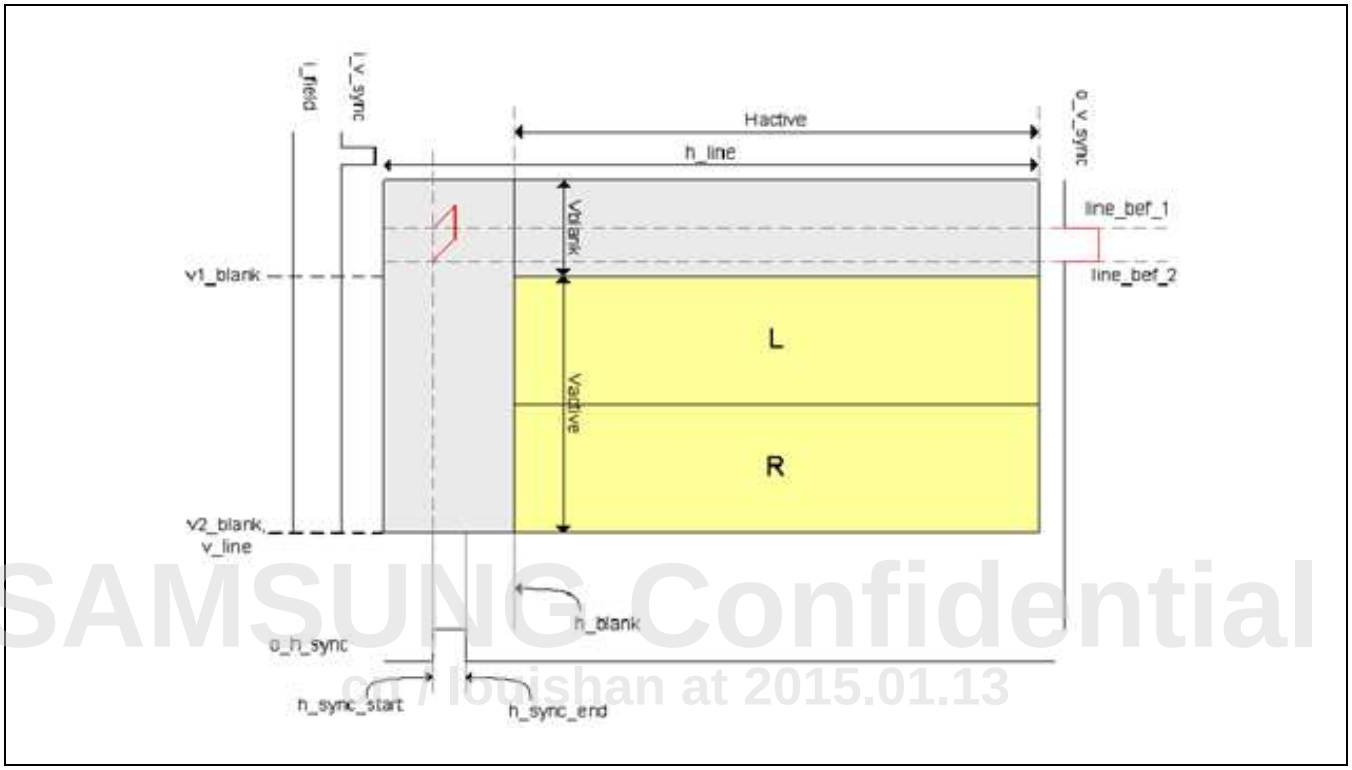


Figure 37-9 3D Top and Bottom Progressive Video Timing

In 3D Line Alternative mode, i_field and i_vsync input video signals indicate starting of image frame. When i_vsync input video signal is active, i_field should be low.

o_v_sync is generated by line_bef_1 and line_bef_2. o_v_sync is generated at h_sync_start in the lines.

v2_blank should be equal to v_line.

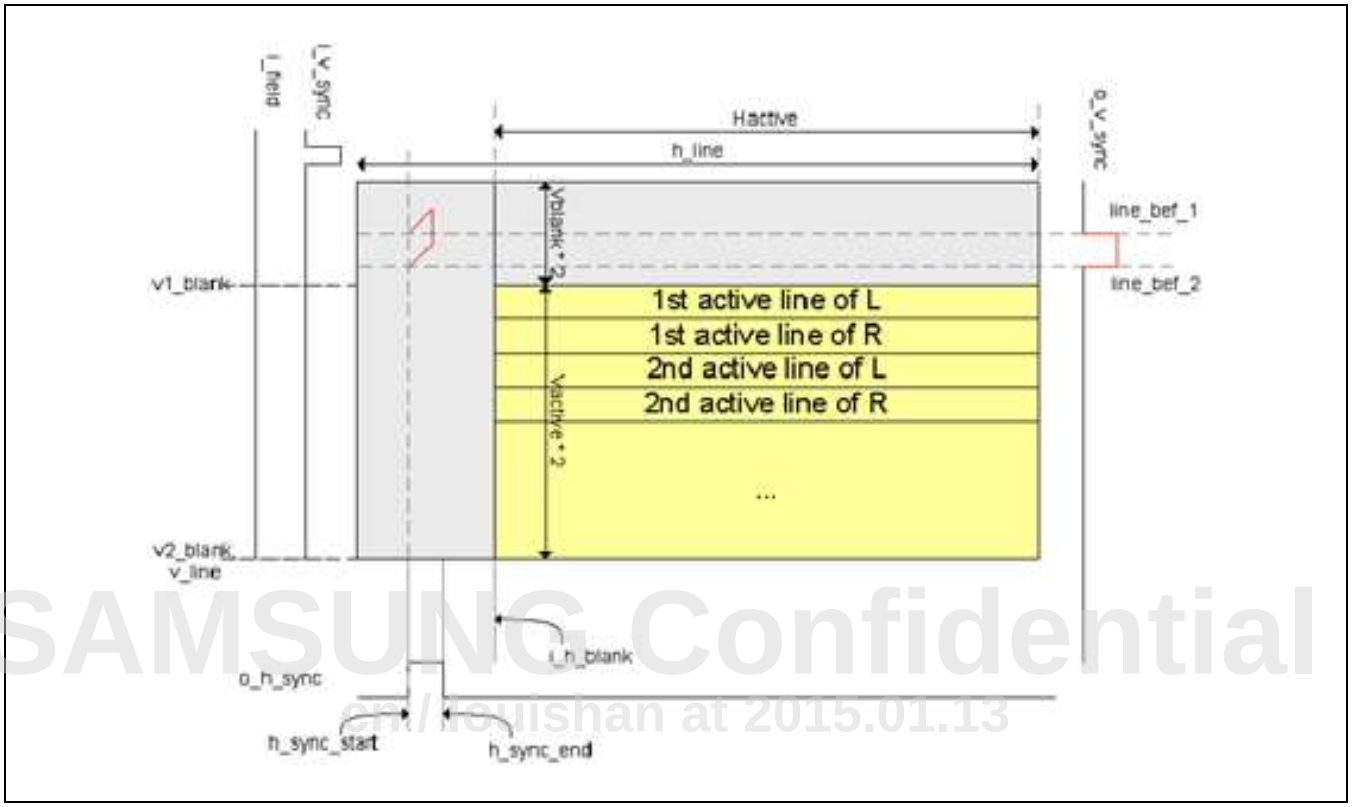


Figure 37-10 3D Line Alternative Video Timing

In 3D Side by side (full) Progressive mode, i_field and i_vsync input video signals indicate starting of image frame.

When i_vsync input video signal is active, i_field should be low.

o_v_sync is generated by line_bef_1 and line_bef_2. o_v_sync is generated at h_sync_start in the lines.

v2_blank should be equal to v_line.

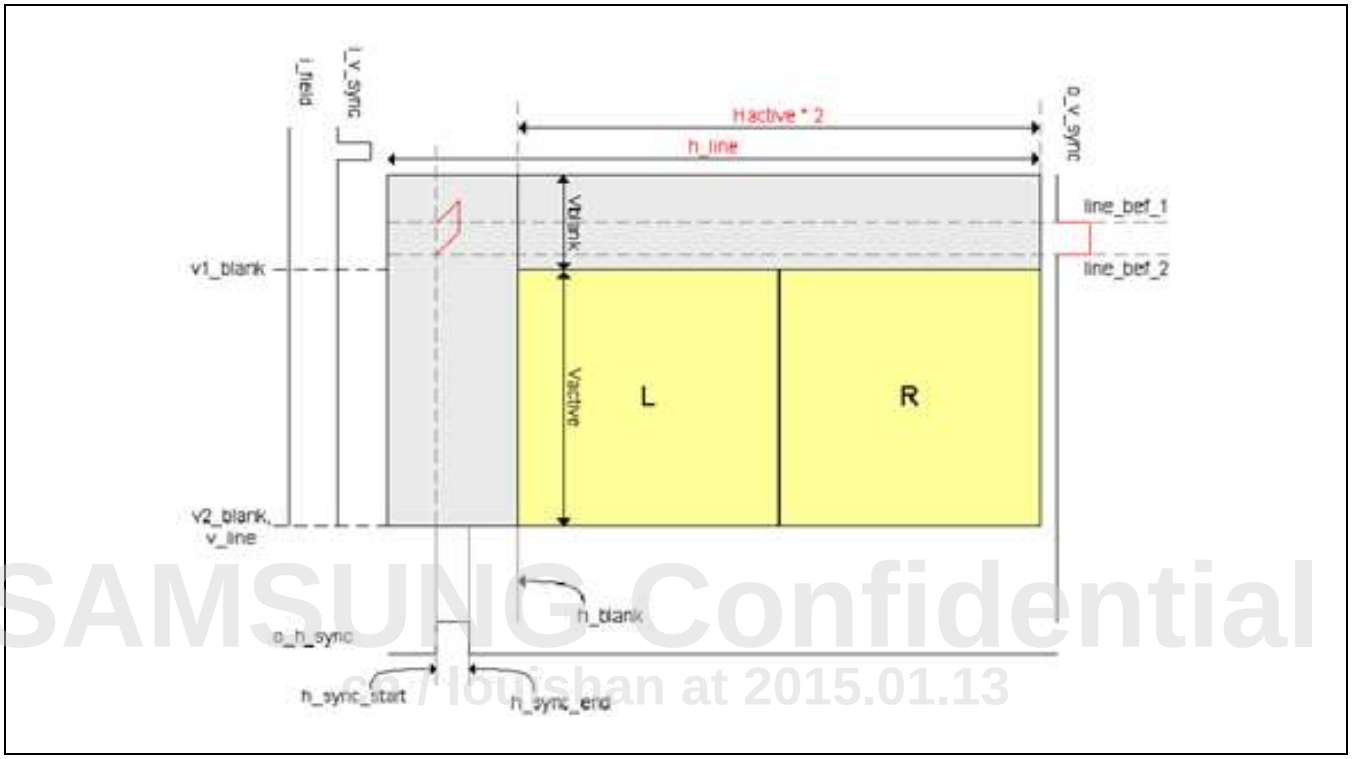


Figure 37-11 3D Side by Side (Full) Progressive Video Timing

In 3D L+Depth mode, i_field and i_vsync input video signals indicate starting of image frame. When i_vsync input video signal is active, i_field should be low.

o_v_sync is generated by line_bef_1 and line_bef_2. o_v_sync is generated at h_sync_start in the lines.

Active space is indicated by vact_sapce1 line and vact_space2 line.

v2_blank should be equal to v_line.

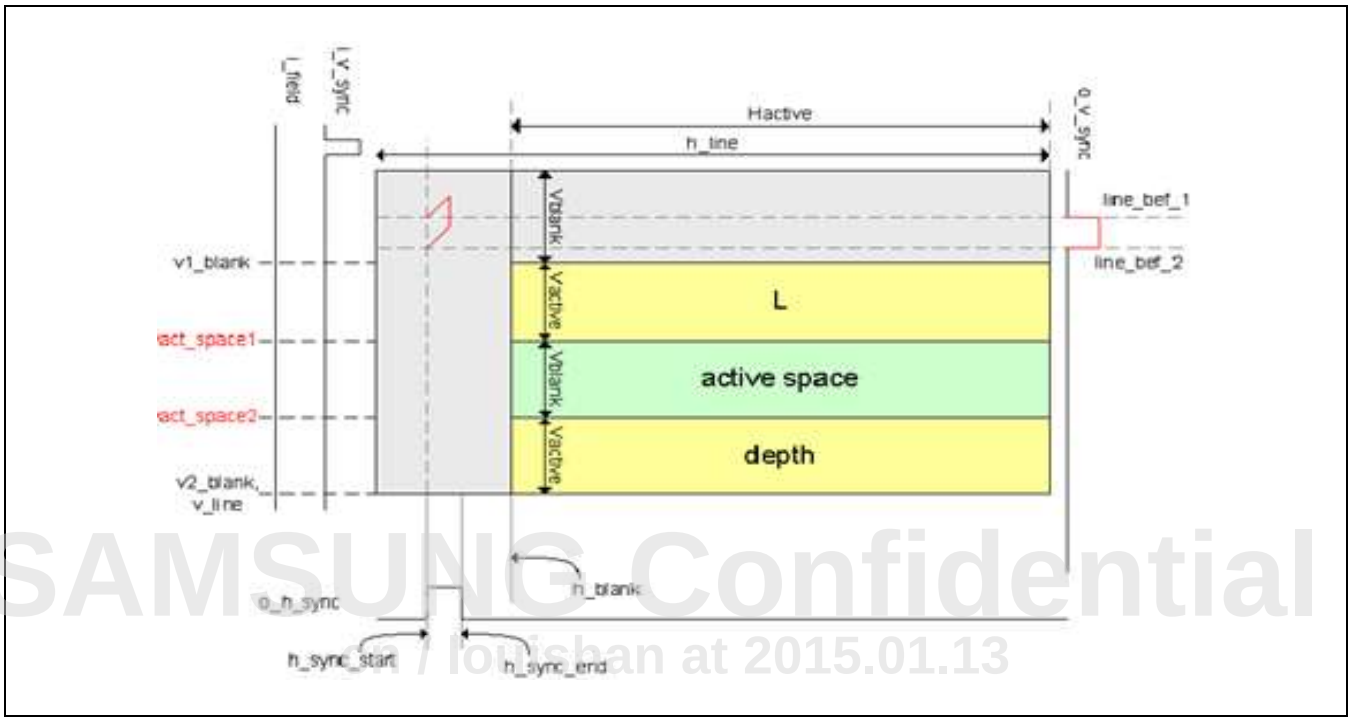


Figure 37-12 3D L + Depth Video

37.4.3.2 Audio Input Interface

The HDMI can decrypt AES-encrypted HDCP key. For HDMI with HDCP function, each device should have a unique HDCP key set.

HDMI 1.4 Tx Subsystem supports two audio input interfaces: SPDIF Rx, and I2S Rx. Users can use SPDIF interface for two-channel Linear or Non-linear PCM Audio transmission and I2S interface for up-to eight channel Linear PCM.

For I2S interface, users can specify the channel status block and the user bit information in registers, which does not inherently exist in I2S audio format.

SPDIF Interface

HDMI 1.4 Tx Subsystem supports SPDIF Interface format that follows the IEC-60958 and IEC-61937 format.
SPDIF

Interface

I2S Interface

I2S interface supports linear PCM, non-linear PCM

NOTE: Not supported HBR audio format.

37.4.3.3 HPD

HPD signal has two transactions: rising (plugged) and falling (unplugged) transition. Users can specify the stage number of the noise filter to reduce the possible glitches during transition.

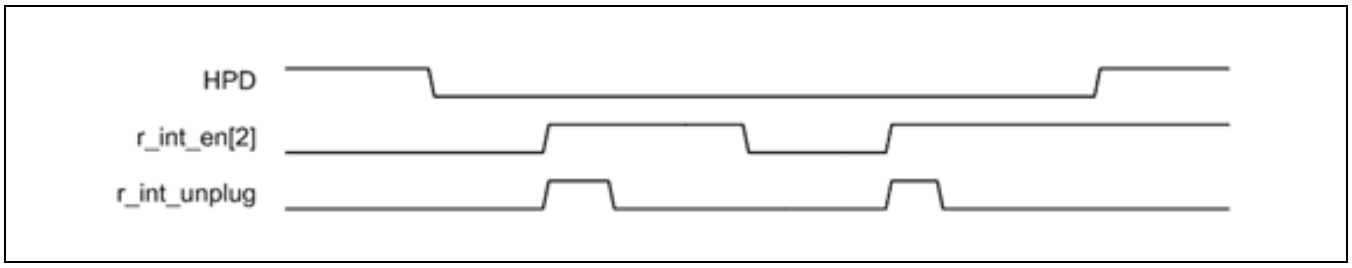


Figure 37-13 Timing Diagram for HPD Unplug Interrupt

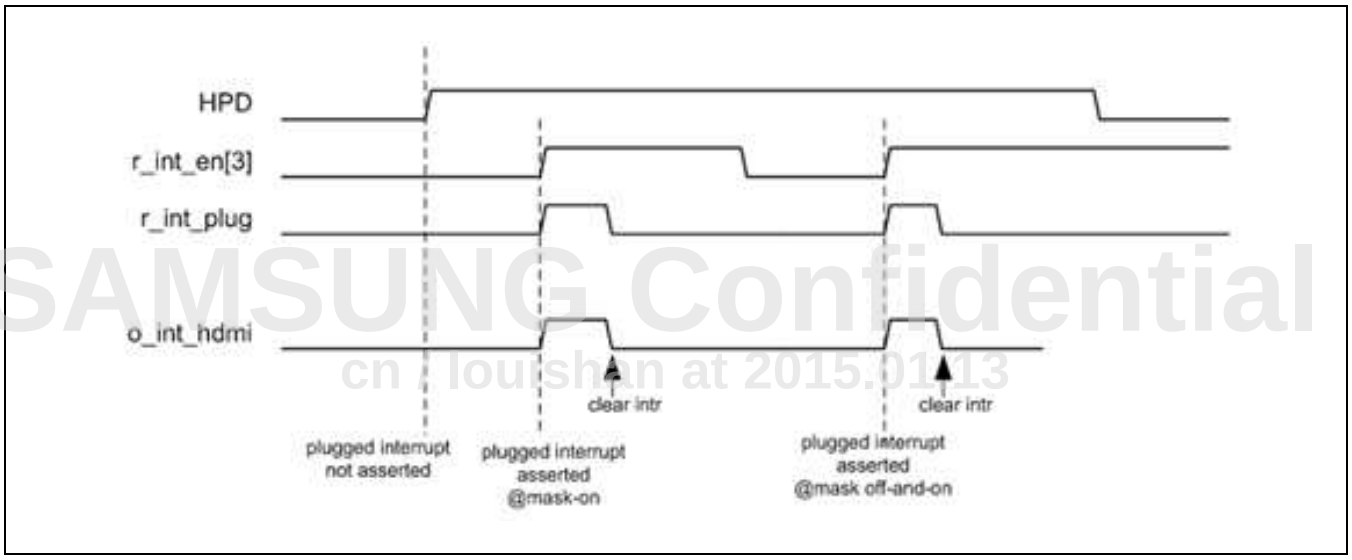


Figure 37-14 Timing Diagram for HPD Plug Interrupt

37.4.3.4 CEC

CEC is abbreviation of Consumer Electronics Control and is used for controlling devices connected to a one-wired "CEC bus". The CEC output port is a bidirectional port, which should be pulled-up to 3.3V using external resistor and voltage supply. (i.e. an open-drain connection)

CEC devices send messages serially (MSB first) via CEC bus and the receiving device sends acknowledge bit by pulling the bus to low at ACK bit timing. For timing of each bit and structure of a message, refer to HDMI specification 1.4a, Supplement 1. (CEC specification)

37.4.3.5 Interrupt Timing

HDMI 1.4 Tx Subsystem generates level-triggered interrupts. Interrupts are masked in two levels: each sub module and controller. On the other hand, interrupt clear happens only in sub module for all interrupts except HPD. For HPD, every plug and unplug will generate, HPD plug interrupt and HPD unplug interrupt, respectively.

37.4.3.6 HDCP KEY Management

The HDMI can decrypt AES-encrypted HDCP key. For HDMI with HDCP function, each device should have a unique HDCP key set. This key set is released by Digital Contents Protection. LLC (www.digital-cp.com).

HDCP key is stored outside of the HDMI Link at a non-volatile memory. It is important that the non-volatile memory does not have original raw-HDCP. The key should be stored safely to prevent the key from eavesdroppers.

The HDMI Link uses the AES encryption algorithm to protect plain HDCP key. Before starting the HDCP authentication protocol, The HDMI Link reads encrypts HDCP keys from the memory (MEM_encr), decrypts the keys using keys and stores the decrypted keys to decryption memory (MEM_decr). The decryption memory can only be accessed by the HDCP engine inside the HDMI Link. The decryption memory cannot be accessed by APB3 inter face to protect the decrypted keys. The AES key is supplied via ports (i_aeskey_data, i_aeskey_hw). For the AES key, various chip id and fixed hardware value can be used. Note that only 128-bit key is supported.

The AES decryption starts by setting AES_Start bit of AES_START register. When the decryption is finished and the decrypted keys are stored in the decryption memory, the AES_Start bit goes to 0, notifying the decryption is done. The size of data to decrypt can be set by AES_DATA_SIZE_H/L register. After checking that AES_Start bit is 0, decrypted data can be used for HDCP key. HDCP cannot operate until the AES_Start bit goes to 0.

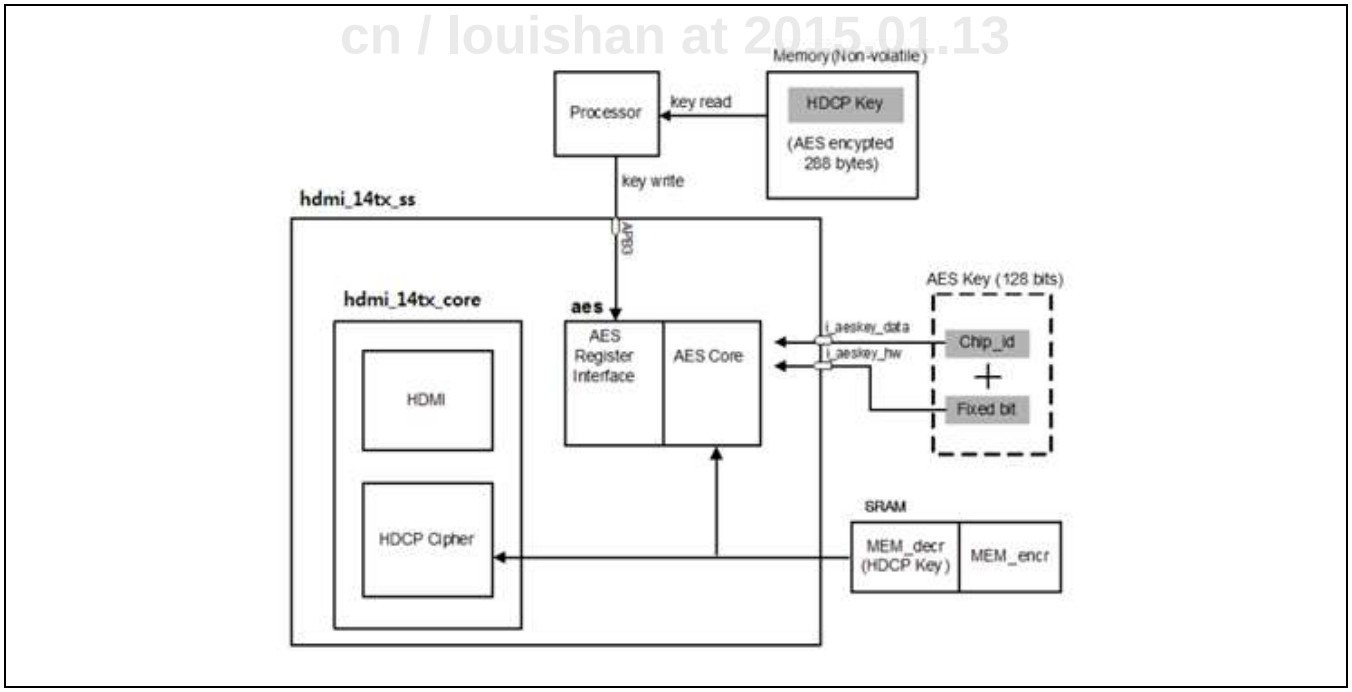


Figure 37-15 Block Diagram of HDCP Key Management

37.5 Register Description

37.5.1 Register Map Summary

- Base Address: 0xC020_0000

Register	Offset	Description	Reset Value
Control Registers			
INTC_CON_0	0x0000	Interrupt Control Register 0	0x00
INTC_FLAG_0	0x0004	Interrupt Flag Register 0	0x00
AESKEY_VALID	0x0008	i_aeskey_valid value	0x0X
HPD	0x000C	HPD signal	0x0X
INTC_CON_1	0x0010	Interrupt Control Register 1	0x00
INTC_FLAG_1	0x0014	Interrupt Flag Register 1	0x0X
PHY_STATUS_0	0x0020	PHY status Register 0	0x0X
PHY_STATUS_CMU	0x0024	PHY CMU status Register	0xXX
PHY_STATUS_PLL	0x0028	PHY PLL status Register	0xXX
PHY_CON_0	0x0030	PHY Control Register	0xXX
HPD_CTRL	0x0040	HPD Signal Control Register	0xXX
HPD_STATUS	0x0044	HPD Status Register	0xXX
HPD_TH_x	0x0050	HPD Status Register (HPD_TH_0 to 3)	0xXX

- Base Address: 0xC021_0000

Register	Offset	Description	Reset Value
Core Registers			
HDMI_CON_0	0x0000	HDMI system control register 0	0x00
HDMI_CON_1	0x0004	HDMI system control register 1	0x00
HDMI_CON_2	0x0008	HDMI system control register 2	0x00
STATUS	0x0010	HDMI system status register	0x00
STATUS_EN	0x0020	HDMI system status enable register	0x00
MODE_SEL	0x0040	HDMI/DVI mode selection	0x00
ENC_EN	0x0044	HDCP encryption enable register	0x00
HDMI_YMAX	0x0060	Maximum Y (or R,G,B) pixel value	0xEB
HDMI_YMIN	0x0064	Minimum Y (or R,G,B) pixel value	0x10
HDMI_CMAX	0x0068	Maximum Cb/Cr pixel value	0xF0
HDMI_CMIN	0x006C	Minimum Cb/Cr pixel value	0x10
H_BLANK_0	0x00A0	Horizontal blanking setting	0x00
H_BLANK_1	0x00A4	Horizontal blanking setting	0x00
V2_BLANK_0	0x00B0	Vertical blanking setting	0x00
V2_BLANK_1	0x00B4	Vertical blanking setting	0x00
V1_BLANK_0	0x00B8	Vertical blanking setting	0x00
V1_BLANK_1	0x00BC	Vertical blanking setting	0x00
V_LINE_0	0x00C0	vertical line setting	0x00
V_LINE_1	0x00C4	vertical line setting	0x00
H_LINE_0	0x00C8	Horizontal line setting	0x00
H_LINE_1	0x00CC	Horizontal line setting	0x00
HSYNC_POL	0x00E0	Horizontal sync polarity control register	0x00
VSYNC_POL	0x00E4	Vertical sync polarity control register	0x00
INT_PRO_MODE	0x00E8	Interlace/Progressive control register	0x00
V_BLANK_F0_0	0x0110	Vertical blanking setting for bottom field	0xFF
V_BLANK_F0_1	0x0114	Vertical blanking setting for bottom field	0x1F
V_BLANK_F1_0	0x0118	Vertical blanking setting for bottom field	0xFF
V_BLANK_F1_1	0x011C	Vertical blanking setting for bottom field	0x1F
H_SYNC_START_0	0x0120	Horizontal sync generation setting	0x00
H_SYNC_START_1	0x0124	Horizontal sync generation setting	0x00
H_SYNC_END_0	0x0128	Horizontal sync generation setting	0x00
H_SYNC_END_1	0x012C	Horizontal sync generation setting	0x00
V_SYNC_LINE_BEF_2_0	0x0130	Vertical sync generation for top field or frame	0xFF
V_SYNC_LINE_BEF_2_1	0x0134	Vertical sync generation for top field or frame	0x1F
V_SYNC_LINE_BEF_1_0	0x0138	Vertical sync generation for top field or frame	0xFF

Register	Offset	Description	Reset Value
V_SYNC_LINE_BEF_1_1	0x013C	Vertical sync generation for top field or frame	0x1F
V_SYNC_LINE_AFT_2_0	0x0140	Vertical sync generation for bottom field - vertical position	0xFF
V_SYNC_LINE_AFT_2_1	0x0144	Vertical sync generation for bottom field - vertical position	0x1F
V_SYNC_LINE_AFT_1_0	0x0148	Vertical sync generation for bottom field - vertical position	0xFF
V_SYNC_LINE_AFT_1_1	0x014C	Vertical sync generation for bottom field - vertical position	0x1F
V_SYNC_LINE_AFT_PXL_2_0	0x0150	Vertical sync generation for bottom field - horizontal position	0xFF
V_SYNC_LINE_AFT_PXL_2_1	0x0154	Vertical sync generation for bottom field - horizontal position	0x1F
V_SYNC_LINE_AFT_PXL_1_0	0x0158	Vertical sync generation for bottom field - horizontal position	0xFF
V_SYNC_LINE_AFT_PXL_1_1	0x015C	Vertical sync generation for bottom field - horizontal position	0x1F
V_BLANK_F2_0	0x0160	Vertical blanking setting for third field	0xFF
V_BLANK_F2_1	0x0164	Vertical blanking setting for third field	0x1F
V_BLANK_F3_0	0x0168	Vertical blanking setting for third field	0xFF
V_BLANK_F3_1	0x016C	Vertical blanking setting for third field	0x1F
V_BLANK_F4_0	0x0170	Vertical blanking setting for fourth field	0xFF
V_BLANK_F4_1	0x0174	Vertical blanking setting for fourth field	0x1F
V_BLANK_F5_0	0x0178	Vertical blanking setting for fourth field	0xFF
V_BLANK_F5_1	0x017C	Vertical blanking setting for fourth field	0x1F
V_SYNC_LINE_AFT_3_0	0x0180	Vertical sync generation for third field - vertical position	0xFF
V_SYNC_LINE_AFT_3_1	0x0184	Vertical sync generation for third field - vertical position	0x1F
V_SYNC_LINE_AFT_4_0	0x0188	Vertical sync generation for third field - vertical position	0xFF
V_SYNC_LINE_AFT_4_1	0x018C	Vertical sync generation for third field - vertical position	0x1F
V_SYNC_LINE_AFT_5_0	0x0190	Vertical sync generation for fourth field - vertical position	0xFF
V_SYNC_LINE_AFT_5_1	0x0194	Vertical sync generation for fourth field - vertical position	0x1F
V_SYNC_LINE_AFT_6_0	0x0198	Vertical sync generation for fourth field - vertical position	0xFF
V_SYNC_LINE_AFT_6_1	0x019C	Vertical sync generation for fourth field - vertical position	0x1F
V_SYNC_LINE_AFT_PXL_3_0	0x01A0	Vertical sync generation for third field - horizontal position	0xFF
V_SYNC_LINE_AFT_PXL_3_1	0x01A4	Vertical sync generation for third field - horizontal position	0x1F
V_SYNC_LINE_AFT_PXL_4_0	0x01A8	Vertical sync generation for third field - horizontal position	0xFF
V_SYNC_LINE_AFT_PXL_4_1	0x01AC	Vertical sync generation for third field - horizontal position	0x1F
V_SYNC_LINE_AFT_PXL_5_0	0x01B0	Vertical sync generation for fourth field - horizontal position	0xFF
V_SYNC_LINE_AFT_PXL_5_1	0x01B4	Vertical sync generation for fourth field - horizontal position	0x1F
V_SYNC_LINE_AFT_PXL_6_0	0x01B8	Vertical sync generation for fourth field - horizontal position	0xFF

Register	Offset	Description	Reset Value
V_SYNC_LINE_AFT_PXL_6_1	0x01BC	Vertical sync generation for fourth field - horizontal position	0x1F
VACT_SPACE1_0	0x01C0	1st Vertical Active Space start line	0xFF
VACT_SPACE1_1	0x01C4	1st Vertical Active Space end line	0x1F
VACT_SPACE2_0	0x01C8	1st Vertical Active Space start line	0xFF
VACT_SPACE2_1	0x01CC	1st Vertical Active Space end line	0x1F
VACT_SPACE3_0	0x01D0	2nd Vertical Active Space start line	0xFF
VACT_SPACE3_1	0x01D4	2nd Vertical Active Space end line	0x1F
VACT_SPACE4_0	0x01D8	2nd Vertical Active Space start line	0xFF
VACT_SPACE4_1	0x01DC	2nd Vertical Active Space end line	0x1F
VACT_SPACE5_0	0x01E0	3rd Vertical Active Space start line	0xFF
VACT_SPACE5_1	0x01E4	3rd Vertical Active Space end line	0x1F
VACT_SPACE6_0	0x01E8	3rd Vertical Active Space start line	0xFF
VACT_SPACE6_1	0x01EC	3rd Vertical Active Space end line	0x1F
GCP_CON	0x0200	GCP packet control register	0x04
GCP_BYTE1	0x0210	GCP packet body	0x00
GCP_BYTE2	0x0214	GCP packet body	0x00
GCP_BYTE3	0x0218	GCP packet body	0x00
ASP_CON	0x0300	ASP packet control register	0x00
ASP_SP_FLAT	0x0304	ASP packet sp_flat bit control	0x00
ASP_CHCFG0	0x0310	ASP audio channel configuration	0x08
ASP_CHCFG1	0x0314	ASP audio channel configuration	0x1A
ASP_CHCFG2	0x0318	ASP audio channel configuration	0x2C
ASP_CHCFG3	0x031C	ASP audio channel configuration	0x3E
ACR_CON	0x0400	ACR packet control register	0x00
ACR_MCTS0	0x0410	Measured CTS value	0x01
ACR_MCTS1	0x0414	Measured CTS value	0x00
ACR_MCTS2	0x0418	Measured CTS value	0x00
ACR_N0	0x0430	N value for ACR packet	0xE8
ACR_N1	0x0434	N value for ACR packet	0x03
ACR_N2	0x0438	N value for ACR packet	0x00
ACP_CON	0x0500	ACP packet control register	0x00
ACP_TYPE	0x0514	ACP packet header	0x00
ACP_DATAx	0x0520	ACP packet body	0x00
ISRC_CON	0x0600	ACR packet control register	0x00
ISRC1_HEADER1	0x0614	ISCR1 packet header	0x00
ISRC1_DATAx	0x0620	ISRC1 packet body	0x00

Register	Offset	Description	Reset Value
ISRC2_DATAx	0x06A0	ISRC2 packet body	0x00
AVI_CON	0x0700	AVI packet control register	0x00
AVI_HEADER0	0x0710	AVI packet header	0x00
AVI_HEADER1	0x0714	AVI packet header	0x00
AVI_HEADER2	0x0718	AVI packet header	0x00
AVI_CHECK_SUM	0x071C	AVI packet checksum	0x00
AVI_BYTEx	0x0720	AVI packet body	0x00
AUI_CON	0x0800	AUI packet control register	0x00
AUI_HEADER0	0x0810	AUI packet header	0x00
AUI_HEADER1	0x0814	AUI packet header	0x00
AUI_HEADER2	0x0818	AUI packet header	0x00
AUI_CHECK_SUM	0x081C	AUI packet checksum	0x00
AUI_BYTEx	0x0820	AUI packet body	0x00
MPG_CON	0x0900	ACR packet control register	0x00
MPG_CHECK_SUM	0x091C	MPG packet checksum	0x00
MPG_DATAx	0x0920	MPG packet body	0x00
SPD_CON	0x0A00	SPD packet control register	0x00
SPD_HEADER0	0x0A10	SPD packet header	0x00
SPD_HEADER1	0x0A14	SPD packet header	0x00
SPD_HEADER2	0x0A18	SPD packet header	0x00
SPD_DATAx	0x0A20	SPD packet body	0x00
GAMUT_CON	0x0B00	GAMUT packet control register	0x00
GAMUT_HEADER0	0x0B10	GAMUT packet header	0x00
GAMUT_HEADER1	0x0B14	GAMUT packet header	0x00
GAMUT_HEADER2	0x0B18	GAMUT packet header	0x00
GAMUT_METADATAx	0x0B20	GAMUT packet body	0x00
VSI_CON	0x0C00	VSI packet control register	0x00
VSI_HEADER0	0x0C10	VSI packet header	0x00
VSI_HEADER1	0x0C14	VSI packet header	0x00
VSI_HEADER2	0x0C18	VSI packet header	0x00
VSI_DATAx	0x0C20	VSI packet body	0x00
DC_CONTROL	0x0D00	Deep Color Control Register	0x00
VIDEO_PATTERN_GEN	0x0D04	Video Pattern Generation Register	0x00
An_Seed_Sel	0x0E48	An seed selection register.	0xFF
An_Seed_0	0x0E58	An seed value register	0x00
An_Seed_1	0x0E5C	An seed value register	0x00
An_Seed_2	0x0E60	An seed value register	0x00

Register	Offset	Description	Reset Value
An_Seed_3	0x0E64	An seed value register	0x00
HDCP_SHA1_x	0x7000	SHA-1 value from repeater	0x00
HDCP_KSV_LIST_x	0x7050	KSV list from repeater	0x00
HDCP_KSV_LIST_CON	0x7064	KSV list control	0x00
HDCP_SHA_RESULT	0x7070	SHA-1 checking result register	0x00
HDCP_CTRL1	0x7080	HDCP control register1	0x00
HDCP_CTRL2	0x7084	HDCP control register2	0x00
HDCP_CHECK_RESULT	0x7090	Ri and Pj value checking result	0x00
HDCP_BKSV_x	0x70A0	KSV of Rx	0x00
HDCP_AKSV_x	0x70C0	KSV of Tx	0x00
HDCP_An_x	0x70E0	An value	0x00
HDCP_BCAPS	0x7100	BCAPS from Rx	0x00
HDCP_BSTATUS_0	0x7110	BSTATUS from Rx	0x00
HDCP_BSTATUS_1	0x7114	BSTATUS from Rx	0x00
HDCP_Ri_0	0x7140	Ri value of Tx	0x00
HDCP_Ri_1	0x7144	Ri value of Tx	0x00
HDCP_I2C_INT	0x7180	I2C interrupt flag	0x00
HDCP_AN_INT	0x7190	An value ready interrupt flag	0x00
HDCP_WATCGDOG_INT	0x71A0	Watchdog interrupt flag	0x00
HDCP_Ri_INT	0x71B0	Ri value update interrupt flag	0x00
HDCP_Ri_Compare_0	0x71D0	HDCP Ri Interrupt Frame number index register 0	0x80
HDCP_Ri_Compare_1	0x71D4	HDCP Ri Interrupt Frame number index register 1	0x7F
HDCP_Frame_Count	0x71E0	Current value of the frame count index in the hardware	0x00
RGB_ROUND_EN	0xD500	round enable for 8/10 bit R/G/B in video_receiver	0x00
VACT_SPACE_R_0	0xD504	vertical active space R	0x00
VACT_SPACE_R_1	0xD508	vertical active space R	0x00
VACT_SPACE_G_0	0xD50C	vertical active space G	0x00
VACT_SPACE_G_1	0xD510	vertical active space G	0x00
VACT_SPACE_B_0	0xD514	vertical active space B	0x00
VACT_SPACE_B_1	0xD518	vertical active space B	0x00
BLUE_SCREEN_R_0	0xD520	R Pixel values for blue screen [3:0]	0x00
BLUE_SCREEN_R_1	0xD524	R Pixel values for blue screen [11:4]	0x00
BLUE_SCREEN_G_0	0xD528	G Pixel values for blue screen [3:0]	0x00
BLUE_SCREEN_G_1	0xD52C	G Pixel values for blue screen [11:4]	0x00
BLUE_SCREEN_B_0	0xD530	B Pixel values for blue screen [3:0]	0x00
BLUE_SCREEN_B_1	0x0D534	B Pixel values for blue screen [11:4]	0x00

- Base Address: 0xC022_0000

Register	Offset	Description	Reset Value
AES Registers			
AES_START	0x0000	AES_START	0x00
AES_DATA_SIZE_L	0x0020	AES_DATA_SIZE_L	0x20
AES_DATA_SIZE_H	0x0024	AES_DATA_SIZE_H	0x01
AES_DATA	0x0040	AES_DATA	0x00

- Base Address: 0xC023_0000

Register	Offset	Description	Reset Value
SPDIF Registers			
SPDIFIN_CLK_CTRL	0x0000	SPDIFIN Clock Control Register	0x02
SPDIFIN_OP_CTRL	0x0004	SPDIFIN Operation Control Register 1	0x00
SPDIFIN_IRQ_MASK	0x0008	SPDIFIN Interrupt Request Mask Register	0x00
SPDIFIN_IRQ_STATUS	0x000C	SPDIFIN Interrupt Request Status Register	0x00
SPDIFIN_CONFIG_1	0x0010	SPDIFIN Configuration Register 1	0x02
SPDIFIN_CONFIG_2	0x0014	SPDIFIN Configuration Register 2	0x00
SPDIFIN_USER_VALUE_1	0x0020	SPDIFIN User Value Register 1	0x00
SPDIFIN_USER_VALUE_2	0x0024	SPDIFIN User Value Register 2	0x00
SPDIFIN_USER_VALUE_3	0x0028	SPDIFIN User Value Register 3	0x00
SPDIFIN_USER_VALUE_4	0x002C	SPDIFIN User Value Register 4	0x00
SPDIFIN_CH_STATUS_0_1	0x0030	SPDIFIN Channel Status Register 0-1	0x00
SPDIFIN_CH_STATUS_0_2	0x0034	SPDIFIN Channel Status Register 0-2	0x00
SPDIFIN_CH_STATUS_0_3	0x0038	SPDIFIN Channel Status Register 0-3	0x00
SPDIFIN_CH_STATUS_0_4	0x003C	SPDIFIN Channel Status Register 0-4	0x00
SPDIFIN_CH_STATUS_1	0x0040	SPDIFIN Channel Status Register 1	0x00
SPDIFIN_FRAME_PERIOD_1	0x0048	SPDIFIN Frame Period Register 1	0x00
SPDIFIN_FRAME_PERIOD_2	0x004C	SPDIFIN Frame Period Register 2	0x00
SPDIFIN_Pc_INFO_1	0x0050	SPDIFIN Pc Info Register 1	0x00
SPDIFIN_Pc_INFO_2	0x0054	SPDIFIN Pc Info Register 2	0x00
SPDIFIN_Pd_INFO_1	0x0058	SPDIFIN Pd Info Register 1	0x00
SPDIFIN_Pd_INFO_2	0x005C	SPDIFIN Pd Info Register 2	0x00
SPDIFIN_DATA_BUF_0_1	0x0060	SPDIFIN Data Buffer Register 0_1	0x00
SPDIFIN_DATA_BUF_0_2	0x0064	SPDIFIN Data Buffer Register 0_2	0x00
SPDIFIN_DATA_BUF_0_3	0x0068	SPDIFIN Data Buffer Register 0_3	0x00
SPDIFIN_USER_BUF_0	0x006C	SPDIFIN User Buffer Register 0	0x00
SPDIFIN_DATA_BUF_1_1	0x0070	SPDIFIN Data Buffer Register 1_1	0x00

Register	Offset	Description	Reset Value
SPDIFIN_DATA_BUF_1_2	0x0074	SPDIFIN Data Buffer Register 1_2	0x00
SPDIFIN_DATA_BUF_1_3	0x0078	SPDIFIN Data Buffer Register 1_3	0x00
SPDIFIN_USER_BUF_1	0x007C	SPDIFIN User Buffer Register 1	0x00

- Base Address: 0xC024_0000

Register	Offset	Description	Reset Value
I2S Registers			
I2S_CLK_CON	0x0000	I2S Clock Enable Register	0x00
I2S_CON_1	0x0004	I2S Control Register 1	0x00
I2S_CON_2	0x0008	I2S Control Register 2	0x16
I2S_PIN_SEL_0	0x000C	I2S Input Pin Selection Register 0	0x77
I2S_PIN_SEL_1	0x0010	I2S Input Pin Selection Register 1	0x77
I2S_PIN_SEL_2	0x0014	I2S Input Pin Selection Register 2	0x77
I2S_PIN_SEL_3	0x0018	I2S Input Pin Selection Register 3	0x07
I2S_DSD_CON	0x001C	I2S DSD Control Register	0x02
I2S_MUX_CON	0x0020	I2S In/Mux Control Register	0x60
I2S_CH_ST_CON	0x0024	I2S Channel Status Control Register	0x00
I2S_CH_ST_0	0x0028	I2S Channel Status Block 0	0x00
I2S_CH_ST_1	0x002C	I2S Channel Status Block 1	0x00
I2S_CH_ST_2	0x0030	I2S Channel Status Block 2	0x00
I2S_CH_ST_3	0x0034	I2S Channel Status Block 3	0x00
I2S_CH_ST_4	0x0038	I2S Channel Status Block 4	0x00
I2S_CH_ST_SH_0	0x003C	I2S Channel Status Block Shadow Register 0	0x00
I2S_CH_ST_SH_1	0x0040	I2S Channel Status Block Shadow Register 1	0x00
I2S_CH_ST_SH_2	0x0044	I2S Channel Status Block Shadow Register 2	0x00
I2S_CH_ST_SH_3	0x0048	I2S Channel Status Block Shadow Register 3	0x00
I2S_CH_ST_SH_4	0x004C	I2S Channel Status Block Shadow Register 4	0x00
I2S_VD_DATA	0x0050	I2S Audio Sample Validity Register	0x00
I2S_MUX_CH	0x0054	I2S Channel Enable Register	0x03
I2S_MUX_CUV	0x0058	I2S CUV Enable Register	0x03
I2S_CH0_L_0	0x0064	I2S PCM Output Data Register	0x00
I2S_CH0_L_1	0x0068	I2S PCM Output Data Register	0x00
I2S_CH0_L_2	0x006C	I2S PCM Output Data Register	0x00
I2S_CH0_R_0	0x0074	I2S PCM Output Data Register	0x00
I2S_CH0_R_1	0x0078	I2S PCM Output Data Register	0x00

Register	Offset	Description	Reset Value
I2S_CH0_R_2	0x007C	I2S PCM Output Data Register	0x00
I2S_CH0_R_3	0x0080	I2S PCM Output Data Register	0x00
I2S_CH1_L_0	0x0084	I2S PCM Output Data Register	0x00
I2S_CH1_L_1	0x0088	I2S PCM Output Data Register	0x00
I2S_CH1_L_2	0x008C	I2S PCM Output Data Register	0x00
I2S_CH1_L_3	0x0090	I2S PCM Output Data Register	0x00
I2S_CH1_R_0	0x0094	I2S PCM Output Data Register	0x00
I2S_CH1_R_1	0x0098	I2S PCM Output Data Register	0x00
I2S_CH1_R_2	0x009C	I2S PCM Output Data Register	0x00
I2S_CH1_R_3	0x00A0	I2S PCM Output Data Register	0x00
I2S_CH2_L_0	0x00A4	I2S PCM Output Data Register	0x00
I2S_CH2_L_1	0x00A8	I2S PCM Output Data Register	0x00
I2S_CH2_L_2	0x00AC	I2S PCM Output Data Register	0x00
I2S_CH2_L_3	0x00B0	I2S PCM Output Data Register	0x00
I2S_CH2_R_0	0x00B4	I2S PCM Output Data Register	0x00
I2S_CH2_R_1	0x00B8	I2S PCM Output Data Register	0x00
I2S_CH2_R_2	0x00BC	I2S PCM Output Data Register	0x00
I2S_Ch2_R_3	0x00C0	I2S PCM Output Data Register	0x00
I2S_CH3_L_0	0x00C4	I2S PCM Output Data Register	0x00
I2S_CH3_L_1	0x00C8	I2S PCM Output Data Register	0x00
I2S_CH3_L_2	0x00CC	I2S PCM Output Data Register	0x00
I2S_CH3_R_0	0x00D0	I2S PCM Output Data Register	0x00
I2S_CH3_R_1	0x00D4	I2S PCM Output Data Register	0x00
I2S_CH3_R_2	0x00D8	I2S PCM Output Data Register	0x00
I2S_CUV_L_R	0x00DC	I2S CUV Output Data Register	0x00

- Base Address: 0xC010_0000

Register	Offset	Description	Reset Value
CEC Registers			
CEC_TX_STATUS_0	0x0000	CEC Tx status registers 0.	0x00
CEC_TX_STATUS_1	0x0004	CEC Tx status registers 1. Number of blocks transferred.	0x00
CEC_RX_STATUS_0	0x0008	CEC Rx status registers 0.	0x00
CEC_RX_STATUS_1	0x000C	CEC Rx status registers 1. Number of blocks received.	0x00
CEC_INTR_MASK	0x0010	CEC interrupt mask register	0x00
CEC_INTR_CLEAR	0x0014	CEC interrupt clear register	0x00
CEC_LOGIC_ADDR	0x0020	HDMI Tx logical address register	0x0F
CEC_DIVISOR_0	0x0030	Clock divisor for 0.05ms period count ([7:0] of 32-bit)	0x00
CEC_DIVISOR_1	0x0034	Clock divisor for 0.05ms period count ([15:8] of 32-bit)	0x00
CEC_DIVISOR_2	0x0038	Clock divisor for 0.05ms period count ([23:16] of 32-bit)	0x00
CEC_DIVISOR_3	0x003C	Clock divisor for 0.05ms period count ([31:24] of 32-bit)	0x00
CEC_TX_CTRL	0x0040	CEC Tx control register	0x10
CEC_TX_BYTE_NUM	0x0044	Number of blocks in a message to be transferred	0x00
CEC_TX_STATUS_2	0x0060	CEC Tx status register 2	0x00
CEC_TX_STATUS_3	0x0064	CEC Tx status register 3	0x00
CEC_TX_BUFFER_x	0x0080	Byte #0 to #15 of CEC message to be transferred. (#0 is transferred 1st)	0x00
CEC_RX_CTRL	0x00C0	CEC Rx control register	0x00
CEC_RX_STATUS_2	0x00E0	CEC Rx status register 2	0x00
CEC_RX_STATUS_3	0x00E4	CEC Rx status register 3	0x00
CEC_RX_BUFFER_x	0x0100	Byte #0 to #15 of CEC message received (#0 is received 1st)	0x00
CEC_FILTER_CTRL	0x0180	CEC Filter control register	0x81
CEC_FILTER_TH	0x0184	CEC Filter Threshold register	0x03

37.5.1.1 Control Registers

37.5.1.1.1 INTC_CON_0

- Base Address: 0xC020_0000
- Address = Base Address + 0x0000, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
IntrPol	[7]	RW	Interrupt Polarity 0 = Active high 1 = Active low	0x0
IntrEnGlobal	[6]	RW	0 = All interrupts are disabled 1 = Interrupts are enabled or disabled by INTC_CON5:0]	0x0
RSVD	[5]	RW	Reserved	0x0
IntrEnCEC	[4]	RW	CEC interrupt enable 0 = Disabled 1 = Enabled	0x0
IntrEnHPDplug	[3]	RW	HPD plugged interrupt enable 0 = Disabled 1 = Enabled	0x0
IntrEnHPDunplug	[2]	RW	HPD unplugged interrupt enable 0 = Disabled 1 = Enabled	0x0
IntrEnSPDIF	[1]	RW	SPDIF interrupt enable 0 = Disabled 1 = Enabled	0x0
IntrEnHDCP	[0]	RW	HDCP interrupt enable 0 = Disabled 1 = Enabled	0x0

37.5.1.1.2 INTC_FLAG_0

- Base Address: 0xC020_0000
- Address = Base Address + 0x0004, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	0x0
RSVD	[5]	RW	Reserved	0x0
IntrCEC	[4]	RW	CEC interrupt flag. (read only) 0 = Not occurred 1 = Interrupt occurred	0x0
IntrHPDplug	[3]	RW	HPD plugged interrupt flag. If it is written by 1, it is cleared. 0 = Not occurred 1 = HPD plugged	0x0
IntrHPDunplug	[2]	RW	HPD unplugged interrupt flag. If it is written by 1, it is cleared. 0 = Not occurred 1 = HPD unplugged	0x0
IntrSPDIF	[1]	RW	SPDIF interrupt flag. (read only) 0 = Not occurred 1 = Interrupt occurred	0x0
IntrHDCP	[0]	RW	HDCP interrupt flag. (read only) 0 = Not occurred 1 = Interrupt occurred	0x0

37.5.1.1.3 AESKEY_VALID

- Base Address: 0xC020_0000
- Address = Base Address + 0x0008, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	R	Reserved	-
aeskey_valid	[0]	R	Reflects i_aeskey_valid signal value.	-

37.5.1.1.4 HPD

- Base Address: 0xC020_0000
- Address = Base Address + 0x000C, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	R	Reserved	-
HPD_Value	[0]	R	Value of HPD signal 0 = Unplugged 1 = Plugged	-

37.5.1.1.5 INTC_CON_1

- Base Address: 0xC020_0000
- Address = Base Address + 0x0010, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
IntEnSinkDetect	[1]	RW	SINK_DET interrupt enable. Triggered when SINK_DET signal from goes PHY high. INTC_CON_1[6] should also be enabled. 0 = Disabled 1 = Enabled	1'b0
IntEnSinknotDetect	[0]	RW	SINK_NOT_DET interrupt enable. Triggered when SINK_DET signal from PHY goes low. INTC_CON_1[6] should also be enabled. 0 = Disabled 1 = Enabled	1'b0

37.5.1.1.6 INTC_FLAG_1

- Base Address: 0xC020_0000
- Address = Base Address + 0x0014, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
IntSinkDetect	[1]	RW	SINK_DET interrupt. Triggered when SINK_DET signal from PHY goes high. INTC_CON_1[6] should also be enabled. If it is written by 1, it is cleared. 0 = Not occurred 1 = SINK_DET positive edge occurred.	-
IntSinknotDetect	[0]	RW	SINK_NOT_DET interrupt. Triggered when SINK_DET signal from PHY goes low. INTC_CON_1[6] should also be enabled. If it is written by 1, it is cleared. 0 = Not occurred 1 = SINK_DET negative edge occurred.	-

37.5.1.1.7 PHY_STATUS_0

- Base Address: 0xC020_0000
- Address = Base Address + 0x0020, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	R	Reserved	-
Sink_Detect	[1]	R	SINK_DET signal from PHY. 0 = Sink not detected 1 = Sink detected	
Phy_Ready	[0]	R	PHY_READY signal from PHY. 0 = PHY not ready 1 = PHY ready	

37.5.1.1.8 PHY_STATUS_CMU

- Base Address: 0xC020_0000
- Address = Base Address + 0x0024, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
CMU_Code	[7:4]	R	CMU_CODE signal from PHY. CMU_CODE is the AFC (automatic frequency calibration) code that is used by the CMU to converge to the target frequency. To lock the CMU, PLL that generated TMDS clock and the pixel clock generator should be locked.	-
RSVD	[3:1]	R	Reserved	-
CMU_Lock	[0]	R	CMU_LOCK signal from PHY. 0 = CMU not locked 1 = CMU locked	-

37.5.1.1.9 PHY_STATUS_PLL

- Base Address: 0xC020_0000
- Address = Base Address + 0x0028, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
PLL_Code	[7:4]	R	VPLL_CODE signal from PHY. VPLL_CODE is the AFC (automatic frequency calibration) code that is used by the VPLL to converge to the target TMDS frequency.	-
RSVD	[3:1]	R	Reserved	-
PLL_Lock	[0]	R	VPLL_LOCK signal from PHY. 0 = VPLL not locked 1 = VPLL locked	-

37.5.1.1.10 PHY_CON_0

- Base Address: 0xC020_0000
- Address = Base Address + 0x0030, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
PHY_Pwr_Off	[0]	RW	PHY power off signal. Value of this bit is propagated to o_phy_pwroff port of hdmi_14tx_ss and when connected to PHY appropriately, can power-off the PHY. Refer to PHY datasheet for more information.	-

37.5.1.1.11 HPD_CTRL

- Base Address: 0xC020_0000
- Address = Base Address + 0x0040, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
HPD_Deglitch_En	[0]	RW	Enable deglitch logic to wait for a stable HPD signal. The duration of stable signal is determined by HPD_TH_0 to 3 registers.	-

37.5.1.1.12 HPD_STATUS

- Base Address: 0xC020_0000
- Address = Base Address + 0x0044, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
HPD_Deglitched	[0]	RW	Current HPD signal status after deglitch logic.	-

37.5.1.1.13 HPD_TH_x

- Base Address: 0xC020_0000
- Address = Base Address + 0x0050, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
HPD_TH_x	[7:0]	RW	A 32-bit HPD filter threshold value. When filter is enabled, it filters out signals stable for less than HPD_Th cycles. (based on APB cycle) Least significant byte first. For example, • HPD_Th[7:0] <= HPD_TH_0[7:0] • HPD_Th[31:24] <= HPD_TH_3[7:0]	-

37.5.1.2 Core Registers

37.5.1.2.1 HDMI_CON_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0000, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	-
Blue_Scr_En	[5]	RW	Blue screen mode control. When set, the input video pixels are discarded and BLUESCREEN register values are transmitted for all video data period. 0 = Disable 1 = Enable	1'b0
Encoding_Option	[4]	RW	10-bit TMDS encoding bit order option 0 = Bit order reverse among the 10-bit encoding (to be set to 1 when connecting to the TMDS PHY 1.3) 1 = Bit order as it is	1'b0
YCBCR422_Sel	[3]	RW	Video Input mode control. 0 = 4:4:4 mode 1 = 4:2:2 12-bit YCbCr When 8-bit mode, the 12-bit inputs are rounded up to generate 8-bit outputs.	1'b0
Asp_E	[2]	RW	Audio sample packet generation control. This bit is only valid when SYSTEM_EN is set. 0 = Discard audio sample 1 = When the audio sample is received, the audio sample packet is generated.	1'b0
Power_Down	[1]	RW	TMDS PHY power down mode. When it's set to 0, data could not be transferred to a receiver. 0 = Normal operation mode 1 = Power down	1'b0
System_En	[0]	RW	HDMI systems enable. 0 = No op. 1 = HDMI enable	1'b0

37.5.1.2.2 HDMI_CON_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0004, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
Pxl_Lmt_Ctrl	[6:5]	RW	Pixel value limitation control 0b00 = By-pass (Do not limit the pixel value) 0b01 = RGB mode All channel's video input pixels are limited according to YMAX and YMIN register values. 0b10 = YCbCr mode The value of I_VIDEO_G is limited according to YMAX and YMIN. The values of I_VIDEO_B and I_VIDEO_R are limited according to CMAX and CMIN. 0b11 = Reserved	2'b0
RSVD	[4:2]	RW	Reserved	-
Pxl_Rep_Ratio	[1:0]	RW	Pixel repetition ratio 0b00 = No pixel repetition 0b01 = 2 times repetition 0b10 = 3 times repetition 0b11 = 4 times repetition Use the resulting video mode setting for pixel repetition. e.g. For 720 × 480p (pixel repetition = 1) Use 1440x480p video mode	2'b0

37.5.1.2.3 HDMI_CON_2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0008, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	-
Vid_Period_En	[5]	RW	Video preamble control. 0 = Video Preamble is applied. (HDMI mode) 1 = Video Preamble is not applied (DVI mode)	1'b0
RSVD	[4:2]	RW	Reserved	-
Dvi_Band_En	[1]	RW	In DIV mode, the leading guard band is not used. 0 = Guard band is applied (HDMI mode) 1 = Guard band is not applied (DVI mode)	1'b0
RSVD	[0]	RW	Reserved	-

37.5.1.2.4 STATUS

- Base Address: 0xC021_0000
- Address = Base Address + 0x0010, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Authen_Ack	[7]	RW	When hdcp is authenticated, it occurs. This bit keeps the authentication signal constantly. It's not cleared at all. It's just one delayed signal of authen_ack signal from hdcp block. This bit is not an interrupt source. Read Only bit 0 = Not authenticated 1 = Authenticated	1'b0
Aud_Fifo_Ovf	[6]	RW	When audio FIFO is overflowed, this bit will be set. Once it is set, it should be cleared by host. 0 = Not full 1 = Full	1'b0
RSVD	[5]	RW	Reserved	-
Update_Ri_Int	[4]	RW	Ri Interrupt status bit If it is written by 1, it is cleared. 0 = Not occurred 1 = Interrupt occurred	1'b0
RSVD	[3]	RW	Reserved	-
An_Write_Int	[2]	RW	Indicates that A randomness value is available, it occurs. When it occurs, users can get A values by reading HDCP_An_x registers. 0 = An value is not available 1 = An value is available. Users can read An values	1'b0
Watchdog_Int	[1]	RW	Indicates that 2nd part of HDCP authentication protocol is initiated and CPU should set a watchdog timer to check 5 sec interval. If it is written by 1, it is cleared. 0 = Not occurred 1 = Interrupt occurred	1'b0
I2C_Init_Int	[0]	RW	Indicates that 1st part of HDCP authentication protocol can start. If it is written by 1, it is cleared. 0 = Not occurred 1 = Interrupt occurred	1'b0

37.5.1.2.5 STATUS_EN

- Base Address: 0xC021_0000
- Address = Base Address + 0x0020, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
Aud_Fido_Ovf_Ee	[6]	RW	Audio buffer overflow interrupt enable When it is set to 1, interrupt assertion is written on the STATUS registers. 0 = Disable 1 = Enable	1'b0
RSVD	[5]	RW	Reserved	-
Update_Ri_Int_En	[4]	RW	UPDATE_RI_INT interrupt enable. 0 = Disable 1 = Enable	1'b0
RSVD	[3]	RW	Reserved	-
An_Write_Int_En	[2]	RW	AN_WRITE_INT interrupt enable. 0 = Disable 1 = Enable	1'b0
Watchdog_Int_En	[1]	RW	WATCHDOG_INT interrupt enable. 0 = Disable 1 = Enable	1'b0
I2C_Int_En	[0]	RW	I2C_INT interrupt enable. 0 = Disable 1 = Enable	1'b0

37.5.1.2.6 MODE_SEL

- Base Address: 0xC021_0000
- Address = Base Address + 0x0040, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
Hdmi_Mode	[1]	RW	Select a mode. 0 = Disable 1 = Enable	1'b0
Dvi_Mode	[0]	RW	Select a mode. 0 = Disable 1 = Enable	1'b0

37.5.1.2.7 ENC_EN

- Base Address: 0xC021_0000
- Address = Base Address + 0x0044, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	
Hdcp_Enc_En	[0]	RW	When set, HDCP encryption is applied. Before setting this bit, the HDCP authentication process has to be accomplished. 0 = Encryption disable 1 = Enable	0x00

37.5.1.2.8 HDMI_YMAX

- Base Address: 0xC021_0000
- Address = Base Address + 0x0060, Reset Value = 0xEB

Name	Bit	Type	Description	Reset Value

HDMI_YMAX	[7:0]	RW	Maximum value of Y (or G for RGB format) value after pixel limit control.
			These registers are used according to Pxl_Lmt_Ctrl bits in HDMI_CON_1 register.
			When Pxl_Lmt_Ctrl bits is 0x1, R and B for RGB format is also limited by the value of this register.
			For RGB mode
			if (i_video_x HDMI_YMAX × 16)
			output = HDMI_YMAX × 16
			else if (i_video_x < HDMI_YMIN × 16)
			output = HDMI_YMIN x 16 else output = i_video_x
			For YCbCr mode, the Y input is dealt with the same as above.
			For Cb and Cr values,
			if (i_video_x HDMI_CMAX × 16)
			output = HDMI_CMAX × 16
			else if (i_video_x < HDMI_CMIN × 16)
			output = HDMI_CMIN × 16 else output = i_video_x
			NOTE: Value 16 in each line compensates the difference of bit width between the input pixel and register value.
				0xEB

37.5.1.2.9 HDMI_YMIN

- Base Address: 0xC021_0000
- Address = Base Address + 0x0064, Reset Value = 0x10

Name	Bit	Type	Description	Reset Value

HDMI_YMIN	[7:0]	RW	Minimum value of Y (or G for RGB format) value after pixel limit control.
			These registers are used according to Pxl_Lmt_Ctrl bits in HDMI_CON_1 register.
			When Pxl_Lmt_Ctrl bits is 0x1, R and B for RGB format is also limited by the value of this register.
			For RGB mode
			if (i_video_x HDMI_YMAX × 16)
			output = HDMI_YMAX × 16
			else if (i_video_x < HDMI_YMIN × 16)
			output = HDMI_YMIN × 16 else output = i_video_x
			For YCbCr mode, the Y input is dealt with the same as above. For Cb and Cr values,
			if (i_video_x HDMI_CMAX × 16)
			output = HDMI_CMAX × 16
			else if (i_video_x < HDMI_CMIN × 16)
			output = HDMI_CMIN × 16 else output = i_video_x
			NOTE: Value 16 in each line compensates the difference of bit width between the input pixel and register value.
				0x10

37.5.1.2.10 HDMI_CMAX

- Base Address: 0xC021_0000
- Address = Base Address + 0x0068, Reset Value = 0xF0

Name	Bit	Type	Description	Reset Value

HDMI_CMAX	[7:0]	RW	Maximum value of Cb and Cr (or R and B for RGB format) value after pixel limit control.
			These registers are used according to Pxl_Lmt_Ctrl bits in HDMI_CON_1 register.
			When Pxl_Lmt_Ctrl bits is 0x2, R and B for RGB format is also limited by the value of this register.
			If Pxl_Lmt_Ctrl bits is 0x1, R and B for RGB format is also limited by
			HDMI_YMAX register. For RGB mode
			if (i_video_x HDMI_YMAX × 16)
			output = HDMI_YMAX × 16
			else if (i_video_x < HDMI_YMIN × 16)
			output = HDMI_YMIN x 16 else output = i_video_x
			For YCbCr mode, the Y input is dealt with the same as above. For Cb and Cr values,
			if (i_video_x HDMI_CMAX × 16)
			output = HDMI_CMAX × 16
			else if (i_video_x < HDMI_CMIN × 16)
			output = HDMI_CMIN × 16 else output = i_video_x
			NOTE: Value 16 in each line compensates the difference of bit width between the input pixel and register value.
				0xF0

37.5.1.2.11 HDMI_CMIN

- Base Address: 0xC021_0000
- Address = Base Address + 0x006C, Reset Value = 0x10

Name	Bit	Type	Description	Reset Value

HDMI_CMIN	[7:0]	RW	Minimum value of Cb and Cr (or R and B for RGB format) value after pixel limit control.
			These registers are used according to Pxl_Lmt_Ctrl bits in HDMI_CON_1 register.
			When Pxl_Lmt_Ctrl bits is 0x2, R and B for RGB format is also limited by the value of this register.
			If Pxl_Lmt_Ctrl bits is 0x1, R and B for RGB format is also limited by
			HDMI_YMIN register. For RGB mode
			if (i_video_x HDMI_YMAX × 16)
			output = HDMI_YMAX × 16
			else if (i_video_x < HDMI_YMIN × 16)
			output = HDMI_YMIN × 16 else output = i_video_x
			For YCbCr mode, the Y input is dealt with the same as above. For Cb and Cr values,
			if (i_video_x HDMI_CMAX × 16)
			output = HDMI_CMAX × 16
			else if (i_video_x < HDMI_CMIN × 16)
			output = HDMI_CMIN × 16 else output = i_video_x
			NOTE: Value 16 in each line compensates the difference of bit width between the input pixel and register value.
				0x10

37.5.1.2.12 H_BLANK_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x00A0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
H_BLANK	[7:0]	RW	H_BLANK [7:0] of 13 bits. Clock Cycles of horizontal Blanking Size. Refer to the Reference CEA-861D	0x00

37.5.1.2.13 H_BLANK_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x00A4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
H_BLANK	[4:0]	RW	H_BLANK [12:8] of 13 bits. Clock Cycles of horizontal Blanking Size. Refer to the Reference CEA-861D	0x00

37.5.1.2.14 V2_BLANK_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x00B0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
V2_BLANK	[7:0]	RW	V2_BLANK [7:0] of 13 bits. V1_BLANK+Active Lines. End Part. This value is the same as V_LINE value for progressive mode. For interlace mode, use the reference value in the table. Refer to the Reference CEA-861D	0x00

37.5.1.2.15 V2_BLANK_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x00B4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
V2_BLANK	[4:0]	RW	V2_BLANK [12:8] of 13 bits. V1_BLANK+Active Lines. End Part. This value is the same as V_LINE value for progressive mode. For interlace mode, use the reference value in the table. Refer to the Reference CEA-861D	0x00

37.5.1.2.16 V1_BLANK_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x00B8, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
V1_BLANK	[7:0]	RW	V1_BLANK [7:0] of 13 bits. Vertical Blanking Line Size. Front Part. Refer to the Reference CEA-861D	0x00

37.5.1.2.17 V1_BLANK_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x00BC, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
V1_BLANK	[4:0]	RW	V1_BLANK [12:8] of 13 bits. Vertical Blanking Line Size. Front Part. Refer to the Reference CEA-861D	0x00

37.5.1.2.18 V_LINE_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x00C0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
V_LINE	[7:0]	RW	V_LINE [7:0] of 13 bits. Vertical Line Length. Refer to the Reference CEA-861D	0x00

37.5.1.2.19 V_LINE_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x00C4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
V_LINE	[4:0]	RW	V_LINE [12:8] of 13 bits. Vertical Line Length. Refer to the Reference CEA-861D	0x00

37.5.1.2.20 H_LINE_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x00C8, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
H_LINE	[7:0]	RW	H_LINE [7:0] of 13 bits. Horizontal Line Length. Refer to the Reference CEA-861D	0x00

37.5.1.2.21 H_LINE_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x00CC, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	R	Reserved	-
H_LINE	[4:0]	RW	H_LINE [12:8] of 13 bits. Horizontal Line Length. Refer to the Reference CEA-861D	0x00

37.5.1.2.22 HSYNC_POL

- Base Address: 0xC021_0000
- Address = Base Address + 0x00E0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
Hsync_Pol	[0]	RW	Set this bit for inverting the generated signal to meet the modes. In 720p mode doesn't need to invert the signal. Others need to be inverted. Refer to the Reference CEA-861D 0 = Active high 1 = Active low	0x00

37.5.1.2.23 VSYNC_POL

- Base Address: 0xC021_0000
- Address = Base Address + 0x00E4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
V_Sync_Pol_Sel	[0]	RW	Start point detection polarity selection bit. 720p's sync shapes are different from 480p, 480i, and 576p's. They are inverted shapes. 0 = Active high 1 = Active low	0x00

37.5.1.2.24 INT_PRO_MODE

- Base Address: 0xC021_0000
- Address = Base Address + 0x00E8, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
INT_PRO_MODE	[0]	RW	Interlaced or Progressive Mode Selection. Refer to the Reference CEA-861D 0 = Progressive 1 = Interlaced.	0x00

37.5.1.2.25 V_BLANK_F0_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0110, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_blank_f0	[7:0]	RW	v_blank_f0 [7:0] of 13 bits. The start position of bottom field's active region. This value is the same as V_LINE value for Interlace mode. For progressive mode, This value is not used. Refer to the Reference CEA-861D	0xFF

37.5.1.2.26 V_BLANK_F0_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0114, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_blank_f0	[4:0]	RW	v_blank_f0 [12:8] of 13 bits. The start position of bottom field's active region. This value is the same as V_LINE value for Interlace mode. For progressive mode, This value is not used. Refer to the Reference CEA-861D	0x1F

37.5.1.2.27 V_BLANK_F1_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0118, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_blank_f1	[7:0]	RW	v_blank_f1 [7:0] of 13 bits. In the interlace mode, v_blank length of even field and odd field is different. This register specifies the end position of bottom field's active region. Refer to the Reference CEA-861D	0xFF

37.5.1.2.28 V_BLANK_F1_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x011C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_blank_f1	[4:0]	RW	v_blank_f1 [12:8] of 13 bits. In the interlace mode, v_blank length of even field and odd field is different. This register specifies the end position of bottom field's active region. Refer to the Reference CEA-861D	0x1F

37.5.1.2.29 H_SYNC_START_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0120, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Hsync_Start	[7:0]	RW	Hsync_Start [7:0] of 11 bits. Set the start point of H sync. Refer to the Reference CEA-861D	0x00

37.5.1.2.30 H_SYNC_START_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0124, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
Hsync_Start	[4:0]	RW	Hsync_Start [12:8] of 11 bits. Set the start point of H sync. Refer to the Reference CEA-861D	0x00

37.5.1.2.31 H_SYNC_END_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0128, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Hsync_End	[7:0]	RW	Hsync_End [7:0] of 11 bits. Set the end point of H sync. Refer to the Reference CEA-861D	0x00

37.5.1.2.32 H_SYNC_END_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x012C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
Hsync_End	[4:0]	RW	Hsync_End [12:8] of 11 bits. Set the end point of H sync. Refer to the Reference CEA-861D	0x00

37.5.1.2.33 V_SYNC_LINE_BEF_2_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0130, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_bef_2	[7:0]	RW	v_sync_line_bef_2 [7:0] of 13 bits. Top field (or frame) V sync end line number. Refer to the Reference CEA-861D	0xFF

37.5.1.2.34 V_SYNC_LINE_BEF_2_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0134, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_bef_2	[4:0]	RW	v_sync_line_bef_2 [12:8] of 13 bits. Top field (or frame) V sync end line number. Refer to the Reference CEA-861D	0x1F

37.5.1.2.35 V_SYNC_LINE_BEF_1_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0138, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_bef_1	[7:0]	RW	Top field (or frame) V sync starts line number. Refer to the Reference CEA-861D	0xFF

37.5.1.2.36 V_SYNC_LINE_BEF_1_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x013C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_bef_1	[4:0]	RW	v_sync_line_bef_1 [12:8] of 13 bits. Top field (or frame) V sync starts line number. Refer to the Reference CEA-861D	0x1F

37.5.1.2.37 V_SYNC_LINE_AFT_2_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0140, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_2	[7:0]	RW	v_sync_line_aft_2 [7:0] of 13 bits. Bottom field V sync end line number. Refer to the Reference CEA-861D	0xFF

37.5.1.2.38 V_SYNC_LINE_AFT_2_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0144, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_2	[4:0]	RW	v_sync_line_aft_2 [12:8] of 13 bits. Bottom field V sync end line number. Refer to the Reference CEA-861D	0x1F

37.5.1.2.39 V_SYNC_LINE_AFT_1_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0148, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_1	[7:0]	RW	v_sync_line_aft_1 [7:0] of 13 bits. Bottom field V sync start line number. Refer to the Reference CEA-861D	0xFF

37.5.1.2.40 V_SYNC_LINE_AFT_1_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x014C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_1	[4:0]	RW	v_sync_line_aft_1 [12:8] of 13 bits. Bottom field V sync start line number. Refer to the Reference CEA-861D	0x1F

37.5.1.2.41 V_SYNC_LINE_AFT_PXL_2_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0150, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_pxl_2	[7:0]	RW	v_sync_line_aft_pxl_2 [7:0] of 13 bits. Bottom field V sync end transition point. Refer to the Reference CEA-861D	0xFF

37.5.1.2.42 V_SYNC_LINE_AFT_PXL_2_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0154, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_pxl_2	[4:0]	RW	v_sync_line_aft_pxl_2 [12:8] of 13 bits. Bottom field V sync end transition point. Refer to the Reference CEA-861D	0x1F

37.5.1.2.43 V_SYNC_LINE_AFT_PXL_1_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0158, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_pxl_1	[7:0]	RW	v_sync_line_aft_pxl_1 [7:0] of 13 bits. Bottom field V sync start transition point. Refer to the Reference CEA-861D	0xFF

37.5.1.2.44 V_SYNC_LINE_AFT_PXL_1_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x015C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_pxl_1	[4:0]	RW	v_sync_line_aft_pxl_1 [12:8] of 13 bits. Bottom field V sync start transition point. Refer to the Reference CEA-861D	0x1F

37.5.1.2.45 V_BLANK_F2_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0160, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_blank_f2	[7:0]	RW	v_blank_f2 [7:0] of 13 bits. The start position of third field's active region. For 2D mode, This value is not used.	0xFF

37.5.1.2.46 V_BLANK_F2_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0164, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_blank_f2	[4:0]	RW	v_blank_f2 [12:8] of 13 bits. The start position of third field's active region. For 2D mode, This value is not used.	0x1F

37.5.1.2.47 V_BLANK_F3_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0168, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_blank_f3	[7:0]	RW	v_blank_f3 [7:0] of 13 bits. The end position of third field's active region. For 2D mode, This value is not used.	0xFF

37.5.1.2.48 V_BLANK_F3_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x016C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_blank_f3	[4:0]	RW	v_blank_f3 [12:8] of 13 bits. The end position of third field's active region. For 2D mode, This value is not used.	0x1F

37.5.1.2.49 V_BLANK_F4_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0170, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_blank_f4	[7:0]	RW	v_blank_f4 [7:0] of 13 bits. The start position of fourth field's active region. For 2D mode, This value is not used	0xFF

37.5.1.2.50 V_BLANK_F4_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0174, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_blank_f4	[4:0]	RW	v_blank_f4 [12:8] of 13 bits. The start position of fourth field's active region. For 2D mode, This value is not used.	0x1F

37.5.1.2.51 V_BLANK_F5_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0178, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_blank_f5	[7:0]	RW	v_blank_f5 [7:0] of 13 bits. The end position of fourth field's active region. For 2D mode, This value is not used.	0xFF

37.5.1.2.52 V_BLANK_F5_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x017C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_blank_f5	[4:0]	RW	v_blank_f5 [12:8] of 13 bits. The end position of fourth field's active region. For 2D mode, This value is not used.	0x1F

37.5.1.2.53 V_SYNC_LINE_AFT_3_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0180, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_3	[7:0]	RW	v_sync_line_aft_3 [7:0] of 13 bits. Third field V sync starts line number.	0xFF

37.5.1.2.54 V_SYNC_LINE_AFT_3_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0184, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_3	[4:0]	RW	v_sync_line_aft_3 [12:8] of 13 bits. Third field V sync starts line number.	0x1F

37.5.1.2.55 V_SYNC_LINE_AFT_4_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0188, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_4	[7:0]	RW	v_sync_line_aft_4 [7:0] of 13 bits. Third field V sync end line number.	0xFF

37.5.1.2.56 V_SYNC_LINE_AFT_4_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x018C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_4	[4:0]	RW	v_sync_line_aft_4 [12:8] of 13 bits. Third field V sync end line number.	0x1F

37.5.1.2.57 V_SYNC_LINE_AFT_5_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0190, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_5	[7:0]	RW	v_sync_line_aft_5 [7:0] of 13 bits. Fourth field V sync starts line number.	0xFF

37.5.1.2.58 V_SYNC_LINE_AFT_5_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0194, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_5	[4:0]	RW	v_sync_line_aft_5 [12:8] of 13 bits. Fourth field V sync starts line number.	0x1F

37.5.1.2.59 V_SYNC_LINE_AFT_6_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0198, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_6	[7:0]	RW	v_sync_line_aft_6 [7:0] of 13 bits. Fourth field V sync end line number.	0xFF

37.5.1.2.60 V_SYNC_LINE_AFT_6_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x019C, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_6	[4:0]	RW	v_sync_line_aft_6 [12:8] of 13 bits. Fourth field V sync end line number.	0x1F

37.5.1.2.61 V_SYNC_LINE_AFT_PXL_3_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01A0, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_pxl_3	[7:0]	RW	v_sync_line_aft_pxl_3 [7:0] of 13 bits. Third field V sync start transition point.	0xFF

37.5.1.2.62 V_SYNC_LINE_AFT_PXL_3_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01A4, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_pxl_3	[4:0]	RW	v_sync_line_aft_pxl_3 [12:8] of 13 bits. Third field V sync start transition point.	0x1F

37.5.1.2.63 V_SYNC_LINE_AFT_PXL_4_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01A8, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_pxl_4	[7:0]	RW	v_sync_line_aft_pxl_4 [7:0] of 13 bits. Third field V sync end transition point.	0xFF

37.5.1.2.64 V_SYNC_LINE_AFT_PXL_4_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01AC, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_pxl_4	[4:0]	RW	v_sync_line_aft_pxl_4 [12:8] of 13 bits. Third field V sync end transition point.	0x1F

37.5.1.2.65 V_SYNC_LINE_AFT_PXL_5_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01B0, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_pxl_5	[7:0]	RW	v_sync_line_aft_pxl_5 [7:0] of 13 bits. Fourth field V sync start transition point.	0xFF

37.5.1.2.66 V_SYNC_LINE_AFT_PXL_5_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01B4, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_pxl_5	[4:0]	RW	v_sync_line_aft_pxl_5 [12:8] of 13 bits. Fourth field V sync start transition point.	0x1F

37.5.1.2.67 V_SYNC_LINE_AFT_PXL_6_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01B8, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
v_sync_line_aft_pxl_6	[7:0]	RW	v_sync_line_aft_pxl_6 [7:0] of 13 bits. Fourth field V sync end transition point.	0xFF

37.5.1.2.68 V_SYNC_LINE_AFT_PXL_6_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01BC, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
v_sync_line_aft_pxl_6	[4:0]	RW	v_sync_line_aft_pxl_6 [12:8] of 13 bits. Fourth field V sync end transition point.	0x1F

37.5.1.2.69 VACT_SPACE1_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01C0, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
vact_space1	[7:0]	RW	vact_space1 [7:0] of 13 bits. first active space start line number	0xFF

37.5.1.2.70 VACT_SPACE1_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01C4, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
vact_space1	[4:0]	RW	vact_space1 [12:8] of 13 bits. first active space start line number	0x1F

37.5.1.2.71 VACT_SPACE2_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01C8, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
vact_space2	[7:0]	RW	vact_space2 [7:0] of 13 bits. first active space end line number	0xFF

37.5.1.2.72 VACT_SPACE2_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01CC, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
vact_space2	[4:0]	RW	vact_space2 [12:8] of 13 bits. first active space end line number	0x1F

37.5.1.2.73 VACT_SPACE3_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01D0, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
vact_space3	[7:0]	RW	vact_space3 [7:0] of 13 bits. second active space start line number	0xFF

37.5.1.2.74 VACT_SPACE3_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01D4, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
vact_space3	[4:0]	RW	vact_space3 [12:8] of 13 bits. second active space start line number	0x1F

37.5.1.2.75 VACT_SPACE4_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01D8, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
vact_space4	[7:0]	RW	vact_space4 [7:0] of 13 bits. second active space end line number	0xFF

37.5.1.2.76 VACT_SPACE4_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01DC, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
vact_space4	[4:0]	RW	vact_space4 [12:8] of 13 bits. Third active space end line number	0x1F

37.5.1.2.77 VACT_SPACE5_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01E0, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
vact_space5	[7:0]	RW	vact_space5 [7:0] of 13 bits. Third active space start line number	0xFF

37.5.1.2.78 VACT_SPACE5_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01E4, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
vact_space5	[4:0]	RW	vact_space5 [12:8] of 13 bits. Third active space start line number	0x1F

37.5.1.2.79 VACT_SPACE6_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x01E8, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
vact_space6	[7:0]	RW	vact_space6 [7:0] of 13 bits. Third active space end line number	0xFF

37.5.1.2.80 VACT_SPACE6_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x01EC, Reset Value = 0x1F

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
vact_space6	[4:0]	RW	vact_space6 [12:8] of 13 bits. Third active space end line number	0x1F

37.5.1.2.81 GCP_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0200, Reset Value = 0x04

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
ENABLE_1st_VSYNC	[3]	RW	Enable this bit to transfer the GCP packet on the 1st VSYNC in a frame 0 = Do not transfer GCP packet 1 = Transfer GCP packet	1'b0
ENABLE_2nd_VSYNC	[2]	RW	For Interlace mode, Enable this bit to transfer the GCP packet on the 2nd VSYNC in a frame 0 = Do not transfer GCP packet 1 = Transfer GCP packet	1'b1
GCP_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x =Transmit every vsync. GCP packet will be transmitted within 384 cycles after active vsync. After transferring first GCP packet, GCP_CON[0] is changed to 0.	2'b0

37.5.1.2.82 GCP_BYTE1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0210, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
GCP_BYTE1	[7:0]	RW	GCP packet's first data byte. It shall be either 0x10 (Clear AVMUTE) or 0x01 (Set AVMUTE). Refer to Table 5-17 of HDMI v1.3 specification	0x00

37.5.1.2.83 GCP_BYTE2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0214, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
PP	[7:4]	RW	PP (Packing Phase), Read Only	4'b0
CD	[3:0]	RW	CD (Color Depth)	4'b0

37.5.1.2.84 GCP_BYTE3

- Base Address: 0xC021_0000
- Address = Base Address + 0x0218, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
GCP_BYTE3	[0]	RW	Default State	1'b0

37.5.1.2.85 ASP_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0300, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
DST_Double	[7]	RW	DST double	1'b0
Aud_Type	[6:5]	RW	Packet type instead of audio type 00 = Audio Sample Packet 01 = One-bit audio packet 10 = HBR packet 11 = DST packet	2'b0
Aud_Mode	[4]	RW	Two channel or multi-channel mode selection This bit will be also used for layout bit in ASP header. 0 = 2 channel mode 1 = Multi-channel mode. Set this bit to transmit HBR packets.	1'b0
SP_Pre	[3:0]	RW	Control sub-packet usage for multi-channel mode only. When two-channel mode, this register value is not used.	4'b0

37.5.1.2.86 ASP_SP_FLAT

- Base Address: 0xC021_0000
- Address = Base Address + 0x0304, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
SP_Flat	[3:0]	RW	The sp_flat/sample_invalid value in the ASP header. Refer to the HDMI specification v1.3 (5.3.4 and 5.3.9)	4'b0

37.5.1.2.87 ASP_CHCFG0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0310, Reset Value = 0x08

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	-
Spk0R_Sel	[5:3]	RW	Audio channel Selection for sub packet 0 right channel data in multi-channel mode. The meaning is the same as SPK3R_SEL	3'b1
Spk0L_Sel	[2:0]	RW	Audio channel Selection for sub packet 0 right channel data in multi-channel mode. The meaning is the same as SPK3R_SEL	3'b0

37.5.1.2.88 ASP_CHCFG1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0314, Reset Value = 0x1A

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	-
SPK1R_SEL	[5:3]	RW	Audio channel Selection for sub packet 1 right channel data in multi-channel mode. The meaning is the same as SPK3R_SEL	3'b3
Spk1L_Sel	[2:0]	RW	Audio channel Selection for sub packet 1 left channel data in multi-channel mode. The meaning is the same as SPK3R_SEL	3'b2

37.5.1.2.89 ASP_CHCFG2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0318, Reset Value = 0x2C

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	-
Spk2R_Sel	[5:3]	RW	Audio channel Selection for sub packet 2 right channel data in multi-channel mode. The meaning is the same as SPK3R_SEL	3'b5
Spk2L_Sel	[2:0]	RW	Audio channel Selection for sub packet 2 left channel data in multi-channel mode. The meaning is the same as SPK3R_SEL	3'b4

37.5.1.2.90 ASP_CHCFG3

- Base Address: 0xC021_0000
- Address = Base Address + 0x031C, Reset Value = 0x3E

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	-
Spk3R_Sel	[5:3]	RW	Audio channel Selection for sub packet 3 right channel data in multi-channel mode. 000 = i_pcm0L is used for sub packet 0 Left channel 001 = i_pcm0R is used for sub packet 0 Left channel 010 = i_pcm1L is used for sub packet 0 Left channel 011 = i_pcm1R is used for sub packet 0 Left channel 100 = i_pcm2L is used for sub packet 0 Left channel 101 = i_pcm2R is used for sub packet 0 Left channel 110 = i_pcm3L is used for sub packet 0 Left channel 111 = i_pcm3R is used for sub packet 0 Left channel	3'b7
Spk3L_Sel	[2:0]	RW	Audio channel Selection for sub packet 3 left channel data in multi-channel mode. The meaning is the same as SPK3R_SEL	3'b6

37.5.1.2.91 ACR_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0400, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	-
RSVD	[4:3]	R	Reserved	-
ACR_Tx_Mode	[2:0]	RW	000 = Do not Tx (Transfer) the ACR packet. 100 = Measured CTS mode. Make ACR packet with CTS value by counting TMDS clock for Fs × 128/N duration. In this case, the 7 LSBs of N value (ACR_N register) should be all zero.	3'b0

37.5.1.2.92 ACR_MCTS0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0410, Reset Value = 0x01

Name	Bit	Type	Description	Reset Value
ACR_MCTS	[7:0]	R	ACR_MCTS[7:0] of 20 bits. This value is the TMDS clock cycles for N[19:7] number of audio sample inputs. It is only valid when measured CTS mode is set on ACR_CON register	0x01

37.5.1.2.93 ACR_MCTS1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0414, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ACR_MCTS	[7:0]	R	ACR_MCTS[15:8] of 20 bits. This value is the TMDS clock cycles for N[19:7] number of audio sample inputs. It is only valid when measured CTS mode is set on ACR_CON register	0x00

37.5.1.2.94 ACR_MCTS2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0418, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
ACR_MCTS	[3:0]	R	ACR_MCTS [19:16] of 20 bits. This value is the TMDS clock cycles for N[19:7] number of audio sample inputs. It is only valid when measured CTS mode is set on ACR_CON register	4'b0

37.5.1.2.95 ACR_N0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0430, Reset Value = 0xE8

Name	Bit	Type	Description	Reset Value
ACR_N	[7:0]	RW	ACR_N [7:0] of 20 bits. The N value in ACR packet	0xE8

37.5.1.2.96 ACR_N1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0434, Reset Value = 0x03

Name	Bit	Type	Description	Reset Value
ACR_N	[7:0]	RW	ACR_N [15:8] of 20 bits. The N value in ACR packet	0x03

37.5.1.2.97 ACR_N2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0438, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
ACR_N	[3:0]	RW	ACR_N [19:16] of 20 bits. The N value in ACR packet	4'b0

37.5.1.2.98 ACP_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0500, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ACP_FR_RATE	[7:3]	RW	Transmit ACP packet once per every ACP_FR_RATE+1 frames (or fields).	5'b0
RSVD	[2]	RW	Reserved	1'b0
ACP_TX_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync with ACP_FR_RATE	2'b0

37.5.1.2.99 ACP_TYPE

- Base Address: 0xC021_0000
- Address = Base Address + 0x0514, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ACP_TYPE	[7:0]	RW	ACP packet header. (HB1 of ACP packet header) See Table 5-18 in HDMI v1.3 specification	0x00

37.5.1.2.100 ACP_DATAx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0520, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ACP_DATAx	[7:0]	RW	ACP packet body data. (PB0 to PB16 of ACP packet body) See 9.3 in HDMI v1.3 specification	0x00

37.5.1.2.101 ISRC_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0600, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ISRC_FR_RATE	[7:3]	RW	Transmit ISRC1 (with ISRC2 or not) packet once per every ISRC_FR_RATE+1 frames (or fields).	5'b0
ISRC2_EN	[2]	RW	Transmit ISRC2 packet with ISRC1 packet	1'b0
ISRC_TX_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync with ISRC_FR_RATE	2'b0

37.5.1.2.102 ISRC1_HEADER1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0614, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ISRC_Cont	[7]	RW	See table 5-20 in HDMI v1.3specification	1'b0
ISRC_Valid	[6]	RW	See table 5-20 in HDMI v1.3 specification	1'b0
RSVD	[5:3]	RW	Reserved	-
ISRC_status	[2:0]	RW	See table 5-20 in HDMI v1.3 specification	3'b0

37.5.1.2.103 ISRC1_DATAx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0620, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ISRC1_DATAx	[7:0]	RW	ISRC1 packet body data. (PB0 to 15 of ISRC1 packet body). See Table 5-21 in HDMI v1.3 specification.	0x00

37.5.1.2.104 ISRC2_DATAx

- Base Address: 0xC021_0000
- Address = Base Address + 0x06A0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
ISRC2_DATAx	[7:0]	RW	ISRC2 packet body data. (PB0 to 15 of ISRC2 packet body). See Table 5-23 in HDMI v1.3 specification.	0x00

37.5.1.2.105 AVI_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0700, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
AVI_TX_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync	2'b0

37.5.1.2.106 AVI_HEADER0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0710, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AVI_HEADER0	[7:0]	RW	HB0 byte of AVI packet header	0x00

37.5.1.2.107 AVI_HEADER1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0714, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AVI_HEADER1	[7:0]	RW	HB1 byte of AVI packet header	0x00

37.5.1.2.108 AVI_HEADER2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0718, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AVI_HEADER2	[7:0]	RW	HB2 byte of AVI packet header	0x00

37.5.1.2.109 AVI_CHECK_SUM

- Base Address: 0xC021_0000
- Address = Base Address + 0x071C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AVI_CHECK_SUM	[7:0]	RW	AVI Info Frame checksum byte. (PB0 byte of AVI packet body)	0x00

37.5.1.2.110 AVI_BYTEx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0720, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AVI_BYTEx	[7:0]	RW	AVI Info frame packet data registers. (PB1 to PB13 bytes of AVI packet body)	0x00

37.5.1.2.111 AUI_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0800, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
AUI_TX_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync	2'b0

37.5.1.2.112 AUI_HEADER0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0810, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AUI_HEADER0	[7:0]	RW	HB0 byte of AUI packet header	0x00

37.5.1.2.113 AUI_HEADER1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0814, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AUI_HEADER1	[7:0]	RW	HB1 byte of AUI packet header	0x00

37.5.1.2.114 AUI_HEADER2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0818, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AUI_HEADER2	[7:0]	RW	HB2 byte of AUI packet header	0x000x00

37.5.1.2.115 AUI_CHECK_SUM

- Base Address: 0xC021_0000
- Address = Base Address + 0x081C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AUI_CHECK_SUM	[7:0]	RW	AUI Info-frame checksum data. (PB0 byte of AUI packet body)	

37.5.1.2.116 AUI_BYTEx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0820, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AUI_BYTEx	[7:0]	RW	AUI Info-frame packet body. (PB1 to PB12 bytes of AUI packet body)	0x00

37.5.1.2.117 MPG_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0900, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
MPG_TX_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync	2'b0

37.5.1.2.118 MPG_CHECK_SUM

- Base Address: 0xC021_0000
- Address = Base Address + 0x091C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
MPG_CHECK_SUM	[7:0]	RW	MPG info-frame checksum register (PB0 byte of MPG packet body)	0x00

37.5.1.2.119 MPG_DATAx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0920, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
MPG_DTATx	[7:0]	RW	MPG Info-frame packet data. (PB1 to PB5 bytes of MPG packet body)	0x00

37.5.1.2.120 SPD_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0A00, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
SPD_TX_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync	2'b0

37.5.1.2.121 SPD_HEADER0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0A10, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
SPD_HEADER0	[7:0]	RW	HB0 byte of SPD packet header	0x00

37.5.1.2.122 SPD_HEADER1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0A14, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
SPD_HEADER1	[7:0]	RW	HB1 byte of SPD packet header	0x00

37.5.1.2.123 SPD_HEADER2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0A18, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
SPD_HEADER2	[7:0]	RW	HB2 byte of SPD packet header	0x00

37.5.1.2.124 SPD_DATAx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0A20, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
SPD_DATAx	[7:0]	RW	SPD packet data registers. (PB0 to PB27 bytes)	0x00

37.5.1.2.125 GAMUT_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0B00, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
GAMUT_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync	2'b0

37.5.1.2.126 GAMUT_HEADER0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0B10, Reset Value =0x00

Name	Bit	Type	Description	Reset Value
HB0	[7:0]	RW	HB0 value in the table 5-30 in HDMI 1.3 specification	0x00

37.5.1.2.127 GAMUT_HEADER1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0B14, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Next_Field	[7]	RW	Set to indicate that the GBD carried in this packet will be effective on the next video field.	1'b0
GBD_profile	[6:4]	RW	Transmission profile number (We only support profile 0)	3'b0
Affected_Gamut_Seq_Num	[3:0]	RW	Indicates which video fields are relevant for this metadata	4'b0

37.5.1.2.128 GAMUT_HEADER2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0B18, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
No_Crnt_GBD	[7]	RW	Set to indicate that there is no gamut metadata available for the currently transmitted video	1'b0
RSVD	[6]	RW	Reserved	-
Packet_Seq	[5:4]	RW	Indicates whether this packet is the only, the first, an intermediate or the last packet in a Gamut metadata packet sequence	2'b0
Current_Gamut_Seq_Num	[3:0]	RW	Indicates the gamut number of the currently transmitted video stream	4'b0

37.5.1.2.129 GAMUT_METADATAx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0B20, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
GAMUT_METADATAx	[7:0]	RW	Gamut Metadata Packet body for P0 transmission profile	0x00

37.5.1.2.130 VSI_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x0C00, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
VSI_TX_CON	[1:0]	RW	00 = Do not transmit 01 = Transmit once 1x = Transmit every vsync	2'b0

37.5.1.2.131 VSI_HEADER0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0C10, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
VSI_HEADER0	[7:0]	RW	HB0 byte of VSI packet header	0x00

37.5.1.2.132 VSI_HEADER1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0C14, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
VSI_HEADER1	[7:0]	RW	HB1 byte of VSI packet header	0x00

37.5.1.2.133 VSI_HEADER2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0C18, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
VSI_HEADER2	[7:0]	RW	HB2 byte of VSI packet header	0x00

37.5.1.2.134 VSI_DATAx

- Base Address: 0xC021_0000
- Address = Base Address + 0x0C20, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
VSI_DATAx	[7:0]	RW	VSI packet data registers. (PB0 to PB27 bytes)	0x00

37.5.1.2.135 DC_CONTROL

- Base Address: 0xC021_0000
- Address = Base Address + 0x0D00, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
Deep_Color_Mode	[1:0]	RW	00 = 8 bits/pixel 01 = 10 bits/pixel 10 = 12 bits/pixel 11 = Not Used	2'b0

37.5.1.2.136 VIDEO_PATTERN_GEN

- Base Address: 0xC021_0000
- Address = Base Address + 0x0D04, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
Ext_Video_En	[1]	RW	0 = Ext Off 1 = Ext En	1'b0
Video_Pattern_Enable	[0]	RW	0 = Disable 1 = Use Internally generated video pattern	1'b0

37.5.1.2.137 An_Seed_Sel

- Base Address: 0xC021_0000
- Address = Base Address + 0x0E48, Reset Value = 0xFF

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
An_Seed_Sel	[0]	RW	0 = Use An_Seed_0 to 3 registers as a seed. 1 = Use input R/G/B as a seed.	0x1

37.5.1.2.138 An_Seed_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x0E58, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
An_Seed	[7:0]	RW	[23:16] of An seed value	0x00

37.5.1.2.139 An_Seed_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x0E5C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
An_Seed	[3:0]	RW	[15:12] of An seed value	4'b0

37.5.1.2.140 An_Seed_2

- Base Address: 0xC021_0000
- Address = Base Address + 0x0E60, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
An_Seed	[7:0]	RW	[11:4] of An seed value	0x00

37.5.1.2.141 An_Seed_3

- Base Address: 0xC021_0000
- Address = Base Address + 0x0E64, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
An_Seed	[3:0]	RW	[3:0] of An seed value	4'b0

37.5.1.2.142 HDCP_SHA1_x

- Base Address: 0xC021_0000
- Address = Base Address + 0x7000, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
HDCP_SHA1_x	[7:0]	RW	An 160-bit HDCP repeater's SHA-1 value. Least significant byte first. For example, • SHA-1 Value[7:0] <= HDCP_SHA1_00[7:0] • SHA-1 Value[159:152] <= HDCP_SHA1_19[7:0] These registers are readable but they are not modified by HDCP H/W. NOTE: Writing to HDCP_SHA1_00 to 19 register (any byte), regardless of the write value, triggers the SHA1 module to start the calculation. Do not write these register for RW testing. Write only when calculating SHA1 value.	0x00

37.5.1.2.143 HDCP_KSV_LIST_x

- Base Address: 0xC021_0000
- Address = Base Address + 0x7050, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
HDCP_KSV_LIST_x	[7:0]	RW	One 40-bit KSV value of the HDCP repeater's KSV list. These registers are readable. Least significant byte first. For example, • KSV value [7:0] <= HDCP_KSV_LIST_0[7:0] • KSV value [39:32] <= HDCP_KSV_LIST_4[7:0]	0x00

37.5.1.2.144 HDCP_KSV_LIST_CON

- Base Address: 0xC021_0000
- Address = Base Address + 0x7064, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
Hdcp_Ksv_Write_Done	[3]	RW	After writing KSV data into HDCP_KSV_LIST_X registers and then writing the value "1" to this register, HW processes the written KSV value and clears this bit to "0" 0 = Not yet written 1 = Written	1'b0
Hdcp_Ksv_List_Empty	[2]	RW	If the number of KSV list is zero, set this value to make SHA-1 module to start to calculate without KSV list. 0 = Not empty 1 = Empty	1'b0
Hdcp_Ksv_End	[1]	RW	It is used to indicate that current KSV value in HDCP_KSV_LIST_X registers is the last one. 0 = Not End 1 = End	1'b0
Hdcp_Ksv_Read	[0]	RW	After writing KSV data into HDCP_KSV_LIST_X registers HD- CP SHA-1 module keeps that KSV value into internal buffer and set this flag into "1" to notify that it has been read. After checking that it is set to "1", SW clears to "0" at the same time when writing the HDCP_KSV_WRITE_DONE bit for next KSV list value. 0 = Not Read 1 = Read	1'b0

37.5.1.2.145 HDCP_SHA_RESULT

- Base Address: 0xC021_0000
- Address = Base Address + 0x7070, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
Hdcp_Sha_Valid_Ready	[1]	RW	Indicates that the SHA comparison has been done by the HW. Must be cleared by SW by writing 0 0 = Not ready 1 = Ready	1'b0
Hdcp_Sha_Valid	[0]	RW	Indicates that the SHA-1 comparison succeeds. Must be cleared by SW by writing 0 0 = Not Valid 1 = Valid	1'b0

37.5.1.2.146 HDCP_CTRL1

- Base Address: 0xC021_0000
- Address = Base Address + 0x7080, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
RSVD	[3]	RW	Reserved	-
imeout	[2]	RW	Set when Rx is repeater and its KSV list is not ready until 5 sec waiting. 0 = Not timeout 1 = Timeout (KSV Ready bit in the HDCP_BCAPS register is not high until 5 sec) and restart the 1st authentication.	1'b0
CP_Desired	[1]	RW	HDCP enable 0 = Not Desired 1 = Desired	1'b0
RSVD	[0]	RW	Reserved	-

37.5.1.2.147 HDCP_CTRL2

- Base Address: 0xC021_0000
- Address = Base Address + 0x7084, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
Revocation_Set	[0]	RW	KSV list is on the revocation list & Fail the 2nd authentication. 0 = Revocation Not set 1 = Revocation Set	1'b0

37.5.1.2.148 HDCP_CHECK_RESULT

- Base Address: 0xC021_0000
- Address = Base Address + 0x7090, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
Ri_Match_Result	[1:0]	RW	Write the result of comparison between Ri of Rx and Tx as the following values. (Ri : Tx, Ri' : Rx) Must be cleared by SW after setting 10 or 11 before next Ri Interrupt oc- curs. 0x = don't care 10 = Ri ` Ri' 11 = Ri = Ri'	2'b0

37.5.1.2.149 HDCP_BKSV_x

- Base Address: 0xC021_0000
- Address = Base Address + 0x70A0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
HDCP_BKSV_x	[7:0]	RW	Key selection vector (KSV) value from receiver. HDCP_BKSV [7:0] <= HDCP_BKSV_0 [7:0] HDCP_BKSV [15:8] <= HDCP_BKSV_1 [7:0] HDCP_BKSV [23:16] <= HDCP_BKSV_2 [7:0] HDCP_BKSV [31:24] <= HDCP_BKSV_3 [7:0] HDCP_BKSV [39:32] <= HDCP_BKSV_4 [7:0]	0x00

37.5.1.2.150 HDCP_AKSV_x

- Base Address: 0xC021_0000
- Address = Base Address + 0x70C0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
HDCP_AKSV_x	[7:0]	RW	KSV value of transmitter HDCP_AKSV [7:0] <= HDCP_AKSV_0 [7:0] HDCP_AKSV [15:8] <= HDCP_AKSV_1 [7:0] HDCP_AKSV [23:16] <= HDCP_AKSV_2 [7:0] HDCP_AKSV [31:24] <= HDCP_AKSV_3 [7:0] HDCP_AKSV [39:32] <= HDCP_AKSV_4 [7:0]	0x00

37.5.1.2.151 HDCP_An_x

- Base Address: 0xC021_0000
- Address = Base Address + 0x70E0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
HDCP_An_x	[7:0]	RW	64-bit Random number generated by Tx (An) HDCP_An [7:0] <= HDCP_An_0_0 [7:0] HDCP_An [15:8] <= HDCP_An_1 [7:0] HDCP_An [23:16] <= HDCP_An_2 [7:0] HDCP_An [31:24] <= HDCP_An_3 [7:0] HDCP_An [39:32] <= HDCP_An_4 [7:0] HDCP_An [47:40] <= HDCP_An_5 [7:0] HDCP_An [55:48] <= HDCP_An_6 [7:0] HDCP_An [63:56] <= HDCP_An_7 [7:0]	0x00

37.5.1.2.152 HDCP_BCAPS

- Base Address: 0xC021_0000
- Address = Base Address + 0x7100, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
Repeater	[6]	RW	The receiver supports downstream connections 0 = Not Repeater 1 = Repeater	1'b0
Ready	[5]	RW	KSV FIFO, SHA-1 calculation ready 0 = Not Ready 1 = Ready	1'b0
Fast	[4]	RW	The receiver devices supports 400 kHz transfer 0 = Not Fast 1 = Fast	1'b0
RSVD	[3:2]	RW	Must be 0's	-
v1p1_Features	[1]	RW	Supports EESS, Advance cipher, Enhanced link verification 0 = Un-set 1 = Set	1'b0
Fast_Reauthentication	[0]	RW	ALL HDMI receiver should be capable of reauthentication 0 = Un-set 1 = Set	1'b0

37.5.1.2.153 HDCP_BSTATUS_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x7110, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Max_Devs_Exceeded	[7]	RW	Topology error indicator 0 = No Error 1 = Error	1'b0
Device_Count	[6:0]	RW	Total number of attached downstream devices	7'b0

37.5.1.2.154 HDCP_BSTATUS_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x7114, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	RW	Reserved	3'b0
Hdmi_Mode	[4]	RW	HDMI mode indication. If set, HDCP is in HDMI mode.	1'b0
Max_Cascade_Exceeded	[3]	RW	Topology error	1'b0
Depth	[2:0]	RW	Cascade depth	3'b0

37.5.1.2.155 HDCP_Ri_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x7140, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
HDCP_Ri	[7:0]	R	HDCP Ri value of the transmitter. HDCP_Ri [7:0] of 16 bits.	0x00

37.5.1.2.156 HDCP_Ri_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x7144, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
HDCP_Ri	[7:0]	R	HDCP Ri value of the transmitter. HDCP_Ri [15:8] of 16 bits.	0x00

37.5.1.2.157 HDCP_I2C_INT

- Base Address: 0xC021_0000
- Address = Base Address + 0x7180, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
HDCP_I2C_INT	[0]	RW	HDCP I2C Interrupt status. Active high. It indicates the start of I2C transaction when it is set. After active, it should be cleared by S/W by writing 0. 0 = Not Occurred 1 = Occurred	1'b0

37.5.1.2.158 HDCP_AN_INT

- Base Address: 0xC021_0000
- Address = Base Address + 0x7190, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
HDCP_AN_INT	[0]	RW	HDCP An Interrupt status. Active high. If An value is available, it is set. After active, it should be cleared by S/W by writing 0. 0 = Not Occurred 1 = Occurred	1'b0

37.5.1.2.159 HDCP_WATCGDOG_INT

- Base Address: 0xC021_0000
- Address = Base Address + 0x71A0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
HDCP_WATCHDOG_INT	[0]	RW	HDCP Watchdog Interrupt status. Active high. If Repeater bit value is set after 1st authentication success, it is set. After active, it should be cleared by S/W by writing 0. 0 = Not Occurred 1 = Occurred	1'b0

37.5.1.2.160 HDCP_Ri_INT

- Base Address: 0xC021_0000
- Address = Base Address + 0x71B0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
HDCP_Ri_INT	[0]	RW	If Ri value is updated internally (at every 128 video frames), it is set to high. After set, it should be cleared by S/W by writing 0. 0 = Not Occurred 1 = Occurred	1'b0

37.5.1.2.161 HDCP_Ri_Compare_0

- Base Address: 0xC021_0000
- Address = Base Address + 0x71D0, Reset Value = 0x80

Name	Bit	Type	Description	Reset Value
Enable	[7]	RW	Enable the interrupt for this frame number index	1'b1
Frame_Number_index	[6:0]	RW	When the Frame count reaches this "Frame number index", an Ri Link integrity check interrupt occurs	7'b0

37.5.1.2.162 HDCP_Ri_Compare_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x71D4, Reset Value = 0x7F

Name	Bit	Type	Description	Reset Value
Enable	[7]	RW	Enable the interrupt for this frame number index	1'b0
Frame_Number_index	[6:0]	RW	When the Frame count reaches this "Frame number index", an Ri Link integrity check interrupt occurs	7'b1111111

37.5.1.2.163 HDCP_Frame_Count

- Base Address: 0xC021_0000
- Address = Base Address + 0x71E0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7]	R	Reserved	-
Frame_Count	[6:0]	R	Current value of the frame count index in the hardware	7'b0

37.5.1.2.164 RGB_ROUND_EN

- Base Address: 0xC021_0000
- Address = Base Address + 0xD500, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	R	Reserved	-
rgb_round_en	[0]	RW	RGB Rounding enable	1'b0

37.5.1.2.165 VACT_SPACE_R_0

- Base Address: 0xC021_0000
- Address = Base Address + 0xD504, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
vact_space_r	[7:0]	RW	vact_space_r [7:0] of 12 bits. Constant pixel color in vact space.	0x00

37.5.1.2.166 VACT_SPACE_R_1

- Base Address: 0xC021_0000
- Address = Base Address + 0x D508, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
vact_space_r	[3:0]	RW	vact_space_r [11:8] of 12 bits. Constant pixel color in vact space.	4'b0

37.5.1.2.167 VACT_SPACE_G_0

- Base Address: 0xC021_0000
- Address = Base Address + 0xD50C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
vact_space_g	[7:0]	RW	vact_space_g [7:0] of 12 bits. Constant pixel color in vact space.	0x00

37.5.1.2.168 VACT_SPACE_G_1

- Base Address: 0xC021_0000
- Address = Base Address + 0xD510, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
vact_space_g	[3:0]	RW	vact_space_g [11:8] of 12 bits. Constant pixel color in vact space.	4'b0

37.5.1.2.169 VACT_SPACE_B_0

- Base Address: 0xC021_0000
- Address = Base Address + 0xD514, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
vact_space_b	[7:0]	RW	vact_space_b [7:0] of 12 bits. Constant pixel color in vact space.	0x00

37.5.1.2.170 VACT_SPACE_B_1

- Base Address: 0xC021_0000
- Address = Base Address + 0xD518, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
vact_space_b	[3:0]	RW	vact_space_b [11:8] of 12 bits. Constant pixel color in vact space.	4'b0

37.5.1.2.171 BLUE_SCREEN_R_0

- Base Address: 0xC021_0000
- Address = Base Address + 0xD520, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
blue_screen_r	[7:0]	RW	blue_screen_r [7:0] of 12 bits.	0x00

37.5.1.2.172 BLUE_SCREEN_R_1

- Base Address: 0xC021_0000
- Address = Base Address + 0xD524, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
blue_screen_r	[3:0]	RW	blue_screen_r [11:8] of 12 bits.	4'b0

37.5.1.2.173 BLUE_SCREEN_G_0

- Base Address: 0xC021_0000
- Address = Base Address + 0xD528, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
blue_screen_g	[7:0]	RW	blue_screen_g [7:0] of 12 bits.	0x00

37.5.1.2.174 BLUE_SCREEN_G_1

- Base Address: 0xC021_0000
- Address = Base Address + 0xD52C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
blue_screen_g	[3:0]	RW	blue_screen_g [11:8] of 12 bits.	4'b0

37.5.1.2.175 BLUE_SCREEN_B_0

- Base Address: 0xC021_0000
- Address = Base Address + 0xD530, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
blue_screen_b	[7:0]	RW	blue_screen_b [7:0] of 12 bits.	0x00

37.5.1.2.176 BLUE_SCREEN_B_1

- Base Address: 0xC021_0000
- Address = Base Address + 0xD534, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
blue_screen_b	[3:0]	RW	blue_screen_b [11:8] of 12 bits.	4'b0

37.5.1.3 AES Registers

37.5.1.3.1 AES_START

- Base Address: 0xC022_0000
- Address = Base Address + 0x0000, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
AES_Start	[0]	RW	AES Start signal If specified amount of data is decrypted and written in memory, then AES start signal goes to 0. 0 = AES does not decrypt data. (AES decryption completed) 1 = AES starts to decrypt data from memory.	1'b0

37.5.1.3.2 AES_DATA_SIZE_L

- Base Address: 0xC022_0000
- Address = Base Address + 0x0020, Reset Value = 0x20

Name	Bit	Type	Description	Reset Value
AES_Data_Size_L	[7:0]	RW	AES data size (in bytes) to decrypt If the data size is not the multiple of 128 bits, zeros should be padded 128 bits align Maximum number is 120h (internal memory size limits the maximum data size Default value: 288 bytes	0x20

37.5.1.3.3 AES_DATA_SIZE_H

- Base Address: 0xC022_0000
- Address = Base Address + 0x0024, Reset Value = 0x01

Name	Bit	Type	Description	Reset Value
AES_Data_Size_H	[7:0]	RW	AES data size (in bytes) to decrypt If the data size is not the multiple of 128 bits, zeros should be padded 128 bits align Maximum number is 120h (internal memory size limits the maximum data size Default value: 288 bytes	0x01

37.5.1.3.4 AES_DATA

- Base Address: 0xC022_0000
- Address = Base Address + 0x0040, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
AES_Data	[7:0]	RW	Write buffer to store AES-encrypted data in memory before starting decryption Memory address is automatically increased. Zeros should be padded for 128 bits align.	0x00

37.5.1.4 SPDIF Registers

37.5.1.4.1 SPDIFIN_CLK_CTRL

- Base Address: 0xC023_0000
- Address = Base Address + 0x0000, Reset Value = 0x02

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
ready_clk_down	[1]	RW	0 = Clock is enabled 1 = Ready for disabling clock (default)	1'b1
power_on	[0]	RW	0 = Clock will be disabled (default) 1 = Clock will be activated If this bit is reset, SPDIFIN stops checking the input signal just before next "sub-frame" of SPDIF signal format and wait the "acknowledge" signal from HDMI for unresolved previous 'request' toward HDMI. Then asserts "ready_clk_down" as HIGH. To initialize internal states, you have to assert S/W reset, i.e. SPDIFIN_OP_CTRL. op_ctrl = 00b right after activating clock again.	1'b0

37.5.1.4.2 SPDIFIN_OP_CTRL

- Base Address: 0xC023_0000
- Address = Base Address + 0x0004, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
op_ctrl	[1:0]	RW	00b = Software reset 01b = Status checking mode (run) 11b = Status checking + HDMI operation mode (run with HDMI) Others = undefined, do not use 00b = During a software reset, all state machines are set to the idle or in it state and all internal registers are set to their initial values. Interrupt status registers are cleared, all other registers that are writable by the system processor keep their values. 01b = This command should be asserted after SPDIFIN_CLK_CTRL.power_on is set. SPDIFIN starts clock recovery. When recovery is done, SPDIFIN begins detecting preambles of SPDIF signal format and stream data header, abnormal time signal input, abnormal signal input, and also reports this status via interrupts in SPDIFIN_IRQ_STATUS. 11b = "01b" case operations + checking internal buffer overflow + write received data, which can be either audio sample word of PCM or payload of stream. Data will be transferred via HDMI. • You should assert op_ctrl = 11b after SPDIFIN_IRQ_STATUS. ch_status_recovered_ir was asserted at least once for linear PCM data. Or you should assert op_ctrl = 11b after SPDIFIN_IRQ_STATUS. stream_header_detected_ir was asserted at least once for non-linear PCM stream data.	2'b0

37.5.1.4.3 SPDIFIN_IRQ_MASK

- Base Address: 0xC023_0000
- Address = Base Address + 0x0008, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
buf_overflow_ir_en	[7]	RW	Mask bit for Interrupt 7	1'b0
RSVD	[6]	RW	Reserved	-
RSVD	[5]	RW	Reserved	-
stream_hdr_det_ir_en	[4]	RW	Mask bit for Interrupt 4 (stream header detected interrupt enable)	1'b0
stream_hdr_not_det_ir_en	[3]	RW	Mask bit for Interrupt 3 (stream header not detected interrupt enable)	1'b0
wrong_preamble_ir_en	[2]	RW	Mask bit for Interrupt 2	1'b0
ch_status_recovered_ir_en	[1]	RW	Mask bit for Interrupt 1	1'b0
wrong_signal_ir_en	[0]	RW	Mask bit for Interrupt 0	1'b0

NOTE:

0 = Interrupt generation is disabled.

1 = Interrupt generation is enabled

37.5.1.4.4 SPDIFIN_IRQ_STATUS

- Base Address: 0xC023_0000
- Address = Base Address + 0x000C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
buf_overflow_ir	[7]	RW	0 = No interrupt 1 = Internal buffer overflow SPDIFIN internal buffer(s) (SPDIFIN_DATA_BUF_x) was overflowed because HDMI did not transfer the data in the buffer(s) to memory in time. • This interrupt will be asserted only if SPDIFIN_OP_CTRL.op_ctrl was set as "011". • If user does not handle this interrupt, SPDIFIN will over write next subframe data to the internal data buffer (SPDIFIN_DATA_BUF_x) and continue data transfer via HDMI.	1'b0
RSVD	[6]	RW	Reserved	-
RSVD	[5]	RW	Reserved	-
stream_hdr_det_ir	[4]	RW	0 = No interrupt 1 = Stream data header (Pa to Pd) detected • This interrupt will be asserted when SPDIFIN_OP_CTRL.op_ctrl = 001b or 011b. • Cases for interrupt case1: Initially after power_on case2: Next stream header at right time when receiving stream data with SPDIFIN_CONFIG.data_type set as stream mode. case3: Initially detected stream header when receiving stream data with SPDIFIN_CONFIG.data_type set as PCM mode.	1'b0
stream_hdr_not_det_ir	[3]	RW	0 = No interrupt 1 = Stream data header not detected for 4096 repetition time • This interrupt will be asserted when SPDIFIN_OP_CTRL.op_ctrl = 001b or 011b. • Cases for interrupt case1: Initially after power_on case2: SPDIFIN was receiving stream but could not find next stream header for 4096 repetition time since previous stream header case3: Could not find stream header for 4096 repetition time since previous reset of repetition time counter after previous interrupt of stream_header_not_detected_ir.	1'b0
wrong_preamble_ir	[2]	RW	0 = No interrupt 1 = Preamble was detected but there is a problem with detected time	1'b0

Name	Bit	Type	Description	Reset Value
			• This interrupt will be asserted when SPDIFIN_OP_CTRL.op_ctrl = 001b or 011b. Meaningless until ch_status_recovered_ir is asserted initially af- ter SPDIFIN_OP_CTRL.op_ctrl=01b • Cases for interrupt case1: preamble was detected in the middle of a sub-frame audio sample word time case2: next preamble was not detected at exact time after a sub-frame duration case3: it was time for preamble B (or M or W) to be detected but other preamble was detected at that time	
ch_status_recovered_ir	[1]	RW	0 = No interrupt 1 = Recovered channel status Detected preamble of 2 consecutive B-preamble thus recovered 192-bit wide channel status. • Only supports consumer mode, so just 36 bits will be reconstructed. If a user wants to see the channel status bits through SPDIFIN_CH_STATUS_x, you'd better read two consecutive "ch_status_recovered_ir" and read that register each time; if these two channel status value are same, you can rely on that value.	1'b0
wrong_signal_ir	[0]	RW	0 = No interrupt 1 = Clock recovery fail Can not recover clock from input because of tolerable range violation(unlock) or because of no signal from outside or because of non-biphase in non-preamble duration • Meaningless until ch_status_recovered_ir is asserted initially after SPDIFIN_OP_CTRL.op_ctrl = 01b	1'b0

For every bit the following holds: Reading returns interrupt request status. Writing "0" has no effect. Writing "1" clears the interrupt request.

1) Detection of stream header Wait for matching of Pa, Pb; 0xF872, 0x4E1F respectively Wait for their petition time (FromdecodedPcvalueorfromuser-setPcinSPDIFIN_USER_VALUE.repetition_time_manual according to SPDIFIN_CONFIG. PcPd_value_mode) Check for matching of Pa, Pb on right time.

37.5.1.4.5 SPDIFIN_CONFIG_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0010, Reset Value = 0x02

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
noise_filter_samples	[6]	RW	0 = Filtering with 3 consecutive samples 1 = Filtering with 2 consecutive samples Noise filtering is done for over-sampled SPDIF input signal. This operation will be done as follows. If "noise_filter_samples" is 0, 3 consecutive over-sampled signals will be regarded as a high or low only when those 3 samples are all high or low respectively. If 1 or 2 samples are low or high respectively for 3 over-sample duration, that noise filtered signal will keep previous value. If "noise_filter_samples" is 1, 2 consecutive oversampled signals will be regarded as a high or low only when those 2 samples are all high or low respectively. This setting can be used for reduced over-sampling ratio; recommended over-sampling ratio is 10 (see also clk_divisor)	1'b0
RSVD	[5]	RW	Reserved (Must be 0)	1'b0
PcPd_value_mode	[4]	RW	0 = Automatically set 1 = Manually set If 0 for automatic setting, Pc, Pd values will be chosen by value of Pc, Pd from decoded stream header reported as in SPDIFIN_Px_INFO. If user sets this register, the receiver will use SPDIFIN_USER_VALUE[31:16], SPDIFIN_USER_VALUE[15:4] value as Pc, Pd respectively instead of decoded data from stream header as reported in SPDIFIN_Px_INFO. (cf) Burst payload length, whether it is automatically set or manually set, will affect the data size to be written in memory via HD- MI by dumping the full sub-frame for the last bit for burst payload length. For example, if burst payload length is 257-bit, i.e. (16 sub-frame 16-bit + 1-bit), then HDMI will write data in 17 consecutive sub-frames.	1'b0
word_length_value_mode	[3]	RW	0 = Automatically set 1 = Manually set If 0 for automatic setting, word length value will be chosen by value of channel status from decoded SPDIF format as reported in SPDIFIN_CH_STATUS_1. word_length. If user sets this register, the receiver will use	1'b0

Name	Bit	Type	Description	Reset Value
			SPDIFIN_USER_VALUE[3:0] value as word length instead of decoded data from channel status as reported in SPDIFIN_CH_STATUS_1.word_length.	
U_V_C_P_report	[2]	RW	0 = Neglects user_bit, validity_bit, channel status parity_bit of SPDIF format. 1 = Reports user_bit, validity_bit, channel status parity_bit of SPDIF format Report will be via HDMI for each sub-frame. Valid only if SPDIFIN_CONFIG. data_align is set for 32-bit mode; see also SPDIFIN_DATA_BUF_x.	1'b0
RSVD	[1]	RW	Reserved (Must be 1)	1'b1
data_align	[0]	RW	0 = 16-bit mode 1 = 32-bit mode • 16-bit: only takes 16 bits from MSB in a subframe of SPDIF format then concatenates two consecutive 16-bit data in one 32-bit register of SPDIFIN_DATA_BUF_x. • 32-bit: data from one sub-frame with zero padding to MSB part. (ex: 0x00ffffff for 24-bit data) When stream mode, you should set "word_length_value_mode" as 1 and set SPDIFIN_USER_VALUE. word_length_manual as 0b000. These two modes will be applied to both modes of SPDIFIN_CONFIG. data_type, i.e. PCM or stream; see also SPDIFIN_DATA_BUF_x.	1'b0

37.5.1.4.6 SPDIFIN_CONFIG_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x0014, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	RW	Reserved	-
clk_divisor	[3:0]	RW	SPDIFIN_internal_clock = system_clock/(clk_divisor + 1) (SPDIFIN_internal_clock ≤ 135 MHz) SPDIFIN over-samples the SPDIF input signal with internally made clock which is divided from system clock. Recommended over-sampling ratio is 8 to 10, thus following calculation holds. Recommended SPDIFIN_internal_clock (ex) 48 kHz × 64 bits × 10 times-over-sampling = 31 MHz	4'b0

37.5.1.4.7 SPDIFIN_USER_VALUE_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0020, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
repetition_time_manual_low	[7:4]	R	Repetition time[3:0] Repetition_time_manual register 12 bits value. This register is low 4 bits. Will be used for counting one block of stream data; valid only when SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. (Unit: frames (1 frame = 2 sub-frames) of SPDIF format) The value should be (actual repetition time – 1). For example, if you want to use 1536 as manually set repetition time, you should write 1535.	4'b0
word_length_manual	[3:0]	R	Word length Will be used as size for transferring da- ta to memory via HDMI; valid only when SPDIFIN_CONFIG.word_length_value_mode is set for man- ual mode; see also SPDIFIN_DATA_BUF_x. [0] is 1 [0] is 0 [3:1] 101 = 24 bits 20 bits 001 = 23 bits 19 bits 010 = 22 bits 18 bits 011 = 21 bits 17 bits 100 = 20 bits 16 bits	4'b0

37.5.1.4.8 SPDIFIN_USER_VALUE_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x0024, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
repetition_time_manual_high	[7:0]	R	Repetition time[11:4] Repetition_time_manual register 12 bits value. This register is high 8 bits. Will be used for counting one block of stream data; valid only when SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. (Unit: frames (1 frame = 2 sub-frames) of SPDIF format) The value should be (actual repetition time – 1). For example, if you want to use 1536 as manually set repetition time, you should write 1535.	0x00

37.5.1.4.9 SPDIFIN_USER_VALUE_3

- Base Address: 0xC023_0000
- Address = Base Address + 0x0028, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
burst_payload_len_manual_low	[7:0]	R	Burst_payload_length_manual[7:0] Burst_payload_length register is 16 bits value. This register is low 8 bits Valid only when SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. (Unit: bits)	0x00

37.5.1.4.10 SPDIFIN_USER_VALUE_4

- Base Address: 0xC023_0000
- Address = Base Address + 0x002C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
burst_payload_len_manual_high	[7:0]	R	Burst_payload_length_manual[15:8] Burst_payload_length register is 16 bits value. this register is high 8 bits Valid only when SPDIFIN_CONFIG.PcPd_value_mode is set for manual mode. (Unit: bits)	0x00

37.5.1.4.11 SPDIFIN_CH_STATUS_0_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0030, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
channel_status_mode	[7:6]	R	00 = Mode 0 others = reserved	2'b0
emphasis	[5:3]	R	000 = Emphasis not indicated 100 = Emphasis - CD type	2'b0
copyright_assertion	[2]	R	0 = Copyright 1 = No copyright	1'b0
audio_sample_word	[1]	R	0 = Linear PCM 1 = Non-linear PCM	1'b0
channel_status_block	[0]	R	0 = Consumer format 1 = Professional format	1'b0

This register will be updated every 192 frames (1 block) of SPDIF format. SPDIFIN_CH_STATUS_0_1[7:0]is matched internal register SPDIFIN_CH_STATUS_0 [7:0].

37.5.1.4.12 SPDIFIN_CH_STATUS_0_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x0034, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
category_code	[7:0]	R	Equipment type: [8:15] CD player: 1000_0000 DAT player: 1100_000L DCC player: 1100_001L Mini disc: 1001_001L (L: information about generation status of the material)	0x00

37.5.1.4.13 SPDIFIN_CH_STATUS_0_3

- Base Address: 0xC023_0000
- Address = Base Address + 0x0038, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
channel_number	[7:4]	R	Channel Number (bit 20 is LSB)	4'b0
source_number	[3:0]	R	Source Number (bit 16 is LSB)	4'b0

37.5.1.4.14 SPDIFIN_CH_STATUS_0_4

- Base Address: 0xC023_0000
- Address = Base Address + 0x003C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	R	Reserved	-
clock_accuracy	[5:4]	R	Clock accuracy 00 = Level II, 1000ppm 01 = Level I, 50ppm 10 = Level III, variable pitch shifted	2'b0
sampling_frequency	[3:0]	R	Sampling Frequency 0100 = 22.05 kHz 0000 = 44.1 kHz 1000 = 88.2 kHz 1100 = 176.4 kHz 0110 = 24 kHz 0010 = 48 kHz 1010 = 96 kHz 1110 = 192 kHz 0011 = 32 kHz	4'b0

37.5.1.4.15 SPDIFIN_CH_STATUS_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0040, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	-
word_length	[3:1]	R	Word Length (field_size = 1) (field_size = 0) 000 = Not indicated not indicated 101 = 24 bits 20 bits 100 = 23 bits 19 bits 010 = 22 bits 18 bits 110 = 21 bits 17 bits 001 = 20 bits 16 bits	3'b0
field_size	[0]	R	Field Size 0 = Maximum length 20 bits 1 = Maximum length 24 bits	1'b0

37.5.1.4.16 SPDIFIN_FRAME_PERIOD_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0048, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
frame_cnt_low	[7:0]	R	Frame count value [7:0] Frame_cnt register is 16 bits value. This is low 8 bits. The period of a frame (2 sub-frames), thus this register will be updated every 2 sub-frames. It will be measured by "SPDIFIN_internal_clk" made with SPDIFIN_CONFIG.clk_divisor. (Unit: SPDIF_internal_clk Cycles) (Recommended value for locking incoming signals: Over 0x220 (8.5 times × 64 bits))	0x00

37.5.1.4.17 SPDIFIN_FRAME_PERIOD_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x004C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
frame_cnt_high	[7:0]	R	Frame count value [15:8] Frame_cnt register is 16 bits value. This is high 8 bits. The period of a frame (2 sub-frames), thus this register will be updated every 2 sub-frames. It will be measured by "SPDIFIN_internal_clk" made with SPDIFIN_CONFIG.clk_divisor. (Unit: SPDIF_internal_clk Cycles) (Recommended value for locking incoming signals: Over 0x220 (8.5 times × 64 bits))	0x00

37.5.1.4.18 SPDIFIN_Pc_INFO_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0050, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
error_flag	[7]	R	0 = Valid burst payload 1 = Burst payload may contain errors	1'b0
RSVD	[6:5]	R	Reserved	-
compressed_data_type	[4:0]	R	0d: Null data 1d: Dolby AC-3 2d: Reserved 3d: Pause 4d: MPEG-1 layer 1 5d: MPEG-1 layer 2 or 3 or MPEG-2 w/o extension 6d: MPEG-2 w/extension 7d: reserved 8d: MPEG-2 layer 1 low sampling freq. 9d: MPEG-2 layer 2 or 3 low sampling freq. 10d: Reserved 11d, 12d, 13d: DTS 14d to 31d: Reserved	5'b0

37.5.1.4.19 SPDIFIN_Pc_INFO_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x0054, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
bit_stream_number	[7:5]	R	Bit stream number.	3'b0
data_type_dependent_info	[4:0]	R	Data type dependent information.	5'b0

37.5.1.4.20 SPDIFIN_Pd_INFO_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0058, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
burst_payload_length_low	[7:0]	R	Length of burst payload [7:0] (Unit: bits)	0x00

37.5.1.4.21 SPDIFIN_Pd_INFO_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x005C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
burst_payload_length_high	[7:0]	R	length of burst payload [15:8] (Unit: bits)	0x00

37.5.1.4.22 SPDIFIN_DATA_BUF_0_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0060, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_0_1	[7:0]	R	PCM or stream data for 1st burst of HDMI SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] When SPDIFIN_CONFIG.data_align is 0 for 16-bit received_data = {data_(N)th, data_(N+1)th} When SPDIFIN_CONFIG.data_align is 1 for 32-bit received_data = {U, V, C, P, zero-padding, data[n:0]} received_data = {zero-padding, data[n:0]} (if SPDIFIN_CONFIG.U_V_P_report is 0) ("n" is dependent on SPDIFIN_CH_STATUS_1. word_length when SPDIFIN_CONFIG. data_type is 0 for PCM. Or "n" is 15 when SPDIFIN_CONFIG.data_type is 1 for stream) If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

37.5.1.4.23 SPDIFIN_DATA_BUF_0_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x0064, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_0_2	[7:0]	R	PCM or stream data for 1st burst of HDMI SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] When SPDIFIN_CONFIG.data_align is 0 for 16-bit received_data = {data_(N)th, data_(N+1)th} When SPDIFIN_CONFIG.data_align is 1 for 32-bit received_data = {U, V, C, P, zero-padding, data[n:0]} received_data = {zero-padding, data[n:0]} (if SPDIFIN_CONFIG.U_V_P_report is 0) ("n" is dependent on SPDIFIN_CH_STATUS_1. word_length when SPDIFIN_CONFIG. data_type is 0 for PCM. Or "n" is 15 when SPDIFIN_CONFIG.data_type is 1 for stream) If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

37.5.1.4.24 SPDIFIN_DATA_BUF_0_3

- Base Address: 0xC023_0000
- Address = Base Address + 0x0068, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_0_3	[7:0]	R	PCM or stream data for 1st burst of HDMI SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] When SPDIFIN_CONFIG.data_align is 0 for 16-bit received_data = {data_(N)th, data_(N+1)th} When SPDIFIN_CONFIG.data_align is 1 for 32-bit received_data = {U, V, C, P, zero-padding, data[n:0]} received_data = {zero-padding, data[n:0]} (if SPDIFIN_CONFIG.U_V_P_report is 0) ("n" is dependent on SPDIFIN_CH_STATUS_1. word_length when SPDIFIN_CONFIG. data_type is 0 for PCM. Or "n" is 15 when SPDIFIN_CONFIG.data_type is 1 for stream) If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

37.5.1.4.25 SPDIFIN_USER_BUF_0

- Base Address: 0xC023_0000
- Address = Base Address + 0x006C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_user_0	[7:4]	R	User bit of 1st burst of HDMI received_data[7:4] = SPDIFIN_DATA_BUF_0[31:28]	4'b0
RSVD	[3:0]	R	Reserved	-

37.5.1.4.26 SPDIFIN_DATA_BUF_1_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x0070, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_data_1_1	[7:0]	R	PCM or stream data for 2nd burst of HDMI SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] When SPDIFIN_CONFIG.data_align is 0 for 16-bit received_data = {data_(N)th, data_(N+1)th} When SPDIFIN_CONFIG.data_align is 1 for 32-bit received_data = {U, V, C, P, zero-padding, data[n:0]} received_data = {zero-padding, data[n:0]} (if SPDIFIN_CONFIG.U_V_P_report is 0) ("n" is dependent on SPDIFIN_CH_STATUS_1. word_length when SPDIFIN_CONFIG. data_type is 0 for PCM. Or "n" is 15 when SPDIFIN_CONFIG.data_type is 1 for stream) If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

37.5.1.4.27 SPDIFIN_DATA_BUF_1_2

- Base Address: 0xC023_0000
- Address = Base Address + 0x0074, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_data_1_2	[7:0]	R	PCM or stream data for 2nd burst of HDMI SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] When SPDIFIN_CONFIG.data_align is 0 for 16-bit received_data = {data_(N)th, data_(N+1)th} When SPDIFIN_CONFIG.data_align is 1 for 32-bit received_data = {U, V, C, P, zero-padding, data[n:0]} received_data = {zero-padding, data[n:0]} (if SPDIFIN_CONFIG.U_V_P_report is 0) ("n" is dependent on SPDIFIN_CH_STATUS_1. word_length when SPDIFIN_CONFIG. data_type is 0 for PCM. Or "n" is 15 when SPDIFIN_CONFIG.data_type is 1 for stream) If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

37.5.1.4.28 SPDIFIN_DATA_BUF_1_3

- Base Address: 0xC023_0000
- Address = Base Address + 0x0078, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_data_1_3	[7:0]	R	PCM or stream data for 2nd burst of HDMI SPDIFIN_DATA_BUF_0_1 = SPDIFIN_DATA_BUF_0[7:0] SPDIFIN_DATA_BUF_0_2 = SPDIFIN_DATA_BUF_0[15:8] SPDIFIN_DATA_BUF_0_3 = SPDIFIN_DATA_BUF_0[23:16] When SPDIFIN_CONFIG.data_align is 0 for 16-bit received_data = {data_(N)th, data_(N+1)th} When SPDIFIN_CONFIG.data_align is 1 for 32-bit received_data = {U, V, C, P, zero-padding, data[n:0]} received_data = {zero-padding, data[n:0]} (if SPDIFIN_CONFIG.U_V_P_report is 0) ("n" is dependent on SPDIFIN_CH_STATUS_1. word_length when SPDIFIN_CONFIG. data_type is 0 for PCM. Or "n" is 15 when SPDIFIN_CONFIG.data_type is 1 for stream) If SPDIFIN_CONFIG.HDMI_burst_size is 1 burst, HDMI accesses only this data register.	0x00

37.5.1.4.29 SPDIFIN_USER_BUF_1

- Base Address: 0xC023_0000
- Address = Base Address + 0x007C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
received_data_user_1	[7:4]	R	User bit of 2nd burst of HDMI received_data[7:4] = SPDIFIN_DATA_BUF_1[31:28]	4'b0
RSVD	[3:0]	R	Reserved	-

37.5.1.5 I2S Registers

37.5.1.5.1 I2S_CLK_CON

- Base Address: 0xC024_0000
- Address = Base Address + 0x0000, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	7'b0
I2S_en	[0]	RW	I2S Clock Enable 0 = I2S will be disabled (default) 1 = I2S will be activated You must set I2S_en, after other registers are configured. When you want to reset the I2S, this register is 0 – 1.	1'b0

37.5.1.5.2 I2S_CON_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x0004, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
r_sc_pol	[1]	RW	SDATA is synchronous to 0 = SCLK falling edge 1 = SCLK rising edge	1'b0
r_ch_pol	[0]	RW	LRCLK polarity 0 = Left Channel for Low polarity 1 = Left Channel for High polarity	1'b0

37.5.1.5.3 I2S_CON_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x0008, Reset Value = 0x16

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
mlsb	[6]	RW	0 = MSB first mode 1 = LSB first mode	1'b0
bit_ch	[5:4]	RW	Bit clock per Frame (Frame = left + right) 0b00 = 32fs 0b01 = 48fs 0b10 = 64fs	2'b0
data_num	[3:2]	RW	Serial data bit per channel 0b01 = 16-bit 0b10 = 20-bit 0b11 = 24-bit	2'b0
I2S_mode	[1:0]	RW	0b00 = I2S basic format 0b10 = Left justified format 0b11 = Right justified format	2'b0

37.5.1.5.4 I2S_PIN_SEL_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x000C, Reset Value = 0x77

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
pin_sel_1	[6:4]	RW	SCLK(I2S) & DSD_D0(DSD) selection 0b111 = i_I2S_in[1] 0b110 = i_I2S_in[6] 0b101 = i_I2S_in[5] 0b100 = i_I2S_in[4] 0b011 = i_I2S_in[3] 0b010 = i_I2S_in[2] 0b001 = i_I2S_in[1] 0b000 = i_I2S_in[0]	3'b111
RSVD	[3]	RW	Reserved	-
pin_sel_0	[2:0]	RW	LRCK(I2S) & DSD_CLK(DSD) selection 0b111 = i_I2S_in[0] 0b110 = i_I2S_in[6] 0b101 = i_I2S_in[5] 0b100 = i_I2S_in[4] 0b011 = i_I2S_in[3] 0b010 = i_I2S_in[2] 0b001 = i_I2S_in[1] 0b000 = i_I2S_in[0]	3'b111

37.5.1.5.5 I2S_PIN_SEL_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x0010, Reset Value = 0x77

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
pin_sel_3	[6:4]	RW	SDATA_1(I2S) & DSD_D2(DSD) selection 0b111 = i_I2S_in[3] 0b110 = i_I2S_in[6] 0b101 = i_I2S_in[5] 0b100 = i_I2S_in[4] 0b011 = i_I2S_in[3] 0b010 = i_I2S_in[2] 0b001 = i_I2S_in[1] 0b000 = i_I2S_in[0]	3'b111
RSVD	[3]	RW	0	-
pin_sel_2	[2:0]	RW	SDATA_0(I2S) & DSD_D1(DSD) selection 0b111 = i_I2S_in[2] 0b110 = i_I2S_in[6] 0b101 = i_I2S_in[5] 0b100 = i_I2S_in[4] 0b011 = i_I2S_in[3] 0b010 = i_I2S_in[2] 0b001 = i_I2S_in[1] 0b000 = i_I2S_in[0]	3'b111

37.5.1.5.6 I2S_PIN_SEL_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x0014, Reset Value = 0x77

Name	Bit	Type	Description	Reset Value
RSVD	[7]	RW	Reserved	-
pin_sel_5	[6:4]	RW	SDATA_3(I2S) & DSD_D4(DSD) selection 0b111 = i_I2S_in[5] 0b110 = i_I2S_in[6] 0b101 = i_I2S_in[5] 0b100 = i_I2S_in[4] 0b011 = i_I2S_in[3] 0b010 = i_I2S_in[2] 0b001 = i_I2S_in[1] 0b000 = i_I2S_in[0]	3'b111
RSVD	[3]	RW	0	-
pin_sel_4	[2:0]	RW	SDATA_2(I2S) & DSD_D3(DSD) selection 0b111 = i_I2S_in[4] 0b110 = i_I2S_in[6] 0b101 = i_I2S_in[5] 0b100 = i_I2S_in[4] 0b011 = i_I2S_in[3] 0b010 = i_I2S_in[2] 0b001 = i_I2S_in[1] 0b000 = i_I2S_in[0]	3'b111

37.5.1.5.7 I2S_PIN_SEL_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x0018, Reset Value = 0x07

Name	Bit	Type	Description	Reset Value
RSVD	[7:3]	RW	Reserved	-
pin_sel_6	[2:0]	RW	DSD_D5(DSD) selection 0b111 = i_I2S_in[6] 0b110 = i_I2S_in[6] 0b101 = i_I2S_in[5] 0b100 = i_I2S_in[4] 0b011 = i_I2S_in[3] 0b010 = i_I2S_in[2] 0b001 = i_I2S_in[1] 0b000 = i_I2S_in[0]	3'b111

37.5.1.5.8 I2S_DSD_CON

- Base Address: 0xC024_0000
- Address = Base Address + 0x001C, Reset Value = 0x02

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
r_dsd_pol	[1]	RW	0 = DSD_DATA change at DSD_CLK falling edge 1 = DSD_DATA change at DSD_CLK rising edge	1'b1
dsd_en	[0]	RW	0 = DSD module disable 1 = DSD module enable	1'b0

37.5.1.5.9 I2S_MUX_CON

- Base Address: 0xC024_0000
- Address = Base Address + 0x0020, Reset Value = 0x60

Name	Bit	Type	Description	Reset Value
f_num	[7:5]	RW	Number of stage of noise filter for I2S input pins 000 = No filtering 001 = 2 stage filter 010 = 3 stage filter 011 = 4 stage filter 100 = 5 stage filter others = Reserved	3'b110
in_en	[4]	RW	Enable I2S_in, a sub-module at the input stage. 0 = I2S_in module disable 1 = I2S_in module enable All output data is "0" if disabled.	1'b0
audio_sel	[3:2]	RW	Audio selection 0b00 = SPDIF audio data enable 0b01 = I2S audio data enable 0b10 = DSD audio data enable	2'b0
CUV_sel	[1]	RW	C.U.V. Selection 0 = SPDIF C.U.V. data enable 1 = I2S C.U.V. data enable	1'b0
mux_en	[0]	RW	Enable I2S_mux, a sub-module for audio selection. 0 = I2S_mux module disable 1 = I2S_mux module enable All output data is "0" if disabled.	1'b0

37.5.1.5.10 I2S_CH_ST_CON

- Base Address: 0xC024_0000
- Address = Base Address + 0x0024, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
channel_status_reload	[0]	RW	0 = The shadow channel status registers are updated. 1 = Set this bit to update the shadow channel status registers with the values updated in I2S_CH_ST_0 to I2S_CH_ST_4. When the shadow channel status registers are updated, this bit is cleared.	1'b0

Channel status information needs to be applied to the audio stream at the IEC 60958 block boundary. For this synchronization, there are two register sets for channel status block. Users can set the channel status registers, I2S_CH_ST_0 to I2S_CH_ST_4, while the I2S Rx module still refers to the shadow channel status registers, I2S_CH_ST_SH_0 to I2S_CH_ST_CH4.To reflect the user configuration in the channel status registers, users should set channel_status_reload bit in I2S_CH_ST_CON then I2S Rx module copies the channel status registers into the shadow channel status registers at the beginning of an IEC-60958 block.

37.5.1.5.11 I2S_CH_ST_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x0028, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
hannel_status_mode	[7:6]	RW	0b00 = Mode 0 others = Reserved	2'b0
emphasis	[5:3]	RW	When bit1 = 0, 0b000 = 2 audio channels without pre-emphasis* 0b001 = 2 audio channels with 50us/15us pre emphasis When bit1 = 1, 0b000 = Default state	3'b0
copyright	[2]	RW	0 = Copyright 1 = No copyright	1'b0
audio_sample_word	[1]	RW	0 = linear PCM 1 = Non-linear PCM	1'b0
channel_status_block	[0]	RW	0 = Consumer format 1 = Professional format	1'b0

Note that bits listed here in Channel Status Registers look swapped from those in IEC-60958-3 Specification, as the bit order is different (LSB is right-most bit)

37.5.1.5.12 I2S_CH_ST_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x002C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
category	[7:0]	RW	Equipment type CD player: 0000_0001 DAT player: L000_0011 DCC player: L100_0011 Mini disc: L100_1001 (L: information about generation status of the material)	0x00

37.5.1.5.13 I2S_CH_ST_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x0030, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
channel_number	[7:4]	RW	Channel Number NOTE: that bit4 is LSB.	4'b0
source_number	[3:0]	RW	Source Number NOTE: that bit0 is LSB.	4'b0

37.5.1.5.14 I2S_CH_ST_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x0034, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	RW	Reserved	-
Clock_Accuracy	[5:4]	RW	Clock Accuracy as specified in IEC-60958-3 0b01 = Level I, 50 ppm 0b00 = Level II, 1000 ppm 0b10 = Level III, variable pitch shifted	2'b0
Sampling_Frequency	[3:0]	RW	Sampling Frequency as specified in IEC-60958-3 0b0000 = 44.1 kHz 0b0010 = 48 kHz 0b0011 = 32 kHz 0b1010 = 96 kHz &	4'b0

37.5.1.5.15 I2S_CH_ST_4

- Base Address: 0xC024_0000
- Address = Base Address + 0x0038, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Org_Sampling_Freq	[7:4]	RW	Original Sampling Frequency 0b1111 = 44.1 kHz 0b0111 = 88.2 kHz 0b1011 = 22.05 kHz 0b0011 = 176.4 kHz & For other frequencies, refer to original sampling frequency specified in IEC-60958-3	4'b0
Word_Length	[3:1]	RW	Word length Max. length 24 bits 24 bits 0b000 = Not defined not defined 0b001 = 20 bits 16 bits 0b010 = 22 bits 18 bits 0b100 = 23 bits 19 bits 0b101 = 24 bits 20 bits 0b110 = 21 bits 17 bits	3'b0
Max_Word_Length	[0]	RW	Maximum sample word length 0 = 20 bits 1 = 24 bits	1'b0

37.5.1.5.16 I2S_CH_ST_SH_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x003C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
channel_status_mode	[7:6]	R	0b00 = Mode 0 Others = Reserved	2'b0
emphasis	[5:3]	R	When bit1 = 0, 0b000 = 2 audio channels without pre-emphasis* 0b001 = 2 audio channels with 50us/15us pre-emphasis When bit1 = 1, 0b000 = Default state	3'b0
copyright	[2]	R	0 = Copyright 1 = No copyright	1'b0
audio_sample_word	[1]	R	0 = Linear PCM 1 = Non-linear PCM	1'b0
channel_status_block	[0]	R	0 = Consumer format 1 = Professional format	1'b0

37.5.1.5.17 I2S_CH_ST_SH_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x0040, Reset Value =0x00

Name	Bit	Type	Description	Reset Value
category	[7:0]	R	Equipment type CD player: 0000_0001 DAT player: L000_0011 DCC player: L100_0011 Mini disc: L100_1001 (L: information about generation status of the material)	0x00

37.5.1.5.18 I2S_CH_ST_SH_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x0044, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
channel_number	[7:4]	R	Channel Number NOTE: that bit4 is LSB.	4'b0
source_number	[3:0]	R	Source Number NOTE: that bit0 is LSB.	4'b0

37.5.1.5.19 I2S_CH_ST_SH_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x0048, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	R	Reserved	-
Clock_Accuracy	[5:4]	R	Clock Accuracy as specified in IEC-60958-3 0b01 = Level I, 50 ppm 0b00 = Level II, 1000 ppm 0b10 = Level III, variable pitch shifted	2'b0
Sampling_Frequency	[3:0]	R	Sampling Frequency as specified in IEC-60958-3 0b0000 = 44.1 kHz 0b0010 = 48 kHz 0b0011 = 32 kHz 0b1010 = 96 kHz &	4'b0

37.5.1.5.20 I2S_CH_ST_SH_4

- Base Address: 0xC024_0000
- Address = Base Address + 0x004C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Org_Sampling_Freq	[7:4]	RW	Original Sampling Frequency 0b1111 = 44.1 kHz 0b0111 = 88.2 kHz 0b1011 = 22.05 kHz 0b0011 = 176.4 kHz & For other frequencies, refer to original sampling frequency specified in IEC-60958-3	4'b0
Word_Length	[3:1]	RW	Word length Max. length 24 bits 20 bits 0b000 = Not defined not defined 0b001 = 20 bits 16 bits 0b010 = 22 bits 18 bits 0b100 = 23 bits 19 bits 0b101 = 24 bits 20 bits 0b110 = 21 bits 17 bits	3'b0
Max_Word_Length	[0]	RW	Maximum sample word length 0 = 20 bits 1 = 24 bits	1'b0

37.5.1.5.21 I2S_VD_DATA

- Base Address: 0xC024_0000
- Address = Base Address + 0x0050, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:1]	RW	Reserved	-
validity_flag	[0]	RW	Validity bit 0 = Audio sample is reliable 1 = Audio sample is unreliable	1'b0

37.5.1.5.22 I2S_MUX_CH

- Base Address: 0xC024_0000
- Address = Base Address + 0x0054, Reset Value = 0x03

Name	Bit	Type	Description	Reset Value
CH3_R_en	[7]	RW	0 = Channel 3 right audio data output is disable 1 = Channel 3 right audio data output is enable	1'b0
CH3_L_en	[6]	RW	0 = Channel 3 left audio data output is disable 1 = Channel 3 left audio data output is enable	1'b0
CH2_R_en	[5]	RW	0 = Channel 2 right audio data output is disable 1 = Channel 2 right audio data output is enable	1'b0
CH2_L_en	[4]	RW	0 = Channel 2 left audio data output is disable 1 = Channel 2 left audio data output is enable	1'b0
CH1_R_en	[3]	RW	0 = Channel 1 right audio data output is disable 1 = Channel 1 right audio data output is enable	1'b0
CH1_L_en	[2]	RW	0 = Channel 1 left audio data output is disable 1 = Channel 1 left audio data output is enable	1'b0
CH0_R_en	[1]	RW	0 = Channel 0 right audio data output is disable 1 = Channel 0 right audio data output is enable	1'b1
CH0_L_en	[0]	RW	0 = Channel 0 left audio data output is disable 1 = Channel 0 left audio data output is enable	1'b1

37.5.1.5.23 I2S_MUX_CUV

- Base Address: 0xC024_0000
- Address = Base Address + 0x0058, Reset Value = 0x03

Name	Bit	Type	Description	Reset Value
RSVD	[7:2]	RW	Reserved	-
CUV_R_en	[1]	RW	0 = Right channel CUV data is disable 1 = Right channel CUV data is enable	1'b1
CUV_L_en	[0]	RW	0 = Left channel CUV data is disable 1 = Left channel CUV data is enable	1'b1

37.5.1.5.24 I2S_CH0_L_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x0064, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.25 I2S_CH0_L_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x0068, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.26 I2S_CH0_L_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x006C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.27 I2S_CH0_R_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x0074, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.28 I2S_CH0_R_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x0078, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.29 I2S_CH0_R_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x007C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.30 I2S_CH0_R_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x0080, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.31 I2S_CH1_L_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x0084, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.32 I2S_CH1_L_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x0088, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.33 I2S_CH1_L_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x008C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.34 I2S_CH1_L_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x0090, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.35 I2S_CH1_R_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x0094, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.36 I2S_CH1_R_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x0098, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.37 I2S_CH1_R_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x009C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.38 I2S_CH1_R_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x00A0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.39 I2S_CH2_L_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x00A4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.40 I2S_CH2_L_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x00A8, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.41 I2S_CH2_L_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x00AC, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.42 I2S_CH2_L_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x00B0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.43 I2S_CH2_R_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x00B4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.44 I2S_CH2_R_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x00B8, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.45 I2S_CH2_R_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x00BC, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.46 I2S_Ch2_R_3

- Base Address: 0xC024_0000
- Address = Base Address + 0x00C0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.47 I2S_CH3_L_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x00C4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.48 I2S_CH3_L_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x00C8, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.49 I2S_CH3_L_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x00CC, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.50 I2S_CH3_R_0

- Base Address: 0xC024_0000
- Address = Base Address + 0x00D0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.51 I2S_CH3_R_1

- Base Address: 0xC024_0000
- Address = Base Address + 0x00D4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.52 I2S_CH3_R_2

- Base Address: 0xC024_0000
- Address = Base Address + 0x00D8, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
I2S_CHX_Y_Z	[7:0]	R	PCM output data from I2S Rx module. X: Channel = 0, 1, 2 Y: Left/Right = L, R Z: Byte number I2S_CHX_Y_0 = PCMX_Y[7:0] I2S_CHX_Y_1 = PCMX_Y[15:8] I2S_CHX_Y_2 = PCMX_Y[23:16] I2S_CHX_Y_3 = PCMX_Y[27:24] Channel 3 has 24-bit width. I2S_CH3_Y_0 = PCM3_Y[7:0] I2S_CH3_Y_1 = PCM3_Y[15:8] I2S_CH3_Y_2 = PCM3_Y[23:16]	0x00

37.5.1.5.53 I2S_CUV_L_R

- Base Address: 0xC024_0000
- Address = Base Address + 0x00DC, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7]	R	Reserved	–
CUV_R	[6:4]	RW	VUCP data of Right channel CUV_R[3:0] = {valid bit, user bit, channel state bit, parity bit}	3'b0
RSVD	[3]	RW	Reserved	–
CUV_L	[2:0]	RW	VUCP data of Left channel CUV_L[3:0] = {valid bit, user bit, channel state bit, parity bit}	3'b0

37.5.1.6 CEC Registers

37.5.1.6.1 CEC_TX_STATUS_0

- Base Address: 0xC010_0000
- Address = Base Address + 0x0000, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	–
Tx_Error	[3]	R	CEC Tx_Error interrupts flag. This bit field also indicates the status of Tx_Error interrupt. This bit is valid only when Tx_Done bit is set. 0 = No error has occurred. 1 = An error has occurred during CEC Tx transfer. It will be cleared: when set to 0 Tx_Enable bit of CEC_TX_CTRL register when set Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit in CEC_INTR_CLEAR register	1'b0
Tx_Done	[2]	R	CEC Tx_Done interrupts flag. This bit field also indicates the status of Tx_Done interrupt. 0 = Running or Idle 1 = CEC Tx transfer finished. It will be cleared: • When reset Tx_Enable bit of CEC_TX_CTRL_0 • When set Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit in CEC_INTR_CLEAR register	1'b0
Tx_Transferring	[1]	R	If set RX-Running, this field is valid 0 = Tx is waiting for CEC Bus 1 = CEC Tx is transferring data via CEC Bus.	1'b0
Tx_Running	[0]	R	0 = Tx Idle 1 = CEC Tx is enabled and is either waiting for the CEC bus or transferring message.	1'b0

37.5.1.6.2 CEC_TX_STATUS_1

- Base Address: 0xC010_0000
- Address = Base Address + 0x0004, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Tx_Bytes_Transferred	[7:0]	R	Number of blocks transferred (1 byte = 1 block in a CEC message). After sending CEC message, field will be updated. It will be cleared when set Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit in CEC_Intr_Clear register.	0x00

37.5.1.6.3 CEC_RX_STATUS_0

- Base Address: 0xC010_0000
- Address = Base Address + 0x0008, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:5]	R	Reserved	-
Rx_BCast	[4]	R	Broadcast message flag 0 = Received CEC message is address to a single device. 1 = Received CEC message is a broadcast message. It will be cleared: • When reset Rx_Enable bit of CEC_RX_CTRL_0 • When set Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register	1'b0
Rx_Error	[3]	R	CEC Rx_Error interrupts flag. This bit field also indicates the status of Rx_Error interrupt. This bit is valid only when Rx_Done bit is set. 0 = No error has occurred. 1 = An error has occurred in receiving a CEC message It will be cleared: • When reset Rx_Enable bit of CEC_RX_CTRL_0 • When set Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register	1'b0
Rx_Done	[2]	R	CEC Rx done interrupt Flag. This bit field also indicates the status of Rx_Done interrupt. 0 = Running or Idle 1 = CEC Rx transfer finished It will be cleared: • When reset Rx_Enable bit of CEC_RX_CTRL_0	1'b0

Name	Bit	Type	Description	Reset Value
			• When set Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register	
Rx_Receiving	[1]	R	0 = Rx is waiting for a CEC message. 1 = Rx is currently receiving data via CEC Bus.	1'b0
Rx_Running	[0]	R	0 = Rx disabled 1 = CEC Rx is enabled and is either waiting for a message on the CEC bus.	1'b0

37.5.1.6.4 CEC_RX_STATUS_1

- Base Address: 0xC010_0000
- Address = Base Address + 0x000C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Rx_Bytes_Received	[7:0]	R	Number of blocks received (1 byte = 1 block in a CEC message). After receiving CEC message, field will be updated. It will be cleared when set Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_Intr_Clear register.	0x00

37.5.1.6.5 CEC_INTR_MASK

- Base Address: 0xC010_0000
- Address = Base Address + 0x0010, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	R	Reserved	–
Mask_Intr_Rx_Error	[5]	RW	Rx_Error interrupt mask bit. 0 = Enabled 1 =Disabled.	1'b0
Mask_Intr_Rx_Done	[4]	RW	Rx_Done interrupt mask bit. 0 = Enabled 1 = Disabled.	1'b0
RSVD	[3:2]	RW	Reserved	–
Mask_Intr_Tx_Error	[1]	RW	Tx_Error interrupt mask bit. 0 = Enabled 1 = Disabled.	1'b0
Mask_Intr_Tx_Done	[0]	RW	Tx_Done interrupt mask bit. 0 = Enabled 1 = Disabled	1'b0

37.5.1.6.6 CEC_INTR_CLEAR

- Base Address: 0xC010_0000
- Address = Base Address + 0x0014, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7:6]	R	Reserved	–
Clear_Intr_Rx_Error	[5]	R/W1C	Rx_Error interrupt clear bit. Writing following values will result in: 0 = No effect 1 = Clear Rx_Error and Rx_Bytes_Received fields in CEC_RX_STATUS_0 and 1 register. It will be cleared after one clock.	1'b0
Clear_Intr_Rx_Done	[4]	R/W1C	Rx_Done interrupt clear bit. Writing following values will result in: 0 = No effect 1 = Clears Rx_Done and Rx_Bytes_Received fields in CEC_RX_STATUS_0 and 1 register. Resets to 0 after one clock.	1'b0
RSVD	[3:2]	R	Reserved	–
Clear_Intr_Tx_Error	[1]	R/W1C	Tx_Error interrupt clear bit. Writing following values will result in: 0 = No effect 1 = Clears Tx_Error and Tx_Bytes_Received fields in CEC_TX_STATUS_0 and 1 register. Resets to 0 after one clock.	1'b0
Clear_Intr_Tx_Done	[0]	R/W1C	Tx_Done interrupt clear bit. Writing following values will result in: 0 = No effect 1 = Clears Tx_Done and Tx_Bytes_Received fields in CEC_TX_STATUS_0 and 1 register. Resets to 0 after one clock.	1'b0

37.5.1.6.7 CEC_LOGIC_ADDR

- Base Address: 0xC010_0000
- Address = Base Address + 0x0020, Reset Value =0x0F

Name	Bit	Type	Description	Reset Value
RSVD	[7:4]	R	Reserved	–
Logic_Addr	[3:0]	RW	HDMI Tx logical address (0 to 15)	4'b0

37.5.1.6.8 CEC_DIVISOR_0

- Base Address: 0xC010_0000
- Address = Base Address + 0x0030, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
CEC_Divisor	[7:0]	RW	(CEC_Divisor[7:0] of 32-bit) A divisor used in counting 0.05ms period. This divisor should satisfy the following equation: (CEC_DIVISOR) × (clock cycle time(ns)) = 0.05ms	0x00

37.5.1.6.9 CEC_DIVISOR_1

- Base Address: 0xC010_0000
- Address = Base Address + 0x0034, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
CEC_Divisor	[7:0]	RW	(CEC_Divisor[15:8] of 32-bit) A divisor used in counting 0.05ms period. This divisor should satisfy the following equation: (CEC_DIVISOR) × (clock cycle time(ns)) = 0.05ms	0x00

37.5.1.6.10 CEC_DIVISOR_2

- Base Address: 0xC010_0000
- Address = Base Address + 0x0038, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
CEC_Divisor	[7:0]	RW	(CEC_Divisor[23:16] of 32-bit) A divisor used in counting 0.05ms period. This divisor should satisfy the following equation: (CEC_DIVISOR) × (clock cycle time(ns)) = 0.05ms	0x00

37.5.1.6.11 CEC_DIVISOR_3

- Base Address: 0xC010_0000
- Address = Base Address + 0x003C, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
CEC_Divisor	[7:0]	RW	(CEC_Divisor[31:24] of 32-bit) A divisor used in counting 0.05ms period. This divisor should satisfy the following equation: (CEC_DIVISOR) × (clock cycle time(ns)) = 0.05ms	0x00

37.5.1.6.12 CEC_TX_CTRL

- Base Address: 0xC010_0000
- Address = Base Address + 0x0040, Reset Value = 0x10

Name	Bit	Type	Description	Reset Value
Reset	[7]	R/W1C	CEC Tx reset bit. Writing following values will result in: 0 = No effect 1 = Immediately resets CEC Tx related registers and state machines to its reset value. Resets to 0 after one clock.	1'b0
Tx_Retrans_Num	[6:4]	RW	Number of retransmissions tried when situations in CEC spec. page CEC-13 occurs. According to the specification, it should be set to 5.	3'b001
RSVD	[3:2]	R	Reserved	-
Tx_BCast	[1]	RW	CEC Tx broadcast message bit. This bit indicates whether a CEC message in CEC_TX_BUFFER_00 to 15 is direcly-addressed (ad- dressed to a single device) or broadcast. This bit has effect on determining whether a block transfer is acknowledged or not. (following ACK scheme in CEC Spec.(section CEC 6.1.2)) 0 = Directly-addressed message 1 = Broadcast message.	1'b0
Tx_Start	[0]	R/W1C	CEC Tx start bit. Writing following values will result in: 0 = Tx idle. 1 = Start CEC message transfer (Resets to 0 after start)	1'b0

WhenResetfieldissetto1, CEC_TX_CTRL, CEC_TX_STATUS_03, CEC_TX_BUFFER015 will be set totheir reset values.

37.5.1.6.13 CEC_TX_BYTE_NUM

- Base Address: 0xC010_0000
- Address = Base Address + 0x0044, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Tx_Byte_Num	[7:0]	RW	Number of blocks in a message to be sent. (1 byte = 1 block in a CEC message).	0x00

37.5.1.6.14 CEC_TX_STATUS_2

- Base Address: 0xC010_0000
- Address = Base Address + 0x0060, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Tx_Wait	[7]	R	CEC Tx signal free time waiting flag bit 0 = Tx is in other state 1 = CEC Tx is waiting for a signal free time (time to stop sending messages after previous attempt to send a message).	1'b0
Tx_Sending_Start_Bit	[6]	R	CEC Tx start bit sending flag bit 0 = Tx is in other state 1 = CEC Tx is currently sending a start bit.	1'b0
Tx_Sending_Hdr_Blk	[5]	R	CEC Tx header block sending flag bit 0 = Tx is in other state 1 = CEC Tx is currently sending the header block.	1'b0
Tx_Sending_Data_Blk	[4]	R	CEC Tx data block sending flag bit 0 = Tx is in other state 1 = CEC Tx is currently sending data blocks.	1'b0
Tx_Latest_Initiator	[3]	R	CEC Tx last initiator flag bit 0 = This device is not the latest initiator on the CEC bus. 1 = This CEC device is the latest initiator to send a CEC message and no other CEC device sent a message. It will be cleared if Rx detects a start bit on the CEC line or Tx_Enable bit of CEC_Tx_Ctrl_0 is set (i.e. becomes a new initiator)	1'b0
RSVD	[2:0]	R	Reserved	–

37.5.1.6.15 CEC_TX_STATUS_3

- Base Address: 0xC010_0000
- Address = Base Address + 0x0064, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7]	R	Reserved	–
Tx_Wait_SFT_Succ	[6]	R	CEC Tx signal free time for successive message transfer waiting flag bit 0 = Tx is in other state 1 = Tx is waiting for a signal free time (SFT) with a precondition that Tx is the most recent initiator on the CEC bus and wants to send another frame immediately after its previous frame. (SFT ≥ 7 × 2.4ms)	1'b0
Tx_Wait_SFT_New	[5]	R	CEC Tx signal free time for a new initiator waiting flag bit 0 = Tx is in other state 1 = Tx is waiting for a signal free time (SFT) with a precondition that Tx is a new initiator and wants to send a frame. (SFT ≥ 5 × 2.4ms)	1'b0
Tx_Wait_SFT_Retran	[4]	R	CEC Tx signal free time for a new initiator waiting flag bit 0 = Tx is in other state 1 = Tx is waiting for a signal free time (SFT) with a precondition that Tx is attempting a retransmission of the message. (SFT ≥ 3 × 2.4ms)	1'b0
Tx_Retrans_Cnt	[3:1]	R	It indicates current retransmissions count. If 0, no retransmission occurred. It will be cleared when set Clear_Intr_Tx_Done or Clear_Intr_Tx_Error bit in CEC_Intr_Clear register.	3'b0
Tx_ACK_Failed	[0]	R	CEC Tx acknowledge failed flag bit 0 = Tx is in other state 1 = Tx is not acknowledged. This bit is set when • ACK bit in a block is logical 1 in a directly-addressed message • ACK bit in a block is logical 0 in a broadcast message	1'b0

37.5.1.6.16 CEC_TX_BUFFER_x

- Base Address: 0xC010_0000
- Address = Base Address + 0x0080, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Tx_Block_x	[7:0]	RW	Byte #0 to #15 of CEC message. Each byte corresponds to a block in a message. Block_0 is the header block and Block_1 to 15 are data blocks. Note that initiator and destination logical address in a header block should written by S/W.	0x00

37.5.1.6.17 CEC_RX_CTRL

- Base Address: 0xC010_0000
- Address = Base Address + 0x00C0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Reset	[7]	R/W1C	CEC Rx reset bit. Writing following values will result in: 0 = No effect 1 = Immediately resets CEC Rx related registers and state machines to its reset value. It will be cleared after one clock.	1'b0
Check_Sampling_Error	[6]	RW	CEC Rx sampling error check enable bit. Writing following values will result in: 0 = Do not check sampling error. 1 = Check sampling error while receiving data bits. CEC Rx samples the CEC bus three times (at 1.00, 1.05, 1.10 ms) and checks whether three samples are identical.	1'b0
Check_Low_Time_Error	[5]	RW	CEC Rx low-time error check enable bit. Writing following values will result in: 0 = Do not check low-time error. 1 = Check low-time error while receiving data bits. In receiving each bit from the CEC bus, CEC Rx checks the duration of logical 0 from the starting of one bit transfer (falling edge on the CEC bus). Rx checks whether the duration is longer than the maximum time the CEC bus can be in logical 0 (max 1.7 ms).	1'b0
Check_Start_Bit_Error	[4]	RW	CEC Rx start bit error check enable bit. Writing following values will result in: 0 = Do not check start bit error. 1 = Check start bit error while receiving a start bit. In receiving a start bit from the CEC bus, CEC Rx checks the duration of logical 0 and 1 of a starting bit as specified in CEC spec. page CEC-8. Rx checks whether the duration meets the specification.	1'b0
RSVD	[3:2]	R	Reserved	-

Name	Bit	Type	Description	Reset Value
Rx_Host_Busy	[1]	RW	CEC Rx host busy bit. Writing following values will result in: 0 = Rx receives incoming message and send acknowledges. 1 = A host processor is unavailable to receive and process CEC messages. Rx sends not acknowledged signal to a message initiator to indicate that a host processor is unavailable to receive and process CEC messages.	1'b0
Rx_Enable	[0]	RW	CEC Rx start bit. Writing following values will result in: 0 = Rx disabled. 1 = Enable CEC Rx module to receive a message. This bit is cleared after receiving a message.	1'b0

When Reset field is set to 1, CEC_RX_CTRL, CEC_RX_STATUS_0 to 3, CEC_RX_BUFFER0 to 15 will be set to their reset values.

37.5.1.6.18 CEC_RX_STATUS_2

- Base Address: 0xC010_0000
- Address = Base Address + 0x00E0, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Rx_Waiting	[7]	R	CEC Rx waiting flag bit 0 = Rx is in other state 1 = CEC Rx is waiting for a message.	1'b0
Rx_Receiving_Start_Bit	[6]	R	CEC Rx start bit receiving flag bit 0 = Rx is in other state 1 = CEC Rx is currently receiving a start bit.	1'b0
Rx_Receiving_Hdr_Blk	[5]	R	CEC Rx header block receiving flag bit 0 = Rx is in other state 1 = CEC Rx is currently receiving a header block.	1'b0
Rx_Receiving_Data_Blk	[4]	R	CEC Rx data block receiving flag bit 0 = Rx is in other state 1 = CEC Rx is currently receiving data blocks.	1'b0
RSVD	[3:0]	R	Reserved	–

37.5.1.6.19 CEC_RX_STATUS_3

- Base Address: 0xC010_0000
- Address = Base Address + 0x00E4, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
RSVD	[7]	R	Reserved	–
Sampling_Error	[6]	R	CEC Rx sampling error flag bit 0 = No sampling error has occurred. 1 = A sampling error has occurred in receiving a message. CEC Rx samples the CEC bus three times (at 1.00, 1.05, 1.10 ms) and sets this bit if • Check_Sampling_Error bit in CEC_RX_CTRL_0 is set and • Three samples are not identical. It will be cleared when set to 0 when Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register.	1'b0
Low_Time_Error	[5]	R	CEC Rx low-time error flag bit 0 = No low-time error has occurred. 1 = A low-time error has occurred in receiving a message. In receiving each bit from the CEC bus, CEC Rx checks the duration of logical 0 from the starting of one-bit transfer (falling edge on the CEC bus). If the duration of longer than the maximum time the CEC bus can be in logical 0 (max 1.7 ms), CEC RX sets this bit. This bit field will be set to 0 when Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set.	1'b0
Start_Bit_Error	[4]	R	CEC Rx start bit error flag bit 0 = No start bit error has occurred. 1 = A start bit error has occurred in receiving a message. In receiving a start bit from the CEC bus, CEC Rx checks the duration of logical 0 and 1 of a starting bit as specified in CEC spec. page CEC-8. If the duration does not meet the spec., CEC RX sets this bit. This bit field will be set to 0 when Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register is set.	1'b0
RSVD	[3:1]	R	Reserved	-
CEC_Line_Error	[0]	R	CEC Rx line error flag bit 0 = No line error has occurred. 1 = A start bit error line error has occurred in receiving a message. In CEC spec. page CEC-13, CEC line error is defined as a situation that period between two consecutive falling edges is smaller than a minimum data bit period. Rx checks for this condition and if it occurs, sends line error notification,	1'b0

Name	Bit	Type	Description	Reset Value
			i.e. sending logical 0 for more than 1.4 to 1.6 times of the nominal data bit period (2.4ms). This bit will be cleared: • When set Rx_Enable bit of CEC_RX_CTRL_0 • When set Clear_Intr_Rx_Done or Clear_Intr_Rx_Error bit in CEC_INTR_CLEAR register.	

37.5.1.6.20 CEC_RX_BUFFER_x

- Base Address: 0xC010_0000
- Address = Base Address + 0x0100, Reset Value = 0x00

Name	Bit	Type	Description	Reset Value
Rx_Block_x	[7:0]	R	Byte #0 to #15 of CEC message. Each byte corresponds to a block in a message. Block_0 is the header block and Block_1 to 15 are data blocks.	0x00

37.5.1.6.21 CEC_FILTER_CTRL

- Base Address: 0xC010_0000
- Address = Base Address + 0x0180, Reset Value = 0x81

Name	Bit	Type	Description	Reset Value
Filter_Cur_Val	[7]	RW	CEC filter current value bit. Indicates current value fed to CEC Tx, Rx. When filter is enabled, this bit is the latest value on the CEC bus that is stable for more than Filter_Th cycles.	1'b0
RSVD	[6:1]	R	Reserved	-
Filter_Enable	[0]	RW	CEC filter enable bit. 0 = Filter disabled. Directly passes CEC input to CEC Tx, Rx. 1 = Enable Filter. Filter propagates signals stable for more Filter_Th cycles.	1'b0

37.5.1.6.22 CEC_FILTER_TH

- Base Address: 0xC010_0000
- Address = Base Address + 0x0184, Reset Value = 0x03

Name	Bit	Type	Description	Reset Value
Filter_Th	[7:0]	RW	Filter threshold value. When filter is enabled, it filters out signals stable for less than Filter_Th cycles	0x00

37.6 HDMI PHY

The HDMI PHY can generate a pixel clock for HDMI 1.4 spec with own PCG (Pixel clock generator) that used 24 MHz reference clock. Following is genera table pixel clock frequency table.

Table 37-2 Available Pixel Clock Frequencies of the Integrated Video PLL

Available Pixel Clock Frequency for DTV (MHz)	Available Pixel Clock Frequency for Monitor (MHz)
25.2	25
25.175	65
27	108
27.027	162
54	
54.054	
74.25	
74.176	
148.5	
148.352	
108.108	
72	

37.6.1 PHY Configuration Change through APB

The HDMI PHY has many internal registers to change its configuration, like pixel clock frequency or analog characteristics. Users can access these registers through APB port. For secure configuration of the PHY core, MODE_SET_DONE register (REG_7C<7>) is used for an indicator of APB setting state as shown in *Figure 37-16*. (MODE_SET_DONE register is also controlled by APB.)

If users want store configure the HDMI PHY by new register setting, it should write 00h on MODE_SET_DONE register (0xC010047C) instead of asserting overall RESET signal. Then PHY_READY signal goes to low state and PHY waits for new register setting. After new values are written on PHY registers; MODE_SET_DONE register should be set to 80h again letting PHY start to configure its state with new register values. Once configuration is done, PHY_READY signal is automatically asserted.

Figure 37-16 PHY Configuration through APB with MODE_SET_DONE Register

37.6.2 PHY Ready Sequence

To assert PHY_READY signal, the HDMI PHY have to precede several steps shown in *Figure 37-17*. The HDMI PHY core has a CMU and PCG for TMDS and pixel clock generation. Both of them should be locked and clock de-skewing between TMDS_CLKHI and TMDS_CLKO should be finished before PHY_READY assertion. Thus, TMDS_CLKHI should be supplied to PHY before PHY_READY signal assertion. The HDMI PHY ready sequence is ignited by PHY_RESET signal which is external reset or in version of MODE_SET_DONE signal. Once PLL_LOCK and CMU_LOCK signals go high, the de-skewing process starts. After de-skewing is finished, the PHY_READY signal goes high meaning The HDMI PHY is ready to correctly send TMDS data.

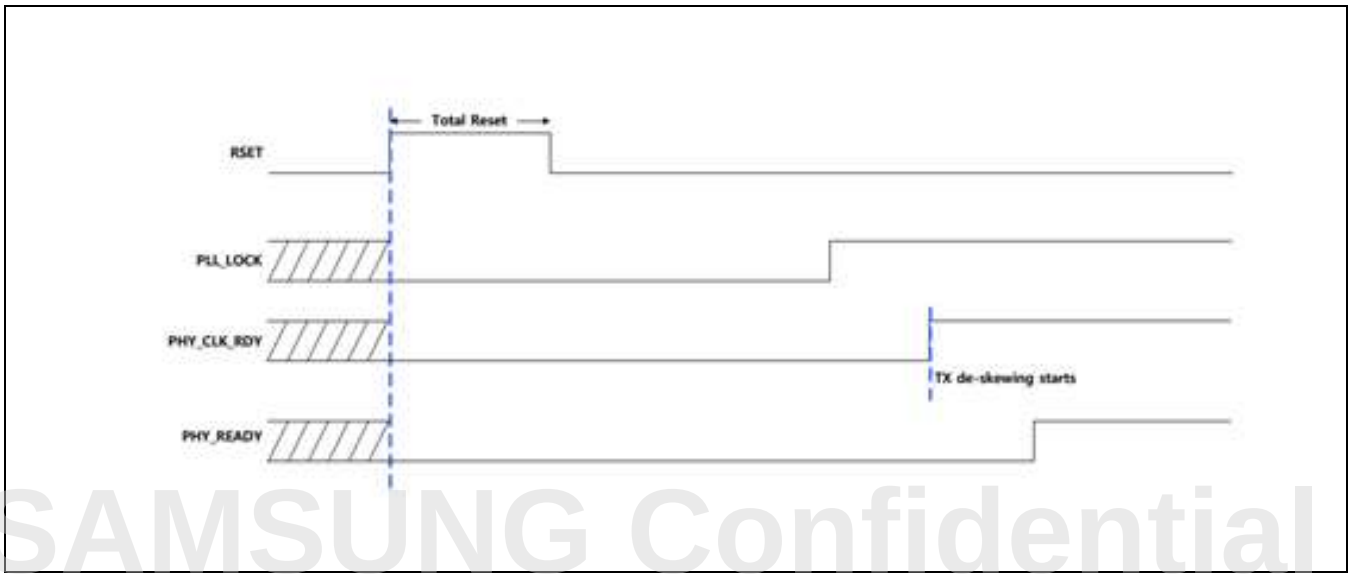


Figure 37-17 PHY Ready Sequence

37.6.3 HDMI PHY Configuration

Users need to set the HDMI PHY configuration to get a generated pixel clock. Following is a sequence of setting the HDMI PHY configuration.

1. Set the HDMI CLKGEN's PCLKMODE with "1" (enable). (RESETREG[0].[10] release need.)
2. Set the TIEOFFREG[3].[0] with "1".
3. Release resets of RESETREG[0].[13] and RESETREG[0].[17] (HDMI PHY reset release).
4. Set the HDMI PHY's registers with *Table 37-3* to generate a pixel clock
5. Check the *PHY_READY*bit of the *PHY_STATUS_0*register (HDMI Link) whether the HDMI PHY's PHY_READY is HIGH.

Table 37-3 HDMI PHY Configuration Table (8-bit Pixel)

Register Address	Pixel Clock Frequency													
	25.2	25.175	27	27.027	54	54.054	74.25	74.176	148.5	148.352	25	65	108	162
0xC0100404	52h	D1h	D1h	D1h	51h	D1h	D1h	D1h	D1h	D1h	D1h	D1h	D1h	D1h
0xC0100408	3Fh	1Fh	22h	2Dh	2Dh	2Dh	1Fh	1Fh	1Fh	1Fh	27h	2Eh	1Fh	27h
0xC010040C	55h	50h	51h	72h	35h	32h	10h	10h	00h	00h	11h	12h	10h	14h
0xC0100410	40h	40h	40h	40h	40h	40h	40h	40h	40h	40h	51h	61h	40h	51h
0xC0100414	01h	20h	08h	64h	01h	64h	40h	5Bh	40h	5Bh	40h	40h	5Bh	5Bh
0xC0100418	00h	1Eh	FCh	12h	00h	12h	F8h	EFh	F8h	EFh	D6h	34h	EFh	A7h
0xC010041C	C8h	C8h	E0h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h	C8h
0xC0100420	82h	81h	98h	43h	82h	43h	81h	81h	81h	81h	81h	82h	81h	84h
0xC0100424	C8h	E8h	E8h	E8h	C8h	E8h	E8h	E8h	E8h	E8h	E8h	E8h	E8h	E8h
0xC0100428	BDh	BDh	CBh	0Eh	0Eh	0Eh	BAh	B9h	BAh	B9h	E8h	16h	B9h	E8h
0xC010042C	D8h	D8h	D8h	D9h	D9h	D9h	D8h	D8h	D8h	D8h	D8h	D9h	D8h	D8h
0xC0100430	45h	45h	45h	45h	45h	45h	45h	45h	45h	45h	45h	45h	45h	45h
0xC0100434	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h
0xC0100438	ACh	ACh	ACh	ACh	ACh	ACh	ACh	ACh	ACh	ACh	ACh	ACh	ACh	ACh
0xC010043C	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h
0xC0100440	06h	06h	06h	06h	06h	06h	56h	56h	66h	66h	56h	56h	56h	56h
0xC0100444	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h
0xC0100448	01h	09h	09h	09h	09h	09h	09h	09h	09h	09h	09h	09h	09h	09h
0xC010044C	84h	84h	84h	84h	84h	84h	84h	84h	84h	84h	84h	84h	84h	84h
0xC0100450	05h	05h	05h	05h	05h	05h	05h	05h	05h	05h	05h	05h	05h	05h
0xC0100454	22h	22h	22h	22h	22h	22h	22h	22h	22h	22h	22h	22h	22h	22h
0xC0100458	24h	24h	24h	24h	24h	24h	24h	24h	24h	24h	24h	24h	24h	24h
0xC010045C	86h	86h	86h	86h	86h	86h	86h	86h	86h	86h	86h	86h	86h	86h
0xC0100460	54h	54h	54h	54h	54h	54h	54h	54h	54h	54h	54h	54h	54h	54h
0xC0100464	F4h	F4h	E4h	E3h	E4h	E3h	A5h	A6h	4Bh	4Bh	84h	B9h	A6h	85h
0xC0100468	24h	24h	24h	24h	24h	24h	24h	24h	25h	25h	24h	25h	24h	24h
0xC010046C	00h	00h	00h	00h	01h	01h	01h	01h	03h	03h	01h	03h	01h	01h
0xC0100470	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0xC0100474	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0xC0100478	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h	01h
0xC010047C	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h	80h
0xC010048C	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h	10h

37.6.4 Register Description

37.6.4.1 Register Map Summary

- Base Address: 0xC010_0000

Register	Offset	Description	Reset Value
HDMI PHY			
HDMIPHY 4h register	0404h	HDMI TX PHY internal PLL Input Clock Selection	0x0000_0091
HDMIPHY 24h register	0424h	REF_CKO Selection	0x0000_0028
HDMIPHY 3ch register	043Ch	TMDS Data Amplitude Control	0x0000_0090
HDMIPHY 40h register	0440h	TMDS Data Amplitude Control	0x0000_0008
HDMIPHY 5ch register	045Ch	TMDS Clock Amplitude Control	0x0000_0086
HDMIPHY 74h register	0474h	PHY APB Mode Control register	0x0000_0000
HDMIPHY 78h register	0478h	PHY Test Mode Enable register	0x0000_0001
HDMIPHY 7Ch register	047Ch	An Indicator of APB setting state register	0x0000_0008
DisplayTop Register Summary			
HDMI_MUXCTRL	1004h	DISPLAYTOP HDMI MUX Control register	0x0000_0000
HDMI_syncctrl0	1014h	DISPLAYTOP HDMI sync Control register 0	0x0000_0000
HDMI_syncctrl1	1018h	DISPLAYTOP HDMI sync Control register 1	0x0000_0000
HDMI_syncctrl2	1018h	DISPLAYTOP HDMI sync Control register 2	0x0000_0000
HDMI_syncctrl3	1018h	DISPLAYTOP HDMI sync Control register 3	0x0000_0000

37.6.4.1.1 HDMI PHY

HDMI PHY's register has own mean. Following is for user reference.

37.6.4.1.1.1 HDMIPHY 4h register

- Base Address: 0xC010_0000
- Address = Base Address + 0x0404h, Reset Value = 0x0000_0091

Name	Bit	Type	Description	Reset Value
RSVD	[31:6]	R	Reserved	0x2
CLK_SEL	[5:4]	RW	Select the HDMI PHY reference clock Users must set both of TIEOFF's register and this Register. This register must be 0.	2'b01
RSVD	[3:0]	–	Reserved	4'b0001

37.6.4.1.1.2 HDMIPHY 24h register

- Base Address: 0xC010_0000
- Address = Base Address + 0x0424h, Reset Value = 0x0000_0028

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	0x0
ref_cko_sel	[7]	RW	0 = REF_OCS 1 = Internal Reference Clock	1'b0
RSVD	[6:0]	–	Reserved	7'b0101000

37.6.4.1.1.3 HDMIPHY 3ch register

- Base Address: 0xC010_0000
- Address = Base Address + 0x043Ch, Reset Value = 0x0000_0090

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
TX_AMP_LVL[0]	[7]	RW	TX_AMP_LVL[0] bit	1'b1
TX_RES[1:0]	[5:4]	RW	TMDS Data Source Termination Resistor Control 0 = Source Termination OFF 1 = 300 Ω 2 = 150 Ω 3 = 100 Ω	2'b01
RSVD	[3:0]	–	Reserved	–

37.6.4.1.1.4 HDMIPHY 40h register

- Base Address: 0xC010_0000
- Address = Base Address + 0x0440h, Reset Value = 0x0000_0008

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
TX_EMP_LVL[3:0]	[7:4]	RW	TMDS Data Pre-emphasis Control 0000 = 400mV diff (Min Value) 1111 = 750mV diff (Max Value)	4'b0
TX_AMP_LVL[4:1]	[3:0]	RW	TX_AMP_LVL[4:1] bit TMDS Data Amplitude Control. 1LSB corresponds to 50 mV diff amplitude level. 00000 = 400 mV diff (Min Value) 11111 = 1950 mV diff (Max Value)	4'b1000

37.6.4.1.1.5 HDMIPHY 5ch register

- Base Address: 0xC010_0000
- Address = Base Address + 0x045Ch, Reset Value = 0x0000_0086

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
TX_CLK_LVL[4:0]	[7:3]	RW	TMDS Clock Amplitude Control 1LSB corresponds to 50 mV diff amplitude level. 00000 = 400 mV diff (Min Value) 11111 = 1950 mV diff (Max Value)	5'b10000
RSVD	[2:0]	R	Reserved	3'b110

37.6.4.1.1.6 HDMIPHY 74h register

- Base Address: 0xC010_0000
- Address = Base Address + 0x0474h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
APB_PDEN	[7]	RW	If APB_PDEN = 1, power down of each building blocks of PHY can be controlled APB Reg74 bit[6:4], bit[2:0] 0 = Disable 1 = Enable	1'b0
PLL_PD	[6]	RW	0 = Normal Status 1 = Power Down Status PLL & Bias Block Power Down	1'b0
TX_CLKSER_PD	[5]	RW	Clock Serializer Power Down	1'b0
TX_CLKDRV_PD	[4]	RW	TMDS Clock Driver Power Down	1'b0
TX_DRV_PD	[2]	RW	TMDS Data Driver Power Down	1'b0
TX_SER_PD	[1]	RW	TMDS Data Serializer Power Down	1'b0
TX_CLK_PD	[0]	RW	TX Internal Clock Buffer/Divider Power Down	1'b0

37.6.4.1.1.7 HDMIPHY 78h register

- Base Address: 0xC010_0000
- Address = Base Address + 0x0478h, Reset Value = 0x0000_0001

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
TESTEN	[7]	RW	PHY Test Mode Enable 0 = Normal Operation Mode 1 = PHY Test Mode	1'b0
TEST	[6:0]	RW	PHY Test Mode Control Signal	7'b0000001

37.6.4.1.1.8 HDMIPHY 7Ch register

- Base Address: 0xC010_0000
- Address = Base Address + 0x047Ch, Reset Value = 0x0000_0008

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved	24'b0
MODE_SET_DONE	[7]	RW	An indicator of APB setting state. Refer to the Section 1.5.1 PHY Configuration Change Through APB	1'b1
RSVD	[6:0]	R	Reserved	7'b0

37.6.4.2 HDMI Application Sequences

Users must be set to the following sequence in order to user HDMI.

- HDMI PHY configuration
- I2S (or SPDIFTX) configuration for the source audio data
- DPC (or Resolution Converter) configuration for the source video data
- HDMI Link configuration
- HDMI Converter configuration

37.6.4.2.1 DisplayTop Register Summary

User use this register to select the RGB Video data between the Primary DPC and the Secondary DPC.

37.6.4.2.1.1 HDMI_MUXCTRL

- Base Address: 0xC010_0000
- Address = Base Address + 0x1004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HDMI_MUXENB	[31]	RW	MUX Enable 0 = MUX Disable 1 = MUX Enable	1'b0
RSVD	[30:2]	RW	Reserved	29'b0
HDMI_MUXSEL	[1:0]	RW	MUX Select 0 = Primary DPC 1 = Secondary DPC 2 – 3 = Reserved (Never use this value)	2'b0

37.6.4.2.1.2 HDMI_syncctrl0

- Base Address: 0xC010_0000
- Address = Base Address + 0x1014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HDMI_vclk_sel	[31]	RW	Must set this value to 0 0 = HDMI PHY's pixel clock used for HDMI Operation 1 = Never set this value	1'b0
RSVD	[30:16]	RW	Reserved	15'b0
HDMI_Vsyncstart	[15:0]	RW	Specifies the start line of i_v_sync for the HDMI Link. Refer *Table 37-1*	16'b0

37.6.4.2.1.3 HDMI_syncctrl1

- Base Address: 0xC010_0000
- Address = Base Address + 0x1018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	16'b0
HDMI_HActivestart	[15:0]	RW	Specifies the start position (h_line) of h_active for the HDMI Link. Refer *Table 37-1*	16'b0

37.6.4.2.1.4 HDMI_syncctrl2

- Base Address: 0xC010_0000
- Address = Base Address + 0x1018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	RW	Reserved	16'b0
HDMI_HActiveend	[15:0]	RW	Specifies the end position of h_active for the HDMI Link. Refer *Table 37-1*	16'b0

37.6.4.2.1.5 HDMI_syncctrl3

- Base Address: 0xC010_0000
- Address = Base Address + 0x1018h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HDMI_VSYNCHSend	[31:16]	RW	Specifies the end position of i_v_sync for the HDMI Link. Refer to *Table 37-1*	16'b0
HDMI_VSYNCHSStart	[15:0]	RW	Specifies the start position of i_v_sync for the HDMI Link. Refer *Table 37-1*	16'b0

38 MIPI

38.1 Overview

The S5P4418 has a MIPI-DSI master and a MIPI-CSI slave.

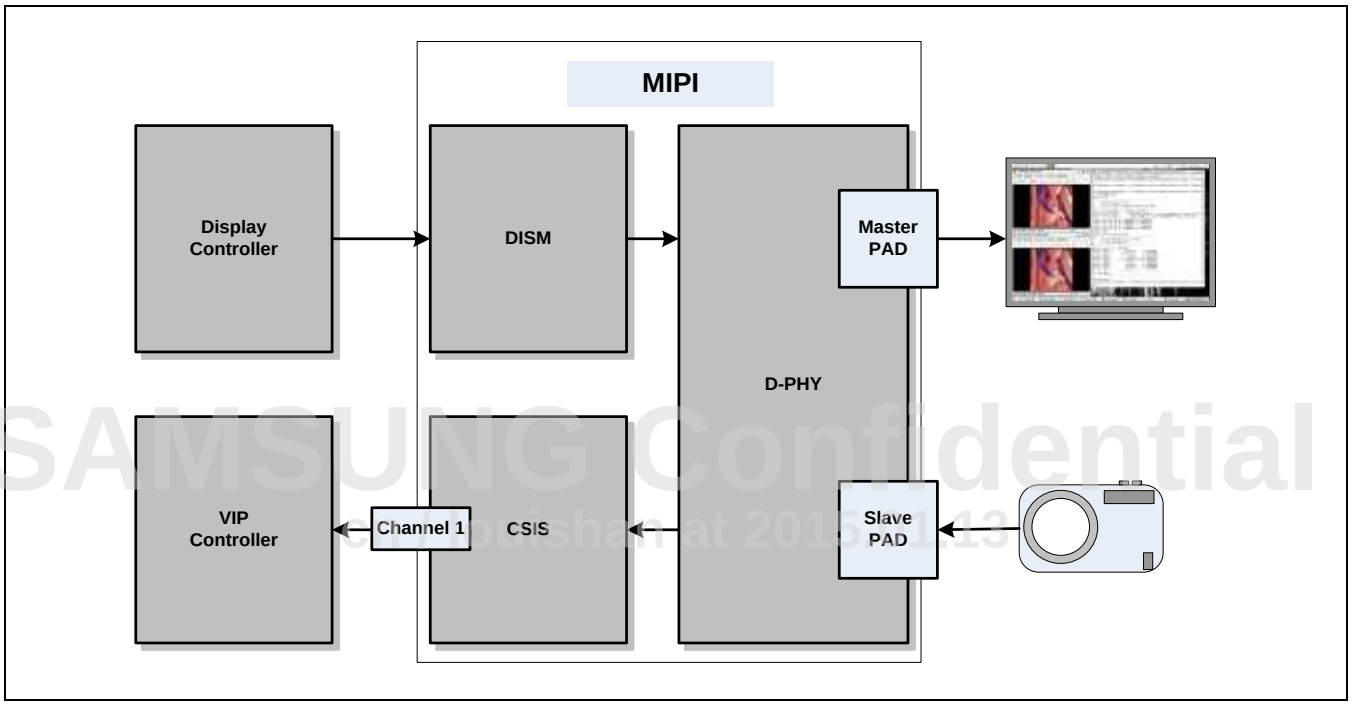


Figure 38-1 MIPI-DSI and MIPI-CSI

38.2 Features

DSI Master Features (DSIM)

The key features of MIPI DSIM include:

- MIPI DSI Standard Specification V1.01r11
- Maximum resolution ranges up to WUXGA (1920 × 1200)
- Supports 1, 2, 3, or 4 data lanes
- Supports pixel format: 16 bpp, 18 bpp packed, 18 bpp loosely packed (3 byte format), and 24 bpp
- Interfaces
  - Supports RGB Interface for Video Image Input from display controller
  - Supports PMS control interface for PLL to configure byte clock frequency
  - Supports Prescaler to generate escape clock from byte clock

CSI Slave Features (CSIS)

- Support YUV422 of 8 bits only. See VIP for more information.

D-PHY Features

The features of MIPI D-PHY are:

- The maximum high speed clock frequency of MIPI D-PHY core is 1 GHz.
- D-PHY spec v1.00 compatible.
- Synchronous link between Master (data source) and Slave (data sink).
- All lanes support high-speed transmission in forward direction.
- Bi-directional data transmission in Low-Power mode at the Master Data Lane 0 only.
- Use token passing to control the communication direction of the link.
- High-Speed mode for fast data traffics and Low-Power mode for controls and low speed data transmission.
- High-Speed mode: differential and terminated, 200 mV swing: 80 to 1000 Mbps
- Low-Power mode: single-ended and non-terminated, 1.2 V swing: 10 Mbps maximum
  (Use this mode for low-speed asynchronous data communications or controls)

38.3 DSIM

38.3.1 Block Diagram of MIPI DSI System

Total System Block Diagram

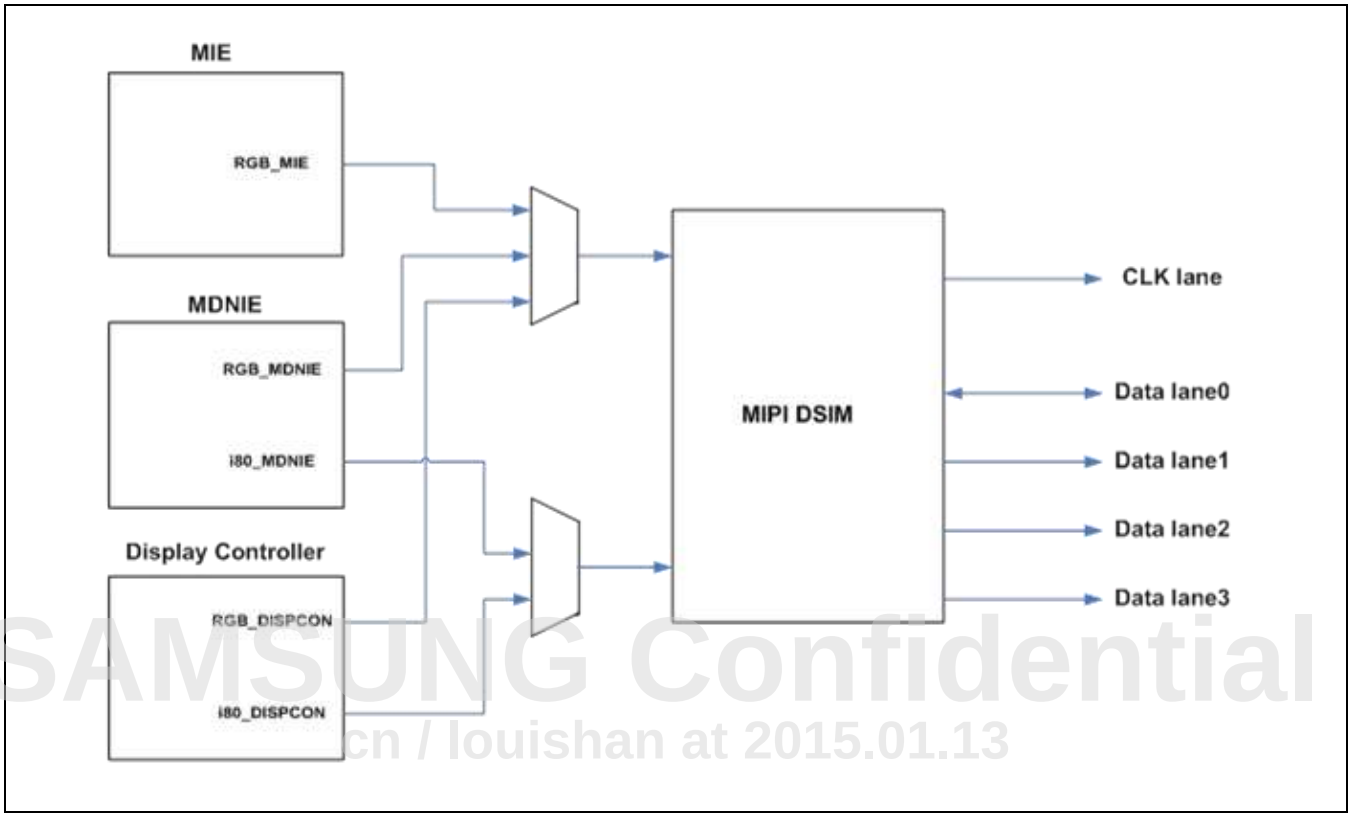


Figure 38-2 MIPI DSI System Block Diagram

- DSIM gets data from the three different IPs, namely, MIE, MDNIE, and Display Controller.
- You can select one of above data paths by setting MDNIE registers.

38.3.1.1 Internal Primary FIFOs

Table 38-1 describes configurable-sized primary FIFOs.

Table 38-1 Internal Primary FIFO List

Port	FIFO Type	Size	Description
Main display	Packet Header FIFO	3 byte × 128 depth	Specifies the packet header FIFO for main display.
	Payload FIFO	4 byte × 2048 depth	Specifies the payload FIFO for main display image.
Sub display for I80 INTERFACE image data	Packet Header FIFO	3 byte × 4 depth	Specifies the packet header FIFO for I80 INTERFACE sub display.
	Payload FIFO	4 byte × 512 depth	Specifies the payload FIFO for I80 INTERFACE sub display image.
Command for I80 INTERFACE command	Packet Header FIFO	3 byte × 16 depth	Specifies the packet header FIFO for I80 INTERFACE command packet.
	Payload FIFO	4 byte × 16 depth	Specifies the payload FIFO for I80 INTERFACE command long packet payload.
SFR for general packets	Packet Header FIFO	3 byte × 16 depth	Specifies the packet header FIFO for general packet.
	Payload FIFO	4 byte × 512 depth	Specifies the payload FIFO for general long packet.
RX FIFO	Packet header and Payload FIFO	4 byte × 64 depth	Specifies Rx FIFO for LPDR. This FIFO is common for packet header and payload.

38.3.1.2 Packet Header Arbitration

There are four-packet headers FIFOs for Tx, namely, main display, sub display, I80 INTERFACE command, and SFR FIFO. The main and sub display FIFO packet headers contain the image data, while the I80 INTERFACE command FIFO packet header contains the command packets. On the other hand, the SFR FIFO packet header contains command packets, sub display image data (in Video mode), and so on.

The packet header arbiter has a "Fixed priority" algorithm. Priority order is fixed as main display, sub display, I80 INTERFACE command, and SFR FIFO packet header.

In the Video mode, sub display and I80 INTERFACE command FIFO are not used. The SFR FIFO packet header checks if the main display FIFO is empty (no request) in not-active image region and then sends its request.

38.3.1.3 RxFIFO Structure

To read the packets received via low power data receiving mode, RxFIFO acts like an SFR. RxFIFO is an asynchronous FIFO with ByteClk and PCLK domains as input clock and output clock domains respectively. The Rx data is synchronized to RxClk. RXBUF has four Rx Byte buffers for aligning byte to word.

The packet headers of all the packets stored in RXFIFO are word-aligned, that is, the first byte of a packet is always stored in LSB. For example, if a long packet has 7 byte payload, the last byte is filled with dummy byte and the next packet is stored in the next word, as shown in *Figure 38-3*.

NOTE: CRC data is not stored in RXFIFO.

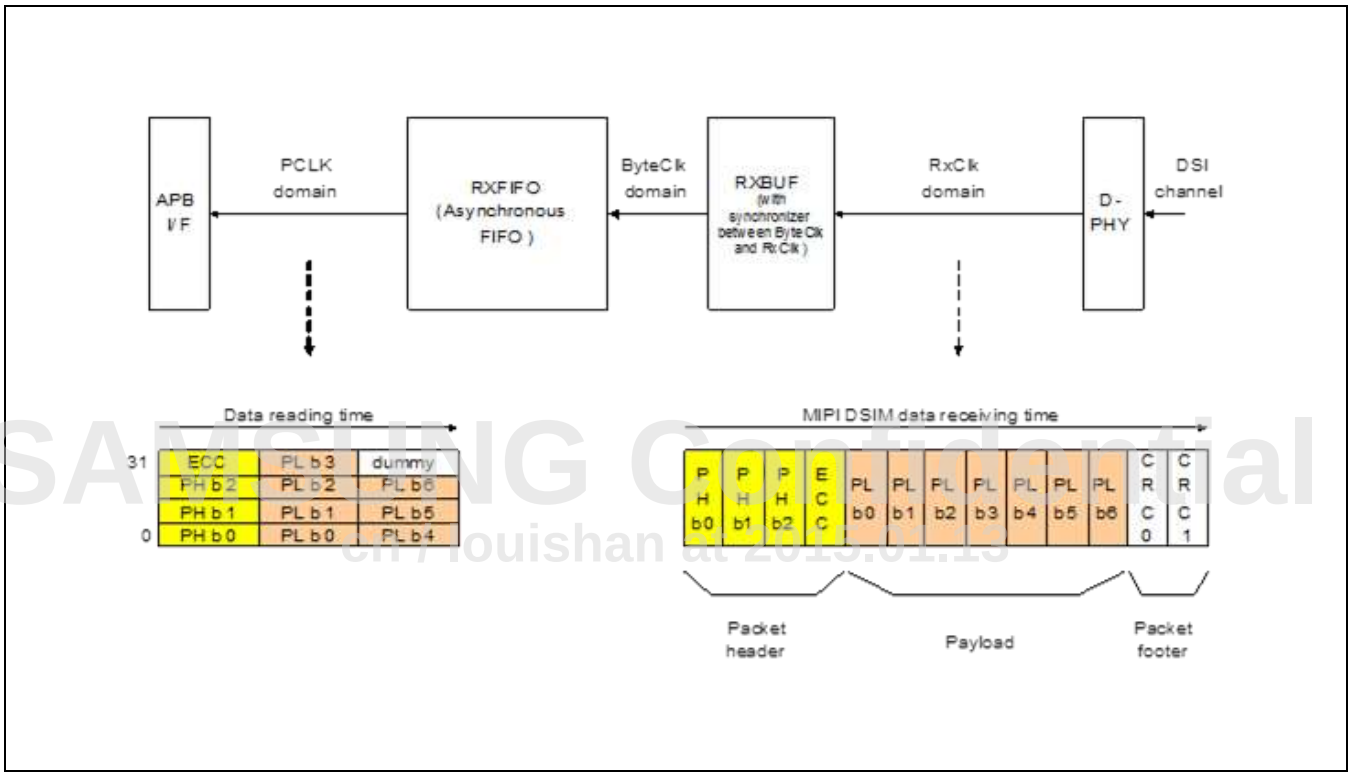


Figure 38-3 Rx Data Word Alignment

38.3.2 Interfaces and Protocol

Display Controller-to-DSI Conceptual Signal Converting Diagram in Video Mode

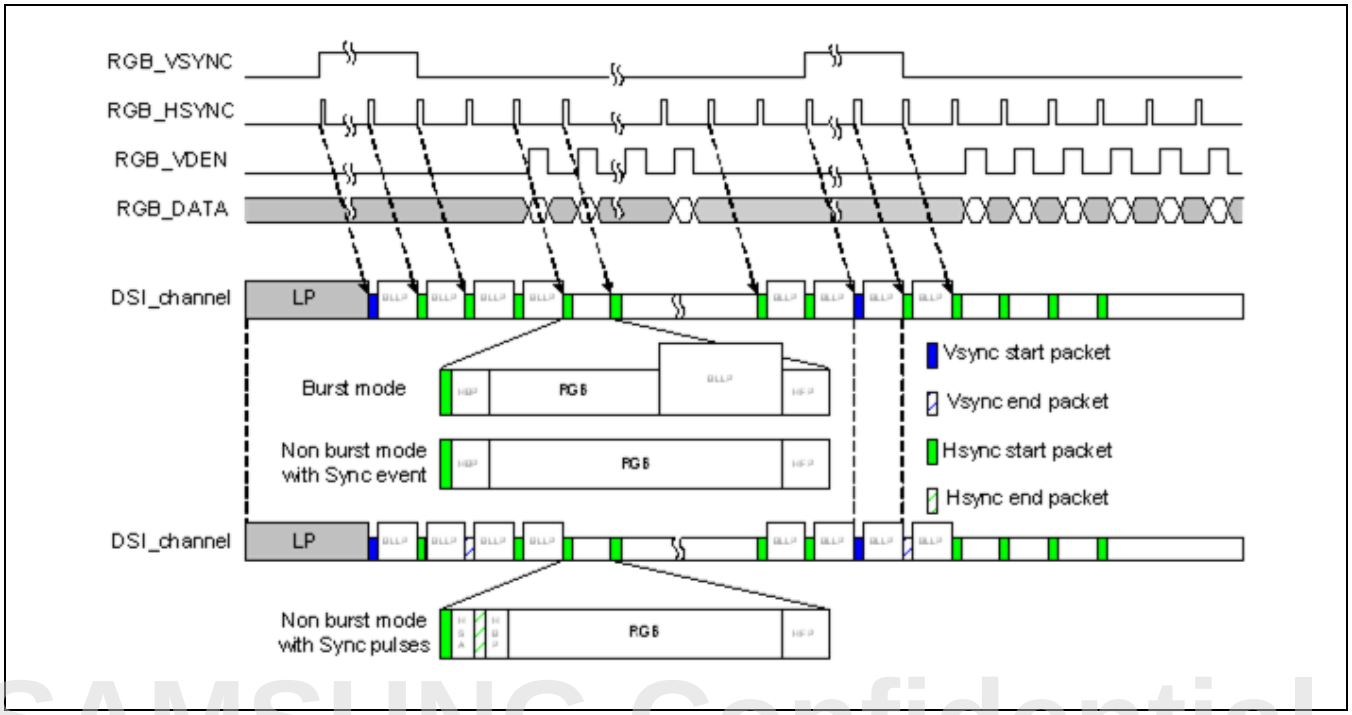


Figure 38-4 Signal Converting Diagram in Video Mode

38.3.2.1 Display Controller Interface

MIPI DSI Master has two-display controller interfaces, namely, RGB INTERFACE for main display and CPU INTERFACE (I80 INTERFACE) for main/ sub display. The Video mode uses RGB INTERFACE while the Command mode uses CPU INTERFACE.

The RGB image data is loaded on the data bus of RGB INTERFACE and I80 INTERFACE with the same order: RGB_VD[23:0] or SYS_VDOUT[23:0] is {R[7:0],G[7:0],B[7:0]}. Each byte aligns to the most significant bit. For instance, in the 12-bit mode, only three 4-bit values are valid as R, G, and B each, that is, data[23:20], data[15:12], and data[7:4]. The DSIM ignores rest of the bits.

38.3.2.2 RGB Interface

Vsync, Hsync, and VDEN are active high signals. Among the three signals, Vsync and Hsync are pulse types that spend several video clocks. RGB_VD[23:0] is {R[7:0],G[7:0],B[7:0]}. All sync signals are synchronized to the rising edge of RGB_VCLK. The display controller sends minimum one horizontal line length of Vsync pulse, V back porch, and V front porch. Hsync pulse width should be longer than 1-byte clock cycle.

38.3.2.3 HSA Mode

HSA mode specifies the Horizontal Sync Pulse area disable mode.

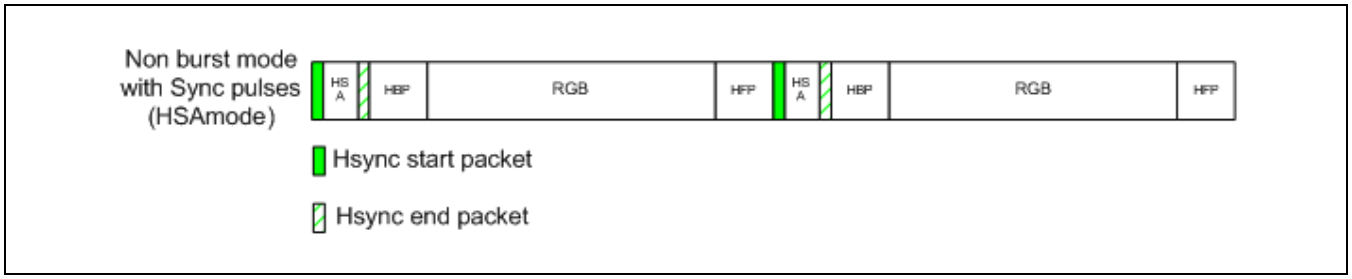


Figure 38-5 Block Timing Diagram of HSA Mode (HSA mode reset: DSIM_CONFIG[20] = 0)

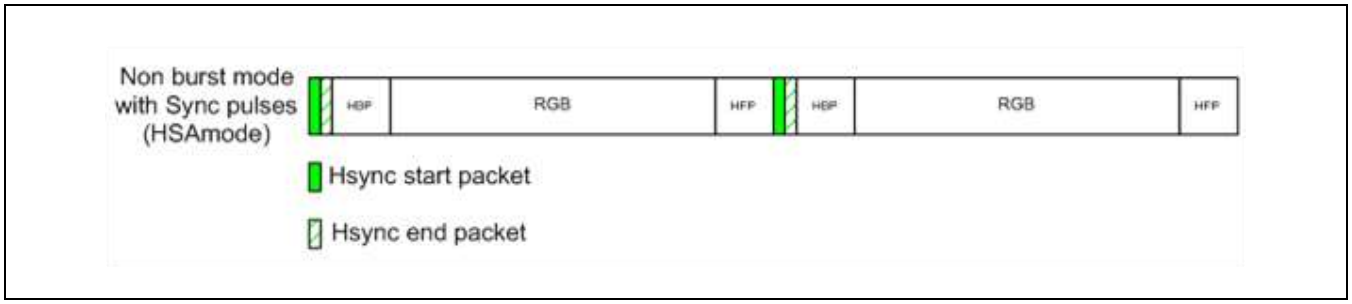


Figure 38-6 Block Timing Diagram of HSA Mode (HSA mode set: DSIM_CONFIG[20] = 1)

HBP mode HBP mode specifies the Horizontal Back Porch disable mode.

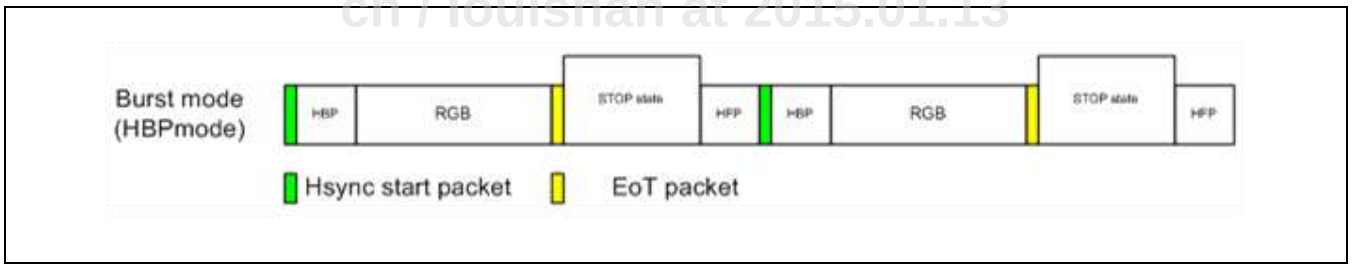


Figure 38-7 Block Timing Diagram of HBP Mode (HBP Mode Reset: DSIM_CONFIG[21] = 0)

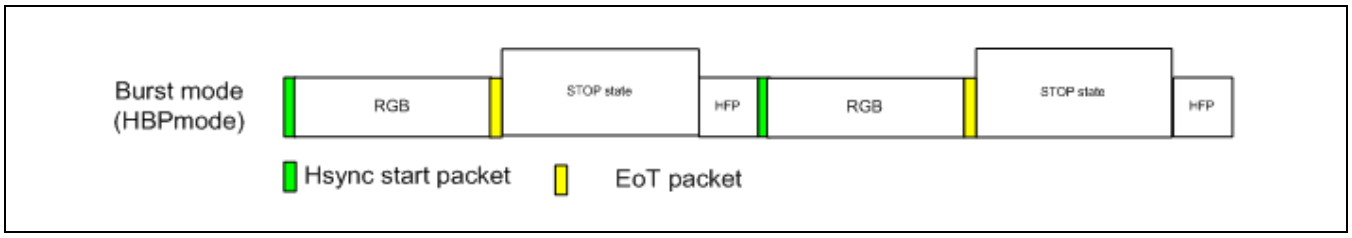


Figure 38-8 Block Timing Diagram of HBP Mode (HBP Mode Set: DSIM_CONFIG[21] = 1)

HFP mode HFP mode specifies the Horizontal Front Porch disable mode.

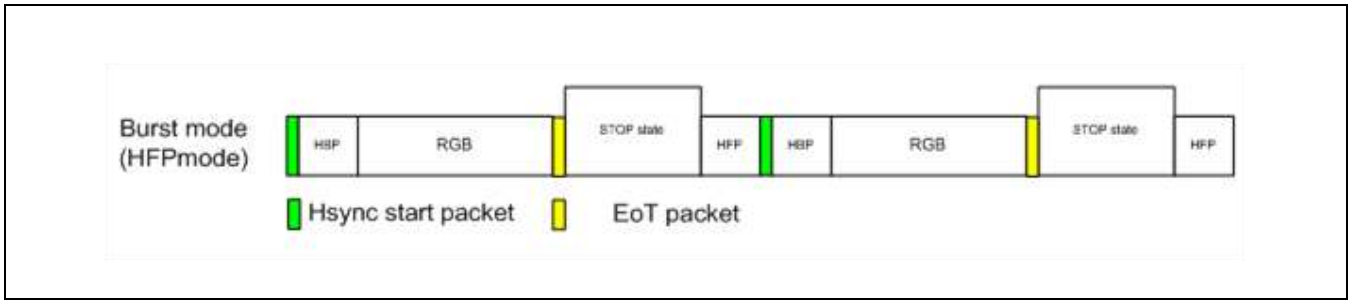


Figure 38-9 Block Timing Diagram of HFP Mode (HFP Mode Reset: DSIM_CONFIG[22] = 0)

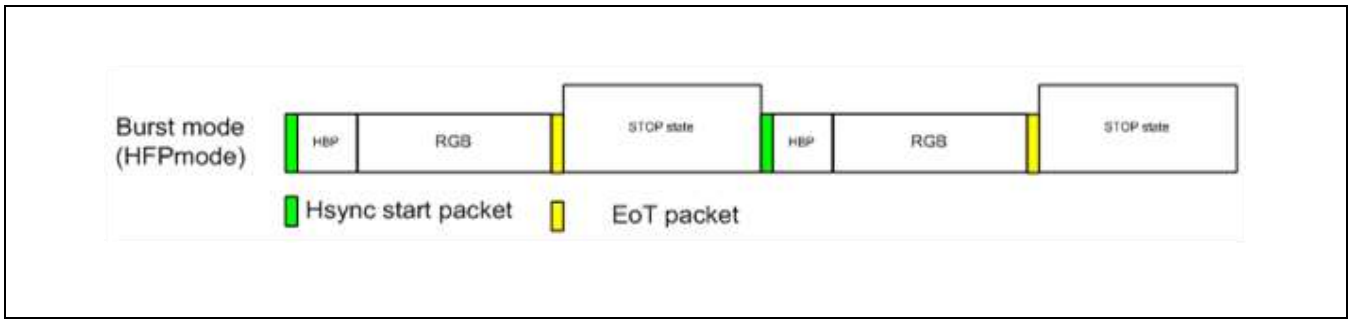


Figure 38-10 Block Timing Diagram of HFP Mode (HFP Mode Set: DSIM_CONFIG[22] = 1)

38.3.2.4 HSE Mode

HSE mode specifies the Horizontal Sync End Packet Enable mode in Vsync pulse or Vporch area.

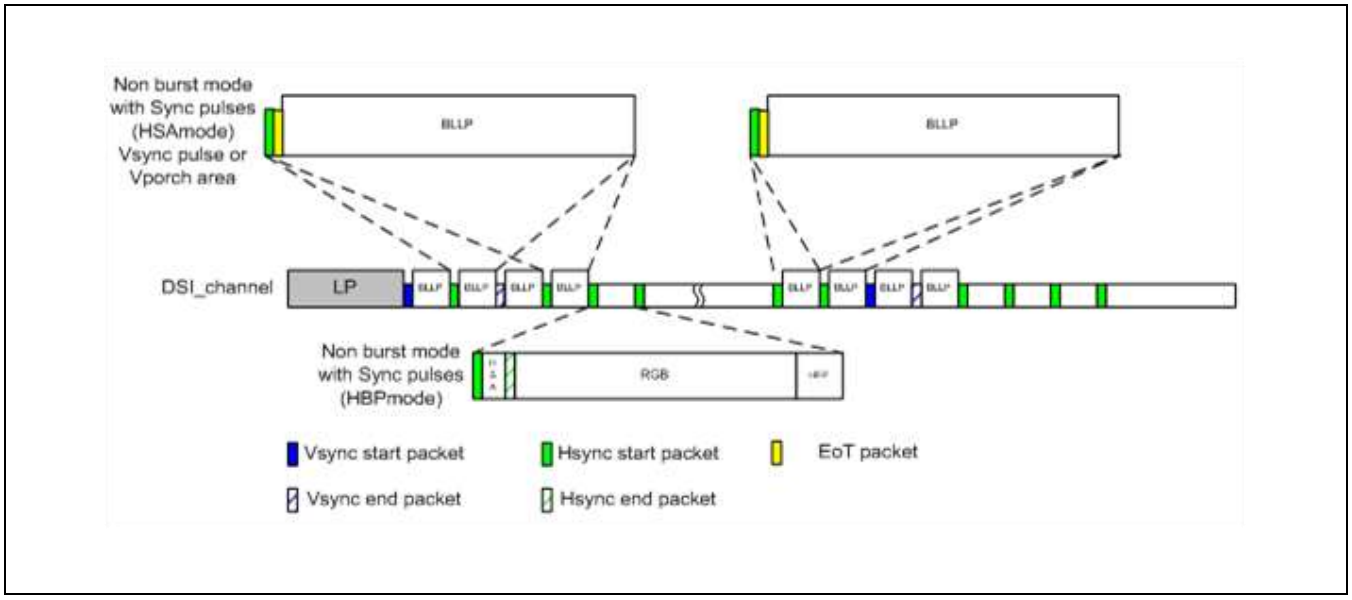


Figure 38-11 Block Timing Diagram of HSE Mode (HSE Mode Reset: DSIM_CONFIG[23] = 0)

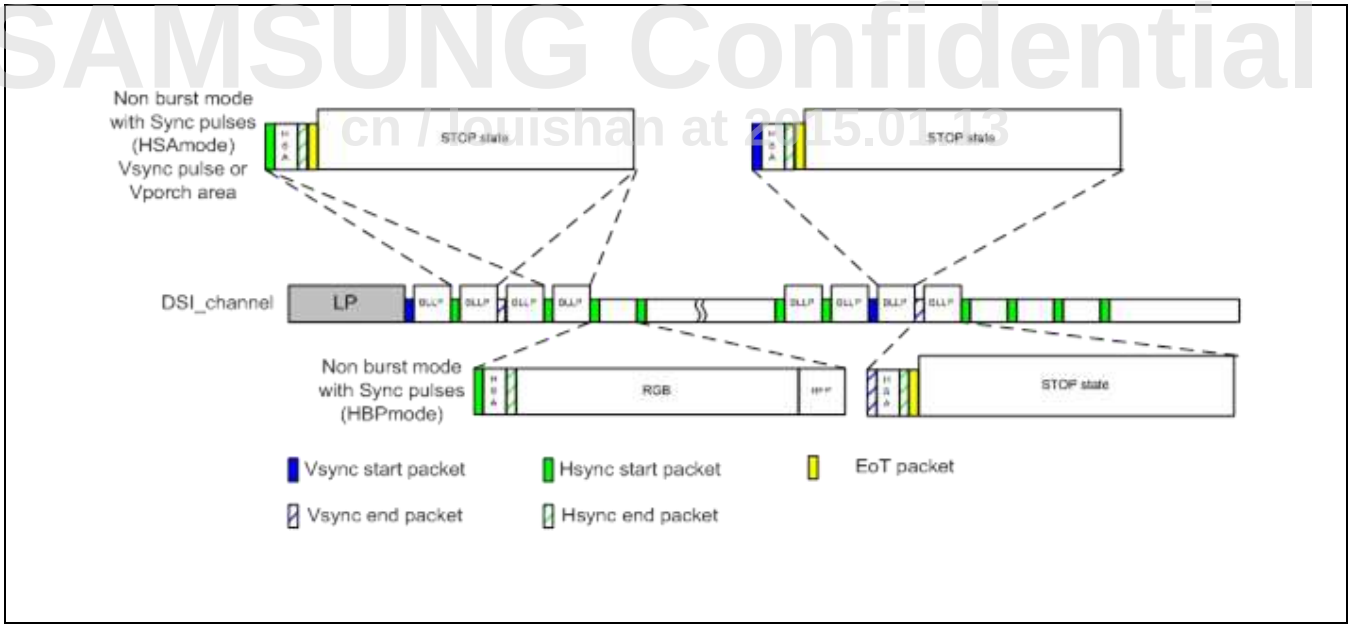


Figure 38-12 Block Timing Diagram of HSE Mode (HSE Mode Set: DSIM_CONFIG[23] = 1)

38.3.2.5 Transfer General Data in Video Mode

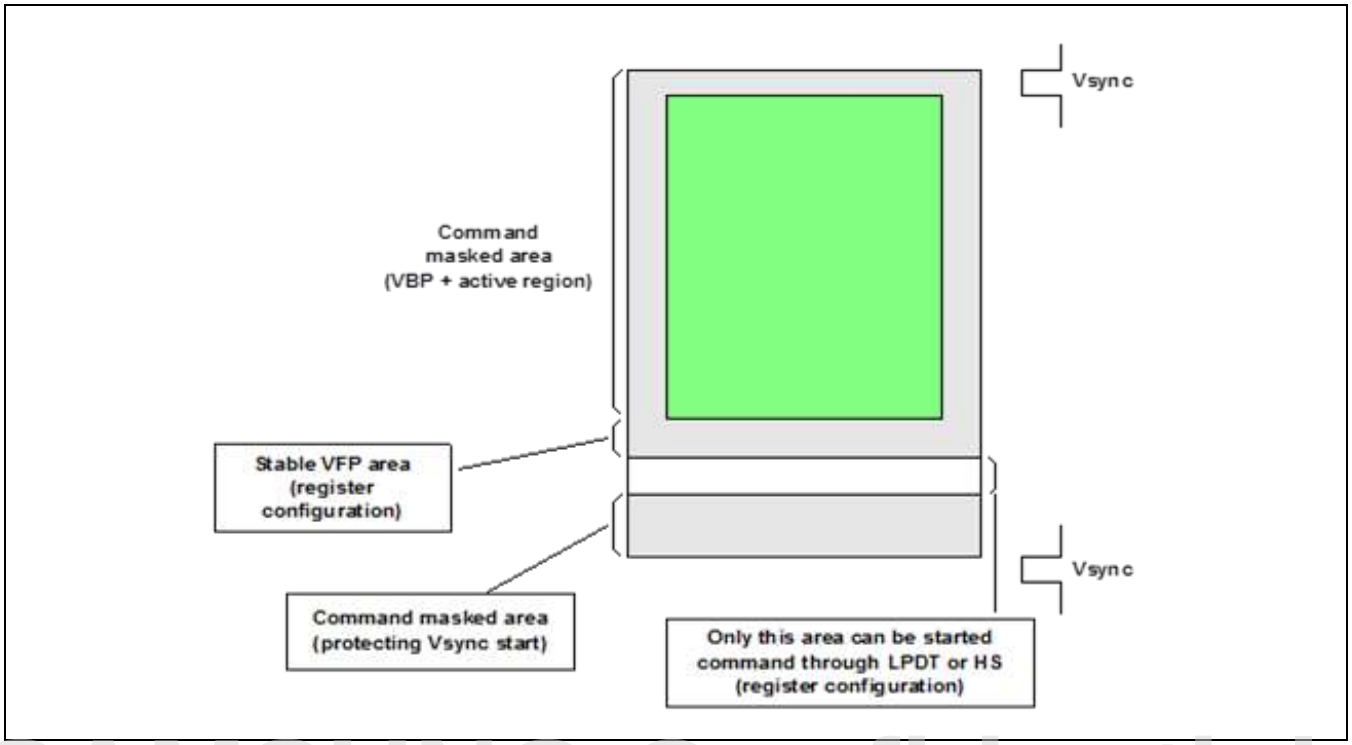


Figure 38-13 Stable VFP Area Before Command Transfer Allowing Area

38.3.2.6 MIPI DSIM Converts RGB Interface to Video Mode

Vsync and Hsync packets are extremely important to protect image in Video mode. MIPI DSIM allows several lines in VFP area to transfer general data transfer. As shown in *Figure 38-13*, the vertical front porch is divided into three areas, namely, stable VFP area, command allowed area, and command masked area.

The register configures stable VFP area. Configuration boundary is 11'h000 to 11'h7FFF in DSIM_MVPORCH.

The register also configures the command allowed area. Configuration boundary is 4'h0 to 4'hF in DSIM_MVPORCH. Only this area is allowed to start "command transfer" through HS mode or LPDT. In LPDT, data transferring takes a long time to complete (approximately hundreds of microseconds or more). In this time, Hsync packet does not arrive due to LPDT long packet. MIPI DSIM comprises of big size FIFO for lost Hsync packet. After LPDT, MIPI DSIM transfers these Hsync packets immediately through HS mode.

To protect Vsync, command masked area is masked area. This area is calculated using LPDT bandwidth. For example, if EscClk is 10 MHz, the maximum long packet payload size is 1KB and LPDT, LPDT transferring time is 824us (packet size: 1030 byte, LPDT maximum bandwidth: 10Mbps). If one line time is 20us, the line timing violation occurs in 42 lines. Therefore, command masked area is larger than 42 + a. This "a" is transferring time of the violated Hsync packets.

Display controller should be configured in such a way that VFP lines are sum of stable vfp, command allowed area, and command masked area.

Relation between Input Transactions and DSI Transactions

Table 38-2 Relation between Input Transactions and DSI Transactions

Input Interface	Input transaction	DSI Transaction
RGB	RGB transaction	Specifies the RGB Packet. 888, 666, 666 (loosely packed), and 565 should be specified via register configuration.
I80	I80 Image Transaction	Specifies the Data type, that is, "DCS Long Write packet". (DCS command is "memory write start/continue".)
I80	I80 Command Transaction	Specifies any DSI packet. Bytes in I80 transaction should be the same bytes in DSI packets.
SFR	Header and Payload FIFO access	Specifies any DSI Packets. Bytes in APB transaction should be the same bytes in DSI packets.

38.3.3 Configuration

Video Mode versus Command Mode

MIPI DSI Master Block supports two modes, namely, Video mode and Command mode.

38.3.4 PLL

To transmit Image data, MIPI DSI Master Block needs high frequency clock (80 MHz to 1 GHz) generated by PLL.

To configure PLL, MIPI DSI Master comprises of SFRs and corresponding interface signals. PLL is embedded in PHY module. You should use other PLL in SoC if it meets the timing specification.

38.3.5 Buffer

In MIPI DSI standard specification, DSI Master sends image stream in burst mode. The image stream transmits in high-speed and bit-clock frequency. This mode allows the device to stay in stop state longer to reduce power consumption. For this mode, MIPI DSI Master has a dual line buffer to store one complete line and send it faster at the next line time.

38.4 Register Description

38.4.1 Register Map Summary

- Base Address: 0xC00D_0100 (DSIMs)

Register	Offset	Description	Reset Value
DSIM			
DSIM_STATUS	0x0000	Specifies the status register.	0x0010_010F
DSIM_SWRST	0x0004	Specifies the software reset register.	0x0000_0000
DSIM_CLKCTRL	0x0008	Specifies the clock control register.	0x0000_FFFF
DSIM_TIMEOUT	0x000C	Specifies the time out register.	0x00FF_FFFF
DSIM_CONFIG	0x0010	Specifies the configuration register.	0x0200_0000
DSIM_ESCMODE	0x0014	Specifies the escape mode register.	0x0000_0000
DSIM_MDRESOL	0x0018	Specifies the main display image resolution register.	0x0300_0400
DSIM_MVPORCH	0x001C	Specifies the main display Vporch register.	0xF000_0000
DSIM_MHPORCH	0x0020	Specifies the main display Hporch register.	0x0000_0000
DSIM_MSYNC	0x0024	Specifies the main display Sync Area register.	0x0000_0000
DSIM_SDRESOL	0x0028	Specifies the sub display image resolution register.	0x0300_0400
DSIM_INTSRC	0x002C	Specifies the interrupt source register.	0x0000_0000
DSIM_INTMSK	0x0030	Specifies the interrupt mask register.	0xBB37_FFFF
DSIM_PKTHDR	0x0034	Specifies the packet header FIFO register.	0x0000_0000
DSIM_PAYLOAD	0x0038	Specifies the payload FIFO register.	0x0000_0000
DSIM_RXFIFO	0x003C	Specifies the read FIFO register.	0xXXXX_XXXX
DSIM_FIFOTHLD	0x0040	Specifies the FIFO threshold level register.	0x0000_01FF
DSIM_FIFOCTRL	0x0044	Specifies the FIFO status and control register.	0x0155_551F
DSIM_MEMACCHR	0x0048	Specifies the FIFO memory AC characteristic register.	0x0000_4040
DSIM_PLLCTRL	0x004C	Specifies the PLL control register.	0x0000_0000
DSIM_PLLCTRL1	0x0050	Specifies the PLL control register 1.	0x0000_0000
DSIM_PLLCTRL2	0x0054	Specifies the PLL control register 2.	0x0000_0000
DSIM_PLLTMR	0x0058	Specifies the PLL timer register.	0xFFFF_FFFF
DSIM_PHYCTRL	0x005C	Specifies the D-PHY control register	0x0000_0000
DSIM_PHYCTRL1	0x0060	Specifies the D-PHY control register 1	0x0000_0000
DSIM_PHYTIMING	0x0064	Specifies the D-PHY timing register	0x0000_0000
DSIM_PHYTIMING1	0x0068	Specifies the D-PHY timing register 1	0x0000_0000
DSIM_PHYTIMING2	0x006C	Specifies the D-PHY timing register 2	0x0000_0000
DSIM_VERSION	0x0070	Specifies the DSIM version register	0x8000_0001
DSIM_S3D_CTL	0x0080	Stereo Scope 3D Register	0x0000_0000
DSIM_P3D_CTL	0x0084	Proprietary 3D Register	0x0023_4D00
DSIM_MIC_CTL	0x0088	MIC Register	0x0023_4D00

Register	Offset	Description	Reset Value
DSIM_P3D_ON_MIC_OFF_HORIZONTAL	0x008C	Proprietary On MIC Off Horizontal	0x0000_0400
DSIM_P3D_OFF_MIC_ON_HORIZONTAL	0x0090	Proprietary Off MIC On Horizontal	0x0000_0400
DSIM_P3D_ON_MIC_ON_HORIZONTAL	0x0094	Proprietary On MIC On Horizontal Register	0x0000_0400
DSIM_P3D_ON_MIC_OFF_HFP	0x0098	Proprietary On MIC Off HFP Register	0x0000_0000
DSIM_P3D_OFF_MIC_ON_HFP	0x009C	Proprietary Off MIC On HFP Register	0x0000_0000
DSIM_P3D_ON_MIC_ON_HFP	0x00A0	Proprietary On MIC On HFP Register	0x0000_0000

38.4.1.1 DSIM_STATUS

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0000, Reset Value = 0x0010_010F

Name	Bit	Type	Description	Reset Value
PllStable	[31]	R	D-phy pll generates stable byteclk.	0
RSVD	[30:21]	–	Reserved	0
SwRstRls	[20]	R	Specifies the software reset status. 0 = Reset state 1 = Release state	1
RSVD	[19:17]	–	Reserved	0
Direction	[16]	R	Specifies the data direction indicator. 0 = Forward direction 1 = Backward direction	0
RSVD	[15:11]	–	Reserved	0
TxReadyHsClk	[10]	R	Specifies the HS clock ready at clock lane. 0 = Not ready for transmitting HS data at clock lane 1 = Ready for transmitting HS data at clock lane	0
UlpsClk	[9]	R	Specifies the ULPS indicator at clock lane. 0 = No ULPS in clock lane 1 = ULSP in clock lane	0
StopstateClk	[8]	R	Specifies the stop state indicator at clock lane. 0 = No stop state in clock lane 1 = Stop state in clock lane	1
UlpsDat[3:0]	[7:4]	R	Specifies the ULPS indicator at data lanes. UlpsDat[0]: Data lane 0 UlpsDat[1]: Data lane 1 UlpsDat[2]: Data lane 2 UlpsDat[3]: Data lane 3 0 = No ULPS in each data lane 1 = ULPS in each data lane	0
StopstateDat[3:0]	[3:0]	R	Specifies the stop state indicator at data lane. StopstateDat[0]: Data lane 0 StopstateDat[1]: Data lane 1 StopstateDat[2]: Data lane 2 StopstateDat[3]: Data lane 3 0 = No stop state in each data lane 1 = Stop state in each data lane	0xF

This register reads and checks internal and interface status. It also checks FSM status, Line buffer status, current image line number, and so on.

38.4.1.2 DSIM_SWRST

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0004, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:17]	–	Reserved	–
FuncRst	[16]	RW	Specifies the software reset (High active). "Software reset" resets all FF in MIPI DSIM (except SFRs: STATUS, SWRST, CLKCTRL, TIMEOUT, CONFIG, ESCMODE*, MDRESOL, MDVPORCH, MHPORCH, MSYNC, INTMSK, SDRESOL, FIFOTHLD, FIFOCTRL**, MEMACCHR, PLLCTRL, PLLTMR, PHYACCHR, and VERINFORM). 0 = Standby 1 = Reset *: ForceStopstate, CmdLpdt, TxLpdt, : nInitRx, nInitSfr, nInitI80, nInitSub, nInitMD	0
RSVD	[15:1]	–	Reserved	–
SwRst	[0]	RW	Specifies the software reset (High active). "Software reset" resets all FF in MIPI DSIM (except some SFRs: STATUS, SWRST, CLKCTRL, PLLCTRL, PLLTMR, and PHYTUNE). 0 = Standby 1 = Reset	0

38.4.1.3 DSIM_CLKCTRL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0008, Reset Value = 0x0000_FFFF

Name	Bit	Type	Description	Reset Value
TxRequestHsClk	[31]	RW	Specifies the HS clock request for HS transfer at clock lane (Turn on HS clock)	0
RSVD	[30:29]	–	Reserved	–
EscClkEn	[28]	RW	Enables the escape clock generating prescaler. 0 = Disables 1 = Enables	0
PLLBypass	[27]	RW	Sets the PLLBypass signal connected to D-PHY module input for selecting clock source bit. 0 = PLL output 1 = External Serial clock This bit must be set to 0.	0
ByteClkSrc	[26:25]	RW	Selects byte clock source. (It must be 00.) 00 = D-PHY PLL (default). PLL_out clock is used to generate ByteClk by dividing 8.	0
ByteClkEn	[24]	RW	Enables byte clock. 0 = Disables 1 = Enables	0
LaneEscClkEn	[23:19]	RW	Enables escape clock for D-phy lane. LaneEscClkEn[0] = Clock lane LaneEscClkEn[1] = Data lane 0 LaneEscClkEn[2] = Data lane 1 LaneEscClkEn[3] = Data lane 2 LaneEscClkEn[4] = Data lane 3 0 = Disables 1 = Enables	0
RSVD	[18:16]	–	Reserved	–
EscPrescaler	[15:0]	RW	Specifies the escape clock prescaler value. The escape clock frequency range varies up to 20MHz. NOTE: The requirement for BTA is that the Host Escclk frequency should range between 66.7 to 150% of the peripheral escape clock frequency. EscClk = ByteClk / (EscPrescaler)	0xFFFF

38.4.1.4 DSIM_TIMEOUT

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x000C, Reset Value = 0x00FF_FFFF

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	–
BtaTout	[23:16]	RW	Specifies the timer for BTA. This register specifies time out from BTA request to change the direction with respect to Tx escape clock.	0xFF
LpdrTout	[15:0]	RW	Specifies the timer for LP Rx mode timeout. This register specifies time out on how long RxValid deasserts, after RxLpdt asserts with respect to Tx escape clock. RxValid specifies Rx data valid indicator. RxLpdt specifies an indicator that D-phy is under RxLpdt mode. RxValid and RxLpdt specifies signal from D-phy.	0xFFFF

38.4.1.5 DSIM_CONFIG

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0010, Reset Value = 0x0200_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:30]	–	Reserved	–
Mflush_VS	[29]	RW	Auto flush of MD FIFO using Vsync pulse. It needs that Main display FIFO should be flushed for deleting garbage data. 0 = Enable (default) 1 = Disable	0
EoT_r03	[28]	RW	Disables EoT packet in HS mode. 0 = Enables EoT packet generation for V1.01r11 1 = Disables EoT packet generation for V1.01r03	0
SyncInform	[27]	RW	Selects Sync Pulse or Event mode in Video mode. 0 = Event mode (non burst, burst) 1 = Pulse mode (non burst only) In command mode, this bit is ignored.	0
BurstMode	[26]	RW	Selects Burst mode in Video mode In Non-burst mode, RGB data area is filled with RGB data and Null packets, according to input bandwidth of RGB interface. In Burst mode, RGB data area is filled with RGB data only. 0 = Non-burst mode 1 = Burst mode In command mode, this bit is ignored.	0
VideoMode	[25]	RW	Specifies display configuration. 0 = Command mode 1 = Video mode	1
AutoMode	[24]	RW	Specifies auto vertical count mode. In Video mode, the vertical line transition uses line counter configured by VSA, VBP, and Vertical resolution. If this bit is set to "1", the line counter does not use VSA and VBP registers. 0 = Configuration mode 1 = Auto mode In command mode, this bit is ignored.	0
HseMode	[23]	RW	In Vsync pulse and Vporch area, MIPI DSI master transfers only Hsync start packet to MIPI DSI slave at MIPI DSI spec 1.1r02. This bit transfers Hsync end packet in Vsync pulse and Vporch area (optional). 0 = Disables transfer 1 = Enables transfer In command mode, this bit is ignored.	0
HfpMode	[22]	RW	Specifies HFP disable mode. If this bit set, DSI master ignores HFP area in Video mode.	0

Name	Bit	Type	Description	Reset Value
			0 = Enables 1 = Disables In command mode, this bit is ignored.	
HbpMode	[21]	RW	Specifies HBP disable mode. If this bit set, DSI master ignores HBP area in Video mode. 0 = Enables 1 = Disables In command mode, this bit is ignored.	0
HsaMode	[20]	RW	Specifies HSA disable mode. If this bit set, DSI master ignores HSA area in Video mode. 0 = Enables 1 = Disables In command mode, this bit is ignored.	0
MainVc	[19:18]	RW	Specifies virtual channel number for main display.	0
SubVc	[17:16]	RW	Specifies virtual channel number for sub display.	0
RSVD	[15]	–	Reserved	–
MainPixFormat	[14:12]	RW	Specifies pixel stream format for main display. 000 = 3 bpp (for Command mode only) 001 = 8 bpp (for Command mode only) 010 = 12 bpp (for Command mode only) 011 = 16 bpp (for Command mode only) 100 = 16-bit RGB (565) (for Video mode only) 101 = 18-bit RGB (666: packed pixel stream) (for Video mode only) 110 = 18-bit RGB (666: loosely packed pixel stream) for Common 111 = 24-bit RGB (888) for common	0
RSVD	[11]	–	Reserved	–
SubPixFormat	[10:8]	RW	Specifies pixel stream format for sub display. 000 = 3 bpp (for Command mode only) 001 = 8 bpp (for Command mode only) 010 = 12 bpp (for Command mode only) 011 = 16 bpp (for Command mode only) 100 = 16-bit RGB (565) (for Video mode only) 101 = 18-bit RGB (666: packed pixel stream) for Video mode only) 110 = 18-bit RGB (666: loosely packed pixel stream) for common) 111 = 24-bit RGB (888) (for Common)	0
RSVD	[7]	–	Reserved	–
NumOfDatLane	[6:5]	RW	Sets the data lane number. 00 = Data lane 0 (1 data lane) 01 = Data lane 0 to 1 (2 data lanes) 10 = Data lane 0 to 2 (3 data lanes) 11 = Data lane 0 to 3 (4 data lanes)	0

Name	Bit	Type	Description	Reset Value
LaneEn[4:0]	[4:0]	RW	Enables the lane. If Lane_EN is disabled, the lane ignores input and drives initial value through output port. 0 = Lane is off. 1 = Lane is on. + LaneEn[0] = Clock lane enabler + LaneEn[1] = Data lane 0 enabler + LaneEn[2] = Data lane 1 enabler + LaneEn[3] = Data lane 2 enabler + LaneEn[4] = Data lane 3 enabler	0

This register configures MIPI DSI master such as data lane number, input interface, porch area, frame rate, BTA, LPDT, ULPS, and so on.

38.4.1.6 DSIM_ESCMODE

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0014, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
STOPstate_Cnt	[31:21]	RW	After transmitting read packet or write "set_tear_on" command, BTA requests to D-phy automatically. This counter value specifies the interval value between transmitting read packet (or write "set_tear_on" command) and BTA request. 11'h000 = 2 EscClk 11'h001 = 2 EscClk + 1 EscClk ~ 11'h3FF = 2 EscClk + 1023 EscClk	0
ForceStopstate	[20]	RW	Forces Stop state for D-PHY.	0
RSVD	[19:17]	–	Reserved	–
ForceBta	[16]	RW	Forces Bus Turn Around. 1 = Sends the protocol layer request to D-PHY. MIPI DSI peripheral becomes master after BTA sequence. This bit clears automatically after receiving BTA acknowledge from MIPI DSI peripheral.	0
RSVD	[15:8]	–	Reserved	–
CmdLpdt	[7]	RW	Specifies LPDT transfers command in SFR FIFO. 0 = HS Mode 1 = LP Mode	0
TxLpdt	[6]	RW	Specifies data transmission in LP mode (all data transfer in LPDT). 0 = HS Mode 1 = LP Mode	0
RSVD	[5]	–	Reserved	–
TxTriggerRst	[4]	RW	Specifies remote reset trigger function. After trigger operation, these bits will be cleared automatically.	0
TxUlpsDat	[3]	RW	Specifies ULPS request for data lane. Manually clears after ULPS exit.	0
TxUlpsExit	[2]	RW	Specifies ULPS exit request for data lane. Manually clears after ULPS exit.	0
TxUlpsClk	[1]	RW	Specifies ULPS request for clock lane. Manually clears after ULPS exit.	0
TxUlpsClkExit	[0]	RW	Specifies ULPS exit request for clock lane. Manually clears after ULPS exit.	0

This register configures MIPI DSI master.

38.4.1.7 DSIM_MDRESOL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0018, Reset Value = 0x0300_0400

Name	Bit	Type	Description	Reset Value
MainStandby	[31]	RW	Specifies standby for receiving DISPCON output in Command mode after setting all configuration. 0 = Not ready 1 = Stand by Standby should be set after configuration (resolution, req type, pixel form, and so on) is set for command mode. In Video mode, if this bit value is 0, data is not transferred.	0
RSVD	[30:28]	–	Reserved	–
MainVResol[11:0]	[27:16]	RW	Specifies Vertical resolution (1 to 1024).	0x300
RSVD	[15:12]	–	Reserved	–
MainHResol[11:0]	[11:0]	RW	Specifies Horizontal resolution (1 to 2047).	0x400

38.4.1.8 DSIM_MVPORCH

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x001C, Reset Value = 0xF000_0000

Name	Bit	Type	Description	Reset Value
CmdAllow	[31:28]	RW	Specifies the number of horizontal lines, where command packet transmission is allowed after Stable VFP period.	0xF
RSVD	[27]	–	Reserved	–
StableVfp[10:0]	[26:16]	RW	Specifies the number of horizontal lines, where command packet transmission is not allowed after end of active region. NOTE: In Command mode, these bits are ignored.	0
RSVD	[15:11]	–	Reserved	–
MainVbp[10:0]	[10:0]	RW	Specifies vertical back porch width for Video mode (line count). In Command mode, these bits are ignored.	0

Transfers command packets after Stable VFP area. Display controller VFP lines should be set based on sum of these values: Stable VFP, command allowing area and command masked area. See the section for transferring general data in Video mode.

38.4.1.9 DSIM_MHPORCH

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0020, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MainHfp[15:0]	[31:16]	RW	Specifies the horizontal front porch width for Video mode. HFP is specified using blank packet. These bits specify the word counts for blank packet in HFP. In Command mode, these bits are ignored.	0
MainHbp[15:0]	[15:0]	RW	Specifies the horizontal back porch width for Video mode. HBP is specified using blank packet. These bits specify the word counts for blank packet in HBP. In Command mode, these bits are ignored.	0

38.4.1.10 DSIM_MSYNC

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0024, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MainVsa[9:0]	[31:22]	RW	Specifies the vertical sync pulse width for Video mode (Line count). In command mode, these bits are ignored.	0
RSVD	[21:16]	–	Reserved	–
MainHsa[15:0]	[15:0]	RW	Specifies the horizontal sync pulse width for Video mode. HSA is specified using blank packet. These bits specify word counts for blank packet in HSA. In command mode, these bits are ignored.	0

38.4.1.11 DSIM_SDRESOL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0028, Reset Value = 0x0300_0400

Name	Bit	Type	Description	Reset Value
SubStandby	[31]	RW	Specifies standby for receiving DISPCON output in Command mode after setting all configuration. 0 = Not ready 1 = Standby Standby should be set after configuration (resolution, req type, pixel form, and so on) is set for command mode. In Video mode, this bit is ignored.	0
RSVD	[30:27]	–	Reserved	–
SubVResol[10:0]	[26:16]	RW	Specifies the Vertical resolution (1 to 1024).	0x300
RSVD	[15:11]	–	Reserved	–
SubHResol[10:0]	[10:0]	RW	Specifies the Horizontal resolution (1 to 1024).	0x400

38.4.1.12 DSIM_INTSRC

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x002C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
PllStable	[31]	RW	Indicates that D-phy PLL is stable.	0
SwRstRelease	[30]	RW	Releases the software reset.	0
SFRPLFifoEmpty	[29]	RW	Specifies the SFR payload FIFO empty.	0
SFRPHFifoEmpty	[28]	RW	Specifies the SFR Packet Header FIFO empty	0
SyncOverride	[27]	RW	Indicates that other DSI command transfer have overridden sync timing.	0
RSVD	[26]	RW	Reserved	–
BusTurnOver	[25]	RW	Indicates when bus grant turns over from DSI slave to DSI master.	0
FrameDone	[24]	RW	Indicates when MIPI DSIM transfers the whole image frame. NOTE: If Hsync is not received during two line times, internal timer is timed out and this bit is flagged.	0
RSVD	[23:22]	RW	Reserved	–
LpdrTout	[21]	RW	Specifies the LP Rx timeout. See time out register (0x10).	0
TaTout	[20]	RW	Turns around Acknowledge Timeout. See time out register (0x10).	0
RSVD	[19]	–	Reserved	–
RxDatDone	[18]	RW	Completes receiving data.	0
RxTE	[17]	RW	Receives TE Rx trigger.	0
RxAck	[16]	RW	Receives ACK Rx trigger.	0
ErrRxECC	[15]	RW	Specifies the ECC multi bit error in LPDR.	0
ErrRxCRC	[14]	RW	Specifies the CRC error in LPDR.	0
ErrEsc3	[13]	RW	Specifies the escape mode entry error lane 3. For more information, refer to standard D-PHY specification.	0
ErrEsc2	[12]	RW	Specifies the escape mode entry error lane 2. For more information, refer to standard D-PHY specification.	0
ErrEsc1	[11]	RW	Specifies the escape mode entry error lane 1. For more information, refer to standard D-PHY specification.	0
ErrEsc0	[10]	RW	Specifies the escape mode entry error lane 0. For more information, refer to standard D-PHY specification.	0
ErrSync2	[9]	RW	Specifies the LPDT sync error lane 3. For more information, refer to standard D-PHY specification.	0
ErrSync2	[8]	RW	Specifies the LPDT Sync Error lane2. For more information, refer to standard D-PHY specification.	0
ErrSync1	[7]	RW	Specifies the LPDT Sync Error lane1. For more information, refer to standard D-PHY specification.	0

Name	Bit	Type	Description	Reset Value
ErrSync0	[6]	RW	Specifies the LPDT Sync Error lane0. For more information, refer to standard D-PHY specification.	0
ErrControl2	[5]	RW	Controls Error lane3. For more information, refer to standard D-PHY specification.	0
ErrControl2	[4]	RW	Controls Error lane2. For more information, refer to standard D-PHY specification.	0
ErrControl1	[3]	RW	Controls Error lane1. For more information, refer to standard D-PHY specification.	0
ErrControl0	[2]	RW	Controls Error lane0. For more information, refer to standard D-PHY specification.	0
ErrContentLP0	[1]	RW	Specifies the LP0 Contention Error (only lane0, because BTA occurs at lane0 only). For more information, refer to standard D-PHY specification.	0
ErrContentLP1	[0]	RW	Specifies the LP1 Contention Error (only lane0, because BTA occurs at lane0 only). For more information, refer to standard D-PHY specification.	0

This register identifies interrupt sources.

Internal block error, data transmit interrupt, inter-layer (D_PHY) error, etc.

The bits are set even if they are masked off by DSIM_INTMSK_REG.

Write "1" to clear the Interrupt.

38.4.1.13 DSIM_INTMSK

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0030, Reset Value = 0xBB37_FFFF

Name	Bit	Type	Description	Reset Value
MskPllStable	[31]	RW	Indicates that D-PHY PLL is stable.	1
MskSwRstRelease	[30]	RW	Releases software reset.	0
MskSFRPLFifoEmpty	[29]	RW	Empties SFR payload FIFO.	1
MskSFRPHFifoEmpty	[28]	RW	Interrupt Mask for SFR packet header FIFO empty	1
MskSyncOverride	[27]	RW	Indicates that other DSI command transfer have overridden sync timing.	1
RSVD	[26]	–	Reserved	–
MskBusTurnOver	[25]	RW	Indicates when bus grant turns over from DSI slave to DSI master.	1
MskFrameDone	[24]	RW	Indicates when MIPI DSIM transfers whole image frame.	1
RSVD	[23:22]	–	Reserved	–
MskLpdrTout	[21]	RW	Specifies LP Rx timeout. See time out register (0x10).	1
MskTaTout	[20]	RW	Specifies turnaround acknowledge timeout. See time out register (0x10)	1
RSVD	[19]	–	Reserved	–
MskRxDatDone	[18]	RW	Specifies completion of data receiving.	1
MskRxTE	[17]	RW	Specifies receipt of TE Rx trigger.	1
MskRxAck	[16]	RW	Specifies receipt of ACK Rx trigger.	1
MskRxECC	[15]	RW	Specifies ECC multi bit error in LPDR.	1
MskRxCRC	[14]	RW	Specifies CRC error in LPDR.	1
MskEsc3	[13]	RW	Specifies escape mode entry error in lane3. For more information, refer to standard D-PHY specification.	1
MskEsc2	[12]	RW	Specifies escape mode entry error in lane2. For more information, refer to standard D-PHY specification.	1
MskEsc1	[11]	RW	Specifies escape mode entry error in lane1. For more information, refer to standard D-PHY specification.	1
MskEsc0	[10]	RW	Specifies escape mode entry error in lane0. For more information, refer to standard D-PHY specification.	1
MskSync3	[9]	RW	Specifies LPDT sync error in lane3. For more information, refer to standard D-PHY specification.	1
MskSync2	[8]	RW	Specifies LPDT sync error in lane2. For more information, refer to standard D-PHY specification.	1
MskSync1	[7]	RW	Specifies LPDT sync error in lane1. For more information, refer to standard D-PHY specification.	1
MskSync0	[6]	RW	Specifies LPDT sync error in lane0. For more information, refer to standard D-PHY specification.	1

Name	Bit	Type	Description	Reset Value
MskControl3	[4]	RW	Controls error in lane3. For more information, refer to standard D-PHY specification.	1
MskControl2	[4]	RW	Controls error in lane2. For more information, refer to standard D-PHY specification.	1
MskControl1	[3]	RW	Controls error in lane1. For more information, refer to standard D-PHY specification.	1
MskControl0	[2]	RW	Controls error in lane0. For more information, refer to standard D-PHY specification.	1
MskContentLP0	[1]	RW	Specifies LP0 contention error. For more information, refer to standard D-PHY specification.	1
MskContentLP1	[0]	RW	Specifies LP1 contention error. For more information, refer to standard D-PHY specification.	1

This register masks interrupt sources.

38.4.1.14 DSIM_PKTHDR

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0034, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	–
PacketHeader	[23:0]	W	Writes the packet header of Tx packet. [7:0] = DI [15:8] = Dat0 (Word Count lower byte for long packet) [23:16] = Dat1 (Word Count upper byte for long packet)	0

This register is the FIFO for packet header to send DSI packets.

38.4.1.15 DSIM_PAYLOAD

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0038, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
Payload	[31:0]	W	Writes the Payload of Tx packet.	0

This register specifies the FIFO for payload to send DSI packets.

38.4.1.16 DSIM_RXFIFO

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x003C, Reset Value = 0xXXXX_XXXX

Name	Bit	Type	Description	Reset Value
RxDat	[31:0]	R	In the Rx mode, you can read Rx data through this register. Note that the CRC in packet is not stored in RxFIFO.	Unknown

This register is the gate of FIFO read

38.4.1.17 DSIM_FIFOTHLD

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0040, Reset Value = 0x0000_01FF

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	–	Reserved	0x0
WfullLevelSfr	[8:0]	RW	Almost full level of SFR payload FIFO	0x1FF

38.4.1.18 DSIM_FIFOCTRL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0044, Reset Value = 0x0155_551F

Name	Bit	Type	Description	Reset Value
RSVD	[31:26]	–	Reserved	0x0
FullRx	[25]	R	Rx FIFO full	0x0
EmptyRx	[24]	R	Rx FIFO empty	0x1
FullHSfr	[23]	R	SFR packet header FIFO full	0x0
EmptyHSfr	[22]	R	SFR packet header FIFO empty	0x1
FullLSfr	[21]	R	SFR payload FIFO full	0x0
EmptyLSfr	[20]	R	SFR payload FIFO empty	0x1
FullHI80	[19]	R	I80 packet header FIFO full	0x0
EmptyHI80	[18]	R	I80 packet header FIFO empty	0x1
FullLI80	[17]	R	I80 payload FIFO full	0x0
EmptyLI80	[16]	R	I80 payload FIFO empty	0x1
FullHSub	[15]	R	Sub display packet header FIFO full	0x0
EmptyHSub	[14]	R	Sub display packet header FIFO empty	0x1
FullLSub	[13]	R	Sub display payload FIFO full	0x0
EmptyLSub	[12]	R	Sub display payload FIFO empty	0x1
FullHMain	[11]	R	Main display packet header FIFO full	0x0
EmptyHMain	[10]	R	Main display packet header FIFO empty	0x1
FullLMain	[9]	R	Main display payload FIFO full	0x0
EmptyLMain	[8]	R	Main display payload FIFO empty	0x1
RSVD	[7:5]	–	Reserved	0x0
nInitRx	[4]	RW	MD FIFO read point initialize	0x1
nInitSfr	[3]	RW	SFR FIFO write point initialize	0x1
nInitI80	[2]	RW	I80 FIFO write point initialize	0x1
nInitSub	[1]	RW	SD FIFO write point initialize	0x1
nInitMain	[0]	RW	MD FIFO write point initialize	0x1

38.4.1.19 DSIM_MEMACCHR

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0048, Reset Value = 0x0000_4040

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	0x00
PGEN_SD	[15]	RW	Sub display FIFO memory power gating	0x0
RETN_SD	[14]	RW	Sub display FIFO memory Retention	0x1
EMAB_SD	[13:11]	RW	Sub display FIFO memory B port margin adjustment	0x0
EMAA_SD	[10:8]	RW	Sub display FIFO memory A port margin adjustment	0x0
PGEN_MD	[7]	RW	Main display FIFO memory power gating	0x0
RETN_MD	[6]	RW	Main display FIFO memory Retention	0x1
EMAB_MD	[5:3]	RW	Main display FIFO memory B port margin adjustment	0x0
EMAA_MD	[2:0]	RW	Main display FIFO memory A port margin adjustment	0x0

In current design, these memory port control was disabled. User can ignore the function of this register.

38.4.1.20 DSIM_PLLCTRL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x004C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:28]	–	Should be 0.	–
BandCtrl	[27:24]	RW	Each bandwidth control registers for Global Operation Timing. 0xF: 1 GHz 0xC: 750 MHz	
PllEn	[23]	RW	Enables PLL.	0
RSVD	[22:20]	–	Should be 0.	–
PMS[19:1]	[19:1]	RW	Specifies the PLL PMS value. 0x33E8: 1 GHz 0x43E8: 750 MHz	0
RSVD	[0]	–	Reserved	0

This register configures PLL control, D-PHY, clock range indication, and so on.

38.4.1.21 DSIM_PLLCTRL1

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0050, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
M_PLLCTL0	[31:0]	RW	It must be 0	0x0000_0000

This register configures D-PHY PLL control (M_PLLCTL[31:0])

38.4.1.22 DSIM_PLLCTRL2

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0054, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	–	Reserved	0x000000
M_PLLCTL1	[7:0]	RW	It must be 0	0x00

This register configures D-PHY PLL control (M_PLLCTL[39:32])

38.4.1.23 DSIM_PLLTMR

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0058, Reset Value = 0xFFFF_FFFF

Name	Bit	Type	Description	Reset Value
PllTimer	[31:0]	RW	Specifies the PLL Timer for stability of the generated clock (System clock cycle base). If the timer value goes to 0x00000000, the clock stable bit of status and interrupt register is set.	0xFFFFFFFF

38.4.1.24 DSIM_PHYCTRL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x005C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
B_DPHYCTL	[31:0]	RW	B_DPHYCTL[31:0] to D-PHY	0x0000_0000

D-PHY Master & Slave Analog block characteristics control registers (B_DPHYCTL).

38.4.1.25 DSIM_PHYCTRL1

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0060, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
M_DPHYCTL	[31:0]	RW	M_DPHYCTL[31:0] to D-PHY	0x0000_0000

D-PHY Master Analog block characteristics control registers (M_DPHYCTL).

38.4.1.26 DSIM_PHYTIMING

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0064, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	0x0000
M_TLPXCTL	[15:8]	RW	M_TLPXCTL[7:0] to D-PHY	0x00
M_THSEXITCTL	[7:0]	RW	M_THSEXITCTL[7:0] to D-PHY	0x00

D-PHY Master global operating timing register.

38.4.1.27 DSIM_PHYTIMING1

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0068, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
M_TCLKPRPRCTL	[31:24]	RW	M_TCLKPRPRCTL[7:0] to D-PHY	0x00
M_TCLKZEROCTL	[23:16]	RW	M_TCLKZEROCTL[7:0] to D-PHY	0x00
M_TCLKPOSTCTL	[15:8]	RW	M_TCLKPOSTCTL[7:0] to D-PHY	0x00
M_TCLKTRAILCTL	[7:0]	RW	M_TCLKTRAILCTL[7:0] to D-PHY	0x00

D-PHY Master global operating timing register.

38.4.1.28 DSIM_PHYTIMING2

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x006C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	0x00
M_THSPRPRCTL	[23:16]	RW	M_THSPRPRCTL[7:0] to D-PHY	0x00
M_THSZEROCTL	[15:8]	RW	M_THSZEROCTL[7:0] to D-PHY	0x00
M_THSTRAILCTL	[7:0]	RW	M_THSTRAILCTL[7:0] to D-PHY	0x00

D-PHY Master global operating timing register.

38.4.1.29 DSIM_VERSION

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0070, Reset Value = 0x8000_0001

Name	Bit	Type	Description	Reset Value
Version	[31:0]	R	Specifies the DSIM version information	0x8000_0001

38.4.1.30 DSIM_S3D_CTL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0080, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	0x00000
3DPRESENT	[11]	RW	Stereo Scope 3D control payload is present	0
RSVD	[10:6]	–	Reserved	0x0
3DL/R	[5]	RW	Left / Right Order 0 = Data sent left eye first, right eye next. 1 = Data sent right eye first, left eye next.	0
3DVSYNC	[4]	RW	Second VSYNC Enabled between Left and Right Images 0 = No sync pulses between left and right data. 1 = Sync pulse (HSYNC, VSYNC, blanking) between left and right data.	0
3DFMT	[1:0]	RW	3D Image Format 00 = Line (alternating lines of left and right data). 01 = Frame (alternating frames of left and right data). 10 = Pixel (alternating pixels of left and right data). 11 = Reserved	0x0
3DMODE	[1:0]	RW	3D Mode On / Off, Display Orientation 00 = 3D Mode Off (2D Mode On). 01 = 3D Mode On, Portrait Orientation. 10 = 3D Mode On, Landscape Orientation. 11 = Reserved.	0

Data ID	Data ID(0x01, VSYNC Start), Fixed							
Data 0	reserved	reserved	reserved	reserved	3DPRESENT	reserved	reserved	reserved
Data 1	0	0	3DL/R	3DVSYNC	3DFMT[1:0]		3DMODE[1:0]	

38.4.1.31 DSIM_P3D_CTL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0084, Reset Value = 0x0023_4D00

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	0x00
Data_ID	[23:16]	RW	Data type for processor-sourced packet data type 0x23 is generic short write, 2 parameters	0x23
P3D_ID	[15:8]	RW	Proprietary 3D ID	0x4D
RSVD	[7:6]	–	Reserved	0x0
P3D_Mode	[5:4]	RW	Proprietary 3D mode 00 = Sub-pixel mode 01 = Side-by-Side mode 10 and 11 = Reserved	0x0
RSVD	[3:2]	–	Reserved	0x0
P3D_EN	[1]	RW	Proprietary 3D enable / disable If this bit is 0, the peripheral may ignore the Proprietary 3D Register.	0
P3D_On_Off	[0]	RW	Proprietary 3D On / Off If 3D On from FIMD, It can be change to 1. This bit is read only.	0

Data ID	Data ID(default : 0x23, Generic short write, 2parameters)						
Data 0	SEC_3D_CTRL(default : 0x4D)						
Data 1	reserved	reserved	proprietary 3d mode	reserved	reserved	Enable / Disable	On / Off

38.4.1.32 DSIM_MIC_CTL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0088, Reset Value = 0x0023_4D00

Name	Bit	Type	Description	Reset Value
RSVD	[31:24]	–	Reserved	0x00
Data_ID	[23:16]	RW	Data type for processor-sourced packet data type 0x23 is generic short write, 2 parameters	0x23
MIC_ID	[15:8]	RW	MIC ID	0x4D
RSVD	[7:2]	–	Reserved	0x00
MIC_EN	[1]	RW	MIC enable / disable If this bit is 0, the peripheral may ignore the MIC Register.	0
MIC_On_Off	[0]	RW	MIC On / Off If MIC On from FIMD, It can be change to 1. This bit is read only.	0

Data ID	Data ID(default : 0x23, Generic short write, 2parameters)							
Data 0	SEC_MIC_CTRL(default : 0x4F)							
Data 1	reserved	reserved	reserved	reserved	reserved	reserved	Enable / Disable	On / Off

38.4.1.33 DSIM_P3D_ON_MIC_OFF_HORIZONTAL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x008C, Reset Value = 0x0000_0400

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	RW	Reserved	0x00000
H_Size	[11:0]	RW	Horizontal size when Proprietary 3D On, MIC Off	0x400

38.4.1.34 DSIM_P3D_OFF_MIC_ON_HORIZONTAL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0090, Reset Value = 0x0000_0400

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	0x00000
H_Size	[11:0]	RW	Horizontal size when Proprietary 3D Off, MIC On	0x400

38.4.1.35 DSIM_P3D_ON_MIC_ON_HORIZONTAL

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0094, Reset Value = 0x0000_0400

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	0x00000
H_Size	[11:0]	RW	Horizontal size when Proprietary 3D On, MIC On	0x400

38.4.1.36 DSIM_P3D_ON_MIC_OFF_HFP

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x0098, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	0x0000
HFP_Size	[15:0]	RW	HFP size when Proprietary 3D On, MIC Off for Video mode. HFP is specified using blank packet. In Command mode, these bits are ignored.	0x0000

38.4.1.37 DSIM_P3D_OFF_MIC_ON_HFP

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x009C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	0x0000
HFP_Size	[15:0]	RW	HFP size when Proprietary 3D Off, MIC On for Video mode. HFP is specified using blank packet. In Command mode, these bits are ignored.	0x0000

38.4.1.38 DSIM_P3D_ON_MIC_ON_HFP

- Base Address: 0xC00D_0100 (DSIMs)
- Address = Base Address + 0x00A0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	–	Reserved	0x0000
HFP_Size	[15:0]	RW	HFP size when Proprietary 3D On, MIC On for Video mode. HFP is specified using blank packet. In Command mode, these bits are ignored.	0x0000

38.5 CSIS

38.5.1 Interfaces and Protocol

38.5.1.1 D-PHY layer FSM

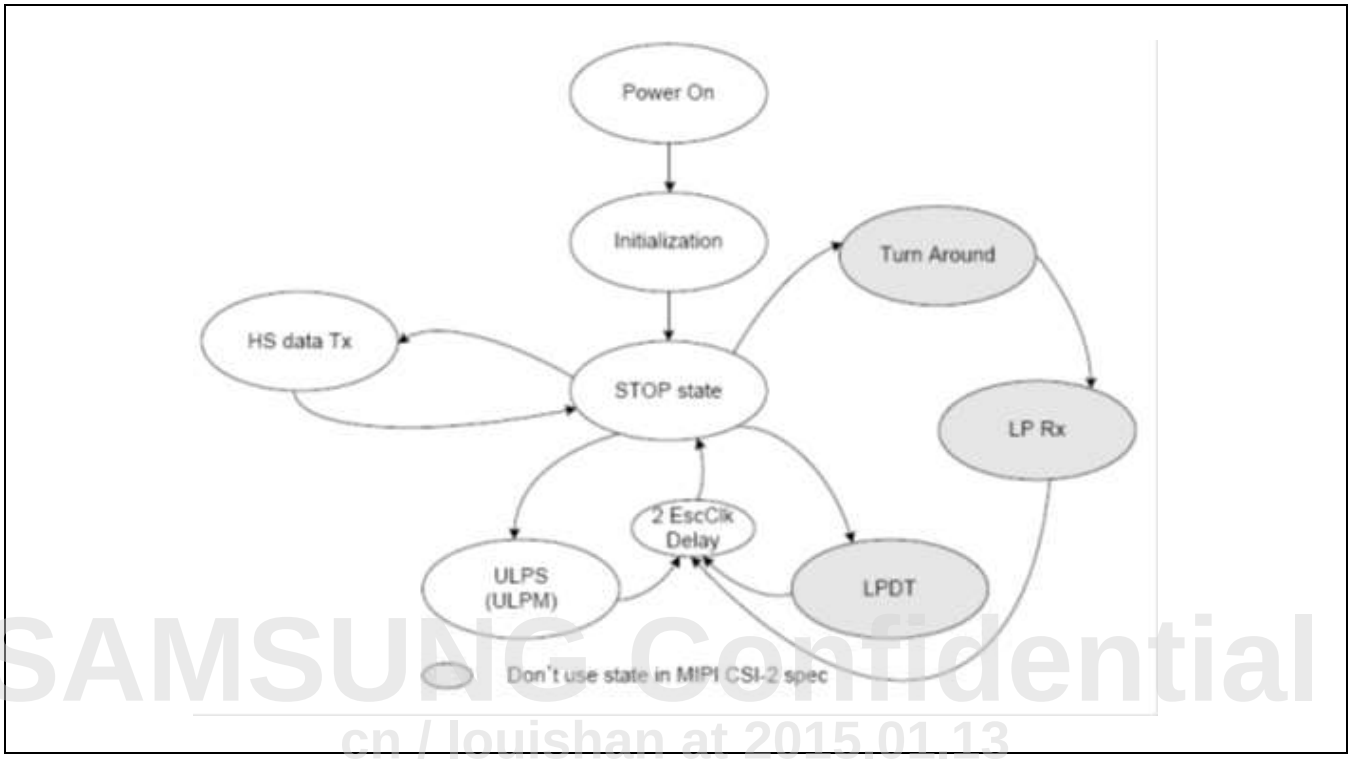


Figure 38-14 D-PHY Finite State Machine (Tx D-phy of Samsung)

MIPI CSIS V3.0 system supports HSDT (High Speed Data transfer) and ULPS (ULPM - Ultra-Low Power State or Mode) only. There is no trigger function, LPDT and BTA.

38.5.1.2 PPI Interface Timing & Protocol

MIPI CSIS V3.0 supports HSDT and ULPM.

38.5.1.2.1 High Speed Data Transfer

In *Figure 38-15*, the upper 5 signals are related with clock lane and the lower 6 signals are related with data lane. Dp and Dn of upper signals are D-phy channel of clock lane. RX_DDRCLKDIV2 is in PPI. BYTE_CLK is generated clock that is generated in link layer (MIPI CSIS V3.0) and divided by 2 from RX_DDRCLKDIV2. Dp and Dn of lower signals are D-phy channel of Data lane. Another signal of lower is PPI. STOP state (and STOPstateClk) indicates that differential channel state of D-phy is LP11 (the voltage level of Dp and Dn is 1.2V)

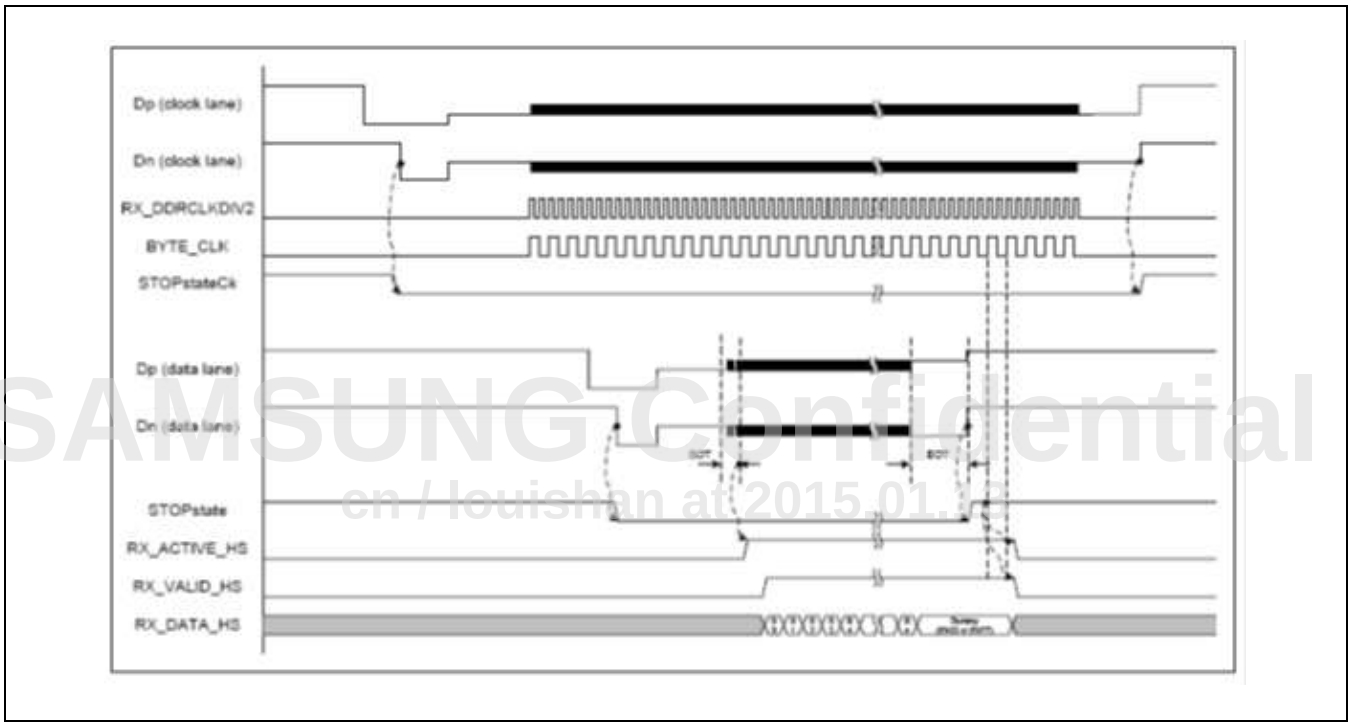


Figure 38-15 Timing Diagram of High Speed Data Transfer

38.5.1.2.2 Ultra-Low Power Mode

In *Figure 38-16*, UlpsActiveNot* and STOPstate* is in PPI. ULPS command in Data lane is only D-phy command that is generated Tx D-phy. Rx D-phy decodes this ULPS command and generates ULPS

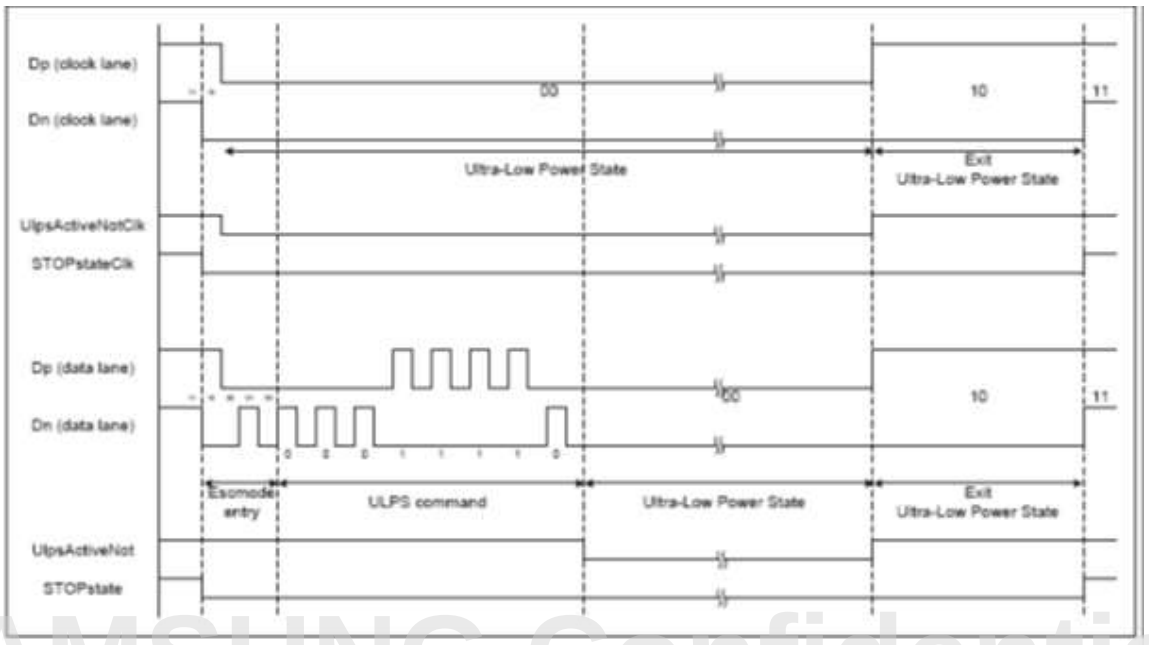


Figure 38-16 Timing Diagram of Ultra Low Power Mode

38.5.1.2.3 ISP (CAM I/F) Interface

MIPI CSIS V3.0 output signals are PIX_CLK, VVALID, HVALID, and DATA. PIX_CLK is output pixel clock what is generated from HCLK, BYTE_CLK or EXTCLK. VVALID is vertical sync signal. HVALID is horizontal sync signal. DATA is image data bus. DATA bus width is dependent on Image format. Maximum bus width is 24 bits because of RGB888. *Figure 38-17* describes the output protocol of MIPI CSIS. All signals are synchronized with the rising edge of PIX_CLK.

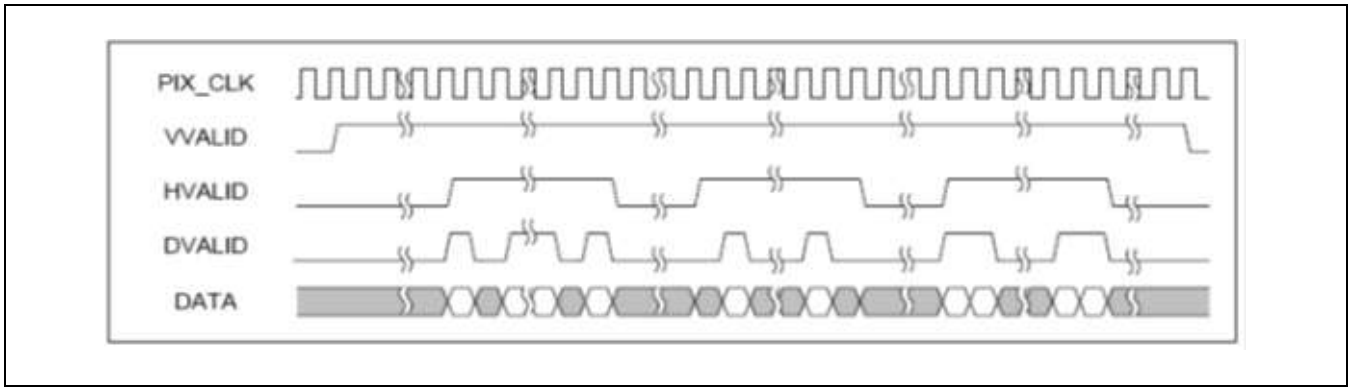


Figure 38-17 Output Protocol of ISP Wrapper of MIPI CSIS V3.0

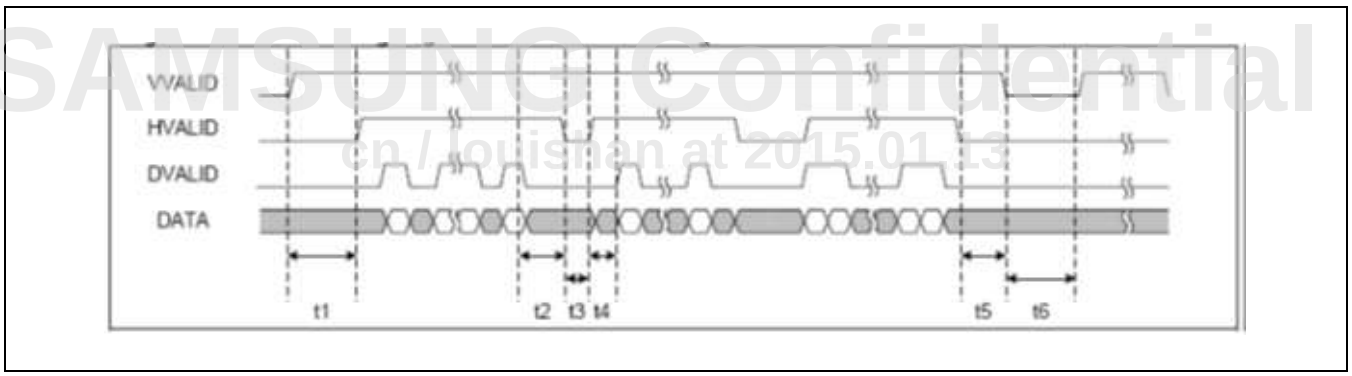


Figure 38-18 Timing Diagram of Output Protocol of ISP Wrapper

Table 38-3 Timing Table of Output Protocol of ISP Wrapper

	Description	Minimum Cycle of Pixel Clock	Maximum Cycle of Pixel Clock
t1	Interval between rising of VVALID and first rising of HVALID	Vsync_SIntv + 1 (1 to 64)	–
t2	Interval between last falling of DVALID and falling of HVALID	Hsync_LIntv + 2 (2 to 66)	–
t3	Interval between falling of HVALID and rising of next HVALID	1	–
t4	Interval between rising of HVALID and first rising of DVALID	0	–
t5	Interval between last falling of HVALID and falling of VVALID	Vsync_EIntv (0 to 4095)	–
t6	Interval between falling of VVALID and rising of next VVALID	1	–

Description of Output Protocol

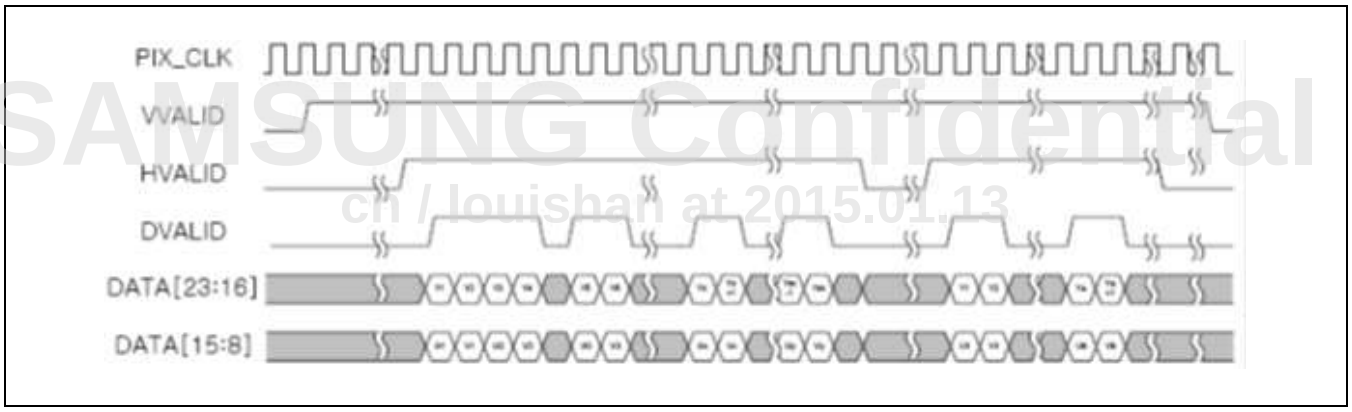


Figure 38-19 Waveform of ISP Interface (CAM I/F)

38.5.2 Configuration

38.5.2.1 Image Resolution

MIPI CSI Slave block needs the configuration of Image resolution to measure Hsync pulse length exactly and detect frame end.

- Vertical resolution register has 16 bits (16'h0001 to 16'hFFFF)
- Horizontal resolution register has 16 bits (16'h0001 to 16'hFFFF).

Image data format

S5P4418 supports YUV422 8-bit format only.

Table 38-4 Image Data Format

Data Type	Description
0x18	YUV420 8-bit
0x19	YUV420 10-bit
0x1A	Legacy YUV420 8-bit
0x1B	Reserved
0x1C	YUV420 8-bit CSPS (Chroma Shifted Pixel Sampling)
0x1D	YUV420 10-bit CSPS (Chroma Shifted Pixel Sampling)
0x1E	YUV422 8-bit
0x1F	YUV422 10-bit

38.5.3 Interrupt

MIPI CSIS V3.0 has many interrupts for checking status, indicating error case and receiving generic data.

- Odd_Before/Odd_After/Even_Before/Even_After

These interrupts are related with generic and embedded data.

Odd_Before and Odd_After interrupts are generated in odd frame. Even_Before and Even_After interrupts are generated in even frame. Odd_Before and Even_Before interrupts are generated when Generic Short packet or Embedded 8-bit based packet is received before image data (Vertical Back porch area)

38.5.4 Clock Specification

MIPI CSI may have 3 clock sources: RX_BYTE_CLK_HS0, I_PCLK, and I_WRAP_CLK.

I_PCLK	PCLK is system clock generated by general processor PLL.(APB clock)
RX_BYTE_CLK_HS0	This signal comes from data lane 0 of D-phy.
I_WRAP_CLK	I_WRAP_CLK is generated by clock generator. Refer to CSI clock in clock controller.

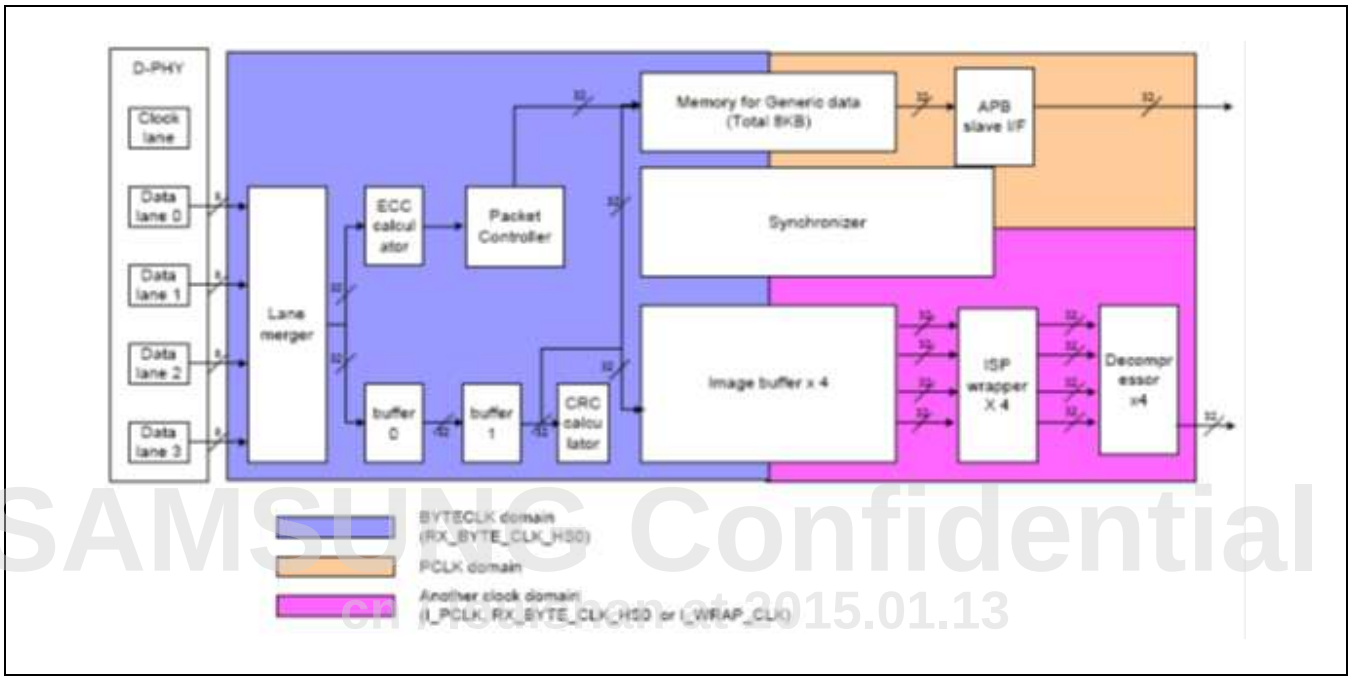


Figure 38-20 Block Diagram of Clock Domain

All clock domains are asynchronous each other. Pixel clock for transmitting image data to ISP is same with HCLK or Wrapper clock.

The relationship between input and output bandwidth is that the output bandwidth should be faster than input bandwidth. There is an equation of previous relationship:

(freq. of RX_BYTE_CLK_HS) (number of data lane) 8 bits ≤ (freq. of Pixel clock) × (bitwidth of image format)

38.5.5 Register Description

38.5.5.1 Register Map Summary

- Base Address: 0xC00D_0000

Register	Offset	Description	Reset Value
CSIS_CTRL	0x0000	Control register	0x0010_0000
CSIS_DPHYCTRL	0x0004	DPHY Analog Control register	0x0000_0000
CSIS_CONFIG_CH0	0x0008	Configuration register of CH0	0x0000_00FC
CSIS_DPHYSTS	0x000C	DPHY Status register	0x0000_00F1
CSIS_INTMSK	0x0010	Interrupt mask register	0x0000_0000
CSIS_INTSRC	0x0014	Interrupt source register Control	0x0000_0000
CSIS_CTRL2	0x0018	Control register about ch1 to 3	0x00E0_0000
CSIS_VERSION	0x001C	CSIS version register	0x8000_0000
CSIS_DPHYCTRL_0	0x0020	DPHY Analog Control register0	0x0000_0000
CSIS_DPHYCTRL_1	0x0024	DPHY Analog Control register1	0x0000_0000
RSVD	0x0028	Reserved	0x0000_0000
CSIS_RESOL_CH0	0x002C	Image Resolution register of CH0	0x8000_8000
RSVD	0x0030	Reserved	0x0000_0000
RSVD	0x0034	Reserved	0x8000_8000
SDW_CONFIG_CH0	0x0038	Shadow register of CH0 Configuration	0x0000_00FC
SDW_RESOL_CH0	0x003C	Shadow register of CH0 Resolution	0x8000_8000
CSIS_CONFIG_CH1	0x0040	Configuration register of CH1	0x0000_00FC
CSIS_RESOL_CH1	0x0044	Image Resolution register of CH1	0x8000_8000
SDW_CONFIG_CH1	0x0048	Shadow register of CH1 Configuration	0x0000_00FC
SDW_RESOL_CH1	0x004C	Shadow register of CH1 Resolution	0x8000_8000
CSIS_CONFIG_CH2	0x0050	Configuration register of CH2	0x0000_00FC
CSIS_RESOL_CH2	0x0054	Image Resolution register of CH2	0x8000_8000
SDW_CONFIG_CH2	0x0058	Shadow register of CH2 Configuration	0x0000_00FC
SDW_RESOL_CH2	0x005C	Shadow register of CH2 Resolution	0x8000_8000
CSIS_CONFIG_CH3	0x0060	Configuration register of CH3	0x0000_00FC
CSIS_RESOL_CH3	0x0064	Image Resolution register of CH3	0x8000_8000
SDW_CONFIG_CH3	0x0068	Shadow register of CH3 Configuration	0x0000_00FC
SDW_RESOL_CH3	0x006C	Shadow register of CH3 Resolution	0x8000_8000
DSIM	0x0100 to 0x01FF		
CSIS_NONIMG_ODD	0x2000 to 0x2FFF	Memory area for storing non-image data. Odd frame	0xXXXX_XXXX
CSIS_NONIMG_EVEN	0x3000 to 0x3FFF	Memory area for storing non-image data. Even frame	0xXXXX_XXXX

38.5.5.1.1 CSIS

38.5.5.1.1.1 CSIS_CTRL

- Base Address: 0xC005_0000
- Address = Base Address + 0000h, Reset Value = 0x0010_0000

Name	Bit	Type	Description	Reset Value
S_DpDn_Swap_Clk	[31]	RW	Swapping Dp and Dn channel of clock lane. 0 = Default 1 = Swapped	0
S_DpDn_Swap_Dat	[30]	RW	Swapping Dp and Dn channel of data lanes. 0 = Default 1 = Swapped	0
RSVD	[29:28]	–	read as zero, do not modify	0
Decomp_form	[27:26]	RW	Decompress format 00 = 10-bit compressed format 01 = Reserved for 12-bit compressed format Do not modify 1x = Reserved This register field related with Data format field in CSIS_CONFIG register	0
Decomp_predict	[25]	RW	Decompress prediction mode of CH0 0 = Simple prediction 1 = Advanced prediction	0
Decomp_en	[24]	RW	Decompress enable 0 = Disable (default) 1 = Enable When default value, input data of de-compressor is bypassed with all protocol signals (Vvalid, Hvalid, Dvalid and Bvalid)	0
Interleave_mode	[23:22]	RW	Select Interleave mode, VC(Virtual channel) and DT(Data type) 3 = VC and DT 2 = VC only 1 = DT only 0 = CH0 only, no data interleave	0
Double_cmpnt	[21]	RW	Double component per clock cycle in YUV422 formats, CH0 0 = single component per clock cycle (half pixel per clock cycle) 1 = double component per clock cycle (a pixel per clock cycle)	0
Parallel	[20]	RW	Output bus width of CH0 is 32 bits. 0 = Normal output 1 = 32-bit data alignment When this bit is set, the outer bus width of MIPI CSIS	1

Name	Bit	Type	Description	Reset Value
			V3.0 is 32.	
Update_Shadow	[19:16]	RW	Strobe of updating shadow registers 0 = default 1 = update the shadow registers. After configuration, User has to set this bit for updating shadow registers. This bit is cleared automatically after updating shadow registers. Bit [19] CH3 to Bit[16]CH0	0
RGB_SWAP	[15:12]	RW	Swapping RGB sequence 0 = MSB is R and LSB is B. 1 = MSB is B and LSB is R. (swapped)0 Bit [15] CH3 to Bit[12]CH0	0
WCLK_Src	[11:8]	RW	Wrapper clock source 0 = PCLK 1 = I_WRAP_CLK This bit determines source of Pixel clock which is clock of transferring image data to ISP or CAM I/F. When data format is "User defined packet", this bit is ignored. Bit [11] CH3 to Bit[8]CH0	0
RSVD	[7:5]	–	read as zero, do not modify	0
SW_RST	[4]	W	Software reset 0 = Ready 1 = Reset All writable registers in CSI2 go back to initial state. After this bit is active for 3 cycles, this bit will be de-asserted automatically NOTE: Almost MIPI CSI2 block uses "ByteClk" from D-phy. This "ByteClk" is not continuous clock. User has to assert software reset when Camera module is turned off.	0
NumOfDataLane	[3:2]	RW	Number of data lane 00 = 1 data lane 01 = 2 data lane 10 = 3 data lane 11 = 4 data lane	0
RSVD	[1]	–	read as zero, do not modify	0
CSI_EN	[0]	RW	MIPI CSI2 system enable 0 = Disable 1 = Enable	0

38.5.5.1.1.2 CSIS_DPHYCTRL

- Base Address: 0xC005_0000
- Address = Base Address + 0004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
HSSETTLE	[31:24]	RW	HS-RX settle time (THS-SETTLE) control register. You should pre-set it before HS-RX operation. Refer to the latest LN28LPP_MIPIDPHYCore1Gbps_Suppliement file for more information	8'b0
S_CLKSETTLECT	[23:22]	RW	TCLK-SETTLE parameter control register You should pre-set it before HS-RX operation. 2'b0x: 110ns to 280ns(v0.87 to v1.00) 2'b10: 150ns to 430ns(v0.83 to v0.86) 2'b11: 60ns to 140ns(v0.82)	2'b0
RSVD	[21:5]	–	Reserved. Do not modify.	17'b0
DPHY_ON	[4:0]	RW	D-PHY enable [4]: data lane 3 [3]: data lane 2 [2]: data lane 1 [1]: data lane 0 [0]: clock lane 0 = Disable 1 = Enable	

38.5.5.1.1.3 CSIS_CONFIG_CH0

- Base Address: 0xC005_0000
- Address = Base Address + 0008h, Reset Value = 0x0000_00FC

Name	Bit	Type	Description	Reset Value
Hsync_LIntv_CH0	[31:26]	RW	Interval between Hsync falling and Hsync rising (Line interval) 6'h00 to 6'h3F cycle of Pixel clock	0
Vsync_SIntv_CH0	[25:20]	RW	Interval between Vsync rising and first Hsync rises. 6'h00 to 6'h3F cycle of Pixel clock	0
Vsync_EIntv_CH0	[19:8]	RW	Interval between last Hsync falling and Vsync falling. 12'h000 to 12'hFFF cycle of Pixel clock	0
DataFormat_CH0	[7:2]	RW	Image Data Format YUV420 (8-bit): 0x18 YUV420 (10-bit): 0x19 YUV420 (8-bit legacy): 0x1A YUV420 (8-bit CSPS): 0x1C YUV420 (10-bit CSPS): 0x1D YUV422 (8-bit): 0x1E YUV422 (10-bit): 0x1F RGB565: 0x22 RGB666: 0x23 RGB888: 0x24 RAW6: 0x28 RAW7: 0x29 RAW8: 0x2A RAW10: 0x2B RAW12: 0x2C RAW14: 0x2D User defined 1: 0x30 User defined 2: 0x31 User defined 3: 0x32 User defined 4: 0x33	0x3F
Virtual_channel_CH0	[1:0]	RW	Set Virtual channel for data interleave. 00: VC = 0 01: VC = 1 10: VC = 2 11: VC = 3	0

38.5.5.1.1.4 CSIS_DPHYSTS

- Base Address: 0xC005_0000
- Address = Base Address + 000Ch, Reset Value = 0x0000_00F1

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	–	Reserved	0
UlpsDat	[11:8]	R	Data lane [3:0] is in ULPS [7]: Data lane 3 [6]: Data lane 2 [5]: Data lane 1 [4]: Data lane 0 0 = Not ULPS 1 = ULPS	0
StopStateDat	[7:4]	R	Data lane [3:0] is in Stop State [7]: Data lane 3 [6]: Data lane 2 [5]: Data lane 1 [4]: Data lane 0 0 = Not Stop state 1 = Stop state	0x1F
RSVD	[3:2]	–	Reserved	0
UlpsClk	[1]	R	Clock lane is in ULPS 0 = Not ULPS 1 = ULPS	0
StopStateClk	[0]	R	Clock lane is in Stop State 0 = Not Stop state 1 = Stop state	1

38.5.5.1.1.5 CSIS_INTMSK

- Base Address: 0xC005_0000
- Address = Base Address + 0010h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
MSK_EvenBefore	[31]	RW	Non Image data are received at Even frame and Before Image 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_EvenAfter	[30]	RW	Non Image data are received at Even frame and After Image 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_OddBefore	[29]	RW	Non Image data are received at Odd frame and Before Image 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_OddAfter	[28]	RW	Non Image data are received at Odd frame and After Image 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_FrameStart	[27:24]	RW	FS packet is received, [CH3,CH2,CH1,CH0] 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_FrameEnd	[23:20]	RW	FE packet is received, [CH3,CH2,CH1,CH0] 0 = Disable (masked) 1 = Enable (unmasked)	0
RSVD	[19:17]	–	read as zero, do not modify	0
MSK_ERR_SOT_HS	[16]	RW	Start of transmission error 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_ERR_LOST_FS	[15:12]	RW	Lost of Frame Start packet, [CH3,CH2,CH1,CH0] 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_ERR_LOST_FE	[11:8]	RW	Lost of Frame End packet, [CH3,CH2,CH1,CH0] 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_ERR_OVER	[7:4]	RW	Image FIFO overflow interrupt, [CH3,CH2,CH1,CH0] 0 = Disable (masked) 1 = Enable (unmasked)	0
RSVD	[3]	–	read as zero, do not modify	0
MSK_ERR_ECC	[2]	RW	ECC error 0 = Disable (masked) 1 = Enable (unmasked)	0

Name	Bit	Type	Description	Reset Value
MSK_ERR_CRC	[1]	RW	CRC error 0 = Disable (masked) 1 = Enable (unmasked)	0
MSK_ERR_ID	[0]	RW	Unknown ID error 0 = Disable (masked) 1 = Enable (unmasked)	0

38.5.5.1.1.6 CSIS_INTSRC

- Base Address: 0xC005_0000
- Address = Base Address + 0014h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
EvenBefore	[31]	RW	Non Image data are received at Even frame and Before Image	0
EvenAfter	[30]	RW	Non Image data are received at Even frame and After Image	0
OddBefore	[29]	RW	Non Image data are received at Odd frame and Before Image	0
OddAfter	[28]	RW	Non Image data are received at Odd frame and After Image	0
FrameStart	[27:24]	RW	FS packet is received, [CH3,CH2,CH1,CH0]	0
FrameEnd	[23:20]	RW	FE packet is received, [CH3,CH2,CH1,CH0]	0
ERR_SOT_HS	[19:16]	RW	Start of transmission error, [CH3,CH2,CH1,CH0]	0
ERR_LOST_FS	[15:12]	RW	Indication of lost of Frame Start packet, [CH3,CH2,CH1,CH0]	0
ERR_LOST_FE	[11:8]	RW	Indication of lost of Frame End packet, [CH3,CH2,CH1,CH0]	0
ERR_OVER	[7:4]	RW	Overflow is caused in image FIFO. [CH3,CH2,CH1,CH0] Outer bandwidth has to be faster than imputer bandwidth. But image FIFO can be overflow because of users fault. There are 2 ways for preventing overflow. Tune output pixel clock faster than current. Tune input byte clock slowr than current. • First case: WCLK_Src in CSIS_CTRL register should be set 1, and then assign faster clock • Second case: user can set register in camera module through I2C channel. When this interrupt is generated, Turn camera off Assert software reset, if you didn.t assert software	0

Name	Bit	Type	Description	Reset Value
			reset, MIPI CSIS could not receive any more data. Tune the clock frequency and re-configure all related registers. MIPI CSIS module is ready for operating.	
RSVD	[3]	–	read as zero, do not modify	0
ERR_ECC	[2]	RW	ECC error	0
ERR_CRC	[1]	RW	CRC error	0
ERR_ID	[0]	RW	Unknown ID error	0

38.5.5.1.1.7 CSIS_CTRL2

- Base Address: 0xC005_0000
- Address = Base Address + 0018h, Reset Value = 0x00E0_0000

Name	Bit	Type	Description	Reset Value
Decomp_predict	[31:29]	RW	Decompress prediction mode of CH3 to CH1 0 = Simple prediction 1 = Advanced prediction Bit [31]: CH3, Bit [30]: CH2, Bit [29]: CH1	0
RSVD	[28]	–	read as zero, do not modify	0
Double_cmpnt	[27:25]	RW	Double component per clock cycle in YUV422 formats 0 = Single component per clock cycle (half pixel per clock cycle) 1 = Double component per clock cycle (a pixel per clock cycle) Bit [27]: CH3, Bit [26]: CH2, Bit [25]: CH1	0
RSVD	[24]	–	read as zero, do not modify	0
Parallel	[23:21]	RW	Output bus width of CH0 is 32 bits. 0 = Normal output 1 = 32-bit data alignment When this bit is set, the outer bus width of MIPI CSIS V3.0 is 32. Bit [23]: CH3, Bit [22]: CH2, Bit [21]: CH1	0x7
RSVD	[20:0]	–	read as zero, do not modify	0

38.5.5.1.1.8 CSIS_VERSION

- Base Address: 0xC005_0000
- Address = Base Address + 001Ch, Reset Value = 0x8000_0000

Name	Bit	Type	Description	Reset Value
CSIS_VERSION	[31:0]	R	CSIS version information	0x8000_0000

38.5.5.1.1.9 B_DphyCtrl

- Base Address: 0xC005_0000
- Address = Base Address + 0020h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
B_DphyCtrl	[31:0]	RW	D-PHY Slave analog block characteristics control register. Do not modify this.	0

38.5.5.1.1.10 S_DphyCtrl

- Base Address: 0xC005_0000
- Address = Base Address + 0024h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
S_DphyCtrl	[31:0]	RW	D-PHY Slave analog block characteristics control register. It must be 0.	0

38.5.5.1.1.11 CSIS_RESOL_CH0

- Base Address: 0xC005_0000
- Address = Base Address + 002Ch, Reset Value = 0x8000_8000

Name	Bit	Type	Description	Reset Value
HResol_CH0	[31:16]	RW	Horizontal Image resolution Input boundary of each image format YUV420 (8-bit): 0x0001 to 0xFFFF YUV420 (10-bit): 4n (n is 1, 2, 3,….) YUV420 (8-bit legacy): 0x0001 ~ 0xFFFF YUV420 (8-bit CSPS): 0x0001 ~ 0xFFFF YUV420 (10-bit CSPS): 4n (n is 1, 2, 3,….) YUV422 (8-bit): 0x0001 to 0xFFFF YUV422 (10-bit): 4n (n is 1, 2, 3,….) RGB565: 0x0001 to 0xFFFF RGB666: 4n (n is 1, 2, 3,….) RGB888: 0x0001 to 0xFFFF RAW8: 0x0001 to 0xFFFF RAW10: 4n (n is 1, 2, 3,….) RAW12: 2n (n is 1, 2, 3,….) RAW14: 4n (n is 1, 2, 3,….)	0x8000
VResol_CH0	[15:0]	RW	Vertical Image resolution Input boundary: 0x0001 to 0xFFFF	0x8000

38.5.5.1.1.12 SDW_CONFIG_CH0

- Base Address: 0xC005_0000
- Address = Base Address + 0038h, Reset Value = 0x0000_00FC

Name	Bit	Type	Description	Reset Value
SDW_Hsync_LIntv_CH0	[31:26]	R	Current interval between Hsync falling and Hsync rising (Line interval)	0
SDW_Vsync_SIntv_CH0	[25:20]	R	Current interval between Vsync rising and first Hsync rises.	0
SDW_Vsync_EIntv_CH0	[19:8]	R	Current interval between last Hsync falling and Vsync falling.	0
SDW_DataFormat_CH0	[7:2]	R	Current image Data Format	0
SDW_Virtual_channel_CH0	[1:0]	R	Set Virtual channel for data interleave	0

38.5.5.1.1.13 SDW_RESOL_CH0

- Base Address: 0xC005_0000
- Address = Base Address + 003Ch, Reset Value = 0x8000_8000

Name	Bit	Type	Description	Reset Value
SDW_HResol_CH0	[31:16]	R	Current Horizontal Image resolution	0x8000
SDW_VResol_CH0	[15:0]	R	Current Vertical Image resolution	0x8000

Channel 1 registers (CSIS_CONFIG_CH1, CSIS_RESOL_CH1, SDW_CONFIG_CH1, SDW_RESOL_CH1)

Address: C00D_0040h, C00D_0044h, C00D_0048h, C00D_004Ch: WORD

Each register has same format with channel 0 register.

38.5.5.1.1.14 Non-Image Data Register

- Base Address : 0xC005_0000
- Address = Base Address + 0x2000 ~ 0x3FFC, Reset Value = Undefined

Name	Bit	Type	Description	Reset Value
NonImgData	[31:0]	R	Non Image Data memory • CSIS_NONIMG_ODD: Memory area for storing non-image data (0x2000 to 0x2FFC: Odd Frame) • CSIS_NONIMG_EVEN: Memory area for storing non-image data (0x3000 to 0x3FFC: Even Frame)	–

38.6 D-PHY

38.6.1 Architecture

38.6.1.1 PLL and Clock Lane Connection

The following figure illustrates the PLL and Clock Lane connection.

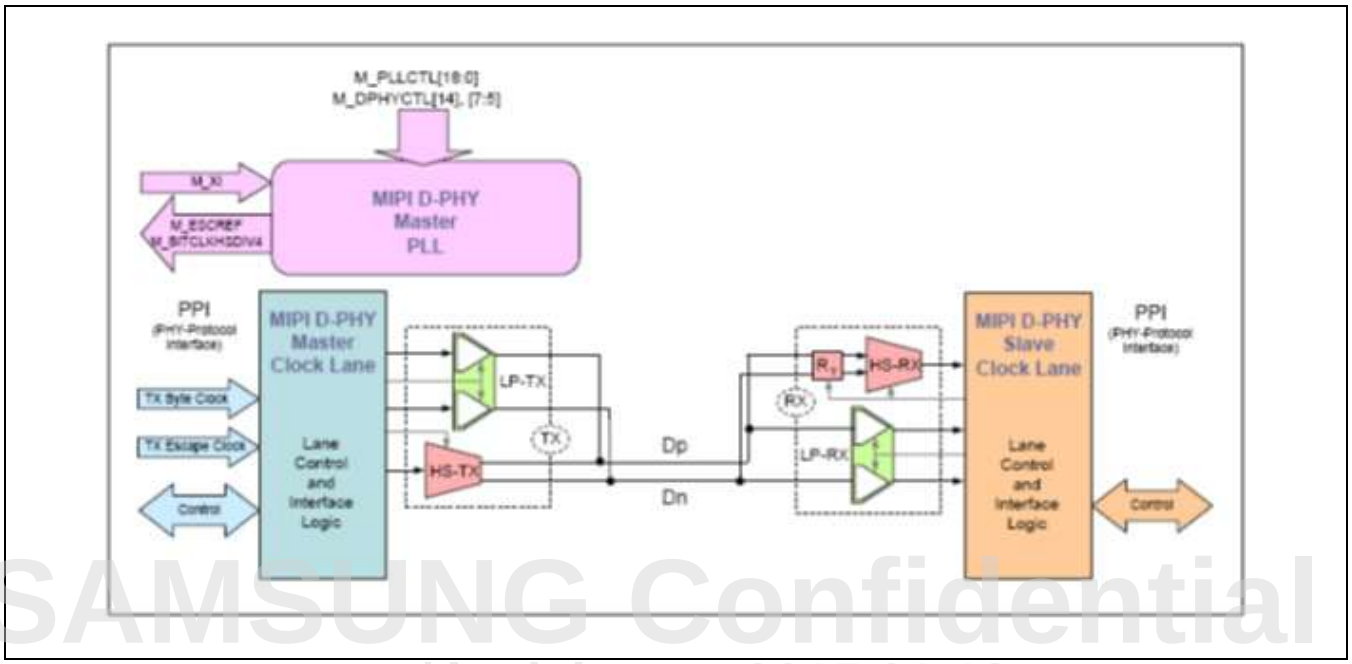


Figure 38-21 PLL and Clock Lane Connection

38.6.1.2 Data Lane Connection

The following figure illustrates the Data Lane connection.

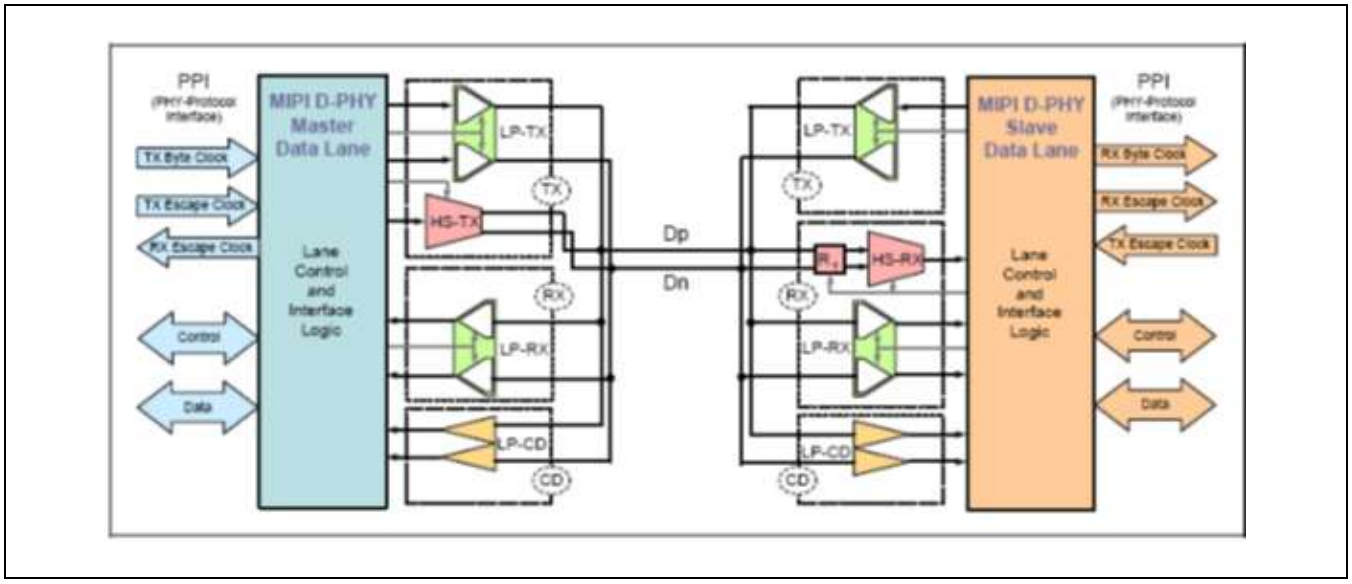


Figure 38-22 Data Lane Connection

38.6.1.3 IP Structure

The MIPI D-PHY core consists of five modules. The modules are:

- Master PLL
- Master Clock lane
- Master Data lane
- Slave Clock lane
- Slave Data lane

You can configure the modules depending on customer requirements.

For example:

- Expanding the number of data lanes up to four lanes
- Omitting the Master PLL when using another PLL for serial clock source
- Providing core in Hard Macro including IO and Power Pads.

We strongly recommend using Master and Slave lane in pair for loop-back test.

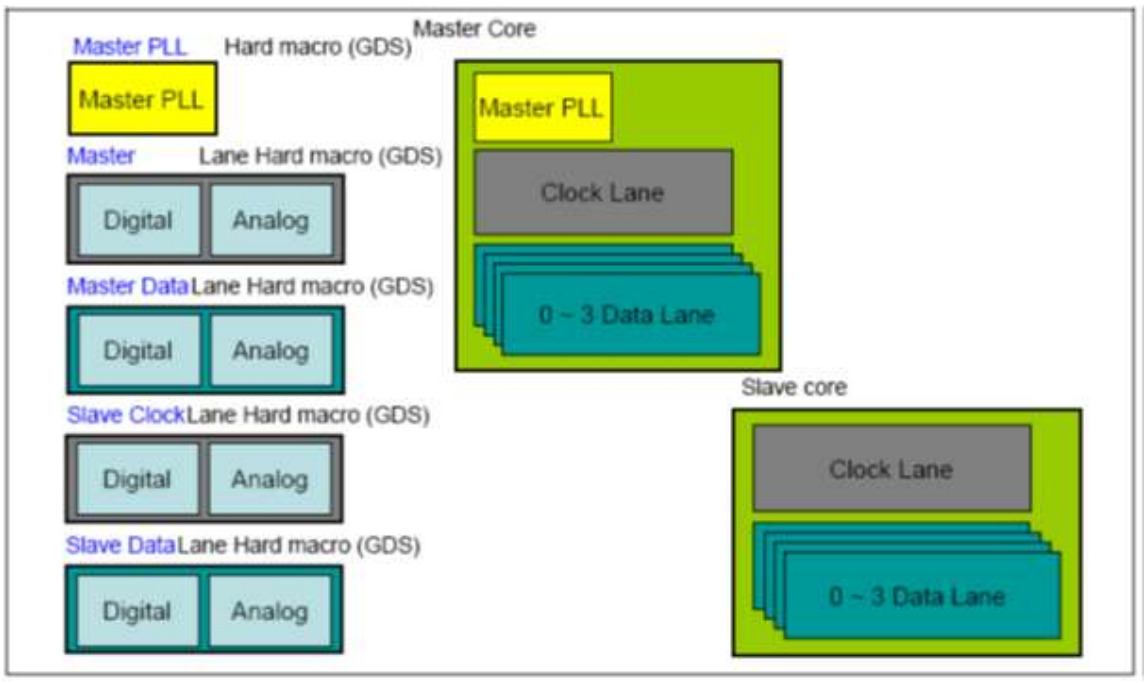


Figure 38-23 IP Structure

38.6.1.4 Power Consumption

- LN28LPP Process (without PAD)
- Operation Voltage conditions = 1.0 V ± 5 %, 1.8 V ± 5 %
- Recommended Operation Temperature range = –20°C to 85°C
- Master and slave lanes are assumed to have 1 clock + 1 data lane

The following table describes the simulation result >> condition: FF, –20°C, 1.05V, 1.89V

Mode	Master PLL	Master Lane	Slave Lane
HS (500 MHz)	2.8 mW	9 mW	3 mW
HS (1 GHz)	3.3 mW	12 mW	3.3 mW
LP (20 MHz)	–	1.2 mW	0.7 mW
ULPS	20 uW	20 uW	20 uW

Mode	AVDD10	AVDD10_PLL	AVDD18
HS (500 MHz)	12.8 mW	2.8 mW	0.3 mW
HS (1 GHz)	16 mW	3.3 mW	0.3 mW
LP (20 MHz)	2.8 mW	–	2 mW

The following table describes the simulation result >> condition: NN, 25°C, 1.0V, 1.8V

Mode	Master PLL	Master Lane	Slave Lane
HS (500 MHz)	2.5 mW	7.5 mW	2.1 mW
HS (1 GHz)	3 mW	10.3 mW	2.4 mW
LP (20 MHz)	–	0.6 mW	0.4 mW
ULPS	10 uW	10 uW	10 uW

Mode	AVDD10	AVDD10_PLL	AVDD18
HS (500 MHz)	10.2 mW	2.5 mW	0.2 mW
HS (1 GHz)	13.5 mW	3 mW	0.2 mW
LP (20 MHz)	1.8 mW	–	1.3 mW

38.6.1.5 Signals

The following table describes the Pad signals.

Name	Description
M_VREG_0P4V	Regulator capacitor connection
M_DPCLK	Master CLK Lane DP
M_DNCLK	Master CLK Lane DN
M_DNDATA0/1/2/3	Master DATA Lanes DP
M_DNDATA0/1/2/3	Master DATA Lanes DN
S_DPCLK	Slave CLK Lane DP
S_DNCLK	Slave CLK Lane DN
S_DPDATA0/1/2/3	Slave DATA Lanes DP
S_DNDATA0/1/2/3	Slave DATA Lanes DN
M_VDD10_PLL	1.0 V Power for PLL
MS_VDD10	1.0 V Power for Internal Logic
MS_VDD18	1.8 V Power for Analog
MS_VSS	Ground
VREG12_EXTPWR	External 1.2 V power connection port. This is not a pad. If you use the Internal 1.2 V Regulator, VREG12_EXTPWR power port should float. Refer to description of B_DPHYCTL[20] of DSIM for mode setting information.

38.6.1.6 Package and Board Connection Guideline

Package and Board Connection Guideline section provides implementation information regarding package and board connections of MIPI D-PHY.

The following table describes the package and board requirements.

Signal Name	Description	Bonding Pad Requirements
M_VREG_0P4V	Analog Signal	Connect a 2nF capacitor between this pin and MS_VSS. Place capacitor closely to chip.
M_DPCLK M_DNCLK M_DPDATA0/1/2/3 M_DNDATA0/1/2/3 S_DPCLK S_DNCLK S_DPDATA0/1/2/3 S_DNDATA0/1/2/3	Analog Signal	The peak current through DP and DN pads is 5.5 mA (0.44 V/80 Ω), for a maximum duty cycle of 4 % during a short-to-ground condition. Make the total resistance of the package, ESD pad, and pad-macro connection 0.5 to 1.0 Ω. To reduce inductance and via in an array-type package, route these signals through shortest traces that reach outer contacts of array. Total capacitance of package, ESD pad, and pad-macro connection should be < 2 pF. Match delays of trace lines as close as possible to minimize skew between CLK's and DATA's. Require adjacent ball assignment to minimize intra-pair differential signals skew. Match CLK and DATA pairs for routing the path to minimize intra-pair differential signals skew. Therefore, you should consider symmetrical allocation for CLK and DATA pairs.
M_VDD10_PLL	PLL 1.0 V Supply	Capable of handling 10 mA. Make the resistance from the I/O pad (s) to the macro < 0.5 Ω, with < 5 % voltage variation at the macro. The VDD and VSS connections require dedicated off-chip supplies.
MS_VDD10	D-PHY 1.0 V Supply	Capable of handling 5 mA per Lane. Make the resistance from the I/O pad (s) to the macro < 0.5 Ω, with < 5 % voltage variation at the macro. The VDD and VSS connections require dedicated off-chip supplies.
MS_VDD18	D-PHY 1.8 V Supply	Capable of handling 2 mA. Make the resistance from the I/O pad (s) to the macro < 0.5 Ω, with < 10 % voltage variation at the macro. The VDD and VSS connections require dedicated off-chip supplies.
MS_VSS	Ground	Common Ground

The followings are RC Guide Line for PKG.

- Differential Signals: R < 0.5 Ω and C < 1 pF
- Power Signals: R < 1Ω and C < 1 pF
- You should consider bump arrangement and package PCB design to ensure high speed differential pair signals goes out to last outer ball (PKG).
- CLK/DATA pairs should have the same routing length (difference < 20 um).
- PAD to BUMP metal line should be straight as possible.
- You should not place the other signals which does not relate to MIPI near MIPI differential signals.(S/W >10, S: Line Space, W: Line Width)

38.6.1.7 Core Interface Timing Diagram

Clock Lane: HS-TX and HX-RX fiction

The following figure illustrates the HS-TX and HS-RX function of Clock Lane.

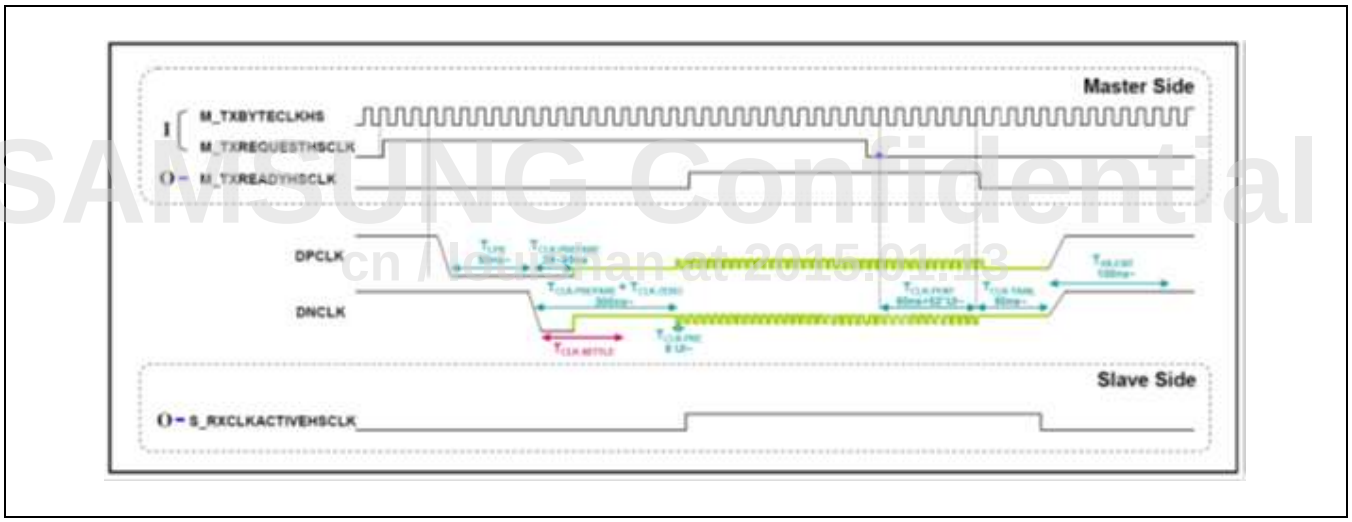


Figure 38-24 Clock Lane: HS-TX and HS-RX Function

Data Lane: HS-TX and HS-RX Function

The following figure illustrates the HS-TX and HS-RX function of Data Lane.

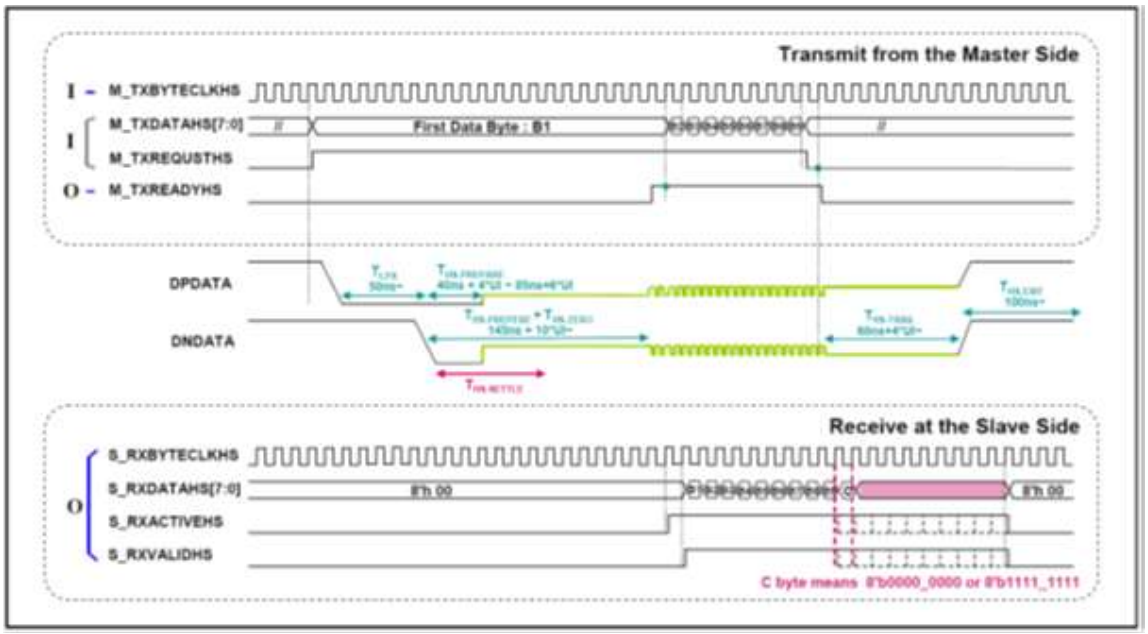


Figure 38-25 Data Lane: HS-TX and HS-RX Function

Clock Lane: ULPS Function

The following figure illustrates the ULPS function of Clock Lane.

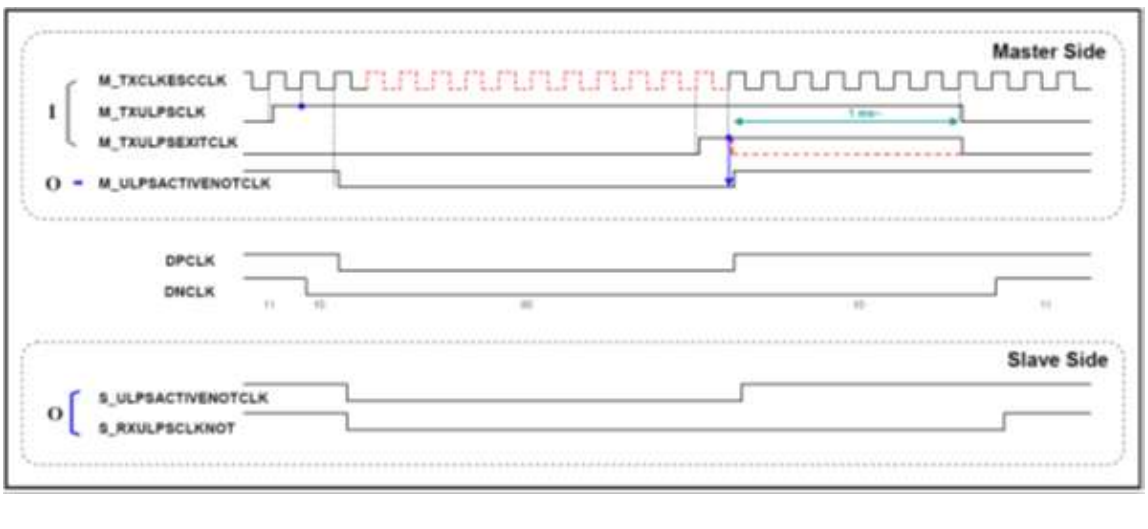


Figure 38-26 Clock Lane: ULPS Function

Data Lane: ULPS Function

The following figure illustrates the ULPS function of Data Lane.

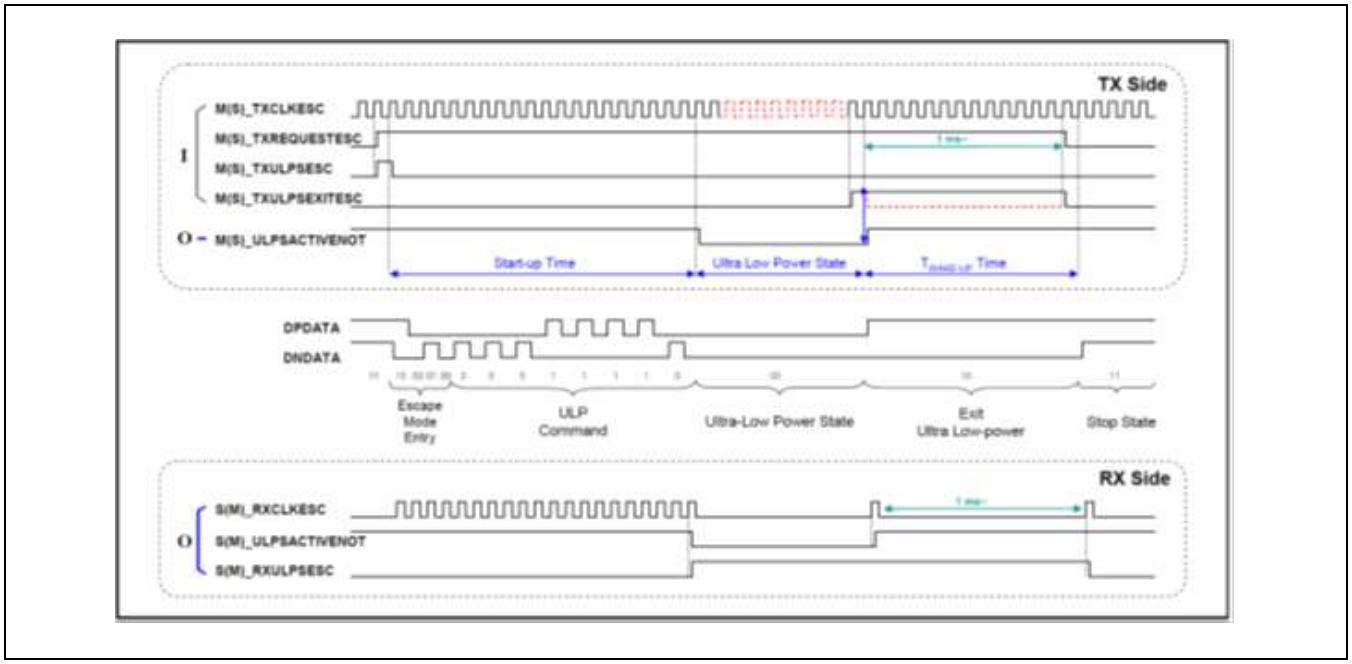


Figure 38-27 Data Lane: ULPS Function

Data Lane: LP-TX and LP-RX Function

The following figure illustrates the LP-TX and LP-RX function of Data Lane.

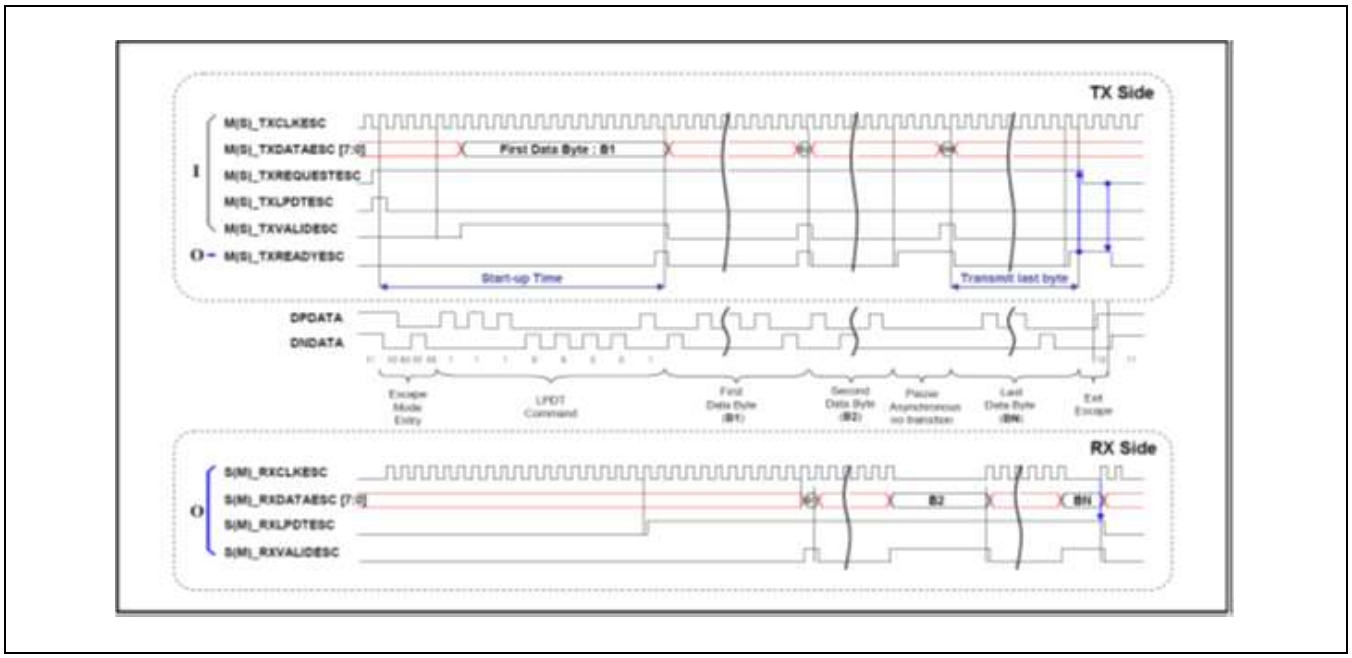


Figure 38-28 Data Lane: LP-TX and LP-RX Function

Data Lane: Remote Trigger Reset

The following figure illustrates the remote trigger reset of Data Lane.

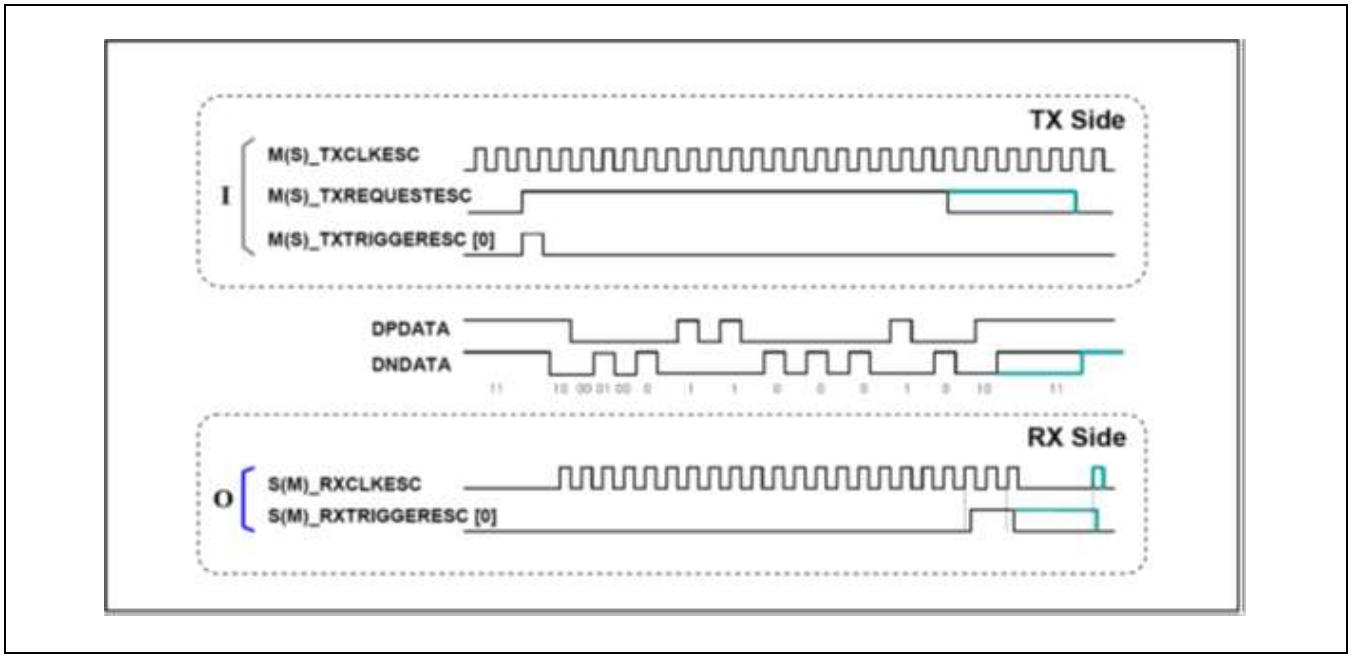


Figure 38-29 Data Lane: Remote Trigger Reset

Data Lane: Turn Around

The following figure illustrates the turnaround of Data Lane.

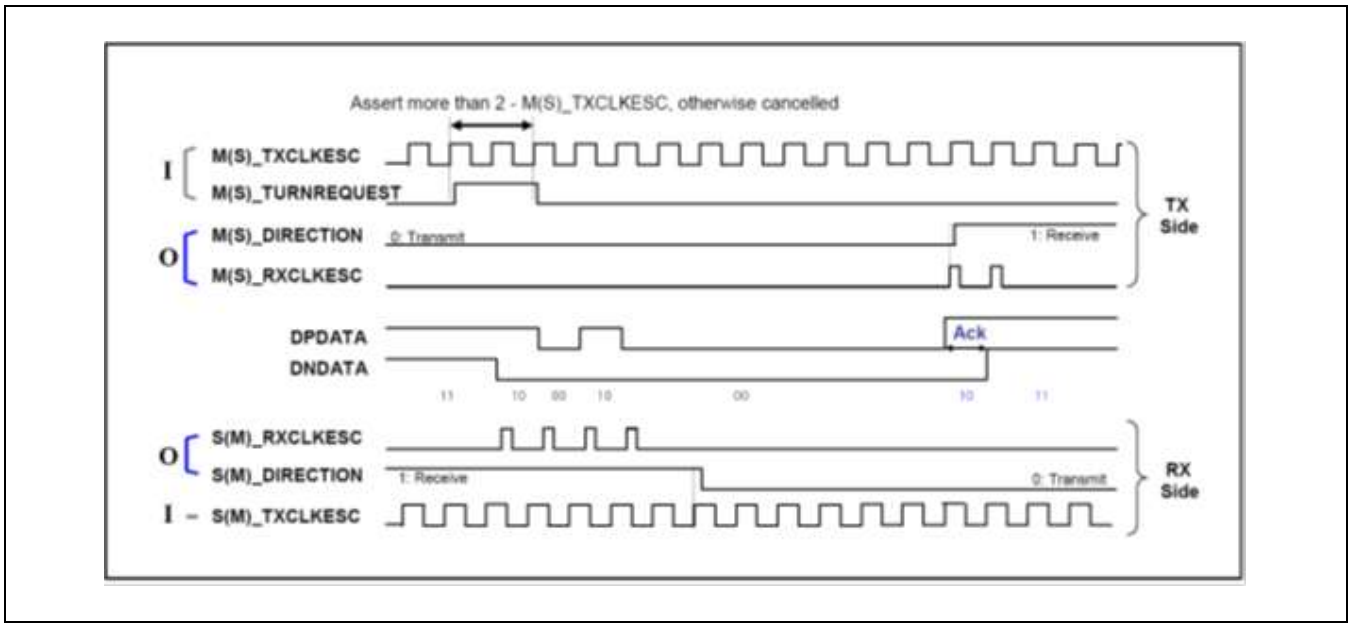


Figure 38-30 Data Lane: Turn Around

Initialization Sequence

The following figure illustrates the initialization sequence.

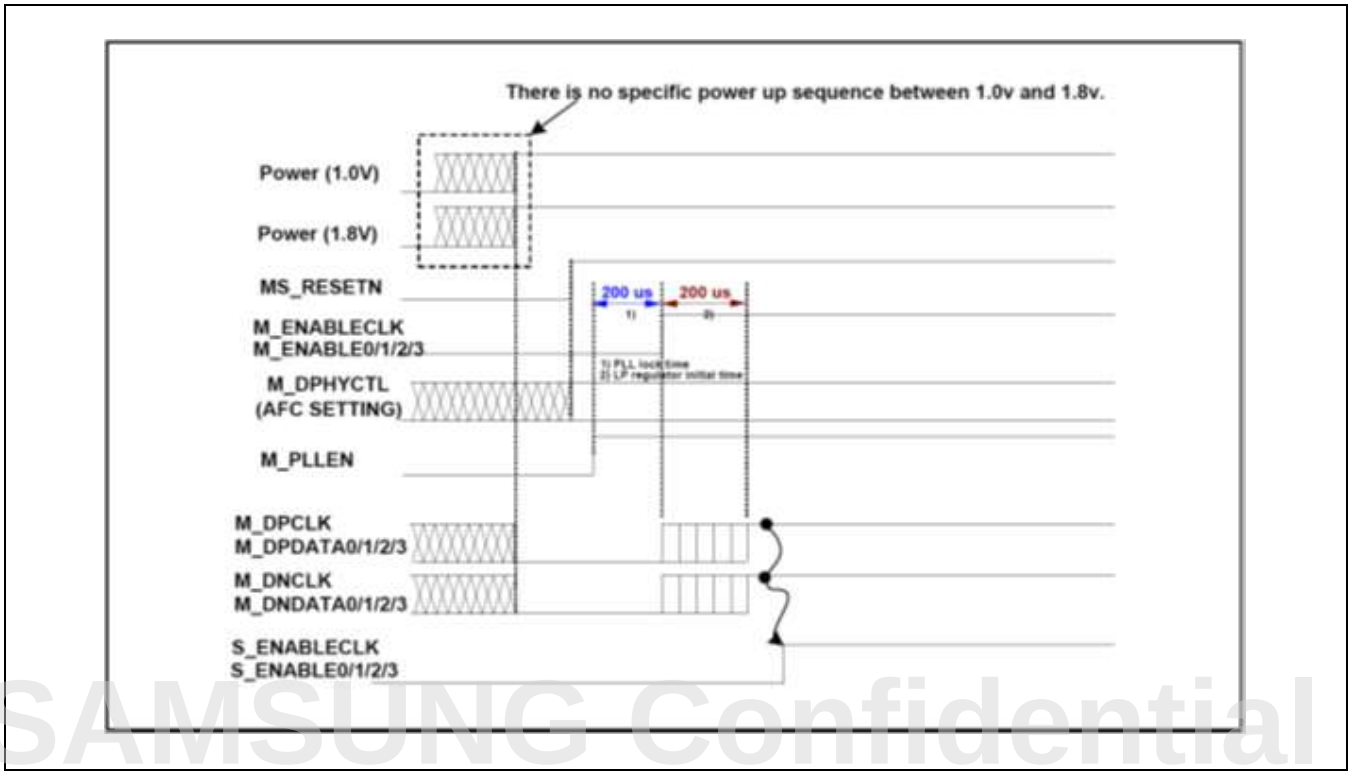


Figure 38-31 Initialization Sequence

39 Video Input Processor (VIP)

39.1 Overview

The Video Input Processor (hereinafter VIP) of the S5P4418 can receive images directly from external camera modules or video decoders. In addition, it can clip or scale down the input images and store them to the memory. The images stored from the VIP can be used for encoding by using MPEG Hardware, and as preview images by using the Multi-Layer Controller (MLC). In addition, the images can be converted to texture images for the 3D Graphics Accelerator by using the Color Space Converter.

39.2 Features

The Video Input Port features:

- ITU-R BT.656 (External CIS) and ITU-R BT.601 (External CIS and MIPI, External 8-bit, MIPI 16-bit) interface supports
- Clock, HSYNC, VSYNC and 8-bit data port (External CIS)
- Clock, HVALID, VVALID, DVALID and 16-bit data port (Internal MIPI CSI)
- External DVALID pin or Field pin supports
- Maximum 8192 × 8192 image supports
- Clipping and Scale-down
- YUV 420/422/444 memory format and Linear YUV 422 memory format
- Horizontal & Vertical Interrupt and Operation Done Interrupt
- Internal Decoder and External interface supports
- 3 Inputs from External CIS and 1 Input from MIPI CSI

39.3 VIP Interconnection

39.3.1 Block Diagram

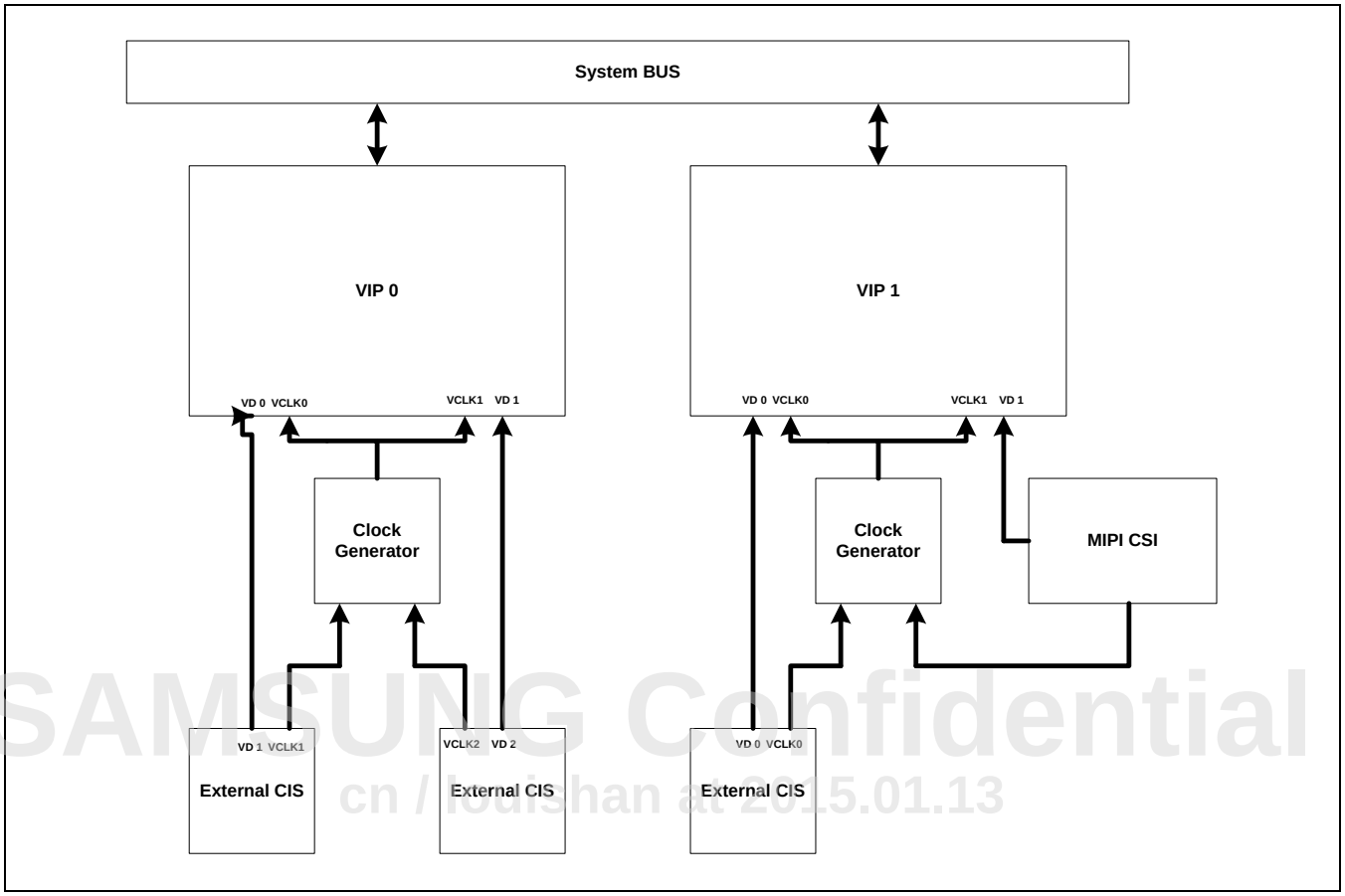


Figure 39-1 Video Input Port Interconnection

The VIP Interconnected with 3 External CIS modules and 1 MIPI CSI module as shown as *Figure 39-1*.

39.3.2 Clock Generation

The VIP can create the video in clock by using an internal PLL or an external VCLK pin as a clock source. The created video in clock is used for sync signal creation and data interface in the Video Input Port block. In general, the Video Input port is designed to fetch data on the rising edge. Therefore, if the video clock fetches data at the falling edge, the CLKSRCSEL should be set as "4".

39.4 Video Input Port

39.4.1 Block Diagram

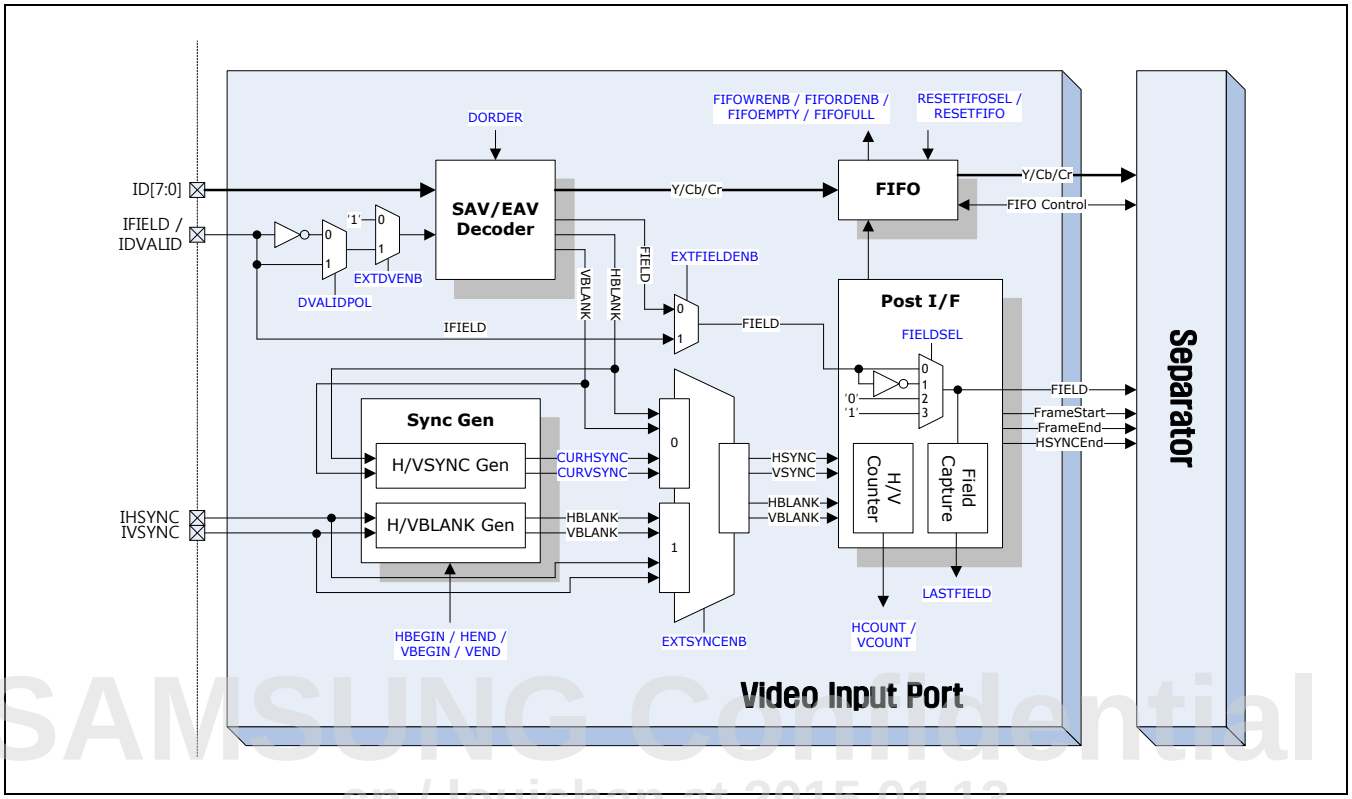


Figure 39-2 Video Input Port Block Diagram

39.4.2 Sync Generation

The horizontal and vertical timing interfaces for the video input port are as shown in *Figure 39-3*.

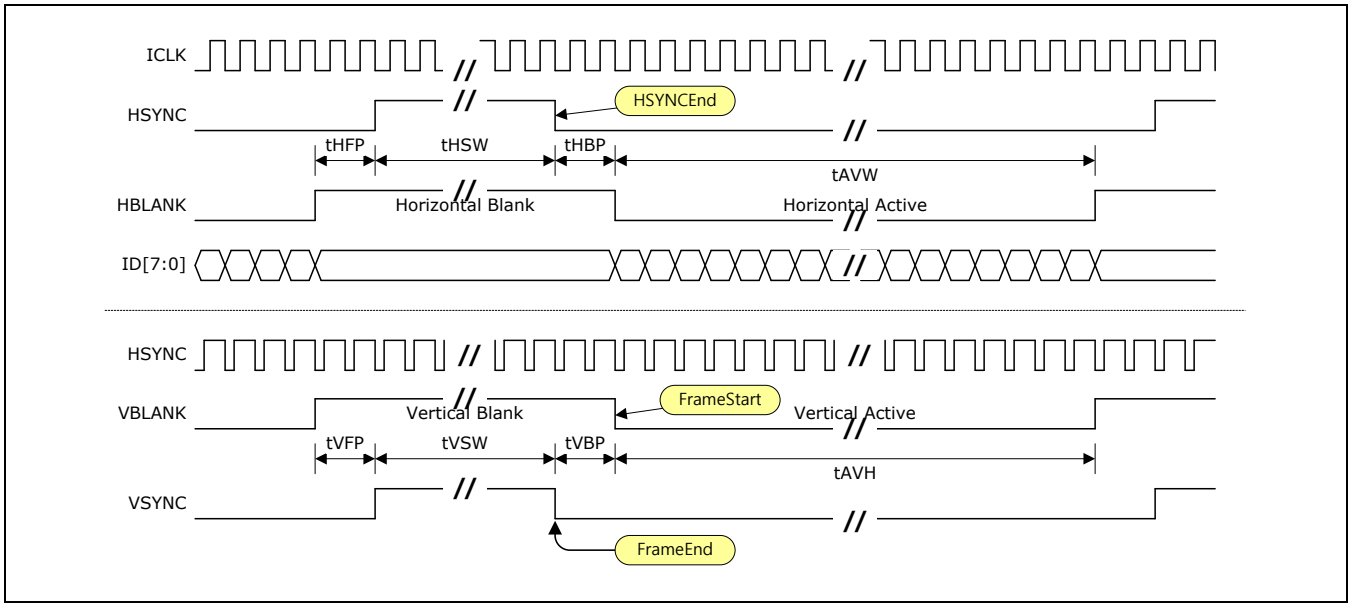


Figure 39-3 Horizontal & Vertical Timings

Each symbol in *Figure 39-3* is described in *Table 39-1*.

Table 39-1 Horizontal & Vertical Timing Symbols

Symbol	Brief	Remark
tHSW	Horizontal Sync Width	Number of ICLKs in the section where the horizontal sync pulse is active
tHBP	Horizontal Back Porch	Number of ICLKs in a section from the end point of the horizontal sync pulse to the start point of the horizontal active
tHFP	Horizontal Front Porch	Number of ICLKs in a section from the end point of the horizontal active to the start point of the horizontal sync pulse
tAVW	Active Video Width	Number of ICLKs in a horizontal active section
tVSW	Vertical Sync Width	Number of lines in a section where the vertical sync pulse is active
tVBP	Vertical Back Porch	Number of lines in a section from the end point of the vertical sync pulse to the start point of the next vertical active
tVFP	Vertical Front Porch	Number of lines in a section from the end point of the vertical active to the start point of the vertical sync pulse
tAVH	Active Video Height	Number of lines in the vertical active section

ITU-R BT.601 8-bit

The video input port has an 8-bit data bus and HSYNC and VSYNC pins, and supports ITU-R BT.601 8-bit input. If the port uses an external HSYNC or VSYNC, the EXTSYNCENB bit should be set as "1". If the EXTSYNCENB bit is "1", the port receives the HSYNC and VSYNC from the outside, and creates the HBLANK and VBLANK internally. The polarity of the external H(V)SYNC only supports high active. *Figure 39-4* shows the relationship between the HBLANK and the VBLANK generated from external HSYNC and VSYNC inputs.

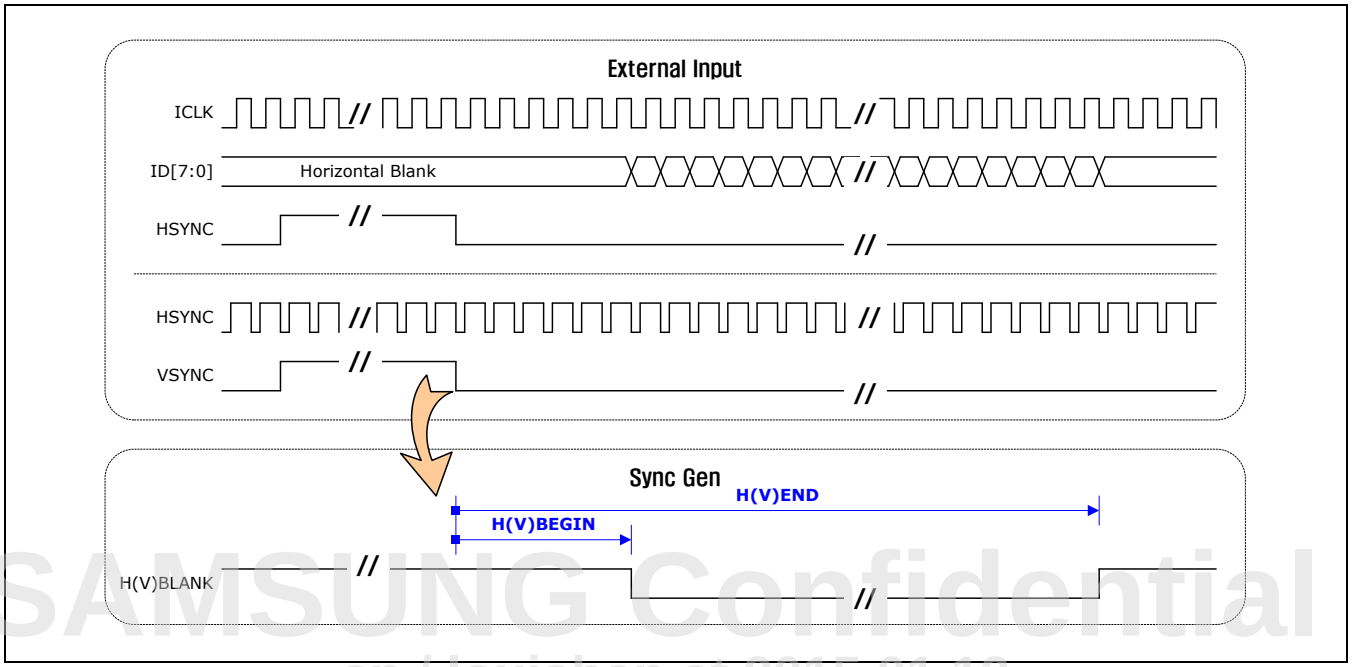


Figure 39-4 Generation for ITU-R BT.601 8-bit

The HBEGIN and the HEND are used to generate the HBLANK from the HSYNC. The VBEGIN and the VEND are used to generate the VBLANK from the VSYNC. The settings for each register are listed in *Table 39-2*.

Table 39-2 Register Settings for ITU-R BT.601 8-bit

Register	Formula	Remark
VBEGIN	tVBP - 1	Number of lines in a section from the end point of the VSYNC to the start point of the vertical active video - 1
VEND	tVBP + tAVH - 1	Number of lines in a section from the end point of the VSYNC to the end point of the vertical active video - 1
HBEGIN	tHBP - 1	Number of clocks in a section from the end point of the HSYNC to the start point of the horizontal active video - 1
HEND	tHBP + tAVW - 1	Number of clocks in a section from the end point of the HSYNC to the start point of the horizontal active video - 1

ITU-R BT.656

In the ITU-R BT.656 format, there is no additional sync signal pin, and the sync information is transmitted along with data via data pins. At this time, the Sync information is inserted as an additional code before the start point of the valid data (SAV) and after the end of the valid data (EAV). Sync information included in data is as shown in *Figure 39-5*.

CB359	Y718	CR359	Y719	FF	00	00	CODE	Blank	FF	00	00	CODE	CB0	Y0	CR0	Y1	
				EAV					SAV								

Figure 39-5 Data Stream Format with SAV/EAV

The SAV and the EAV consists of [FF, 00, 00, CODE]. Each code contains Field (F), VSYNC (V) and HSYNC (H) data, and each code is composed as follows:

Table 39-3 Embedded Sync Code

Bit		7	6	5	4	3	2	1	0	Hex	Brief Description
Function		1	F	V	H	P3	P2	P1	P0		
(FVH)	0	1	0	0	0	0	0	0	0	80h	SAV of odd field
	1	1	0	0	1	1	1	0	1	9Dh	EAV of odd field
	2	1	0	1	0	1	0	1	1	ABh	SAV of odd blank
	3	1	0	1	1	0	1	1	0	B6h	EAV of odd blank
	4	1	1	0	0	0	1	1	1	C7h	SAV of even field
	5	1	1	0	1	1	0	1	0	DAh	EAV of even field
	6	1	1	1	0	1	1	0	0	ECh	SAV of even blank
	7	1	1	1	1	0	0	0	1	F1h	EAV of even blank

- F: Field select (0 = Odd field, 1 = Even field)
- V: Vertical blanking (0 = Active, 1 = Blank)
- H: SAV/EAV (0 = SAV, 1 = EAV)
- Parity: P3 = V xor H, P2 = F xor H, P1 = F xor V, P0 = F xor V xor H

To create the HBLANK and VBLANK from the sync information contained in the data, the EXTSYNCENB should be set as "0". The SAV/EAV decoder blocks generate the HBLANK and VBLANK from the sync information contained in the data. The Sync Gen block generates the HSYNC and the VSYNC based on the HBLANK and VBLANK signals. *Figure 39-6* shows the relationship that generates the H(V)BLANK and H(V)SYNC from the SAV/EAV contained in the data.

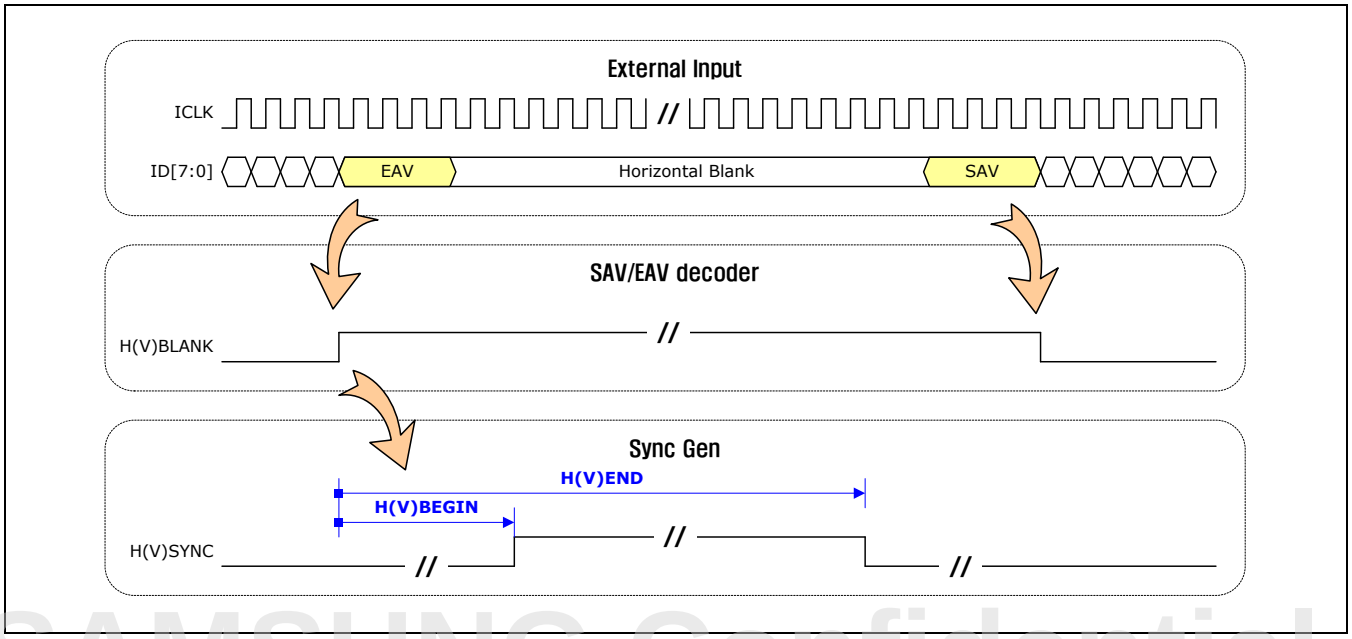


Figure 39-6 Sync Generation for ITU-R BT.656

If the EXTSYNCENB is "0", the HBEGIN and HEND*are used to generate the HSYNC signal from the HBLANK. The *VBEGIN and VEND are used to generate the VSYNC signal from the VBLANK. The settings for each register are listed in *Table 39-4*.

Table 39-4 Register Settings for ITU-R BT.656

Register	Formula	Remark
VBEGIN	tVFP + 1	Number of lines in a section from the end point of the vertical active video to the start point of the VSYNC - 1
VEND	tVFP + tVSW + 1	Number of lines in a section from the end point of the vertical active video to the end point of the VSYNC + 1
HBEGIN	tHFP - 7	Number of clocks in a section from the end point of the horizontal active video to the start point of the HSYNC - 7
HEND	tHFP+ tHSW - 7	Number of clocks in a section from the end point of the horizontal active video to the end point of the HSYNC - 7

ITU BT.656-like support

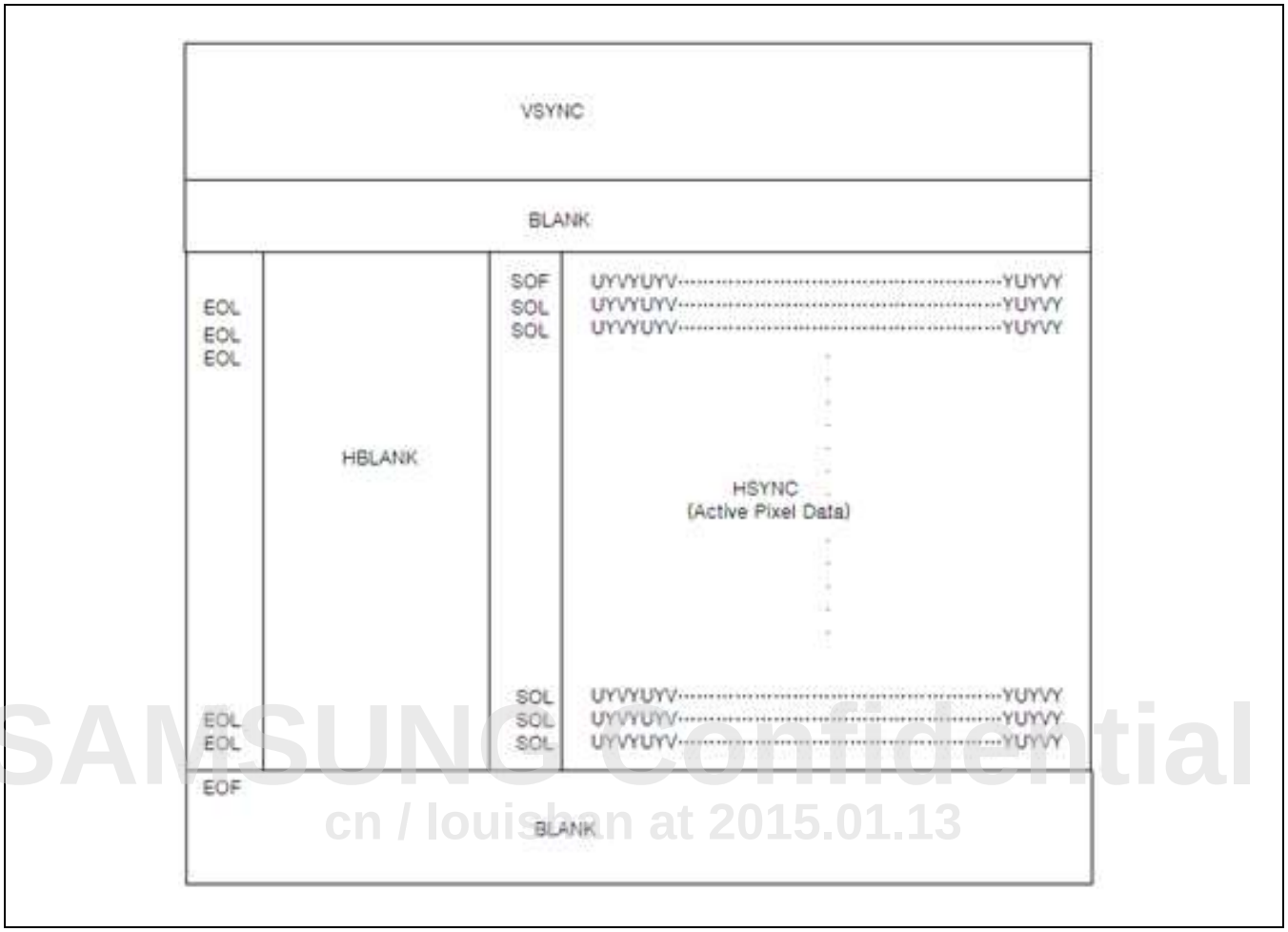


Figure 39-7 Frame Structure of ITU656-like

Our VIP supports ITU656-like which could be configurable as follows:

- SOF = 0xFF00_0080
- EOF = 0xFF00_00B6
- SOL = 0xFF00_0080
- EOL = 0xFF00_009D

39.4.3 External Data Valid and Field

The video input port can receive data valid signals or field signals from the outside. Since the IDVALID and the IFIELD share a pin, users can use only one of them.

External Data Valid

If the EXTDVENB is set as "1", users can use the input signal from the IFIELD/IDVALID pad as the IDVALID signal. In this case, the polarity is determined by the DVALIDPOL. The video input port is designed to use the IDVALID signal of active high mode internally. Therefore, if the polarity of an external IDVALID signal is active low, the input signal should be inverted by setting the DVALIDPOL as "0". If the polarity of an external IDVALID signal is active high, the input signal should be bypassed by setting the DVALIDPOL as 1.

Even though an external IDVALID signal is used, the internal HBLANK and VBLANK signals are used. Therefore, the user should set the H(V)BEGIN and the H(V)END.

External Field

If an external field signal is used, the EXTFIELDENB should be set as 1. In the ITU-R BT.656 format, the input signal from the IFIELD/IDVALID pad can be used as an external field signal by setting the EXTFIELDENB as "1". The video input port internally considers it as an odd field if the polarity of the field signal is low. If the polarity of a field signal is high, the port considers it as an even field. The user can select the polarity of a field signal by using FIELDSEL, or can fix the polarity as "0 or "1".

39.4.4 Data Order

The video input port can select the order of input data. Basically, the ITU-R BT.656 format or the ITU-R BT.601 8-bit format has the order [Cb, Y0, Cr, Y1]. If the order of the input data is different from the default order, users can change the order via DORDER. The data orders supported by the video input port are listed in *Table 39-5*.

Table 39-5 Input Data Order

DORDER	0				1				2				3			
ICLK	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th
ID[7]	Cb[7]	YN[7]	Cr[7]	YN+1[7]	Cr[7]	YN+1[7]	Cb[7]	YN[7]	YN[7]	Cb[7]	YN+1[7]	Cr[7]	YN+1[7]	Cr[7]	YN[7]	Cb[7]
ID[6]	Cb[6]	YN[6]	Cr[6]	YN+1[6]	Cr[6]	YN+1[6]	Cb[6]	YN[6]	YN[6]	Cb[6]	YN+1[6]	Cr[6]	YN+1[6]	Cr[6]	YN[6]	Cb[6]
ID[5]	Cb[5]	YN[5]	Cr[5]	YN+1[5]	Cr[5]	YN+1[5]	Cb[5]	YN[5]	YN[5]	Cb[5]	YN+1[5]	Cr[5]	YN+1[5]	Cr[5]	YN[5]	Cb[5]
ID[4]	Cb[4]	YN[4]	Cr[4]	YN+1[4]	Cr[4]	YN+1[4]	Cb[4]	YN[4]	YN[4]	Cb[4]	YN+1[4]	Cr[4]	YN+1[4]	Cr[4]	YN[4]	Cb[4]
ID[3]	Cb[3]	YN[3]	Cr[3]	YN+1[3]	Cr[3]	YN+1[3]	Cb[3]	YN[3]	YN[3]	Cb[3]	YN+1[3]	Cr[3]	YN+1[3]	Cr[3]	YN[3]	Cb[3]
ID[2]	Cb[2]	YN[2]	Cr[2]	YN+1[2]	Cr[2]	YN+1[2]	Cb[2]	YN[2]	YN[2]	Cb[2]	YN+1[2]	Cr[2]	YN+1[2]	Cr[2]	YN[2]	Cb[2]
ID[1]	Cb[1]	YN[1]	Cr[1]	YN+1[1]	Cr[1]	YN+1[1]	Cb[1]	YN[1]	YN[1]	Cb[1]	YN+1[1]	Cr[1]	YN+1[1]	Cr[1]	YN[1]	Cb[1]
ID[0]	Cb[0]	YN[0]	Cr[0]	YN+1[0]	Cr[0]	YN+1[0]	Cb[0]	YN[0]	YN[0]	Cb[0]	YN+1[0]	Cr[0]	YN+1[0]	Cr[0]	YN[0]	Cb[0]

39.4.5 Status

Horizontal & Vertical Counter

The video input port can inform the user of the size of the active section. The HCOUNT*indicates the total clock numbers of a line in the active video section. The *VCOUNT indicates the total line numbers in the active video section.

Current HSYNC & VSYNC Status

When the EXTSYNCENB is "0" the CURHSYNC and the CURVSYNC bits are provided to show the HSYNC and VSYNC states.

Current Field Status

Users can display the status of the current field signal by using the LASTFIELD bit as shown in *Figure 39-8*.

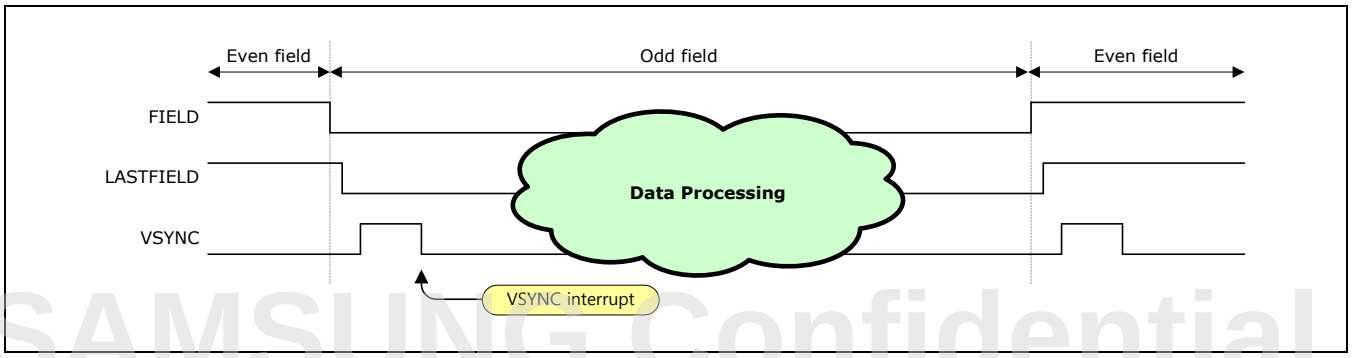


Figure 39-8 Field Information

LASTFIELD is updated whenever a field signal is changed. In addition, when a VSYNC interrupt occurs, the user can get the field status of the next data by using LASTFIELD. Since LASTFIELD is updated by using the PCLK, the PCLK should be always enabled by setting the PCLKMODE as "1" to obtain a proper field status.

39.4.6 FIFO Controls

The video input port block can inform the user of the current status of the internal FIFO. The FIFOWRENB indicates if data is being written to the FIFO. The FIFORDENB indicates if data is being read from the FIFO. If the FIFO is empty, the FIFOEMPTY is set as "1". If the FIFO is full, the FIFOFULL is set as "1".

In addition, users can reset the FIFO at a specific point. According to the RESETFIFOSEL*setting, the reset point of the FIFO can be controlled by selecting either FrameEnd (the end of VSYNC, *RESETFIFOSEL is "0"), Frame Start (the start of vertical active video, RESETFIFOSEL is "1") or the RESETFIFO bit (RESETFIFOSEL is "2"), or by selecting all of them (RESETFIFOSEL is "3"). The RESETFIFO bit is valid only when the RESETFIFOSEL*is "2" or "3". If the FIFO is reset by setting the *RESETFIFO as "1", the RESETFIFO should be set as "0" again.

39.4.7 Recommend Setting for Video Input Port

Table 39-6 lists the recommend settings for the video input port by input formats.

Table 39-6 Recommend Setting for Video Input Port

Register	ITU-R BT.656	ITU-R BT.601 8-bit	
		Progressive	Interlace
EXTSYNCENB	0	1	
DWIDTH	1	1	
DORDER	0 (default)	0 (default)	
EXTFIELDENB	0	0	1
FIELDSEL	0	3	0 or 1
EXTDVENB	0	0 or 1	0
DVALIDPOL	Not used	0 or 1	Not used
VBEGIN	tVFP + 1	tVBP - 1	
VEND	tVFP + tVSW + 1	tVBP + tAVH - 1	
HBEGIN	tHFP - 7	tHBP - 1	
HEND	tHFP+ tHSW - 7	tHBP + tAVW - 1	

39.5 Clipper & Decimator

39.5.1 Clipping & Scale-down

The VIP can store input images to the memory after clipping or scaling down. An input image is transmitted to the Clipper through the video input port and the Separator. The Clipper clips a specific area from the input image, and then stores the result in the memory and transmits the result to the Decimator. The Decimator can store the image transmitted from the Clipper in the memory after scaling down the image. *Figure 39-9* shows the procedure for clipping and scaling down an input image.

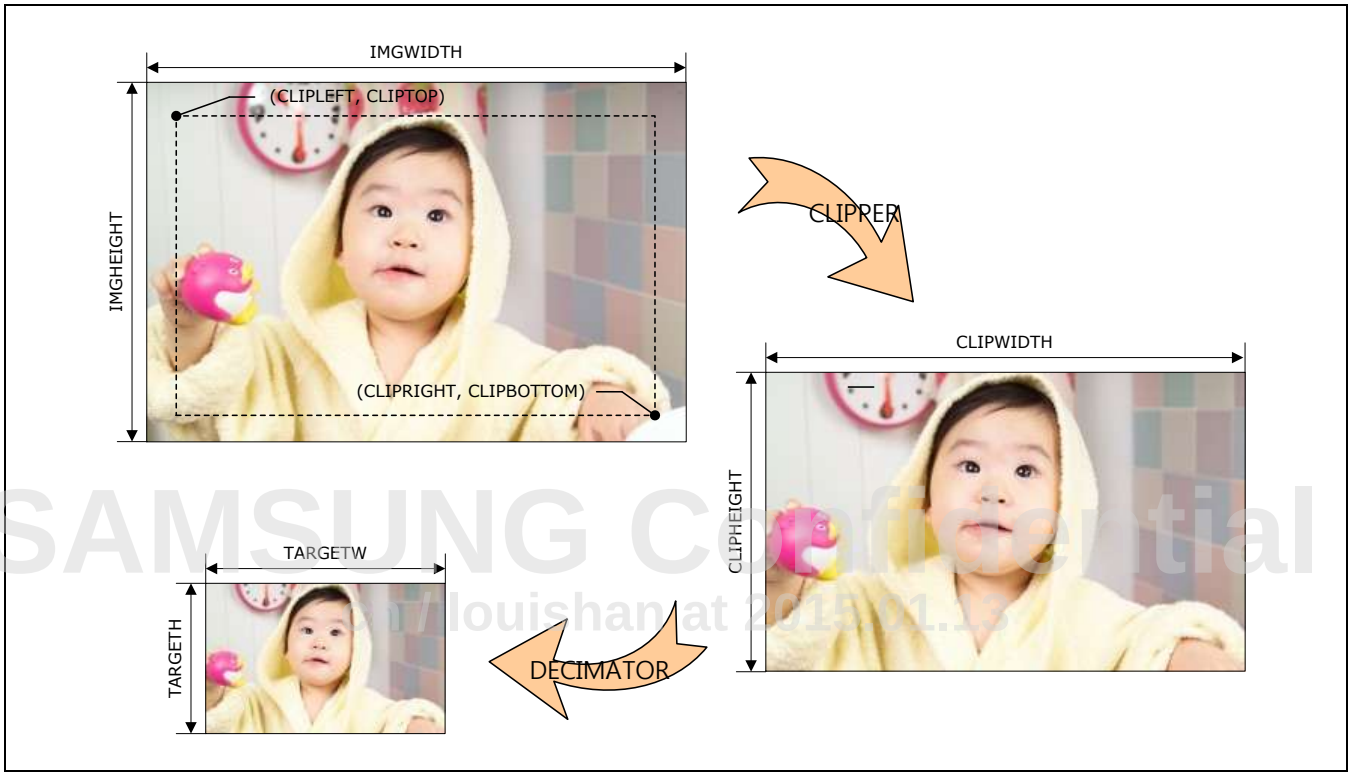


Figure 39-9 Clipping & Decimation

Users can enable the Clipper to clip an input image by specifying the relevant area, using CLIPLEFT, CLIPRIGHT, CLIPTOP and CLIPBOTTOM.

The Decimator scales down the clipped image by using the Bresenham algorithm. To this end, TARGETW, TARGETH, DELTAW, DELTAH, CLEARW, and *CLEARH*are used. *Table 39-7* lists the settings for each register.

Table 39-7 Registers for Scaling

Register	Formula	Range	Unit	Remark
TARGETW	–	0 to 8191	Pixel	Width of a scaled-down image
TARGETH	–	0 to 8191	Pixel	Height of a scaled-down image
DELTAW	CLIPWIDTH - TARGETW	0 to 8191	Pixel	Width difference between the original image and the result image
DELTAH	CLIPHEIGHT - TARGETH	0 to 8191	Pixel	Height difference between the original image and the result image
CLEARW	TARGETW - DELTAW	–8192 to 8191	Pixel	Difference between the width of the result image and the DELTAW
CLEARH	TARGETH - DELTAH	–8192 to 8191	Pixel	Difference between the height of the result image and the DELTAH

39.5.2 Output Data Format

The VIP can store input images in separated YUV format and linear YUV 4:2:2 format. The Clipper supports both separated YUV format and linear YUV 4:2:2 format. If the YUYVENB is set as "0", data is stored in separated YUV format. If the YUYVENB is set as "1", data is stored in linear YUV 4:2:2 format. The Decimator only supports separated YUV format.

Linear YUV 4:2:2 format

Linear YUV format is the YUYV format, and Y (luminance) exists in each pixel. Cb and Cr (Chrominance) separately exist in each of two pixels, and two pixels share the Cr and the Cb (Chrominance). The VIP has 2-pixel information per 32-bit and is managed in 2-pixel units. *Table 39-8* shows the memory format that Y/Cb/Cr data are stored in.

Table 39-8 YUYV Format

Pixel Format	YUYVENB	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
YUYV	1	Cr[7:0]								Y1[7:0]								Cb[7:0]								Y0[7:0]							

The BASEADDRL(H)*and the*STRIDEL(H)*are used for the addressing of the linear YUV 4:2:2 format. The *BASEADDR*is a 32-bit linear address, and specifies the memory address where output images from the Clipper are stored. The *STRIDE is the memory offset from one scan line in the image buffer to the next. The STRIDE is expressed in byte units and is also called pitch. If there is no-memory gap between lines in the image buffer, the stride can be specified as CLIPWIDTH * 2.

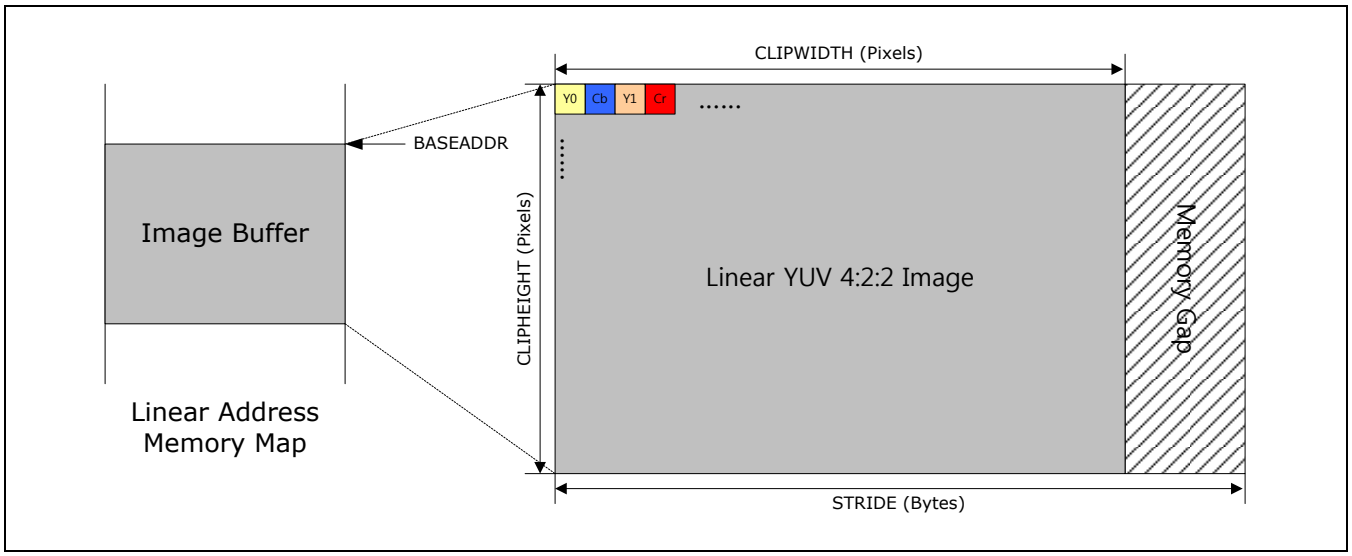


Figure 39-10 Address Generation for Linear YUV 422 Format

The linear YUV 4:2:2 format is only supported by the Clipper, and YUYVENB should be set as "1".

Separated YUV format

In separated YUV format, each of Y, U and V exists at separate memory spaces. In addition, separated YUV format is divided into 4:4:4, 4:2:2 and 4:2:0 in proportion to U and V for Y. Separated YUV format is the addressing format, and each component has a size of 64 × 32 and linearity in block units. These features provide the S5P4418's unique memory format, to enhance the effectiveness of memory access when the S5P4418 manages data in macro block units through an algorithm to compress/decompress images such as MPEG files.

According to each format, Y, U and V correspond to 2 × 2 pixels as follows:

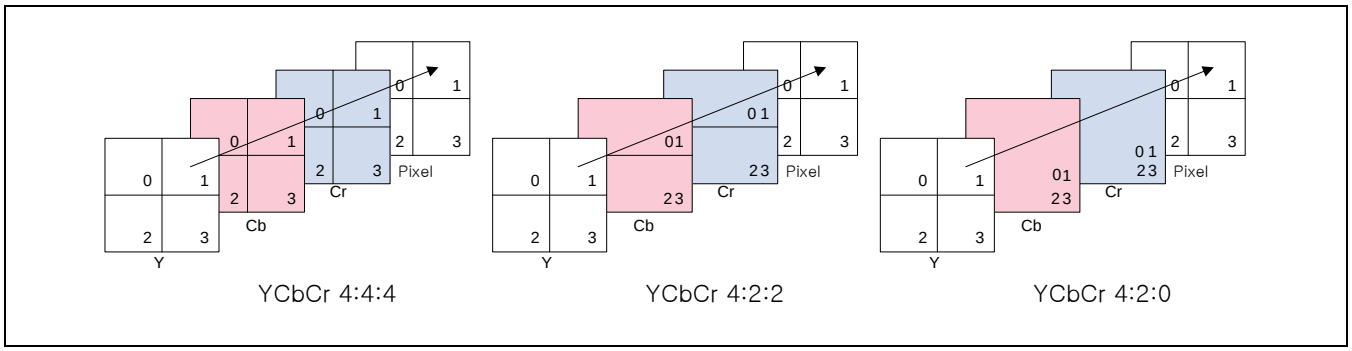


Figure 39-11 Separated YUV Format

Users can select wither 4:4:4, 4:2:2 or 4:2:0 format by using FORMATSEL. In the Clipper.

In the separator YUV addressing format, the memory address to which data is stored is specified by stride. The Clipper stride has 16-bit width and it is up to 65535. And this values set by STRIDEL(H), STRIDEL(L). In Decimation, TARGETW register uses stride of decimator. X and Y coordinates can have values between 0 and 4095 as the offsets for each axis in a segment. The X-axis area is specified by using LEFT and RIGHT, and the Y-axis area is specified by using TOP and BOTTOM. These parameters are provided for each of Y, Cb and Cr separately and are listed in *Table 39-9*.

Table 39-9 Address Generation Registers for Separated YUV Format

Component	Segment	Left	Right	Top	Bottom
Y	LUSEG	LULEFT	LURIGHT	LUTOP	LUBOTTOM
Cb	CBSEG	CBLEFT	CBRIGHT	CBTOP	CBBOTTOM
Cr	CRSEG	CRLEFT	CRRIGHT	CRTOP	CRBOTTOM

39.5.3 Interlace Scan Mode

If the INTERLACENB is set as "1" for interlace scan mode, the Clipper and Decimator store output images by field signals. The Clipper and Decimator can also select the polarity of a field signal by using FIELDINV. The Clipper supports frame-based output images, and outputs the images after automatically adjusting the start address and the start line depending on the field signal. For interlaced images, the Decimator only handles and stores even field data.

39.5.4 Pixels Alignment

The VIP Input and output image size should be aligned to 64 pixels.

39.6 Interrupt Generation

The VIP has three interrupt sources. The three interrupt sources are the HSINT, which generates an interrupt at the end of a horizontal sync, the VSINT, which generates an interrupt at the end of a vertical sync, and the ODINT, which generates an interrupt when the Clipper and Decimator operations are finished. The Pending bits and the Enable bits for each interrupt exist, and each register is listed in *Table 39-10*.

Table 39-10 Interrupt Registers

Interrupt	Enable bit	Pending bit	Condition
HSINT	HSINTENB	HSINTPEND	End of a horizontal sync pulse
VSINT	VSINTENB	VSINTPEND	End of a vertical sync pulse
ODINT	ODINTENB	ODINTPEND	Completion of the Clipper and Decimator operations

39.7 Register Description

39.7.1 Register Map Summary

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)

Register	Offset	Description	Reset Value
VIP_CONFIG	0x00 (VIP0)/ 0x00 (VIP1)	VIP Configuration Register	0x0000_0000
VIP_INTCTRL	0x04 (VIP0)/ 0x04 (VIP1)	VIP Interrupt Control Register	0x0000_0000
VIP_SYNCCTRL	0x08 (VIP0)/ 0x08 (VIP1)	VIP Sync Control Register	0x0000_0000
VIP_SYNCMON	0x0C (VIP0)/ 0x0C (VIP1)	VIP Sync Monitor Register	0x0000_0003
VIP_VBEGIN	0x10 (VIP0)/ 0x10 (VIP1)	VIP Vertical Sync Start Register	0x0000_0000
VIP_VEND	0x14(VIP0)/ 0x14 (VIP1)	VIP Vertical Sync End Register	0x0000_0000
VIP_HBEGIN	0x18 (VIP0)/ 0x18 (VIP1)	VIP Horizontal Sync Start Register	0x0000_0000
VIP_HEND	0x1C (VIP0)/ 0x1C (VIP1)	VIP Horizontal Sync End Register	0x0000_0000
VIP_FIFOCTRL	0x20 (VIP0)/ 0x20 (VIP1)	VIP FIFO Control Register	0x0000_0000
VIP_HCOUNT	0x24 (VIP0)/ 0x24 (VIP1)	VIP Horizontal Counter Register	0x0000_0000
VIP_VCOUNT	0x28 (VIP0)/ 0x28 (VIP1)	VIP Vertical Counter Register	0x0000_0000
RSVD	0x2C to 0xFF (VIP0)/ 0x2C to 0xFF (VIP1)	Reserved	-
VIP_CDENB	0x200 (VIP0)/ 0x200 (VIP1)	VIP Clipper & Decimator Enable Register	0x0000_0000
VIP_ODINT	0x204 (VIP0)/ 0x204 (VIP1)	VIP Operation Done Interrupt Register	0x0000_0000
VIP_IMGWIDTH	0x208 (VIP0)/ 0x208 (VIP1)	VIP Image Width Register	0x0000_0000
VIP_IMGHEIGHT	0x20C (VIP0)/ 0x20C (VIP1)	VIP Image Height Register	0x0000_0000
CLIP_LEFT	0x210 (VIP0)/ 0x210 (VIP1)	VIP Clipper Left Register	0x0000_0000
CLIP_RIGHT	0x214 (VIP0)/	VIP Clipper Right Register	0x0000_0000

Register	Offset	Description	Reset Value
	0x214 (VIP1)		
CLIP_TOP	0x218 (VIP0)/ 0x218 (VIP1)	VIP Clipper Top Register	0x0000_0000
CLIP_BOTTOM	0x21C (VIP0)/ 0x21C (VIP1)	VIP Clipper Bottom Register	0x0000_0000
DECI_TARGETW	0x220 (VIP0)/ 0x220 (VIP1)	VIP Decimator Target Width Register	0x0000_0000
DECI_TARGETH	0x224 (VIP0)/ 0x224 (VIP1)	VIP Decimator Target Height Register	0x0000_0000
DECI_DELTAW	0x228 (VIP0)/ 0x228 (VIP1)	VIP Decimator Delta Width Register	0x0000_0000
DECI_DELTAH	0x22C (VIP0)/ 0x22C (VIP1)	VIP Decimator Delta Height Register	0x0000_0000
DECI_CLEARW	0x230 (VIP0)/ 0x230 (VIP1)	VIP Decimator Clear Width Register	0x0000_0000
DECI_CLEARH	0x234 (VIP0)/ 0x234 (VIP1)	VIP Decimator Clear Height Register	0x0000_0000
DECI_LUSEG	0x238 (VIP0)/ 0x238 (VIP1)	VIP Decimator Lu Segment Register	0x0000_0000
DECI_CRSEG	0x23C (VIP0)/ 0x23C (VIP1)	VIP Decimator Cr Segment Register	0x0000_0000
DECI_CBSEG	0x240 (VIP0)/ 0x240 (VIP1)	VIP Decimator Cb Segment Register	0x0000_0000
DECI_FORMAT	0x244 (VIP0)/ 0x244 (VIP1)	VIP Decimator Format Register	0x0000_0000
DECI_ROTFLIP	0x248 (VIP0)/ 0x248 (VIP1)	VIP Decimator Rotation & Flip Register	0x0000_0000
DECI_LULEFT	0x24C (VIP0)/ 0x24C (VIP1)	VIP Decimator Lu Left Register	0x0000_0000
DECI_CRLEFT	0x250 (VIP0)/ 0x250 (VIP1)	VIP Decimator Cr Left Register	0x0000_0000
DECI_CBLEFT	0x254 (VIP0)/ 0x254 (VIP1)	VIP Decimator Cb Left Register	0x0000_0000
DECI_LURIGHT	0x258 (VIP0)/ 0x258 (VIP1)	VIP Decimator Lu Right Register	0x0000_0000
DECI_CRRIGHT	0x25C (VIP0)/ 0x25C (VIP1)	VIP Decimator Cr Right Register	0x0000_0000
DECI_CBRIGHT	0x260 (VIP0)/ 0x260 (VIP1)	VIP Decimator Cb Right Register	0x0000_0000
DECI_LUTOP	0x264 (VIP0)/ 0x264 (VIP1)	VIP Decimator Lu Top Register	0x0000_0000
DECI_CRTOP	0x268 (VIP0)/ 0x268 (VIP1)	VIP Decimator Cr Top Register	0x0000_0000

Register	Offset	Description	Reset Value
DECI_CBTOP	0x26C (VIP0)/ 0x26C (VIP1)	VIP Decimator Cb Top Register	0x0000_0000
DECI_LUBOTTOM	0x270 (VIP0)/ 0x270 (VIP1)	VIP Decimator Lu Bottom Register	0x0000_0000
DECI_CRBOTTOM	0x274 (VIP0)/ 0x274 (VIP1)	VIP Decimator Cr Bottom Register	0x0000_0000
DECI_CBBOTTOM	0x278 (VIP0)/ 0x278 (VIP1)	VIP Decimator Cb Bottom Register	0x0000_0000
CLIP_LUSEG	0x27C(VIP0)/ 0x27C (VIP1)	VIP Clipper Lu Segment Register	0x0000_0000
CLIP_CRSEG	0x280 (VIP0)/ 0x280 (VIP1)	VIP Clipper Cr Segment Register	0x0000_0000
CLIP_CBSEG	0x284 (VIP0)/ 0x284 (VIP1)	VIP Clipper Cb Segment Register	0x0000_0000
CLIP_FORMAT	0x288 (VIP0)/ 0x288 (VIP1)	VIP Clipper Format Register	0x0000_0000
CLIP_ROTFLIP	0x28C (VIP0)/ 0x28C (VIP1)	VIP Clipper Rotation & Flip Register	0x0000_0000
CLIP_LULEFT	0x290 (VIP0)/ 0x290 (VIP1)	VIP Clipper Lu Left Register	0x0000_0000
CLIP_CRLEFT	0x294 (VIP0)/ 0x294 (VIP1)	VIP Clipper Cr Left Register	0x0000_0000
CLIP_CBLEFT	0x298 (VIP0)/ 0x298 (VIP1)	VIP Clipper Cb Left Register	0x0000_0000
CLIP_LURIGHT	0x29C (VIP0)/ 0x29C (VIP1)	VIP Clipper Lu Right Register	0x0000_0000
CLIP_CRRIGHT	0x2A0 (VIP0)/ 0x2A0 (VIP1)	VIP Clipper Cr Right Register	0x0000_0000
CLIP_CBRIGHT	0x2A4 (VIP0)/ 0x2A4 (VIP1)	VIP Clipper Cb Right Register	0x0000_0000
CLIP_LUTOP	0x2A8 (VIP0)/ 0x2A8 (VIP1)	VIP Clipper Lu Top Register	0x0000_0000
CLIP_CRTOP	0x2AC (VIP0)/ 0x2AC (VIP1)	VIP Clipper Cr Top Register	0x0000_0000
CLIP_CBTOP	0x2B0 (VIP0)/ 0x2B0 (VIP1)	VIP Clipper Cb Top Register	0x0000_0000
CLIP_LUBOTTOM	0x2B4 (VIP0)/ 0x2B4 (VIP1)	VIP Clipper Lu Bottom Register	0x0000_0000
CLIP_CRBOTTOM	0x2B8 (VIP0)/ 0x2B8 (VIP1)	VIP Clipper Cr Bottom Register	0x0000_0000
CLIP_CBBOTTOM	0x2BC (VIP0)/ 0x2BC (VIP1)	VIP Clipper Cb Bottom Register	0x0000_0000

Register	Offset	Description	Reset Value
VIP_SCANMODE	0x2C0 (VIP0)/ 0x2C0 (VIP1)	VIP Scan Mode Register	0x0000_0000
CLIP_YUYVENB	0x2C4 (VIP0)/ 0x2C4 (VIP1)	VIP Clipper Linear YUYV Enable Register	0x0000_0000
CLIP_BASEADDRH	0x2C8 (VIP0)/ 0x2C8 (VIP1)	VIP Clipper Linear Base Address High Register	0x0000_0000
CLIP_BASEADDRL	0x2CC (VIP0)/ 0x2CC (VIP1)	VIP Clipper Linear Base Address Low Register	0x0000_0000
CLIP_STRIDEH	0x2D0 (VIP0)/ 0x2D0 (VIP1)	VIP Clipper Linear Stride High Register	0x0000_0000
CLIP_STRIDEL	0x2D4 (VIP0)/ 0x2D4 (VIP1)	VIP Clipper Linear Stride Low Register	0x0000_0000

39.7.1.1 VIP_CONFIG

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x00, 0x00, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	R	Reserved for future use.	6'b0
RSVD	[9]	RW	Reserved for future use. You have to write "0" only.	1'b0
EXTSYNCENB	[8]	RW	Specifies the use of external sync signals. 0 = Embedded Sync 1 = External Sync	1'b0
RSVD	[7:4]	R	Reserved for future use.	4'b0
DORDER	[3:2]	RW	Specifies the order of input video data. 00 = Cb, Y0, Cr, Y1 01 = Cr, Y1, Cb, Y0 10 = Y0, Cb, Y1, Cr 11 = Y1, Cr, Y0, Cb	2'b0
DWIDTH	[1]	RW	Specifies the bit-width of an input video signal 0 = 16-bit 1 = 8-bit	1'b0
VIPENB	[0]	RW	VIP Enable 0 = Disable 1 = Enable	1'b0

39.7.1.2 VIP_INTCTRL

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x04, 0x04, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	R	Reserved for future use.	6'b0
HSINTENB	[9]	RW	Specifies the generation of an interrupt when an HSYNC event occurs. HSYNC events occur at the end of the HSYNC pulse. 0 = Disable 1 = Enable	1'b0
VSINTENB	[8]	RW	Specifies the generation of an interrupt when a VSYNC event occurs. VSYNC events occur at the end of the VSYNC pulse. Therefore, the event occurs at every frame for Progressive input, and at every field for Interlace input. 0 = Disable 1 = Enable	1'b0
RSVD	[7:2]	R	Reserved for future use.	6'b0
HSINTPEND	[1]	RW	Indicates the Pending status of the HSYNC interrupt. This bit always works regardless of the setting of the HSINTENB bit. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0
VSINTPEND	[0]	RW	Indicates the Pending status of the VSYNC interrupt. This bit always works regardless of the setting of the VSINTENB bit. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0

39.7.1.3 VIP_SYNCCTRL

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x08, 0x08, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:10]	R	Reserved for future use.	6'b0
VSYNCPOL	[9]	RW	External Vertical Sync Polarity. 1'b0 = V Sync Polarity is Low Active 1'b1 = V Sync Polarity is High Active	1'b0
HSYNCPOL	[8]	RW	External Horizontal Sync Polarity. 1'b0 = H Sync Polarity is Low Active 1'b1 = H Sync Polarity is High Active	1'b0
RSVD	[7:6]	R	Reserved for future use.	2'b0
LASTFIELD	[5]	R	Indicates the status of the internal Field signal that is updated at every Frame Start (the start of vertical active video). For the operation of this bit, the PCLKMODE is set as "1". 0 = The last field is an odd field. 1 = The last field is an even field.	1'b0
DVALIDPOL (MIPI only)	[4]	RW	In case of MIPI, this bit should be set to 1'b1. Other case should be set to 1'b0.	1'b0
RSVD	[3]	RW	This bit should be set to 1'b0.	1'b0
EXTDVENB (MIPI only)	[2]	RW	In case of MIPI, this bit should be set to 1'b1. Other case should be set to 1'b0.	1'b0
FIELDSEL	[1:0]	RW	Selects a field signal. 00 = Bypass (Low is odd field) 01 = Invert (Low is even field) 10 = Fix 0 (odd field) 11 = Fix 1 (even field)	2'b0

39.7.1.4 VIP_SYNCMON

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x0C, 0x0C, Reset Value = 0x0000_0003

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved for future use.	14'bx
CURHSYNC	[1]	R	Indicates the status of the VSYNC created by the internal sync generator in Embedded Sync mode. This bit is valid only when the *EXTSYNCENB*is "0". 0 = Inactivate 1 = Activate	1'b1
CURVSYNC	[0]	R	Indicates the status of the VSYNC created by the internal sync generator in Embedded Sync mode. This bit is valid only when the *EXTSYNCENB*is "0". 0 = Inactivate 1 = Activate	1'b1

39.7.1.5 VIP_VBEGIN

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x10, 0x10, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
VBEGIN	[15:0]	RW	When the EXTSYNCENB is "1", this value is used for the creation of an internal vertical blank. This value specifies the number of lines in a section from the end of the vertical sync pulse to the end of the vertical blank. • VBEGIN = tVBP – 1 When the *EXTSYNCENB*is "0", this value is used for the creation of an internal vertical sync pulse. This value specifies the number of lines in a section from the start of the vertical blank to the start of the vertical sync pulse. • VBEGIN = tVFP + 1	16'b0

39.7.1.6 VIP_VEND

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x14, 0x14, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
VEND	[15:0]	RW	When the *EXTSYNCENB*is "1", this value is used for the creation of an internal vertical blank. This value specifies the number of lines in a section from the end of the vertical sync pulse to the start of the vertical blank. • VBEGIN = tVBP + tAVH – 1 When the *EXTSYNCENB*is "0", this value is used for the creation and the internal vertical sync pulse. This value specifies the number of lines in a section from the start of the vertical blank to the end of the vertical sync pulse. • VBEGIN = tVFP + tVSW + 1	16'b0

39.7.1.7 VIP_HBEGIN

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x18, 0x18, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
HBEGIN	[15:0]	RW	When the EXTSYNCENB is "1", this value is used for the creation of an internal horizontal blank. This value specifies the number of clocks in a section from the end of the horizontal sync pulse to the end of the horizontal blank. • HBEGIN = tHBP – 1 When the EXTSYNCENB is "0", this value is used for the creation of an internal horizontal sync pulse. This value specifies the number of clocks in a section from the start of the horizontal blank to the start of the horizontal sync pulse. • HBEGIN = tHFP – 7	16'b0

39.7.1.8 VIP_HEND

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x1C, 0x1C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
HEND	[15:0]	RW	When the EXTSYNCENB is "1", this value is used for the creation of an internal horizontal blank. This value specifies the number of clocks in a section from the end of the horizontal sync pulse to the start of the horizontal blank. • HBEGIN = tHBP + tAVW – 1 When the EXTSYNCENB is "0", this value is used for the creation of an internal horizontal sync pulse. This value specifies the number of clocks in a section from the start of the horizontal blank to the end of the horizontal sync pulse. • HBEGIN = tHFP + tHSW – 7	16'b0

39.7.1.9 VIP_FIFOCTRL

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x20, 0x20, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
FIFOWRENB	[11]	R	Indicates the data write status of the internal FIFO of the VIP. 0 = No write 1 = Writing	1'b0
FIFORDENB	[10]	R	Indicates the data read status of the internal FIFO of the VIP. 0 = No read 1 = Reading	1'b0
FIFOEMPTY	[9]	R	Indicates whether the internal FIFO of the VIP is empty or not. 0 = Not empty 1 = Empty	1'b1
FIFOFULL	[8]	R	Indicates whether the internal FIFO of the VIP is full or not. 0 = Not full 1 = Full	1'b0
RSVD	[7:3]	R	Reserved for future use.	5'b0
RESETFIFOSEL	[2:1]	RW	Controls the point at which the FIFO of the VIP is reset. 00 = Frame End (the end of the vertical sync pulse) 01 = Frame Start (the start of the vertical active video) 10 = RESETFIFO bit (Clear by user) 11 = ALL (Frame End or Frame Start or RESETFIFO bit)	2'b0
RESETFIFO	[0]	W	Resets the internal FIFO of the VIP. This bit should be reset as "0" after being set as "1", and it is valid only when the RESETFIFOSEL is "2" or "3". 0 = Release FIFO Reset 1 = Reset FIFO	1'b0

39.7.1.10 VIP_HCOUNT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x24, 0x24, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
HCOUNT	[15:0]	RW	Indicates the total number of clocks in the horizontal active video section. When EXTSYNCENB is "0", this value has "horizontal active video clocks + 4".	16'b0

39.7.1.11 VIP_VCOUNT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x28, 0x28, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
VCOUNT	[15:0]	RW	Indicates the total number of lines in the vertical active video section.	16'b0

39.7.1.12 VIP_CDENB

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x200, 0x200, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	R	Reserved for future use.	7'b0
SEPENB	[8]	RW	Enables/disables the Separator. 0 = Disable 1 = Enable	1'b0
RSVD	[7:2]	R	Reserved for future use.	6'b0
CLIPENB	[1]	RW	Enables/disables the memory writing function of the Clipper block. This bit is valid only when the SEPENB is "1". 0 = Disable 1 = Enable	1'b0
DECIENB	[0]	RW	Enables/disables the memory writing function of the Decimator block. This bit is valid only when the SEPENB is "1". 0 = Disable 1 = Enable	1'b0

39.7.1.13 VIP_ODINT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x204, 0x204, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:9]	R	Reserved for future use.	7'b0
ODINTENB	[8]	RW	Specifies the generation of an interrupt when the Clipper/Decimator complete a frame/field. 0 = Disable 1 = Enable	1'b0
RSVD	[7:1]	R	Reserved for future use.	7'b0
ODINTPEND	[0]	RW	Indicates the Pending status of Clipper & Decimator Operation Done events. This bit always operates regardless of the setting of the ODINTENB bit. Read: 0 = Not pended 1 = Pended Write: 0 = No affect 1 = Clear	1'b0

39.7.1.14 VIP_IMGWIDTH

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x208, 0x208, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
IMGWIDTH	[11:0]	RW	Specifies the width of input images in pixel units. When EXSYNCENB is "0", you have to set it as "image width + 2".	12'b0

39.7.1.15 VIP_IMGHEIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x20C, 0x20C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved for future use.	5'b0
IMGHEIGHT	[10:0]	RW	Specifies the height of input images in line units.	11'b0

39.7.1.16 CLIP_LEFT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x210, 0x210, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CLIPLEFT	[11:0]	RW	Specifies the X-coordinate on the top left corner of the area to be clipped, in pixels. The clipping width (CLIPRIGHT – CLIPLEFT) must be a multiple of 16.	12'b0

39.7.1.17 CLIP_RIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x214, 0x214, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CLIPRIGHT	[11:0]	RW	Specifies the X-coordinate on the bottom right corner of the area to be clipped, in pixels. It should have a greater value than the CLIPLEFT. The clipping width (CLIPRIGHT – CLIPLEFT) must be a multiple of 16.	12'b0

39.7.1.18 CLIP_TOP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x218, 0x218, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved for future use.	5'b0
CLIPTOP	[10:0]	RW	Specifies the Y-coordinate on the top left corner of the area to be clipped, in pixels. The clipping height (CLIPBOTTOM – CLIPTOP) must be an even number.	11'b0

39.7.1.19 CLIP_BOTTOM

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x21C, 0x21C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved for future use.	5'b0
CLIPBOTTOM	[10:0]	RW	Specifies the Y-coordinate on the bottom right corner of the area to be clipped, in pixels. It should have a greater value than the CLIPTOP. The clipping height (CLIPBOTTOM – CLIPTOP) must be an even number.	11'b0

39.7.1.20 DECI_TARGETW

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x220, 0x220, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
TARGETW	[11:0]	RW	Specifies the width of the Decimator output image, in pixels. The width of the output image should be narrower than that of the clipped input image and be a multiple of 16.	12'b0

39.7.1.21 DECI_TARGETH

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x224, 0x224, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved for future use.	5'b0
TARGETH	[10:0]	RW	Specifies the height of the Decimator output image, in lines. The height of the output image should be lower than that of the clipped input image and be an even number.	11'b0

39.7.1.22 DECI_DELTAW

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x228, 0x228, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
DELTAW	[11:0]	RW	Specifies the width difference between the input image and the output image of the Decimator in pixel units. • DELTAW = (CLIPRIGHT – CLIPLEFT) – TARGETW	12'b0

39.7.1.23 DECI_DELTAH

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x22C, 0x22C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved for future use.	5'b0
DELTAH	[10:0]	RW	Specifies the line difference between the input image and the output image of the Decimator in line units. • DELTAH = (CLIPBOTTOM – CLIPTOP) – TARGETH	11'b0

39.7.1.24 DECI_CLEARW

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x230, 0x230, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved for future use.	3'b0
CLEARW	[12:0]	RW	Specifies the difference between the width of the Decimator output image and the DELTAW in pixel units. This value has 2's complement format. • CLEARW = TARGETW – DELTAW	13'b0

39.7.1.25 DECI_CLEARH

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x234, 0x234, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CLEARH	[11:0]	RW	Specifies the difference between the height of the Decimator output image and the DELTAH in line units. This value has 2's complement format. • CLEARH = TARGETH – DELTAH	12'b0

39.7.1.26 DECI_LUSEG

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x238, 0x238, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved for future use.	8'b0
LUSEG	[7:0]	RW	Specifies the index of the segment where the output Y data of the Decimator is stored. This value has a Linear address [31:24].	8'b0

39.7.1.27 DECI_CRSEG

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x23C, 0x33C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved for future use.	8'b0
CRSEG	[7:0]	RW	Specifies the index of the segment where the output Cr data of the Decimator is stored. This value has a Linear address [31:24].	8'b0

39.7.1.28 DECI_CBSEG

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x240, 0x240, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved for future use.	8'b0
CBSEG	[7:0]	RW	Specifies the index of the segment where the output Cb data of the Decimator is stored. This value has a Linear address [31:24].	8'b0

39.7.1.29 DECI_FORMAT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x244, 0x244, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved for future use.	14'b0
FORMATSEL	[1:0]	RW	Specifies the output format of the Decimator. 00 = Separated YUV 4:2:0 01 = Separated YUV 4:2:2 10 = Separated YUV 4:4:4 11 = Reserved	2'b0

39.7.1.30 DECI_ROTFLIP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x248, 0x248, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved for future use.	13'b0
ROTATION	[2]	RW	Specifies whether to rotate the output image of Decimator 90 degree clockwise. 0 = Disable 1 = Enable	1'b0
VFLIP	[1]	RW	Specifies whether to flip the output image of Decimator vertically. 0 = Disable 1 = Enable	1'b0
HFLIP	[0]	RW	Specifies whether to flip the output image of Decimator horizontally. 0 = Disable 1 = Enable	1'b0

39.7.1.31 DECI_LULEFT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x24C, 0x24C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LULEFT	[11:0]	RW	Specifies the X-coordinate on the top left corner of the area in the segment where the output Y data of the Decimator is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.32 DECI_CRLEFT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x250, 0x250, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRLEFT	[11:0]	RW	Specifies the X-coordinate on the top left corner of the area in the segment where the output Cr data of the Decimator is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.33 DECI_CBLEFT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x254, 0x254, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBLEFT	[11:0]	RW	Specifies the X-coordinate on the top left corner of the area in the segment where the output Cb data of the Decimator is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.34 DECI_LURIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x258, 0x258, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LURIGHT	[11:0]	RW	Specifies the X-coordinate on the bottom right corner of the area in the segment where the output Y data of the Decimator is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.35 DECI_CRRIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x25C, 0x25C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRRIGHT	[11:0]	RW	Specifies the X-coordinate on the bottom right corner of the area in the segment where the output Cr data of the Decimator is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.36 DECI_CBRIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x260, 0x260, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBRIGHT	[11:0]	RW	Specifies the X-coordinate on the bottom right corner of the area in the segment where the output Cb data of the Decimator is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.37 DECI_LUTOP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x264, 0x264, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LUTOP	[11:0]	RW	Specifies the Y-coordinate on the top left corner of the area in the segment where the output Y data of the Decimator is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.38 DECI_CRTOP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x268, 0x268, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRTOP	[11:0]	RW	Specifies the Y-coordinate on the top left corner of the area in the segment where the output Cr data of the Decimator is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.39 DECI_CBTOP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x26C, 0x26C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBTOP	[11:0]	RW	Specifies the Y-coordinate on the top left corner of the area in the segment where the output Cb data of the Decimator is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.40 DECI_LUBOTTOM

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x270, 0x270, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LUBOTTOM	[11:0]	RW	Specifies the Y-coordinate on the bottom right corner of the area in the segment where the output Y data of the Decimator is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.41 DECI_CRBOTTOM

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x274, 0x274, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRBOTTOM	[11:0]	RW	Specifies the Y-coordinate on the bottom right corner of the area in the segment where the output Cr data of the Decimator is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.42 DECI_CBBOTTOM

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x278, 0x278, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBBOTTOM	[11:0]	RW	Specifies the Y-coordinate on the bottom right corner of the area in the segment where the output Cb data of the Decimator is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.43 CLIP_LUSEG

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x27C, 0x27C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved for future use.	8'b0
LUSEG	[7:0]	RW	Specifies the index of the segment where the output Y data of the Clipper is stored. This value has a Linear address [31:24].	8'b0

39.7.1.44 CLIP_CRSEG

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x280, 0x280, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved for future use.	8'b0
CRSEG	[7:0]	RW	Specifies the index of the segment where the output Cr data of the Clipper is stored. This value has a Linear address [31:24].	8'b0

39.7.1.45 CLIP_CBSEG

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x284, 0x284, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:8]	R	Reserved for future use.	8'b0
CBSEG	[7:0]	RW	Specifies the index of the segment where the output Cb data of the Clipper is stored. This value has a Linear address [31:24].	8'b0

39.7.1.46 CLIP_FORMAT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x288, 0x288, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved for future use.	14'b0
FORMATSEL	[1:0]	RW	Specifies the output format of the Clipper. 00 = Separated YUV 4:2:0 01 = Separated YUV 4:2:2 10 = Separated YUV 4:4;4 11 = Reserved	2'b0

39.7.1.47 CLIP_ROTFLIP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x28C, 0x28C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:3]	R	Reserved for future use.	13'b0
ROTATION	[2]	RW	Specifies whether to rotate the output image of Clipper 90 degree clockwise. When YUYVENB is "0", you have to disable the rotation function. 0 = Disable 1 = Enable	1'b0
VFLIP	[1]	RW	Specifies whether to flip the output image of Clipper vertically. 0 = Disable 1 = Enable	1'b0
HFLIP	[0]	RW	Specifies whether to flip the output image of Clipper horizontally. 0 = Disable 1 = Enable	1'b0

39.7.1.48 CLIP_LULEFT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x290, 0x290, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LULEFT	[11:0]	RW	Specifies the X-coordinate on the top left corner of the area in the segment where the output Y data of the Clipper is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.49 CLIP_CRLEFT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x294, 0x294, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRLEFT	[11:0]	RW	Specifies the X-coordinate on the top left corner of the area in the segment where the output Cr data of the Clipper is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.50 CLIP_CBLEFT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x298, 0x298, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBLEFT	[11:0]	RW	Specifies the X-coordinate on the top left corner of the area in the segment where the output Cb data of the Clipper is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.51 CLIP_LURIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x29C, 0x29C, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LURIGHT	[11:0]	RW	Specifies the X-coordinate on the bottom right corner of the area in the segment where the output Y data of the Clipper is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.52 CLIP_CRRIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2A0, 0x2A0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRRIGHT	[11:0]	RW	Specifies the X-coordinate on the bottom right corner of the area in the segment where the output Cr data of the Clipper is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.53 CLIP_CBRIGHT

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2A4, 0x2A4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBRIGHT	[11:0]	RW	Specifies the X-coordinate on the bottom right corner of the area in the segment where the output Cb data of the Clipper is stored. The X-coordinate should be a multiple of 8.	12'b0

39.7.1.54 CLIP_LUTOP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2A8, 0x2A8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LUTOP	[11:0]	RW	Specifies the Y-coordinate on the top left corner of the area in the segment where the output Y data of the Clipper is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.55 CLIP_CRTOP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2AC, 0x2AC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRTOP	[11:0]	RW	Specifies the Y-coordinate on the top left corner of the area in the segment where the output Cr data of the Clipper is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.56 CLIP_CBTOP

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2B0, 0x2B0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBTOP	[11:0]	RW	Specifies the Y-coordinate on the top left corner of the area in the segment where the output Cb data of the Clipper is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.57 CLIP_LUBOTTOM

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2B4, 0x2B4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
LUBOTTOM	[11:0]	RW	Specifies the Y-coordinate on the bottom right corner of the area in the segment where the output Y data of the Clipper is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.58 CLIP_CRBOTTOM

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2B8, 0x2B8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CRBOTTOM	[11:0]	RW	Specifies the Y-coordinate on the bottom right corner of the area in the segment where the output Cr data of the Clipper is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.59 CLIP_CBBOTTOM

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2BC, 0x2BC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:12]	R	Reserved for future use.	4'b0
CBBOTTOM	[11:0]	RW	Specifies the Y-coordinate on the bottom right corner of the area in the segment where the output Cb data of the Clipper is stored. The Y-coordinate should be a multiple of 8.	12'b0

39.7.1.60 VIP_SCANMODE

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2C0, 0x2C0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:2]	R	Reserved for future use.	14'b0
INTERLACEENB	[1]	RW	Specifies the scan mode of an input image. 0 = Progressive scan mode 1 = Interlace scan mode	1'b0
FIELDINV	[0]	RW	Specifies the polarity of the field signal transmitted from the VIP block to the Clipper and to the Decimator. 0 = Bypass (Low is odd field) 1 = Invert (Low is even field)	1'b0

39.7.1.61 CLIP_YUYVENB

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2C4, 0x2C4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:1]	R	Reserved for future use.	31'b0
YUYVENB	[0]	RW	Specifies the output format of the Clipper as the linear format or the separated format. 0 = Separated YUV format 1 = Linear YUV(YUYV) format	1'b0

39.7.1.62 CLIP_BASEADDRH

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2C8, 0x2C8, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
BASEADDRH	[15:0]	RW	Specifies the upper [31:16] of the base address where the linear YUV data of the Clipper is stored. In interlace scan mode, the address to store an even field image is calculated automatically. The value is used only when the YUYVENB is "1".	16'b0

39.7.1.63 CLIP_BASEADDRL

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2CC, 0x2CC, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
BASEADDRL	[15:0]	RW	Specifies the lower [15:0] of the base address where the linear YUV data of the Clipper is stored. This value must be a multiple of 8. In interface scan mode, the address to store an even field image is calculated automatically. The value is used only when the YUYVENB is "1".	16'b0

39.7.1.64 CLIP_STRIDEH

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2D0, 0x2D0, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
STRIDEH	[15:0]	RW	Specifies the Y data of the Clipper is stored. In general, the stride has the pixel width of a line. Since this value is automatically doubled in interlace scan mode, the value in progressive scan mode should be specified.	16'b0

39.7.1.65 CLIP_STRIDEL

- Base Address: 0xC006_4000 (VIP 0)
- Base Address: 0xC006_3000 (VIP 1)
- Address = Base Address + 0x2D4, 0x2D4, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved for future use.	16'bx
STRIDEL	[15:0]	RW	Specifies the CB-CR data of the Clipper is stored. In general, the stride has the pixel width of a line. Since this value is automatically doubled in interlace scan mode, the value in progressive scan mode should be specified.	16'b0

40 Multi-Format Video Codec

40.1 Overview

The multi format video codec (hereinafter referred to as "VPU") is a full HD multi-standard video IP for consumer multimedia products such as HDTVs, HD set-top boxes, and HD DVD players. It can decode compressed video in a format of H.264 BP/MP/HP, VC-1 SP/MP/AP, MPEG-1/2, MPEG-4 SP/ASP, H.263P3, VP8,Theora, AVS, RV-8/9/10, and JPEG (max. 8192 × 8192) It can also perform H.264, MPEG-4, and H.263 encoding up to Full-HD 1920 × 1088 (max. 8192 × 8192 JPEG) resolution. The VPU can perform simultaneous multiple real times encoding, decoding, or both encoding and decoding of different format video streams at multiple resolutions.

The VPU contains a 16-bit DSP called BIT processor. The BIT processor communicates with a host CPU through a host interface and controls the other sub-blocks of the VPU. The host CPU require slow resources under 1 MIPS, because all of the functions such as bit stream parsing, video hardware sub- blocks control and error resilience are implemented in the BIT processor. Moreover it is designed to optimally share most of the sub-blocks that are used in common for video processing, which contributes to the ultra low power and low gate count.

It is connected with a host CPU system via 32-bit AMBA 3 APB bus for system control and 128-bit AMBA3 AXI for data. There are two 128-bit AXI buses: primary and secondary. The secondary bus can be connected to on-chip memories to achieve high performance.

40.2 Functional Description

40.2.1 List of Video CODECs

The following table shows many different video standards supported by VPU.

Table 40-1 Supported Video Standards

	Standard	Profile	Level	Max. Resolution	Min. Resolution	Bitrate
Encoder	H.264	Baseline	4.0	1920 × 1088	96 × 16	20Mbps
	MPEG-4	SP	5/6	1920 × 1088	96 × 16	20Mbps
	H.263	Profile3	70	1920 × 1088	96 × 16	20Mbps
Decoder	H.264	BP/MP/HP	4.2	1920 × 1088	16 × 16	50Mbps
	MPEG-4	ASP		1920 × 1088	16 × 16	40Mbps
	H.263	Profile3		1920 × 1088	16 × 16	20Mbps
	VC-1	SP/MP/AP	3	1920 × 1088	16 × 16	45Mbps
	MPEG-1/2	MP	High	1920 × 1088	16 × 16	80Mbps
	VP8			1920 × 1088	16 × 16	20Mbps
	Theora			1280 × 720	16 × 16	20Mbps
	AVS	Jizhun	6.2	1920 × 1088	16 × 16	40Mbps
	RV	8/9/10		1920 × 1088	16 × 16	40Mbps
Encoder	MJPEG	Baseline		8192 × 8192	16 × 16	160Mpel/s atYUV422
Decoder	MJPEG	Baseline		1920 × 1088	16 × 16	120Mpel/s atYUV444

40.2.2 Supported Video Encoding Tools

H.264/AVC BP/CBP Encoder

- Compatible with the ITU-T Recommendation H.264 specification
- The encoder uses only one reference frame for the motion estimation.
- 1/4-pel accuracy motion estimation with programmable search range up to [±128, ±64]
- Search range is reconfigurable by SW
  - Horizontal (–128 to 127), Vertical (–64 to 63)
  - Horizontal (–64 to 63), Vertical (–32 to 31)
  - Horizontal (–32 to 31), Vertical (–16 to 15)
  - Horizontal (–16 to 15), Vertical (–16 to 15)
- 16 × 16, 16 × 8, 8 × 16 and 8 × 8 block sizes are supported.
- Available block sizes can be configurable.
- Intra-prediction
  - Luma I4 × 4 Mode: 9 modes
  - Luma I16 × 16 Mode: 3 modes (Vertical, Horizon, DC)
  - Chroma Mode: 3 modes (Vertical, Horizon, DC)
- Minimum encoding image size is 96 pixels in horizontal and 16 pixels in vertical.
- The encoder supports the following error resilience tools: video packet (fixed number of bits, and fixed number of macro blocks), CIR (Cyclic Intra Refresh), and multi-slice structure.
- FMO/ASO tool of H.264 is not supported.
- The encoder rate control is configurable for low-delay and long-delay, and configurable from macro block-level rate control to frame-level rate control.
- Field encoding is available without PAFF, MBAFF.

MPEG4-SP Encoder

- Compatible with the ISO/IEC 14496-2 specification
- MV with unrestricted motion vector
- AC/DC prediction
- 1/2-pel accuracy motion estimation with search range up to [±128, ±64]
- Search range is reconfigurable by SW
  - Horizontal (–128 to 127), Vertical (–64 to 63)
  - Horizontal (–64 to 63), Vertical (–32 to 31)
  - Horizontal (–32 to 31), Vertical (–16 to 15)
  - Horizontal (–16 to 15), Vertical (–16 to 15)
- Error resilience tools such as re-sync marker, data-partitioning with reversible VLC.

H.263 P0/P3 (Interactive and Streaming Wireless Profile) Encoder

- MV with unrestricted motion vector mode compliant to Annex D
- Search range is –16 to 15 in horizontal and –16 to 15 in vertical
- H.263 Baseline profile + Annex J, K (RS = 0 and ASO = 0), and T

40.2.3 Supported Video Decoding Tools

H.264/AVC Decoder

- Fully compatible with the ITU-T Recommendation H.264 specification in BP, MP and HP.
- Supports MVC Stereo High profile
- Supports CABAC/CAVLC
- Variable block size (16 × 16, 16 × 8, 8 × 16, 8 × 8, 8 × 4, 4 × 8 and 4 × 4)
- Error detection, concealment and error resilience tools with FMO/ASO support

VC-1/WMV-9 Decoder

- Supports all VC-1 profile features - SMPTE Proposed SMPTE Standard for Television: VC-1 Compressed
- Video Bit stream format and Decoding Process
- Supports Simple/Main/Advanced Profile
- Supports multi-resolution (Dynamic resolution) without scaling that returns related information

MPEG-4 Decoder

- Fully compatible with the ISO/IEC 14496-2 specification in SP/ASP except GMC(Global motion compensation)
- Full XviD compatibility
- Support for short video header

Sorenson Spark Decoder

- Fully compatible with Sorenson Spark decoder specification

H.263 V2 (Interactive and Streaming Wireless Profile, Profile 3) Decoder

- H.263 Baseline profile + Annex I, J, K (except RS/ASO), and T

MPEG-1/MPEG-2

- Fully compatible with ISO/IEC 13818-2 MPEG2 specification in Main Profile
- Support I, P and B frame
- Support field coded picture (interlaced) and fame coded picture

AVS Decoder

- Supports Jizhun profile level 6.2 (exclude 422 case)

Real Video 10 Decoder

- Fully compatible with RV-8/9/10 except re-sampling feature
- Minimum decoding size is 32 × 32 pixels.

VP8 Decoder

- Fully compatible with VP8 decoder specification
- Supporting both simple and normal in-loop de-blocking

Theora Decoder

- Fully compatible with Theora decoder specification

40.2.4 Supported JPEG Tools

MJPEG Baseline Process Encoder and Decoder

- Baseline ISO/IEC 10918-1 JPEG compliance
- Support 1 or 3 color components
- 3 component in a scan (interleaved only)
- 8-bit samples for each component
- Support 4:2:0, 4:2:2, 2:2:4, 4:4:4 and 4:0:0 color format (max. six 8 × 8 blocks in one MCU)
- Minimum encoding size is 16 × 16 pixels.

40.2.5 Non-codec related features

Value Added Features

- De-ringing (MPEG-2/4 only), rotator/mirroring
- Built-in de-blocking filter for MPEG-2/MPEG-4
- Pre/Post rotator/mirror

Programmability

- The VPU embeds 16-bit DSP processor dedicated to processing bit stream and controlling their video hardware.
- General purpose registers and interrupt for communication between a host processor and the video IP

Optimal External Memory Accesses

- Configurable frame buffer formats (linear or tiled) for longer burst-length
- 2D cache for motion estimation and compensation to reduce external memory accesses
- Secondary AXI port for on-chip memory to enhance performance

41 3D Graphic Engine

41.1 Overview

S5P4418 has powerful 3D GPU engine. 3D GPU is a hardware accelerator for 2D and 3D graphics systems.

The GPU consist of:

- Two Pixel Processors (PPs)
- A Geometry Processor (GP)
- A 32 Kbyte Level 2 Cache (L2)
- A Memory Management Unit (MMU) for each GP and PP
- A Power Management Unit (PMU).

The GPU and its associated software is compatible with the following graphics standards:

- OpenGL ES 2.0
- OpenGL ES 1.1
- OpenVG 1.1.

41.2 Features

41.2.1 Pixel Processor Features

The pixel processor features are:

- Each pixel processor used processes a different tile, enabling a faster turnaround
- Programmable fragment shader
- Alpha blending
- Complete non-power-of-2 texture support
- Cube mapping
- Fast dynamic branching
- Fast trigonometric functions, including arctangent
- Full floating-point arithmetic
- Frame buffer blend with destination Alpha
- Indexable texture samplers
- Line, quad, triangle and point sprites
- No limit on program length
- Perspective correct texturing
- Point sampling, bilinear, and tri-linear filtering
- Programmable mipmap level-of-detail biasing and replacement
- Stencil buffering, 8-bit
- Two-sided stencil
- Unlimited dependent texture reads
- 4-level hierarchical Z and stencil operations
- Up to 512 times Full Scene Anti-Aliasing (FSAA). 4x multisampling times 128x supersampling
- 4-bit per texel compressed texture format

41.2.2 Geometry Processor Features

The geometry processor features are:

- Programmable vertex shader
- Flexible input and output formats
- Autonomous operation tile list generation
- Indexed and non-indexed geometry input
- Primitive constructions with points, lines, triangles and quads.

41.2.3 Level 2 Cache Controller Features

The L2 cache controller features are:

- 32KB 4-way set-associative
- Supports up to 32 outstanding AXI transactions
- Implements a standard pseudo-LRU algorithm
- Cache line and line fill burst size is 64 bytes
- Supports eight to 64 bytes un-cached read bursts and write bursts
- 128-bit interface to memory sub-system
- Support for hit-under-miss and miss-under-miss with the only limitation of AXI ordering rules

41.2.4 MMU

The MMU features are:

- Accesses control registers through the bus infrastructure to configure the memory system
- Each processor has its own MMU to control and translate memory accesses that the GPU initiates

41.2.5 PMU

The PMU features are:

- Programmable power management
- Powers up and down each GP, PP and Level 2 cache controller separately
- Controls the clock, isolation and power of each device
- Provides an interrupt when all requested devices are powered up

41.3 Operation

41.3.1 Clock

The S5P4418 has a clock for 3D GPU. The operation frequency can be up to 333MHz. See the system controller and clock controller for setting up the 3D GPU clock.

41.3.2 Reset

The S5P4418 has a reset for 3D GPU. See the reset controller for setting up the 3D GPU reset.

41.3.3 Interrupt

The S5P4418 has an interrupt number for 3D GPU. See the interrupt controller for setting up the 3D GPU interrupt.

42 Crypto Engine

42.1 Overview

Crypto Engine block executes AES, DES, HASH Encryption and Decryption.

42.2 Features

- Big-endian Encryption & Decryption
- Supports DMA Interface
- Supports AES ECB, CBC, CTR -128, 192, 256 Mode
- Supports DES ECB, CBC -64 Mode
- Supports 3DES -64 Mode
- Supports HASH Mode (SHA1, MD5)
- Supports input share Mode (AES & HASH)
- Supports AES and HASH working at the same time (Refer *Figure 42-2*)

42.3 Block Diagram

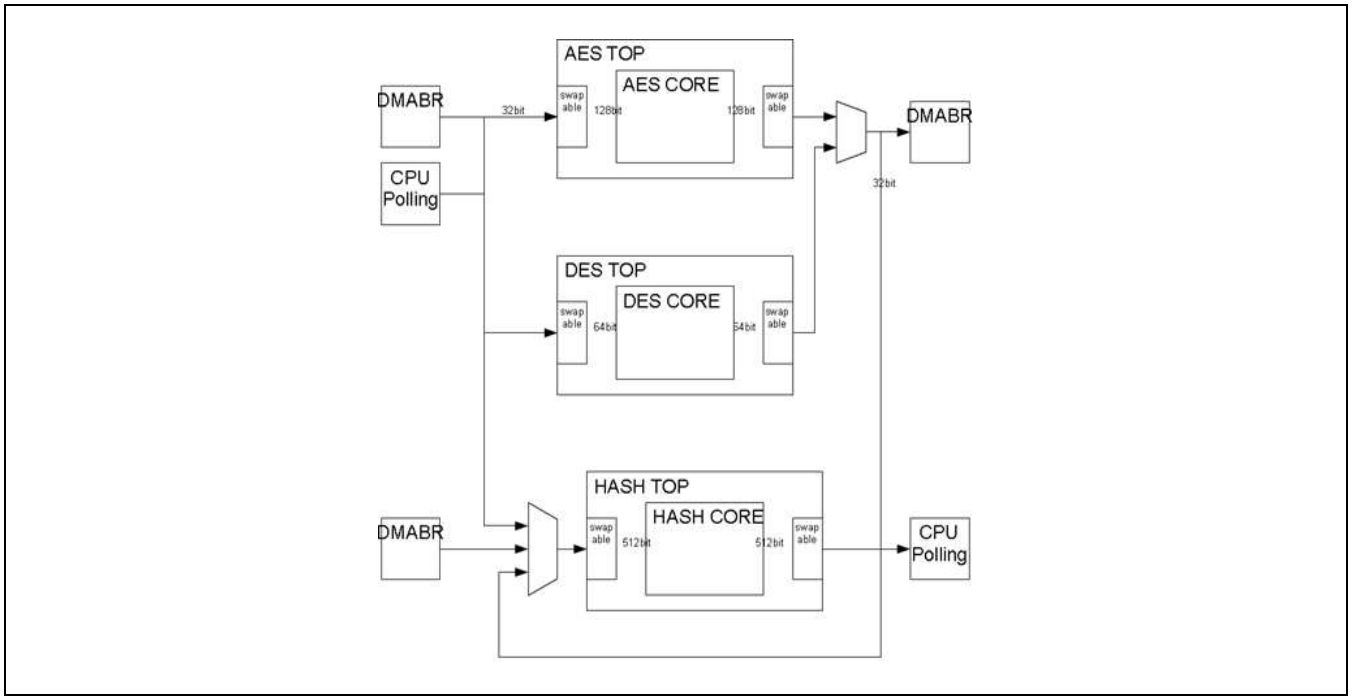


Figure 42-1 CRYPTO Block Diagram

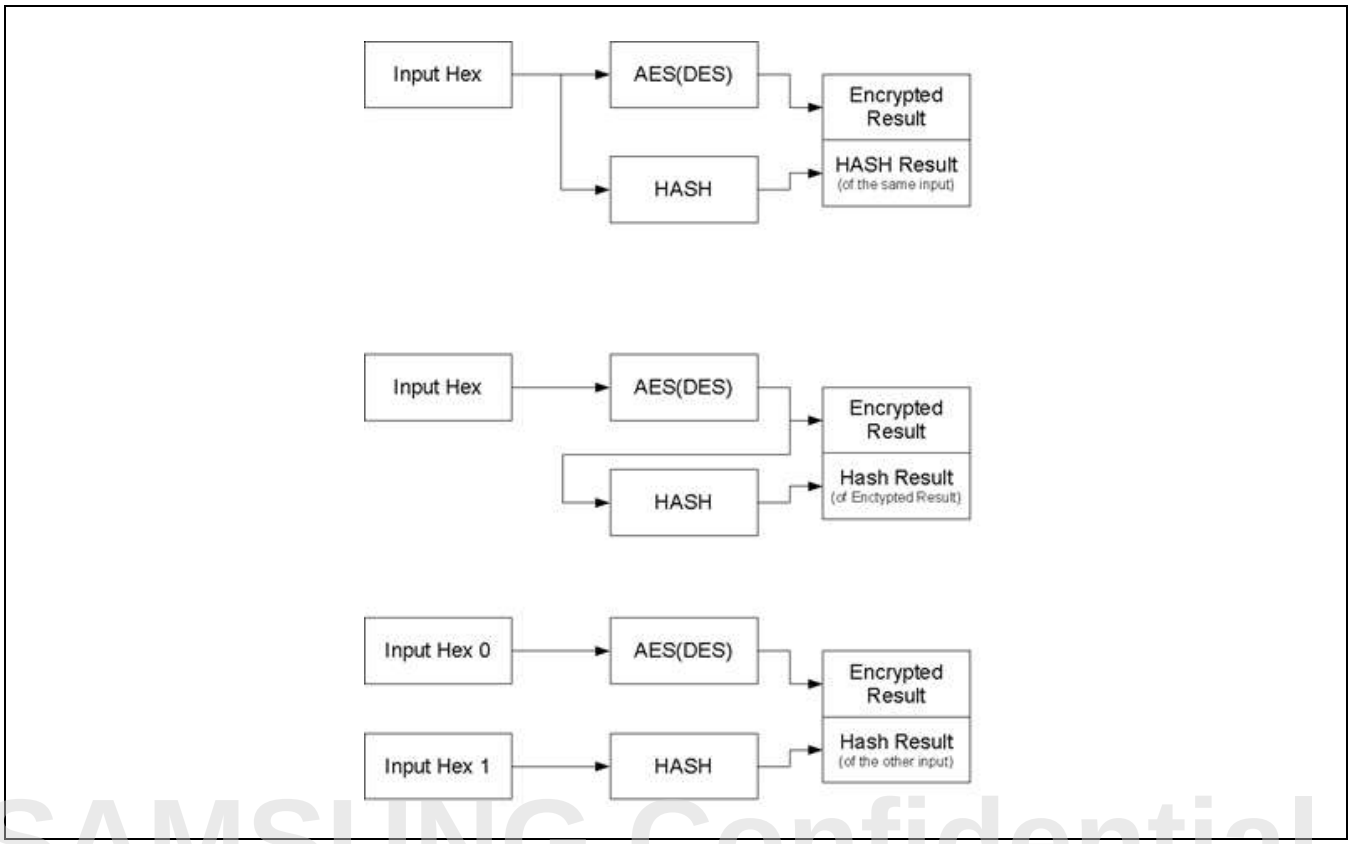


Figure 42-2 CRYPTOAES & HASH Operation Scenario

42.4 Functional Description

42.4.1 Polling Mode

In polling mode, CPU can write/read the register directly.

Access Sequence:

1. Set AES Key
2. Set Initial Vector and Set CPU_AES_LOADCNT with 1
3. Set AES_TESTIN
4. Set AES Control Register & Enable
5. Set CPU_AES_LOADCNT with 0
6. Set IDLC_ANNY WITH 1 (AES_START)
7. WAIT FOR IDLE_AES=1
8. Get Result Vector

42.4.2 Mode

In Channel DMA mode, users need to DMA Mode Enable.

42.5 Register Description

42.5.1 Register Map Summary

- Base Address: 0xC001_5000

Register	Offset	Description	Reset Value
CRT_CTRL0	0x00h	CRYPTO Control register	0x0000_0000
AES_CTRL0	0x0Ch	CRYPTO AES Control register	0x0000_0000
AES_iv0	0x10h	CRYPTO AES INIT vector register 0	0x0000_0000
AES_iv1	0x14h	CRYPTO AES INIT vector register 1	0x0000_0000
AES_iv2	0x18h	CRYPTO AES INIT vector register 2	0x0000_0000
AES_iv3	0x1Ch	CRYPTO AES INIT vector register 3	0x0000_0000
AES_key0	0x30h	CRYPTO AES key register 0	0x0000_0000
AES_key1	0x34h	CRYPTO AES key register 1	0x0000_0000
AES_key2	0x38h	CRYPTO AES key register 2	0x0000_0000
AES_key3	0x3Ch	CRYPTO AES key register 3	0x0000_0000
AES_key4	0x40h	CRYPTO AES key register 4	0x0000_0000
AES_key5	0x44h	CRYPTO AES key register 5	0x0000_0000
AES_key6	0x48h	CRYPTO AES key register 6	0x0000_0000
AES_key7	0x4Ch	CRYPTO AES key register 7	0x0000_0000
AES_TEXTIN0	0x50h	CRYPTO AES TEXTIN register 0	0x0000_0000
AES_TEXTIN1	0x54h	CRYPTO AES TEXTIN register 1	0x0000_0000
AES_TEXTIN2	0x58h	CRYPTO AES TEXTIN register 2	0x0000_0000
AES_TEXTIN3	0x5Ch	CRYPTO AES TEXTIN register 3	0x0000_0000
AES_TEXTOUT0	0x60h	CRYPTO AES TEXTOUT register 0	0x0000_0000
AES_TEXTOUT1	0x64h	CRYPTO AES TEXTOUT register 1	0x0000_0000
AES_TEXTOUT2	0x68h	CRYPTO AES TEXTOUT register 2	0x0000_0000
AES_TEXTOUT3	0x6Ch	CRYPTO AES TEXTOUT register 3	0x0000_0000
DES_CTRL0	0x70h	CRYPTO DES Control register	0x0000_0000
DES_iv0	0x74h	CRYPTO DES INIT vector register 0	0x0000_0000
DES_iv1	0x78h	CRYPTO DES INIT vector register 1	0x0000_0000
DES_KEY0_0	0x7Ch	CRYPTO DES KEY register 0_0	0x0000_0000
DES_KEY0_1	0x80h	CRYPTO DES KEY register 0_1	0x0000_0000
DES_KEY1_0	0x84h	CRYPTO DES KEY register 1_0	0x0000_0000
DES_KEY1_1	0x88h	CRYPTO DES KEY register 1_1	0x0000_0000
DES_KEY2_0	0x8Ch	CRYPTO DES KEY register 2_0	0x0000_0000
DES_KEY2_1	0x90h	CRYPTO DES KEY register 2_1	0x0000_0000
DES_TEXTIN0	0x94h	CRYPTO DES TEXTIN register	0x0000_0000
DES_TEXTIN1	0x98h	CRYPTO DES TEXTIN register 1	0x0000_0000

Register	Offset	Description	Reset Value
DES_TEXTOUT0	0x9Ch	CRYPTO DES TEXTOUT register 0	0x0000_0000
DES_TEXTOUT1	0xA0h	CRYPTO DES TEXTOUT register 1	0x0000_0000
BDMAR	0xA4h	CRYPTO DMA BDMAR register	0x0000_0000
BDMAW	0xA8h	CRYPTO DMA BDMAW register	0x0000_0000
HDMAR	0xACh	CRYPTO DMA HDMAR register	0x0000_0000
HASH_CTRL0	0xB0h	CRYPTO HASH Control register 0	0x0000_0000
HASH_iv0	0xB4h	CRYPTO HASH INIT TABLE register 0	0x0000_0000
HASH_iv1	0xB8h	CRYPTO HASH INIT table register 1	0x0000_0000
HASH_iv2	0xBCh	CRYPTO HASH INIT table register 2	0x0000_0000
HASH_iv3	0xC0h	CRYPTO HASH INIT table register 3	0x0000_0000
HASH_iv4	0xC4h	CRYPTO HASH INIT table register 4	0x0000_0000
HASH_TEXTOUT0	0xC8h	CRYPTO HASH TEXTOUT register 0	0x0000_0000
HASH_TEXTOUT1	0xCCh	CRYPTO HASH TEXTOUT register 1	0x0000_0000
HASH_TEXTOUT2	0xD0h	CRYPTO HASH TEXTOUT register 2	0x0000_0000
HASH_TEXTOUT3	0xD4h	CRYPTO HASH TEXTOUT register 3	0x0000_0000
HASH_TEXTOUT4	0xD8h	CRYPTO HASH TEXTOUT register 4	0x0000_0000
HASH_TEXTIN	0xDCh	CRYPTO HASH TEXTIN register 0	0x0000_0000
HASH_MSG_SIZE	0xE0h	CRYPTO HASH TMSG SIZE register 0	0x0000_0000
HASH_MSG_SIZE	0xE4h	CRYPTO HASH TMSG SIZE register 1	0x0000_0000

42.5.1.1 CRT_CTRL0

- Base Address: 0xC001_5000
- Address = Base Address + 0x00h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved	21'b0
CPU_INT_ENB	[10]	RW	Enable the Interrupt 0 = Disable 1 = Enable	1'b0
CPU_INT_MASK	[9]	RW	Masking the Interrupt 0 = Masked 1 = Not Masked	1'b0
CPU_DMAW_SRC	[8]	RW	Specifies the DMA En/Decryption Mode 0 = AES 1 = DES	1'b0
IDLE_HASHCORE	[7]	R	Indicates the HASH CORE is Idle 0 = Not Idle 1 = Idle	1'b0
RSVD	[6]	R	Reserved	1'b0
INTPEND	[5]	RW	Read: Interrupt Pending Bit Write 1: Interrupt Pending Clear	1'b0
CPU_DES_LOADCNT	[4]	W	Users must this bit to 1 after users set the DES Initial Value.	-
CPU_AES_LOADCNT	[3]	W	Users must this bit to 1 after users set the AES Initial Value.	-
IDLE_HASH	[2]	RW	Indicates the HASH is Idle Write 1: HASH Start	1'b0
IDLE_DES	[1]	RW	Indicates the DES is Idle Write 1: DES Start	1'b0
IDLE_AES	[0]	RW	Indicates the AES is Idle Write 1: AES Start	1'b0

42.5.1.2 AES_CTRL0

- Base Address: 0xC001_5000
- Address = Base Address + 0x0Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:16]	R	Reserved	16'b0
AES_SELKEY	[15]	RW	Select the AES KEY Mode 0 = CPU configuration 1 = ECID AESKEY	1'b0
RSVD	[14:10]	R	Reserved	5'b0
AES_SWAPOUT	[9]	RW	Enable the AES Output Swap 0 = Not Swap 1 = Masked	1'b0
AES_SWAPIN	[8]	RW	Enable the AES Input Swap 0 = Not Swap 1 = Masked	1'b0
AES_BLKMODE	[7:6]	RW	Specifies the AES Block Mode 0 = ECB 1 = CBC 2 = CTR 3 = Reserved	2'b0
AES_MODE	[5:4]	RW	Specifies the AES bit Mode 0 = 128-bit 1 = 192-bit 2 = 256-bit 3 = Reserved	2'b0
AES_128CNT	[3]	RW	Enable the AES 128-bit Counter	1'b0
AES_DMAMODE	[2]	RW	Enable the AES DMA Interface 0 = Disable 1 = Enable	1'b0
AES_ENC	[1]	RW	Specifies the AES Encoding Mode (Encryption/Decryption) 0 = Decryption 1 = Modulation	1'b0
AES_ENB	[0]	RW	Enable the AES Mode 0 = Disable 1 = Enable	1'b0

42.5.1.3 AES_iv0

- Base Address: 0xC001_5000
- Address = Base Address + 0x10h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_IV[127:96]. AES Initial vector	32'b0

42.5.1.4 AES_iv1

- Base Address: 0xC001_5000
- Address = Base Address + 0x14h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_IV[95:64]. AES Initial vector	32'b0

42.5.1.5 AES_iv2

- Base Address: 0xC001_5000
- Address = Base Address + 0x18h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_IV[63:32]. AES Initial vector	32'b0

42.5.1.6 AES_iv3

- Base Address: 0xC001_5000
- Address = Base Address + 0x1Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_IV[31:0]. AES Initial vector	32'b0

42.5.1.7 AES_key0

- Base Address: 0xC001_5000
- Address = Base Address + 0x30h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[255:224]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.8 AES_key1

- Base Address: 0xC001_5000
- Address = Base Address + 0x34h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[223:192]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.9 AES_key2

- Base Address: 0xC001_000
- Address = Base Address + 0x38h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[192:160]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.10 AES_key3

- Base Address: 0xC001_5000
- Address = Base Address + 0x3Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[159:128]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.11 AES_key4

- Base Address: 0xC001_5000
- Address = Base Address + 0x40h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[127:96]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.12 AES_key5

- Base Address: 0xC001_5000
- Address = Base Address + 0x44h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[95:64]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.13 AES_key6

- Base Address: 0xC001_5000
- Address = Base Address + 0x48h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[63:32]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.14 AES_key7

- Base Address: 0xC001_5000
- Address = Base Address + 0x4Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_AES_IV	[31:0]	RW	O_CPU_AES_key[31:0]. AES Key (AES_SELKEY = 0*)*	32'b0

42.5.1.15 AES_TEXTIN0

- Base Address: 0xC001_5000
- Address = Base Address + 0x50h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTIN	[31:0]	RW	CPU_AES_TESTIN[127:96]. AES Input Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.16 AES_TEXTIN1

- Base Address: 0xC001_5000
- Address = Base Address + 0x54h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTIN	[31:0]	RW	CPU_AES_TESTIN[95:64]. AES Input Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.17 AES_TEXTIN2

- Base Address: 0xC001_5000
- Address = Base Address + 0x58h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTIN	[31:0]	RW	CPU_AES_TESTIN[63:32]. AES Input Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.18 AES_TEXTIN3

- Base Address: 0xC001_5000
- Address = Base Address + 0x5Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTIN	[31:0]	RW	CPU_AES_TESTIN[31:0]. AES Input Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.19 AES_TEXTOUT0

- Base Address: 0xC001_5000
- Address = Base Address + 0x60h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTOUT	[31:0]	RW	CPU_AES_TESTOUT[127:96]. AES Result Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.20 AES_TEXTOUT1

- Base Address: 0xC001_5000
- Address = Base Address + 0x64h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTOUT	[31:0]	RW	CPU_AES_TESTOUT[95:64]. AES Result Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.21 AES_TEXTOUT2

- Base Address: 0xC001_5000
- Address = Base Address + 0x68h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTOUT	[31:0]	RW	CPU_AES_TESTOUT[63:32]. AES Result Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.22 AES_TEXTOUT3

- Base Address: 0xC001_5000
- Address = Base Address + 0x6Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_AES_TEXTOUT	[31:0]	RW	CPU_AES_TESTOUT[31:0]. AES Result Vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.23 DES_CTRL0

- Base Address: 0xC001_5000
- Address = Base Address + 0x70h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:11]	R	Reserved	21'b0
DES_TMODE	[10:8]	RW	3DES Mode Setting [8]: 1st stage Mode 0 = Decoding 1 = Encoding [9]: 2nd stage Mode 0 = Decoding 1 = Encoding [10]: 3th stage Mode 0 = Decoding 1 = Encoding	3'b0
RSVD	[7]	R	Reserved	1'b0
DES_SWAPOUT	[6]	RW	Enable the DES Output Swap 0 = Not Swap 1 = Masked	1'b0
DES_SWAPIN	[5]	RW	Enable the DES Input Swap 0 = Not Swap 1 = Masked	1'b0
DES_BLKMODE	[4]	RW	Specifies the DES Block Mode 0 = ECB 1 = CBC	1'b0
DES_DMAMODE	[3]	RW	Enable the DES DMA Interface 0 = Disable 1 = Enable	1'b0
DES_MODE	[2]	RW	Specifies the DES Mode 0 = DES 1 = 3DES	1'b0
DES_ENC	[1]	RW	Specifies the DES Encoding Mode (Encryption/Decryption) 0 = Decryption 1 = Modulation	1'b0
DES_ENB	[0]	RW	Enable the DES Mode 0 = Disable 1 = Enable	1'b0

42.5.1.24 DES_iv0

- Base Address: 0xC001_5000
- Address = Base Address + 0x74h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_IV	[31:0]	RW	O_CPU_DES_IV[63:32]. DES Initial vector	32'b0

42.5.1.25 DES_iv1

- Base Address: 0xC001_0000
- Address = Base Address + 5078h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_IV	[31:0]	RW	O_CPU_DES_IV[31:0]. DES Initial vector	32'b0

42.5.1.26 DES_KEY0_0

- Base Address: 0xC001_0000
- Address = Base Address + 507Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_KEY0	[31:0]	RW	O_CPU_DES_KEY0[63:32]. DES Key (DES and 1st stage of 3DES)	32'b0

42.5.1.27 DES_KEY0_1

- Base Address: 0xC001_0000
- Address = Base Address + 5080h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_KEY0	[31:0]	RW	O_CPU_DES_KEY0[31:0]. DES Key (DES and 1st stage of 3DES)	32'b0

42.5.1.28 DES_KEY1_0

- Base Address: 0xC001_5000
- Address = Base Address + 0x84h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_KEY1	[31:0]	RW	O_CPU_DES_KEY1[63:32]. DES Key (2nd stage of 3DES)	32'b0

42.5.1.29 DES_KEY1_1

- Base Address: 0xC001_5000
- Address = Base Address + 0x88h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_KEY1	[31:0]	RW	O_CPU_DES_KEY1[31:0]. DES Key (2nd stage of 3DES)	32'b0

42.5.1.30 DES_KEY2_0

- Base Address: 0xC001_5000
- Address = Base Address + 0x8Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_KEY2	[31:0]	RW	O_CPU_DES_KEY2[63:32]. DES Key (3th stage of 3DES)	32'b0

42.5.1.31 DES_KEY2_1

- Base Address: 0xC001_5000
- Address = Base Address + 0x90h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_DES_KEY2	[31:0]	RW	O_CPU_DES_KEY2[31:0]. DES Key (3th stage of 3DES)	32'b0

42.5.1.32 DES_TEXTIN0

- Base Address: 0xC001_5000
- Address = Base Address + 0x94h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_DES_TESTIN	[31:0]	RW	CPU_DES_TESTIN[63:32]. DES Input vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.33 DES_TEXTIN1

- Base Address: 0xC001_5000
- Address = Base Address + 0x98h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_DES_TESTIN	[31:0]	RW	CPU_DES_TESTIN[31:0]. DES Input vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.34 DES_TEXTOUT0

- Base Address: 0xC001_5000
- Address = Base Address + 0x9Ch, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_DES_TESTOUT	[31:0]	RW	CPU_DES_TESTOUT[63:32]. DES Input vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.35 DES_TEXTOUT1

- Base Address: 0xC001_5000
- Address = Base Address + 0xA0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_DES_TESTOUT	[31:0]	RW	CPU_DES_TESTOUT [31:0]. DES Input vector in PIO mode (Not DMA Mode)	32'b0

42.5.1.36 BDMAR

- Base Address: 0xC001_5000
- Address = Base Address + 0xA4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
REG_CRT_BDMAR	[31:0]	W	DMA Access registers for AES, DES Input Vectors.	

42.5.1.37 BDMAW

- Base Address: 0xC001_5000
- Address = Base Address + 0xA8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
REG_CRT_BDMAW	[31:0]	R	DMA Access registers for AES, DES Output Vectors. (Result Vector)	

42.5.1.38 HDMAR

- Base Address: 0xC001_5000
- Address = Base Address + 0xACh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
REG_CRT_BDMAR	[31:0]	W	DMA Access register for HASH Input Vectors	

42.5.1.39 HASH_CTRL0

- Base Address: 0xC001_5000
- Address = Base Address + 0xB0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
RSVD	[31:7]	R	Reserved	25'b0
HASH_INSRC	[6:5]	RW	Specifies the Input of HASH 0 = AES input share 1 = DES input share 2 = HRDMA 3 = BWDMA	3'b0
HASH_SWAPIN	[4]	RW	Enable the HASH Input Swap 0 = Not Swap 1 = Masked	1'b0
HASH_MODE	[3]	RW	Specifies the HASH Mode 0 = SHA1 1 = MD5	1'b0
RSVD	[2]	R	Reserved	1'b0
HASH_DMAMODE	[1]	RW	Enable the HASH DMA Interface 0 = Disable 1 = Enable	1'b0
HASH_ENB	[0]	RW	Enable the HASH Mode 0 = Disable 1 = Enable	1'b0

42.5.1.40 HASH_iv0

- Base Address: 0xC001_5000
- Address = Base Address + 0xB4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_HASH_IV	[31:0]	RW	O_CPU_HASH_IV[159:128]. HASH Initial table	32'b0

42.5.1.41 HASH_iv1

- Base Address: 0xC001_5000
- Address = Base Address + 0xB8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_HASH_IV	[31:0]	RW	O_CPU_HASH_IV[127:96]. HASH Initial table	32'b0

42.5.1.42 HASH_iv2

- Base Address: 0xC001_5000
- Address = Base Address + 0xBCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_HASH_IV	[31:0]	RW	O_CPU_HASH_IV[95:64]. HASH Initial table	32'b0

42.5.1.43 HASH_iv3

- Base Address: 0xC001_5000
- Address = Base Address + 0xC0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_HASH_IV	[31:0]	RW	O_CPU_HASH_IV[63:32]. HASH Initial table	32'b0

42.5.1.44 HASH_iv4

- Base Address: 0xC001_5000
- Address = Base Address + 0xC4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
o_CPU_HASH_IV	[31:0]	RW	O_CPU_HASH_IV[31:0]. HASH Initial table	32'b0

42.5.1.45 HASH_TEXTOUT0

- Base Address: 0xC001_5000
- Address = Base Address + 0xC8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_TEXTOUT	[31:0]	RW	CPU_HASH_TESTOUT[159:128]. HASH result output	32'b0

42.5.1.46 HASH_TEXTOUT1

- Base Address: 0xC001_5000
- Address = Base Address + 0xCCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_TEXTOUT	[31:0]	RW	CPU_HASH_TESTOUT[127:96]. HASH result output	32'b0

42.5.1.47 HASH_TEXTOUT2

- Base Address: 0xC001_5000
- Address = Base Address + 0xD0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_TEXTOUT	[31:0]	RW	CPU_HASH_TESTOUT[96:64]. HASH result output	32'b0

42.5.1.48 HASH_TEXTOUT3

- Base Address: 0xC001_5000
- Address = Base Address + 0xD4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_TEXTOUT	[31:0]	RW	CPU_HASH_TESTOUT[63:32]. HASH result output	32'b0

42.5.1.49 HASH_TEXTOUT4

- Base Address: 0xC001_5000
- Address = Base Address + 0xD8h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_TEXTOUT	[31:0]	RW	CPU_HASH_TESTOUT[31:0]. HASH result output	32'b0

42.5.1.50 HASH_TEXTIN

- Base Address: 0xC001_5000
- Address = Base Address + 0xDCh, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_TEXTIN	[31:0]	RW	CPU_HASH_TESTIN[127:0]. For DMA and PIO mode	32'b0

42.5.1.51 HASH_MSG_SIZE

- Base Address: 0xC001_5000
- Address = Base Address + 0xE0h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_MSGSIZE	[31:0]	RW	CPU_HASH_MSGSIZE[63:32]. HASH result output	32'b0

42.5.1.52 HASH_MSG_SIZE

- Base Address: 0xC001_5000
- Address = Base Address + 0xE4h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
CPU_hash_MSGSIZE	[31:0]	RW	CPU_HASH_MSGSIZE[31:0]. HASH result output	32'b0

43 Electrical Characteristics

43.1 Absolute Maximum Ratings

Table 43-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Min.	Max.	Unit
DC Supply Voltage	VDD	1.0V VDD	–0.5	1.5	V
		1.8V VDD	–0.5	2.5	V
		1.5V VDD	–0.5	3.6	V
		3.3V VDD	–0.5	3.8	V
DC Input Voltage	VIN	1.8V Input Buffer	–0.5	2.5	V
		2.5V Input Buffer	–0.5	3.6	V
		3.3V Input Buffer	–0.5	3.8	V
DC Output Voltage	VOUT	1.8V Output Buffer	–0.5	2.5	V
		2.5V Output Buffer	–0.5	3.6	V
		3.3V Output Buffer	–0.5	3.8	V
DC In/Out Current	Iinout	–	–20	20	mA
Storage Temperature	Tsa	–	–50 to 150		°C

43.2 Recommended Operating Conditions

Table 43-2 Recommended Operating Conditions

Pin Name/Symbol	Description	Min.	Typ.	Max.	Unit	Note
VDDI_ARM	DC supply voltage for Cortex-A9 CPU	0.95	1.0	1.365	V	ARM Speed: TBD
		1.045	1.1	1.365	V	ARM Speed: TBD
		1.14	1.2	1.365	V	ARM Speed: TBD
		–	–	–	–	–
VDDI	DC supply voltage for CORE	0.95	1.0	1.26	V	–
		1.045	1.1	1.26	V	–
		1.14	1.2	1.26	V	–
VDDP18	DC supply voltage for 1.8V Internal IO	1.7	1.8	1.9	V	–
DVDD33_IO	DC supply voltage for 3.3V IO	3.0	3.3	3.6	V	–
VDDQ	DC supply voltage for DRAM IP (LPDDR2)	1.14	1.2	1.26	V	–
	DC supply voltage for DRAM IP (LPDDR3)	1.14	1.2	1.26	V	–
	DC supply voltage for DRAM IP (1.35V DDR3)	1.283	1.35	1.417	V	–
	DC supply voltage for DRAM IP (1.5V DDR3)	1.425	1.5	1.575	V	–
VDDI10_ALIVE	DC supply voltage for CORE ALIVE	0.95	1.0	1.05	V	–
VDDP18_ALIVE	DC supply voltage for 1.8V Internal IO ALIVE	1.7	1.8	1.9	V	–
VDD33_ALIVE	DC supply voltage for 3.3V ALIVE	3.0	3.3	3.6	V	–
DVDD10_USB0	DC supply voltage for 1.0V USB OTG	0.95	1.0	1.05	V	–
VDD18_USB0	DC supply voltage for 1.8V USB OTG	1.7	1.8	1.9	V	–
VDD33_USB0	DC supply voltage for 3.3V USB OTG	3.0	3.3	3.6	V	–
DVDD10_USBHOST0	DC supply voltage for 1.0V USB HOST	0.95	1.0	1.05	V	–
VDD18_USBHOST	DC supply voltage for 1.8V USB HOST	1.7	1.8	1.9	V	–
VDD33_USBHOST	DC supply voltage for 3.3V USB HOST	3.0	3.3	3.6	V	–
DVDD12_HSIC	DC supply voltage for 1.2V USB HSIC HOST	1.15	1.2	1.25	V	(NOTE)
VDD18_RTC	DC supply voltage for 1.8V RTC Crystal	1.7	1.8	1.9	V	–
VDD18_OSC	DC supply voltage for 1.8V PLL Crystal	1.7	1.8	1.9	V	–
AVDD10_LV	DC supply voltage for 1.0V LVDS	0.95	1.0	1.05	V	(NOTE)
AVDD18_LV	DC supply voltage for 1.8V LVDS	1.71	1.8	1.89	V	(NOTE)
AVDD10_HM	DC supply voltage for 1.0V HDMI	0.95	1.0	1.05	V	(NOTE)
VDD10_HM_PLL	DC supply voltage for 1.0V HDMI PLL	0.95	1.0	1.05	V	(NOTE)
VDD18_HM	DC supply voltage for 1.8V HDMI	1.71	1.8	1.89	V	(NOTE)

Pin Name/Symbol	Description	Min.	Typ.	Max.	Unit	Note
M_VDD10	DC supply voltage for 1.0V MIPI	0.95	1.0	1.05	V	(NOTE)
M_VDD10_PLL	DC supply voltage for 1.0V MIPI PLL	0.95	1.0	1.05	V	(NOTE)
M_VDD18	DC supply voltage for 1.8V MIPI	1.7	1.8	1.9	V	(NOTE)
AVDD18_ADC	DC supply voltage for 1.8V ADC	1.7	1.8	1.9	V	–
ADCREF	Reference 1.8V for ADC	1.7	1.8	1.9	V	–
AVDD18_PLL	DC supply voltage for 1.8V PLL	1.7	1.8	1.9	V	–
DVDD_VID0	DC supply voltage for 2.8V VID0	1.7	2.8	3.6	V	–
DVDD_VID2_SD2	DC supply voltage for 2.8V VID2/SD2	1.7	2.8	3.6	V	–
DVDD_GMAC	DC supply voltage for 2.8V Ethernet MAC	1.7	2.8	3.6	V	(NOTE)
Ta	Operating Ambient Temperature	TBD			°C	

NOTE: This power pin can be tied to GND when this function is not used

43.3 D.C. Electrical Characteristics

Table 43-3 D.C. Electrical Characteristics (3.3V TOL)

(VDD = 1.65V to 3.60V, Vext = 3.0 to 3.6V, Ta = –25 to 85°C)

Parameter		Condition		Min.	Typ.	Max.	Unit
Vtol	Tolerant external voltage (NOTE)	VDD Power Off& On				3.6	V
Vih	High Level Input Voltage						
	CMOS Interface			0.7VDD		VDD + 0.3	V
Vil	Low Level Input Voltage						
	CMOS Interface	VDD = 2.5V ± 10%, 3.3V ± 10%		–0.3		0.7	V
		VDD = 1.8V ± 10%		–0.3		0.3VDD	
ΔV	Hysteresis Voltage			0.15			V
Iih	High Level Input Current						
	Input Buffer	Vin = VDD	VDD Power ON	–3		3	uA
			VDD Power Off & SNS = 0	–5		5	uA
	Input Buffer with pull-down	Vin = VDD	VDD = 3.3V ± 10%	15	40	80	uA
			VDD = 2.5V ± 10%	15	40	80	uA
			VDD = 1.8V ± 10%	15	40	80	uA
Iil	Low Level Input Current						
	Input Buffer	Vin = VSS	VDD Power ON & Off	–3		3	uA
	Input Buffer with pull-down	Vin = VSS	VDD = 3.3V ± 10%	–15	–40	–110	uA
			VDD = 2.5V ± 10%	–15	–40	–110	uA
			VDD = 1.8V ± 10%	–15	–40	–110	uA
Voh	Output High Voltage	Ioh = –1.8mA, –3.6mA, –7.2mA, –10.8mA		0.8VDD		VDD	V
Vol	Output Low Voltage	Ioh = –1.8mA, –3.6mA, –7.2mA, –10.8mA		0		0.2VDD	V
Ioz	Output Hi-z Current			–5		5	uA
CIN	Input Capacitance	Any input and Bi-directional buffers				5	pF
COUT	Output capacitance	Any output buffer				5	pF

NOTE: Specification is only available on tolerant cells