# **GUI User Manual**

Revision 0.0.0

\*Technology by



### 1. Purpose

Graphic User Interface (GUI) is a software program that verifies and tests the function of the Silicon Mitus product. This document is based on SMA2503 GUI.



The Silicon Mitus evaluation system has an I2C port, so the user can control the action via the GUI program. The diagram below describes the connection for the Silicon Mitus evaluation system using the GUI Program with test equipment, USB to I2C Board, PC, USB cable and Silicon Mitus Evaluation Board (EVB) Kit.





## 2. Installation

Unzip SMA2503\_Control\_Panel.zip to a local PC. To install the program, run "Setup.exe" file.

SMA2503	-		X
Destination Directory Select the installation directories.			
All software will be installed in the following locations. To install software into a			
different location, click the Browse button and select another directory.			
Target directory for application			
Comprogram Files (Xob) wiron Device Corporation wSMr			
Target directory for National Instruments software	_		
C: WProgram Files (X0b) Wivational instruments W Browse			
<< Back	>>	Canc	el
		_	V
SMA2503	-	,LL	X
Start Installation Review the following summary before continuing.			
Adding or Changing			
SMA2503 Files			
Click the Next button to begin installation. Click the Back button to change the installation	settings.		
Click the Next button to begin installation. Click the Back button to change the installation	settings.	Cano	
Click the Next button to begin installation. Click the Back button to change the installation	settings.	Canc	el
Click the Next button to begin installation. Click the Back button to change the installation Save File << Back Next	settings.		el X
Click the Next button to begin installation. Click the Back button to change the installation           Save File         << Back	settings.		el X
Click the Next button to begin installation. Click the Back button to change the installation           SMA2503	settings.	<u>C</u> anc	el X
Click the Next button to begin installation. Click the Back button to change the installation           Save File         << Back	settings.	<u>C</u> anc	el X
Click the Next button to begin installation. Click the Back button to change the installation           Save File         << Back	settings.	<u>C</u> anc	el X
Click the Next button to begin installation. Click the Back button to change the installation           Gave File         << Back	>> Settings.	Canco Cano Canco C	el X
Click the Next button to begin installation. Click the Back button to change the installation Save File SMA2503 Generating script operations for action:	settings.	<u>C</u> anc	el ×
Click the Next button to begin installation. Click the Back button to change the installation          Save File       << Back	settings.	<u>C</u> anc	el ×
Click the Next button to begin installation. Click the Back button to change the installation           Save File         << Back	>>	Canc	el ×
Click the Next button to begin installation. Click the Back button to change the installation           Save File         << Back	settings.	Cance Cance Cancella Cancella	el

U SMA2503		-		×
Installation Complete				
The installer has finished updating your syste	em,			
	<< <u>B</u> ack	<u>N</u> ext>>	Ein	ish

Installation Path

1. Windows Start  $\rightarrow$  Click " SMA2503 " SMA2503

2. C:\Program Files (x86)\Iron Device Corporation\SMA2503 folder. Run with SMA2503.exe

## 3. Device Configuration

Connect 'USB to I2C Board' to the Evaluation Board Kit.

- 1. Run SMA2503 GUI Program
- 2. If the USB to I2C Board is not connected normally, an error message pop-up window will appear.



Figure 3. Error Message Pop-up

### 4. Board Manual

### 4.1 Introduction

The SMA2503 Evaluation (EV) Board is a demonstration and evaluation board that shows the capabilities and features of SMA2503 chipset designed by Silicon Mitus (Iron Device). This board has an I2S interface for digital. Implementation of an amplifier with 2 x 150 W at 4  $\Omega$  (BTL mode) on four layers PCB.

### 4.2 Board Package Content

The SMA2503 EV Board package includes the following:

- 1. SMA2503 EV Board
- 2. USB to I2C Control Board
- 3. Cable set to connect the board in lab conditions.
- 4. Control S/W (Released by e-mail. Please contact Silicon Mitus separately.)

### 4.3 EV Board Overview



Figure 4. SMA2503-T EV Board Placement and EV Board



Figure 5. USB to High Speed I2C Control Board

Type: 2.54 mm Pitch Pin Header for J6			
Pin	Description	Value	
1	3.3 V LDO Output	+3.3 V	
2 IOVDD IOVDD			
Connect Pin 1 and Pin 2 if IO voltage is +3.3 V			

Type: 2.54 mm Pitch Pin Header for J7		
Pin	Description	Value
1	IOVDD	IOVDD (+3.3 V)
2	GND	GND
3	SCL	0 V to +3.3 V
4	SDA	0 V to +3.3 V

### 4.4 Board Schematic



Figure 6. SMA2503-T EV Board Schematic

### 4.5 Connectors

J19[SMA2503-T]: Power Stage and Analog Power Supply			
Type: Micro-Fit 3.0™ Right Angle Header (43650-0200, Molex)			
Pin Description Value			
1 PGND GND			
2 PVDD Maximum +40 V / 8.5 A			

#### LS4[SMA2503-T]: Left Speaker Output

Type: Micro-Fit 3.0™ Right Angle Header (43650-0200, Molex)		
Pin	Description	Value
1	SPK Output1 P	Maximum +40 V
2	SPK Output1 N	Maximum +40 V

#### LS3[SMA2503-T]: Right Speaker Output

Type: Micro-Fit 3.0™ Right Angle Header (43650-0200, Molex)			
Pin	Description	Value	
1	SPK Output2 N	Maximum +40 V	
2	SPK Output2 P	Maximum +40 V	

#### J31[SMA2503-T]: I2C Control Pin

Type: 2.54 mm Pitch Pin Header		
Pin	Description	Value
1	IOVDD	0 V to +3.3 V
2	GND	GND
3	SCL	0 V to +3.3 V
4	SDA	0 V to +3.3 V

#### J30[SMA2503-T]: I2S Input Port

Type: 2.54 mm Pitch Pin Header			
Pin	Description	Value	
1, 3, 5, 7	GND	GND	
2	LRCK	0 V to +3.3 V	
4	SCK	0 V to +3.3 V	
6	SDI (input data from source)	0 V to +3.3 V	
8	SDO (output data from chipset)	0 V to +3.3 V	

#### J29[SMA2503-T]: External Clock(MCLK) Input

Type: 2.54 mm Pitch Pin Header			
Pin	Description	Value	
1	GND	GND	
2	MCLK	24.576MHz	

#### J35[SMA2503-T]: Master Clock(MCLKO) Output

Type: 2.54 mm Pitch Pin Header

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Pin	Description	Value
1	GND	GND
2	MCLKO	24.576MHz

### 4.6 Measurement Set Up (APX525)

This set up is for the evaluation of SMA2503. Reference equipment is APX-525 from Audio Precision.

#### 4.6.1 Connection



Figure 7. Measurement Connection (I2S input)

### 4.6.2 Control S/W (GUI) – Quick Start (Register File Download)

This is a quick start initiated by downloading the device register file. Test steps are as the following:

- 1. Setup the H/W connection, and use the register file for device operation
- 2. Install SMA2503 Control Panel, and run SMA2503.exe
- 3. Click on "Load Registers" from "File"
- 4. Select the provided register file (.dat) for device operation
- 5. The device on the EVB will run
- 6. You can control other functionalities as desired

SMA2503 Register Control Panel				
File I2C Address Tool Help	)			
Load Registers			Volume Control	
Save Registers	TOP Manager	Power Rott	LEFT VOL 🔲 RIGHT VOL	
Exit			FF= L=R FF=	
Input Set, TDM	Vol. Ctrl.	SPK Mute	C8- C8-	
		Rch Lch	96- 96-	
Signal Path Setting	DSP Ctrl. Tone	Muted, Muted,	64- 64-	
	_DSR_0p/0ff		32- 32-	
EQ Control		2.1 ch Mode	00- 00-	
		Rch Lch	7 7	
Bass Boost	Bass Boost	Muted, Muted,	‡ x 58	
	Comp/Limiter		-20.0 [dB] -20.0 [dB]	
DRC(Comp/Limit)	Muti-DRC		td	
		Beed from Device Write to De		
Modulator	LDO Control	Tieau IIoni Device Wille to De		
modulator	Ebo control		<b>Icon Device</b>	
Power Stage	Control Setting	Status Monitoring		
. onor otago	Sound Obuning	OSC CLOCK_M	on Cilicon Mitue	
PLL Control	Test	00000000 00000000		

Figure 8. Loading Register File

Name of File to Read X						
Directory <u>H</u> istory: ∣C:₩Pr	rogram Files (x86)†	∀Iron Device Corporation*	#SMA2503	ļ		•
찾는 위치(!):	SMA2503		-	← 🗈 🎟▼		
바로 가기	이름 🎬 SMA2503_defa	ault		수정한 날짜 2018-08-06 오후 11	유형 DAT 파일	
<mark></mark> 바탕 화면						
ini angle a						
LH PC						
<b>1</b>						
네트워크	<					>
	파일 이름( <u>N</u> ):	default		•	<u>0</u> K	
	파일 형식( <u>T</u> ):	(*,dat)		<b>T</b>	취소	



### 5. Detail Controls

#### SMA2503 Register Control Panel × File I2C Address Tool Help (8) (9) (3) Volume Control • Power J Off LEFT VOL □ L=R **RIGHT VOL TOP Manager** System Setting FF= FF= SPK Mute C8-C8-Input Set, TDM Vol. Ctrl. Rch 96-96-Lch Signal Path Setting DSP Ctrl, Tone 2 Muted, Muted, 64-64-32-32-DSP On/Off 2,1 ch Mode EQ Control 00-00-(6) 🗌 EQ Rch Lch 🔲 Bass Boost ‡ <sub>×</sub>58 ‡ <sub>×</sub>58 Muted, Muted, Bass Boost Comp/Limiter -20,0 [dB] -20,0 [dB] (5) (4) Muti-DRC DRC(Comp/Limit) Write to Device Read from Device Modulator LDO Control Iron Device Status Monitoring **Control Setting** Power Stage Silicon Mitus 7 OSC CLOCK\_MON 00000000 00000000 PLL Control Test

### 5.1 Control Panel Overview (Main Panel)

Figure 10. SMA2503 Register Control Panel

No.	Item	Description
1	Power On/Off with Sequence	Power On: Power-up $\rightarrow$ Speaker Output On $\rightarrow$ De-mute Power Off: Mute $\rightarrow$ Speaker Output Off $\rightarrow$ Power Off
2	Mute Control	Mute and De-mute Control
3	Volume Control	Master Volume Control
4	Read from Device	Read I2C from DUT and Set Panel
5	Write to Device	Read Set Value from Panels and Write to DUT
6	DSP On/Off	DSP block on/off – this is the same control at Signal Setting Panel
7	Status Monitoring	Click on "Status Monitoring" Reads status register and updates display every 0.2 seconds Stops monitoring when clicked again
8	Menu Bar – File	Load Register: Register Load from .dat file Save Register: Register Save to .dat file and .datx file Export Filter Parameters: Structure of coefficients for C file to .datx file
9	Menu Bar – Tool	Direct Register Control Panel – Open Direct Register Control Panel

### 5.2 Initialization

#### 5.2.1 System CLK

- System Setting Panel 1.
- Select the System CLK depending on the system 2.
  - Internal OSC using an internal oscillator -

  - Crystal OSC (24.576 MHz) Ext. CLK 19.2 MHz: External clock with IOVDD Level \_
  - Ext. CLK 24.576 MHz: External clock with IOVDD Level

### 5.2.2 CVDD EN (Clock VDD)

- LDO Control Panel 1.
  - LDO\_CVDD Enable: Enable \_

#### 5.2.2 Change the Default Value (these values were tuned)

- 1. Power Stage Panel
  - FLT\_VDD\_GAIN: b'01111 to b'00101
  - Dead time HS: b'0010 to b'0001 \_
  - Dead time LS: b'0010 to b'0110 \_
  - Slope Control HS: b'10 to b'01 \_
  - Slope Control LS: b'10 to b'00
- 2. Feedback Control
  - SPK BDELAY: b'100000 to b'011101 -

#### 5.2.2 Input Mode Selection

- Case 1) I2S (fs = 48 kHz): Using Default Value 1.
- 2. Case 2) I2S (fs = 192 kHz)
  - Use a PLL setting
    - Or use Down Conversion Top Management Panel
      - DAC Down Conversion: Down Conversion

### 5.3 BassBoost



#### Figure 11. BassBoost Control Panel

No.	Item	Description
1	HPF Frequency	1 <sup>st</sup> Order High Pass Filter Frequency Setting. "0" is off
2	Boost Frequency	Boost Frequency Setting: 20 Hz to 1 kHz
3	B.Boost Input	Select input of Bass Boost Block (Pre or Post HPF)
4	Filter Type	Band Pass Filter or Low Pass Filter Type
5	B.Boost Gain	Bass Boost Gain Setting
6	B.BoostTHRES (Boost Trigger)	Set the starting limit of Bass Boost
7	Attack Release Time (Boost Trigger)	Set the attack/release time limit of Bass Boost
8	Low Pass Frequency (Boost Trigger)	Low pass filter of the signal that controls the attack release function Should be set above boost frequency

### 5.4 EQ Control

٦	Seq Control Panel X							
	EQ Mode Selection							
	EQ1 (Fc=140Hz)	EQ2 (Fc=355Hz)	EQ3 (Fc=1kHz)	EQ4 (Fc=2,8kHz)	EQ5 (Fc=7,5kHz)			
	12dB-	12dB-	12dB-	12dB-	12dB-			
	6dB -	6dB -	6dB -	6dB -	6dB -			
	OdB -	0dB -	OdB -	0dB -	0dB -			
	-6dB -	-6dB -	-6dB -	-6dB -	-6dB -			
	-12dB-=	-12dB - =	-12dB - =	-12dB - =	-12dB-=			
	Bypass 🗖	Bypass 🗖	Bypass 🗖	Bypass 🗖	Bypass 🗖			
	Parametric EQ							



#### Figure 12. Parametric EQ Panel

No.	Item	Description
1	EQ	There are three EQ BANKs in cascade EQ is bypassed if checked
2	Linkwitz-Riley filters	Open Linkwitz-Riley filter panel and pre-set
3	MDRC	Open MDRC panel and pre-set for MDRC
4	EQ Band	Q Factor Biquad Filter Type PEQ 2 <sup>nd</sup> BW (Butter Worth) HPF

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		2 <sup>nd</sup> BW (Butter Worth) LPF LSF (Low Shelf Filter) HSF (High Shelf Filter) Piezo Tune Notch Gain -20 dB to +20 dB Frequency 20 Hz to 20 kHz Check Box Checked: On
5	LR SUB MODE	Test purpose register

### 5.5 DRC (Comp/Limit)

![](_page_16_Figure_2.jpeg)

Figure 13. Compressor/Limiter Control Panel

No.	Item	Description
1	Threshold	Compressor Threshold Maximum high level: - 0.1 dB Compressor off: 0.0 dB Limiter Threshold Maximum high level: - 0.3 dB Limiter off: 0.0 dB
2	Hard Limiter	Clip the signal when it exceeds the threshold
3	Compressor	Compressor Ratio Amount of compression
4	Attack / Release Time for Compressor	Attack / Release Time
5	Attack / Release Time for Limiter	Attack / Release Time
6	SPK DRC	Compressor/Limiter setting for speaker path
7	Half Bridge DRC	Compressor/Limiter setting for half-bridge path
8	MDRC	Compressor/Limiter setting for speaker multi-band
9	BPDRC	Compressor/Limiter setting for speaker band-pass post

### 5.6 2-Way Speaker – Mono (use L-R filter)

![](_page_17_Figure_2.jpeg)

Figure 14. LR Filter Control Panel

### 5.6.1 Signal Mono Set

- 1. Signal Path Setting - Mono Mix: On
- 2. EQ Setting
  - Main Panel
  - DSP EQ: Check

Linkwitz-Riley Filter Set						
No.	Item	Description				
1	LR Filter Order	Recommended 4 <sup>th</sup> Order				
2 Туре		HPF: EQ for Tweeter LPF: EQ for Woofer				
③ LR Filter Frequency		Cross Over Frequency Set				

### 5.7 2.1ch Mode

Power Stage Co	ontrol Panel					-		×
I2C_CE H U L	I2C_OE1 H U L	I2C_OE2 H J L	DIS_SCP Disable ) Enable	· I e e	DIS_MOS_FW Disable U Enable	OCP_CN	IT_GAIN H L	
TSD Level	OCP_LVL_H ₽⊾ OO	OCP_LVL ₽ 00	L SET	LEB 00	SET_FLT_DLY	Test for F ₽ Þ	PBTL Co	ntrol
Dead Time HS         Dead Time LS         Slope Control HS         Slope Control LS           00000         0101         1010         1111         000         01         10         11           1         1         1         1         1         1         1         1         1           1						F > 1		
1 Mode (	Control 2 × SE	FLT_VDD_	GAIN F	DPEC Enab Norm	le FDPEC nal Operation	FIX_GAIN Fixed Norm	l Gain Ial Mode	
DIS_GUVI Disab U Enabl Soft Start Enabl U Disab	LO Ile GVDD UVLO Ile GVDD UVLO Ile	Attac 0000 1111	Class G C k Level : Boost On : Boost Off	Atta (0,3 (0,3 Releas (10ms,	ck Level 1 1125FS/step) 50000 se Time 1 /step @48kHz) 50000	Attack L (0,0625F Belease Ti (10ms/ste	evel 2 (S/step) (I) (me 2 (p @48kH) (0)	z)

Figure 15. Power Stage Control Panel for 2.1ch

### 5.7.1 Mode Control

No.	Item	Description
1	Mode Control	1 x BTL + 2 x SE

#### 5.7.2 System Setting

![](_page_19_Picture_2.jpeg)

Figure 16. System Setting for 2.1ch

No.	Item	Description
1	Speaker Mode	Mono signal at left terminals
2	Half Bridge Path Mode	Stereo

#### 5.7.3 H/W Connection

- 1. Left Output: BTL mode Woofer
- 2. Right Output: SE mode Left/Right

### 5.8 DOUT (SDO)

#### 5.8.1 I2S Input to DOUT (SDO)

- 1. TOP Manager Panel
  - Master Mode: Master Mode Selection
- 2. Signal Path Setting Panel
  - Port Config: OUT: Port3, IN: Port1, 2
  - Port Select: (See Figure 20. Signal Path Setting)

![](_page_20_Figure_8.jpeg)

Figure 17. TOP Manager Panel for I2S Input to DOUT

### 6. Other Control Panels

### 6.1 System Setting

![](_page_21_Figure_3.jpeg)

#### Figure 18. System Setting for Other Control Panel

No.	Item	Description
1	System CLK	Internal OSC Crystal OSC (24.576 MHz) FLL Ext. CLK 19.2 MHz Ext. CLK 24.576 MHz
2	Power Up	Analog Block Power On
3	Internal Clock Calibration	Internal OSC Frequency Calibration
4	Oscillator Precision	Precision setting in case of Audio Calibration mode
5	Speaker Mode	Speaker Output selection mode after DSP
6	Half Bridge Path Mode	Normally Off This should be set to "Stereo" in case of half bridge path mode (2.1ch)
7	I2C Reset	Reset for I2C register

### 6.2 Input Receiver Control

### 6.2.1 Input Receiver Control Panel

- Digital input format setting
   It is recommended to use the default in case of I2S signal

Input Control Panel	- 🗆 ×					
1 Input1CTRL1	2 Input1CTRL2					
2S/PCM Clock Mode Master Mode	Input Audio Mode I2S Mode 🔻					
I2S Input Format Phillips Standard I2S ▼	Data L/R Exchange Inverted (Right-first) (Both for I2C & PCM) Normal (Left-first)					
First-channel Polarity	Companding PCM Companding.					
High for first-channel data Low for first-channel data	Decoding Select PCM Sample Fre. A-law u-law 8Khz					
Data Written On SCK Rising Edge SCK Falling Edge	PCM Stereo/Mono PCM Data Length Stereo Mode 16bit Mono Mode 8bit					
3 Input1CTRL3,4	(3) Input1CTRL3,4					
# of Slot pr, Sample Period(PCM)     Default is 2 slot (PCM_CLK 128kHz@8bit)     PCM n-Slot ♀ 1	Position of the sample@ 8,16kHz (Slot Number) 1st n-Slot 2nd n-Slot 1 1 1					
4 SRC Bypassed 🗆	INPUT 1					

Figure 19. Input Receiver Control Panel

No.	Item	Description
1	Input1 CTRL 1	I2S input format settings
2	Input1 CTRL 2	PCM input format settings
3	Input1 CTRL 3,4	PCM slot setting
4	SRC Bypass	Sample Rate Converter turns off if checked

### 6.3 Signal Path Setting

![](_page_23_Figure_2.jpeg)

#### Figure 20. Signal Path Setting

No.	Item	Description
1	Port Config	Port Configuration Normal Mode: Not used for SDO output Audio Data Output: Used for SDO output
2	Port Output Format	I2S format for SDO
3	Output Source	Select signal to output in case of only master/slave mode (see the TOP Manager Panel) Disable Format Convert Input Mixer Output@48kHz SPK Path after DSP(48kHz) Half Bridge Path after DSP(48kHz) For Test (LR Mixing Before DSP) For Test (Tone & Fine Vol.) For Test (LR Mixing after Tone & Fine)
4	Input Receiver Setting	Open the Input Receiver Control Panel
5	Pre-Gain into Mixer	Mixer Gain of Digital Input signal
6	Mono Mix (Left Signal + Right signal) / 2 This function should be used for 2-way speaker application	
7	DSP	DSP On/Off – it is the same control as DSP On/Off in Main Panel
8	Output Mode Setting	Open the System Setting Panel

### 6.4 TOP Manager

![](_page_24_Figure_2.jpeg)

Figure 21. TOP Manager Panel

No.	Item	Description
1	Top manage1	I2S format for SDO output
2	PLL Reference Clock1	PLL Reference clock selection
3	PLL Reference Clock1	PLL Reference clock selection
4	PLL_PD	PLL power-down On/Off
5	DAC Down Conversion	DAC down conversion for 192kHz input signal
6	Master Mode	Master or Slave mode selection
7	SDO PAD Output Control	Normal or SDO Output
8	PLL Lock Skip Mode	PLL Lock Skip disable or enable
9	Top manager3/4	Register setting for test purpose

### 6.5 Volume Control

![](_page_25_Figure_2.jpeg)

#### Figure 22. Volume Control Panel

No.	Item	Description
1	SPK Volume Control	Speaker Left / Right Volume
2	Half-Bridge Volume Control	Left / Right Volume in 2.1ch mode
3	Vol./Mute Control	Volume and Mute Slope Control Fade in / Fade out effect

### 6.6 Power Stage

![](_page_26_Figure_2.jpeg)

Figure 23. Power Stage Control Panel

No.	Item	Description
1	TSD Level	Thermal shut down level (high temperature: b'11)
2	OCP Level	Over current protection level: High (b'11) to Low (b'00), 0.5 A/Step
3	Dead Time	PWM Dead time control (b'1111: short to b'0000: long)
4	Slope Control	PWM Slope Control (b'11: fast to b'00: slow)
5	Mode Control	Output Mode: BTL x 2 or 1BTL + 2 x SE (2.1ch)
6	FLT_VDD_GAIN	Normally this value should be set as b'100 This should be set in Fixed Gain Mode and Class G operation with Boost converter (SMA6021)
7	FDPEC	Output Feedback Loop On/Off
8	FIX_GAIN	Fixed gain mode makes fixed FS (full scale) FS depends on PVDD Level in normal mode
9	Class G Control	This function is only for class G operation with SMA6021 Boost Converter

### 6.7 LDO Control

![](_page_27_Figure_2.jpeg)

Figure 24. LDO Control Panel

No.	Item	Description
1	LDO_CVDD Enable	Internal LDO enable for CVDD (clock power)
2	LDO2(DVDD) Output	Internal LDO voltage for DVDD (digital power)

### 6.8 Feedback Control

🛸 Modulator Control Panel	;
1 Half-Bridge Path Hysteresis 2,0 MHz 🗨	(3) SPK Hysteresis Feedback 625 kHz  ▼
② Half-Bridge Path BDELAY	④ SPK_BDELAY ● 000000

Figure 25. Modulator Control Panel

No.	Item	Description
1	Half-Bridge Path Hysteresis	PWM frequency of SE output in 2.1ch mode
2	Half-Bridge Path BDELAY	Do not control
3	SPK Hysteresis Feedback	PWM frequency of speaker output
4	SPK_BDELAY	Do not control this value. This value should be provided by and used as accordingly to Silicon Mitus

### 6.9 Control Setting

![](_page_28_Picture_2.jpeg)

Figure 26. Control Setting Panel

No.	Item	Description	
1	Thermal protection option	Disable Ignore Threshold1 (TSDW), Shutdown at Threshold2 (TSD) Reduced 6 dB output at Threshold1 (TSDW), shutdown at Threshold2 (TSD) Shutdown at Threshold1 (TSDW) and Threshold2 (TSD)	
2	OCP Mode	Permanent shutdown of output Auto recover (1 second)	
Other controls are not used			

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Revisio	Revision History					
Rev	DATE	CHANGES	Issued by	Notes		
0.0.0	09/07/2018	Initial Release and reviewed with IronDevice	Gyuhwa			

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