

Troubleshooting Manual

C905



ABOUT

General information

The purpose of this document is to provide enhanced technical information for Sony Ericsson repair technicians in order to assist during service, repair and troubleshooting operations on Sony Ericsson mobile phones. It should be used as a complement to other repair instructions and tools as notified by the local Sony Ericsson representative.

To search for components throughout the entire document use the “search” function in Adobe Acrobat Reader 7.0 (or later version) and enter the component name or other word. Use zoom to enlarge.

For easier navigation of the document you can use the bookmarks that appear in the Bookmarks tab on the left side of the Adobe Acrobat Reader window. Each bookmark jumps to a page in the document.

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Revision History

Rev.	Date	Changes / Comments
1	12/05/2008	Initial revision.

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C905 Equipment List



Note! Additional information about the equipment used for TRS can be found in the following locations:

Location 1: CSPN – Repair Instructions – Additional Soldering Process – C905, C905a or C905c – Equipment List.

Location 2: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf or matrix.xls – C Model Tab.

Troubleshooting Fixture

Location: CSPN – Repair Instructions – Additional Soldering Process – C905, C905a or C905c – Equipment List.

Part number: 1218-4986

Note! Additional information about the TRS Fixture Kit can be found in the Trouble Shooting Fixtures Setup Instructions document which is included in the appendix of this manual.

Dummy Battery

Location: CSPN – Repair Instructions – Additional Soldering Process – C905, C905a or C905c – Equipment List.

Part number: 1208-5627

Note! The resistance between GND and BDATA should be approximately 27K Ohm.

Instruments

Power Supply Channel 1 (VBATT)

Agilent 6632B or similar

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Instrument Settings:

Voltage: **3.8 Volt**

Limiter: **2.0 A**

Note! Maximal cable length between the Power Supply Channel 1 VBATT and the dummy battery cannot be more than 1 meter. The cable must be able to handle at least 16A.

Power Supply Channel 2 (DCIO/SEPI)

Agilent 6632B or similar

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Instrument Settings:

Voltage: **5.0 Volt**

Limiter: **2.0 A**

Oscilloscope

Agilent DSO7052A or similar

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Digital Multimeter (DMM)

Fluke 83 or similar

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Note! The 0, 64 mm Test Probes is recommended by Sony Ericsson when DMM is in use see Picture 1.

Picture 1



Spectrum Analyzer

R&S FSL 9 kHz – 3 GHz or similar

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

RF probe

HP 85024A or similar

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Mobile Phone Tester

Yokogawa VC200 or similar

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

FM Signal Generator

R&S SMC100A or similar

Location: -

RF Adaptor

Adaptor 33 N-BNC-50-1

Adaptor to Signal Generator RF Output

See Picture 2

Location: -

Picture 2



PC Package & PC Software

PC Package (Computer)

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Urquell Fault Trace SW with project file

Location: CSPN – Repair Instructions - Electrical – C905, C905a or C905c – Trouble Shooting Application

Project File: C905, C905a, C905c Project_R1A

Drivers

SEPI BOX Drivers

Location: <http://emma.extranet.sonyericsson.com> – Drivers – DSS / SEPI / SEMUTS

SE Communication Interface SEPI BOX

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Part number: LTN 214 1484

See Picture 3.

Picture 3



Cables

USB Computer Cable

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – Re

See Picture 4.

Picture 4



DSU-60 / USB Cable

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – Re

Part number: KRY 101 1413

RF Test Cable Flexible

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – Re

Part number: RPM 119 885

See Picture 5.

Picture 5



SEPI Interface Cable – A1

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – Re

Part number: KRY 101 1119/1

See Picture 6.

Picture 6



Power Cable RED to Power Supply Channel 1 (VBATT)

Maximum Length: 1m

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Power Cable BLACK to Power Supply Channel 1 (VBATT)

Maximum Length: 1m

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Customized Power Supply Channel 2 Cable (DCIO/SEPI)

Customize the cable according to following instructions below:

(Step 1, Step 2, Step 3 and Step 4)

Step 1:

Take the CST-75 battery charger and cut of the charger according to Picture 7.

Picture 7



Note! The Cable length must be exactly 1.3 meters.

Step 2:

Connect the CST-75 charger Red or White wire to the Plus Output and the Black wire to the Minus (GND) Output at backside of the Power Supply Channel 2 (DCIO/SEPI) according to Picture 8.

Picture 8



Step 3:

Cut off insulating material from the inside of the charger plug according to Picture 9.

Picture 9



Step 4:

Connect DCIO Cable and SEPI Interface Cable – A1 according to Picture 10.

Picture 10



Picture 11



Note! The setup example presented in the Picture 11 is wrong!

Connection Instructions for the Dummy Battery

This is the correct setup when using the Dummy Battery.
See Pictures 12 and 13.

Picture 12



Picture 13



Customized FM Radio Cable

Step 1:

Use the Test lead BNC-4mm 1,5m Cable, see Picture 14.

Picture 14



Product Name: Test lead BNC-4mm 1,5m

Product Description: Test lead with 4 mm lab plugs at one end and a BNC plug at the other.

Manufacturer: PMK Germany

Location: <http://www.elfa.se/en/> or other supplier.

Part number: 46-310-40

Note! This is the ELFA part number.

Step 2:

Cut the Red Lab Plug connector according to Picture 15.

Picture 15



Step 3:

Use any Hands-Free (PHF) Cable and cut it according to Picture 16.

Picture 16

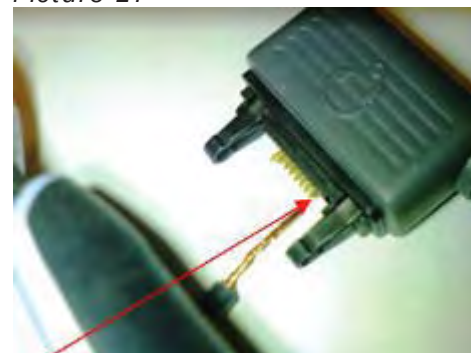


Note! Cable length should be at least 40 cm.

Step 4:

Only use the Wire that is connected to PIN2 and cut out all others according to Picture 17.

Picture 17



Note! Use DMM instrument to ensure which of the wires are connected to PIN2 at Hands-Free (PHF) system connector plug.

Step 5:

Connect the Cable from the Picture 15 and Cable from the Picture 17 according to Picture 18.

Note! Use a soldering iron for this action and then use insulating material to protect the contact point.

Picture 18



Test Cards

Local SIM

Any functional Local SIM Card
See Picture 19.

Picture 19



Test SIM GSM/UMTS

One Test SIM GSM/UMTS is needed to perform Current Consumption Test, see Picture 20.

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – RepairToolsCatalogue.pdf

Note! To buy a Test SIM GSM/UMTS, please contact your supplier of test equipment.

Picture 20



Sony Memory Stick M2

Any functional Memory Stick Micro M2 Card
See Picture 21.

Picture 21



SMK RF Probe

Location: CSPN – Repair Instructions – Mechanical – Tool Catalogue – Re

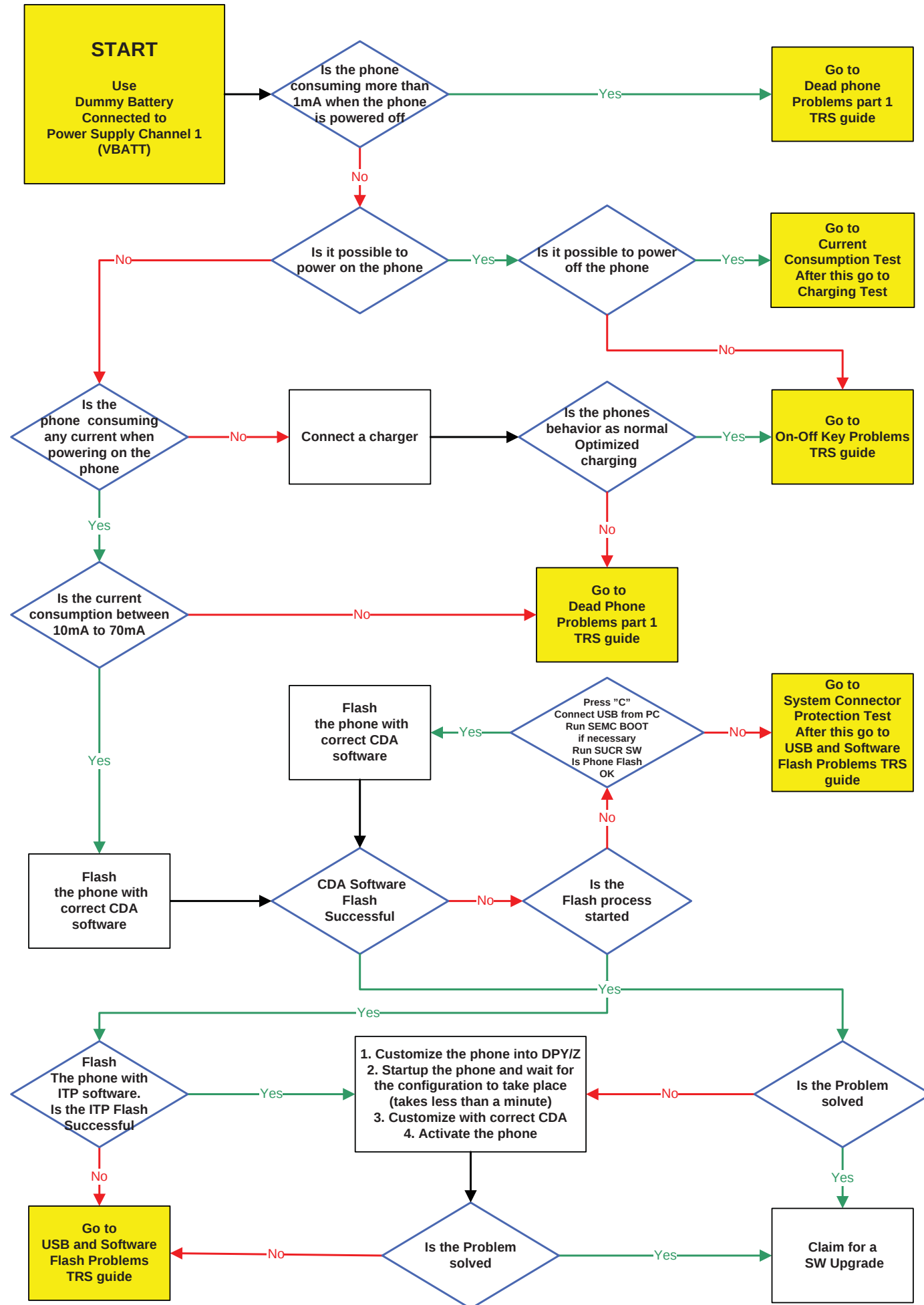
Part number: SXA 109 6356

See Picture 22.

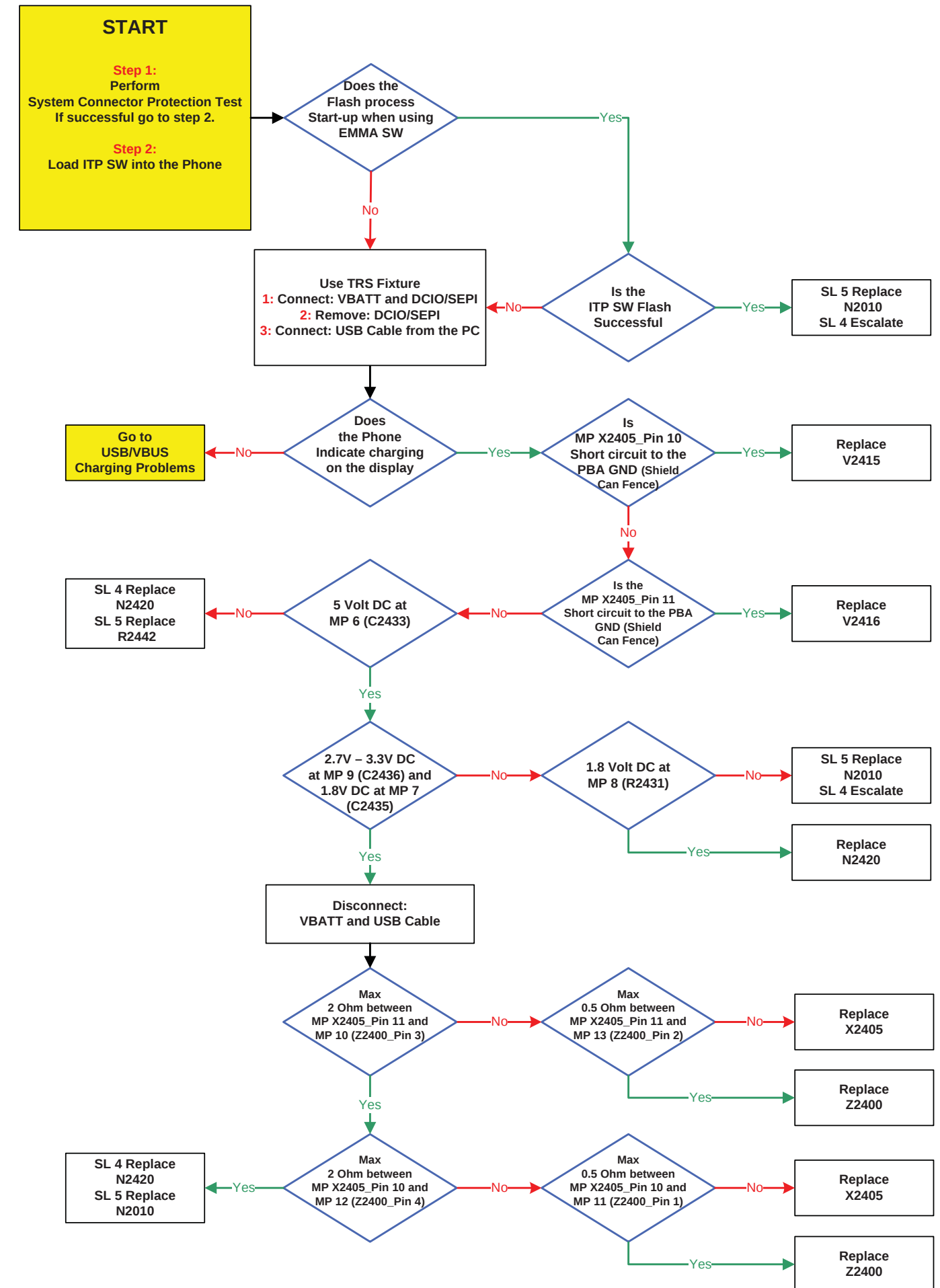
Picture 22



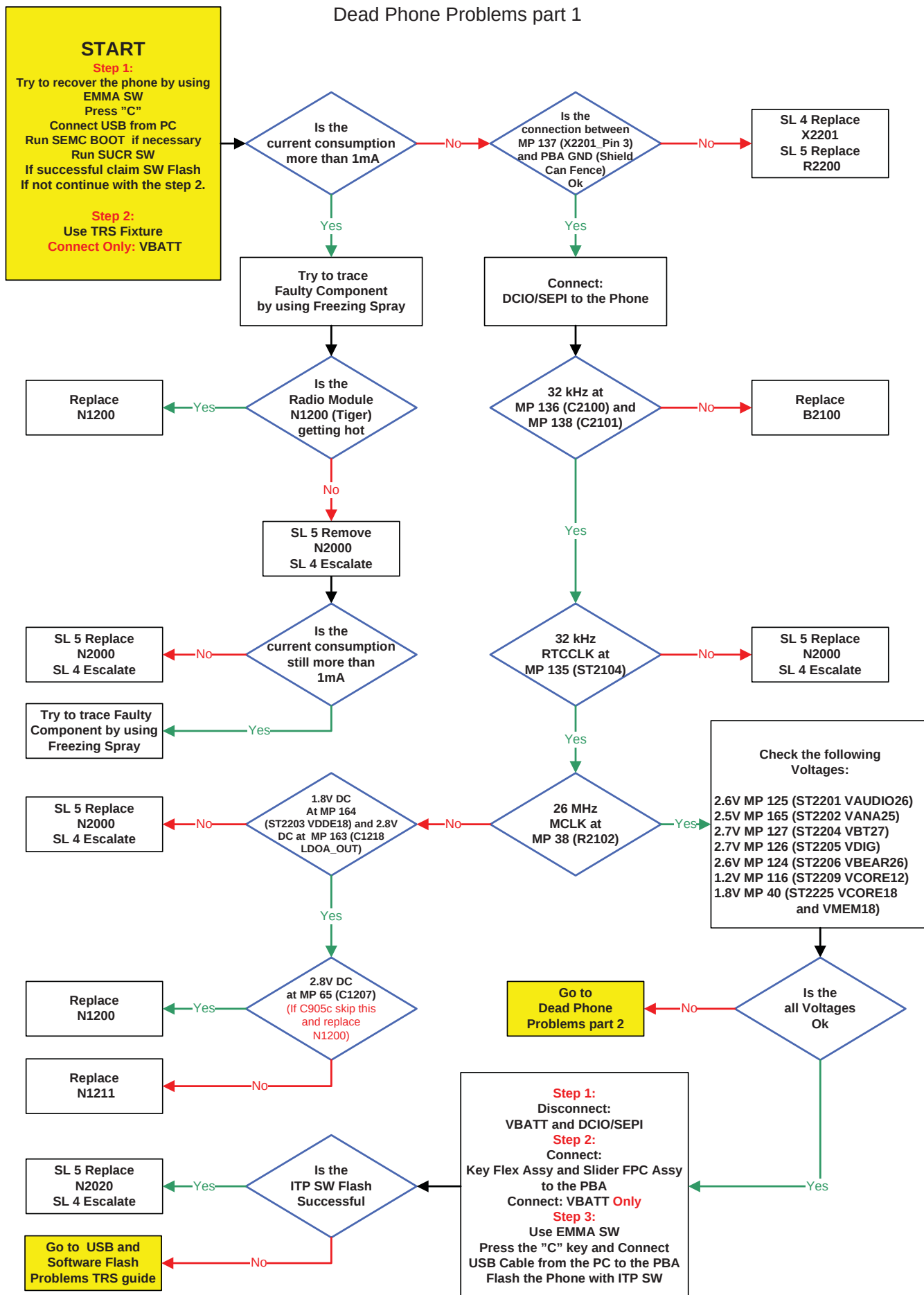
Power On/Off Problems



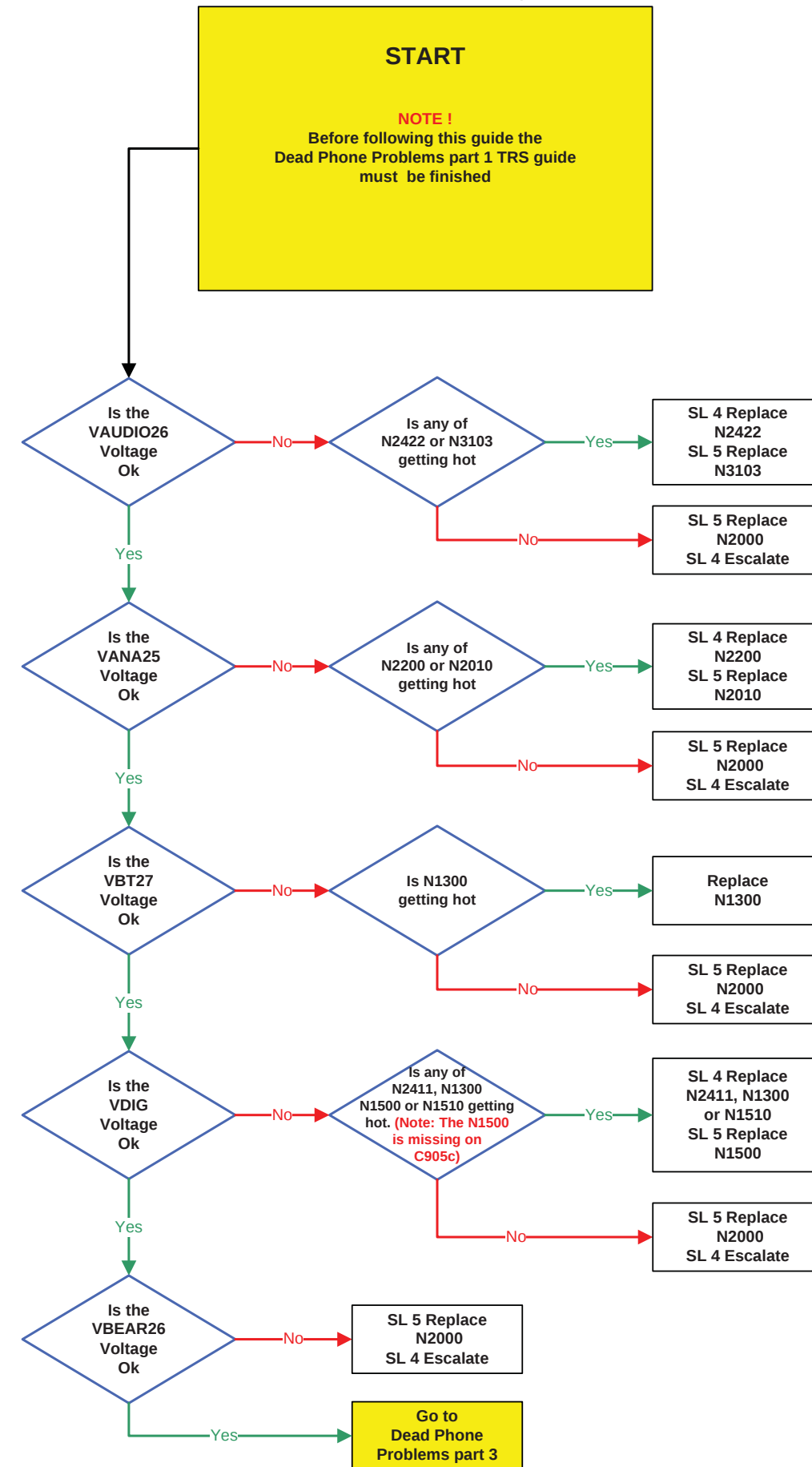
USB and Software Flash Problems



Dead Phone Problems part 1



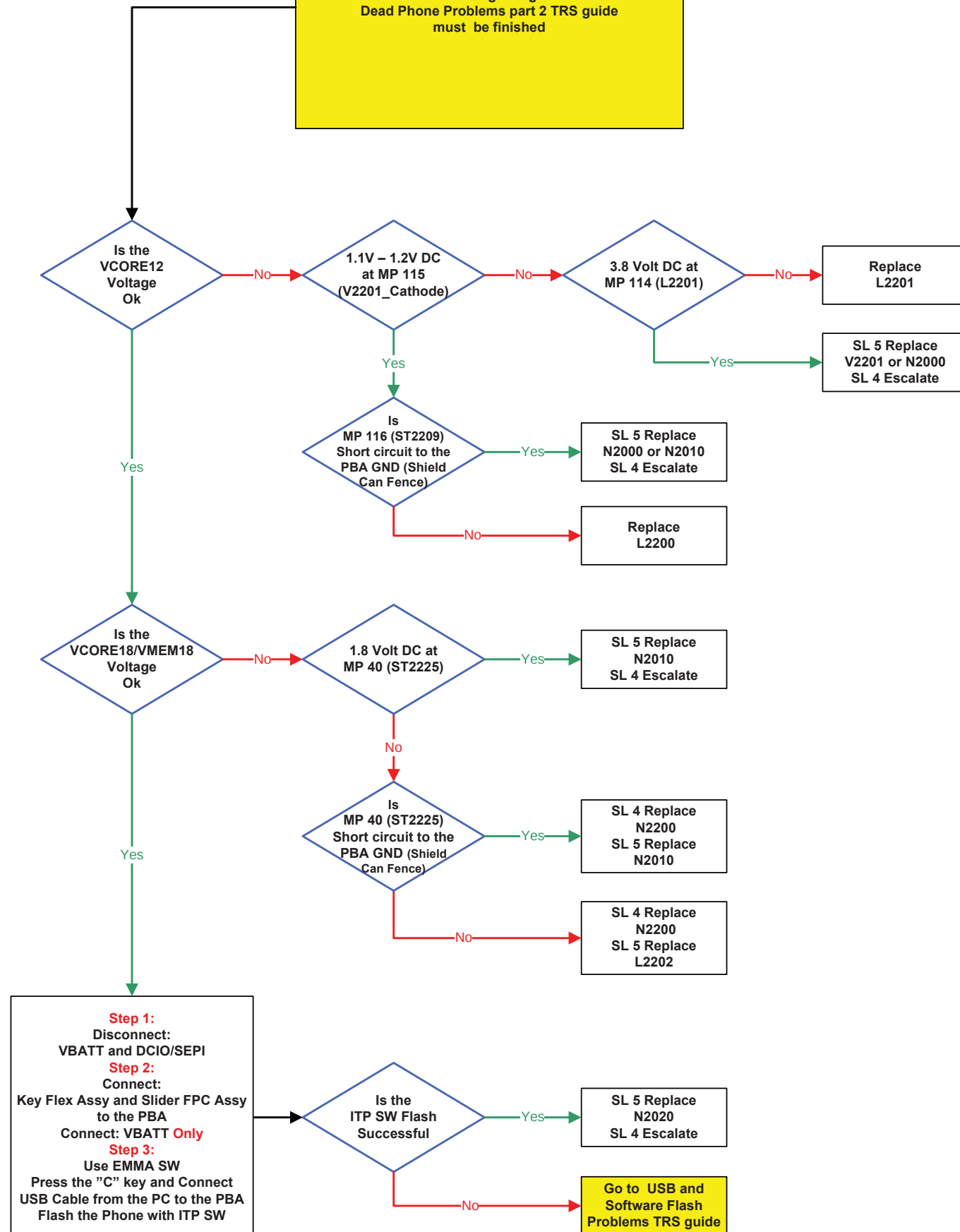
Dead Phone Problems part 2



Dead Phone Problems part 3

START

NOTE !
Before following this guide the
Dead Phone Problems part 2 TRS guide
must be finished

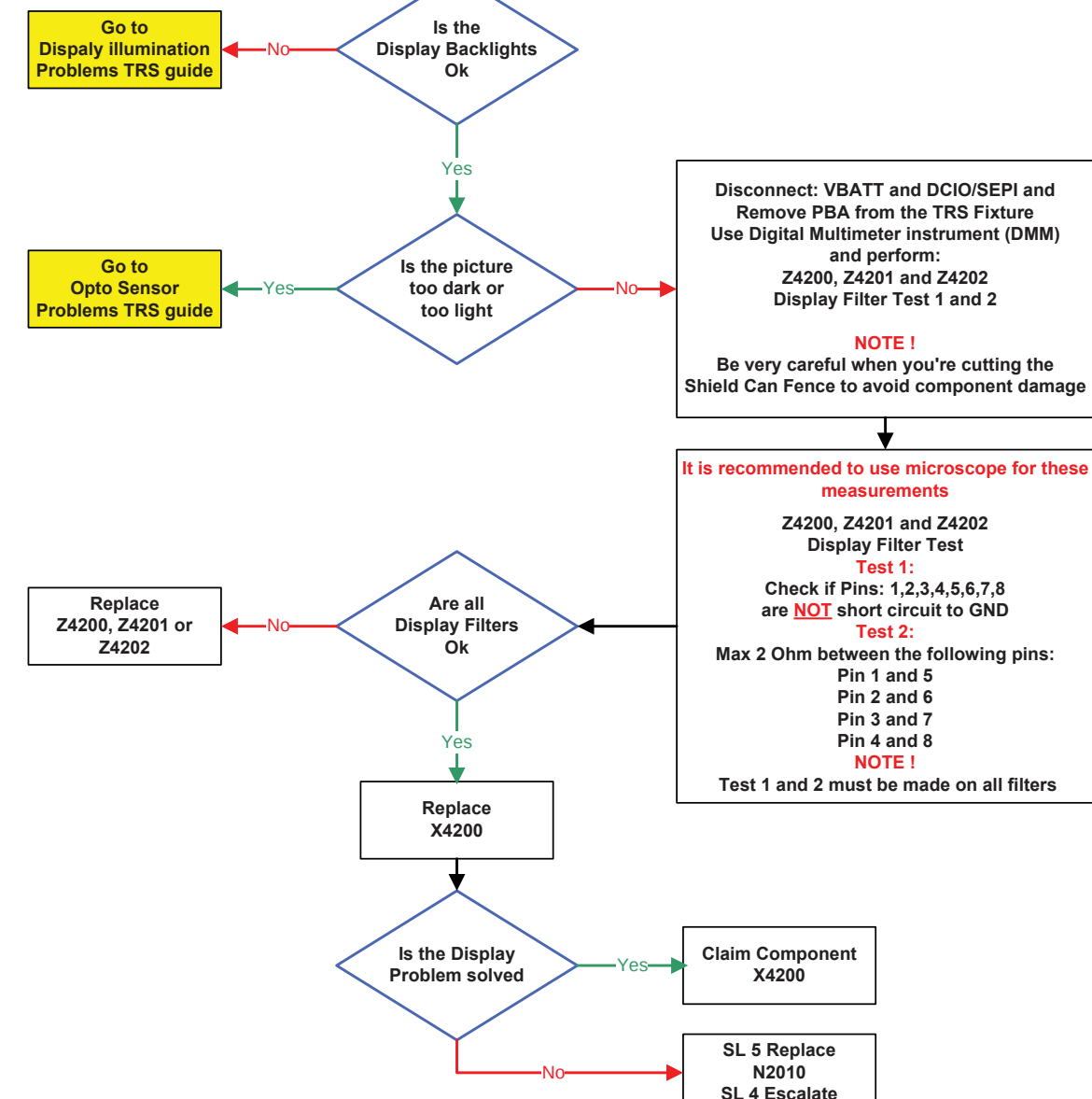


Display Problems

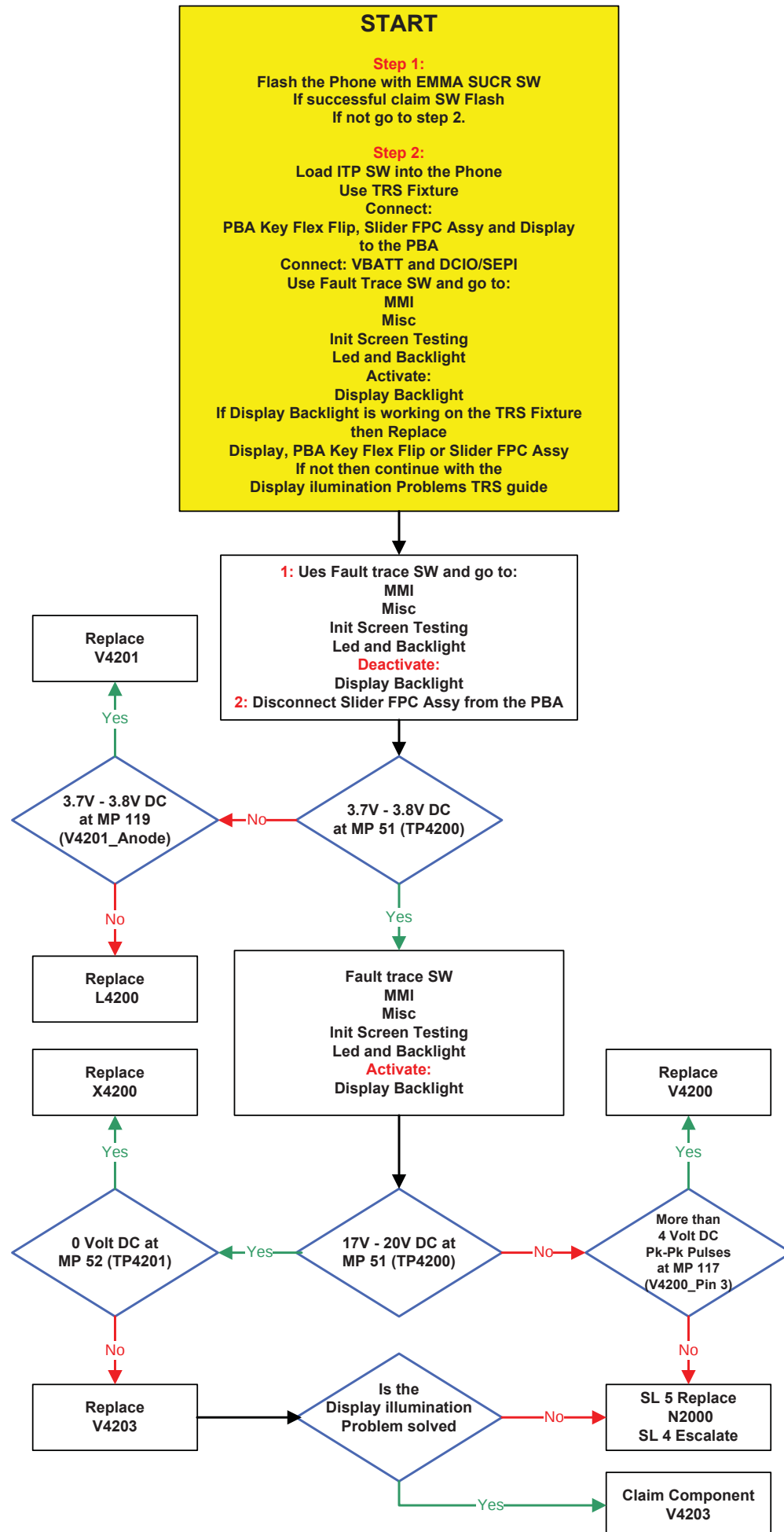
START

Step 1:
Flash the Phone with EMMA SUCR SW
If successful claim SW Flash
If not go to step 2.

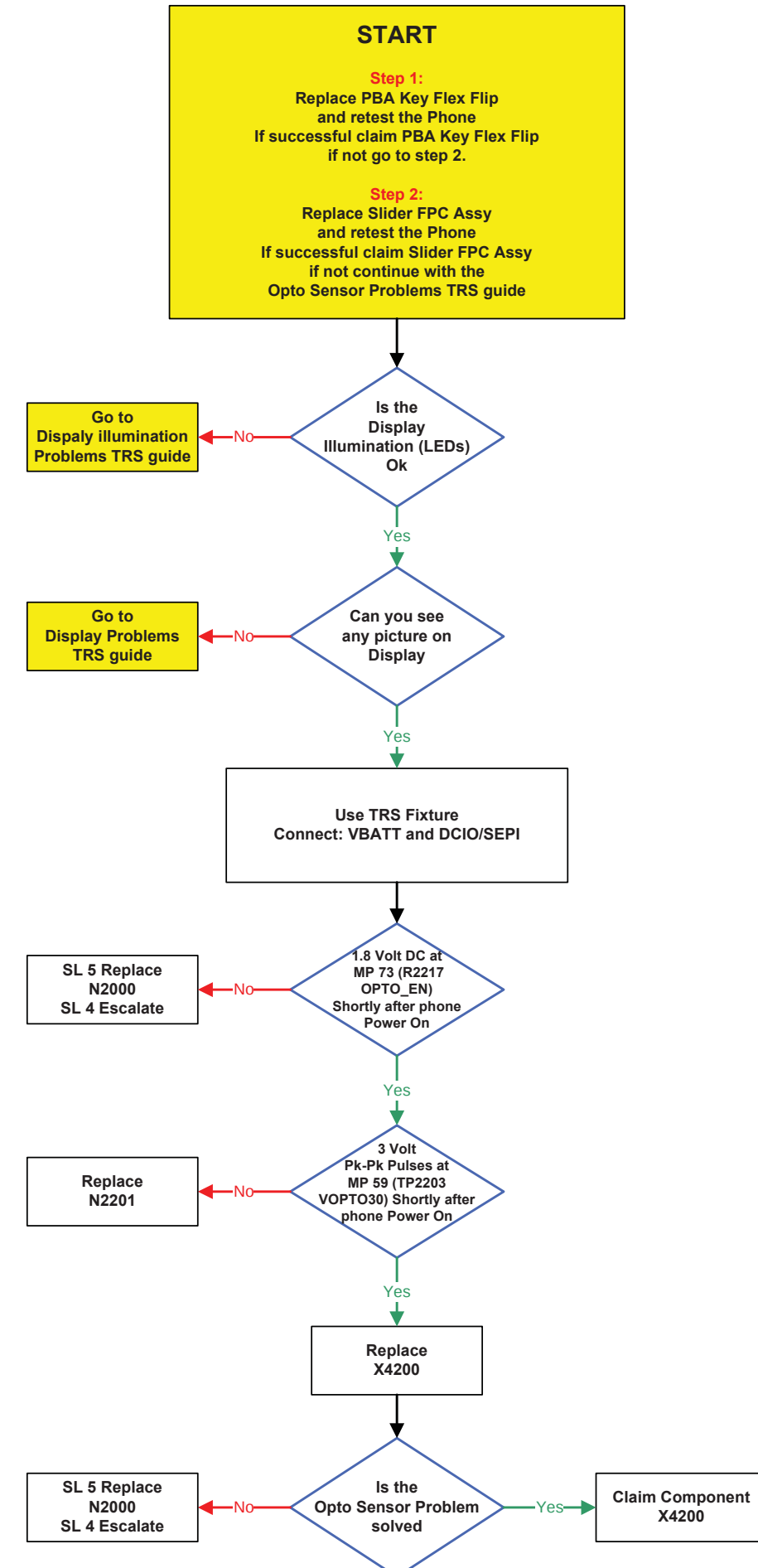
Step 2:
Load ITP SW into the Phone
Use TRS Fixture
Connect:
PBA Key Flex Flip, Slider FPC Assy and Display
to the PBA
Connect: VBATT and DCIO/SEPI
Use Fault Trace SW and go to:
MMI
Misc
Init Screen Testing
Display Pattern
Activate:
TV Test Pattern
If Display is working on the TRS Fixture
then Replace
Display, PBA Key Flex Flip or Slider FPC Assy
If not then continue with
Display illumination Problems TRS guide



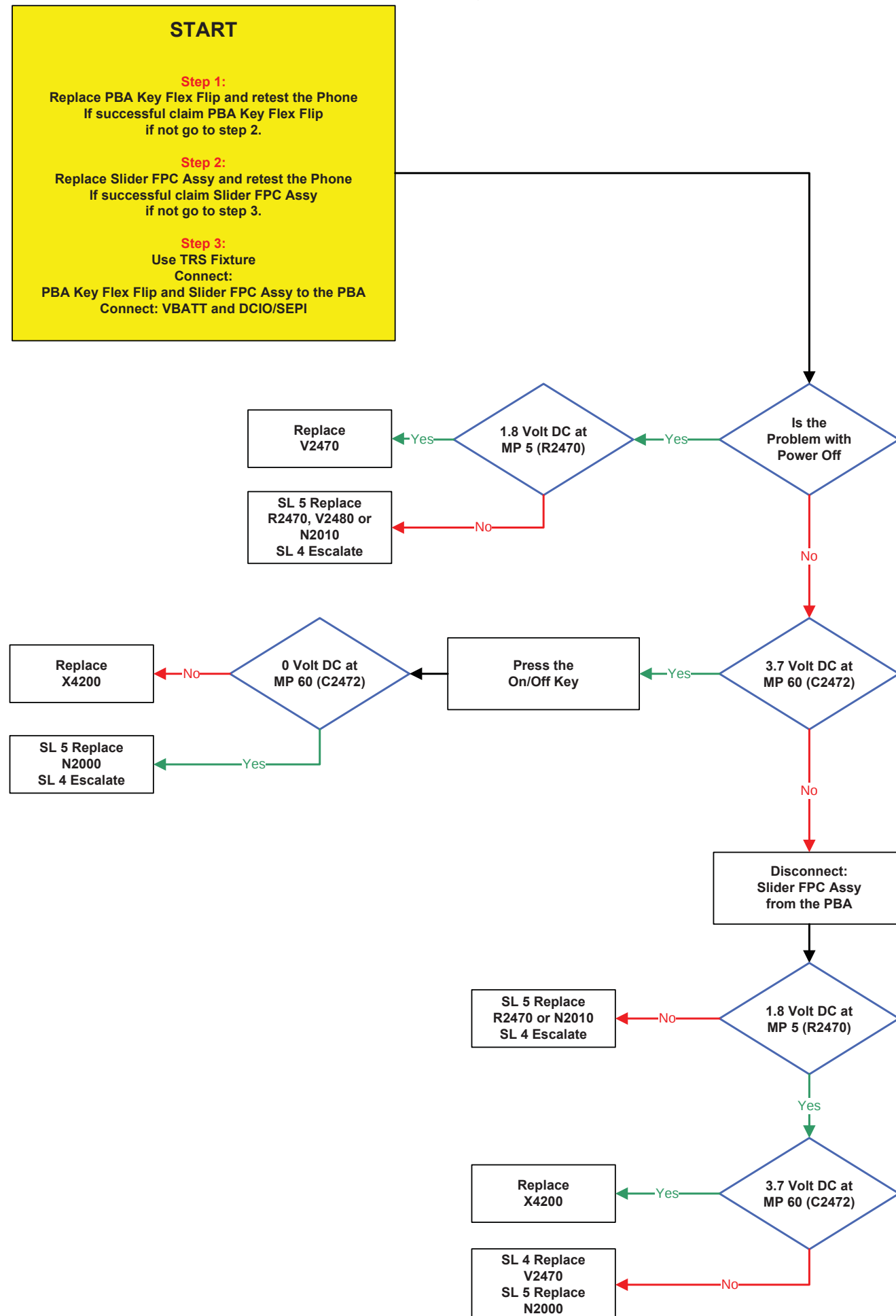
Display Illumination Problems



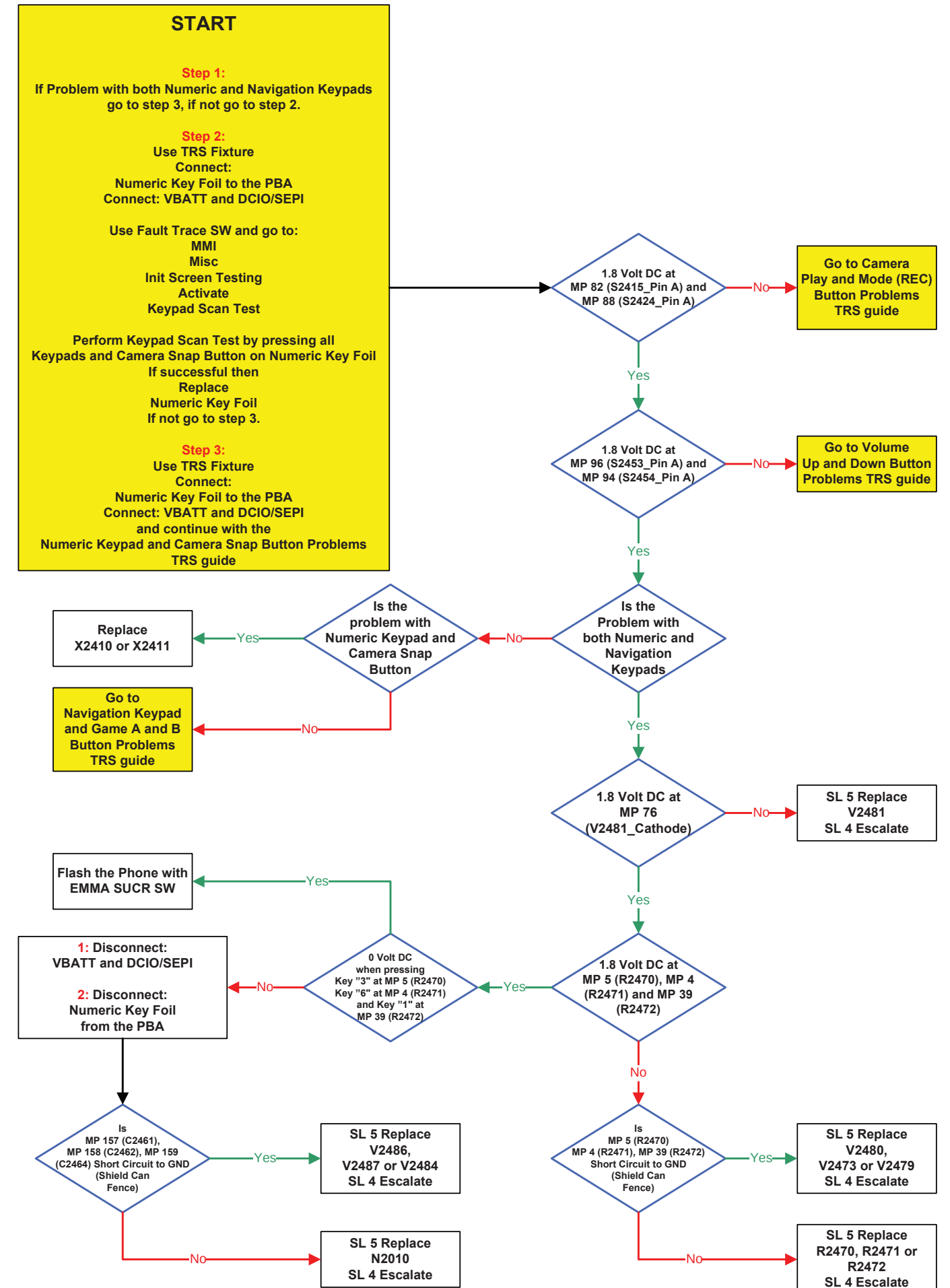
Opto Sensor Problems



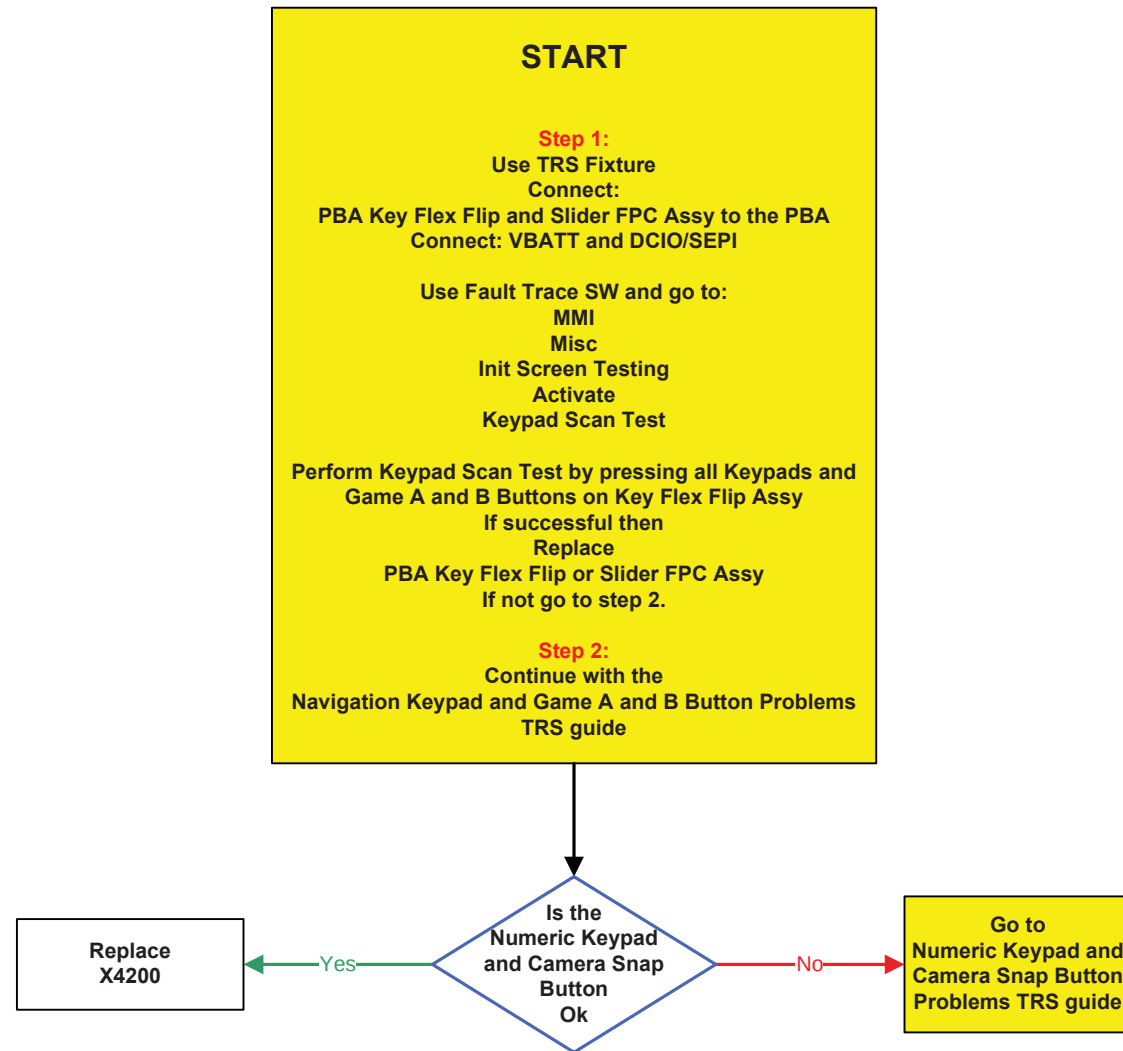
On-Off Key Problems



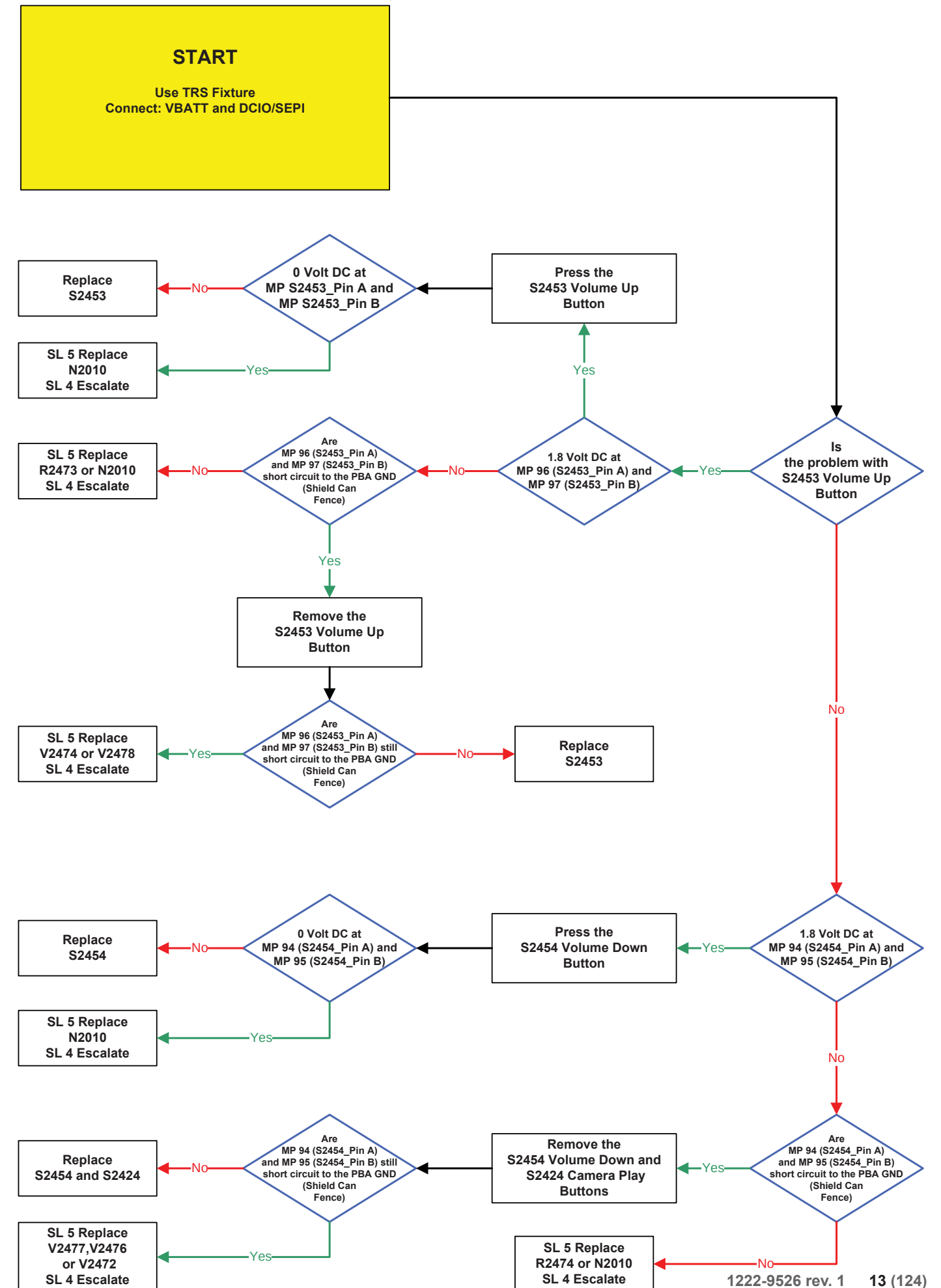
Numeric Keypad and Camera Snap Button Problems



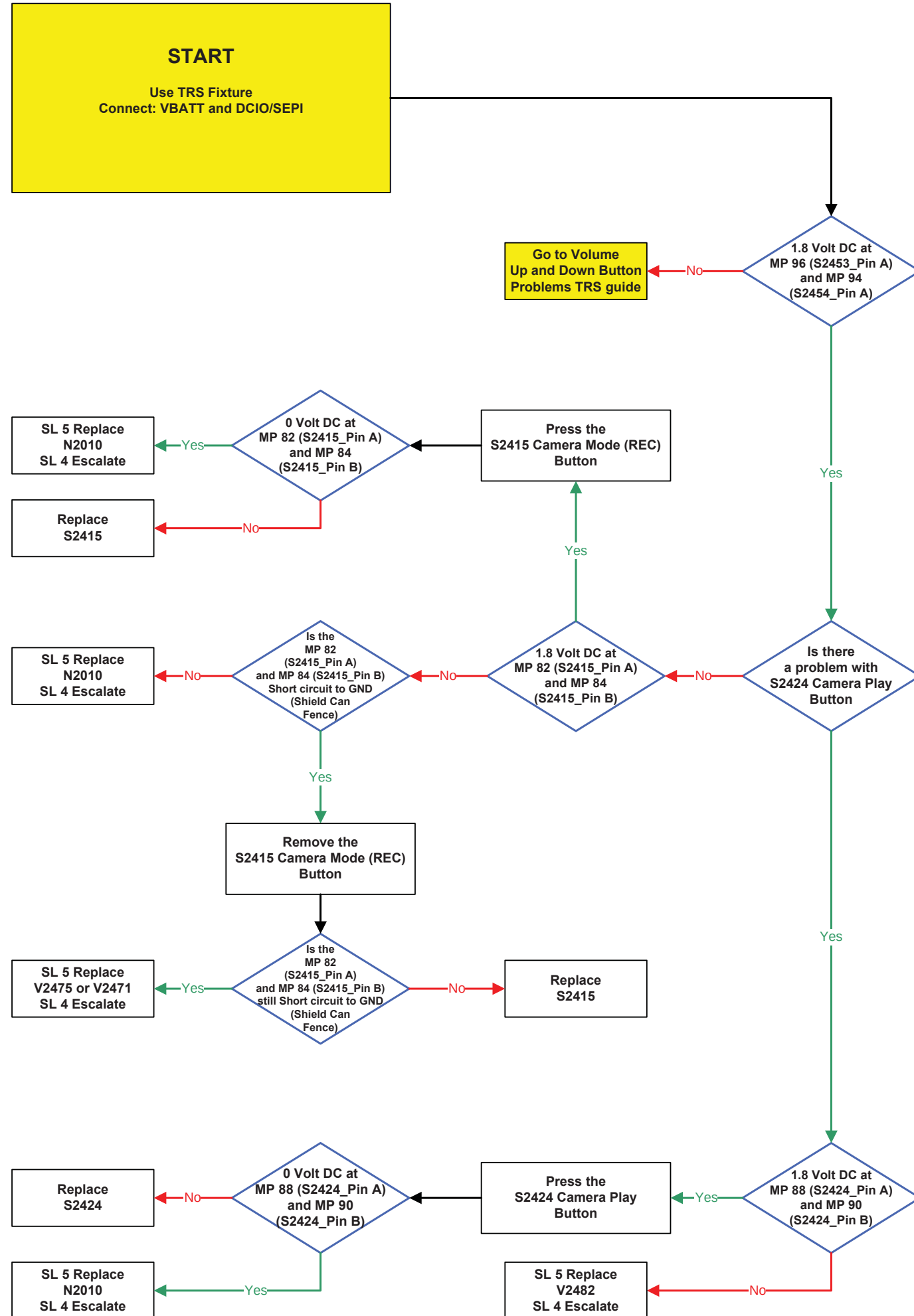
Navigation Keypad and Game A and B Button Problems



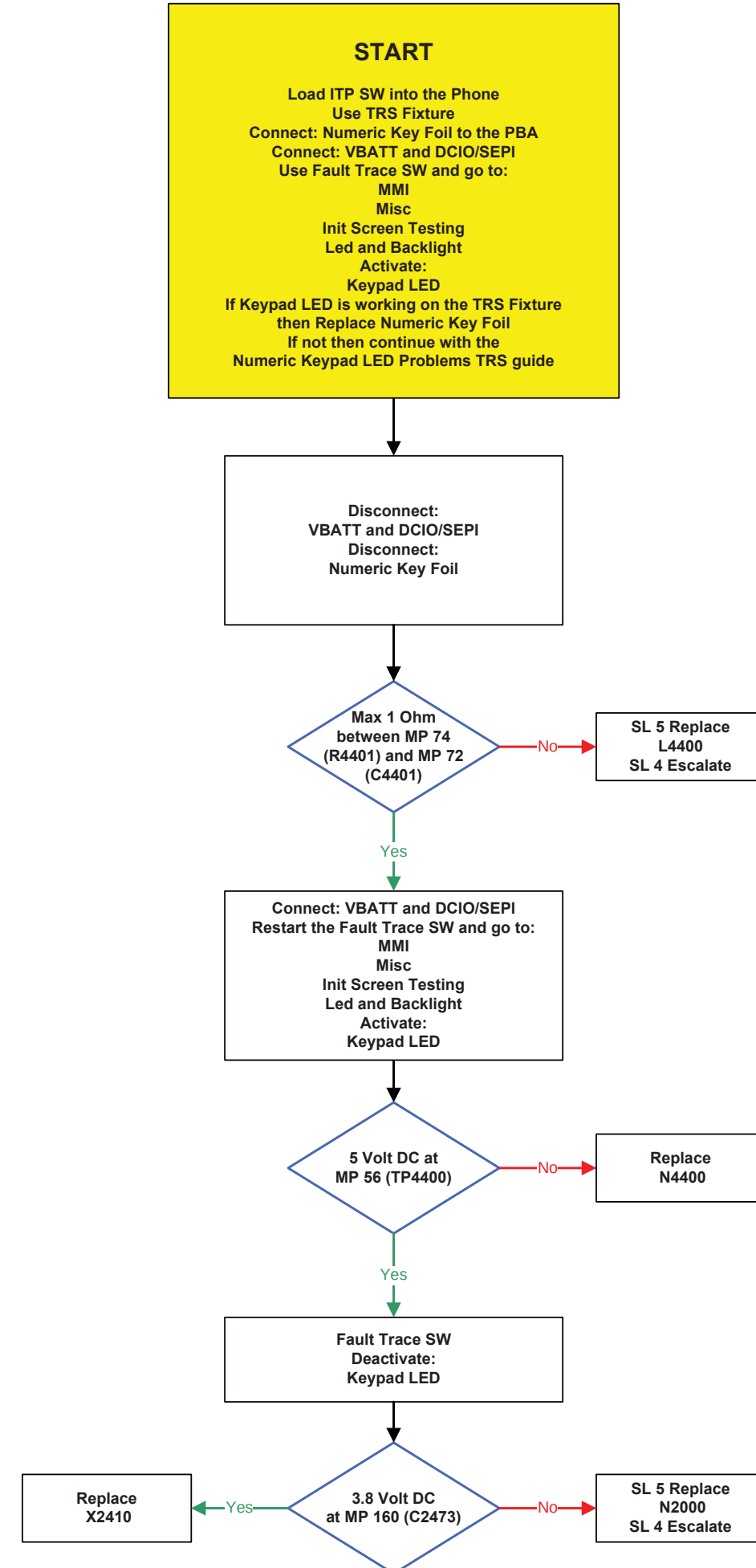
Volume Up and Down Button Problems



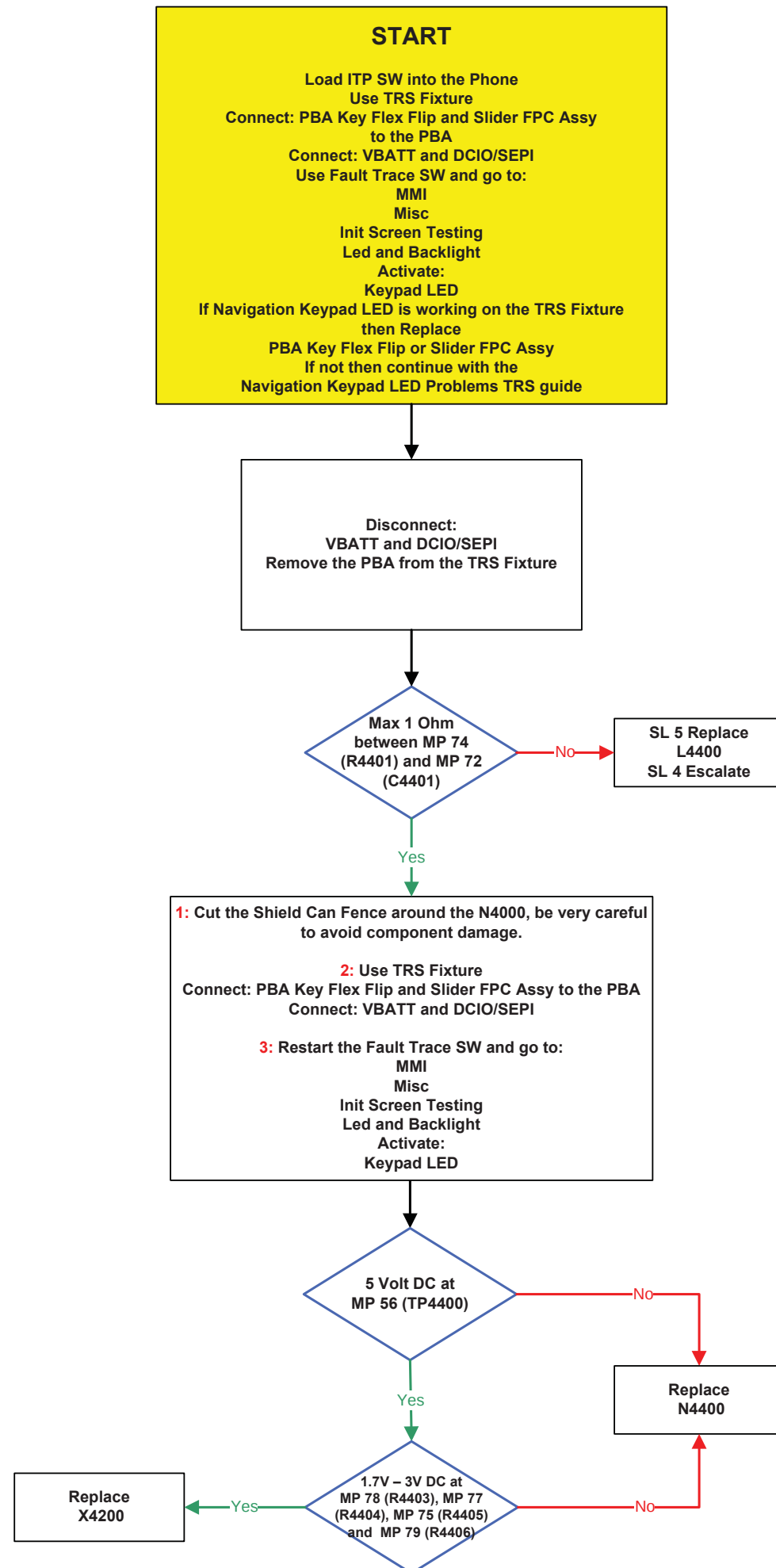
Camera Play and Mode (REC) Button Problems



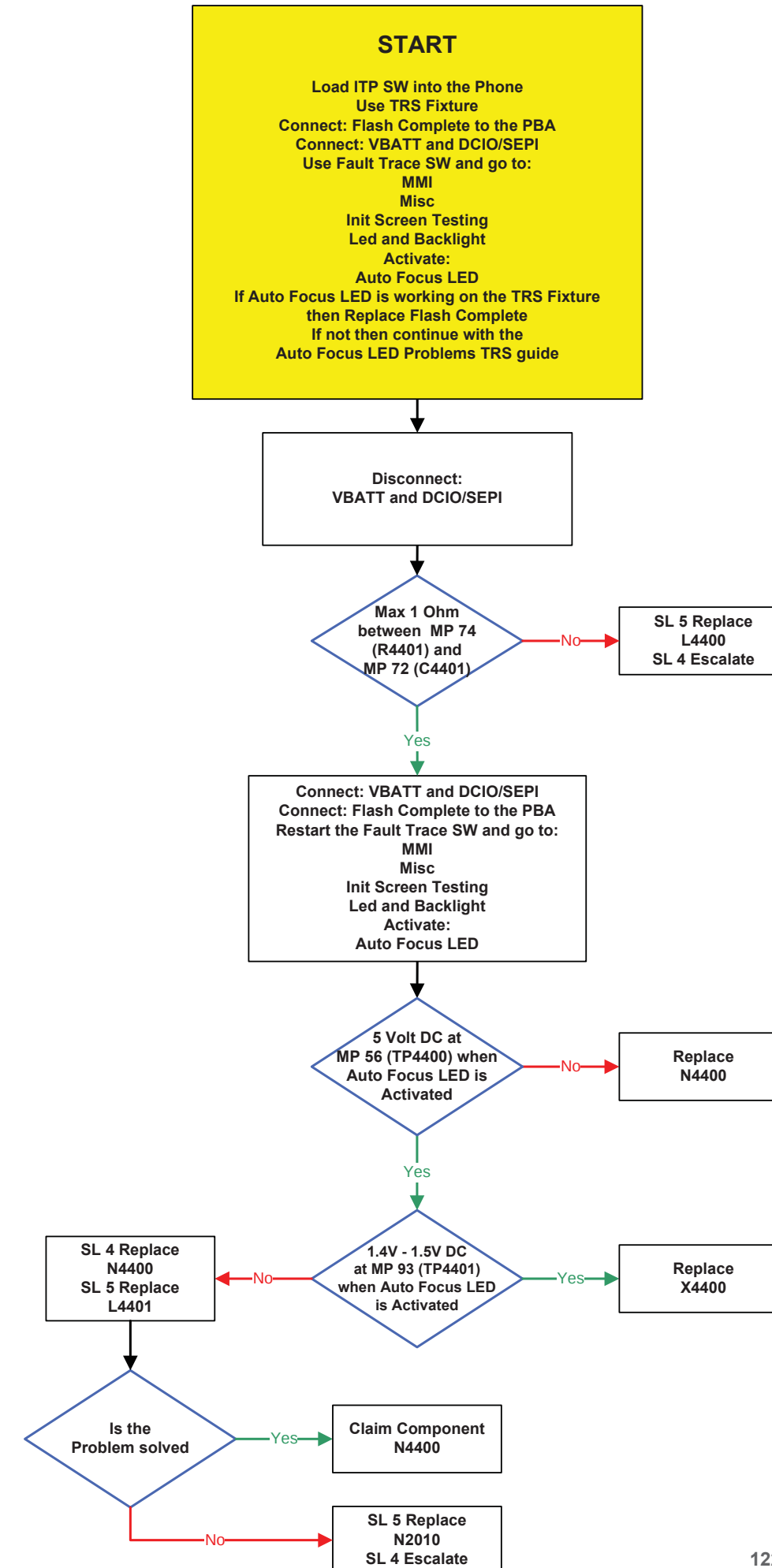
Numeric Keypad LED Problems



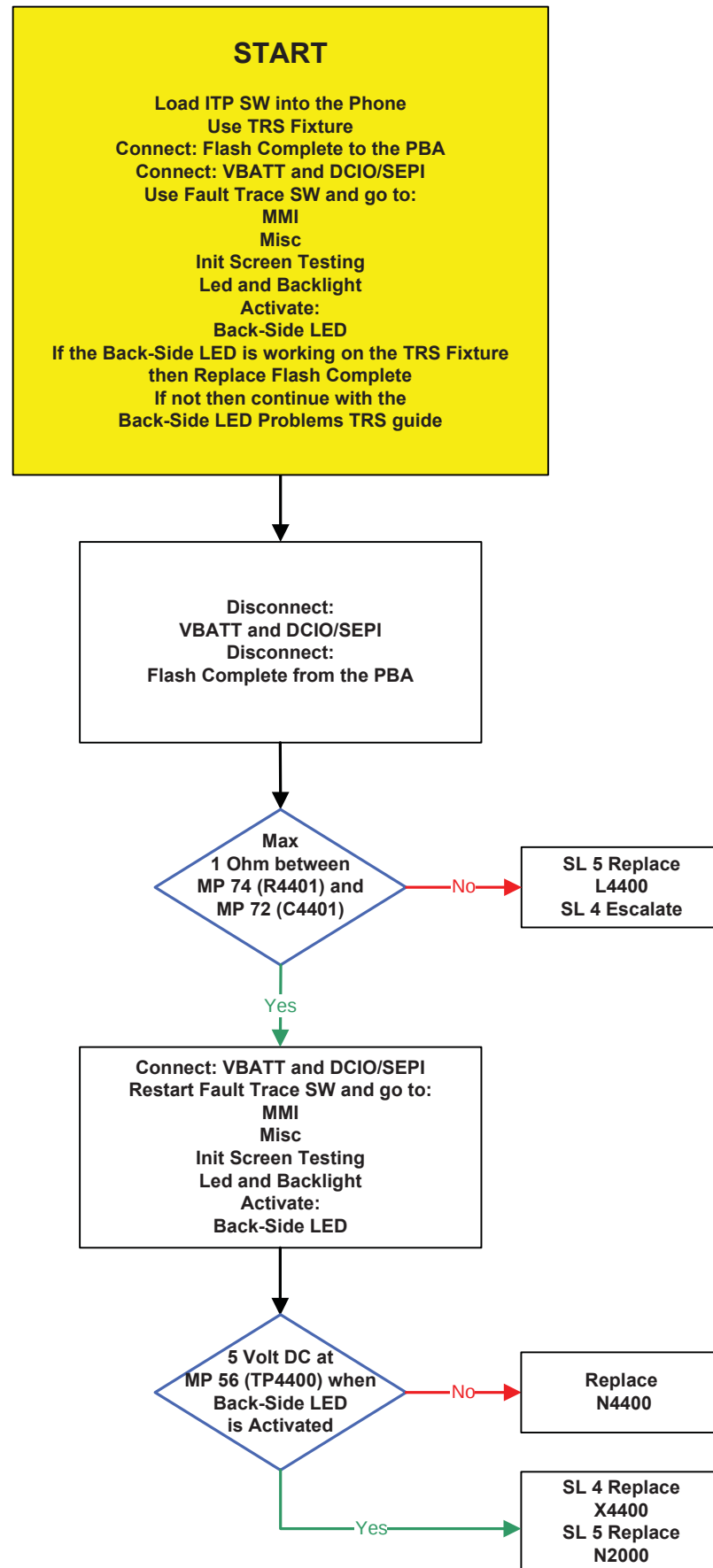
Navigation Keypad LED Problems



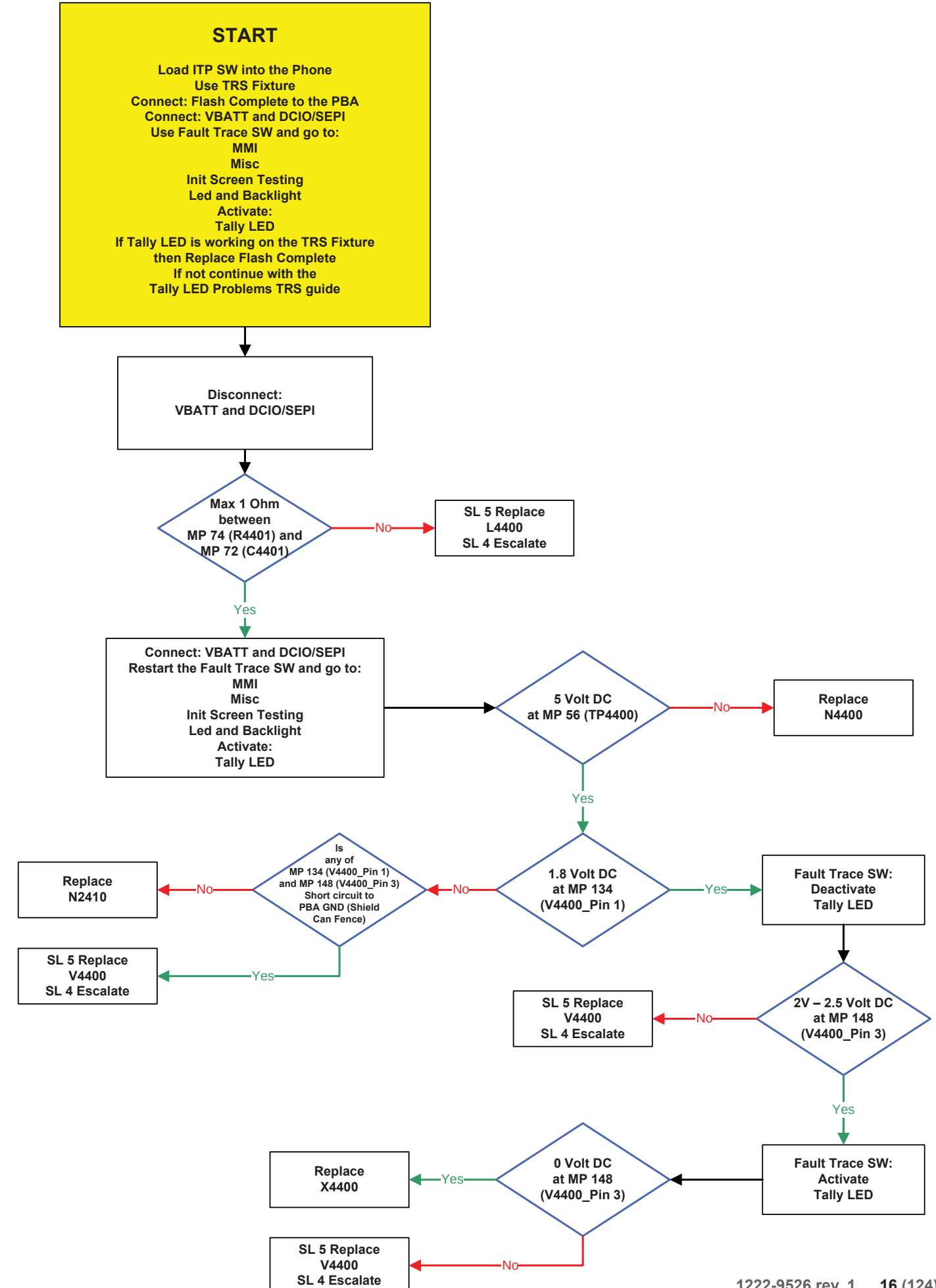
Auto Focus LED Problems



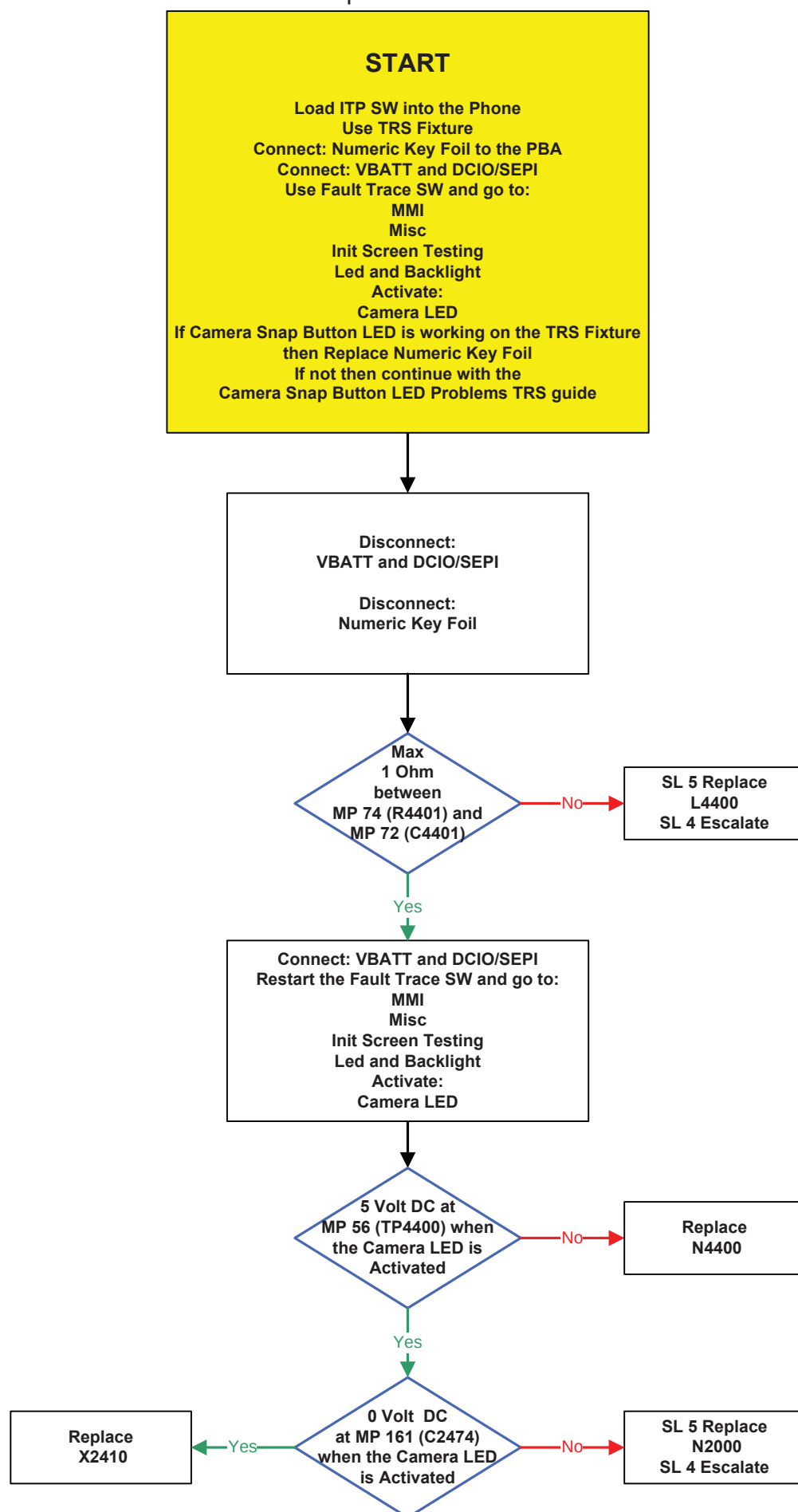
Back-Side LED Problems



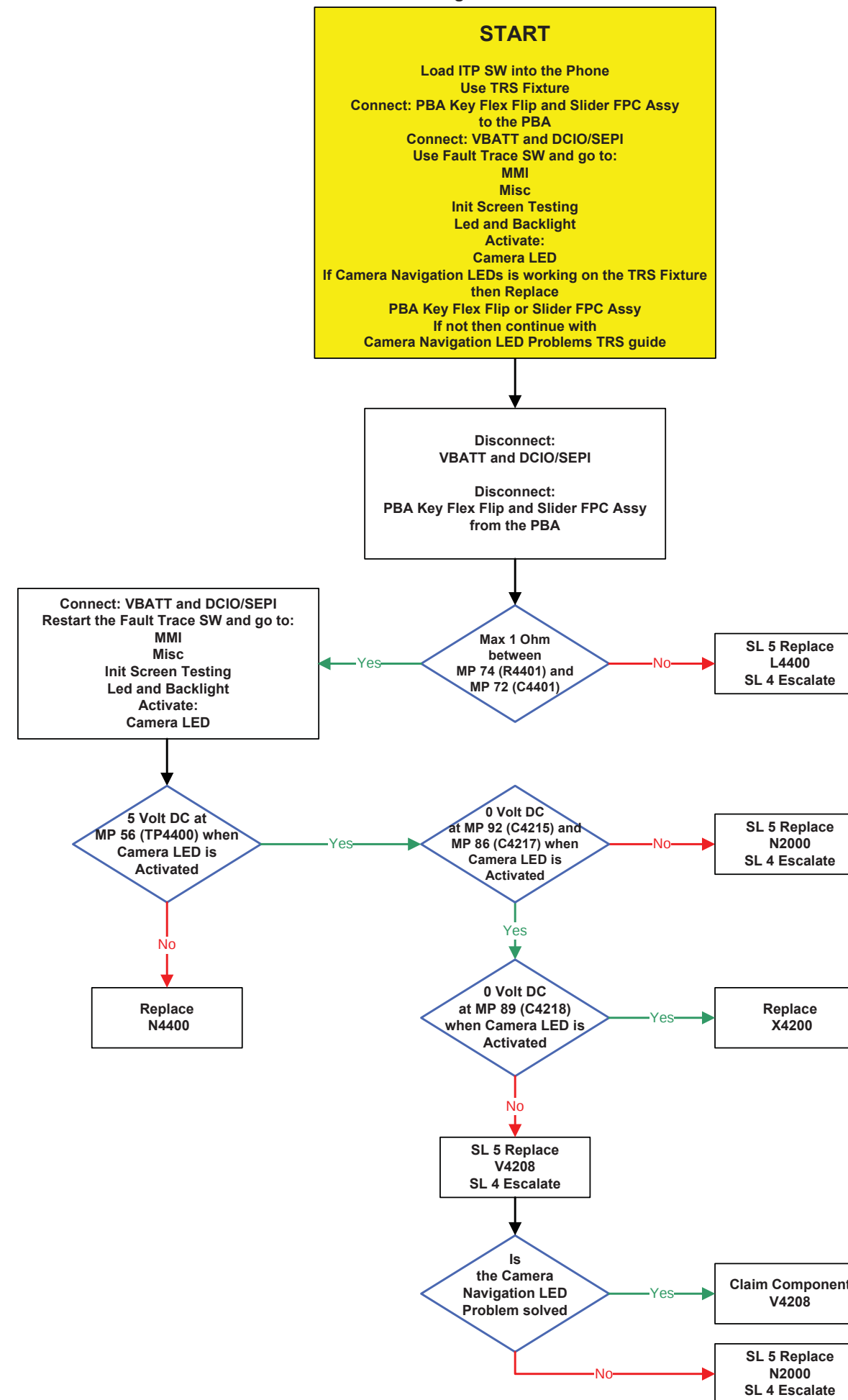
Tally LED Problems



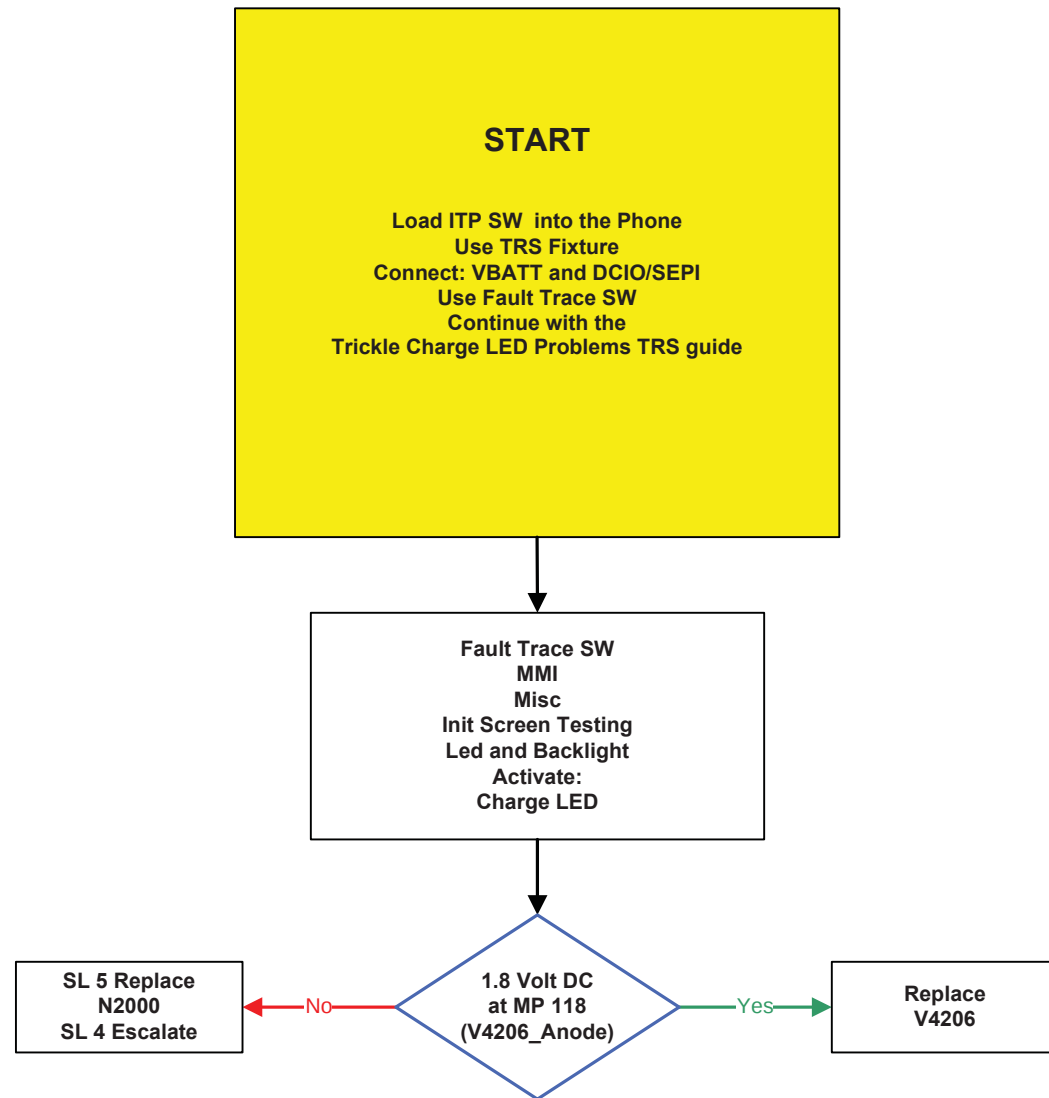
Camera Snap Button LED Problems



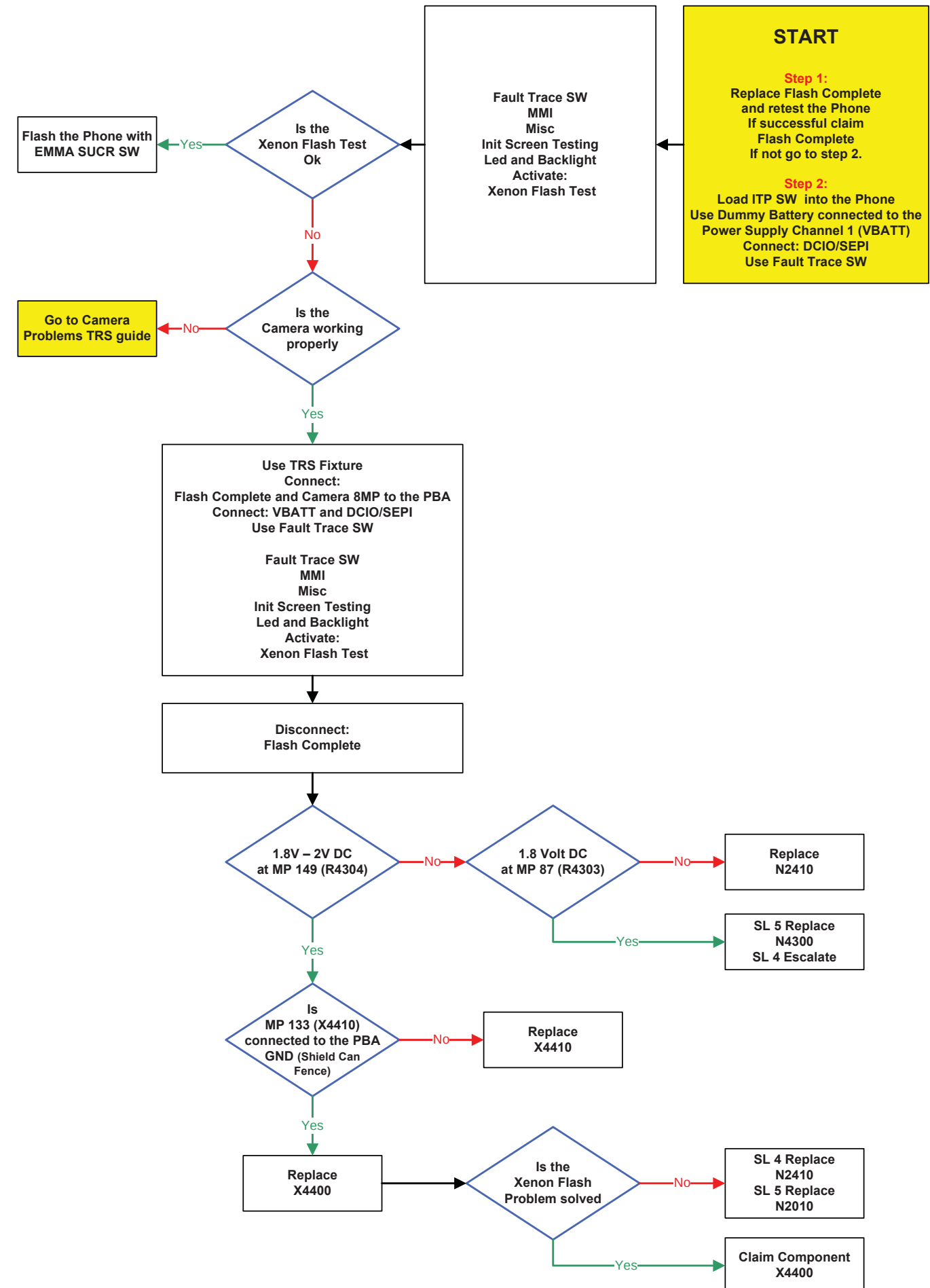
Camera Navigation LED Problems



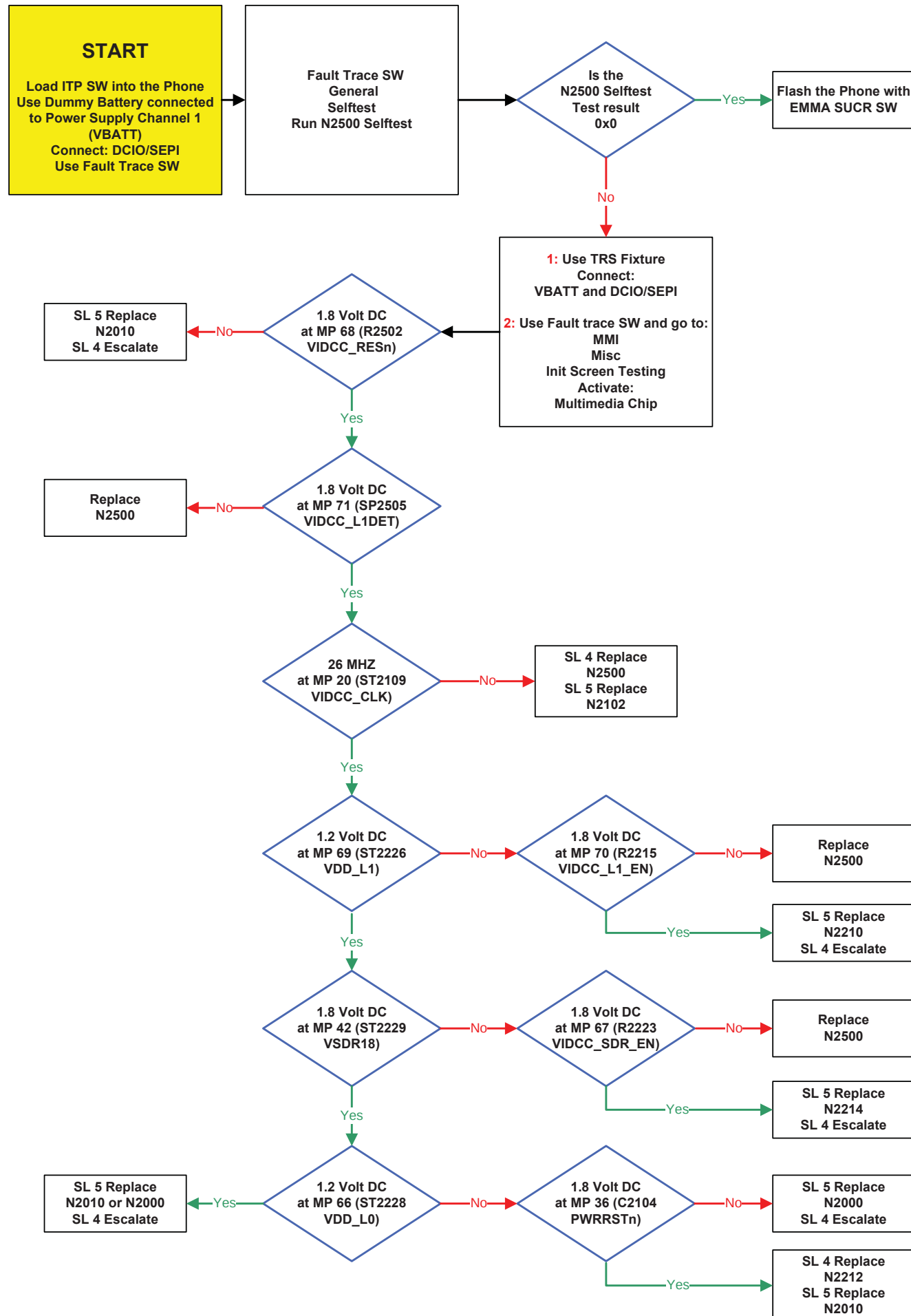
Trickle Charge LED Problems



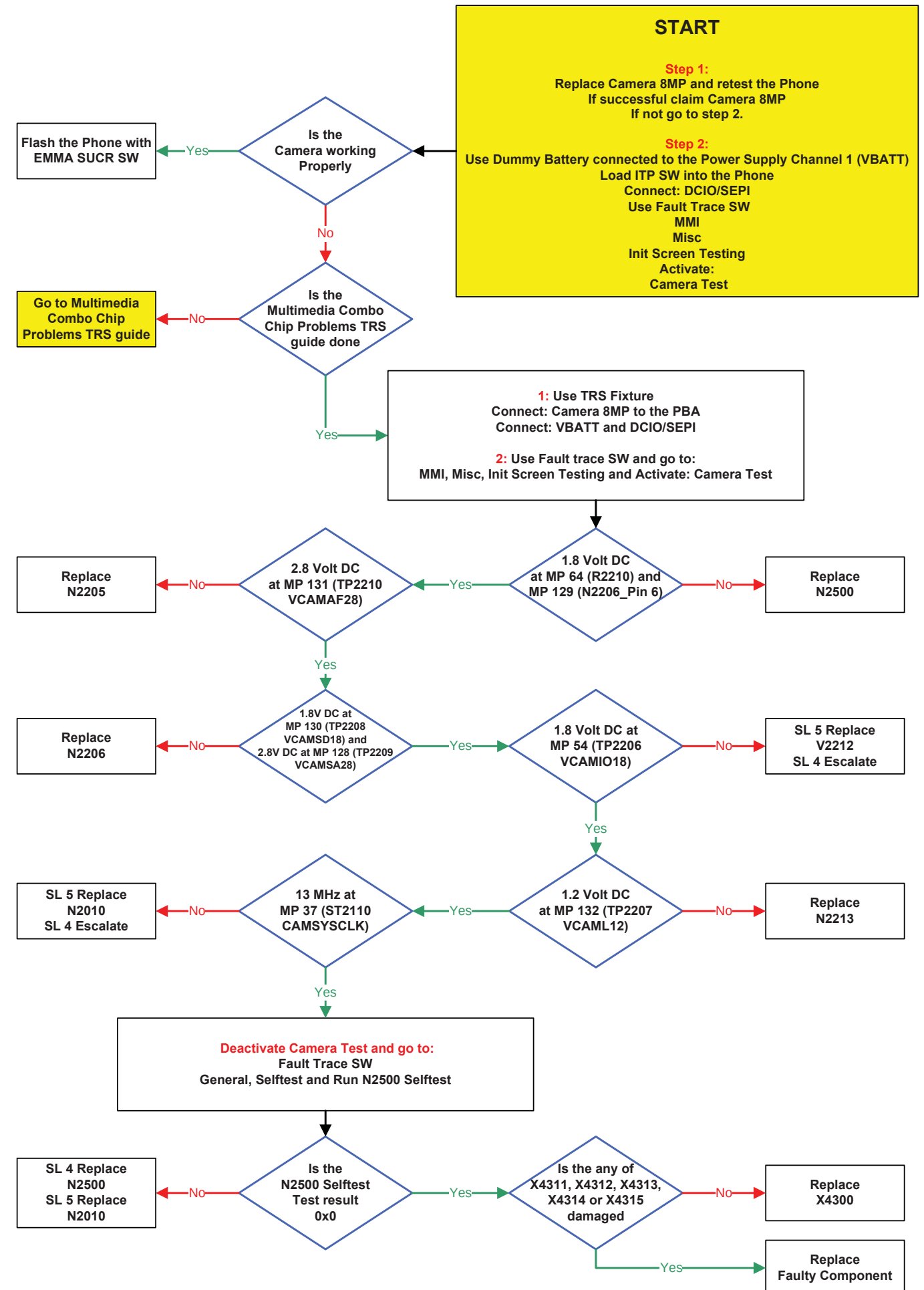
Xenon Flash Problems



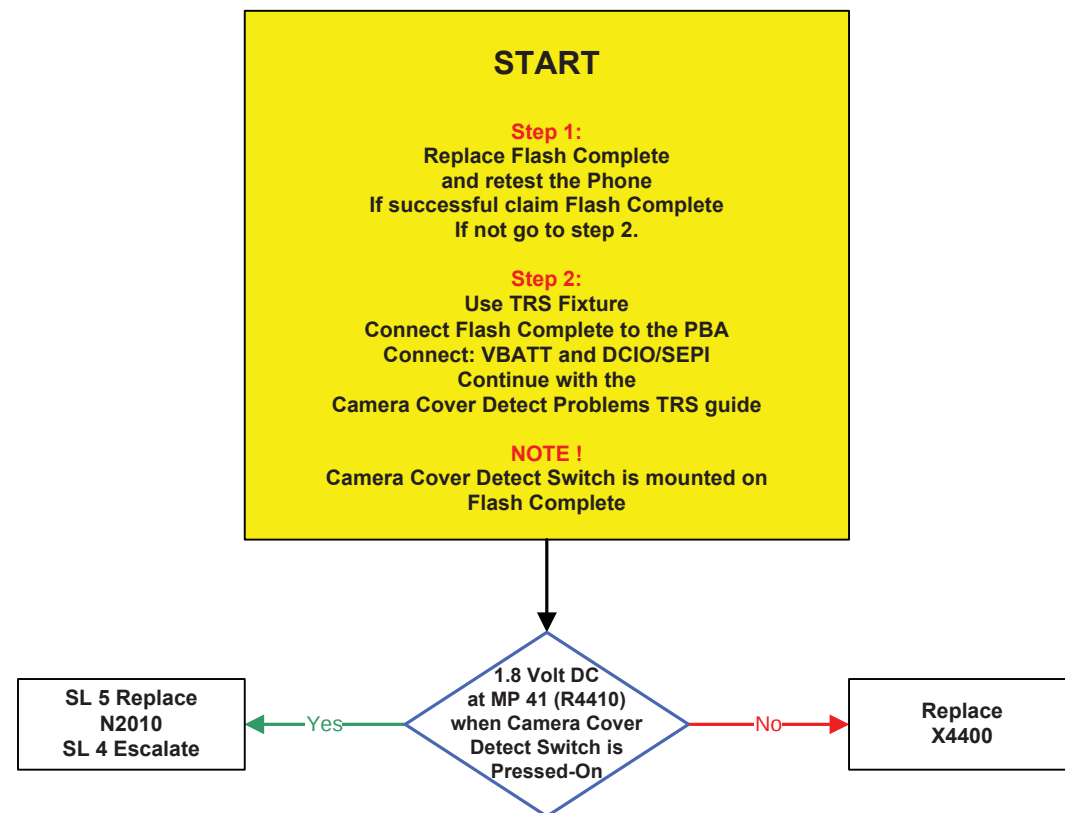
Multimedia Combo Chip Problems



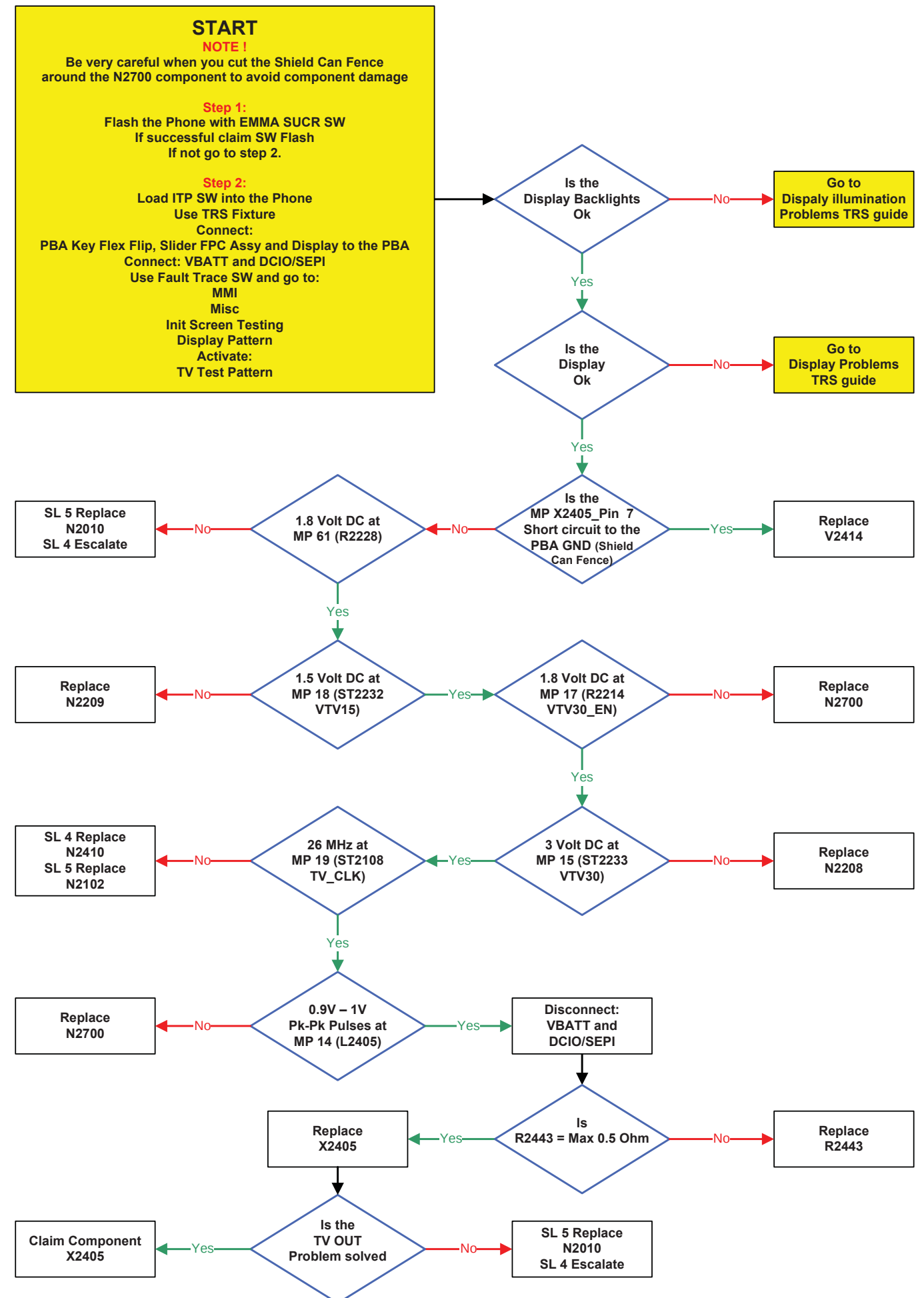
Camera Problems



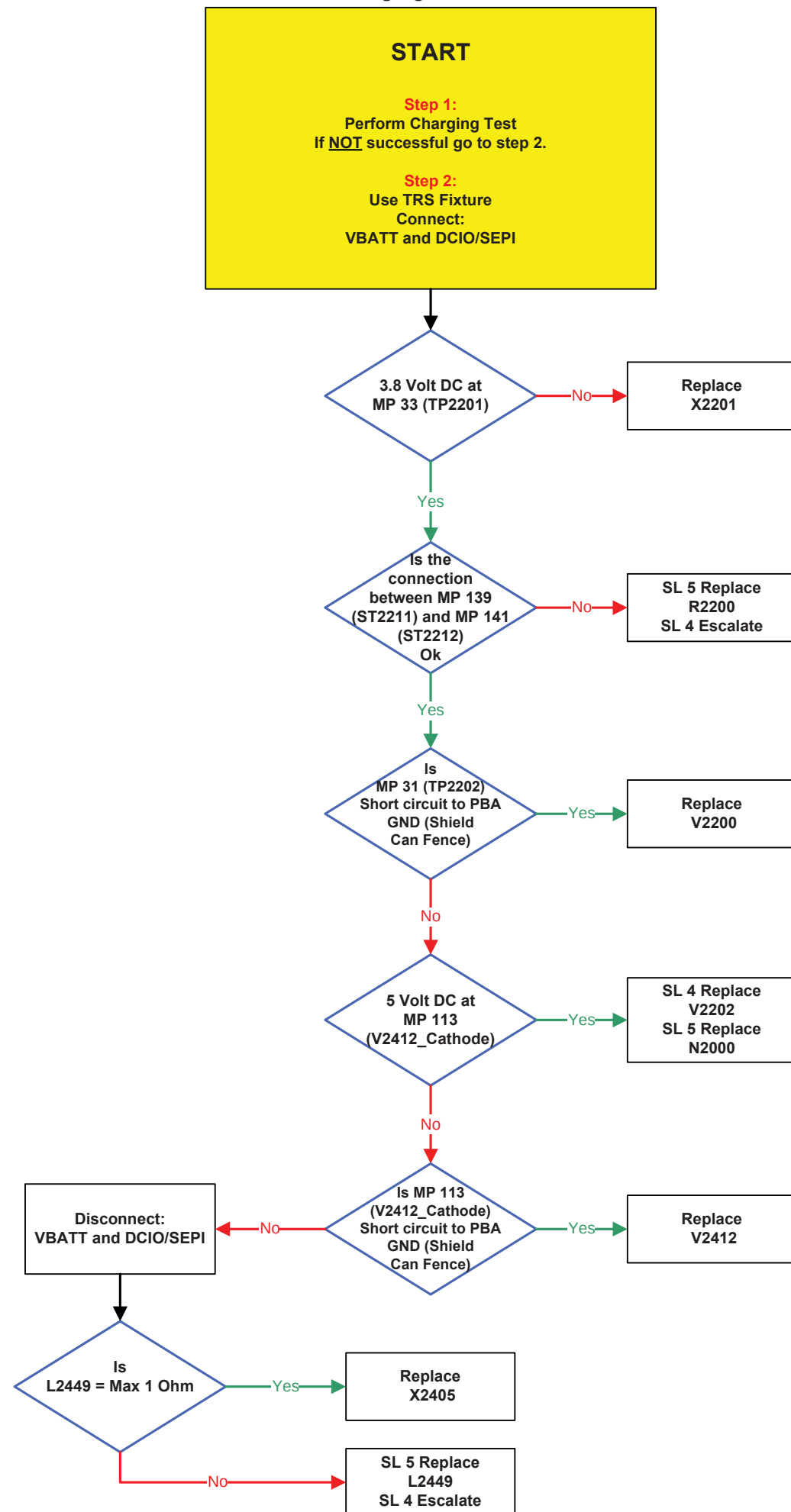
Camera Cover Detect Problems



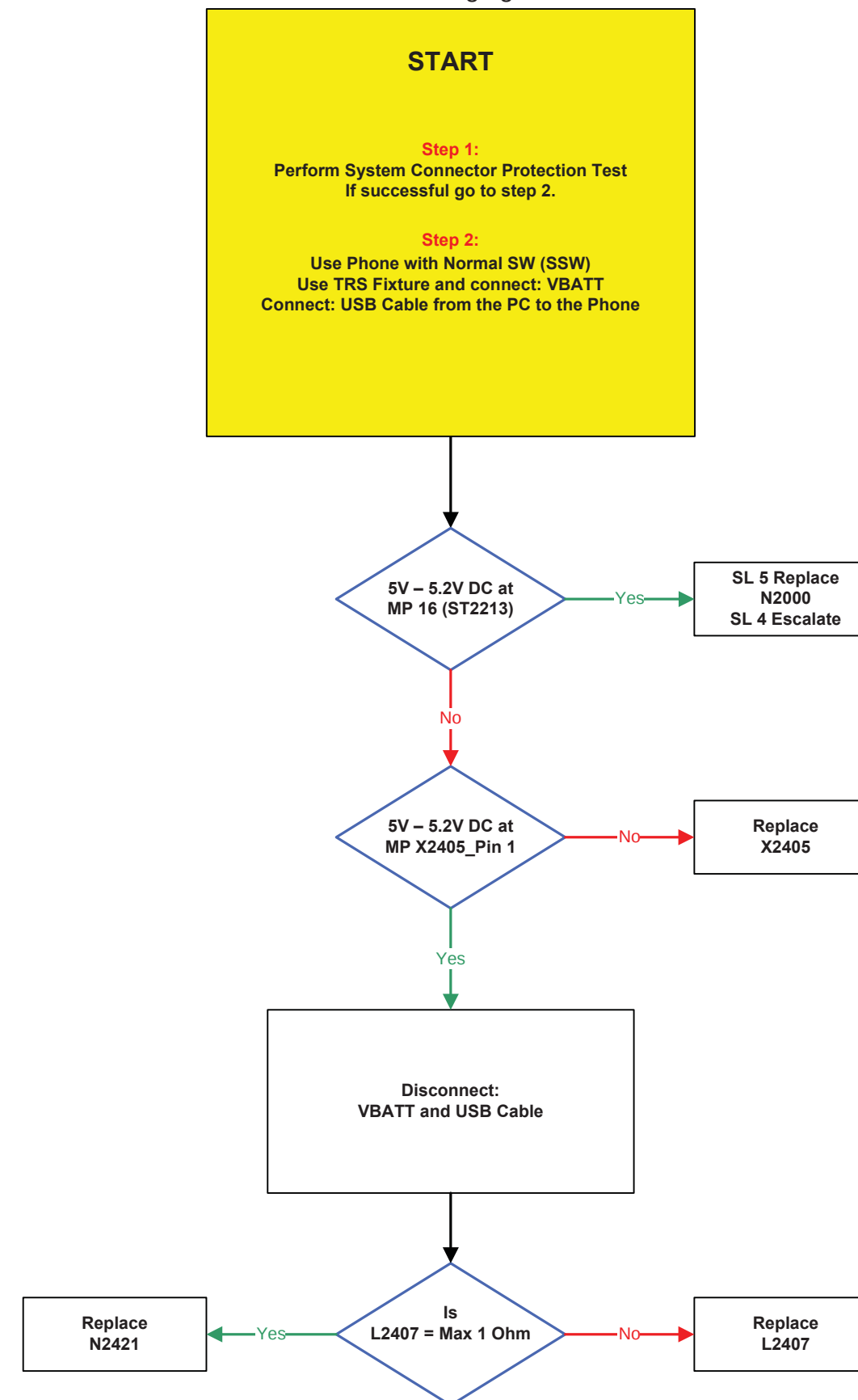
TV OUT Problems



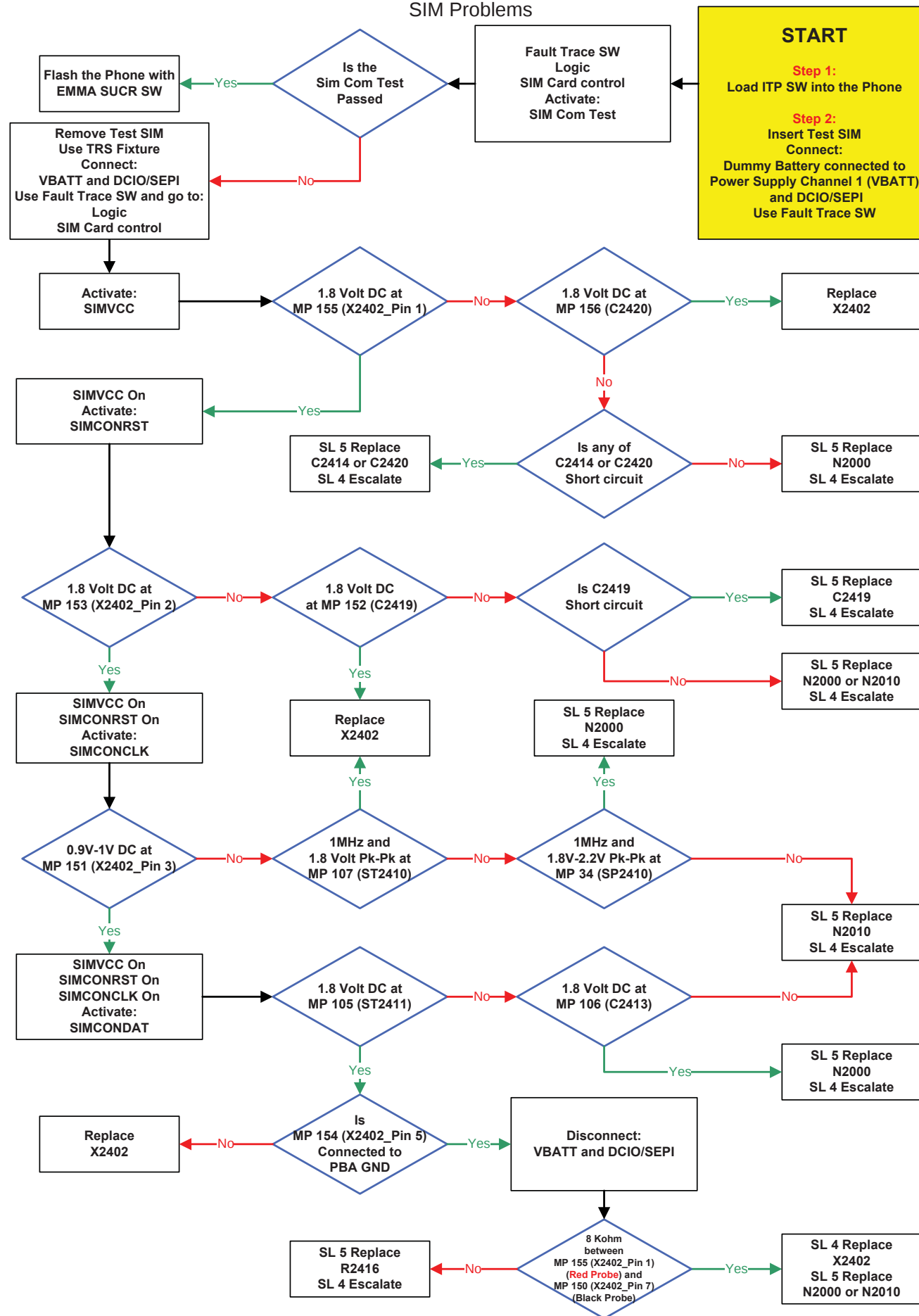
Charging Problems



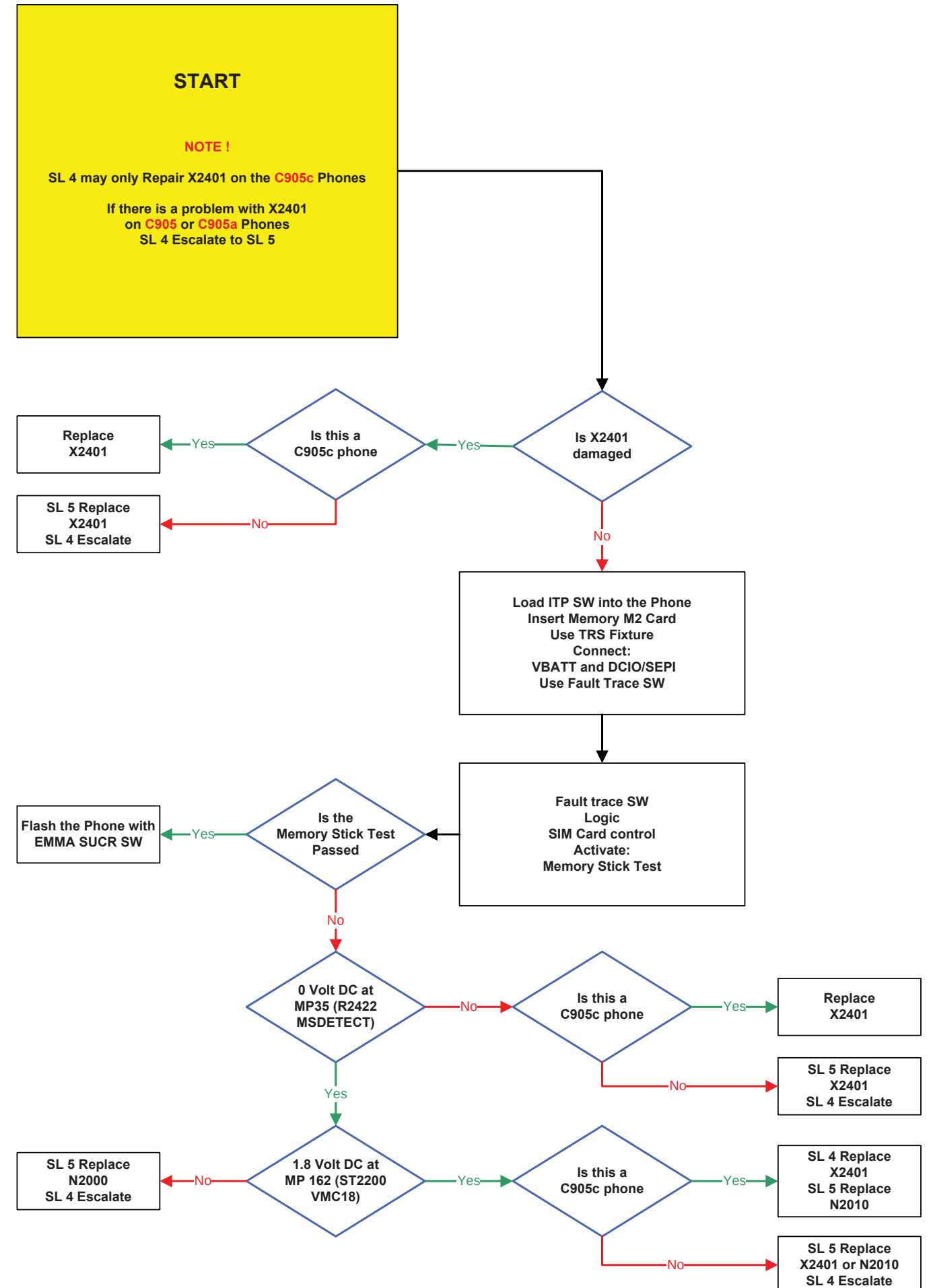
USB/VBUS Charging Problems



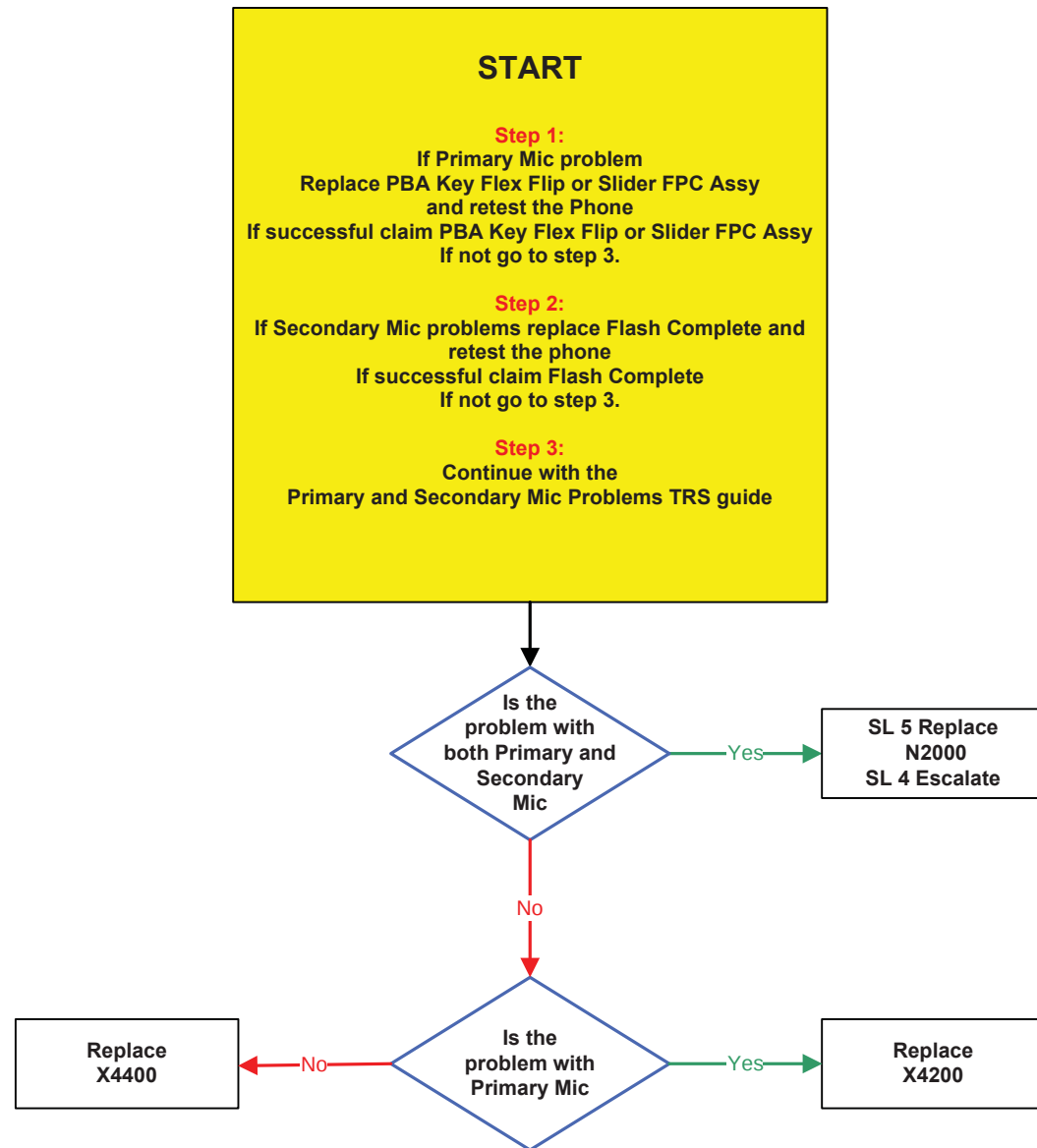
SIM Problems



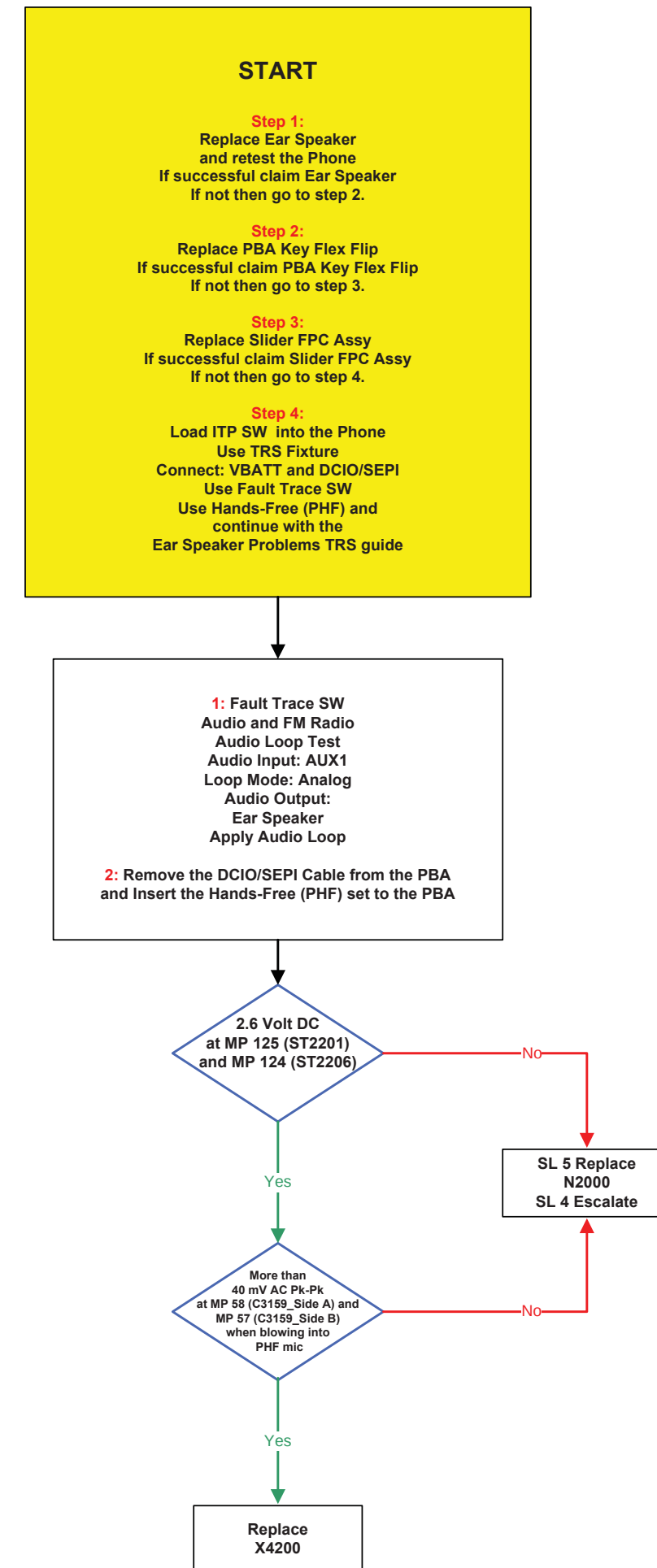
Memory Stick Problems



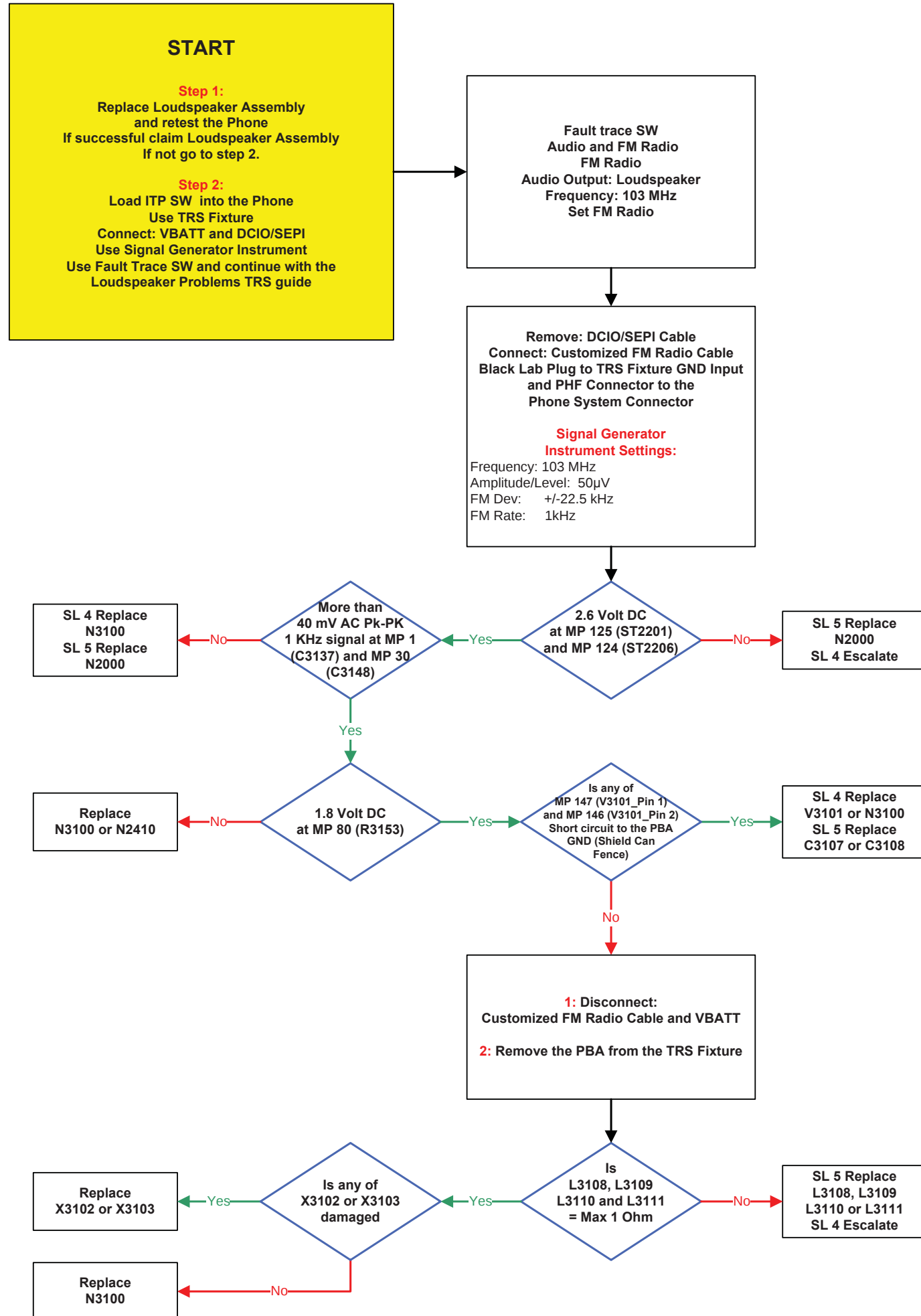
Primary and Secondary Mic Problems



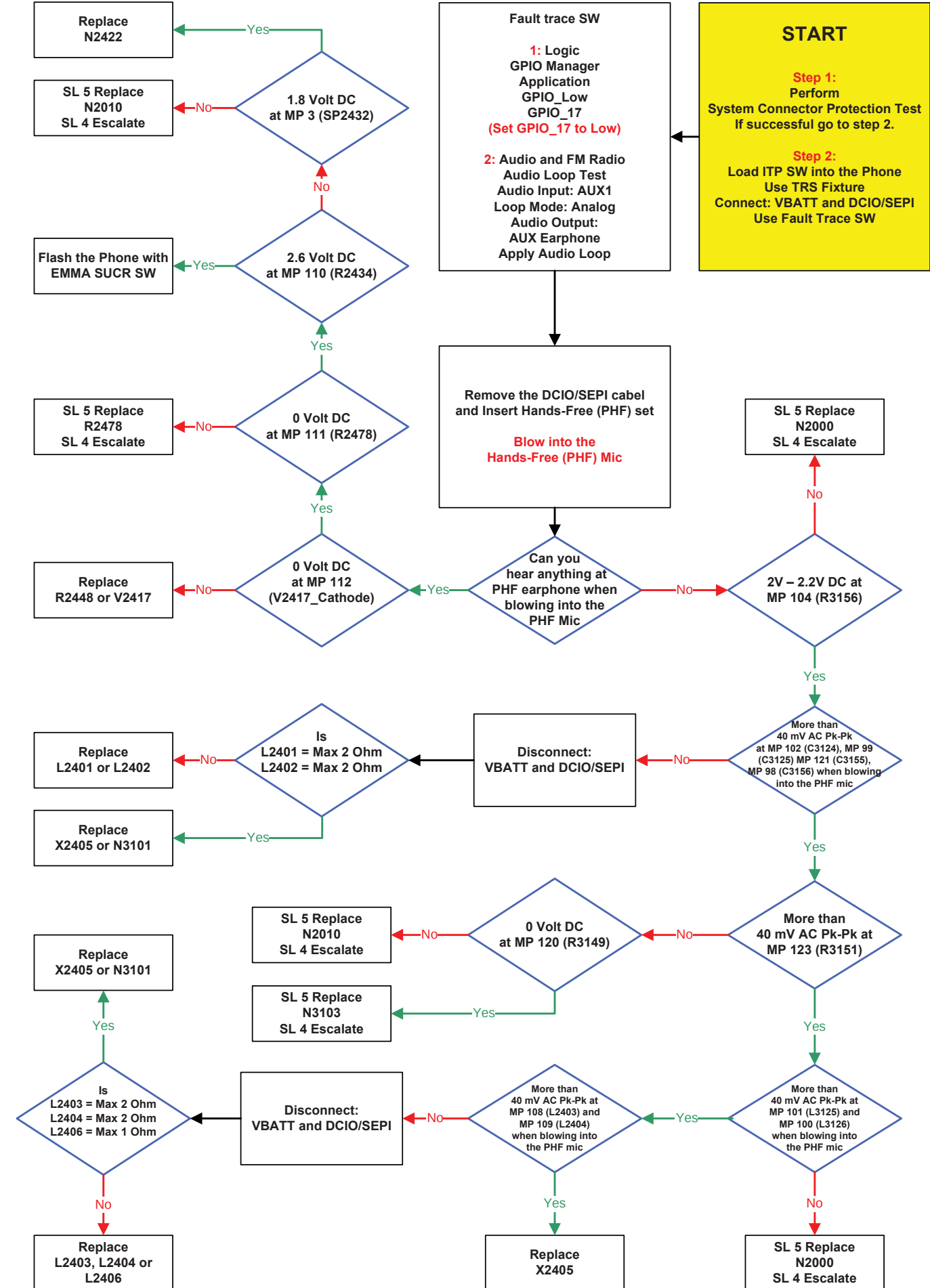
Ear Speaker Problems



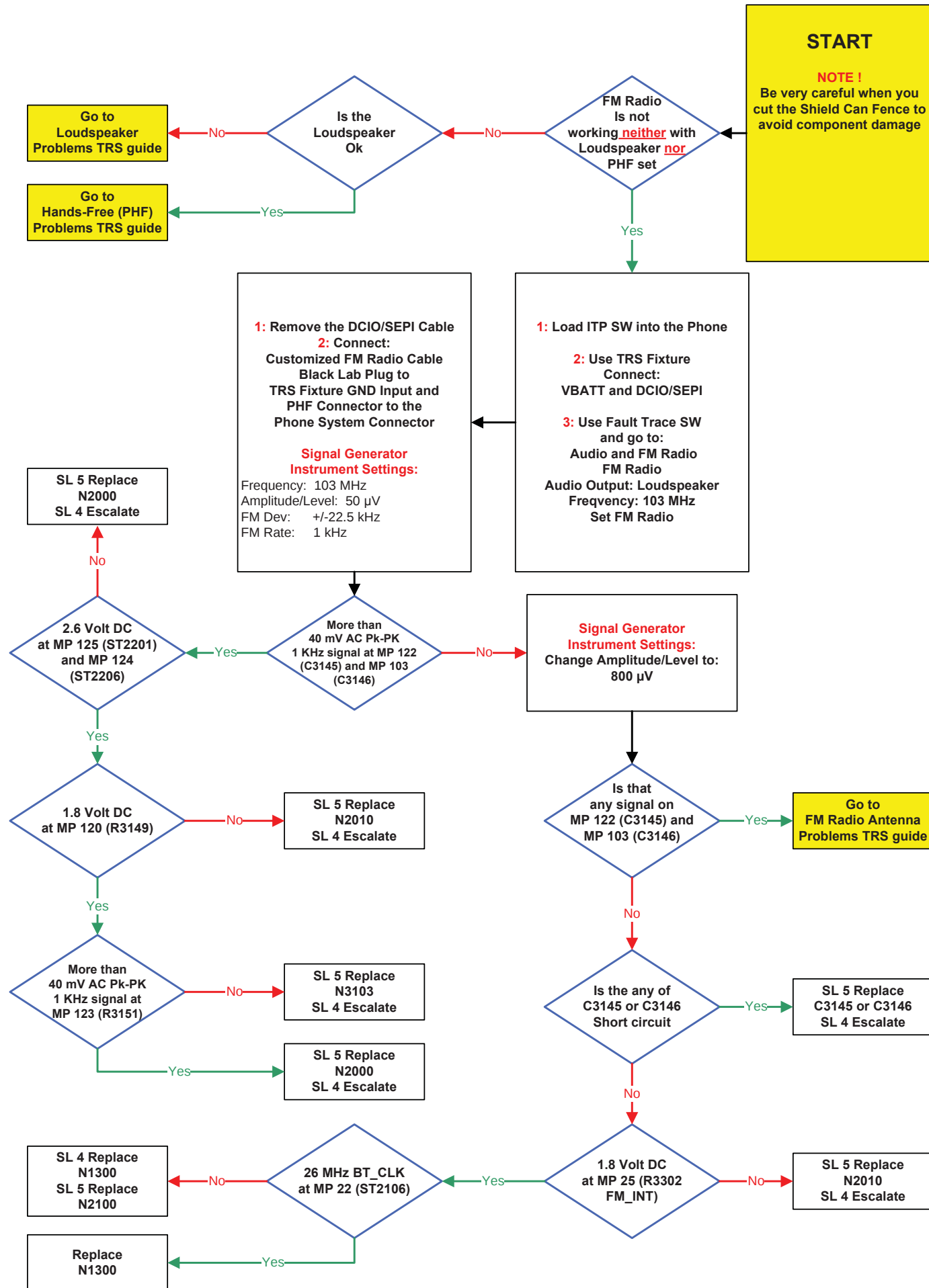
Loudspeaker Problems



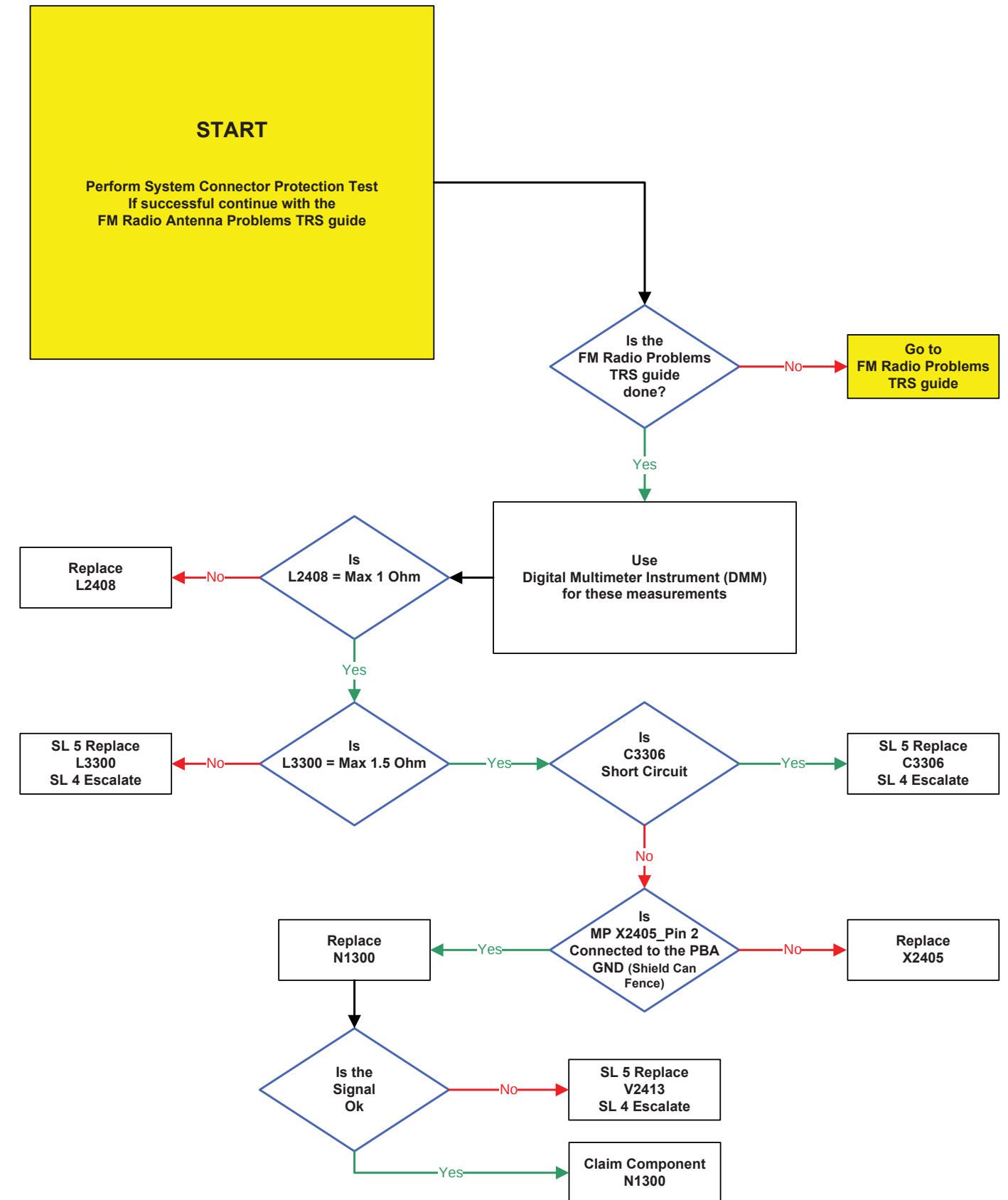
Hands-Free (PHF) Problems



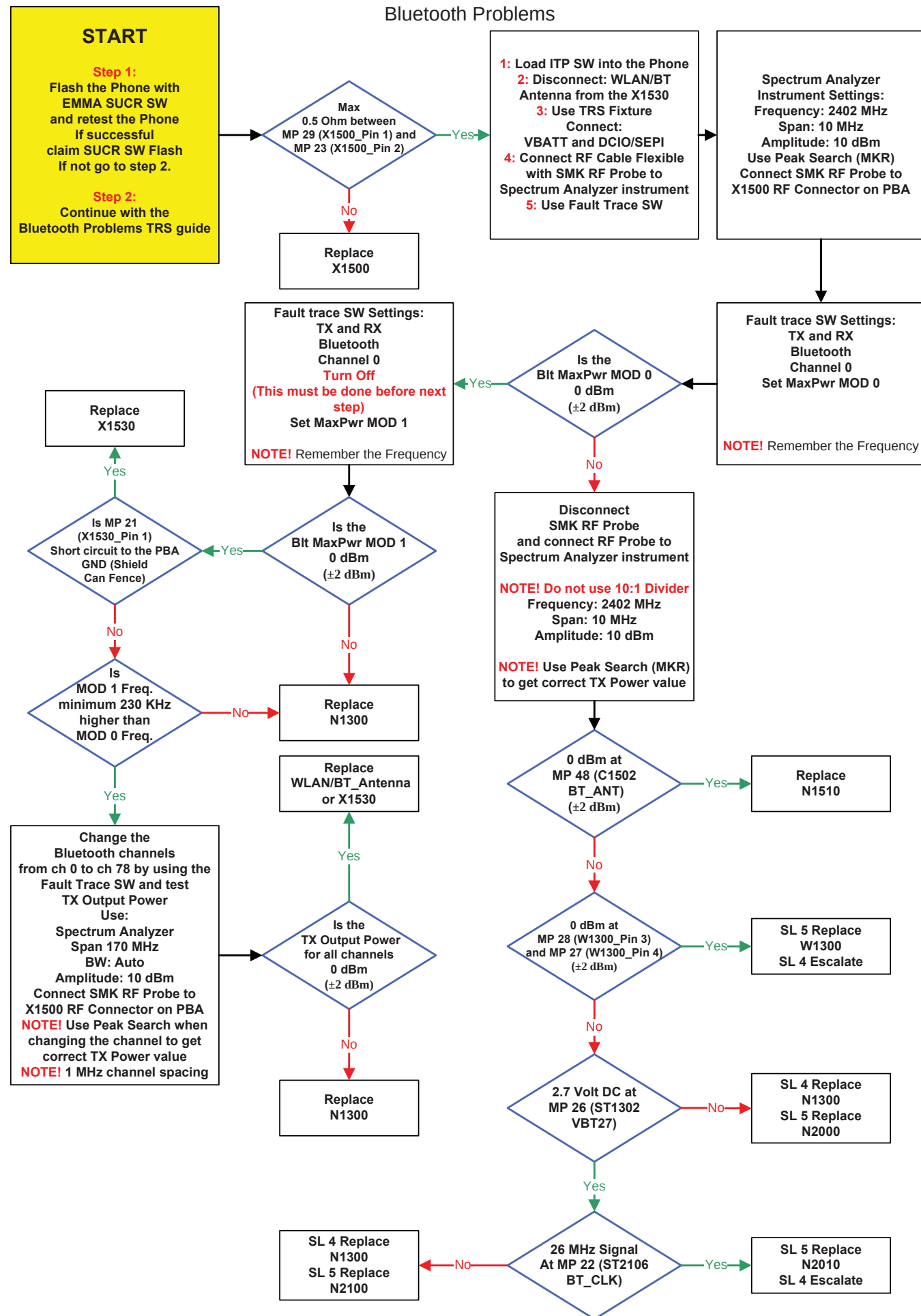
FM Radio Problems



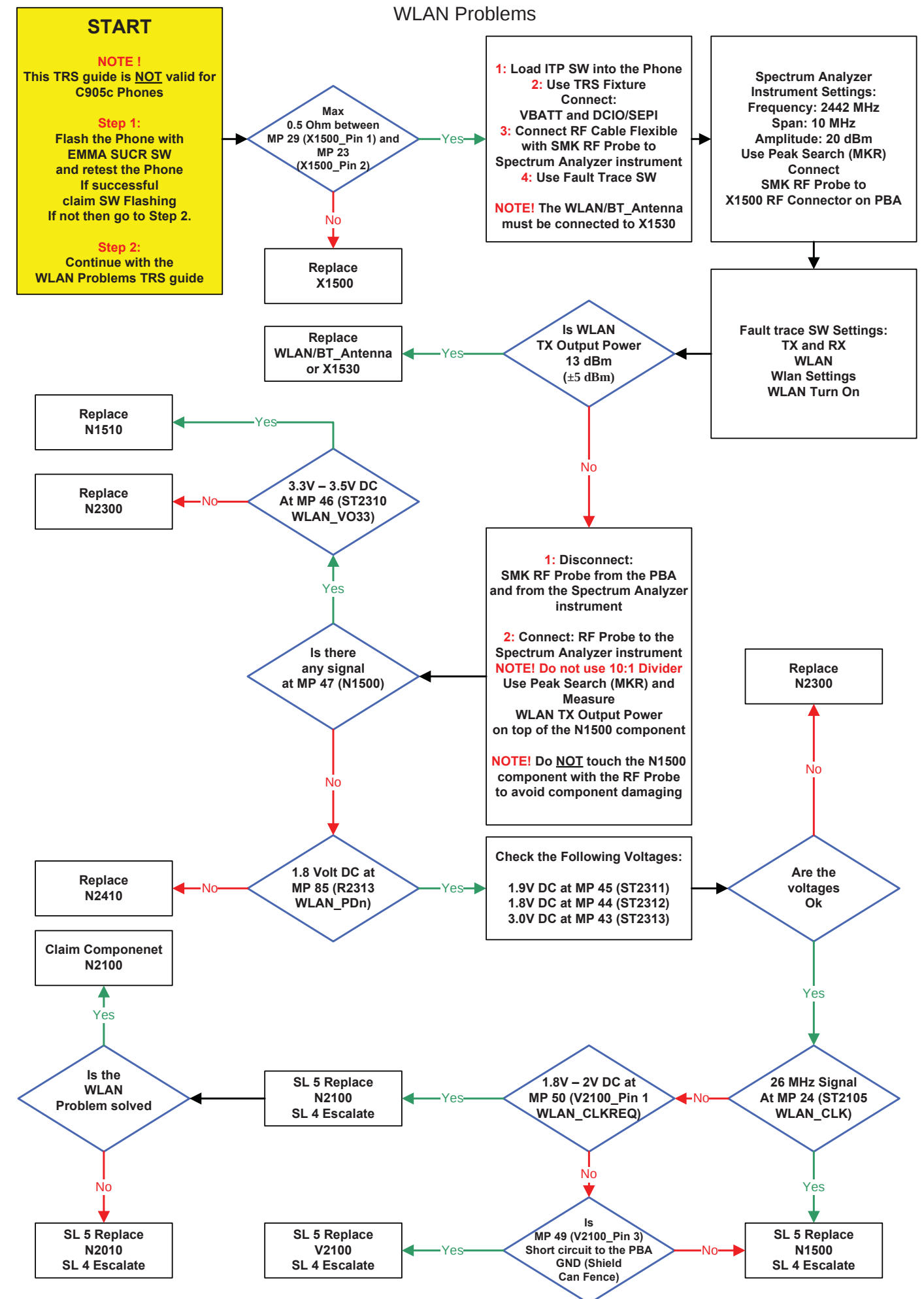
FM Radio Antenna Problems



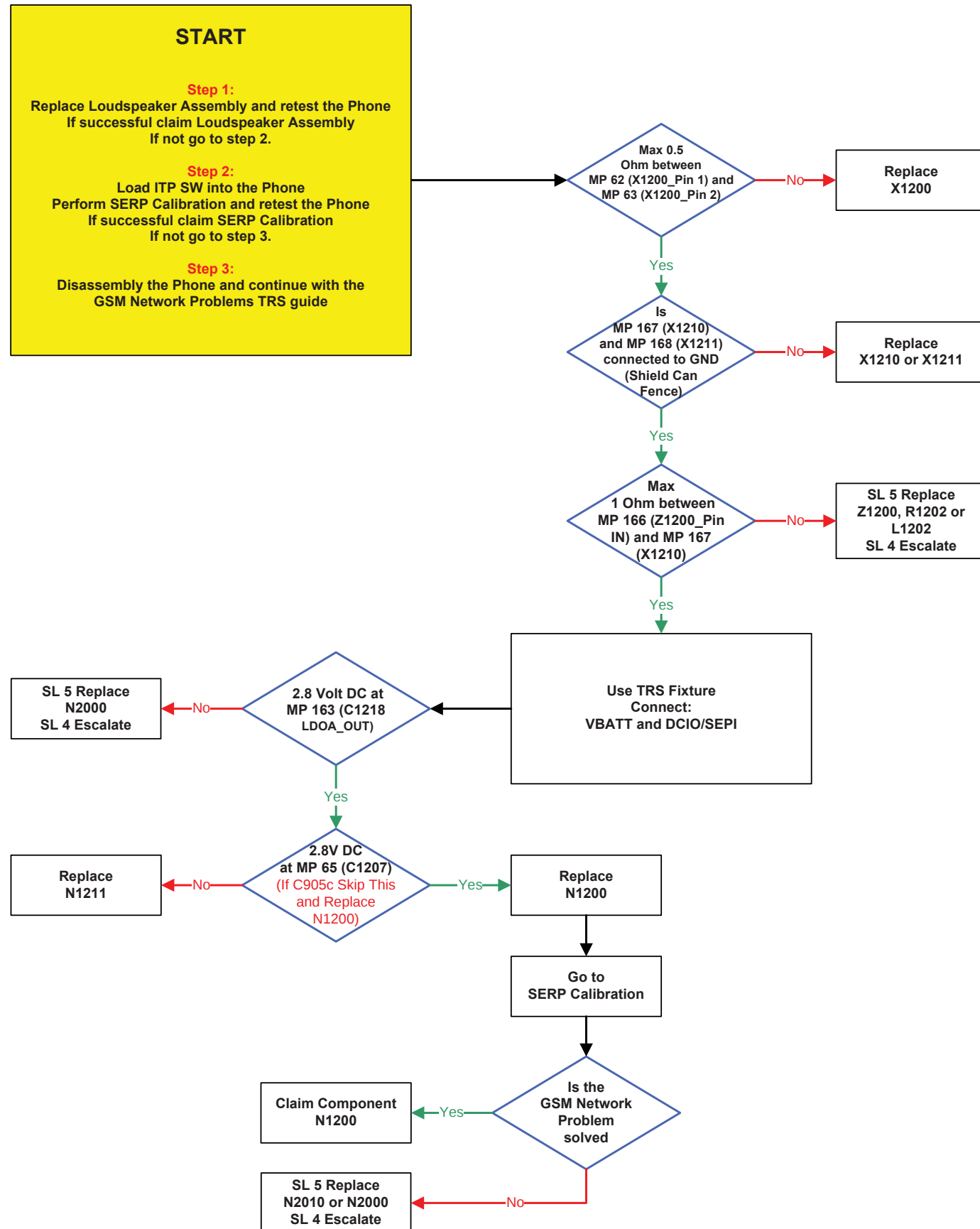
Bluetooth Problems



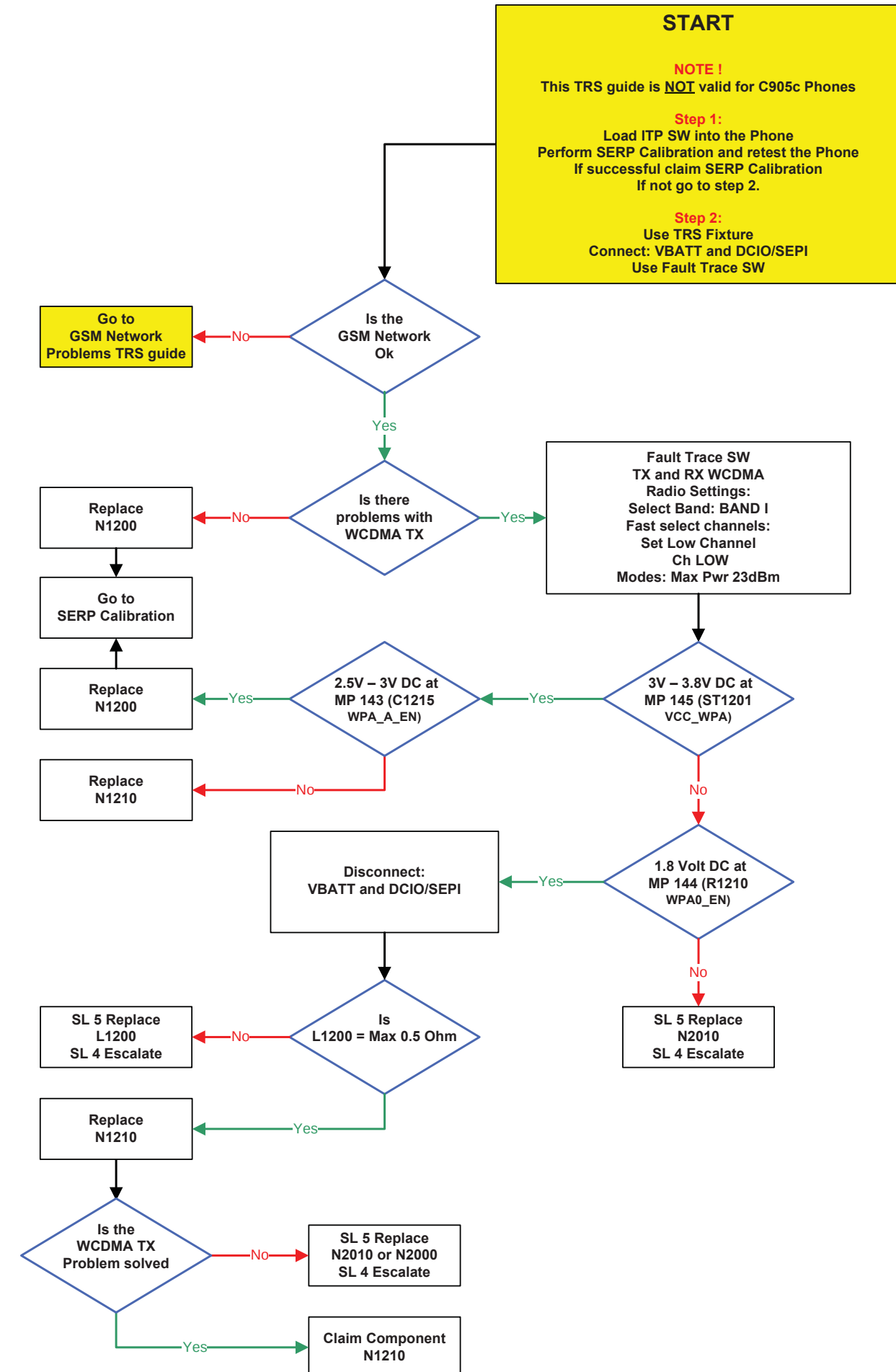
WLAN Problems



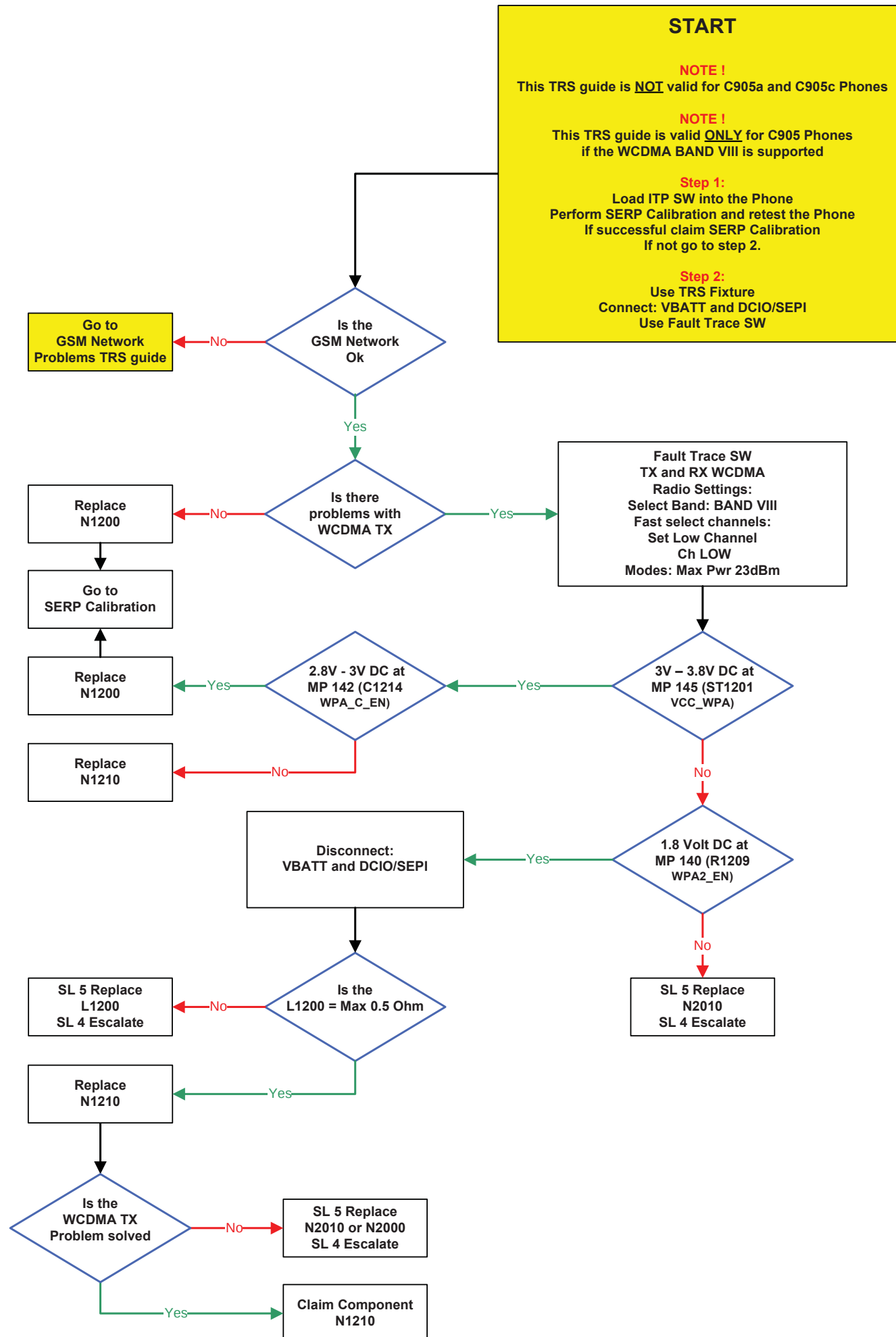
GSM Network Problems



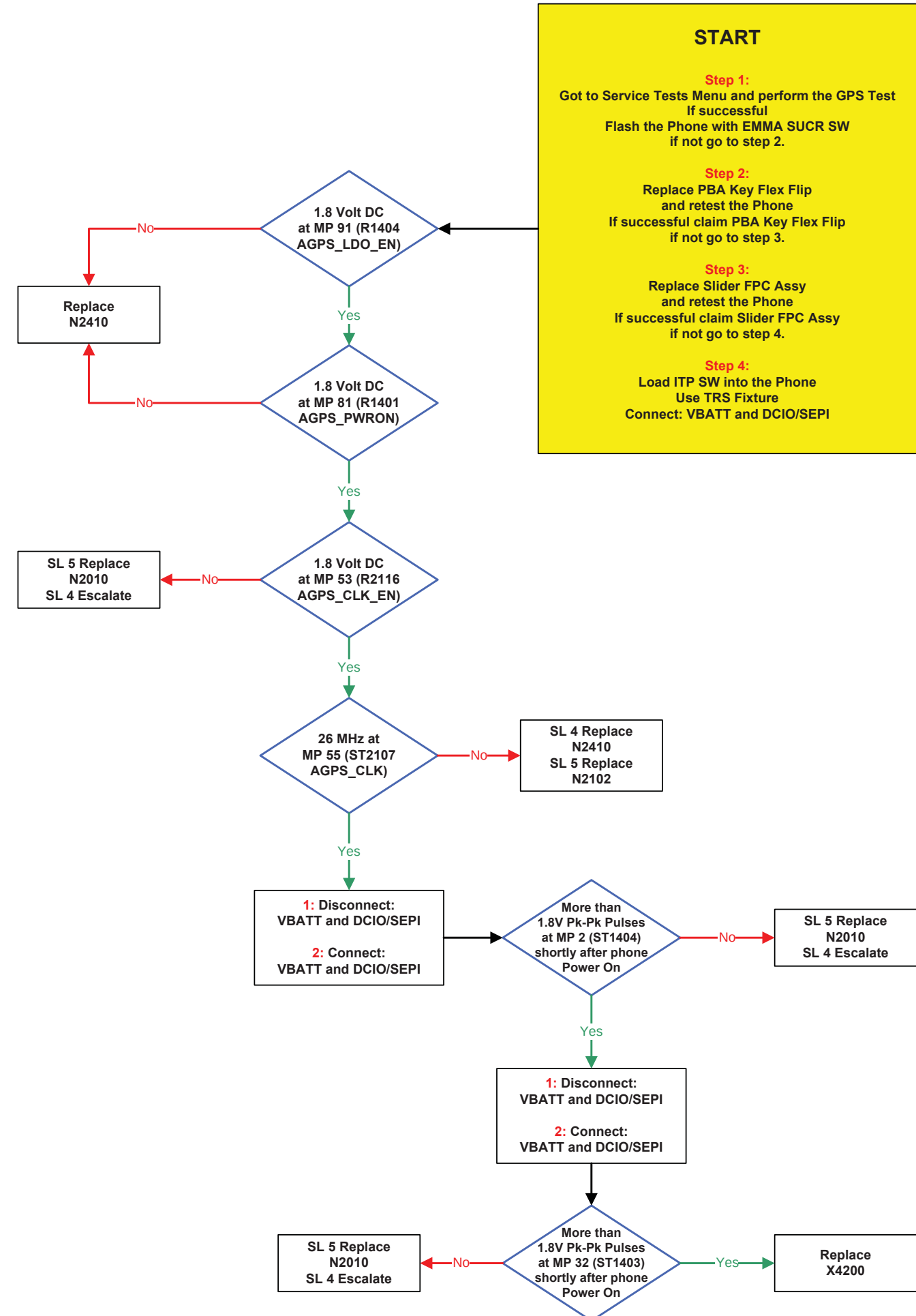
WCDMA BAND I,II,V Network Problems



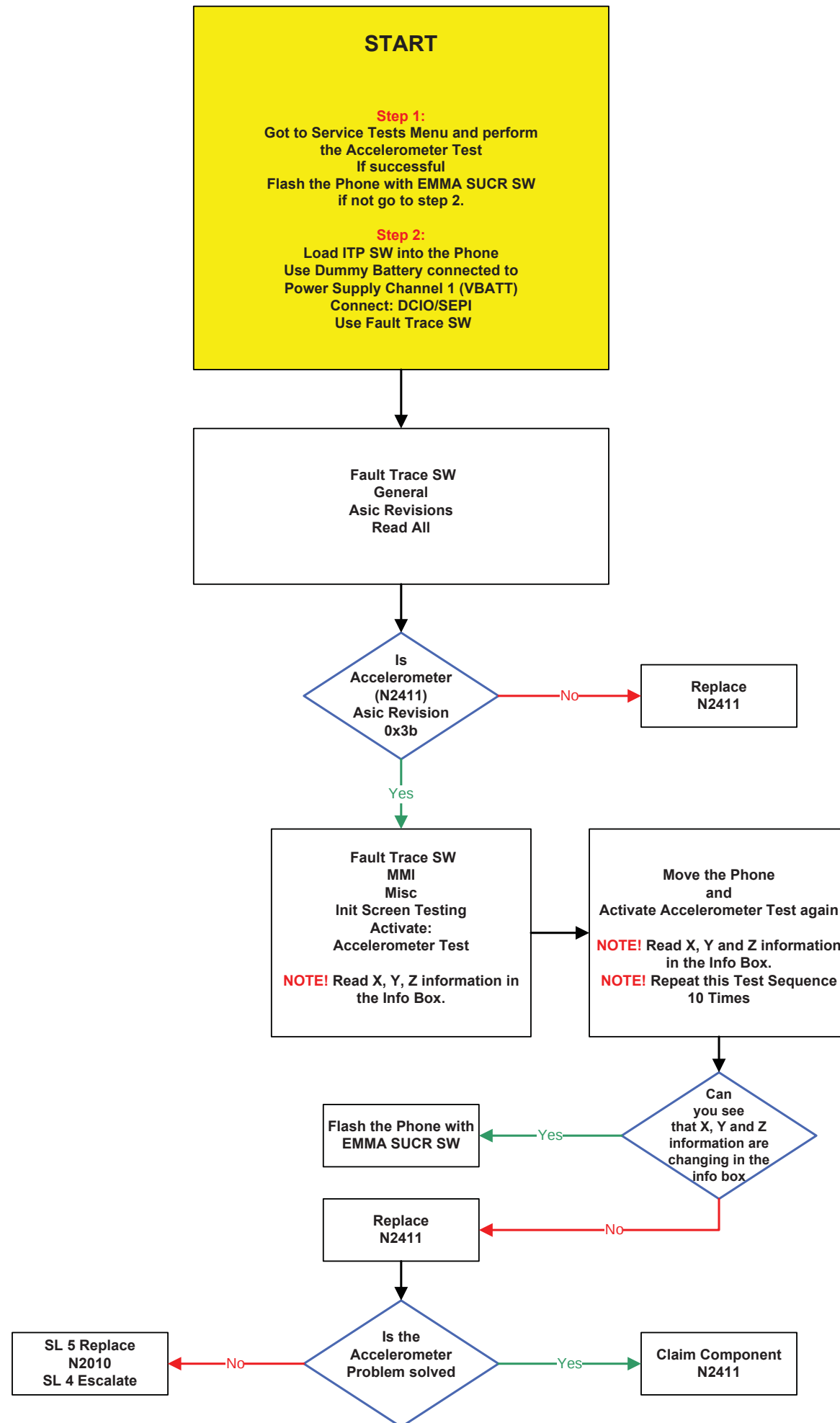
WCDMA BAND VIII Network Problems



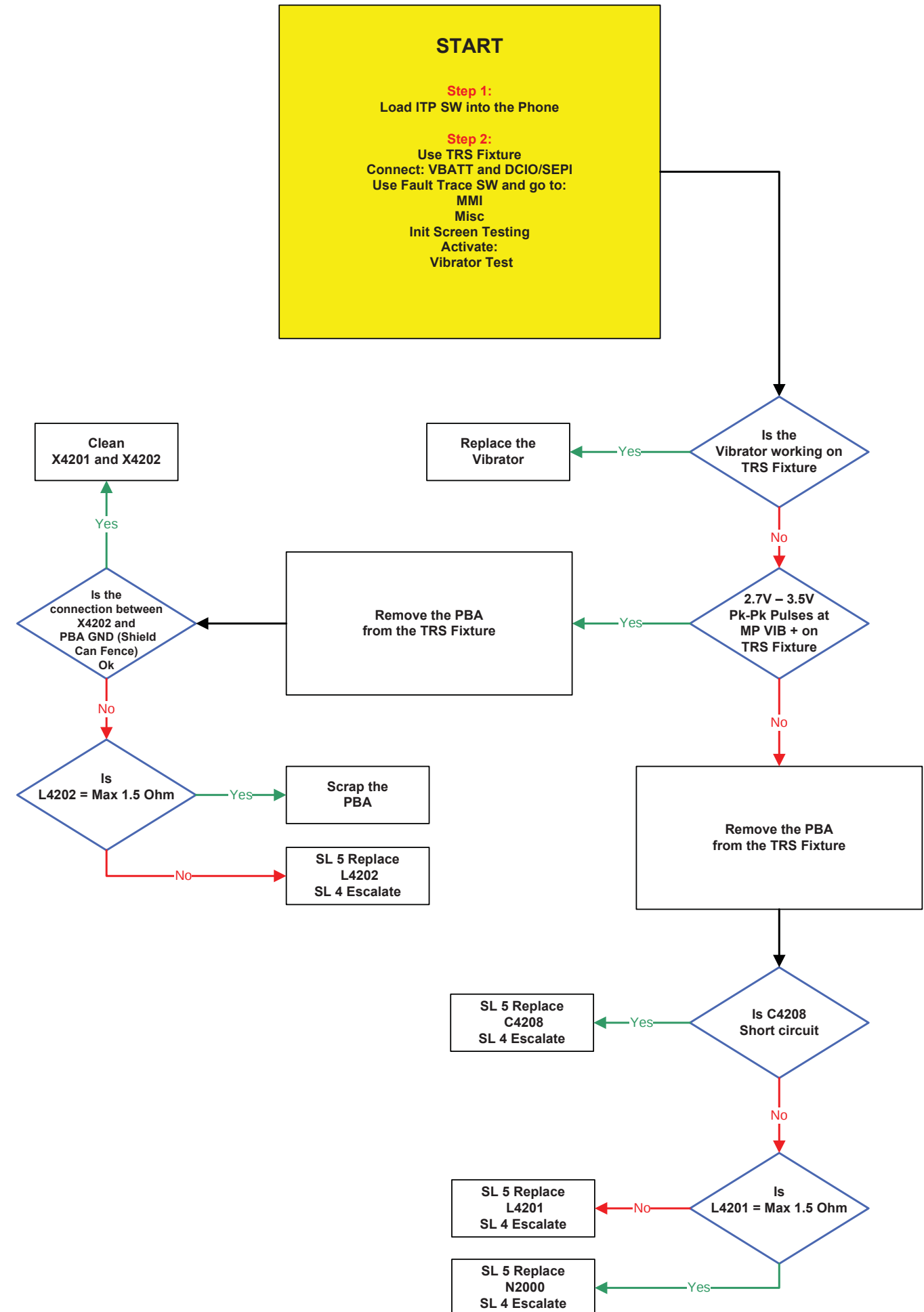
A-GPS Problems



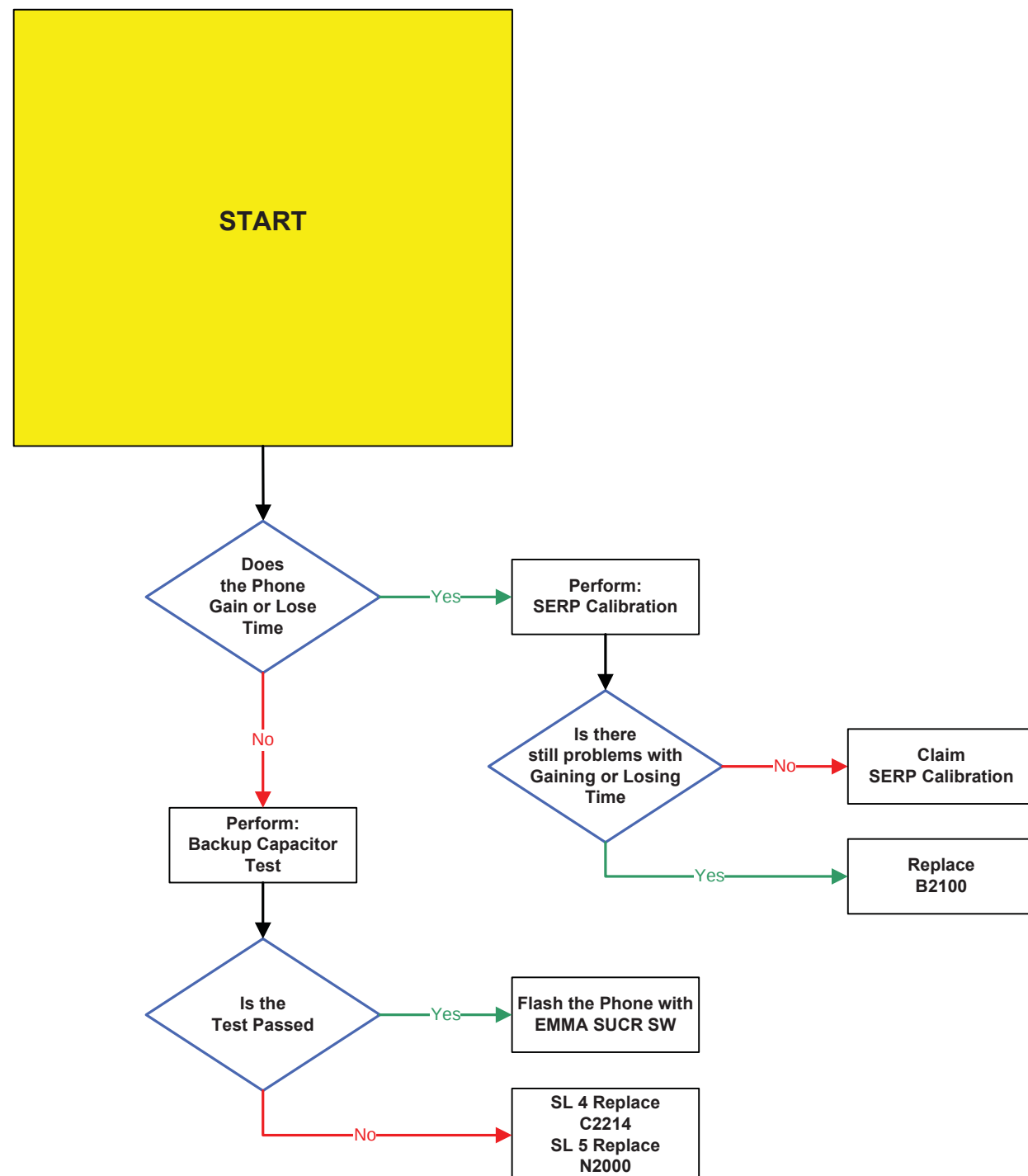
Accelerometer Problems



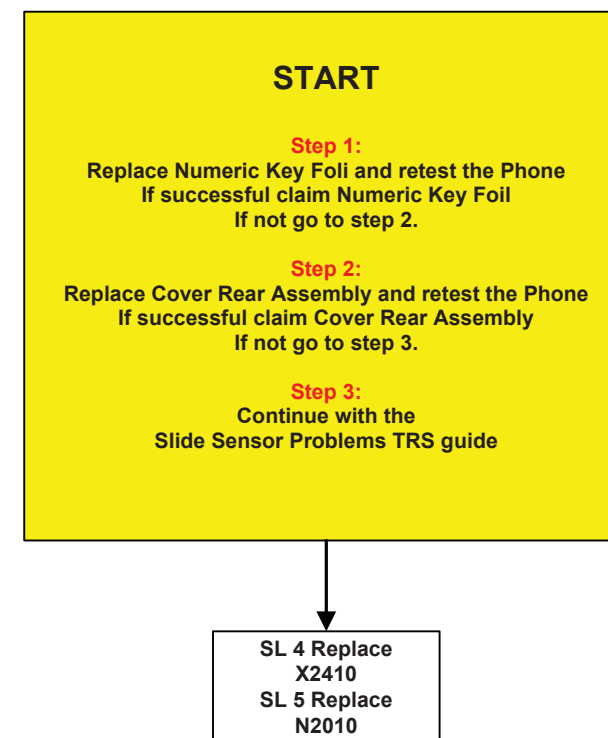
Vibrator Problems



Real Time Clock Problems



Slide Sensor Problems



System Connector Protection Test

Perform Diode and Ohm measurements, use the DMM instrument.

Note! The Battery must be removed from the Phone during this test.

Note! Connect the Black probe to X2405_PIN 9 (GND).



PIN_1 PIN_9 GND PIN_12

System Conn. X2405 (PIN Position)	Diode Measurements (Volt)	Ohm Measurements (Ohm)	SL 4 (Repair Action)	SL 5 (Repair Action)
1	0L	1M - 0L	X2405 L2407 N2421 if lower	C2439 if lower
2	0	0	X2405 if higher L2406 if higher	No Action
3	2.6 – 2.8	12K	X2405 if higher L2401 if higher N3101 if lower or higher	C2443 if lower
4	0.7 - 1.2	1.0K – 1.1K	L2402 if higher N3101 if lower or higher X2405 if higher	C2442 if lower
5	1.8 – 2.0	2.0K – 2.2K	X2405 if higher L2403 if higher N3101 if lower or higher	C2448 if lower
6	1.8 – 2.0	2.0K – 2.2K	X2405 if higher L2404 if higher N3101 if lower or higher	C2447 if lower
7	0	75	X2405 if higher V2414 if lower R2443 if higher N2700 if lower or higher	C2445 if lower L2405 if higher C2444 if lower R2453 if higher
8	2.0 - 2.6	500K – 700K	X2405 if higher R2448 if higher V2417 if lower N2422 if lower or higher	R2478 if higher R2434 if higher
9	GND	GND	X2405 if higher	L2449 if higher
10	0.7 – 0L	50K – 0L	X2405 Z2400 V2415 if lower N2420 if lower	R2445
11	0.7 – 0L	50K – 360K	X2405 if higher Z2400 if higher V2416 if lower N2420 if lower or higher	R2446 if higher
12	0L	75K – 0L	V2412 if lower V2202 if lower	C2440 if lower C2441 if lower

Current Consumption Test

Step 1:

Insert a Local SIM Card and use the phone with the Normal SW (SSW).

Use Dummy Battery connected to Power Supply Channel 1 (VBATT).

Instrument settings: Voltage: 3.8 Volt, Limiter 3A.

Note: (Dummy Battery)

The resistance between GND and BDATA should be approximately 27KOhm.

Measure the current consumption when Phone is turned off.

Take a note of the current consumption at Power Supply Channel 1 (VBATT).

The Current consumption in off mode should be less than 1mA.

If more than 1mA go to **Dead Phone Problems part 1 TRS guide**.

Step 2:

Turn the Phone On:

Measure the deep sleep current max 6mA typical between **0-3mA**. Make sure that the operator is running with deep sleep mode.

Note: This operation can be switched off by operator if network is busy or heavily-loaded.

If phone using more than 6mA, then go to EMMA and run Software Update Contents Refresh (SUCR SW).

Step 3 with Fault Trace SW application:

- Flash the phone with ITP SW
- Use Dummy Battery connected to the Power Supply Channel 1 (VBATT)
- Use Fault Trace SW

Connect the:

- Dummy Battery connected to the Power Supply Channel 1 (VBATT):
Instrument settings: Voltage: 3.8 Volt, Limiter 3 A

- Connect DCIO/SEPI to the phone:
Instrument settings: Voltage: 5 Volt, Limiter 2 A

Perform the following tests:

- **Max TX Power GSM 850 MHz**

Fault Trace SW settings:

TX and RX GSM

GSM Mode Settings:

TX Switched

GSM Radio Settings:

Select Band: GSM 850

Channel: 128

Power Level: 5

- Limits GSM 850 MHz
- Transmitter current: **325mA**
- **Tolerance: $\pm 30\%$**
- **Max TX Power GSM 900 MHz**

Fault Trace SW settings:

TX and RX GSM
GSM Mode Settings:
TX Switched
GSM Radio Settings:
Select Band: GSM 900
Channel: 1
Power Level: 5

- Limits GSM 900 MHz
- Transmitter current: **250mA**
- **Tolerance: $\pm 30\%$**
- **Max TX Power DCS 1800 MHz**

Fault Trace SW settings:

TX and RX GSM
GSM Mode Settings:
TX Switched
GSM Radio Settings:
Select Band: DCS 1800
Channel: 512
Power Level: 0

- Limits DCS 1800 MHz
- Transmitter current: **220mA**
- **Tolerance: $\pm 30\%$**
- **Max TX Power PCS 1900 MHz**

Fault Trace SW settings:

TX and RX GSM
GSM Mode Settings:
TX Switched
GSM Radio Settings:
Select Band: PCS 1900
Channel: 512
Power Level: 0

- Limits PCS 1900 MHz
- Transmitter current: **180mA**
- **Tolerance: $\pm 30\%$**
- **Max TX Power WCDMA BAND I**
(Note: Valid only for C905 and C905a)

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

- Limits WCDMA BAND I
- Transmitter current: **550mA**
- **Tolerance: $\pm 25\%$**
- **Max TX Power WCDMA BAND II**
(Note: Valid only for C905a)

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

- Limits WCDMA BAND I
- Transmitter current: **470mA**
- **Tolerance: $\pm 20\%$**
- **Max TX Power WCDMA BAND V**
(Note: Valid only for C905a)

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

- Limits WCDMA BAND I
- Transmitter current: **590mA**
- **Tolerance: $\pm 10\%$**
- **Max TX Power WCDMA BAND VIII**
(Note: Valid only for C905 if WCDMA BAND VIII is supported)

Fault Trace SW settings:

TX and RX WCDMA
Radio Settings:
Select Band: BAND I
Fast Select Channels: Ch LOW
Modes: Max Pwr 23dBm

- Limits WCDMA BAND I
- Transmitter current: **700mA**
- **Tolerance: $\pm 10\%$**

If current consumption is out of the test limits, try to solve the problem by running SERP Calibration. If still problem with current consumption then go to:
GSM and WCDMA Network problems TRS guides.

If the current consumption is equal to the test limits then go to:
Charging Test.

Backup Capacitor Test

To perform this test use:

- Phone with ITP SW
- Power Supply Channel 1 VBATT: Instrument settings: Voltage: 3.8V, Limiter: 2A
- Power Supply Channel 2 DCIO/SEPI: Instrument settings Voltage: 5V, Limiter: 2A

This test should be performed in 3 steps:

Step1:

Measure the voltage at the Backup capacitor by using **Fault Trace SW- Logic - ADC Values – Read ADC Value** (Reading 1).

Step2:

This step should be done **30 seconds** after Step 1. Measure the voltage at the Backup capacitor by using **Fault Trace SW - Logic – ADC Values - ADC Channels – Read ADC Value** (Reading 2).

Step3:

Compare the difference between Reading 1 and Reading 2 with the reference table below. If the Reading 1 value is between 50 and 680 go to Interval 1, if between 681 and 800 go to Interval 2, if between 801 and 880 go to Interval 3 and compare with the Reading 2 – Reading 1 Min and Max Limits.

Reference Table:

	Min	Max	Unit
Absolute readout Reading 1	50	880	Dec

Reading 1 (Dec)	Reading 2 – Reading 1 (Dec)	
	Min	Max
Interval 1 (50 – 680)	20	210
Interval 2 (681 – 800)	5	30
Interval 3 (801 – 880)	0	10

Note: The upper table contains the absolute limits for the readouts. The lower table contains the allowed delta between the first and the second readout, separated in time with 30 seconds.

If the readings are out of limits replace **C2214** Backup capacitor.

If the problem is not solved then SL 5 Replace N2000 SL 4 Escalate.

Charging Test

To perform this test use:

- Phone with the Normal SW (SSW)
- Dummy Battery connected to Power Supply Channel 1 (VBATT)
Note! The Dummy Battery should have approximately 27 KOhm resistance between GND and BDATA.
- Power Supply Channel 1 (VBATT)
Instrument settings:
Voltage: from 3.0 Volt to 4.2 Volt, according to VBATT row in the Reference Table.
Limiter: 2A
- Power Supply Channel 2 (DCIO/SEPI)
Instrument settings:
Voltage: 5V
Limiter: 2A

Test instructions:

- Disconnect the DCIO/SEPI Cable between each measurement and wait for the phone to shut down when changing VBATT voltage.
- Take a note of Current measurements at Power Supply Channel 2 DCIO/SEPI and Display charging indicator X seconds after DCIO/SEPI cable has been inserted according to Test Time row in the reference table below.
- Compare test results with reference table below, tolerance +/-20%.

Reference Table

VBATT x Volt	3.0	3.1	3.2	3.3	3.4	3.5	3.6	3.7	3.8	3.9	4.0	4.1	4.2
Test Time x sec.	15s	15s	15s	25s	25s	25s	25s	30s	30s	30s	30s	30s	45s
DCIO/SEPI Current mA	250	250	250-500	500	500	500	500	800-1000	800-1000	800-1000	800-1000	500-750	0
Display indicate charging	Nothing	Nothing	Yes or Nothing	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Fully Charged

Note! The Power Supply Channel 1 (VBATT) must allow reverse current.

If the charging current is **NOT** equal to the reference table then go to:

Charging Problems TRS Guide.

If the charging current is equal to the reference table value then insert the normal battery and test the charging current to verify that the phone battery is working properly.

Measure the voltage at the battery to define the current level.

If the battery is receiving the right current, then the phone and the battery are working properly.

ASIC Revision Test

Note:

The Keypad Scan Test may not be activated when performing this test.

Purpose:

- To verify that the ASIC is correctly mounted, that the communication works and that the revision is correct.

The tested ASICs are:

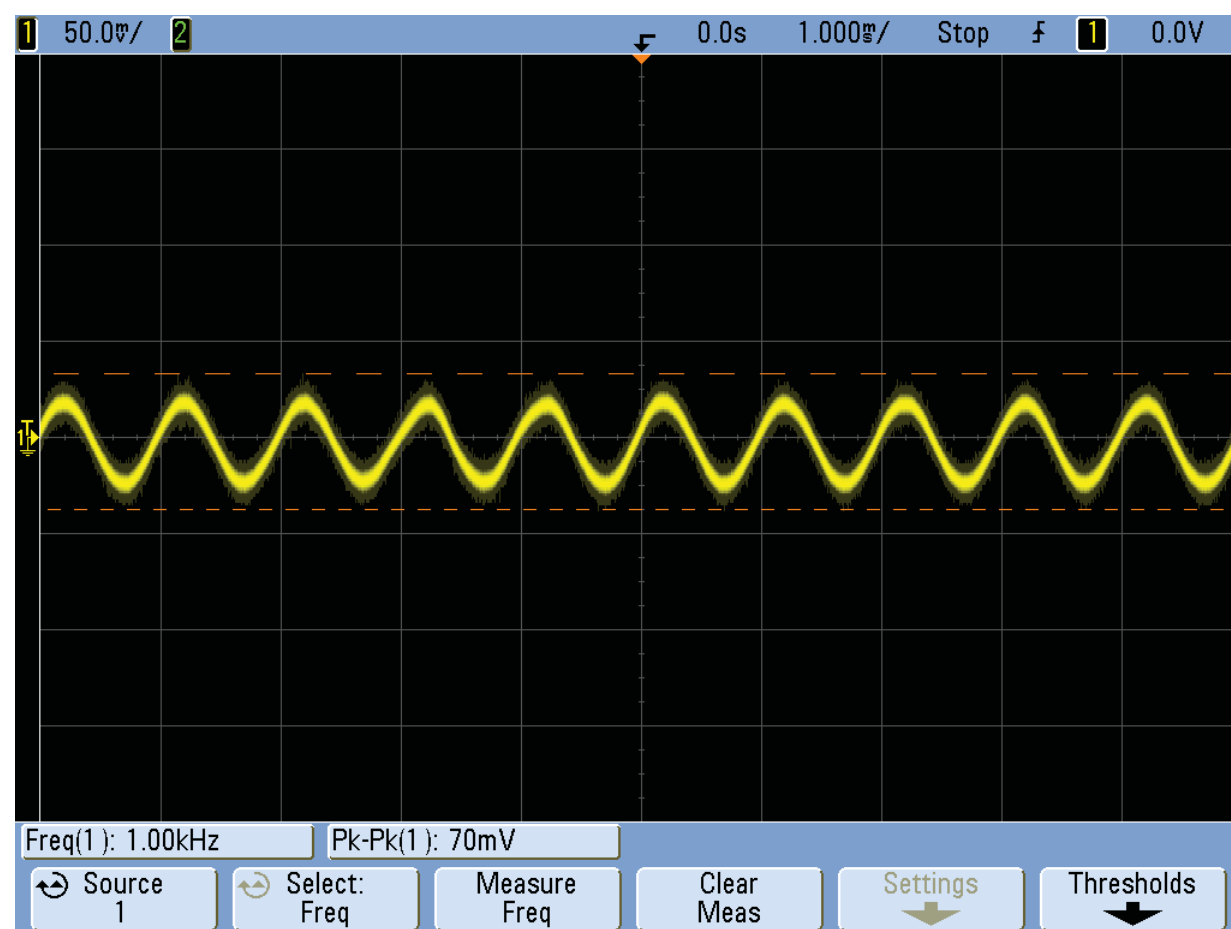
- D2010 (Kajsa)
- N2000 (Vera)
- N1300 (Bluetooth and FM Radio ASIC)
- N2411 (Accelerometer)
- N1400 (A-GPS Module)

To perform this test use:

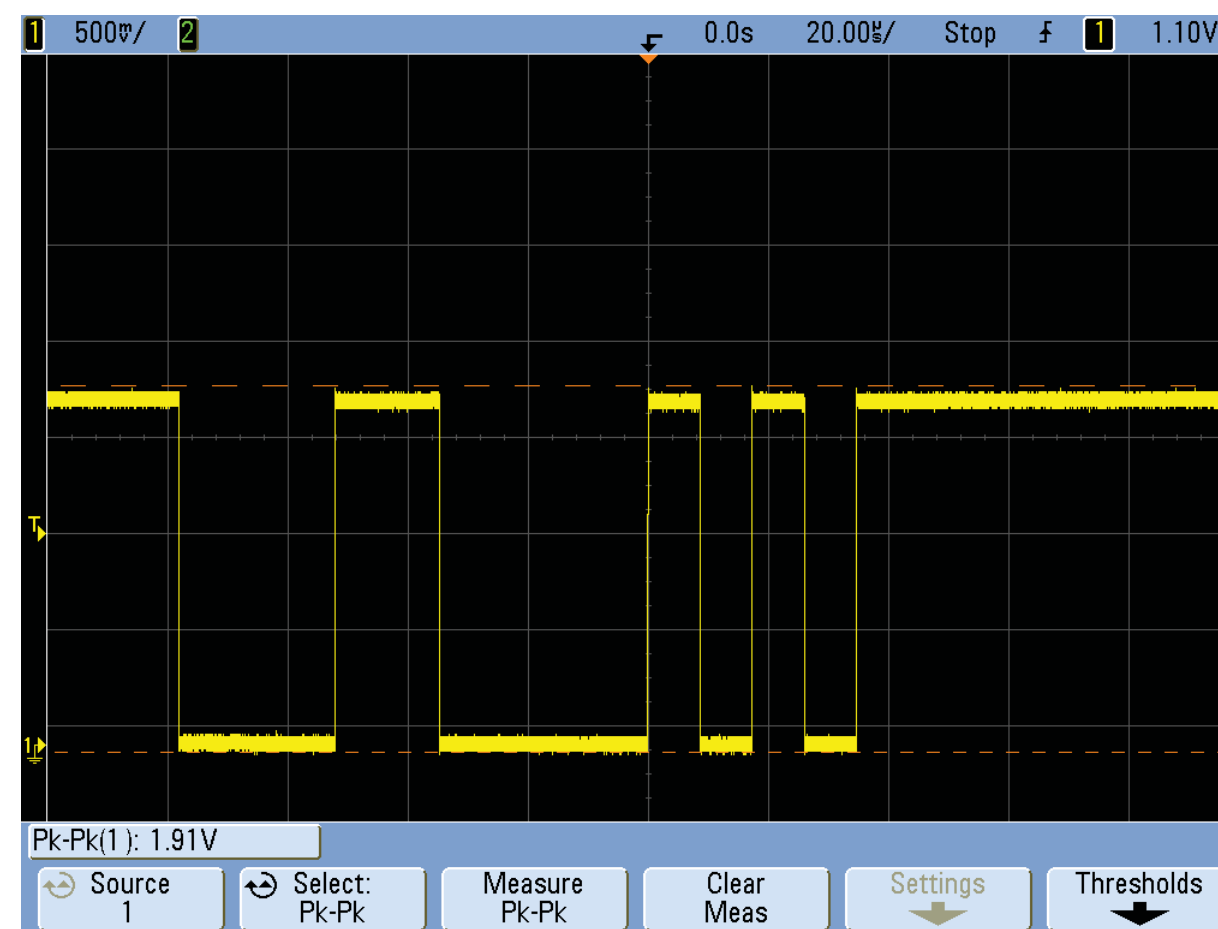
- Phone with ITP SW
- TRS Fixture
- Power Supply Channel 1 VBATT (Voltage: 3.8V, Limiter: 2A)
- Power supply Channel 2 DCIO/SEPI (Voltage: 5V, Limiter: 2A)
- Fault Trace SW, go to: General – Asic Revisions – Read All

Reference Table:

ASIC	Part number	Description	Return value (hex)
N2010	1208-3871	CPU (Kajsa)	0xE8
N2000	1202-0639	Power Management (Vera)	0xC8
N1300	1200-6182	Bluetooth	
		Firmware Revision	0x5,0x3
		Chip ID	0x0,0x0,0x0,0x0 Will always return 0 on STLC because Chip ID is not supported.
N2411	1202-1676	Accelerometer	0x3b
N1400	1200-0700	A-GPS Module	254,0,253,192,0,242,113,9,16,252
			NOTE! The Key Flip Flex Assy must be connected to the PBA during this test.
N1300	1200-6182	FM Radio	When FM Radio is On : 0x1253 When FM Radio is Off : 0x1200

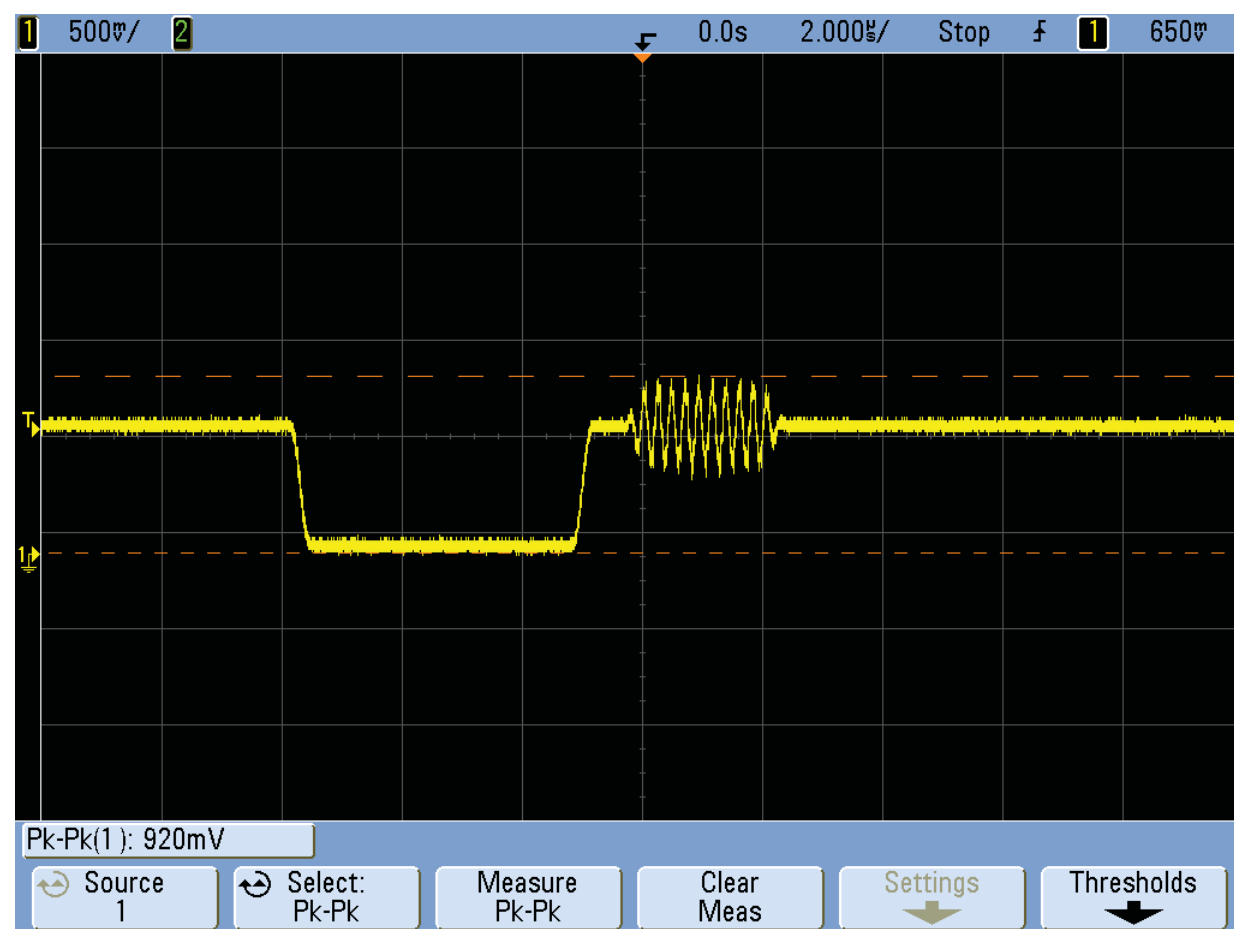


MP 1, MP 30 (C3137 and C3148)

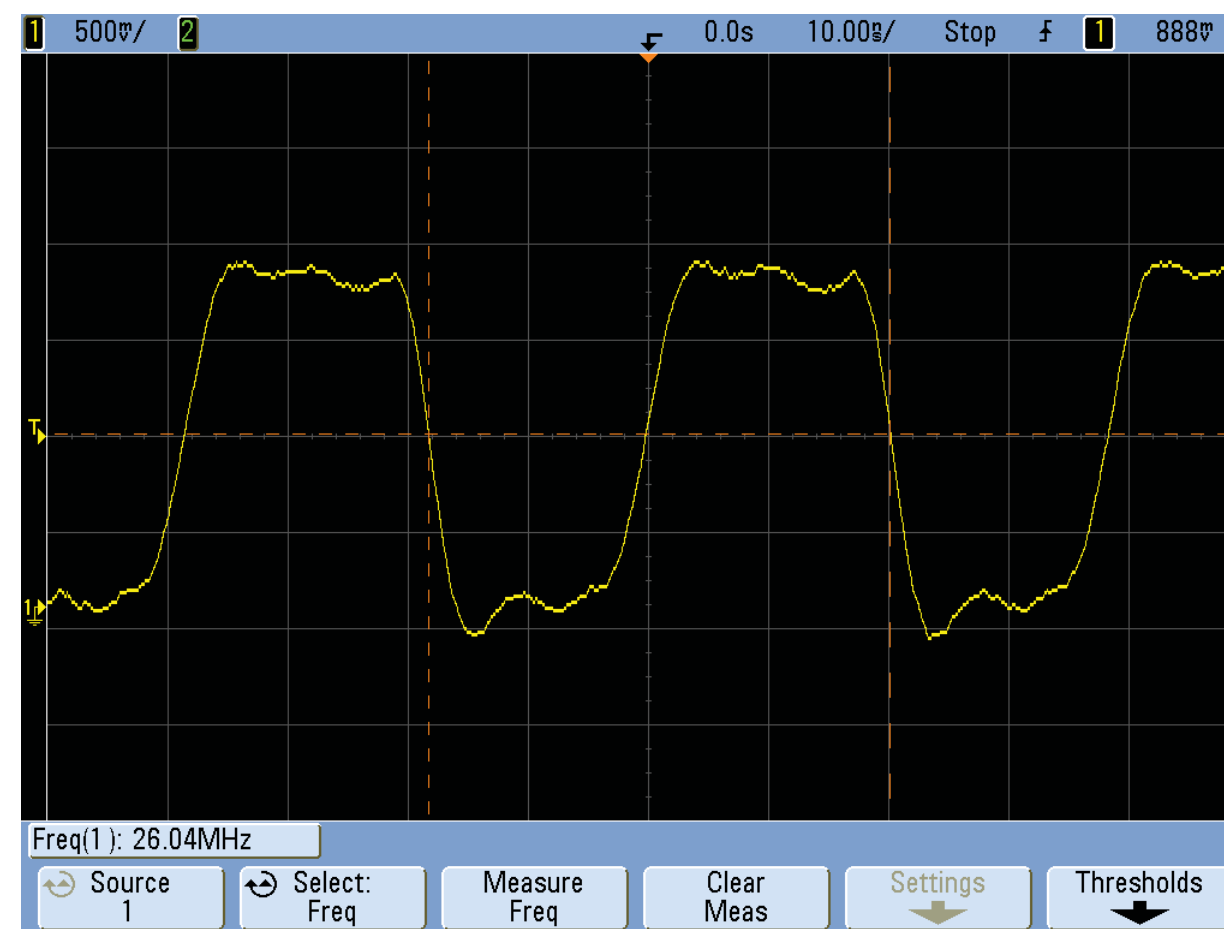


MP 2 (ST1404) Shortly after the phone is powered on

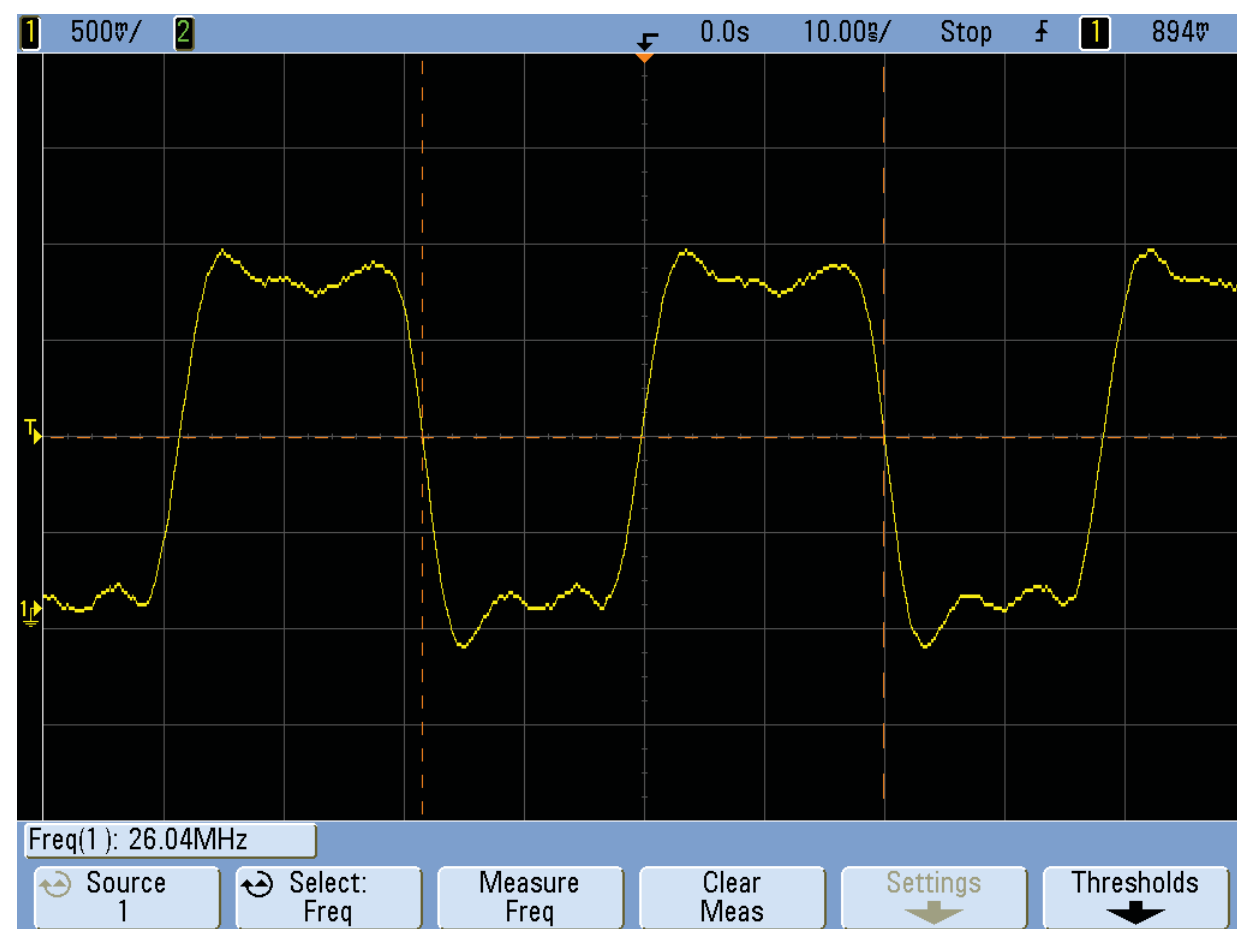
Note: This is an example! The shape of the signal can be different.



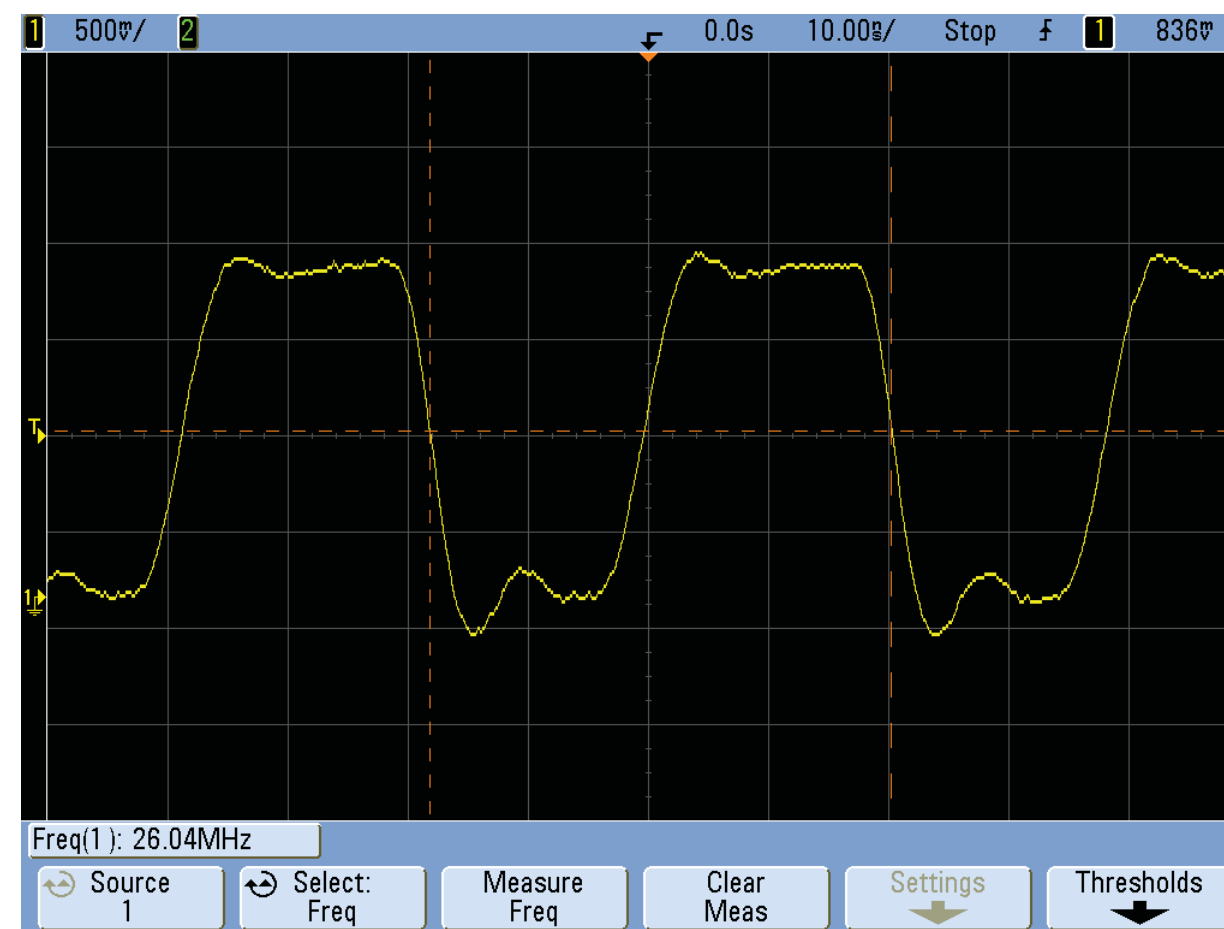
MP 14 (L2405 TV_OUT)



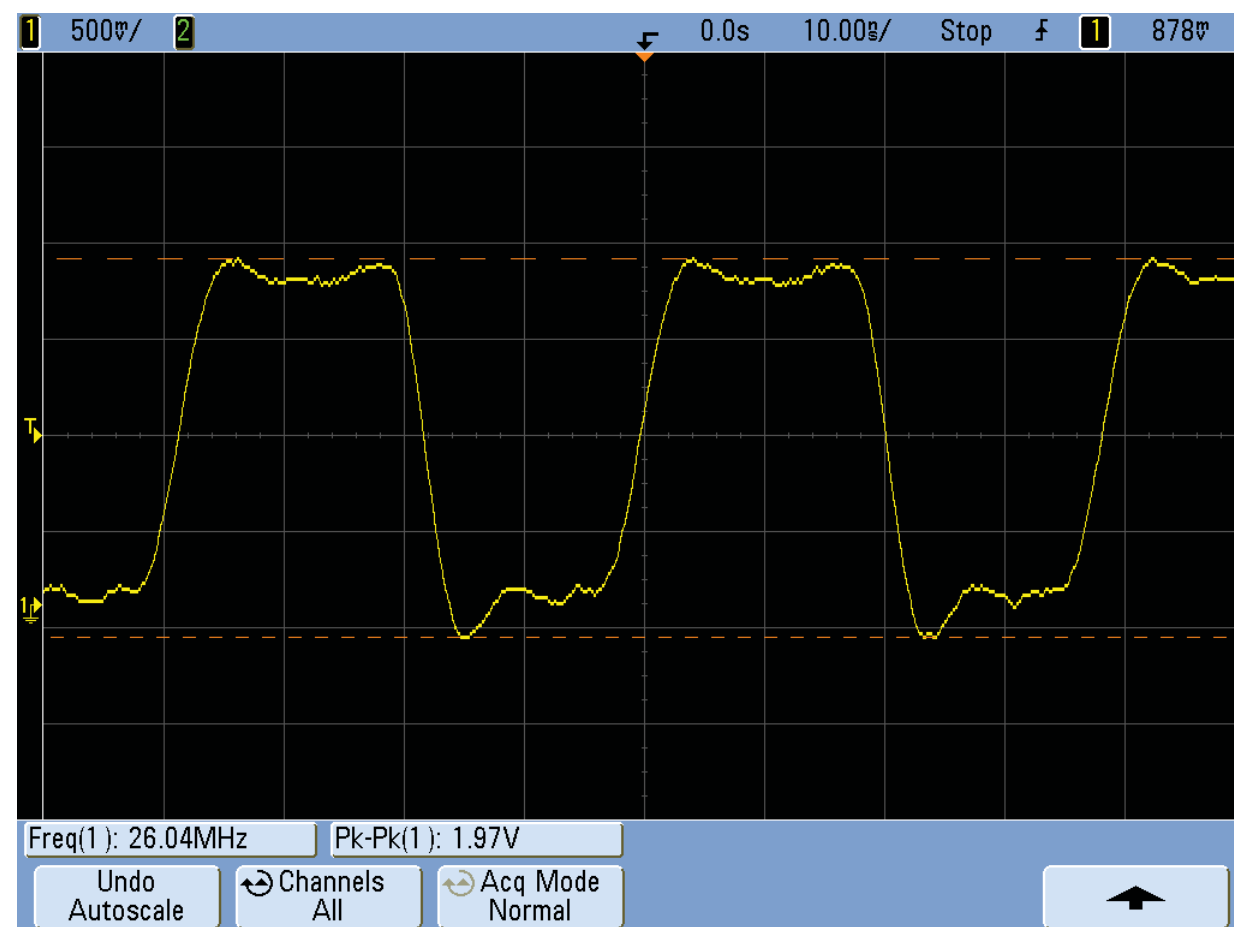
MP 19 (ST2108 TV_CLK)



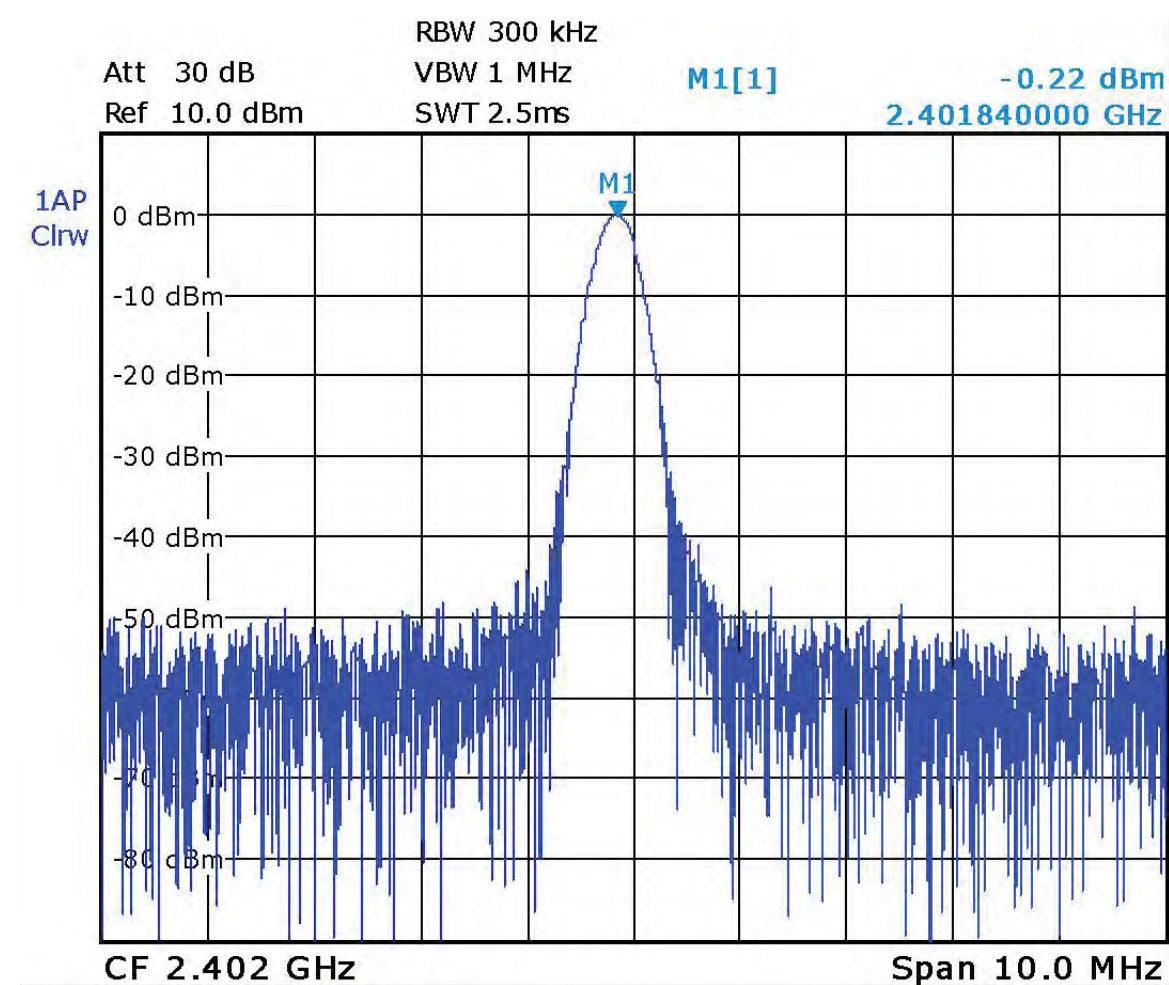
MP 20 (ST2109 VIDCC_CLK)



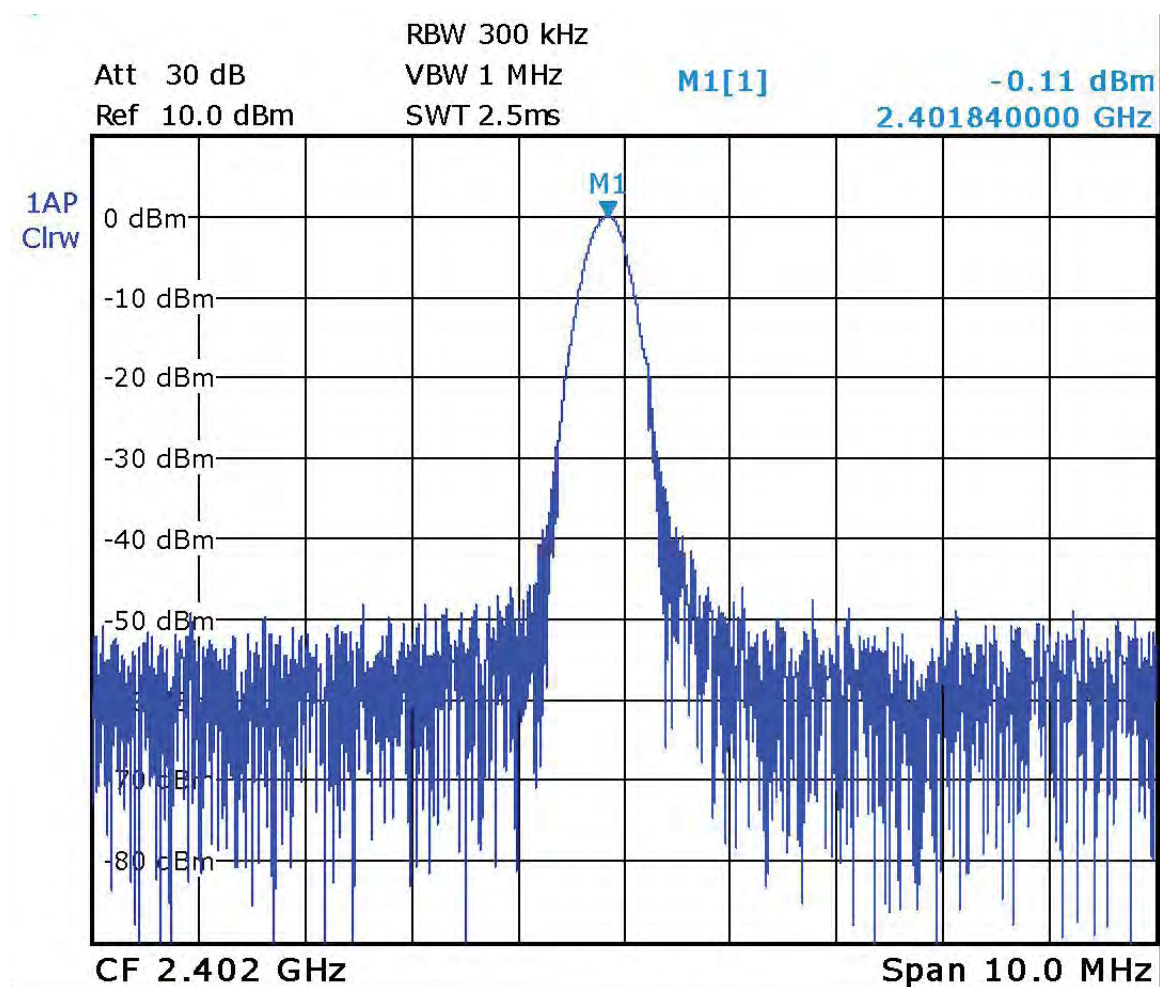
MP 22 (ST2106 BT_CLK)



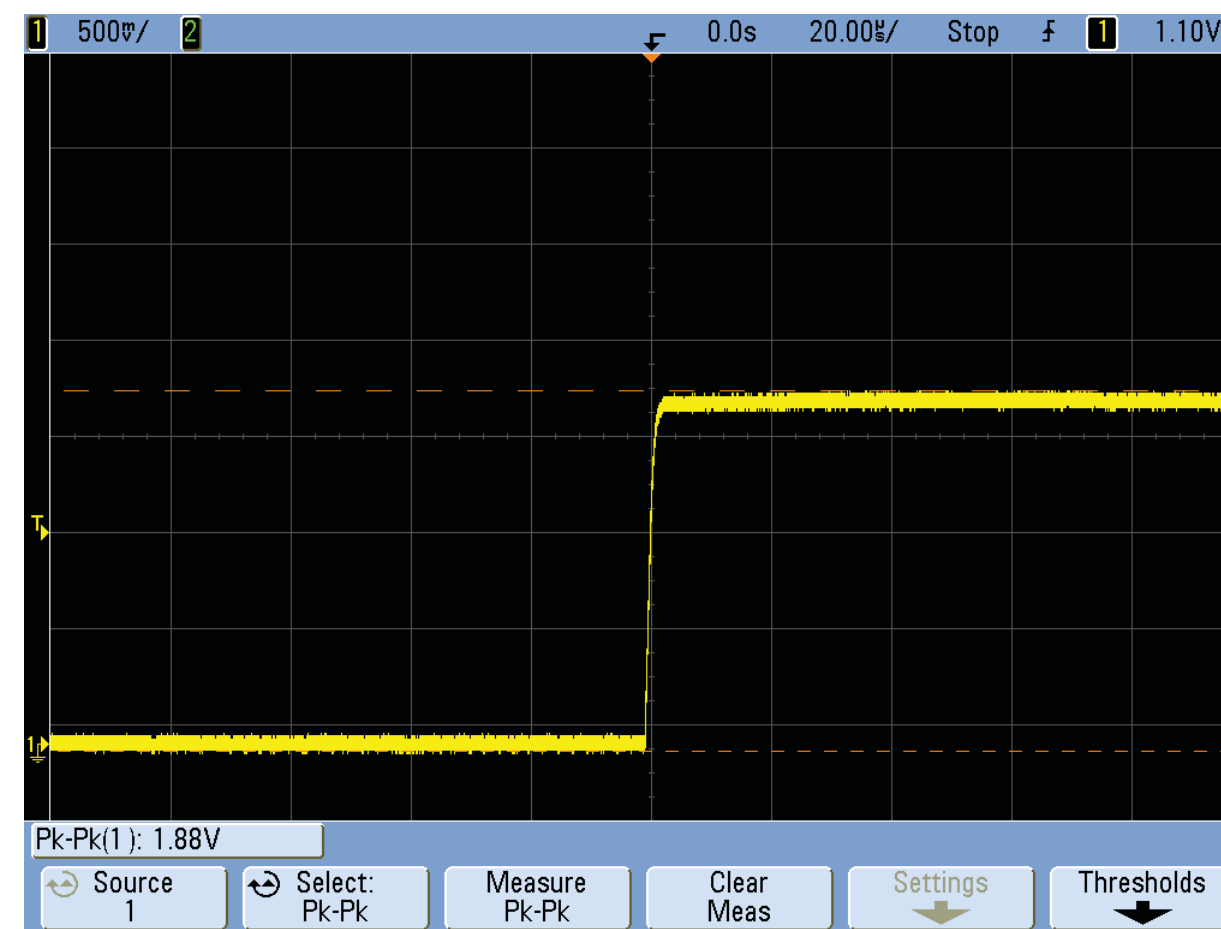
MP 24 (ST2105 WLAN_CLK)



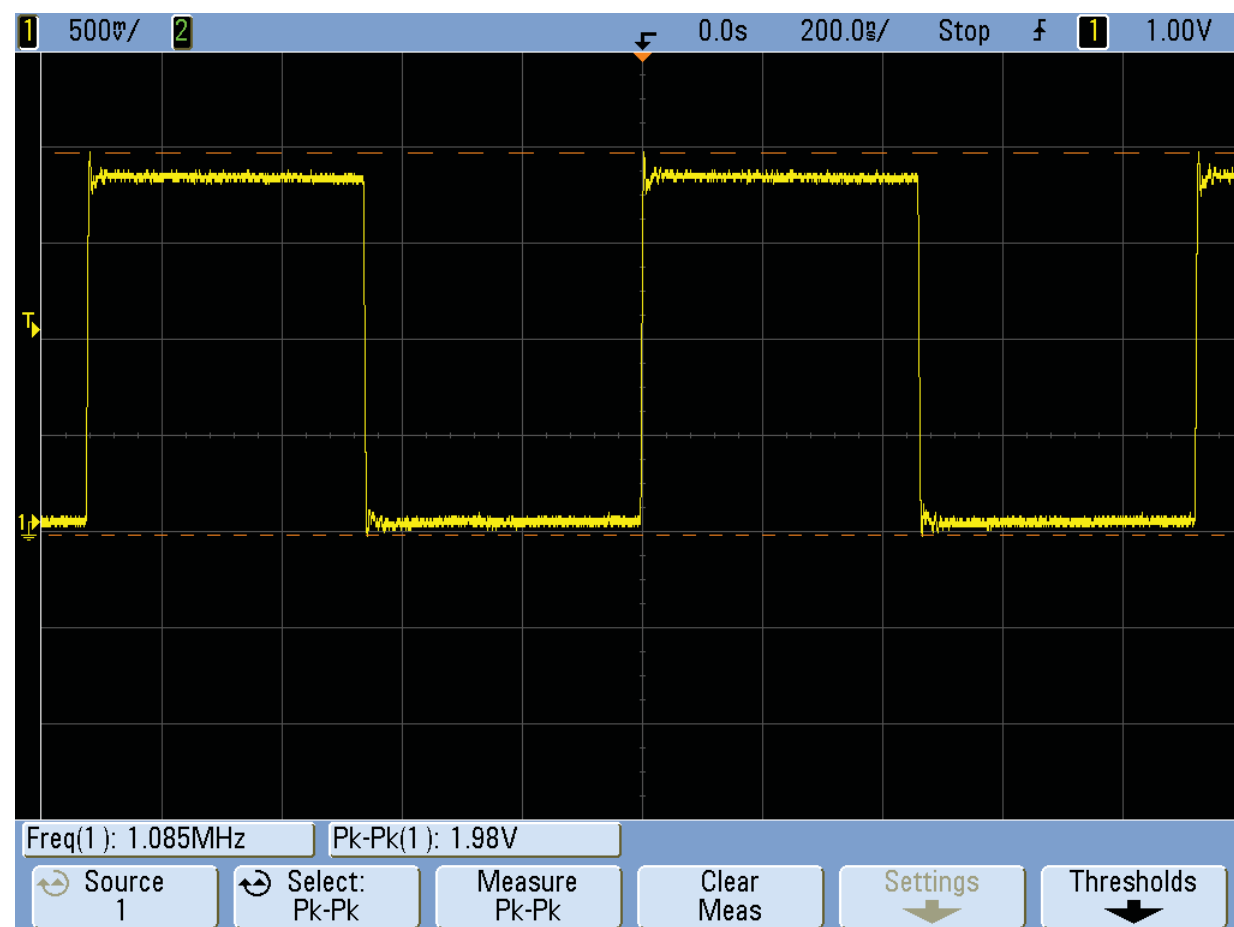
MP 27 (W1300_Pin 4)



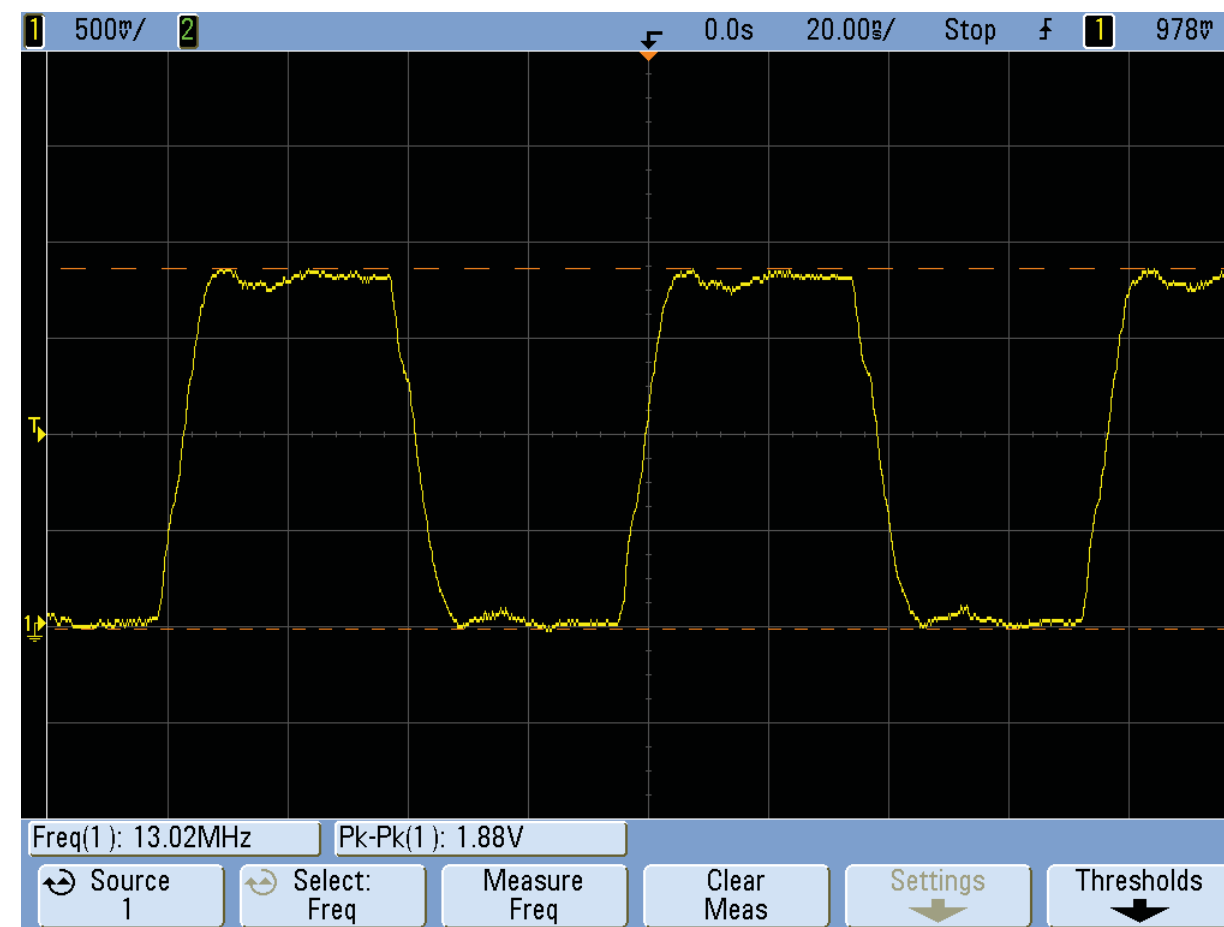
MP 28 (W1300_Pin 3)



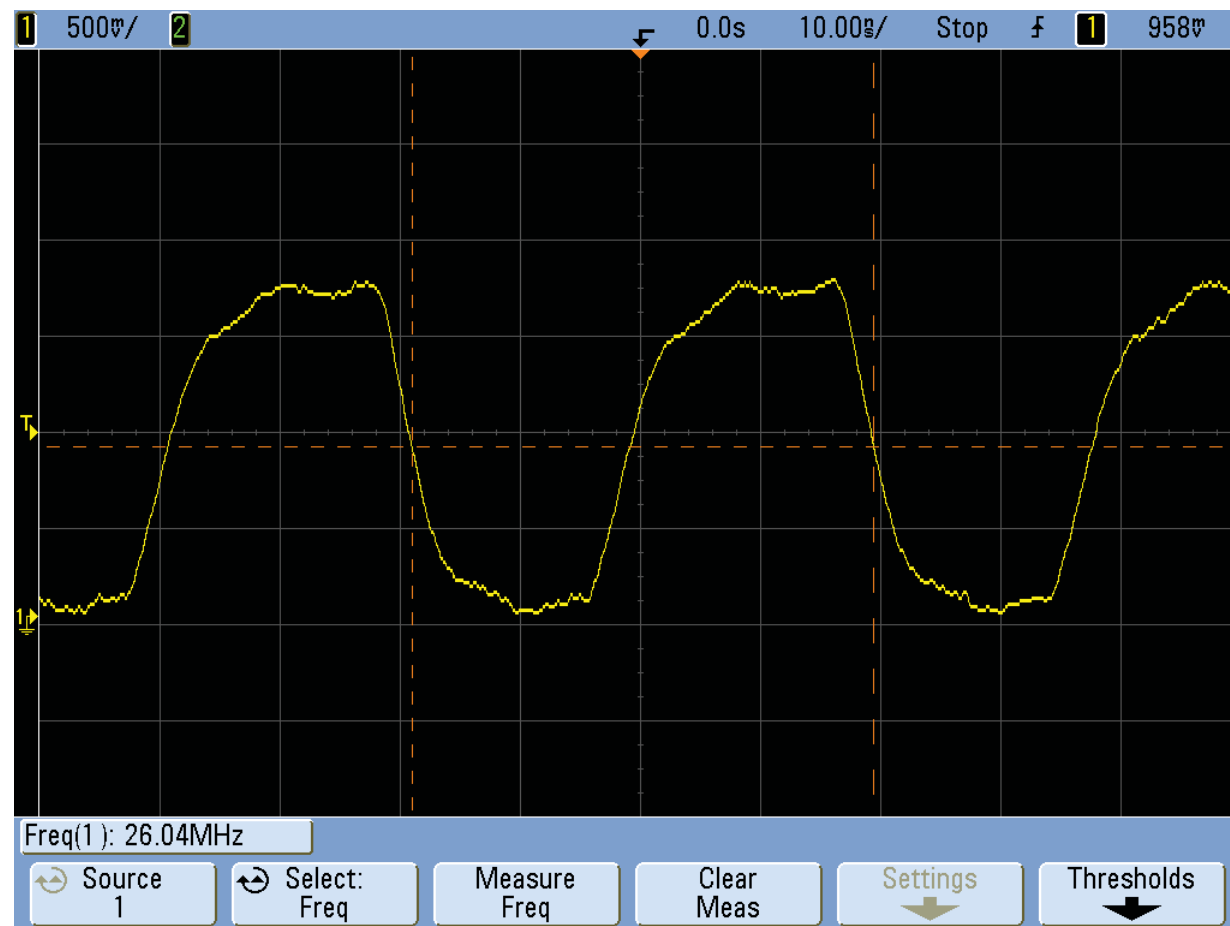
MP 32 (ST1403) Shortly after the phone is powered on



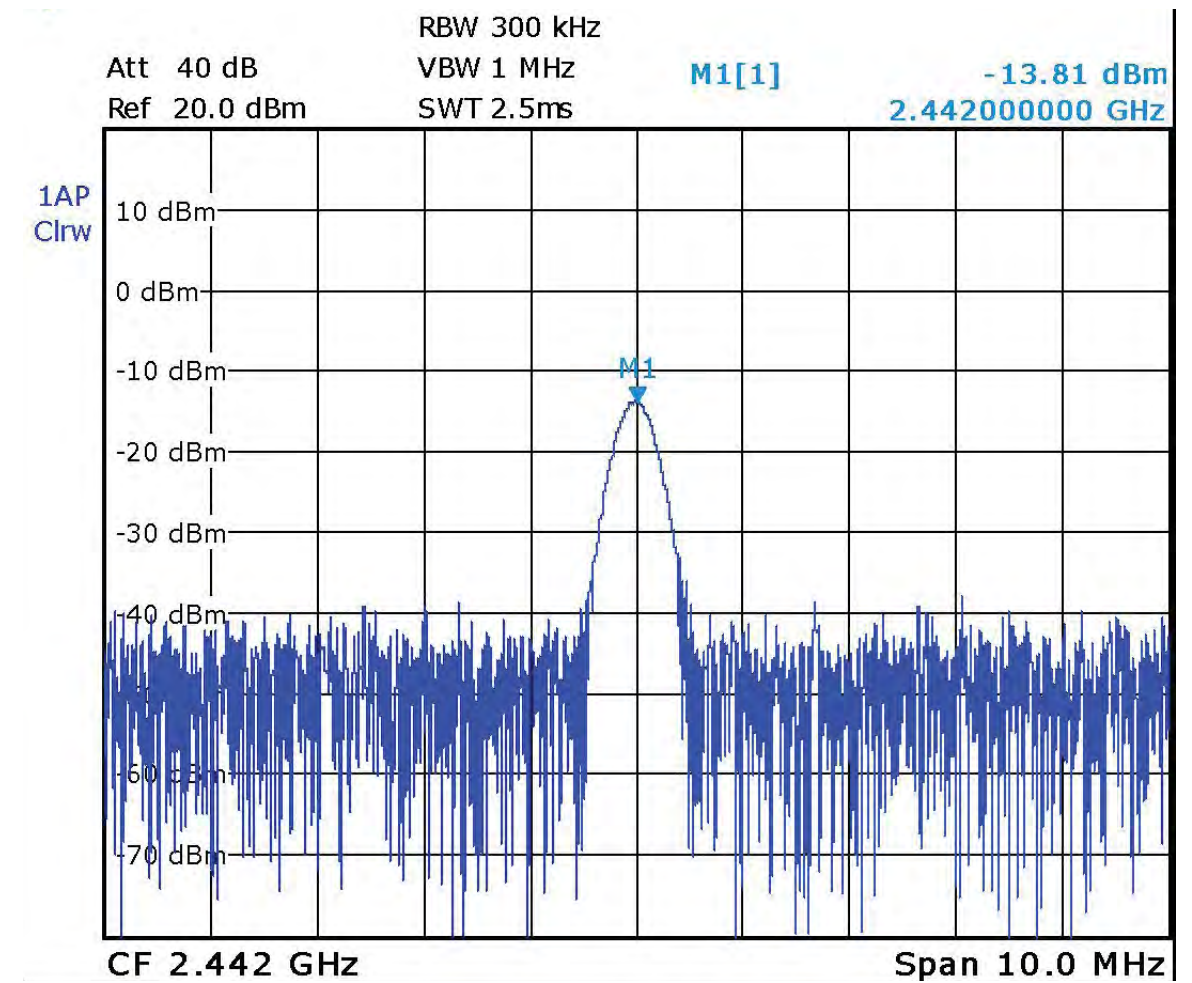
MP 34 (SP2410)



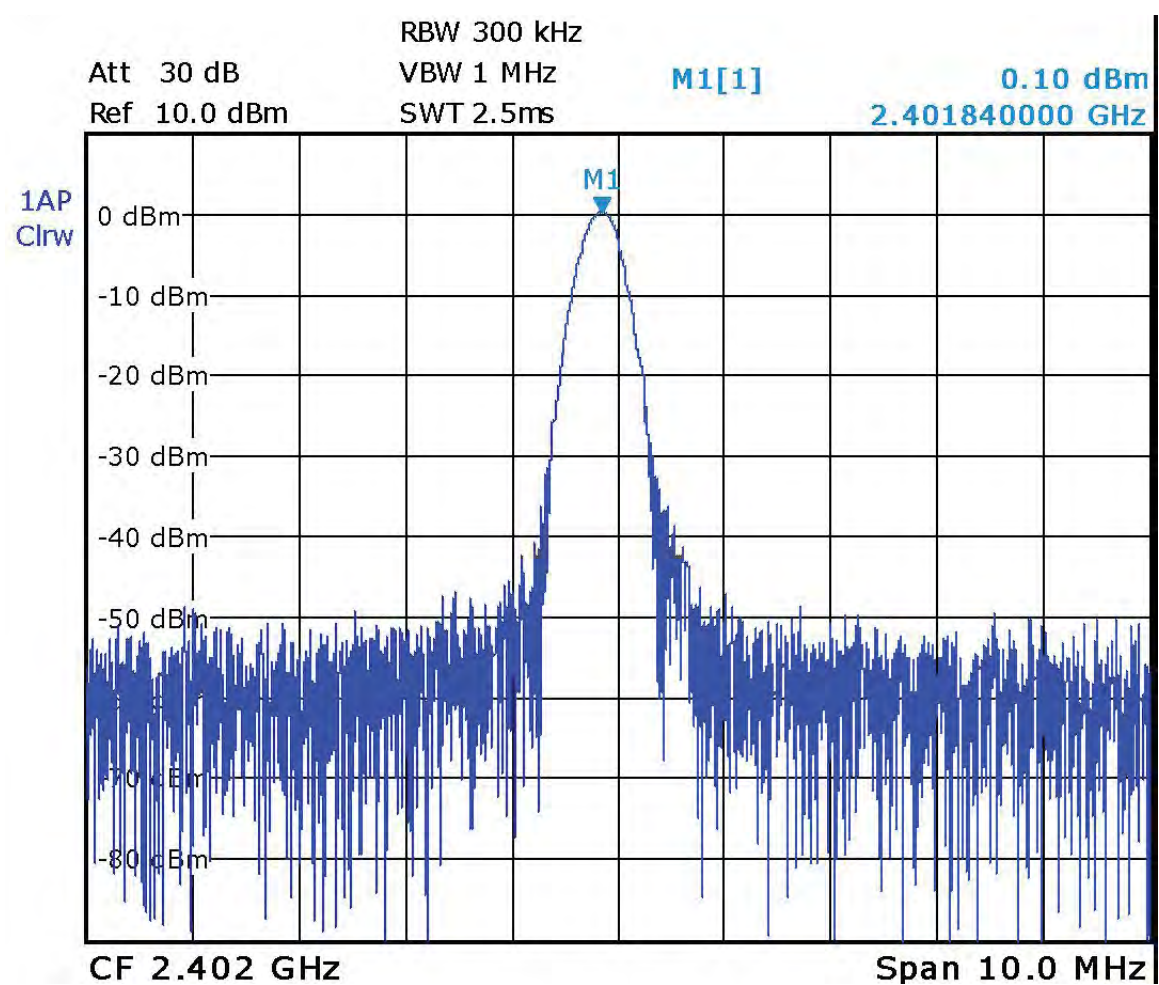
MP 37 (ST2110 CAMSYSCLK)



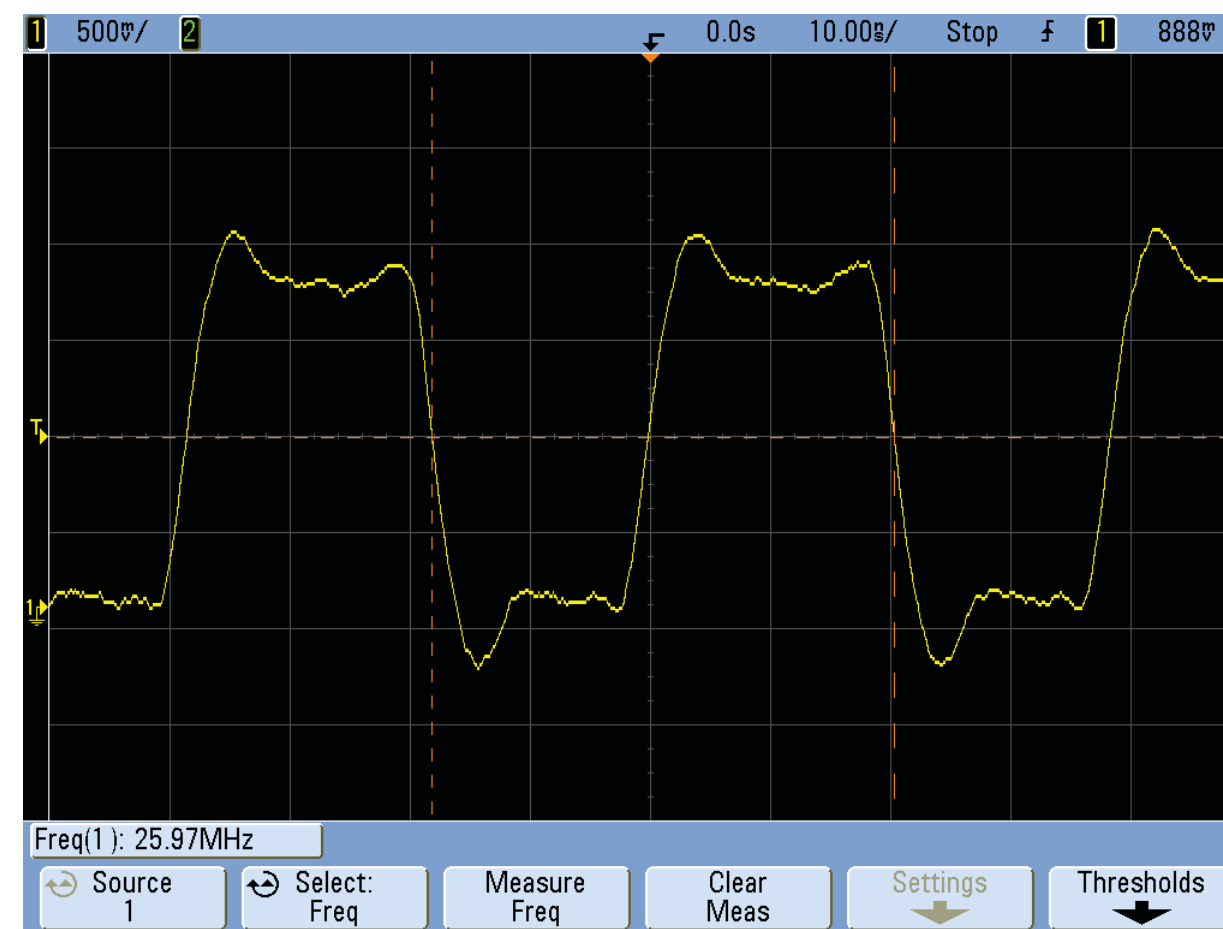
MP 38 (R2102_MCLK)



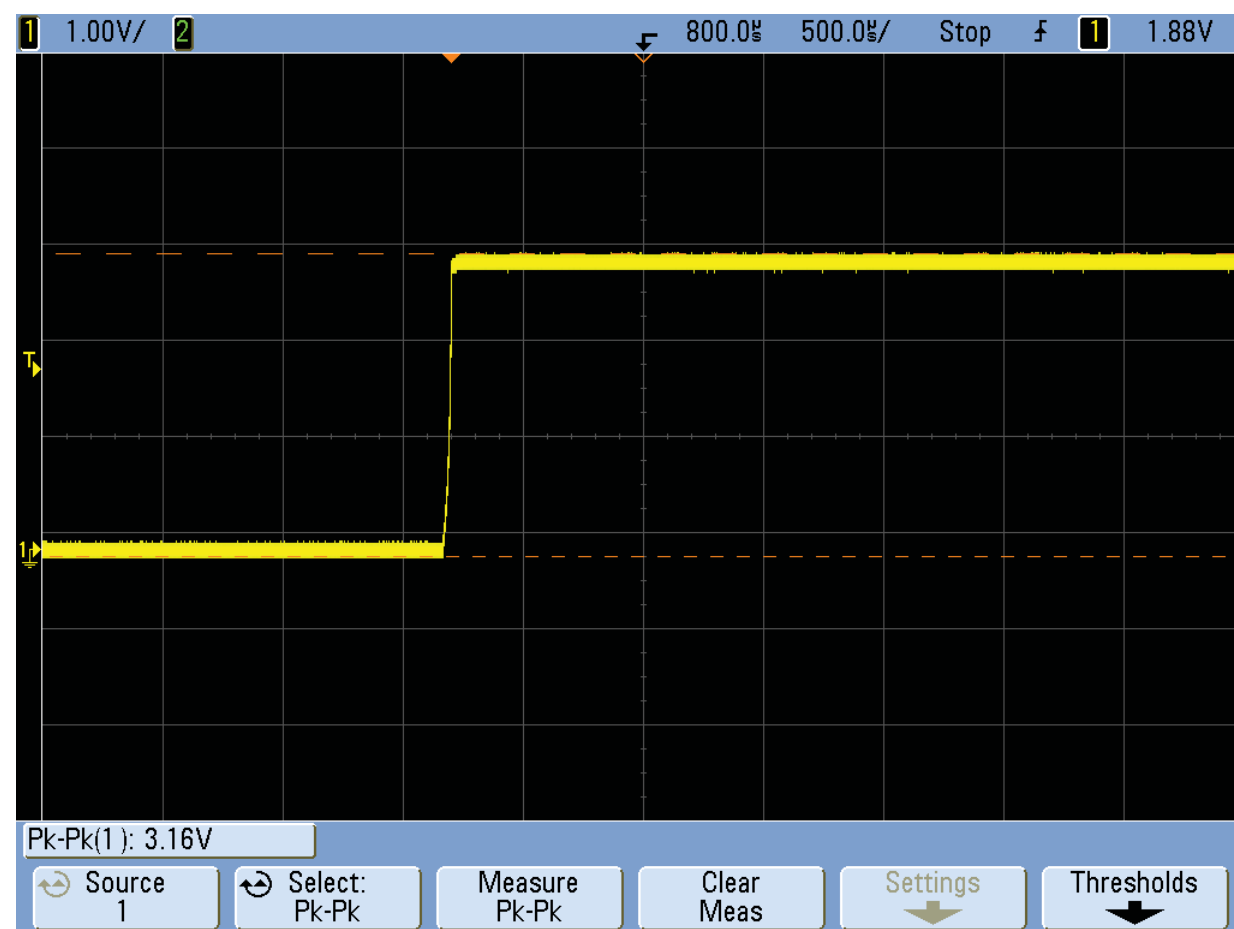
MP 47 (N1500)



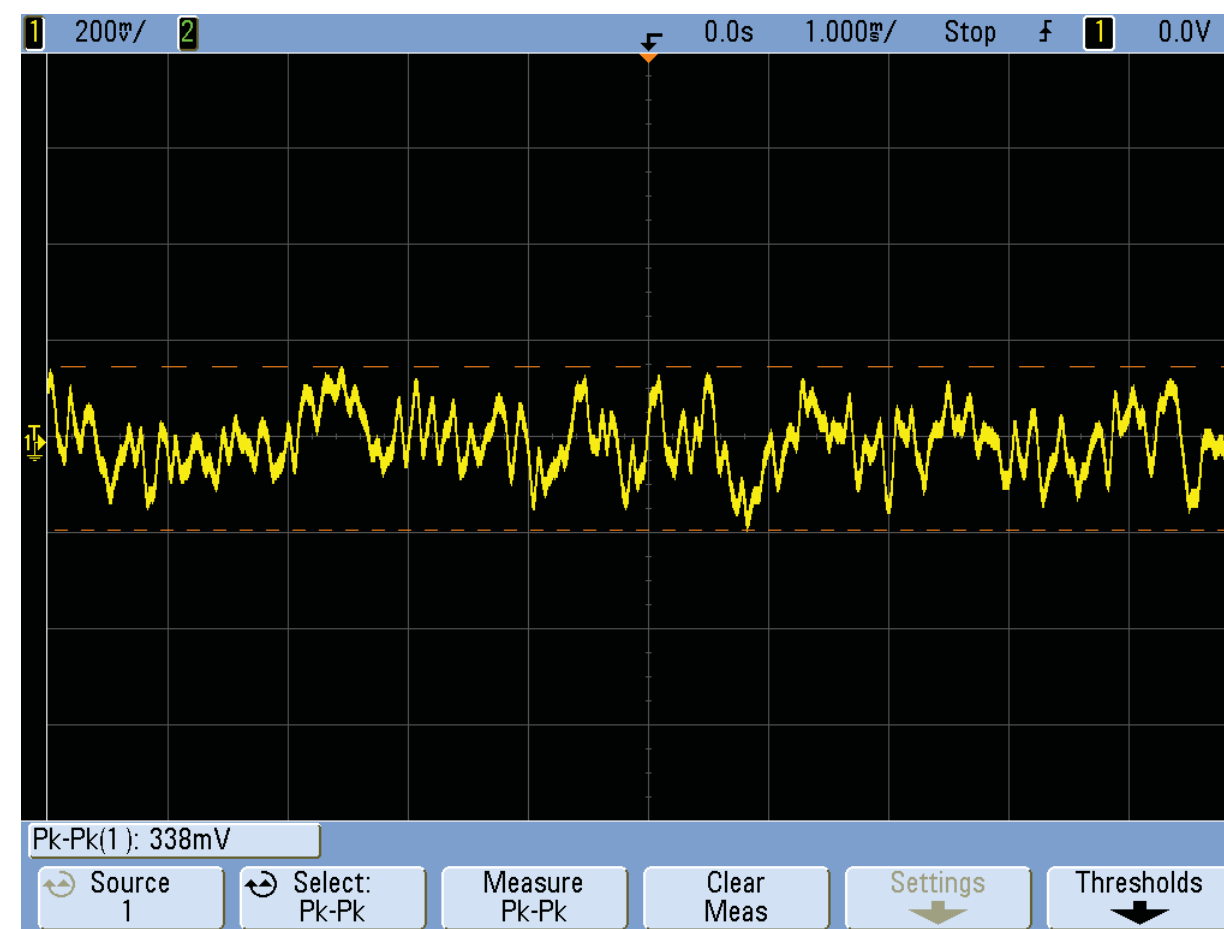
MP 48 (C1502 BT_ANT)



MP 55 (ST2107 AGPS_CLK)

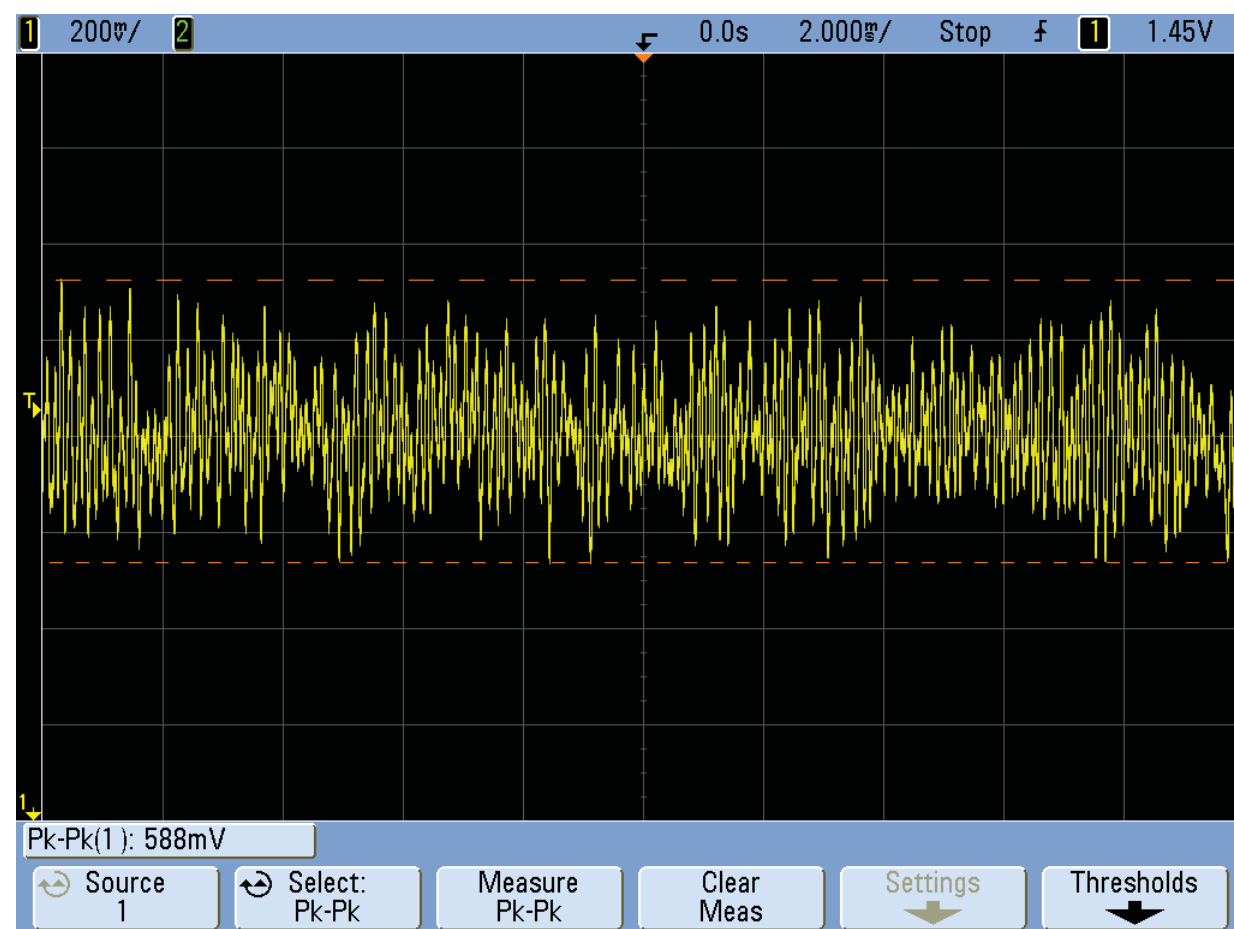


MP 59 (TP2203 VOPTO30)



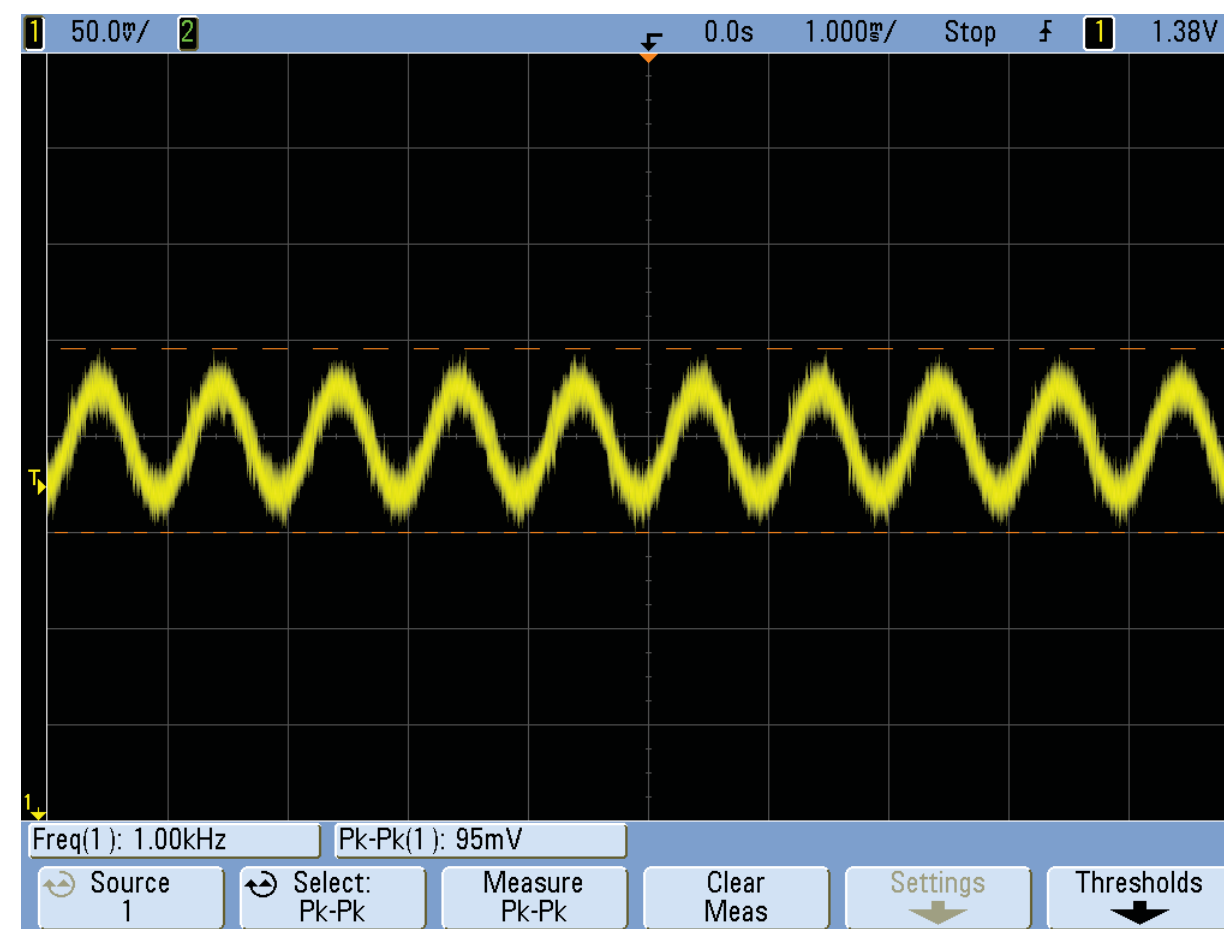
MP 100, MP 101 (L3126, L3125)

Note: This is an example! The shape of the signal can be different.

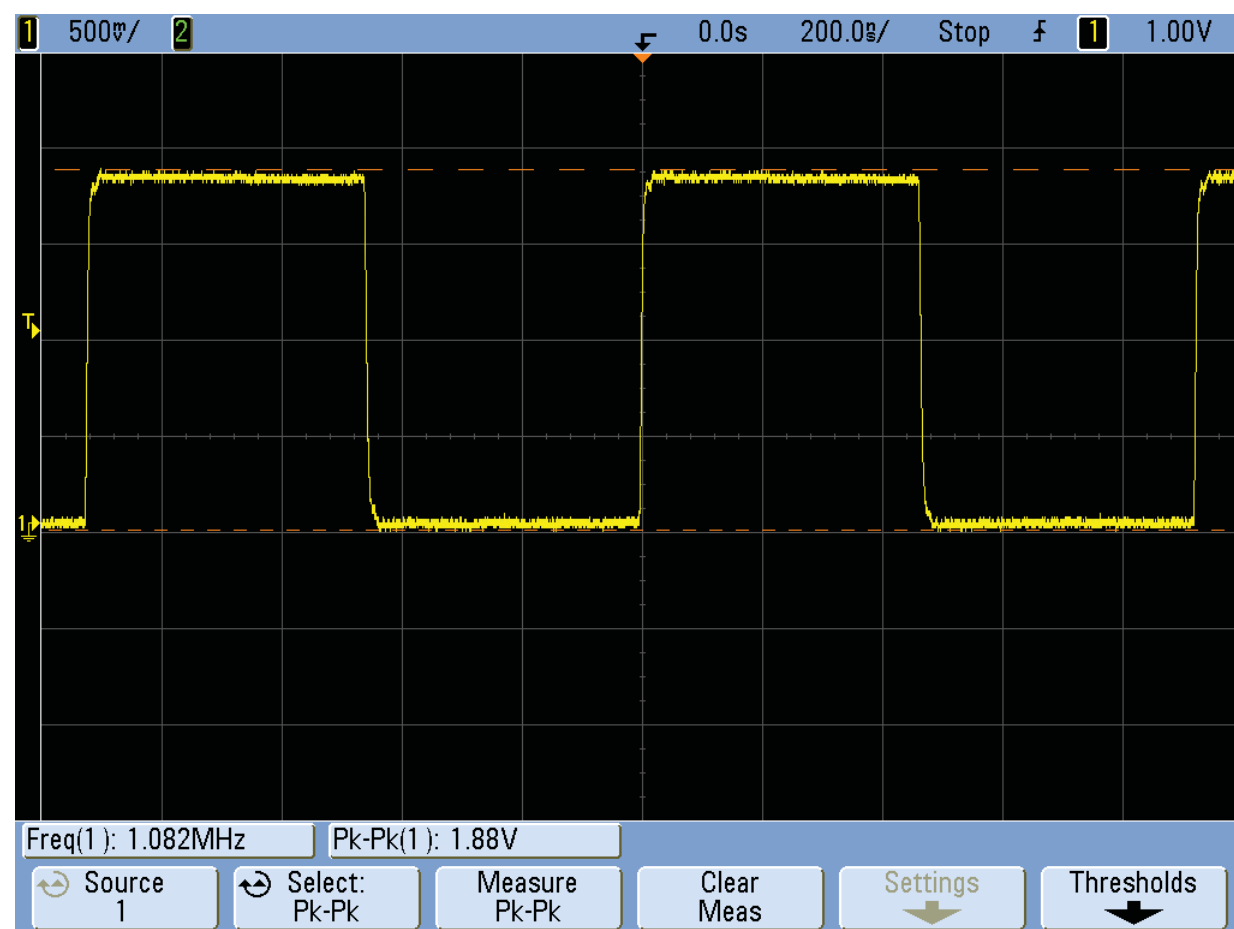


MP 99, MP 102 (C3125, C3124)

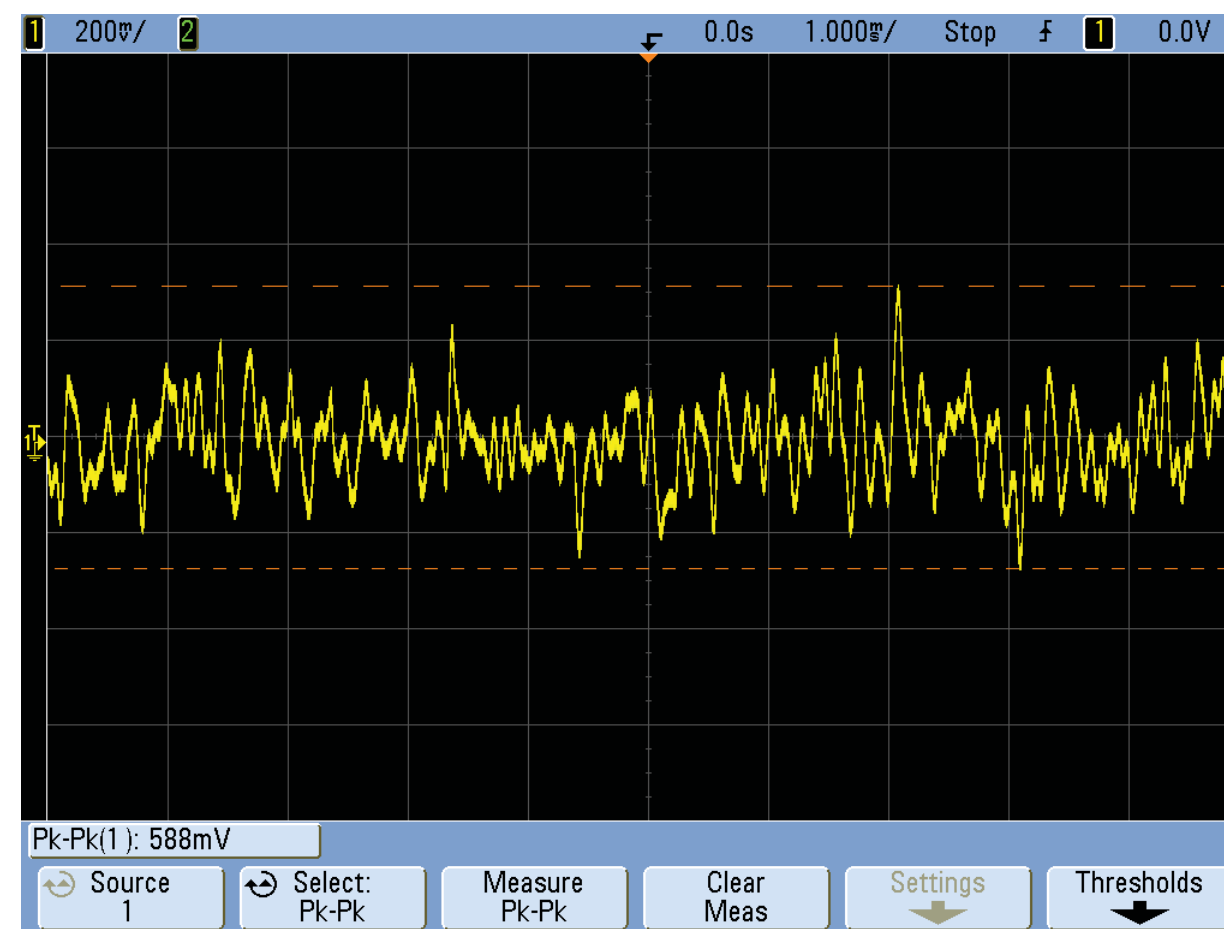
Note: This is an example! The shape of the signal can be different.



MP 103 (C3146)

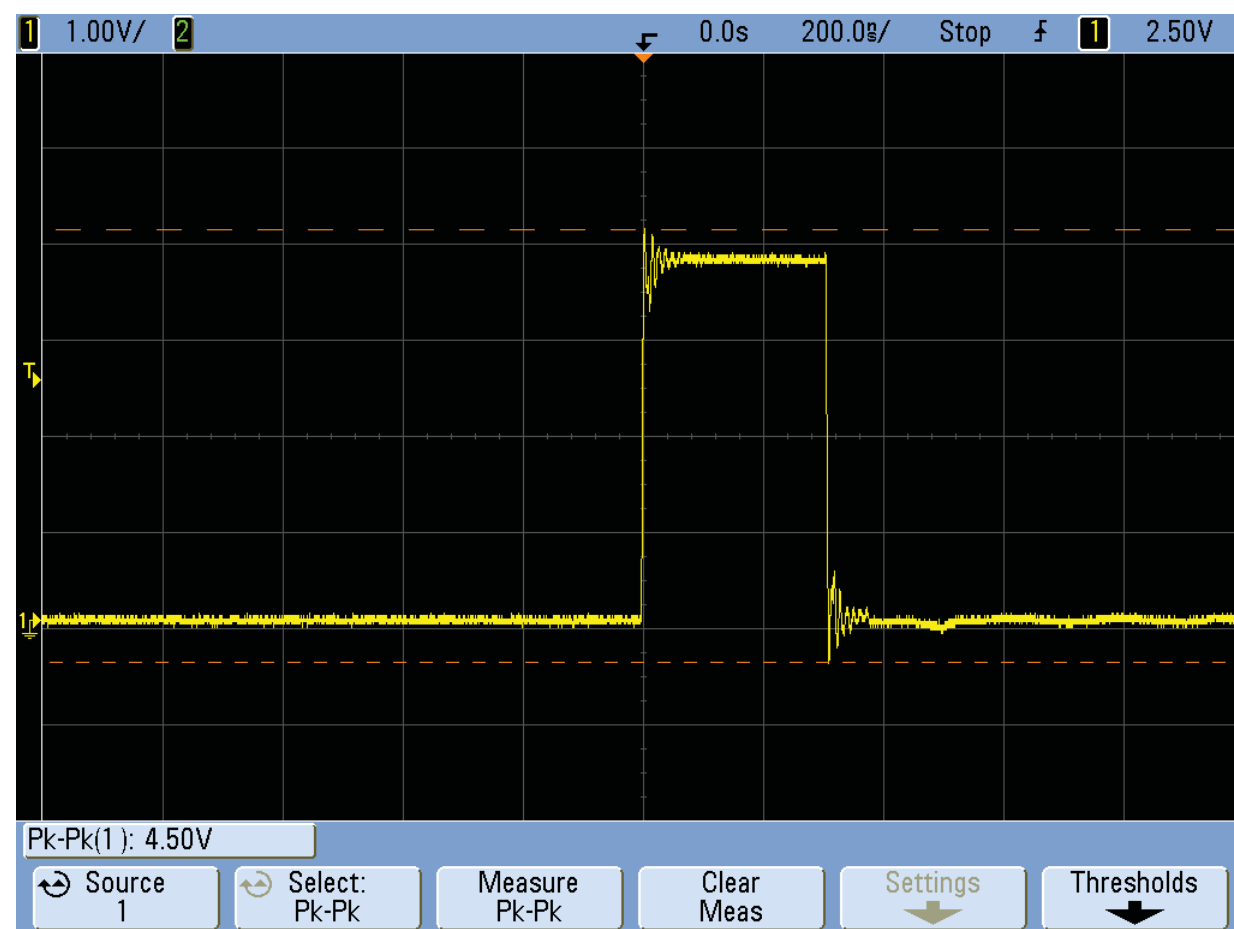


MP 107 (ST2410)

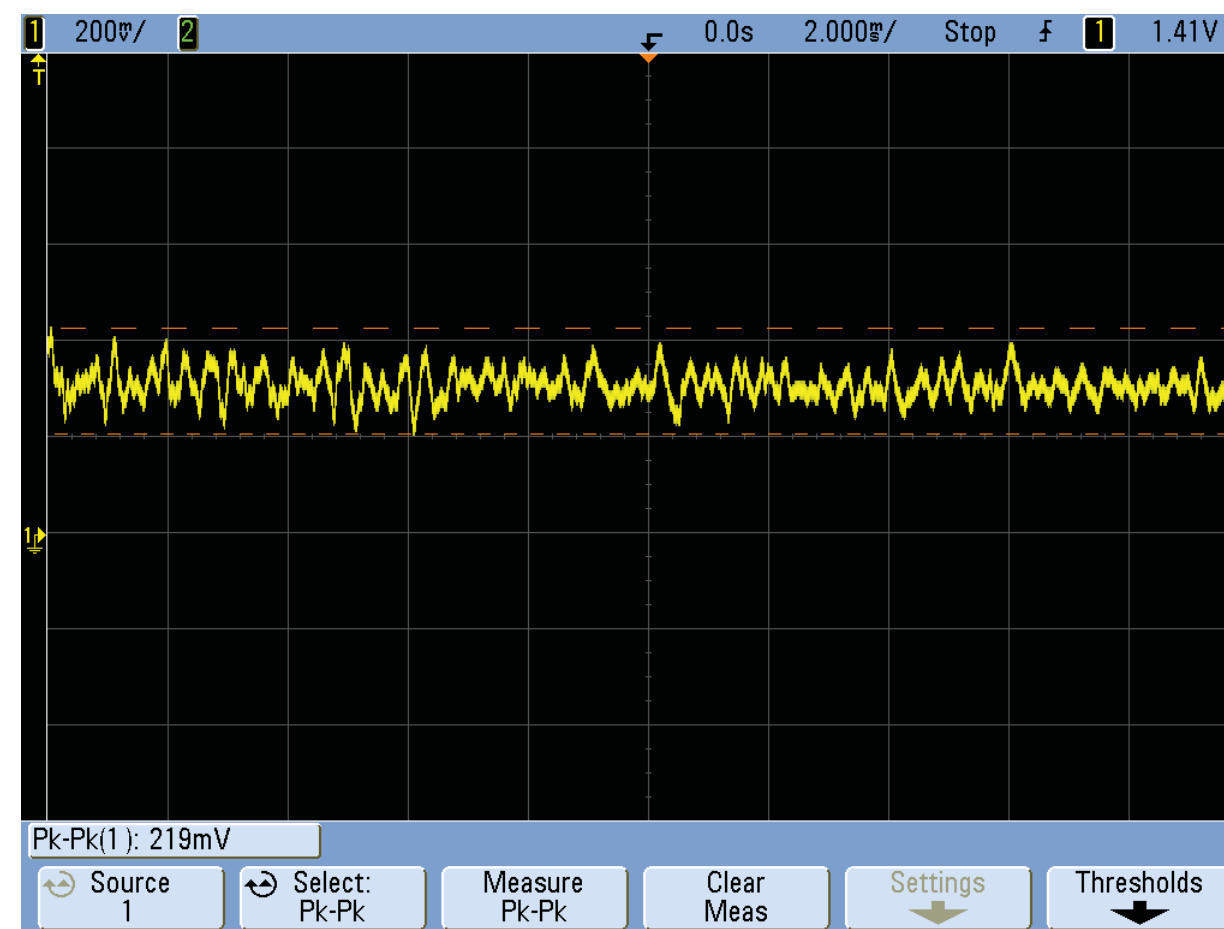


MP 108, MP 109 (L2403, L2404)

Note: This is an example! The shape of the signal can be different.

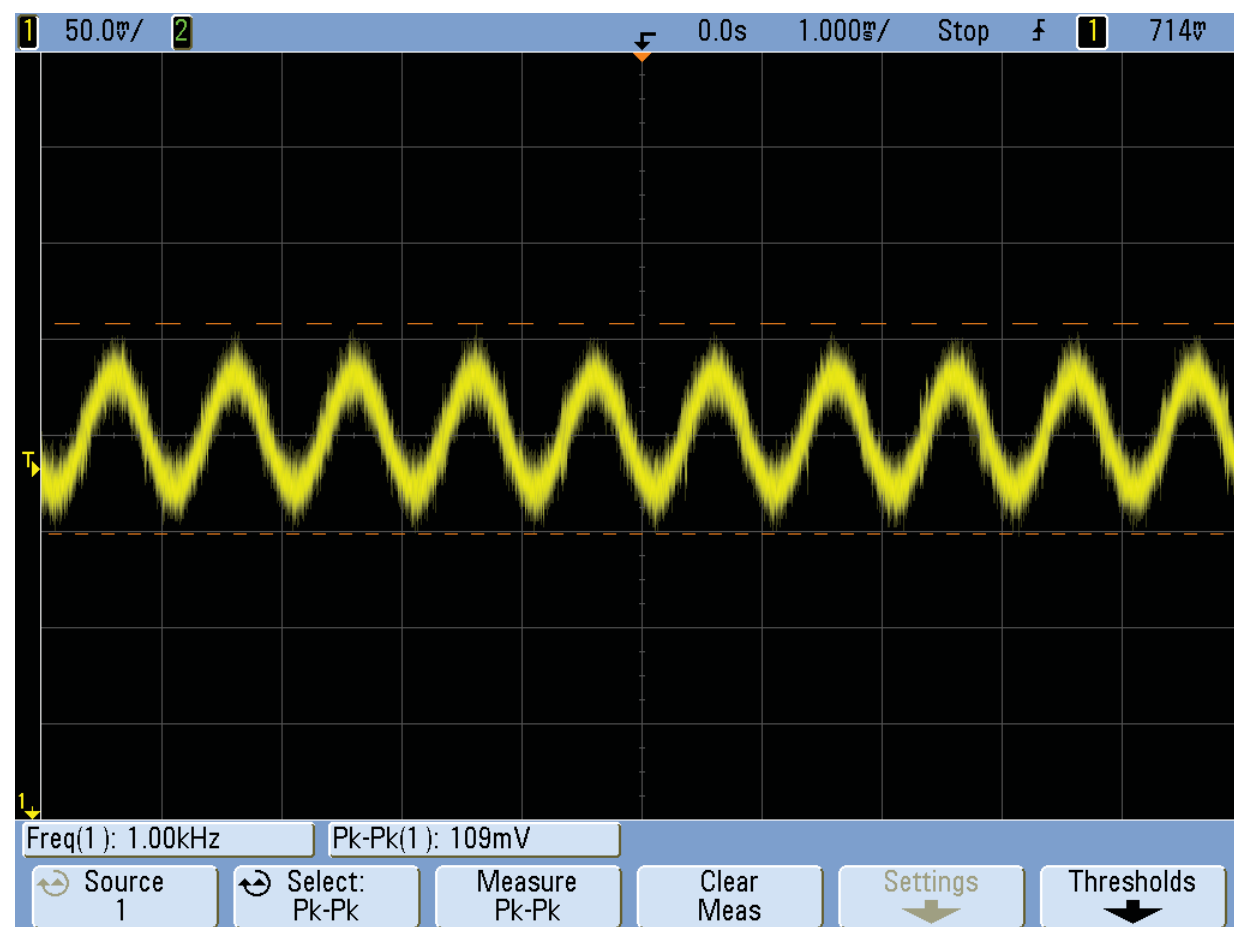


MP 117 (V4200_Pin 3)

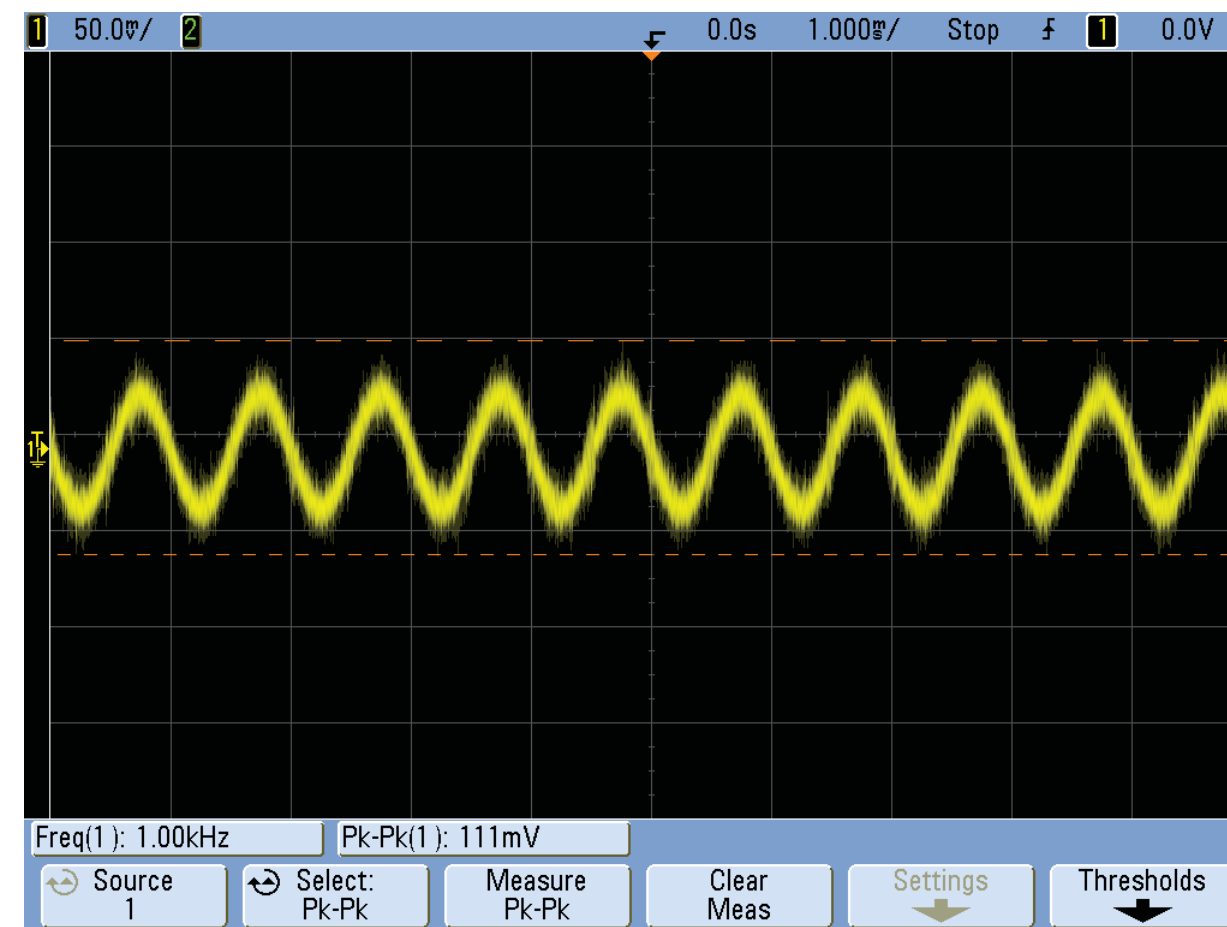


MP 98, MP 121 (C3156, C3155)

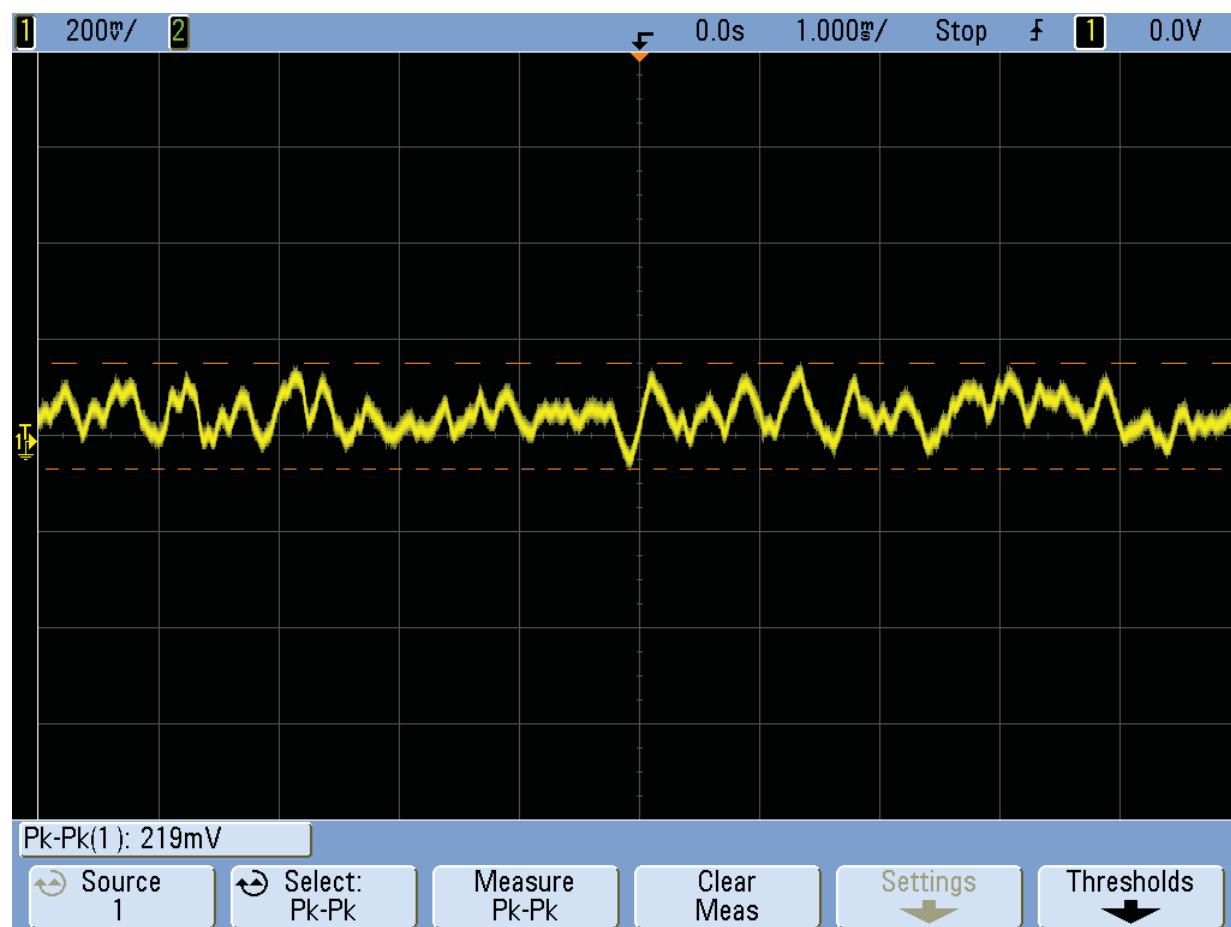
Note: This is an example! The shape of the signal can be different.



MP 122 (C3145)

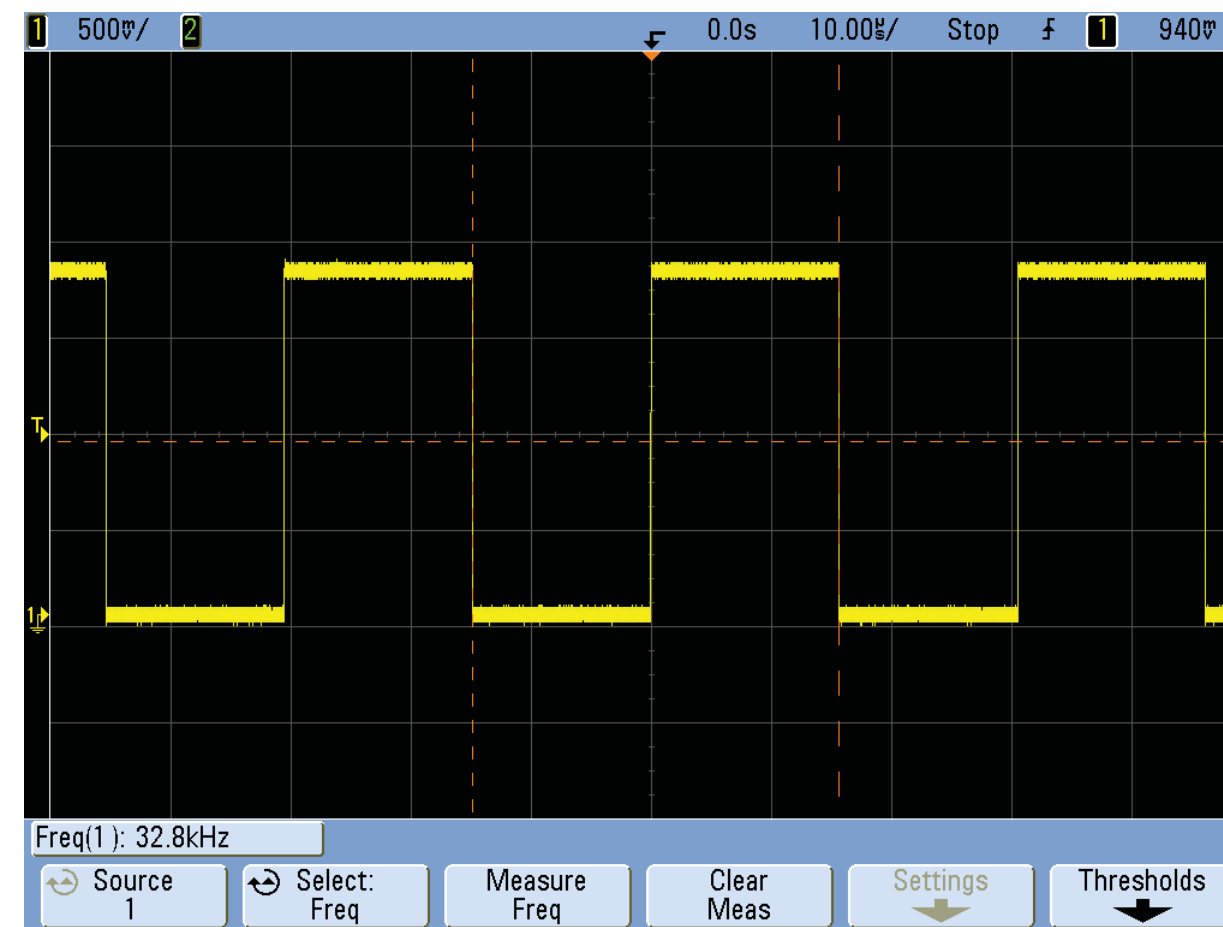


MP 123 (R3151 1 kHz)

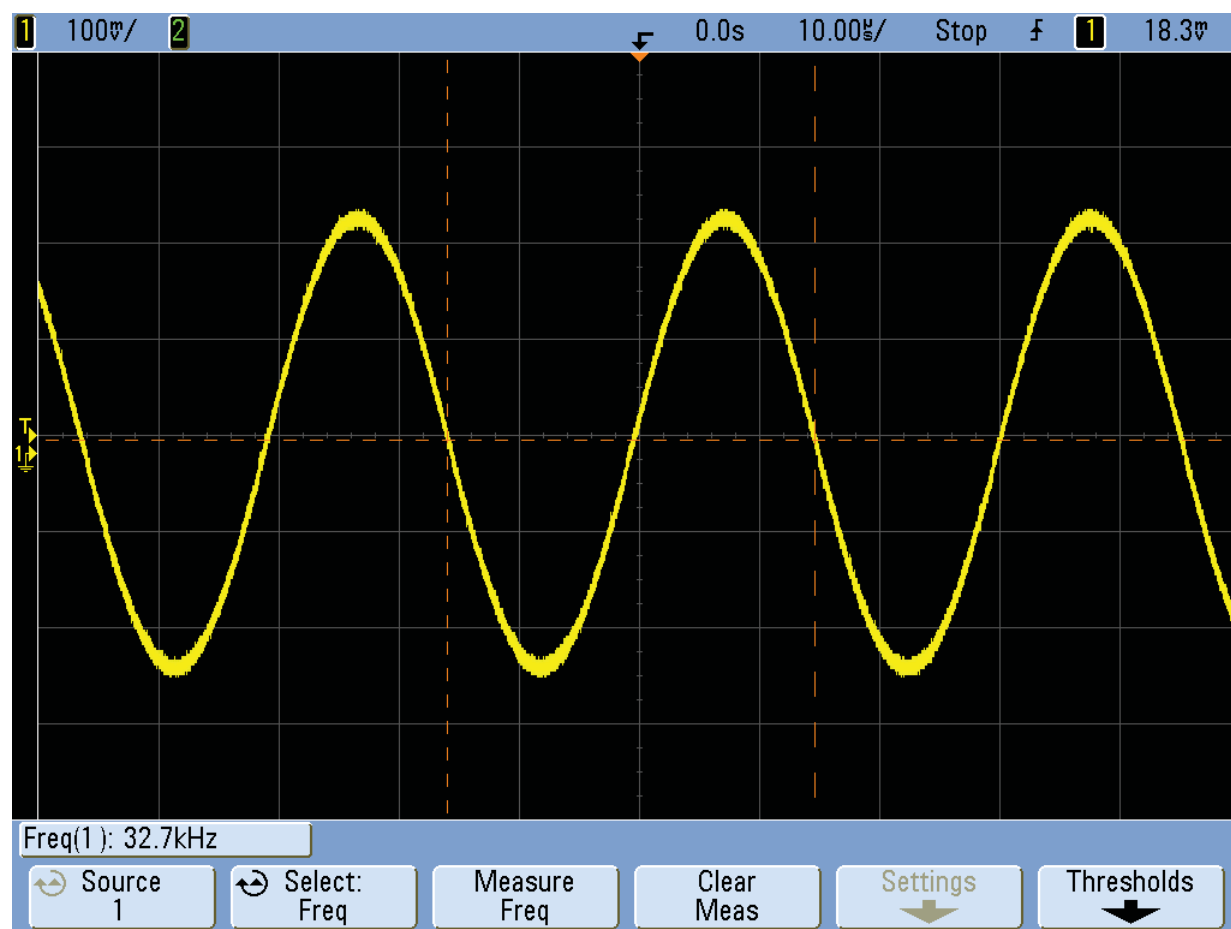


MP 123 (R3151) Handsfree (PHF) Problems TRS-Guide

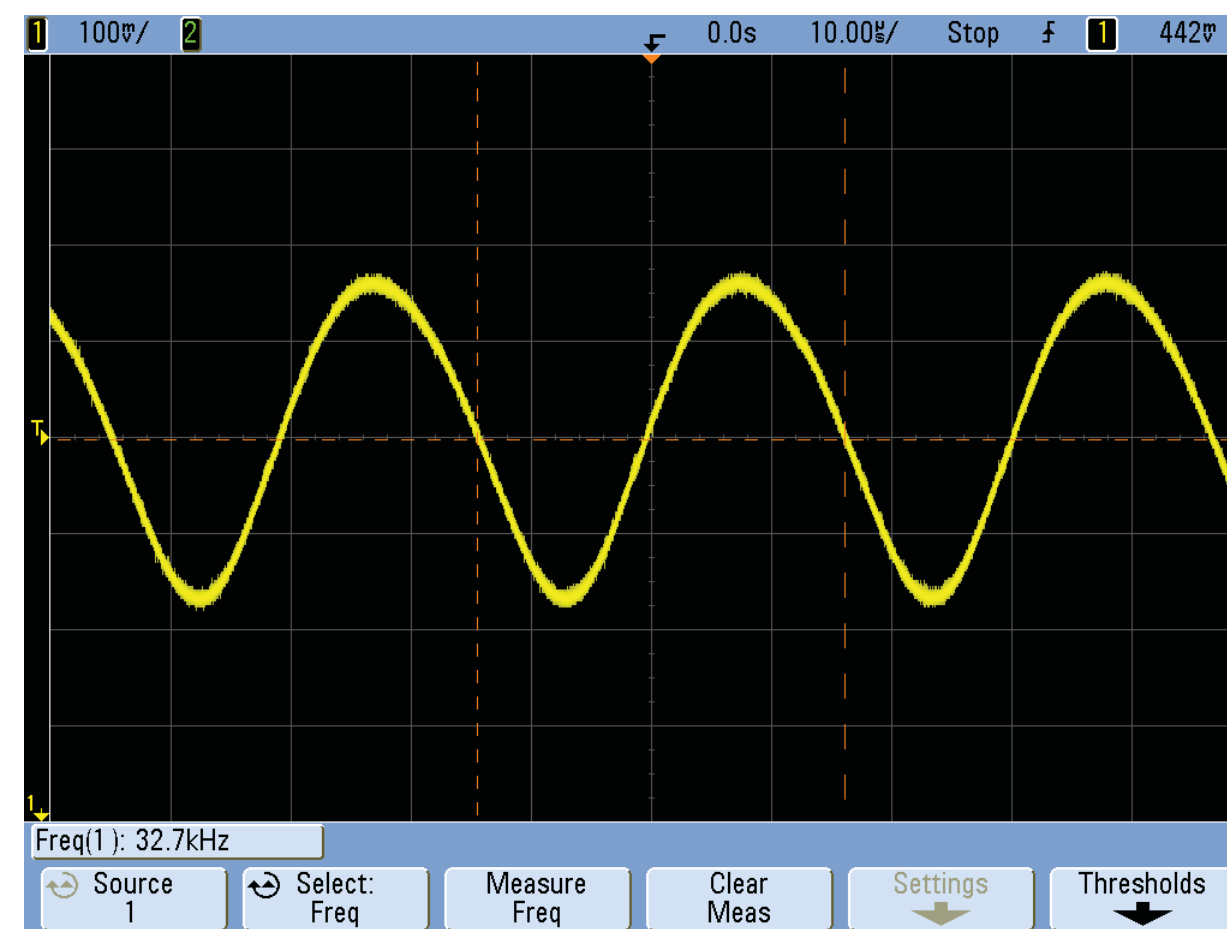
Note: This is an example! The shape of the signal can be different.



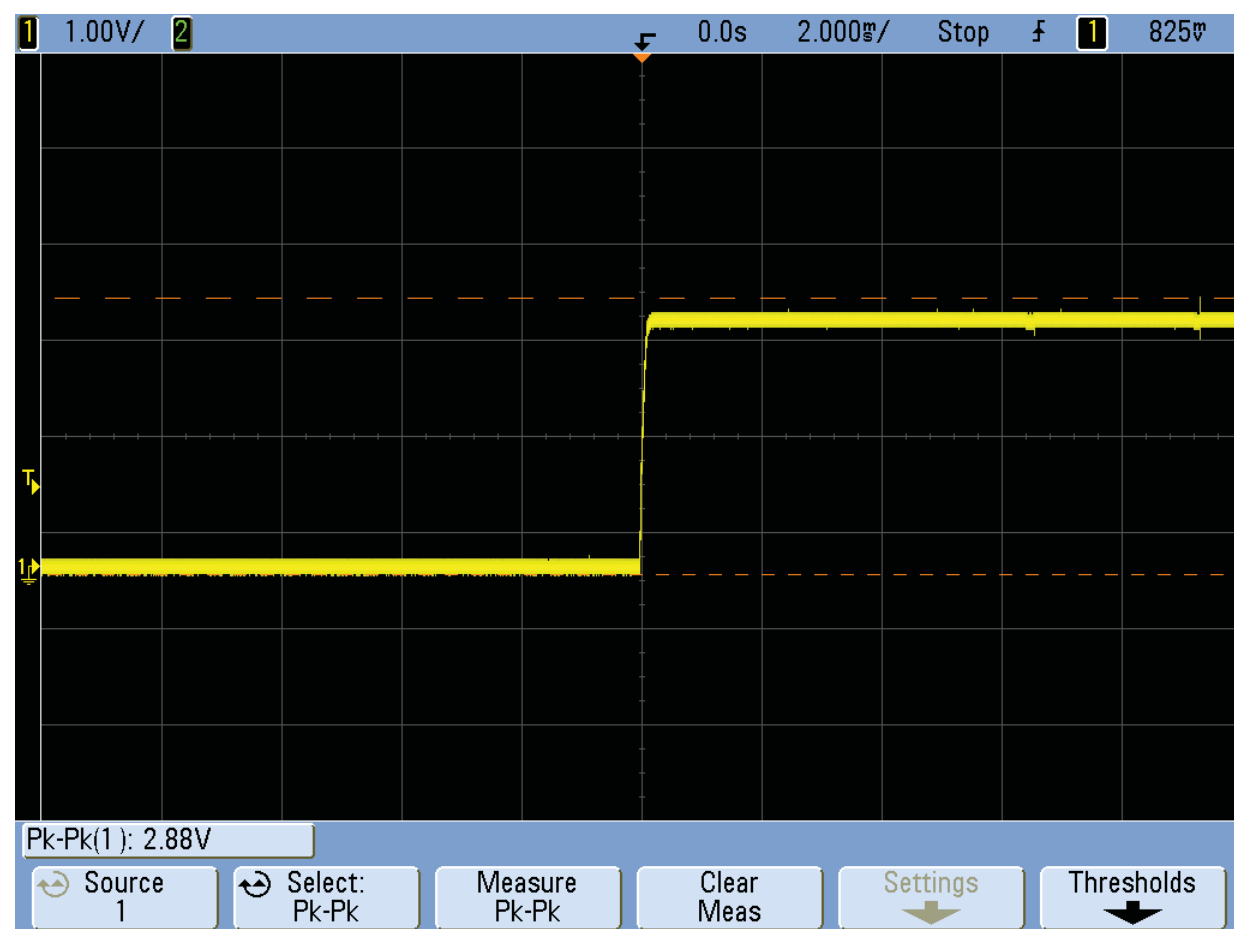
MP 135 (ST2104 RTCCLK)



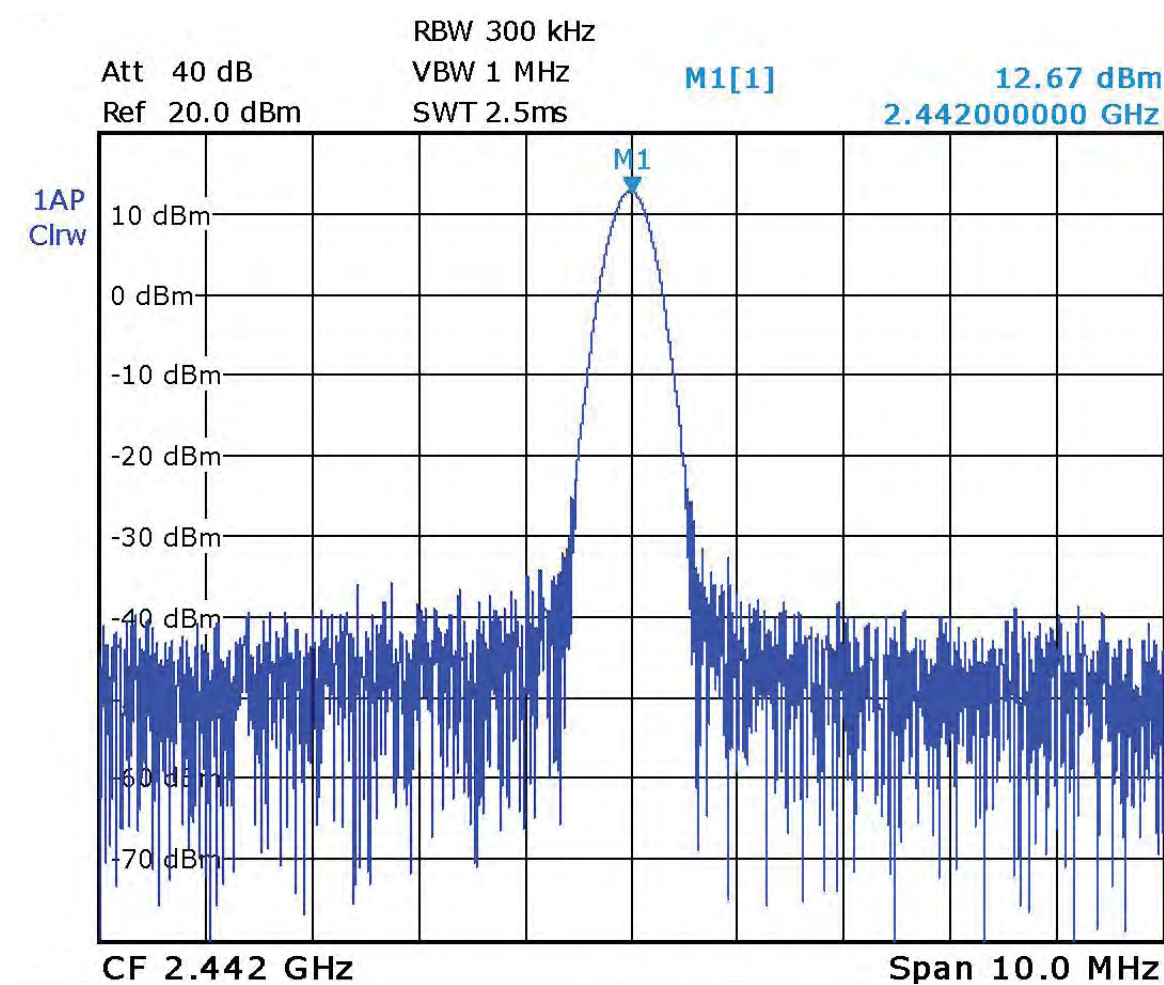
MP 136 (C2100 32 kHz)



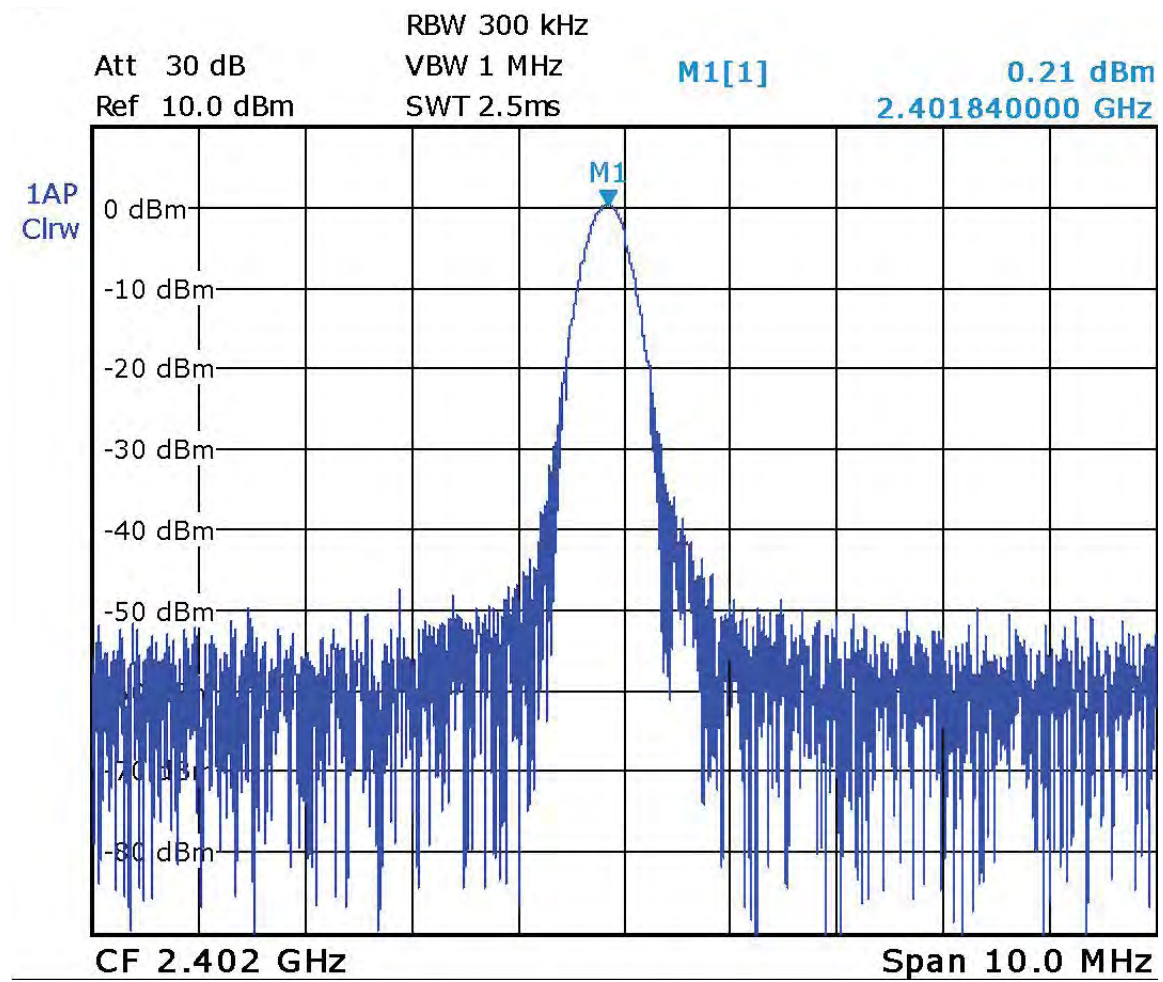
MP 138 (C2101 32 kHz)



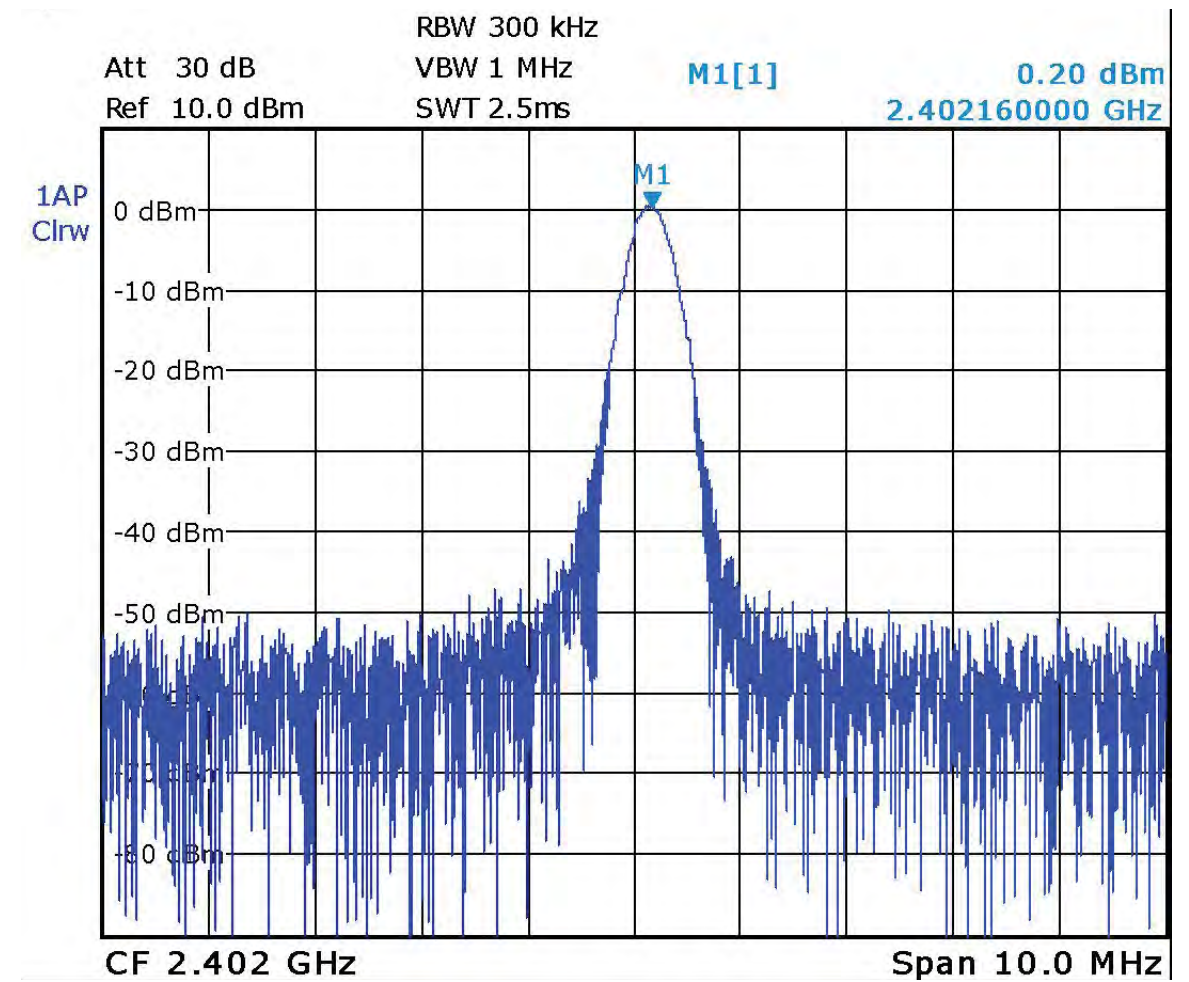
MP Vibrator + on TRS Fixture



WLAN TX Output Power

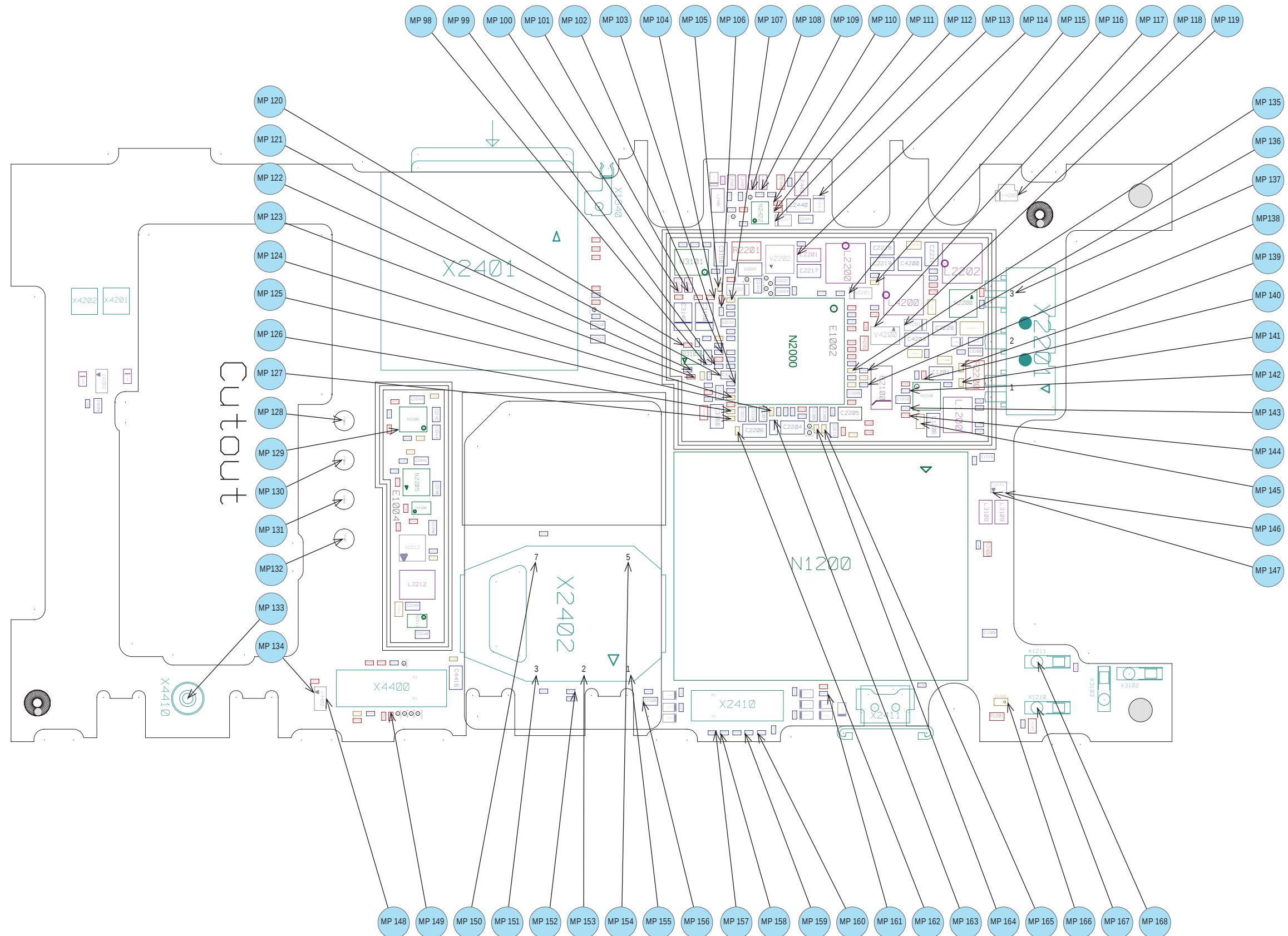


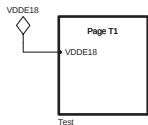
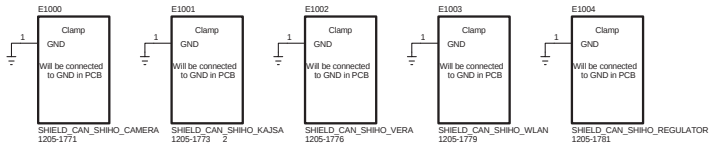
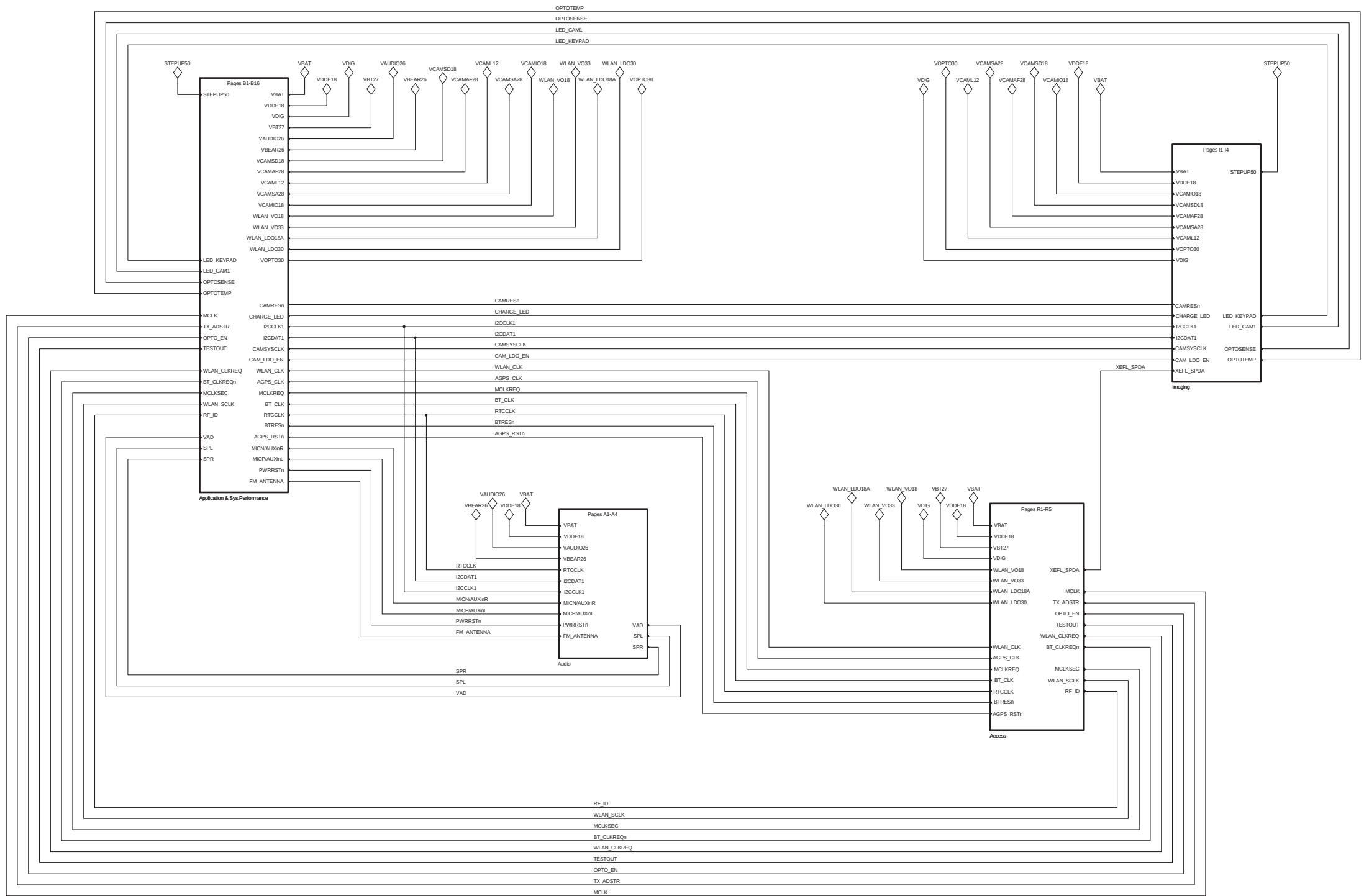
Blt MacPwr MOD 0



Blt MaxPwr MOD 1







Access side GPIO mapping		
Port	Usage	Page
AccGPIO00	USB_HSSTP	B14
AccGPIO01	USB_HSDIR	B14
AccGPIO02	CTMS	B14
AccGPIO03	CFMS	B14
AccGPIO04	USB_HSINCLK	B14
AccGPIO05	USB_HSNXT	B14
AccGPIO06	USB_HSDATA4	B14
AccGPIO07	USB_HSDATA5	B14
AccGPIO08	USB_HSDATA6	B14
AccGPIO09	USB_HSDATA7	B14
AccGPIO10	UART3_RX	R04
AccGPIO11	UART3_TX	R04
AccGPIO12	UART3_CTS	R04
AccGPIO13	UART3_RTS	R04
AccGPIO14	CH_DET_OP	B14
AccGPIO15	CH_DET_OM	B14
AccGPIO16	USB_HSCHIP_SEL	B14
AccGPIO17	AGPS_SYNC	R04
AccGPIO18	USB_SYNC	B14
AccGPIO19	WLAN_SPL_CSn	R05
AccGPIO20	ACC_SPL_Di	R03
AccGPIO21	ACC_SPL_DO	R03
AccGPIO22	ACC_SPL_CLK	R03
AccGPIO23	OVP_FLAG	B14
AccGPIO24	not used	T01
AccGPIO25	WLAN_SPL_IRQ	R05
AccGPIO26	BT_SPL_CSn	R03
AccGPIO27	BT_SPL_INT	R03

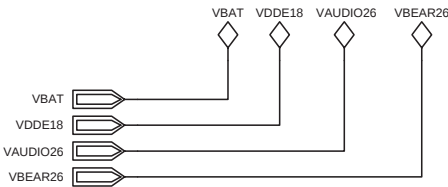
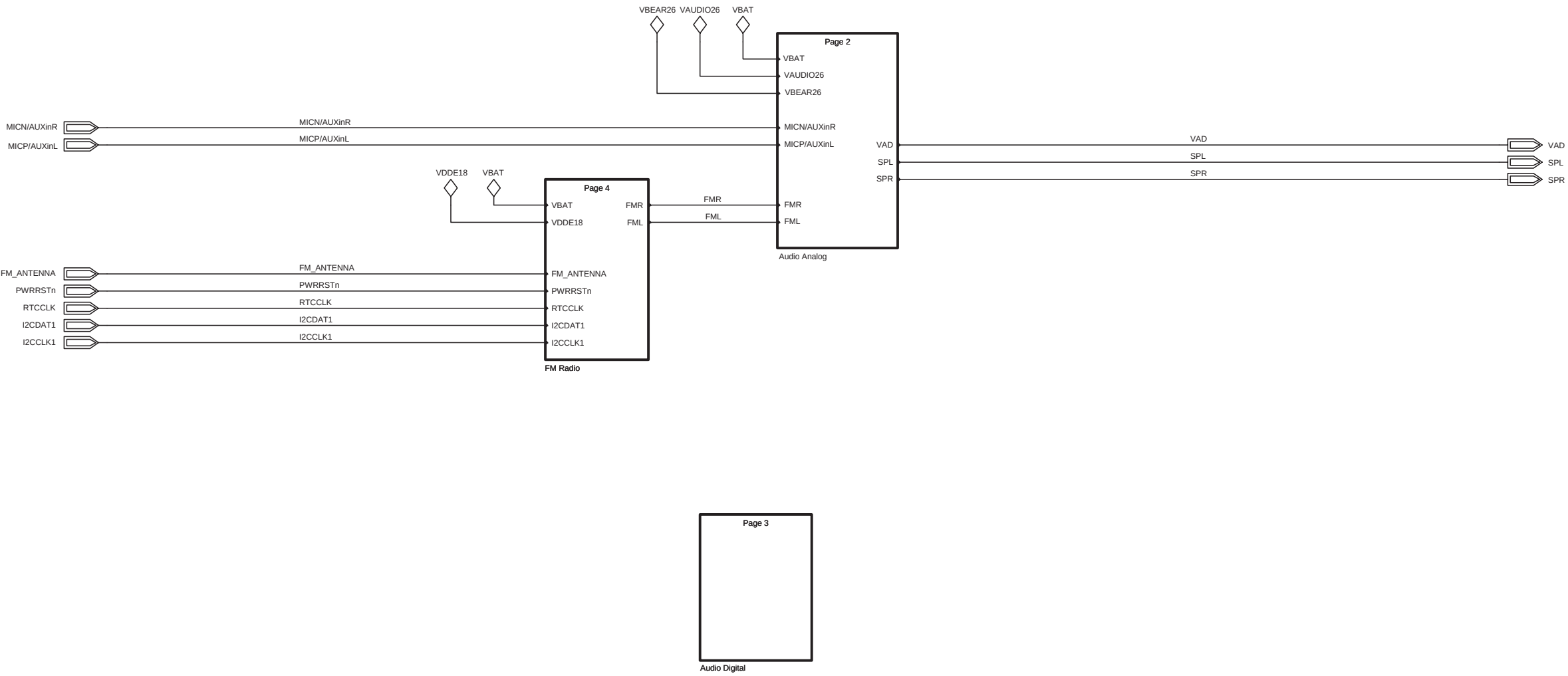
BT-chip GPIO mapping		
Port	Usage	Page
BTGPIO0	WLAN_CONFIRM	R03
BTGPIO8	WLAN_BT_STATE	R03
BTGPIO9	not used	R03
BTGPIO10	not used	R03
BTGPIO11	WLAN_BT_PRIORITY	R03
BTGPIO16	not used	R03

Application side GPIO mapping		
Port	Usage	Page
AppGPIO00	FM_INT	A04
AppGPIO01	APP_LOG	B14
AppGPIO02	CAMIRQ	R03
AppGPIO03	COVER_OPEN	R03
AppGPIO04	SLIDE_SENSE	B15
AppGPIO05	VIDCC_SPL_CS	B16
AppGPIO06	VTI15_EN	B06
AppGPIO07	VIDCC_SPL_Di	B16
AppGPIO08	VIDCC_SPL_DO	B16
AppGPIO09	VIDCC_SPL_CLK	B16
AppGPIO10	AGPS_CLK_EN	B03
AppGPIO11	X_CHARGE_RDY	B14
AppGPIO12	MSDETECT	B13
AppGPIO13	AFLED_EN	B14
AppGPIO14	TV_CS	B02
AppGPIO15	DCON	xxx
AppGPIO16	VIDCC_INT	B16
AppGPIO17	FM_SELECT	A02
AppGPIO18	VIDCC_RESn	B16
AppGPIO19	TV_RESn	B02

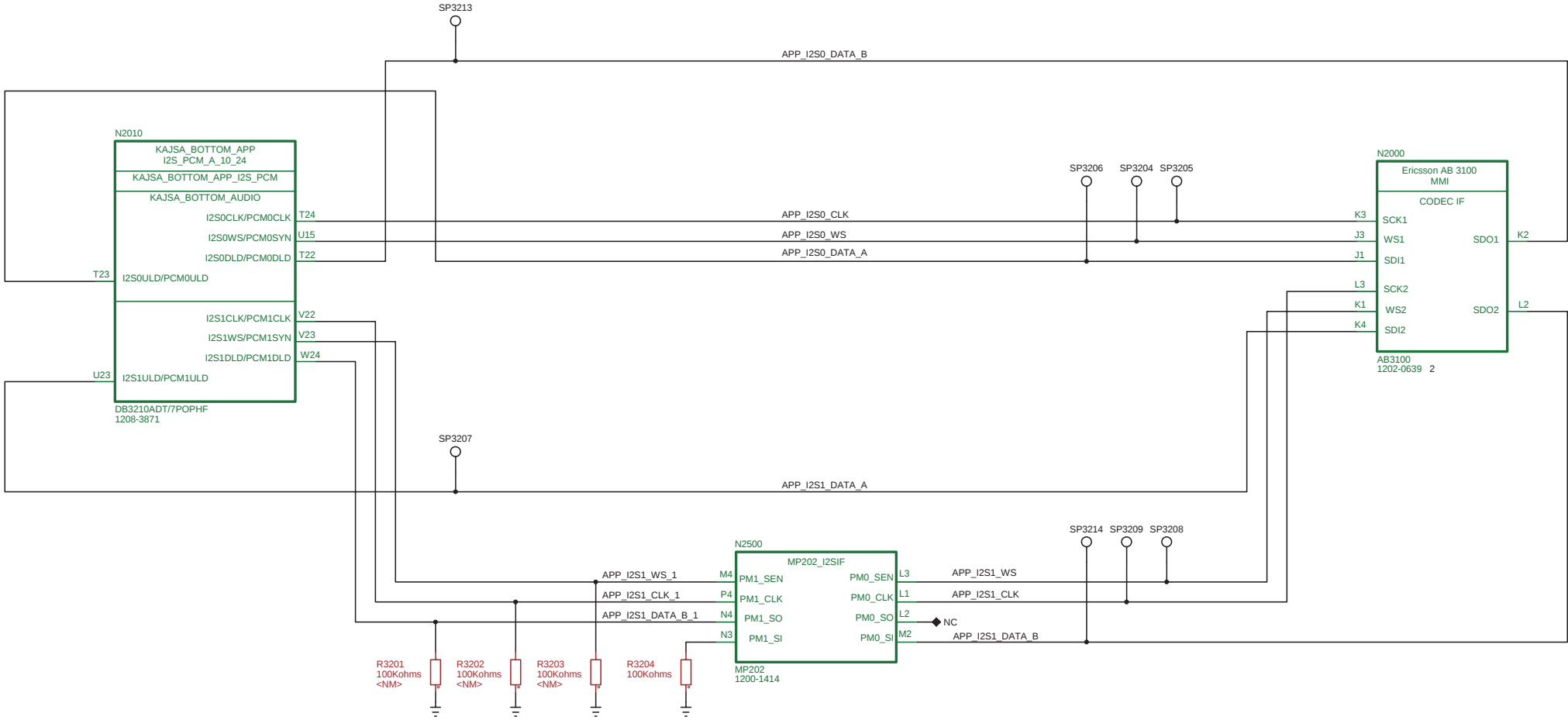
MP202 GPIO mapping		
Port	Usage	Page
GPIO_P0	not used	B16
GPIO_P1	not used	B16
GPIO_P2	not used	B16
GPIO_P3	not used	B16
P00	CAM_LDO_EN	B16
P01	not used	B16
P02	VCAMSD_EN	B16
P03	CAMRESn	B16
P04	VIDCC_L1DET	B16
P05	VIDCC_L1_EN	B16
P06	VIDCC_SDR_EN	B16
P07	VIDCC_CLKREQn	B16

GPIO expander mapping		
Port	Usage	Page
GPIO_00	not used	T01
GPIO_01	AGPS_LDO_EN	R04
GPIO_06	AMPCTRL	A02
GPIO_07	AGPS_PWRON	R04
GPIO_08	LED_TALLY	B14
GPIO_09	WLAN_RSTn_P0n	R05
GPIO_010	WLAN_P0n	B10
GPIO_011	XEFL_CHARGE_EN	R03
GPIO_012	XEFL_FCD	B14
GPIO_013	XEFL_SB	B14
GPIO_014	XEFL_SPD1	B14
GPIO_015	XEFL_SPD0	B14
GPIO_P2	AGPS_CLKREQn	B03
GPIO_P3	TV_CLKREQn	B03
GPIO_P4	not used	T01
GPIO_P5	not used	T01

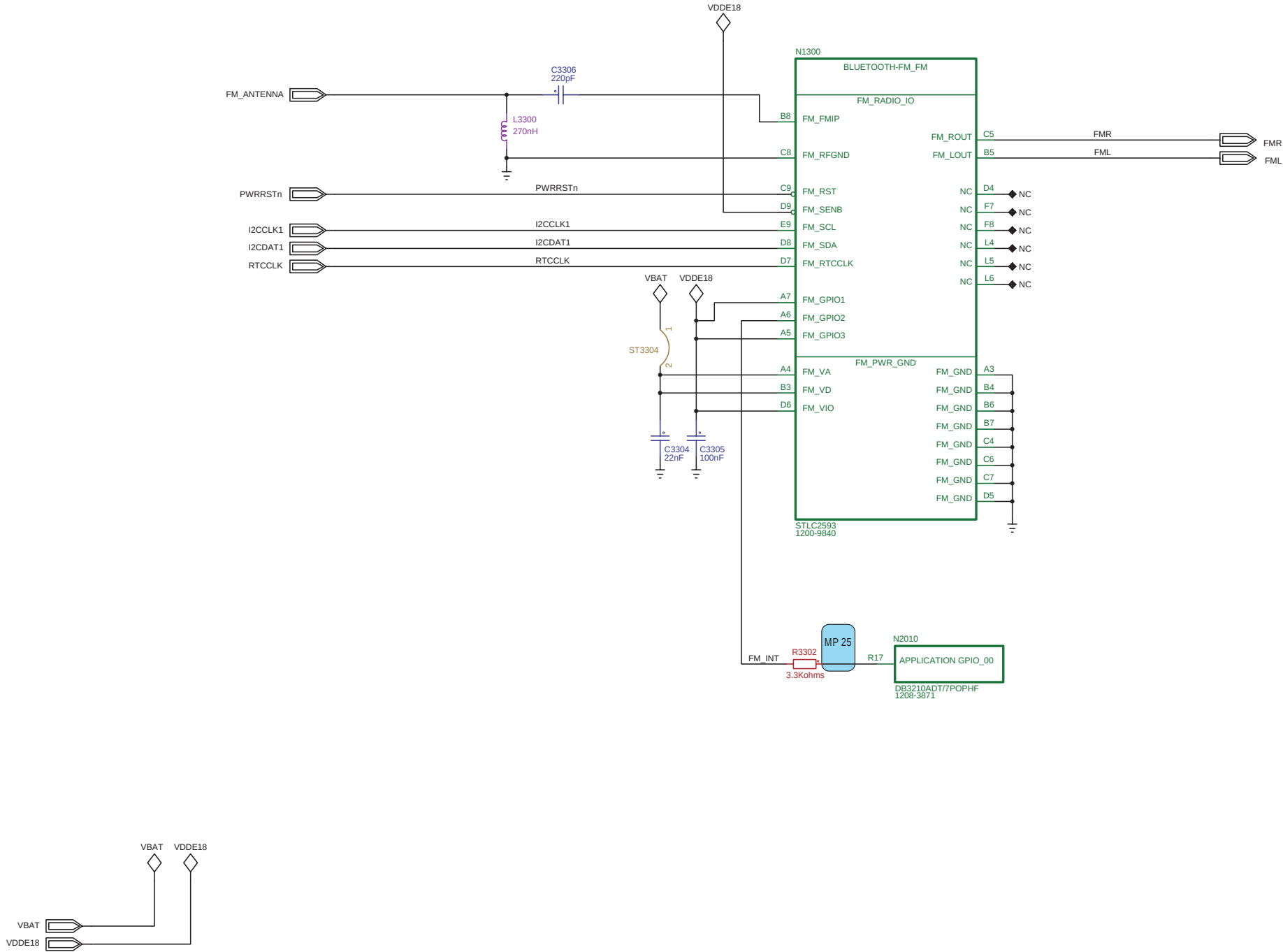
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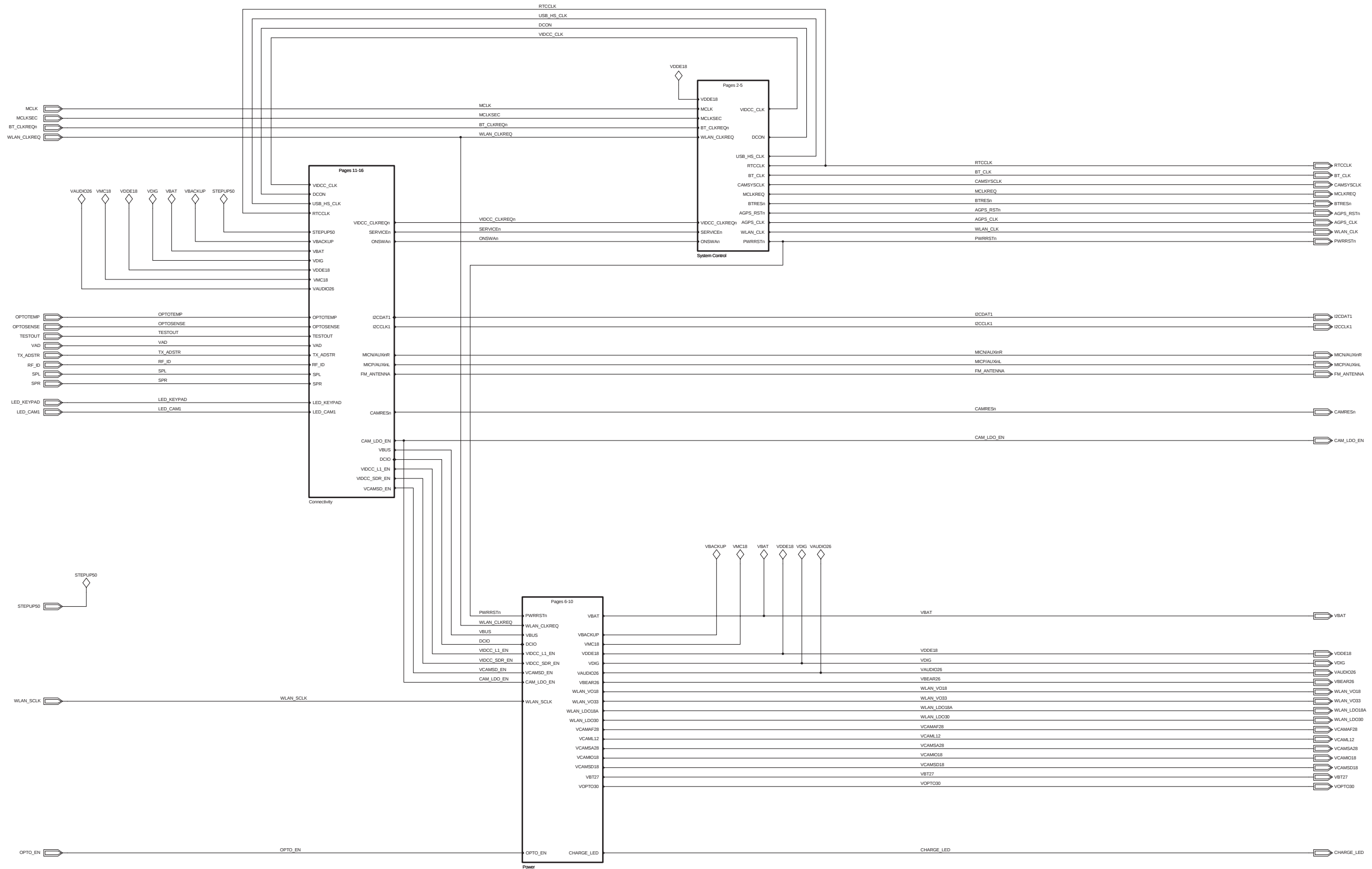
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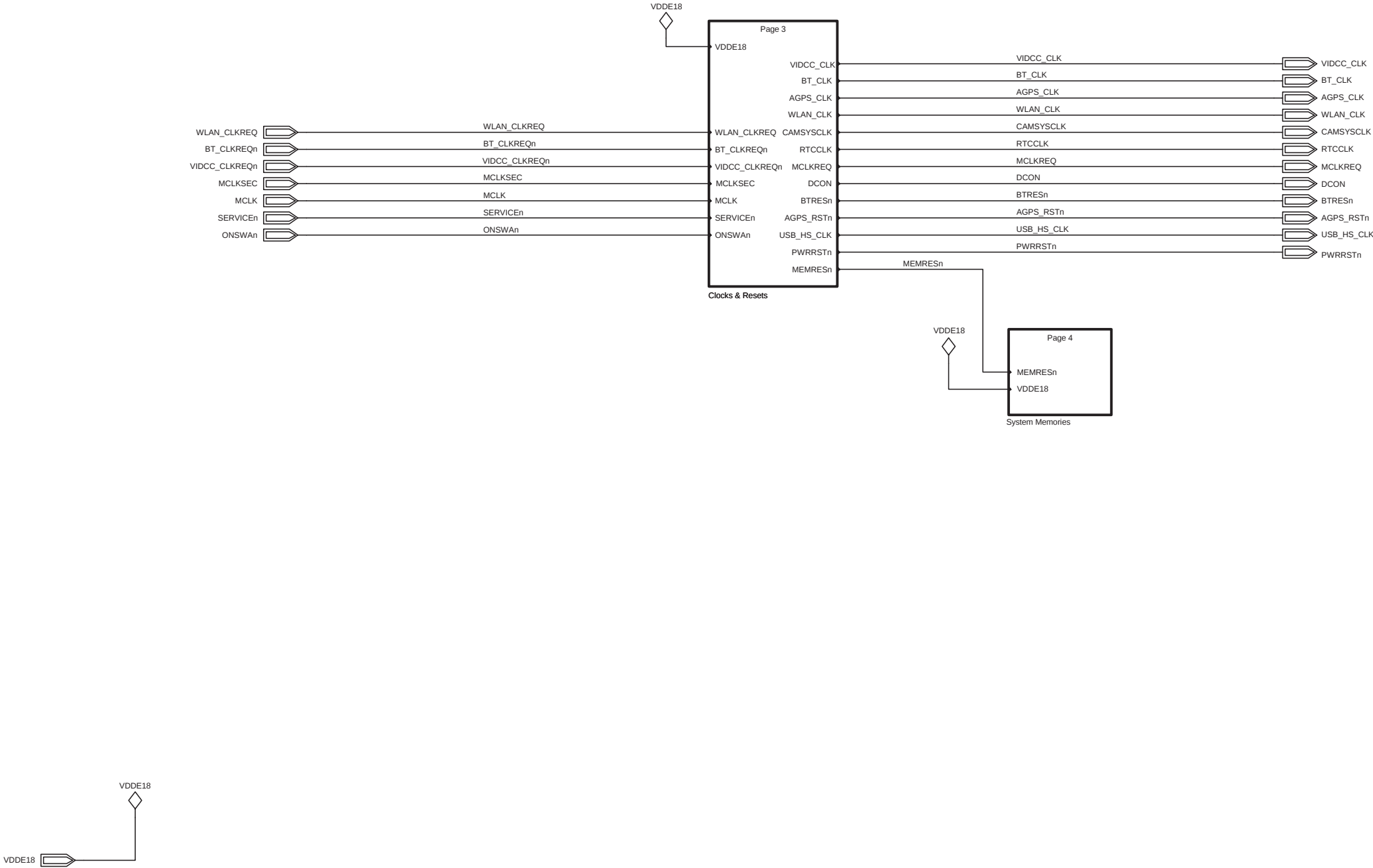
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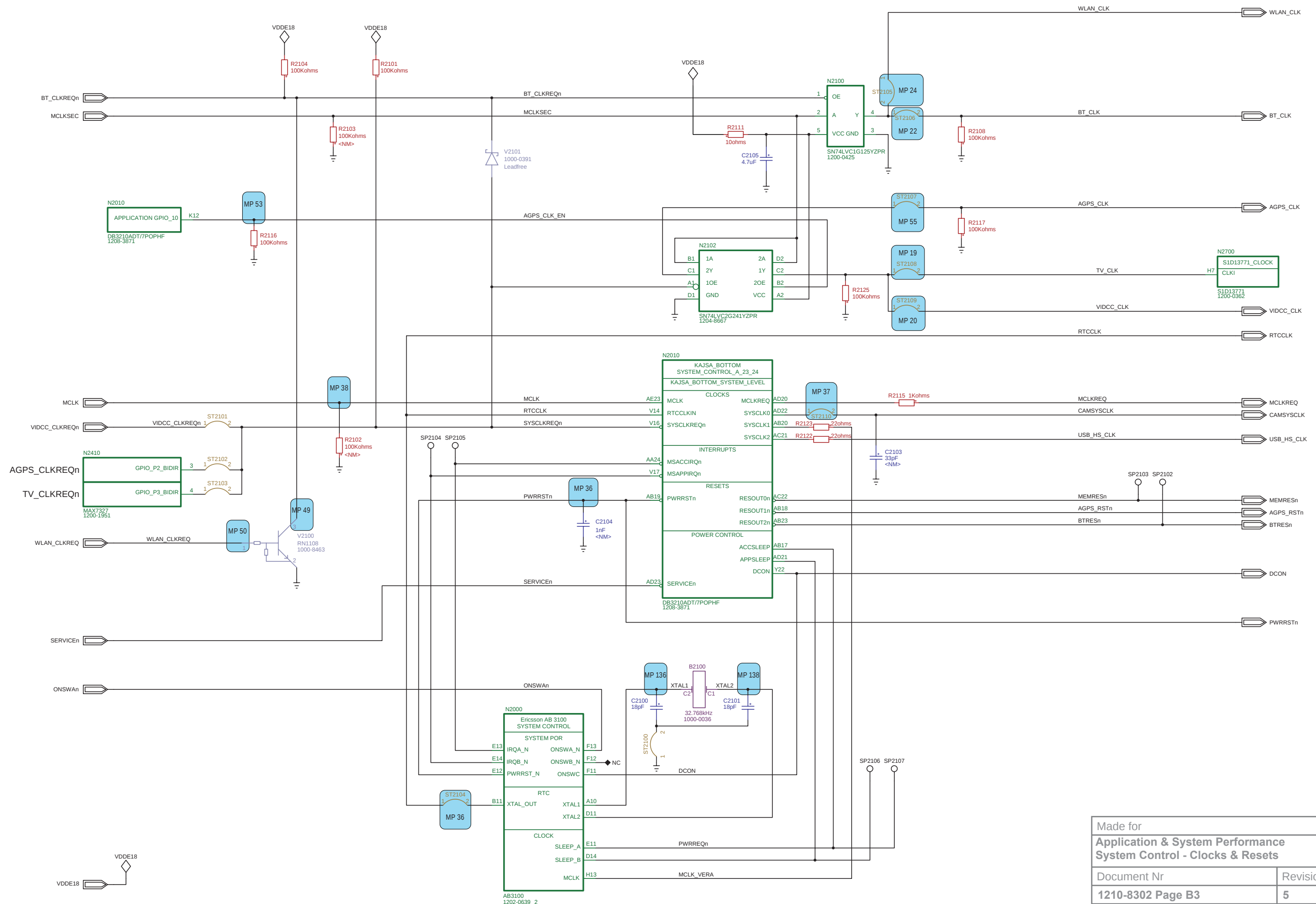
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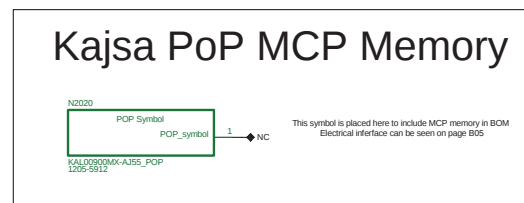
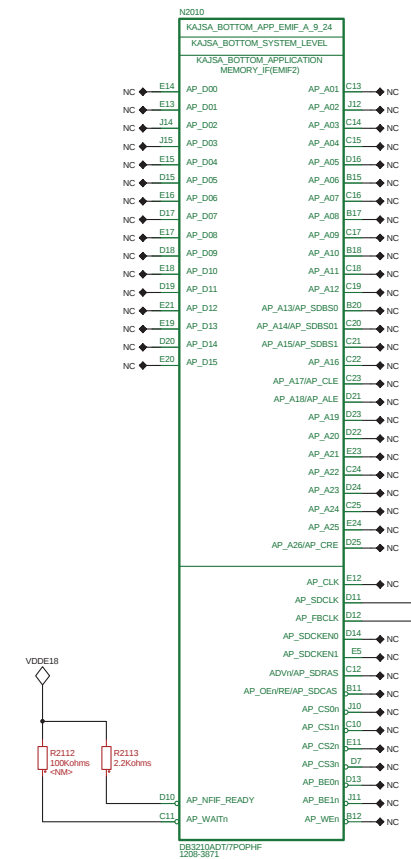
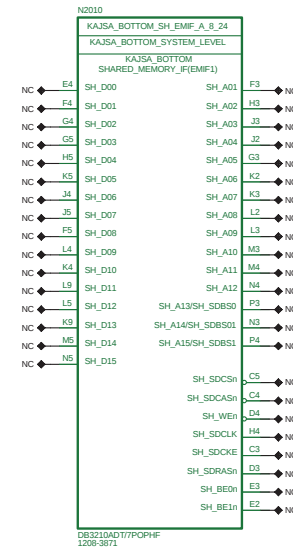
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Document Nr	Revision
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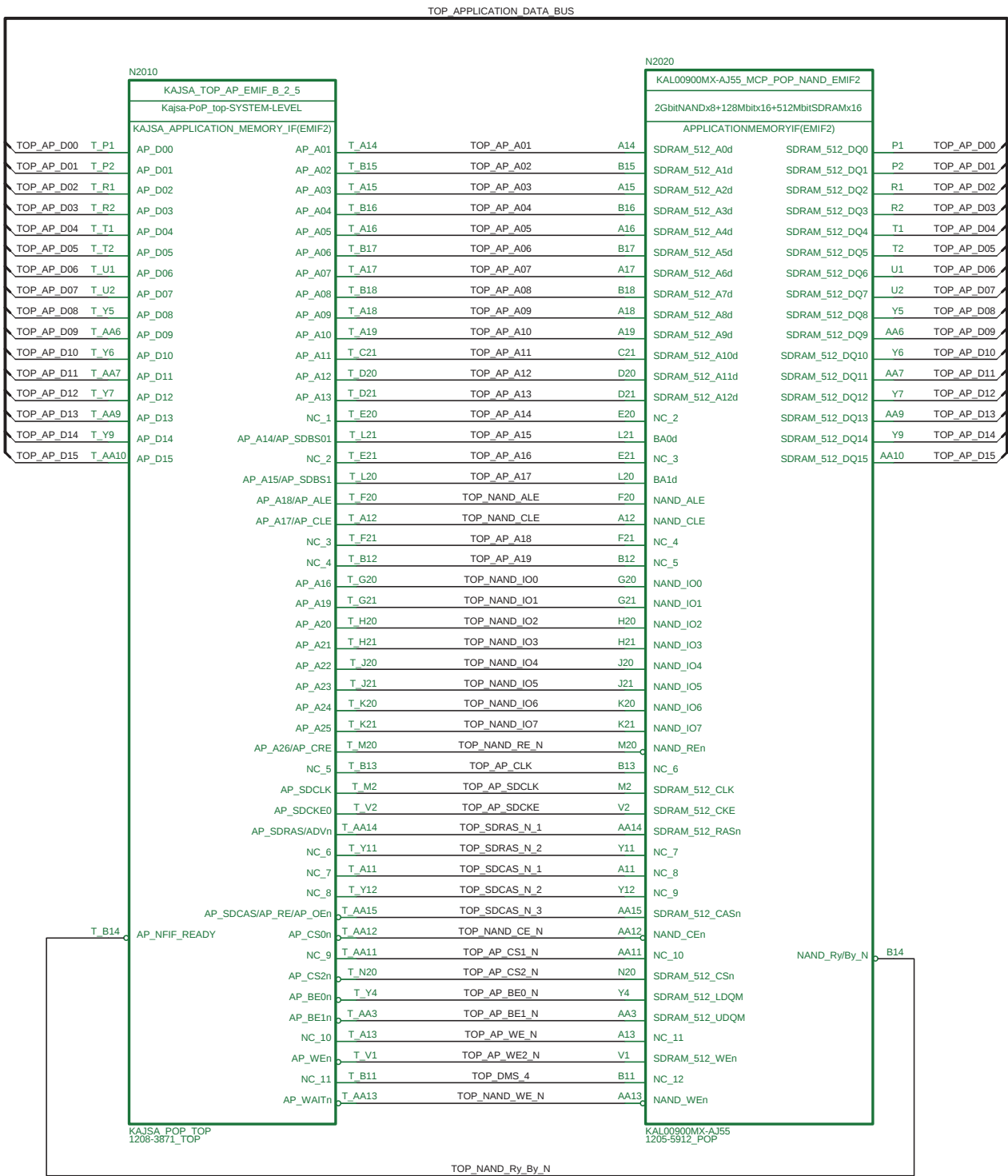
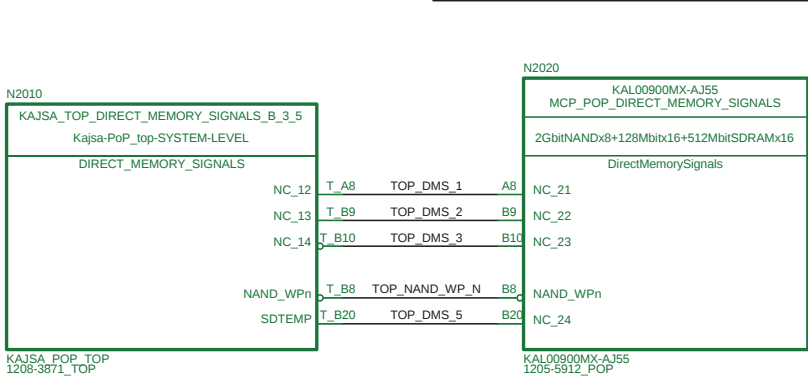
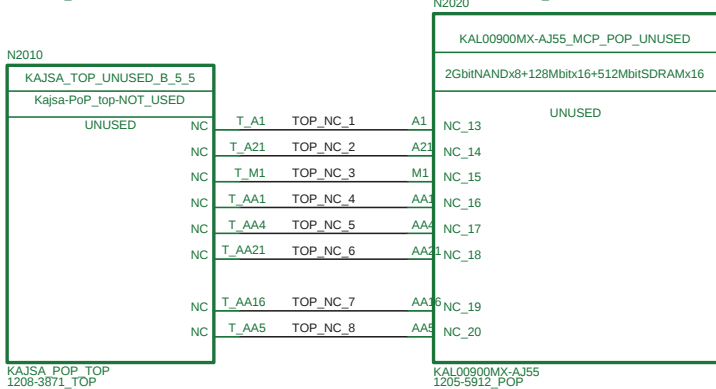
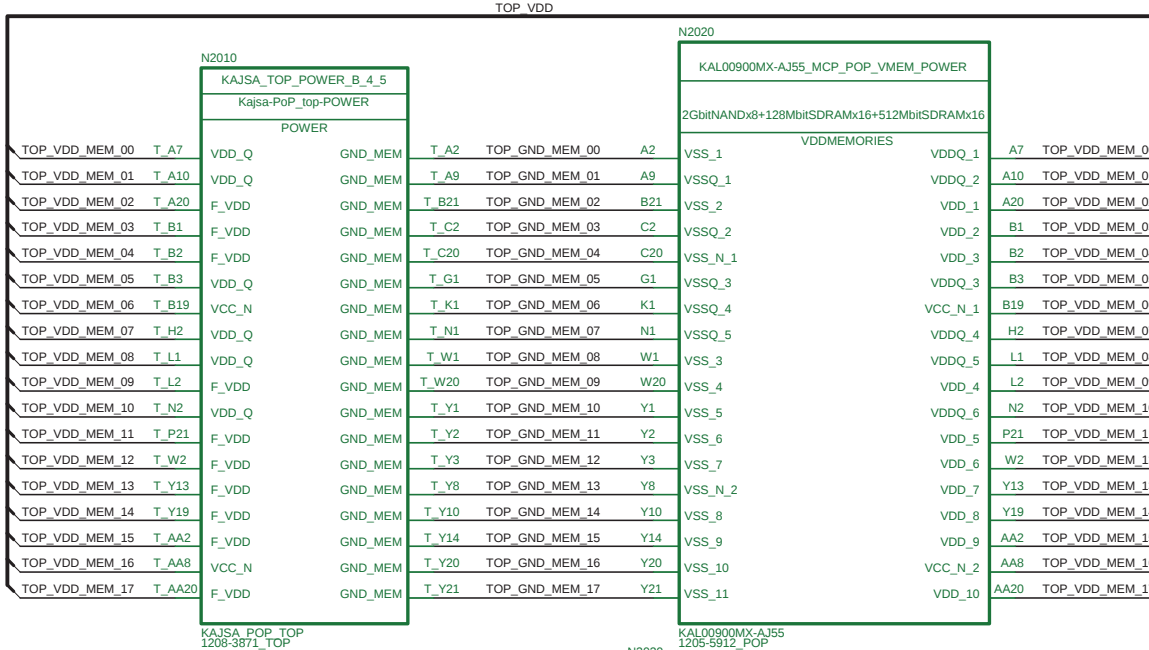
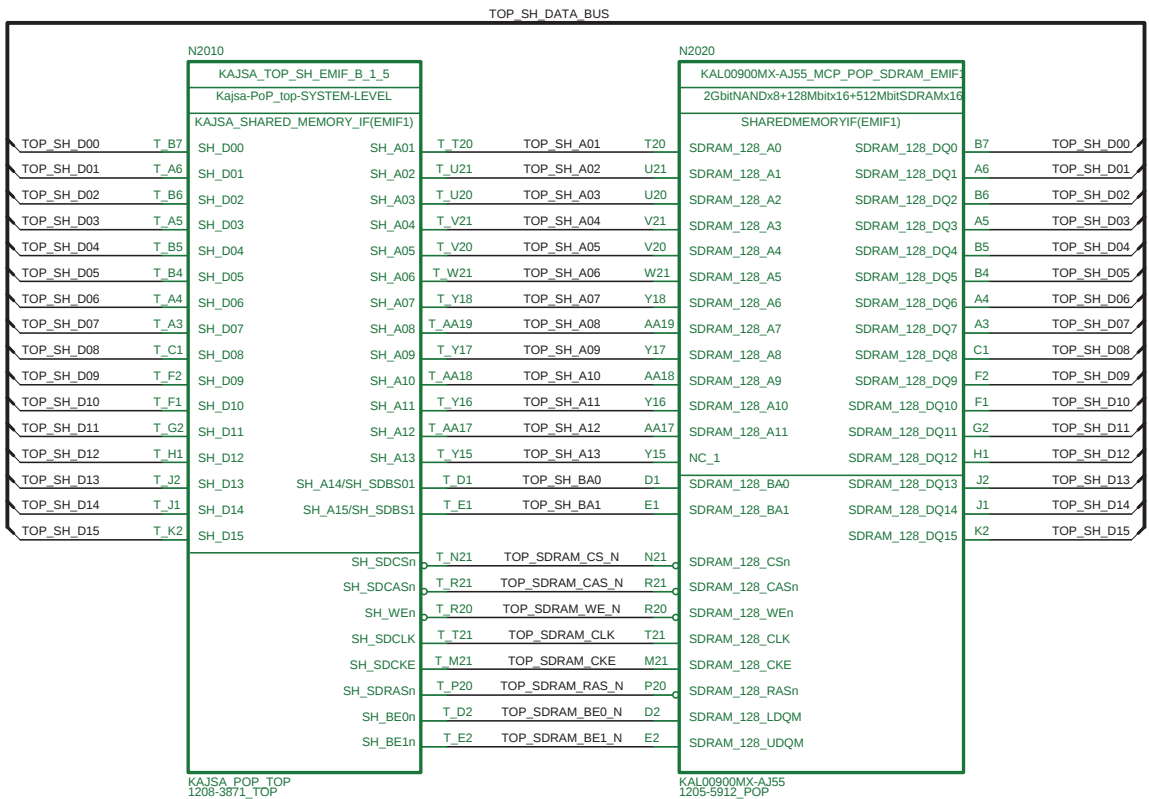


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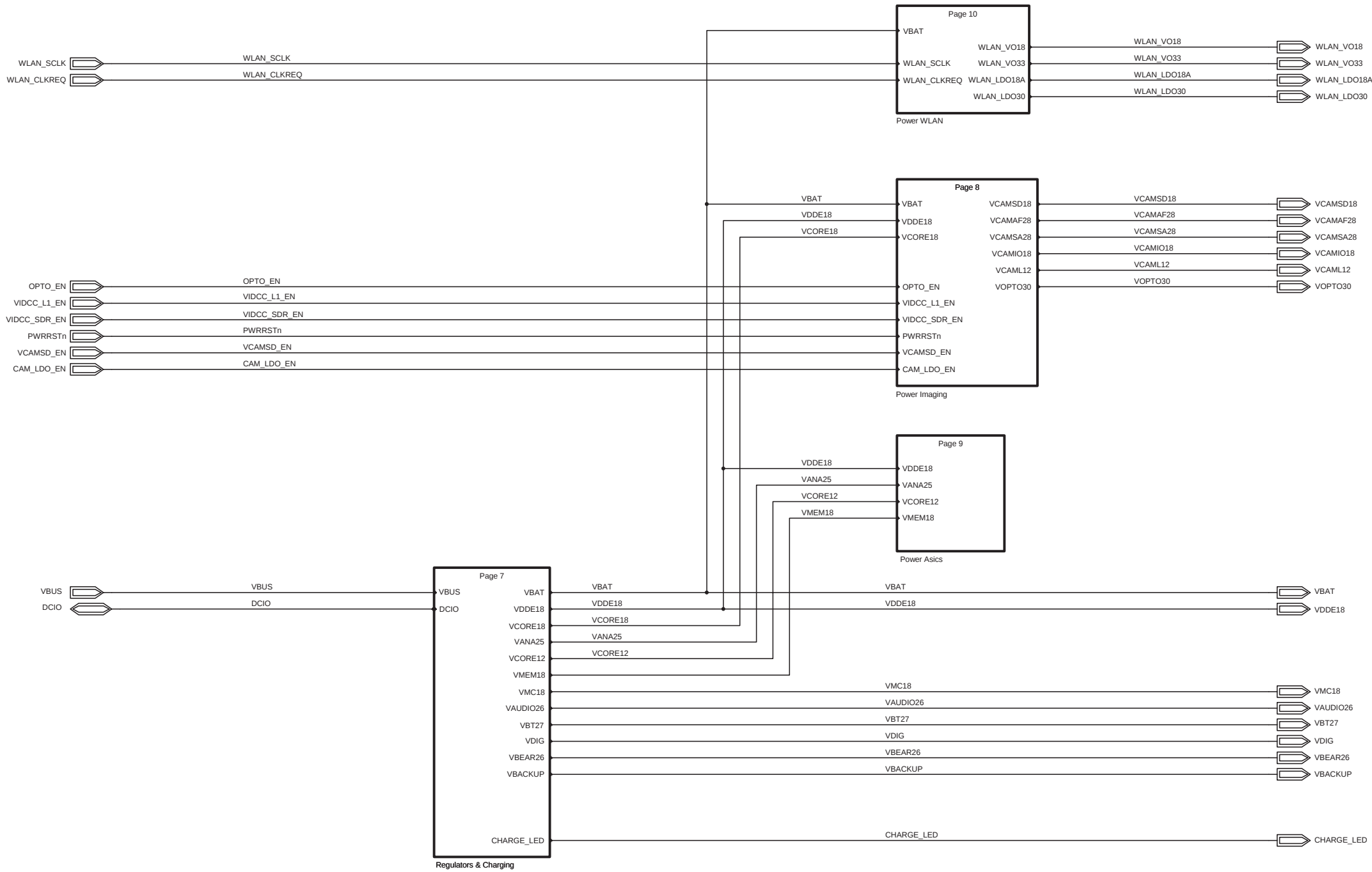


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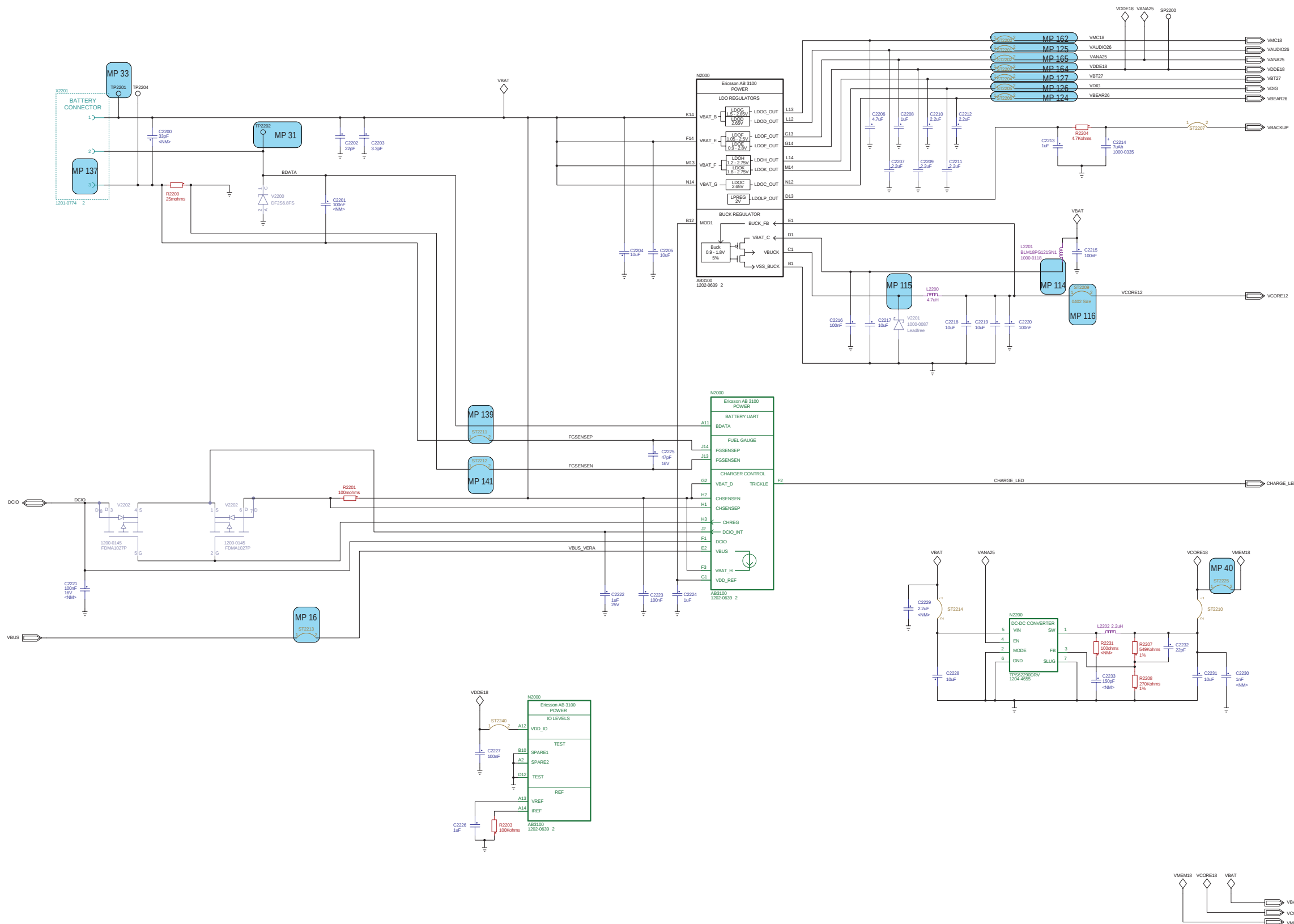




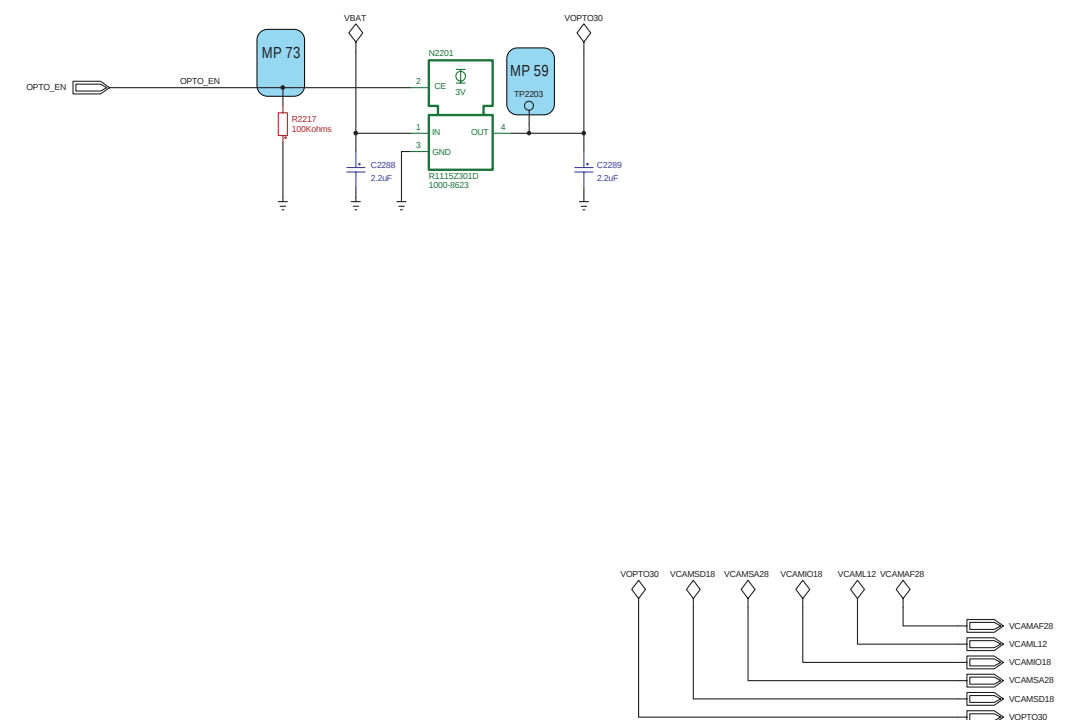
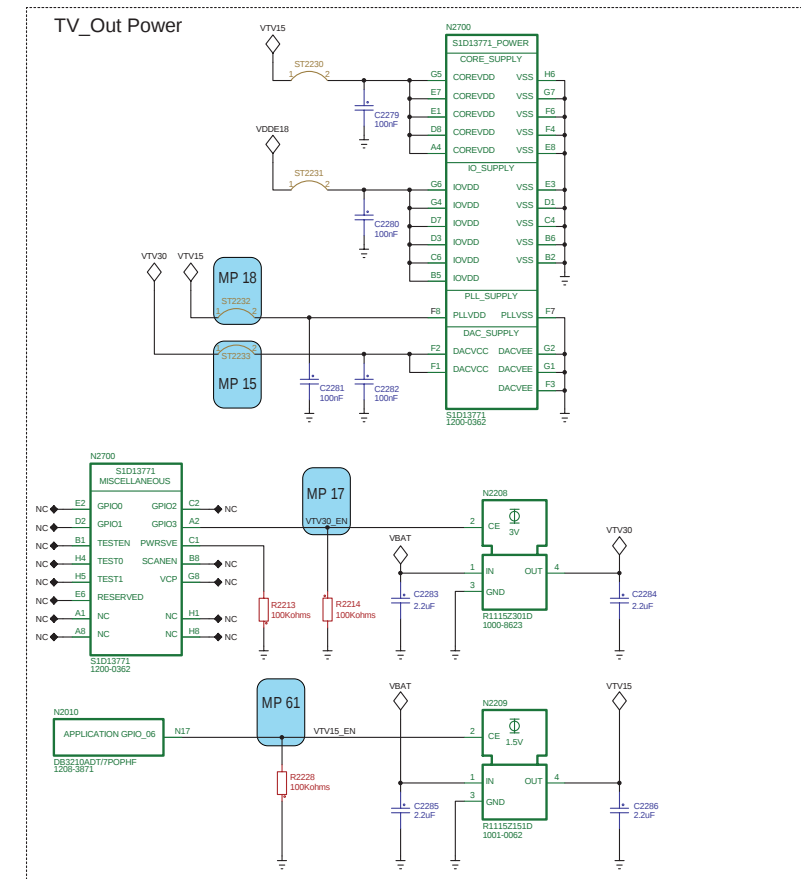
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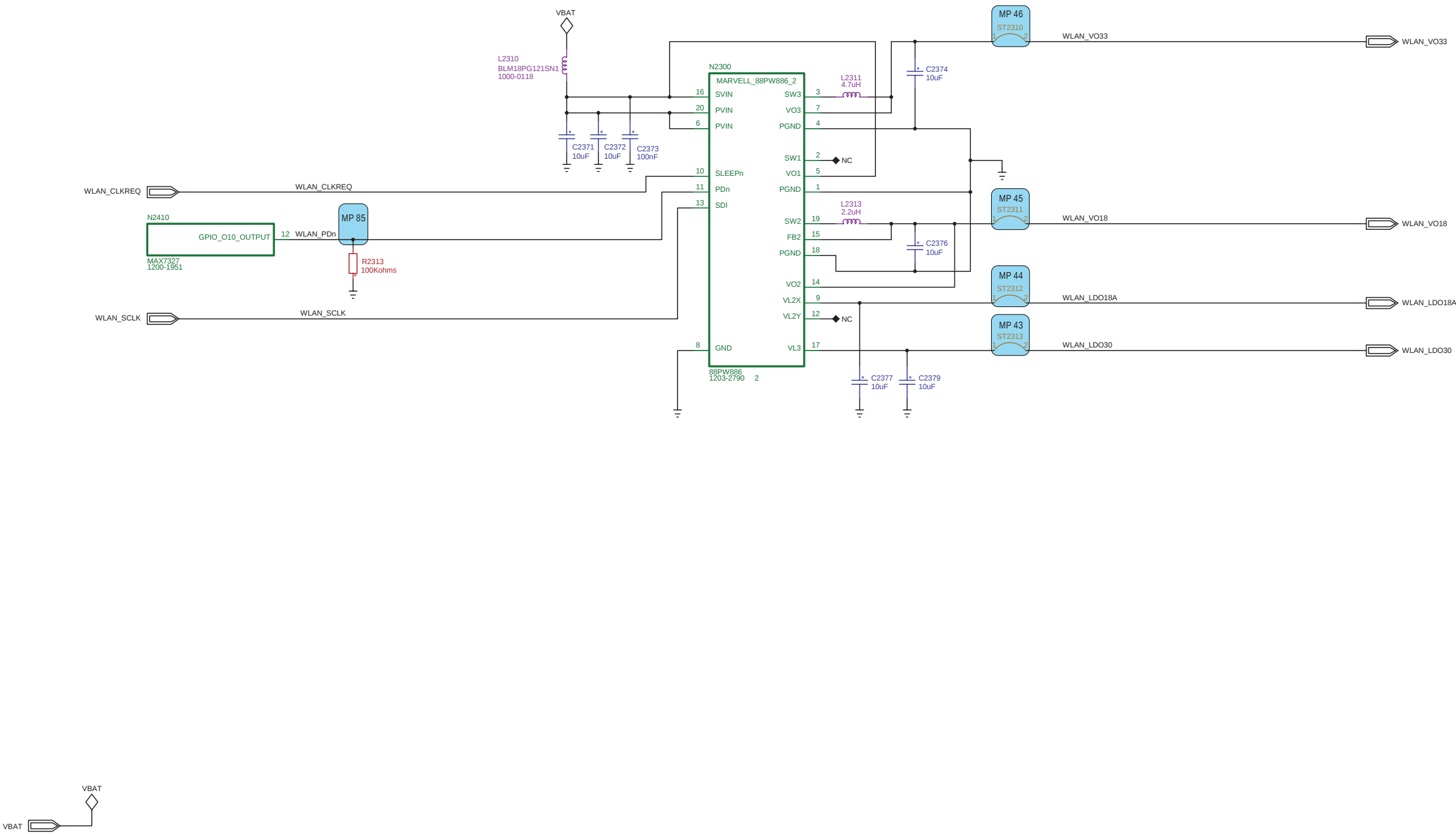


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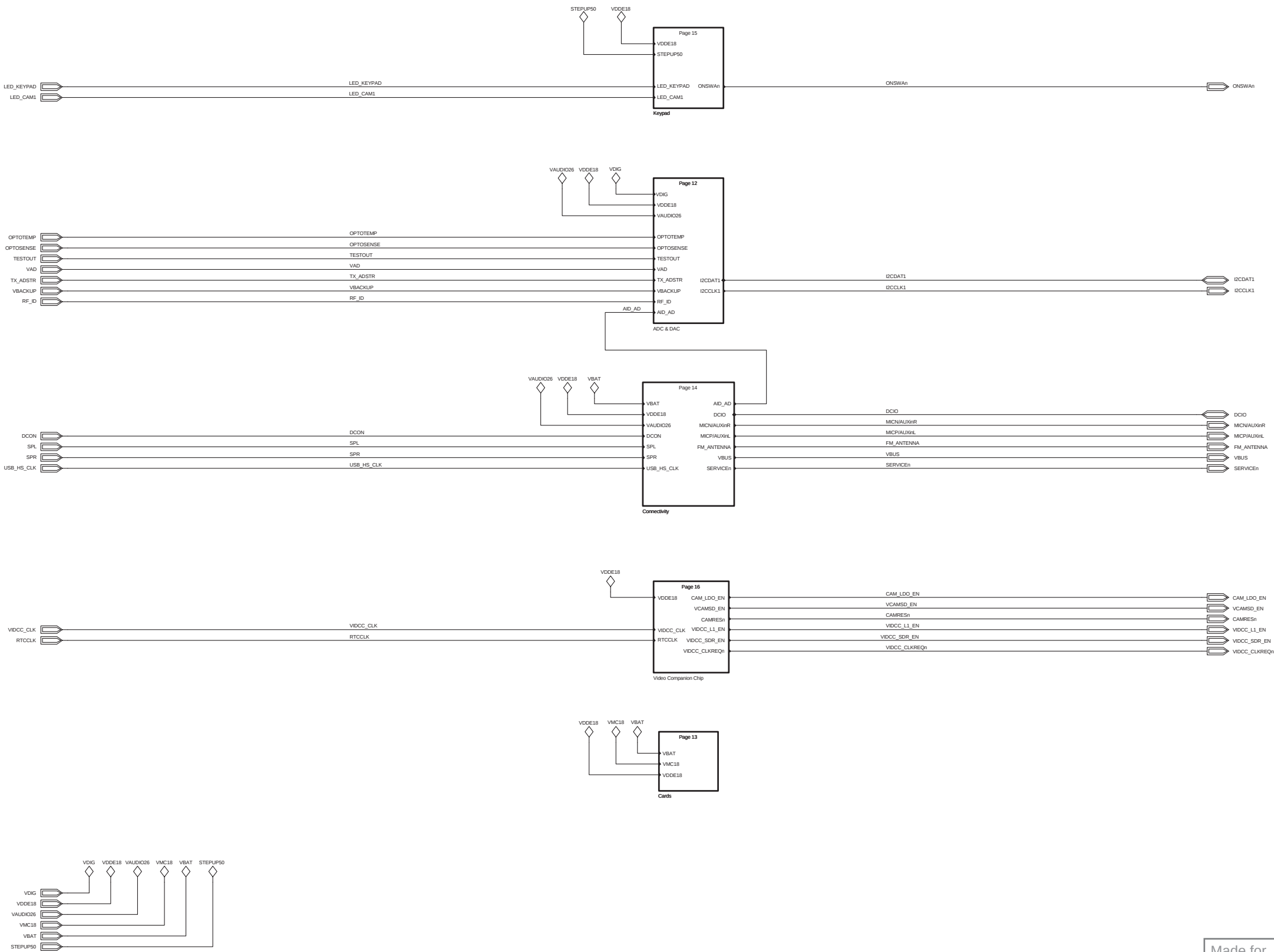


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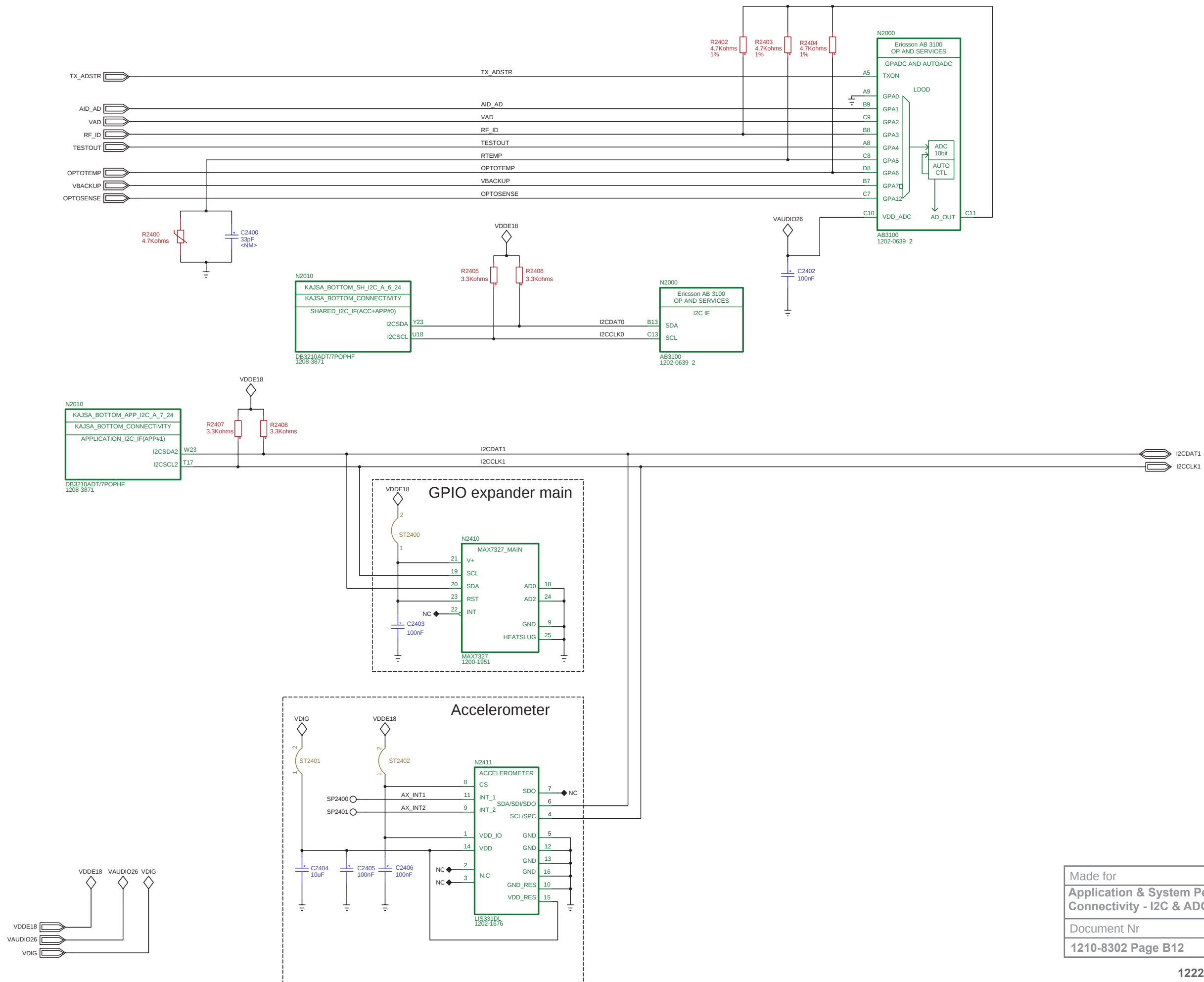




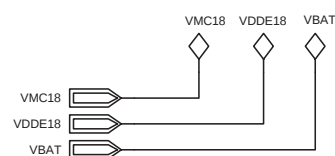
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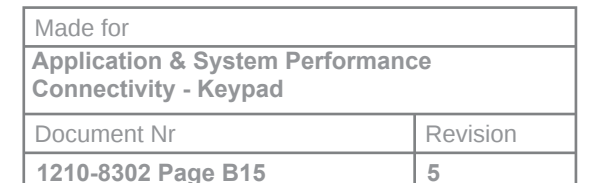
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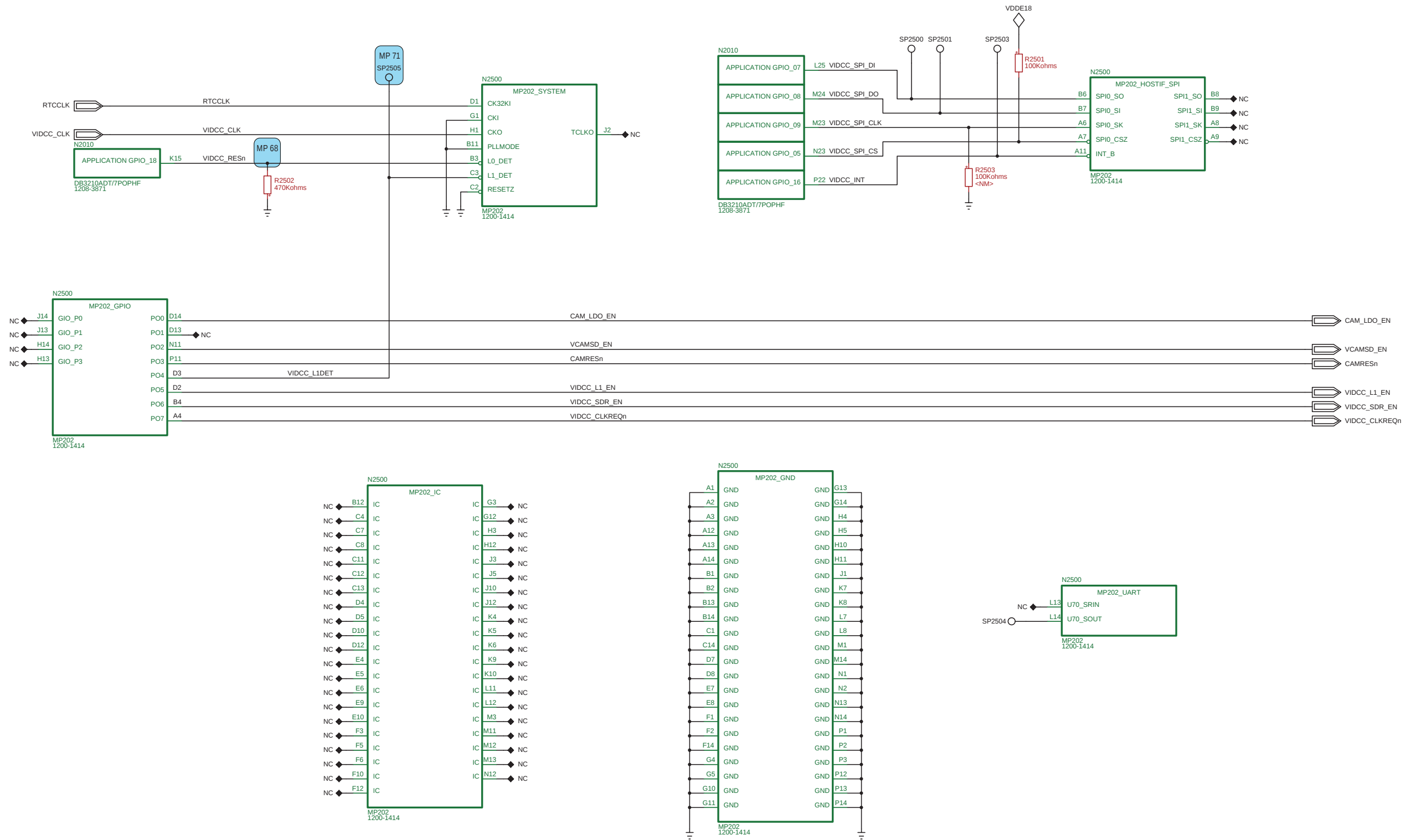


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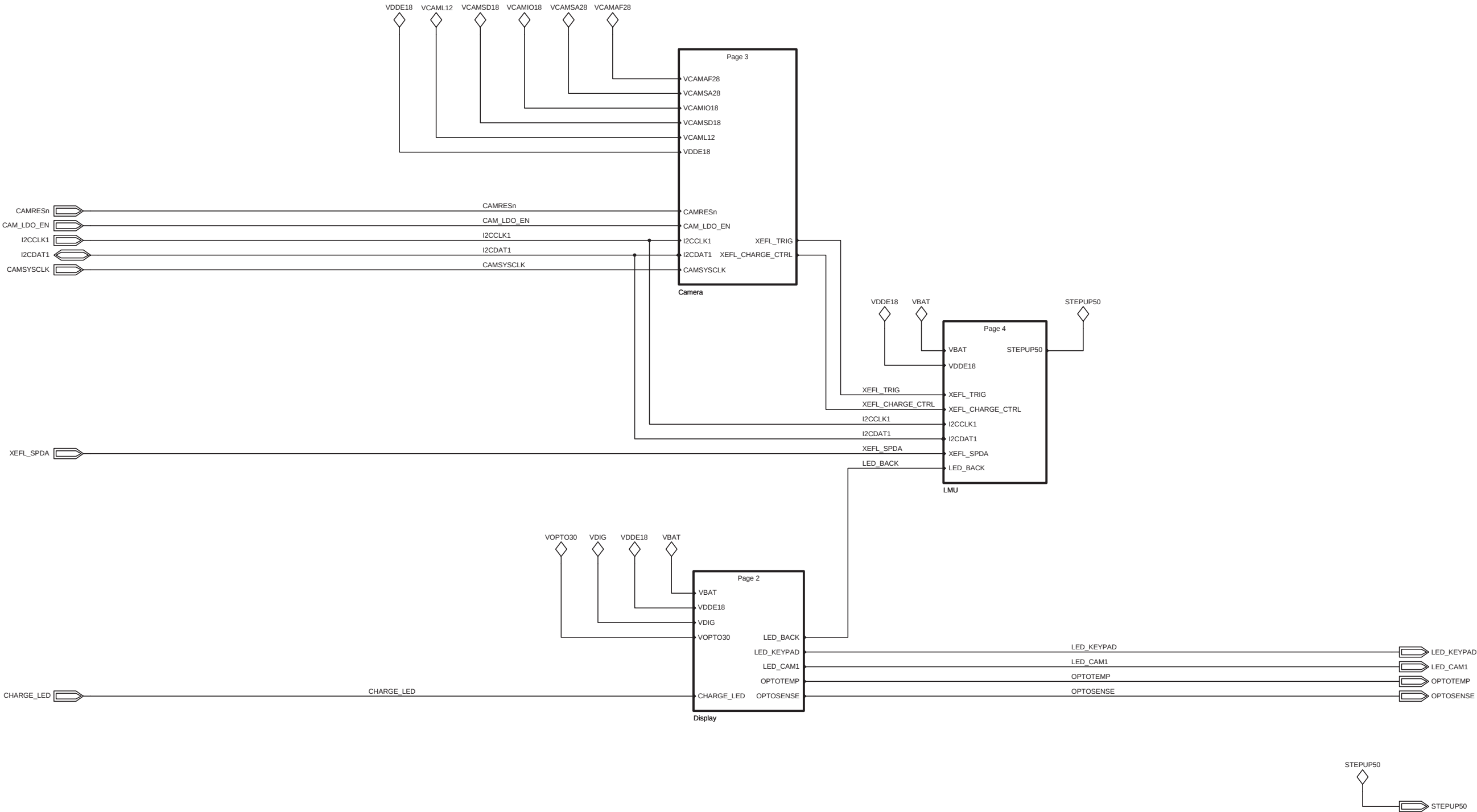
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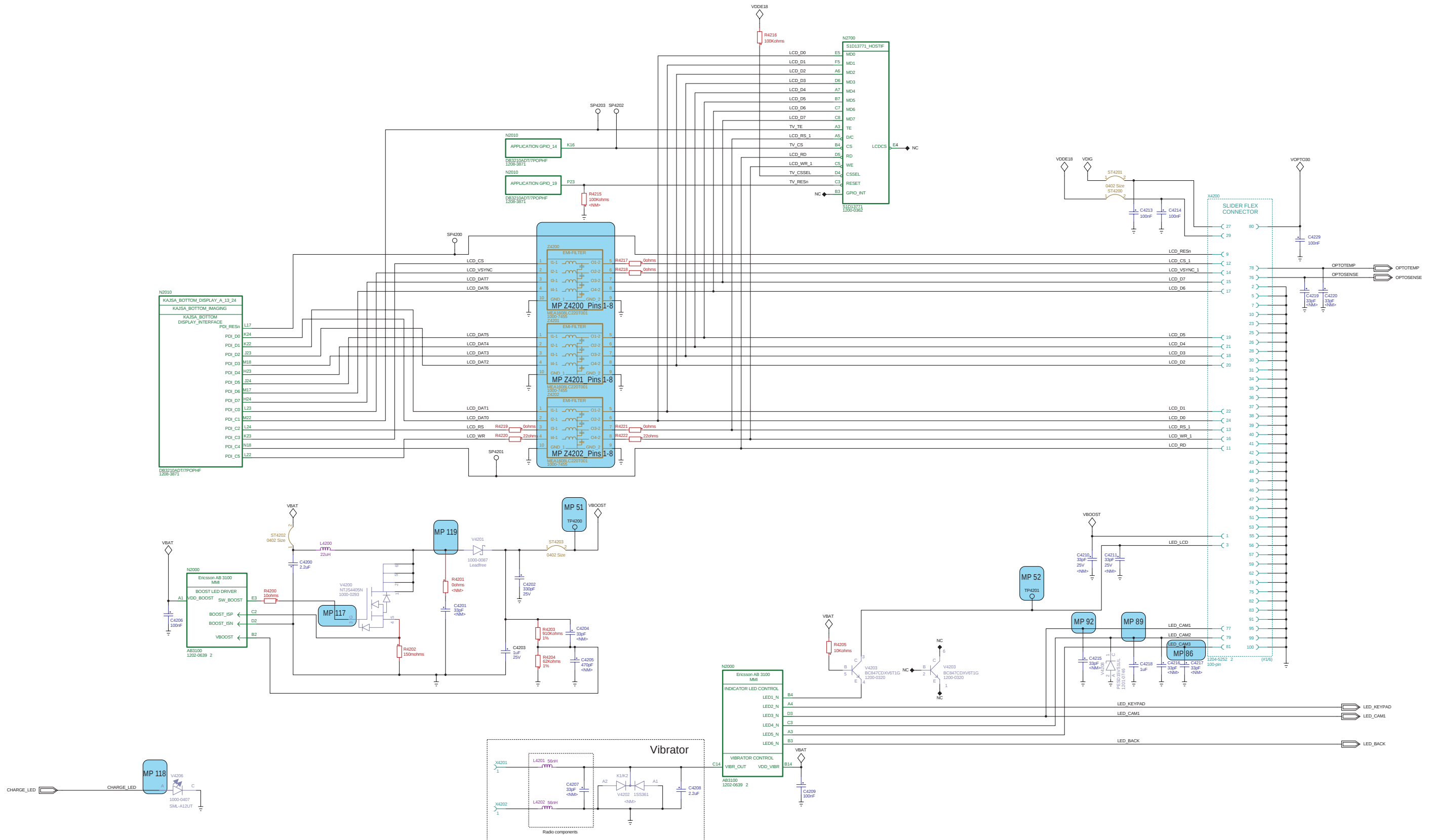


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**Application & System Performance
Connectivity - Video Companion Chip**

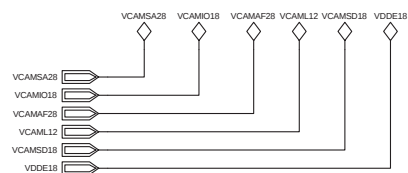
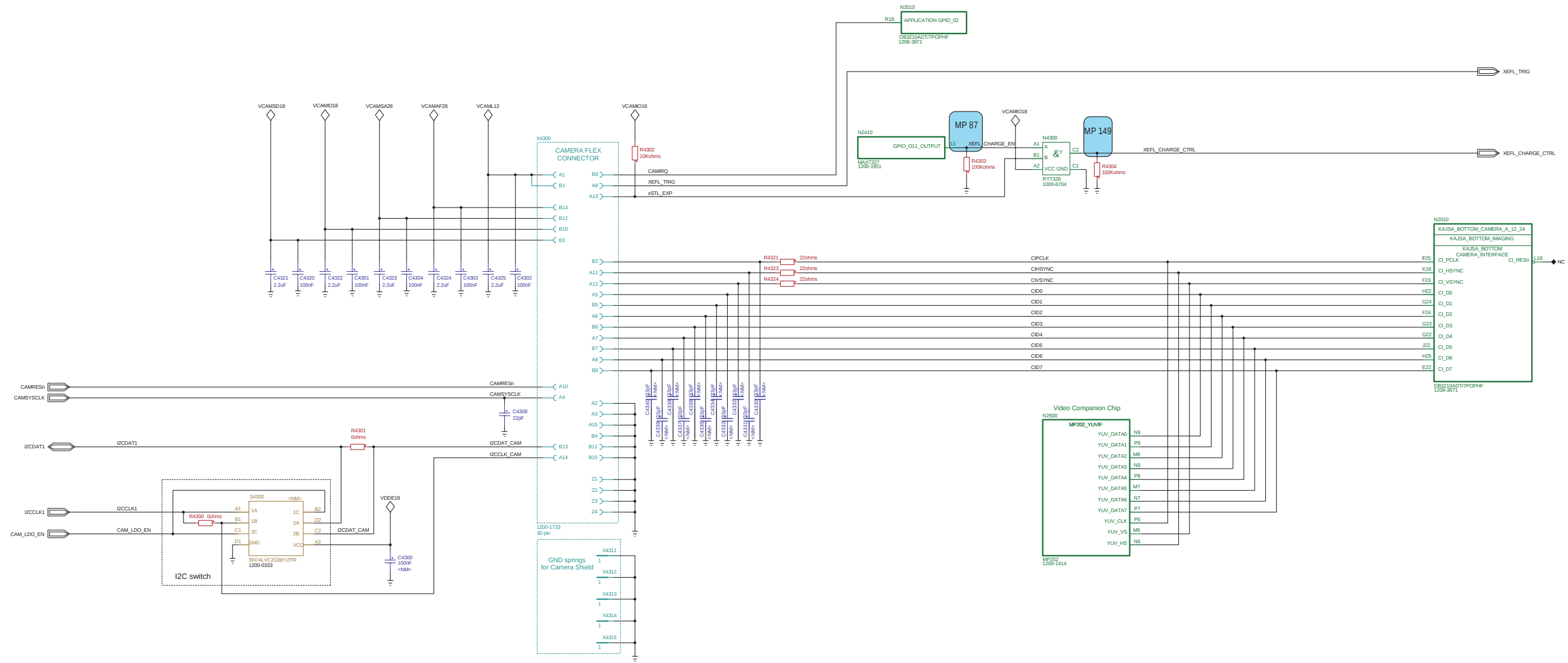
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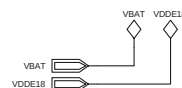
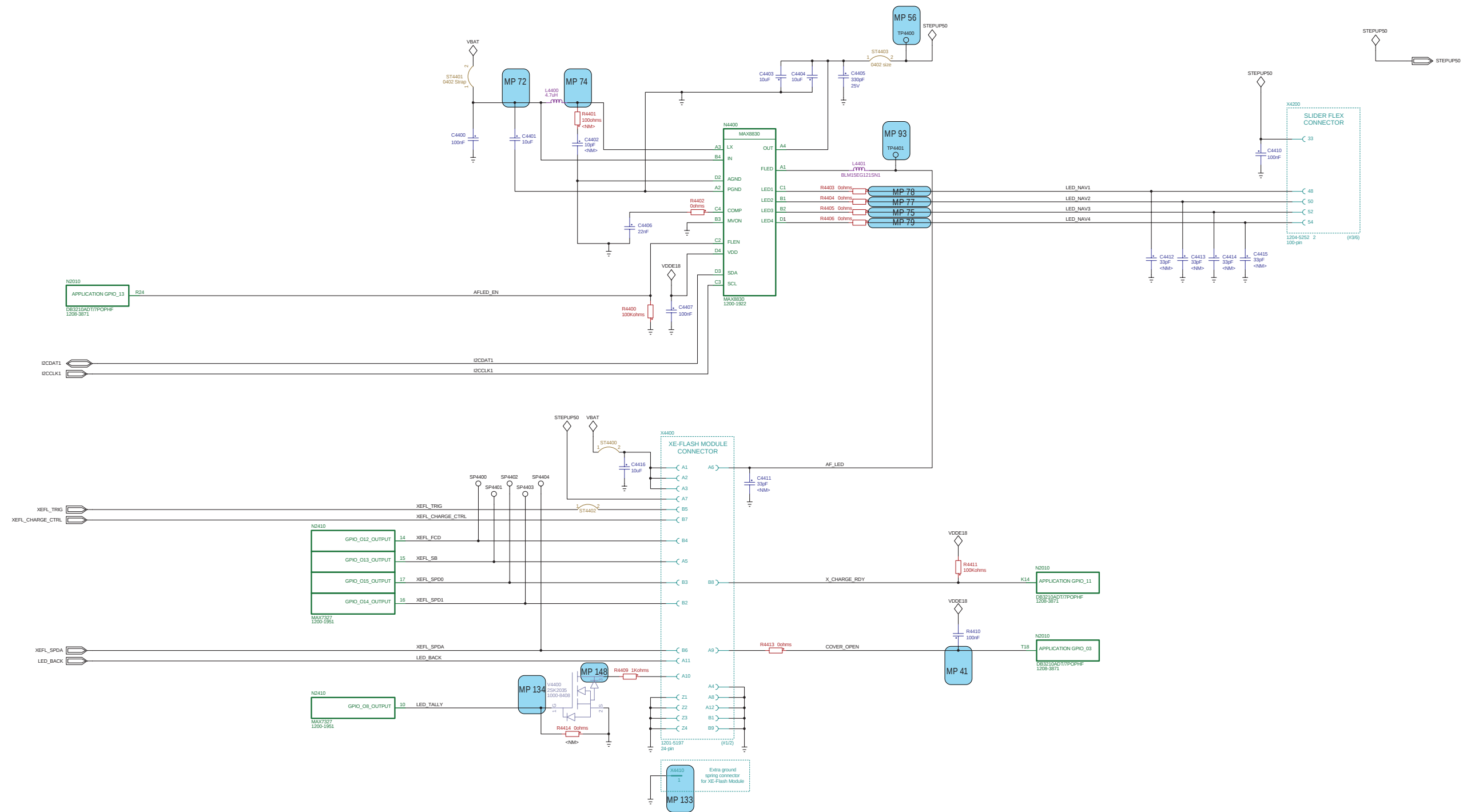
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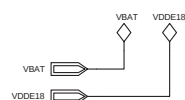
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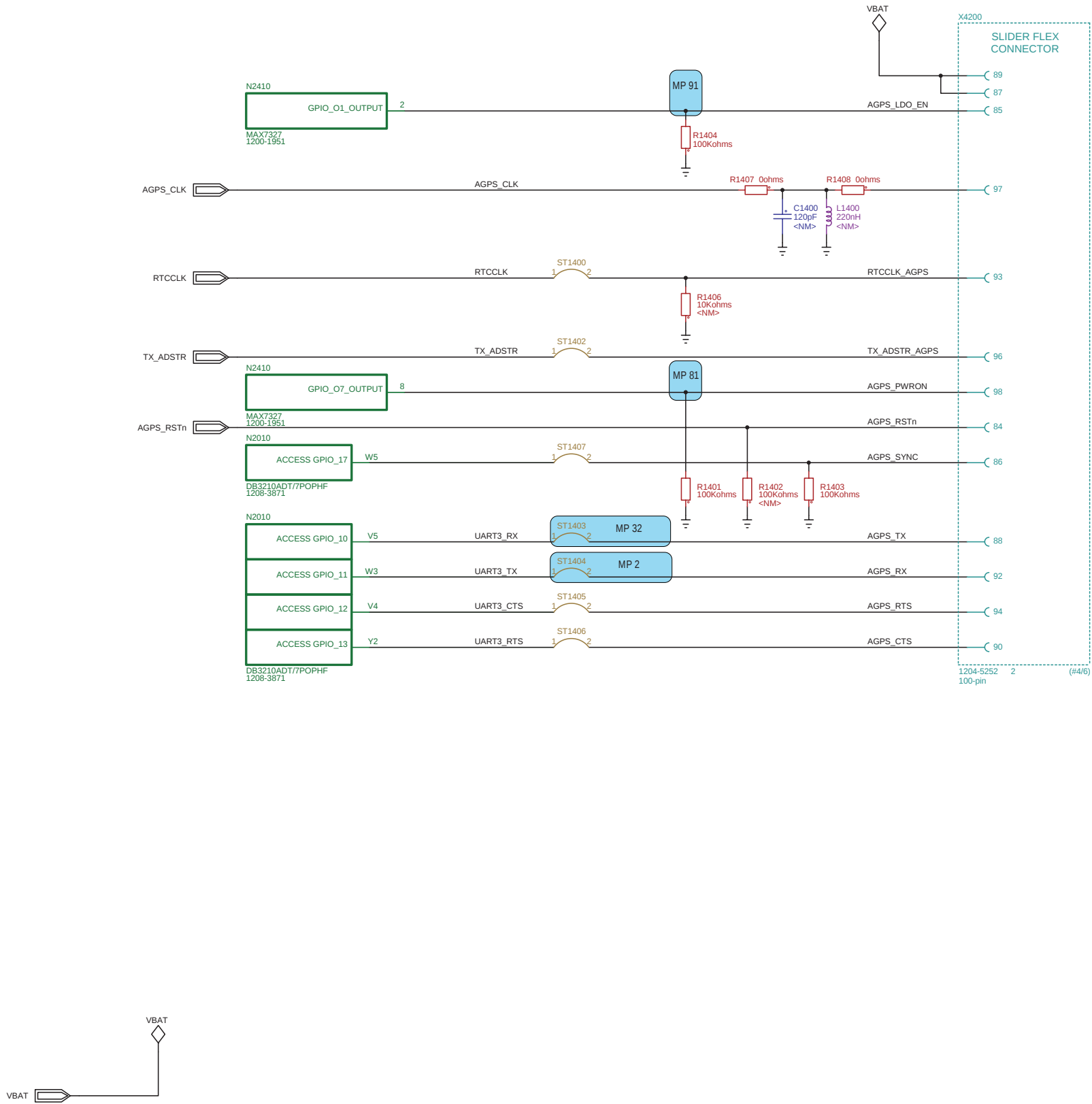
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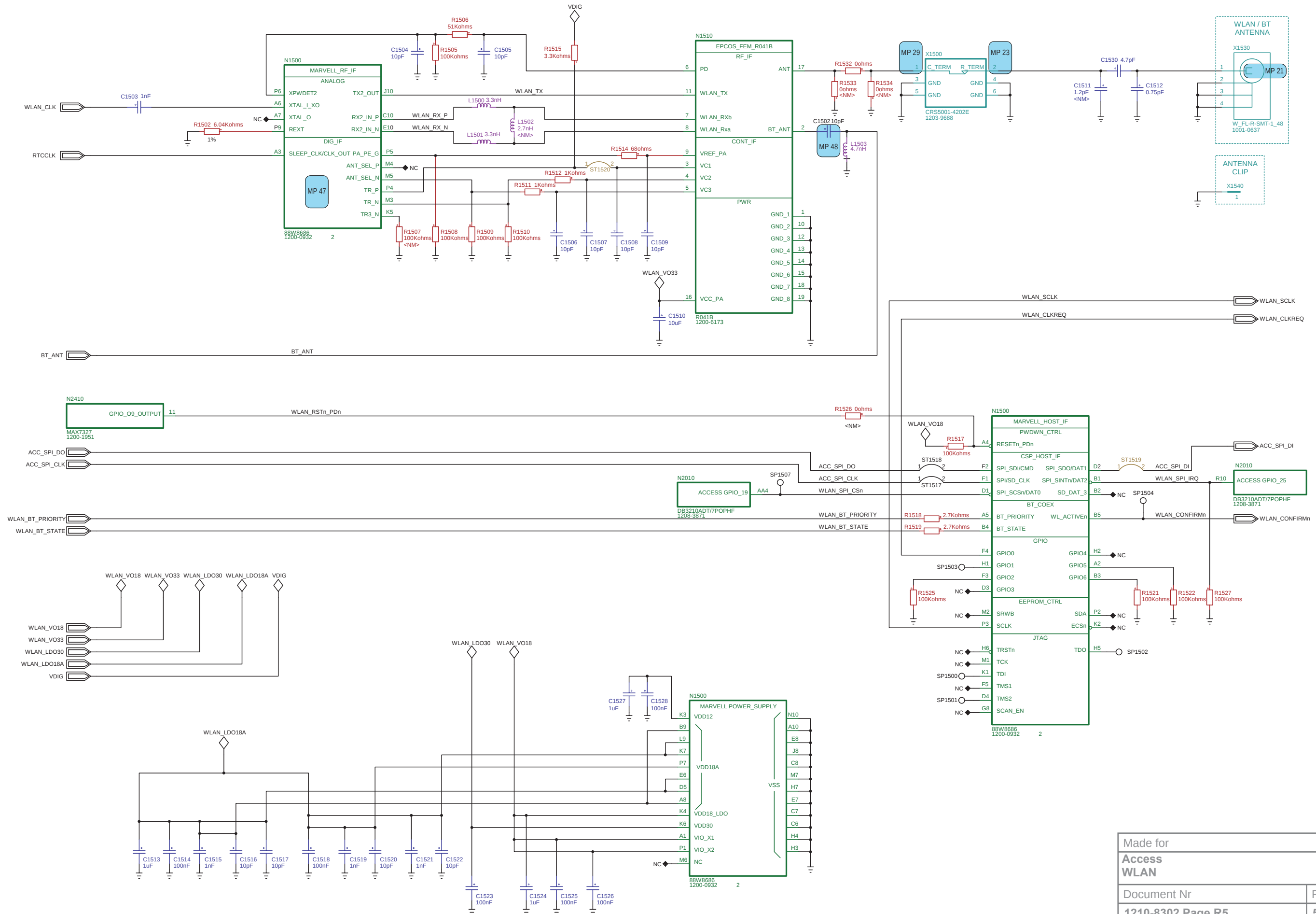




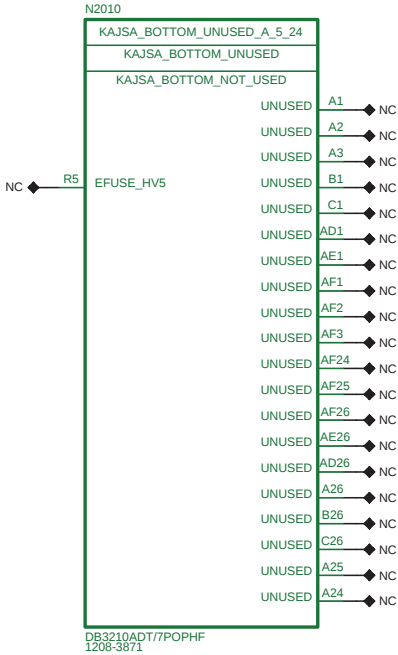
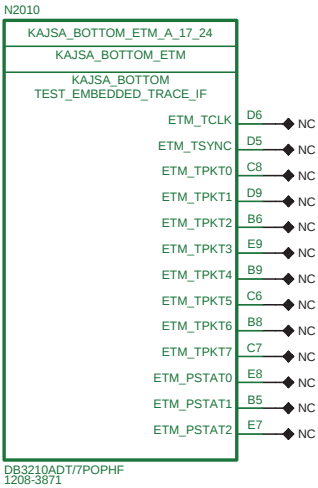
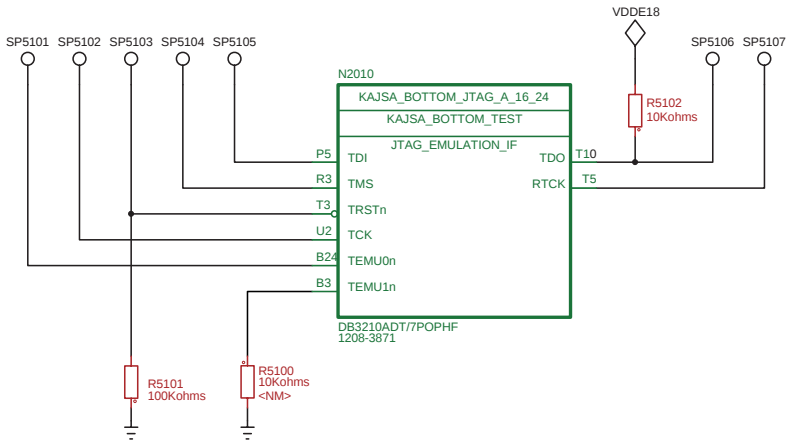
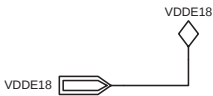
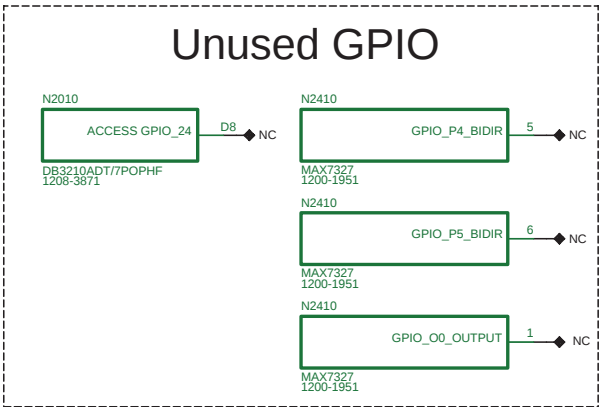




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R - Replaceable
See Appendix for
more information.



R - Replaceable
See Appendix for
more information.

C905 Function Overview



General Information

Size

104 X 49 X 18 mm

Weight

136 grams

Colors

Ice Silver
Copper Gold
Night Black

Screen

262,144 color TFT, Resolution 240 x 320 pixels, Size: 2.4 inches

Phone memory

Up to 160 MB
Memory Stick Micro™ (M2™) support

Talk time

GSM/GPRS: Up to 9 hrs
UMTS: Up to 4 hrs

Standby time

GSM/GPRS: Up to 380 hrs
UMTS: Up to 360 hrs

Networks

C905: GSM/GPRS/EDGE 850/900/1800/1900, UMTS/HSDPA 2100
C905a: GSM/GPRS/EDGE 850/900/1800/1900, UMTS/HSDPA 850/1900/2100
C905c: GSM/GPRS/EDGE 850/900/1800/1900

Features

Camera

8.1 megapixel camera
Up to 16x digital zoom
Auto focus, Face detection
Smart contrast
BestPic™, Photo fix
Photo feeds, x-Pict Story™
Xenon flash
Video light
Red-eye reduction
PictBridge printing
Image stabilizer
Video stabilizer
Picture blogging
Video blogging
Video recording

Music

Media player, Bluetooth™ stereo (A2DP), Album art,
Music tones (MP3/AAC), PlayNow™, TrackID™

Internet

Access NetFront™, Web browser, Web feeds

Communication

Video calling, Speaker phone, Polyphonic ringtones, Vibrating alert

Messaging

Email, Exchange ActiveSync®, Text messaging (SMS), Picture messaging (MMS),
Instant messaging, Predictive text input, Sound recorder

Design

Navigation key, Auto rotate, Picture wallpaper, Wallpaper animation

Entertainment

3D games, FM radio, Java, Video streaming, Video viewing

Organiser

Calendar, Phone book, Tasks, Notes, Alarm clock, Timer, Calculator, Stopwatch, Flight mode

Location-based services

aGPS, Pre-installed maps, Geo tagging of photos

Connectivity

DLNA Certified™, Bluetooth™ technology, Modem, Synchronization, USB mass storage,
USB, support, Wi-Fi™

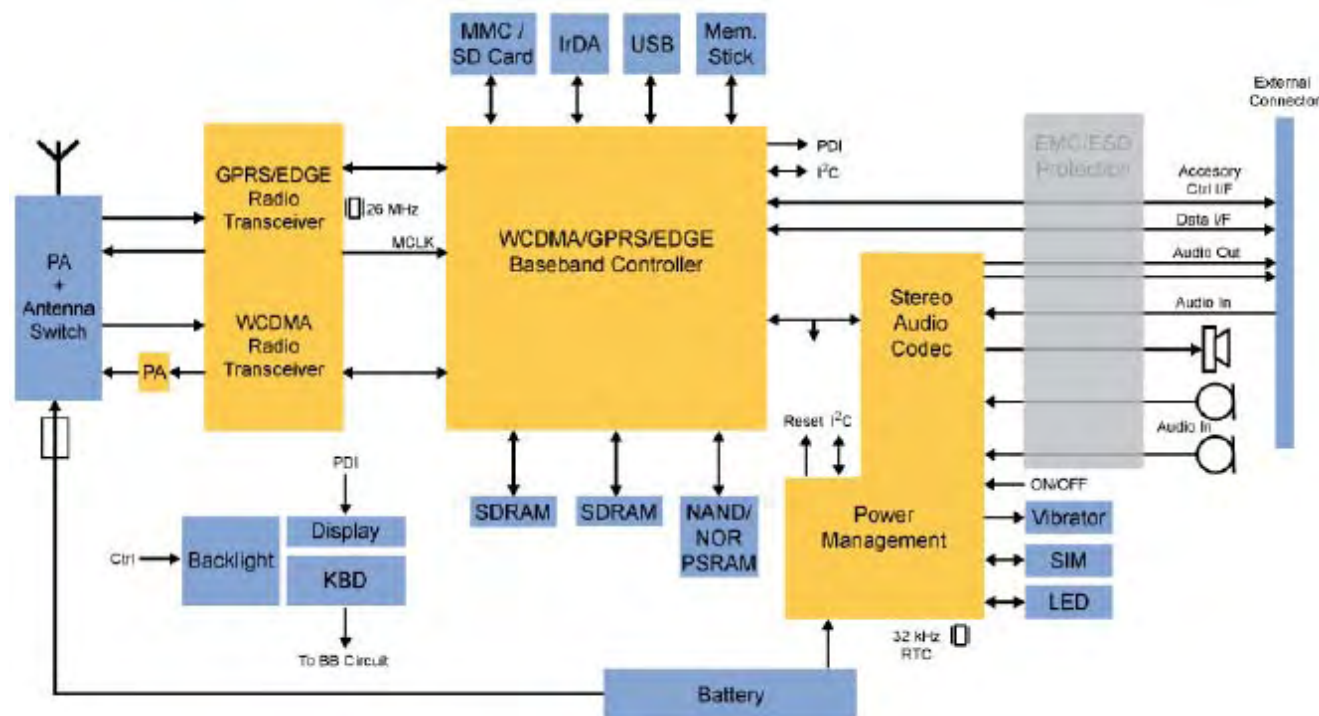
Note! *Wi-Fi (WLAN) is only supported by C905 and C905a.*

Hardware Overview

Platform Information

The C905 is using the U365 platform provided by Ericsson Mobile Platform (EMP)

U365 Platform Block Diagram:



Hardware Overview

Baseband Part

Analog Baseband Controller N2000 (Vera)

This component is not replaceable on SL 4 because Baseband calibration is required. The analog baseband controller is the main power management circuit. It has converters and regulators that generate a number of supply voltages, each optimized for its load.

The analog baseband controller is a mixed digital and analog device that supports the following circuitry:

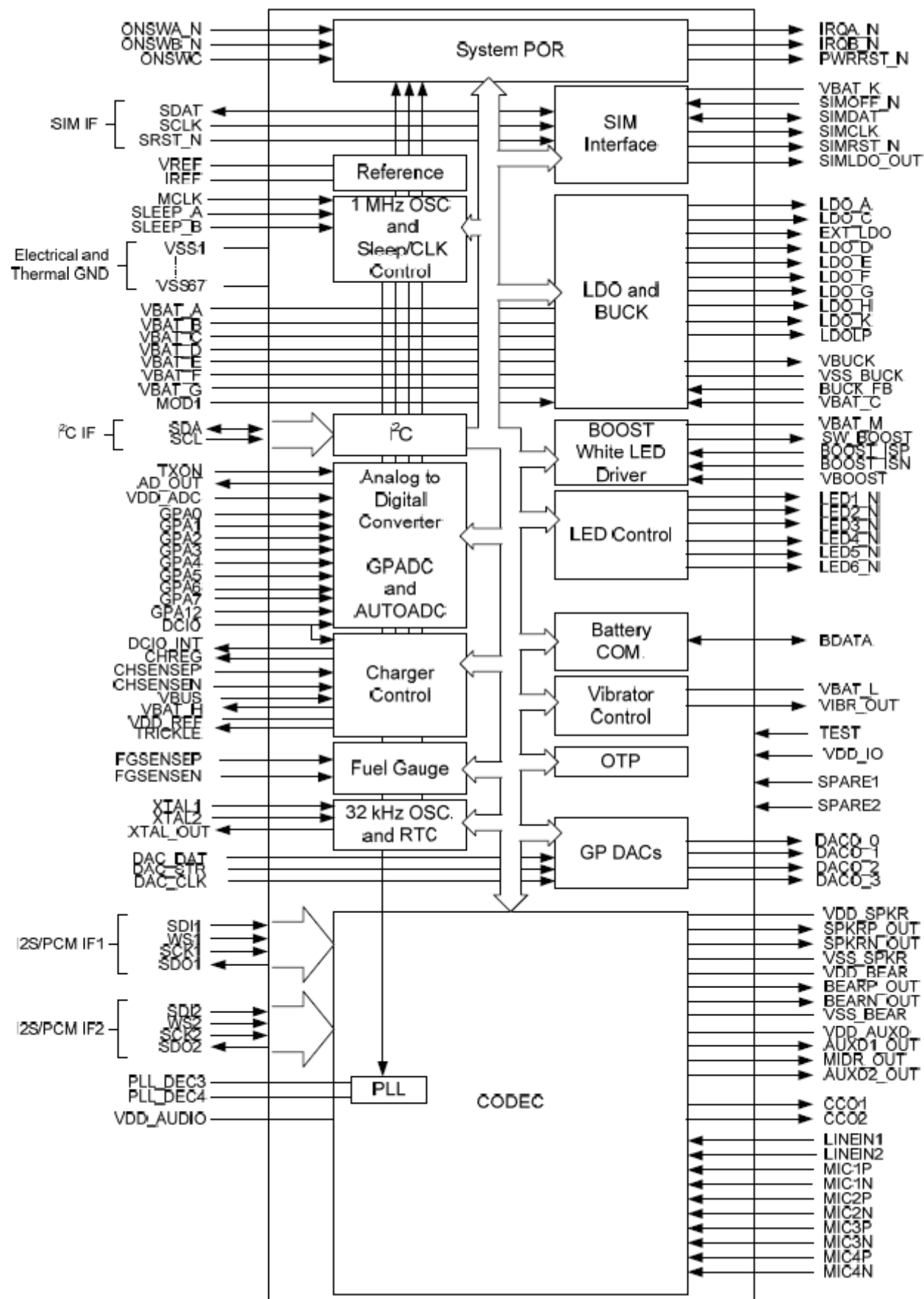
- Power management circuitry
- Voltage regulation circuitry
- Eight Low Dropout (LDO) regulators and low power regulator
- 600 mA integrated Buck regulator
- Boost step-up DC/DC converter for White Light Emitting Diode (WLED) driving
- Battery charging and communication circuitry
- Battery fuel gauging circuitry
- Analog-to-Digital Converter (ADC)
- Digital-to-Analog Converter (DAC)
- SIM interface
- Six programmable LED drivers
- Accurate band gap reference
- Vibrator driver
- Real Time Clock (RTC)
- 8-byte One-Time Programmable (OTP) memory
- Pulse Code Modulation (PCM) voice coder/decoder
- PCM audio coder/decoder
- Microphone interface
- Stereo line input
- Earphone driver
- Earpiece driver
- 8- Ω speaker driver / Stereo line output

The analog baseband controller is controlled by an I2C™ interface. It also comprises the main power management circuits, equipped with a number of converters and regulators for generating the required supply voltages.

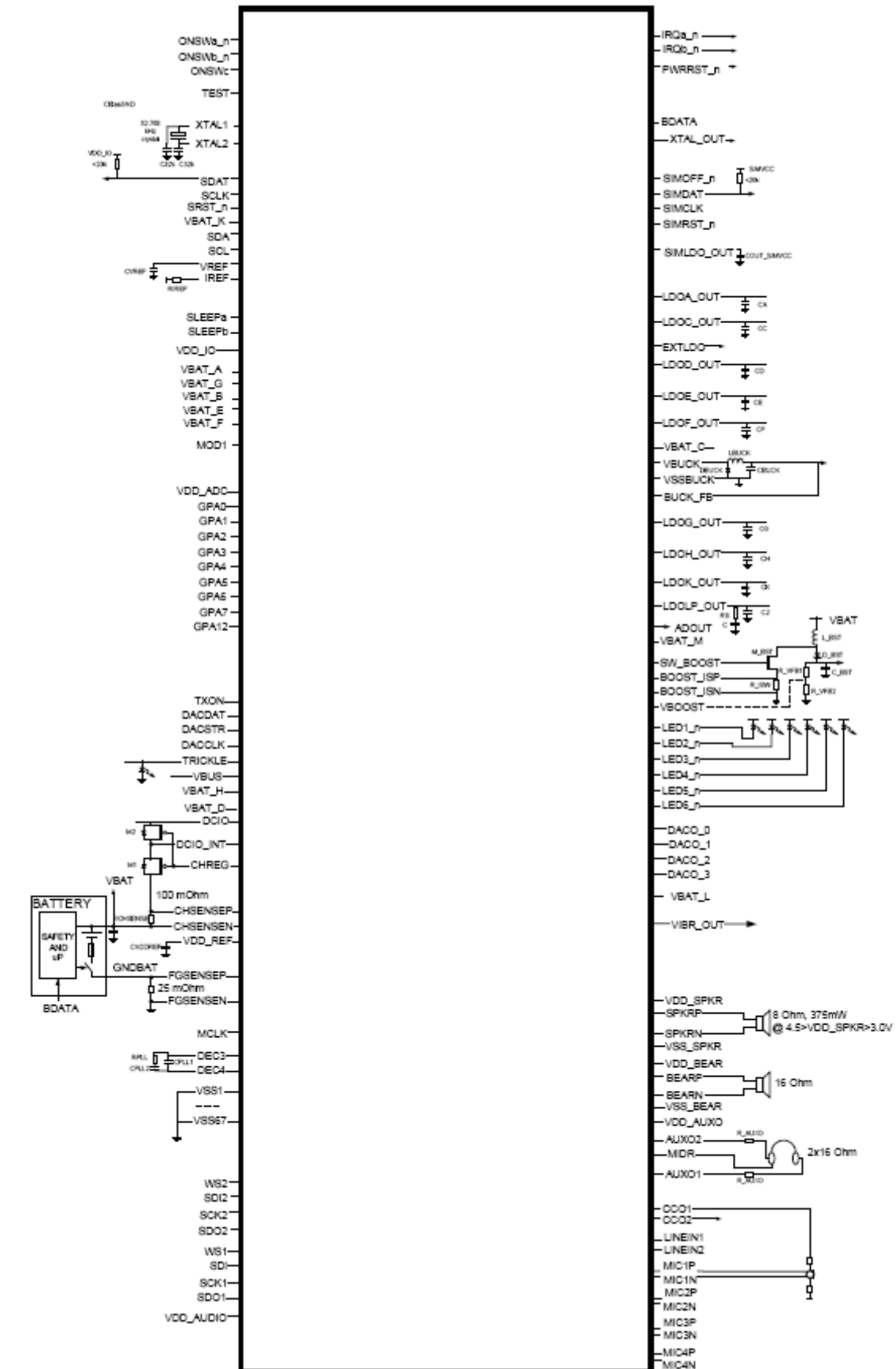
The analog baseband controller supports the following features:

- Lithium battery
- Full audio CODEC functionality
- Supports stereo audio sampling rates of 8/16 kHz voice coding/decoding and 44.1/48 kHz for high quality audio recording/playback (for example MIDI and MP3 applications)
- Double CODEC I2S/PCM interfaces
- Flexible microphone interface
- Integrated headphone amplifiers
- Integrated earpiece amplifiers
- Integrated speaker amplifier
- Integrated flexible audio mixing functionality
- Boost driver capable of driving up to four WLEDs in series, supplying 50 mA
- Designed to meet power management demands of GSM and WCDMA
- Automated power management ADC to relieve CPU
- Battery identification and communication
- Single-terminal charger and accessory power interface for compact connector design
- Integrated USB charging
- OTP memory
- Integrated hardware fuel gauge to accurately monitor battery capacity
- Reduced number of external components as a result of integrated programmable LED and vibrator drivers
- 32 kHz real time clock with alarm wake up capability
- Designed to support two host controllers.

Functional Blocks of the Analog Baseband Controller:



Connection Diagram:



Charger Control

A programmable charger is used for battery charging. Limits can be set for the output voltage at CHSENSE- and the output current from DCIO through the sense resistor to CHSENSE-. The programmable charger is enabled or disabled by the assertion/negation of the external signal DCIO. Parts of the programmable charger are activated and deactivated depending on the level of VBAT. The rest of the programmable charger is activated and deactivated through I2C.

The programmable charger supports the following functions:

- Constant current charging
- Constant voltage charging
- Trickle charging
- PWM controlled charging
- Over-voltage and over current detection
- Watchdog termination
- DCIO assertion/removal detection
- Voltage and current measure functions
- Low resistive path (reverse mode)

The programmable charger is able to control the voltage and limit the current to a load seen at CHSENSE-. The programmable charger can also be run in PWM mode to turn the charging on and off in accordance with the particular period and duty cycle. When the charging is on, it is set to the current and voltage selected by I2C.

A low resistive path from VBAT to DCIO can be formed when DCIO is not detected. When this setting is done in the appropriate registers, a lowering of CHREG to 0 V turns on the external pass device. The pass device is automatically turned off when an external source is detected on DCIO, or when the watchdog termination block times out. The watchdog termination block must be active when the external switch is enabled, both in normal charging mode and in the low resistive path mode. The watchdog is set through the serial interface, and if it has not been set again before timeout, the watchdog turns off the external switch. The watchdog is disregarded during trickle charging. When no battery is present, the system can be booted and supplied from DCIO by applying the correct voltage on DCIO.

USB Charger

The analog baseband controller contains a standalone USB charger. The USB charger has a separate input and incorporates full functionality during low VBAT.

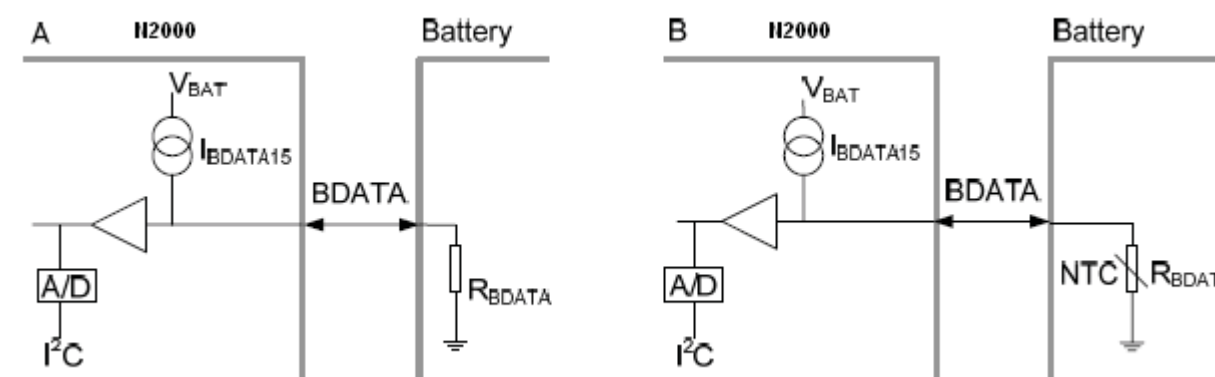
The programmable charger supports the following functions:

- Trickle charging
- Constant current charging
- Watchdog termination
- Trickle LED indication
- VBUS assertion/removal detection

Resistance Identification and Temperature Measurement

The resistance identification mode utilizes the constant current source to feed the battery data output while monitoring the voltage at the battery data node with general purpose ADC the conversion is started through I2C.

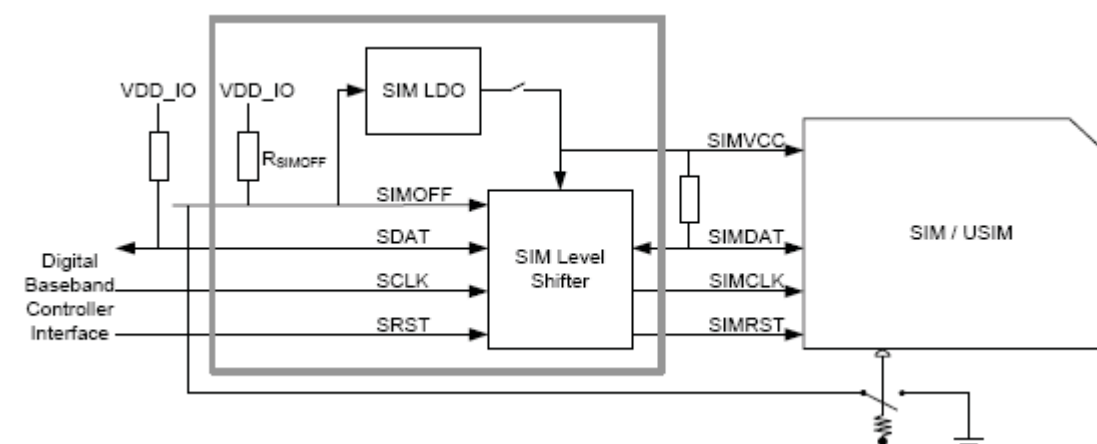
Resistance Identification (A) and Temperature Measurement (B):



SIM Interface

The SIM interface supplies level is shifting between the digital baseband controller and the SIM/USIM card. Moreover, hard-wired SIM deactivation functionality manages removal of a SIM card that has not been powered down.

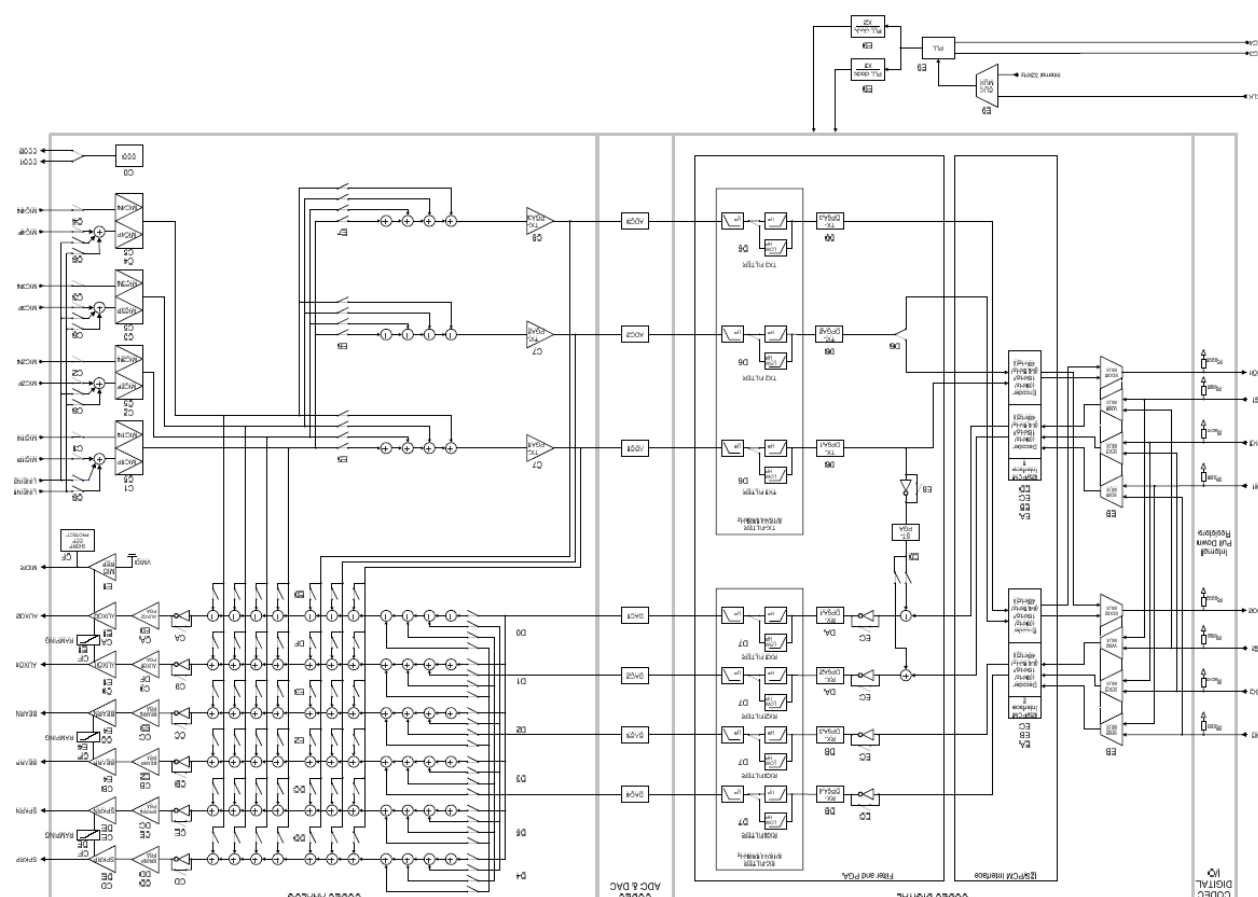
Block Diagram of the SIM Interface:



CODEC Overview

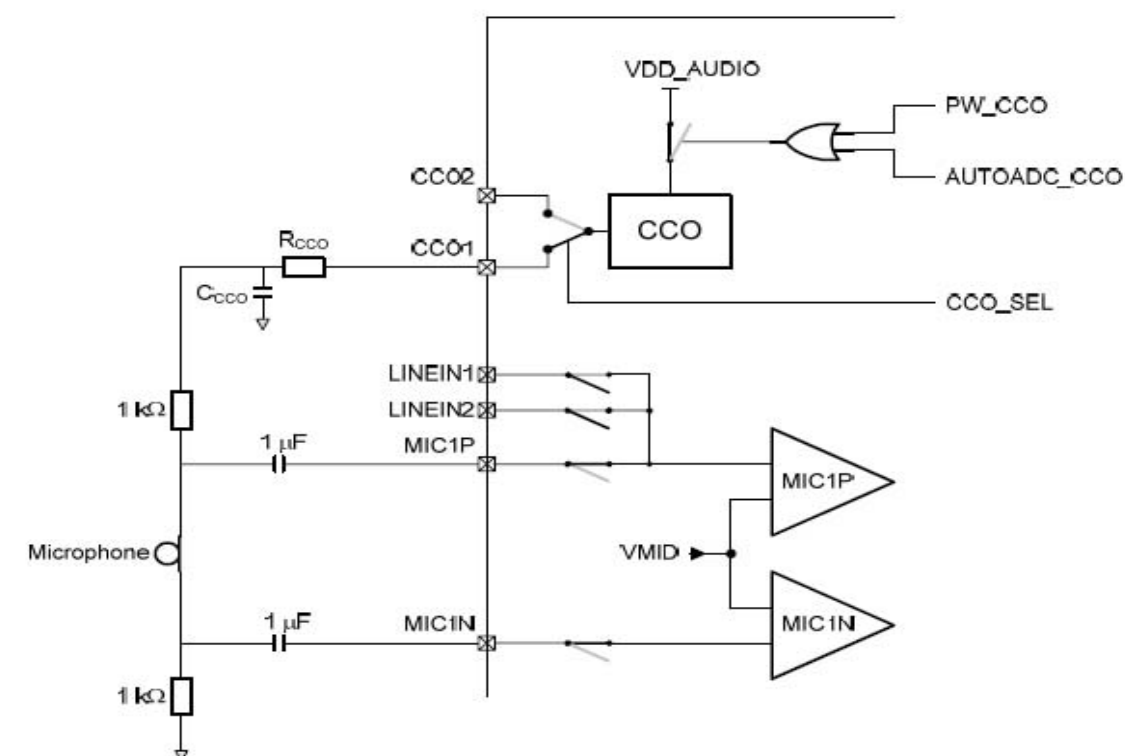
The CODEC is encoding analog audio signals and analog voice signals into digital signals using Analog to Digital converters (ADCs). This is done in the coder section of the CODEC, also named the TX path (transfer section). The CODEC is also decoding digital audio signals and digital voice signals into analog signals using DACs. This is done in the decoder section of the CODEC, also named the RX path (receiver section).

CODEC Block Schematic:



CODEC CCO Voltage Source

There is an internal voltage source CCO that provides the necessary drive current for electret microphones. The voltage source is I²C programmable to 2.2 V or 2.4 V. The source can be disabled during standby. A typical use case with a microphone connected to MIC1 and the CCO is shown in picture below.



Earphone Amplifier

The earphone amplifiers (BEARP and BEARN) are mainly intended to be differentially configured and drive a low impedance dynamic transducer (earpiece) but they can also be single ended configured. The BEARP and BEARN amplifiers can be powered down by the I2C. The amplifiers can exhibit high impedance to 1.4V or low impedance to ground when powered-down. Fifty-one gains are available for BEARP and BEARN: from +15dB down to -60dB in 1.5dB steps. When the BEARP and BEARN outputs are operating in differential mode, an I²C selectable bit must invert one of the inputs.

Speaker Amplifier

The speaker amplifiers, SPKRP and SPKRN, are intended to drive a low impedance (8Ω) speaker in a differential mode or to be used as a stereo configured line output amplifier supporting external high power amplifiers. The output buffer shall exhibit low impedance to ground when powered-down and the current consumption shall be minimal. When the SPKRP and SPKRN outputs are operating in differential mode, an I²C selectable bit must invert one of the inputs.

Digital Baseband Controller (CPU) N2010 (Kajsa)

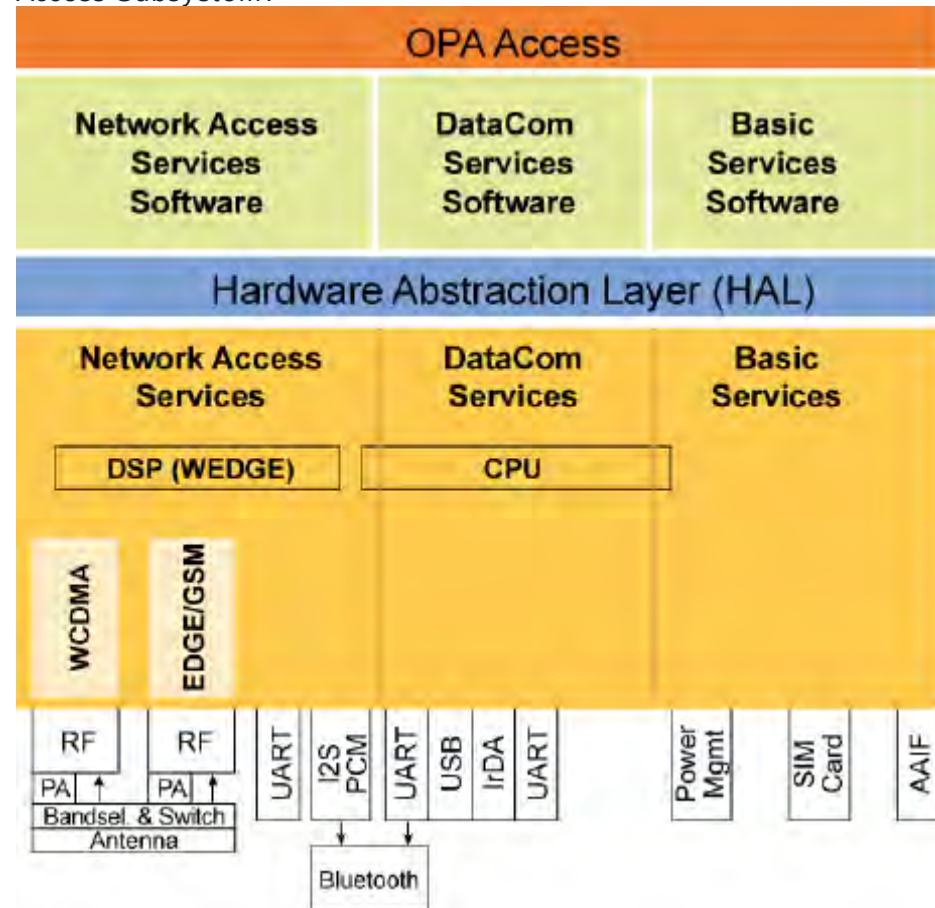
This component is not replaceable on SL 4 because Baseband calibration is required.
The Digital Baseband Controller is divided in two subsystems: Access and Application

Access Subsystem

All modem functionality in the digital baseband controller resides in the Access subsystem. This includes EDGE/GPRS/GSM interface, WCDMA interface, USB, IrDA, and other peripheral modules. The control CPU is an ARM926 and a DSP is used for signal processing and layer one control code.

The main communication between the blocks in the Access subsystem is done through the Advanced High-performance Bus (AHB) matrix, which is a set of control buses connecting the different parts together. A block called Syscon is responsible for distributing clocks and resets to all parts of the Access subsystem. This block is under SW control. The Access subsystem is connected to the Shared EMIF, an interface for communication with an external SDRAM. The Shared EMIF is shared between the Access subsystem and the Application subsystem.

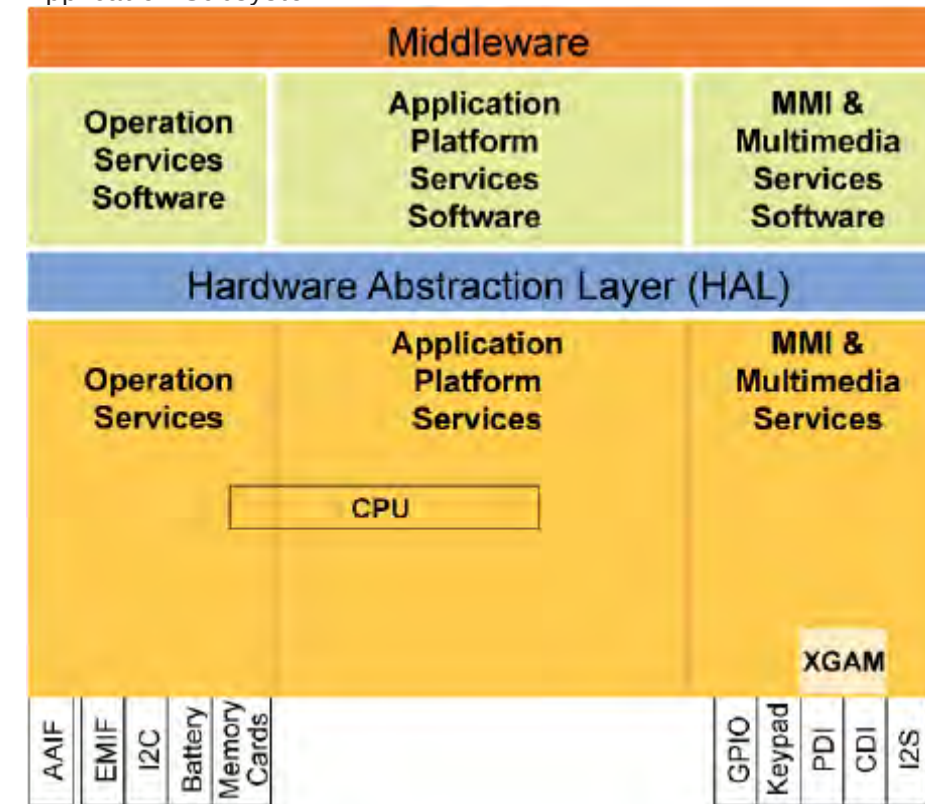
Access Subsystem:



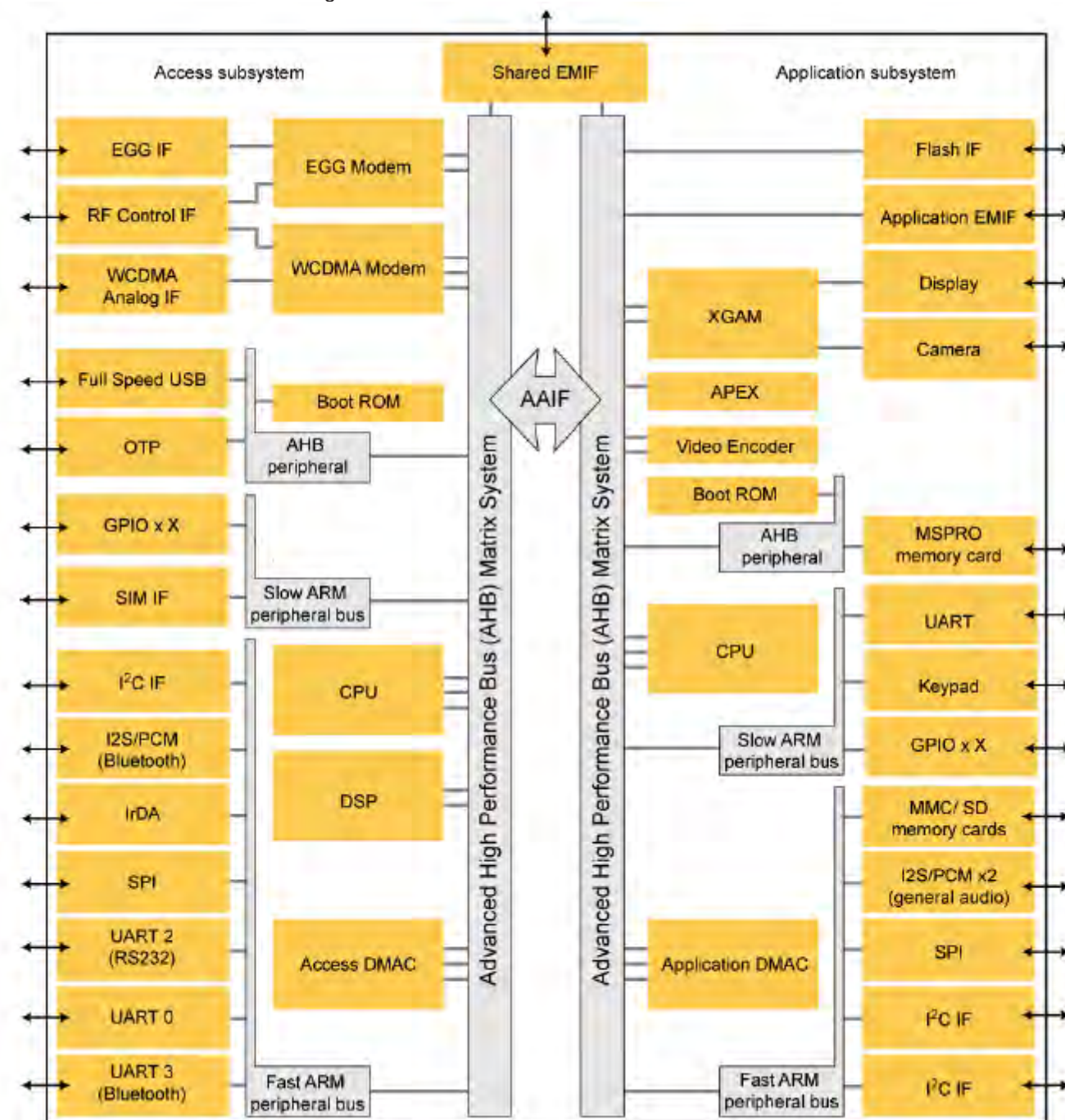
Application Subsystem

The Application subsystem contains functionality related to functions such as MMI, graphics, audio and memory media. The control CPU is an ARM926 with three external memory interfaces, one shared with the Access subsystem and two dedicated for the Application subsystem. The Application subsystem contains several blocks. The main communication between the blocks is done through the Advanced High performance bus (AHB) matrix, which is a set of control buses connecting the different parts. A block called Syscon is responsible for distributing clocks and resets to all parts of the Application subsystem. This block is under SW control. The Application subsystem is connected to the Shared EMIF that is used for code execution or data storage. In addition, a dedicated EMIF that support SDRAM or static memory like NOR, PsRAM or NAND are also available. The Application EMIF is a general interface for communication with, for example external SDRAM, PSRAM, NOR flash, NAND flash and companion chips

Application Subsystem:



The functional blocks of the digital baseband controller:



Keypad

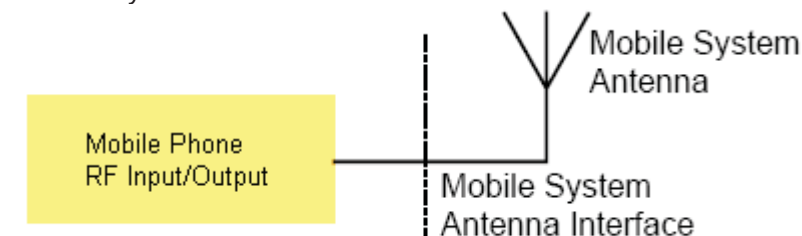
The keypad interface block supports up to 30 keys with 65 columns and 6 rows and operates in both scan and idle mode. The keypad scan is performed by software. Any transition in the state of the column inputs is written directly to the register. The keypad interface differentiates between single key presses, simultaneous presses of any keys with a function key, and any key releases. The period between successive scans is programmable over the range 5 ms to 80 ms, in 5 ms steps. During scan mode, the keypad generates an interrupt whenever a valid keypad state change occurs (including a release of any pressed keys). The scan function is disabled during system power-up. The keypad is able to detect at least four simultaneous key presses. Not all combinations are supported.

Radio Part

Antenna

The mobile system antenna interface connects the Wideband Code Division Multiple Access (WCDMA) and Global System for Mobile Communication (GSM) input/output to the antenna of the Mobile Phone. It is a bi-directional RF interface containing signals in the range 800 MHz to 2.2 GHz. The mobile system antenna interface is the interface between the Mobile Phone Radio Frequency (RF) input/output and the mobile system antenna. The interface handles the GSM 850, EGSM 900, GSM 1800, GSM 1900 and WCDMA Band I, II and V, RF inputs/outputs.

Mobile System Antenna Interface:



Radio Module N1200 (Tiger)

Front End

The Front End block connects the proper block in the radio system to the antenna. The Front End has two inputs for EDGE/GSM/GPRS, one for low band (850/900 MHz) and one for high band (1800/1900 MHz). The EDGE/GSM/GPRS power amplifier output is filtered by the low pass filter in the Front End and then connected to the antenna through a switch. In receive mode, the EDGE/GSM/GPRS signal from the antenna passes through the switch to one of the four receive SAW filters. The SAW filter provides receive band selectivity. In GSM/GPRS/EDGE systems, transmit and receive operations are divided in time and the switch connects the proper block in accordance with the mode of operation (that is, transmit or receive; one at a time).

In WCDMA the transmit outputs from the WCDMA transceiver are filtered by an external SAW filter that cleans up the spectrum. The SAW filter output is connected to the power amplifier, one for each band. For power control, a sample of the transmit output is taken by a directional coupler and converted to a DC level by the power detection circuit. This signal is used to control the transmitter output power. The transmit signal passes through an isolator and then a duplexer. The duplexer output is selected by the switch in the Front End for connection to the antenna. In WCDMA receive mode the signal from the antenna is switched by the Front End to the correct duplexer. The output from the duplexer is connected to the LNA input in the WCDMA receiver.

Transceiver

The transceiver is a multi-mode transceiver for WCDMA/EGDE/GPRS/GSM. The EDGE/GPRS/GSM part of the transceiver use a digital baseband interface that is shared between received and transmitted data. The receive interface is based on I and Q data and the transmitter interface is based on envelope and frequency data. The WCDMA part of the transceiver use differential analog in-phase and quadrature-phase interfaces, which is an IQ-interface, in the receiver and the transmitter data paths.

Frequency Generation

The 26 MHz reference signal is used as the reference for the on-chip synthesizers. To cover the required frequency range, the integrated Voltage Controlled Oscillator (VCO) operates at twice the frequency for band 1800/1900/2100, and at four times the desired frequency for band 800/900. The two synthesizers are controlled through the serial bus from the access side of the digital baseband controller.

EDGE/GPRS/GSM Transmitter Part

Polar modulation transmitter architecture based on the direct phase/frequency modulation/synthesizer architecture is implemented for GSM, GPRS and EDGE. This architecture has the capability of generating both the GSM/GPRS constant envelope GMSK modulation and the linear EDGE 8-PSK modulation in a very cost efficient way. The motivation for a polar modulation transmitter architecture compared to traditionally linear architectures is to reduce the output noise (thus eliminating the need for off-chip filters) reduce the power consumption by utilizing non-linear switching analog signal processing blocks, and to eliminate the need for an RF isolator.

In brief, the phase/frequency modulator in this polar modulation architecture is a sigma-delta controlled fractional-N frequency synthesizer with an additional frequency insertion point after the loop filter at the input of the VCO. The Phase-locked Loop (PLL) has two information inputs: the divider ratio in the feedback path and a direct path to the VCO. The phase locked loop generates the radio frequency carrier including the phase modulation information at the desired channel frequency.

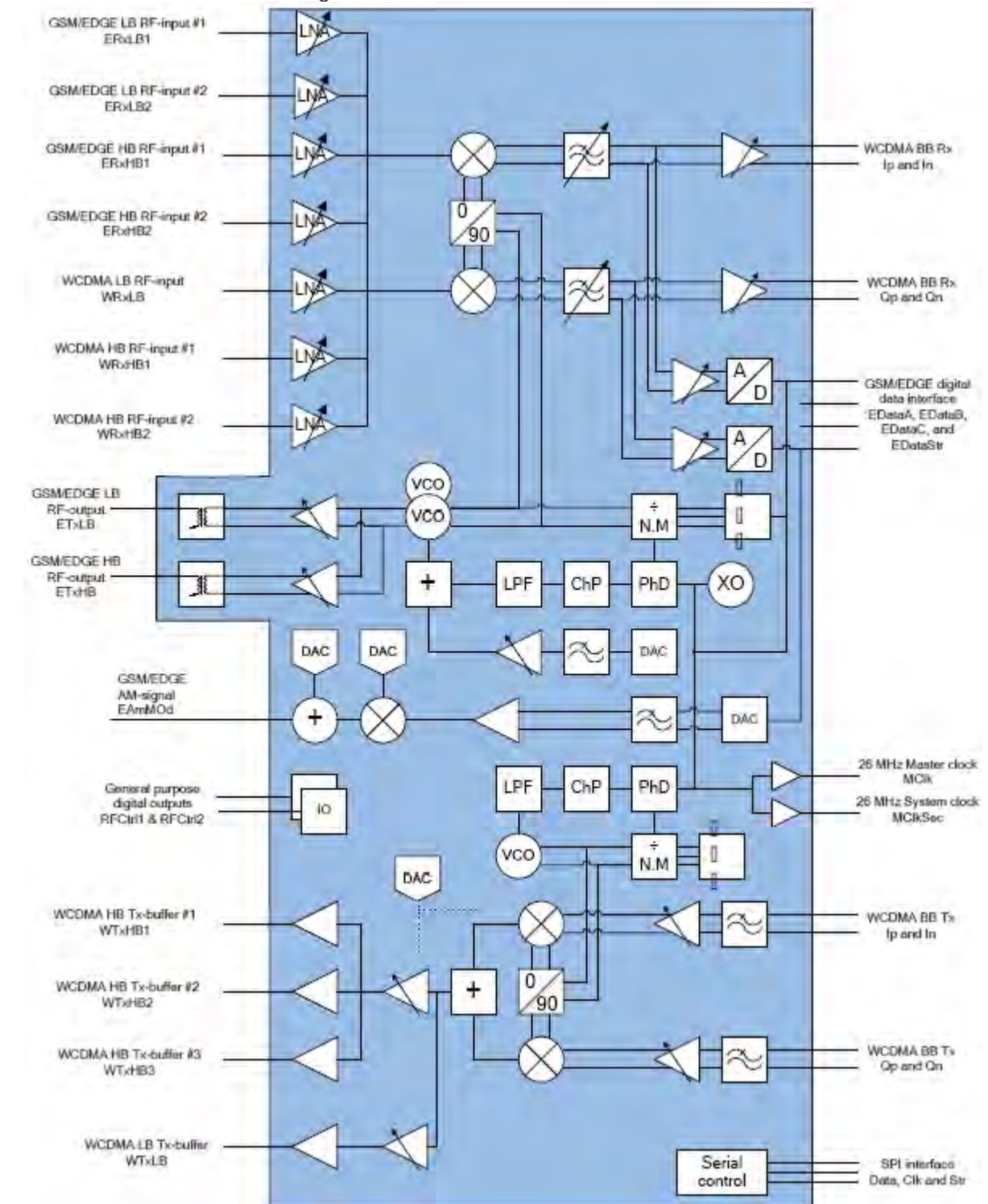
WCDMA Transmitter Part

The WCDMA transmitter architecture is an on frequency linear direct up-conversion IQ-modulator. The in-phase and quadrature-phase reconstruction filters are fully integrated and a programmable gain amplifier implements the gain control. An external SAW filter between the WCDMA circuit and the power amplifier is used to improve noise performance. After the power amplifier, the signal is sent through an isolator and through the duplex filter, which directs the transmit signal to the antenna connector through the antenna switch. The supply voltage and bias of the power amplifier are adapted depending on the output power to achieve high efficiency at every transmitter power level. A high efficiency DC/DC converter regulates the supply voltage and the bias operation point is controlled by a D/A-converter in the WCDMA radio circuit.

Receiver Part

The receiver architecture is a direct down-conversion zero-IF receiver with integrated low-pass filters. The complete receiver with seven Low Noise Amplifiers (LNAs), one for each supported band, is integrated on chip. After the down-conversion, the in-phase and quadrature-phase components are low pass filtered and if the receiver is in EDGE/GPRS/GSM mode the signals are fed to the integrated high dynamic range sigma-delta A/D-converters.

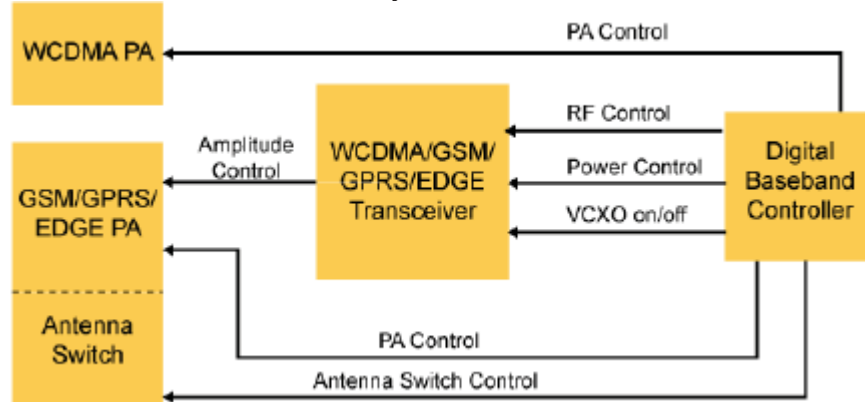
Ericsson RF 3300 Block Diagram:



RF System Control

The access side of the digital baseband controller controls the overall radio system. In both EDGE/GSM/GPRS and WCDMA air interface mode, the digital baseband controller controls the radio system through a three-wire serial bus. The digital baseband controller also manages PA band control and the antenna switch mechanism in the front end module. The 26 MHz VCXO clock residing in the transceiver is turned on only when required and initiated by the digital baseband controller.

The control flow for the RF system:



EDGE / GPRS / GSM

TX Frequency, Channel and Power Level Range:

GSM 850:

TX Frequency Range: 824,2 MHz – 848,8 MHz
Channel Range TX: 128 – 251
Power Level: Min 19 – Max 5

GSM 900:

TX Frequency Range: 890,2 MHz – 914,8 MHz
Channel Range TX: 1 - 124
Power Level: Min 19 – Max 5

EGSM 900:

TX Frequency Range: 880,2 MHz – 889,8 MHz
Channel Range TX: 975 - 1023
Power Level: Min 19 – Max 5

DCS 1800:

TX Frequency Range: 1710,2 MHz – 1784,8 MHz
Channel Range TX: 512 – 885
Power Level: Min 15 – Max 0

PCS 1900:

TX Frequency Range: 1850,2 MHz – 1909,8 MHz
Channel Range TX: 512 - 810
Power Level: Min 15 – Max 0

RX Frequency and Channel Range:

GSM 850:

RX Frequency Range: 869,2 MHz – 893,8 MHz
Channel Range RX: 128 – 251

GSM 900:

Frequency Range: 935,2 MHz – 959,8 MHz
Channel Range RX: 1 - 124

EGSM 900:

RX Frequency Range: 925,2 MHz – 934,8 MHz
Channel Range RX: 975 – 1023

DCS 1800:

RX Frequency Range: 1805,2 MHz – 1879,8 MHz
Channel Range RX: 512 – 885

PCS 1900:

RX Frequency Range: 1930,2 MHz – 1989,8 MHz
Channel Range RX: 512 - 810

WCDMA

TX and RX Frequency and Channel Range

Band I:

Channel Range TX: 9612 - 9888
TX Frequency Range: 1920 – 1980 MHz
Channel Range RX: 10562 - 10838
RX Frequency Range: 2110 – 2170 MHz

Band II:

Channel Range TX: 9262 - 9538
TX Frequency Range: 1850 – 1910 MHz
Channel Range RX: 9662 - 9938
RX Frequency Range: 1930 – 1990 MHz

Band V:

Channel Range TX: 4132 – 4233
TX Frequency Range: 824 – 849 MHz
Channel Range RX: 4357 – 4458
RX Frequency Range: 869 – 894 MHz

Band VIII:

Channel Range TX: 2712 – 2863
TX Frequency Range: 880 – 915 MHz
Channel Range RX: 2937 – 3088
RX Frequency Range: 925 – 960 MHz

Bluetooth and FM Radio

The Bluetooth/FM Radio circuit combines Bluetooth and FM tuner functionality into one.

Bluetooth

The Bluetooth implementation is compliant with Bluetooth specification 2.1 + EDR. The Bluetooth™ transceiver has frequency channels with 1 MHz separation from 2402 to 2480 MHz. The same band is used for both transmission and reception. This gives 79 frequency channels.

Receiver

The Bluetooth section implements a low-IF receiver for Bluetooth modulated input signals. The radio signal is taken from a balanced RF input and amplified by an LNA. The mixers are driven by two quadrature LO signals, which are locally generated from a VCO signal running at twice the frequency. The I and Q mixer output signals are band pass filtered by a poly-phase filter for channel filtering and image rejection. The output of the band pass filter is amplified by a VGA to the optimal input range for the A/D converter. Further channel filtering is done in the digital part. The digital part demodulates the GFSK, π/4-DQPSK or 8-DPSK coded bit stream by evaluating the phase information. RSSI data is extracted. Overall automatic gain amplification in the receive path is controlled digitally. The RC time constants for the analog filters are automatically calibrated on chip.

Transmitter

The transmitter uses the serial transmit data from the Bluetooth Controller. The transmitter modulator converts this data into GFSK, π/4-DQPSK or 8-DPSK modulated I and Q digital signals for respectively 1, 2 and 3 Mbps transmission speed. These signals are then converted to analog signals that are low pass filtered before up-conversion. The carrier frequency drift is limited by a closed loop PLL.

FM Radio

FM Receiver

The receiver uses a digital low-IF architecture. The receive (RX) section integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (76 to 108 MHz). An automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. An image-reject mixer down converts the RF signal to low-IF. The quadrature mixer output is amplified, filtered and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the use of digital signal processing (DSP) to perform channel selection, FM demodulation and stereo audio processing.

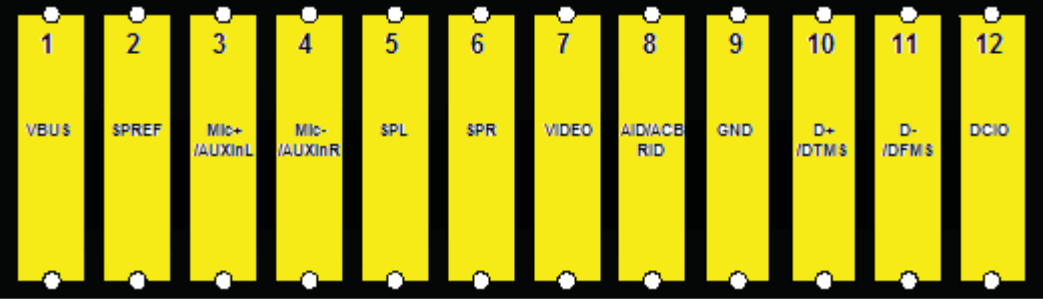
Tuning

The receiver uses frequency synthesizer technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception. The tuning frequency is defined as: $\text{Freq (MHz)} = \text{Spacing (kHz)} \times \text{Channel} + \text{Bottom of Band (MHz)}$

External Connectors

External units are connected to the transceiver by means of a 12-pin connector on the bottom of the phone.

System connector pin input/output overview:



Clocks

Clock Distribution

The clocking for the access and application subsystems is separated. This means that the subsystems can wake up or go to sleep mode independently. The access subsystem is clocked by the 26 MHz Voltage Controlled Crystal Oscillator (VCXO) located in the GSM/EDGE circuit. When the access subsystem has a job to do, the Master Clock (MCLK) signal is requested from the RF part. Most other clocks needed within the access subsystem are generated from the MCLK. Some minor parts like sleep timer and cable detect use the 32 kHz real-time clock. The 32 kHz real-time clock clocks the application subsystem, and all other internal clocks needed within the application subsystem are generated from this clock. However, when audio is transferred between the application and the access subsystems, the MCLK is used.

Master Clock
(26 MHz)

The 26.00 MHz VCXO-based MCLK is distributed as a square wave signal from the GSM/EDGE circuit. In order to have full control over the load on the MCLK, only the access side of the digital baseband controller is allowed to request the MCLK. However, by indirect means also the application side CPU can issue the request. A VCXO-based square wave is also distributed to the WCDMA circuit, but is turned on only upon a command from the digital baseband controller.

Real-time Clock
(32. 768 KHz)

A 32.768 kHz crystal oscillator provides a low frequency clock whenever the platform has power. This clock is used to keep the Real-Time Clock (RTC) block functioning, so that the platform can keep track of the time and date. The low frequency clock is generated in the analog baseband controller and distributed to the digital baseband controller, and if necessary to external devices like Bluetooth, FM radio and A-GPS.

A-GPS

The Assisted GPS functionality in the phone is realized with the Global Locate Hammerhead GPS module. The Global Locate Hammerhead belongs to the Type 2 GPS solutions. The PMB 2525 Hammerhead II GPS IC is a GPS single chip device containing a complete radio frequency front-end as well as the signal processing functionality in a single die. The device allows the usage of assistance data by supporting A-GPS (assisted GPS) standards (RRLP, RRC, OMA SUPL). One of three serial interfaces, UART, I²C or SPI, is used for communication with the host system.

Clock Reference Frequency

The platform provides two reference frequencies, a 32.768 kHz clock (RTCCLK) from the Analog Baseband Controller, and a 26 MHz reference clock (SYSCLK) from the Digital Baseband Controller. The RTCCLK is used by the phone real time clock function. The RTCCLK is distributed to the A-GPS module as a logical square wave. SYSCLK is derived from the reference modulation clock MCLK to the platform access system and is distributed from the Digital Baseband Controller to the A-GPS module. This 26 MHz clock is synchronized with the cellular network to an accuracy of ± 0.1 ppm. Automatic frequency updates can also cause large frequency corrections, with associated phase discontinuities. In order to isolate the A-GPS module for the unstable effects of SYSCLK, an external reference clock is required. This external reference frequency provided by a TCXO is required to provide a clock with very high short term stability. The frequency of the TCXO is calibrated against the cellular reference clock by the A-GPS module enabling the use of a more economical less accurate TCXO.

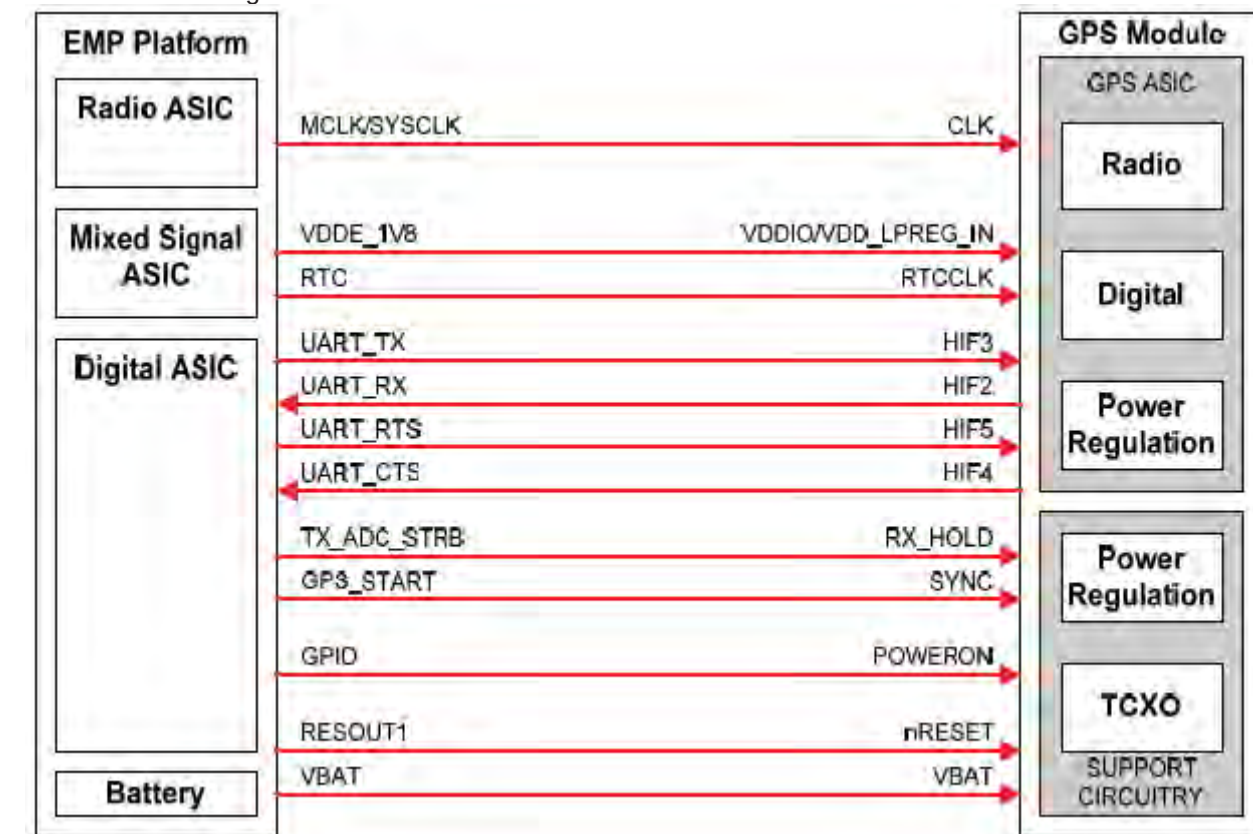
Interface and Control

The Interface and control consists of system timing and control. The control interface includes a communication link where both data and control information are transferred between platform and the A-GPS module. Data and command information is transferred using a full-duplex Universal Asynchronous Receiver Transmitter (UART) interface.

Other control signals include the following:

- A GPIO or platform reset used as a reset signal (nRESET) to the GPS module.
- A Transmission On signal (TXON/ RX_HOLD), is used to indicate to the A-GPS module when the ME is transmitting. The A-GPS modules receiver is disabled whilst the ME is transmitting.
- A hardware timing pulse (GPSSTART/SYNC) providing the A-GPS module with a highly accurate timing reference. The A-GPS is able to accurately synchronize its GPS time to this reference pulse.
- A GPIO used as an enable (POWERON) signal to the GPS module.
- A GPIO used for power control for the GPS module.

A-GPS Block Diagram:



WLAN (Wi-Fi)

This WLAN module is based on the new Marvell 88W8686 chipset. WLAN module is designed to support IEEE 802.11a or 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11b data rates of 1, 2, 5.5 and 11 Mbps. For security the WLAN module supports the IEEE 802.11i security standard through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), and Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP) security mechanism. For video, voice and multimedia applications the WLAN module supports 802.11e Quality of Service (QoS). The 3-wire Bluetooth / WiFi co-existence interface is also supported. The WLAN module has a fully integrated RF to baseband transceiver that operates in both the 2.4 GHz ISM radio band for 802.11g/b WLAN applications and 5 GHz UNII radio band for 802.11a WLAN applications. It contains all the circuitry to support both transmit and receive operations. The integrated LNA and AGC on the receive path is seamlessly controlled by baseband functions. Integrated transmitters up-convert the quadrature baseband signal and the deliver the RF signals to external power amplifiers for 2.4 GHz and 5 GHz radio band transmission. Local oscillator frequencies are generated by a fully integrated programmable frequency synthesizer. The loop bandwidth is optimized for phase noise and dynamic performance and quadrature signals are generated on-chip.

BT / WLAN Co-existence

Standards bodies did not fully anticipate the range of scenarios in which WLAN and Bluetooth would compete for the same spectrum therefore IEEE 802.11 (WLAN) and Bluetooth use the same 2.4 GHz ISM frequency band (although they use different access mechanisms). They also did not include comprehensive, robust, and cooperative mechanisms in their respective standards to mitigate interference. Since no mechanism for exchanging signal status information has been built into the two standards, the task of minimizing interference must be accomplished by other means. Co-location refers to the situation where both Bluetooth and WLAN are in functional mode, that is, they are both fully radio operational, performing either transmission or reception activities (or ready to do so immediately). They also either share an antenna or each module has its

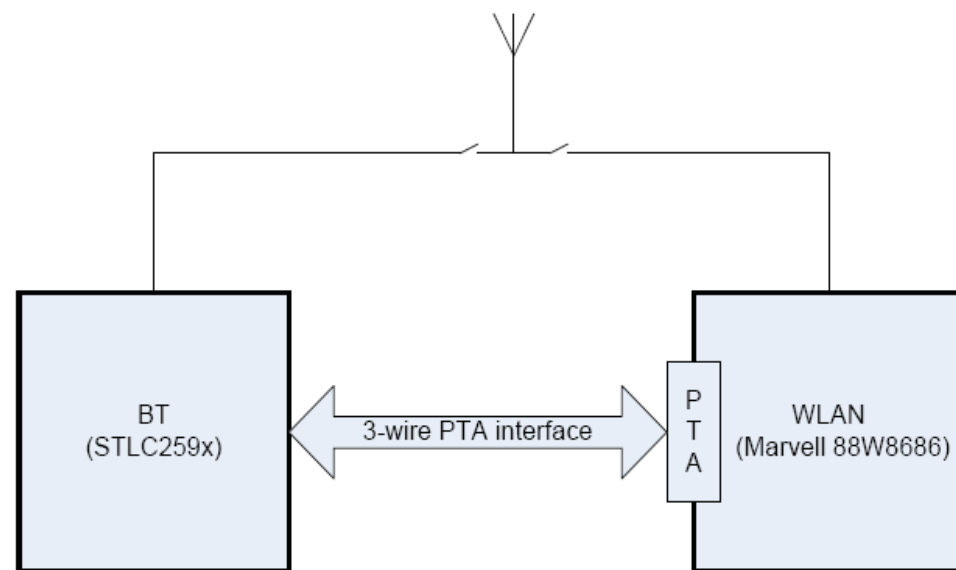
own antenna, on the same device. Because both Bluetooth and WLAN operate in the same unlicensed ISM band (2.4GHz), steps are required to avoid disturbances and allow coexistence. The HW solution is a single antenna controlled by an Antenna Switch with 3-wired lines between WLAN Device and BT Device. The used algorithm to decision whether WLAN device or BT device gets the antenna is Packet Traffic Arbitration (PTA). WLAN LD configures the PTA during startup of the WLAN device. All PTA parameters are stored in GDFS. The PTA is configured to prioritize BT traffic if it is a BT high request. All WLAN traffic should have priority before any BT traffic that is categorized as BT low requests.

WLAN Driver sends status events to BT Driver to inform about:

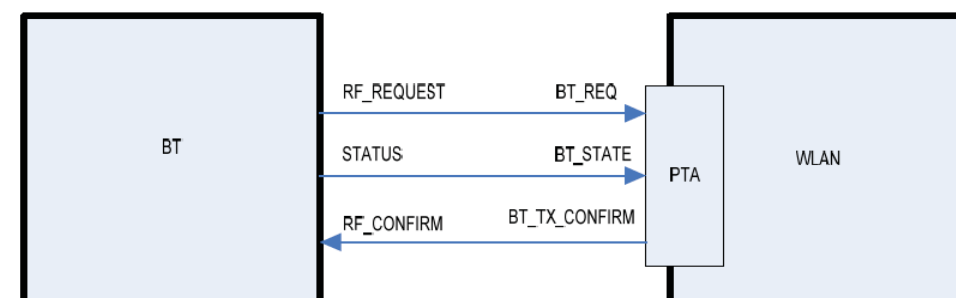
- WLAN startup and shutdown
- WLAN association and disassociation
- The current WLAN channel in use

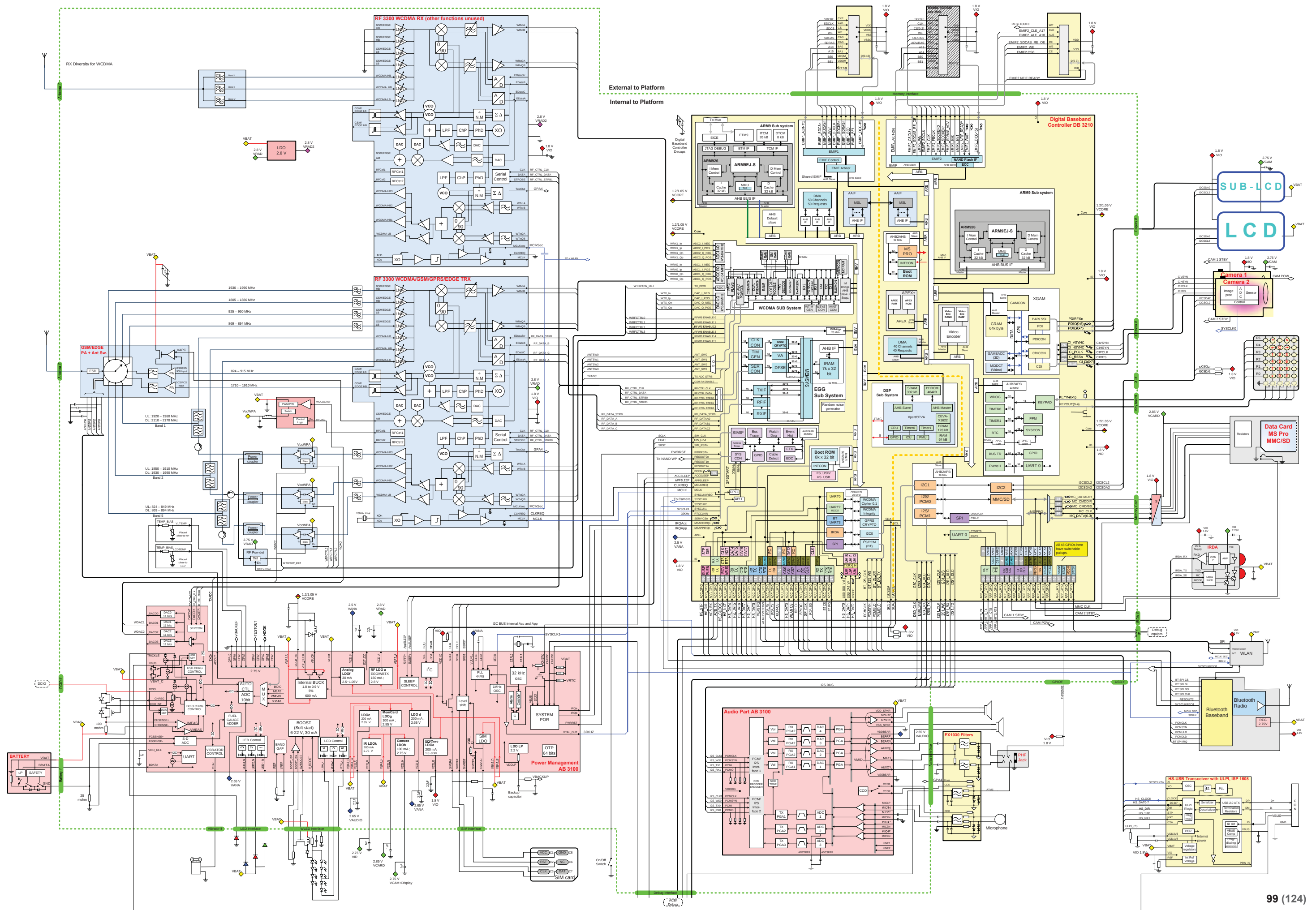
In the cases of WLAN startup and shutdown the BT Logical Driver configures the BT Device to request the antenna from PTA or not. BT LD also monitors if WLAN have any connection running. In that case, BT avoids the BT frequencies mapping to the WLAN channel. WLAN monitors if BT has started any BT Inquiry or page. If this happens any link loss mechanisms should be temporary turned off for the BT Inquiry or page period.

Bluetooth and WLAN PTA Mechanism:

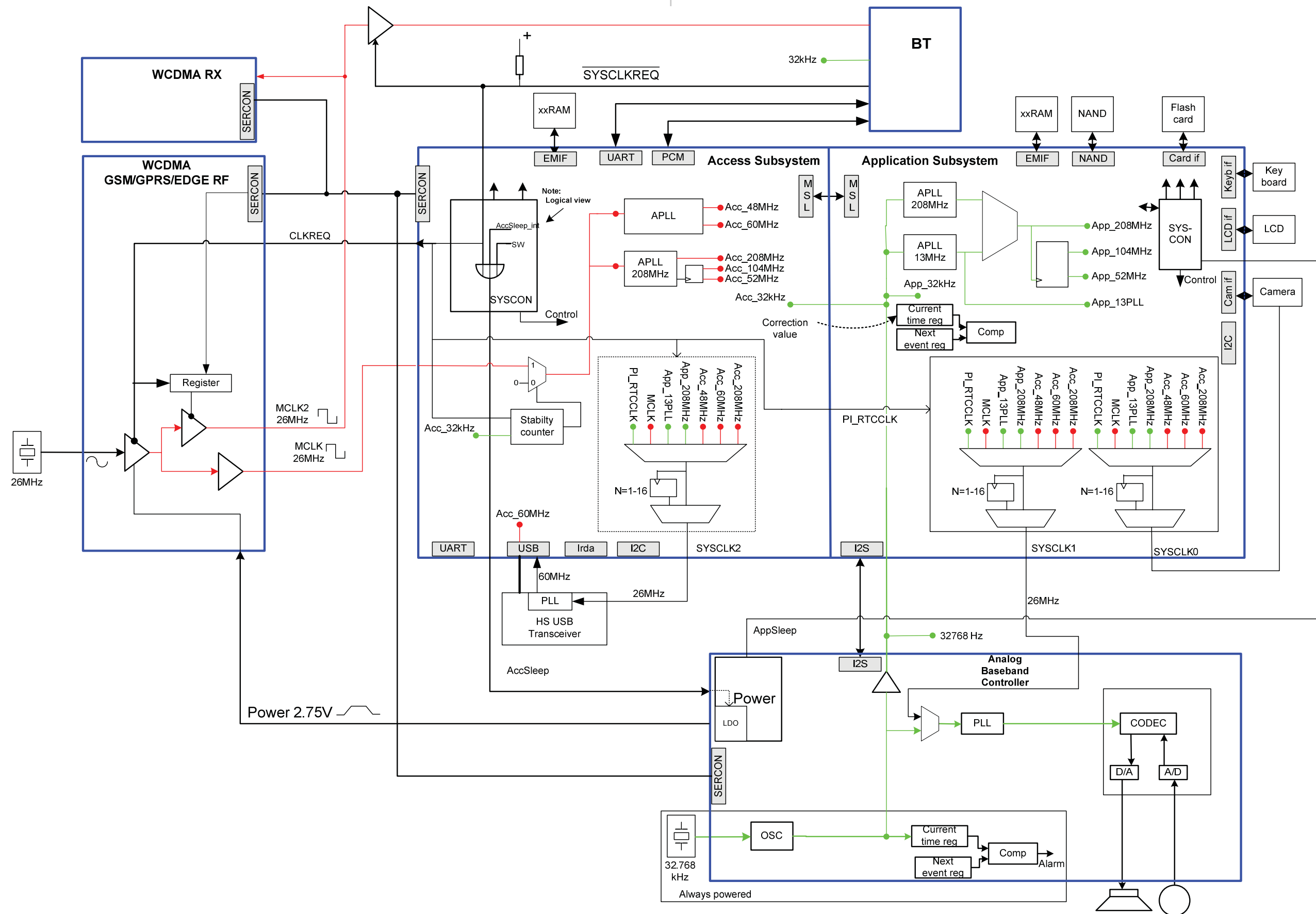


Bluetooth and WLAN Chip 3-wire Interface:









Part List Main Board

Contains only components that are possible to replace on the main board.
Pos. number refers to the components position number on the board.

Some components are noted as MSL X. These components are moisture-sensitive and are rated at various levels (MSL):

- Level 1:** Unlimited floor life; does not require dry pack or re-baking.
- Level 2:** 1 year floor life; ≤ 30 C; 60%rh; shipped in dry pack; must be re-baked after being opened if floor life is exceeded.
- Level 2A:** 4 week floor life; ≤ 30 C; 60%rh; shipped in dry pack; must be re-baked after being opened if floor life is exceeded.
- Level 3:** 168 hours floor life; ≤ 30 C; 60%rh; shipped in dry pack; must be re-baked after being opened if floor life is exceeded.
- Level 4:** 72 hours floor life; ≤ 30 C; 60%rh; shipped in dry pack; must be re-baked after being opened if floor life is exceeded.
- Level 5:** 48 hours floor life; ≤ 30 C; 60%rh; shipped in dry pack; must be re-baked after being opened if floor life is exceeded.
- Level 5A:** 24 hours floor life; ≤ 30 C; 60%rh; shipped in dry pack; must be re-baked after being opened if floor life is exceeded.
- Level 6:** 6 hours floor life; ≤ 30 C; 60%rh; shipped in dry pack; must be re-baked after being opened if floor life is exceeded.

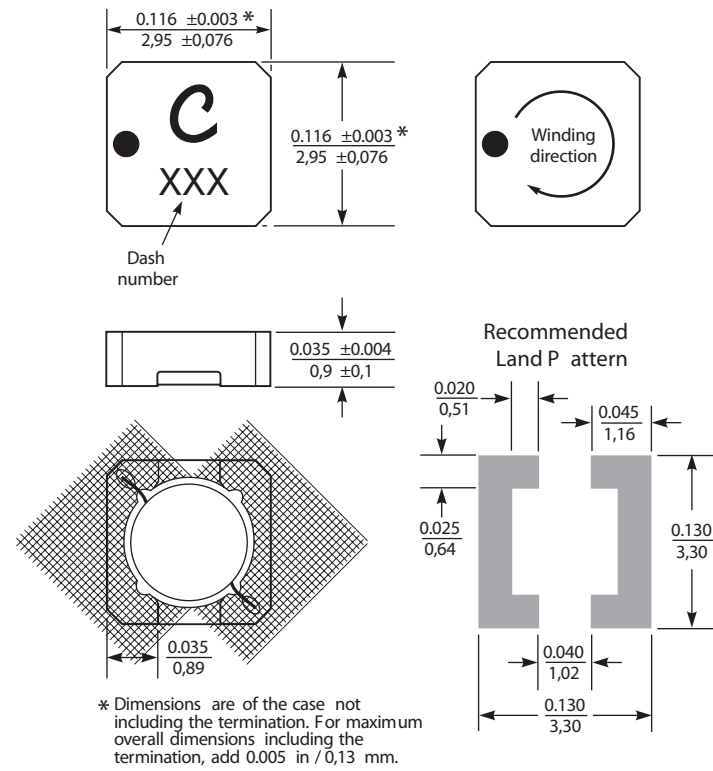
NOTE! RF Calibration by using SERP can only be done by authorized repair centers.
Fence modification according to Working Instruction Electrical.

F = Front Side, B = Back Side.

Side	Pos.	Description	Part Number	Comments	Page
F	C2214	0,07 F 3.3 V Capacitor	RJE3551335/7		
B	L2200	Ind WW 4,7 uH $\pm 20\%$ 2,95x2,95x0,9	1201-2245		103
B	L2201	120ohm 0603 2A 50mohm Bead	REG70605/15		
B	L2401	Filter 0.0Hz 0402	REG70618/20		103
B	L2402	Filter 0.0Hz 0402	REG70618/20		103
B	L2403	Filter 0.0Hz 0402	REG70618/20		103
B	L2404	Filter 0.0Hz 0402	REG70618/20		103
B	L2406	Filter	1209-2182		103
F	L2407	Filter 1.0 GHz 0402	REG70618/18		
B	L2408	Transformer	REG70609/06		
B	L4200	Inductor Chip	1200-6306		103
B	N1210	IC Linear	1203-5870		104
F	N1211	LDO Regulator 300mA low noise	1204-5903		104
F	N1300	Bluetooth and RDS FM radio tuner	1200-9840		105
F	N1510	Mod Radio WLAN R041D	1200-6173	Not on EDGE variant, C905c	104
B	N2200	IC Vreg SON 6-Pin 2x2x0.8mm	1204-4655		104
F	N2201	LDO, 3.0V, 150mA, CS-4	RYT113955/7		
B	N2205	LDO regulator 500mA	RYT1137807/1		
B	N2206	LDO Dual 2.8 V & 1.8 V	1201-6517		105
F	N2208	LDO, 3.0V, 150mA, CS-4	RYT113955/7		
F	N2209	LDO regulator 150mA low noise	RYT113955/4		
F	N2212	LDO regulator 150mA	1200-1974		105
B	N2213	Step Down Converter 500mA	1208-4678		105
F	N2300	ASIC Power Management	1203-2790		106
F	N2410	IC IF 3.5x3.5x0.8 thin QFN	1200-1951		106
F	N2411	ASIC Accelerometer	1202-1676		106
F	N2420	IC IF ISP1508 ES3 (3.5*3.5*0.8)	1200-1694		107

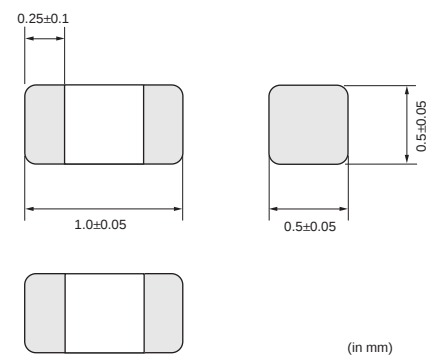
Side	Pos.	Description	Part Number	Comments	Page
F	N2421	IC ESD Prot UDFN 6 2x2 mm	1200-6309		107
B	N2422	ASIC Baseband	1201-4120		107
F	N2500	Companion chip MP202	1200-1414		108
F	N2700	TV Out Graphics Engine	1200-0362		108
F	N3100	IC CS-9	1200-9978		108
B	N3101	ASIC Tjatte3 CSP20	ROP1013074/1		109
F	N4400	IC Dri MAX8830 ES3 4x4 UCSP	1200-1922		109
F	R2443	Resistor 0.0 Ohm $\pm 5\%$ NA mW K0402	REP622001/0		
B	R2448	Resistor 0.0 Ohm $\pm 5\%$ NA mW K0402	REP622001/0		
F	S2415	Input Switch	1204-1127		109
F	S2424	Input Switch	1204-1127		109
F	S2453	Input Switch	1204-1127		109
F	S2454	Input Switch	1204-1127		109
B	V2200	Zener diode	RKZ223911/1		109
B	V2202	Trans P-ch FET	RYN122910/1		109
B	V2412	Zener Diode voltage regulator 15V 5%	RKZ223905/2		109
F	V2414	Diode Protection 5, V SOD-923	1201-8440		110
F	V2415	Diode Protection 5, V SOD-923	1201-8440		110
F	V2416	Diode Protection 5, V SOD-923	1201-8440		110
B	V2417	Zener Diode voltage regulator 15V 5%	RKZ223905/2		109
F	V2470	Schottky Barrier Diodes 2PIN	RKZ123905/1		110
B	V3101	Dual ESD protection diode 6V	RKZ223914/2		
B	V4200	Transistor, Mosfet, N-Channel	RYN123915/1		
B	V4201	Diode Schottky 0, SOD523	RKZ123905/2		110
F	V4203	Trans Array	1200-0320		110
B	V4206	LED Red	RKZ433924/1		110
F	X1200	RF probe contact 6 Pin	1203-9688		110
B	X1210	Conn Leaf Spring	1200-2144		110
B	X1211	Conn Leaf Spring	1200-2144		110
F	X1500	RF probe contact 6 Pin	1203-9688		110
F	X1530	Conn other	RNT79925		
B	X1540	Clip BT antenna	1211-1063		111
B	X2201	Battery Leaf Connector	1201-0774		111
B	X2401	Memory Card Reader	RNK87147/3	<i>Replaceable on EDGE variant only</i>	111
B	X2402	SIM Card Reader	1202-0528		111
F	X2405	System Connector	1202-1195		
B	X2410	BtB Receptacle 24pin	1208-3264		112
B	X2411	Clip Camera switch	1208-2932		
B	X3102	Conn Leaf Spring	1200-2144		110
B	X3103	Conn Leaf Spring	1200-2144		110
F	X4200	100 pin FPC connector	1204-5252		112
F	X4300	Conn BtB 30 pin	1200-1733		112
F	X4311	Ground Spring Finger 1 pin	1204-9353		112
F	X4312	Ground Spring Finger 1 pin	1204-9353		112
F	X4313	Ground Spring Finger 1 pin	1204-9353		112
F	X4314	Ground Spring Finger 1 pin	1204-9353		112
F	X4315	Ground Spring Finger 1 pin	1204-9353		112
B	X4400	Conn BtB 24 pin	1201-5197		112
B	X4410	Pogopin Plug 1pin	1208-0925		113
F	Z2400	Filter 100, MHz K1210	1201-6833		113
F	Z4200	LC Filter	REV50148/1		113
F	Z4201	LC Filter	REV50148/1		113
F	Z4202	LC Filter	REV50148/1		113

L2200 Ind WW 4,7 uH +-20% 1201-2245

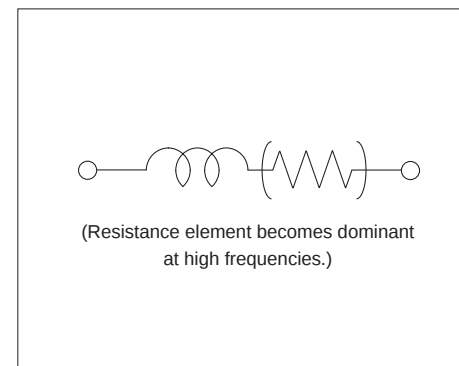


L2401-04 Filter 0.0 Hz 0402 REG70618/20

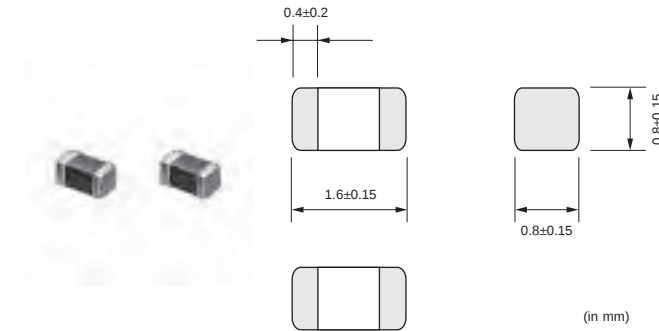
■ Dimension



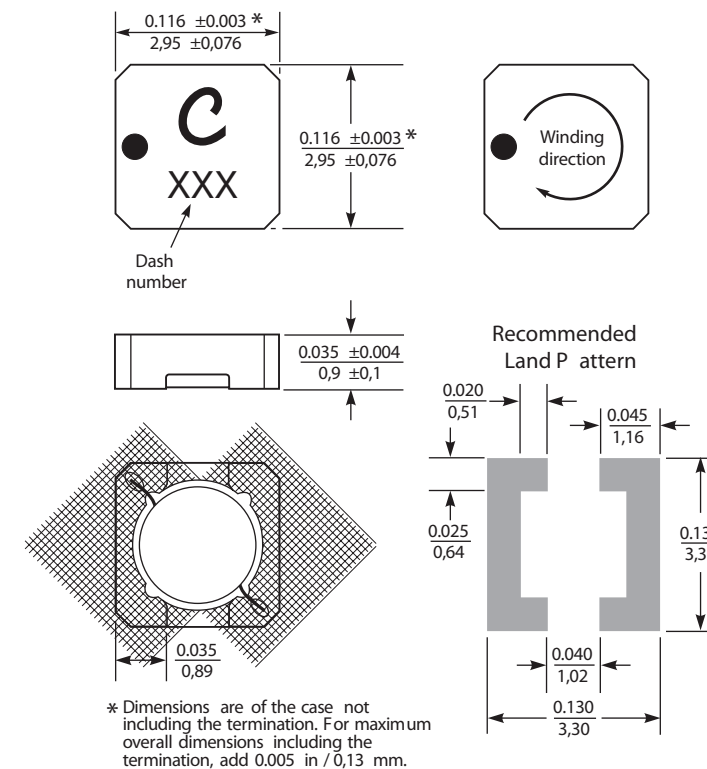
■ Equivalent Circuit



L2406 Filter 1209-2182

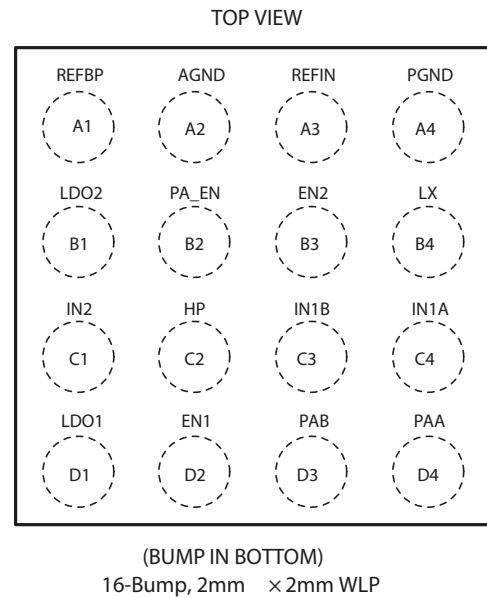


L4200 Inductor Chip 1200-6306

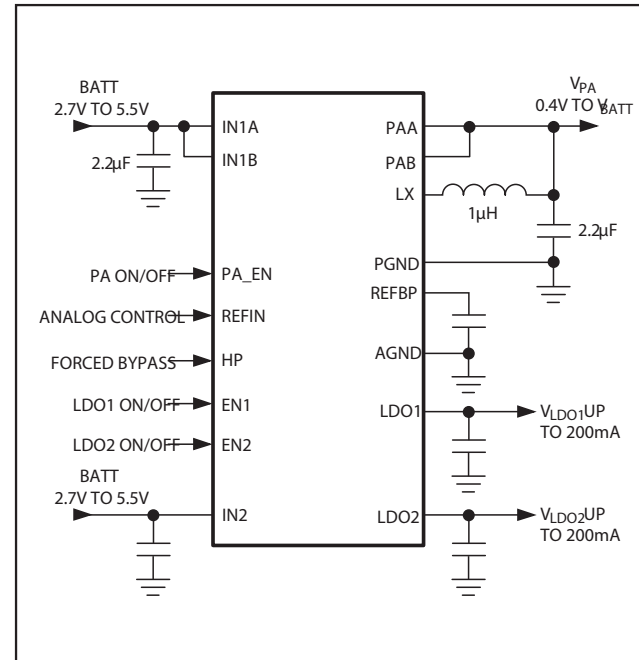


N1210 IC Linear 1203-5870

Pin Configuration



Typical Operating Circuit

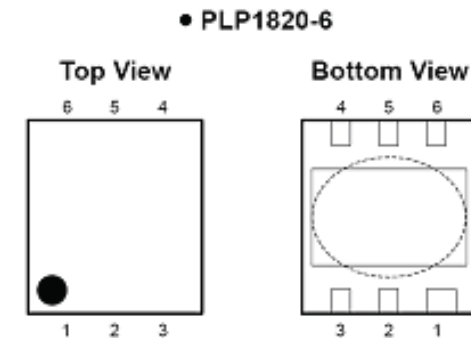


Pin Description

PIN	NAME	FUNCTION
A1	REFBP	Reference Noise Bypass. Bypass REFBP to AGND with a 0.22µF ceramic capacitor to reduce noise on the LDO outputs. REFBP is internally pulled down through a 1kΩ resistor during shutdown.
A2	AGND	Low-Noise Analog Ground
A3	REFIN	DAC-Controlled Input. The output of the PA step-down converter is regulated to 2 x V _{REFIN} . When V _{REFIN} reaches 0.465 x V _{IN2} , bypass mode is enabled.
A4	PGND	Power Ground for PA Step-Down Converter
B1	LDO2	200mA LDO Regulator 2 Output. Bypass LDO2 with a 1µF ceramic capacitor as close as possible to LDO2 and AGND. LDO2 is internally pulled down through a 1kΩ resistor when this regulator is disabled.
B2	PA_EN	PA Step-Down Converter Enable Input. Connect to IN ₂ or logic-high for normal operation. Connect to GND or logic-low for shutdown mode.
B3	EN2	LDO2 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
B4	LX	Inductor Connection. Connect an inductor from LX to the output of the PA step-down converter.
C1	IN2	Supply Voltage Input for LDO1, LDO2, and Internal Reference. Connect IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN2 with a 2.2µF ceramic capacitor as close as possible to IN2 and AGND. Connect IN2 to the same source as IN1A and IN1B.
C2	HP	High-Power Mode Set Input. Drive HP high to invoke forced bypass mode. Bypass mode connects the input of the PA step-down converter directly to its output through the internal bypass MOSFET. Drive HP low to disable the forced bypass mode.
C3, C4	IN1B, IN1A	Supply Voltage Input for PA Step-Down Converter. Connect IN1 ₂ to a battery or supply voltage from 2.7V to 5.5V. Bypass the connection of IN1 ₂ with a 2.2µF ceramic capacitor as close as possible to IN1 ₂ , and PGND. IN1A and IN1B are internally connected together. Connect IN1 ₂ to the same source as IN2.
D1	LDO1	200mA LDO Regulator 1 Output. Bypass LDO1 with a 1µF ceramic capacitor as close as possible to LDO1 and AGND. LDO1 is internally pulled down through a 1kΩ resistor when this regulator is disabled.
D2	EN1	LDO1 Enable Input. Connect to IN2 or logic-high for normal operation. Connect to AGND or logic-low for shutdown mode.
D3, D4	PAB, PAA	PA Connection for Bypass Mode. Internally connected to IN1 ₂ using the internal bypass MOSFET during bypass mode. PA ₂ is connected to the internal feedback network. Bypass PA ₂ with a 2.2µF ceramic capacitor as close as possible to PA ₂ and PGND.

N1211 LDO Regulator 300mA Low Noise 1204-5903

PIN CONFIGURATIONS



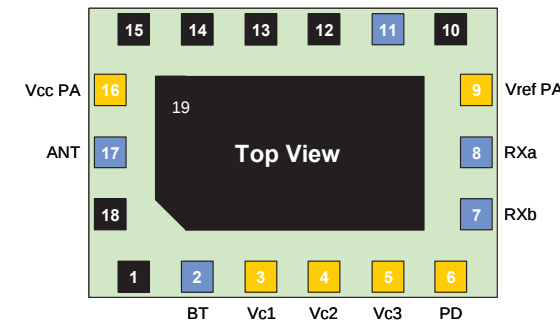
• PLP1820-6*

Pin No.	Symbol	Description
1	V _{OUT}	Output Pin
2	V _{OUT}	Output Pin
3	GND	Ground Pin
4	CE	Chip Enable Pin
5	V _{DD}	Input Pin
6	V _{DD}	Input Pin

* Tab in the parts have GND level.
(They are connected to the back side of this IC.)
Do not connect to other wires or land patterns.

N1510 Mod Radio WLAN R041D 1200-6173

Pin configuration

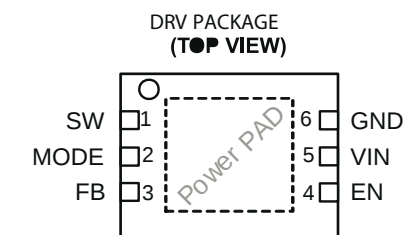


Pin assignment:

- | | |
|---------------------------|------------------------------|
| 1 - GND | 11 - TX |
| 2 - Bluetooth | 12 - GND |
| 3 - Vc1 (switch control) | 13 - GND |
| 4 - Vc2 (switch control) | 14 - GND |
| 5 - Vc3 (switch control) | 15 - GND |
| 6 - Power detector output | 16 - Vcc PA |
| 7 - RXb (balanced) | 17 - ANT |
| 8 - RXa (balanced) | 18 - GND |
| 9 - Vref PA | 19 - GND (center ground pad) |
| 10 - GND | |

N2200 IC Vreg SON 6-pin 1204-4655

PIN ASSIGNMENTS

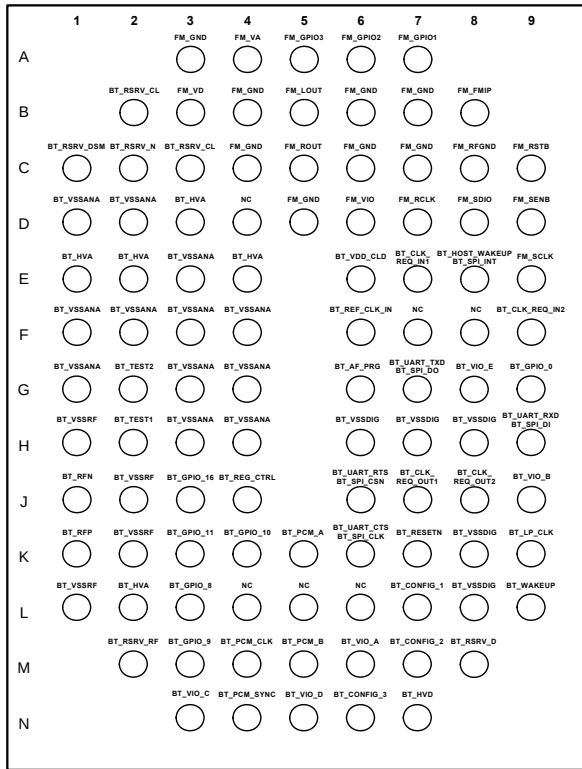


TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V _{IN}	5	PWR	VIN power supply pin.
GND	6	PWR	GND supply pin
EN	4	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	1	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
FB	3	I	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor
MODE	2	I	MODE pin = high forces the device to operate in fixed-frequency PWM mode. Mode pin = low enables the Power Save Mode with automatic transition from PFM mode to fixed-frequency PWM mode.

N1300 Bluetooth and RDS FM Radio Tuner 1200-9840

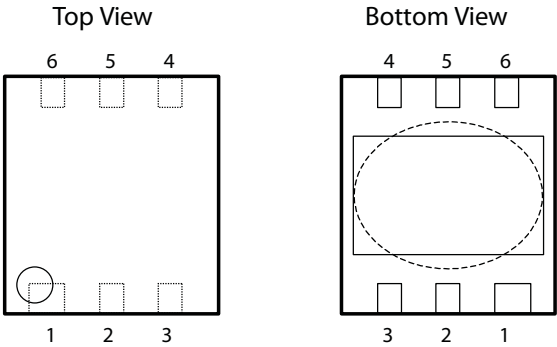
Pinout Top View



Bluetooth Section						
Name	Pin #	Description	Type	Reset ⁽¹⁾	Default ⁽²⁾ after reset	
BT_PCM_SYNC	N4	PCM frame signal	I/O ⁽⁴⁾	Input PD	Input PD	
BT_PCM_CLK	M4	PCM clock signal				
BT_PCM_A	K5	PCM data				
BT_PCM_B	M5	PCM data				
JTAG Interface						
BT_GPIO_9	M3	JTAG_TDI or GPIO	I/O ⁽⁴⁾	Input PU ⁽⁶⁾	Input PU ⁽⁶⁾	
BT_GPIO_11	K3	JTAG_TDO or GPIO		Input PD ⁽⁶⁾	Input PD ⁽⁶⁾	
BT_GPIO_10	K4	JTAG_TMS or GPIO		Input PU ⁽⁶⁾	Input PU ⁽⁶⁾	
BT_GPIO_16	J3	JTAG_NTRST (Active low) or Alternate function		Input PD ⁽⁶⁾	Input PU ⁽⁶⁾	
BT_GPIO_8	L3	JTAG_TCK or GPIO		Input PD ⁽⁶⁾	Input PD ⁽⁶⁾	
General Purpose Input/Output Pins						
BT_GPIO_0	G9	General purpose I/O	I/O ⁽⁴⁾	Input PD	Input PD	
Configuration Pins						
BT_CONFIG_1	L7	Configuration signal	I	Input	Input	
BT_CONFIG_2	M7					
BT_CONFIG_3	N6					
RF Signals						
BT_RFP	K1	Differential RF port	I/O			
BT_RFN	J1					
Power Supply						
BT_HVA	L2	Power supply (Connect to 2.75 V)				
	D3					
	E1					
	E2					
BT_HVD	N7	1.65 V to 2.85 V I/Os supply ⁽⁷⁾				
BT_VIO_A	M6					
BT_VIO_C	N3					
BT_VIO_D	N5					
BT_VIO_E	G8	1.17 V to 2.85 V I/Os supply ⁽⁷⁾				
BT_VIO_B	J9					
BT_VDD_CLD	E6	System clock supply 1.65 V to 2.85 V (Connect to BT_VIO_A in case of a digital reference clock input, to BT_VSSANA in case of an analog reference clock input.)				
Bluetooth Section						
Name	Pin #	Description	Type	Reset ⁽¹⁾	Default ⁽²⁾ after reset	
BT_VSSDIG	H6	Digital ground				
	H7					
	H8					
	K8					
	L8					
BT_VSSANA	D1	Analog ground				
	D2					
	E3					
	F1					
	F2					
	F3					
	F4					
	G1					
	G3					
	G4					
BT_VSSRF	H1	RF ground				
	L1					RF regulator ground
	J2					
BT_TEST1	H2	Test pin	I/O	Input ⁽⁶⁾	Input ⁽⁶⁾	
BT_TEST2	G2					
BT_AF_PRG	G6					Test pin (Leave unconnected) ⁽⁹⁾
FM Radio Section						
FM_GND	A3	FM ground (connect to ground plane on PCB)				
	B4					
	B6					
	B7					
	C4					
	C6					
	C7					
FM_VA	A4	Analog supply voltage (may be connected directly to battery)				
FM_VD	B3	Digital supply voltage (may be connected directly to battery)				
FM_GPIO1	A7	General purpose FM input/output	I/O	Input/Output	Input/Output	
FM_GPIO2	A6					
FM_GPIO3	A5					
FM_FMIP	B8	FM RF input				
FM_ROUT	C5	FM right audio output				
FM_LOUT	B5	FM left audio output				
FM_RF_GND	C8	FM RF ground (connect to ground plane on PCB)				
FM_RSTB	C9	FM reset (Active low) input	I	Input low	Input high	
FM_VIO	D6	FM I/O supply voltage				
FM_RCLK	D7	FM External reference oscillator input	I	Input	Input	
FM_SDIO	D8	FM Serial data input / output	I/O	Input/Output	Input/Output	
FM_SENB	D9	FM Serial enable input (active low)	I	Input	Input	
FM_SCLK	E9	FM Serial clock input	I	Input	Input	
Other Pins						
BT_RSRV_CL	B2	Test pin (Leave unconnected) ⁽⁹⁾				
BT_RSRV_D	C3					
BT_RSRV_DSM	M8					
BT_RSRV_N	C1					
BT_RSRV_RF	M2					
BT_REG_CTRL	J4					Regulator control pin ⁽¹⁰⁾
NC	D4	Any use ⁽¹¹⁾				
	F7					
	F8					
	L4					
	L5					
	L6					

- Pin behaviour during HW reset (BT_RESETN low).
- Pin behaviour immediately after HW reset and internal chip initialization, but before SW parameter download.
- See also pin BT_VDD_CLD.
- Reconfigurable I/O pin. The functionality of these I/Os can be configured through software parameter download
- Should be strapped to BT_VSSDIG if not used.
- JTAG mode.
- Described in section 4.3.
- To be strapped to BT_VSSANA.
- Pin is ST - reserved for test function and it must be soldered to an isolated pad (not connected to anything, just floating)
- Described in section 5.8.
- Pin is not connected internally in the package; any connection can be done on board, in order to ease the board layout.

N2206 LDO Dual 2.8V & 1.8V 1201-6517

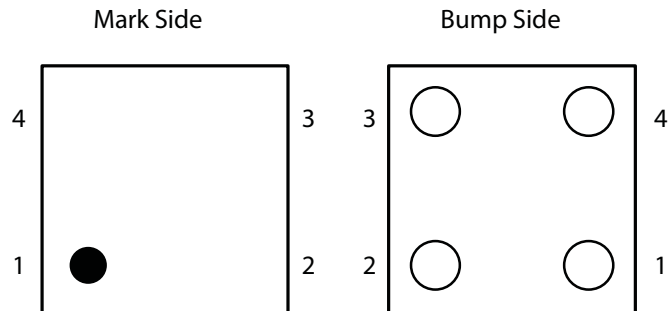


Pin No.	Symbol	Description
1	V _{OUT2}	Output Pin 2
2	V _{DD}	Input Pin
3	V _{OUT1}	Output Pin 1
4	GND	Ground Pin
5	CE 1	Chip E nable P in 1
6	CE2	Chip Enable Pin 2

* Tab in the  parts have GND level.
(They are connected to the reverse side of this IC.)
Do not connect to other wires or land patterns.

N2212 LDO Regulator 150mA 1200-1974

PIN CONFIGURATION

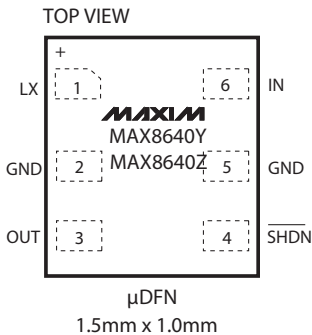


PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	V _{DD}	Input Pin
2	NC	No Connection
3	GND	Ground Pin
4	V _{OUT}	Output Pin

NN2213 Step Down Converter 500mA 1208-4678

Pin Configuration



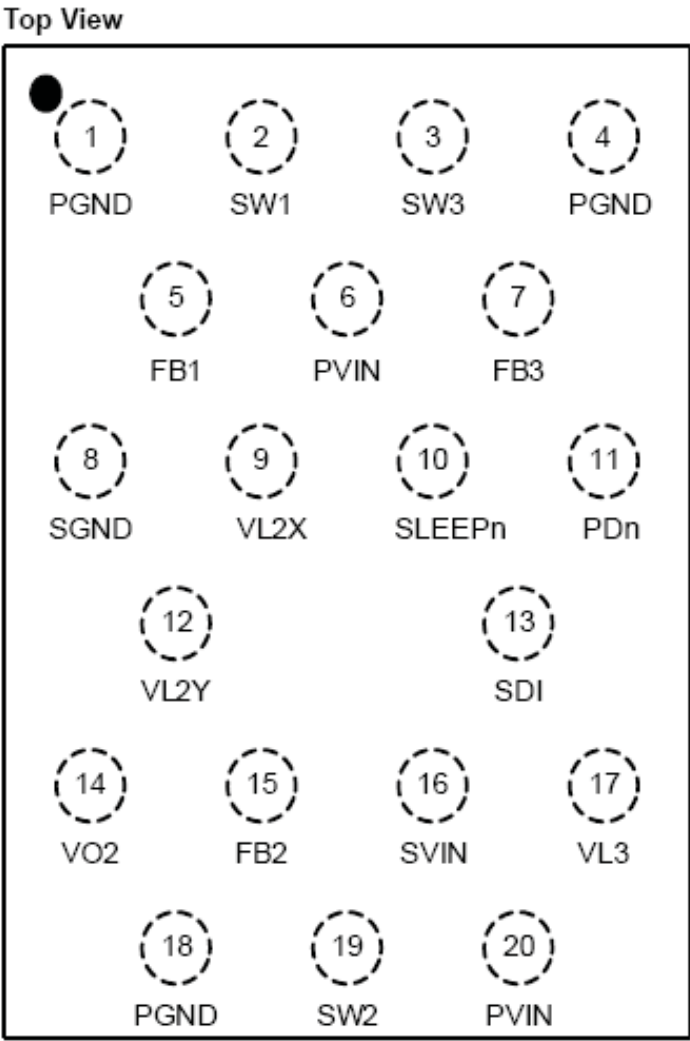
Pin Description and Assignment

The table shows the pin list of the STLC2593.
In columns "Reset" and "Default after reset", the "PD/PU" shows the pads implementing an internal pull-down/up for the internal Bluetooth section.
The column "Reset" shows the state of the pins during hardware reset; the column "Default after reset" shows the state of the pins after the hardware reset state is left, but before any software parameter download.
The column "Type" describes the pin directions:
– I for Input (All inputs have a Schmitt trigger function.)
– O for Output
– I/O for Input/Output
– O/I for tri-state output
For the output pin the default drive capability is 2 mA, except for pin K3 (BT_GPIO_11) and pin L3 (BT_GPIO_8) where it is 8 mA such that when used for Class 1, these 2 pins can be used for a switch control in a cheaper way.

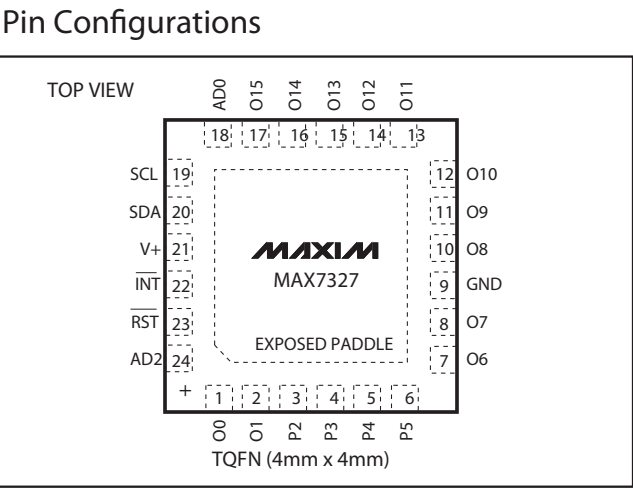
The STLC2593 Pin List (Functional and Supply)

Bluetooth Section					
Name	Pin #	Description	Type	Reset ⁽¹⁾	Default ⁽²⁾ after reset
Clock and Reset Pins					
BT_RESETN	K7	Global reset - active low	I	Input	Input
BT_REF_CLK_IN	F6	Reference clock input ⁽³⁾			
BT_LP_CLK	K9	Low power clock input			
SW Initiated Low Power mode					
BT_CLK_REQ_OUT_1	J7	Wake-up signal to Host (Active high or Active low, depending on configuration pins)	I/O ⁽⁴⁾	Input PD/IPU, depends on config	Output depends on config
BT_CLK_REQ_OUT_2	J8	Wake-up signal to Host. Active low (SPI mode only)		Input PU	I/O depends on config
BT_CLK_REQ_IN_1	E7	Clock request input (Active high)		Input PD	Input PD
BT_CLK_REQ_IN_2	F9	Clock request input (Active low)		Input PU	Input PU
BT_HOST_WAKEUP/ BT_SPI_INT	E8	Wake-up signal to Host or SPI interrupt		Input PD	Output
BT_WAKEUP	L9	Wake-up signal to Bluetooth (Active high)	I/O	Input ⁽⁵⁾	Input
UART Interface					
BT_UART_RXD/ BT_SPI_DI	H9	UART receive data SPI data in	I/O ⁽⁴⁾	Input PD	Input PD
BT_UART_TXD/ BT_SPI_DO	G7	UART transmit data SPI data out			Output high Input PD
BT_UART_CTS/ BT_SPI_CLK	K6	UART clear to send SPI clock		Input PU	Input PD
BT_UART_RTS/ BT_SPI_CSN	J6	UART request to send SPI chip select			Output low Input PU
PCM Interface					

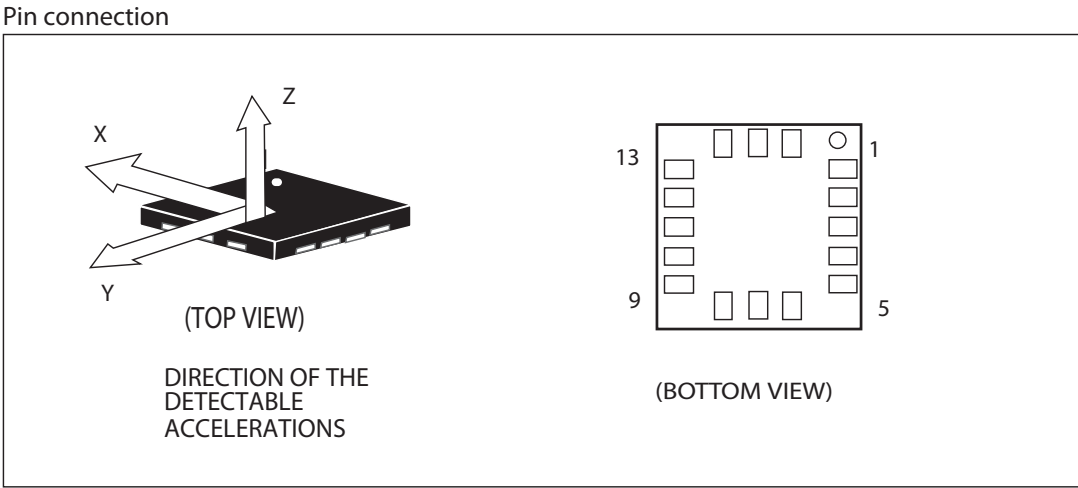
N2300 ASIC Power Management 1203-2790



N2410 IC IF 3.5x3.5x0.8 thin QFN 1200-1951



N2411 ASIC Accelerometer 1202-1676

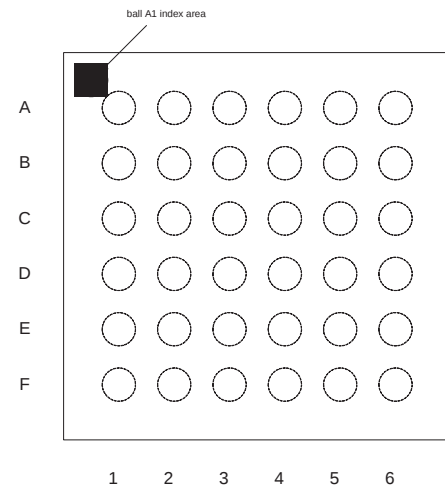


Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not Connected
3	NC	Not Connected
4	SCL SPC	I ² C Serial Clock (SCL) SPI Serial Port Clock (SPC)
5	GND	0V supply
6	SDA SDI SDO	I ² C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
7	SDO	SPI Serial Data Output I ² C less significant bit of the device address
8	CS	SPI enable I ² C/SPI mode selection (1: I ² C mode; 0: SPI enabled)
9	INT 2	Inertial interrupt 2
10	Reserved	Connect to Gnd
11	INT 1	Inertial interrupt 1
12	GND	0V supply
13	GND	0V supply
14	Vdd	Power supply
15	Reserved	Connect to Vdd
16	GND	0V supply

N2420 IC IF ISP1508 ES3 1200-1694

Pin Diagram



ISP1508 TFBGA36 pinout (top view)

Pin Description

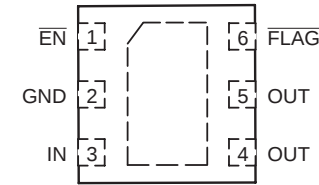
Symbol ¹	Ball No	Type ²	Description
RREF	C2	AI/O	Resistor reference. Connect through 12kΩ ±1% to GND.
DM	C1	AI/O	Connect to D- pin of the USB connector - USB mode: D- input/output - UART mode: TXD output
DP	D1	AI/O	Connect to D+ pin of the USB connector - USB mode: D+ input/output - UART mode: RXD input
FAULT	E2	I	Input for Vbus digital over-current or fault detector signal. If this pin is not in use, connect it to GND Plain input, 5V tolerant
ID	D3	I	identification (ID) pin of the mini-USB cable. If this pin is not in use, leave this pin open(there's internal pull-up). Plain input, TTL
VBUS	F4	AI/O	Connect to VBUS pin of the USB connector.
VCC	F3	P	Input supply voltage or battery source. Nominally 3.0V to 4.5V. Note: Below 3.0V, USB FS and LS transactions are not guaranteed to work though some devices may work with ISP1508 at these voltages.
PSW_N	D4	OD	Controls an external, active low VBUS power switch or charge pump. An external pull up resistor is required. Open drain,output, 5V tolerant.
REG3V3	E3	P	3.3V regulator output for USB mode or 2.7V regulator output for UART mode; requiring parallel 0.1 uF and 4.7 uF capacitors. Internally powers ATX and other analog circuits. Should not be used to power external circuits.
XTAL1	F5	AI/O	Crystal/clock input. 1.8V peak input allowed. Frequency depends on status on CFG1 and CFG2 pins.
XTAL2	F6	AI/O	Crystal output. If crystal is not in use, leave this pin open
CHIP_SEL	C3	I	Active HIGH chip select input. When this pin is none-active, ULPI pins will be in 3-state and the chip

¹ Symbol names ending with underscore N (for example, NAME_N) indicate active low signals

² I=input; O=output; I/O = Digital Input/Output; OD = Open Drain Output; AI/O = Analog Input/Output; P = Power or Ground pin

N2421 IC ESD Prot UDFN 6 2x2mm 1200-6309

PIN CONNECTIONS

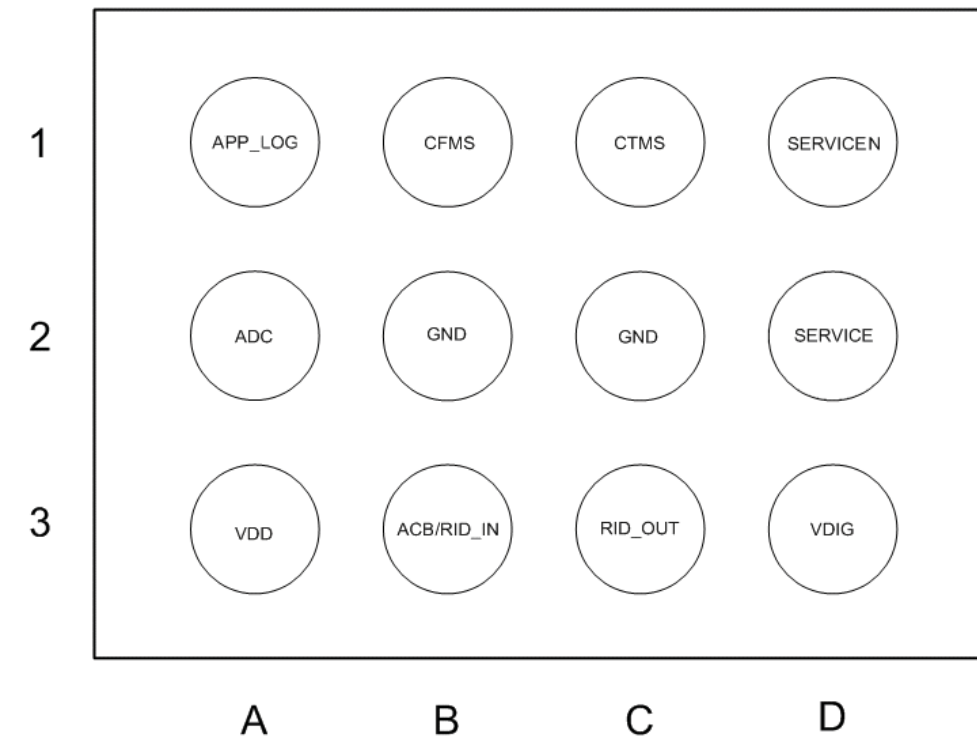


PIN FUNCTION DESCRIPTION

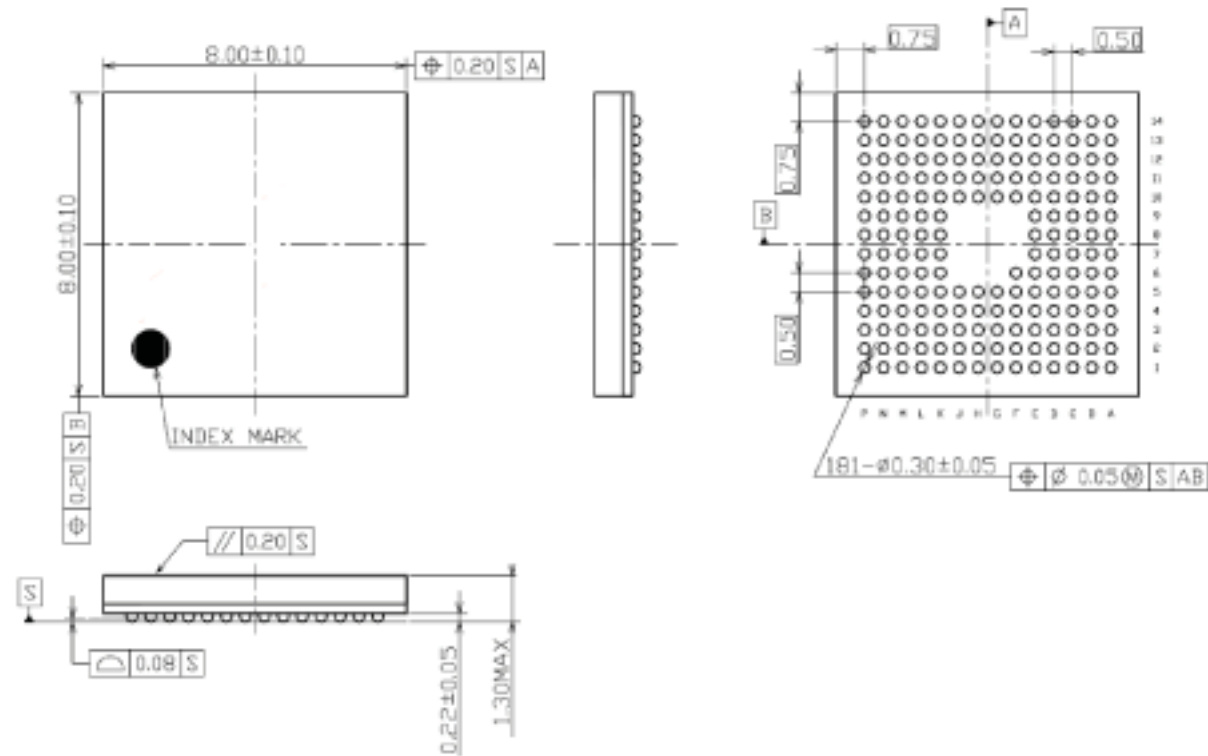
Pin No.	Name	Type	Description
1	EN	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the EN pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.
2	GND	POWER	Ground
3	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
4, 5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to these pins. The two OUT pins must be hardwired to common supply.
6	FLAG	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The FLAG pin goes low when input voltage exceeds OVLO threshold. Since the FLAG pin is open drain functionality, an external pull up resistor to V _{CC} must be added.

N2422 ASIC Baseband 1201-4120

Pin-out, top view; bumps down.



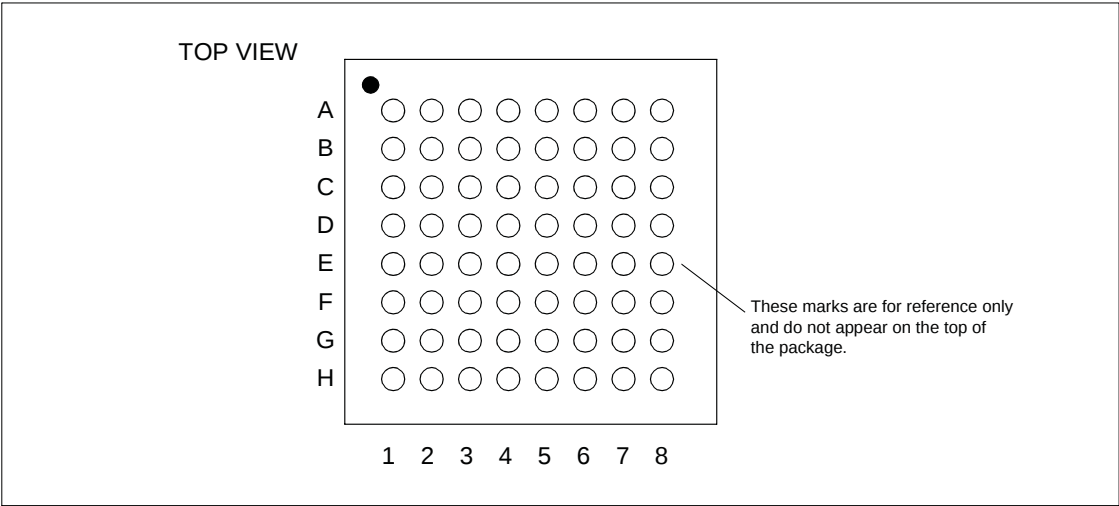
N2500 Companion Chip MP202 1200-4120



Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	GND	D5	I.C	H2	PLLVD	L14	U70_SOUT
A2	GND	D6	SDRVDD	H3	I.C	M1	GND
A3	GND	D7	GND	H4	GND	M2	PM0_SI
A4	PO7	D8	GND	H5	GND	M3	I.C
A5	IOVDD	D9	SDRVDD	H10	GND	M4	PM1_SEN
A6	SPI0_SK	D10	I.C	H11	GND	M5	L1VDD
A7	SPI0_CSZ	D11	LOVDD	H12	I.C	M6	YUV_VS
A8	SPI1_SK	D12	I.C	H13	GIO_P3	M7	YUV_DATA5
A9	SPI1_CSZ	D13	PO1	H14	GIO_P2	M8	YUV_DATA2
A10	IOVDD	D14	PO0	J1	GND	M9	SDRVDD
A11	INT_B	E1	IOVDD	J2	TCLKO	M10	L1VDD
A12	GND	E2	IOVDD	J3	I.C	M11	I.C
A13	GND	E3	L1VDD	J4	SDRVDD	M12	I.C
A14	GND	E4	I.C	J5	I.C	M13	I.C
B1	GND	E5	I.C	J10	I.C	M14	GND
B2	GND	E6	I.C	J11	SDRVDD	N1	GND
B3	LO_DET	E7	GND	J12	I.C	N2	GND
B4	PO6	E8	GND	J13	GIO_P1	N3	PM1_SI
B5	IOVDD	E9	I.C	J14	GIO_P0	N4	PM1_SO
B6	SPI0_SO	E10	I.C	K1	IOVDD	N5	IOVDD
B7	SPI0_SI	E11	L1VDD	K2	IOVDD	N6	YUV_HS
B8	SPI1_SO	E12	L1VDD	K3	L1VDD	N7	YUV_DATA6
B9	SPI1_SI	E13	IOVDD	K4	I.C	N8	YUV_DATA3
B10	IOVDD	E14	IOVDD	K5	I.C	N9	YUV_DATA0
B11	PLLMODE	F1	GND	K6	I.C	N10	IOVDD
B12	I.C	F2	GND	K7	GND	N11	PO2
B13	GND	F3	I.C	K8	GND	N12	I.C
B14	GND	F4	SDRVDD	K9	I.C	N13	GND
C1	GND	F5	I.C	K10	I.C	N14	GND
C2	RESETZ	F6	I.C	K11	L1VDD	P1	GND
C3	L1_DET	F10	I.C	K12	L1VDD	P2	GND
C4	I.C	F11	SDRVDD	K13	IOVDD	P3	GND
C5	L1VDD	F12	I.C	K14	IOVDD	P4	PM1_CLK

N2700 TV Out Graphics Engine 1200-0362

S1D13771 Pinout Diagram



S1D13771 W-CSP 64-pin Pinout Diagram (Top View)

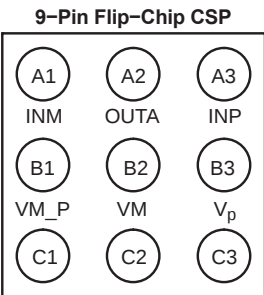
S1D13771 W-CSP 64-pin Pinout (Top View)

	1	2	3	4	5	6	7	8	
A	NC	GPIO3	TE	COREVDD	D/C#	MD2	MD4	NC	A
B	TESTEN	VSS	GPIO_INT	CS#	IOVDD	VSS	MD5	SCANEN	B
C	Reserved	GPIO2	RESET#	VSS	WE#	IOVDD	MD6	MD7	C
D	VSS	GPIO1	IOVDD	CS#SEL	RD#	MD3	IOVDD	COREVDD	D
E	COREVDD	GPIO0	VSS	LCDCS#	MD0	Reserved	COREVDD	VSS	E
F	DACVCC	DACVCC	DACVEE	VSS	MD1	VSS	PLLSS	PLLVD	F
G	DACVEE	DACVEE	VREF	IOVDD	COREVDD	IOVDD	VSS	VCP	G
H	NC	AOUT	VADJ	TEST0	TEST1	VSS	CLKI	NC	H

Note
Pins marked as NC are not used and must be left unconnected. Pins marked as Reserved must be left unconnected, unless otherwise specified.

N3100 IC CS-9 1200-9978

PIN CONNECTIONS



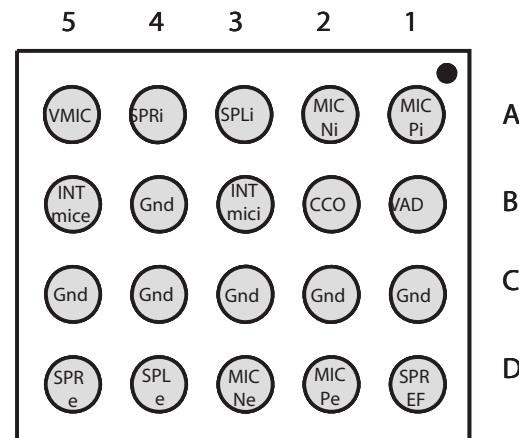
BYPASS OUTB SHUTDOWN
(Top View)

PIN DESCRIPTION

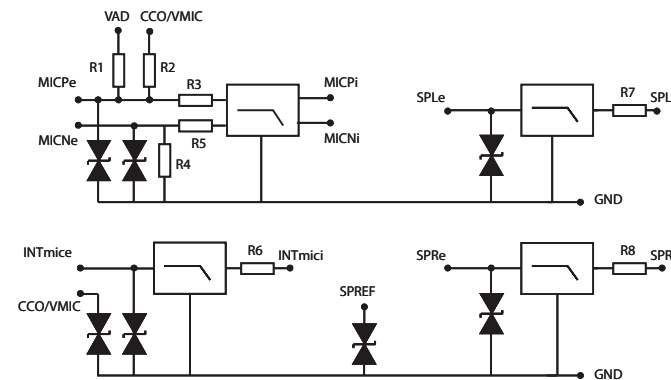
Pin	Type	Symbol	Description
A1	I	INM	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R_f and to the input resistor R_{in} .
A2	O	OUTA	Negative output of the NCP2990. Connected to the load and to the feedback resistor R_f .
A3	I	INP	Positive input of the first amplifier, receives the common mode voltage.
B1	I	VM_P	Power Analog Ground.
B2	I	VM	Core Analog Ground.
B3	I	Vp	Positive analog supply of the cell. Range: 2.2 V–5.5 V.
C1	I	BYPASS	Bypass capacitor pin which provides the common mode voltage ($V_p/2$).
C2	O	OUTB	Positive output of the NCP2990. Connected to the load.
C3	I	SHUTDOWN	The device enters in shutdown mode when a low level is applied on this pin.

N3101 ASIC Tjatte3 CSP20 1200-9978

Pin configuration (Bump side)



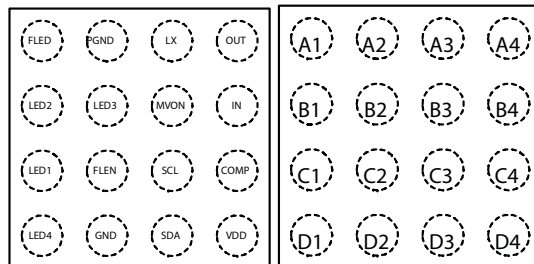
Electrical diagram



N4400 IC Dri MAX8830 ES3 4x4 UCSP

Pin configuration

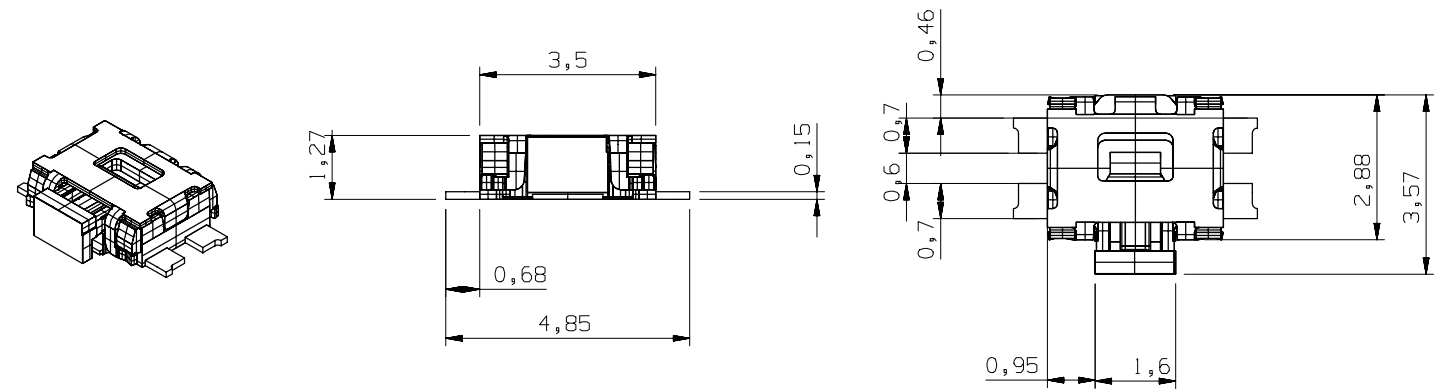
(Top View, Bump Side down)



16-pin 2.5 x 2.5mm UCSP

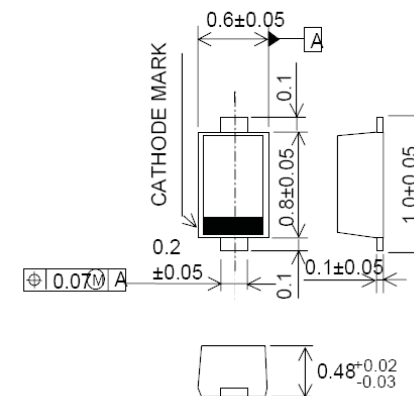
Pin	NAME	FUNCTION
B4	IN	Analog Supply Voltage Input. The input voltage range is 2.7V to 5.5V. Bypass IN to AGND and PGND with a 10µF ceramic capacitor as close to the IC as possible. IN is high impedance during shutdown.
D2	GND	Analog Ground. Connect AGND to PGND
A2	PGND	Power Ground. Connect PGND to AGND and to the input capacitor ground. Also, connect PGND to the PCB ground plane.
C4	COMP	Compensation Input. Connect a TBDkohm resistor and TBDµF ceramic capacitor in series from COMP to AGND for regulator stability.
B3	MVON	Movie On Logic Input. Connect to VDD or drive with logic 1 to enable the Movie Mode. The FLED movie current is set in I ² C registers. Connect to AGND or drive with logic 0 to turn off the Movie Mode. The Movie Mode may also be enabled via the I ² C registers.
C2	FLEN	Flash Enable Logic Input. A transition from logic 0 to logic 1 on FLEN starts the Flash Mode. The flash duration and FLED flash current are set in I ² C registers. The Flash Mode ends when either FLEN transitions back to logic 0 or after the flash duration timer expires (in case FLEN gets stuck high).
C3	SCL	I ² C Clock Input. Data is read on the rising edge of SCL.
D3	SDA	I ² C Data Input. Data is read on the rising edge of SCL.
D4	VDD	Logic Input Supply Voltage. Connect VDD to the logic supply driving SCL, SDA, MVON, and FLEN. Bypass VDD to AGND with a 0.1µF ceramic capacitor.
B2, B1, C1, D1	LED3, LED2, LED1, LED4	LED Current Sink Regulators. Current flowing into these pins is based on the internal I ² C registers. Connect LED _n to the Cathodes of external LED's. LED _n is high impedance during shutdown. If unused, LED _n may be shorted to ground or left floating.
A1	FLED	Flash LED Current Sink Regulator. Current flowing into these pins is based on the internal I ² C registers. Connect FLED to the Cathode of an external Flash LED or LED Module. FLED is high impedance during shutdown. If unused, FLED may be shorted to ground or left floating.
A4	OUT	Regulator Output. Connect OUT to the anodes of the external LED's. Bypass OUT to PGND with a 10µF or larger ceramic capacitor. During shutdown, OUT is one body-diode drop below the input voltage.
A3	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX is internally connected to the drains of the internal MOSFETs. Both MOSFETs are off during shutdown.

S2415, S2424, S2453, S2454 Input Switch 1204-1127

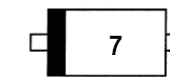


V2200 Zener Diode RKZ223911/1

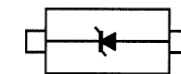
Unit in mm



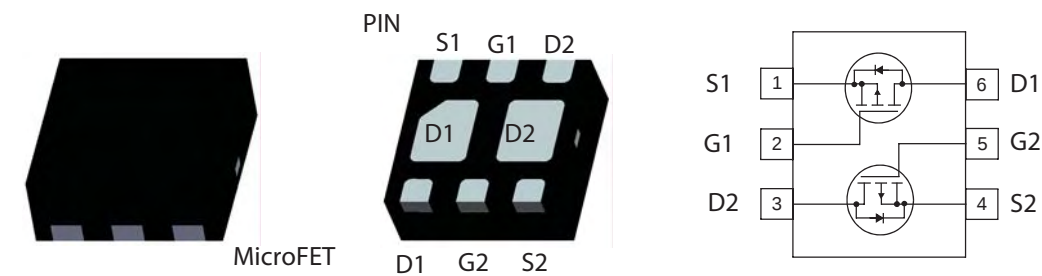
Marking



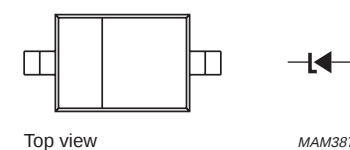
Equivalent Circuit (Top View)



V2202 Trans P-ch FET RYN122910/1



V2412, V2417 Zener Diode Voltage Regulator 15V 5% RKZ223905/2



Top view

MAM387

The marking bar indicates the cathode.

PINNING

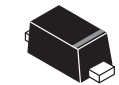
PIN	DESCRIPTION
1	cathode
2	anode

V2414, V2415, V2416 Diode Protection 5, V SOD-923 1201-8440

MARKING DIAGRAM



D = Specific Device Code
M = Date Code

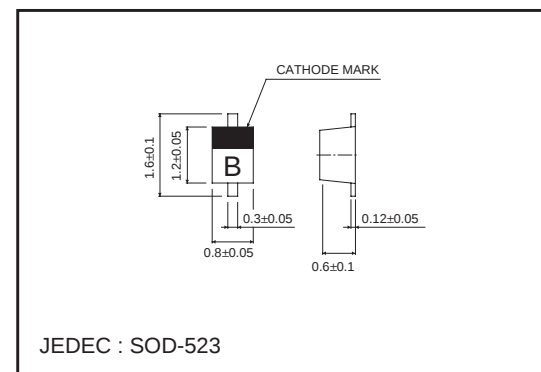


SOD-923
CASE 514AB



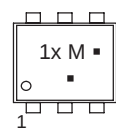
V2470, V4201 Schottky Barrier Diodes 2PIN RKZ123905/1

●External dimensions (Units : mm)



V4203 Trans Array 1200-0320

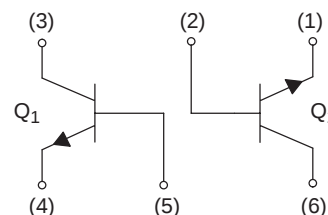
MARKING DIAGRAMS



1x = Device Code
x = G or M
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

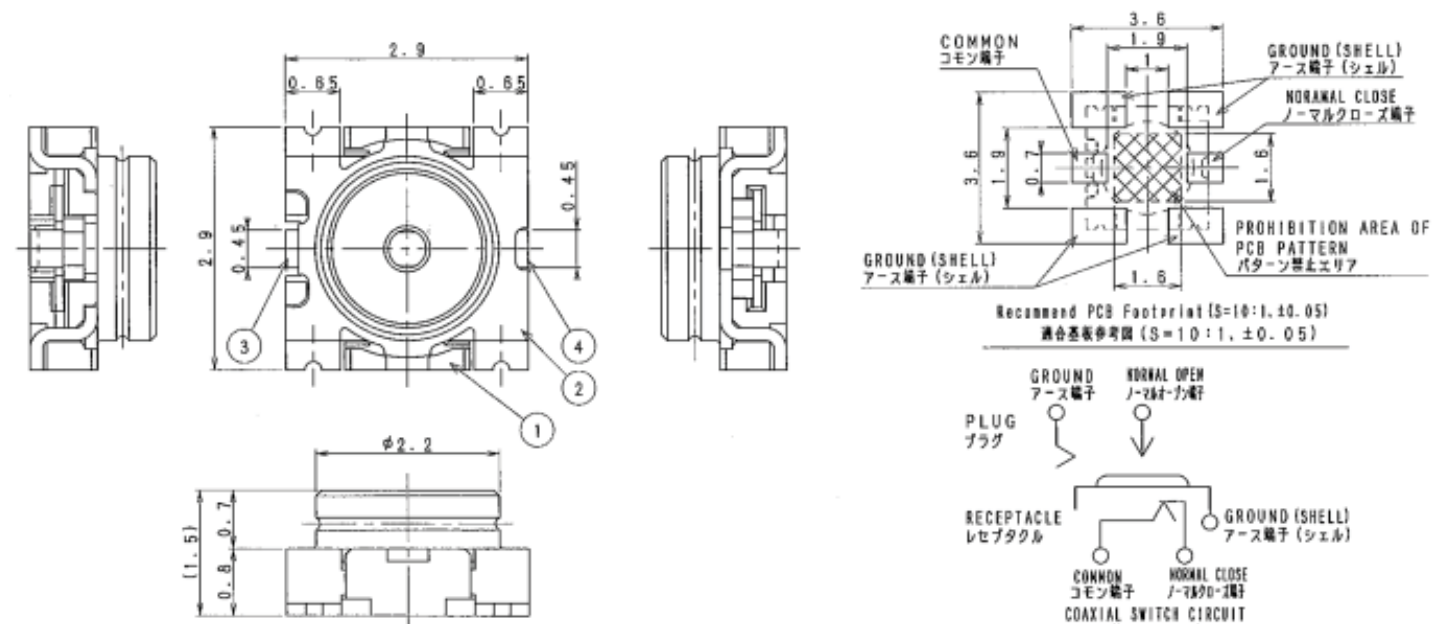


SOT-563
CASE 463A
PLASTIC



BC847CDXV6T1

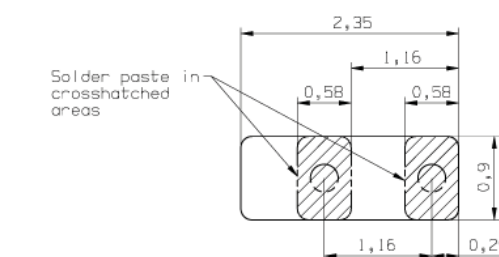
X1200, X1500 RF Probe Contact 6 Pin 1203-9688



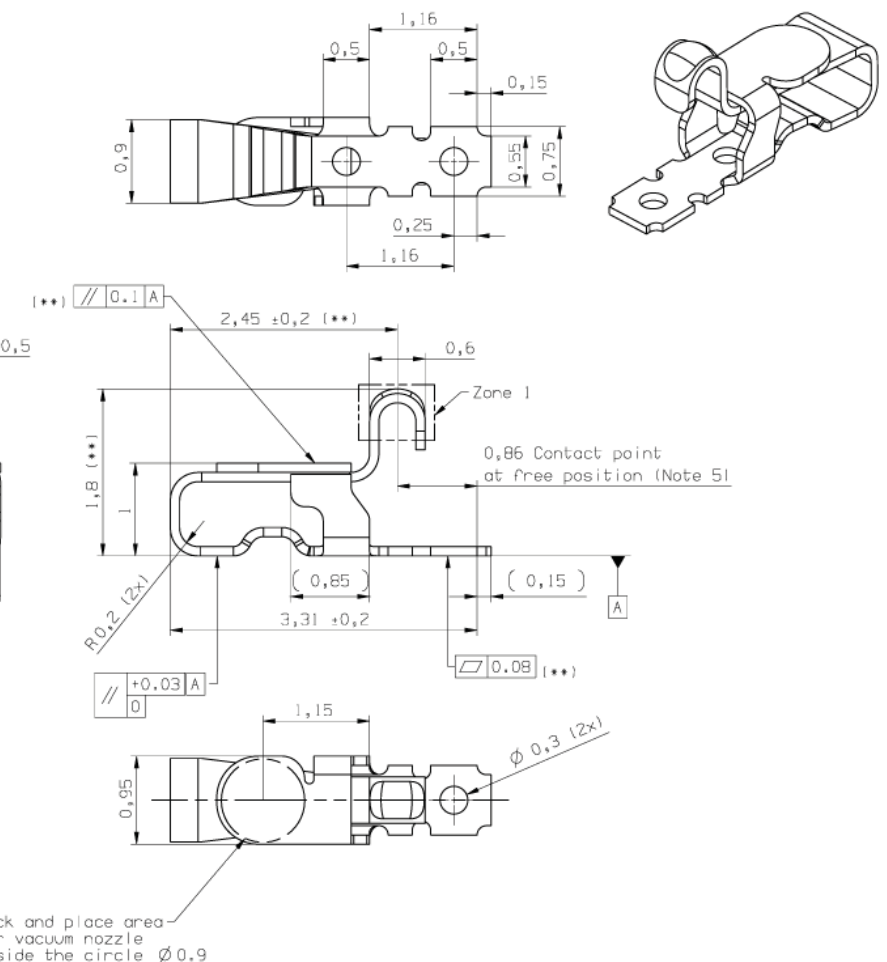
X1210, X1211, X3102, X3103 Conn Leaf Spring 1200-2144

1. Material: Stainless steel.
2. Plating:
MIN 1.3 μ m Nickel underlayer all over.
Gold flash all over.
MIN 0.5 μ m gold plating in Zone 1.
Plating in Zone 1 must be made after bending.
3. Pre-load force: 0.3 - 0.5 N. (**)
4. Force at full compression (1.0 mm height):
0.8 - 1 N. (**)
5. Contact point location:
Uncompressed (1.8 mm height) - 0.86 mm.
Nominal compression (1.2 mm height) - 0.6 mm.
Full compression (1 mm height) - 0.55 mm.
6. The requirements of the Sony Ericsson
Lists of banned and restricted substances
(2/034 01-LXE 108 239) must be fulfilled.
7. Part must meet all constraints after
being subjected to the reflow profile
described in J-STD-020C.
(Peak temperature 260°C)
8. Tyco drawing number C-1857724 and
part number 1857724-4.

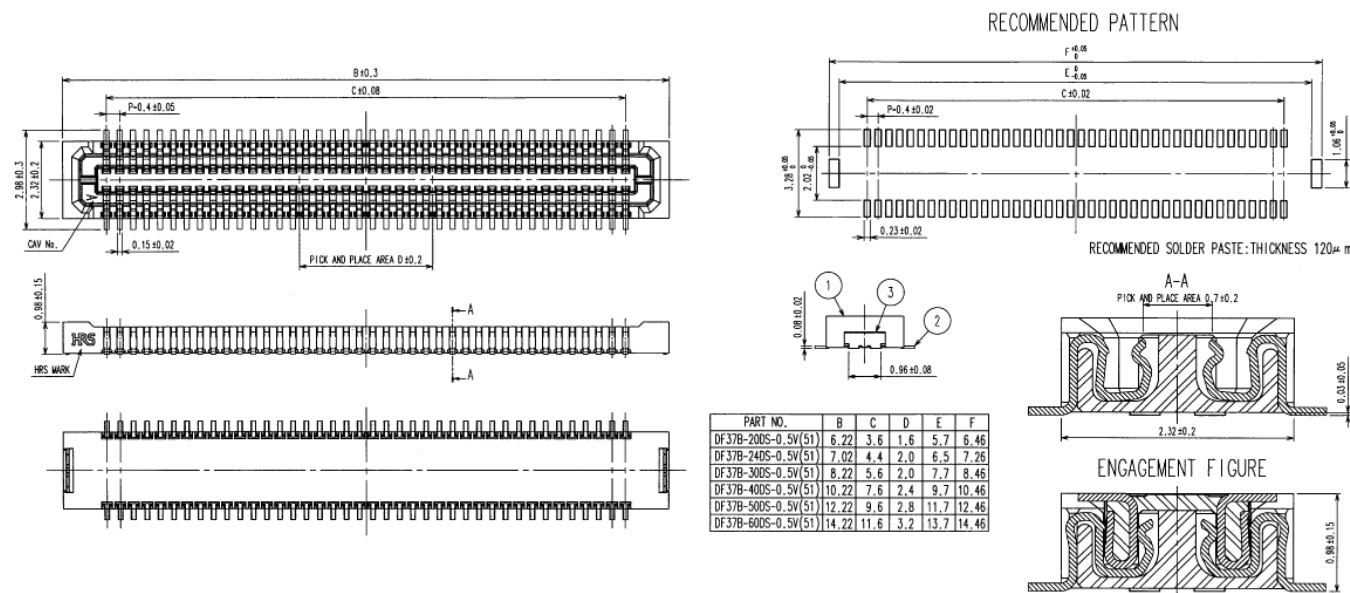
PSA-dimensions marked (**)
Contact forces should also
be measured in PSA



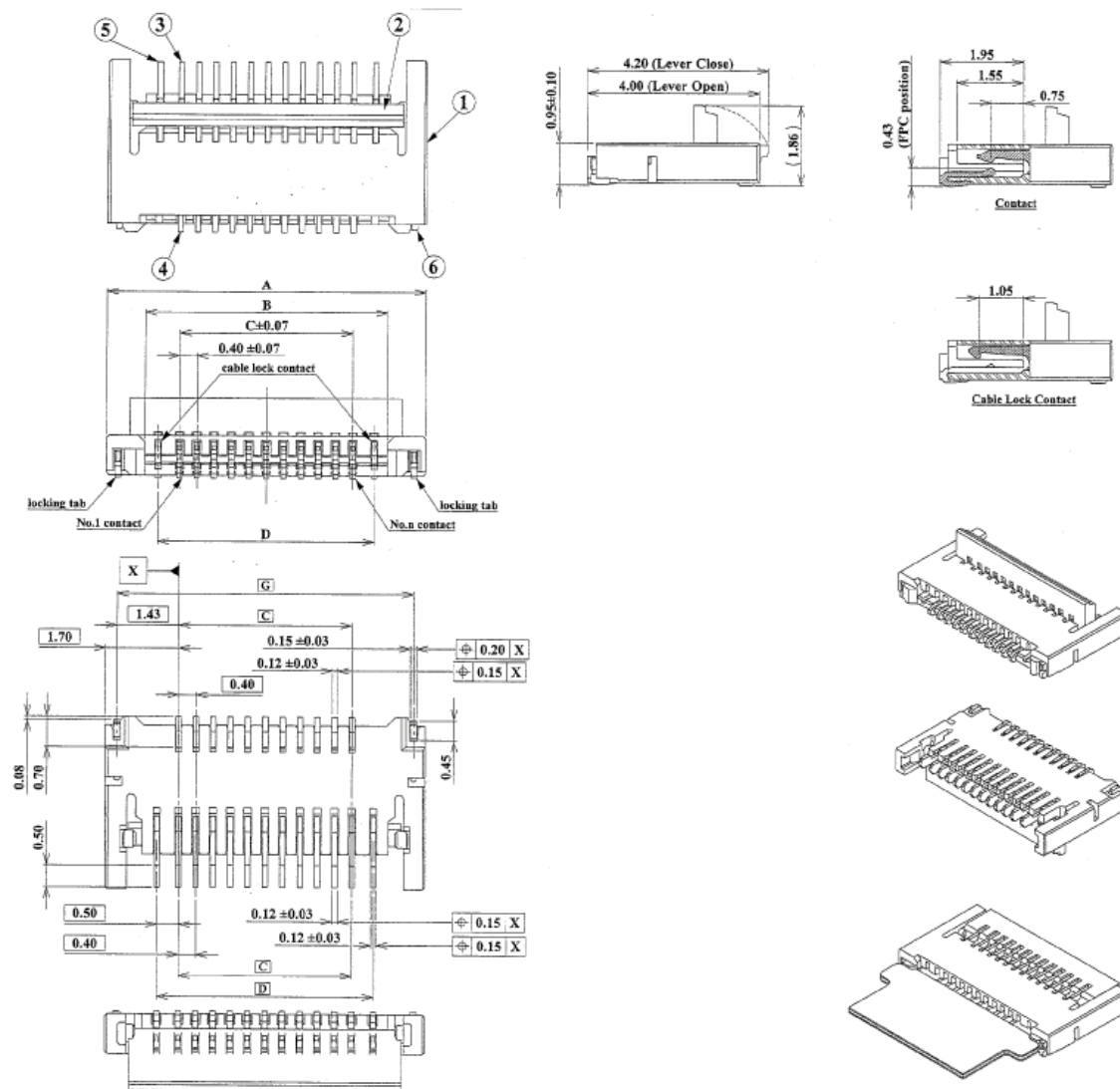
Recommended PWB-layout.
The location of the connectors
bottom holes are indicated
by the circles.



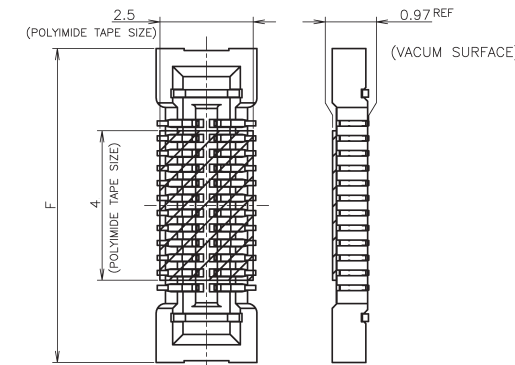
X2410 BtB Receptable 24pin 1208-3264



X4200 100 pin FPC Connector 1204-5252

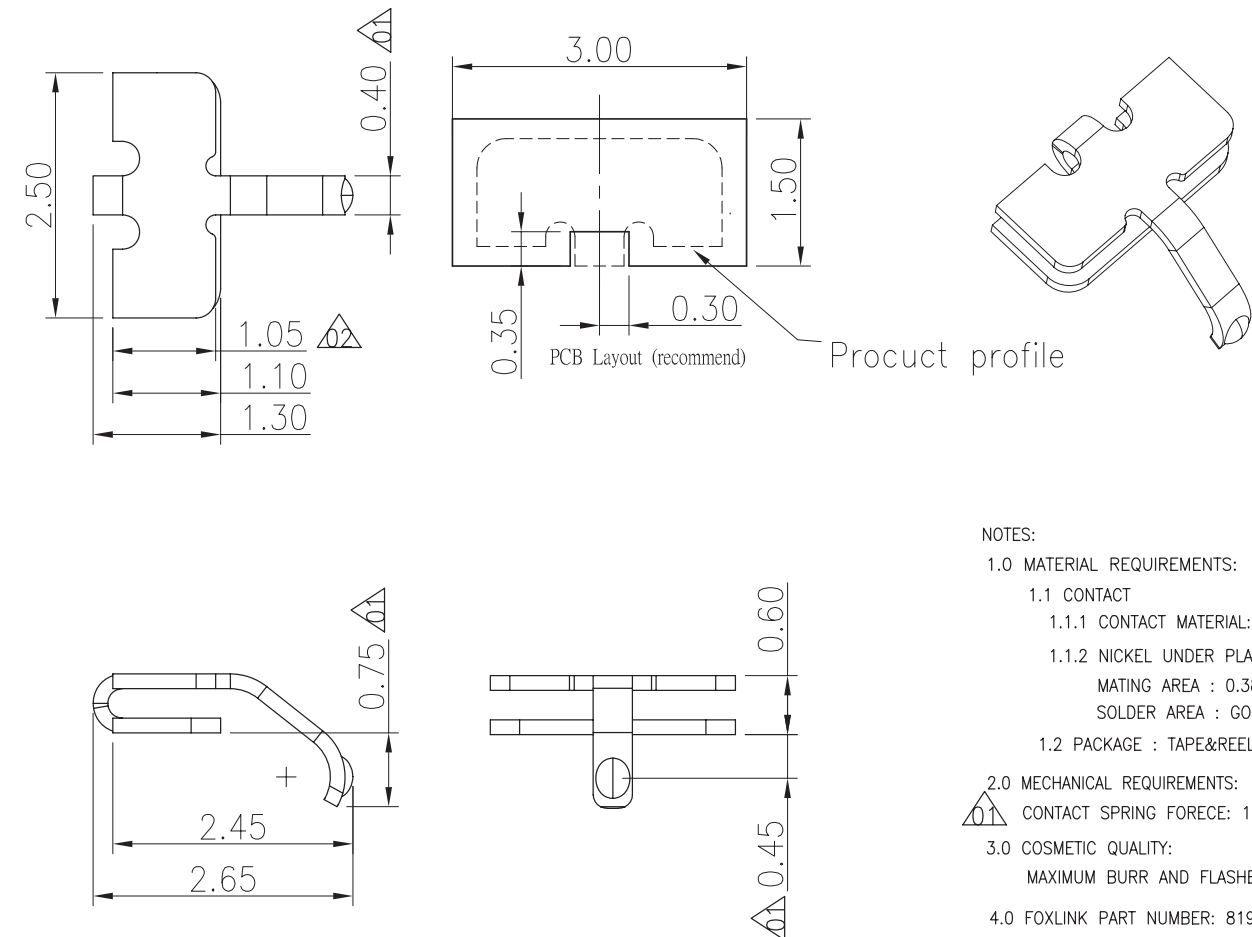


X4300 Conn BtB 30 pin 1200-1733



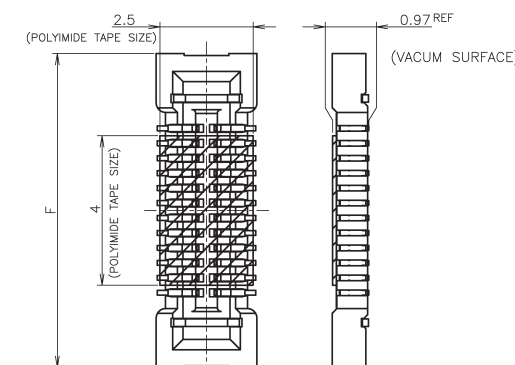
8-1747769-0	38.4	32.4	0.0606	15.6	17.2	19.6	19.9	16.9	14.2	28.4	32	8-2013134-0	80
7-1747769-0	30.4	24.4	0.0546	13.6	15.2	17.6	17.9	14.9	11.5	—	24	7-2013134-0	70
4-1747769-0	30.4	24.4	0.0366	7.6	9.2	11.6	11.9	8.9	11.5	—	24	4-2013134-0	40
3-1747769-0	30.4	24.4	0.0306	5.6	7.2	9.6	9.9	6.9	11.5	—	24	3-2013134-0	30
2-1747769-8	30.4	24.4	0.0294	5.2	6.8	9.2	9.5	6.5	7.5	—	16	2-2013134-8	28
2-1747769-4	22.4	16.4	0.0270	4.4	6.0	8.4	8.7	5.7	7.5	—	16	2-2013134-4	24
2-1747769-2	22.4	16.4	0.0258	4.0	5.6	8.0	8.3	5.3	7.5	—	16	2-2013134-2	22
2-1747769-0	22.4	16.4	0.0246	3.6	5.2	7.6	7.9	4.9	7.5	—	16	2-2013134-0	20
1-1747769-6	22.4	16.4	0.0222	3.6	4.4	6.8	7.1	4.1	7.5	—	16	1-2013134-6	16
REFERENCE													
W/O BAR CODE	P/N	W2	W1	WEIGHT(g)	H	G	F	E	D	C	B	A	QTY/REEL
TAPING P/N													
POS													

X4311, 12, 13, 14, 15 Ground Spring Finger 1 pin 1204-9353



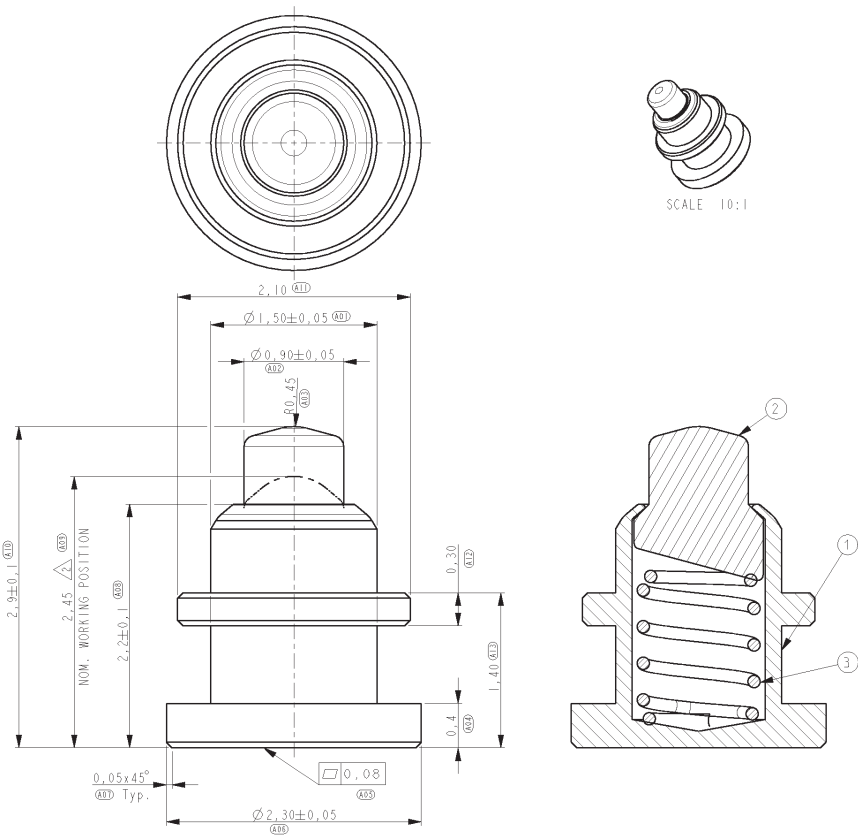
- NOTES:
- MATERIAL REQUIREMENTS:
 - CONTACT
 - CONTACT MATERIAL: Ti-Cu
 - NICKEL UNDER PLATE 2um ALL OVER.
 - MATING AREA : 0.38um Au MIN.
 - SOLDER AREA : GOLD FLASH
 - PACKAGE : TAPE&REEL
 - MECHANICAL REQUIREMENTS:
 - CONTACT SPRING FORCE: 1.4-1.8N
 - COSMETIC QUALITY:
 - MAXIMUM BURR AND FLASHES: 0.03mm
 - FOXLINK PART NUMBER: 819M-1501-SH80

X4400 Conn BtB 24 pin 1201-5197



8-1747769-0	38.4	32.4	0.0606	15.6	17.2	19.6	19.9	16.9	14.2	28.4	32	8-2013134-0	80
7-1747769-0	30.4	24.4	0.0546	13.6	15.2	17.6	17.9	14.9	11.5	—	24	7-2013134-0	70
4-1747769-0	30.4	24.4	0.0366	7.6	9.2	11.6	11.9	8.9	11.5	—	24	4-2013134-0	40
3-1747769-0	30.4	24.4	0.0306	5.6	7.2	9.6	9.9	6.9	11.5	—	24	3-2013134-0	30
2-1747769-8	30.4	24.4	0.0294	5.2	6.8	9.2	9.5	6.5	7.5	—	16	2-2013134-8	28
2-1747769-4	22.4	16.4	0.0270	4.4	6.0	8.4	8.7	5.7	7.5	—	16	2-2013134-4	24
2-1747769-2	22.4	16.4	0.0258	4.0	5.6	8.0	8.3	5.3	7.5	—	16	2-2013134-2	22
2-1747769-0	22.4	16.4	0.0246	3.6	5.2	7.6	7.9	4.9	7.5	—	16	2-2013134-0	20
1-1747769-6	22.4	16.4	0.0222	3.6	4.4	6.8	7.1	4.1	7.5	—	16	1-2013134-6	16
REFERENCE													
W/O BAR CODE	P/N	W2	W1	WEIGHT(g)	H	G	F	E	D	C	B	A	QTY/REEL
TAPING P/N													
POS													

X4410 Pogopin Plug 1pin 1208-0925



NOTES:

△ PLATING
CONTACT AREA: 0.15 μm AU MIN. over 2.0 μm Ni-P MIN.
REMAINDER: 0.10 μm AU MIN. over 1.2 μm Ni-P MIN.

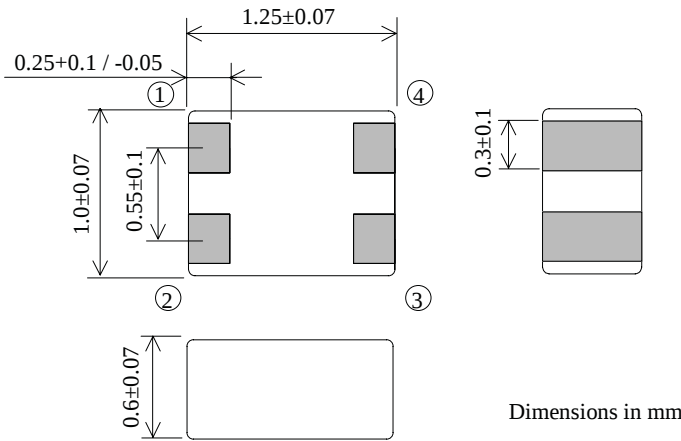
△ CONTACT FORCE: see table

3 Dimensions used for PSA and SPVR studies
to be determined.

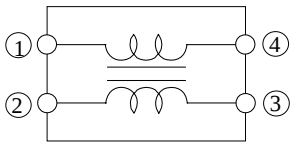
4 PACKAGING: see sheet 2

CONTACT FORCE vs. DEFLECTION (STROKE)			
	LENGTH (mm)	STROKE (mm)	F (N)
INITIAL	2.9	0	-
MIN.	2.75	0.15	0.2
NOMINAL	2.45	0.45	0.6
MAX.	2.35	0.55	0.8
FULL	2.2	0.7	2 MAX.

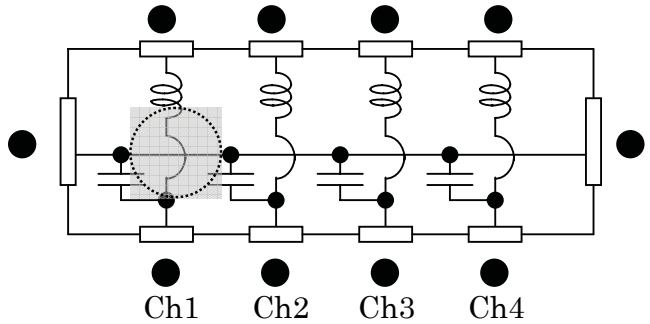
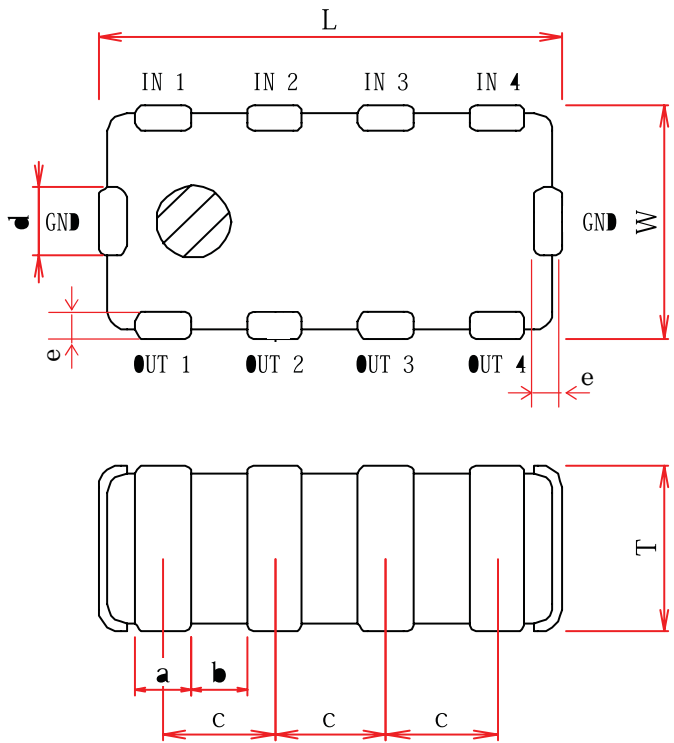
Z2400 Filter 100 Mhz K1210 1201-6833



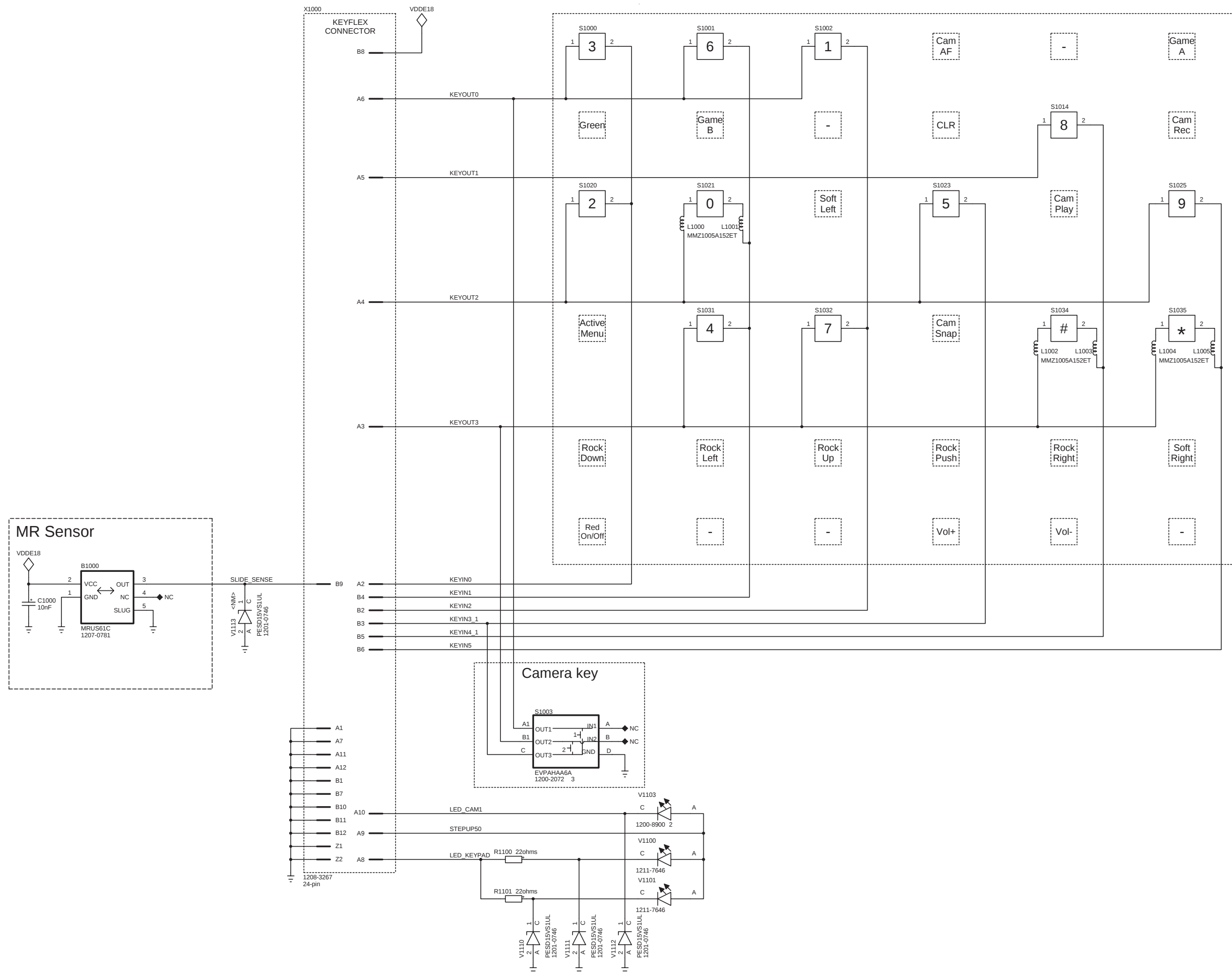
Equivalent circuit



Z4200, Z4201, Z4202 LC Filter REV50148/1



Dimensions [mm]							
L	W	T	a	b	c	d	e
1.6±0.10	0.8±0.10	0.5±0.10	0.175±0.05	0.225±0.05	0.4±0.05	0.175±0.05	0.10±0.10 -0.05



Troubleshooting Software Documentation

Introduction

Using this software you can control most parts and functions of all Sony Ericsson mobile phones. It is a GUI (**G**raphical **U**ser **I**nterface) for the commands implemented in the ITP (**I**ntegrated **T**est **P**rogram). The software communicates with the phone through standard serial communication over a USB/RS232 interface (SEPI).

Note: The Troubleshooting Software application is to be used with the Troubleshooting Manual and the Troubleshooting fixture kit.

The functions in the Troubleshooting Software application are divided into three main sections: **Communication Settings**, **Radio Control** and **Base Band Controls**. These main sections are presented under six different tabs.



All settings and functions are collected under these six main tabs.

Communication Settings

All settings for the communication between the Troubleshooting Software application and the phone are presented under the Communication Settings Tab.

Radio Controls

Note: Some parts of Radio Control functions may not be implemented since they are not supported by the ITP SW.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

All Radio Control Functions implemented in the Troubleshooting Software are presented under the **Tx and Rx** tab. The main radio functions of the mobile phone presented in this tab are:

- GSM radio part
- WCDMA radio part
- Bluetooth radio part

In the GSM and the WCDMA radio control part the following radio functions can be controlled: Transmitter (TX) and Receiver (RX)

In the Bluetooth radio control part only the Transmitter (TX) function is supported.

Base Band Controls

Note: Some parts of Base Band Control functions may not be implemented since they are not supported by the ITP SW.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available for all products.

The functions for Base Band Control are presented under the following four different tabs:

Audio and FM Radio

Used for setting Audio Loop mode and test the functionality of the FM Radio.

Logic

Used to:

- Read out of the ADC channels
- Control or Test of SIM and Memory Stick Card
- Perform of Battery and Current Calibration
- Check Radio and Display temperature
- Etc.

GPIO Manager

Used to control GPIO ports at the Access and Application CPU.

Note: It is very important to follow the GPIO activation sequence according to the Troubleshooting Guide instructions when the GPIO manager is used to avoid Hardware or SW function interruption.

MMI

Used for:

- Main and VGA Camera Tests
- Camera Door Test
- Keyboard Scan Test
- Vibrator Test
- LED and Backlight Tests
- Xenon Flash Test
- Display Test
- Etc.

General

Used to:

- Read out Software and Product Data Information flashed into the phone
- Perform ASIC Revision test
- Perform available Self tests

Equipment Setup

Note: During calibration the accurate voltage from VBATT must be within ± 0.015 V. If this is not fulfilled it will cause a faulty calibration. For more information about recommended power supply units, see the Repair Tool Catalogue in CSPN under the Mechanical level. The Power Supply Channel 1 VBATT must allow reverse current.

Note: Before starting calibration test, the phone must be flashed with ITP Software.

Instructions for Customization of Power Supply Channel 2 DCIO/SEPI Cable

To perform Current Calibration the phone must be powered directly through the system connector. Customize the cable according to following instructions: Take the CST-75 battery charger and cut off the charger according to picture 1. **Length of the cable must be exact 1.3m.** Connect the CST-75 charger **Red** or **White** cable to the **Positive (+) Output** at Power Supply and the **Black** cable to the **Negative (GND) Output** at the Power Supply according to picture 2. Cut off isolation material from inside of the charger plug according to picture 3.

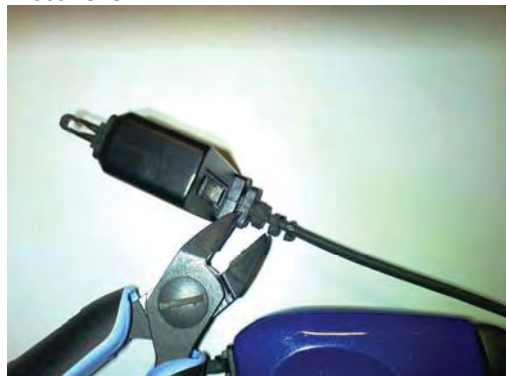
Picture 1



Picture 2



Picture 3



Power Supply Channel 2 DCIO/SEPI Cable Connection Setup

Note: The Power Supply Channel 1 (VBATT) must allow reverse current.

Note: The maximal cable length between the Power Supply Channel 1 VBATT and the dummy battery must not exceed 1m. The cable must have a capacity for at least 16A.

Picture 4



Correct DCIO and SEPI A1 Cable setup when the Troubleshooting Fixture is used.

Picture 5



Correct DCIO and SEPI A1 Cable setup when a Dummy Battery is used.

Picture 6



This setup between DCIO and SEPI A1 Cable is WRONG!

Note: Voltage and Current settings for the Power Supply Channel 1 VBATT and 2 DCIO/SEPI can be found in the Equipment List included in the Product Specific Troubleshooting Manual.

Note: Instructions about the Troubleshooting fixture connections with the External RF connector, Display, SIM Card, Memory Stick Card, Keyboard etc. can be found in Troubleshooting Fixture Connection Instruction included in the Product Specific Troubleshooting Manual.

System Requirements

Note: Before start using the Troubleshooting Software, the phone must be flashed with ITP SW.

The system requirements for running the application are:

- At least a Pentium III 500 MHz, with 128 MB of RAM
- Win2000 or Win XP
- One free USB connector
- USB Computer Cable
- At least 1024x768 display resolution. (1152x864 is recommended.)
- SEPI Drivers must be installed
- SEPI BOX
- SEPI A1 Cable
- Phone Specific Dummy Battery
- Phone Specific TRS Fixture
- CST-75 Charger cable
- One Dual or Two Single Channel Power Supplies

TX and RX - Tab

Communication Functions

Note: Some parts of the Communications functions may not be implemented since they are not supported by ITP Software.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

GSM

GSM Mode Settings

Used for selecting of the GSM radio mode. The following Radio Modes are available:

- TX and RX Switched
- TX and RX Static

Note: In the TX Switched mode all parameters are available (Band, Channel and Power Level). In the TX Static mode the control of Power Level is hidden and the transmitter works with a predefined DAC value. This is done to protect the power amplifier against overheating.

GSM Radio Settings

Used for Channel and Power Level control of the selected GSM Band. The TX and RX frequency value for selected band and channel will be presented in the TX and RX frequency box.

1. Select the desired GSM band. Available options are **GSM 850** (Ch 128...251), **GSM 900** (Ch 1...124), **EGSM 900** (Ch 975...1023), **DCS 1800** (Ch 512...885) and **PCS 1900** (Ch 512...810).
2. Use default value or select desired channel.
3. Use default value or select desired power level.

Note: Any GSM band not used by the Mobile Phone will be unavailable in the GSM Radio Settings.

GSM RSSI measurements

This measurement is only possible to perform when RX Switched mode is selected. Use the Mobile Phone Tester instrument for feeding a signal to the mobile phone's receiver. For Instrument and Phone's settings go to Troubleshooting Manual – GSM Network problems.

1. Select RX Switched Mode.
2. Select desired GSM band and Channel.
3. Go to GSM RSSI Measurements and Start RSSI Test.

Note: The RSSI Test can be performed differently from product to product due to the limited ITP Software support.

WCDMA

Note: Unused WCDMA Bands will not be available in the WCDMA Radio Settings.

Note: For some products the TX and RX WCDMA Channels range can be reduced due to the limited product functionality or Test Instrument limitation. This is done to avoid wrong and incorrect measurement results.

Radio Settings

Used for TX and RX Channels control of the selected WCDMA Band. The TX and RX Channels frequency for selected band will be presented in the TX and RX frequency box.

1. Select the desired WCDMA band. Available options are **Band I** (TX Ch 9612...9888, RX Ch 10562...10838), **BAND II** (TX Ch 9262...9538, RX Ch 9662...9938), **BAND IV** (TX Ch 1312...1513, RX Ch 1537...1738), **BAND V** (TX Ch 4132...4233, RX Ch 4357...4458) and **BAND VIII** (TX Ch 2712...2863, RX Ch 2937...3088)
2. Use default value or select desired TX or RX channel.

Fast select channels

Set High Channel: The High Channel for selected WCDMA Band will be set by the Troubleshooting SW.

Set Mid Channel: The Mid Channel for selected WCDMA Band will be set by the Troubleshooting SW.

Set Low Channel: The Low Channel for selected WCDMA Band will be set by the Troubleshooting SW.

Modes

Max Pwr 23dBm set the Phone to transmit with maximum power at the selected Band and TX Channel. The limit is 23dBm.

Min Pwr Max -50dBm set the Phone to transmit with minimum power at the selected Band and TX Channel. The limit is -50dBm.

Read RSSI set the Phone in RX mode at the selected Band and RX Channel.

Out Pwr level x dBm set the Phone in TX mode at the desired power level value at the selected Band and TX Channel (Power level range to choose is: from -50dBm to 23dBm).

INP/OUT Pwr check set the Phone to transmit with maximum power and switch the receiver On at the selected Band and TX/RX Channel

Reset output set the Phone in WCDMA Off mode.

Rx on

Read measurement read the RSSI and report the result at Phone reported power. This function can only be used when the Receiver is On.

Note: *The RSSI Measurement can be performed differently from product to product due to the limited ITP Software support.*

VCO and VCXO Functions

Note: *These calibrations are only possible to perform when RX static mode is selected.*

Note: *These calibrations may not be possible to implement for all products due to limitations in ITP Software.*

VCO Calibration (TX)

Uses the default values in the TP to adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the TXVCO (measured with an ADC) is within the valid range and the optimal value is chosen. The optimal value is defined as: The CVCO value that gives loop voltages within the limits for both high and low channel and that has the lowest maximum loop voltage.

The optimum value is stored in GDFS.

VCXO Control

Used to fine tune the VCXO to **MCLK** frequency by calibrating the DAC that sets the VCXO control voltage. It is also used to verify the VCXO tuning range. When transmission is in Switched TX mode you are allowed to calibrate the VCXO oscillator controlling the DAC value on the AFC pin.

1. Switch the GSM tester to GSM900, Ch1.
2. Read the stored VCXO value from the GDFS by clicking the "**Read from GD**" button.
3. Start transmitting by clicking the "**TX Switched**" mode button.
4. To apply the VCXO DAC value you set, click the "**Set VCXO**" button.
5. Check your GSM tester.
6. Set the frequency error as close to 0 Hz as possible by using the up/down arrows and then click the "**Set VCXO**" button again.
7. The button "**Mean Value**" sets the value to 1024.
8. When the procedure is finished, click on "**Save VCXO**" button to store the calibrated value in GDFS.

VCO Calibration (RX)

Uses the default values in the TP to adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the RXVCO (measured with an ADC) is within the valid range, and the optimal value is chosen. The optimal value is defined as: The CVCO value that gives loop voltages within the limits for both high and low channel and that has the lowest maximum loop voltage.

The optimum value is stored in GDFS.

Audio and FM Radio - Tab

Audio & Radio Functions

Note: *Some parts of Audio and FM Radio may not be possible to implement for all products due to limitations in ITP Software.*

Note: *There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.*

Audio Loop Test

1. Select desired Audio Loop Test
2. Click "**Apply Audio Loop**" to start the test.
3. To switch off the loop, select **OFF** from **Audio Output** and click "**Apply Audio Loop**".

Audio input:

- **Mic1** is the internal microphone.
- **Aux1** is the input from the system connector.

Loop mode:

- **Analogue**, where the loop is set before and after the AD/DA conversions.
- **Digital/DSP** loop, where the DSP signal processing also affects to the audio signal.
- **CPU/PCM** loop, where the loop is set between the PCM audio signals.
- **Dictaphone** loop.

Audio output:

- **Earphone** is the internal Earpiece speaker of the unit.
- **AUX earphone** connected to the system connector.
- **Loudspeaker** is the internal loudspeaker of the unit.
- **OFF** is used to switch off the currently used Audio Loop.

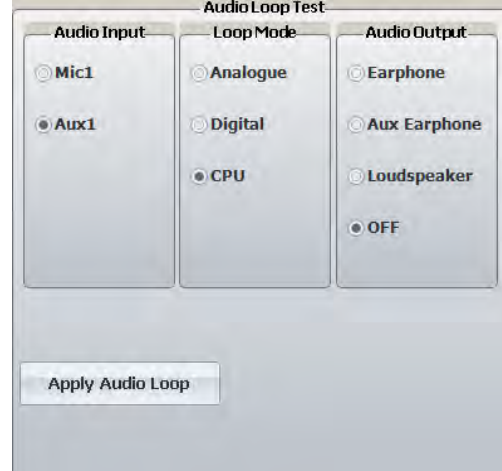
Examples of different Audio Loop Test setups in Fault Trace SW.

Picture 9



K800 Project Setup

Picture 10



K850 Project Setup

Note: Audio output and input pins can be used by disconnecting the blue SEPI connector from the phone after the audio loop has been applied. Now the Portable Handsfree can be connected to the System Connector. After function test operation, disconnect the PHF or external audio device from the System Connector and connect the SEPI cable to proceed with other Audio Loop Tests.

FM Radio

- To activate the FM radio, click at the **Set FM Radio** button.
- To turn off the FM radio, click at the **Turn OFF FM Radio** button.

Audio output

Used for selecting Audio Output from the FM Radio. Most common Audio Outputs for all projects are AUX Stereo (Portable Handsfree, PHF) or Loudspeaker.

Frequency in MHz

Frequency range box for the FM Radio. The frequency value can be selected in two different ways:

- The first one is with up/down spin buttons
- The second one is to type it directly into the Frequency field.

When typing directly into the Frequency field, the Frequency Span should be 100 KHz when changing from one frequency to another. The Frequency Range used in the Troubleshooting Software is from 87.50 MHz to 108.00 MHz.

Examples of different FM Radio Test setups in the Troubleshooting Software

Picture 11



K850 Project FM Radio Setup

Picture 12



K800 Project FM Radio Setup

Logic – Tab

Logic Functions

Note: Some of the Logic functions may not be possible to implement for all products due to limitations in the ITP Software.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

Battery Calibration

Note: To perform this test only Power Supply channel 1 is needed. Make sure that the correct voltage values are set for each test step, otherwise the test will fail.

The Battery Calibration test is similar to the Battery Calibration test performed in the factory environment.

1. Click **1. Battery Calibration**.
2. Click **SET VBATT to 3.2 Volt**.
3. Adjust Power Supply channel 1 (the dummy battery) to 3.2 V.
4. Click **VBAT1**.
5. Click **SET VBATT to 4.1 Volt**.
6. Adjust Power Supply channel 1 to 4.1 V and click **VBAT2**.
7. Adjust Power Supply channel 1 to 3.8 V and click **SET VBATT to 3.8 Volt**.
8. The test result (**Passed** or **Failed**) will now be displayed.

When the measured values are within the limits the calibration will be passed otherwise the test will be failed. The compensation factor will be calculated and stored in the GDFS.

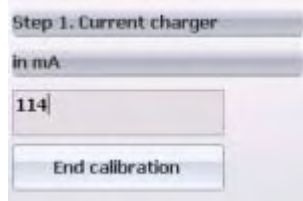
More information about the test limits can be found in the product specific Troubleshooting Manual and in the **Read Limits Table** in the **Battery and Current Calibration Test** document.

Current Calibration

The Current Calibration test is similar to the Current Test for the charging algorithm in the factory environment.

Note: For a correct and accurate result, perform the **Battery Calibration Test** before current calibration. To perform this test you will need both channel 1 and 2 from the Power Supply.

1. Click **2. Current Calibration.**
2. Adjust channel 1 (the dummy battery) to 3.8 V.
3. Click button **SET VBATT to 3.8 Volt.**
4. Note the measured current for channel 2 (the customized charger with SEPI).
5. Type in the measured current (in mA) in the text box.



In this example the current is measured to 114 mA.

6. Press **Enter.**
7. The phone will switch to charging with 800mA. Note the measured current value result at Power Supply Channel 2 DCIO/SEPI.
8. Type the new value in the text box.
9. Press **Enter.**
10. The test result (**Passed** or **Failed**) will now be displayed.

When the measured values are within the limits the calibration will be passed otherwise the test will be failed. The compensation factor will be calculated and stored in the GDFS.

More information about the test limits can be found in the product specific Troubleshooting Manual and in the **Read Limits Table** in the **Battery and Current Calibration Test** document.

ADC Values

1. Select the desired ADC Channel.
2. Click **Read ADC value.**

- The measured value will be presented in both hex and decimal info boxes.
- N/A means that the General Purpose port is not used by this phone or this port is not supported by ITP.
- If a port is missing in the Troubleshooting SW that port is not supported by the ITP SW.

SIM Card Control

This section controls the SIM interface in the phone.

SIM VCC: Voltage for the SIM Card will be activated.

SIM RESET, SIM DATA and **SIM CLOCK:** Activate the Reset, Data and Clock signals for the SIM Card.

SIM Com Test: Checks the communication with the SIM Card.

The test result (**Passed** or **Failed**) will be displayed in the info box.

Note: A SIM card must be inserted and a card reader connected to run this test.

Memory stick test checks the communication with the Memory stick card.

The test result (**Passed** or **Failed**) will be displayed in the info box.

Note: A Memory stick card must be inserted and a Memory card reader connected to run this test.

End Calibration

Ends the calibration and no data will be stored.

Go Idle for 2 sec

The unit will be set to IDLE mode for 2 seconds.

Reboot Phone

IPT command **KILL** will be send and the phone will restart.

Radio Temperature

The value of the Radio Temperature will be displayed in the info box.

Display Temperature

The value of the Display Temperature will be displayed in the info box.

GPIO Manager Functions

Set GPIO port at Access and/or Application CPU to High or Low and Read Out status of the port.

MMI – Tab

Functions

Note: Some parts of MMI functions may not be possible to implement for all products due to limitations in the ITP Software.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

Display Pattern

Activate different test patterns on the display.

LED and Backlight

Activate/Deactivate LEDs and Backlights on the phone.

Misc

Activate/Deactivate tests such as:

- Main Camera Test
- VGA Camera Test

- Camera Door Test
- Vibrator Test
- Keyboard Scan Test
- Etc.

Note: When one test has been deactivated the phone will be restarted.

General – Tab

Functions

Note: Some parts of General functions may not be possible to implement for all products due to limitations in ITP Software.

Note: There are some differences in the user interface depending on the phone project file loaded. Some functions may not be available on all products.

Software Information

This function is used to display the following information stored into the phone:

- ITP version
- IMEI number
- OTP number
- CID number
- PAF status
- Lock Status
- Etc.

Note: The OTP number must match the IMEI number otherwise the IMEI has been changed.

Note: Some of these functions may not be available for all products due to security reasons.

Product Data

This function displays production data stored in the phone, such as:

- First Identification (Serial Nr.)
- PBA Nr.
- PBA Rev.
- DPY Nr. (Sales Unit)
- Etc.

ASIC Revisions

This function displays the types and revisions of the different ASICs. To find out more information about which components are included in this test go to the **ASIC Revision Test** document **included in** the product specific **Troubleshooting Manual**.

Self Test

This function runs available self tests on the Phone.

Fault Trace SW Error Messages

1.

...timeout when reading

Check the following items:

- Connection between Power Supply Channel 2 (DCIO) and SEPI A1 cable (Se picture 4, 5 and 6).
- If the SEPI BOX works properly (The Green LED at the SEPI BOX must be on).
- If the USB cable between SEPI BOX and PC is connected properly.
- If the phone has been flashed with the correct ITP version.
- If VBATT and DCIO Power Supply instruments are on.

2.

...timeout when writing

...timeout when reading

Check if the correct COM Port is selected in Troubleshooting Software - Communication Settings Tab

3.

...Port has not been succesfully opened timeout

- Check if COM Port is connected
- Check if the correct Phone Project File is loaded
- Restart the Troubleshooting Software application and try again

4.

Command failed due to:

.... Error_InvalidParameter, ERR

or

CERR: Error_CommandDoesNotExist, ERR

- Check if the correct Phone Project File is loaded
- Check if the phone has been flashed with the correct ITP version.

Troubleshooting Fixture Setup Instructions

Top part overview of the TRS Fixture, see picture 1.

Picture 1



Bottom part overview of the TRS Fixture, see picture 2.

Picture 2



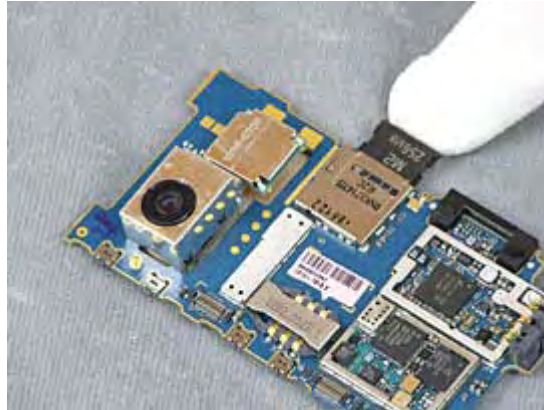
Connect Camera 8MP directly to the PBA if needed, according to picture 3.

Picture 3



Insert Memory Card if needed, according to picture 4.

Picture 4



Insert SIM Card if needed, according to picture 5.

Picture 5



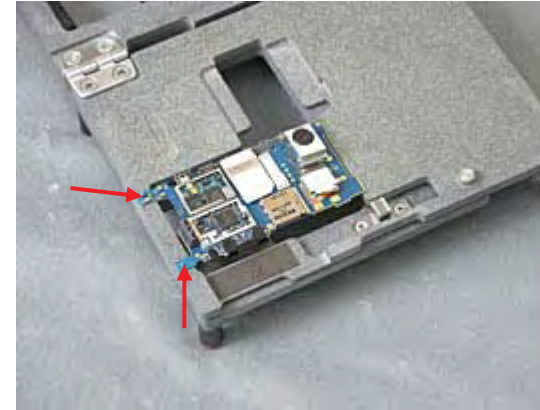
Open the Top part of the TRS Fixture, according to picture 6.

Picture 6



Place the PBA by using the Guide Pin mounted inside the TRS Fixture, according to picture 7.

Picture 7



Connect the Numeric Key Foil with the Keyboard directly to the PBA if needed, according to picture 8.

Picture 8



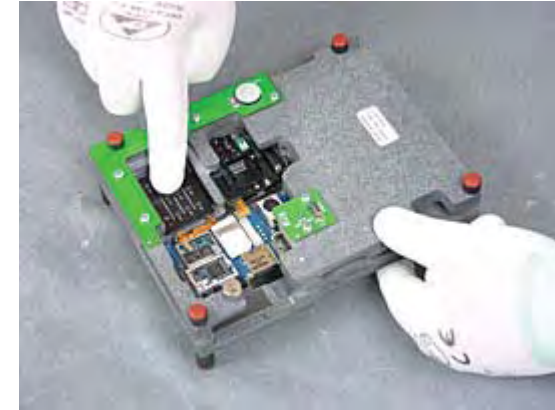
Connect the Flash Complete directly to the PBA if needed, according to picture 9.

Picture 9



Close the Top part of the TRS Fixture according to picture 10.

Picture 10



Open the Bottom part of the TRS Fixture, according to pictures 11 and 12.

Picture 11



Picture 12



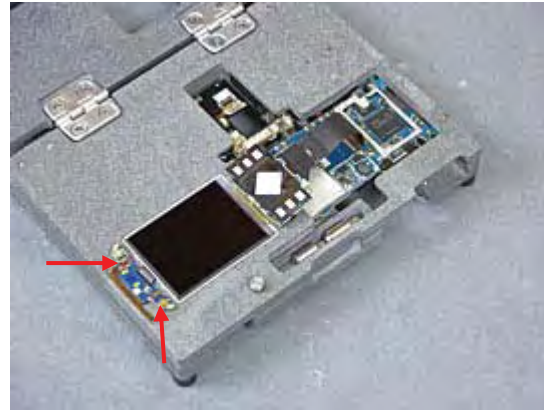
When the Display or Navigation Keyboard is in use then use the PBA Key Flex Flip, Display and Slider FPC Assy, mounted according to pictures 13 and 14.

Picture 13



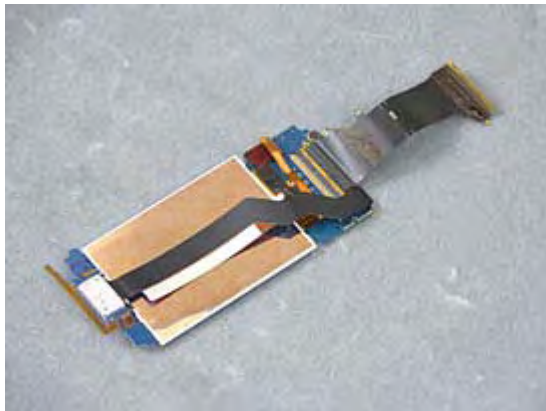
Place the PBA Key Flex Flip and Display by using the Guide Pin inside the Display holder, according to picture 16.

Picture 16



Close the Bottom part of the TRS Fixture, according to pictures 17 and 18.

Picture 14



Picture 17



Connect the Slider FPC Assy to the PBA, according to picture 15.

Picture 15

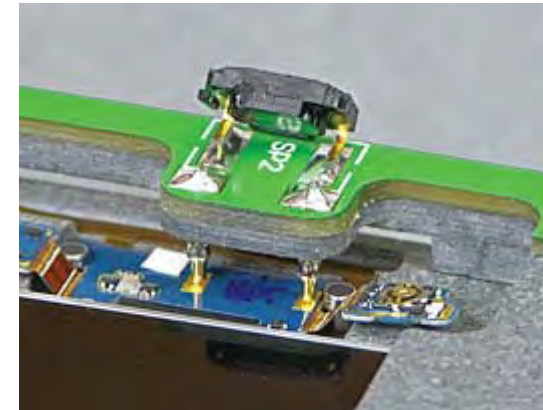


Picture 18



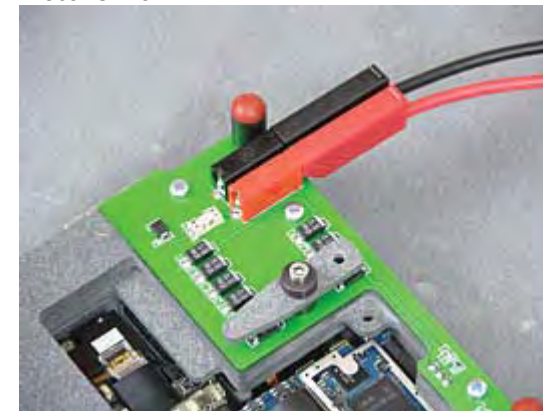
Check that the Ear Speaker is connected properly to the PBA Key Flex Flip, see picture 19.

Picture 19



Connect Power Supply Channel 1 (VBATT) Black and Red Lab Plugs to the TRS Fixture according to picture 20.

Picture 20



Connect the Power Supply Channel 2 Cable (DCIO/SEPI), according to picture 21.

Picture 21



Secure the DCIO/SEPI Cable by using the locking screw, according to picture 22.

Picture 22



Connect SMK RF Probe to the X1200 RF Switch if needed, according to picture 23.

Picture 23



Secure the SMK RF Probe with the RF Probe locking device, according to picture 24.

Picture 24



Connect SMK RF Probe to the X1500 RF Switch if needed, according to picture 25.

Picture 25



Connect the Customized FM Radio Cable, according to Step 1 and 2.

Step 1:

Connect the Black Lab Plug to the TRS Fixture GND input, according to picture 27.

Picture 27



Step 2:

Connect the Hands-Free (PHF) connector to the Phone system connector (X2405), according to picture 28.

Picture 28



Secure the SMK RF Probe with the RF Probe locking device, according to picture 26.

Picture 26



Please see picture 29 for the final Customized FM Radio Cable connection setup with the TRS Fixture.

Picture 29



The PIN marked with the GND text on the Top part of the TRS Fixture can be used as MP TRS Fixture GND or grounding for the oscilloscope probe, see picture 30.

Picture 30



The PIN marked with the GND text on the Bottom part of the TRS Fixture can be used as MP TRS Fixture GND or grounding for the oscilloscope probe, see picture 31.

Picture 31

