



# **IBM** Field Engineering Theory of Operation

**1052 Adapter and 2150 Console**

## PREFACE

This manual describes the operation of the IBM 1052 Printer-Keyboard Adapter for the IBM System/360. The adapter is assumed to be connected to the computer through a multiplexor channel.

Introductory material in the first chapter describes the data flow and control of the adapter. The functional units chapter describes the clock, translators, registers, and controls. The theory of operation chapter presents the circuit details, by operation, in positive logic form.

This manual is written to engineering change level 254147. Future engineering changes may alter the logic operations. Prior knowledge of the multiplexor

channel and the IBM 1052 Printer-Keyboard is assumed.

The Field Engineering Instruction-Maintenance Manual, IBM 1052 Keyboard Printer, Form 225-3179, may be used as supplementary reference material. (Descriptions of the mechanical functions of the keyboard and printer presented in Form 225-3179 are valid for the 1052 adapter; however, the descriptions of operations were written for the IBM 1050 Data Communications System, and do not apply to the 1052 adapter.) Descriptions of the 1052 operations for the 1052 adapter are included herein.

### MAJOR REVISION (May 1966)

This manual, Form Y22-2808-0, is a major revision of the preceding edition, Form 223-2808-0. This revision applies to the new reduced function printer and updates the manual to engineering change level 254151. This change makes the sequencing of the read/write clock in the control unit dependent on the printer's mechanical cycle, eliminates the tab, backspace, and line-feed operations, and forces the printer to space in the event an operator tries to shift the printer to the same case the type head is in.

In addition, information on the 2150 console has been added as a separate section following the 1052 adapter information. The two sections are indexed separately.

### MINOR REVISION (Feb 1967)

This is a minor revision of publications Form Y22-2808-0 incorporating FES S23-4034-0 dated 7/21/66, affecting Contents page, illustrations, and pages 34, 61, 62, and 70.

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This is a minor revision of Y22-2808-1 incorporating changes released in FE Supplement Y27-2208, affecting contents page and pages 5, 6, 9, 10, 23 through 30, 33 through 36, 47, 48, and 53 through 69. Other minor changes are indicated by revision bars on pages 33 and 52.

A form is provided at the back of this publication for reader's comments. If the form has been removed, comments may be addressed to: IBM Systems Development Division, Product Publications, Dept. 520, Neighborhood Road, Bldg 960-1, Kingston, N.Y., 12401

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## ABBREVIATIONS

AC	Alternate Coding	EOB	End-of-Block	Oper	Operational
ACR	Automatic Carrier Return	EOL	End-of-Line	PB	Push Button (key)
ALD	Automated Logic Diagram			ROCP	Remote Operator Control Panel
Altn	Alternate	Funct	Function	Rst	Reset
Attn	Attention	Gen	General	Sel	Select
Aux	Auxiliary Magnet	ICR	Inhibit Carrier Return	Serv	Service
		Init	Initial	SS	Singleshot
BCD	Binary Coded Decimal	Intlk	Interlock	Tgr	Trigger
CE	Customer Engineer	I/O	Input/Output	T/R	Tilt/Rotate
Ch	Channel	LC	Lower Case	UC	Upper Case
Chk	Check	LF	Line Feed	Xlat	Translate
Cmd	Command	Lth	Latch		
CR	Carrier Return	MD	Maintenance Diagram		
CU	Control Unit				
Disc	Disconnect				

- Control unit
- 1052 Printer-Keyboard

The 1052 operator's console consists of an I/O Control Unit and an I/O Printer Keyboard. The printer is a modified IBM Selectric<sup>®</sup> typewriter, and the keyboard is a modified IBM 024/026 alphabetic keyboard. The printer and keyboard are mechanically and electrically independent, although they are both housed under the same cover.

The console provides two basic functions: facilities through which the operator can enter data under control of a monitor program; and facilities for printing data also under control of a monitor program. The console is available as an integrated central processing unit (CPU) feature for the IBM System/360 Models 40, 50, 65, 67, and 75, and is also available in the form of the 2150 free standing console for the Models 50, 65, 67 and 75. When provided as an integrated feature, the console is operated on a multiplex or selector channel; when provided as the 2150, the console is operated on a selector channel. Power and cooling for the integrated feature is a function of the host computer, while the free standing console provides its own power and cooling. The 1052 is standard on the 2044 CPU, IBM System/360 Model 44.

The console I/O device is handled like other I/O devices in that it is connected to a system through either a multiplex or a selector channel and an I/O control unit. When attached to a multiplex channel operating in multiplex mode, the console control unit receives or transmits one 8-bit byte of data from or to the channel, and then releases the channel to service other I/O devices. This byte mode of operation continues until the end of data transmission. With this mode of operation the console control unit releases the channel within the microsecond range for each byte of data. When attached to a selector channel, operating in burst mode, the I/O control unit monopolizes the channel facilities until the completion of the data transfer. (Write commands with a byte count of one release the selector channel in the microsecond range.)

INTERFACE LINES

- Channel interface
- 1052 interface

The I/O control unit has two sets of interface lines: those connecting the control unit with the channel and those connecting the control unit with the 1052.

Channel Interface

The interface lines between the channel and the control unit are:

<u>From Channel to CU</u>	<u>Bus Lines</u>	<u>From CU to Channel</u>
Bus Out Bit P		Bus In Bit P
Bus Out Bit 0		Bus In Bit 0
Bus Out Bit 1		Bus In Bit 1
Bus Out Bit 2		Bus In Bit 2
Bus Out Bit 3		Bus In Bit 3
Bus Out Bit 4		Bus In Bit 4
Bus Out Bit 5		Bus In Bit 5
Bus Out Bit 6		Bus In Bit 6
Bus Out Bit 7		Bus In Bit 7
	<u>Tag Lines</u>	
Address Out		Address In
Command Out		Status In
Service Out		Service In
	<u>Scan Control Lines</u>	
Select Out		Select In
Hold Out		Request In
Suppress Out		
	<u>Interlock Lines</u>	
Operational Out		Operational In
	<u>Metering-Lines</u>	
Metering-Out		Metering-In
Clock-Out		

The bus lines carry the data, sense, status, and address bytes between the channel and the console control unit. The tag lines identify the bytes on the bus lines. The scan control lines control the sequence of priority of the various control units on the channel. The interlock lines provide the controls for connecting to and disconnecting from the channel.

Channel Interface Signal Sequence

One of the most important assumptions of this manual is the prior knowledge of the signal sequence of the channels to which the control unit can be attached. For the purpose of review, the following material is presented at this time.

Initial Selection

Figure 1 illustrates the sequence of interface signals for a complete write operation on a multiplex channel. The channel itself begins the initial selection sequence. The channel raises the address-out and hold-out lines to all the control units connected

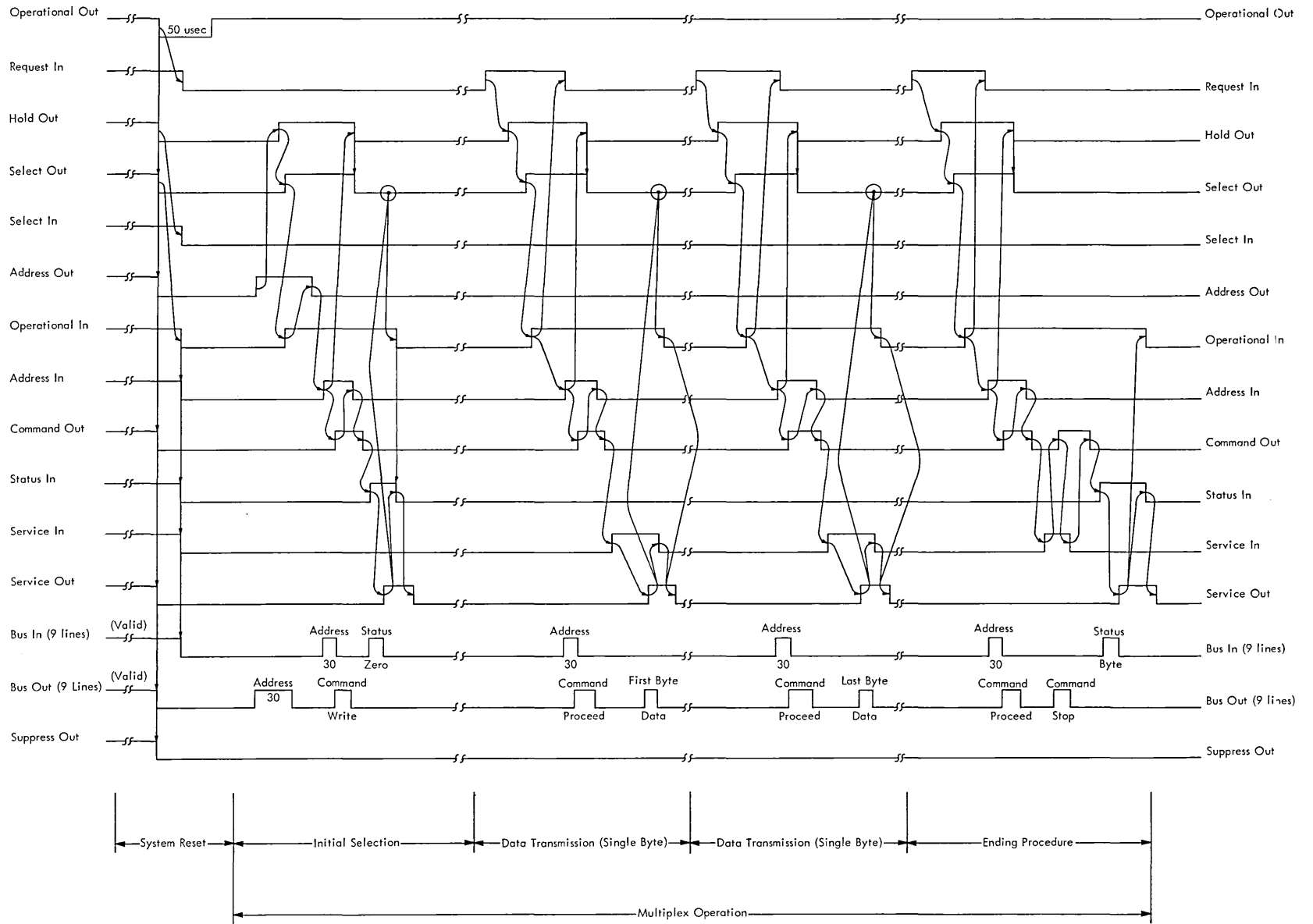


FIGURE 1. CHANNEL INTERFACE SIGNAL SEQUENCE

to the interface. The select-out line is raised to the control unit with the highest priority. The address byte designating a particular control unit is placed on the bus-out lines at the same time. The first control unit compares the address byte against its own address, and if the two do not match, the control unit propagates select-out to the control unit with the next lowest priority. This attempt at address matching continues at each control unit in turn until the control unit whose address is on the bus-out lines is reached.

When the designated control unit makes the address match, the control unit raises the operational-in line to the channel. The channel recognizes the operational-in, and drops the address-out line. When the control unit recognizes that the address-out line has been dropped, it raises the address-in line to the channel, and places its own address on the bus-in lines.

The channel accepts the address byte and the address-in tag line, and in response raises the command-out line and drops the select-out and hold-out lines. The channel also places a command byte on the bus-out lines at this time. For the sake of illustration, we are considering the command byte to indicate a write-inhibit carrier return (ICR) command.

The control unit reacts to the command-out line from the channel by dropping the address-in line and the channel then drops command-out in response to the dropped address-in line. Now the control unit raises the status-in line to the channel, indicating to the channel that the control unit has a status byte to send. The channel responds to the status-in line with service out, indicating the acceptance of the status byte. When the service-out line comes up, the control unit drops the operational-in line and the status-in line, and the channel in turn drops the service-out line. The initial selection sequence is complete.

#### Data Service

The sequence of signals during the data transfer is begun by the control unit raising the request-in line to the channel. The control unit raises request-in automatically for the first data byte following the initial selection sequence. The channel replies to the request-in with the hold-out and select-out lines. The address-out line is not raised by the channel at this time, because this is not the initial selection sequence. Channel has already established the fact (during initial selection) that it is in communication with this particular control unit. Therefore, as soon as the control unit recognizes the hold-out and select-out lines, it raises the operational-in line to the channel, and then raises the address-in line to the channel and places its own address on the bus-in lines.

The channel responds with command-out at this time. During the initial selection sequence, the

channel placed a command byte on the bus-out lines at the same time that it raised the command-out line. During the data transfer sequence, however, the bits on the bus-out lines are all zeros, with the exception of the parity bit. The command-out line rising at this time during the data transfer sequence, with the command byte bits set to zeros, indicates "proceed" to the control unit.

The control unit, in response to the command-out line from the channel, drops the address-in line, and the channel in turn drops the command-out line. The control unit reacts to the dropping of the command-out line by raising the service-in line. This indicates to the channel that the control unit is now ready for a data byte. The channel places the data byte on the bus-out lines, and raises the service-out line to the control unit. The control unit receives both the data byte and the service-out line, and in turn drops the service-in and operational-in lines. At this point the data transfer sequence is complete. When the 1052 has finished printing the character, the control unit raises the request-in line to begin the next data transfer sequence to get the next character from the channel.

#### End Sequence

The data transfer sequences continue until all of the characters to be sent by the channel have been received by the control unit. When the control unit raises the request-in line, requesting another character, and all of the characters have been sent, the channel begins the ending sequence. The sequences of the request-in, select-out, and hold-out lines are as previously described. The control unit again brings up operational-in in response to the hold-out and select-out lines, and sends the address-in line and the address byte in to the channel. Channel again responds with command out, indicating proceed, and the control unit replies with service in, indicating that the control unit is ready for the data byte. The channel, however, replies with command out instead of service out. Command out coming up in response to the service-in line indicates "stop" to the control unit.

When the control unit recognizes the stop indication, it drops the service-in line, and indicates to the channel that it is going to send status to the channel by raising the status-in line. If the channel is able to accept the status byte at this time, it indicates this by raising the service-out line to the control unit. When the control unit receives the service-out reply from the channel in response to the status-in line, the operation is complete, and the operational-in line is dropped. The I/O control unit is finished with the full write operation, and is free to be used for another operation by the channel.

The write ICR command was considered here because it is a typical sequence. All other signal sequences may be treated as variations of these basic initial selection, data transfer, and ending sequences.

## 1052 Interface

The 1052 interface lines are:

<u>From CU to 1052</u>	<u>From 1052 to CU</u>
T1	Keyboard BCD 1
T2	Keyboard BCD 2
R1	Keyboard BCD 4
R2	Keyboard BCD 8
R2A	Keyboard BCD A
R5	Keyboard BCD B
Cycle Clutch	Keyboard BCD C
Space	Keyboard Strobe
	End of Forms Contact
	RH Margin
	1052 Busy
Carrier Return-Line Feed	1052 Not Busy
Upper Case Shift	Request PB N/O, N/C
Lower Case Shift	Ready PB
Lock Keyboard	Not Ready PB

The first six lines to the 1052 energize the tilt/rotate magnets, and the seventh energizes the cycle clutch magnet. The next four lines energize the function magnets, and the last line operates the keyboard restore magnets to lock the keys.

The first seven lines from the 1052 to the control unit are from the keyboard bail contacts, providing the BCD coding for each key. The eighth line provides an indication to the control unit that a BCD bit configuration has been set up in the bail contacts, and that these contacts are to be sampled. The end of forms contact line signals the control unit when the 1052 has run out of paper.

The tenth line from the 1052 to the control unit signals the control unit when the 1052 carrier has reached the end of the writing line. The control unit then causes the carrier to return to the left-hand margin.

The 1052 busy line indicates to the control unit that the printer is taking a mechanical cycle. This line is energized by the printer whenever the printer shifts, spaces, prints or performs a carriage return, and sets a busy latch in the control unit.

The 1052 not busy line is activated by the printer near the end of its mechanical cycle, and resets the busy latch in the control unit. The last three lines are activated by the ready, not ready, and request pushbuttons mounted on the cover to the right of the carrier return key.

## COMMANDS

- Seven valid commands: test I/O, sense, control no-op, control alarm, write-ACR, write-ICR, read.

The I/O control unit decodes commands from the channel and indicates the acceptance or rejection of the command to the channel. If the command is accepted by the control unit, and requires a printer output (write), the control unit requests data from the channel. The control unit receives the data as a byte consisting of 8 bits plus a parity bit. This 8-bit byte is translated into a tilt/rotate code to pick the proper tilt/rotate magnets in the printer for a printable character, or into a function code to pick the proper function magnet in the printer.

If the command is accepted by the control unit, and requires the operator to enter data (read), the operator keys in the desired character or printer function. The control unit receives the data from the keyboard one byte at a time, each byte consisting of 6 bits plus a parity bit. This data is translated into an 8-bit-plus-parity byte for subsequent transfer to the channel. The control unit requests service from the channel and places the character on the bus-in lines. When the channel accepts the data byte, the character is printed on the printer, or the printer function is performed. No commands (other than read and write) accepted by the control unit require the direct participation of the I/O device.

On the multiplexor channel, read, write, and sense require an initial selection sequence, and then the console control unit disconnects from the channel. Each byte of data transmitted or received by the console control unit requires the console control unit to first transmit its address and then request service from the channel. Upon acknowledgement of the request by the channel, the console control unit again disconnects from the channel. This procedure continues until data transmission is ended.

### Read

Upon acceptance of the read command, the keyboard is unlocked and the proceed light is lit. The proceed light indicates that the operator may key in a character. When the operator keys in a character, it is parity checked (6 bits plus parity) from the keyboard, translated to an 8-bit byte, and set into the data register. The console control unit then requests service from the channel. When the channel accepts the data byte the proceed light is extinguished, the keyboard is locked, the character is translated to a tilt/rotate or function code, and the printer either prints the character or performs the function. The keyboard is unlocked, and the proceed light is again turned on. This procedure continues until a termination is indicated.



A read command may be terminated in one of three ways: byte count equals zero at the channel, end-of-block (EOB) signal given by the keyboard operator, or a cancel signal given by the keyboard operator. The EOB signal is issued by the operator holding down the alternate coding key while operating the numeric 5 key. The EOB signal is used to indicate the end of a block of data. The cancel signal is issued by the operator holding down the alternate coding key while operating the numeric 0 key. The cancel signal is used to indicate an operator error in the message, and the entire message must be retransmitted.

When the control unit detects any of the above terminating signals, it locks the keyboard (which stays locked until a new read command is issued), turns off the proceed light, initiates a carrier-return operation, and sends a channel-end status to the channel. The unit exception status bit is sent with the channel end if the termination was accomplished by the cancel signal. When the carrier is returned to the left-hand margin, the control unit requests service from the channel to present a status byte consisting of device end. The unit check status bit sent with channel end or device end indicates one or more of the following conditions: BCD parity error from the keyboard, no mechanical cycle of the printer, or an error between the BCD keyboard output and the output of the printer translator.

#### Write

There are two write commands available: write-auto carrier return, and write-inhibit carrier return. Write-auto carrier return automatically returns the carrier to the left margin at the end of the write operation. Write-inhibit carrier return does not cause the carrier to return at the end of the write operation.

#### Write-ACR

Upon acceptance of the write command the control unit disconnects from the channel. The control unit then requests service from the channel for each data byte, and disconnects after each data byte. When the stop signal is presented by the channel, the control unit sends channel-end status, and disconnects from the channel. When the carrier is returned to the left margin, the control unit signals for a device-end interrupt. Device-end status is sent when the channel responds.

#### Write-ICR

This command proceeds the same as write-ACR, except that upon receipt of the stop signal the control

unit transmits both channel-end and device-end in one status byte.

#### Test I/O

If the Test I/O command reaches the control unit and no outstanding status bits are present, a zero status byte is returned to the channel.

If status information is pending, all status bits present (except busy, when caused by channel end, device end, attention, or status stacked) are transmitted to the channel.

#### Control No-Op

The control No-Op command is a control immediate. Channel-end and device-end status are transmitted together in the initial selection sequence.

#### Control Alarm

The control alarm command is a control immediate. This command activates an alarm for approximately two seconds. Channel end and device end are transmitted during the initial selection status. Control alarm commands should not be issued at intervals of less than five seconds.

#### Sense

The sense command transmits one 8-bit byte plus parity to the channel. This byte consists of the contents of the sense triggers. After this data transfer, a final status byte consisting of channel end and device end is sent to the channel. The control unit does not disconnect from a multiplex channel between transmission of the sense byte and final status (forced burst mode operation).

#### CONTROL UNIT PRIORITY

- Determined at time of installation
- Pluggable

The priority of the console control unit is not necessarily dictated by the physical placement of the control unit on the I/O interface. The console control unit can be plugged to receive either select out or select in as the scanning line. The priority of the scanning line is set at the time of installation. The control unit provides the option of connecting its selection logic in series on either the select-out or the select-in line. Ascending order priority from the channel can be established on the select-out line, and the remaining control units can maintain a descending order priority from the channel on the select-in line. See Figure 2.

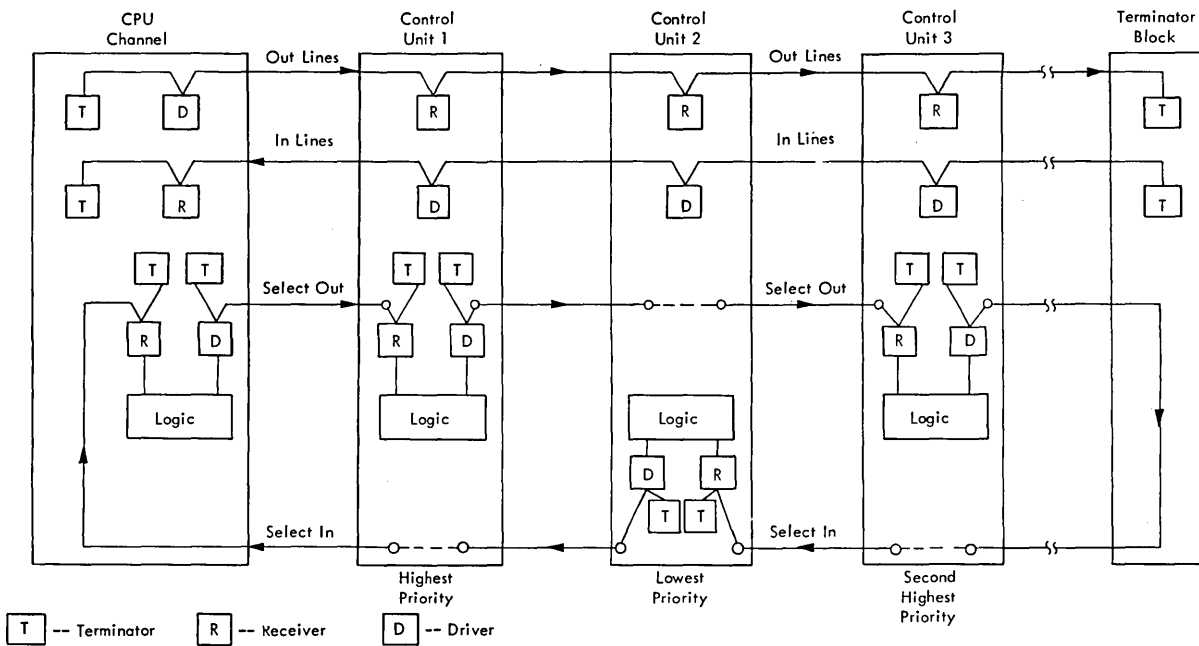


FIGURE 2. I/O INTERFACE INTERCONNECTIONS

Plugging locations for the select-out bypass card are as follows:

Model	Board Location
65A	01ED1-B6
65B	01EB1-B6
67	01ED1-B6
75A	02AD4-B6
75B	02BA1-B6
2150	01AB1-B6

NOTE: The equivalent card position is not used for intermediate systems. For these systems refer to logic page PG011 for priority wiring.

#### DATA FLOW

- Figure MD-1 illustrates both data flow and control.
- Data flow path from data register to printer is the same for both read and write.

#### Controls

The interface controls govern the sequence of signals the console control unit sends to the channel on the inbound tag and selection-control lines. The interface controls are acted upon by both the active and inactive states of the out-bound tag and selection-control lines. They are also acted upon by the command decoder, the command register, and the address compare circuits.

The address and command bytes are received from the channel on the bus-out lines. The address byte

is compared against a fixed address plugged within the console control unit to determine whether the address byte is that of the console control unit. The command decoder decodes the command byte to determine whether the command is one of the seven acceptable to the control unit, and to determine just which of the seven commands it is.

#### Write Data Path

Data bytes are received on the bus-out lines during a write operation. Each data byte is checked for parity when it is taken from the bus-out lines, and the parity bit is then dropped. The 8-bit byte is stored in the data register by the data register controls. The contents of the data register are then analyzed by the function decoder to determine whether the character in the data register is a function character or a printable character.

If the data register contains a printable character, that character is translated (by the 8-bit to tilt/rotate (printer) translator) from the 8-bit code to the tilt/rotate code.

#### Read Data Path

The keyboard generates data and function bytes in a 6-bit-plus-parity code during a read operation. The output of the keyboard is powered, parity checked, and fed to the BCD-to-8-bit (keyboard) translator. The keyboard translator translates the BCD code to the 8-bit code, and the data register controls store the 8-bit character in the data register. (Figure 3 illustrates the translation of the keyboard code and

6-Bit Code	Lower Case		Upper Case	
	Keyboard Print Function	8-Bit Code	Keyboard Print Function	8-Bit Code
BA8421		01234567		01234567
000000	Space	01000000	Space	01000000
000001	1	11110001	=	01111110
000010	2	11110010	<	01001100
000011	3	11110011	;	01111111
000100	4	11110100	:	01110100
000101	5	11110101	%	01101100
000110	6	11110110	'	01111101
000111	7	11110111	>	01101111
001000	8	11111000	*	01011100
001001	9	11111001	(	01001101
001010	0	11110000	)	01011101
001011	#	01111011	"	01001111
010000	@	01111100	ç	01101110
010001	/	01100001	?	01100011
010010	s	10100010	S	11100010
010011	t	10100011	T	11100011
010100	u	10100100	U	11100100
010101	v	10100101	V	11100101
010110	w	10100110	W	11100110
010111	x	10100111	X	11100111
011000	y	10101000	Y	11101000
011001	z	10101001	Z	11101001
011011	,	01101011	l	01101011
100000	-	01100000	-	01110010
100001	j	10010001	J	11010001

6-Bit Code	Lower Case		Upper Case	
	Keyboard Print Function	8-Bit Code	Keyboard Print Function	8-Bit Code
BA8421		01234567		01234567
100010	k	10010010	K	11010010
100011	l	10010011	L	11010011
100100	m	10010100	M	11010100
100101	n	10010101	N	11010101
100110	o	10010110	O	11010110
100111	p	10010111	P	11010111
101000	q	10011000	Q	11011000
101001	r	10011001	R	11011001
101011	\$	01011011	!	01011011
101101	New Line	00010101	New Line	00010101
110000	&	01010000	+	01001110
110001	a	10000001	A	11000001
110010	b	10000010	B	11000010
110011	c	10000011	C	11000011
110100	d	10000100	D	11000100
110101	e	10000101	E	11000101
110110	f	10000110	F	11000110
110111	g	10000111	G	11000111
111000	h	10001000	H	11001000
111001	i	10001001	I	11001001
111011	.	01001011	⌋	01001011
001110	Up-Shift			
111110	Down-Shift			

FIGURE 3. 1052 KEYBOARD CODE TRANSLATION AND PRINTER OUTPUT

the corresponding printer output.) At this point the interface controls request service from the channel.

When the channel responds, the data byte is gated to the bus-in lines through the parity generator. The parity generator inserts P bits as required to make the byte on the bus-in lines odd parity. The byte is sent to the printer at the same time it is sent to the bus-in lines. The character path to the printer from the data register is the same for both read and write.

#### Address-In, Sense, and Status Bytes

The address generator is gated to the bus-in lines during those I/O interface signal sequences requiring the control unit to send its own address in to the

channel. Because the parity bit is plugged along with the rest of the bits in the address generator, the output of the address generator is not passed through the parity generator.

The output of the sense-bit latches is gated to the bus-in lines during the execution of a sense command. This byte is passed through the parity generator because the bit structure of the byte varies, and the parity bit must be inserted as needed. The output of the status triggers is gated to the bus-in lines during an initial selection sequence and during an ending sequence. Correct parity must also be generated for the status byte because the structure of the status byte is also variable.

- Data register
- Read/write clock
- Printer translator
- Keyboard translator
- Shift controls
- Function decoder
- 1052 Printer-Keyboard

DATA REGISTER

- Used for Read Command
- Used for Both Write Commands

The data register itself is composed of eight latches, one for each of the bit lines 0 through 7. Each latch has three possible set and reset lines. Figure 4 illustrates the input and output controls for the data register.

Write Operation

One group of set lines for the eight latches comes from the bus-out lines from the channel. These lines are AND'ed with SS 1, not CE mode, and not busy or stop to set the data byte on the bus-out lines into the data register. The function decode circuits activate the function line at SS 2 time if the character in the data register is a function character. SS 2, write command, and not busy, sets cycle time.

Cycle time gates either the function decoder output (function character in the data register) to energize a function magnet in the printer, or the 8-bit-to-tilt/rotate (printer) translator output (printable character in the data register) to energize the tilt/rotate and cycle clutch magnets in the printer. Cycle time also sets the printer busy latch when SS 2 times out.

The 1052 busy line, energized by the printer, sets the busy latch in the control unit which will reset cycle time. 1052 not busy, energized by the printer near the completion of its cycle, resets the busy latch in the control unit which will set SS 4 if the end of line latch is not on.

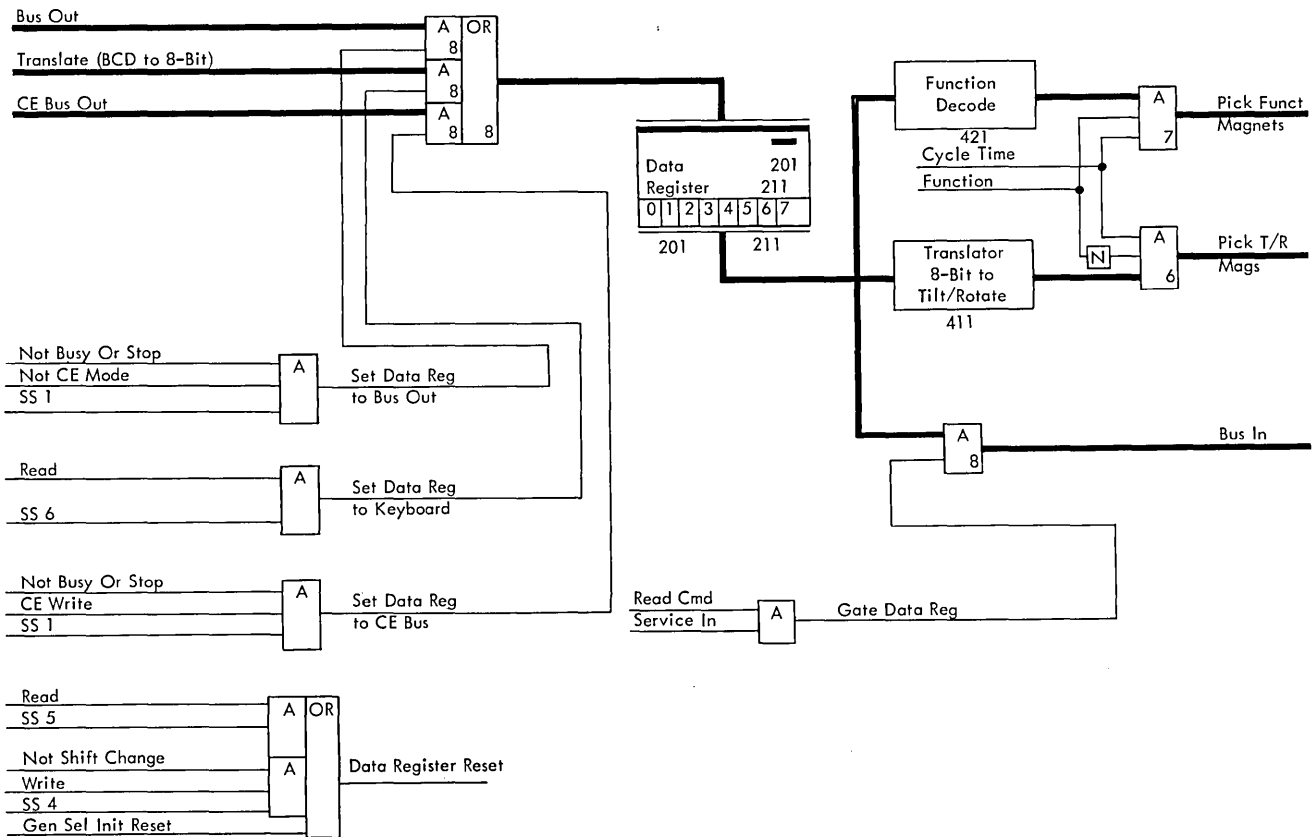


FIGURE 4. DATA REGISTER, INPUT AND OUTPUT CONTROLS

SS 4 AND's with write and not shift change to reset the data register. The not shift change line indicates that the character in the data register did not require case-shifting the printer. If the data register had contained an upper case character and the printer had been in lower case, or vice versa, the character would have been held in the data register while the printer was shifted. The clock would have run through SS 4 during the shifting, but the data register would not have been reset, the reset having been blocked by the not shift change line being inactive. When the shift is complete, the clock is again started at SS 1. The data register cannot be set again because the printer busy latch is on when the clock starts again at SS 1. When the clock runs through SS 4 the second time, the data register is reset.

### Read Operation

A second group of set lines for the data register latches comes from the BCD-to-8-bit (keyboard) translator.

For a read operation, SS 5 of the read/write clock is turned on by the AND condition of read, not busy, and keyboard strobe. The data register is reset during SS 5 time and the 28 ms delay provides time for the keyboard contacts to settle down. When SS 5 times out, it fires SS 6 if the carrier is not being returned to the left-hand margin. SS 6 AND's with read to gate the translated keyboard output into the data register.

SS 6 and not right-hand margin, resets the carriage return latch. Printer busy is reset by SS 6 and not shift change. When SS 6 times out, SS 7 fires. SS 7 requests service from the channel by raising the request-in line to the channel, indicating that the console control unit has a data byte ready for transfer to the channel.

When the channel responds, and connections are established between the channel and the console control unit, the service-in line (AND'ed with read command) gates the output of the data register to the bus-in lines. The channel responds to service-in with service-out, and the console control unit AND's service response with read command to turn on cycle time of the read/write clock. From this point the data byte proceeds to the printer exactly as described for the write operation. The data byte has now been placed on the bus-in lines and has also been printed.

### READ/WRITE CLOCK

- Used for read and write commands.
- Used to return carrier, space, and shift.

- Start and stop points vary with operation.

The read/write clock is used for three of the seven valid commands accepted by the control unit: read, write-auto carrier return, and write-inhibit carrier return. The clock is stepped sequentially from SS 1 through SS 7 for both of the write commands, but starts at SS 5 for the read command.

During the data transfer sequence of a write command, the control unit activates the service response line (Figure 5) by AND'ing the service-in and service-out tag lines. Service response then starts the clock by firing SS 1. SS 1 gates the data byte on the bus-out lines into the data register (Figure 3).

SS 2 fires when SS 1 times out. SS 2 controls the lower case/upper case latch and the shift change latch (Figure 8). The outputs of SS 2 and cycle time are overlapped, but the duration of SS 2 is only 200 nanoseconds whereas the duration of cycle time is controlled by the printer. The printer busy latch is set by cycle time and not SS 2. Cycle time is AND'ed with the outputs of the function decoder and the printer translator to pick the function or the tilt/rotate and cycle clutch magnets in the 1052 (Figures 6 and 9).

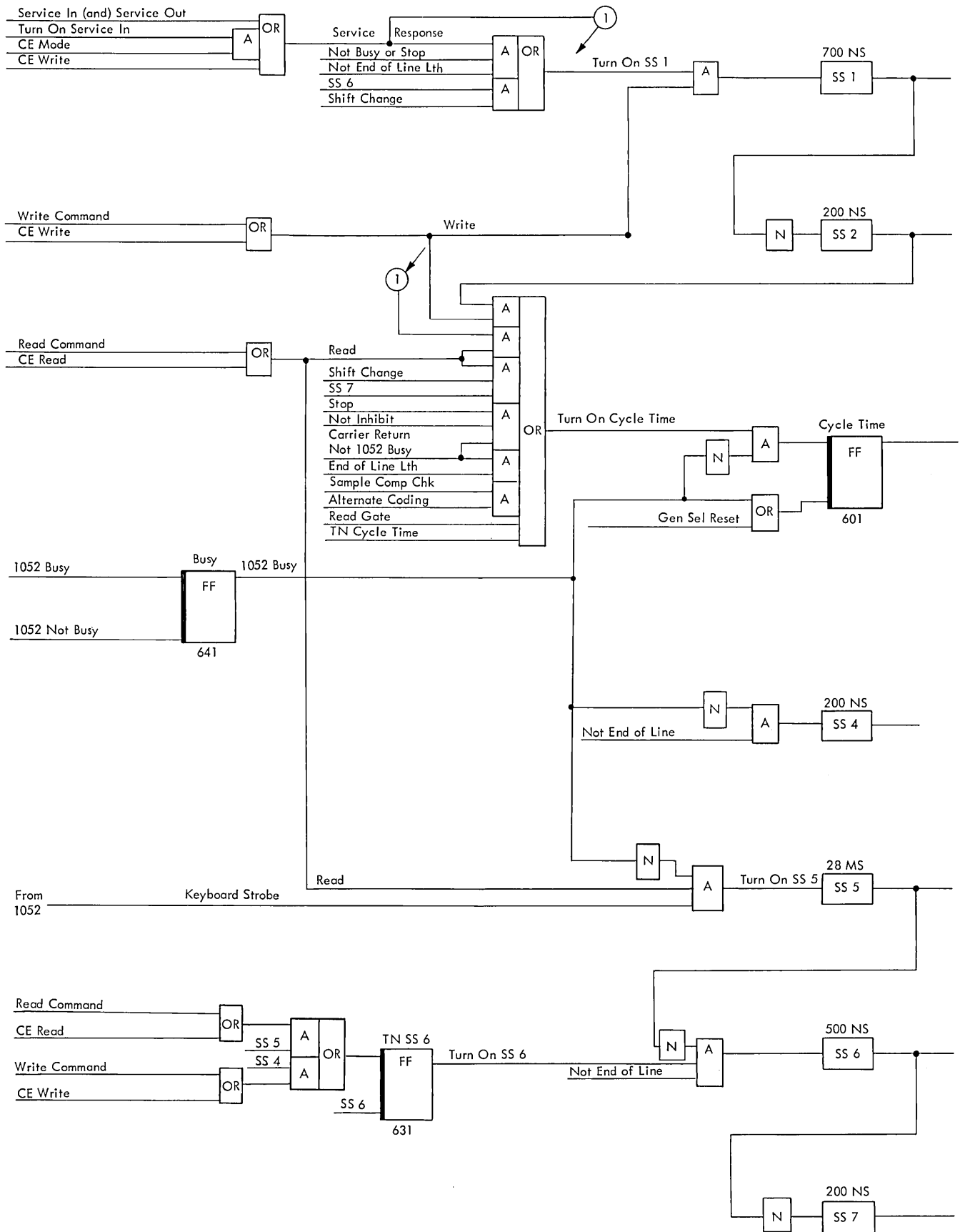
Cycle time is reset by the busy latch. This latch is turned on by the 1052 busy line energized by the printer when it takes a mechanical cycle. 1052 not busy is energized by the printer near the end of the printer cycle. This line resets the busy latch which fires SS 4.

For a read command, the SS 4 output resets the shift change latch if it has been set. SS 4, on a read command, also resets the printer busy latch, and not shift change resets the data register and SS 4. For the write command, SS 4 brings up the line "Turn on SS 6." Turn on SS 6 AND'ed with not end of line and not SS 5, fires SS 6.

The read/write clock is started at SS 5 for the read command. SS 5 is fired by read AND'ed with the keyboard strobe and not busy. The data register is reset during SS 5 time. When SS 5 times out, it fires SS 6 if the end-of-line latch is not on.

For the read command, SS 6 is used to gate the output of the BCD-to-8-bit (keyboard) translator to the data register. SS 6 also turns on the service request latch, to indicate to the channel that the control unit is ready for another data byte (write command) or ready to send another data byte to the channel (read command).

SS 7 fires when SS 6 times out. SS 7 resets the shift change latch for the write command. It also fires cycle time during the read command if the shift change latch has been set. The clock outputs are related to the various operations in detail in the Theory of Operation section.



● FIGURE 5. READ/WRITE CLOCK

## PRINTER TRANSLATOR

- Translates 8-bit code to tilt/rotate code.

Figure 6 illustrates the 8-bit-to-tilt/rotate translator. The series of AND's and OR's connected to the data register output decode the 8-bit byte stored in the data register into the corresponding tilt/rotate code. Note that all translating AND/OR functions except T2 use negative logic; that is, making the OR prevents the energizing of the corresponding tilt/rotate magnet. T2, the exception, is picked when the OR is made.

The output of this translator is gated with cycle time and not function. If the byte in the data register is a function character, the function decoder (Figure 9) activates the function line at SS 1 time, when the data byte is set into the data register. Conversely, if the data byte in the data register is not a function character, the function line is inactive, and allows cycle time to gate the lines picking the tilt/rotate magnets.

## KEYBOARD TRANSLATOR

- Translates 6-bit code to 8-bit code.

Figure 7 illustrates the translation of the BCD output of the 1052 keyboard to the 8-bit code. All of the AND/OR logic is not illustrated because all functions are similar to each other. Note that four of the eight output lines are negative logic in that activating the output line prevents the corresponding bit from being set into the data register. The other four output lines are positive logic; activating these lines results in setting the corresponding bit into the data register.

Also note the lower/upper case latch. The output of this latch is AND'ed into the translator to control the translation of the BCD output of the keyboard. Each key results in the same BCD coding for both the upper and lower case. The translation to either upper or lower case 8-bit code is controlled by the lower/upper case latch. For example, the output of the letter key "B" is  $B \bar{A} \bar{8} \bar{4} \bar{2} \bar{1}$  in the BCD code. This code is the same for both upper and lower case. When the lower/upper case latch is on (lower case), the  $B \bar{A} \bar{8} \bar{4} \bar{2} \bar{1}$  is translated to  $0 \bar{1} \bar{2} \bar{3} \bar{4} \bar{5} \bar{6} \bar{7}$ . When the lower/upper case latch is off (upper case)  $B \bar{A} \bar{8} \bar{4} \bar{2} \bar{1}$  is translated to  $0 \bar{1} \bar{2} \bar{3} \bar{4} \bar{5} \bar{6} \bar{7}$ . The control of the lower/upper case latch is described in the section "Functional Units, Shift Controls."

## SHIFT CONTROLS

- Controls case hemisphere of typing element.

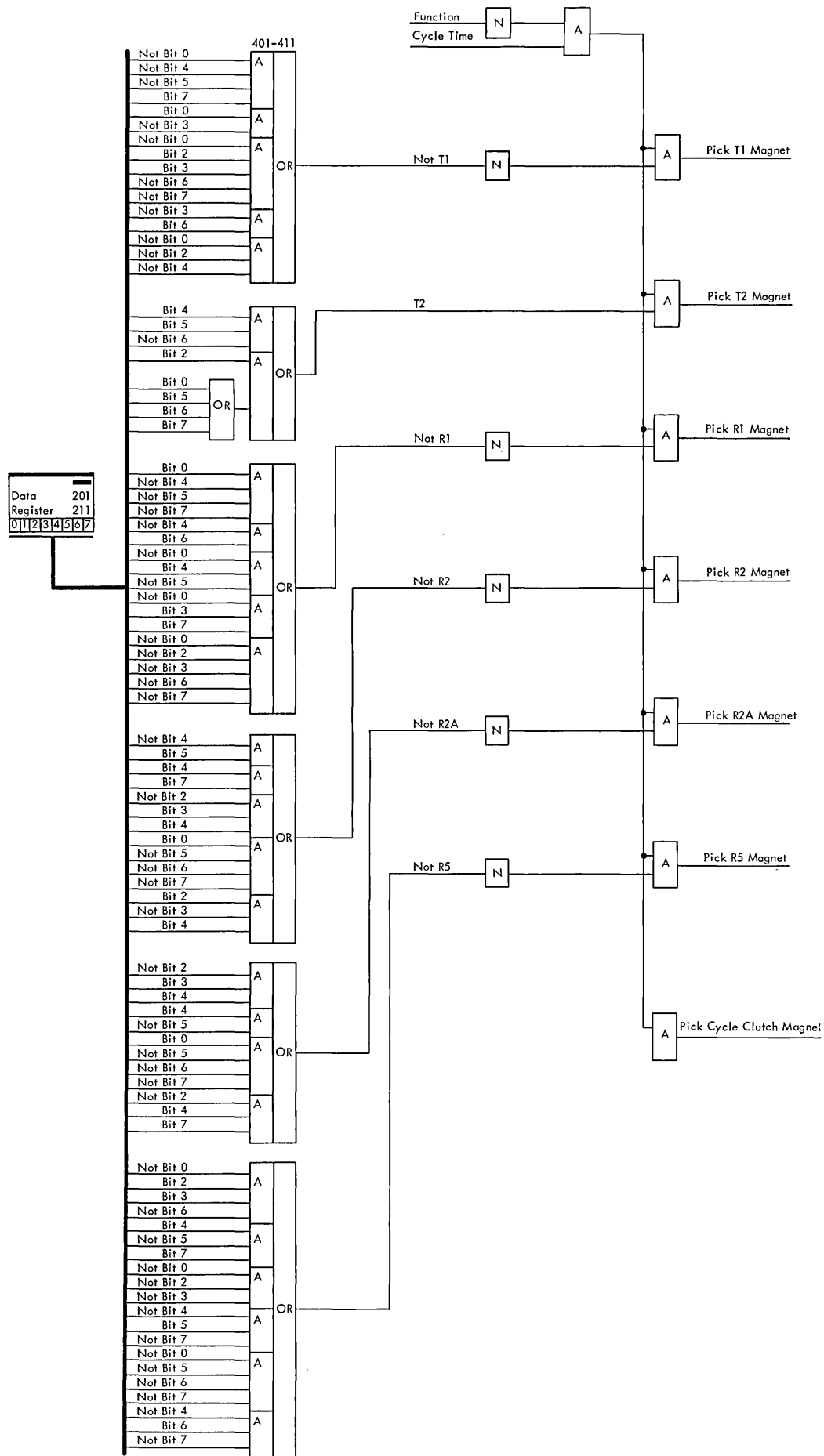
Figure 8 illustrates the shift change latch, the lower/upper case latch, and the SP latch.

During a write operation, the lower/upper case latch and the shift change latch are controlled by the output of the data register. If the lower/upper case latch is on, indicating that the printer is in lower case, and the character in the data register is an upper case character, the printer must be shifted to upper case before the character can be printed. The upper case character line is activated by the upper case character in the data register. Upper case character is AND'ed with lower case and SS 2 to turn the lower/upper case latch off, and also turn on the shift change latch. The shift change latch coming on causes the character to be held in the data register while the clock is run to shift the printer to the upper case. After the shift cycle is complete, the clock is again run to print the character.

Had the printer been in upper case, and had the character in the data register been a lower case character, the printer would have been shifted to lower case before gating the output of the data register to the printer translator. If the printer had been in upper case, the lower/upper case latch would have been off, and SS 2 would have been AND'ed with not upper case character and lower case latch off to turn both the shift change latch and the lower/upper case latch on. Again, the shift change latch would have caused the character in the data register to be held there while the clock was run to shift the printer to the lower case. After the shift cycle was completed, the clock would have been run to print the lower case character.

The read operation is similar to the write operation. The major difference lies in the control of the two latches. When the shift key on the keyboard is operated, the keyboard sends the BCD bits  $\bar{C} \bar{B} \bar{A} \bar{8} \bar{4} \bar{2} \bar{1}$  to the control unit. The keyboard strobe is also sent to the control unit. The keyboard strobe starts the clock at SS 5, and the upshift BCD bit configuration is AND'ed with SS 6 to turn off the lower/upper case latch and turn on the shift change latch. The shift change latch causes the read/write clock to run to shift the printer from lower case to upper case. The shift change latch also blocks SS 7 from setting the service request latch to raise request-in to the channel. No byte is sent to the channel for shifting.





●FIGURE 6. PRINTER TRANSLATOR (TRANSLATE 8-BIT TO TILT/ROTATE)

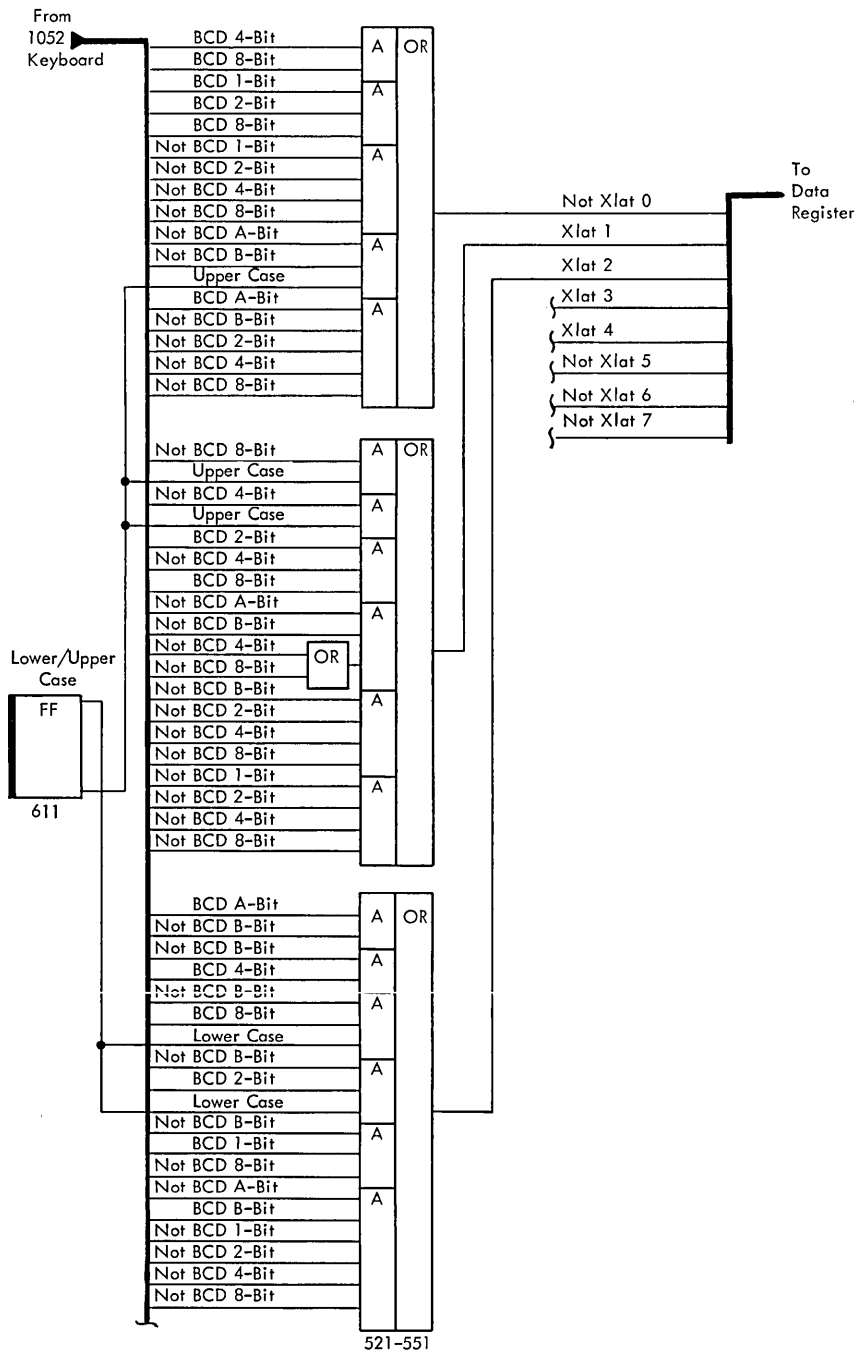


FIGURE 7. KEYBOARD TRANSLATOR

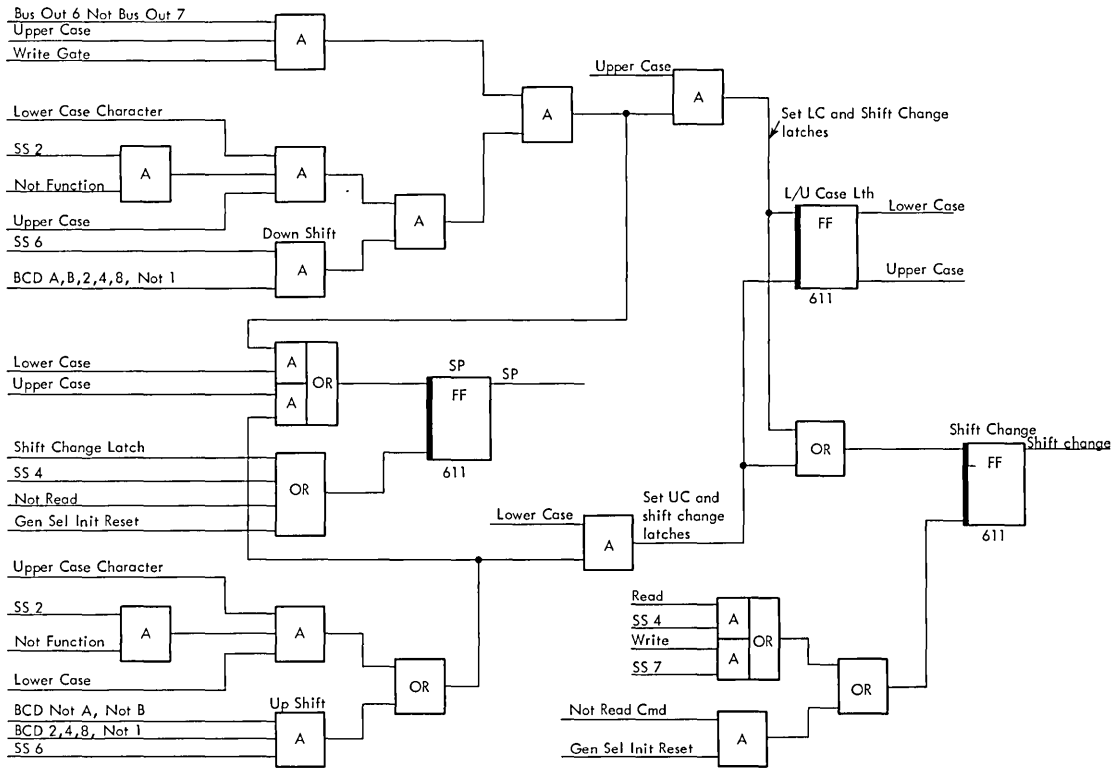


FIGURE 8. SHIFT CONTROLS

When the shift key is released at the keyboard, a sequence similar to that described in the above paragraph occurs. The BCD bits differ in that instead of  $\bar{C} \bar{B} \bar{A} 8 4 2 \bar{1}$  (upshift) the keyboard sends  $\bar{C} B A 8 4 2 \bar{1}$  to the control unit along with the keyboard strobe. The lower/upper case latch is turned on along with the shift change latch. The clock is started by read AND'ed with keyboard strobe; the printer is shifted to the lower case, and the request-in line is blocked.

Additional circuitry has been provided to space the printer if the operator attempts to shift the printer to the same case the type head is in. See Figure 8. These circuits were provided to put the printer through a mechanical cycle in order to allow the read/write clock to complete its sequence. The 1052 busy line from the printer is required to reset cycle time and 1052 not busy fires SS 4. If the printer were not forced to space under the previously mentioned condition, it would hang up.

Following are the two possibilities of an operator's attempting to shift to the same case the type head is in:

1. An operator might release the shift lock to place the head in lower case for a read operation when the head is in lower case at the time.
2. An operator, upon completing a continuous write operation in CE mode, might attempt to shift

to upper case when the continuous write operation was terminated with the head in upper case.

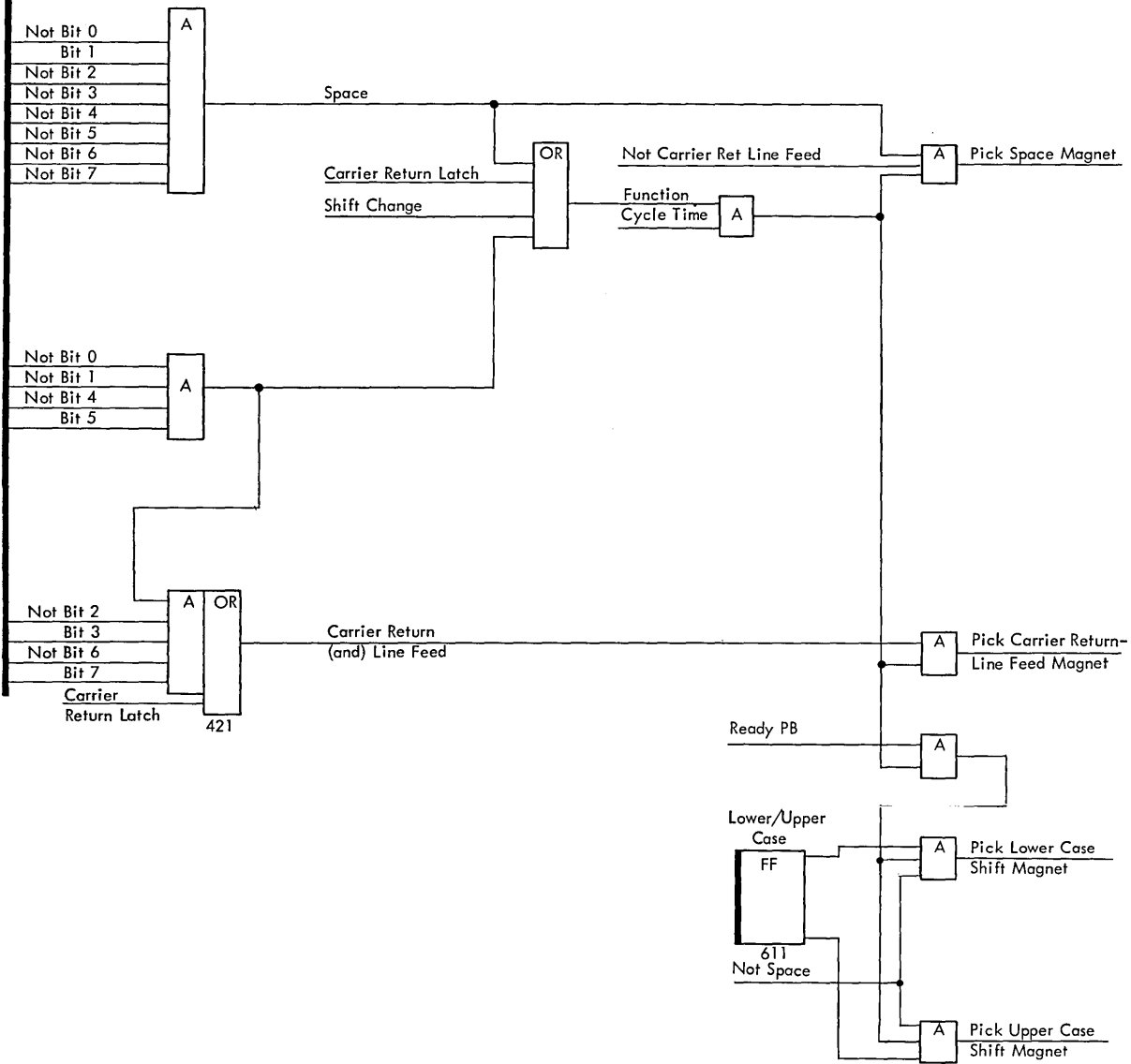
#### FUNCTION DECODER

- Determines whether the data register contains function or printable character.
- Operates printer function magnets.

Figure 9 illustrates the function decode circuits. These circuits analyze the character in the data register to decide whether that character is to perform a function at the printer. Just as the tilt/rotate magnets are energized by cycle time, so are the function magnets. The 8-bit bytes for the space and carrier return-line feed characters activate the function line. This line is activated at SS 1 during a write operation when the data register is set with the character on the bus-out lines, or at SS 6 when the data register is set with the output of the keyboard translator for the read operation.

Note that the carrier return-line feed magnet may be operated by either a carrier return-line feed character in the data register or the carrier return latch. Note also that the function line is activated by either the shift change latch, the carrier return latch, or any function character in the data register.

Data	201						
Register	211						
0	1	2	3	4	5	6	7



• FIGURE 9. FUNCTION DECODER

The lower case shift magnet and the upper case shift magnet are operated from the lower/upper case latch. Any time the case of the printer is to be changed, the shift change latch is turned on, and the output of the shift change latch activates the function line. Cycle time then may be AND'ed with the on or off output of the lower/upper case latch to perform the shifting in the printer.

## 1052 PRINTER-KEYBOARD

- Selectric printer
- Keypunch keyboard

The IBM 1052 Printer-Keyboard is a page printer with printing mechanism similar to the IBM Selectric typewriter. The 1052 keyboard is a modified IBM 024/026 keyboard housed in the same cover as the printing mechanism of the IBM Selectric typewriter. The printer and keyboard are electrically, not mechanically, connected by means of the console control unit, which allows these two units to operate independently.

### Printer

The 1052 printer is a self-contained package including the drive motor. It is designed for placement on a flat surface convenient to the operator. The printer is cable-connected to the I/O control unit, which contains the 8-bit-to-tilt/rotate (printer) translator. The printer can accept data at a maximum rate of 15.5 characters per second from the channel. Although the printer has a removable print head, allowing the selection of different print arrangements, one print arrangement is standard. The standard print head is Part Number 1167938. The arrangement of the characters on the print head is illustrated in Figure 10.

The printer recognizes 44 printable characters in the up shift mode, and 44 in the down shift mode. The printer performs four functions: space, carrier return and line feed, up shift, and down shift.

A paper presence control constitutes part of the interlock circuitry that places the printer in a ready status. As the trailing edge of the last form reaches a point about two inches from the printing line, the printer signals this condition to the console control unit, and reverts to a not-ready status. Printing is not interrupted by this action.

A carrier return-line feed operation interrupts the printing operation to allow enough time for the printer to complete this function. More than one character time will normally be required. When the printer begins a carrier return-line feed operation, the busy latch is set in the control unit. The

busy latch interlocks the control unit until the printer completes the function. When the function is complete, the printer resets the busy latch in the control unit and the control unit resumes its operation.

The basic printing operation is the same as in the IBM Selectric typewriter. The tilt and rotate selector latches in the printer are controlled by the tilt and rotate (tilt/rotate) magnets in the printer. If the character in the data register in the control unit is a printable character, the corresponding tilt/rotate lines in the control unit are activated to energize the tilt/rotate magnets in the printer. If the character in the data register is a function character, the corresponding printer function line is activated to energize the function magnet in the printer.

Refer to the I/O printer manual for the description of the mechanical operations performed by the tilt/rotate magnets and the function magnets in the printer.

### Keyboard

The 1052 keyboard is an adaptation of the IBM 024/026 keyboard, with the numeric keys located in a fourth bank similar to a typewriter keyboard. The keyboard is mechanically independent of all other units, and is connected electrically only to the I/O control unit. Data may be sent from the keyboard to the channel and/or the printer only through the console control unit.

The basic arrangement of the four-bank keyboard is shown in Figure 11. There is a total of 53 function and character keys. Each key, except the alternate coding key, generates a BCD code for the character or function associated with that key. The two shift keys, and the shift lock, generate the up shift code when depressed. The down shift code is generated when either shift key is released. Output from the keyboard is the IBM paper tape and transmission code, and is in odd parity.

### Alternate Coding

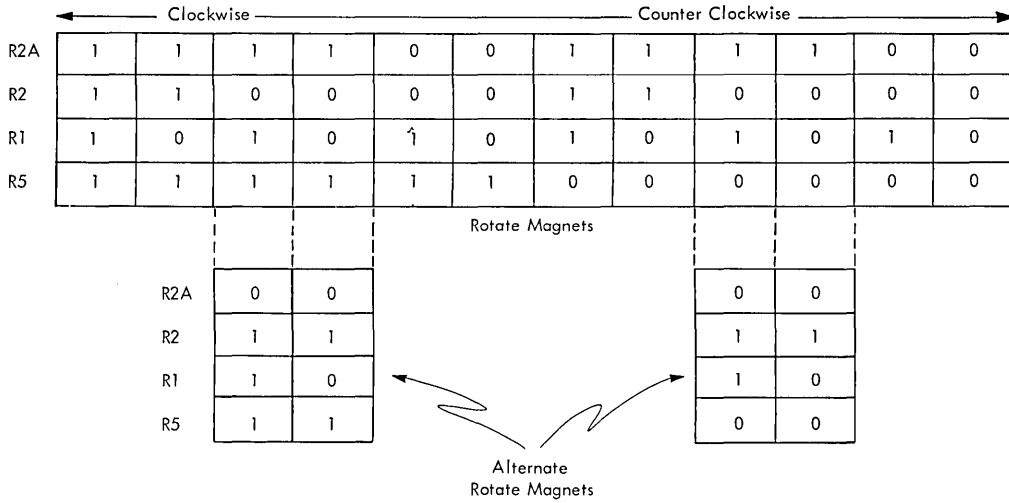
There is an alternate set of definitions for two of the numeric keys. The numeric 5 key sends the BCD bits  $C \bar{B} \bar{A} \bar{8} 4 \bar{2} 1$  to the console control unit. If the keyboard and printer are in the lower case, the keyboard (BCD to 8-bit) translator translates the  $C \bar{B} \bar{A} \bar{8} 4 \bar{2} 1$  to  $0 1 2 3 \bar{4} 5 \bar{6} 7$ . This is the 8-bit code for a five. If the keyboard and printer are in the upper case, the  $C \bar{B} \bar{A} \bar{8} 4 \bar{2} 1$  is translated to  $\bar{0} 1 2 \bar{3} 4 5 \bar{6} \bar{7}$ , the 8-bit code for the percent sign.

The alternate definition for the 5 key is obtained when the alternate coding key is held depressed while the 5 key is operated. Under these conditions, the keyboard output is the BCD bit combination  $C \bar{B} A 8 4 2 \bar{1}$ . This BCD bit combination is the code for

Typehead Characters

= 1	; 3	% 5	> 7	* 8	) 0		< 2	: 4	▼ 6	( 9	" #
? /	T t	V v	X x	Y y		¢ @	S s	U u	W w	Z z	I ,
J j	L l	N n	P p	Q q		— -	K k	M m	O o	R r	! \$
A a	C c	E e	G g	H h		+ &	B b	D d	F f	I i	⌋ .
-5	-4	-3	-2	-1	0		+1	+2	+3	+4	+5

Tilt Position	Tilt Magnets	
	T1	T2
0	1	1
+1	0	1
+2	1	0
+3	0	0



Note:  
1 = Magnet Energized  
0 = Magnet Not Energized

FIGURE 10. 1052 INTERNAL TILT/ROTATE CODE

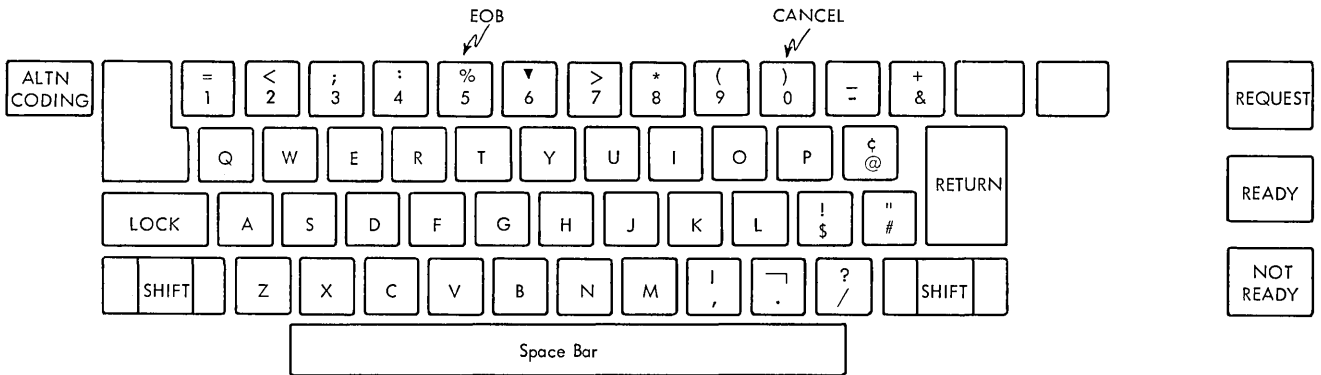


FIGURE 11. 1052 KEYBOARD

end-of-block (EOB). When the operator is through keying data to the channel, he holds the alternate coding key down while depressing the 5 key. This EOB code indicates to the console control unit and to the channel that the operator has completed the operation.

The second numeric key affected by the alternate coding key is the numeric zero. When data are being transmitted to a channel from the keyboard, and a keying error is made, the operator indicates an error condition by operating the zero key while holding down the alternate coding key. This procedure generates an even-parity code (B C bits) which indicates to the console control unit that the channel must be made aware of the fact that a keying error was made, and that provisions must be made for the operator to re-key the information to the channel. Neither the cancel character nor the EOB character is printed on the printer.

The alternate codes are obtained by switching from the right-hand-bail contacts to the left-hand bail contacts. Normally, the bail contacts on the right-hand side of the keyboard are used to generate the codes for each of the keys on the keyboard. When the alternate coding key is operated, the points of relay 20 remove the right bail contacts from the BCD output lines of the typewriter and insert the left bail contacts into these output lines. The circuits for the 1052 keyboard are shown in the ALD's for the console control unit. Figure 12 in this manual illustrates the arrangement of the bail, latch, and key-stem contacts in the keyboard. Depressing the alternate coding key and then any other key except 5 or 0 (zero) may cause an error condition when the printer adapter is operated on line. In CE mode, the alternate coding key, when used with any other key, causes the printer to stop (printer hang condition).

### CE Panel

A CE panel is mounted in the vertical portion of the 1052 cover just above the keyboard. This panel is illustrated in Figure 13. There are two switches on the CE panel: CE mode/on line, and continuous write/read. The continuous write/read switch is inoperative when the CE mode/on line switch is set to the on line position. When on line, the 1052 is operated in conjunction with the channel and the console control unit.

### Switches

For diagnostic purposes, the 1052 and the console control unit can both be taken off line by setting the CE mode/on line switch to the CE mode position. The

control unit and the 1052 are then under the control of the continuous write/read switch. When the CE mode switch is set to CE mode, and the continuous write/read switch is set to continuous write, the output of a character emitter in the console control unit is gated to the data register. From the data register, the characters follow the normal data path for a write operation. The character emitter must be plugged by the CE to emit two characters in the 8-bit code. Figure 14 illustrates the operation of the emitter. Note that in Figure 14, B (Intermediate Systems) when the switches are set to CE mode and continuous write, the CE write line is activated. The CE write line starts the read/write clock with SS 1 (Figure 5), gates the CE bus to the data register (Figure 3), and also operates the binary latch at SS 4 of each clock cycle. Note that in Figure 14, A (Large Systems) the operation is similar. The difference is that a CE mode signal is generated by setting a latch. When the latch is set, off-line relay K2 is picked and the CE write signal is generated. The interface disable switch (on the 2150 unit), when placed in the disable position, grounds the interface driver circuits while power is applied or removed from the 2150.

The CE continuous write mode provides a semi-fixed means to check up to 90% of the printer controls within the adapter, check decoding of the EBCDIC code to appropriate printer functions and characters, and mechanically check the printer portion of the 1052. The continuous write mode allows the customer engineer to set up any two EBCDIC codes and perform the desired operations alternately by the printer. The plugging is performed on the pin side of SLT board X1. The board is factory wired (yellow) for zero alternating with upper case A.

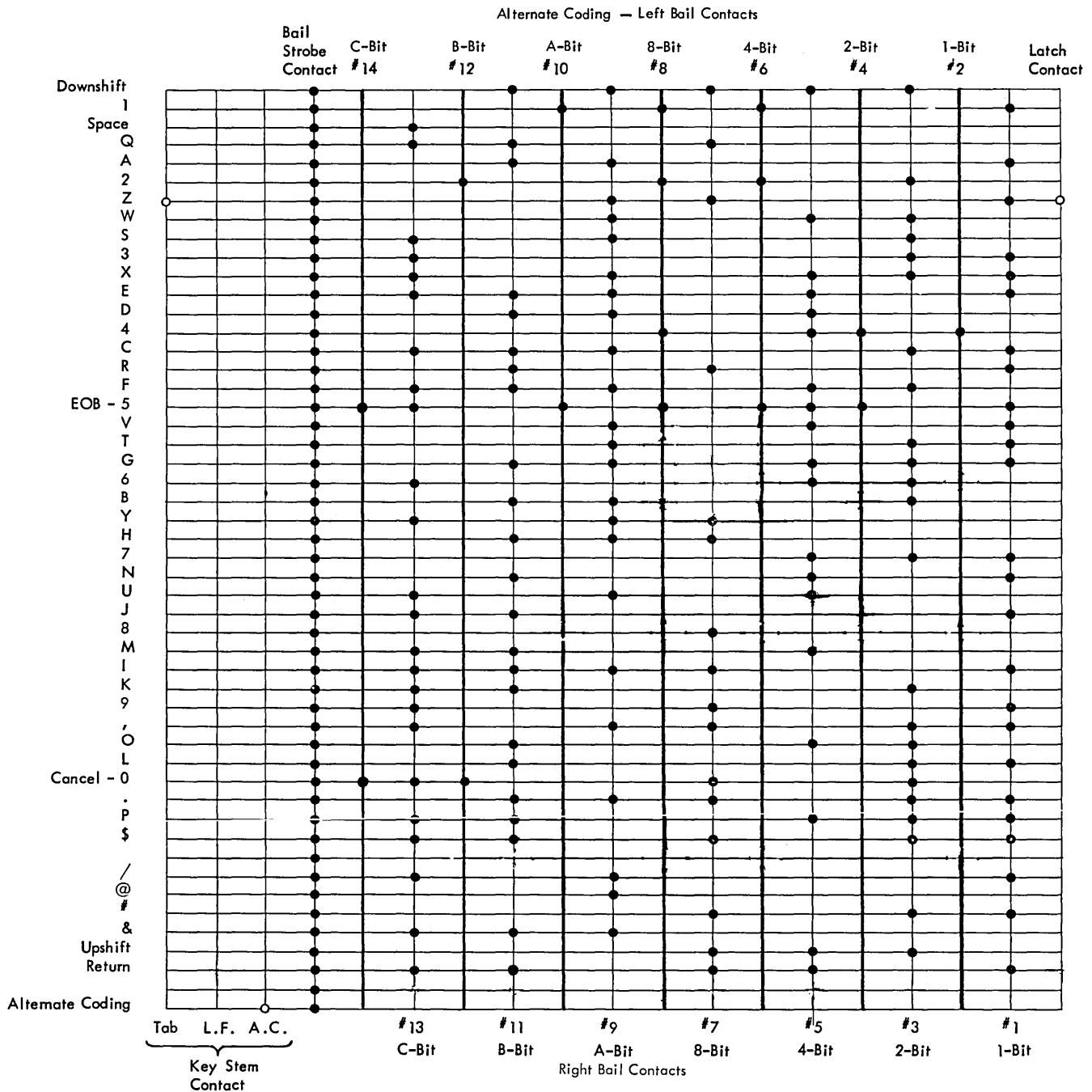
SLT board X1 locations for the various System/360 models are:

<u>Model</u>	<u>X1 Board Location</u>
40	Gate B--C1
50	Gate C--D4
65A	Gate E--D1
65B	Gate E--B1
67	Gate E--D1
75A	Gate A--D4
75B	Gate B--A1

When the 2150 free-standing console is used on Models 50, 65, 67, and 75, the pluggable board is in location B1 in the console.

The 1052 Adapter is standard on the System/360 Model 44 and integrated into the 2044 Central Processing Unit. The pluggable board is in Gate D--B1.

See Figure 15 for plugging instructions and Figure 16 for the EBCDIC code set.



**Keyboard Common Contact Numbers 1 and 2.** These contacts open when the keyboard-restore magnets are energized. Number 1 common contact disconnects the supply voltage from the bit lines and prevents sending any bits during a keyboard-restore operation.

Number 2 common contact opens the direct circuit to the restore magnets and puts a current-limiting resistor in series with the restore magnets. This permits locking the keyboard by continually energizing the restore magnets.

**Left-Hand Latch Contact (Tab and Z).** This latch contact closes whenever the Z or tab key is pressed. When the tab key is pressed, the tab keystem contact is closed and the B- and 4-bit keyboard lines are pulsed to complete the tab code.

**Alternate-Coding Keystem Contact.** When the alternate-coding key is pressed, the alternate-coding contact is closed and the alternate-coding

relay, R-20, is picked. This operation connects the left-bail contacts to the keyboard bit lines and disconnects the right-bail contacts from the bit lines.

**Strobe Bail Contact.** When any permutation bar drops, the strobe bail contact makes and starts the read/write clock in the console control unit.

**Right-Hand Latch Contact (Carrier Return and Line Feed, and Line Feed-CR/LF and LF).** The contact closes whenever the return or line-feed key is pressed. When the return key is pressed, the right-hand latch contact closes and pulses the B-bit keyboard line to complete the CR/LF code. When the line-feed key is pressed, the right-hand latch contact closes and the line-feed keystem contact also transfers, and the A-bit keyboard line is pulsed to complete the line-feed code.

FIGURE 12. 1052 LATCH, BAIL, AND KEYSTEM CONTACT ARRANGEMENTS



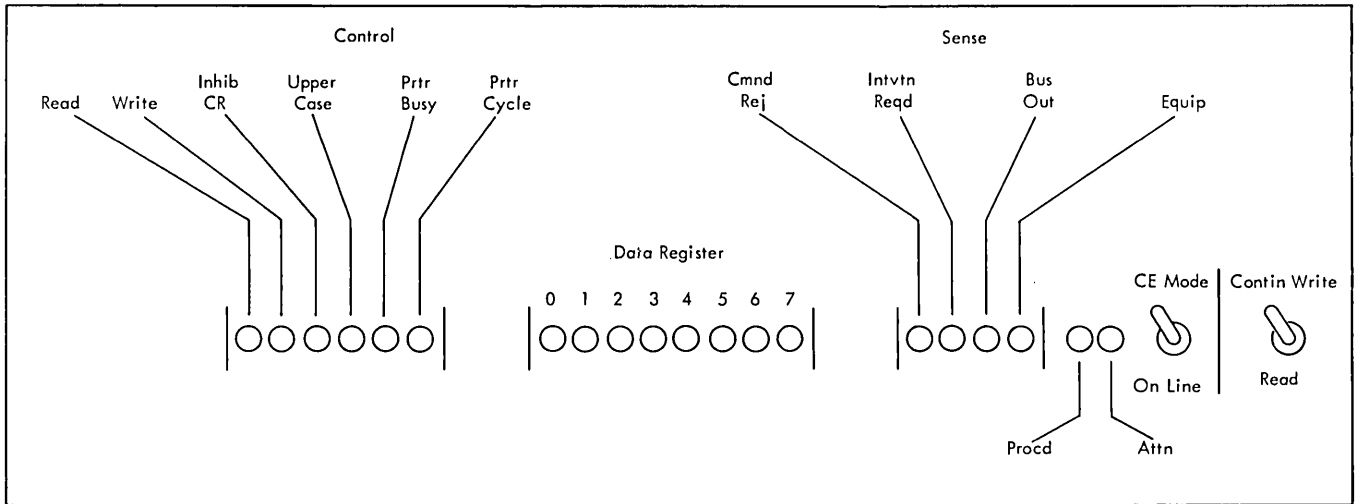


FIGURE 13. 1052 CE PANEL

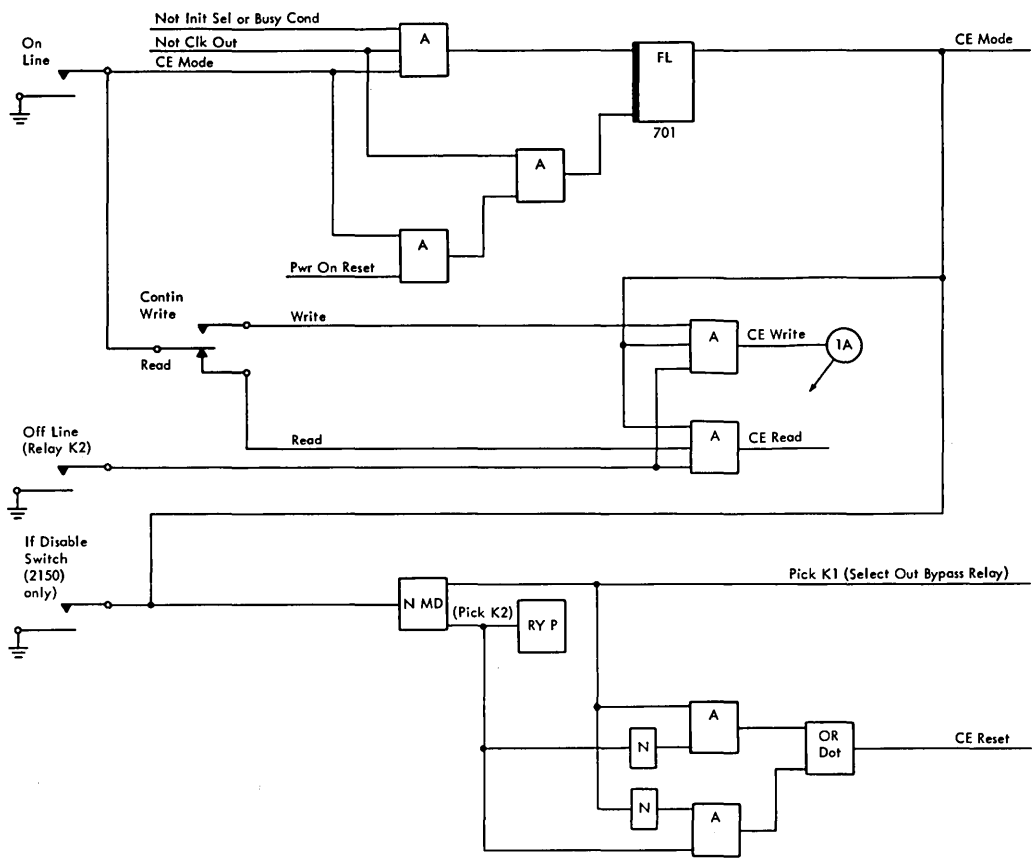
CE read permits keying in of all characters on the keyboard and performing the desired operation, printing or printer/function. All read controls can be checked including PTTC/8 to EBCDIC translation and EBCDIC to tilt/rotate or printer function. The data register indicators contain the PTTC/8 to EBCDIC translation and remain set until a subsequent character is keyed.

#### Lights

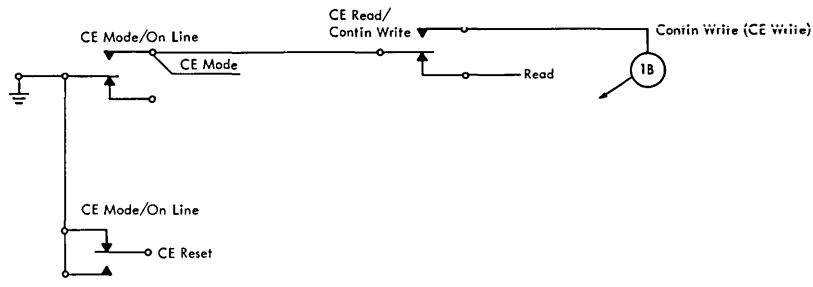
The six control lights on the CE panel indicate the controlled state of the 1052. The read lamp is lit whenever the read command latch in the control unit is on, or when the switches on the CE panel are set to CE mode and read. The write lamp is lit whenever the write command latch in the control unit is on, or when the switches on the CE panel are set to CE mode and continuous write. The inhibit-carrier-return

lamp is lit whenever the inhibit-carrier-return latch is on in the control unit. The upper case lamp is lit whenever the lower/upper case latch in the control unit is off, indicating that the printer and keyboard are in upper case. The printer-busy lamp is lit whenever the printer busy latch in the control unit is on.

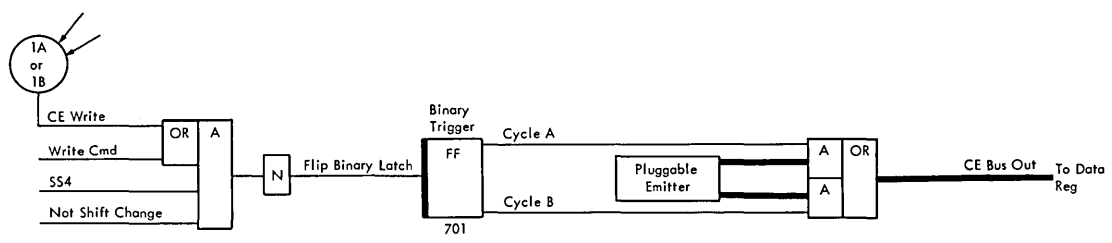
The data register lamps indicate the contents of the data register. Each lamp indicates the on-state of its associated data-bit latch. The sense lamps indicate the on-state of the sense bit latches. The proceed lamp is lit whenever the keyboard is unlocked to allow the keying of data or functions from the 1052 keyboard. The attention lamp is lit when the request pushbutton on the 1052 keyboard cover is operated. The lamp remains lit until the gate-status-in line comes up. The lamp indicates the on-state of the store request latch.



A. Large Systems (Note 1)

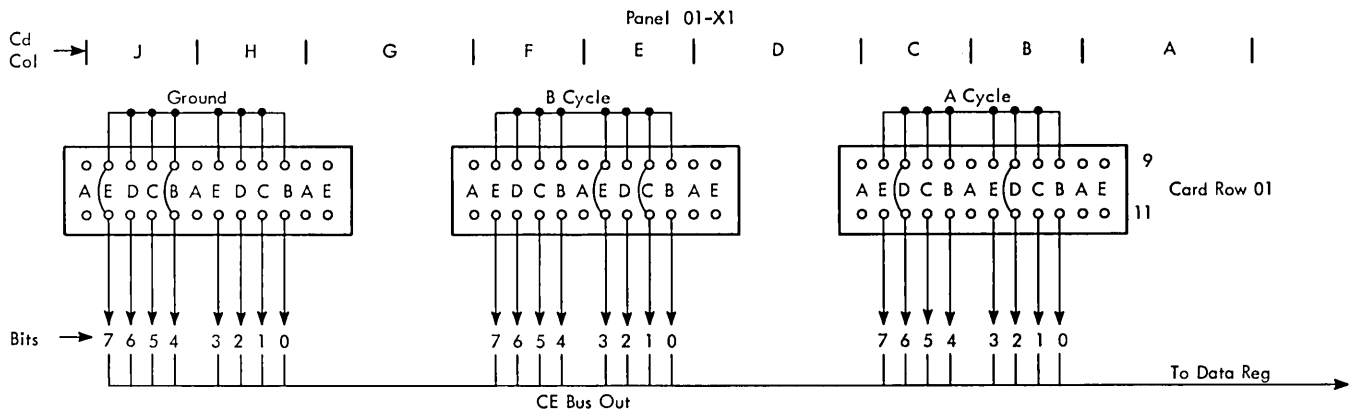


B. Intermediate Systems (Note 2)

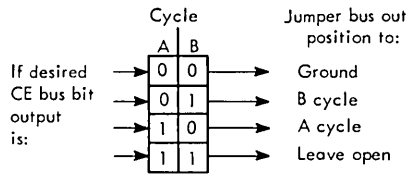


- Notes:
1. System/360 Models 65, 67, and 75. The unit isolation feature must be installed on the 2150.
  2. System/360 Models 40, 44, and 50.

FIGURE 14. CE WRITE



Instructions



Example (see sample wiring above)  
Print lower case W on A cycle  
Print upper case M on B cycle

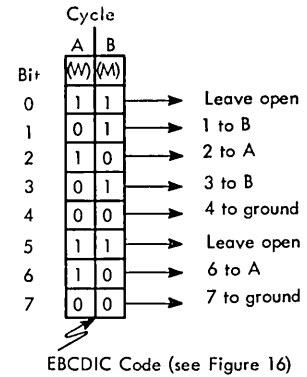


FIGURE 15. CE CONTINUOUS WRITE MODE - WIRING CHART

	0123	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000					SP	&	-										0
0001							/			a	i			A	J		1
0010										b	k	s		B	K	S	2
0011										c	l	t		C	L	T	3
0100										d	m	u		D	M	U	4
0101										e	n	v		E	N	V	5
0110		NL								f	o	w		F	O	W	6
0111										g	p	x		G	P	X	7
1000										h	q	y		H	Q	Y	8
1001										i	r	z		I	R	Z	9
1010					←	!		:									
1011					.	\$	,	#									
1100					<	*	%	@									
1101					(	)	-	'									
1110					+	;	>	=									
1111					!	~	?	"									

SP - Space  
NL - New Line  
NOTE: Graphic representations are undefined for the bit patterns outside the heavily outlined portions of the chart.

FIGURE 16. EBCDIC CODE SET

## THEORY OF OPERATION

- Figure MD-1 is the 1052 unit data and control diagram.
- Figures MD-2 through MD-6 are I/O operations diagrams.
- All commands described within the framework of: initial selection, data transfer, ending sequence.

This section of the manual presents the detailed circuit descriptions of the control unit by command. Figures MD-2 through MD-6 present the information in positive logic form, with the sequence of the circuits in these figures corresponding to the I/O interface signal sequence for the command being described. The seven valid commands are:

<u>Command</u>	<u>Bit Configuration</u>
	<u>P 0 1 2 3 4 5 6 7</u>
Test I/O	1 0 0 0 0 0 0 0
Sense	0 0 0 0 0 0 1 0 0
Control No-Op	1 0 0 0 0 0 0 1 1
Control Alarm	0 0 0 0 0 1 0 1 1
Write-Auto Carrier Return	1 0 0 0 0 1 0 0 1
Write-Inhibit Carrier Return	0 0 0 0 0 0 0 0 1
Read	1 0 0 0 0 1 0 1 0

All other command byte bit configurations with correct parity are considered to be invalid commands.

### WRITE

- Initial selection sequence
- Data transfer sequence
- Ending sequence

#### Initial Selection Sequence

The initial selection sequence for the write operation (write-ICR or write-ACR) is begun by the channel, and is illustrated in Figure MD-2. The channel raises the select-out, hold-out, and address-out lines, and places the address byte of the console control unit on the bus-out lines. The console control unit matches the address byte against the internally plugged address, and if the two match the address match line is activated and AND'ed with address out to turn on both the initial select trigger and the address-in trigger. The on-output of the address-in trigger turns on the operational-in trigger to raise the operational-in line to the channel.

The channel drops the address-out line to the console control unit when it receives the operational-

in line from the console control unit. When address-out drops, the control unit raises the address-in line to the channel, and gates the output of the address bit generator to the bus-in lines, thereby generating the address-in byte.

The channel receives the address byte and the address-in line, and responds by placing a command byte on the bus-out lines and raising the command-out line. The command-out line from the interface (command-out cable out) AND's with the on-output of the operational-in trigger to raise the command-out line with the console control unit. A few nanoseconds after command out is raised, the command-out delay line becomes active. The delay is the result of passing command-out through two inverters, each of which introduces a few nanoseconds' delay into the signal.

Command-out sets the operational-in interlock and activates the command gate. Command gate raises sense gate, and sense gate in turn raises write gate. Write gate then sets the write command latch (the bit configuration of the command byte having activated valid command and write command bits) and the service request latch.

Command-out delay resets the address-in trigger, dropping address-in to the channel. When the channel recognizes the dropped address-in line, it drops command-out. The inactive command-out line now turns on the status-in trigger in the control unit. The status-in trigger raises status-in to the channel and gates the status byte to the bus-in lines.

The channel receives the status-in line and the status byte and replies with service-out, indicating its acceptance of the status byte. The initial selection sequence is complete at this point.

#### Data Transfer Sequence

The service request latch is set during the initial selection sequence (Figure MD-2), but its on-output is not used until the end of the initial selection sequence. The service request line in Figure MD-2 activates the status conditions line. Status conditions activates the request-in line to the channel as soon as the operational-in trigger is reset. The request-in line causes the channel to raise the hold-out and select-out lines as during the initial selection sequence. The channel, however, does not raise address-out, nor does it place an address byte on the bus-out lines. This allows the address-in trigger to be set, but not the initial select trigger. The control unit responds with address-in and its address byte as before, and channel in turn activates command-out to the control unit.

The channel does not place a command byte on the bus-out lines during the data transfer sequence; therefore the write gate (Figure MD-2) is not activated in the control unit, and the service request latch is not set by command-out during the data transfer sequence. The write command latch is set during the initial selection, and remains set through the data transfer sequence.

The busy condition latch (Figure MD-3) is set when the initial selection trigger is reset by AND'ing not initial select trigger with write command. The busy condition latch is set at the end of the initial selection sequence. The on-output of the busy condition latch is then AND'ed with service request, operational-in trigger, not address-in trigger, and not command or service-out to set the service-in trigger when command-out falls during the data transfer sequence. The service-in trigger raises service-in to the channel, indicating the control unit is ready for a data byte.

The channel replies to service-in with service-out and places a data byte on the bus-out lines. The control unit AND's service-in and service-out to activate service response (Figure MD-3), and start the read/write clock at SS 1. SS 1 gates the data byte from the bus-out lines to the data register. The clock runs through SS 7 to complete the operation by gating the output of the data register to and through the printer translator and/or function decoder.

SS 2 is AND'ed with not printer busy, write, and not stop to activate turn off service-in to reset the service-in trigger and drop the service in line to the channel (Figure MD-3). Channel then drops service-out, and the data transfer sequence is complete. SS 6 is AND'ed with not end of line, write, not busy or stop, and not service-in and service-out to activate turn on service-in (Figure MD-2). The active turn on service-in line sets the service request latch and service request activates status conditions (Figure MD-3) to begin another data transfer sequence by raising request-in to the channel. The data transfer sequences are continued until an ending sequence occurs in place of a data transfer sequence.

### Ending Sequence

The write-ICR and write-ACR commands are distinguished by the ending sequences. The inhibit carrier return latch is set during the initial selection for the write-ICR command, allowing the control unit to present both the channel-end and the device-end status bits to the channel during the same ending sequence.

The write-ACR command does not set the inhibit carrier return latch during the initial selection.

Therefore only the channel-end status bit is presented to the channel during the first ending sequence. The carrier is started moving to the left margin at about the same time that the channel-end status is presented to the channel. A second ending sequence is required to present the device-end status bit to the channel when the carrier reaches the left margin and stops moving.

### Write-ICR

The inhibit carrier return latch is set during the initial selection sequence. Write gate (activated by command-out) AND's with not bus out 4 to set the inhibit carrier return latch during the time that the command byte is on the bus-out lines (Figure MD-4). The request-in line is activated to the channel at the end of the previous data transfer sequence (Figure MD-3). The channel, however, has no more data to send to the console control unit (channel byte count has gone to zero). The following signal sequence occurs: channel raises hold-out and select-out; console control unit raises operational-in and address-in and places its address byte on the bus-in lines; channel raises command-out; console control unit raises service-in; thus far the sequence is the same as for a data transfer sequence. Now, however, channel raises command-out a second time as a reply to service-in, instead of service-out. A command-out reply to service-in indicates stop.

Figure MD-4 illustrates the ending sequence for both write-ICR and write-ACR. Service-in and command-out are AND'ed together to activate write/read turn on channel end. Write/read turn on channel end sets both the channel end and the stop latches. The on-output of the stop latch sets the store device end latch. The on-output of the store device end latch activates device end interrupt, which sets the device end latch.

In Figure MD-3, the service-in trigger is reset when the channel replies to service-in with command-out. Channel then drops command-out when service-in drops. In Figure MD-4, the channel end latch activates the status conditions line, and status conditions AND's (in Figure MD-2) with operational-in trigger, not address-in trigger, not service-in trigger, and not command or service-out to set the status-in trigger and raise the status-in line to the channel. The on-outputs of the status bit latches are gated to the bus-in lines at the same time.

The channel replies with service-out to status-in from the control unit, indicating the acceptance of the status byte. Device end AND's with status-in (Figure MD-3) to activate command reset. The write command latch and the inhibit carrier return latch are reset by command reset.

## Write-ACR

The ending sequence for the write-ACR operation begins the same as the ending sequence for write-ICR. The major difference lies in the effect of not setting the inhibit carrier return latch during the initial selection. When the ending sequence proceeds to the point where the channel replies to service-in with the second command-out, indicating stop, the write/read turn on channel end line (Figure MD-4) sets both the channel-end and stop latches. The channel-end latch again activates the status conditions line, and the status conditions line again sets the status-in trigger (raising status-in to the channel) when command-out falls the second time.

Because the inhibit carrier return latch is off, the carrier return latch is set (stop AND'ed with not printer busy and not inhibit carrier return - Figure MD-3) and the read/write clock is started at cycle time. Cycle time then sets the printer busy latch, picks the carrier return-line feed magnet in the printer, and picks the lower case shift magnet in the printer if the printer was in upper case. The printer busy latch now AND's with stop and carrier return to set the inhibit carrier return latch (Figure MD-4).

Up to this point, the channel end status bit has been sent to the channel, the carrier has started returning to the left margin, but the device-end status bit has not been sent to the channel. The turn on device end line becomes active (to set the store device-end latch - Figure MD-4) when the carrier has finished returning to the left and the busy latch is reset. The on-output of the store device end latch then activates device end interrupt, and device end interrupt in turn activates the status conditions line to raise request-in to the channel (Figure MD-4).

The following sequence occurs: control unit raises request-in to the channel, channel raises hold-out and select-out; console control unit raises operational-in and address-in, and places its address byte on the bus-in lines; channel raises command-out; control unit drops address-in; channel drops command-out; control unit raises service-in; channel again raises command-out; control unit drops service-in; channel drops command-out. Up to this point the sequence is the same as when the channel-end status bit was sent to the line. The difference is in the fact that this sequence was begun by the device-end interrupt line raising request-in to the channel.

The device end interrupt line has been active during the above sequence, and device end interrupt has kept the status conditions line active. When channel drops command-out the second time, the status-in trigger (Figure MD-2) is set by the status conditions line. Status-in is raised to the channel, and the on-output of the device end latch is gated to

the bus-in lines as the device-end status bit. Channel rejects the status by replying to status-in with command-out, and the status is stacked.

## READ

- Initial selection sequence
- Data transfer sequence
- Ending sequence

### Initial Selection

Initial selection for the read command is almost identical to the initial selection for the write command. The inhibit-carrier-return latch is not set during the initial selection sequence because the read command byte contains the 4-bit. The read command latch (Figure MD-2) is set while command-out is up and the read command byte is on the bus-out lines. Note that the service request trigger is not set at command-out time during the initial selection sequence. Recall that for the write command the service request latch was set by command out and the write command byte. This led to the first data transfer sequence.

### Data Transfer

The 1052 keyboard is unlocked when the read command latch is set. Figure MD-5 illustrates the circuits used for the data transfer sequence of the read command. When a key is operated at the keyboard, the keyboard strobe line becomes active, and is AND'ed with read and not 1052 busy to start the read/write clock at SS 5. SS 5 resets the data register, and SS 6 sets the output of the keyboard translator into the data register (Figure 3). SS 7 AND's with not shift change, keyboard strobe and not stop to activate turn on service in to set the service request latch (Figure MD-5). Service request in turn activates status conditions, and status conditions raises the request-in line to the channel.

The channel replies to the request-in with select-out and hold-out, and the data transfer sequence proceeds the same as the data transfer sequence for the write command, with one exception. For the write command, data is placed on the bus-out lines by the channel when the channel raises service-out. For the read command, the control unit places data on the bus-in lines when the control unit raises service-in. The last character remains stored in the data register since the register is not cleared until a general reset occurs or until SS 5 time occurs during the following keyboard strobe.

With respect to Figure MD-4, select-out AND's with request-in to set the address-in trigger, and the address-in trigger in turn sets the operational-in

trigger, raising operational-in to the channel. Because address-out is not active when operational-in comes up, the console control unit raises address-in and gates its own address to the bus-in lines. Channel replies to address-in with command-out, and command-out delay drops the address-in line by resetting the address-in trigger. Channel drops command-out because the console control unit drops address-in. The service-in trigger is set when command-out falls, raising the service-in line to the channel and gating the output of the data register to the channel.

Channel responds to service-in with service-out and the console control unit AND's service-in with service-out to activate service response to start the read/write clock at cycle time. Cycle time causes the printer either to print the character in the data register or to perform the function called for by the character in the data register. The output of the keyboard has now been transferred to the channel and the printer, and the sequence is complete.

#### Ending Sequence

The ending sequence is similar to that for the write-ACR command, but can be started three different ways. First, the console control unit can try to send one more data byte to the channel after the channel byte count has gone to zero. In this event, the sequence described under data transfer proceeds to the point where the character is stored in the data register and the console control unit raises request-in. Channel makes a reply to service-in from the console control unit. Instead of replying with service-out as during the data transfer sequence, channel replies with command-out for the second time, indicating stop. From this point on the ending sequence is identical to the ending sequence for the write-ACR command. Service response is not generated (Figure MD-4) to start the read/write clock because service-out is not given as a reply to service-in. The last character stored in the data register is not printed because the clock is not started, nor is it accepted by the channel.

The second means of obtaining the ending sequence for the read command is through the use of the EOB signal. When the operator has finished keying in data, if the byte count in the channel has not previously gone to zero he may end the read operation by holding the alternate coding key down while operating the numeric 5 key. This causes the EOB line in Figure MD-4 to activate the write/read turn on channel end line. From this point on, this ending sequence proceeds exactly the same as the ending sequence described in the preceding paragraph.

The third means of obtaining the ending sequence for the read command is through the use of the cancel signal. If the operator has made a keying error he may cause the channel to ignore the block of data in which the error was made. The operator holds the alternate coding key down while operating the numeric 0 key. This action activates the cancelline in Figure MD-4 and causes the ending sequence to proceed as described in the first paragraph of this section.

#### Status Byte Composition

The status byte transferred to the channel may be composed of any six bits. Figure MD-6 illustrates the composition of the status byte. Bit position 0 indicates the request pushbutton on the 1052 has been operated. Bit position 3 indicates that the channel has attempted to execute an initial selection sequence with the control unit while the control unit was busy executing another command. Bit position 4 indicates the control unit has finished executing a command and the channel has not yet been made aware of this condition. Bit position 5 indicates the 1052 has finished executing a command and the channel has not yet been made aware of this condition. Bit position 6 indicates an error condition has occurred. Bit position 7 indicates the cancel key has been operated (read command only). Bit positions 1 and 2 are not used in the status byte.

The individual error conditions indicated by bit position 6 are not defined in the status byte. The channel must issue a sense command to determine the particular cause of the error indication.

#### SENSE COMMAND

- Initial selection sequence
- Sense byte transfer sequence
- Ending sequence (a continuation of the sense byte transfer)

The sense command is normally issued following an error indication in the status byte of an ending sequence for either a read or write command. If the status byte contains the unit check (6) status bit, the channel will usually issue a sense command to determine the cause of the error indication.

#### Initial Selection Sequence

The initial selection sequence for the sense command is almost identical to the initial selection sequence for the write command. When the sequence

proceeds to the point where the channel raises command-out and places the sense command on the bus-out lines, the control unit sets the operational-in interlock, the sense command latch, and the service request latch (Figure MD-2). The operational-in trigger is reset at the end of the initial selection sequence, and the control unit disconnects from the channel.

#### Sense Byte Transfer Sequence

The control unit raises the request-in line to the channel when the operational-in trigger is reset because the service request latch is on. The channel and control unit then proceed through a signal sequence identical to a read data transfer sequence to the point where the control unit raises service-in to the channel. Figure MD-6 shows that when the control unit raises service-in with the sense command latch on, the gate sense in line is activated, gating the on-output of the command reject, bus-out check, and equipment channel check latches to the bus-in lines. The off-output (on-output inverted) of the ready latch is also gated to the bus-in lines at this time. The configuration of the sense byte then indicates just what condition caused the 6-bit to be set in the status byte.

#### Ending Sequence

For the read and write commands, the control unit disconnects from the multiplexor channel after a byte is transferred to or from the channel. This disconnect does not occur between the sense byte and the final status byte for the sense command. The operational-in trigger is reset when the operational-in interlock turns off (not operational-in interlock - Figure MD-2) but the command latch is not reset by service-in AND'ed with service-out while the sense command latch is on (Figure MD-2).

In Figure MD-4, sense command is AND'ed with service-in and service-out to set both the channel-end and device-end latches. The channel-end latch activates the status conditions line, and in Figure MD-2 the status conditions line sets the status-in trigger when the service-in trigger is reset.

Therefore, as soon as the channel accepts the sense byte by replying to service-in with service-out, the control unit sets the channel end and device end latches (Figure MD-4), resets the service-in trigger (Figure MD-3), and sets the status-in trigger (Figure MD-2) to present the channel end and device end status bits to the channel. When the channel replies to the service-in with service-out the operation is complete.

## CONTROL COMMANDS

There are two control commands: control alarm and control no-op. Both cause only an initial selection sequence to take place. The channel end and device end status bits are included in the initial selection status byte. Initial selection for these two commands proceeds the same as the initial selection for the write commands to the point where the channel raises command out and places the command byte on the bus-out lines.

When the control unit raises the sense gate (Figure MD-2), the control command byte bit configuration activates the control line (Figure MD-4) to set both the channel end and the device end latches. These two latches being on when the status-in trigger (Figure MD-2) is set allows the status byte to contain both the channel end and device end status bits.

The only difference between the two commands is the 4-bit. The control alarm command contains the 4-bit, while the control no-op command does not. Control no-op is a programming aid producing no useful function within the control unit or 1052. Control alarm activates an alarm bell once each command. Figure MD-4 illustrates the control alarm line that fires a 20-millisecond single shot to pick the controlling duo relay and five-second timer relay.

## TEST I/O COMMAND

The test I/O command is issued to interrogate the status of the control unit. An initial selection sequence will complete the operation. The channel raises service-out in reply to status-in to end the operation.

The test I/O latch (Figure MD-2) is set during the time that command-out is up. Not initial select trigger resets the test I/O latch as soon as the initial selection sequence is completed. If the test I/O command is issued while the control unit is executing a read, write, or sense command, the channel control examines the unit control word and recognizes that a previous operation is in progress. Initial selection does not take place; the channel itself sets the busy bit.

Test I/O clears any of the following pending interrupt conditions: attention status, device end status, channel end status, and status stacked. The busy bit is not included in the status byte when any of these four conditions are cleared.

## HALT I/O

Halt I/O is not a command in the same sense as read, write, sense, test I/O, and control. These five



commands result in at least an initial selection sequence, with the channel placing a command byte on the bus-out lines while raising the command-out line. Halt I/O is, instead, a condition of the interface lines where address-out and operational-in are up while select-out is down.

This condition is generated by the channel to stop a read or write operation currently in progress. The halt I/O latch (Figure MD-4) is set by operational-in trigger AND'ed with address-out and not select-out. These three conditions result in activating the turn on stop, busy, channel end line. This line sets the stop, busy condition, and channel-end latches. The halt I/O latch activates the general, selective, or I/O disconnect reset line (Figure MD-4), resetting the operational-in and initial select triggers (Figure MD-2), the service request latch (Figure MD-2), and the service-in trigger (Figure MD-3). The halt I/O latch resets when address-out falls.

The channel end latch (Figure MD-4) raises request-in to present channel end status to the channel. This channel end interrupt is cleared by the channel accepting the channel end status byte by replying to status-in with service-out.

#### General or Selective Reset

The general or selective reset lines are illustrated in Figure MD-4. Selective reset affects only the control unit whose operational-in trigger is on. This reset then affects only the one control unit connected to the channel when operational-out is dropped. General reset affects all control units on the channel, since the operational-in trigger is not one of the limiting conditions. CE reset is generated by the CE mode/on line switch (Figure 14) when it is operated through its center position.

#### MISCELLANEOUS CONTROLS

- Request pushbutton
- Ready pushbutton
- Not ready pushbutton

#### Request Pushbutton

The request pushbutton is mounted on the 1052 cover to the right of the keyboard. When operated, it sets the store request and the attention status latches (Figure MD-6). The attention status latch, in turn, activates the attention interrupt line, and the attention interrupt line activates the status conditions line (Figure MD-4). The request-in line is raised to begin a status transfer sequence with the channel in, which the status byte with 0-bit transferred to the channel. The 0-bit then indicates that the request pushbutton has been operated.

Note the store request latch in Figure MD-6. The store request latch and the request PB interlock to the left form a single reset-dominant-latch configuration. The store request latch is reset by the reset attention stored line, and the request PB interlock is reset by the inverted request pushbutton line.

The store request latch may be reset within nanoseconds after the request pushbutton is operated, and the operator may still be holding the pushbutton after the reset drops. When this condition occurs, the request PB interlock prevents the pushbutton from setting the latch again. The pushbutton must be released and depressed once more to set the store request latch again.

#### Ready and Not Ready Pushbuttons

The ready and not ready pushbuttons are mounted on the 1052 cover to the right of the keyboard. The ready pushbutton sets the ready latch (Figure MD-6) and the not ready pushbutton resets the ready latch. The ready latch may also be reset by the end-of-forms contacts when the printer runs out of paper.

A 6-bit is set into the status byte by the unit check latch when the ready latch is reset. When the ready latch is first set, it fires a single shot to set the store device end latch (Figure MD-4). The device end interrupt line then requests a status transfer sequence from the channel to signal the channel that the 1052 is ready; no sense bits are set. Depressing the ready pushbutton causes the print ball to rotate to the same case position (upper or lower) established by the U/L case latch.

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## INTRODUCTION

- 1052-7 Printer-Keyboard
- 1052 Adapter
- Power supply
- Power control panel
- Remote operator control panel (optional)
- Multiplex and selector channel application

The 2150 Console (Figure 17) controls the flow of data originating from a multiplex or selector channel and intended for printout on the 1052-7 Printer-Keyboard. It also controls data that is entered, via the 1052-7 Printer-Keyboard, for processing by a CPU in a System/360 Models 50, 65, 67, and 75.

The 2150 Console comprises a 1052-7 Printer-Keyboard that serves as the console's I/O device and the 1052 Adapter (consisting of two SLT boards) that enables an I/O channel (multiplex or selector) to communicate with the I/O device. In addition, the 2150 Console is equipped with a power supply, an associated power control panel, and a cooling fan mounted on its rear gate. The power control panel

controls the power supply voltages used to power the 1052 Adapter and the 1052-7 Printer-Keyboard. The unit can also be equipped with one or two remote operator control panels, each of which is connected to a separate CPU. The ROCP's, however, are provided on an optional basis and are not connected with the console's control unit logic.

## SELECTOR CHANNEL OPERATION

- The 2150 Console is attached to a selector channel on Models 50, 65, 67, and 75.
- The I/O interface sequence consists of three different parts:
  1. Initial Selection
  2. Data Transmission
  3. Ending Sequence
- The selector channel and 2150 Console remain interlocked during all three parts of the interface sequence.
- The channel holdout and select-out lines remain up during the entire operation.

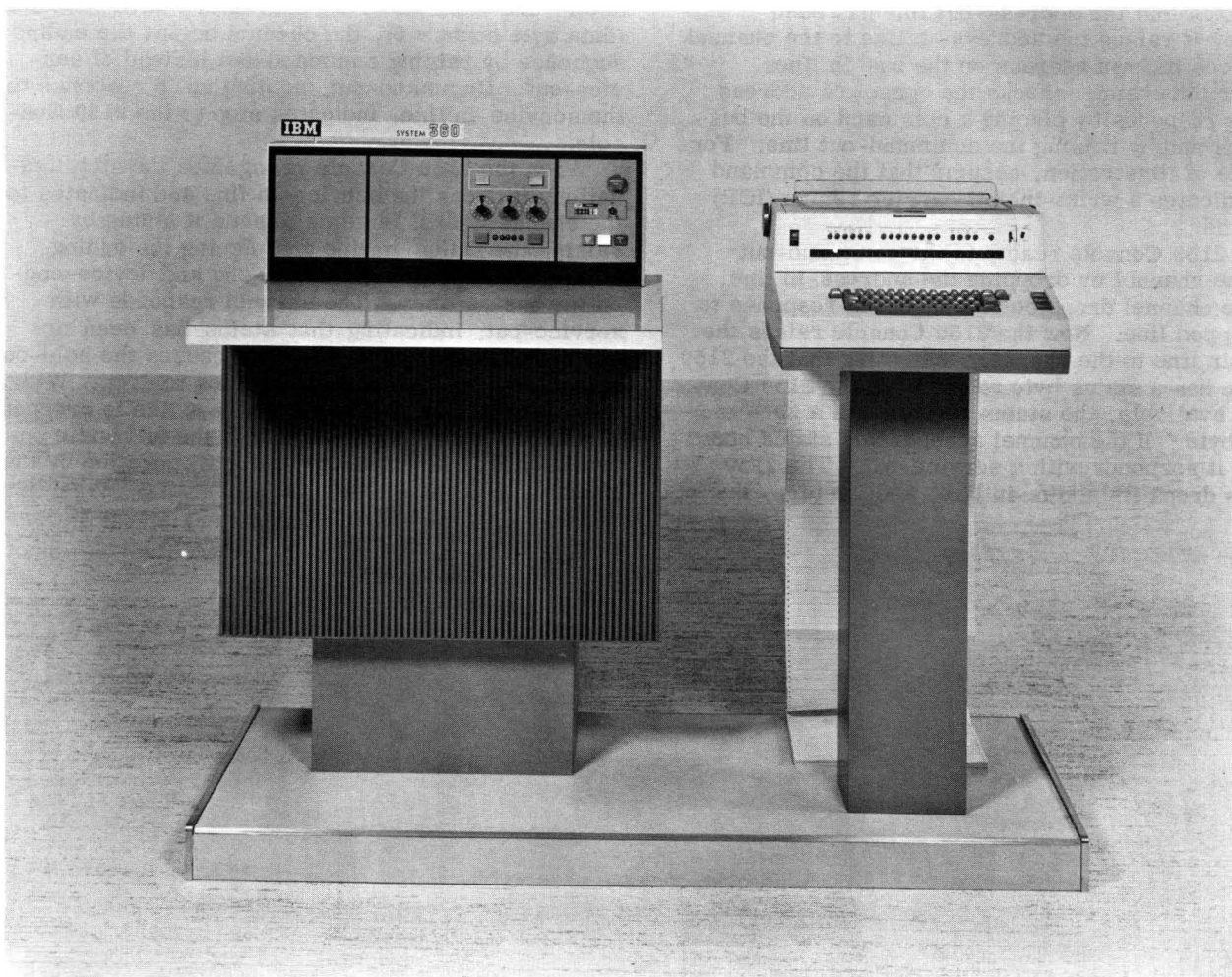


FIGURE 17. 2150 CONSOLE UNIT

- The 2150 Console operational-in line also remains up during the entire operation.
- The data transmission sequence is simply service in - service out for each data byte, since channel and console are interlocked.
- The end sequence is simplified to command-out at byte count = 0, status-in, service-out.

### Initial Selection

Selection of the 2150 Console, when attached to a selector channel, commences when the channel places the address of the 2150 Console on bus-out and then raises the address-out lines. Assuming that the 2150 Console matches the address present on the bus-out lines, the address-out line causes the initial-selection and address-in triggers to be set. The channel then issues the select-out signal (select-out and hold-out are AND'ed in the 2150) to the 2150 Console. This signal causes the operational-in trigger to be set, thus raising the operational-in line and inhibiting propagation of the select-out line to other units that may also be connected to the channel. When the operational-in line rises and is sent to channel, the channel responds by dropping address-out. When the 2150 Console recognizes that the address-out line has been dropped, it raises the address-in line to the channel and places its own address on the bus-in lines.

After the channel checks the console's address byte, it responds by placing a command on the bus-out lines and by raising the command-out line. For the sake of illustration, assume that the command byte indicates a write-inhibit carrier return (ICR) command.

The 2150 Console reacts to the command-out from the channel by dropping the address-in line; then the channel drops command-out in response to the dropped line. Now the 2150 Console raises the status-in line to the channel, indicating that the 2150 Console has a status byte to send. If the 2150 Console is available, the status reflected is a zero status byte. If the channel accepts this status condition, it responds with a service-out. The 2150 console drops its status-in line, and, in turn, the

channel drops its service-out line to complete the initial-selection sequence of the 2150 Console by a selector channel.

### Data Transmission

At the termination of the initial-selection sequence, the 2150 Console will raise its service-in line to request data from the channel. The channel places the data byte on bus-out and signals the 2150 Console with service-out. The control unit receives both the data byte and the service-out line and, in turn, drops the service-in line. This completes the transfer sequence of one data byte from the channel to the 2150 Console. When the 1052-7 Printer has finished printing the character, the 2150 Console raises its service-in line to begin the next data-transfer sequence of the succeeding character from the channel.

### Ending Sequence

The data-transfer sequences continue until all of the characters to be sent by the channel have been received by the 2150 Console. When the 2150 Console raises its service-in line, requesting another character, and when all of the characters have been sent (data byte count = 0), the channel begins the ending sequence by raising command-out instead of service-out. Command-out, coming up in response to the service-in line, indicates stop to the 2150 Console.

When the 2150 Console recognizes the stop indication, it drops the service-in line and indicates to the channel that it is going to send its status by raising the status-in line and placing the ending status byte containing channel-end and device-end on the bus-in lines. The channel responds with service-out, indicating that status has been accepted. The rise of service-out causes the hold-out, select-out, and operational-in lines to drop. With the fall of the latter, the service-out line is dropped. The 2150 Console is finished with the full write operation and is now free for another operation by the channel.

This section pertains to the theory of operation of the 2150 Console when it is attached to a selector channel of a System/360. The information reflects the commands that are unique to the 2150 Console and the operations caused by the commands. The seven valid commands and their respective byte configurations are as follows:

Commands	Bit Configuration								
	P	0	1	2	3	4	5	6	7
Test I/O	1	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	0	1	0	0
Control No-Op	0	0	0	0	0	0	0	1	1
Control Alarm	0	0	0	0	0	1	0	1	1
Write Auto Carrier Return	1	0	0	0	0	1	0	0	1
Write-Inhibit Carrier Return	0	0	0	0	0	0	0	0	1
Read	0	0	0	0	0	1	0	1	0

All other command byte bit configurations with correct parity are considered invalid commands. Figures MD-2 through MD-6 are simplified diagrams, illustrated in positive logic form, that show the circuits in a sequence that corresponds to the I/O interface signal sequence for the command being described. In addition, timing charts for each command operation are provided.

#### WRITE

- Initial-selection sequence
- Data-transfer sequence
- Ending sequence

#### Initial-Selection Sequence

The initial-selection sequence for the write operation (write-ICR or write-ACR) is begun by the channel and is illustrated in Figures 18 and MD-2. The channel raises the select-out, hold-out, and address-out lines and places the address byte of the console control unit on the bus-out lines. The console control unit matches the address byte with the internally plugged address; if they match, the address-match line is activated and AND'd with address-out to turn on the initial-select trigger and the address-in trigger. The on-output of the address-in trigger turns on the operational-in trigger to raise the operational-in line to the channel.

The channel drops the address-out line to the console control unit when it receives the operational-in line from the control unit. When address-out drops, the control unit raises the address-in line to the channel and gates the output of the address bit

generator to the bus-in lines, thus generating the address-in byte.

The channel receives the address byte and the address-in line and responds by placing a command byte on the bus-out lines and raising the command-out line. The command-out line from the interface (command-out cable out) AND's with the on-output of the operational-in trigger to raise the command-out line to the console control unit. A few nanoseconds after command-out is raised, the command-out delay line becomes active. The delay is the result of passing command-out through two inverters, each of which introduces the delay of a few nanoseconds in the signal.

Command-out sets the operational-in interlock and activates the command gate. The command gate raises the sense gate; the sense gate, in turn, raises the write gate. The write gate then sets the write-command latch (the bit configuration of the command byte having activated the valid-command and write-command bits) and the service-request latch.

Command-out delay resets the address-in trigger, dropping address-in to the channel. When the channel recognizes the dropped address-in line, it drops command-out. The inactive command-out line now turns on the status-in trigger in the control unit. The status-in trigger raises status-in to the channel and gates the status byte to the bus-in lines.

The channel receives the status-in line and the status byte and replies with service-out, indicating acceptance of the status byte. The initial-selection sequence is complete at this point.

#### Data-Transfer Sequence

The service-request latch is set during the initial-selection sequence (Figures 18 and MD-2), but its on-output is not used until the end of the initial-selection sequence. Further, the write-command latch, having been set during the initial-selection sequence, remains set throughout the data-transfer sequence. Consequently, the output of this latch is AND'd with the output of the initial-selection trigger (which is in the reset state) to turn on the busy-condition latch (Figure MD-3). This function occurs at the end of the initial-selection sequence. The output of this latch is AND'd with the service-request, operational-in trigger, not-address-in trigger, and not-command or service-out to set the service-in trigger. The service-in trigger raises service-in to the channel, indicating that the 2150 Console is ready for a data byte.

The channel replies to service-in with service-out and places a data byte on the bus-out lines. The 2150 Console AND's service-in and service-out to activate service-response (Figures MD-3 and 19) and start the read/write clock at SS 1 (Figure 20). SS 1 gates the data byte from the bus-out lines to the data register. The clock runs through SS 7 to complete the operation by gating the output of the data register through the printer translator and/or function decoder.

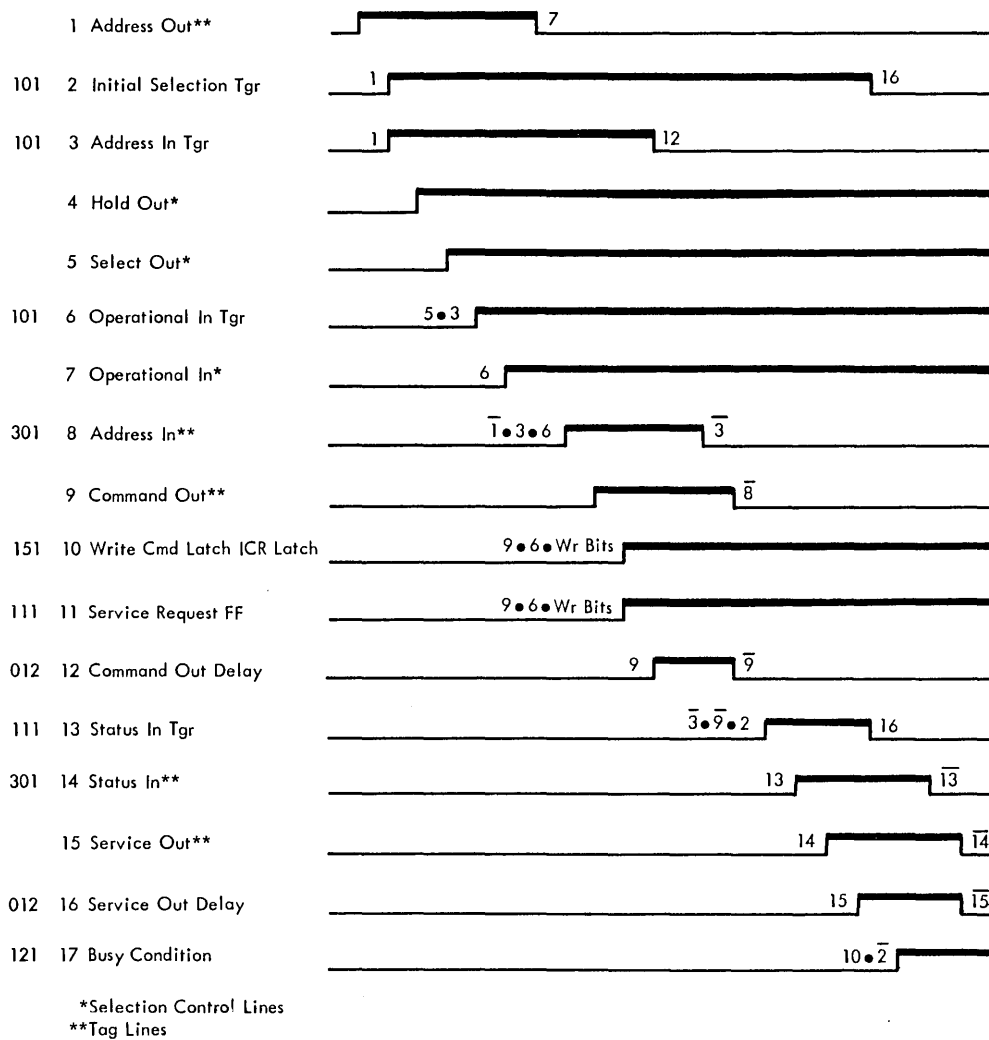


FIGURE 18. INITIAL-SELECTION SEQUENCE, WRITE-INHIBIT OR WRITE-AUTO CARRIER RETURN, SELECTOR CHANNEL

SS 2 is AND'ed with not-printer-busy, write, and not-stop to reset the service-in trigger and drop the service-in line to the channel (Figure MD-3). The channel then drops service-out, and the data-transfer sequence is complete. SS 6 is AND'ed with not-end-of-line, write, not-busy or stop, not-service-in, and service-out to activate the service-request latch. In turn, the latch output is AND'ed with the output of the busy-condition trigger, together with the operational-in trigger output, the not-address-in trigger, and not-command or service-out, to turn on the service-in trigger (Figure MD-3). The service-in line is again raised to begin a new data-transfer sequence with the channel. The data-transfer sequences are continued until an ending sequence occurs in place of a data-transfer sequence.

#### Ending Sequence

The write-ICR and write-ACR commands are distinguished by the ending sequences. The inhibit-carrier-return latch is set during the initial

selection for the write-ICR command, allowing the control unit to present the channel-end and device-end status bits to the channel during the same ending sequence.

The write-ACR command does not set the inhibit-carrier-return latch during the initial selection. Therefore, only the channel-end status bit is presented to the channel during the first ending sequence. The carrier is started moving to the left margin at about the same time that the channel-end status is presented to the channel. A second ending sequence is required to present the device-end status bit to the channel when the carrier reaches the left margin and stops moving.

#### Write-ICR

The inhibit-carrier-return latch is set during the initial-selection sequence. The write gate (activated by command-out) AND's with not-bus-out 4 to set the inhibit-carrier-return latch while the command byte is on the bus-out lines (Figure MD-4). The service-in line is activated to the channel at the

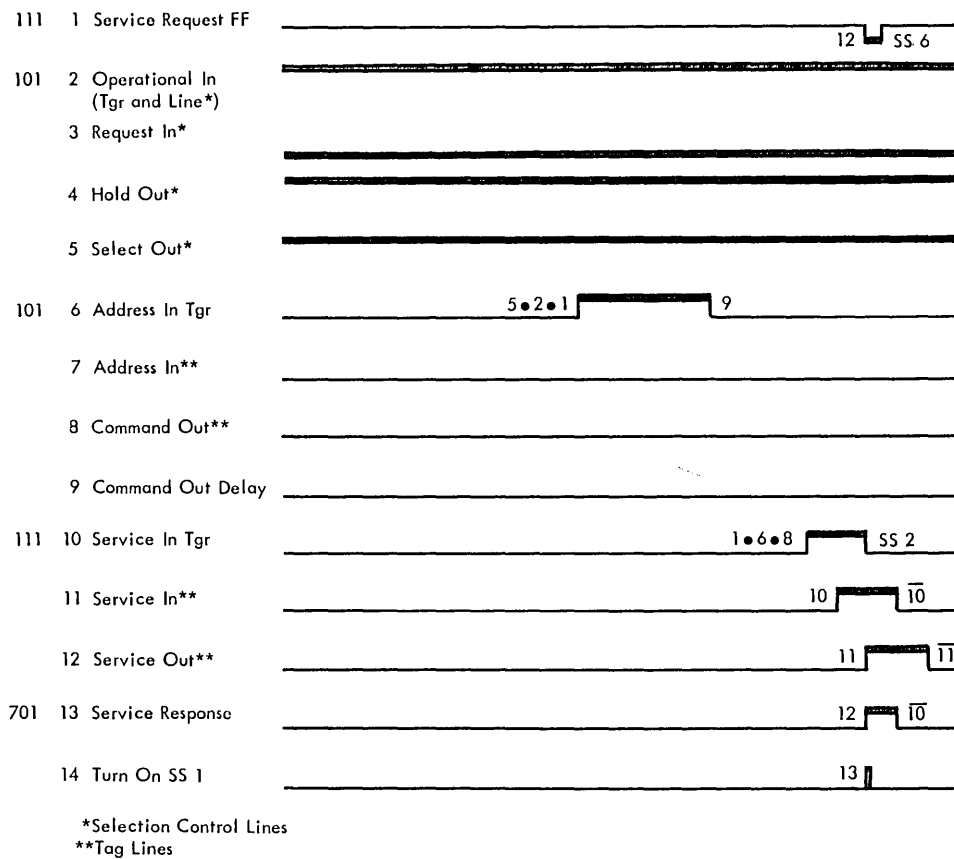


FIGURE 19. SEQUENCE DURING DATA TRANSMISSION, WRITE-INHIBIT OR WRITE-AUTO CARRIER RETURN, SELECTOR CHANNEL

end of the previous data-transfer sequence (Figure MD-3). The channel, however, has no more data to send to the console control unit (channel byte count has gone to zero). The following signal sequence occurs. Thus, the channel raises command-out as a reply to service-in instead of service-out. A command-out reply to service-in indicates stop (Figure 21).

Figure MD-4 illustrates the ending sequence for both write-ICR and write-ACR. Service-in and command-out are AND'ed together to activate write/read turn-on channel-end. Write/read turn-on channel-end sets both the channel-end and the stop latches. The on-output of the stop latch sets the store-device-end latch. The on-output of the store-device-end latch activates device-end-interrupt, which sets the device-end latch.

In Figure MD-3, the service-in trigger is reset when the channel replies to service-in with command-out. The channel then drops command-out when service-in drops. In Figure MD-4, the channel-end latch activates the status-conditions line, and status-conditions AND's (Figure MD-2) with the operational-in trigger, not-address-in trigger, not-service-in trigger, and not-command or service-out to set the status-in trigger and raise the status-in line to the channel. The on-outputs of the status-

bit latches are gated to the bus-in lines at the same time.

#### Write-ACR

The ending sequence for the write-ACR operation begins the same as the ending sequence for write-ICR. The major difference is that the inhibit-carrier-return latch is not set during the initial selection. When the ending sequence reaches the point where the channel replies to service-in with command-out, indicating stop, the write/read turn-on channel-end line (Figures MD-4 and 22) sets both the channel-end and stop latches. The channel-end latch again activates the status-conditions line, and the status-conditions line again sets the status-in trigger (raising status-in to the channel) when command-out falls.

Because the inhibit-carrier-return latch is off, the carrier-return latch is set (stop AND'ed with not-printer-busy and not-inhibit-carrier-return - Figure MD-3) and the read/write clock is started at cycle time. Cycle time then sets the printer-busy latch, picks the carrier return-line feed magnet in the printer, and picks the lower-case shift magnet in the printer if the printer was in upper case. The

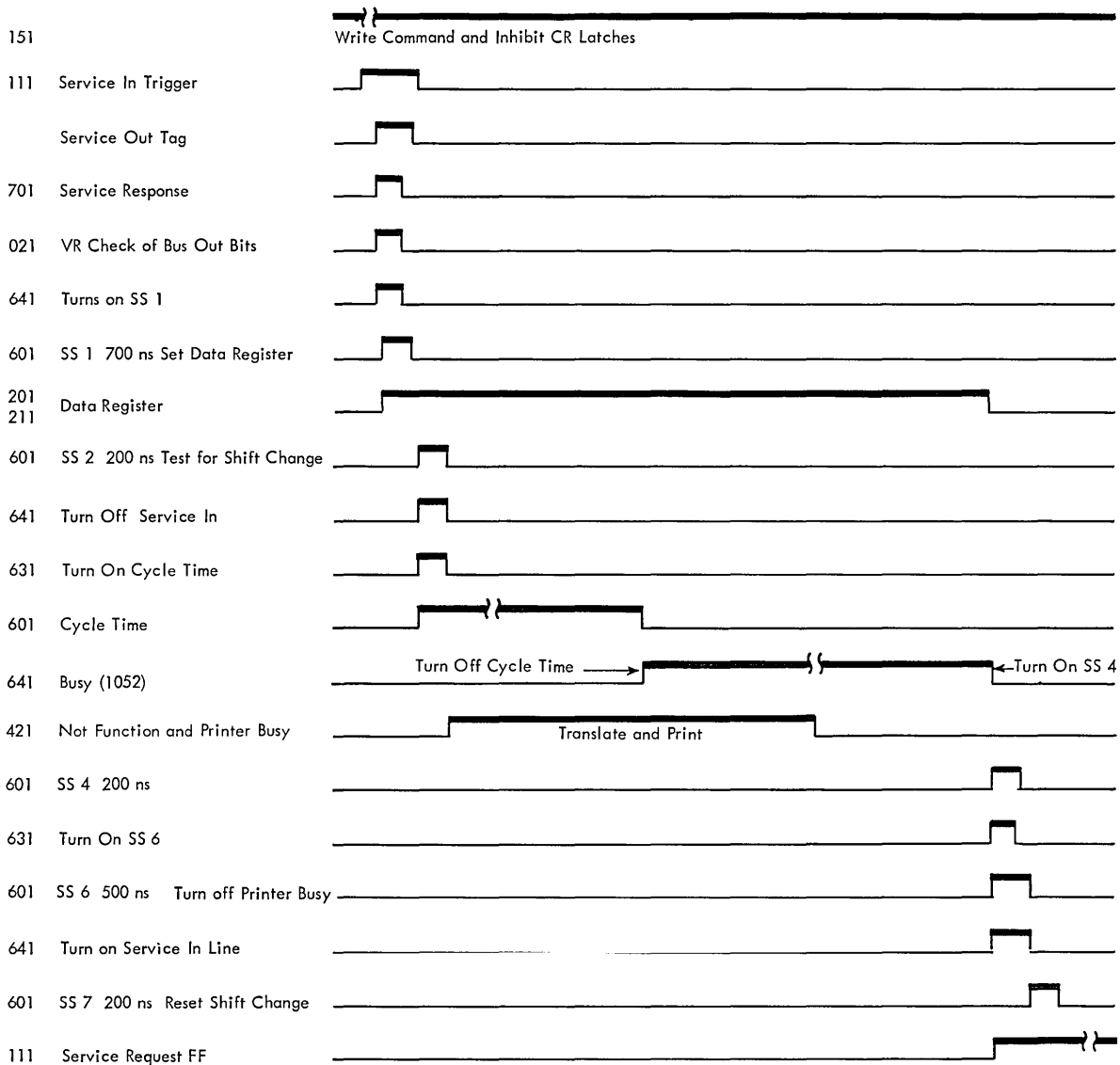


FIGURE 20. PRINT CYCLE FOR WRITE OPERATION, NO SHIFT, SELECTOR CHANNEL

busy latch now AND's with stop and carrier-return to set the inhibit-carrier-return latch (Figure MD-4)

#### Device End Status Presentation

Up to this point, the channel-end status bit has been sent to the channel and the carrier has started returning to the left margin, but the device-end status bit has not been sent to the channel. The turn-on device-end line becomes active (to set the store-device-end latch, Figure MD-4) when the carrier has finished returning to the left and the carrier-in-motion latch is reset. The on-output of the store-device-end latch then activates device-end interrupt which, in turn, activates the status-conditions line

to raise request-in to the channel (Figures MD-4 and 23).

The following sequence occurs: control unit raises request-in to the channel; channel raises hold-out and select-out; console control unit raises hold-out and select-out; console control unit raises operational-in and address-in, and places its address byte on the bus-in lines; channel raises command-out; control unit drops address-in; channel drops command-out.

The device-end interrupt line has been active during the above sequence, and device-end interrupt has kept the status-conditions line active. When channel drops command-out, the status-in trigger (Figure MD-2) is set by the status-conditions line.



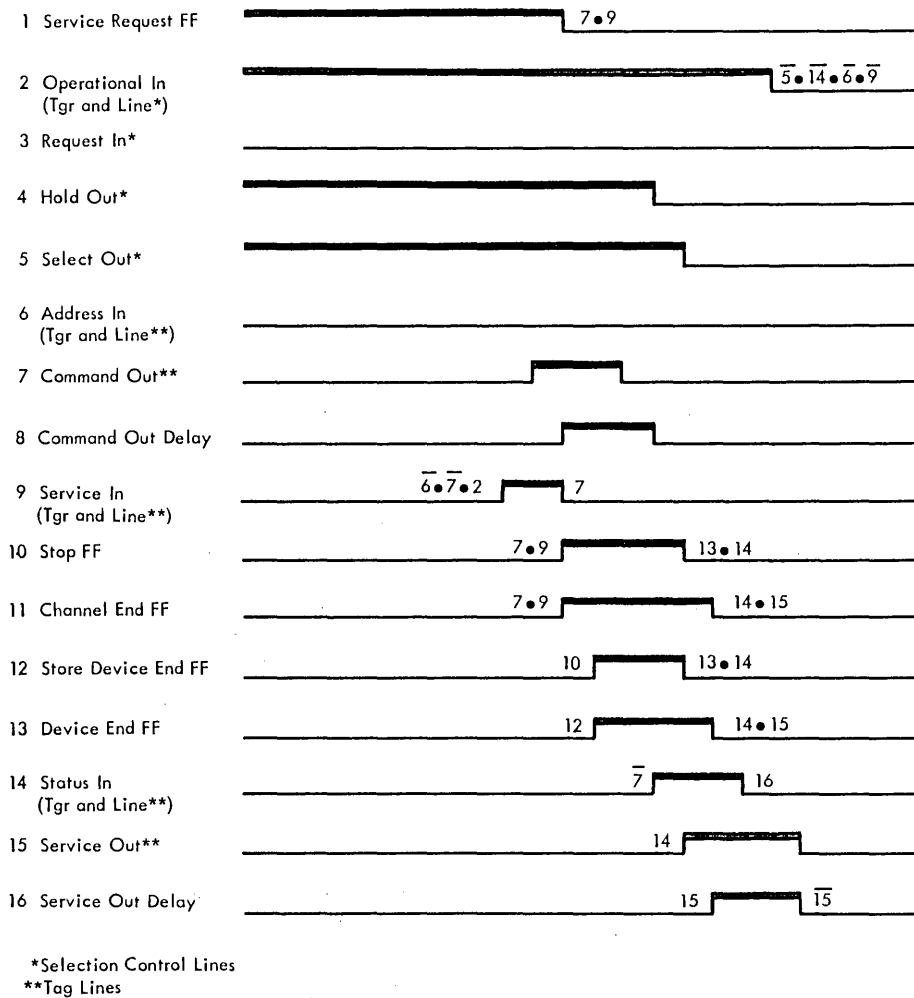


FIGURE 21. ENDING SEQUENCE, WRITE-INHIBIT CARRIER RETURN, SELECTOR CHANNEL

Status-in is raised to the channel, and the on-output of the device-end latch is gated to the bus-in lines as the device-end status bit. Channel rejects the status by replying to status-in with command-out and suppress-out, and the status is stacked.

If the CPU does not allow the channel to take an interrupt at this time, the channel leaves suppress-out up, thus suppressing further status presentation.

If the CPU allows the channel to take an interrupt at this time, the channel hardware will cause a "pseudo" test I/O operation, thereby enabling the channel to accept the status of the control unit.

## READ

- Initial-selection sequence
- Data-transfer sequence
- Ending sequence

### Initial Selection

Initial selection for the read command is almost identical with that for the write command. The in-

hibit-carrier-return latch is not set during the initial-selection sequence because the read-command byte contains the 4 bit. The read-command latch (Figure MD-2) is set while command-out is up and the read command byte is on the bus-out lines. Note that the service-request trigger is not set at command-out time during the initial-selection sequence. Recall that for the write command the service-request latch was set by command-out and the write-command byte. This led to the first data-transfer sequence.

### Data Transfer

The 1052 keyboard is unlocked when the read-command latch is set. Figure MD-5 shows the circuits used for the data-transfer sequence of the read command. When a key is operated at the keyboard, the keyboard-strobe line becomes active and is AND'ed with read to start the read/write clock at SS 5. (See Figure 24). SS 5 resets the data register, and SS 6 sets the output of the keyboard translator in the data register (see Figure 4 in Functional

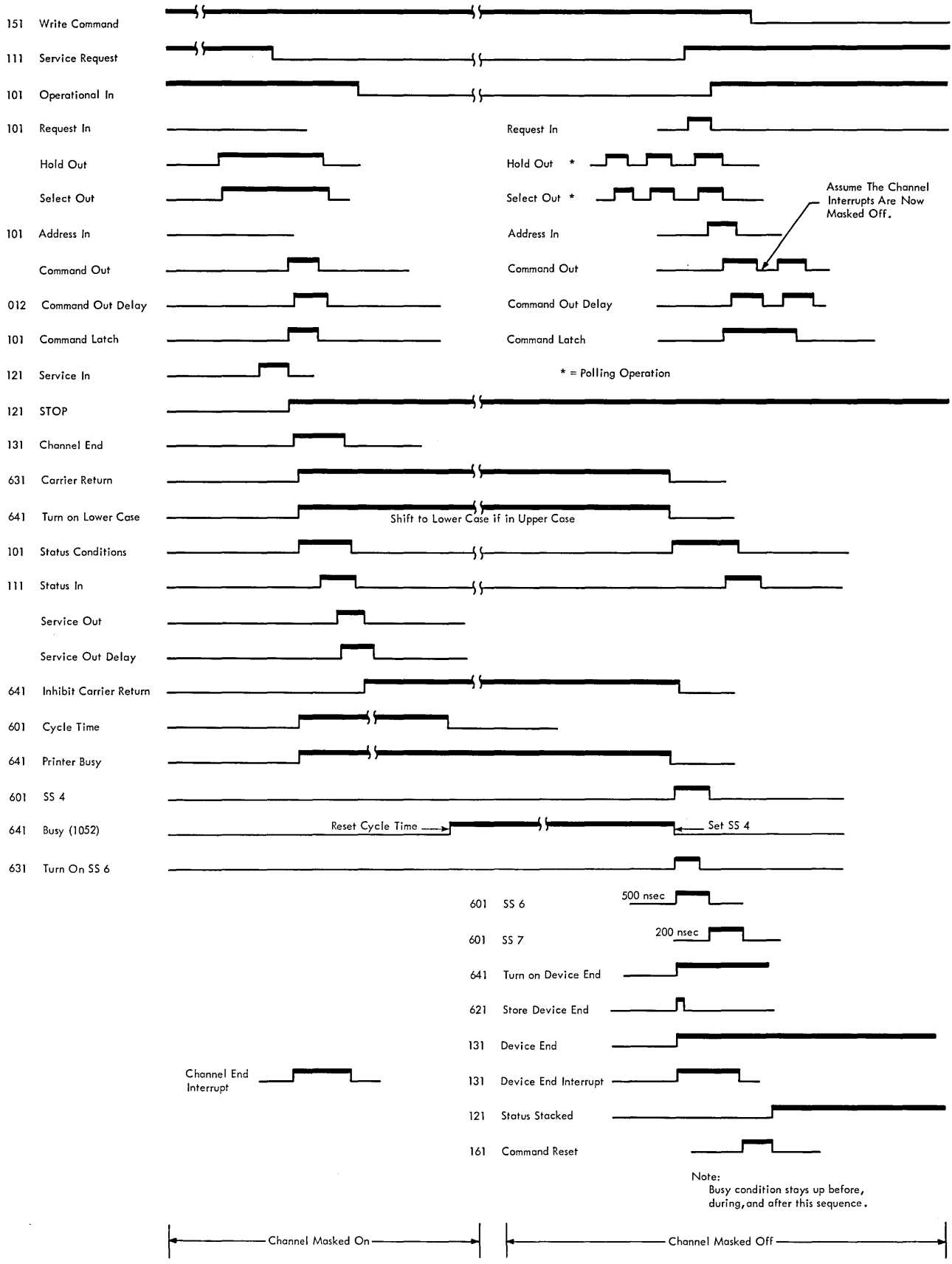


FIGURE 22. WRITE-AUTOMATIC CARRIER RETURN, END SEQUENCE, SELECTOR CHANNEL

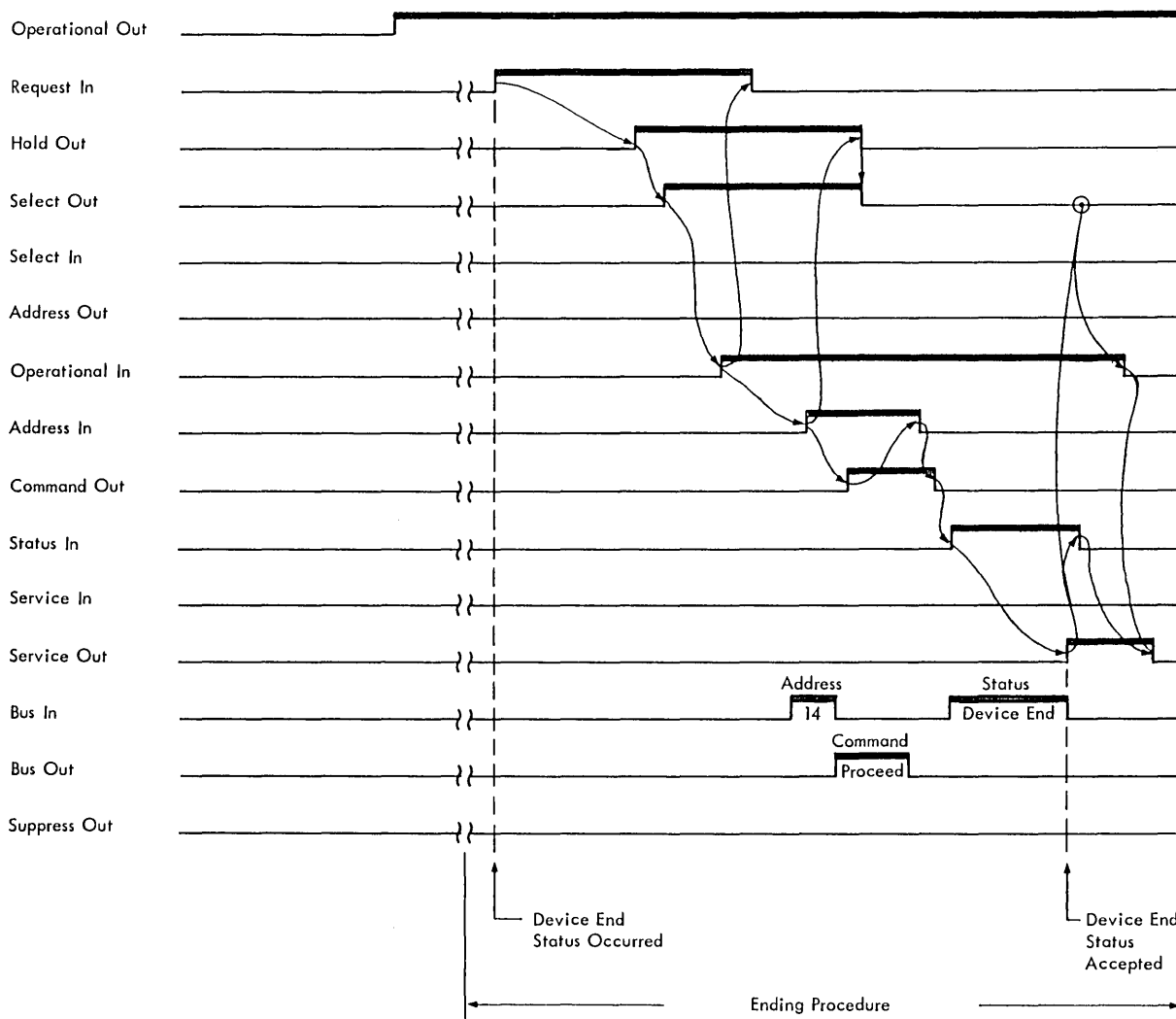


FIGURE 23. CONSOLE UNIT-INITIATED SELECTION SEQUENCE FOR ENDING PROCEDURE, SELECTOR CHANNEL

Units section). SS 7 AND's with not-shift-change, keyboard-strobe, and not-stop to turn on service-in and to set the service-request latch (Figure MD-5). Service-request, in turn, activates status-conditions and status-conditions raises the request-in line to the channel.

The channel replies to the request-in with select-out and hold-out, and the data-transfer sequence proceeds the same as the data-transfer sequence for the write command, with one exception. For the write command, data is placed on the bus-out lines by the channel when the channel raises service-out. For the read command, the control unit places data on the bus-in lines when the control unit raises service-in. The last character stored in the data register is not printed because the clock is not started, nor is it gated to the channel.

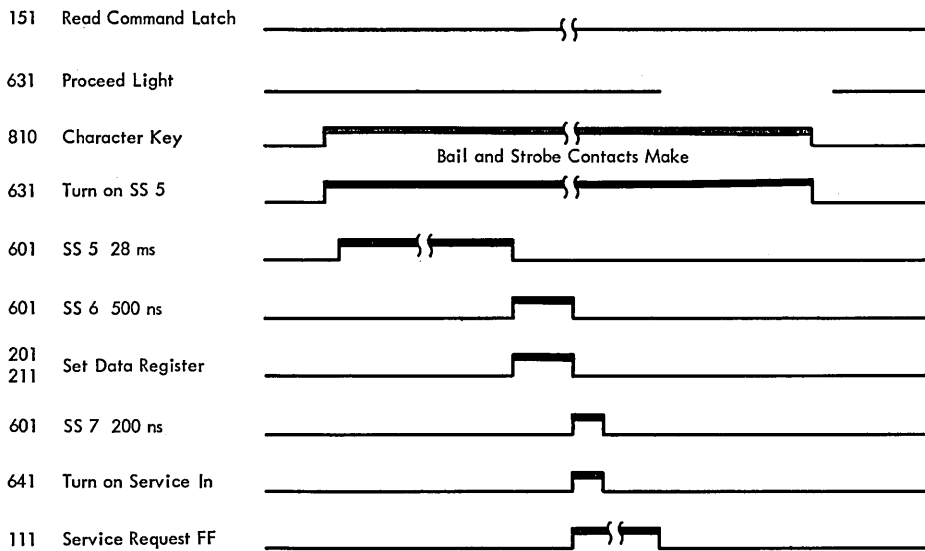
With respect to Figure MD-2, select-out AND's with request-in to set the address-in trigger, and the address-in trigger, in turn, sets the operational-in trigger, raising operational-in to the channel. Because address-out is not active when operational-in comes up, the console control unit raises address-

in and gates its own address to the bus-in lines. Channel replies to address-in with command-out, and command-out delay drops the address-in line by resetting the address-in trigger. Channel drops command-out because the console control unit drops address-in. The service-in trigger is set when command-out falls, raising the service-in line to the channel and gating the output of the data register to the channel.

Channel responds to service-in with service-out, and the console control unit AND's service-in with service-out to activate service-response to start the read/write clock at cycle time. Cycle time causes the printer to print the character in the data register or to perform the function called for by the character in the data register. The output of the keyboard has now been transferred to the channel and the printer, and the sequence is complete.

#### Ending Sequence

The ending sequence is similar to that for the write-ACR command, but can be started three different



The intervening signals and timing depend on the type of channel.

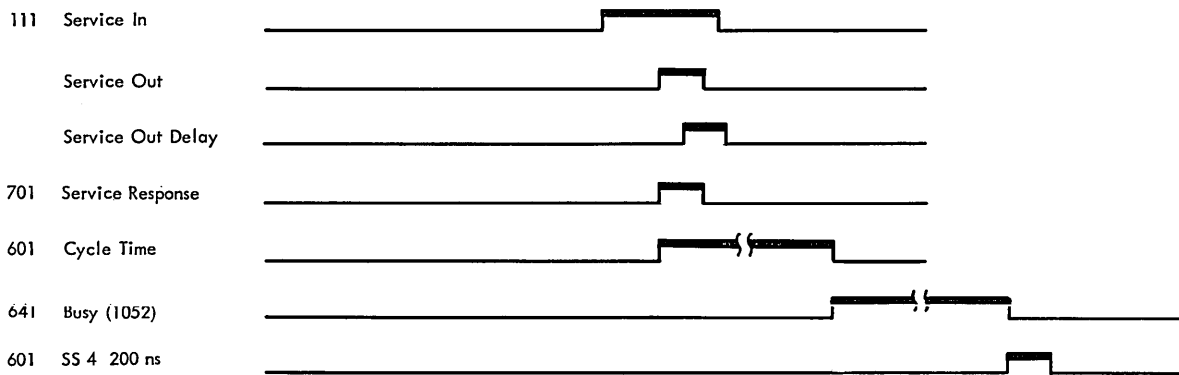


FIGURE 24. PRINT CYCLE FOR READ OPERATION, NO SHIFT, SELECTOR CHANNEL

ways. First, the console control unit can try to send one more data byte to the channel after the channel byte count has gone to zero. In this event, the sequence described under data transfer proceeds to the point where the character is stored in the data register and the console control unit raises request-in. Channel makes a reply to service-in from the console control unit. Instead of replying with service-out as during the data-transfer sequence, channel replies with command-out, indicating stop. From this point on, the ending sequence is identical with that for the write-ACR command. Service-response is not generated (Figure MD-5) to start the read/write clock because service-out is not given as a reply to service-in. The last character stored in the data register is not printed because the clock is not started, nor is it accepted by the channel.

The second means of obtaining the ending sequence for the read command is through the use of

the EOB signal. When the operator has finished keying in data, if the byte count in the channel has not previously gone to zero he may end the read operation by holding the alternate coding key down while operating the numeric 5 key. This causes the EOB line shown in Figure MD-4 to activate the write/read turn-on channel-end line. From this point on, the ending sequence proceeds exactly the same as the ending sequence described in the preceding paragraph.

The third means of obtaining the ending sequence for the read command is through the use of the cancel signal. If the operator has made a keying error, he may cause the channel to ignore the block of data in which the error was made. The operator holds the alternate coding key down while operating the numeric 0 key. This action activates the cancel line in Figure MD-4 and causes the ending sequence to proceed as described in the first paragraph of this section.

## SENSE COMMAND

- Sense byte format
- Sense byte description
- Initial-selection sequence
- Sense byte transfer sequence
- Ending sequence

The sense command is normally issued following an error indication in the status byte of an ending sequence for either a read or write command. If the status byte contains the unit check (6) status bit, the programmer may, at his own discretion, issue a sense command to determine the cause of the error indication.

The sense operation consists of initial selection followed by a combined data transfer and end sequence. The sense byte is transferred to the channel during the data-transfer sequence.

### Sense Byte Format

The sense byte format is as follows:

<u>Bus Position</u>	<u>Indications</u>
P	Parity
0	Command Reject
1	Intervention Required
2	Bus Out Check
3	Equipment Check
4	Not Used
5	Not Used
6	Not Used
7	Not Used

### Sense Byte Description

The 2150 Console utilizes only four sense bits (0 through 4) of the sense byte. Bits 4, 5, 6, and 7 remain in their zero states. The sense byte generated to the channel must contain odd parity.

Sense Bit 0 - Command-Reject indicates that the 2150 Console detected a programming error.

Command-reject will be set if a command is generated and the 2150 Console is not designed to execute it (invalid command).

Sense Bit 1 - Intervention-Required is generated when the last operation could not be executed by the 2150 Console because of a condition requiring intervention. Intervention-required is also turned on when the 2150 Console is in the not-ready state, is in a test mode, or the printer is out of forms.

NOTE: The intervention-required condition will not terminate a read or write operation that is already in progress.

Sense Bit 2 - Bus Out Check indicates the 2150 Console received a command code or data byte with invalid parity over the I/O interface. The bus-out-check bit is set when one of the following occurs:

1. A command code with invalid parity is detected at the 2150 Console during a channel-initiated selection and the console is not in a busy condition.
2. Invalid parity is detected on a data byte during a write operation.

Sense Bit 3 - Equipment Check is caused when the 2150 Console has detected an equipment malfunction during an operation.

Normally, data transmission stops and the operation in progress is terminated. The equipment-check bit is set when one of the following occurs:

1. Invalid parity is detected from the keyboard during a read operation.
2. There is an error between the BCD output and the tilt-rotate output during a read operation.

### Initial-Selection Sequence

The initial-selection sequence for the sense command is almost identical with the initial-selection sequence for all commands. The channel raises the select-out, hold-out, and address lines, and places the address byte of the console control unit on the bus-out lines. The console control unit matches the address byte with the internally plugged address; if the two match, the address-match line is activated and AND'ed with address-out to turn on both the initial-selection trigger and the address-in trigger. The on-output of the address-in trigger turns on the operational-in trigger to raise the operational-in line to the channel.

The channel drops the address-out line to the console control unit when it receives the operational-in line from the console control unit. When address-out drops, the control unit raises the address-in line to the channel and gates the output of the address bit generator to the bus-in lines, thereby generating the address-in byte.

The channel receives the address byte and the address-in line and responds by placing the sense command byte (0 0000 0100) on the bus-out lines and raising the command-out line. The command-out line from the interface (command-out cable out)

AND's with the on-output of the operational-in trigger to raise the command-out line to the console control unit. A few nanoseconds after command-out is raised, the command-out delay line becomes active. Command-out sets the operational-in interlock and activates the command gate. The command gate raises the sense gate, and the sense gate and sense command bits (6, 7) are AND'ed to set the sense-command latch (the bit configuration of the command byte having activated valid and sense-command bits) and the service-request latch.

Command-out delay resets the address-in trigger, dropping address-in to the channel. When the channel recognizes the dropped address-in line, it drops command-out. The inactive command-out line now turns on the status-in trigger in the control unit. The status-in trigger raises status-in to the channel and gates the status byte to the bus-in line. The channel receives the status-in line and the status byte and replies with service-out, indicating acceptance of the status byte. The initial-selection sequence is completed at this time.

Sense Byte Transfer Sequence

The service-request latch (Figures MD-2 and 25) is set during the initial-selection sequence, but its on-

output is not used until the end of the initial-selection sequence. Further, the sense-command latch, having been set during the initial-selection sequence, will remain set through the sense byte transfer to the channel. Consequently, the output of this latch is AND'ed with the output of the initial-selection trigger (which is in the reset state as a result of command-out and gate-status-in lines being AND'ed) to turn on the busy-condition latch (Figures MD-3 and 23). This function occurred at the end of the initial-selection sequence. The output of the busy-condition latch is AND'ed with service-request, operational-in trigger, not-address-in trigger, and not-command-out or service-out to set the service-in trigger. The output of the service-in trigger is AND'ed with the output of the sense-command latch

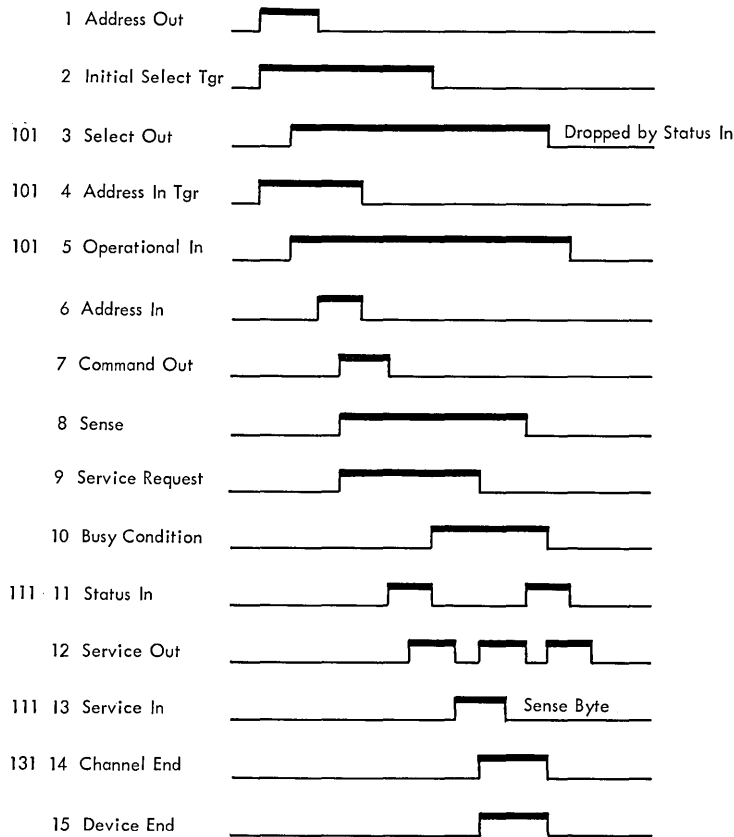


FIGURE 25. SENSE COMMAND OPERATION, SELECTOR CHANNEL

(Figure MD-4) to sample and to gate the sense byte data onto the bus-in lines. In addition, the service-in line to the channel is raised as an indication that the sense byte is present on the bus-in lines. Service-in, service-out, and the output of the sense-command latch (Figure MD-4) are AND'ed to turn on both the channel-end and device-end latches. Thus, with the transfer of the sense byte data, the CE and DE bits of the status byte are set.

### Ending Sequence

The channel begins the ending sequence by responding with service-out, indicating that status has been accepted. The rise of service-out causes the hold-out, select-out, and operational-in lines to drop. With the fall of the operational-in line, the service-out line is dropped. The 2150 Console is finished processing the sense-command operation and is now free for another operation by the selector channel.

### CONTROL COMMANDS

There are two control commands: control alarm and control no-op. Both cause only an initial-selection sequence to take place. The channel-end and device-end status bits are included in the initial-selection status byte. Initial selection for these two commands proceeds the same as initial selection for the write commands, to the point where the channel raises command-out and places the command byte on the bus-out lines.

When the control unit raises the sense gate (Figure MD-2), the control command byte bit configuration activates the control line (Figure MD-4) to set both the channel-end and the device-end latches. These two latches being on when the status-in trigger (Figure MD-2) is set allow the status byte to contain both the channel-end and device-end status bits.

The only difference between the two commands is the 4 bit. The control-alarm command contains the 4 bit, whereas the control no-op command does not. Control no-op is a programming aid performing no useful function within the control unit or 1052. Control-alarm activates an alarm bell once each command. Figure MD-4 illustrates the control-alarm line that fires a 20-ms single-shot to pick the controlling duo relay and five-second timer relay.

### TEST I/O COMMAND

The test I/O command is issued to interrogate the status of the control unit. An initial-selection sequence will complete the operation. The channel raises service-out in reply to status-in to end the operation.

The test I/O latch (Figure MD-2) is set while command-out is up. Not-initial-select trigger resets the test I/O latch as soon as the initial-selection sequence is completed. If the test I/O command is issued while the control unit is completing the ending sequence for a read/write ACR operation, the control unit will generate a busy bit in the status byte.

Test I/O clears any of the following pending interrupt conditions: attention-status, device-end-status, channel-end-status, and status-stacked. The busy bit is not included in the status byte when any of these four conditions are cleared.

### HALT I/O

Halt I/O is not a command in the same sense as read, write, sense, test I/O, and control. These five commands result in at least an initial-selection sequence, with the channel placing a command byte on the bus-out lines while raising the command-out line. Halt I/O is, instead, a condition of the interface lines where address-out and operational-in are up while select-out is down.

This condition is generated by the channel to stop a read or write operation currently in progress. The halt I/O latch (Figure MD-4) is set by the operational-in trigger AND'ed with address-out and not-select-out. These three conditions activate the turn-on-stop, busy, channel-end line. This line sets the stop, busy-condition, and channel-end latches. The halt I/O latch activates the general, selective, or I/O disconnect-reset line (Figure MD-4), resetting the operational-in and initial-select triggers (Figure MD-2), the service-request latch (Figure MD-2), and the service-in trigger (Figure MD-3). The halt I/O latch resets when address-out falls.

The channel-end latch (Figure MD-4) raises request-in to present channel end status to the channel. This channel-end interrupt is cleared by the channel accepting the channel end status byte by replying to status-in with service-out.

### GENERAL OR SELECTIVE RESET

The general or selective reset lines are illustrated in Figure MD-4. Selective-reset affects only the control unit whose operational-in trigger is on. This reset then affects only the one control unit connected to the channel when operational-out is dropped. General reset affects all control units on the channel, since the operational-in trigger is not one of the limiting conditions. CE reset is generated by the CE mode/on line switch (Figure 14) when it is operated through its center position.

### MISCELLANEOUS CONTROLS

- Request pushbutton
- Ready pushbutton
- Not ready pushbutton

#### Request Pushbutton

The request pushbutton is mounted on the 1052 cover to the right of the keyboard. When operated, it sets the store-request and the attention-status latches. (Figure MD-6). The attention-status latch, in turn, activates the attention-interrupt line which activates the status-conditions line (Figure MD-4). The request-in line is raised to begin a status-transfer

sequence with the channel in, which the status byte with 0-bit transferred to the channel. The 0 bit then indicates that the request pushbutton has been operated.

Note the store-request latch in Figure MD-6. The store-request latch and the request PB interlock to the left form a single reset-dominant-latch configuration. The store-request latch is reset by the reset-attention-stored line, and the request PB interlock is reset by the inverted request-pushbutton line.

The store-request latch may be reset within nanoseconds after the request pushbutton is operated, and the operator may still be holding the pushbutton after the reset drops. When this condition occurs, the request PB interlock prevents the pushbutton from resetting the latch. The pushbutton must be released and depressed once more to set the store-request latch again.

### Ready and Not Ready Pushbuttons

The ready and not ready pushbuttons are mounted on the 1052 cover to the right of the keyboard. The ready pushbutton sets the ready latch (Figure MD-6), and the not ready pushbutton resets the ready latch. The ready latch may also be reset by the end-of-forms contacts when the printer runs out of paper.

A 6 bit is set into the status byte by the unit-check latch when the ready latch is reset. When the ready latch is first set, it fires a single-shot to set the store-device-end latch (Figure MD-4). The device-end-interrupt line then requests a status-trans-

fer sequence from the channel to signal the channel that the 1052 is ready; no status bits are set. Depressing the ready pushbutton causes the print ball to rotate to the same case position (upper or lower) established by the U/L case latch.

### POWER CONTROL

#### Power Interface Lines

The power control interface consists of six lines, assigned as shown in Figure 26.

Pin	Line	Abbreviation
1	Unit Source	Unit Source
2	EPO Control	EPO Ctrl
3	System Source	Sys Source
4	Powering Complete	Pwr Cmpl
5	Power Hold	Pwr Hold
6	Power Pick	Pwr Pick

#### Unit Source

The unit-source line is a voltage source from the 2150 Console that is being sequenced. This line supplies the voltage and current for the EPO-control, power-pick, and power-hold lines.

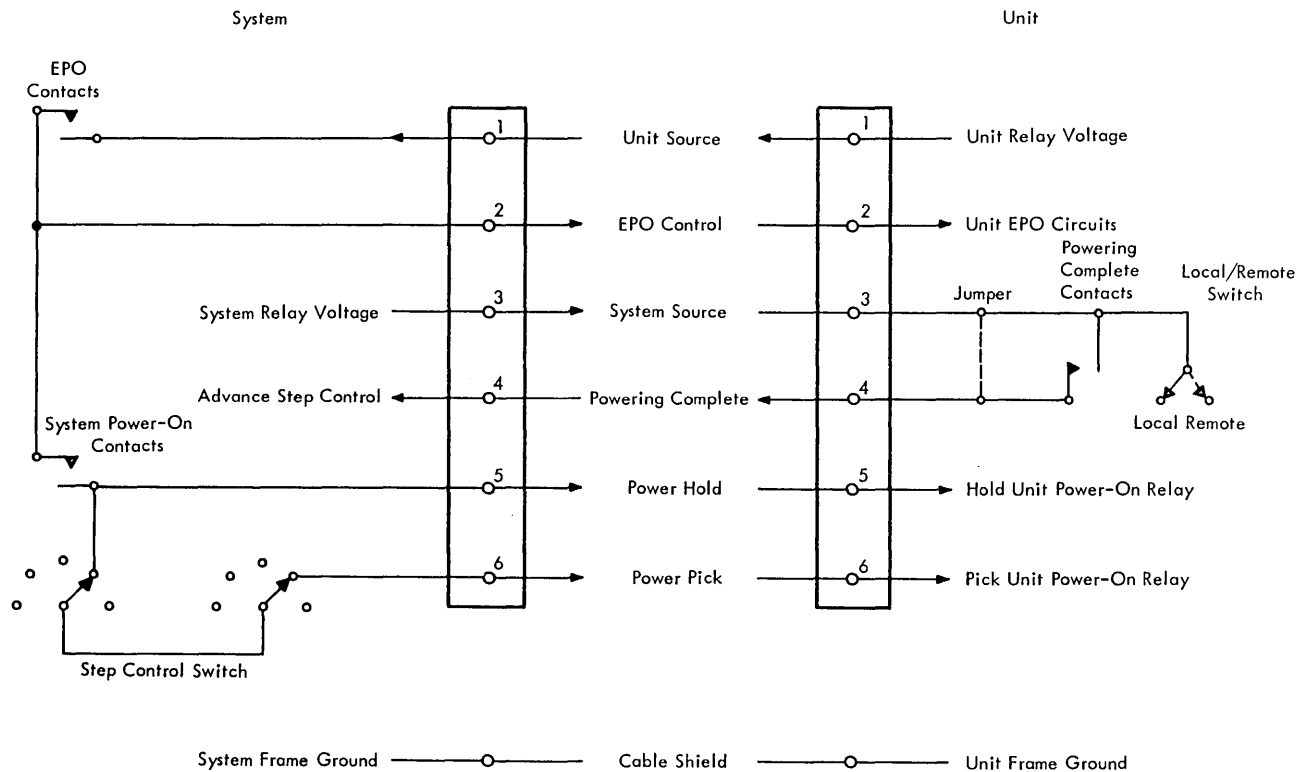


FIGURE 26. 2150 CONSOLE POWER INTERFACE LINES



## EPO Control

The EPO-control line is effectively shorted to the unit-source line emanating from the 2150 Console, when the EPO contacts (of the host CPU) are closed. If an emergency-power-off condition occurs, the EPO contacts will open.

## System Source

The system-source line is a voltage source originating from the System/360 that is switched to the 2150 Console. The latter is not considered a load when viewed from the host system that it services.

## Powering Complete

Powering-complete is established when the system-source line is shorted to the powering-complete line during one of the following conditions:

1. Local/remote switch is in the local position.
2. Local/remote switch is in the remote position and the 2150 Console power sequence is complete.
3. Power for the 2150 Console is not controlled by a System/360 and a jumper is placed between the system-source line and the powering-complete line.

## Power Hold

The power-hold line is shorted to the unit-source line when a System/360 has power on. Power-hold causes the 2150 Console power to remain on until:

1. System/360 power is dropped when the 2150 console's local/remote switch is in the remote position.
2. 2150 Console power is turned off locally while its local/remote switch is in the local position.

## Power Pick

The power-pick line is shorted to the power-hold line when the step-control switch (Figure 26) closes the contacts for this unit. It remains shorted until the step-control senses a signal on the powering-complete line. The power-pick line initiates the console power-on sequence when the unit is in remote status.

## AC Power Sequencing and Distribution

Power to the 2150 Console is obtained from a wall receptacle that supplies 208 vac, 3-phase, 60 cycles. The main source of ac power is supplied through a 4-conductor cable. Three of the conductors carry voltage; the fourth is connected to earth ground. Power enters the unit via the main circuit breaker CB1 (Figure 27) and is routed to the line side of main power contactor K2. The phase 2 and 3 lines are tapped (line side) to the primary winding of the 24v step-down transformer, T2. The output voltage

from T2 supplies the 24 vac control voltage to power the ac control relays within the 2150 Console. The phase 1 and phase 3 lines are tapped (line side of main power contactor K2) to supply 208 vac to the 115v step-down transformer, T3. The output voltage of T3 supplies the ac voltage to power the convenience outlet in the 2150 Console and the driver motor of the 1052 Printer-Keyboard. Main power contactor K2 controls the application of the 208 vac that is required to power the gate fans, the use-meter, and the dc power supplies via CB4 and TB1 connector.

As shown in Figure 27, the 24 vac control voltage derived from T2 is used to energize relay K1, if the unit-source line is shorted, via the EPO contacts of the host System/360, to the EPO control line (Figure 26). When relay K1 is energized, the 208 vac source voltage present on the phase 1 and phase 3 lines is supplied to the input winding of the 115v step-down transformer, T3. The T3 output voltage (115v) is used to power the convenience outlet mounted in the rear of the 2150 Console, and when main power contactor K2 is activated, power is supplied to the driver motor of the 1052-7 Printer-Keyboard.

The 24 vac control voltage from T2 is routed through the n/o contacts of relay K1 to energize the time delay 2 (TD2) relay. This relay provides a 2-second time delay. Further, the 24 vac is routed through the K3-2 n/c contact as a monitoring voltage to ensure that the CB auxiliary contacts in the dc power supply are closed before the dc power supply is powered. In addition, the CB/thermal indicator is illuminated for a brief moment. If the gate thermal sensing contact is closed, in the 2-second time interval that TD2 is energized, the 24 vac is routed through the CB auxiliary contacts in the dc power supply and the n/c contact of TD2 to energize relay K3. At the end of the 2-second time delay, the n/c contact of TD2 opens, and relay K3 remains energized via its K3-3 n/o contact.

Relay K3 can also be energized by depression of the CB/thermal reset pushbutton that is located within the 2150 Console. This is an optional feature that is restricted for CE usage only. In effect, relay K3 ensures that malfunctions due to thermal excesses in the 2150 Console or in the dc power supplies are not in evidence prior to activation of the dc power supplies. The ac power-on sequence is terminated when relay K3 is energized. The ac power-on sequence described will occur regardless of whether the 2150 Console is in local or remote status, assuming that it is connected to the wall receptacle and no circuit breakers have been tripped.

## DC Power Sequencing - Local Status

With the remote/local switch of the host CPU or 2150 Console in the local position, the dc power sequencing operations are initiated by depression of the power on pushbutton. This causes the 24 vac control voltage to be routed through the local position contacts (9 and 10) of the remote/local switch and through the K3-1 n/o

OPERATORS CONSOLE

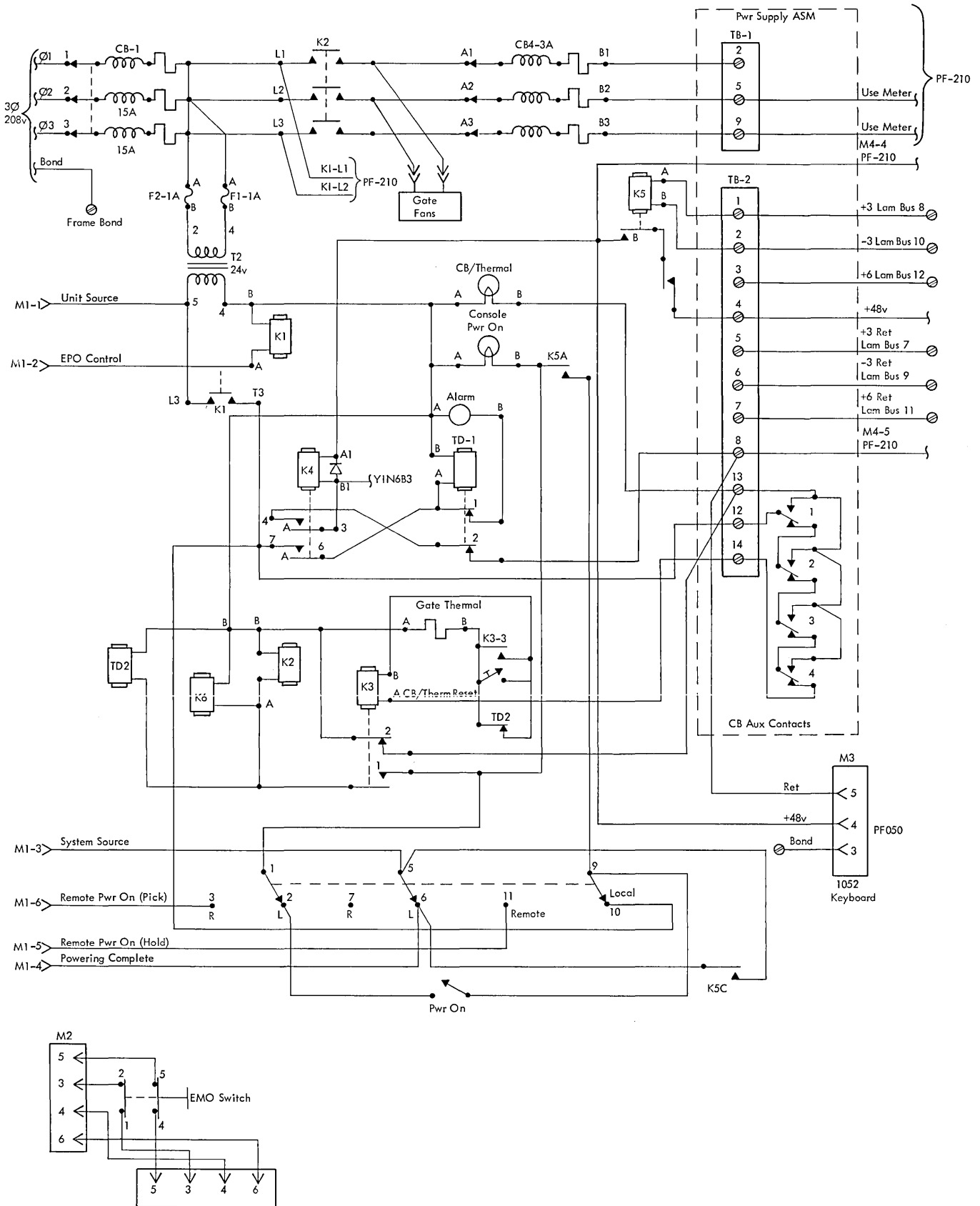


FIGURE 27. 2150 CONSOLE POWER CONTROL DIAGRAM (SHEET 1 OF 2)

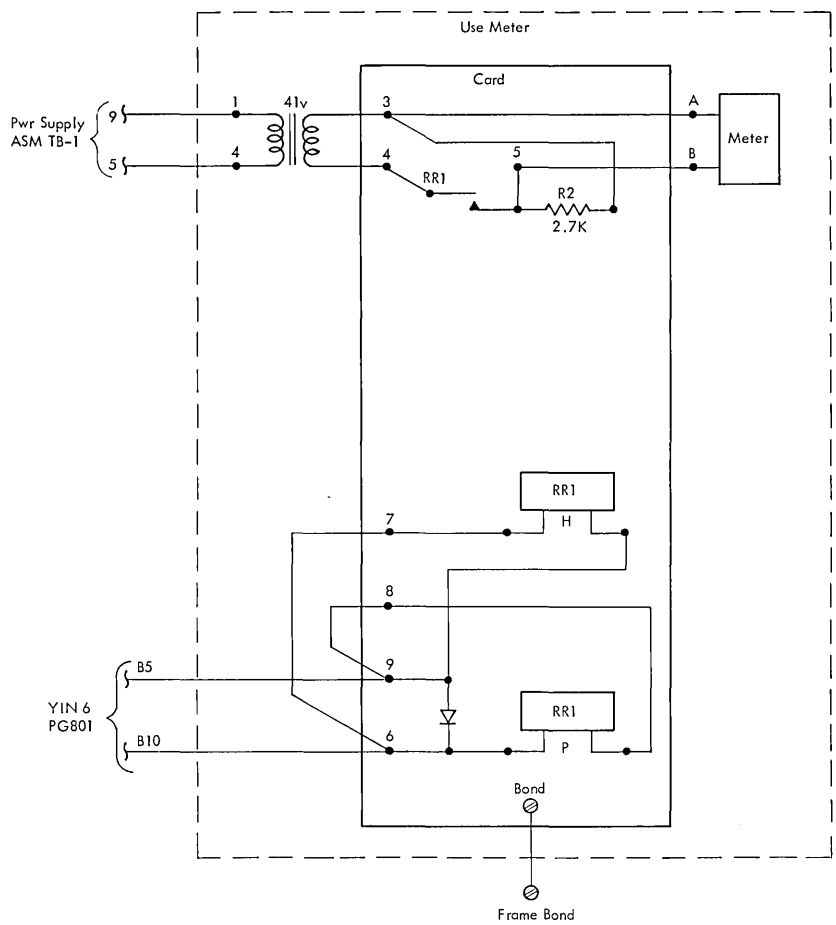
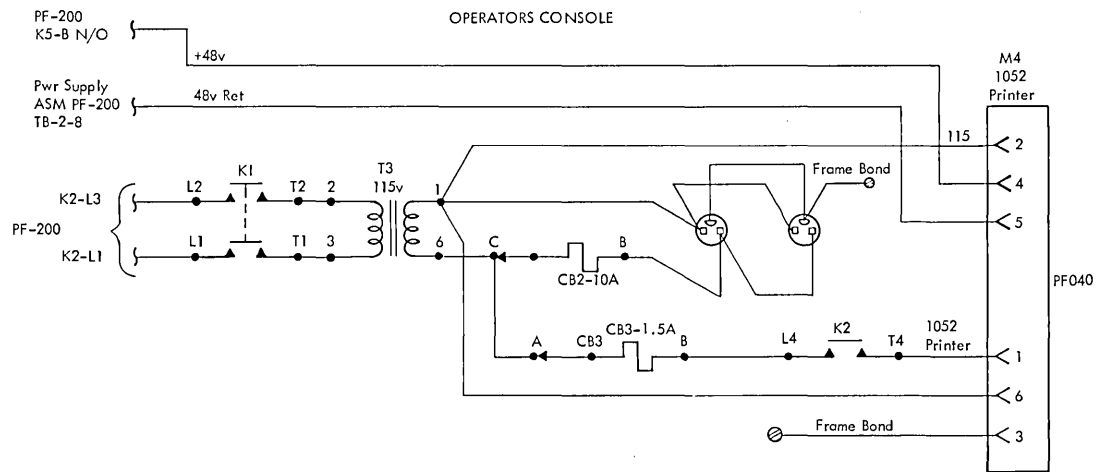


FIGURE 27. 2150 CONSOLE POWER CONTROL DIAGRAM (SHEET 2 OF 2)

contact to energize main power contactor K2 and relay K6. In addition, the console power on indicator will light. First, with relay K2 in an energized state, the 208 vac source voltage on the phase 1 and phase 2 lines is applied to power the gate fans in the 2150 Console. Second, the 115v output voltage from step-down transformer T3 is routed through CB3 and K2 n/o contacts to power the driver motor in the 1052-7 Printer-Keyboard. Third, the 208 vac on the phase 2 and 3 lines is routed through CB4 to the input winding of the 41v step-down transformer, the output of which is used to drive the use-meter. Fourth, the 208 vac is sent through CB4 (3 amp) and TB1 connector points 2, 5, and 9 to activate the SMS dc power supplies. In turn, regulated dc voltage is then fed from the dc power supplies to a laminar bus, TB2. Table 1 lists the individual dc power supply voltages and their respective current ratings.

Table 1. Console Power Supplies

VOLTAGE	AMPERES	OUTPUTS
+3v	6	1-5
-3v	2	2-6
+6v	6	3-7
+48v	2	4-8

TB2 pin contacts 1 and 2 (+3v/-3v) supply the 6 vdc required to energize relay K5.

Energized relay K5 controls the routing of the +48 vdc within the 2150 Console and to the 1052-7 Printer-Keyboard. It also provides an alternate path, via K5A n/o contact, for the 24 vac control voltage that illuminates the power on console indicator. Further, since the 2150 is in local status, it causes the system-source line to be shorted to the powering-complete line via K5C n/o contact and the remote/local switch contacts. This indicates to the host system that the powering sequence for the 2150 Console is completed.

TB2 pin contacts 4 and 8 are connected to the +48 vdc source. Since relay K6 was previously energized, the +48 vdc is routed through the K6-1 n/o contacts and the K5B n/o contact to the 1052-7 Printer-Keyboard. This voltage is also routed to one side (pin A1) of relay K4. The latter is energized only upon receipt of a signal from the 1052 Adapter at logic point Y1 N6 B3 and is applied to the other side of the K4 relay coil (pin B1). In effect, this is achieved by momentarily grounding point K4B1. Once relay K4 is energized, it remains picked because of the K4 A3, K4 A 4 n/o contacts and TD1-2 n/c contacts which provide a dc return path to the 1052-7 Printer-Keyboard. Energized

relay K4 also allows the 24 vac control voltage to be routed through K4 A7 and K4 A6 n/o contacts to energize the 2-second TD1 relay which, in turn, causes the 2150 Console alarm to ring. At the end of the 2-second period, the alarm ceases to ring, as a result of TD1 being picked. When this occurs, the TD1-1 and 2 n/c contacts open, removing the +48v return line required to energize relay K4 and the 24 vac control voltage required to activate relay TD1.

#### DC Powering Sequencing - Remote Status

When the remote/local switch on the 2150 Console is in the remote position, the 2150 Console power-sequencing operation is controlled by the host System/360 that it services. Remote power sequencing is achieved with the power control interface, that provides for a sequential and interlocked means of system powering. By stepping power to discrete units of a System/360, customer power requirements are decreased, and power-surge noise generation can also be reduced substantially. In the remote control status, the 2150 Console is effectively under control of the host system's CPU power on/power off switch. Every System/360 CPU is equipped with a step-control switch (Figure 26) that is used as a step control to sequentially power a stand-alone unit (such as a channel or storage unit); in this case, the 2150 Console.

Remote powering of the 2150 Console by the host system is achieved in a manner similar to the power-sequence operation initiated at the 2150 Console; i.e., the ac power-sequence operation previously described is also applicable when the 2150 Console is in the remote status. However, the dc power-sequencing operation that occurs thereafter differs in the manner described in the following paragraphs.

The host System/360 CPU generates a remote-power-on (pick) signal which is routed through remote/local switch contacts 1 and 3 and the K3-2 n/o contact to energize power contactor K2 and relay K6 and to light the console power on indicator. Energizing K2 allows the following events:

1. The 208 vac on the phase 1 and 2 lines is applied to power the gate fans in the 2150 Console.
2. The 115v output voltage from transformer T3 is passed through CB3 and the K2 n/o contact to power the motor in the 1052-7 Printer-Keyboard.
3. The 208 vac on the phase 2 and 3 lines is routed through CB4 and applied to the input winding of the 41v step-down transformer, the output of which is used to drive the use-meter.
4. The 208 vac is sent through CB4 and TB1 connector points 2, 5, and 9 to activate the SMS dc power supplies.

Regulated dc voltages are then fed from the dc power supplies to laminar bus TB2. TB2 pin contacts

1 and 2 (+3v/-3v) supply the 6v required to energize relay K5 via the K6-1 n/o contact. Energized relay K5 controls the routing of the +48 vdc within the 2150 Console and to the 1052-7 Printer-Keyboard. In addition, the remote-power-on (hold) line is shorted to the remote-power-on (pick) line via K5A n/o contact and remote/local switch contacts 4, 9, and 12. These lines remain shorted until the step-control of the host System/360 senses a signal on the powering-complete line. Energized relay K5 also causes the system-source line to be shorted via the K5C n/o contact to the powering-complete line, indicating to the host system that the 2150 Console power sequence is complete. Upon receipt of the powering-complete signal from the 2150 Console, the step control of the host System/360 is advanced to the next position, thereby removing the power-pick signal to the 2150 Console. The normal power-on sequence for the 2150 Console, when under control of a host System/360 (remote), is presented in the following paragraph.

Power-On Sequence (Remote)

1. The EPO switch is reset, and the power-on switch of the host system is closed.
2. The system source voltage is routed to the 2150 Console.
3. The unit source voltage is routed from the 2150 Console through the EPO and power-on/power-off contacts of the host system and is returned to the 2150 Console as the EPO-control and power-hold lines.

4. The step control of the host system is advanced to the first position. This shorts the power-hold line to the power-pick line.

5. If the 2150 Console local/remote switch is in LOCAL, the 2150 Console power-on sequence is inhibited, even when the power-pick line is activated. In this case, the system-source line is shorted to the powering-complete line via the contacts of the local/remote switch.

6. If the 2150 Console local/remote switch is in REMOTE, the 2150 Console power-on sequence occurs. When the sequence is complete, the system-source line is shorted to the powering-complete line via the contacts of the local/remote switch.

7. If the 2150 Console power is not controlled by a host system, the system-source line is shorted to the powering-complete line via the local/remote switch.

8. Upon receipt of the powering-complete signal by the host system, the step control is advanced to the next position. This will remove the power-pick signal to the 2150 Console and enable a subsequent I/O unit to be powered.

9. Steps 5, 6, 8, and 9 are repeated until the power-sequencing operation for each unit attached to the host system has been completed.

Power Control Panel Description

The power control panel (Figure 28) comprises an emergency power off switch, a use-meter, and a

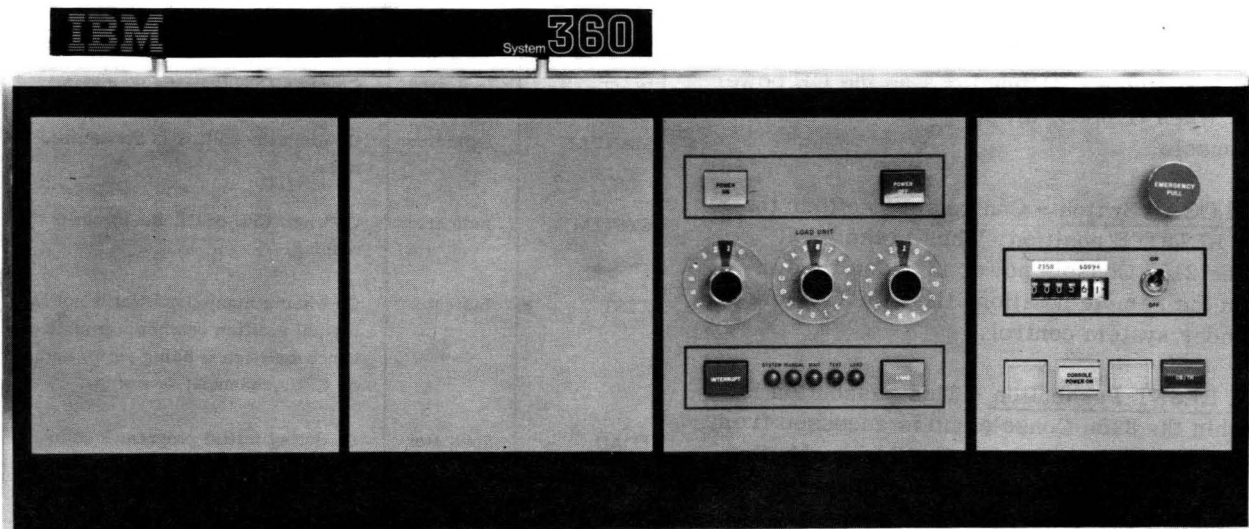


FIGURE 28. 2150 CONSOLE, REMOTE OPERATOR CONTROL PANEL AND POWER CONTROL PANEL

power on and a CB/thermal indicator that function as described below:

EMERGENCY (pull) Switch - Removes all power beyond the entry terminal of the 2150 Console. Only a CE or maintenance personnel can restore the EMERGENCY switch to the IN position. When the EMERGENCY switch is pulled (OUT position), the 2150 Console power-on switch is ineffective.

Use Meter - The use meter records the elapsed time of operation for the 2150 Console and the 1052-7 Printer-Keyboard. The meter operates in conjunction with the CPU of the host System/360 when power is on. The meter is inoperative when power is off.

POWER ON Indicator - Indicates that power has been sequenced in the 2150 Console and 1052-7 Printer-Keyboard.

CB/THERMAL Indicator - When illuminated, indicates that a circuit breaker has been tripped or a thermal overload condition has occurred in the 2150 Console.

#### CE Controls

The following controls are located within the 2150 Console. Their use is restricted to the CE's only.

POWER ON Switch - A momentary contact switch which is operative only when the remote/local switch is in the LOCAL position. (CE function only.) Power is normally brought up or down remotely from the host system.

POWER OFF Switch - CB1 functions as the CE power off switch. When tripped, all power is removed from the 2150 Console.

REMOTE/LOCAL Switch - Can be set to either the LOCAL or REMOTE position. When in the local position, the 2150 Console power is under its own control. In the remote position, the 2150 Console power is under system control.

THERMAL RESET Pushbutton - This pushbutton is located within the 2150 Console and is accessed from the rear of the console. Depressing this pushbutton resets the gate thermal sensing device following a power or thermal overload condition.

AUDIBLE ALARM - The alarm gong is located within the 2150 Console and is powered by the 24 vac control voltage. The alarm will sound for a 2-second time period at the beginning of a normal initial-selection sequence or upon receipt of a command signal from the host CPU.

#### Remote Operator Control Panel

A description of the controls and indicators mounted on the remote operator control panel (Figure 28) is presented in Table 2.

Table 2. Remote Operator Control Panel (ROCP)

CONTROL	TYPE	FUNCTION
POWER ON	Pushbutton	Initiates a power-on sequence for the system. A system reset, as part of the sequence, performs no instructions or I/O operations until directed. Main storage remains protected. An indicator shows when sequence is complete.
POWER OFF	Pushbutton	Initiates power-off sequence to the system. Main storage is protected provided the system is in a stop state. The pushbutton is effective while power is present in the system.
INTERRUPT	Pushbutton	Requests an external interruption. Pushbutton is effective while power is present in the system and external Interrupts are marked ON.
LOAD UNIT	Rotary	Provides the 11-bit address of the device to be used for program loading.
LOAD	Pushbutton	Starts initial program loading. Pushbutton is effective while power is present in the system.
WAIT	Indicator	On when CPU is in the wait state.
MANUAL	Indicator	On when the CPU is in the stopped state.
SYSTEM	Indicator	On when CPU or CE use meter is running.
TEST	Indicator	On when a manual control is not in normal position or when a maintenance function is being performed on CPU, channels, or storage.
LOAD	Indicator	On during initial program loading. Lights when LOAD key is depressed. Turned off after loading of IPL PSW is complete.

**IF DISABLE Switch** - This switch is provided on units equipped with the isolation feature. The switch is used during the power-off sequence to ground the interface driver circuits.

**IF DISABLE Indicator** - Indicates that the unit is in CE mode.

**NOTE:** Refer to decal, behind switch for power-off procedure.

Power Control Component Functions

The power control components and their functions are listed in Table 3.

Table 3. Power Control Component Functions

COMPONENT	FUNCTION
K1	Power contactor that controls the routing of the 208 vac, 3-phase, 60-cps within the 2150 Console. Controls the application of the 24 vac control voltage used to activate the control relays and controls the application of the 115 vac to the convenience outlet and to the drive motor in the 1052-7 Printer-Keyboard.
K2	Power contactor that controls the routing of the 208 vac, 3-phase, 60-cps required to power the gate fans, the use-meter, and the SMS power supply. In conjunction with K1, it controls the routing of the 115 vac required to power the driver motor in the 1052-7 Printer-Keyboard.
K3	Functions as a thermal sense relay and controls the voltage required to activate power contactor K2 and ac relay K6 in the remote or local state.
K4	A +48 vdc control relay that controls the routing of the +48 vdc to the 1052-7 Printer-Keyboard. Controls the application of the 24 vac required to energize relay TD1 (Time Delay) which, in turn, activates the 2150 Console alarm.
K5	A 6 vdc control relay that controls the routing of the +48 vdc required to activate relay K4 and to supply +48 vdc to the 1052-7 Printer-Keyboard. Also used to bypass the POWER ON pushbutton when the 2150 Console is powered from a remote system.
K6	A 24 vac control relay that, in tandem with relay K5, controls the routing of the +48 vdc to energize relay K4 and to supply power to the 1052-7 Printer-Keyboard. Relay K6 and power contactor K2 are energized at the same time.
TD-1	A 2-second time delay relay that is used to activate the 2150 Console alarm and to deactivate relay K4.

Table 3. Power Control Component Functions (Cont)

COMPONENT	FUNCTION
TD-2	A 2-second time delay relay that is used to bypass the CE CB/THERMAL RESET pushbutton, allowing relay K3 to be energized either from a remote system source or from an internal source.
CB1	Functions as the CE POWER OFF switch.
CB2	Functions as a protective device for the 115 vac applied to the convenience outlet in the 2150 Console.
CB3	Functions as a protective device for the 115 vac line used to power the driver motor in the 1052-7 Printer-Keyboard.
CB4	Functions as a protective device for the 208 vac required to power the gate fans, use-meter, and SMS power supply.
CB AUX	Functions as a protective device whenever the maximum permissible temperature limit of the gate thermal is exceeded or as an overcurrent protective device to protect the SMS power supply components. If either of these two cases occurs, the CB THERMAL indicator will light.
T2	A 24v step-down transformer that supplies the control voltage used to power the ac relays within the 2150 Console.
T3	A 115v step-down transformer that supplies the ac voltage to the 2150 Console convenience outlet and the driver motor in the Printer-Keyboard.
T4	A transformer that provides 12v 60-cycle power used to activate a counter as part of a 1-second time-out delay circuit.  NOTE: This component is provided only on 2150 units equipped with the unit isolation feature.

Power Control Component Locations

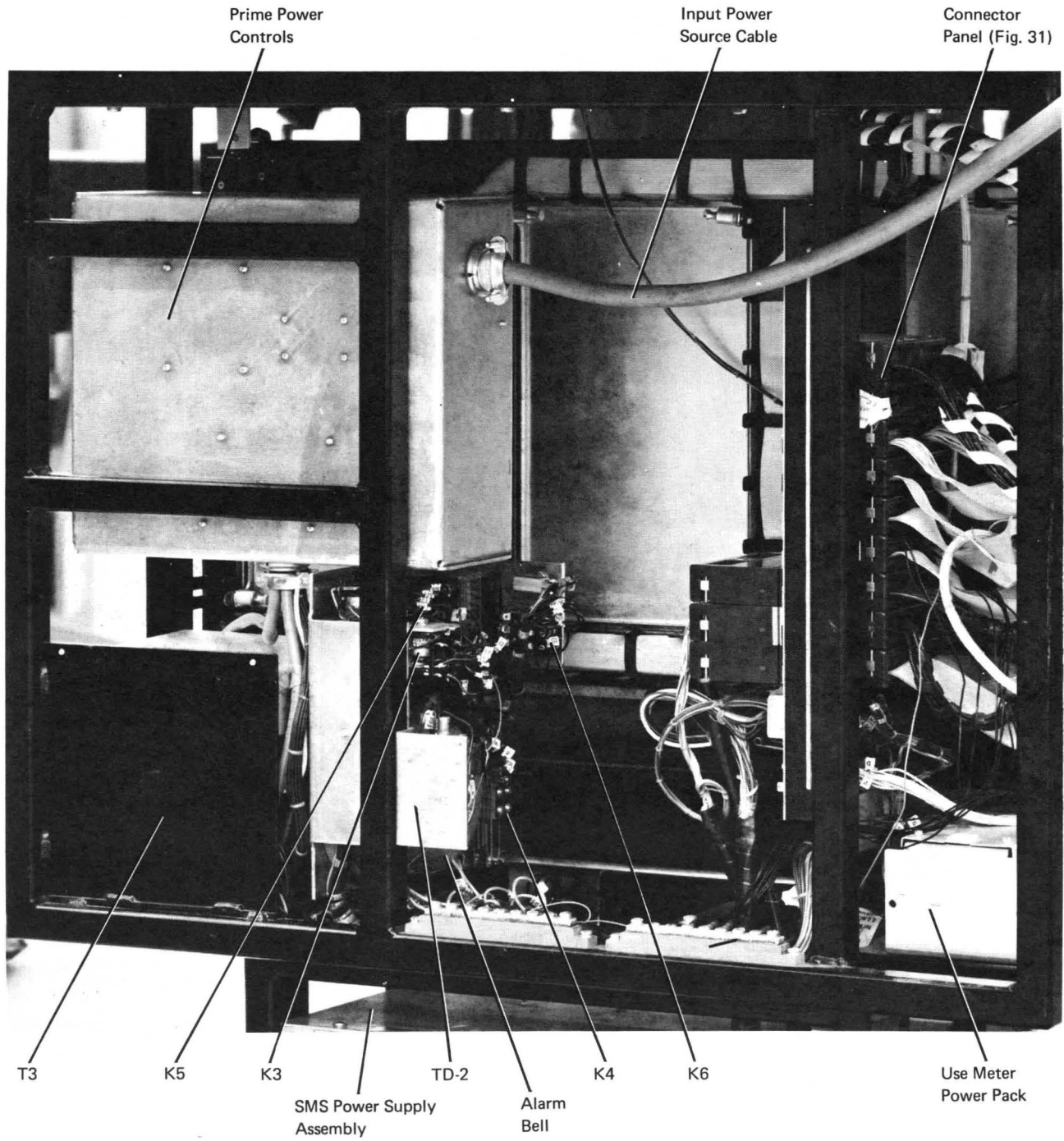
The power control component locations within the 2150 Console are illustrated in Figures 28, 29, and 30.

Console I/O and Power Cable Routing

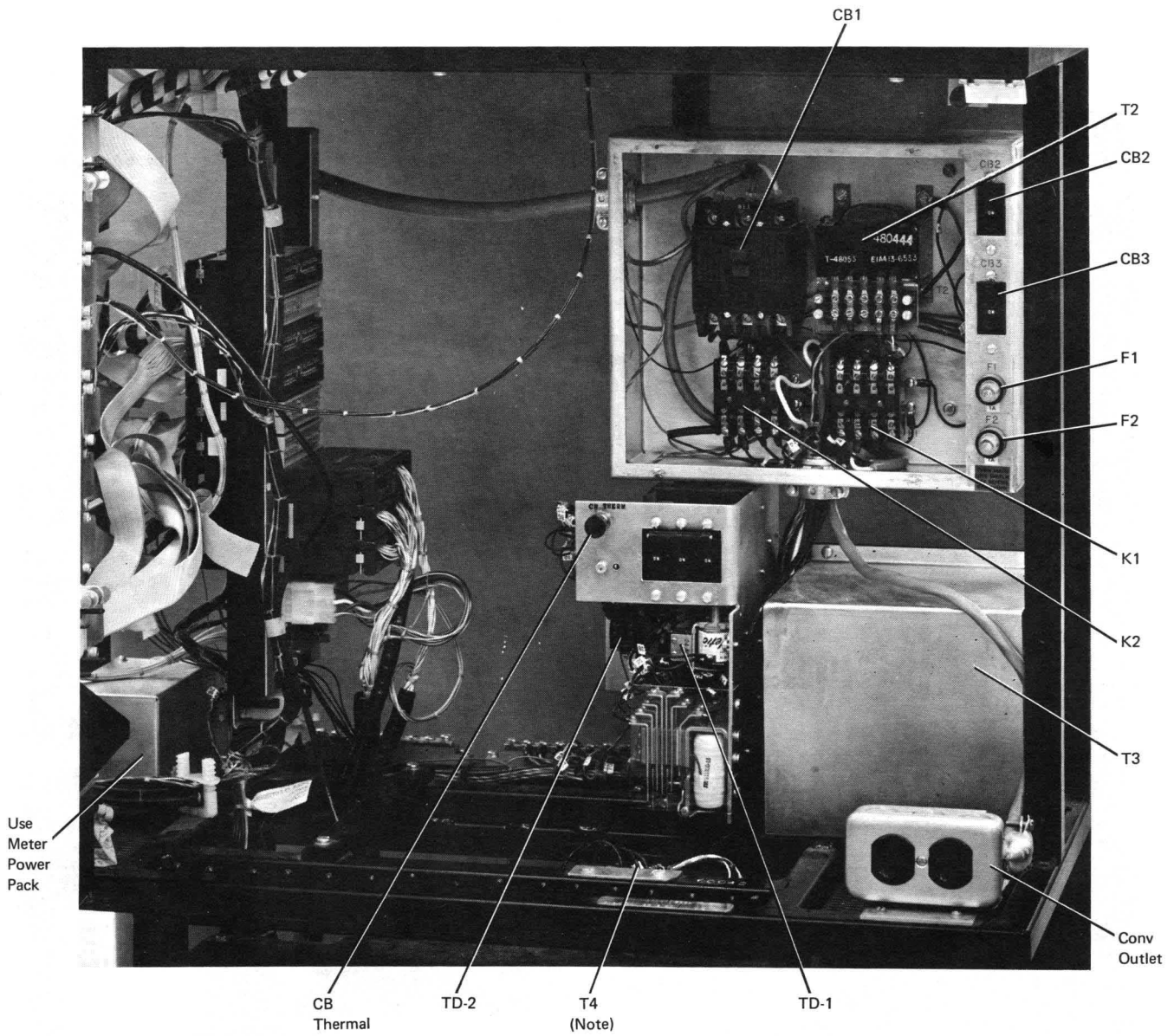
The I/O and power cable routing within the 2150 Console are illustrated in Figures 31 and 32.







● FIGURE 29. 2150 CONSOLE, COMPONENT LOCATIONS, FRONT VIEW



NOTE: This component is provided only on 2150 units equipped with the unit isolation feature.

FIGURE 30. 2150 CONSOLE, COMPONENT LOCATIONS, REAR VIEW

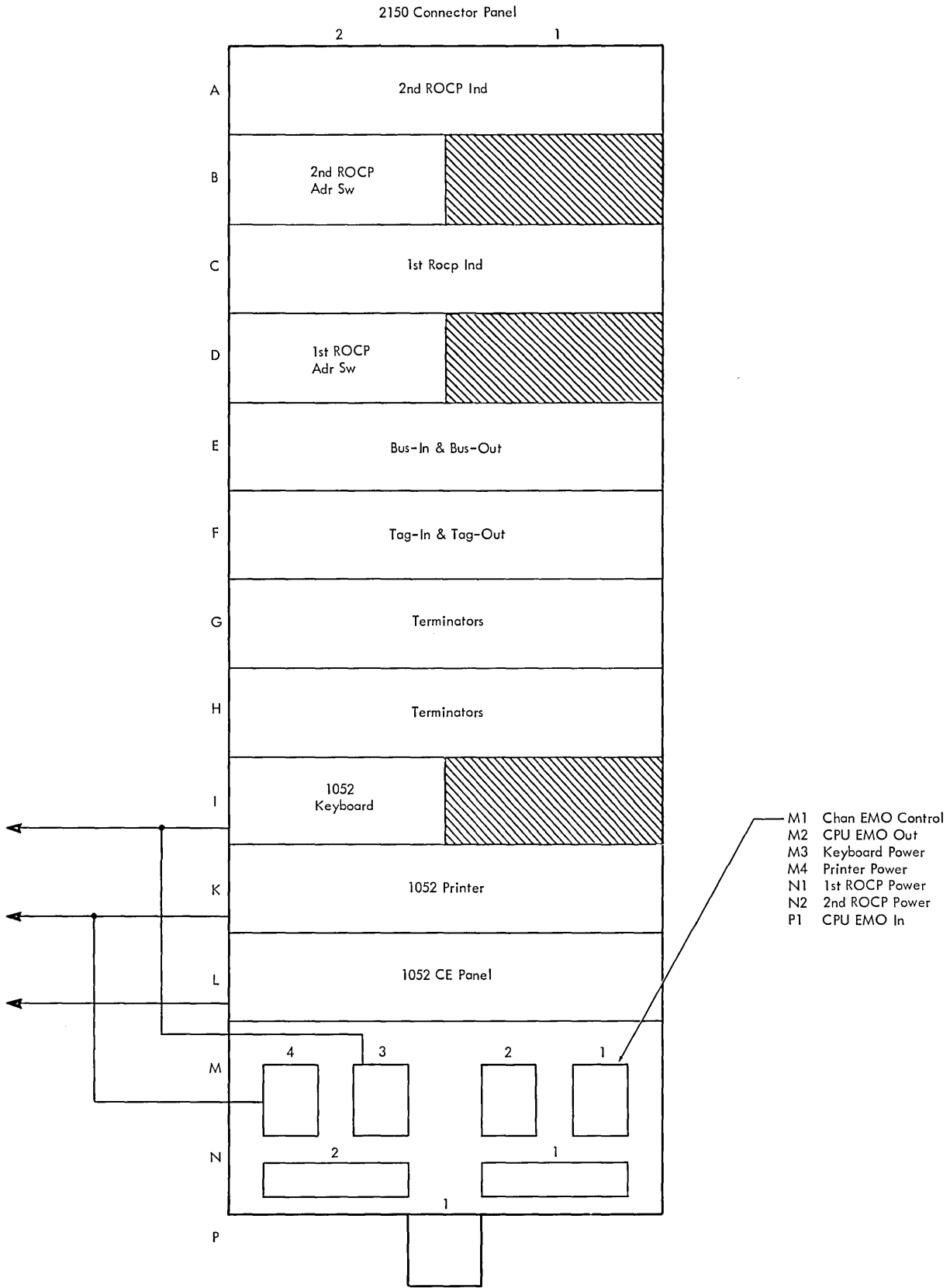


FIGURE 31. 2150 CONSOLE CONNECTOR PANEL

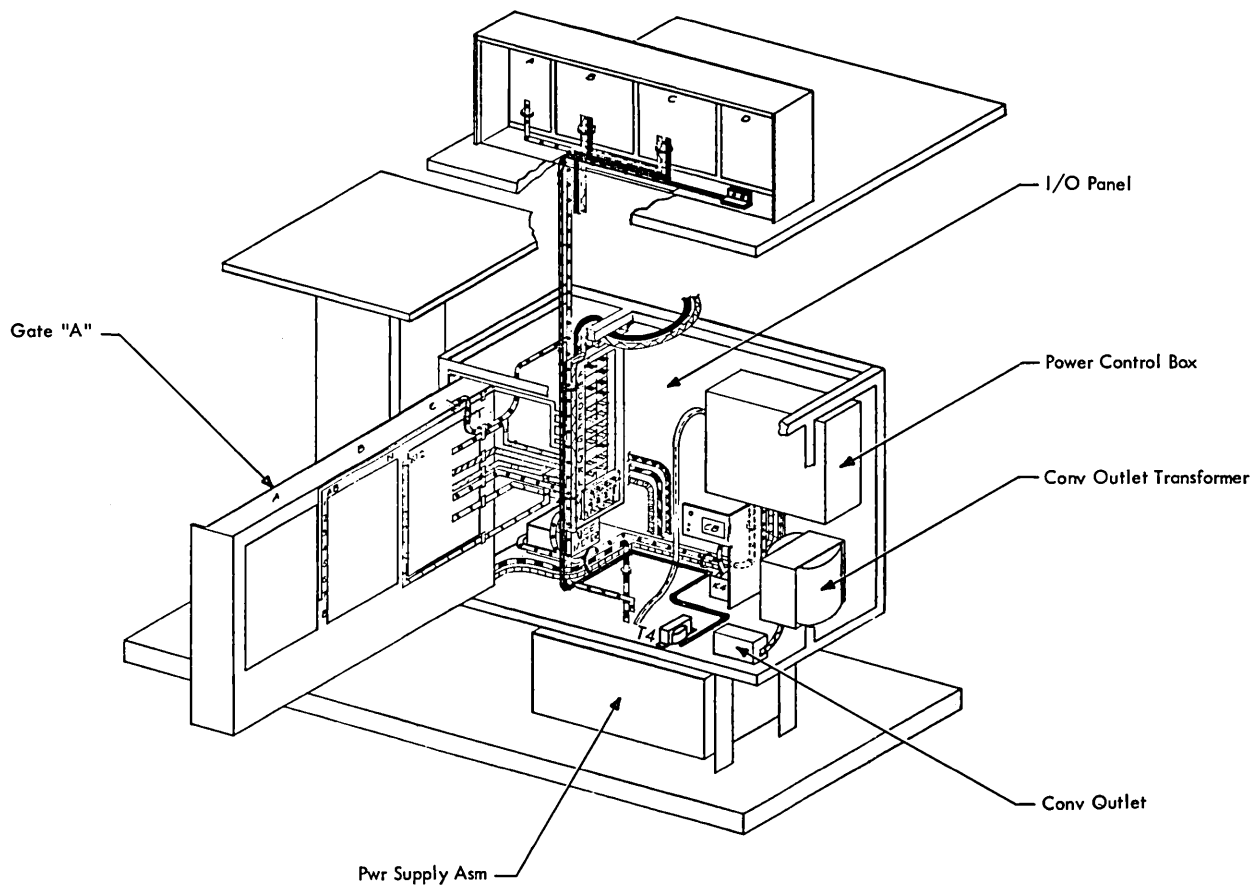


FIGURE 32. 2150 CONSOLE CABLE ROUTING AND TERMINATIONS (SHEET 1 OF 2)

From I/O	To	Cable Code	Function
A1 & A2	ROCP C		I/F (Optional)
B1	ROCP C		I/F (Optional)
C1 & C2	ROCP B		I/F (Optional)
D1	ROCP B		I/F (Optional)
E1	B1A2		Channel Interface
E2	B1A6		↑ ↓
F1	B1A4		
F2	B1B3		
G1	B1A3		
G2	B1A7		
H1	B1A5		↑ ↓
H2	B1B4		
J1	C1N2		1052 Keyboard
K1 & K2	C1N4 & N5		1052 Printer
L1 & L2	C1A2 & N7		1052 CE Panel
M1, M2, M3, M4	Power Ctls		Power Dist & Control
N1	ROCP B		ROCP Pwr (Optional)
N2	ROCP C		ROCP Pwr (Optional)
Wall Pwr	Pwr Ctrl Box		Prime Pwr Input
Conv Outlet	CB & Transformer		Conv Outlet
Blower	K2		Blower
Laminar Bus	Pwr Supply		Laminar Bus
T3	K1		Conv Transformer
J1-M3	1052 Keyboard		1052 Feature
K1 & K2-M4	1052 Printer		↑ ↓
L1 & L2	1052 CE Panel		
Printer Bond	Frame Ground		Ground Jumper
Wall Power	Power Supply		Prime Power Input
C1N3	T4 I/O Switch and Indicator		I/O Interface

●FIGURE 32. 2150 CONSOLE CABLE ROUTING AND TERMINATIONS (SHEET 2 OF 2)

## APPENDIX

### LATCHES/TRIGGERS

<u>Name</u>	<u>MD Figure</u>	<u>ALD</u>
Address In	2, 5	PG101
Attention Status	6	PG131
Binary Trigger	(Figure 14)	PG701
Bus Out Check	6	PG021
Busy Condition	3, 4	PG121
Busy	(Figure 5)	PG641
Carrier Return	4	PG631
Channel End	4	PG131
Command Reject	6	PG141
Cycle Time	4, (Figure 5)	PG601
Device End	4	PG131
End of Line	4	PG641
Equipment Check	6	PG021
Halt I/O	4	PG161
Inhibit Carrier Return	4	PG151
Initial Select	2	PG101
Lower/Upper Case	4	PG611
Operational In	2, 5	PG101
Operational In Interlock	2	PG101
Printer Busy	4	PG641
Read Command	2	PG151
Ready	4, 6	PG621
Request PB Interlock	6	PG621
Sense Command	2	PG151
Service In	3, 5	PG111
Service Request	2, 5	PG611
Shift Change	(Figure 8)	PG611
SP	(Figure 8)	PG111
Status In	2	PG111
Status Stacked	4	PG121
Stop	4	PG121
Store Device End	4	PG621
Store Request	6	PG621
Test I/O	2	PG141
TN SS 6	5	PG631
Unit Check	6	PG131
Unit Exception	6	PG131
Write Command	2	PG151

### 1052 SINGLE-SHOT ADJUSTMENTS

Measure all time durations at the 1.5v level. Before adjusting single shots 1 through 7, turn on CE mode switch and place continuous write/read switch in continuous write position.

Single Shot Test Point		Potentiometer		
<u>Designation</u>	<u>(Note 1)</u>	<u>Duration</u>	<u>Adjustment</u>	<u>Logic</u>
1	XXX YY G7D13	700ns ± 35ns	Center	PG 601
2	XXX YY G7B13	200ns ± 10ns	Lower	PG 601
4	XXX YY E7D13	200ns ± 10ns	Center	PG 601
5	XXX YY D7D04	28ms + 1.4ms - 0ms	Center	PG 601
6	XXX YY E7B13	500ns ± 25ns	Lower	PG 601
7	XXX YY E7D12	200ns ± 10ns	Upper	PG 601
Alarm	XXX YY D7D06	30ms ± 1.5ms	Lower	PG 621
(Note 2)				
Ready	XXX YY G7D12	200ns ± 10ns	Upper	PG 621
(Note 3)				

#### NOTES:

1. XXX gate location and YY panel location depend on system or unit.
2. Key in program to ring alarm bell.
3. Depress ready followed by not ready pushbuttons. Depress system reset between each ready-not ready sequence.

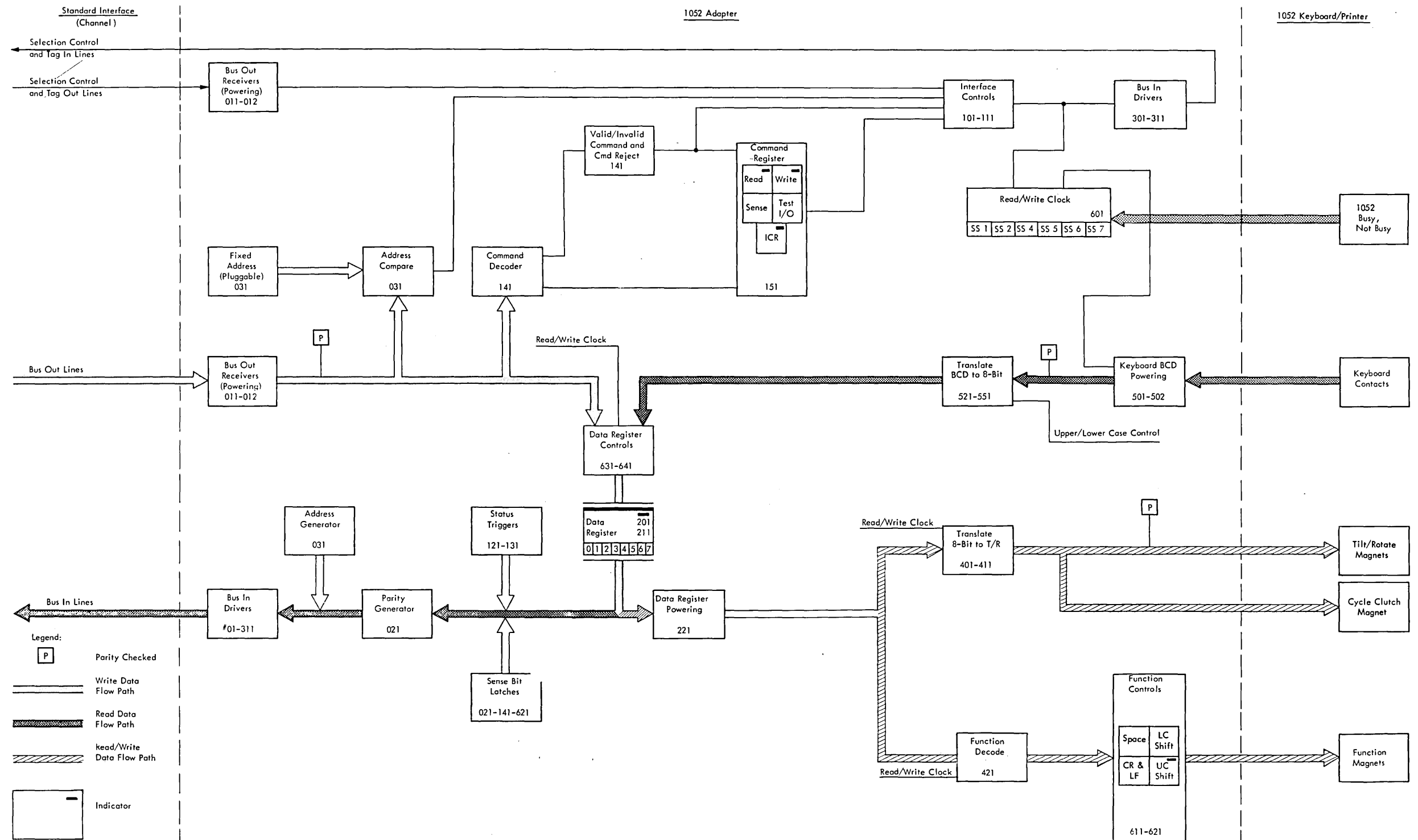
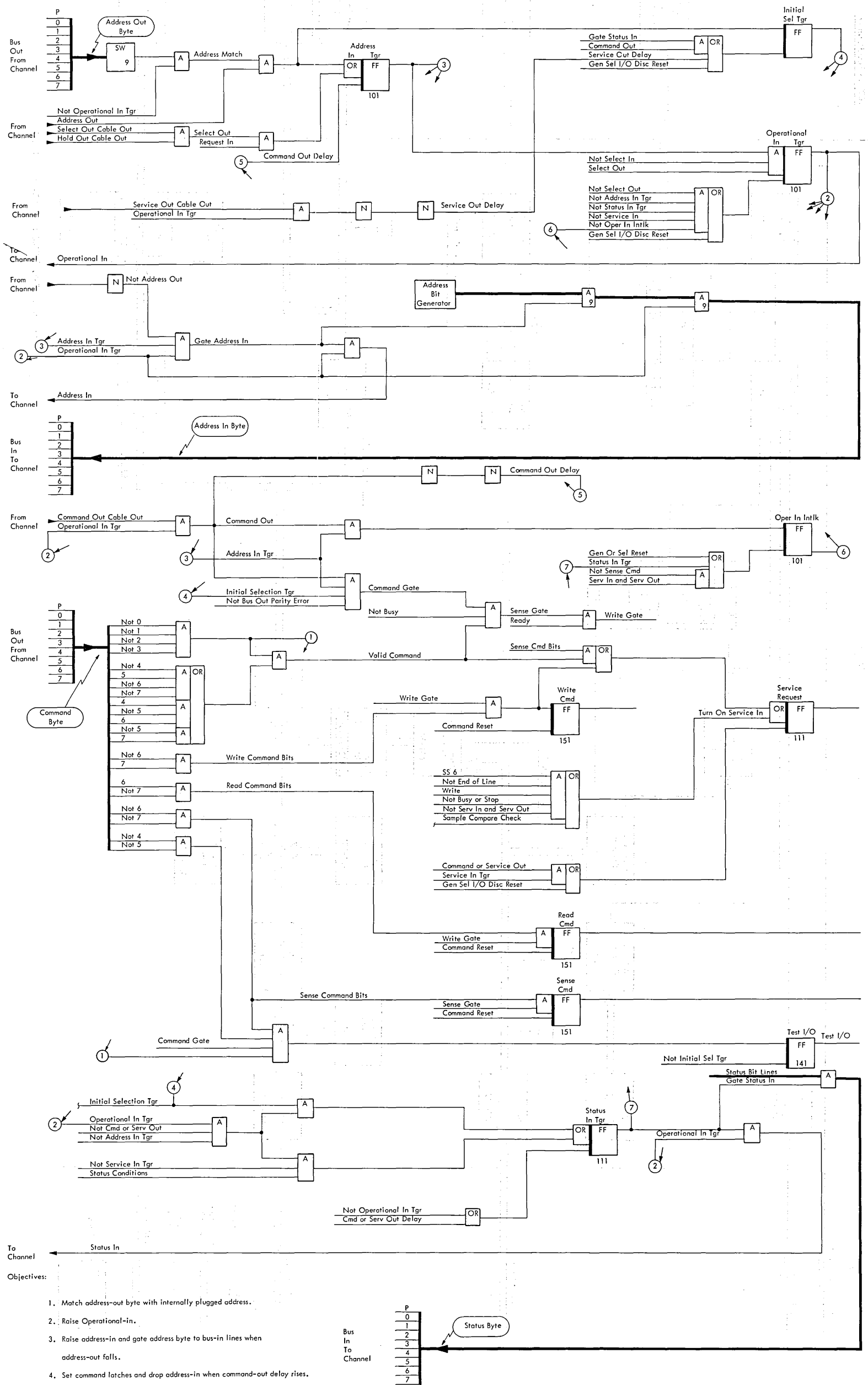


FIGURE MD-1. (UDC) 1052 ADAPTER UNIT



- Objectives:
1. Match address-out byte with internally plugged address.
  2. Raise Operational-in.
  3. Raise address-in and gate address byte to bus-in lines when address-out falls.
  4. Set command latches and drop address-in when command-out delay rises.
  5. Raise status-in and gate status byte to bus-in lines when command-out falls.
  6. Drop operational-in and status-in when service-out rises.

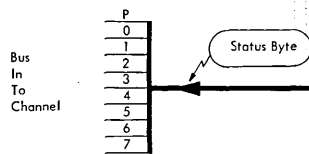
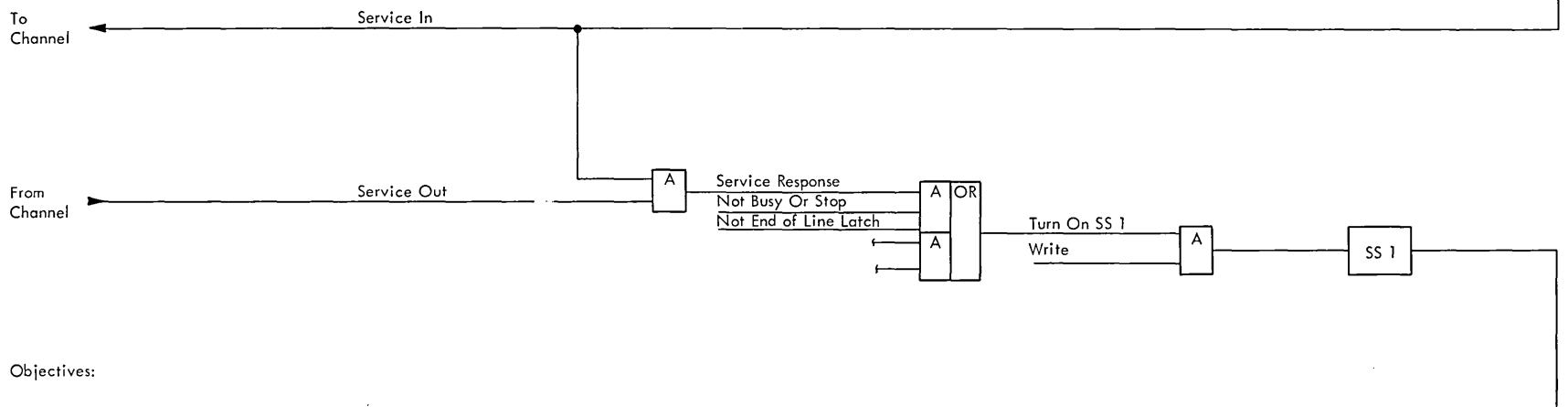
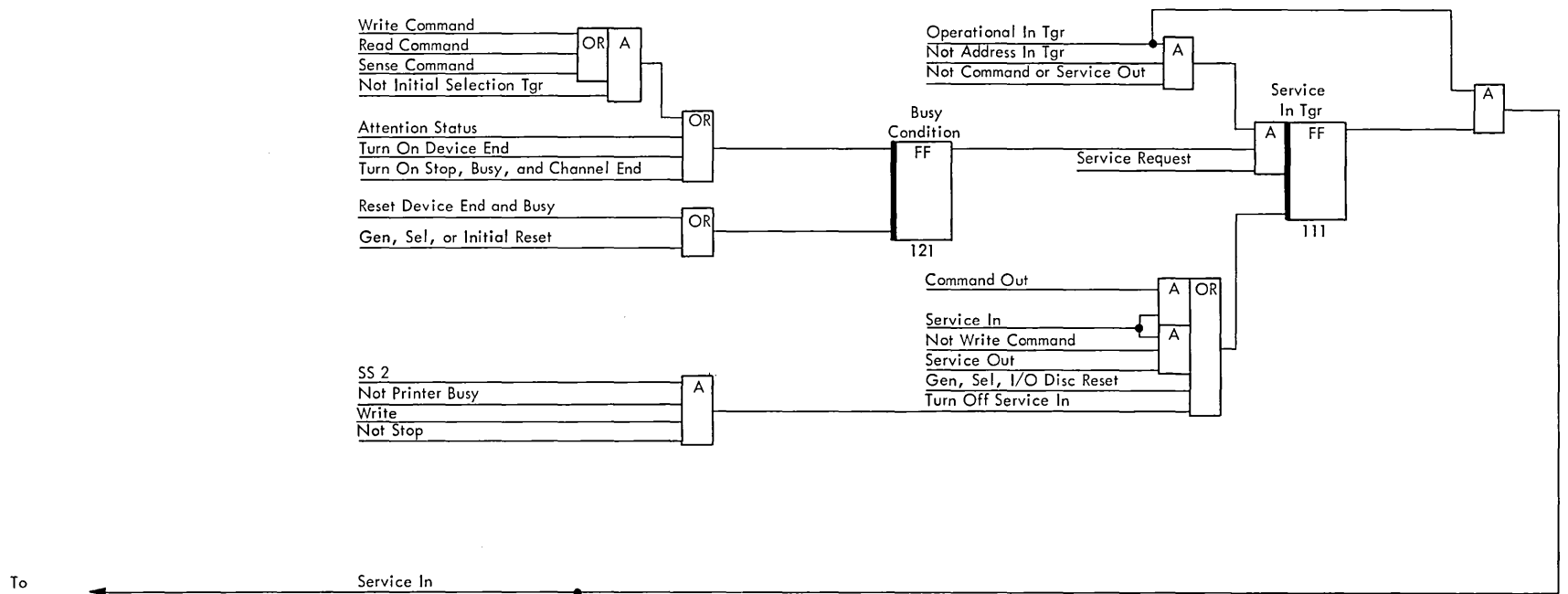
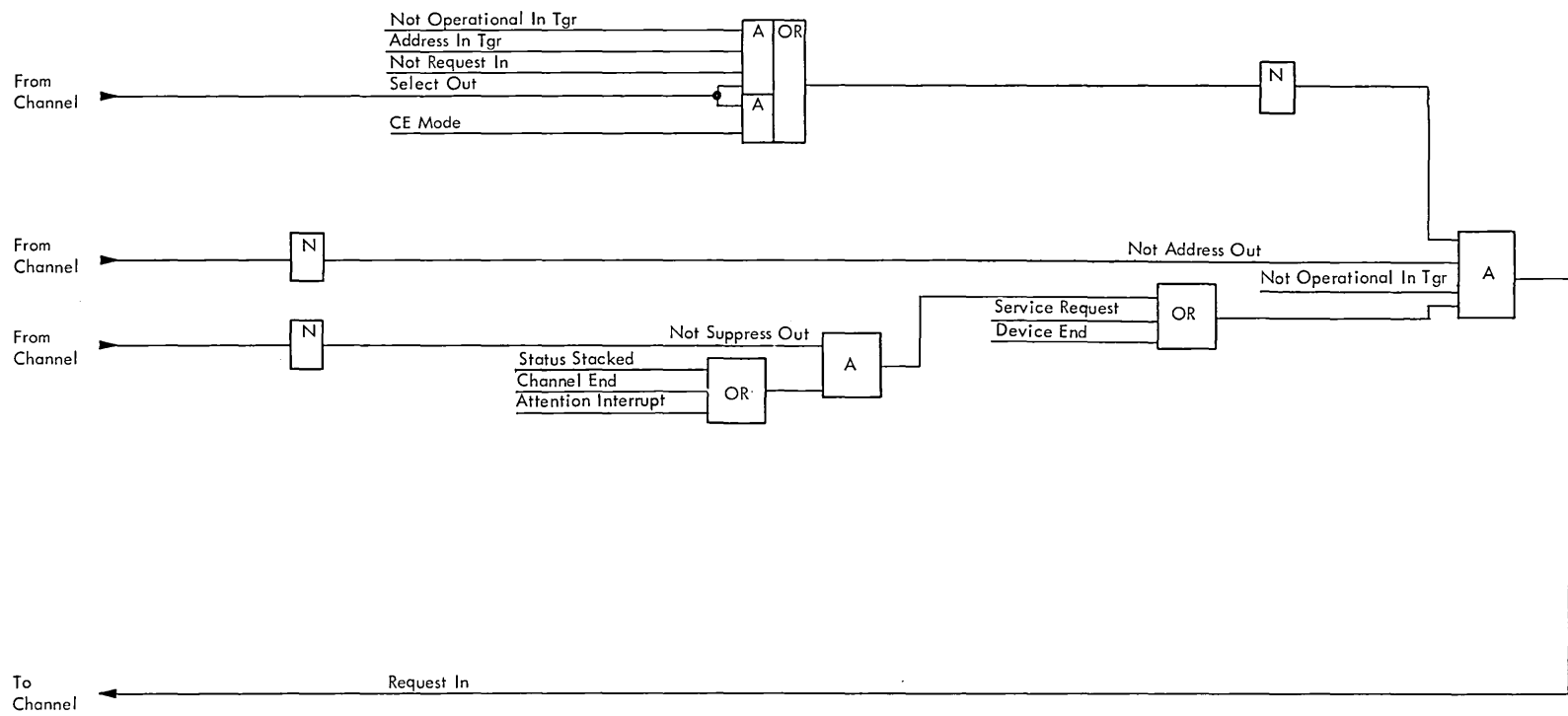


FIGURE MD-2. (I/O) INITIAL SELECTION--READ, WRITE, SENSE  
1052 & 2150 PFTO/PEDM (5-66) 64





Objectives:

1. Raise request-in:
  - A. Immediately after initial selection (service request latch, Figure MD-2)
  - B. When the printer has finished printing the previous character, or when the printer has finished performing the function defined by the previous character (service request latch, Figure MD-2).
2. Raise service-in when command-out line indicates "proceed".
3. Start read/write clock and gate bus out lines to data register when service-out rises.
4. Repeat, starting with 1B, and continue until the command-out line indicates "Stop."

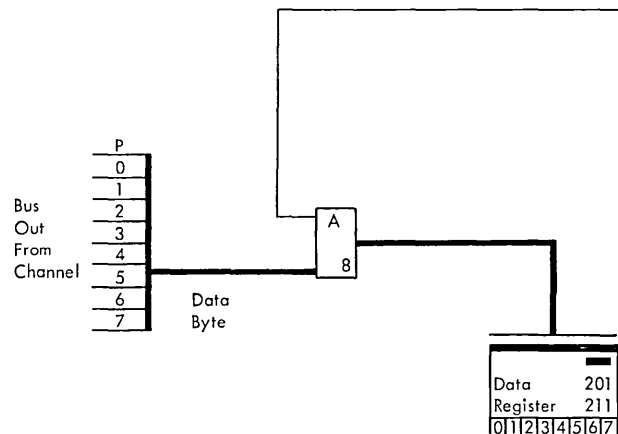
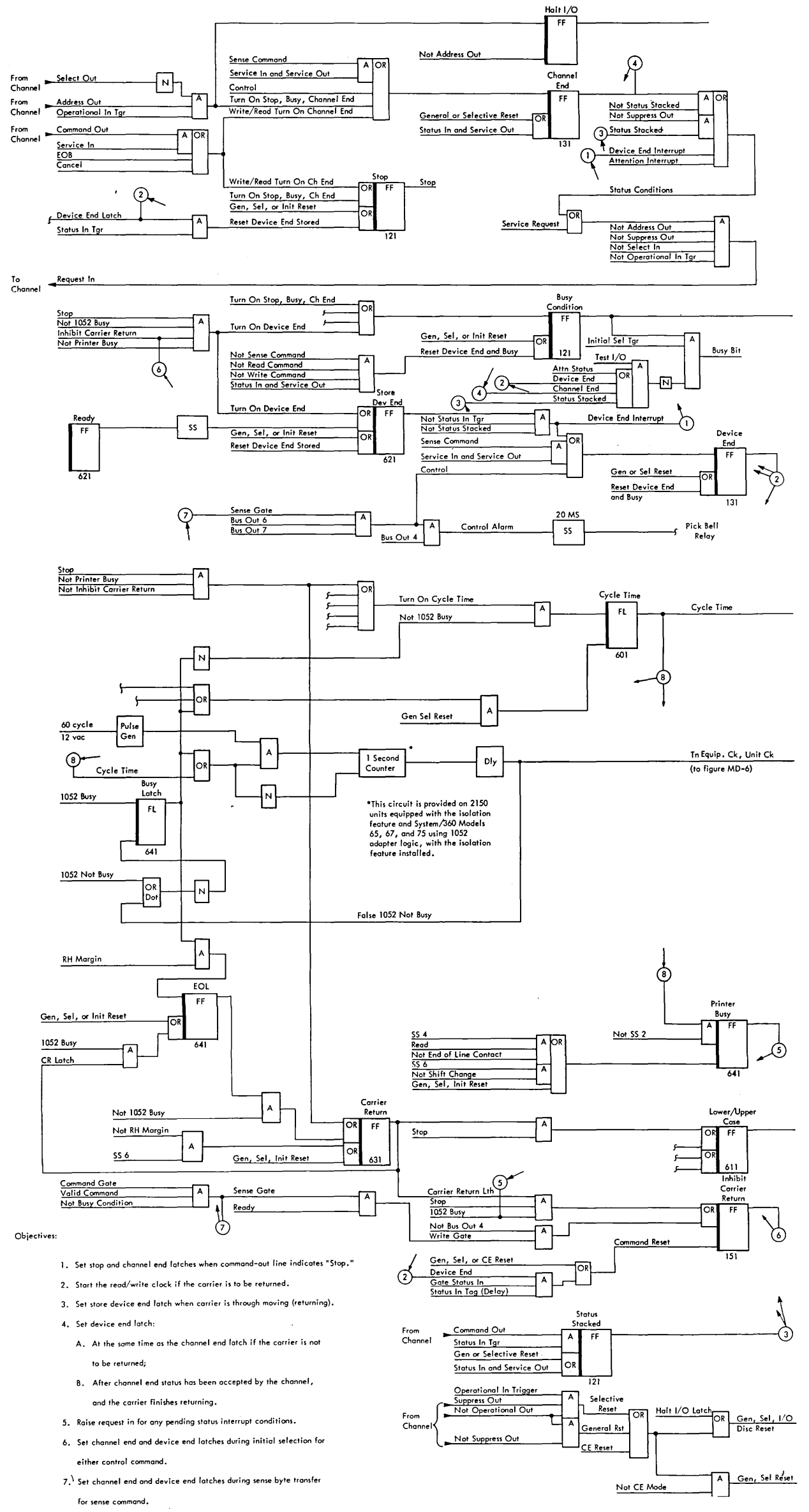
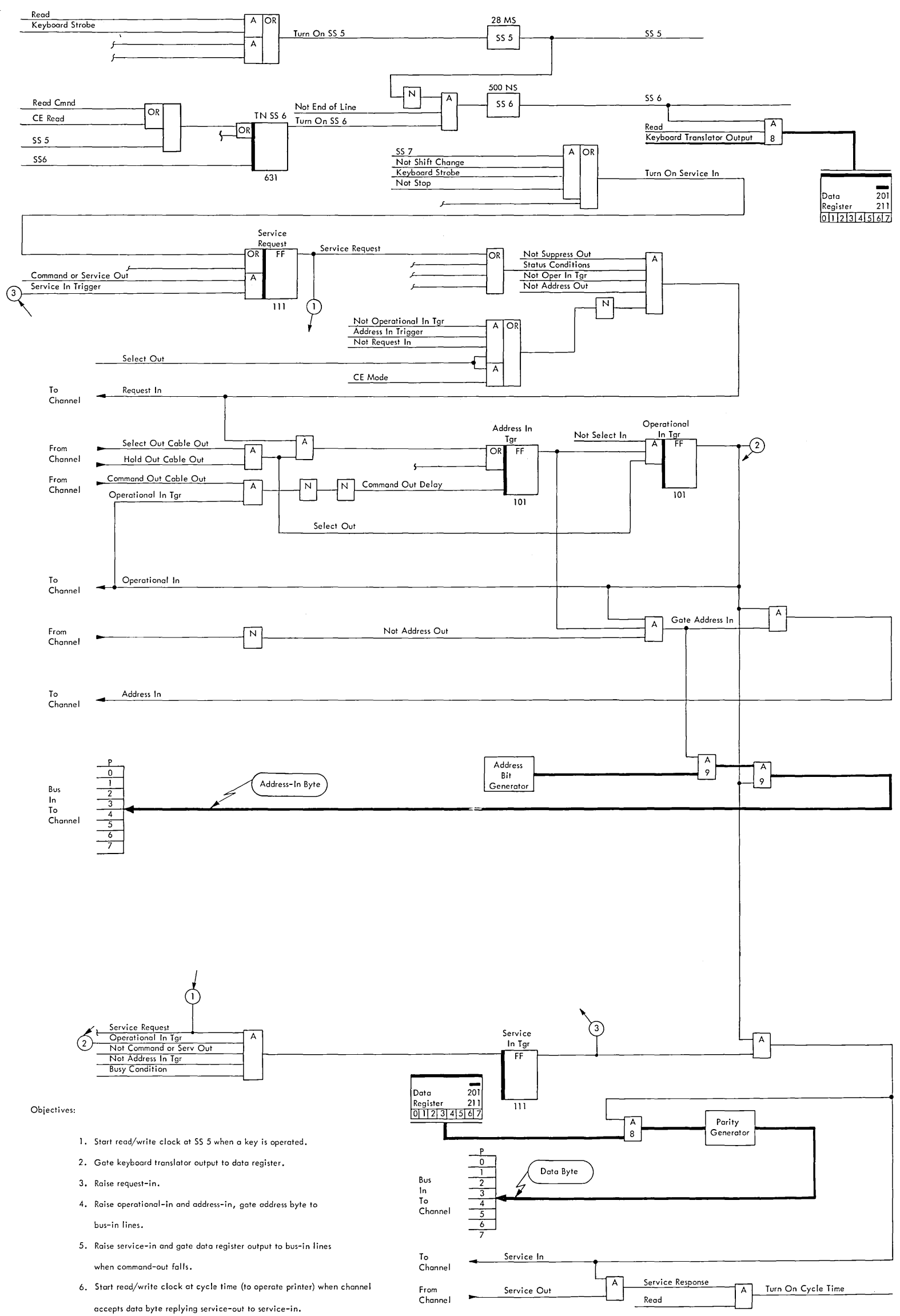


FIGURE MD-4. (I/O) ENDING SEQUENCE



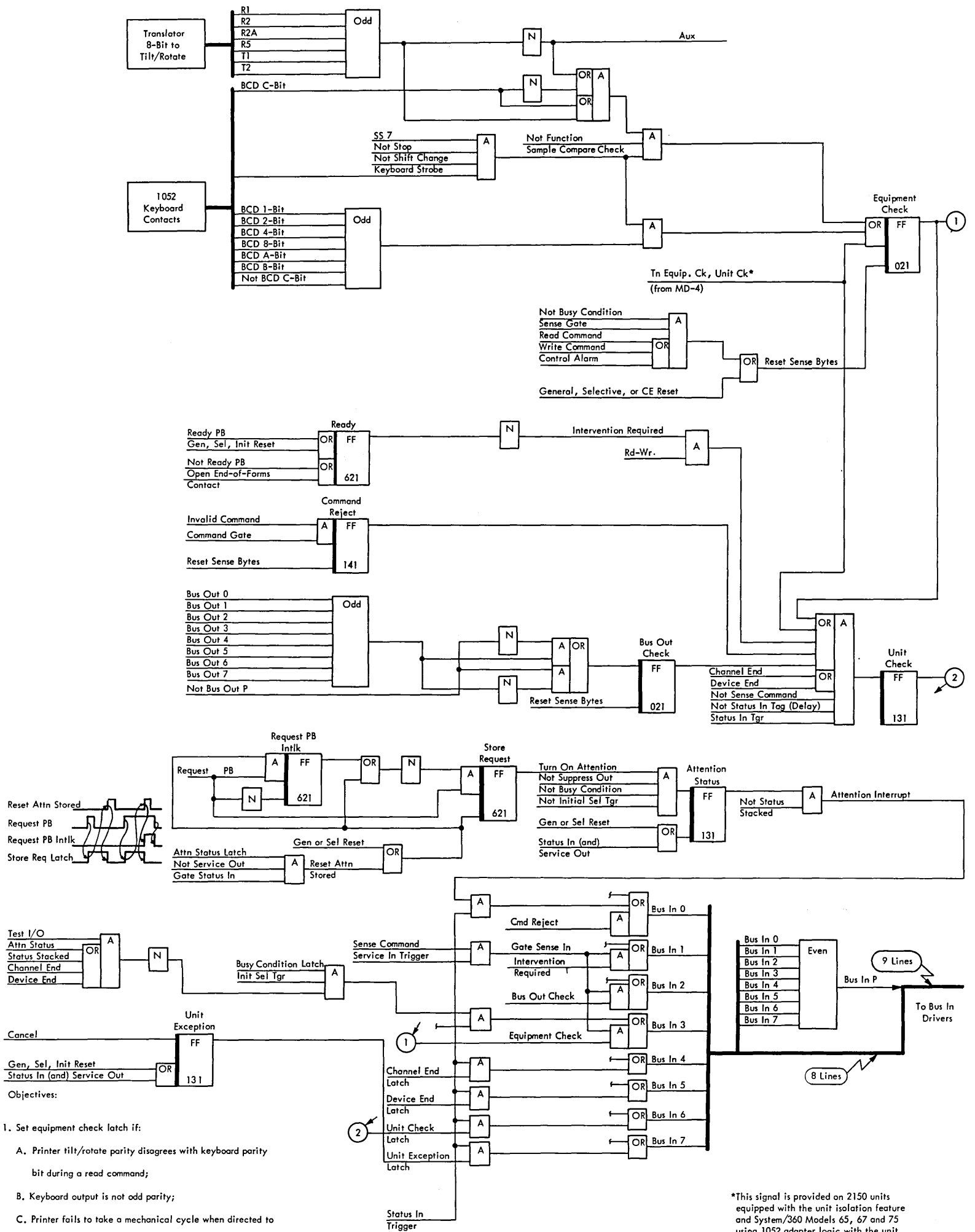


Objectives:

1. Start read/write clock at SS 5 when a key is operated.
2. Gate keyboard translator output to data register.
3. Raise request-in.
4. Raise operational-in and address-in, gate address byte to bus-in lines.
5. Raise service-in and gate data register output to bus-in lines when command-out falls.
6. Start read/write clock at cycle time (to operate printer) when channel accepts data byte replying service-out to service-in.

FIGURE MD-5. (I/O) DATA TRANSFER--READ Maintenance Diagrams (5-66) 67

FIGURE MD-6. (I/O OP) SENSE AND STATUS BYTES



- Objectives:
- Set equipment check latch if:
    - Printer tilt/rotate parity disagrees with keyboard parity bit during a read command;
    - Keyboard output is not odd parity;
    - Printer fails to take a mechanical cycle when directed to print, up- or down-shift, tab, space, or backspace.
  - Set unit check latch when status-in trigger is on for any of the following conditions:
    - Equipment check latch is on
    - Ready Latch is not on
    - Command reject latch is on
    - Bus-out check latch is on (even parity byte on bus-out lines).

\*This signal is provided on 2150 units equipped with the unit isolation feature and System/360 Models 65, 67 and 75 using 1052 adapter logic with the unit isolation feature installed.

Note: See page 34 for 1052 Adapter Index.

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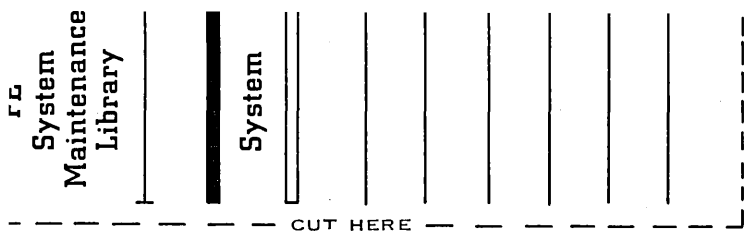
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