MOTOROLA

Commercial Series
CP040 Radios

Power Distribution and Controller
Service Information

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Chapter 1

THEORY OF OPERATION

1.0 Overview

This Chapter provides a detailed theory of operation for the controller circuits in the radio. The components of these circuits are contained on the Main Board. Refer to the RF sections of this manual for the component location details and the parts lists of the Controller Circuits.

2.0 Radio Power Distribution

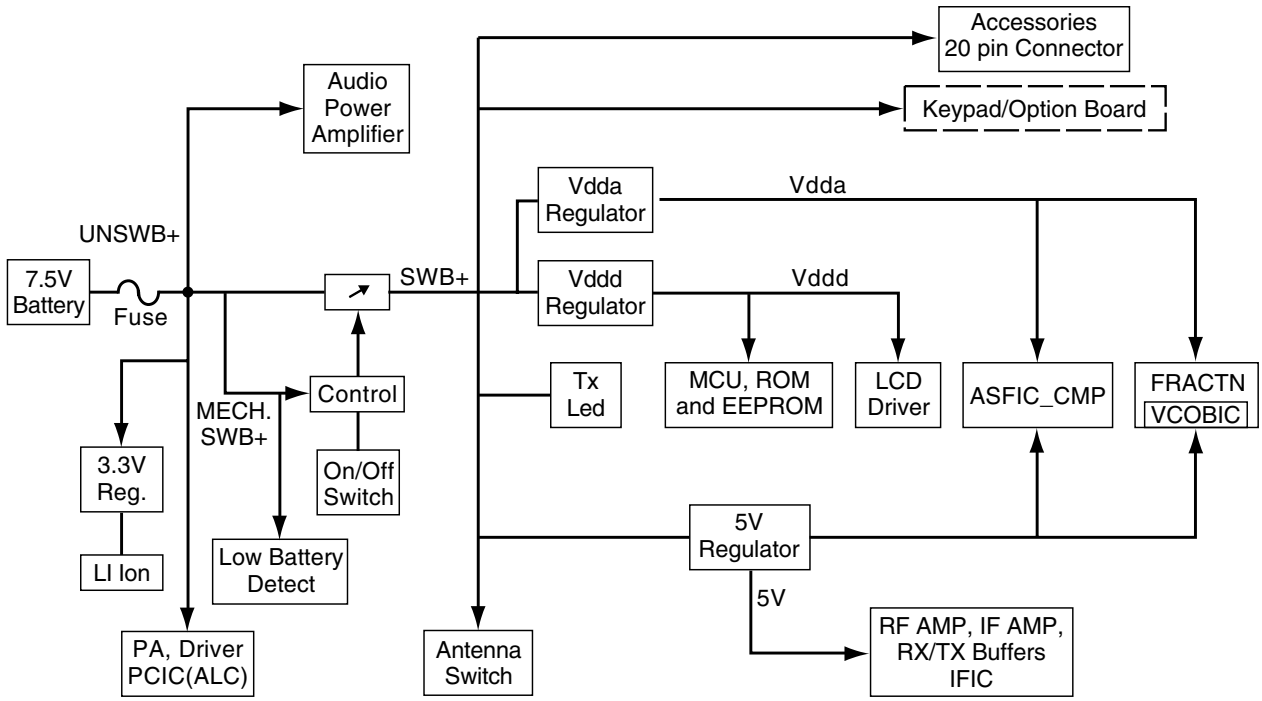


Figure 1-1 DC Power Distribution Block Diagram

Figure 1-1 illustrates the DC distribution throughout the radio board.

Battery voltage enters at connector J301 and is routed through fuse F301 to become USWB+. VR301 protects against ESD, and D301 provides reverse polarity protection. This voltage is routed to:

- FET switch Q170 in the TX power control circuit (turned on during transmit)
- TX power amplifier module U110 (via R150)
- input pins of regulators U310, U320 and U330
- FET switch Q493 (turned on whenever the radio is on)
- on-off switch S444 (part of on-off-volume control) to become SWB+

When the radio is turned on, SWB+ is present and is applied to:

- transistor switch Q494 (pins 1 and 6) which turns on Q493
- RX audio power amplifier U490
- voltage divider R420/R421 and port PE0, a microprocessor A/D input which measures battery voltage and radio on/off status

The output of FET switch Q493 is applied to the control pins of regulators U310, U320 and U330, turning them on. The following regulators are used:

Table 1-1 Voltage Regulators

Reference No.	Description	Type
U310	5V Regulator	TK71750S
U320	Digital 3.3V Regulator	LP2986
U330	3V Regulator	TK71730S

The 5V source is applied to:

- RX back end circuitry
- synthesizer super filter input and charge pump supply
- RED/GRN LEDs
- RX audio buffer U510
- portions of ASFIC U451

The 5V source is also applied to FET switches Q311 and Q312. Q311 is turned on by Q313 when RX_ENA (from U401 pin 49) is high, and supplies the "5R" source to the RF front end stages Q21-Q22, and the VCO RX injection buffer Q280. Q312 is turned on by Q313 when TX_ENA (from U401 pin 50) is high, and supplies the "5T" source to the first transmitter stage Q100.

The digital 3.3 volt source from U320 (D_3.3V) is applied to:

- microprocessor U401
- EEPROM U402
- S-RAM U403 (not used)
- flash ROM U404

The 3V regulated source from U330 is applied to:

- synthesizer IC U201
- VCO/buffer IC U251
- portions of ASFIC U451
- microphone bias circuitry

While the radio is turned on, port PH3 (U401 pin 44) is held high. When the radio is turned off, SWB+ is removed and port PE0 (U401 pin 67) goes low, initiating a power-down routine. Port PH3 (pin 44) remains high, keeping the voltage regulators on via Q493 and Q494, until the operating state of the radio has been stored in EEPROM and other turn-off data functions have been completed. PH3 then goes low, turning off Q494 and Q493, and all regulated voltages are removed.

3.0 Controller Circuits

3.1 General

The controller board is the central interface between the various subsystems of the radio. It provides the following functions:

- interface with controls and indicators
- serial bus control of major radio circuit blocks
- encoding and/or decoding of selective signaling formats such as PL, DPL, MDC1200 and QuikCall II
- interface to CPS programming via the microphone connector
- storage of customer-specific information such as channel frequencies, scan lists, and signaling codes
- storage of factory tuning parameters such as transmitter power and deviation, receiver squelch sensitivity, and audio level adjustments
- power-up, power-down and reset routines

In the UHF and VHF sections, the Radio Block Interconnect Diagram show the interconnections between the controller and the various other radio blocks, while the Controller Interconnect Schematic diagram (in this chapter) shows the connections between the following circuit areas which comprise the controller block:

- microprocessor circuitry
- audio circuitry
- DC regulation circuitry
- rotary and pushbutton controls and switches

The majority of the circuitry described below is contained in the Microprocessor Circuit schematic diagrams. However, portions are also found in the DC Regulation and UHF/VHF Audio Circuit schematics.

3.2 Microprocessor Circuitry

The microprocessor circuitry includes microprocessor (U401) and associated EEPROM and Flash ROM memories. The following memory IC's are used:

Table 1-2 Radio Memory Requirements

Reference No.	Description	Type	Size
U402	Serial EEPROM	AT25128	16K x 8
U403	Static RAM	(not used)	
U404	Flash ROM	AT49LV001N_70V	128K x 8

3.2.1 Memory Usage

Radio operation is controlled by software that is stored in external Flash ROM memory (U404). Radio parameters and customer specific information is stored in external EEPROM (U402). The operating status of the radio is maintained in RAM located within the microprocessor. When the radio is turned off, the operating status of the radio is written to EEPROM before operating voltage is removed from the microprocessor.

Parallel communication with U403 and U404 is via:

- address lines A(0)-A(16), from U401 port F ADDR0-ADDR13 and port G XA14-XA16
- data lines D(0)-D(7), from U401 port C DATA0-DATA7
- chip-select for U403, from PH6 (U401 pin 41)
- chip-enable for U404, from PH7 (U401 pin 38)
- output enable for U404, from PA7 (U401 pin 86)
- write-enable for both U403 and U404, from PG7_R/W (U401 pin 4)

Serial communication with U402 is via:

- the SPI bus
- chip-select for U402, from PD6 (U401 pin 3)

3.2.2 Control and Indicator Interface

Ports PI3 and PI4 are outputs which control the top-mounted LED indicator. When PI3 is high, the indicator is red. When PI4 is high, the indicator is green. When both are high, the indicator is amber. When both are low, the indicator is off.

Pressing the side-mounted PTT button (S441) provides a low to port PJ0 (U401 pin 71), which indicates PTT is asserted. Side-mounted option buttons 1 and 2 (S442 and S443) are connected to Ports PJ6 (pin 77) and PJ7 (pin 78), respectively.

3.2.3 Serial Bus Control of Circuit Blocks

The microprocessor communicates with other circuit blocks via a SPI (serial peripheral interface) bus using ports PD2 (data into uP), PD3 (data out of uP) and PD4 (clock). The signal names and microprocessor ports are defined in Table 1-3.

Table 1-3 SPI Bus Signal Definitions

Signal Name	Microprocessor Port	Microprocessor Pin
SPI-DATA_IN	PD2-MISO	U401 Pin 99
SPI_DATA_OUT	PD3-MOSI	U401 pin 100
SPI_CLK	PD4-SCK	U401 pin 1

These signals are routed to:

- the audio filter IC (U451) to control internal functions such as gain change between 25 kHz and 12.5 kHz channels, transmit or receive mode, volume adjustment, etc.
- the synthesizer IC U201 to load receive and transmit channel frequencies
- option board connector J460-1 for internal option configuration and control (not used in CP040)
- serial EEPROM U402 (both SPI_DATA_IN and SPI_DATA_OUT are used)

In order for each circuit block to respond only to the data intended for it, each peripheral has its own chip select (or chip enable) line. The device will only respond to data when its enable line is pulled low by one of the microprocessor ports, as follows:

- port PD5 (U401 pin 2) for the audio filter IC
- port PH0 (U401 pin 47) for the synthesizer IC
- port PH4 (U401 pin 43) for the option board/display enable (not used in CP040)
- port PD6 (U401 pin 3) for the serial EEPROM

3.2.4 Interface to RSS Programming

The radio can be programmed, or the programmed information can be read, using a computer with CPS (Customer Programming Software) connected to the radio via a RIB (radio interface box) or with the RIB-less cable. Connection to the radio is made via the microphone connector (part of accessory connector J471). The SCI line connects the programming contact (J471 pin 6) to ports PD0_RXD (data into uP, pin 97) and PD1_TXD (data out of uP, pin 98). Transistor Q410 isolates the input and output functions by allowing PD1 to pull the line low, but does not affect incoming data from being read by port PD0. This isolation allows high-speed 2-wire programming via TP401 and TP402 for factory programming and tuning.

3.2.5 Storage of Customer-Specific Information

Information that has been programmed using CPS, such as channel frequencies or selective signaling codes, are stored in the external EEPROM, where it is retained permanently (unless reprogrammed) without needing DC power applied to the microprocessor.

3.2.6 Sensing of Externally-Connected Accessories

Port PJ1 is used to detect the presence of externally connected accessories. Port PJ1 (U401 pin 72) is normally low, unless accessories (lapel speaker microphone, lightweight headset, etc.) are used with the radio. This port is used to detect an accessory PTT or auto sensing of a VOX accessory.

If VOX is programmed into the radio channel codeplug information, and PJ1 is high during power-up, the radio will activate VOX operation. If a low is present at port PJ1 during power-up, the radio will use this port as an external PTT indicator.

3.2.7 Microprocessor Power-Up, Power-Down and Reset Routine

On power-up, the microprocessor is held in reset until the digital 3.3V regulator (U320 pin 5) provides a stable supply voltage. Once the digital supply reaches steady state and releases the reset line (U320 pin 7), the microprocessor begins to start up. The ASFIC_CMP (U451) has already started running and is providing the startup clock to the microprocessor. After reset release by all circuits, the software within the microprocessor begins executing port assignments, RAM checking, and initialization. A fixed delay of 100 ms is added to allow the audio circuitry to settle. Next, an alert beep is generated and the steady state software begins to execute (buttons are read, radio circuits are controlled).

When the radio is turned off, SWB+ is removed and port PE0 (U401 pin 67) goes low, initiating a power-down routine. Port PH3 (pin 44) remains high, keeping the voltage regulators on via Q493 and Q494, until the operating state of the radio has been stored in EEPROM. PH3 then goes low, and all regulated voltages are removed.

The microprocessor reset line (pin 94) can be controlled directly by the digital 3.3 V regulator (U320 pin 7), the microphone jack (part of accessory connector J471) via Q472 and Q471, and the microprocessor itself. U320 pulls the reset line low if the digital 3.3 V source loses regulation. This prevents possible MOS latch-up or overwriting of registers in the microprocessor because the reset line is higher in voltage than the microprocessor VDD ports (U401 pins 12, 39, 59, 88). The microprocessor can drive the reset line low if it detects a fault condition such as an expired watchdog timer, software attempting to execute an infinite loop, unplanned hardware inputs, static discharge, etc. Finally, the Q471 can pull the reset line low during use of the programming cable and CPS by the application of a sufficiently negative voltage to the microphone connector tip contact (J471 pin 4), however this reset method is not utilized.

3.2.8 Boot Mode Control

When power-up reset occurs, the microprocessor will boot into either normal or flash mode depending on the logic level of ports MODA (U401 pin 58) and MODB (pin 57). The Flash Adapter is a programming accessory which provides negative 9 volts dc via a 1K resistor to microphone connector J471 pin 4. This turns on Q471 and Q472 via D471 and VR472, pulling MODA and MODB low and allowing booting in the flash mode by cycling power to reset the radio. Software upgrades can then performed by loading the new software code into Flash ROM U404.

3.2.9 Microprocessor 7.3975 MHz Clock

The 7.3975 MHz clock signal (uP_CLK) is provided from the ASFIC_CMP (U451 pin 28). Upon startup the 16.8MHz crystal provides the signal to the ASFIC_CMP, which sends out the uP_CLK at 3.8MHz until a steady-state condition is reached and the clock is increased to 7.3975MHz for the microprocessor.

3.2.10 Battery Gauge

Various battery types are available having different capacities. The different battery types contain internal resistors connected from the BATT_CHARGE contact to ground (which is routed to the microprocessor as BATT_DETECT). A voltage divider is formed with R255 producing a different DC voltage for each battery type, which is read by microprocessor port PE2 (pin 65). This allows the software to recognize the battery chemistry being used and adjust the battery gauge for best accuracy.

3.3 Audio Circuitry

3.3.1 Transmit and Receive Low-Level Audio Circuitry

The majority of RX and TX audio processing is performed by U451, the Audio Filter IC (ASFIC_CMP), which provides the following functions:

- Tone PL/Digital PL encoding and decode filtering
- Tone PL/Digital PL rejection filter in RX audio path
- TX pre-emphasis amplifier
- TX audio modulation limiter
- Post-limiter (splatter) filter
- TX deviation adjust (digitally-controlled attenuators)
- Programmable microphone gain attenuator
- RX audio volume control (digitally controlled attenuator)
- Carrier squelch adjustment (digitally controlled attenuator)
- Microprocessor output port expansion
- 2.5 volt dc reference source
- Microprocessor clock generation (from the 16.8 MHz reference oscillator input)

The parameters of U451 that are programmable are selected by the microprocessor via the CLOCK (U451 pin 21), DATA (U451 pin 22) and chip enable (U451 pin 20) lines.

RX audio buffer U510 amplifies the audio level from the DEMOD output of the IFIC before being applied to the audio filter IC input (DISC, U451 pin 2). The buffer is DC coupled to avoid corruption of low-frequency data waveforms such as DPL. Because such waveforms are polarity sensitive, this buffer is configured as a single-stage inverting amplifier (U510-1 only) for VHF models where high-side first injection is used, or is configured as a two-stage non-inverting amplifier (U510-1 and -2) for UHF models using low-side first injection. The gain of the buffer is 1.5 times or 3.5 dB.

U480 and associated components are not used in CP040. Stage U480-1 is bypassed by jumper R487.

Volume adjustment is performed by a digital attenuator within U451. The volume control (10KO, part of S444) is connected to D_3.3V and ground via R506 and R507. When the volume control is rotated, it varies the dc voltage applied to microprocessor A/D input port PE1 (U401 pin 66) between approximately 0 volts dc at minimum volume to 3.3 volts dc at maximum volume. Depending on this voltage, the appropriate setting of the digital volume attenuator is selected. This technique is less susceptible to noise than a conventional analog volume control.

3.3.2 Audio Power Amplifier

The audio power amplifier IC U490 amplifies receiver audio from U451 pin 41 to a level sufficient to drive a loudspeaker. U490 is a bridge amplifier delivering 3.46 volts rms between pins 5 and 8 without distortion, which is sufficient to develop 500 milliwatts of audio power into the internal 24 ohm speaker or an external 24 ohm load. The audio power amplifier is muted whenever speaker audio is not required to reduce current drain. The audio amp is muted when U451 pin 14 is low. When U451 pin 14 is high, U490 pin 1 is pulled low by Q490, enabling the audio amplifier.

Because the power amplifier is a bridge-type, neither speaker terminal is grounded. Care should be taken that any test equipment used to measure the speaker audio voltage does not ground either speaker output terminal, otherwise damage to the audio power amplifier IC may result. When a 24-ohm load resistor is used it should be connected between the tip and the sleeve of accessory jack J471 (3.5mm port), never to ground. External SPKR plug insertion mechanically disconnects the internal speaker. Voltage measurements using test equipment that is not isolated from ground may be made from one side of the speaker or load resistor (either the tip or the sleeve of J471) to chassis ground, in which case the voltage indicated will be one half of the voltage applied to the speaker or load resistor. The Motorola RLN4460 Portable Test Set and PMKN4004 Programming Test Cable provide the proper interface between the radio's ungrounded audio output and ground-referenced test equipment.

3.3.3 Internal Microphone Audio Voice Path

Microphone audio from internal microphone is routed from J470-1 via C475, L471, and C470 to the ASFIC_CMP mic audio input (MICINT, U451 pin 46). During transmit, Q470 is turned on by a low at U451 pin 35, providing dc bias for the internal MIC via R478. External MIC plug insertion mechanically disconnects the internal microphone. External MIC audio is coupled through L471 and C470 to the mic audio input. An input level of 10 mV at J471 pin 4 produces 200 mV at the output of U451 pin 40, which corresponds to 60% deviation.

3.3.4 PTT Circuits

The internal side-mounted PTT switch (S441) is sensed directly by microprocessor port PJ0 (U401 pin 71). External mic PTT is sensed by measuring the current drawn through the accessory connector (J471-4) by the mic cartridge (which is in series with the accessory PTT switch). This current is drawn through the base (pin 5) and emitter (pin 4) of a transistor in Q470, causing its collector (pin 3) to supply a logic-high to microprocessor port PJ1 (pin 72).

3.3.5 VOX Operation

VOX audio accessories do not have a PTT switch. Instead, the mic cartridge is wired directly from J471-4 to ground. If the radio has been programmed for VOX operation and the VOX accessory is plugged in prior to turning the radio on, the current drawn by the cartridge will turn on Q470 (pins 3-4-5) and a logic high will be seen at port PJ1 at turn-on. The microprocessor then assumes VOX operation, with PTT controlled by the presence of audio at the mic cartridge. A dc voltage proportional to the audio level at the input of the ASFIC_CMP (U451 pin 46) is fed to an A/D input of microprocessor U401 (pin 62). During VOX operation, PTT is activated when the dc level exceeds a preset threshold.

3.3.6 Battery Charging Through Microphone Jack

A wall-type charging power supply may be connected to the 2.5 mm microphone jack (part of accessory connector J451). The voltage present at the tip contact (pin 4) is applied to the center charging contact of the battery via diode D470. Another diode, internal to the battery, applies this voltage to the (+) battery terminal. Only the recommended charger and battery type should be charged in this manner.

Different battery types contain internal resistors connected from the BATT_CHARGE contact to ground, which is routed to the microprocessor as BATT_DETECT. A voltage divider is formed with R255 producing a DC voltage which is read by microprocessor port PE2 (pin 65). This allows the software to recognize the battery chemistry being used and adjust the battery gauge for best accuracy. The value of R255 is chosen so that the voltage at the BATT_CHARGE node (cathode of D470) is never low enough to turn on the EXT_MIC_PTT sense transistor (part of Q470).

3.3.7 Programming and Flashing Through Microphone Jack

The ring contact on the 2.5 mm microphone jack is used for reading, programming or re-flashing the radio using CPS. This contact (J471 pin 6) is routed to ports PD0_RXD (data into uP, pin 97) and PD1_TXD (data out of uP, pin 98). Transistor Q410 isolates the input and output functions by allowing PD1 to pull the line low, but does not affect incoming data from being read by port PD0.

To re-flash the radio (overwrite the software in the Flash ROM with new software), the radio must power up in the boot mode. This is accomplished by using a flash adapter accessory, which provides SCI communication with the programming ring contact (J471 pin 6) and also allows a negative voltage (negative 9 volts dc via a 1K resistor) to be applied to the tip contact (J471 pin 4). This voltage is sufficient to turn on the base-emitter junction (pins 1 and 2) of Q472 via L471, D471, VR472 and R471. Pin 6 of Q472 goes high, turning on Q471 (pins 3 and 4) and pulling the BOOT_ENA line (ports MODA and MODB of the microprocessor) low. Cycling power generates a reset which causes the radio to boot in the flash mode.

Chapter 2

TROUBLESHOOTING TABLES

1.0 Troubleshooting Tables for Board and IC Signals (includes Controller, DC Regulation and Audio)

This section contains detailed troubleshooting tables. These tables should be used as a guide in determining the problem areas. They are not a substitute for knowledge of circuit operation and astute troubleshooting techniques. It is advisable to refer to the related detailed circuit descriptions in the theory of operation sections prior to troubleshooting a radio.

Most troubleshooting tables end up by pointing to an IC to replace. It is not always noted, but it is good practice to verify supplies and grounds to the affected IC and to trace continuity to the malfunctioning signal and related circuitry before replacing any IC. For instance, if a clock signal is not available at a destination, continuity from the source IC should be checked before replacing the source IC.

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U310 5V Regulator	1	Vin	7.48	
	2	Ground	GND	
	3	Control input	7.48	
	4	Bypass capacitor	1.26	
	5	Vout	4.96	
U320 3.3V Regulator	1	Ground	GND	
	2	Feedback	1.23	
	3	Tap (NU)	0	
	4	Vin	7.48	
	5	Vout	3.23	
	6	Sense (NU)	0	
	7	Error (reset output)	3.20	
	8	Shutdown input	7.48	
U330 3V Regulator	1	Vin	7.48	
	2	Ground	GND	
	3	Control input	7.48	
	4	Bypass capacitor	1.26	
	5	Vout	3.00	

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	1	PD4_SCK serial clock input	0	
	2	PD5_SS	3.23	ASFIC chip select
	3	PD6_VLIN	3.23	EEPROM chip select
	4	PG7_R_W	3.21	
	5	PG6_AS	3.23	
	6	PG0_XA13	3.23	
	7	PB7_ADDR15	0.026	
	8	PB6_ADDR14	0.028	
	9	PB3_ADDR11	3.06	
	10	PB1_ADDR9	3.05	
	11	PB2_ADDR10	0.16	
	12	VDD	3.23	
	13	VSS	GND	
	14	PBO_ADDR8	3.05	
	15	PB5_ADDR13	0.13	
	16	PG1_XA14	0.20	
	17	PG4_XA17	3.17	
	18	PG5_XA18	0	
	19	PG3_XA16	3.21	
	20	PG2_XA15	0.30	
	21	PB4_ADDR12	0.22	
	22	PF7_ADDR7	3.03	
	23	PF6_ADDR6	3.08	
	24	PF5_ADDR5	3.06	
	25	PF4_ADDR4	0.16	
	26	PF3_ADDR3	0.26	
	27	PF2_ADDR2	3.06	
	28	PF1_ADDR1	3.06	
	29	PFO_ADDR0	3.05	
	30	PC0_DATA0	0.69	
	31	PC1_DATA1	0.96	
	32	PC2_DATA2	1.10	
	33	PC3_DATA3	0.81	
	34	PC4_DATA4	0.62	
	35	PC5_DATA5	0.68	
	36	PC6_DATA6	0.67	
	37	PC7_DATA7	0.73	

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	38	PH7_CSPROG	3.05	
	39	VDDL	3.23	
	40	VSSL	GND	
	41	PH6_CSGP2	3.23	
	42	PH5_CSGP1	3.23	
	43	PH4_CSIO	0	
	44	PH3_PW4	3.21	On/off control output
	45	PH2_PW3	0	
	46	PH1_PW2	3.00	
	47	PH0_PW1	3.23	Synth chip select
	48	XIRQ	3.00	
	49	PI7	1.48	RX enable
	50	PI6	0.01	TX enable
	51	PI5	3.23	
	52	PI4	0	Green LED enable
	53	PI3	0	Red LED enable
	54	PI2	0	
	55	PI1	0	
	56	PI0	2.98	Lock detect from U201-4
	57	MODB_VSTBY	3.22	Boot mode enable
	58	MODA_LIR	3.12	
	59	AVDD	3.23	
	60	PE7_AN7	3.20	
	61	PE6_AN6	3.20	
	62	PE5_AN5	2.91	VOX threshold detect
	63	PE4_AN4	0.73	RSSI input
	64	PE3_AN3	0.14	
	65	PE2_AN2	1.62	
	66	PE1_AN1	0 - 3.3 V	Volume control wiper
	67	PE0_AN0	2.48	33% of battery voltage
	68	VRL	0	
	69	VRH	3.20	
	70	AVSS	GND	
	71	PJ0_CSGP3	3.23	Side PTT button
	72	PJ1_CSGP4	0	External MIC PTT
	73	PJ2	3.23	
	74	PJ3	3.23	

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U401 Microprocessor	75	PJ4	3.23	
	76	PJ5	0	
	77	PJ6	3.23	Bottom option button
	78	PJ7	3.23	Top option button
	79	PA0_IC3	0	
	80	PA1_IC2	1.57	
	81	PA2_IC1	3.00	
	82	PA3_IC4_OC5_OC1	3.00	
	83	PA4_OC4_OC1	0	Squelch detect input
	84	PA5_OC3_OC1	0	Channel activity input
	85	PA6_OC2_OC1	0	
	86	PA7_PA1_OC1	0	
	87	VSSR	GND	
	88	VDDR	3.23	
	89	ECLK (NU)	1.60	
	90	EXTAL	1.70	Clock from U451-28
	91	XTAL	1.40	Not used
	92	VDDSYN	0	
	93	XFC (NU)	0	
	94	RESET	3.20	From U320
	95	LVOUT	0	
	96	IRQ	3.20	
	97	PD0_RXD	3.23	
	98	PD1_TXD	1.9	
	99	PD2_MISO	0	
	100	PD3_MOSI	3.23	
U402 EEPROM	1	Chip select	3.23	From U401-3
	2	Serial data out	0	
	3	Write protect	3.23	
	4	Vss	GND	
	5	Serial data in	3.23	
	6	Serial clock	0	
	7	Hold	3.23	
	8	Vcc	3.23	

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U404 Flash ROM	1	A11	3.06	
	2	A9	3.08	
	3	A8	3.05	
	4	A13	0.13	
	5	A14	0.31	
	6	NC	3.17	
	7	EN_WE	3.21	From U401-4
	8	Vcc	3.23	
	9	RESET	3.20	
U404 Flash ROM	10	A16	3.17	
	11	A15	0.30	
	12	A12	0.22	
	13	A7	3.03	
	14	A6	3.08	
	15	A5	3.06	
	16	A4	0	
	17	A3	0.24	
	18	A2	3.08	
	19	A1	3.05	
	20	A0	3.05	
	21	D0	0.69	
	22	D1	0.94	
	23	D2	1.08	
	24	GND	GND	
	25	D3	0.78	
	26	D4	0.59	
	27	D5	0.66	
	28	D6	0.67	
	29	D7	0.75	
	30	EN_CE	3.01	From U401-38
	31	A10	0.16	
	32	EN_OE	0	From U401-86

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U451 ASFIC_CMP	1	VDD for analog circuits	3.00	
	2	DISC audio input	1.34	From U510
	3	Ground for analog circuits	GND	
	4	DACU output	0	
	5	DACR output	0	
	6	DACG output	2.38 (typ)	Power set (TX mode)
	7	VOX peak detector output	2.91	
	8	PLCAP for DC integrator	0.40	
	9	SQIN	0.01	
	10	Universal audio input/output	0	
	11	VDD for DACs	4.95	
	12	SQCAP	0	
	13	GCB2 general purpose output	0	Audio PA_EN (unsquelched)
	14	GCB1 general purpose output	0	
	15	GCB0 general purpose output	3.00	BW select (25 kHz mode)
	16	Squelch channel activity output	0	To U401-84
	17	Squelch detect digital output	0	To U401-83
	18	PL/low speed data I/O	1.50	
	19	High speed data I/O	3.00	
	20	Chip select	3.23	From U401-2
	21	Serial clock input	0	
	22	Serial data input	3.23	
	23	Ground for clock synthesizer	GND	
	24	Loop filter cap for clock syn	0.74	
	25	PLCAP2 for LS integrator	1.17	
	26	Not used	0	
	27	Vdd for clock synthesizer	3.00	
	28	Clock synthesizer output	1.70	
	29	1200 Hz ref for MDC decode	3.00	
	30	GNDDO	GND	
	31	Ground for digital circuits	GND	
	32	Vdd for analog switches	4.96	
	33	Vdd for digital circuits	3.00	
	34	16.8 MHz master clock input	1.54	
	35	GCB3 general purpose output	3.00	Internal MIC enable
	36	TX audio return from option	0	
	37	GCB4 general purpose output	0	

IC Designator	Pin	Pin Function	DC Voltage	Comments (Condition)
U451 ASFIC_CMP	38	GCB5 general purpose output	0	
	39	RX audio send to option	1.48	
	40	Modulation output	1.50	To U201-10
	41	RX audio out to power amp	1.51	
	42	Flat TX audio return from option	0.20	
	43	RX audio return to option	1.50	
	44	Flat TX audio send to option	1.50	
	45	Vdd for audio path I/O filters	3.00	
	46	Mic audio input	1.50	
	47	Ground for audio path I/O filters	GND	
	48	Ext mic audio input (not used)	0	
U480 Dual Opamp	1	Unit 1 output	2.48	
	2	Unit 1 (-) input	2.48	
	3	Unit 1 (+) input	2.46	
	4	Ground	GND	
	5	Unit 2 (+) input	0.28	
	6	Unit 2 (-) input	0.29	
	7	Unit 2 output	0	
	8	Vcc	4.96	
U490 Audio Power Amp	1	Enable/shutdown	0.12	(Unsquelched)
	2	Bias reference	3.26	(Unsquelched)
	3	(+) input	3.26	(Unsquelched)
	4	(-) input	3.27	(Unsquelched)
	5	(-) output	3.25	(Unsquelched)
	6	Vcc	7.48	(Unsquelched)
	7	Ground	GND	
	8	(+) output	3.29	(Unsquelched)
U510 Dual Opamp	1	Unit 1 output	1.75	
	2	Unit 1 (-) input	1.56	
	3	Unit 1 (+) input	1.55	
	4	Ground	GND	
	5	Unit 2 (+) input	1.55	
	6	Unit 2 (-) input	1.56	
	7	Unit 2 output	1.38	
	8	Vcc	4.96	

1. All voltages are measured with a high-impedance digital voltmeter and expressed in volts DC relative to ground (0V).
2. Voltages are measured with a DC input voltage of 7.50 + .02 volts DC applied to the battery connector (J301).
3. All voltages are measured in the squelched receive mode, unless otherwise indicated.
4. Voltages are identical for VHF and UHF models unless otherwise indicated.

Chapter 3

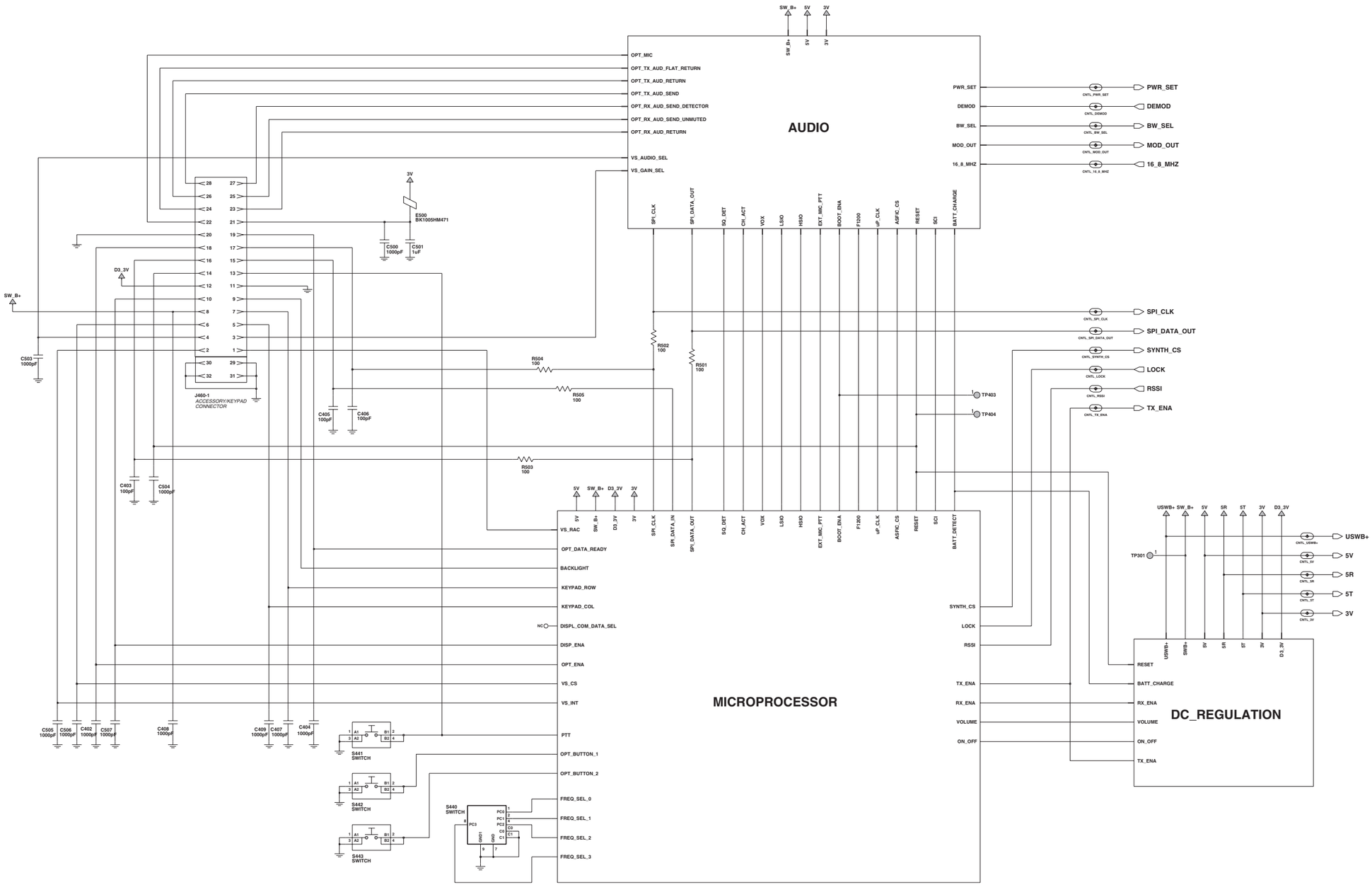
CONTROLLER SCHEMATICS

1.0 Allocation of PCBs and Schematic Diagrams

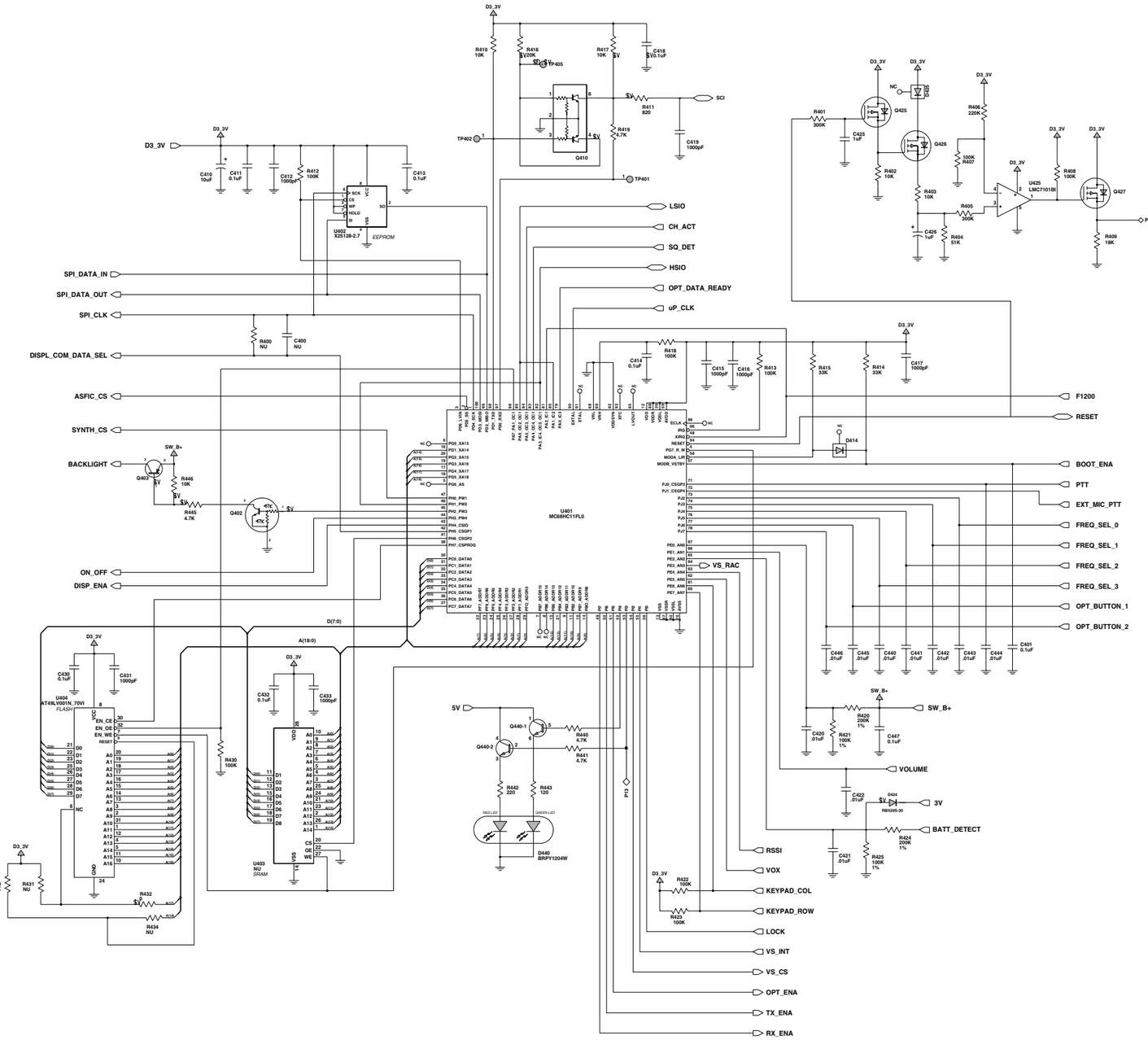
The Controller circuits are contained on the printed circuit board (PCB) containing the RF circuits. This Chapter shows the schematics for the Controller circuits only, refer to the relevant RF section for details of the related RF circuits, the PCB component layouts and the complete radio parts lists. The Controller schematic diagrams and the related PCBs are shown below.

Table 3-1 PCBs and Schematics

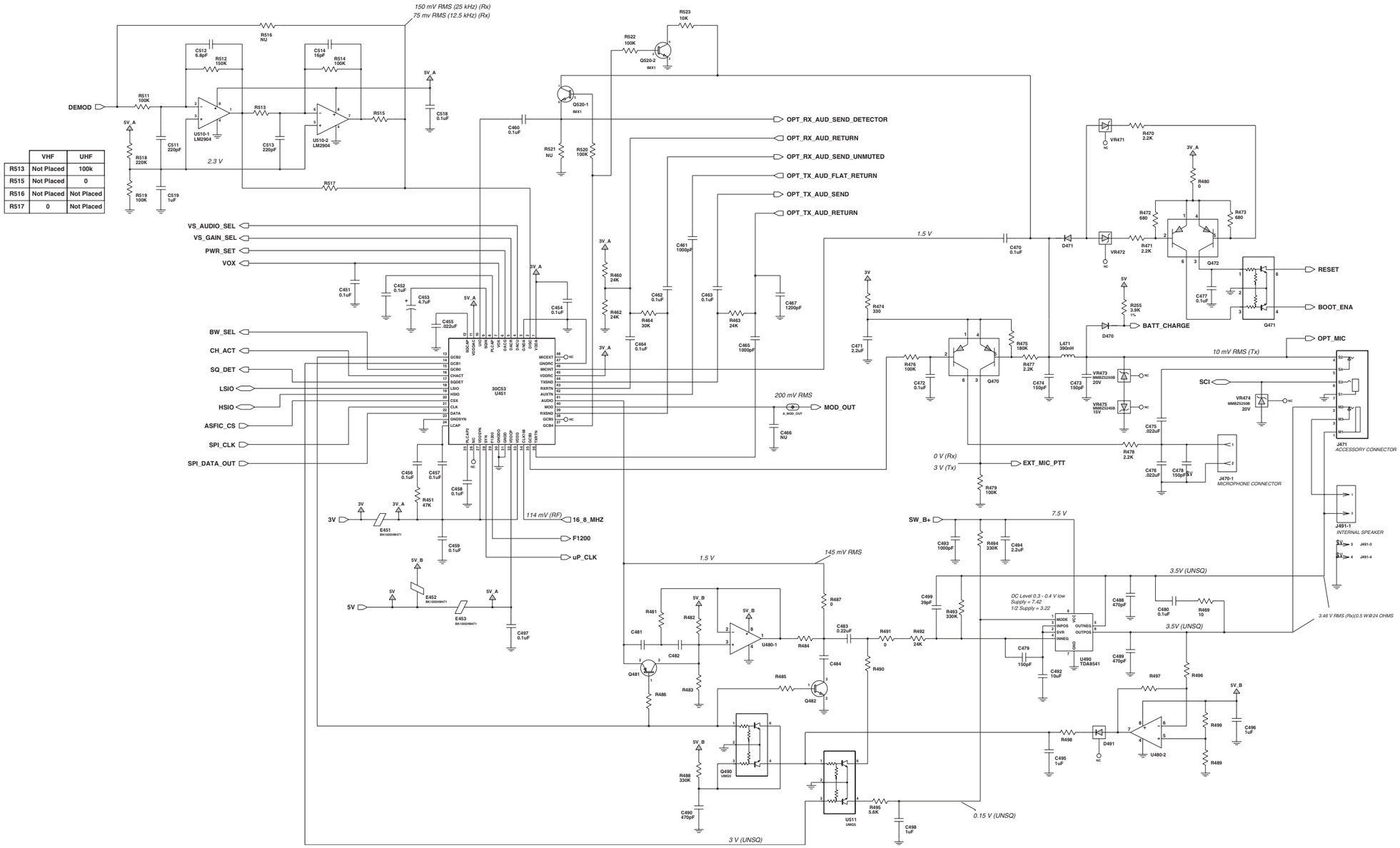
2.0 Controller Schematics



Controller Interconnect Schematic Diagram

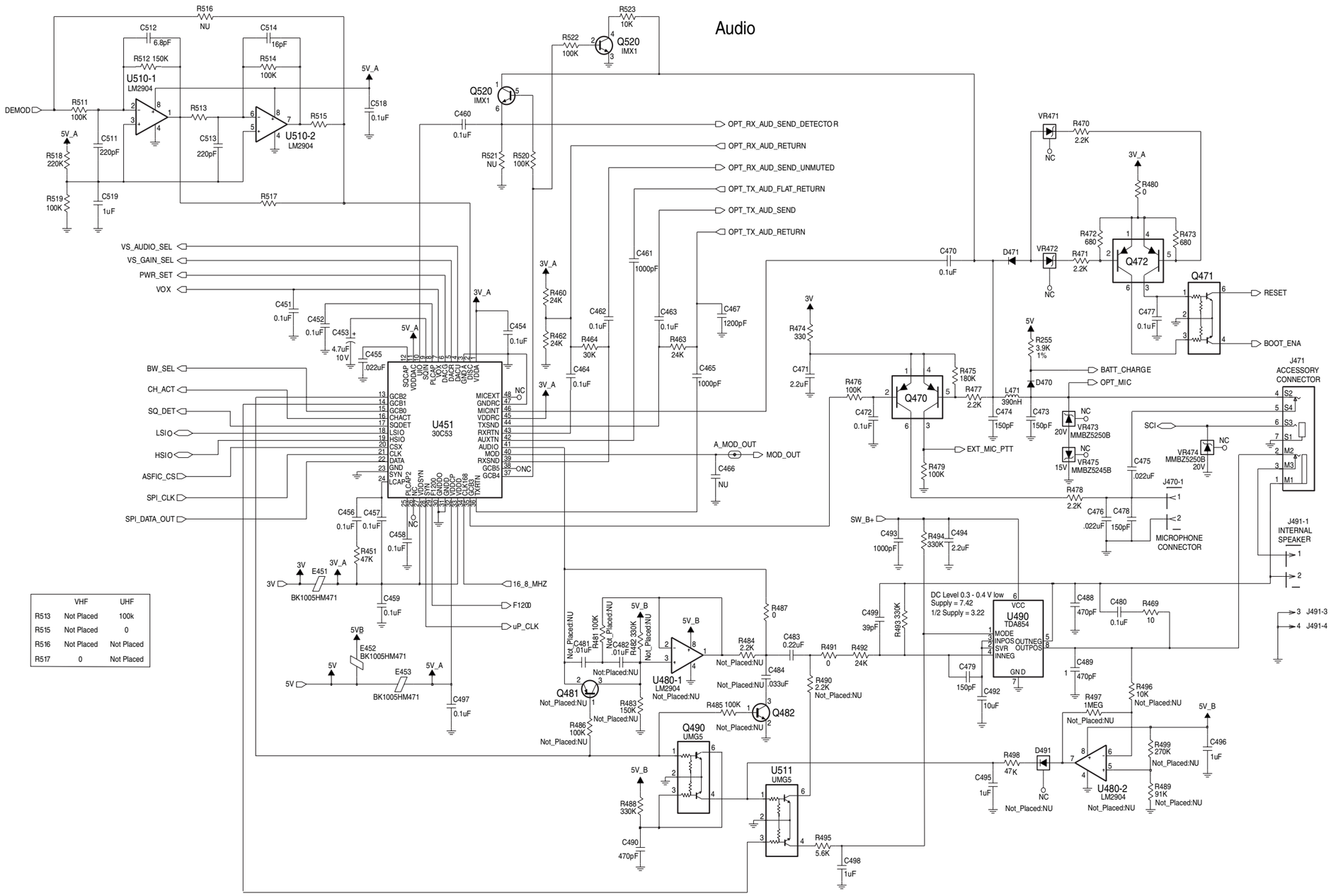


Microprocessor Circuit Schematic Diagram



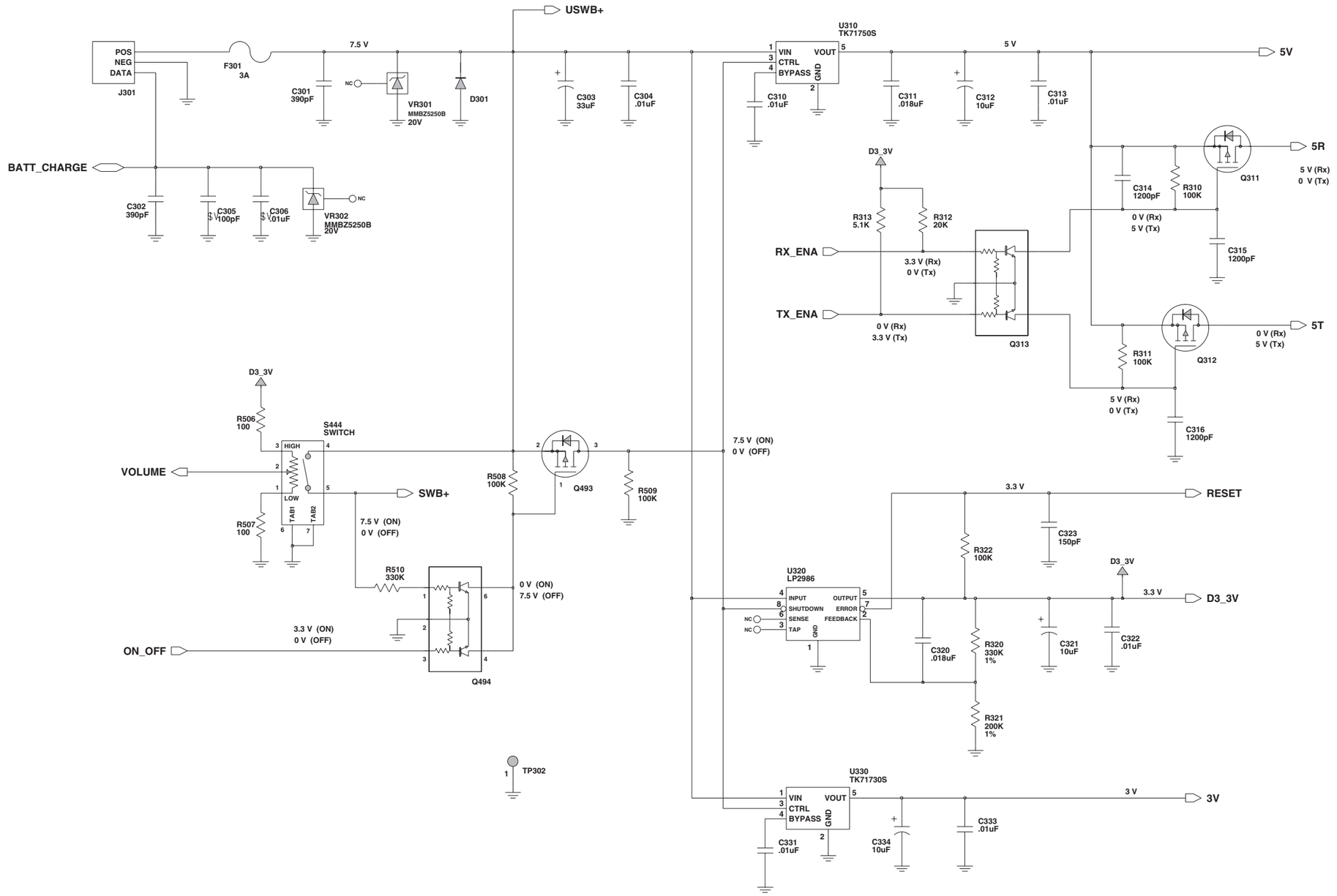
	VHF	UHF
R513	Not Placed	100k
R515	Not Placed	0
R516	Not Placed	Not Placed
R517	0	Not Placed

Audio Circuit Schematic Diagram (VHF)



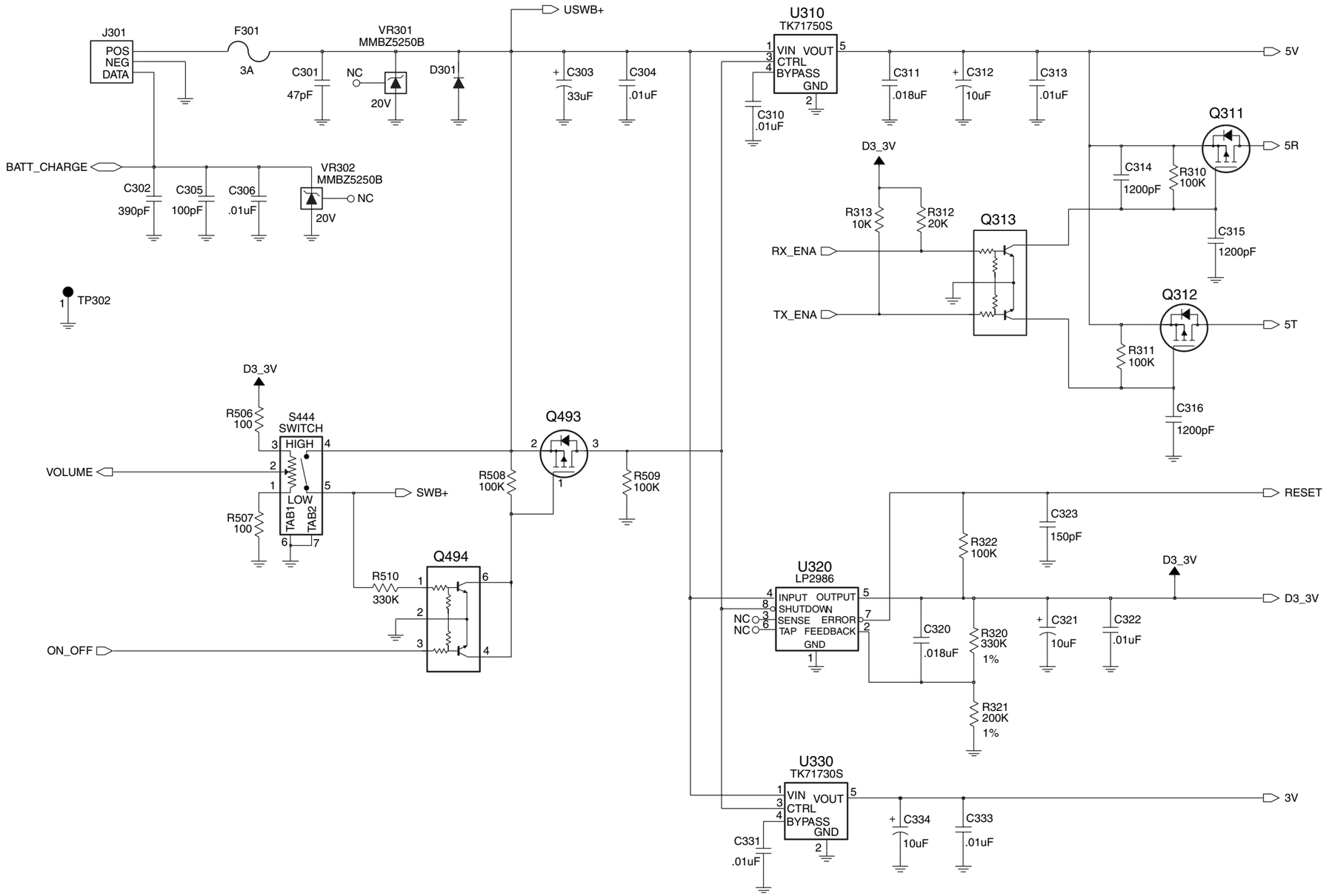
	VHF	UHF
R513	Not Placed	100k
R515	Not Placed	0
R516	Not Placed	Not Placed
R517	0	Not Placed

Audio Circuit Schematic Diagram (UHF)



DC Regulation Schematic Diagram (VHF1/VHF2/UHF1/UHF2)

DC Regulation



DC Regulation Schematic Diagram (UHF3)