# DIGITAL LOGIC & SYSTEM DESIGN



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## Setup and Submission Instructions

**Setup Instructions:**

Please follow the below instructions to setup your unix environment for being able to run Xilinx tools:

1. Logon to the machine using your GCL account.
2. In your home folder, open the .bashrc file and add the below lines (create a new file if .bashrc doesn't exist):

export XILINXD_LICENSE_FILE=2100@10.208.22.170:/extra/xilinxlic/Xilinx.lic

source /opt/Xilinx/14.7/ISE_DS/settings64.sh

source /opt/Xilinx/Vivado/2016.4/settings64.sh

3. Alternatively, you can add the below alias and whenever you open a shell, run the command "enable_xilinx":

alias enable_xilinx="export XILINXD_LICENSE_FILE=2100@10.208.22.170:/extra/xilinxlic/Xilinx.lic;

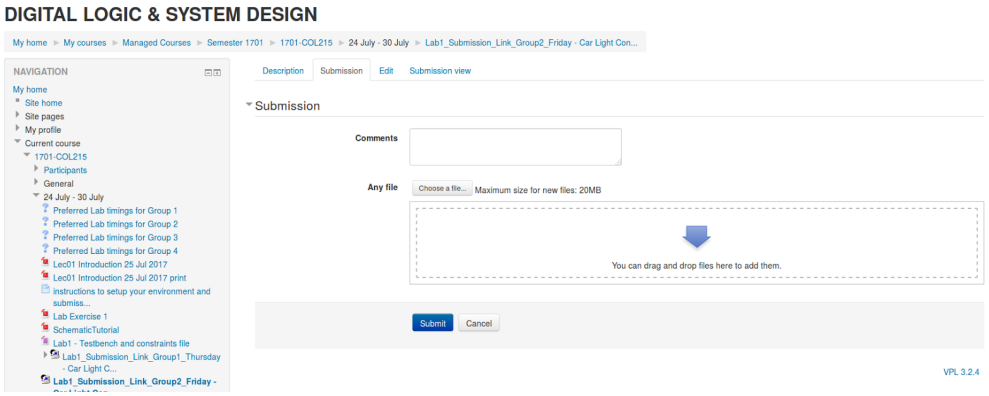
source /opt/Xilinx/14.7/ISE_DS/settings64.sh; source /opt/Xilinx/Vivado/2016.4/settings64.sh"

3. After making changes to .bashrc, run "source .bashrc" in terminal.

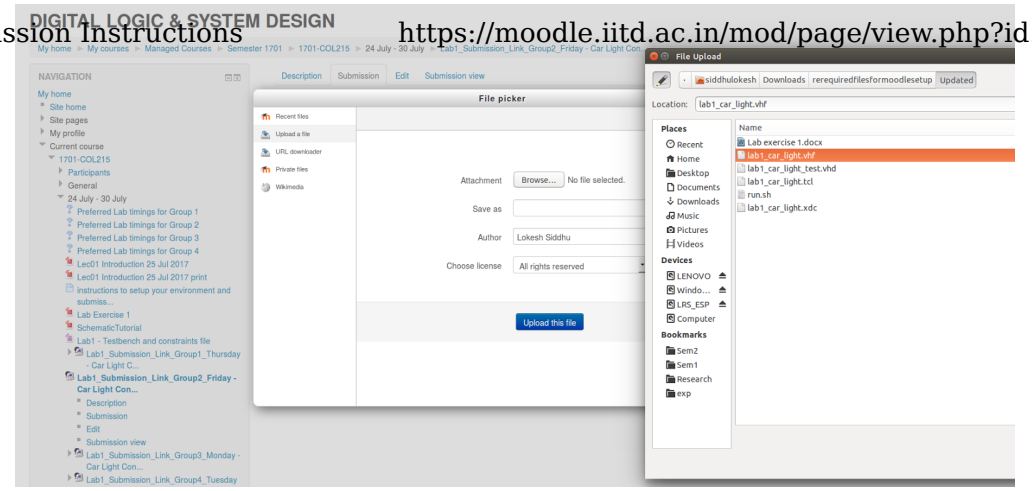
**Submission Instructions:**

Only one of the partner needs to submit. Also, you need to mention the partners name, entry ID (while doing the submission).

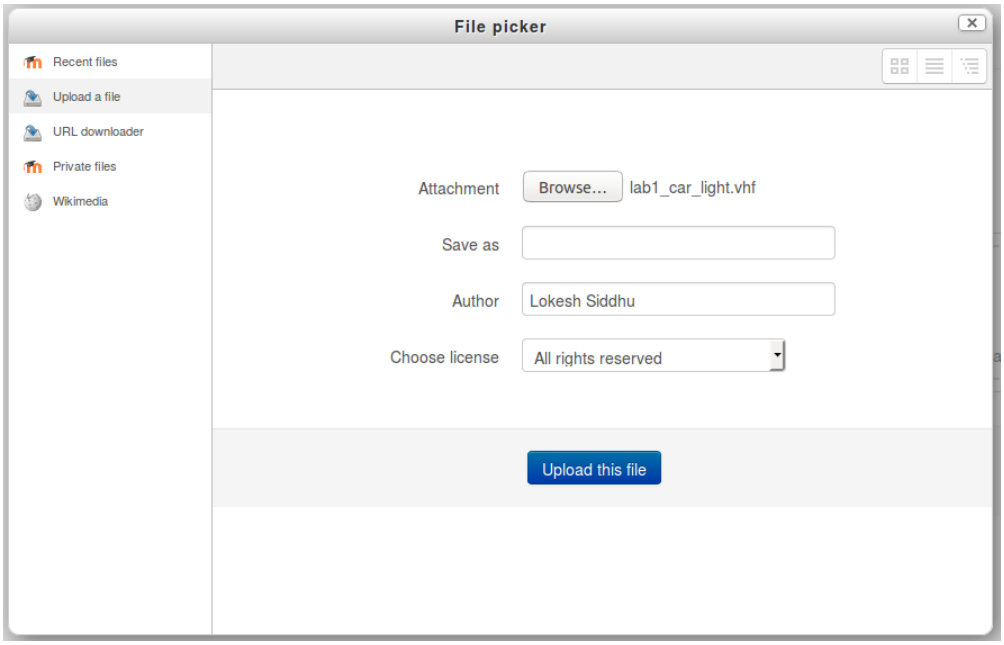
1. Go to the submission tab.



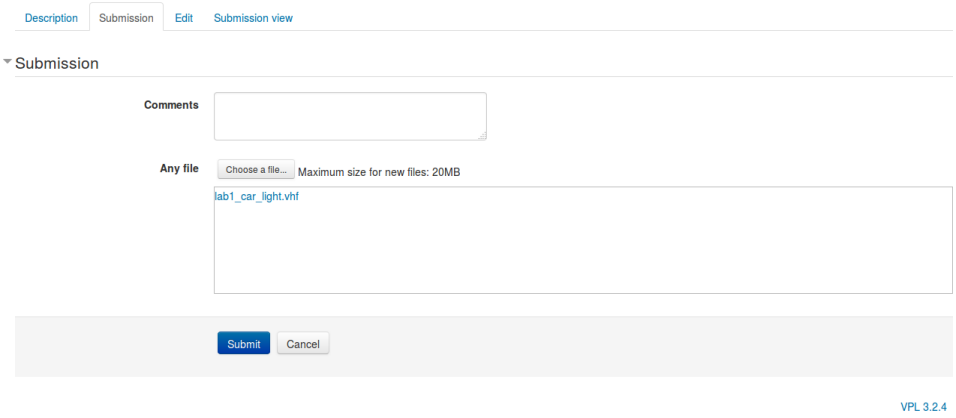

2. Upload the lab1_car_light.vhf by clicking on “choose a file” and then “browse...”



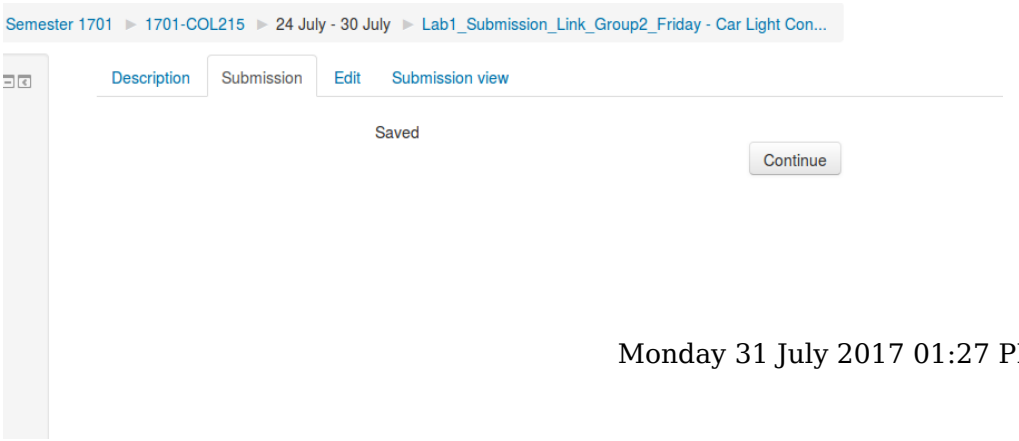

3. Click “Upload this file”




4. Click submit. Mention your name (and entry ID) , your partner's name (and entry ID) in the comments.




5. Click continue.



18 December - 24 December
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1 January - 7 January
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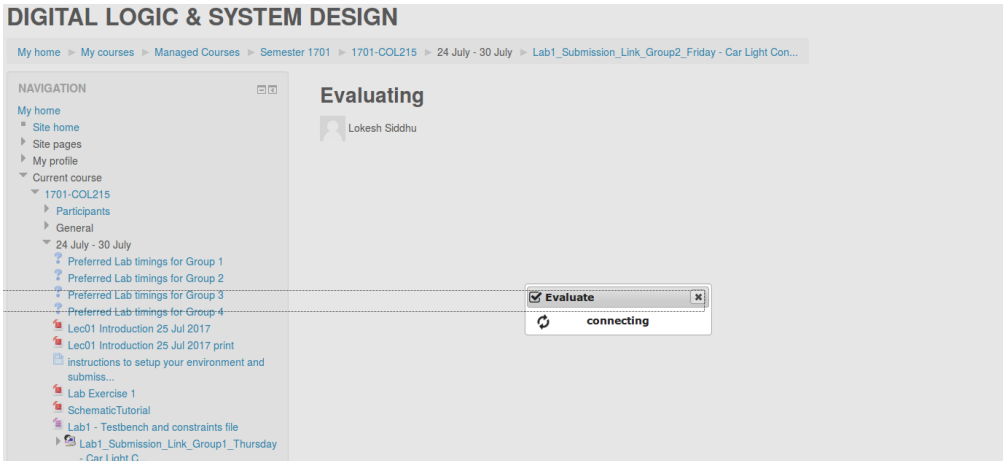
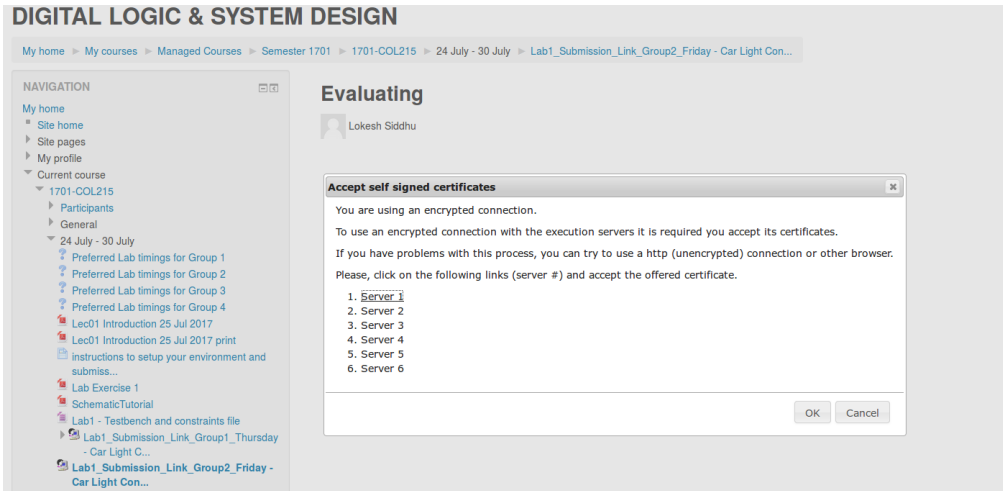
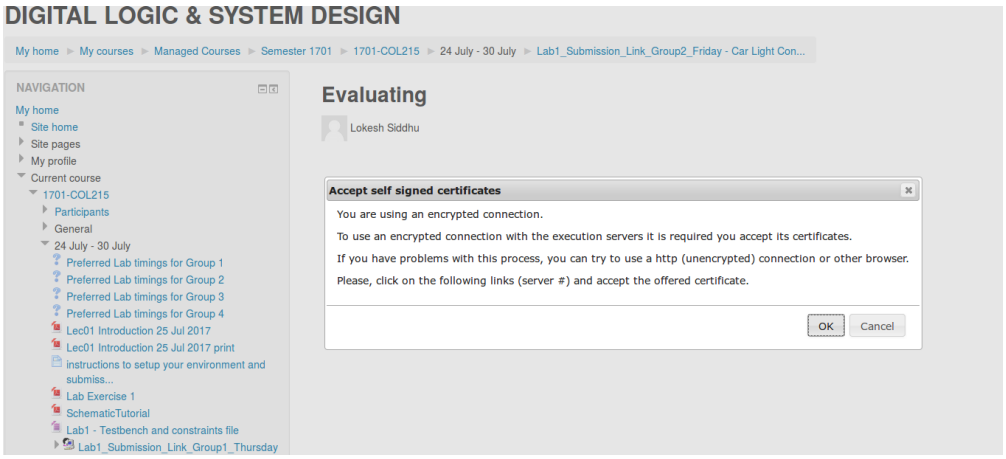
6. Automatic evaluation will start.




7. Accept certificates for all the servers.




8. After accepting all certificates, please click OK.




9. If no progress bar is shown, please press F5 button or re-submit the assignment.
10. Moodle execution server should start evaluating your assignment (In case it does not, re-submit.).

    Finally you would see the grade and the assessment report. Make sure you see your grade and go through the assessment report to understand the errors

Description Submission Edit Submission view

## Grade

Reviewed on Wednesday, 26 July 2017, 8:51 PM by Automatic grade
**Grade** 100 / 100
**Assessment report**

```
****** Vivado v2016.4 (64-bit)
**** SW Build 1733598 on Wed Dec 14 22:35:42 MST 2016
**** IP Build 1731160 on Wed Dec 14 23:47:21 MST 2016
** Copyright 1986-2016 Xilinx, Inc. All Rights Reserved.

source lab1_car_light.tcl
# create_project lab1_car_light ./vivado_tcl/lab1_car_light -part xc7a35tcpg236-1
# import_files -norecurse {./lab1_car_light.vhf}
# import_files -norecurse {./lab1_car_light_test.vhd}
# set_property top lab1_car_light_tb [get_fileset sim_1]
# launch_simulation
INFO: [SIM-utils-51] Simulation object is 'sim_1'
INFO: [USF-XSim-37] Inspecting design source files for 'lab1_car_light_tb' in fileset 'sim_1'...
INFO: [USF-XSim-97] Finding global include files...
INFO: [USF-XSim-98] Fetching design files from 'sim_1'...
INFO: [USF-XSim-2] XSim::Compile design
INFO: [USF-XSim-61] Executing 'COMPILE and ANALYZE' step in '/home/p16072/vivado_tcl/lab1_car_light/lab1_car_light.sim/sim_1/behav'
xvhdl -m64 --relax -prj lab1_car_light_tb_vhdl.prj
INFO: [VRFC 10-163] Analyzing VHDL file "/home/p16072/vivado_tcl/lab1_car_light/lab1_car_light.srcs/sources_1/imports/p16072/lab1_car_light.vhf" into library xil_defaultlib
INFO: [VRFC 10-307] analyzing entity lab1_car_light
INFO: [VRFC 10-163] Analyzing VHDL file "/home/p16072/vivado_tcl/lab1_car_light/lab1_car_light.srcs/sources_1/imports/p16072/lab1_car_light_test.vhd" into library xil_defaultlib
INFO: [VRFC 10-307] analyzing entity lab1_car_light_tb
INFO: [USF-XSim-69] 'compile' step finished in '0' seconds
INFO: [USF-XSim-3] XSim::Elaborate design
INFO: [USF-XSim-61] Executing 'ELABORATE' step in '/home/p16072/vivado_tcl/lab1_car_light/lab1_car_light.sim/sim_1/behav'
Vivado Simulator 2016.4
Copyright 1986-1999, 2001-2016 Xilinx, Inc. All Rights Reserved.
Running: /jail/opt/Xilinx1/Vivado/2016.4/bin/unwrapped/lnx64.o/xelab -wto 8cb2c37e82934103b404b12d0d5e329d --debug typical --relax --mt 8 -L xil_defaultlib -L secureip --snapshot
lab1_car_light_tb_behav xil_defaultlib.lab1_car_light_tb -log elaborate.log
Using 8 slave threads.
Starting static elaboration
```

Last modified: Friday, 28 July 2017, 5:24 PM

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Moodle Docs for this page

You are logged in as Rajesh Kedia (Log out)
1701-COL215