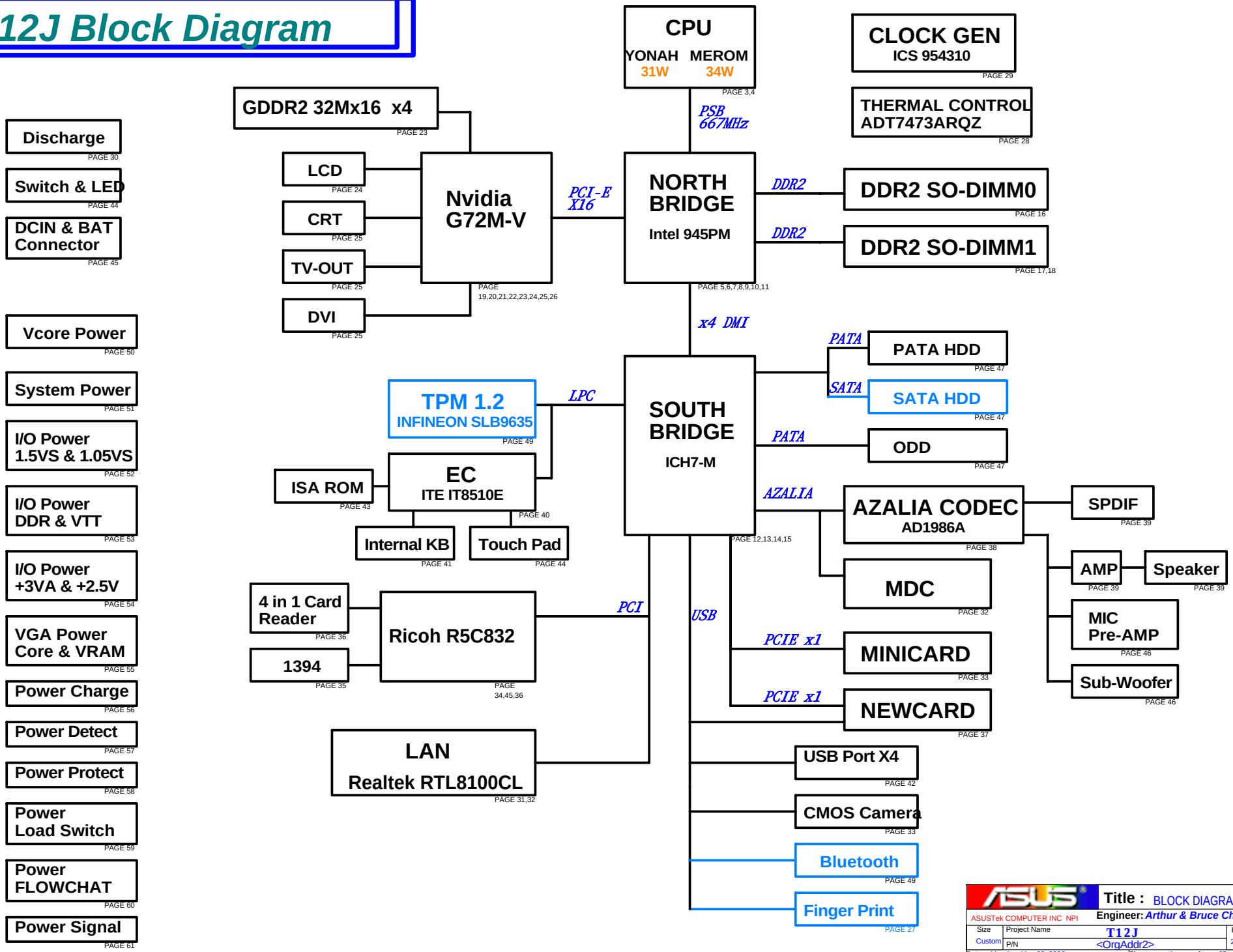
T12J Block Diagram



ASUSTek COMPUTER INC NPI	Title : BLOCK DIAGRAM		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 1 of 65		

EC_ITE8511 GPIO List

Pin	Pin Name	Signal Name	Type	Active
32	PWM0/GPA0	NC		GPO
33	PWM1/GPA1	FAN_PWM	O	High
36	PWM2/GPA2	NC		GPO
37	PWM3/GPA3	NC		GPO
38	PWM4/GPA4	CHG_LED_UP#	O	Low
39	PWM5/GPA5	PWR_LED_UP#	O	Low
40	PWM6/GPA6	BATSEL_3S#	O	Low
43	PWM7/GPA7	LCD_BACKOFF#	O	Low
153	RXD/GPB0	NUM_LED	O	High
154	TXD/GPB1	CAP_LED	O	High
162	GPB2	SCRL_LED	O	High
163	SMCLK0/GPB3	SMB0_CLK	I/0	
164	SMDAT0GPB4	SMB0_DAT	I/0	
5	GA20/GPB5	A20GATE	O	High
6	KBRST#/GPB6	RC_IN#	O	Low
165	GPB7	THRO_CPU	O	High
47	CLKOUT/GPC0	NC		GPO
169	SMCLK1/GPC1	SMB1_CLK	I/0	
170	SMDAT1/GPC2	SMB1_DAT	I/0	
171	GPC3	NC		GPO
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	Low
175	GPC5	OP_SD#	O	Low
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	Low
1	CK32KOUT/GPC7	NC	O	GPO
26	RI1#/WUI0/GPD0	PM_SUSB#	I	Low
29	RI2#/WUI1/GPD1	PM_SUSC#	I	Low
30	LPCRST#/WUI4/GPD2	BUF_PLT_RST#	I	Low
31	ECSCI#/GPD3	EXT_SCI#	O	Low
41	GPD4	NC		GPO
42	GINT/GPD5	NC		GPO
62	TACH0/GPD6	FAN_TACH	I	High
63	TACH1/GPD7	NC	O	GPO
87	ADC4/GPE0	WLAN_SW#	I	Low
88	ADC5/GPE1	NC	I	
89	ADC6/GPE2	MARATHON#	I	Low
90	ADC7/GPE3	DISTP_SW#	I	Low
2	PWRSW/GPE4	PWR_SW#	I	Low
44	WUI5/GPE5	NC		
24	LPCPD#/WUI6/GPE6	LID_EC#	I	Low
25	CLKRUN#/WUI7/GPE7	WLAN_V_ON#	PU	GPO
110	PS2CLK0/GPF0	/	PU	
111	PS2DAT0/GPF1	/	PU	
114	PS2CLK1/GPF2	/	PU	
115	PS2DAT1/GPF3	/	PU	
116	PS2CLK2/GPF4	TP_CLK		
117	PS2DAT2/GPF5	TP_DAT		
118	PS2CLK3/GPF6	PWRLMT#	I	Low
119	PS2DAT3/GPF7	/	PU	
113	FA16/GPG0	FA16		
112	FA17/GPG1	FA17		
104	FA18/GPG2	FA18		
103	FA19/GPG3	NC		
3	FA20/GPG4	THRM_ALERT#	I	
4	FA21/GPG5	NC		
27	LPC80HL/GPG6	PMTHERM#	O	
28	LPC80LL/GPG7	AC_APR_UC#	I	

EC_ITE8511 GPIO List

Pin	Pin Name	Signal Name	Type	Active
48	GPH0	VSUS_ON	O	High
54	GPH1	VSUS_GD#	I	Low
55	GPH2	CPUPWR_GD#	I	Low
69	GPH3	PM_PWRBTN#	O	Low
70	GPH4	SUSC#	O	Low
75	GPH5	SUSB#	O	Low
76	GPH6	CPU_VRON	O	High
105	GPH7	PM_RSMRST#	O	Low
148	GPI0	ICH7_PWROK	O	High
149	GPI1	NC	O	GPO
152	GPI2	NC		GPO
155	GPI3	CHG_EN#	O	Low
156	GPI4	PRECHG	O	High
168	GPI5	BAT_LL#	O	Low
174	GPI6	BAT_LEARN	O	High
148	GPL0	WLAN_ON#	I	Low
149	GPL1	BT_ON#	I	Low
152	GPL2	RF_OFF_SW#	I	Low
155	GPL3	RF_LED_ON	I	High
156	GPL4	NC		GPO
168	GPL5	NC		GPO
174	GPL6	NC		GPO

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Active
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	
C8	GPIO01/REQ5#	PCI_REQ#5	I	
G8	GPIO02/PIRQE#	PCI_INTE#	I	
F7	GPIO03/PIRQF#	PCI_INTF#	I	
F8	GPIO04/PIRQG#	PCI_INTG#	I	
G7	GPIO05/PIRQH#	PCI_INTH#	I	
AC21	GPIO06	BTLED_ON	O	
AC18	GPIO07	NC	I	
E21	GPIO08	EXTSMI#	I	
E20	GPIO09	SATA_DET#0	I	
A20	GPIO10	NC	O	
B23	SMBALERT#/GPIO11	SMB_ALERT#	PU	
F19	GPIO12	KBC_SCI#	I	
E19	GPIO13	NC	O	
R4	GPIO14	NC	O	
E22	GPIO15	WLAN_LED#	O	
AC22	GPIO16	PM_DPRSLPVR	O	
D8	GPIO17/GNT5#	PCI_GNT#5	O	
AC20	GPIO18/STP_PCI#	STP_PCI#	O	
AH18	GPIO19/SATA1GP	NC	PU	
AF21	GPIO20/STP_CPU#	STP_CPU#	O	
AE19	GPIO21/SATA0GP	NC	PU	
A13	GPIO22/REQ4#	PCI_REQ#4	I	
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O	
R3	GPIO24	P4G_LED#	O	
D20	GPIO25	NC	O	
A21	GPIO26/EL_RSVD	BT_DET#	I	
B21	GPIO27/EL_STATE0	NC	I	
E23	GPIO28/EL_STATE1	NC	I	
C3	GPIO29/OC#5	USB_OC#5	I	
A2	GPIO30/OC#6	NEWCARD_OC#	I	
B3	GPIO31/OC#7	USB_OC#7	I	
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	
AC19	GPIO33/AZ_DOCK_EN#	NC	O	
U2	GPIO34/AZ_DOCK_RST#	NC	O	
AD21	GPIO35	NC	O	
AH19	GPIO36/SATA2GP	NC	O	
AE19	GPIO37/SATA3GP	PCB_ID0	I	
AD20	GPIO38	PCB_ID1	I	
AE20	GPIO39	PCB_ID2	I	
A14	GNT4#/GPIO48	PCI_GNT#4	O	
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	C
1394	AD17	0	B
LAN	AD23		

PCIE Device	Bus		
RTL8111B	PE(T/R)(p/n)1		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(ADT7473)	01011100x (5C)
VGA Thermal Sensor(ADT7473)	0100000x (40)

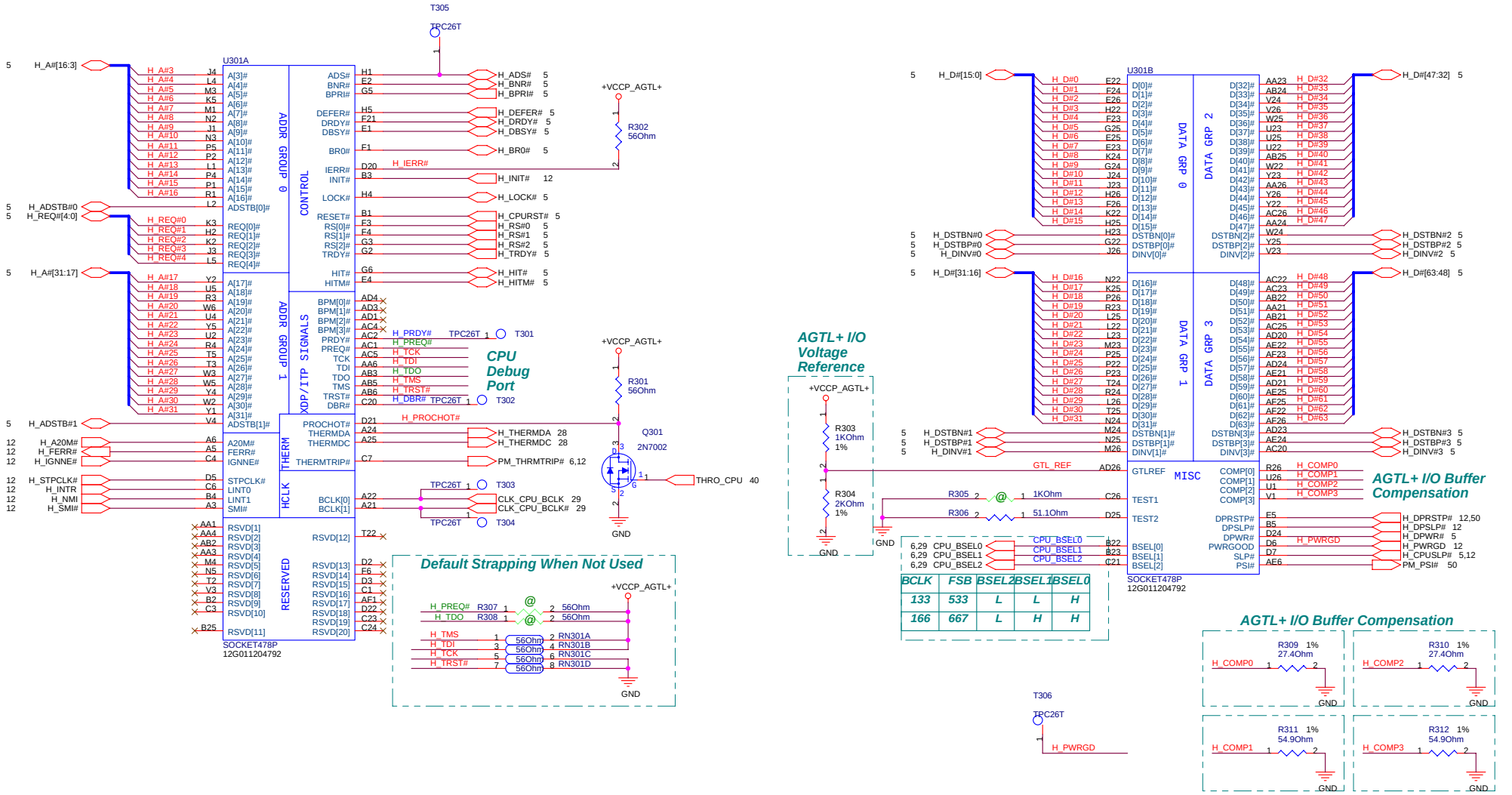
ASUSTek COMPUTER INC NPI

Title : GPIO SETTING

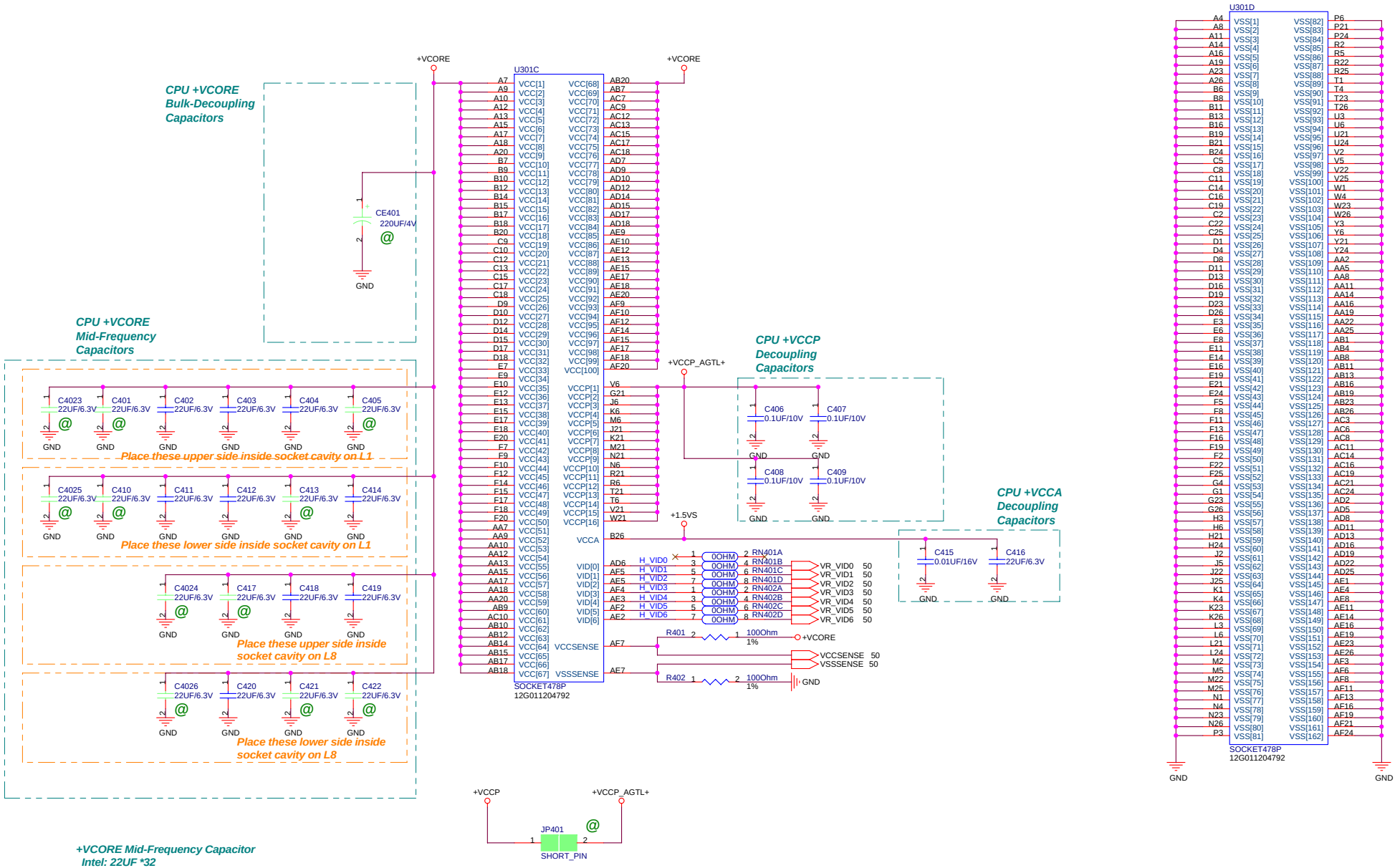
Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

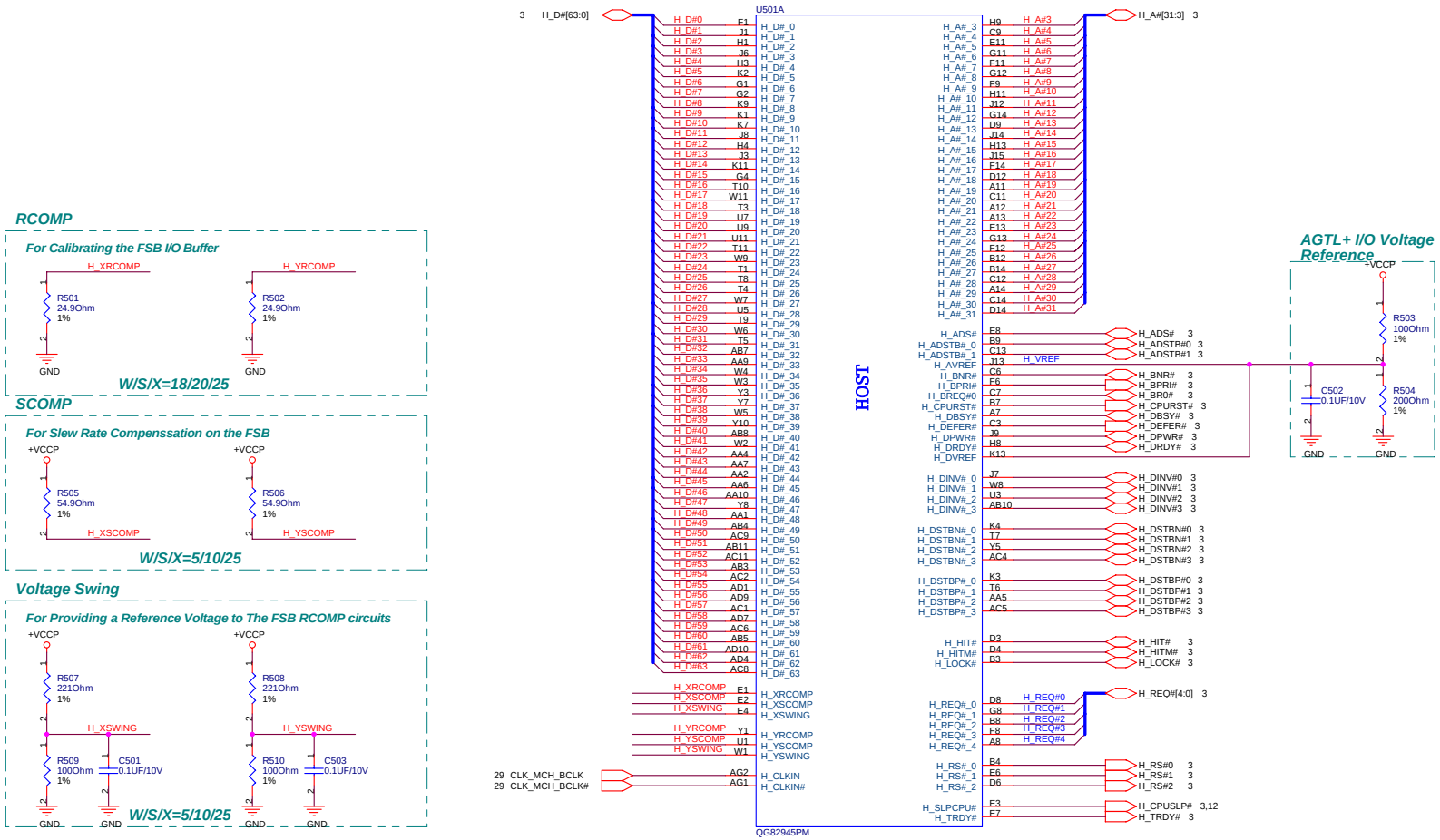
Date: Monday, May 29, 2006 Sheet 2 of 65



ASUSTek COMPUTER INC NPI	Title : CPU-YONAH(HOST)			
	Engineer: Arthur & Bruce Chen			
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>		Rev: 1.2
Date: Monday, May 29, 2006	Sheet 3 of 65			



ASUSTek COMPUTER INC NPI	Title : CPU_YONAH(PWR)	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 4 of 65	



ASUSTek COMPUTER INC NPI	Title : NB-945PM(HOST)		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 0.1
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 5 of 65		

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

MCH_CFG_5 — R601 1 — 2 1KOhm @ — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU
1 = Mobile CPU (D)

MCH_CFG_7 — R602 1 — 2 1KOhm @ — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)

MCH_CFG_15 — R603 1 — 2 1KOhm @ — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)

MCH_CFG_9 — R606 1 — 2 1KOhm @ — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R607 1 — 2 1KOhm @ — GND

CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)

MCH_CFG_10 — R610 1 — 2 1KOhm @ — GND

CFG18 : VCC Select

0 = 1.05V (D)
1 = 1.5V

+3VS — MCH_CFG_18 — R611 1 — 2 1KOhm @ — GND

CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)

MCH_CFG_11 — R613 1 — 2 1KOhm @ — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)
1 = Lanes Reversed

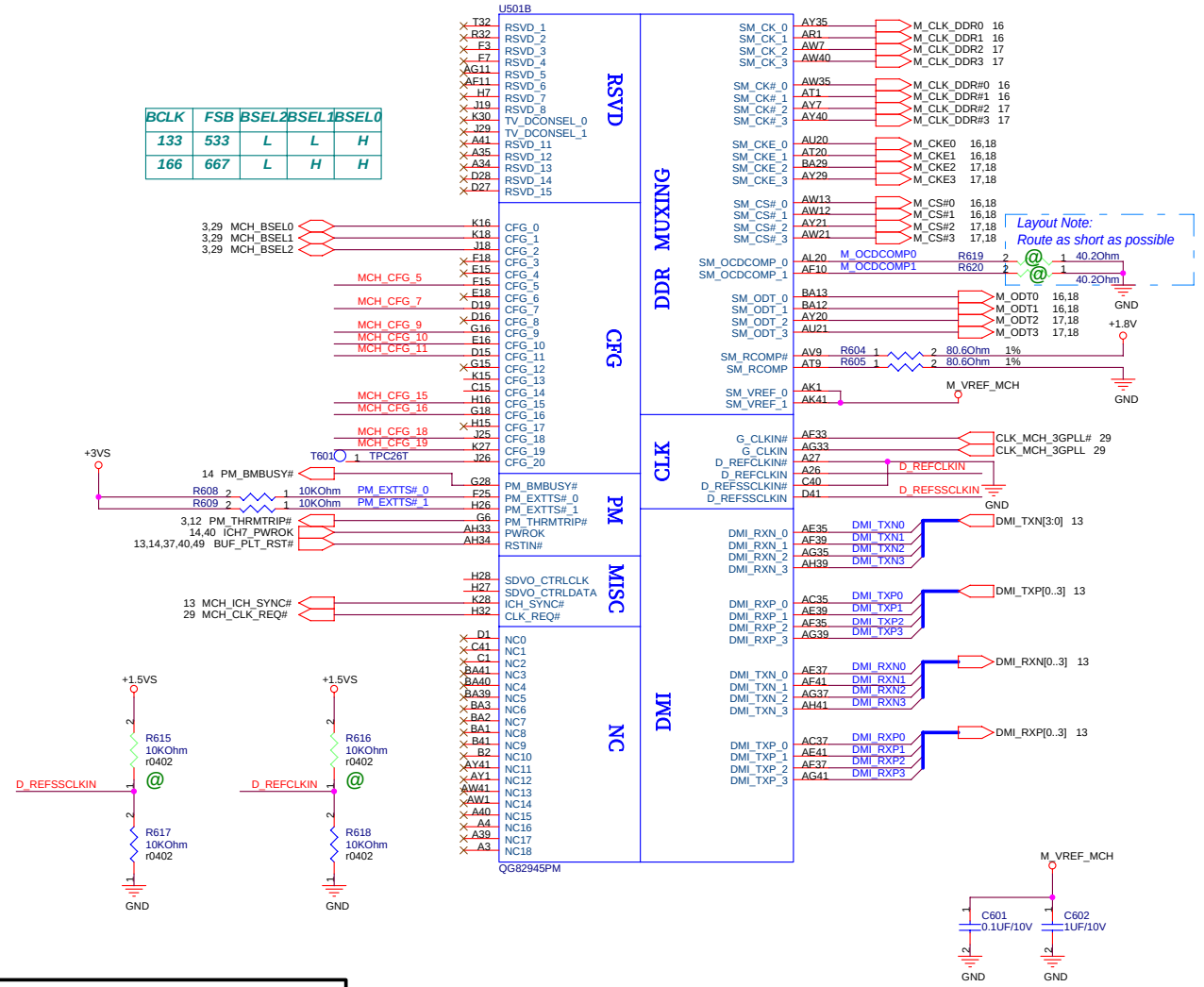
+3VS — MCH_CFG_19 — R614 1 — 2 1KOhm @ — GND

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

CFG All are sampled with respect to the leading edge of the GMCH PWROK

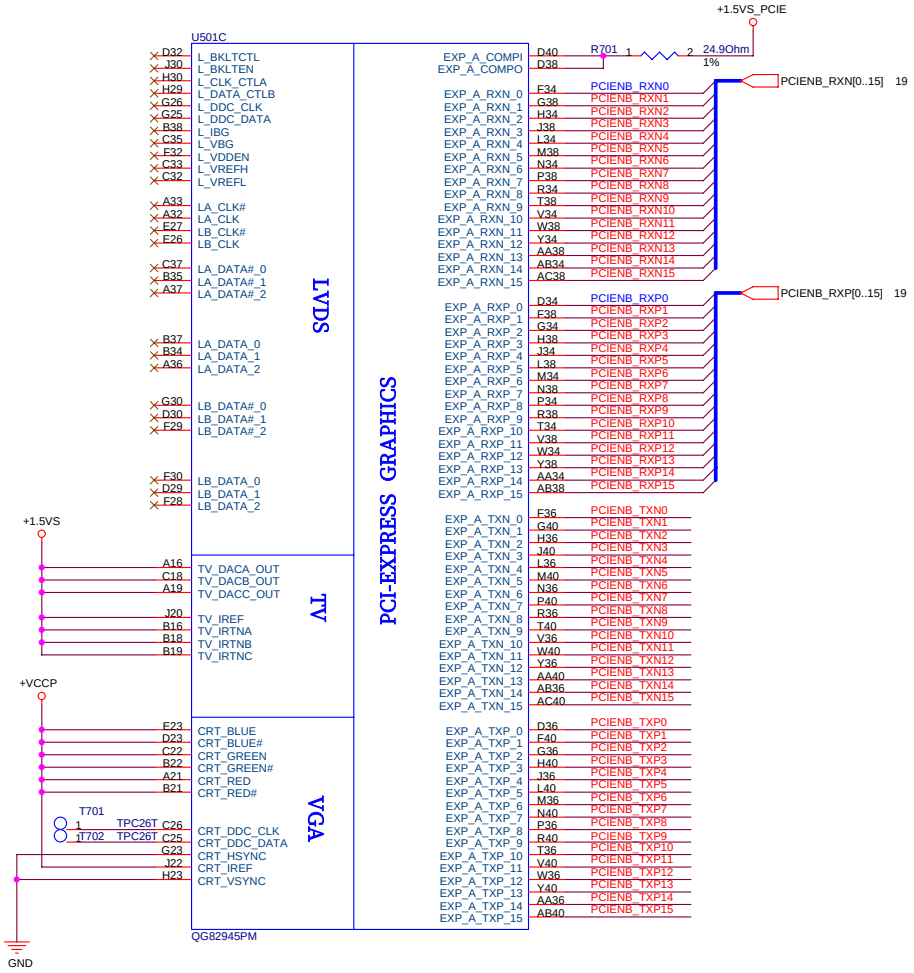
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4
6		(Default)
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

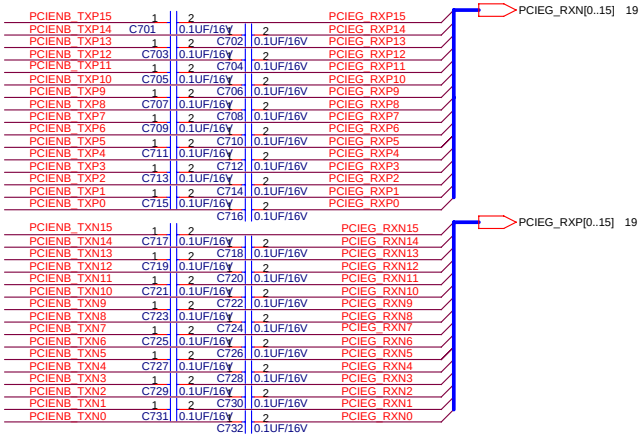
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



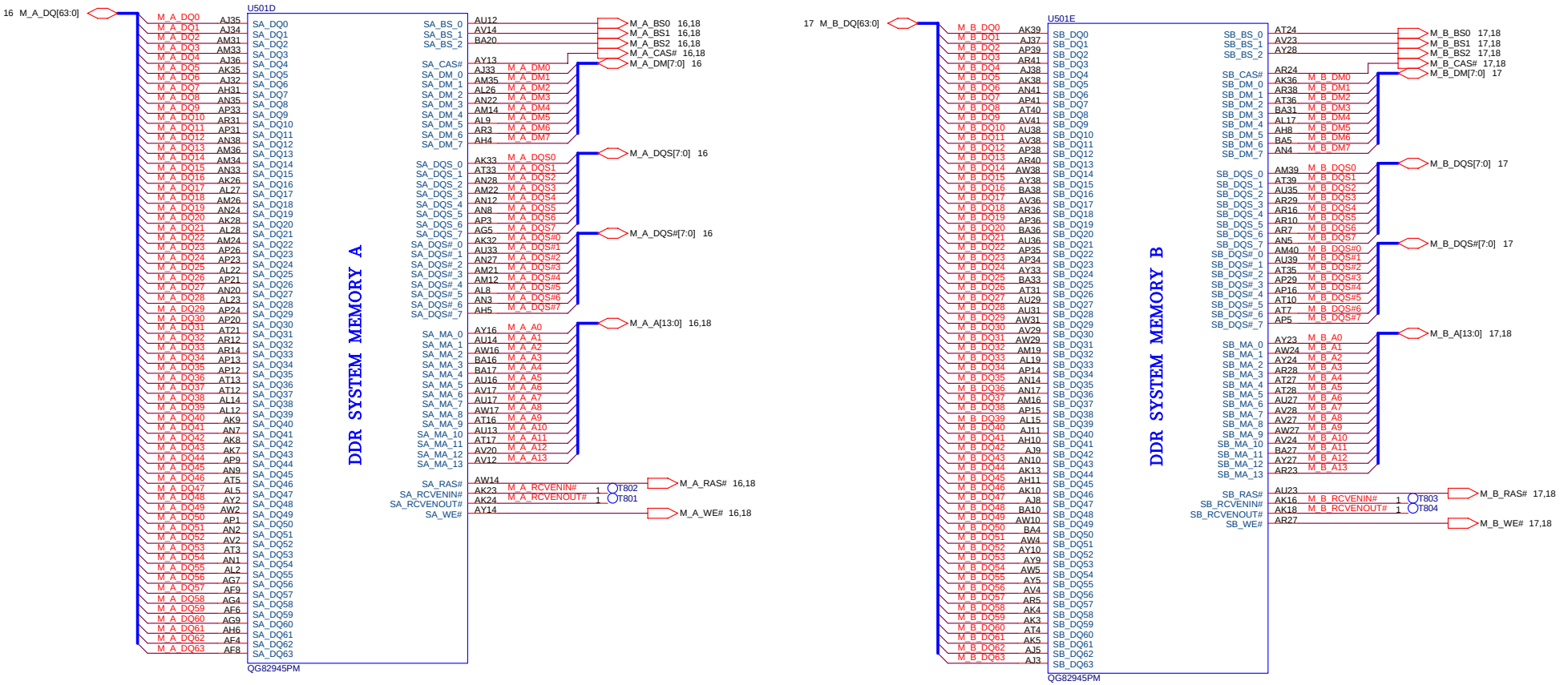
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

ASUSTek COMPUTER INC NPI	Title : NB-945PM(DMI & CFG)	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 6 of 65	

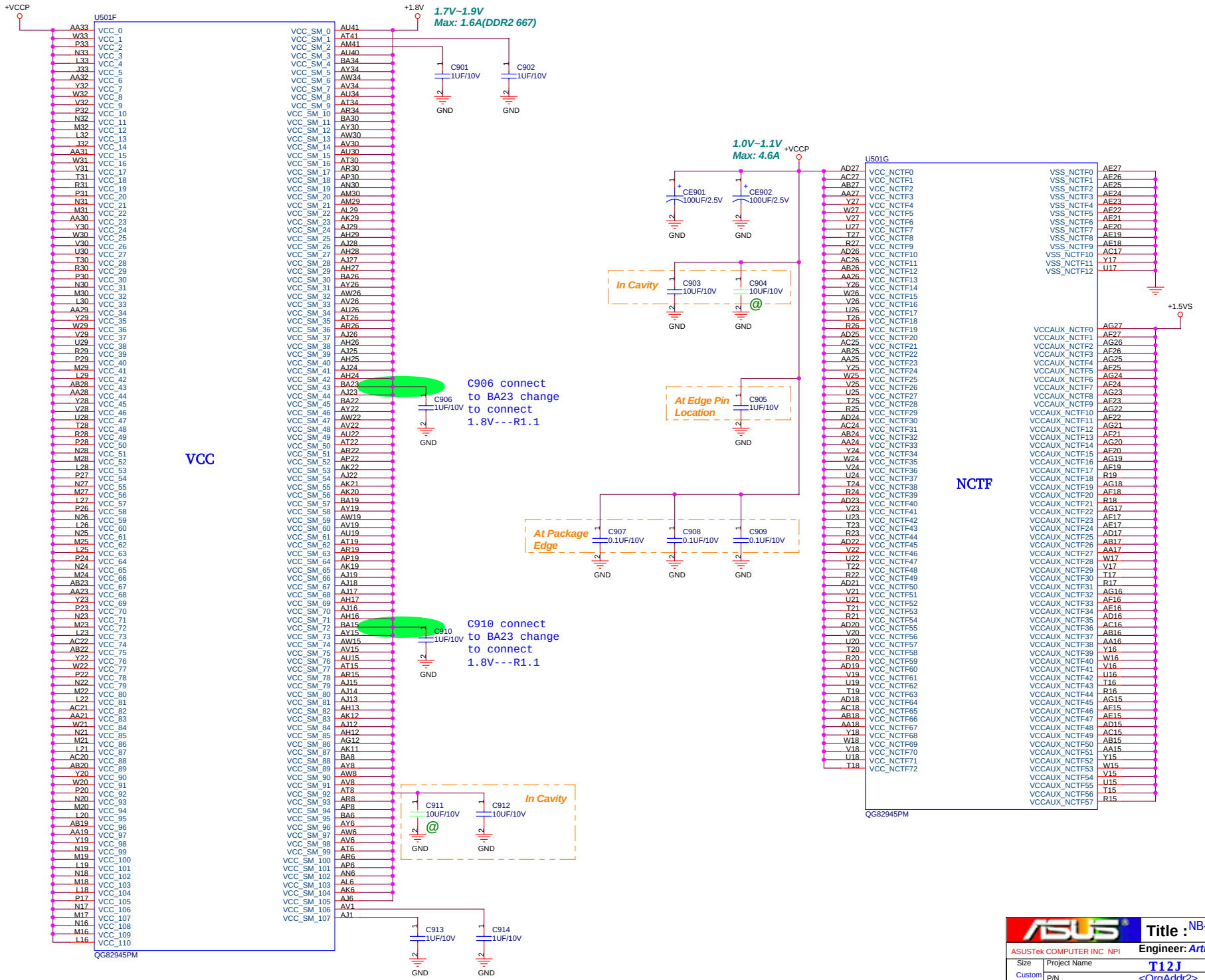




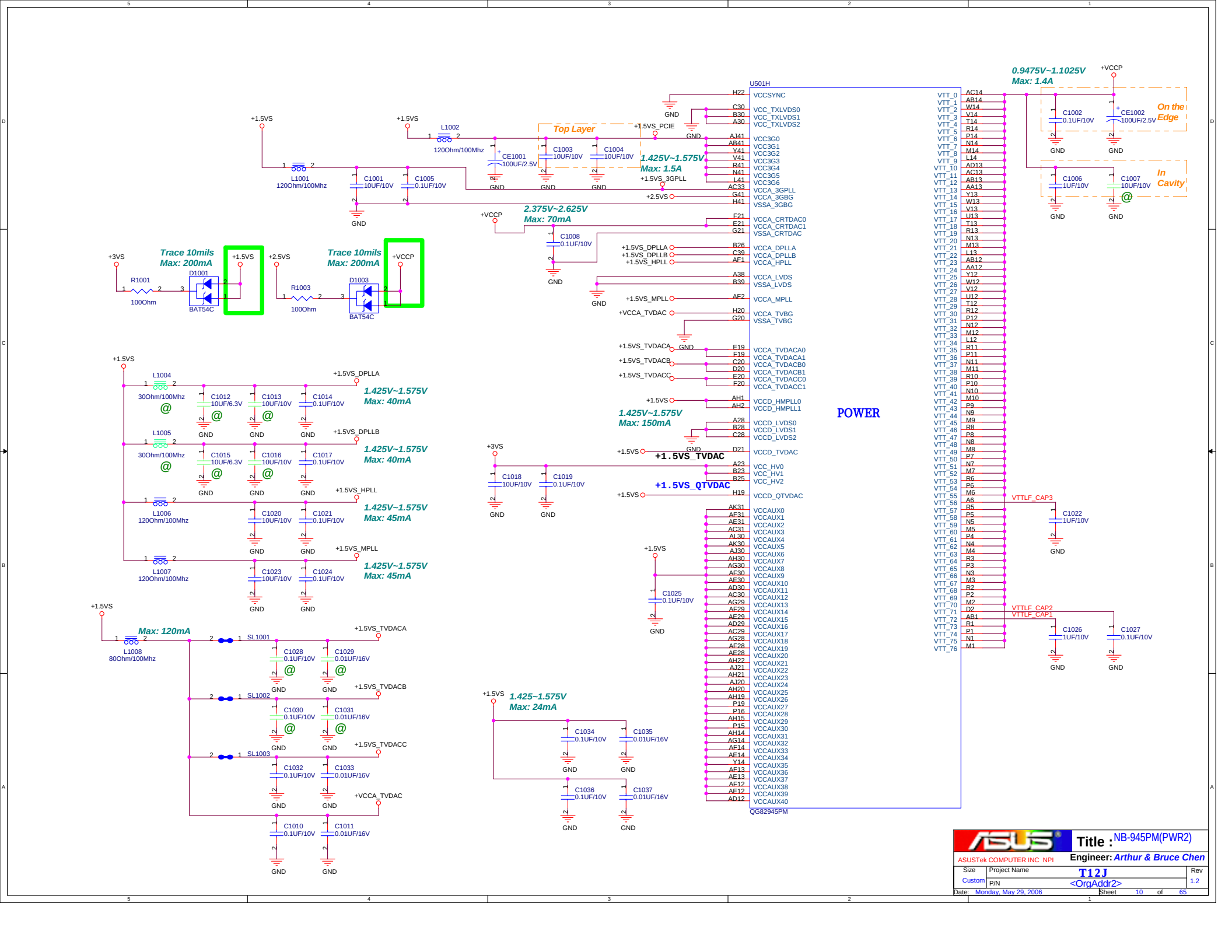
Title :	NB_945PM(GRAPHIC)
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen
Size: Custom	Project Name: T12J
P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 7 of 65

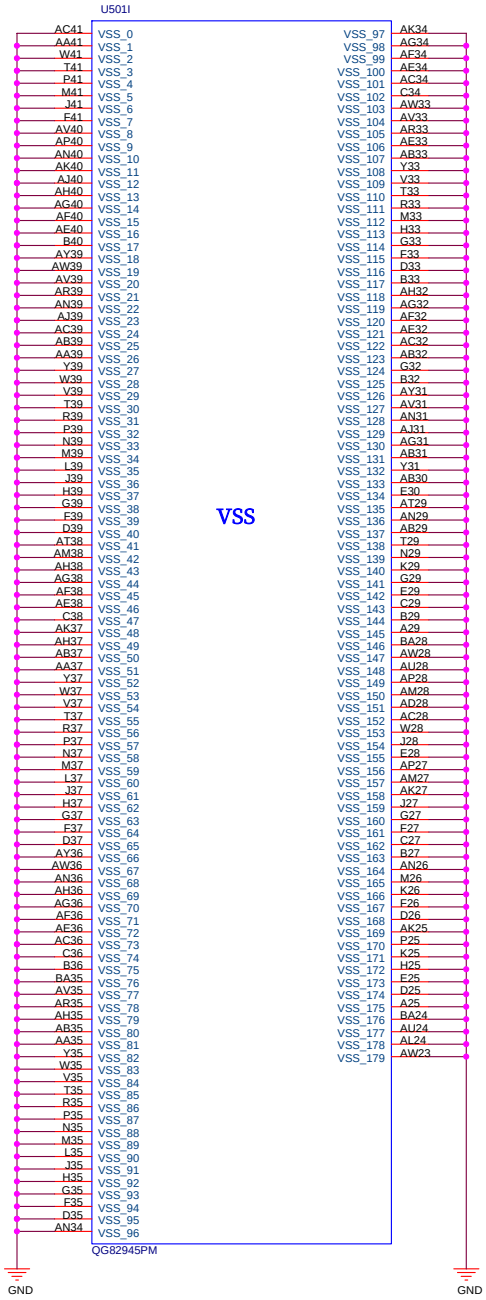


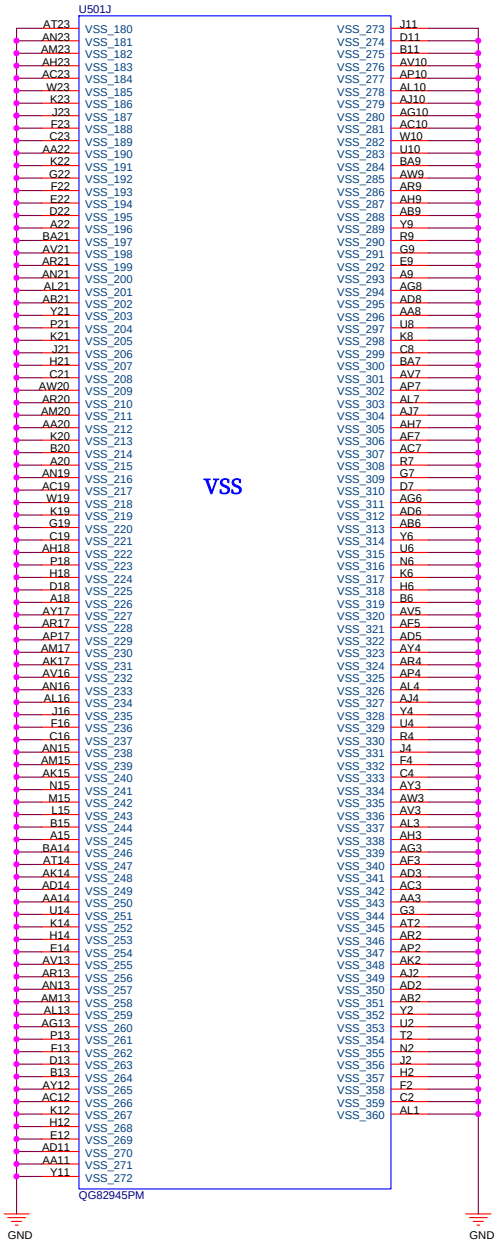
ASUSTek COMPUTER INC NPI	Title : NB-945PM(DDR2)	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 8 of 65	



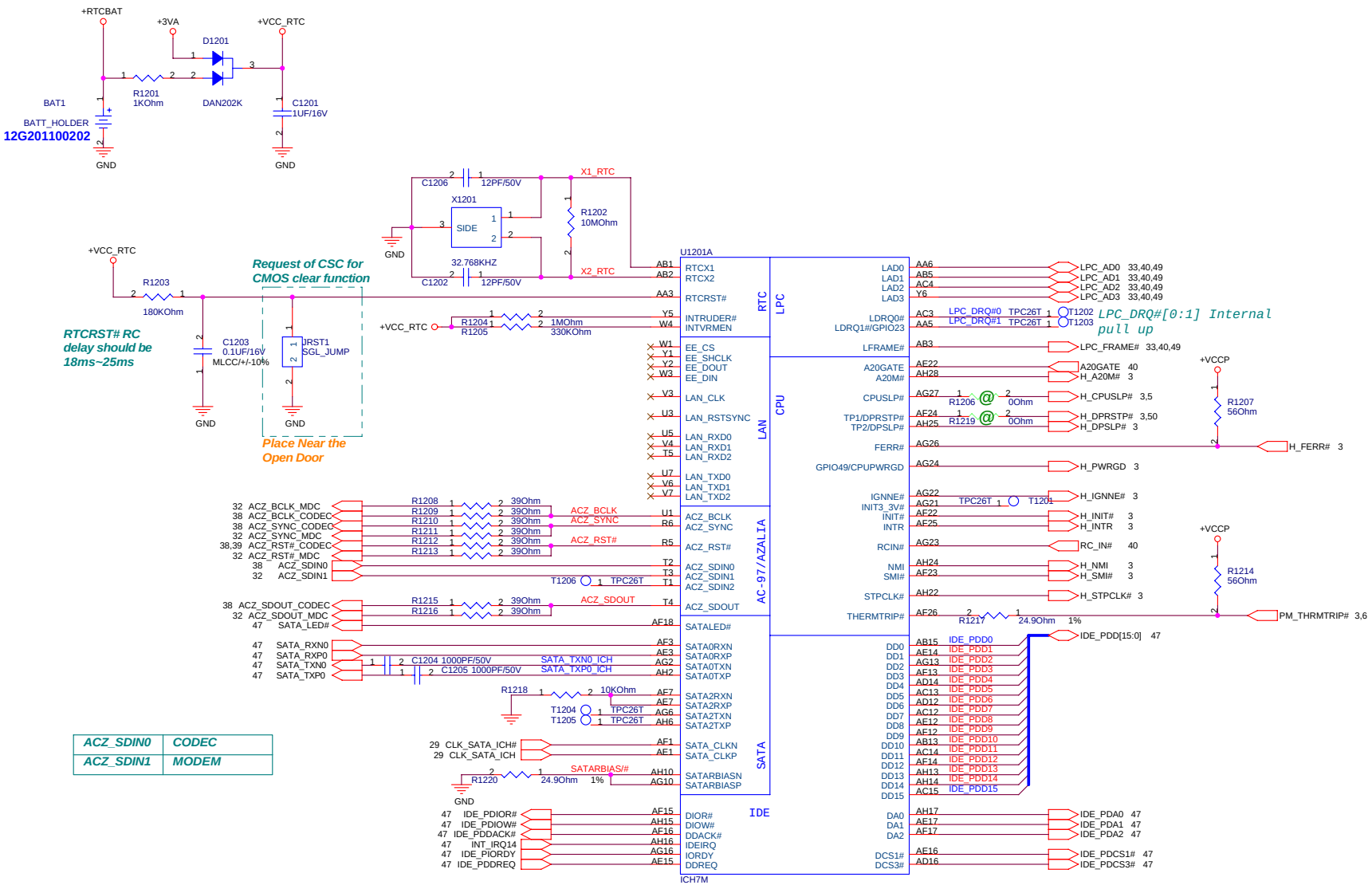
ASUSTek COMPUTER INC NPI	Title : NB-945PM(PWR)	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 9 of 65	


POWER
U501H
QG82945PM
Top Layer
On the Edge
In Cavity
Trace 10mils
Max: 200mA
Trace 10mils
Max: 200mA
0.9475V~1.1025V
Max: 1.4A
1.425V~1.575V
Max: 1.5A
2.375V~2.625V
Max: 70mA
1.425V~1.575V
Max: 150mA
+1.5VS_TVDAC
+1.5VS_QTVDAC
1.425~1.575V
Max: 24mA
Max: 120mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
Title : NB-945PM(PWR2)
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Project Name T12J
P/N <OrgAddr2>
Rev 1.2
Date: Monday, May 29, 2006
Sheet 10 of 65

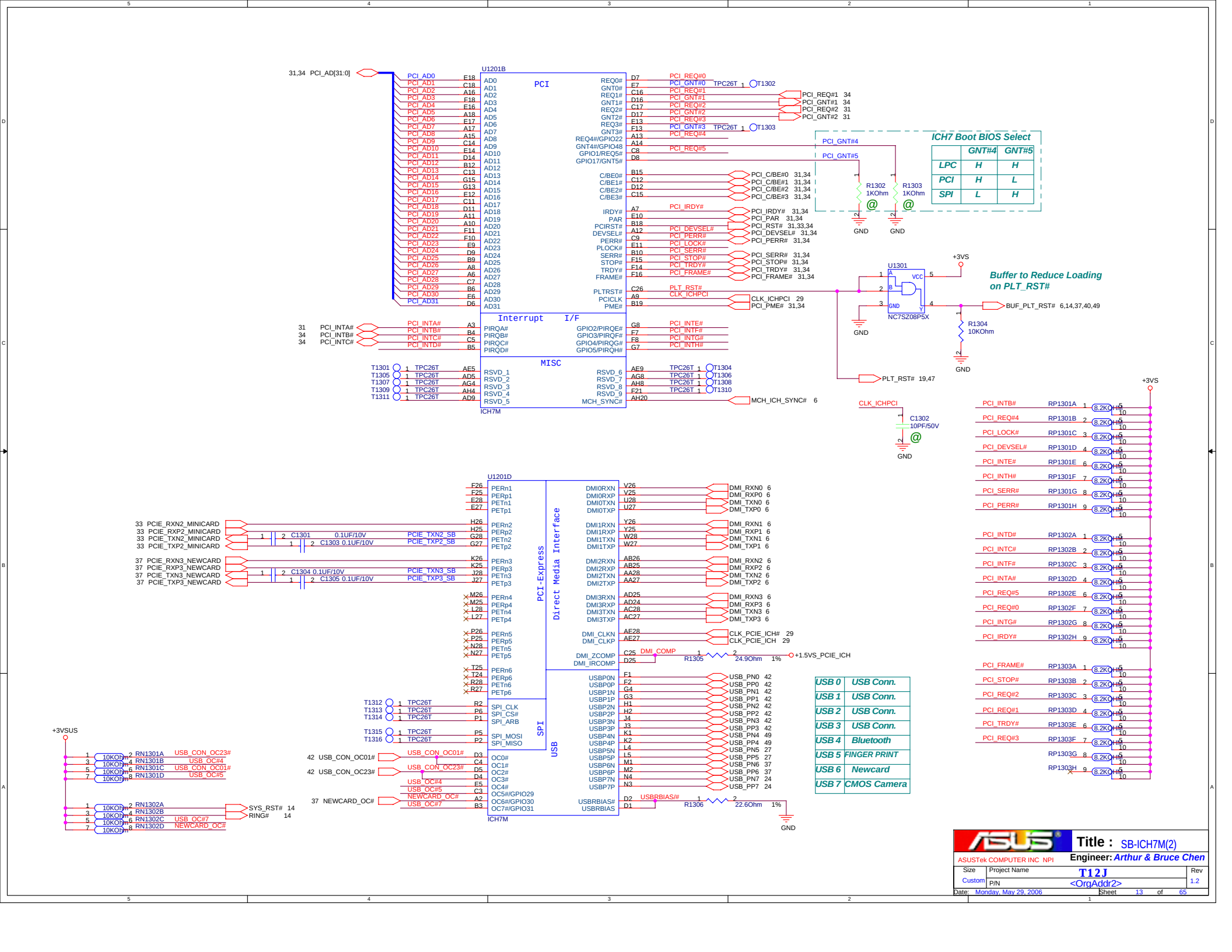


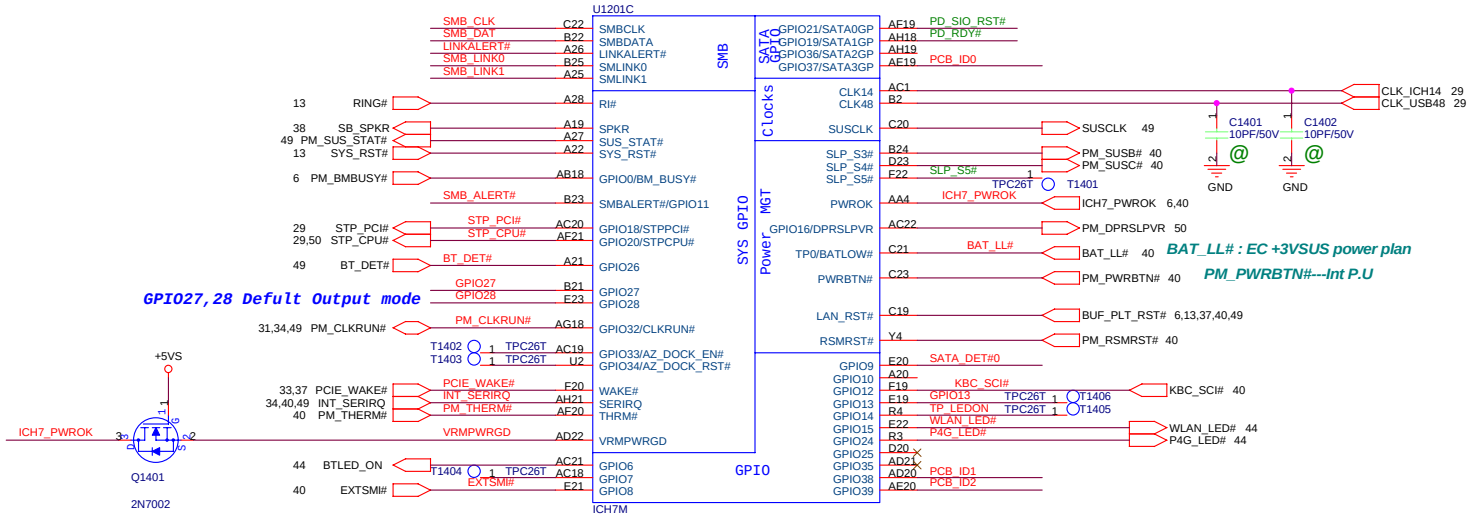


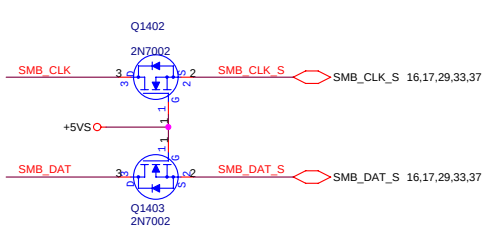
ASUSTek COMPUTER INC NPI	Title : NB-945PM(GND)	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 11 of 65	

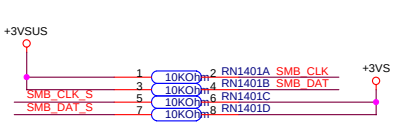


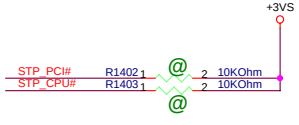
Title : SB-ICH7-M(1)	
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen
Size: Custom	Project Name: T12J
P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 12 of 65

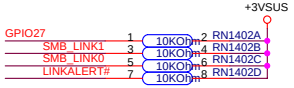

U1201B
PCI
Interrupt I/F
MISC
ICH7M
PCI_AD[31:0]
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_REQ#0
PCI_GNT#0
PCI_REQ#1
PCI_GNT#1
PCI_REQ#2
PCI_GNT#2
PCI_REQ#3
PCI_GNT#3
PCI_REQ#4
PCI_REQ#5
PCI_GNT#4
PCI_GNT#5
ICH7 Boot BIOS Select
LPC H H
PCI H L
SPI L H
R1302 1KOhm
R1303 1KOhm
PCI_C/BE#0
PCI_C/BE#1
PCI_C/BE#2
PCI_C/BE#3
PCI_IRDY#
PCI_PAR
PCI_RST#
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
PLT_RST#
CLK_ICHPCI
PCI_PME#
U1301
NC7SZ08P5X
Buffer to Reduce Loading on PLT_RST#
BUF_PLT_RST#
R1304 10KOhm
PLT_RST# 19,47
C1302 10PF/50V
MCH_ICH_SYNC#
U1201D
PCI-Express
Direct Media Interface
SPI
USB
PCIE_RXN2_MINICARD
PCIE_RXP2_MINICARD
PCIE_TXN2_MINICARD
PCIE_TXP2_MINICARD
C1301 0.1UF/10V
C1303 0.1UF/10V
PCIE_TXN2_SB
PCIE_TXP2_SB
PCIE_RXN3_NEWCARD
PCIE_RXP3_NEWCARD
PCIE_TXN3_NEWCARD
PCIE_TXP3_NEWCARD
C1304 0.1UF/10V
C1305 0.1UF/10V
PCIE_TXN3_SB
PCIE_TXP3_SB
DMI_COMP
R1305 24.9Ohm 1%
+1.5VS_PCIE_ICH
DMI_ZCOMP
DMI_IRCOMP
USBRBIAS#
R1306 22.6Ohm 1%
SPI_CLK
SPI_CS#
SPI_ARB
SPI_MOSI
SPI_MISO
USB_CON_OC01#
USB_CON_OC23#
USB_OC#4
USB_OC#5
NEWCARD_OC#
USB_OC#7
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 FINGER PRINT
USB 6 Newcard
USB 7 CMOS Camera
+3VSUS
RN1301A USB_CON_OC23#
RN1301B USB_OC#4
RN1301C USB_CON_OC01#
RN1301D USB_OC#5
RN1302A
RN1302B
RN1302C USB_OC#7
RN1302D NEWCARD_OC#
SYS_RST# 14
RING# 14
RP1301A PCI_INTB#
RP1301B PCI_REQ#4
RP1301C PCI_LOCK#
RP1301D PCI_DEVSEL#
RP1301E PCI_INTE#
RP1301F PCI_INTH#
RP1301G PCI_SERR#
RP1301H PCI_PERR#
RP1302A PCI_INTD#
RP1302B PCI_INTC#
RP1302C PCI_INTF#
RP1302D PCI_INTA#
RP1302E PCI_REQ#5
RP1302F PCI_REQ#0
RP1302G PCI_INTG#
RP1302H PCI_IRDY#
RP1303A PCI_FRAME#
RP1303B PCI_STOP#
RP1303C PCI_REQ#2
RP1303D PCI_REQ#1
RP1303E PCI_TRDY#
RP1303F PCI_REQ#3
RP1303G
RP1303H
8.2KOHM
Title : SB-ICH7M(2)
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Size Custom
Project Name T12J
P/N <OrgAddr2>
Rev 1.2
Date: Monday, May 29, 2006
Sheet 13 of 65

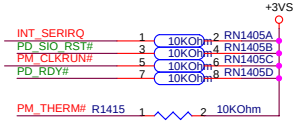


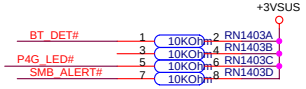


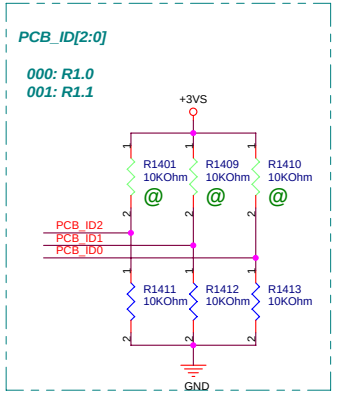


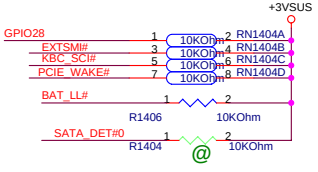


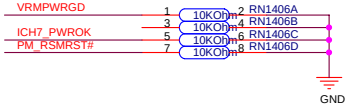












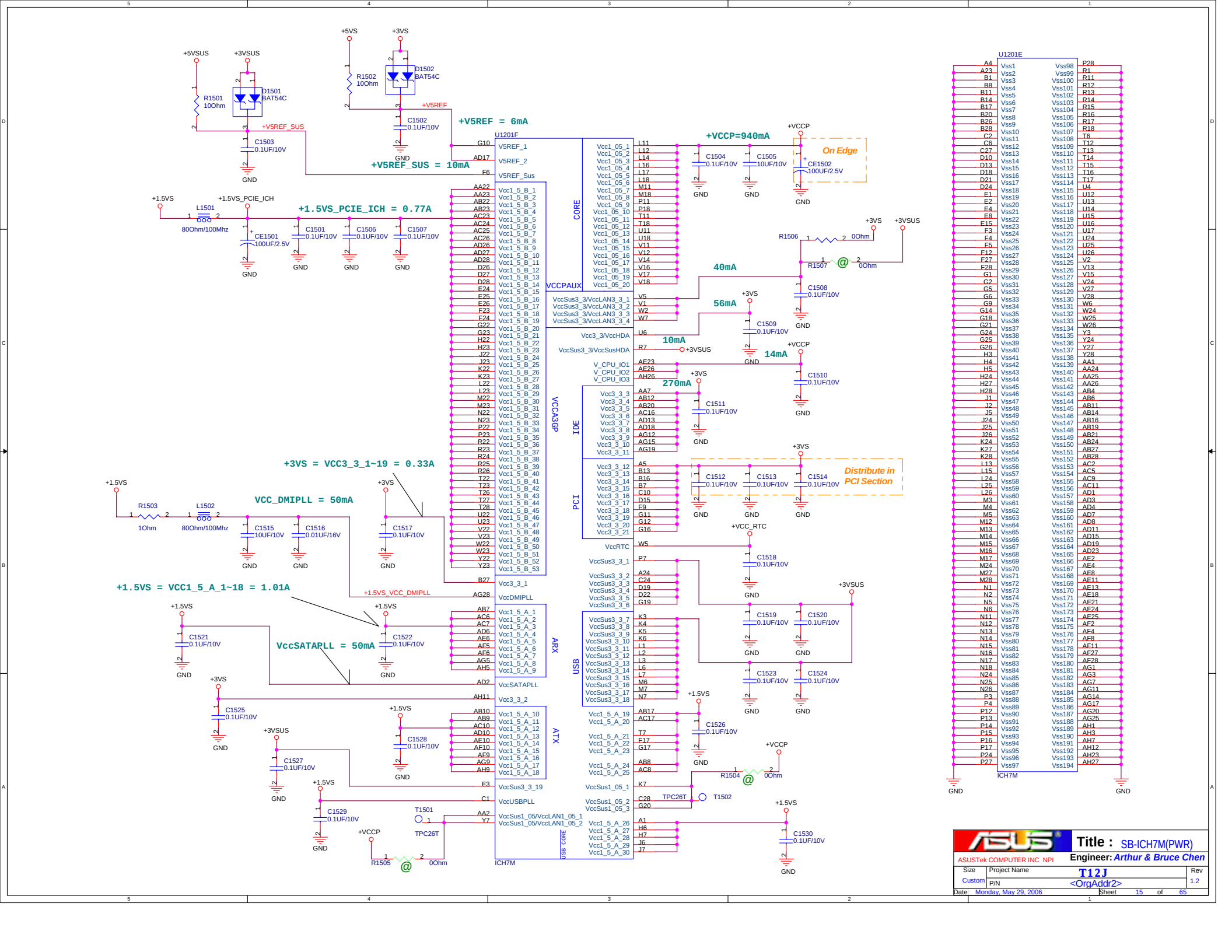
ASUSTek COMPUTER INC NPI

Title : SB-ICH7M(3)

Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 14 of 65


+5VSUS
+3VSUS
R1501
10Ohm
D1501
BAT54C
+5VS
+3VS
R1502
10Ohm
D1502
BAT54C
+V5REF
C1502
0.1UF/10V
+V5REF_SUS
C1503
0.1UF/10V
GND
+V5REF = 6mA
+V5REF_SUS = 10mA
U1201F
G10
V5REF_1
AD17
V5REF_2
F6
V5REF_Sus
+1.5VS
+1.5VS_PCIE_ICH
L1501
80Ohm/100Mhz
+1.5VS_PCIE_ICH = 0.77A
CE1501
100UF/2.5V
C1501
0.1UF/10V
C1506
0.1UF/10V
C1507
0.1UF/10V
AA22
AA23
AB22
AB23
AC23
AC24
AC25
AC26
AD26
AD27
AD28
D26
D27
D28
E24
E25
E26
F23
F24
G22
G23
H22
H23
J22
J23
K22
K23
L22
L23
M22
M23
N22
N23
P22
P23
R22
R23
R24
R25
R26
T22
T23
T26
T27
T28
U22
U23
V22
V23
W22
W23
Y22
Y23
Vcc1_5_B_1
Vcc1_5_B_2
Vcc1_5_B_3
Vcc1_5_B_4
Vcc1_5_B_5
Vcc1_5_B_6
Vcc1_5_B_7
Vcc1_5_B_8
Vcc1_5_B_9
Vcc1_5_B_10
Vcc1_5_B_11
Vcc1_5_B_12
Vcc1_5_B_13
Vcc1_5_B_14
Vcc1_5_B_15
Vcc1_5_B_16
Vcc1_5_B_17
Vcc1_5_B_18
Vcc1_5_B_19
Vcc1_5_B_20
Vcc1_5_B_21
Vcc1_5_B_22
Vcc1_5_B_23
Vcc1_5_B_24
Vcc1_5_B_25
Vcc1_5_B_26
Vcc1_5_B_27
Vcc1_5_B_28
Vcc1_5_B_29
Vcc1_5_B_30
Vcc1_5_B_31
Vcc1_5_B_32
Vcc1_5_B_33
Vcc1_5_B_34
Vcc1_5_B_35
Vcc1_5_B_36
Vcc1_5_B_37
Vcc1_5_B_38
Vcc1_5_B_39
Vcc1_5_B_40
Vcc1_5_B_41
Vcc1_5_B_42
Vcc1_5_B_43
Vcc1_5_B_44
Vcc1_5_B_45
Vcc1_5_B_46
Vcc1_5_B_47
Vcc1_5_B_48
Vcc1_5_B_49
Vcc1_5_B_50
Vcc1_5_B_51
Vcc1_5_B_52
Vcc1_5_B_53
CORE
VCCPAUX
VCCA3GP
IDE
PCI
USB
ARX
ATX
Vcc1_05_1
Vcc1_05_2
Vcc1_05_3
Vcc1_05_4
Vcc1_05_5
Vcc1_05_6
Vcc1_05_7
Vcc1_05_8
Vcc1_05_9
Vcc1_05_10
Vcc1_05_11
Vcc1_05_12
Vcc1_05_13
Vcc1_05_14
Vcc1_05_15
Vcc1_05_16
Vcc1_05_17
Vcc1_05_18
Vcc1_05_19
Vcc1_05_20
L11
L12
L14
L16
L17
L18
M11
M18
P11
P18
T11
T18
U11
U18
V11
V12
V14
V16
V17
V18
+VCCP=940mA
C1504
0.1UF/10V
C1505
10UF/10V
+VCCP
On Edge
CE1502
100UF/2.5V
VccSus3_3/VccLAN3_3_1
VccSus3_3/VccLAN3_3_2
VccSus3_3/VccLAN3_3_3
VccSus3_3/VccLAN3_3_4
V5
V1
W2
W7
40mA
56mA
C1508
0.1UF/10V
C1509
0.1UF/10V
Vcc3_3/VccHDA
U6
10mA
R7
+3VSUS
VccSus3_3/VccSusHDA
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
AE23
AE26
AH26
14mA
C1510
0.1UF/10V
270mA
C1511
0.1UF/10V
Vcc3_3_3
Vcc3_3_4
Vcc3_3_5
Vcc3_3_6
Vcc3_3_7
Vcc3_3_8
Vcc3_3_9
Vcc3_3_10
Vcc3_3_11
AA7
AB12
AB20
AC16
AD13
AD18
AG12
AG15
AG19
Vcc3_3_12
Vcc3_3_13
Vcc3_3_14
Vcc3_3_15
Vcc3_3_16
Vcc3_3_17
Vcc3_3_18
Vcc3_3_19
Vcc3_3_20
Vcc3_3_21
A5
B13
B16
B7
C10
D15
F9
G11
G12
G16
C1512
0.1UF/10V
C1513
0.1UF/10V
C1514
0.1UF/10V
Distribute in
PCI Section
+3VS = VCC3_3_1~19 = 0.33A
+1.5VS
R1503
1Ohm
L1502
80Ohm/100Mhz
VCC_DMIPLL = 50mA
C1515
10UF/10V
C1516
0.01UF/16V
C1517
0.1UF/10V
+1.5VS = VCC1_5_A_1~18 = 1.01A
+1.5VS_VCC_DMIPLL
B27
Vcc3_3_1
AG28
VccDMIPLL
VccRTC
W5
+VCC_RTC
C1518
0.1UF/10V
VccSus3_3_1
P7
VccSus3_3_2
VccSus3_3_3
VccSus3_3_4
VccSus3_3_5
VccSus3_3_6
A24
C24
D19
D22
G19
C1519
0.1UF/10V
C1520
0.1UF/10V
+3VSUS
VccSus3_3_7
VccSus3_3_8
VccSus3_3_9
VccSus3_3_10
VccSus3_3_11
VccSus3_3_12
VccSus3_3_13
VccSus3_3_14
VccSus3_3_15
VccSus3_3_16
VccSus3_3_17
VccSus3_3_18
K3
K4
K5
K6
L1
L3
L6
L7
M6
M7
N7
C1523
0.1UF/10V
C1524
0.1UF/10V
+1.5VS
C1521
0.1UF/10V
C1522
0.1UF/10V
VccSATAPLL = 50mA
AB7
AC6
AC7
AD6
AE6
AF5
AF6
AG5
AH5
Vcc1_5_A_1
Vcc1_5_A_2
Vcc1_5_A_3
Vcc1_5_A_4
Vcc1_5_A_5
Vcc1_5_A_6
Vcc1_5_A_7
Vcc1_5_A_8
Vcc1_5_A_9
AD2
VccSATAPLL
AH11
Vcc3_3_2
C1525
0.1UF/10V
+3VSUS
C1527
0.1UF/10V
+1.5VS
C1528
0.1UF/10V
AB10
AB9
AC10
AD10
AE10
AF10
AF9
AG9
AH9
Vcc1_5_A_10
Vcc1_5_A_11
Vcc1_5_A_12
Vcc1_5_A_13
Vcc1_5_A_14
Vcc1_5_A_15
Vcc1_5_A_16
Vcc1_5_A_17
Vcc1_5_A_18
E3
VccSus3_3_19
C1
VccUSBPLL
C1529
0.1UF/10V
T1501
TPC26T
+VCCP
R1505
@
0Ohm
AA2
Y7
VccSus1_05/VccLAN1_05_1
VccSus1_05/VccLAN1_05_2
USB_CORE
Vcc1_5_A_19
Vcc1_5_A_20
Vcc1_5_A_21
Vcc1_5_A_22
Vcc1_5_A_23
Vcc1_5_A_24
Vcc1_5_A_25
AB17
AC17
T7
F17
G17
AB8
AC8
K7
VccSus1_05_1
VccSus1_05_2
VccSus1_05_3
C28
G20
TPC26T
T1502
C1526
0.1UF/10V
+1.5VS
+VCCP
R1504
@
0Ohm
Vcc1_5_A_26
Vcc1_5_A_27
Vcc1_5_A_28
Vcc1_5_A_29
Vcc1_5_A_30
A1
H6
H7
J6
J7
C1530
0.1UF/10V
ICH7M
R1506
0Ohm
+3VS
+3VSUS
R1507
@
0Ohm
U1201E
Vss1
Vss2
Vss3
Vss4
Vss5
Vss6
Vss7
Vss8
Vss9
Vss10
Vss11
Vss12
Vss13
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Vss179
Vss180
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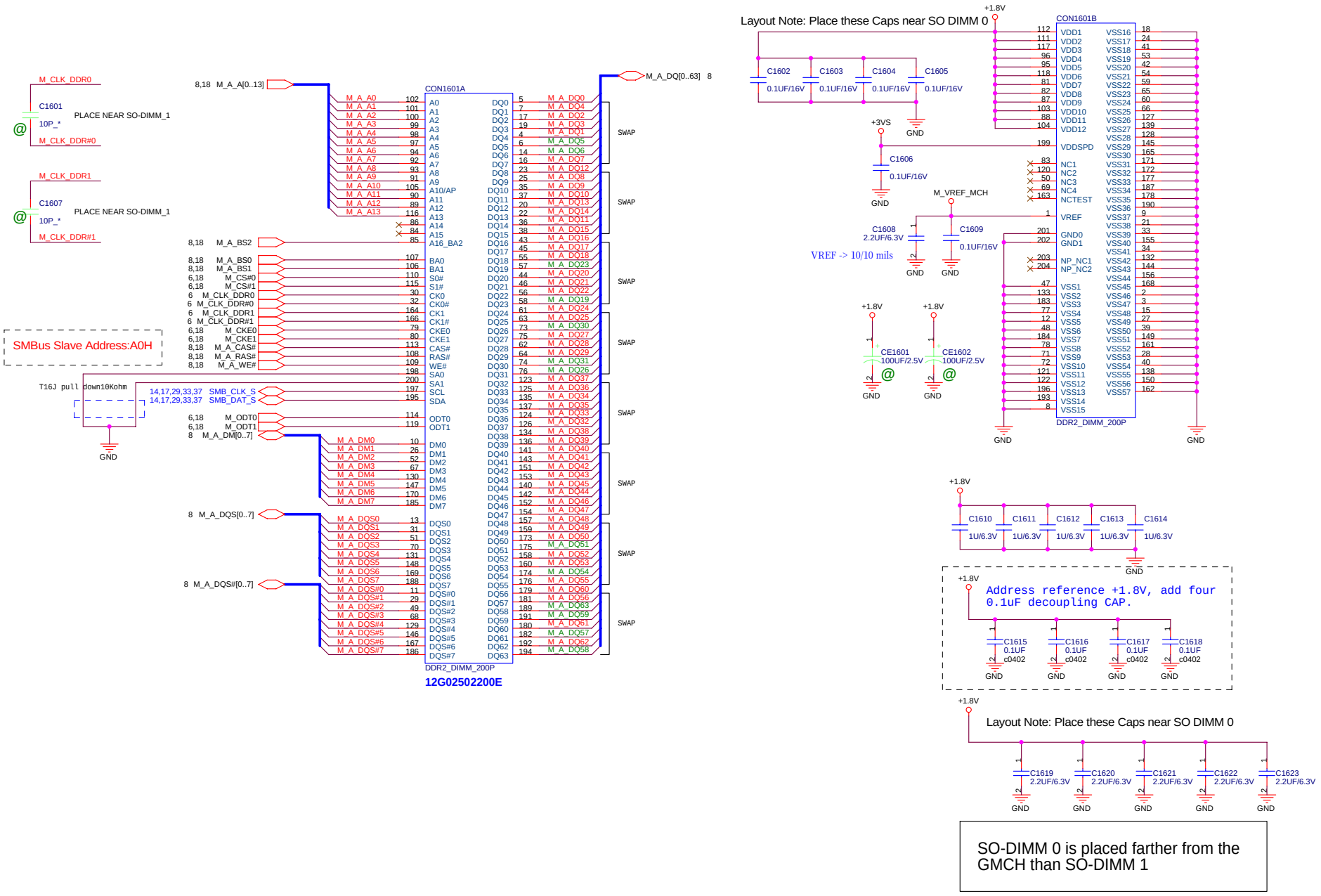
Vss182
Vss183
Vss184
Vss185
Vss186
Vss187
Vss188
Vss189
Vss190
Vss191
Vss192
Vss193
Vss194
P28
R1
R11
R12
R13
R14
R15
R16
R17
R18
T6
T12
T13
T14
T15
T16
T17
U4
U12
U13
U14
U15
U16
U17
U24
U25
U26
V2
V13
V15
V24
V27
V28
W6
W24
W25
W26
Y3
Y24
Y27
Y28
AA1
AA24
AA25
AA26
AB4
AB6
AB11
AB14
AB16
AB19
AB21
AB24
AB27
AB28
AC2
AC5
AC9
AC11
AD1
AD3
AD4
AD7
AD8
AD11
AD15
AD19
AD23
AE2
AE4
AE8
AE11
AE13
AE18
AE21
AE24
AE25
AF2
AF4
AF8
AE11
AF27
AF28
AG1
AG3
AG7
AG11
AG14
AG17
AG20
AG25
AH1
AH3
AH7
AH12
AH23
AH27
ICH7M
GND
Title : SB-ICH7M(PWR)
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Size
Custom
Project Name
T12J
Rev
1.2
P/N
<OrgAddr2>
Date: Monday, May 29, 2006
Sheet 15 of 65



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	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
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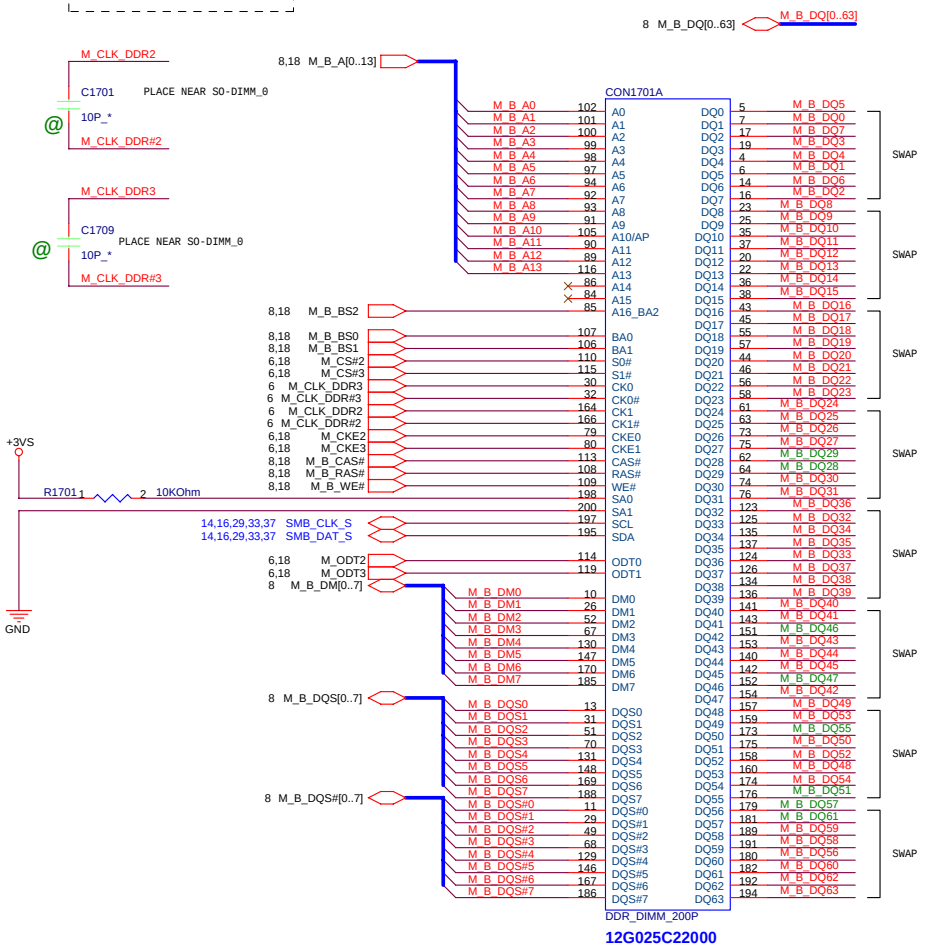
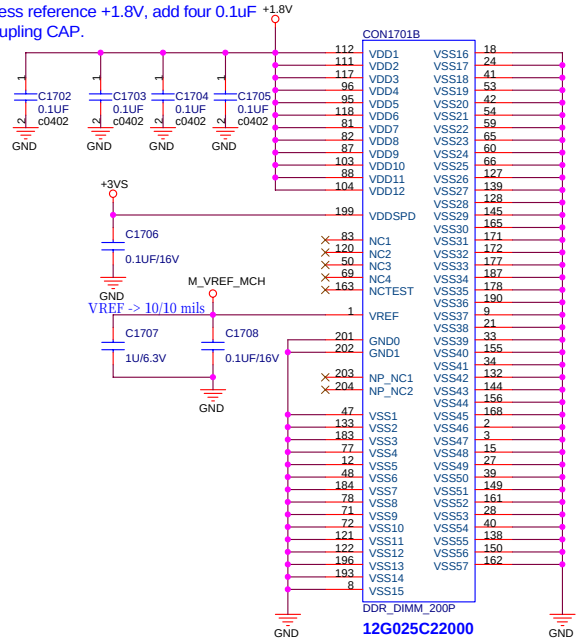
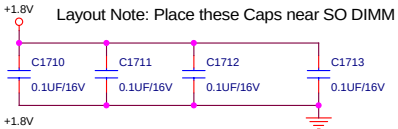
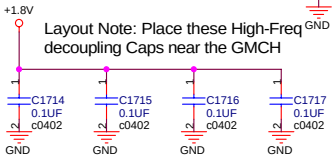
SMBus Slave Address:A4H

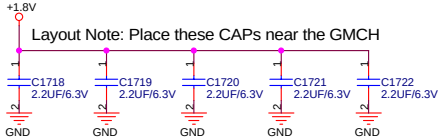


Address reference +1.8V, add four 0.1uF decoupling CAP.









ASUSTek COMPUTER INC NPI	Title : DDR2 SO-DIMM1	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
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ASUSTek COMPUTER INC NPI	Title : DDR2 TERMINATION		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 1.2
	P/N: <OrgAddr2>		
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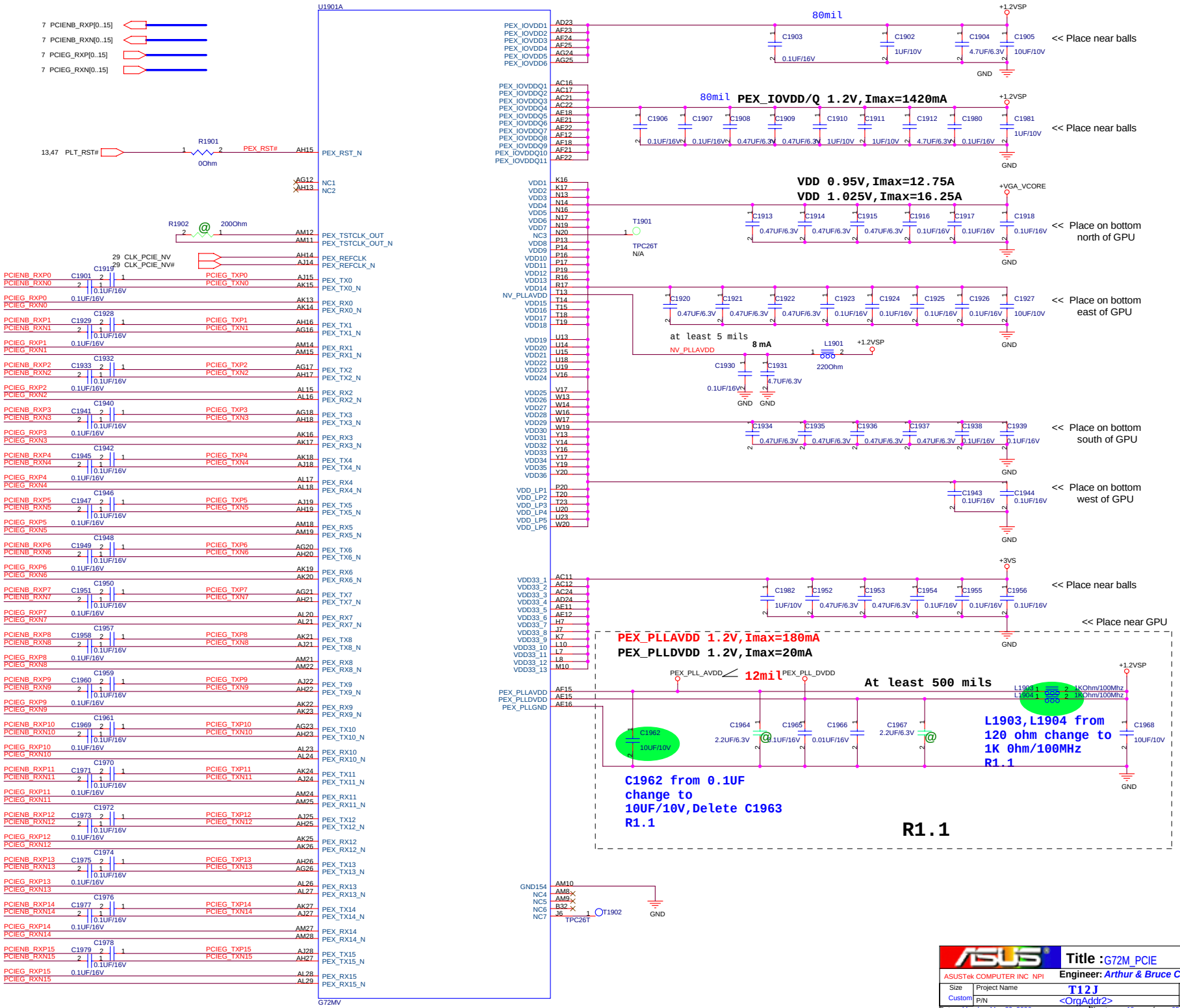

ASUSTek COMPUTER INC NPI	Title : G72M_PCIE		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 1.2
	P/N: <OrgAddr2>		
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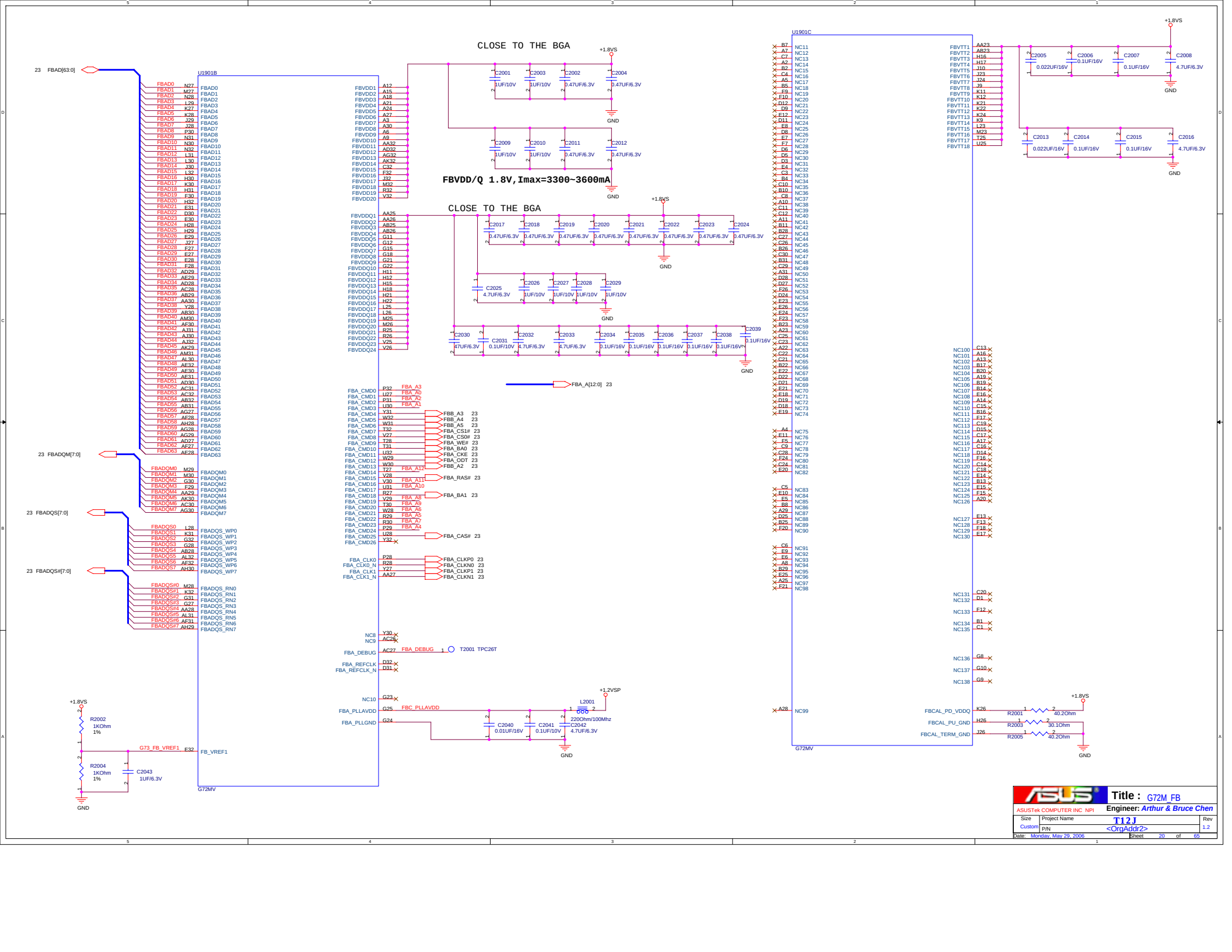
CLOSE TO THE BGA
FBVDD/Q 1.8V,Imax=3300~3600mA
CLOSE TO THE BGA
U1901B
U1901C
G72MV
+1.8VS
+1.2VSP
GND
FBAD[63:0]
FBADQM[7:0]
FBADQS[7:0]
FBADQS#[7:0]
FBA_A[12:0]
T2001 TPC26T
L2001
220Ohm/100Mhz
R2002 1KOhm 1%
R2004 1KOhm 1%
C2043 1UF/6.3V
R2001 40.2Ohm
R2003 30.1Ohm
R2005 40.2Ohm
Title : G72M_FB
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Project Name T12J
Custom
P/N <OrgAddr2>
Rev 1.2
Date: Monday, May 29, 2006
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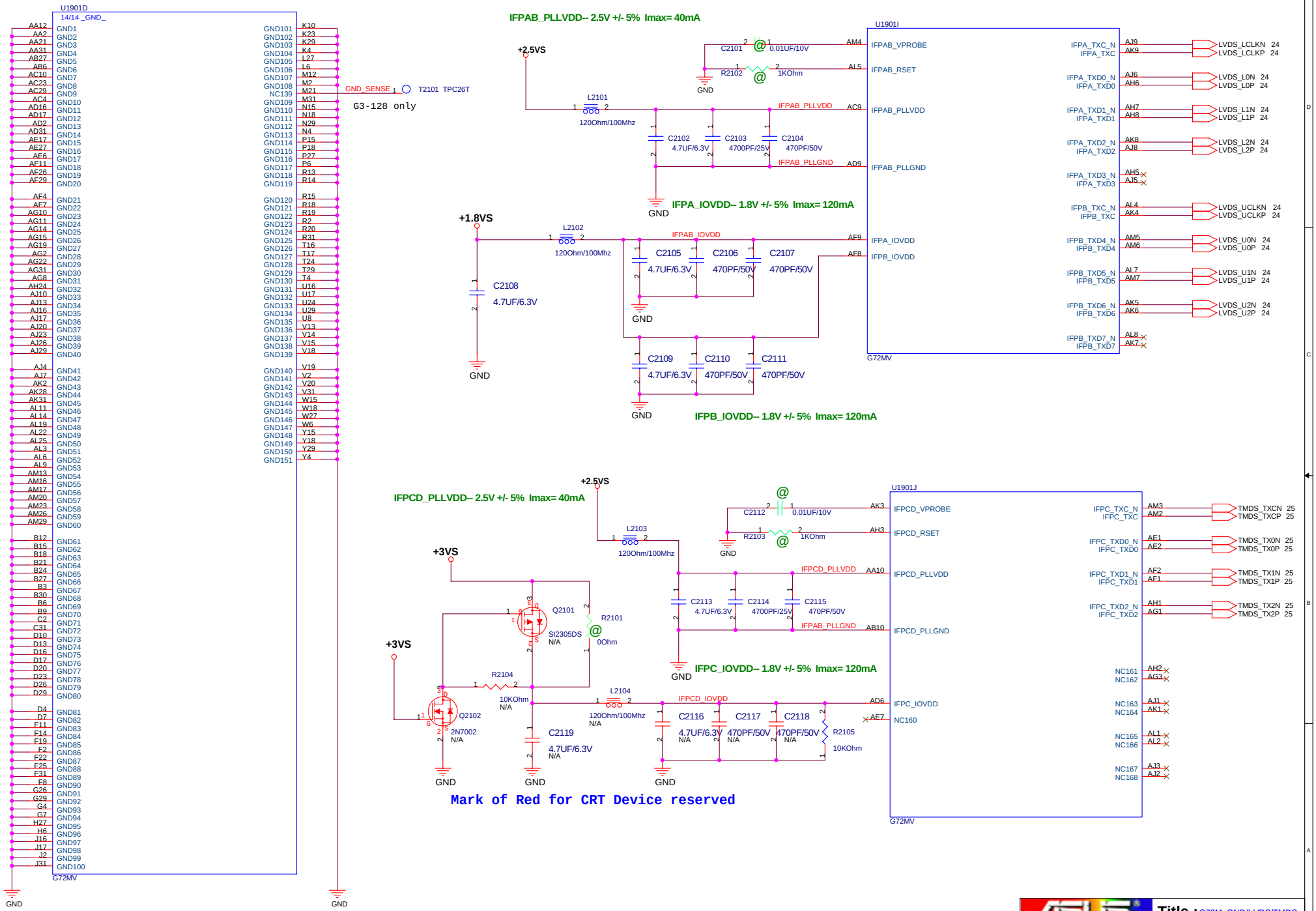
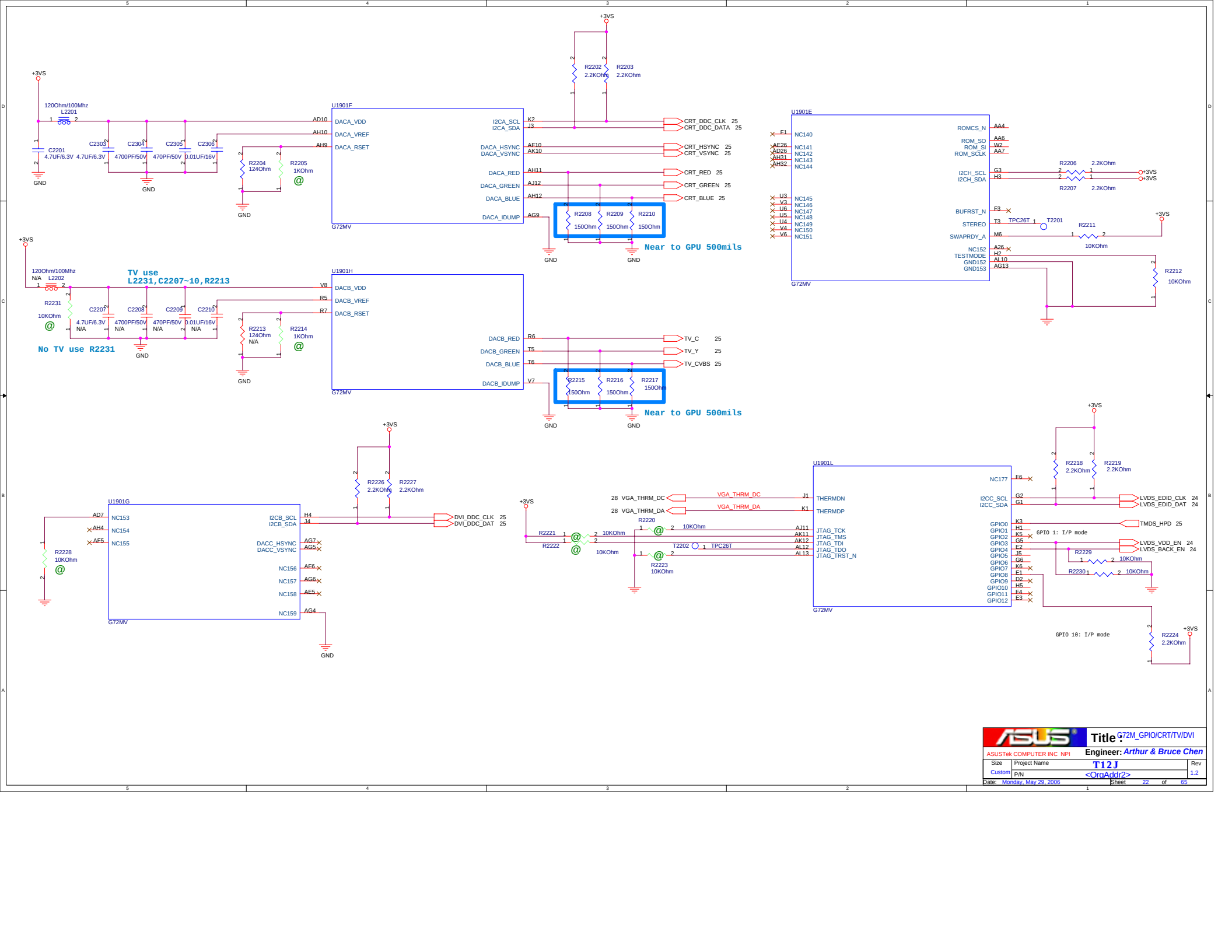
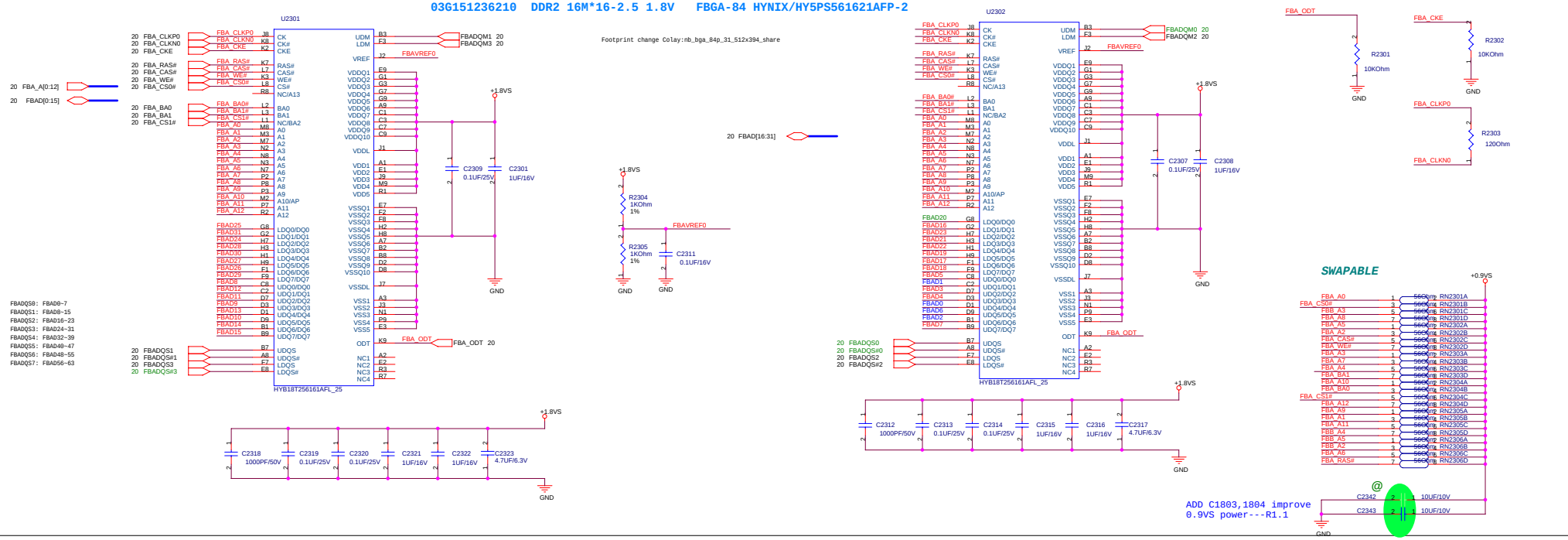

U1901D
14/14 _GND_
GND_SENSE
T2101 TPC26T
G3-128 only
G72MV
IFPAB_PLLVDD-- 2.5V +/- 5% Imax= 40mA
+2.5VS
C2101 0.01UF/10V
R2102 1KOhm
L2101 120Ohm/100Mhz
C2102 4.7UF/6.3V
C2103 4700PF/25V
C2104 470PF/50V
IFPA_IOVDD-- 1.8V +/- 5% Imax= 120mA
+1.8VS
L2102 120Ohm/100Mhz
C2108 4.7UF/6.3V
C2105 4.7UF/6.3V
C2106 470PF/50V
C2107 470PF/50V
C2109 4.7UF/6.3V
C2110 470PF/50V
C2111 470PF/50V
IFPB_IOVDD-- 1.8V +/- 5% Imax= 120mA
IFPCD_PLLVDD-- 2.5V +/- 5% Imax= 40mA
C2112 0.01UF/10V
R2103 1KOhm
L2103 120Ohm/100Mhz
C2113 4.7UF/6.3V
C2114 4700PF/25V
C2115 470PF/50V
Q2101 SI2305DS N/A
R2101 0Ohm
R2104 10KOhm N/A
Q2102 2N7002 N/A
L2104 120Ohm/100Mhz N/A
C2119 4.7UF/6.3V N/A
C2116 4.7UF/6.3V N/A
C2117 470PF/50V N/A
C2118 470PF/50V N/A
R2105 10KOhm
IFPC_IOVDD-- 1.8V +/- 5% Imax= 120mA
Mark of Red for CRT Device reserved
Title : G72M_GND/LVDS/TMDS
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Size Custom
Project Name T12J
P/N <OrgAddr2>
Rev 1.2
Date: Monday, May 29, 2006
Sheet 21 of 65



ASUSTek COMPUTER INC NPI		Title: G72M_GPIO/CRT/TV/DVI	
		Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006		Sheet 22 of 65	

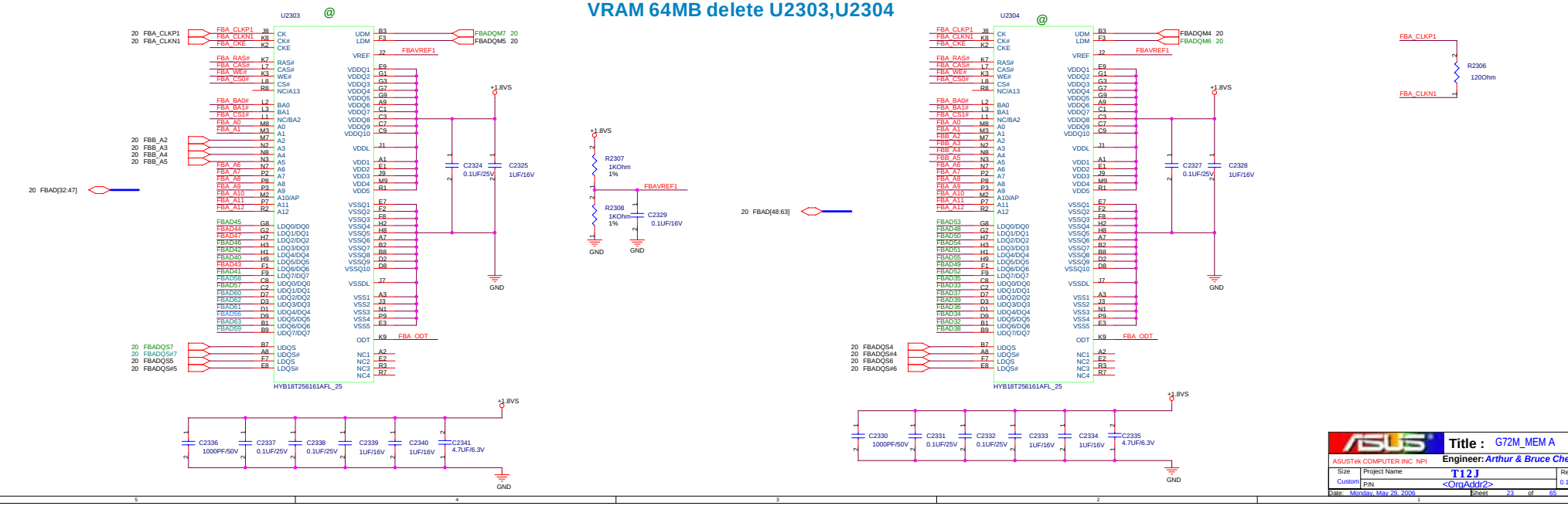
Partition A Low 32 bits

03G151236210 DDR2 16M*16-2.5 1.8V FBGA-84 HYNIX/HY5PS561621AFP-2



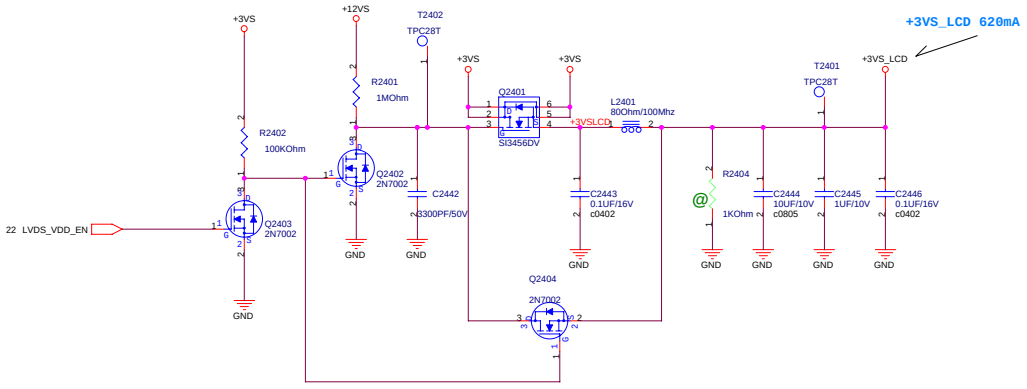
Partition A High 32 bits

VRAM 64MB delete U2303,U2304

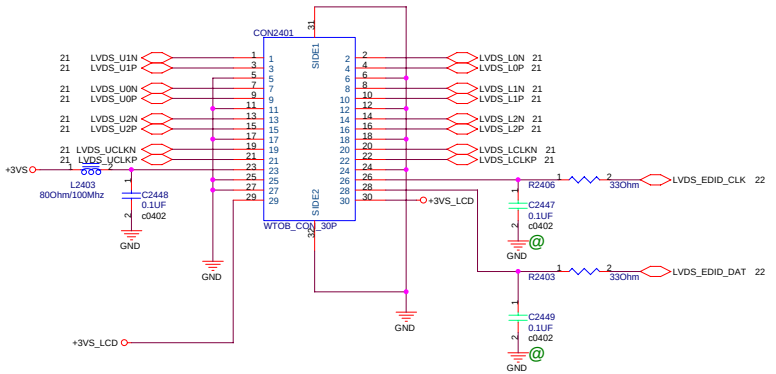


ASUSTeK COMPUTER INC NPI	Title : G72M_MEM A		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 0.1
Date: Monday, May 29, 2006	Sheet 23 of 65		

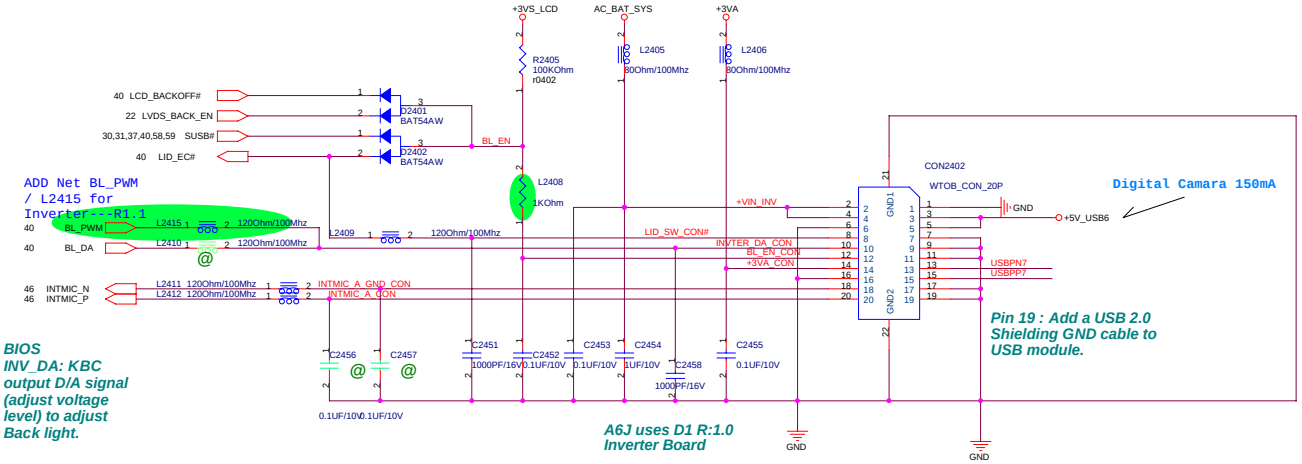
LCD LVDS Interface



Pin define is the same as A7

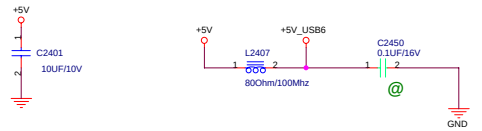


BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

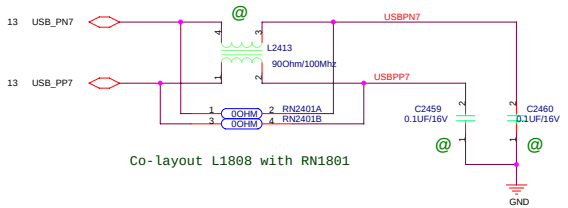


BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

A6J uses D1 R:1.0 Inverter Board

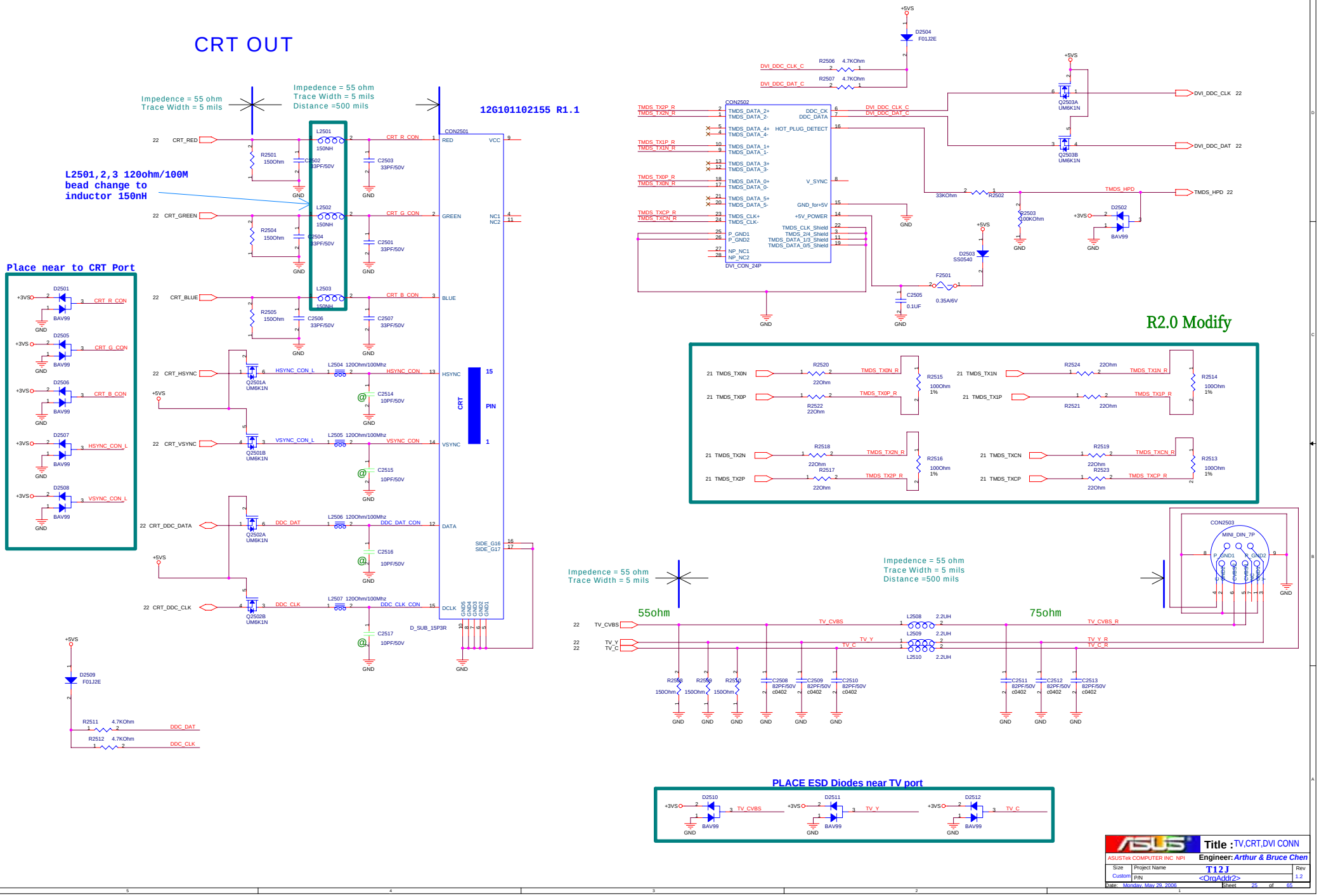


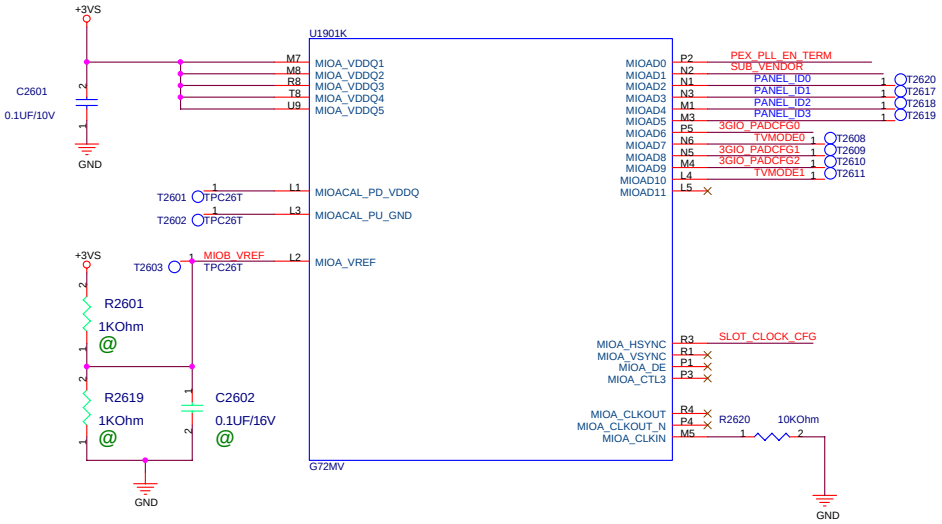
USB PORT 6 for USB CAMERA

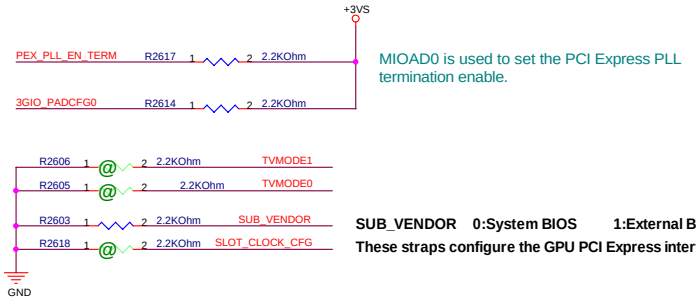


ASUSTek COMPUTER INC NPI	Title : LVDS & INVERTER CONN		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 24 of 65		

CRT OUT


12G101102155 R1.1
Impedence = 55 ohm
Trace Width = 5 mils
Impedence = 55 ohm
Trace Width = 5 mils
Distance =500 mils
L2501,2,3 120ohm/100M
bead change to
inductor 150nH
Place near to CRT Port
CON2501
D_SUB_15P3R
CRT
15
PIN
1
R2 0 Modify
CON2502
DVI_CON_24P
CON2503
MINI_DIN_7P
55ohm
75ohm
Impedence = 55 ohm
Trace Width = 5 mils
Distance =500 mils
PLACE ESD Diodes near TV port
Title : TV,CRT,DVI CONN
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Project Name T12J
P/N <OrgAddr2>
Rev 1.2
Date: Monday, May 29, 2006
Sheet 25 of 65

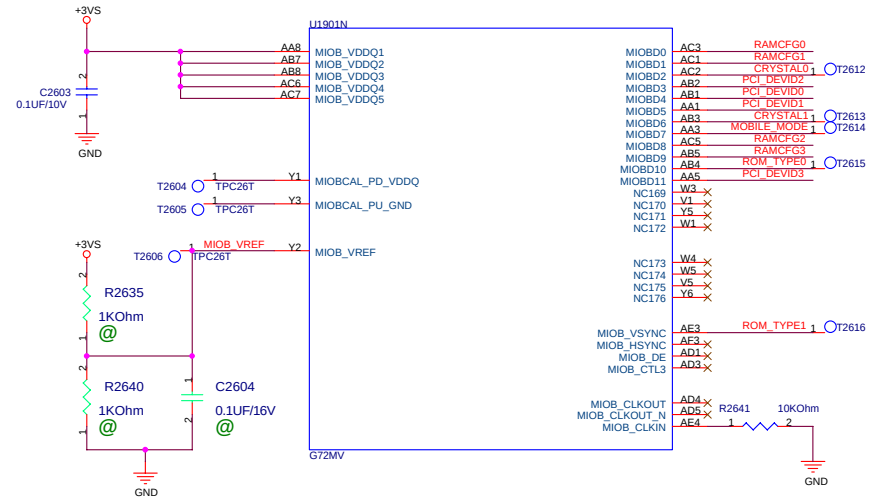


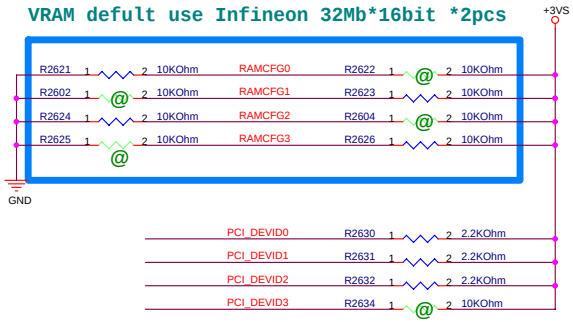


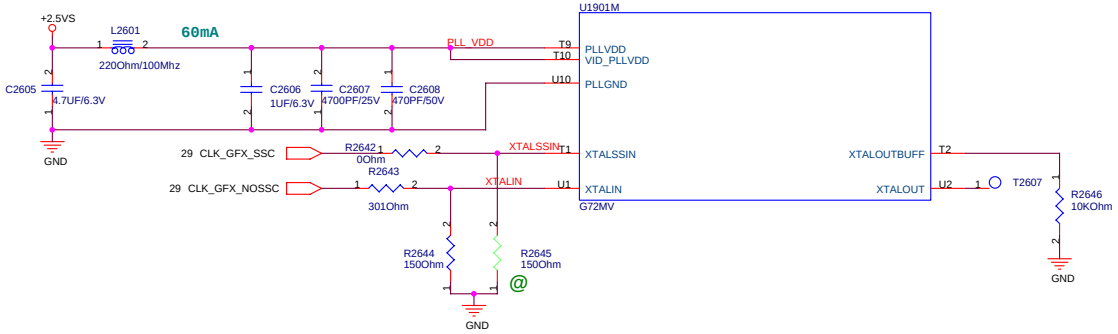
MIOAD0 is used to set the PCI Express PLL termination enable.

SUB_VENDOR 0:System BIOS 1:External BIOS

These straps configure the GPU PCI Express interface.







PANEL_ID[3:0]	**1XXX:Customer Defined**
TVMODE[1:0]	**00:SECAM**
	01:NTSC
	10:PAL
	11:VGA
3GIO_PADCFG[2:0]	**001:For G7x**
RAMCFG[2:0]	**0001:16M x 16 DDR2 64-bit Samsung**
	0010:16M x 16 DDR2 64-bit Infineon
	0011:16M x 16 DDR2 64-bit Hynix
	0101:32M x 16 DDR2 64-bit Samsung
	0110:32M x 16 DDR2 64-bit Infineon
	0111:32M x 16 DDR2 64-bit Hynix
RAMCFG3	**0:Full width of the frame buffer**
	1:Half width of the frame buffer
CRYSTAL[1:0]	**10:27.0MHz**
PCI_DEVID[3:0]	**0111:G72M-V**
	1000:G72M
ROM_TYPE[1:0]	**00:Parallel**
	01:Serial
	10:Reserved
	11:LPC

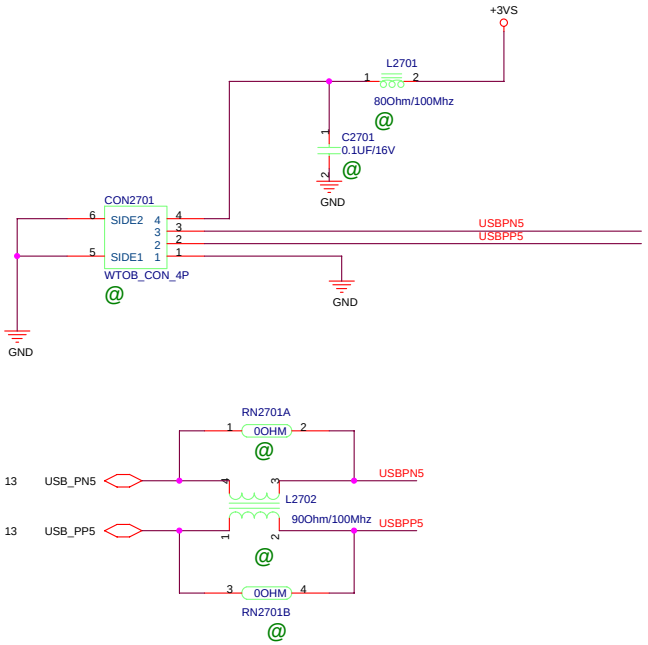
ASUSTek COMPUTER INC NPI

Title : G72M_STRAP/XTAL

Engineer: *Arthur & Bruce Chen*

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 26 of 65



ASUSTek COMPUTER INC NPI	Title : FINGER PRINT		
	Engineer: *Arthur & Bruce Chen*		
Size: Custom	Project Name: T12J		Rev: 2.0
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 27 of 65		

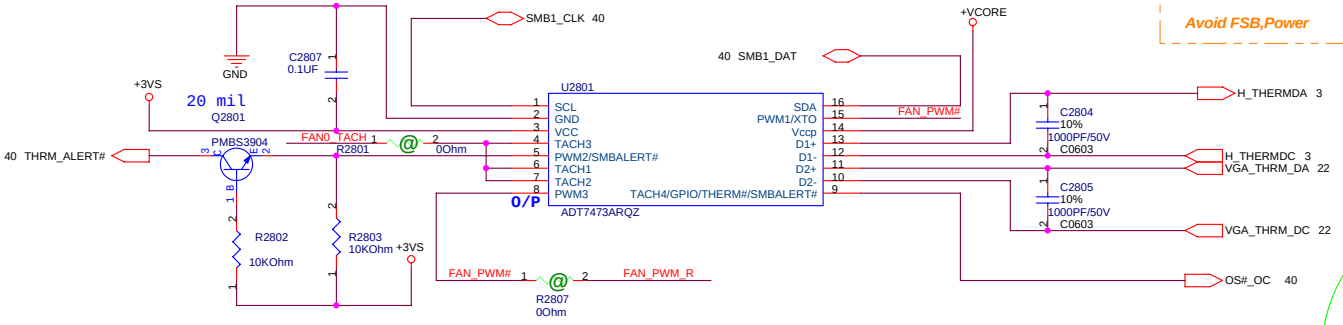
Thermal Sensor

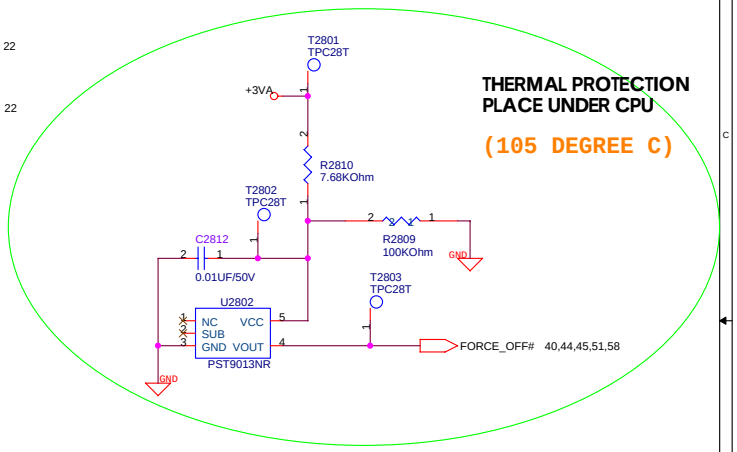
Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
========GND
15 mils
----------OTHER SIGNALS

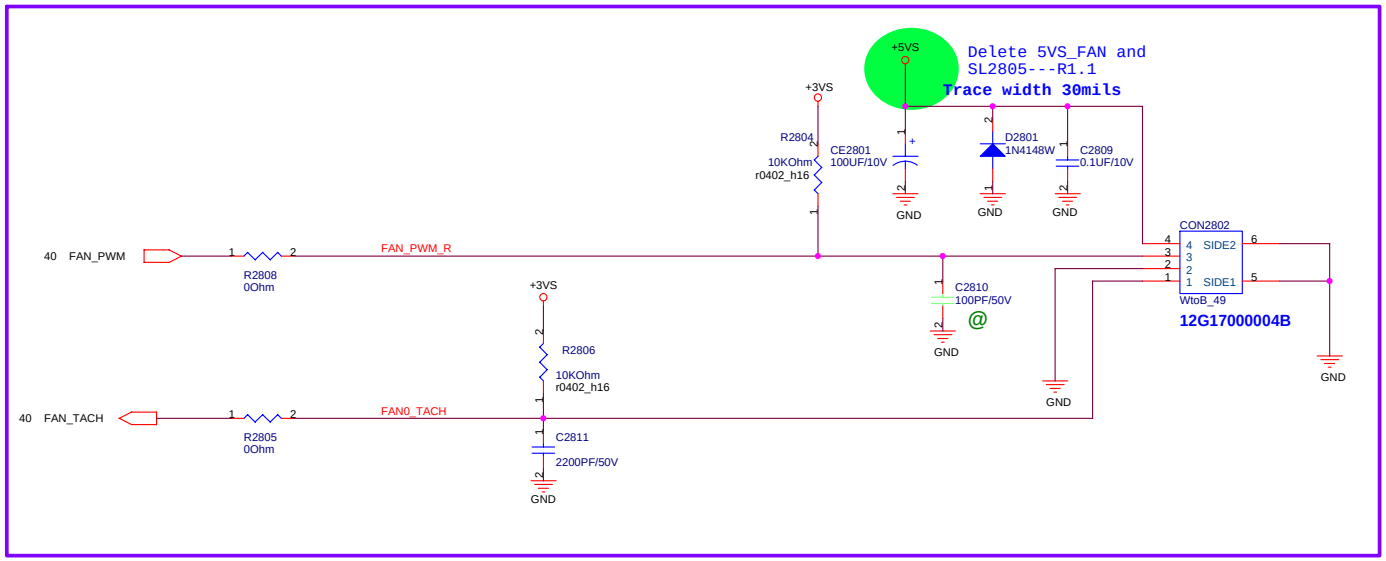
Avoid FSB,Power

Monitors processor core voltage (0 – 3V)

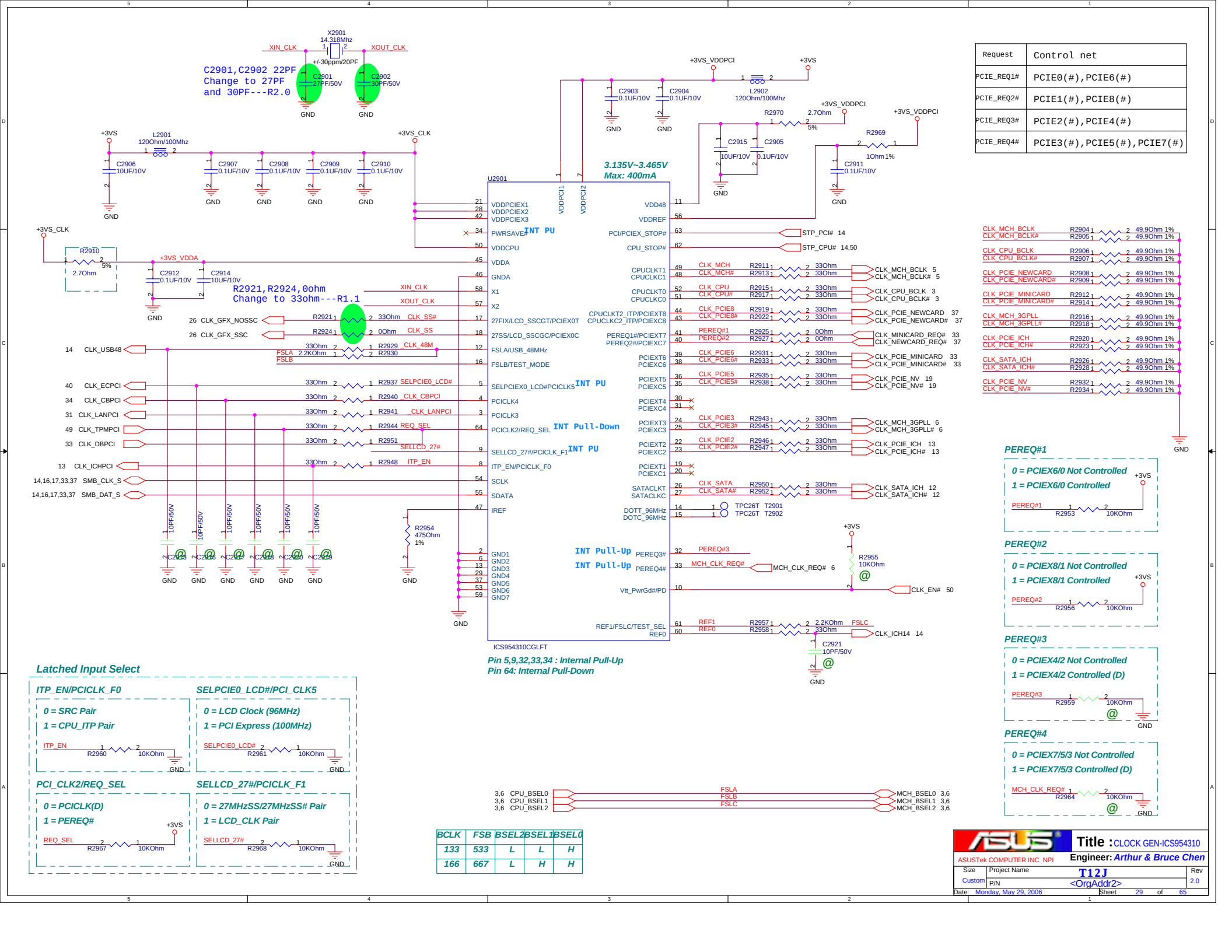




DC FAN Control



ASUSTek COMPUTER INC NPI	Title : THER SENSOR & FAN	
Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	Rev: 2.0
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 28 of 65	



Request	Control net
PCIE_REQ1#	PCIE0(#),PCIE6(#)
PCIE_REQ2#	PCIE1(#),PCIE8(#)
PCIE_REQ3#	PCIE2(#),PCIE4(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#),PCIE7(#)

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

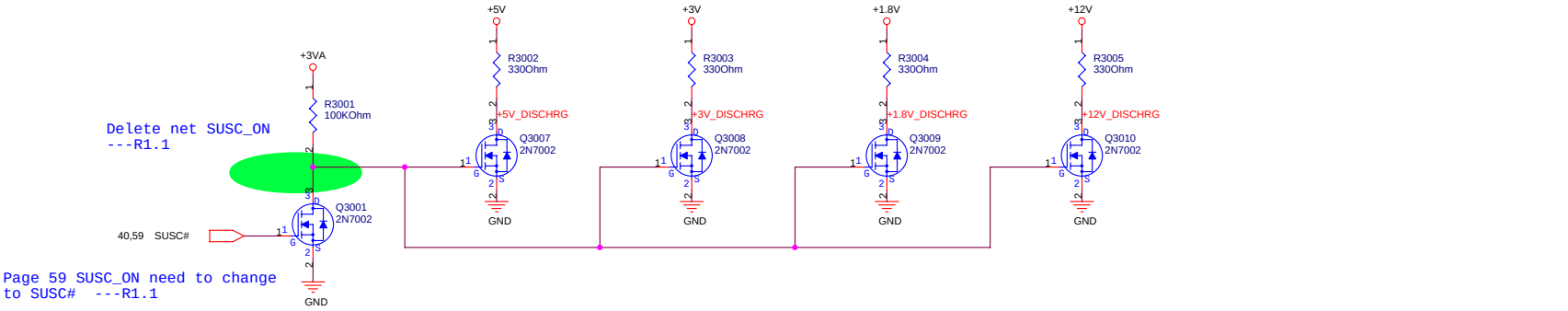
ASUSTek COMPUTER INC NPI

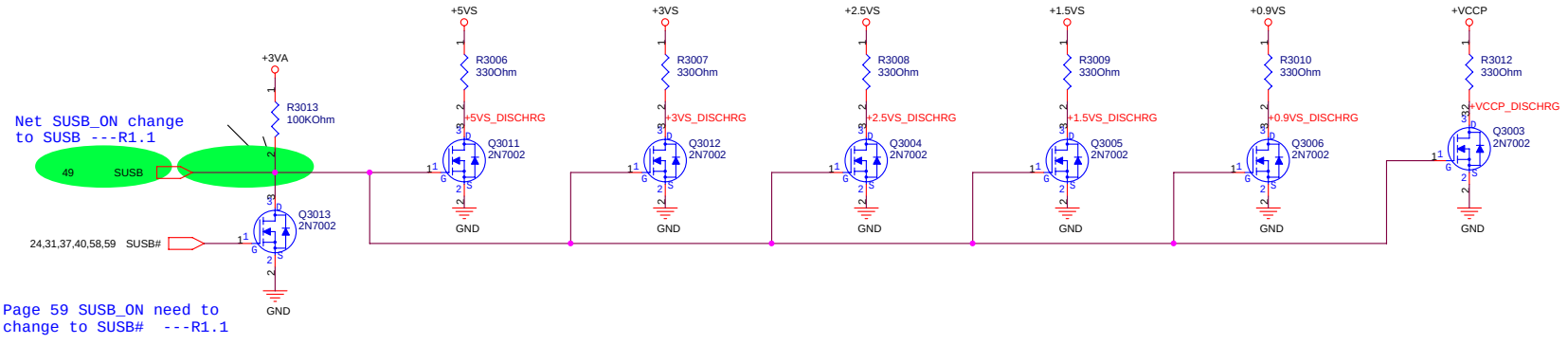
Title : CLOCK GEN-ICS954310

Engineer: Arthur & Bruce Chen

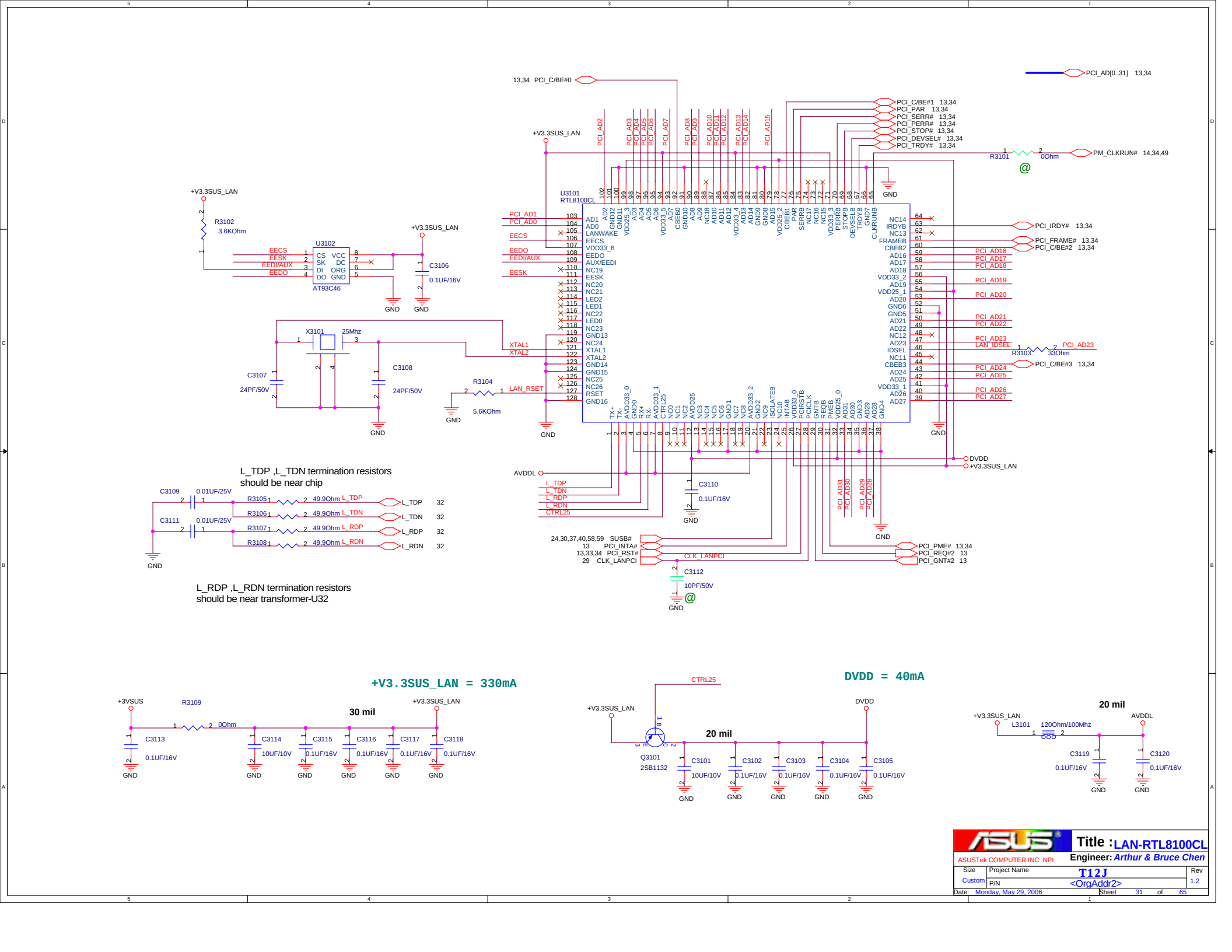
Size	Project Name	Rev
Custom	T12J	2.0
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 29 of 65

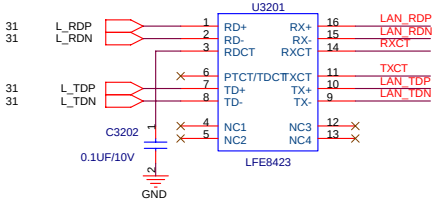




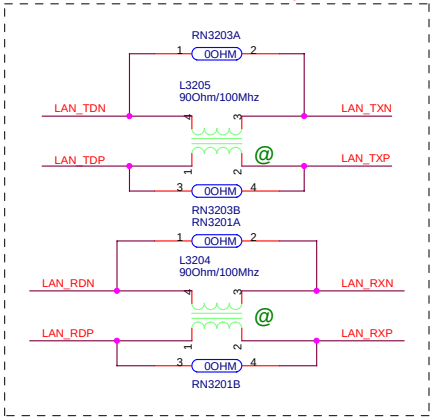
ASUSTek COMPUTER INC NPI	Title : DISCHARGE & EMI CAP		
	Engineer: *Arthur & Bruce Chen*		
Size: Custom	Project Name: T12J		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 30 of 65		

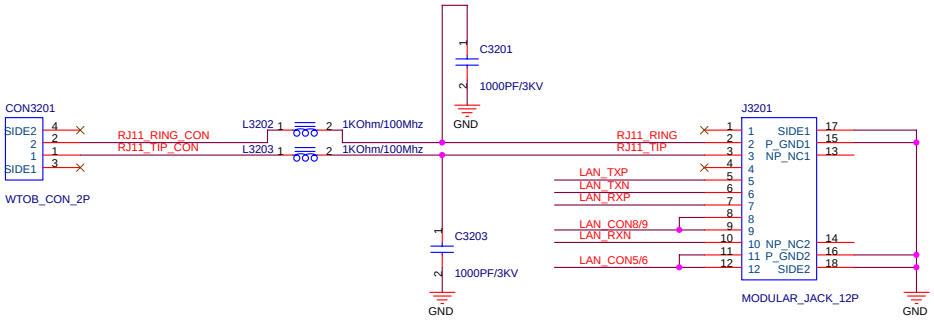

PCI_AD[0..31] 13,34
13,34 PCI_C/BE#0
PCI_C/BE#1 13,34
PCI_PAR 13,34
PCI_SERR# 13,34
PCI_PERR# 13,34
PCI_STOP# 13,34
PCI_DEVSEL# 13,34
PCI_TRDY# 13,34
R3101 0Ohm @
PM_CLKRUN# 14,34,49
+V3.3SUS_LAN
U3101
RTL8100CL
PCI_IRDY# 13,34
PCI_FRAME# 13,34
PCI_C/BE#2 13,34
PCI_C/BE#3 13,34
R3103 33Ohm
LAN_IDSEL
R3102 3.6KOhm
U3102
AT93C46
EECS
EESK
EEDI/AUX
EEDO
C3106 0.1UF/16V
X3101 25Mhz
C3107 24PF/50V
C3108 24PF/50V
XTAL1
XTAL2
R3104 5.6KOhm
LAN_RSET
GND
L_TDP ,L_TDN termination resistors
should be near chip
C3109 0.01UF/25V
C3111 0.01UF/25V
R3105 49.9Ohm L_TDP
R3106 49.9Ohm L_TDN
R3107 49.9Ohm L_RDP
R3108 49.9Ohm L_RDN
L_TDP
L_TDN
L_RDP
L_RDN
32
L_RDP ,L_RDN termination resistors
should be near transformer-U32
AVDDL
DVDD
+V3.3SUS_LAN
C3110 0.1UF/16V
C3112 10PF/50V @
CTRL25
CLK_LANPCI
24,30,37,40,58,59 SUSB#
13 PCI_INTA#
13,33,34 PCI_RST#
29 CLK_LANPCI
PCI_PME# 13,34
PCI_REQ#2 13
PCI_GNT#2 13
+V3.3SUS_LAN = 330mA
+3VSUS
R3109 0Ohm
30 mil
C3113 0.1UF/16V
C3114 10UF/10V
C3115 0.1UF/16V
C3116 0.1UF/16V
C3117 0.1UF/16V
C3118 0.1UF/16V
DVDD = 40mA
20 mil
Q3101 2SB1132
C3101 10UF/10V
C3102 0.1UF/16V
C3103 0.1UF/16V
C3104 0.1UF/16V
C3105 0.1UF/16V
20 mil
L3101 120Ohm/100Mhz
C3119 0.1UF/16V
C3120 0.1UF/16V
Title : LAN-RTL8100CL
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Size Custom
Project Name T12J
P/N <OrgAddr2>
Rev 1.2
Date: Monday, May 29, 2006
Sheet 31 of 65

RJ11&RJ45 Port

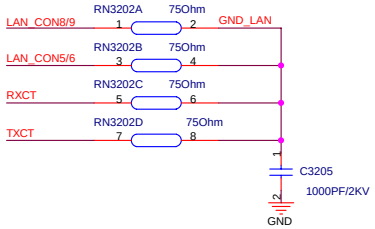


FOR EMI Co-Lay

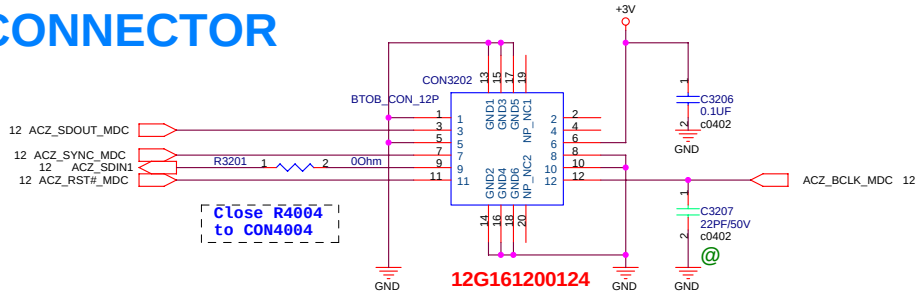


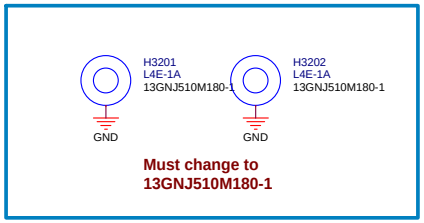


Change
12G142111120 R1.1

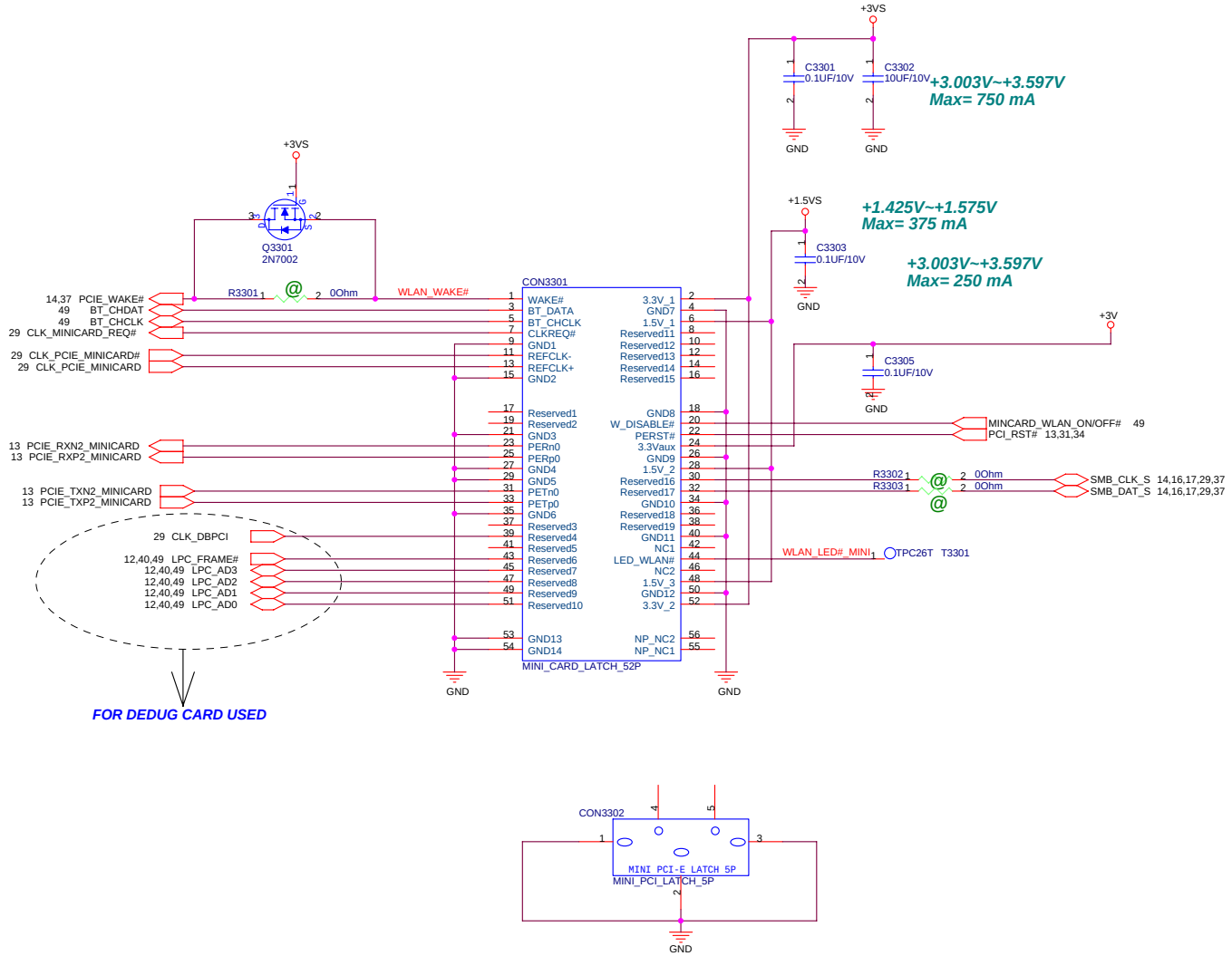


MDC CONNECTOR

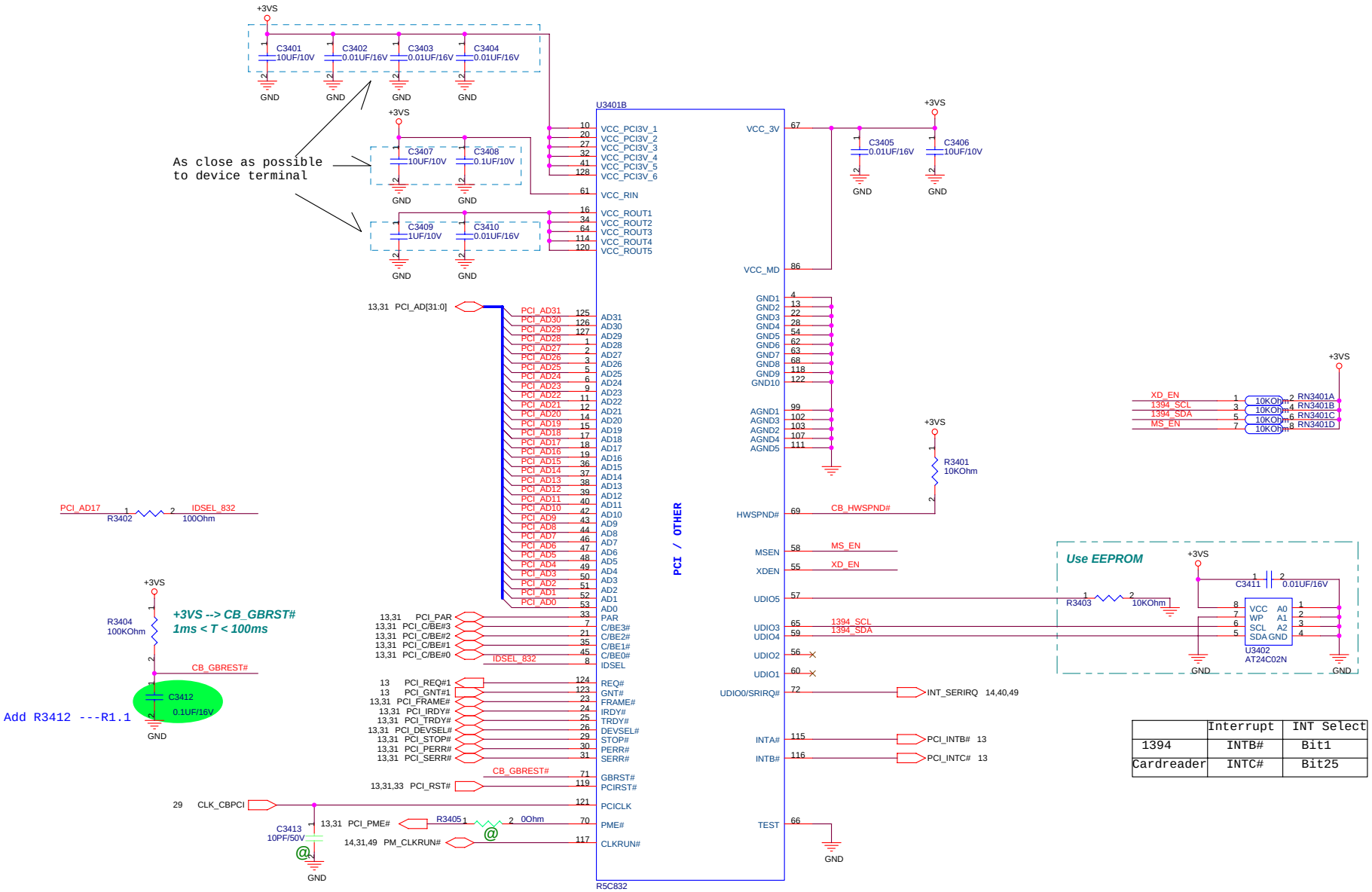




ASUSTek COMPUTER INC NPI	Title : MDC & RJ45+11	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 32 of 65	



ASUSTek COMPUTER INC NPI	Title : MINICARD	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 2.0
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 33 of 65	



	Interrupt	INT Select
1394	INTB#	Bit1
Cardreader	INTC#	Bit25

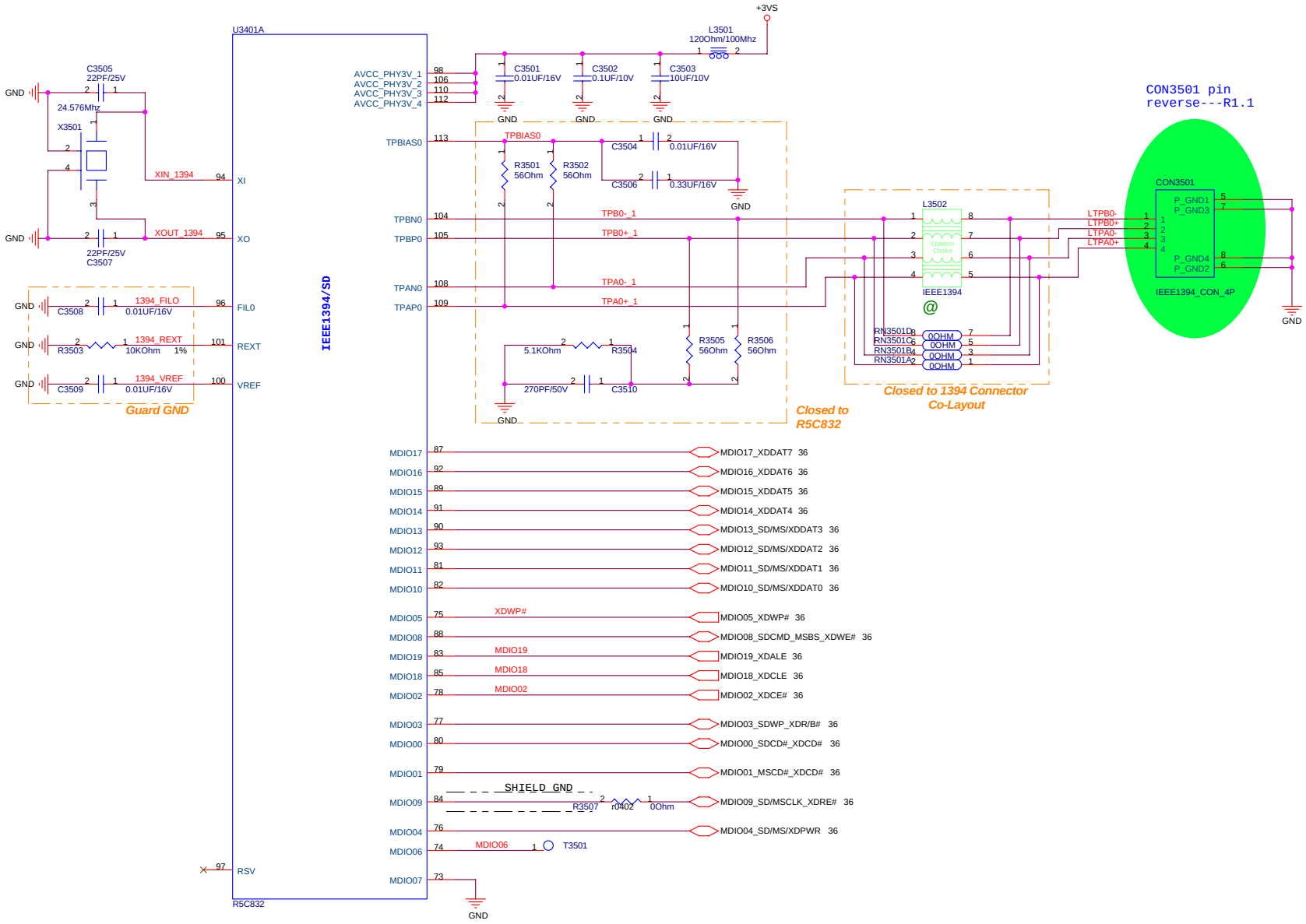
ASUSTek COMPUTER INC NPI

Title : R5C832(1)-PCI

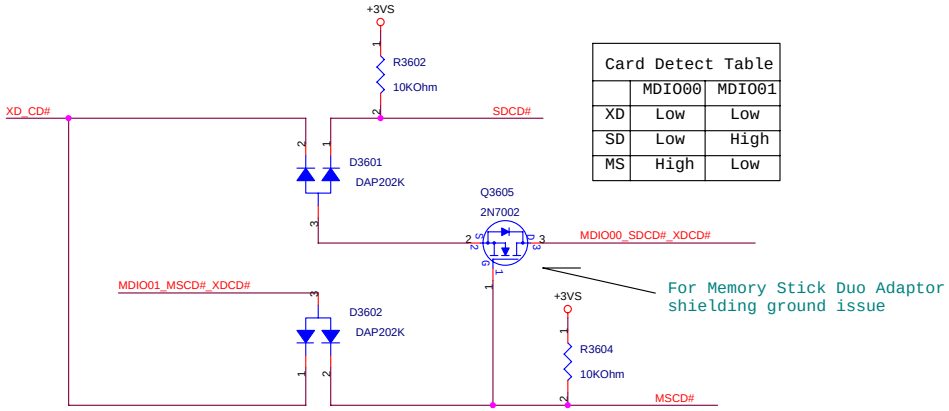
Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 34 of 65

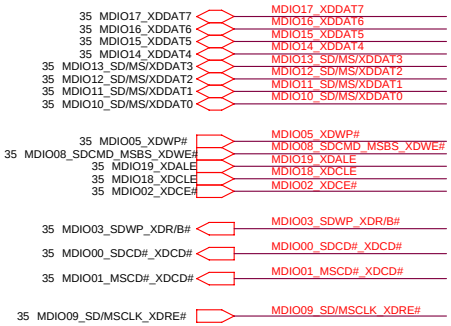


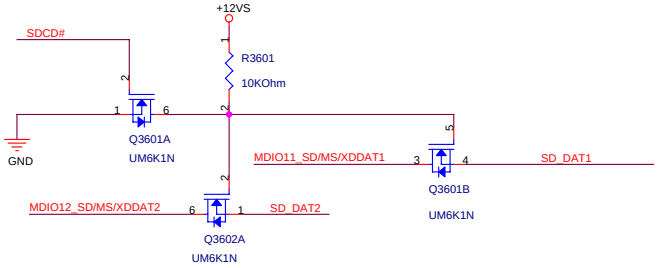
ASUSTek COMPUTER INC NPI	Title : R5C832-1394(2)	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 35 of 65	

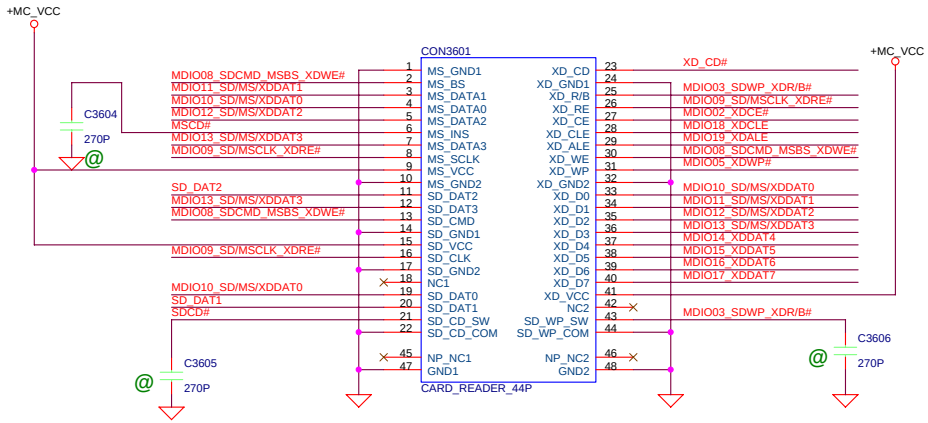


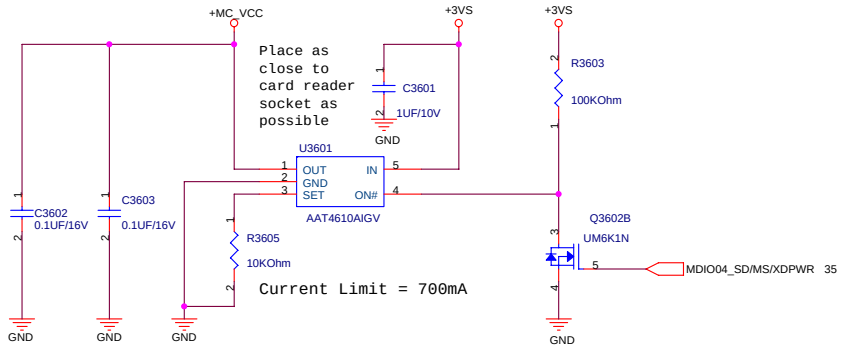
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU







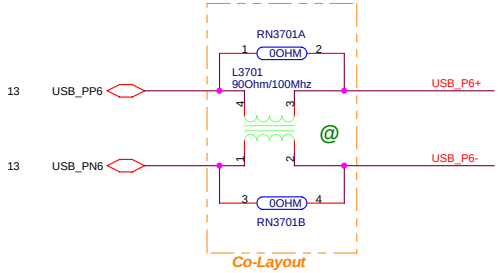


ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen

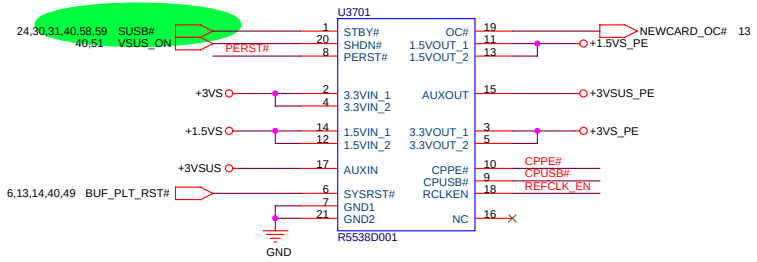
Title : 4 in 1 CARD READER

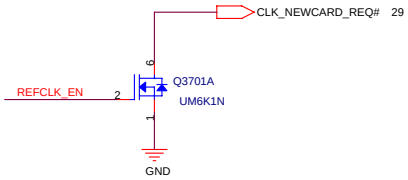
Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 36 of 65



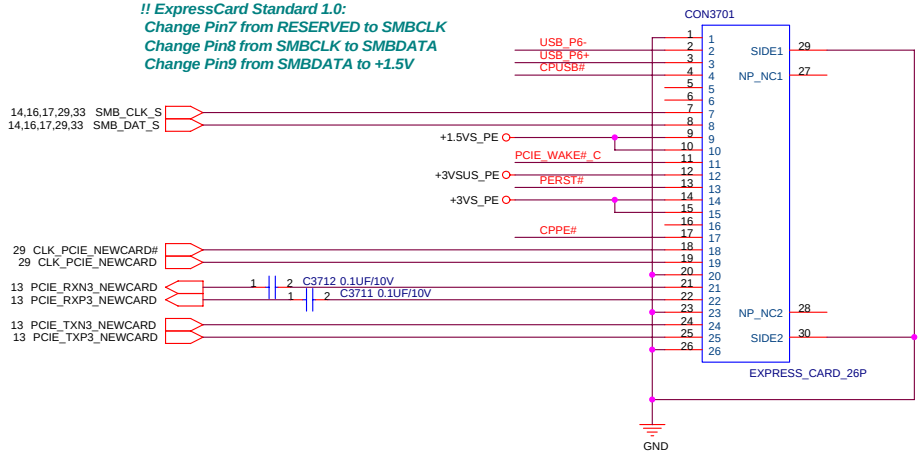
SUSB_ON change to
SUSB# ---R1.1



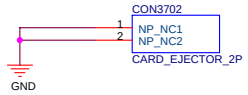


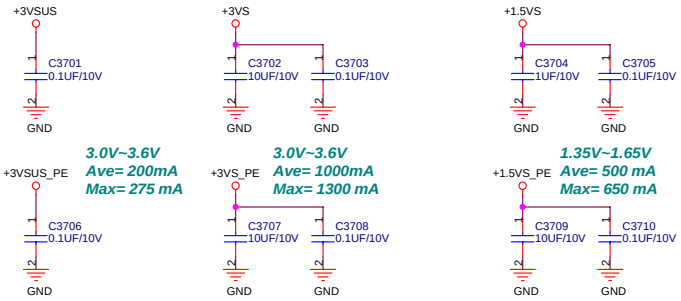
NewCard Header

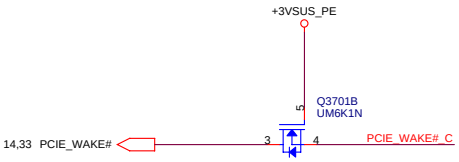
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



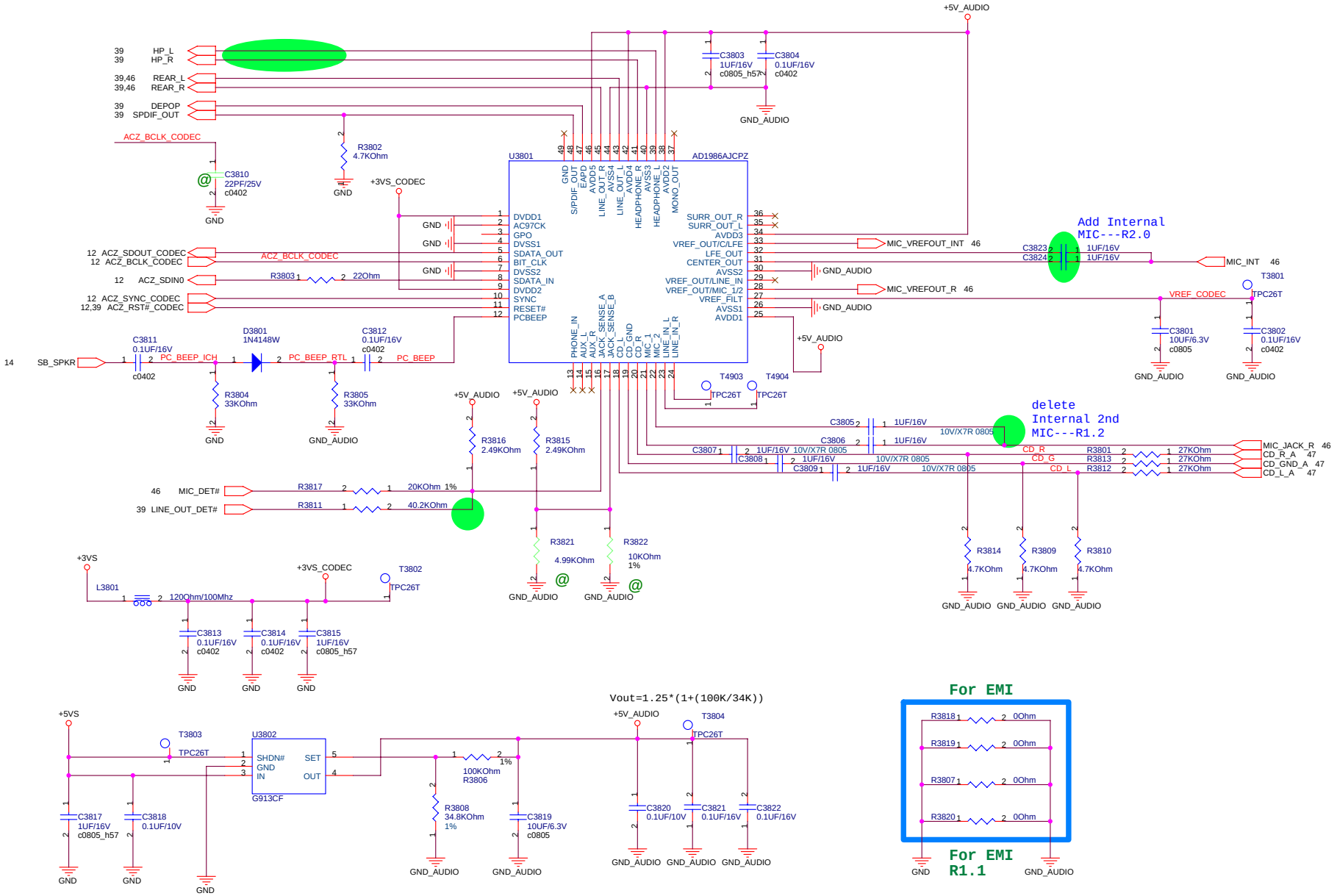
NewCard Ejecter







ASUSTek COMPUTER INC NPI	Title : NEWCARD	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 37 of 65	



ASUSTek COMPUTER INC NPI	Title : AUDIO-AD1986A		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 38 of 65		

Headphone & Middle/High Range Frequency Amplifier (Tweeter)

FL = TBD
FH = TBD

C3907,C3914 change from 0.47 to 10UF/6.3V ---R1.2

(Headphone Mode) FL = TBD
(Headphone Mode) FH = TBD

R3917 change from 10G212106004030 to 10G212105004010

CE3901,CE3902 (11G041233758)change footprint from cesmd_209x209_h217 to hh_cesmd_260x260_hin---R1.1

INTERNAL SPEAKER CONNECTOR

To Internal Speaker Connector

0603 package

Change chanel---R1.2

12G171000049

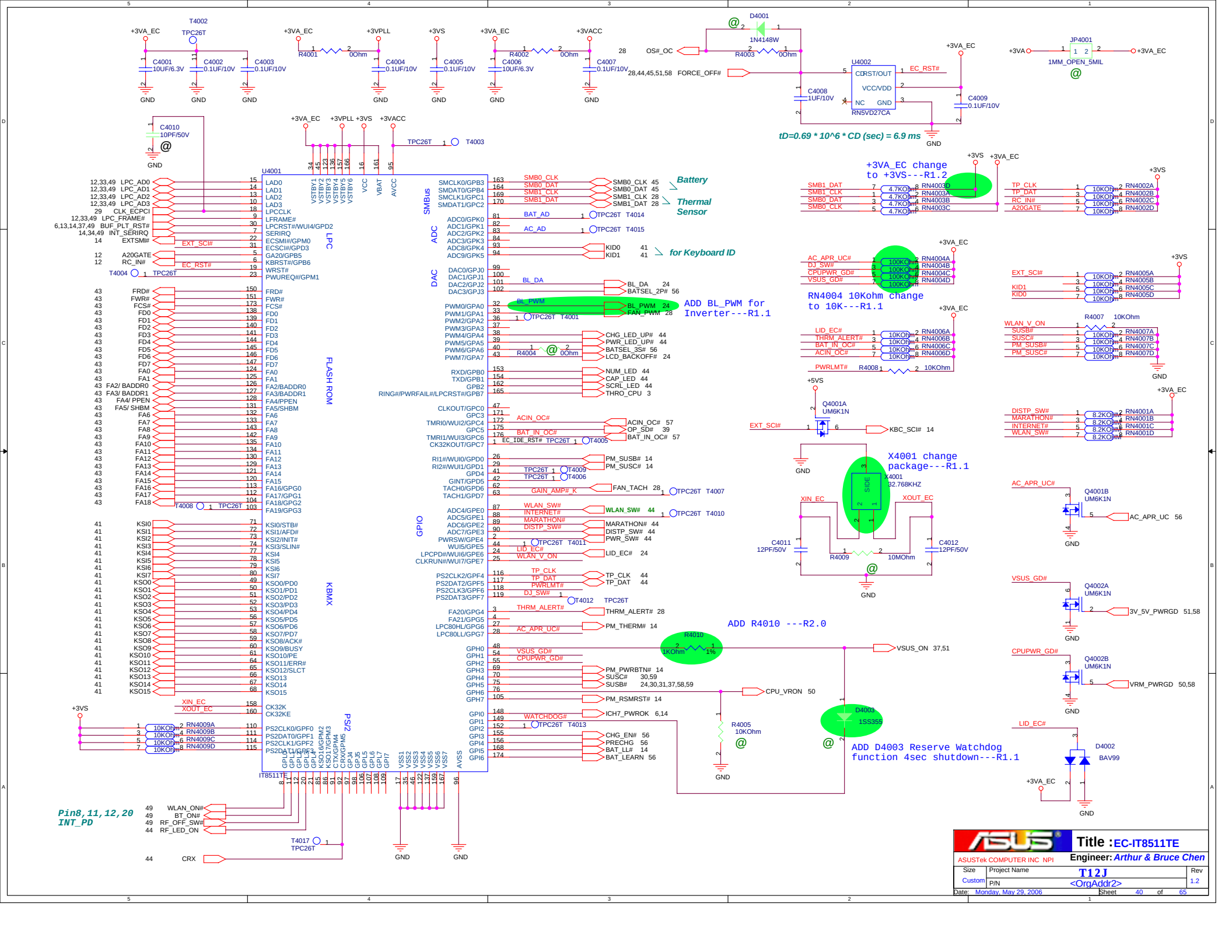
SPIDF JACK

For EMI

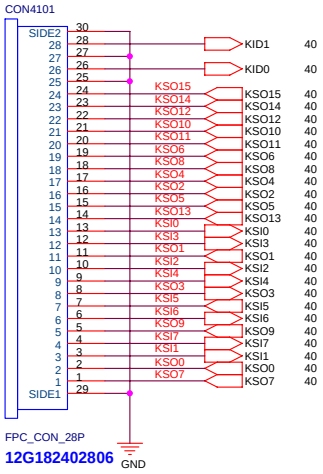
For EMI R1.1

For EMI

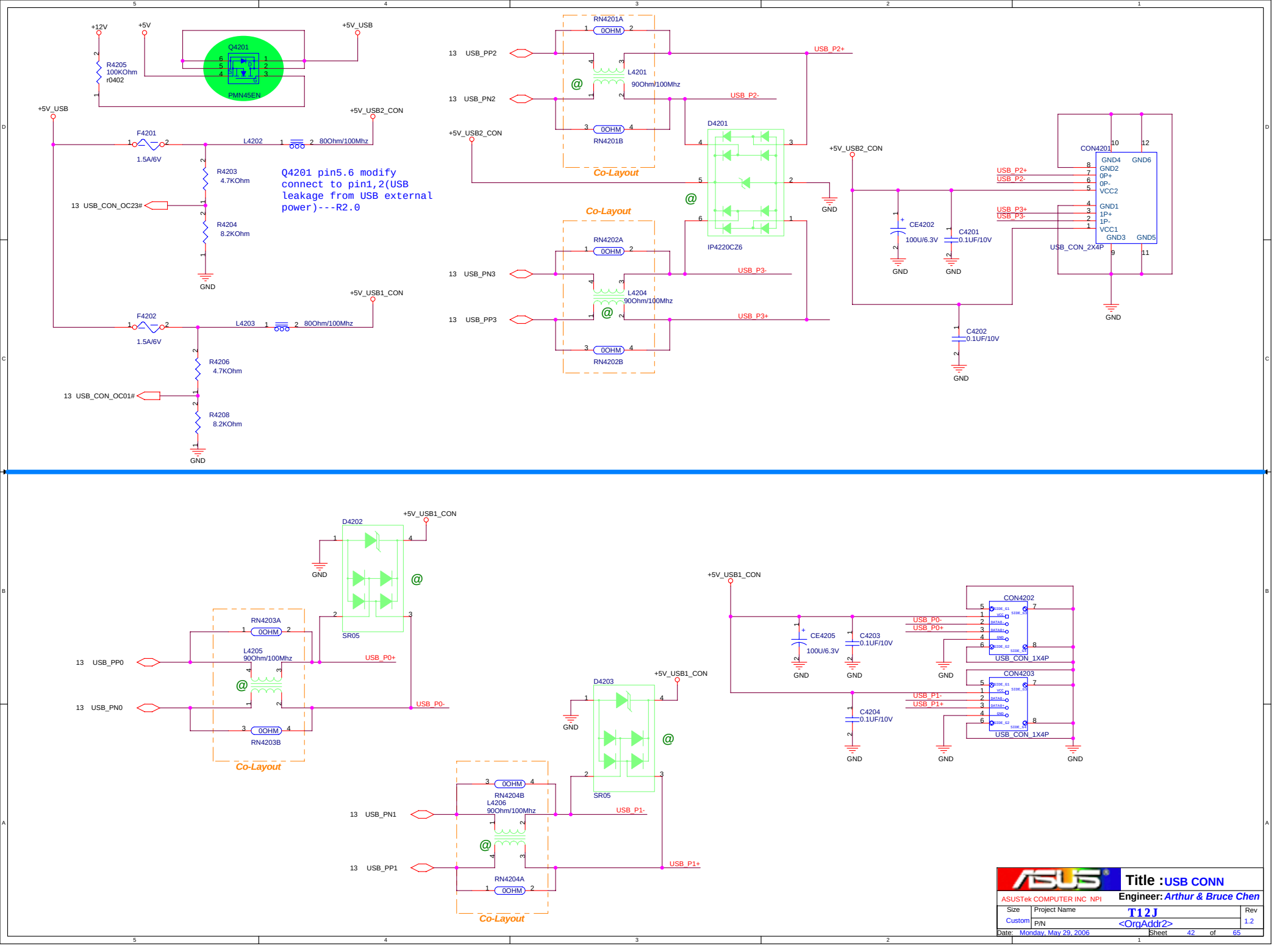
ASUSTek COMPUTER INC NPI	Title : AUDIO AMP & SPDIF		
	Engineer: *Arthur & Bruce Chen*		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 39 of 65		


U4001
IT8511TE
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
Battery
Thermal Sensor
for Keyboard ID
ADD BL_PWM for Inverter---R1.1
+3VA_EC change to +3VS---R1.2
RN4004 10Kohm change to 10K---R1.1
X4001 change package---R1.1
ADD R4010 ---R2.0
ADD D4003 Reserve Watchdog function 4sec shutdown---R1.1
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
Pin8,11,12,20 INT_PD
Title : EC-IT8511TE
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Project Name T12J
P/N <OrgAddr2>
Rev 1.2
Date: Monday, May 29, 2006
Sheet 40 of 65

For Keyboard
Metrix Define same Z94



ASUSTek COMPUTER INC NPI	Title : Keyboard CONN		
	Engineer: *Arthur & Bruce Chen*		
Size: Custom	Project Name: T12J		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 41 of 65		


+12V
+5V
+5V_USB
Q4201
PMN45EN
R4205
100KOhm
r0402
+5V_USB
+5V_USB2_CON
F4201
1.5A/6V
L4202
80Ohm/100Mhz
R4203
4.7KOhm
13 USB_CON_OC23#
R4204
8.2KOhm
GND
Q4201 pin5.6 modify
connect to pin1,2(USB
leakage from USB external
power)---R2.0
+5V_USB1_CON
F4202
1.5A/6V
L4203
80Ohm/100Mhz
R4206
4.7KOhm
13 USB_CON_OC01#
R4208
8.2KOhm
GND
RN4201A
0OHM
13 USB_PP2
13 USB_PN2
L4201
90Ohm/100Mhz
RN4201B
USB_P2+
USB_P2-
D4201
IP4220CZ6
Co-Layout
RN4202A
13 USB_PN3
13 USB_PP3
L4204
90Ohm/100Mhz
RN4202B
USB_P3-
USB_P3+
CE4202
100U/6.3V
C4201
0.1UF/10V
C4202
0.1UF/10V
CON4201
GND4
GND6
GND2
0P+
0P-
VCC2
GND1
1P+
1P-
VCC1
GND3
GND5
USB_CON_2X4P
D4202
SR05
RN4203A
13 USB_PP0
13 USB_PN0
L4205
90Ohm/100Mhz
RN4203B
USB_P0+
USB_P0-
CE4205
100U/6.3V
C4203
0.1UF/10V
C4204
0.1UF/10V
CON4202
CON4203
USB_CON_1X4P
D4203
RN4204B
13 USB_PN1
13 USB_PP1
L4206
90Ohm/100Mhz
RN4204A
USB_P1-
USB_P1+
Co-Layout
Title : USB CONN
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
Size
Custom
Project Name
T12J
P/N
<OrgAddr2>
Rev
1.2
Date: Monday, May 29, 2006
Sheet 42 of 65

ISA ROM

EC Hardware Strapping

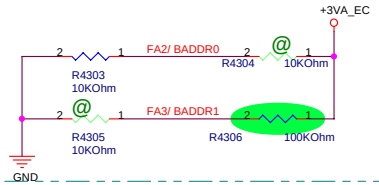
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

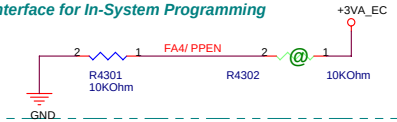


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

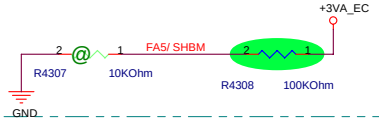
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



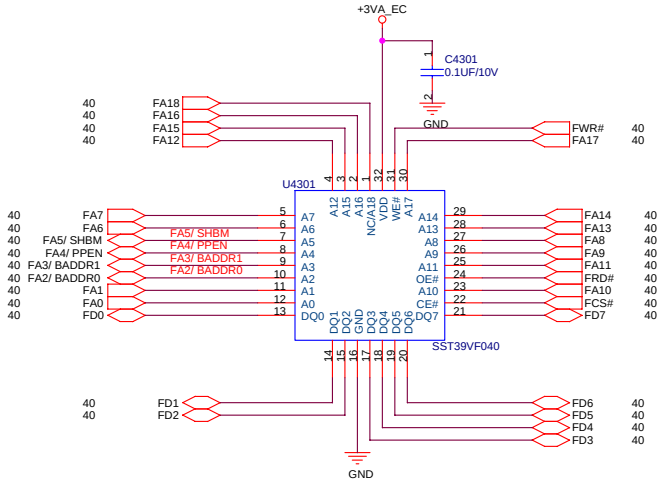
FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

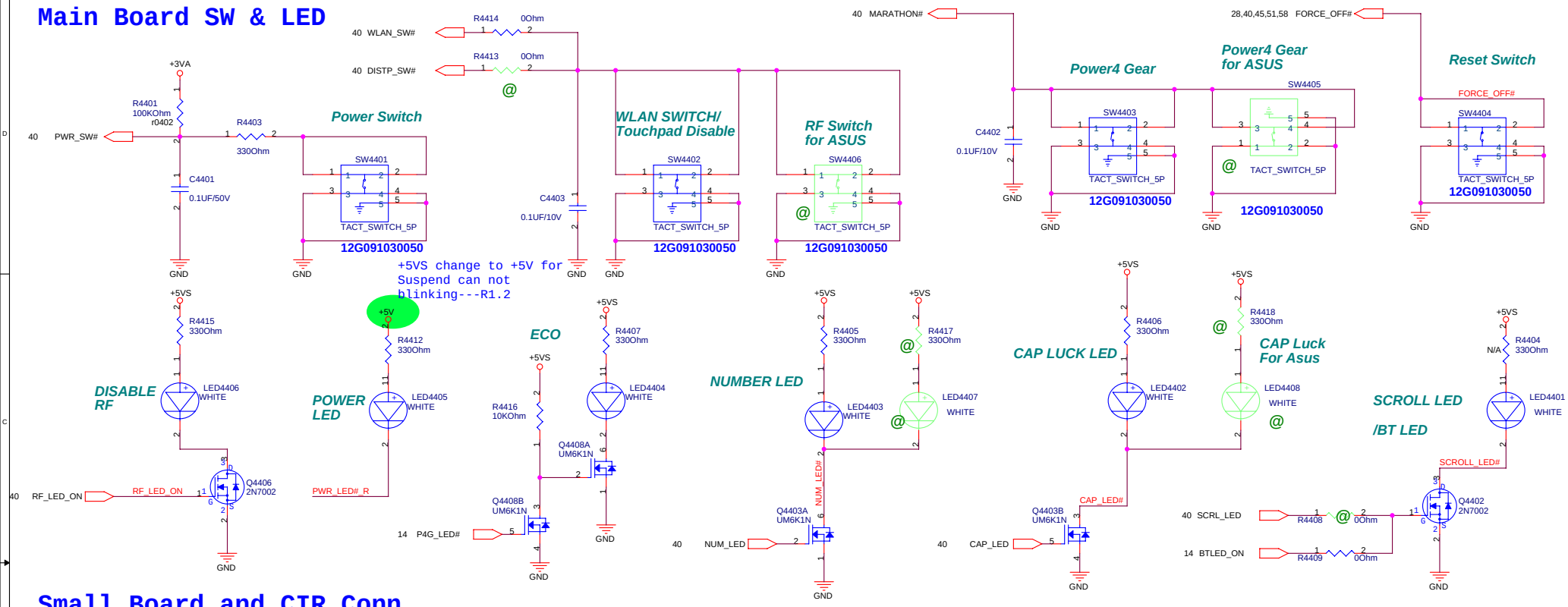


R4306,R4308 10Kohm change to 100Kohm---R1.2



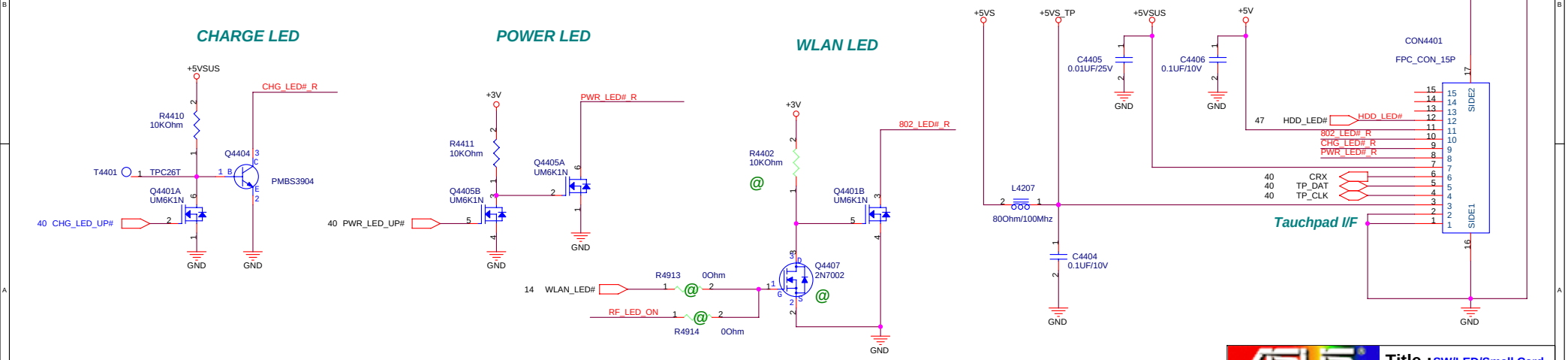
Title : ISA ROM		
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 43 of 65	

Main Board SW & LED



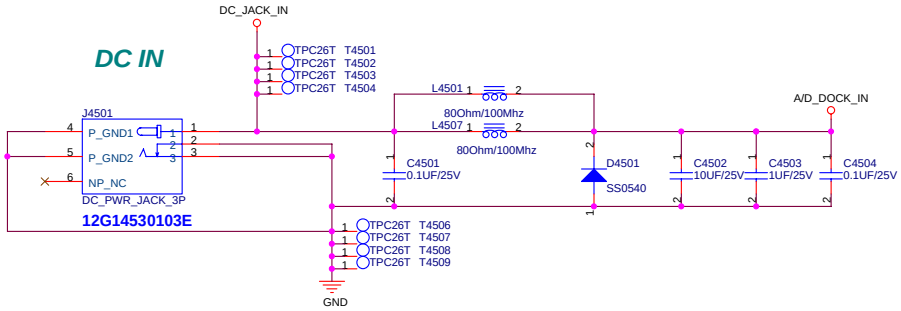
Small Board and CIR Conn.

LED Board Connector



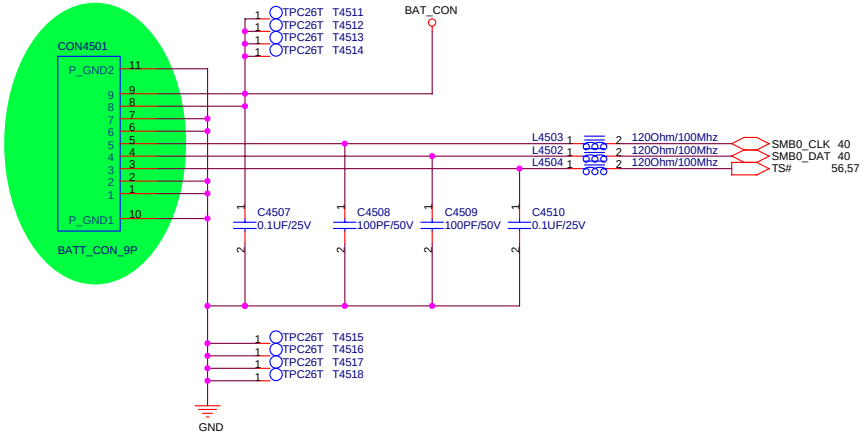
ASUSTek COMPUTER INC NPI	Title : SW/LED/Small Card	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 44 of 65	

DC IN



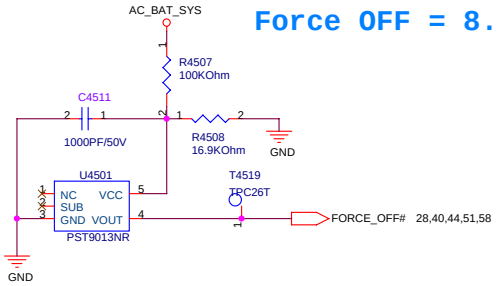
BAT IN

CON4501 change package---R1.1



Without Battery & Pull out Adapter

Force OFF = 8.99V

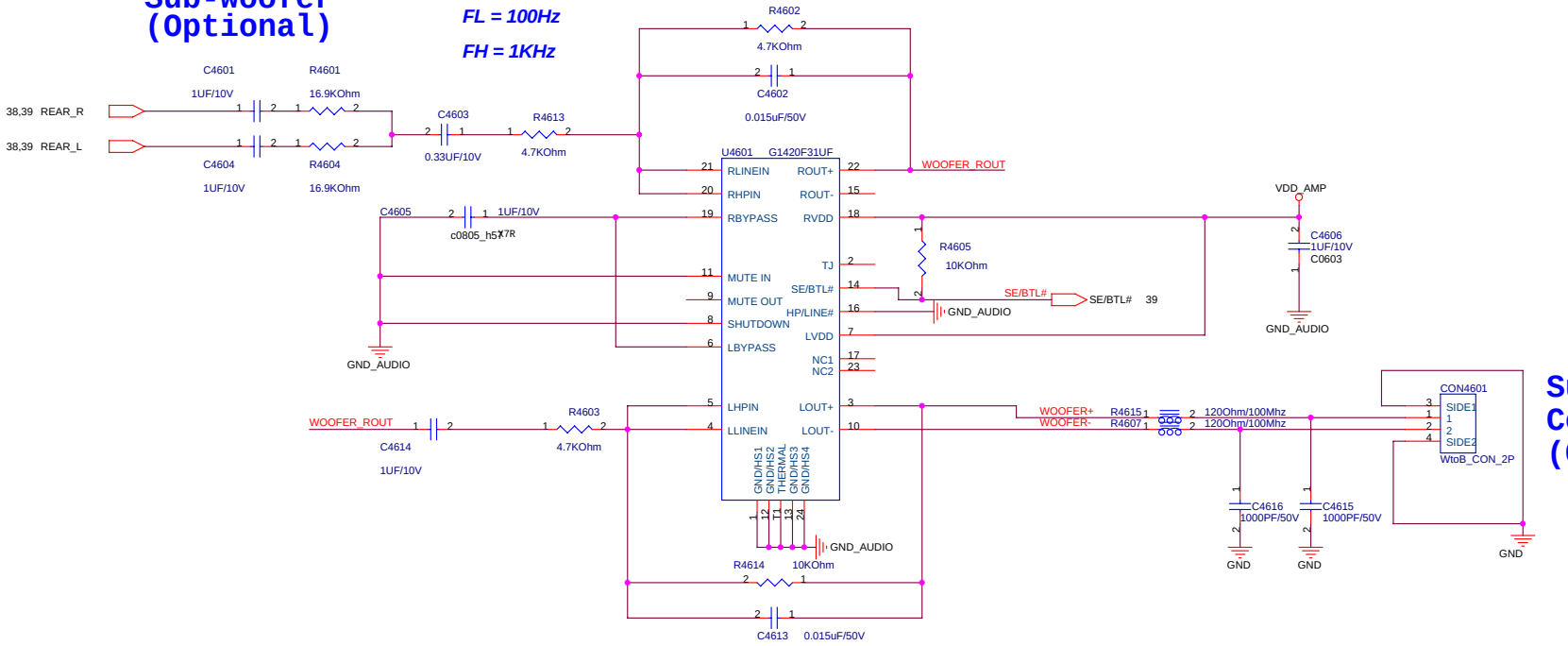


ASUSTek COMPUTER INC NPI	Title : DC & BAT IN	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 0.1
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 45 of 65	

Sub-woofer (Optional)

FL = 100Hz

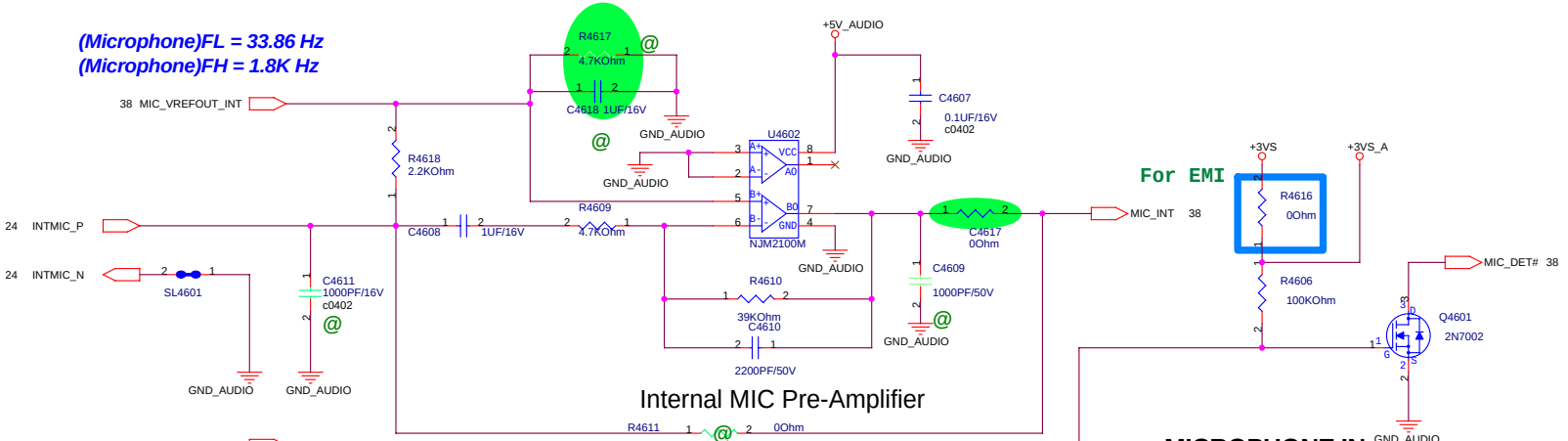
FH = 1KHz



Sub-woofer Connector (Optional)

(Microphone)FL = 33.86 Hz

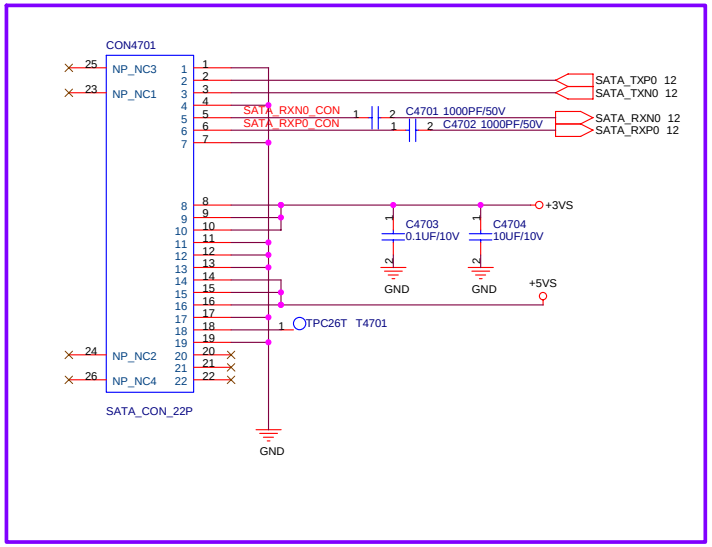
(Microphone)FH = 1.8K Hz



CON4601(Pin3) net name GND_JACK change to Floating---R1.1

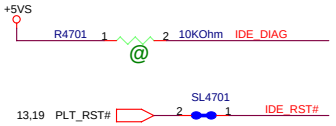
CON4601(12G14000106G) package change to 12G14030106E---R1.1

ASUSTek COMPUTER INC NPI	Title : MIC & PreAMP	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 46 of 65	

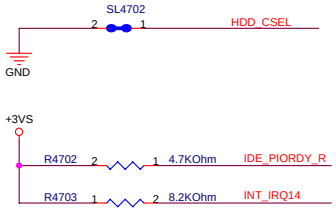


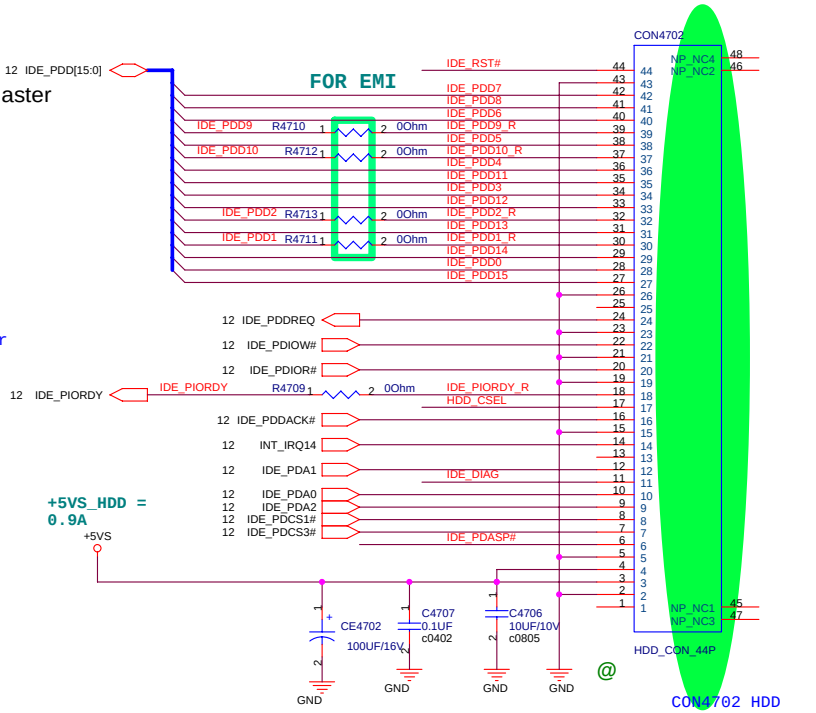
SATA HDD

HD_CSEL : Pull-Down, HDD as Master



HDD_CSEL : Pull-Down HDD as Master



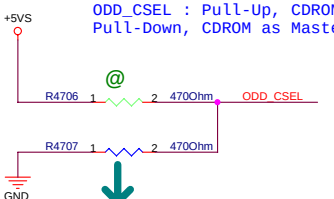


CON4702 HDD connector reverse---R1.1

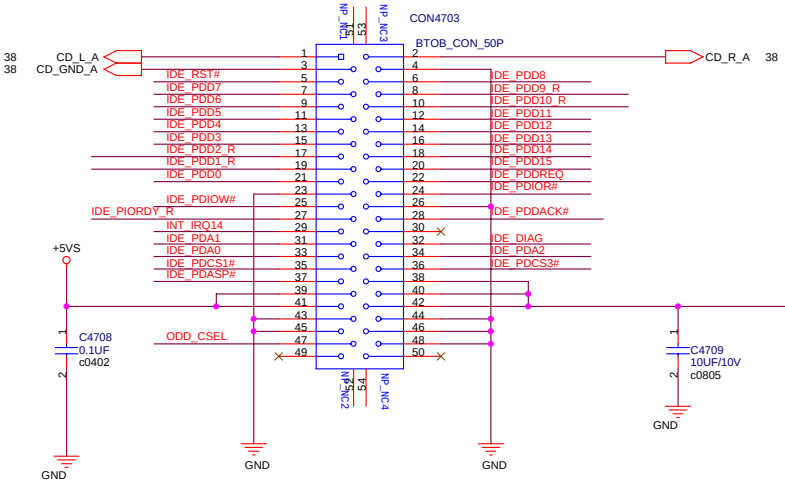
PATA HDD

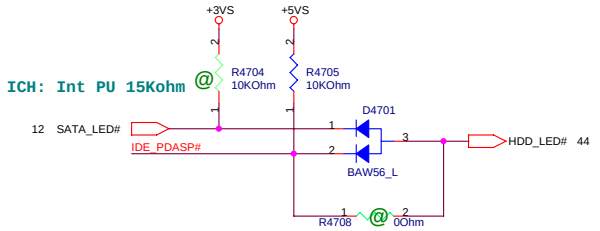
CD-ROM

ODD_CSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master



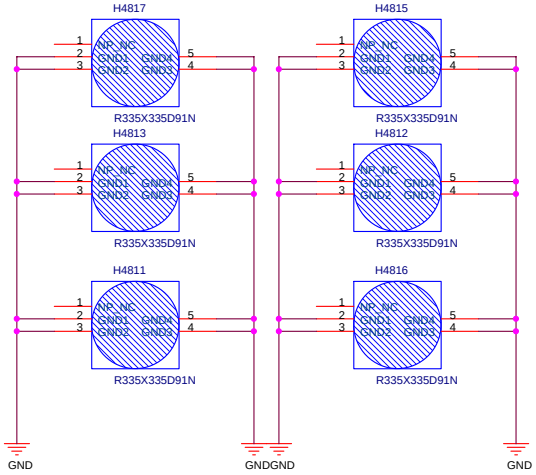
Use SATA HDD BOM the ODD select R4707(Secondary Master)



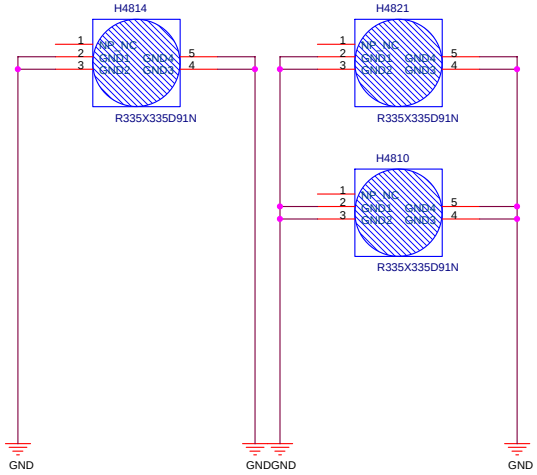


ASUSTek COMPUTER INC NPI	Title : SATA-HDD & ODD	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 47 of 65	

A Hole / TOP Side



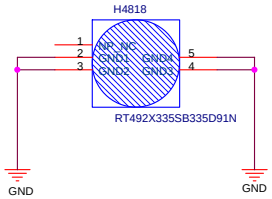
A Hole / Bottom Side



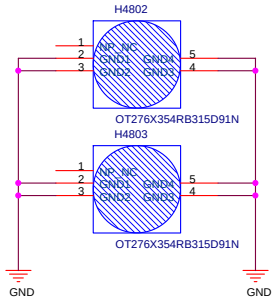
Drill Hole for Fix

圓孔　　橢圓孔　　圓孔New R1.1

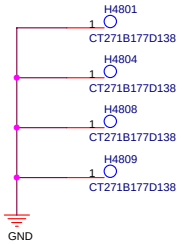
A Hole Special / Bottom Side



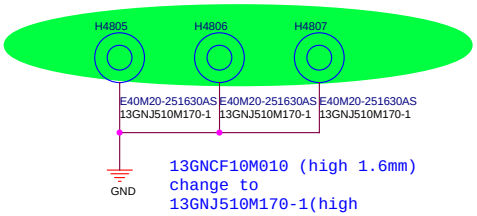
E Hole for Main board fix



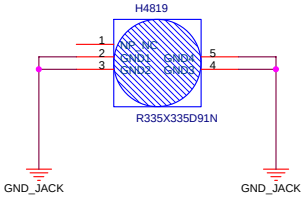
F Hole for CPU



銅柱 Hole for VGA 13GNJ510M170-1

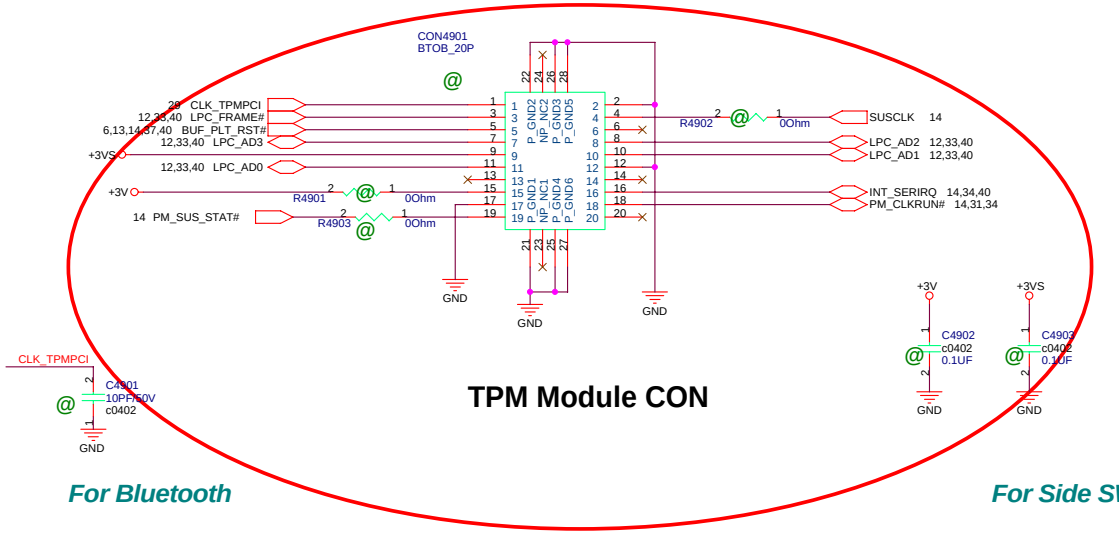


13GNCF10M010 (high 1.6mm) change to 13GNJ510M170-1(high 1.2mm)---R1.1

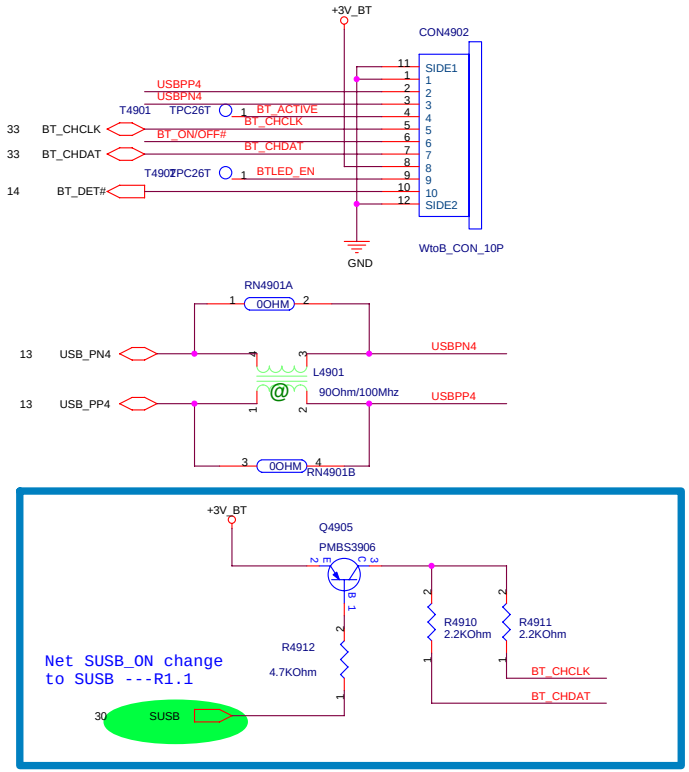


ASUSTek COMPUTER INC NPI	Title : SREW HOLE	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 0.1
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 48 of 65	

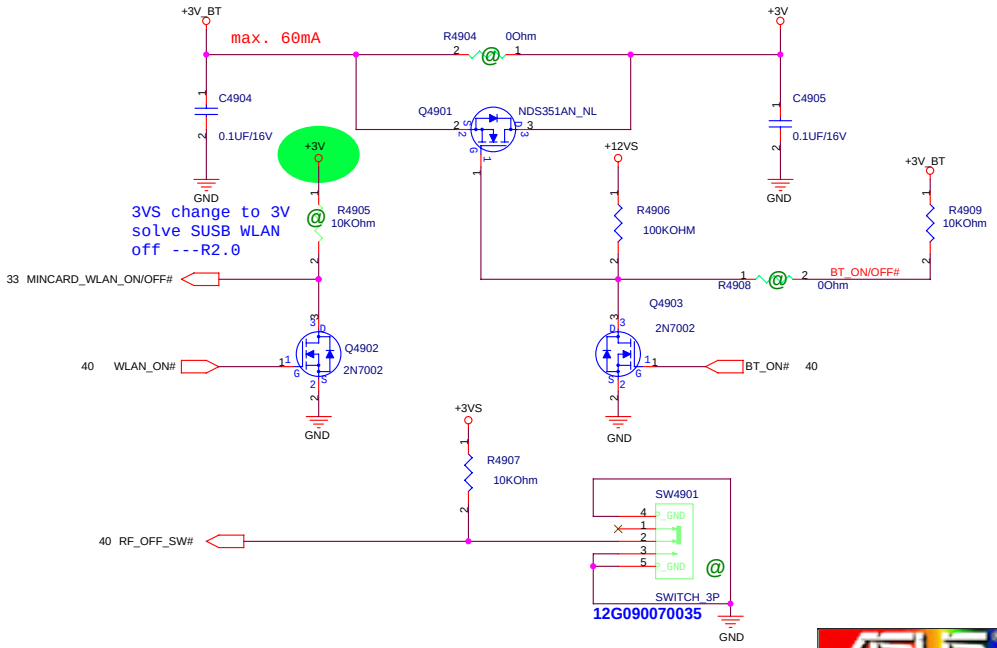
TPM



BLUETOOTH



WLAN/BT ON/OFF Control



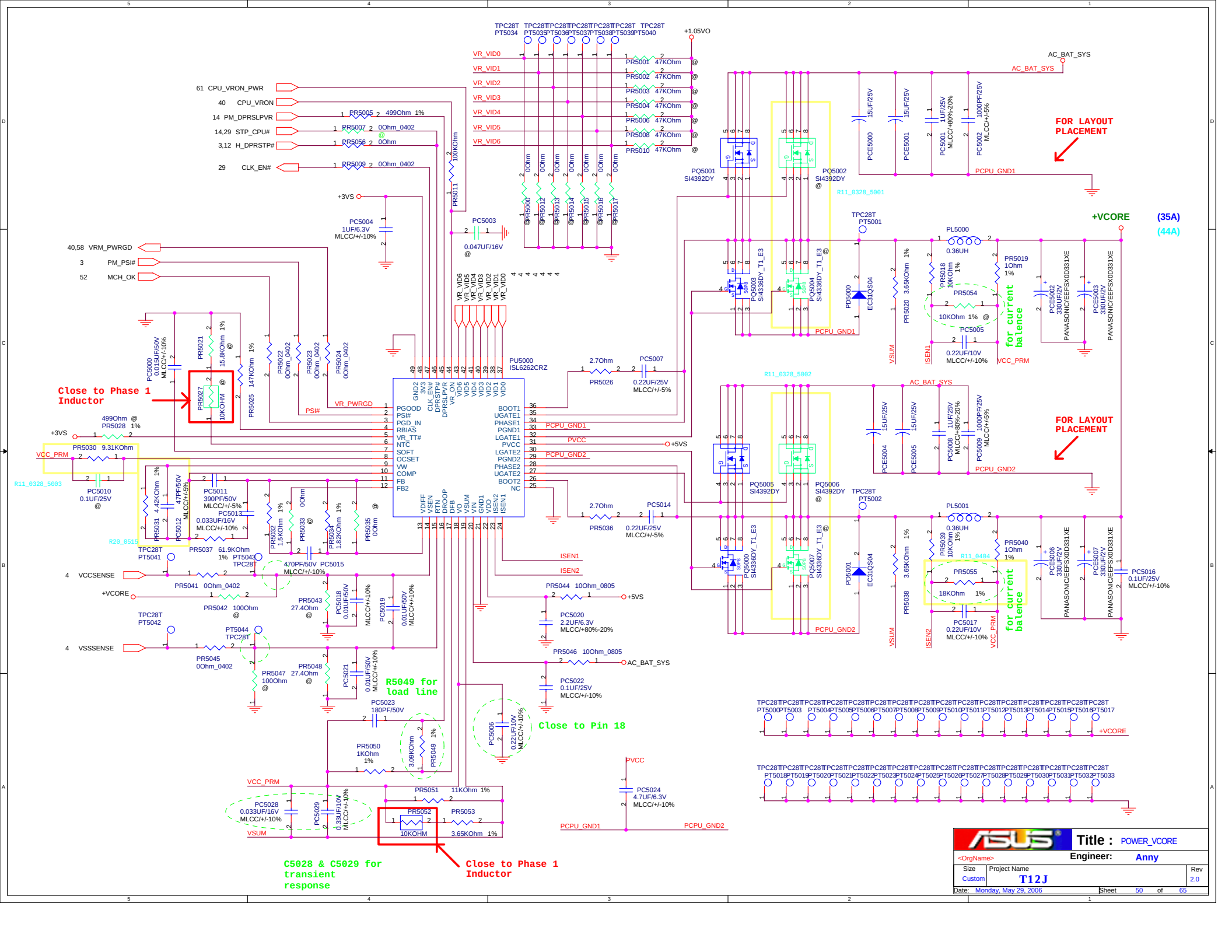
ASUSTek COMPUTER INC NPI

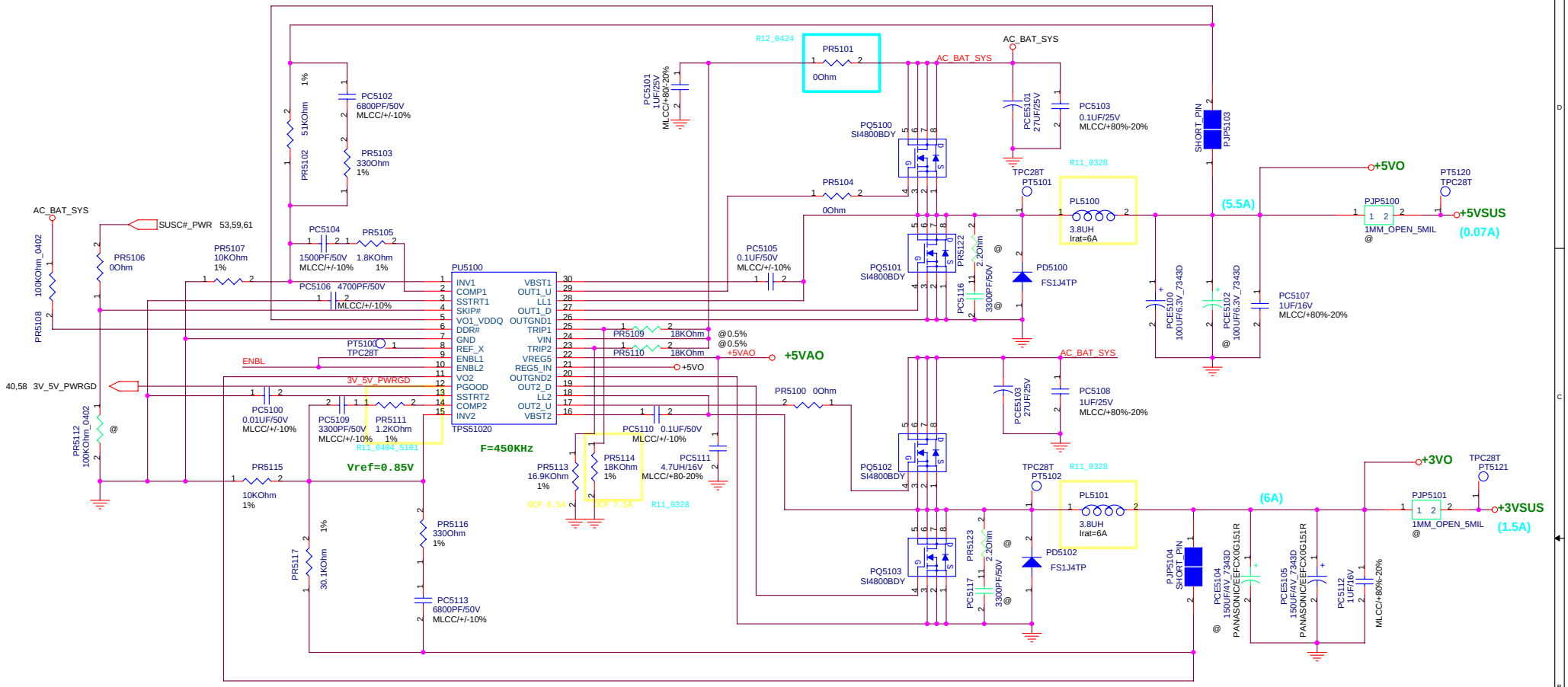
Title : BLUETOOTH&TPM

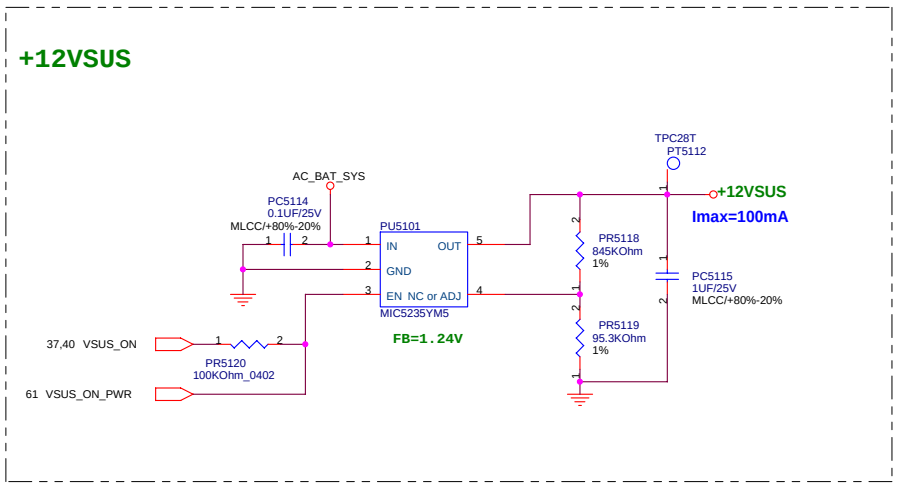
Engineer: Arthur & Bruce Chen

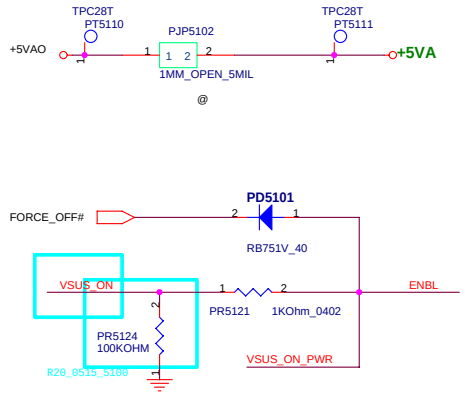
Size	Project Name	Rev
Custom	T12J	0.1
	P/N <OrgAddr2>	

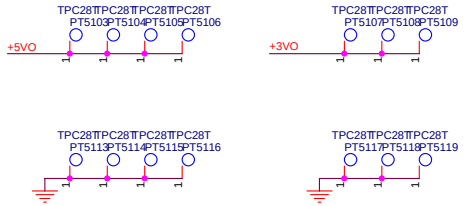
Date: Monday, May 29, 2006 Sheet 49 of 65


Close to Phase 1 Inductor
FOR LAYOUT PLACEMENT
FOR LAYOUT PLACEMENT
for current balence
for current balence
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
+VCORE (35A) (44A)
PU5000 ISL6262CRZ
Title : POWER_VCORE
Engineer: Anny
Project Name T12J
Rev 2.0
Date: Monday, May 29, 2006
Sheet 50 of 65









ASUS

Title : POWER_SYSTEM

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	T12J	2.0

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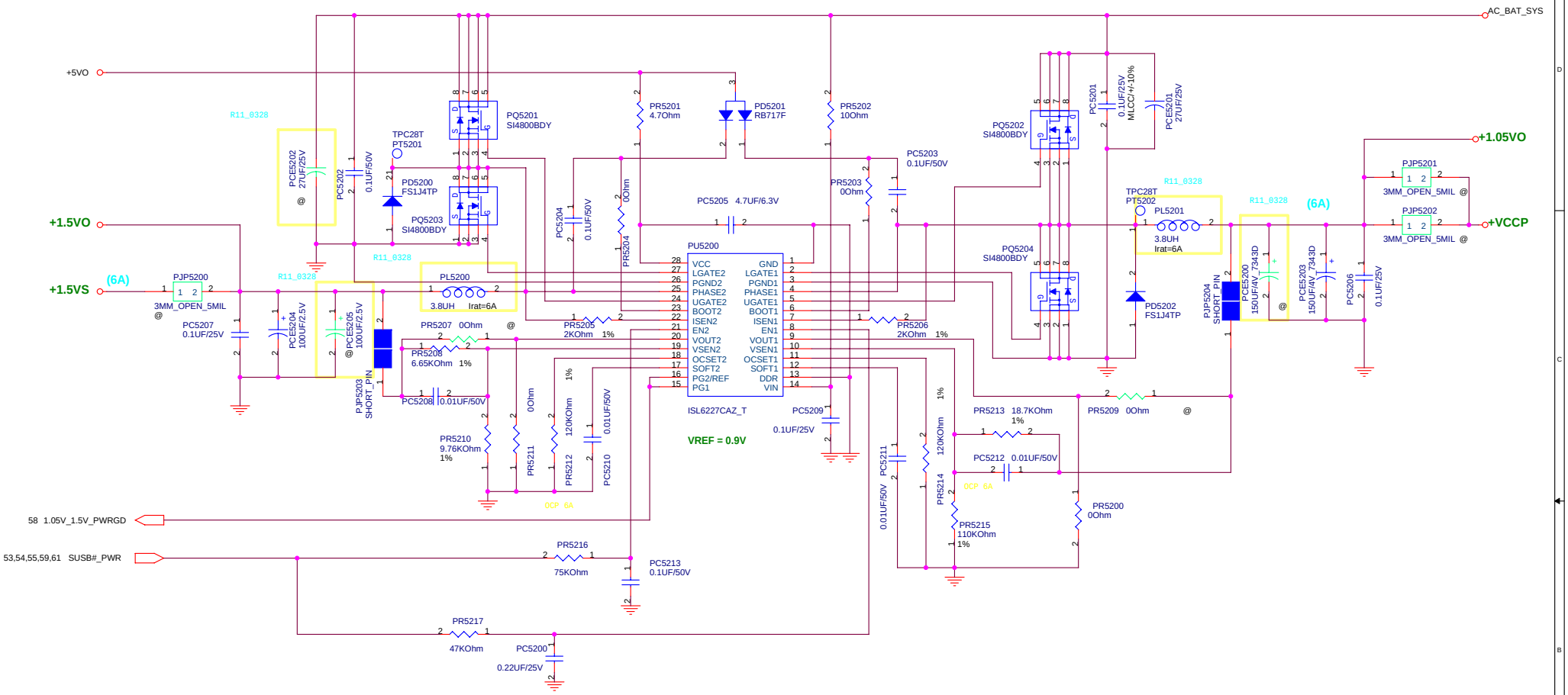
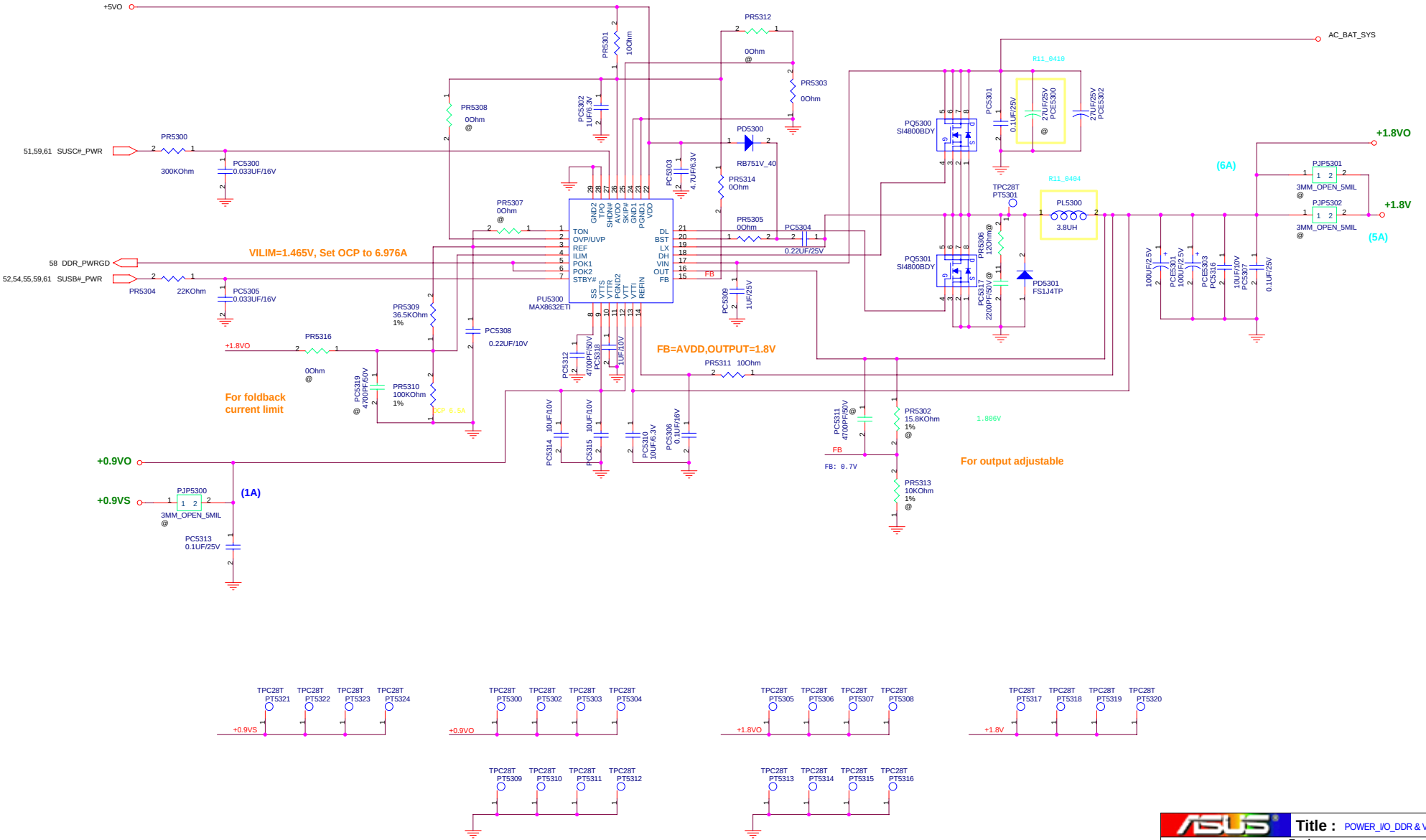
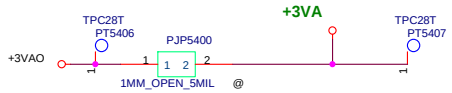


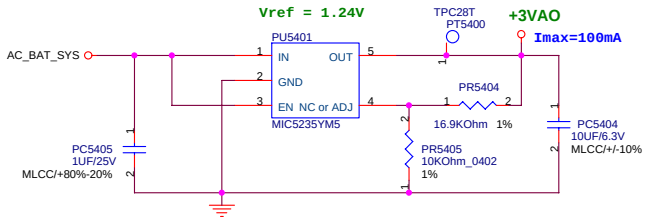
Title : POWER_I/O_1.5VS & 1.05VS		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 52 of 65	



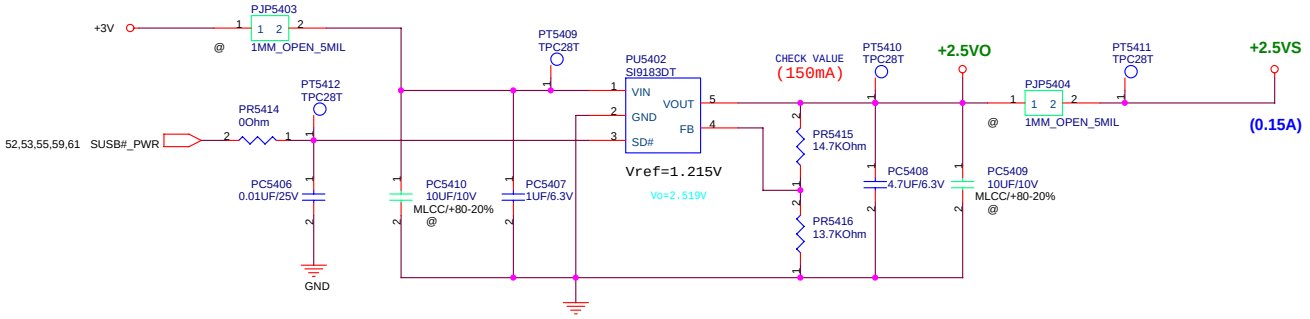
ASUS	Title :	POWER_I/O_DDR & VTT
<OrgName>	Engineer:	Anny
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 53 of 65	

+3VA0

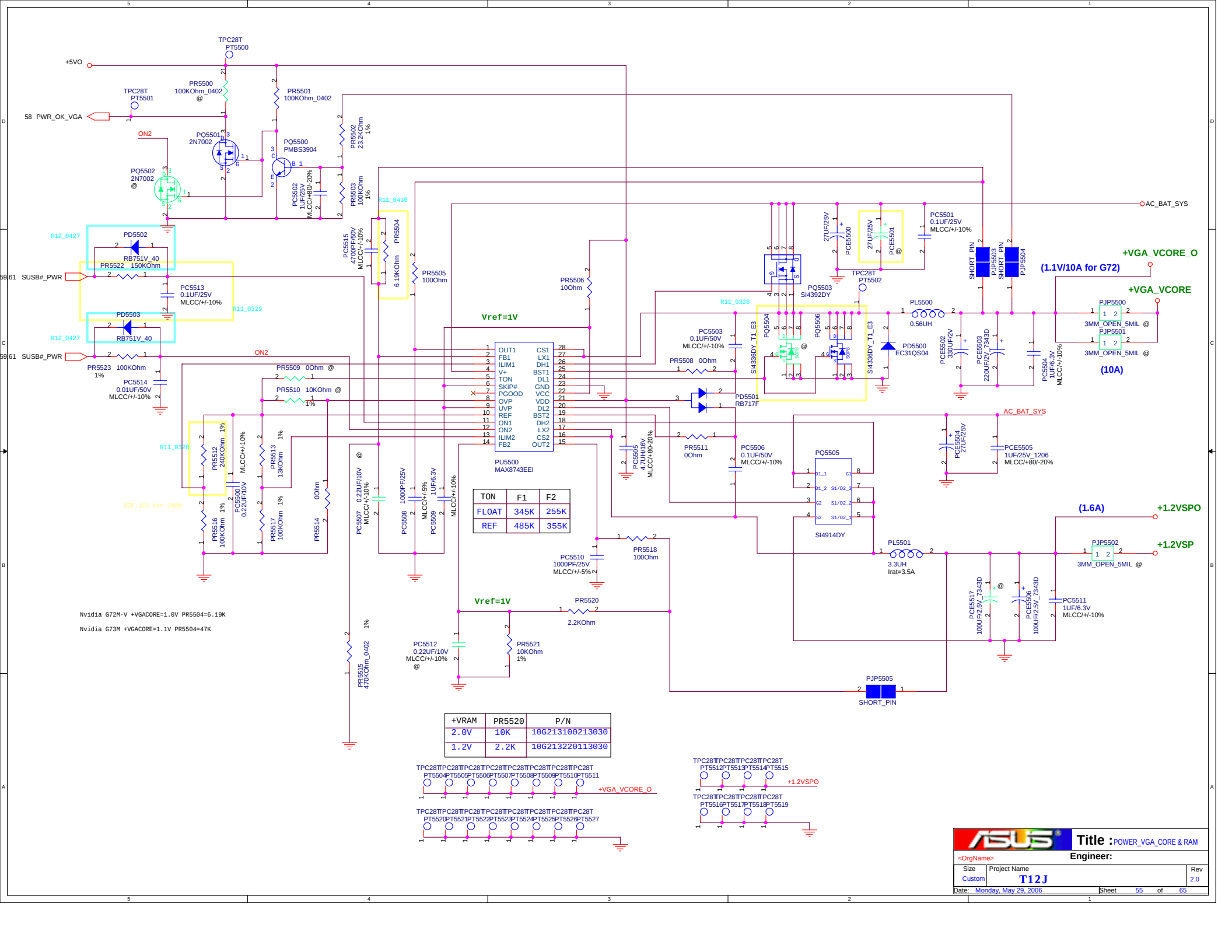


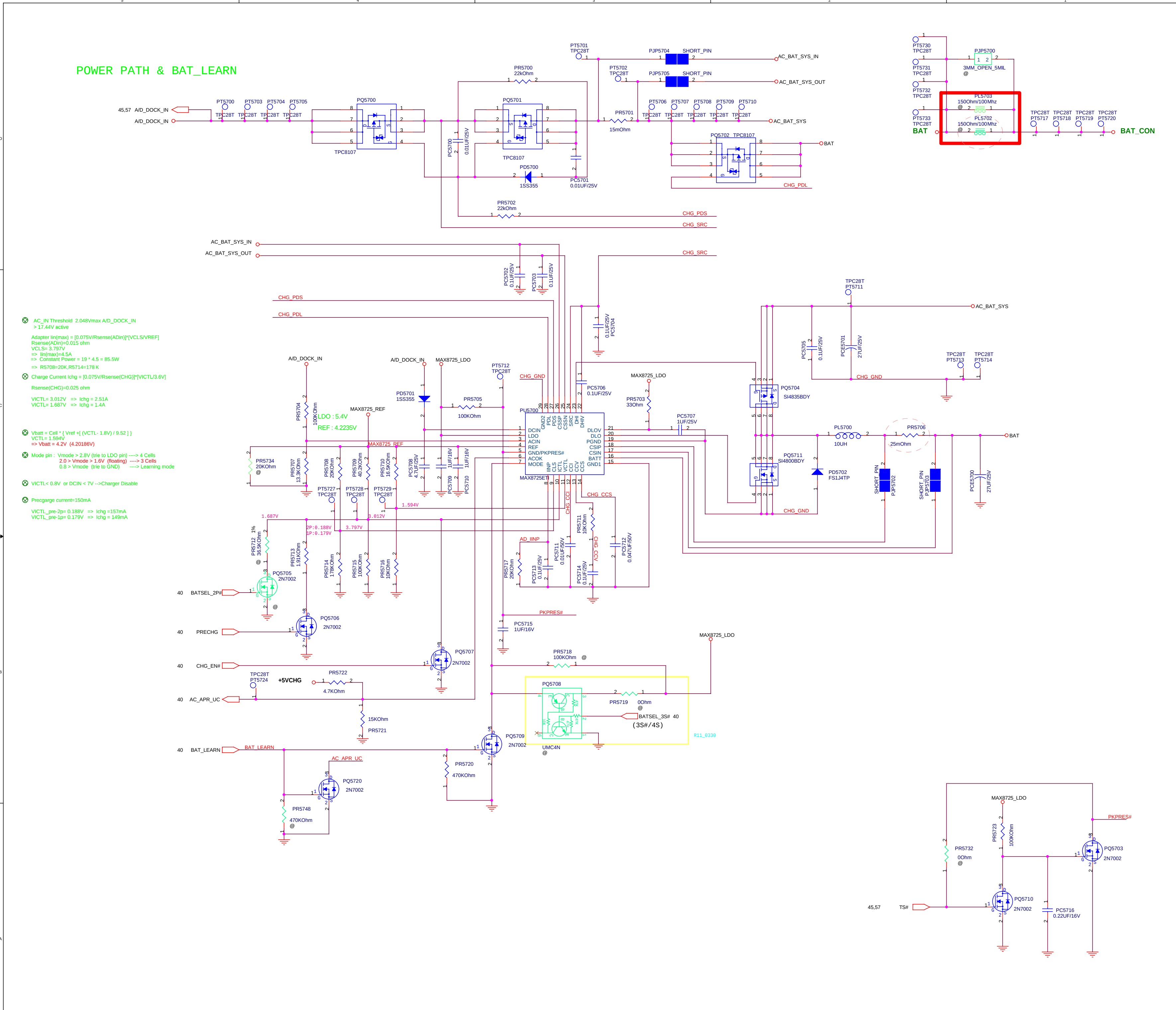


+2.5VS



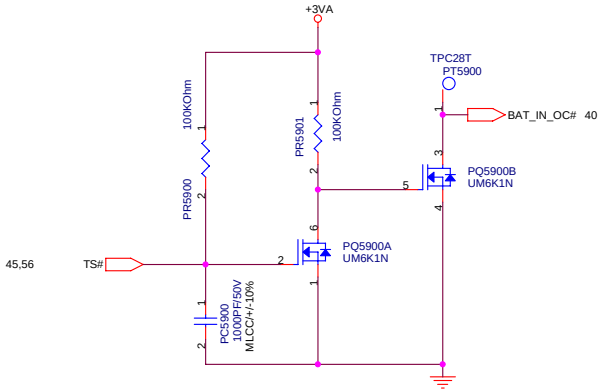
ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 54 of 65	


+5VO
58 PWR_OK_VGA
ON2
59,61 SUSB#_PWR
AC_BAT_SYS
Vref=1V
PU5500
MAX8743EEI
PQ5503
SI4392DY
PQ5505
SI4914DY
PD5500
EC31QS04
PD5501
RB717F
PD5502
RB751V_40
PD5503
RB751V_40
+VGA_VCORE_O
(1.1V/10A for G72)
+VGA_VCORE
(10A)
+1.2VSPO
(1.6A)
+1.2VSP
PJP5505
SHORT_PIN
OCP:16A for 240K
Nvidia G72M-V +VGACORE=1.0V PR5504=6.19K
Nvidia G73M +VGACORE=1.1V PR5504=47K
+VRAM | PR5520 | P/N
2.0V | 10K | 10G213100213030
1.2V | 2.2K | 10G213220113030
TON | F1 | F2
FLOAT | 345K | 255K
REF | 485K | 355K
Title : POWER_VGA_CORE & RAM
<OrgName>
Engineer:
Size Custom
Project Name T12J
Rev 2.0
Date: Monday, May 29, 2006
Sheet 55 of 65

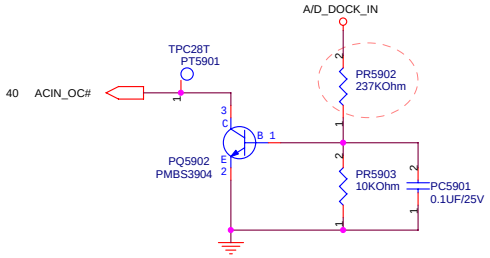


Title :	POWER_CHARGER
<OrgName>	Engineer: Anny
Size: Custom	Project Name: T12J
Rev	2.0
Date: Monday, May 29, 2006	Sheet 56 of 65

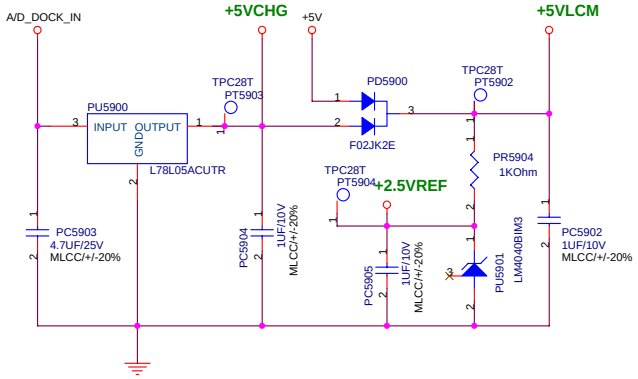
BATTERY IN DETECT



ADAPTER IN DETECT

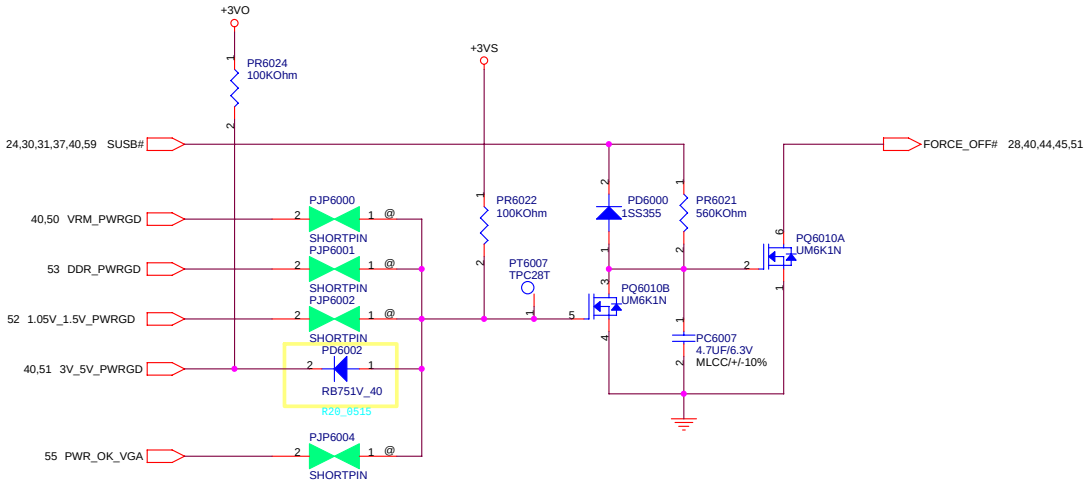


+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 57 of 65	

POWER GOOD DETECTER



TPC28T PT6003 1 VRM_PWRGD

TPC28T PT6004 1 DDR_PWRGD

TPC28T PT6005 1 3V_5V_PWRGD

TPC28T PT6006 1 1.05V_1.5V_PWRGD

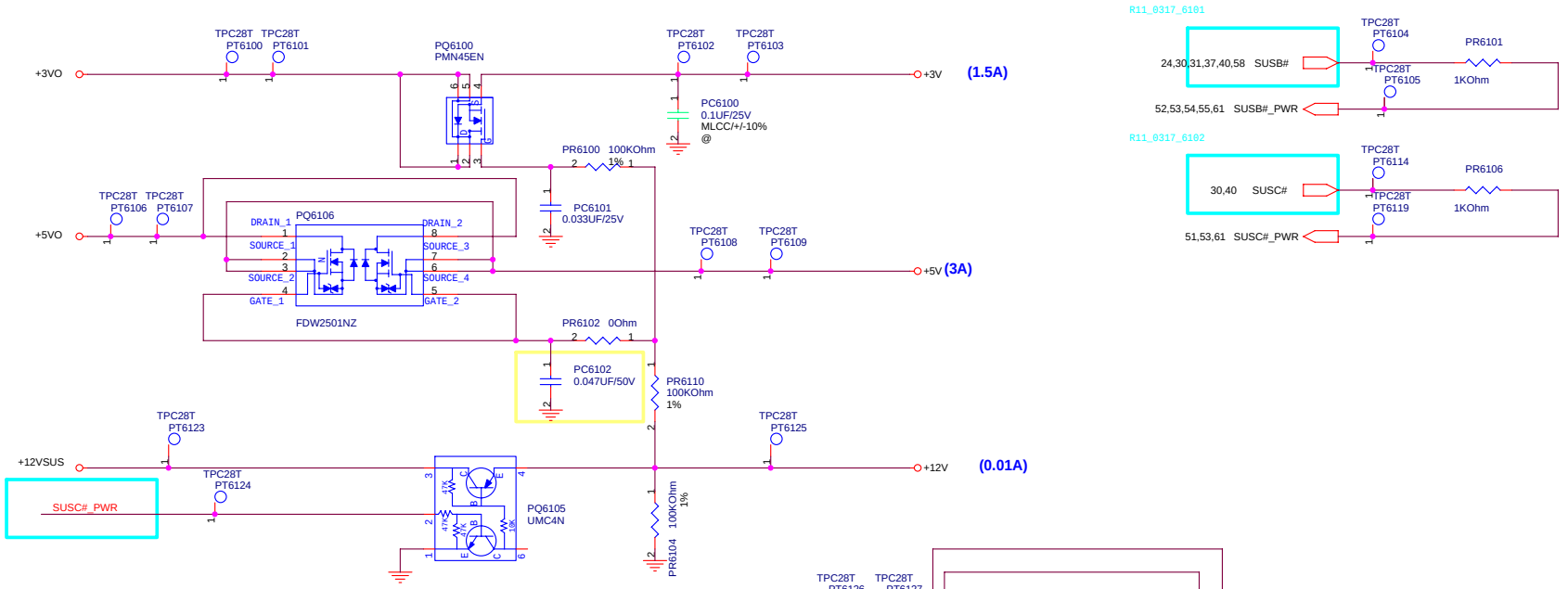
TPC28T PT6008 1 PWR_OK_VGA

R12_0424

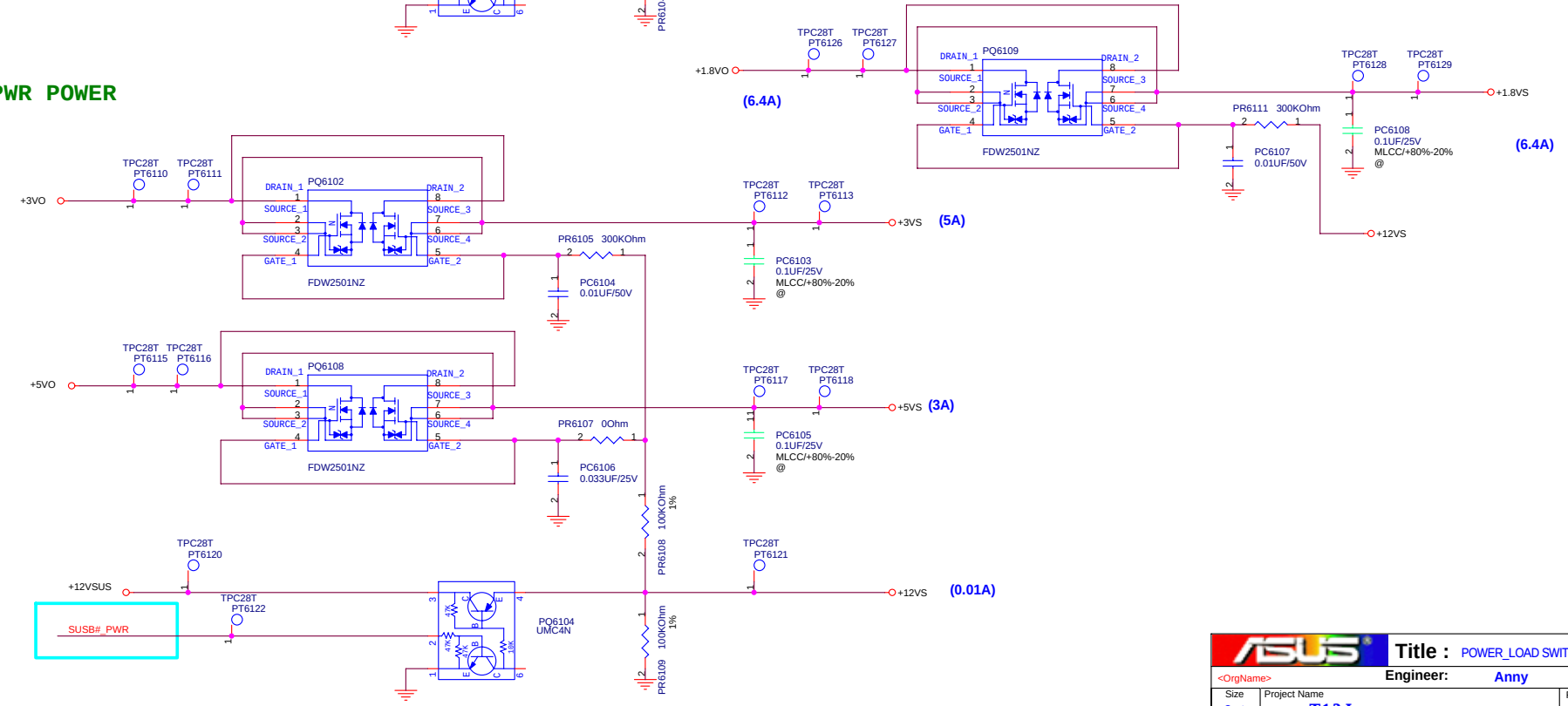
Title : POWER_PROTECT		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 58 of 65	

(6.5A)

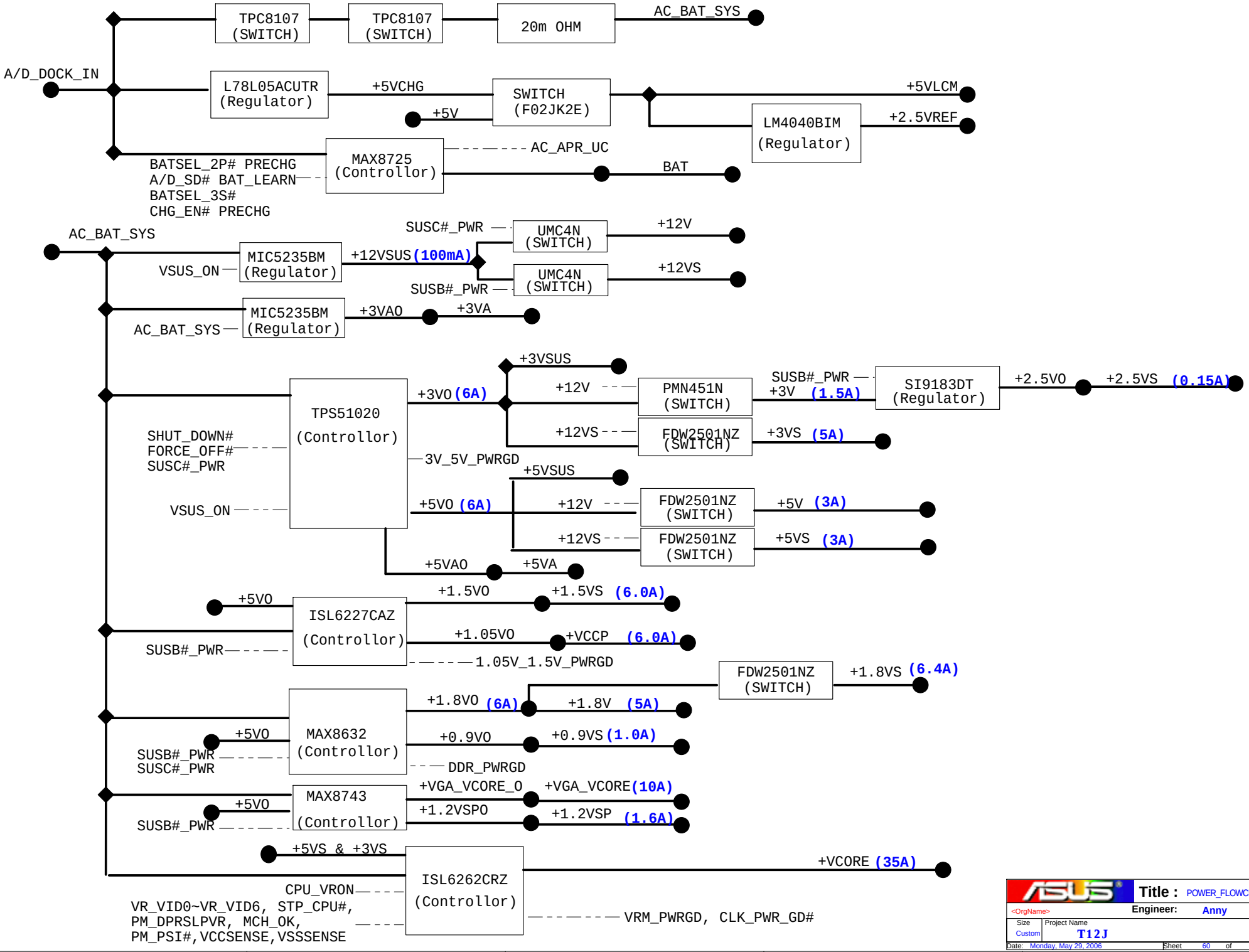
SUSC#_PWR POWER



SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 59 of 65	



Title : POWER_FLOWCHART		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 60 of 65	

AC_BAT_SYS — AC_BAT_SYS 24,45,50,51,52,53,54,55,56

+3VA — +3VA 12,24,28,30,39,40,44,54,57

+5VA — +5VA 51

+5VO — +5VO 51,52,53,55,59

+3VO — +3VO 51,52,58,59

+3VSUS — +3VSUS 13,14,15,31,37,51

+5VSUS — +5VSUS 15,44,51

+3V — +3V 30,32,33,44,49,54,59

+3VS — +3VS 6,10,13,14,15,16,17,19,21,22,24,25,26,27,28,29,30,33,34,35,36,37,38,39,40,46,47,49,50,52,58,59

+12VSUS — +12VSUS 51,59

+12V — +12V 30,42,59

+12VS — +12VS 24,36,39,49,59

+5V — +5V 24,30,42,44,57,59

+5VS — +5VS 14,15,25,28,30,38,39,40,44,47,50,59

+2.5VO — +2.5VO 54

+2.5VS — +2.5VS 10,21,26,30,54

+1.8VO — +1.8VO 53,59

+1.8V — +1.8V 6,9,16,17,30,53

+VCCP — +VCCP 4,5,7,9,10,12,15,30,52

+VCCP_AGTL+ — +VCCP_AGTL+ 3,4

+VCCP_GMCH — +VCCP_GMCH

+VCCP_ICH — +VCCP_ICH

+0.9VS — +0.9VS 18,23,30,53

BAT — BAT 56

+5VCHG — +5VCHG 56,57

+5VLCM — +5VLCM 57

+2.5VREF — +2.5VREF 57

+VCORE — +VCORE 4,28,50

BAT_CON — BAT_CON 45,56

FOR POWER TEST

+3VA

PJP6300 — SGL_JUMP @ — 1 — 1 2 — 2 — CPU_VRON_PWR 50

PJP6301 — SGL_JUMP @ — 1 — 1 2 — 2 — SUSB#_PWR — SUSB#_PWR 52,53,54,55,59

PJP6302 — SGL_JUMP @ — 1 — 1 2 — 2 — SUSC#_PWR — SUSC#_PWR 51,53,59

PJP6303 — SGL_JUMP @ — 1 — 1 2 — 2 — VSUS_ON_PWR — VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 61 of 65	

Rev	Date	Description
1.0	10/04/05	1. Initial release.
1.1	12/26/05	

Rev	Date	Description

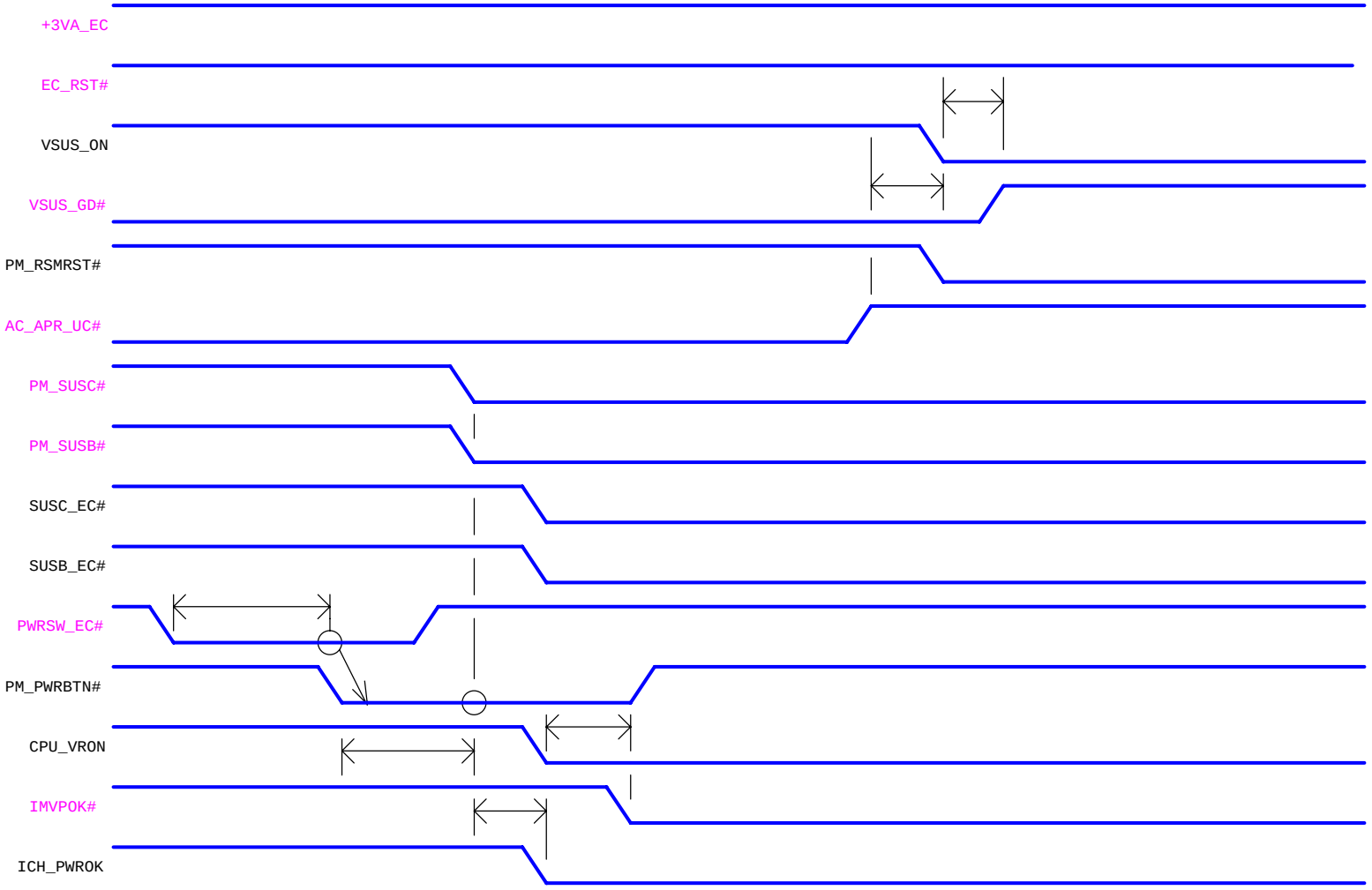
ASUSTek COMPUTER INC NPI

Title : History

Engineer: *Arthur & Bruce Chen*

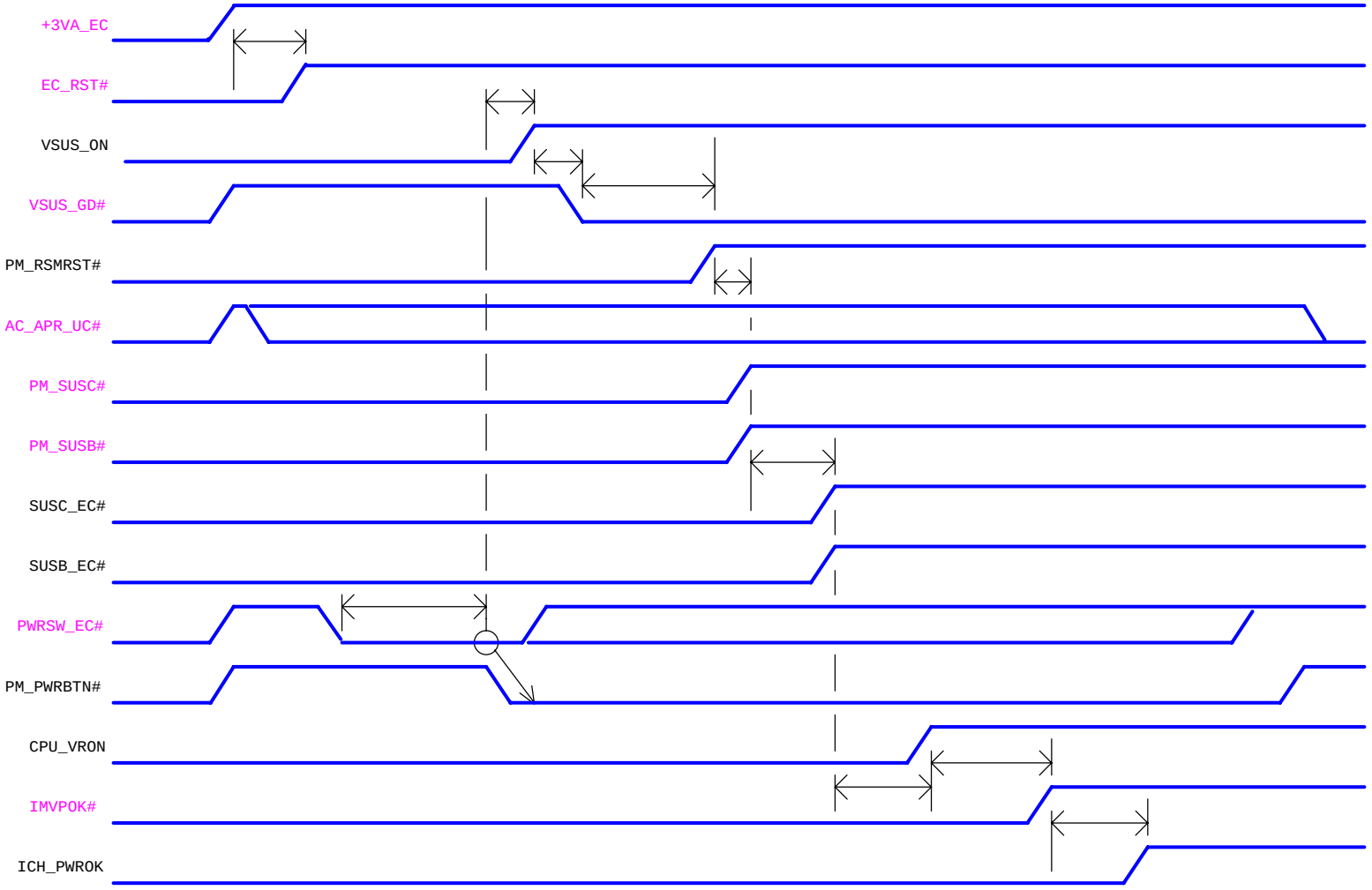
Size	Project Name	Rev
Custom	T12J	0.1
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 62 of 65



POWER OFF TIMING

ASUSTek COMPUTER INC NPI	Title : Power OFF		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 0.1
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 63 of 65		



POWER ON TIMING

ASUSTek COMPUTER INC NPI	Title : Power ON		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 0.1
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 64 of 65		

R1.0

Item	Before	After	Reason	Owner	Date

R1.1

Item	Before	After	Reason	Owner	Date
R11_0317_6001	Pull hi to +5VA	Pull hi to +3VA	To meet EC power request		2006.03.17
R11_0317_5401	IC:CM8562GISTR	IC:SI9183DT	Cost down		2006.03.17
R11_0317_6101	SUSB_ON	SUSB#	For EE request		2006.03.17
R11_0317_6102	SUSC_ON	SUSC#	For EE request		2006.03.17
R11_0317_5701	PD5705: 1SS355(07G001007100)	PD5705: RB751V_40(07G004020710)	Down Vf		2006.03.17
R11_0322_5702	Error fumction	Del Error fumction and add PD5707			2006.03.22
R11_0328_5001 ~ R11_0328_5003	mount: PQ5002, PQ5004, PQ5006, PQ5007 PR5030 16K	unmount: PQ5002, PQ5004, PQ5006, PQ5007 PR5030 change to 9.31K to tune OCP to 47A	Cost down		2006.03.28
R11_0404_5101	2.7K	1.2K	避免磁場干擾		2006.03.28
R12_0413_57	AD error and pwr limit function	DEL AD error and pwr limit function	Cost down		2006.04.24
R12_0413_60	batteru OVP protect function	DEL batteru OVP protect function	Cost down		2006.04.24
R12_0427		Add PD5502 and PD5503	Add PD5502 and PD5503 to avoid on1 voltage drop slow when disable.		

R2.0

Item	Before	After	Reason	Owner	Date
R20_0515_5100		add PR5124	Pull ground to avoid vsus_on is float.		2006.05.15

ASUS

Title : POWER_PIC

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

Date: Monday, May 29, 2006 Sheet 65 of 65