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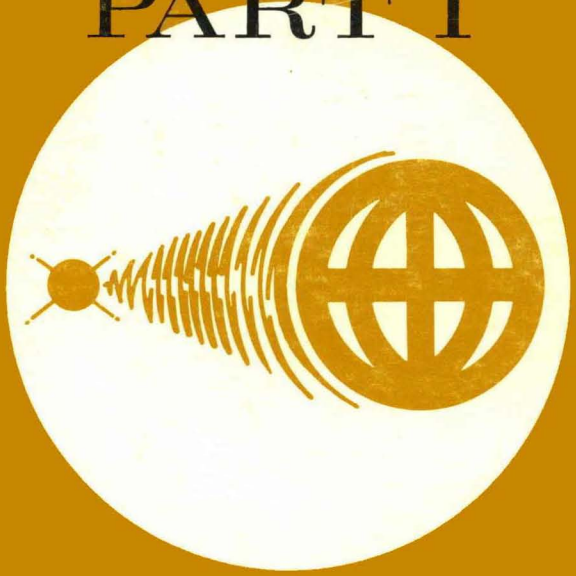
TEXAS INSTRUMENTS INCORPORATED • SEMICONDUCTOR-COMPONENTS DIVISION

Communications HANDBOOK PART I



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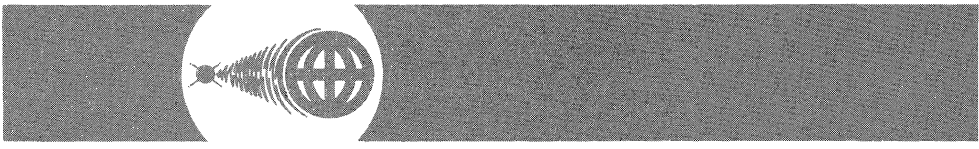

Communications Handbook

PART I

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SEMICONDUCTOR-COMPONENTS DIVISION
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COMMUNICATIONS HANDBOOK

SC-6219

Preface

Communications Handbook, Parts I and II, are the first two paperback volumes in the Texas Instruments Microlibrary. The objective of the Handbook is to give the communications circuit designer as much useful and current information as can be supplied in a work of 400 pages. Obviously, we cannot hope to present comprehensive coverage of the vast communications field; instead, we have tried to include material that has proved to be of current interest, as evidenced by reactions to papers delivered at Texas Instruments technical seminars, acceptance of our monthly Technical Newsletter, and requests from customers for special information.

New editions of the Handbook will be published periodically, to reflect improvements in design techniques and devices.

Please send any queries regarding material in this Handbook to the individual author, in care of Texas Instruments Incorporated, Post Office Box 5012, Dallas, Texas 75222.

Texas Instruments Incorporated
Semiconductor-Components Division

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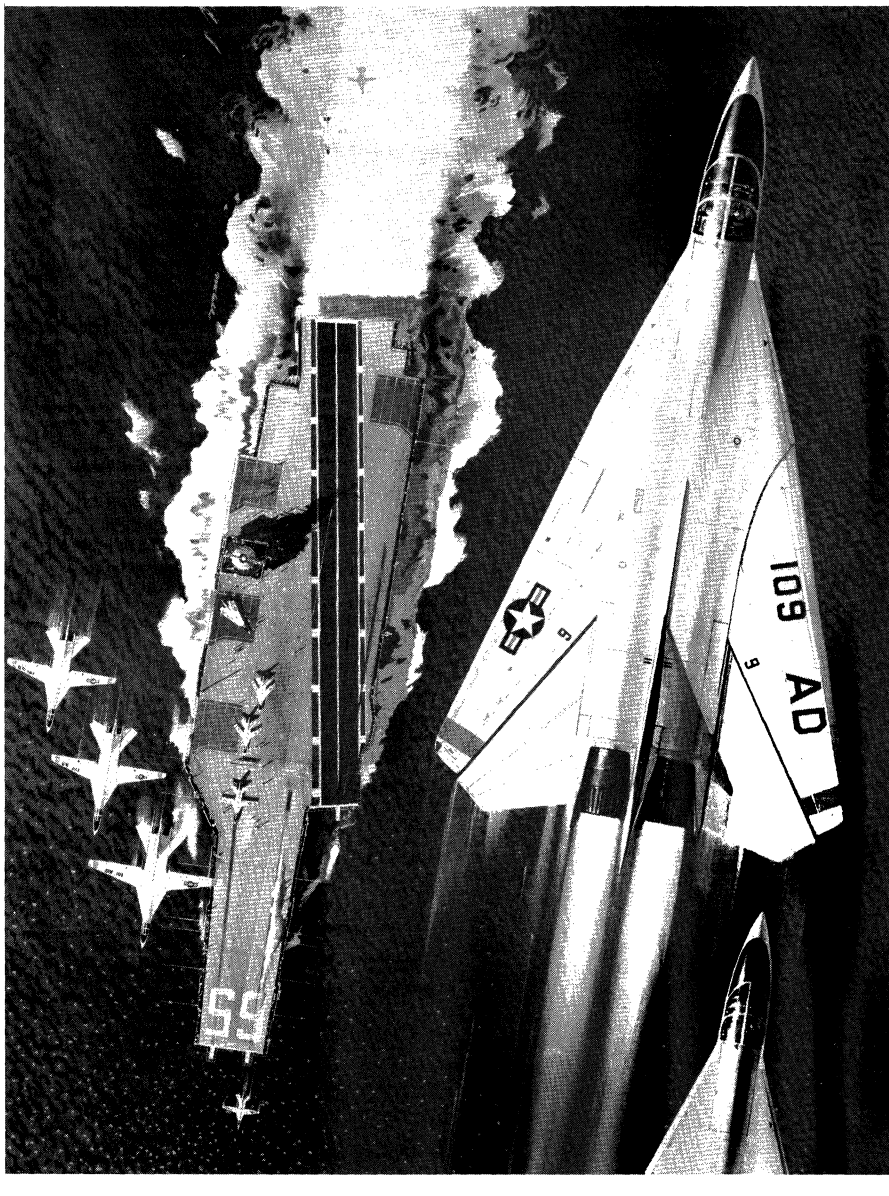


Artist's conception of F-111 supersonic fighters engaged in carrier operations. Built by General Dynamics, a fully armed F-111 is projected as carrying more than 7000 TI networks and several thousand TI discrete transistors.

DALCOM COMMUNICATIONS TRANSISTORS — APPLICATIONS CHART

Small Signal

Large Signal

FREQUENCY RANGE	RF AMPLIFIERS	IF AMPLIFIERS	MIXERS & CONVERTERS	LOW-LEVEL OSCILLATORS	HIGH-LEVEL OSCILLATORS	LOW-POWER AUDIO/VIDEO AMPLIFIERS	POWER AMPLIFIERS ONE WATT OR LESS	POWER AMPLIFIERS LESS THAN FIVE WATTS	POWER AMPLIFIERS GREATER THAN FIVE WATTS
0-20 KC						2N780 (Si Mesa) 2N2861/62 (Si Planar PNP) USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) USA2N760A (Si Mesa) 2N650A-2N652A (Alloy) 2N524-2N527 (Alloy) 2N1273/74 (Alloy) 2N1370-2N1383 (Alloy) 2N2500 (Si FET) 2N1149-2N1153 (Grown) 2N332-2N338 (Grown) 2N1566A/2N736A (Si Mesa)	2N243/44 (Grown Diff Si) 2N342B (Grown Diff Si) 2N343B (Grown Diff Si)	2N497/98 (Diff Si) 2N656/57 (Diff Si) 2N1038-2N1041 (Alloy) 2N2564-2N2567 (Alloy)	2N1046 (Alloy) 2N250/51 (Alloy) 2N456A-2N458A (Alloy) 2N1021/22 (Alloy) 2N511-2N514B (Alloy) 2N2552/2N1045 (Alloy) 2N389 (Diff Si) 2N424 (Diff Si) 2N1047-2N1050 (Diff Si)
20 KC TO 2 MC	USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) TI363 (Alloy) 2N2188 Series (Alloy) 2N332-338 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) TI363/364 (Alloy) 2N1302-2N1309 (Alloy) 2N2188 Series (Alloy) 2N332-2N338 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) TI363/64 (Alloy) 2N2188 Series (Alloy) 2N332-2N338 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	TI363/64 (Alloy) 2N1302-2N1305 (Alloy) 2N2188 Series (Alloy) 2N332-2N338 (Grown) 2N780 (Si Mesa) USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	2N696 (Si Planar) 2N697 (Si Planar) 2N698/99 (Si Planar)	2N697 (Si Mesa) 2N780 (Si Mesa) USA2N929/USA2N930 (Si Planar) 2N2861/62 (Si Planar PNP) 2N696 (Si Mesa) 2N698/99 (Si Mesa) 2N524-2N527 (Alloy) 2N650A-2N652A (Alloy) 2N332-2N338 (Grown) 2N1149-2N1153 (Grown) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	2N1141/42/43 (Ge Mesa) 2N2863 (Si Planar) 2N2864 (Si Planar)	2N1131/32 (Si Planar) 2N696/97/98/99 (Si Planar) 2N1613-2N1711 (Si Planar) 2N1890 (Si Planar) 2N1893 (Si Planar) 2N1899 (Si Planar) 2N497/98 (Diff Si) 2N656/57 (Diff Si) 2N2863 (Si Planar) 2N2864 (Si Planar)	2N1046/2N1908 (Alloy Diff) 2N389 (Diff Si) 2N424 (Diff Si) 2N1047-2N1050 (Diff Si)
2-10 MC	2N1141/42/43 (Ge Mesa) USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) 2N2188 Series (Alloy) 3N34/35 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	2N1141/42/43 (Ge Mesa) USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) 2N2188 Series (Alloy) 3N34/35 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	2N1141/42/43 (Ge Mesa) USA2N929/USA2N930 (Si Planar) 2N2188 Series (Alloy) 3N34/35 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	2N1141/42/43 (Ge Mesa) 2N1302-2N1309 (Alloy) 2N2188 Series (Alloy) 3N34/35 (Grown) 2N780 (Si Mesa) USA2N929/USA2N930 (Si Planar) 2N2586 (Si Planar) 2N1566A/2N736A (Si Mesa)	2N1141/42/43 (Ge Mesa) 2N696 (Si Planar) 2N697 (Si Planar) 2N698/99 (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N697 (Si Planar) 2N696 (Si Planar) 2N780 (Si Mesa) 2N2861/62 (Si Planar PNP) USA2N929/USA2N930 (Si Planar) 2N698/99 (Si Planar) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa)	2N1141/42/43 (Ge Mesa) 2N1714-2N1717 (Si Mesa) 2N2863 (Si Planar) 2N2864 (Si Planar) 2N2987-2N2994 (Si Planar)	2N1131/32 (Si Planar) 2N1714-2N1721 (Si Planar) 2N1722-2N1724 (Si Mesa) 2N1890/93/99 (Si Planar) 2N1936/37 (Si Mesa) 2N2150/51 (Si Mesa) 2N2863/64 (Si Planar) 2N2983-2N2986 (Si Mesa) 2N2987-2N2994 (Si Planar) TI-816 (Si Planar)	2N1046/2N1908 (Alloy Diff) 2N1047B-2N1050B (Si Mesa) 2N1722-2N1724 (Si Mesa) 2N1723-2N1725 (Si Mesa) 2N1936/37 (Si Mesa) 2N2150/51 (Si Mesa) 2N2983-2N2986 (Si Mesa)
10-30 MC	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) USA2N929/USA2N930 (Si Planar) 2N743/44 (Si Planar) 2N706A (Si Planar) USA2N760A (Si Mesa) 2N780 (Si Mesa) 2N2411/2N2412 (Si Planar) 2N2188 Series (Alloy) 3N34/35 (Grown) TIX3032 (Ge Planar) 2N2865 (Si Planar) 2N2586 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) 2N2861/62 (Si Planar PNP) USA2N929/USA2N930 (Si Planar) 2N744/43 (Si Planar) 2N706A (Si Planar) 2N2188 Series (Alloy) 3N34/35 (Grown) TIX3032 (Ge Planar) USA2N760(A) (Si Mesa) 2N2865 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) USA2N929/USA2N930 (Si Planar) 2N2188 Series (Alloy) 3N34/35 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) TIX3032 (Ge Planar) 2N2586 (Si Planar) 2N2865 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) 2N743/44 (Si Planar) 2N2188 Series (Alloy) 3N34/35 (Grown) USA2N929/USA2N930 (Si Planar) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N2586 (Si Planar) TIX3032 (Ge Planar) 2N2865 (Si Planar)	2N1142/43 (Ge Mesa) 2N698/99 (Si Planar) 2N706A (Si Planar) 2N696/97 (Si Planar) 2N743/44 (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N698/99 (Si Planar) 2N2861/62 (Si Planar PNP) 2N696/97 (Si Planar) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa) 2N2217-2N2222 (Si Planar) 2N3570/71/72 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N743/44 (Si Planar) 2N706A (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar)	2N1131/32 (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar) TI 816 (Si Planar)	2N2876 (Si Planar)*
30-70 MC	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N743/44 (Si Planar) 2N918 (Si Planar) 2N2191 (Alloy) 3N35 (Grown) TIX3032 (Ge Planar) USA2N760A (Si Mesa) 2N2865 (Si Planar) 2N3570/71/72 (Si Planar)	2N2996/97/98 (Ge Mesa) 2N1141/42/43 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N3570/71/72 (Si Planar) TIX3032 (Ge Planar) 2N2861/62 (Si Planar PNP) 2N918 (Si Planar) 2N2189 (Alloy) 2N2191 (Alloy) 3N35 (Grown) 2N2865 (Si Planar)	2N2996/97/98 (Ge Mesa) 2N1141/42/43 (Ge Mesa) 2N918 (Si Planar) TIX3032 (Ge Planar) 2N2189 (Alloy) 2N2191 (Alloy) 3N35 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N3570/71/72 (Si Planar) 2N2865 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) 2N743/44 (Si Planar) 2N2188 Series (Alloy) 3N35 (Grown) 2N780 (Si Mesa) USA2N760A (Si Mesa) 2N1566A/2N736A (Si Mesa) 2N2865 (Si Planar) 2N918 (Si Planar) 2N3570/71/72 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N706A (Si Planar) 2N743/44 (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar) 2N3570/71/72 (Si Planar)	2N2861/62 (Si Planar PNP) 2N743/44 (Si Planar) 2N2217-2N2222 (Si Planar) 2N3570/71/72 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N743/44 (Si Planar) 2N706A (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar) 2N2217-2N2219 (Si Planar) 2N2883/84 (Si Planar)	2N2863 (Si Planar) 2N2864 (Si Planar) 2N2884 (Si Planar)	2N2876 (Si Planar) *
70-400 MC	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N918 (Si Planar) 2N2865 (Si Planar) 2N3570/71/72 (Si Planar) TIX3024 (Ge Mesa)	2N1141/42/43 (Ge Mesa) 2N2996/97/98 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N918 (Si Planar) 2N2865 (Si Planar) 2N3570/71/72 (Si Planar) TIX3024 (Ge Mesa)	2N2996/97/98 (Ge Mesa) 2N1141/42/43 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N918 (Si Planar) 2N818 (Si Planar) 2N3570/71/72 (Si Planar) TIX3024 (Ge Mesa)	2N1141/42/43 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N2996/97/98 (Ge Mesa) 2N918 (Si Planar) TIXS09 (Si Planar) TIXS10 (Si Planar) 2N2865 (Si Planar) 2N3570/71/72 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N743/44 (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar) 2N3570 (Si Planar) TIXS09 (Si Planar) TIXS10 (Si Planar) 2N2883/84 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N743/44 (Si Planar) 2N2861/62 (Si Planar PNP) 2N2217-2N2222 (Si Planar) 2N3570/71/72 (Si Planar) TIXS09 (Si Planar) TIXS10 (Si Planar)	2N1141/42/43 (Ge Mesa) 2N743/44 (Si Planar) 2N2863 (Si Planar) 2N2864 (Si Planar) 2N2217-2N2219 (Si Planar) TIXS09 (Si Planar) TIXS10 (Si Planar) 2N2883/84 (Si Planar)	2N2863 (Si Planar) 2N2864 (Si Planar) 2N2884 (Si Planar) 2N2876 (Si Planar) * TIX3016A (Si Planar)	
400 MC TO 3 GC	2N2998/99 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N2865 (Si Planar) TIX3024 (Ge Mesa) 2N918 (Si Planar) 2N3570 (Si Planar)	2N2998/99 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N2865 (Si Planar) TIX3024 (Ge Mesa) 2N918 (Si Planar) 2N3570 (Si Planar)	2N2998/99 (Ge Mesa) 2N2415/16 (Ge Mesa) 2N2865 (Si Planar) TIX3024 (Ge Mesa) 2N918 (Si Planar) 2N3570 (Si Planar)	2N2998/99 (Ge Mesa) 2N3570 (Si Planar) TIX3016A (Si Planar) TIXS09 (Si Planar) TIXS10 (Si Planar)	2N3570 (Si Planar) TIX3016A (Si Planar) TIXS09 (Si Planar) TIXS10 (Si Planar) TIXS12 (Si Planar) TIXS13 (Si Planar)	2N3570 (Si Planar) TIX3016A (Si Planar) TIXS09 (Si Planar) TIXS10 (Si Planar) TIXS12 (Si Planar) TIXS13 (Si Planar)	TIX3016A (Si Planar) TIXS12 (Si Planar) TIXS13 (Si Planar)	TIX3016A (Si Planar) TIXS12 (Si Planar)	

*To be announced March 1965

1

New Communications Devices

by Ted Small

This chapter is designed to familiarize the communications equipment designer and manufacturer with the newer linear communications devices recently announced by Texas Instruments.

We have included information that will supplement the basic data sheet information; in some cases, we have summarized important major device characteristics in tabular form. If we can provide any additional information concerning these devices, or if you have special applications problems, please contact your nearest TI sales office.

SUMMARY OF HIGH-FREQUENCY SMALL-SIGNAL AMPLIFIER CHARACTERISTICS

Tables 1 and 2 and Fig. 1 provide a graphic summary of our transistor capabilities.

SILICON SMALL-SIGNAL TRANSISTORS

2N3570 and TIX3016A are silicon planar epitaxial transistors having a seven-finger interdigitated geometry.

They have higher frequency capabilities than any other silicon unit presently on the market. Their power capability will enable equipment manufacturers to use these solid-state devices as low-power klystron replacements; they will possibly open a new area such as airborne microwave equipment, where size and weight are important.

We have built an eight-stage experimental amplifier using the TIX3016A. It has a bandwidth of 500 mc to 1465 mc, 30-db gain, and a noise figure of approximately 8.0 db. We have also demonstrated the TIX3016A operating at a 2.3-Gc fundamental and driving an X4 varactor multiplier; it provides 25 mw PO at 9.2 Gc (X band). The TIX3016A can be used as a fundamental oscillator up to 3

Table 1. High-frequency Germanium Transistors

Type & package	f_{max} Guaranteed minimum	F_T		Noise figure		Fundamental oscillator PO	Area of operation
		Typical	Guaranteed minimum	Typical	Guaranteed maximum		
TIX3024 TI-line	4.5 Gc	1.7 Gc	1.5 Gc	1.6 db at 200 Mc 4.0 db at 1 Gc	5.0 db at 1 Gc		L & S band amplifier
2N2999 TO-18	3.3 Gc	1.6 Gc	1.4 Gc	5.0 db at 1.0 Gc	7.0 db at 1.0 Gc		L band amplifier S band oscillator
2N2998 TO-18	2.2 Gc	1.0 Gc	600 Mc	6.5 db at 1.0 Gc	8.0 db at 1.0 Gc		UHF amplifier L band oscillator
2N2415 TO-18	1.6 Gc	800 Mc	500 Mc	2.5 db at 200 Mc	3.0 db at 200 Mc		UHF amplifier
TIX3032 TO-18	1.8 Gc	700 Mc	500 Mc	3.5 db at 200 Mc	4.0 db at 200 Mc	20 mw at 1 Gc; 12 v, 12 ma; 14% eff. 10 mw at 1 Gc; 12 v, 6 ma	VHF amplifier UHF oscillator
2N2997 TO-18	1.4 Gc	700 Mc	400 Mc	3.0 db at 200 Mc	4.5 db at 200 Mc		UHF amplifier
2N2996 TO-18	1.1 Gc	600 Mc	400 Mc	3.5 db at 200 Mc	5.0 db at 200 Mc		VHF amplifier UHF oscillator

NOTE: Any of the above devices can be supplied in TO-18, μmesa, or TI-line packages. For other specifications, refer to individual data sheets.

Table 2. High-frequency Silicon Transistors

Type & package	f_{max} Guaranteed minimum	F_T		Noise figure		Fundamental oscillator PO		Area of operation
		Typical	Guaranteed minimum	Typical	Guaranteed maximum	Typical	Guaranteed minimum	
TI3016A		1.7 Gc		6 db at 1 Gc		50 mw at 2.0 Gc	30 mw at 2 Gc 20 v, 15 ma	L & S band oscillator
TIXS09		1.4 Gc		3.5 db at 450 Mc		60 mw at 1.5 Gc	30 mw at 1.5 Gc 20 v, 15 ma	UHF oscillator
TIXS10		1.2 Gc		4.5 db at 450 Mc		70 mw at 1.0 Gc	30 mw at 1.0 Gc 20 v, 15 ma	VHF oscillator
2N3570	2.75 Gc	1.7 Gc	1.5 Gc	6 db at 1 Gc	7 db at 1 Gc R_g = 50 ohms	60 mw at 1.0 Gc		UHF & L band amplifier
2N3571	2.20 Gc	1.4 Gc	1.2 Gc	3.5 db at 450 Mc	4 db at 450 Mc R_g = 100 ohms			Low-noise VHF-UHF amp.
2N3572	1.80 Gc	1.2 Gc	1.0 Gc	4.5 db at 450 Mc	6 db at 450 Mc R_g = 100 ohms			VHF-UHF amplifier
2N2865	1.25 Gc	900 Mc	600 Mc	3.5 db at 200 Mc	4.5 db at 200 Mc R_g = 75 ohms	55 mw at 500 Mc	40 mw at 500 Mc 10 v, 12 ma	Low-noise VHF-UHF amp.
2N918		900 Mc	600 Mc	3.0 db at 60 Mc	6 db at 60 Mc R_g = 400 ohms	50 mw at 500 Mc	30 mw at 500 Mc 15 v, 8 ma	Gen. Purpose VHF amplifier
2N917	510 Mc	800 Mc	500 Mc	3.0 db at 60 Mc	6 db at 60 Mc R_g = 400 ohms	20 mw at 500 Mc	10 mw at 500 Mc 15 v, 8 ma	Gen. Purpose RF amplifier

NOTE: Any of the above devices can be supplied in TO-18, μmesa, or TI-line packages. For other specifications, refer to individual data sheets.

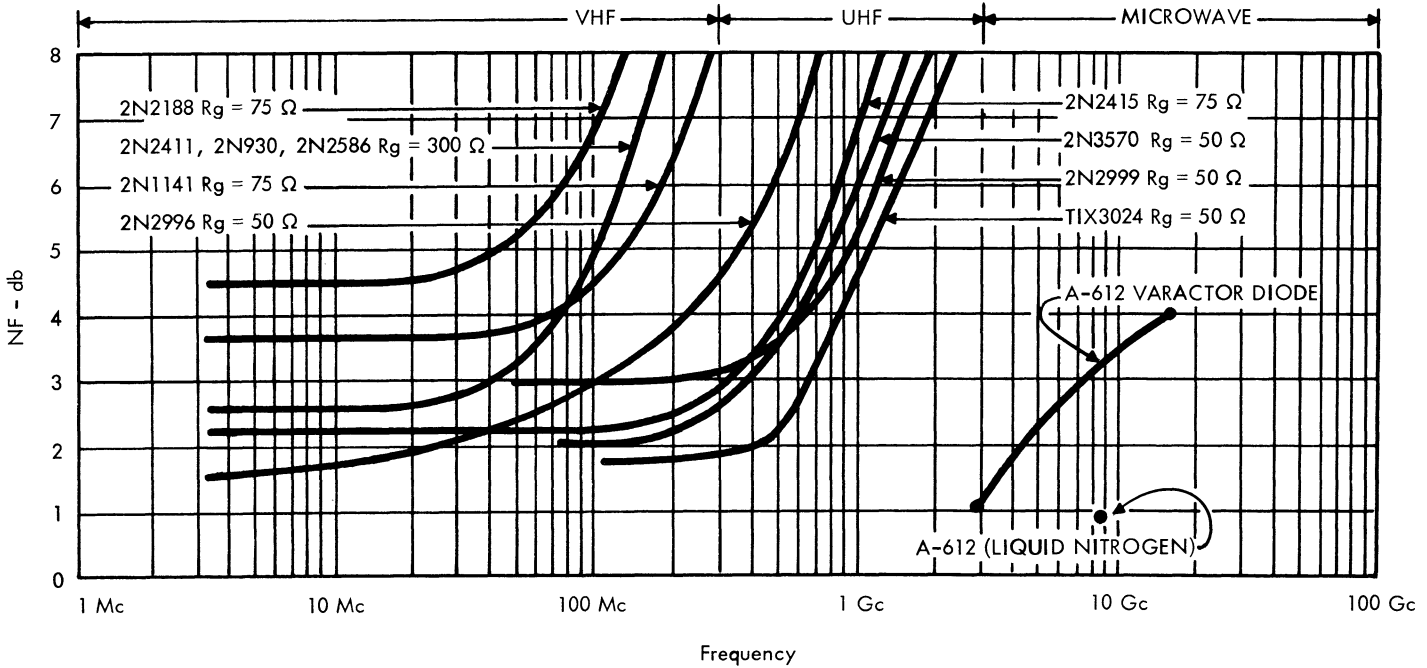

VHF
UHF
MICROWAVE
NF - db
8
7
6
5
4
3
2
1
0
2N2188 Rg = 75 Ω
2N2411, 2N930, 2N2586 Rg = 300 Ω
2N1141 Rg = 75 Ω
2N2996 Rg = 50 Ω
2N2415 Rg = 75 Ω
2N3570 Rg = 50 Ω
2N2999 Rg = 50 Ω
TIX3024 Rg = 50 Ω
A-612 VARACTOR DIODE
A-612 (LIQUID NITROGEN)
1 Mc
10 Mc
100 Mc
1 Gc
10 Gc
100 Gc
Frequency

Figure 1

Gc, a harmonic oscillator, or a power driver for varactor multiplier chains; multiple chips can be paralleled in one package.

Figure 2, showing power output vs. frequency, demonstrates what we feel are the present capabilities of these oscillator configurations. The units can be supplied in a TO-18, μmesa*, TI-axial*, or TI-line* package.

2N2865 has an NF specification better than that of the 2N918, which has no maximum 200-mc NF specification. As the two units are about the same price, the 2N2865 should be more attractive to the amplifier circuit designer; TI supplies both transistor types.

GERMANIUM SMALL-SIGNAL TRANSISTORS

TIX3032 *is the First Germanium Planar Transistor in the industry.* Perfection of this technology allows the use of expanded lead contacts — similar to those used in silicon planar transistors. This will decrease bonding problems (lower manufacturing cost), permit us to use smaller geometries eventually (higher frequency capability), and to have an oxide-passivated surface. This transistor could become the work horse in the VHF-UHF amplifier area. Note that its frequency

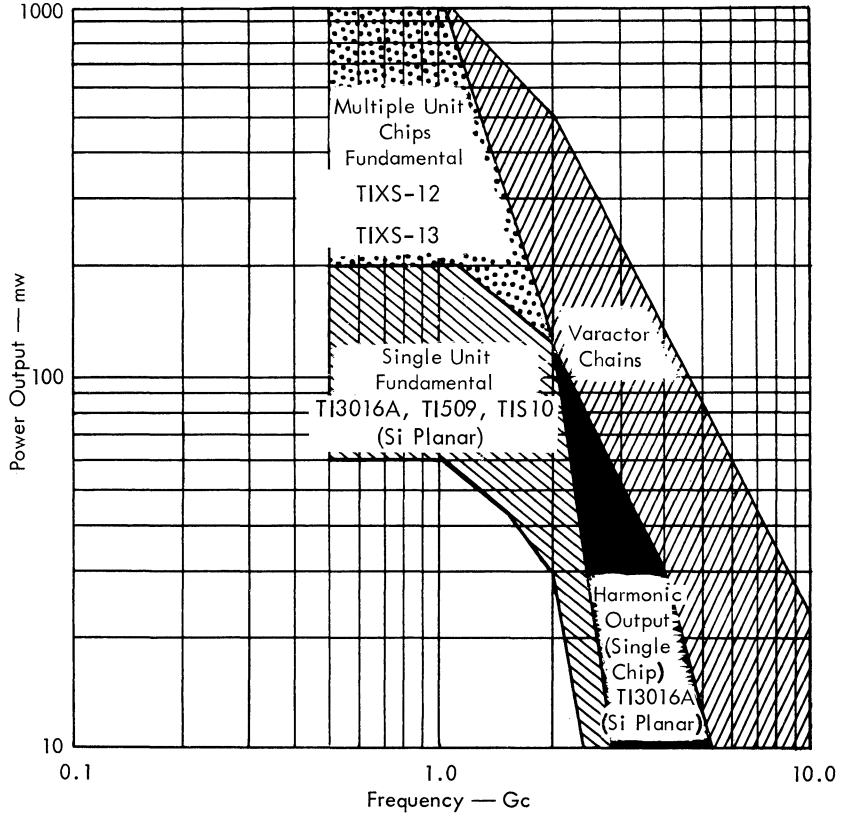


Figure 2

*Trademark of Texas Instruments

capabilities place it between the 2N2997 and the 2N2415. As an oscillator, it is specified at two current levels, demonstrates 14% efficiency, and is usable over a 2:1 range of collector current.

TIX3024 is a planar germanium epitaxial transistor designed as an amplifier. As an amplifier, its capability exceeds the 2N2999 in both gain and noise figure. The primary package is the TI-line package.

Amplifier applications are in the 1- to 3-Gc range, but the unit is also ideal in a broadband amplifier from 500 mc upwards, or as the first-stage amplifier following a balanced mixer.

DIODES

We are establishing a broader line of varactor diodes and voltage variable capacitors; their characteristics are summarized in Table 3.

The following covers the major characteristics of each of these families:

XA706 Series. The XA706 is an epitaxial silicon varactor diode intended primarily for use in frequency multiplier chains, but it may also be used effectively as a tuning element, microwave switch, or parametric amplifier diode. The proven microwave cartridge package houses the device. This package gives the advantage of low series inductance (0.4 nanohenry typical) plus matched temperature coefficients of expansion for added reliability.

When used in frequency multiplier chains (doubler, tripler, etc.) the XA706 can provide up to 10 watts depending on available power input and circuit efficiency. The capacitance-voltage relationship approximates the ½ power law obtained with a theoretical abrupt junction.

XA900 Series. The XA900 is an epitaxial gallium arsenide varactor diode intended primarily for microwave frequency multiplication, but it, too, may be used effectively as a tuning element, microwave switch, or parametric amplifier diode. This unit has the highest available breakdown voltage for the highest available cutoff frequency in the industry, typically 50-VR breakdown and 300-Gc f_{co} at −6 volts.

The popular microwave double-pill-prong package offers low series inductance (0.4 nanohenry) plus matched temperature coefficients of expansion for added reliability; the package is adaptable to coaxial circuit configurations. This unit will provide excellent reproducible results when used in multiplier circuits with inputs at 1 to 10 Kmc.

XA580 Series. This series of voltage variable capacitance diodes comprises epitaxial silicon units with a voltage-capacitance relationship that approximates the ½ power law associated with the theoretical abrupt junction. The units were designed primarily for tuning applications, but they may also be used effectively as frequency multipliers and AFC diodes.

The units are glass-passivated for high reliability and are packaged in the proved Moly/G® hard-glass structure. They feature a close capacitance tolerance at a low price, as well as excellent capacitance tracking qualities.

When used in tuning applications, these units can be relied upon to give highly reproducible results from unit to unit... minimizing circuit design problems.

XD500 Series. The XD500, A610, and A600 series diodes were the first gallium arsenide varactor diodes introduced to the market. These diodes continue to offer, through improved techniques, the best in parametric amplifier diodes. They

Table 3. High-frequency Diodes

Unit type (series)	Package	f_{co}	CT (range)	BV_R (range)	Operating range	Primary application	Technology
XA706	Cartridge	140 Gc	0.4-30 pf	24-120 v	1-5 Gc	Harmonic generator.	Si epitaxial
XA900	Dbl. pill prong	300 Gc	0.4-1.4 pf	30-50 v	1-10 Gc	Harmonic generator	GaAs epitaxial
XA580	Moly/G®	5 Gc	22-47 pf	35-65 v	DC-500 Mc	Electronic tuning (Voltage variable capacitor)	Si epitaxial
XD500	Cartridge	150 Gc	0.4-1.0 pf	8 v	1-5 Gc	Parametric amplifier	Diffused GaAs
TIVO1	Pill	300 Gc	0.35-1.0 pf	6 v	1-15 Gc	Parametric amplifier	Diffused GaAs

NOTE: Where range is given, it means that the *family* of devices covers the range — not necessarily each device.

Applications:
- **Harmonic Generators**
- **Electronic Tuning**
- **Parametric Amplifiers**

are the most "use-proven" parametric varactors on the market... and in the final analysis, use is the only true test of varactor performance.

TIV01 Series. This series comprises state-of-the-art parametric amplifier diode types. Devices in the series offer the highest available cutoff frequencies. Device structures are fabricated using a gallium arsenide diffused epitaxial process. The TIV01 Series offers ideal units for low-noise parametric amplifier operation.

HIGH-FREQUENCY TRANSISTOR PACKAGES

TI developed co-axial and TI-line packages to permit full utilization of the maximum frequency capability of the transistor chip. The package must have a low series equivalent resistance and inductance at the desired frequency or the full performance of the transistor chip can not be realized.

Figure 3 is a plot of the equivalent series resistance vs. frequency of our present microwave packages. Note that the TO-18 is usable only to 1 Gc. Preferred packages above 1 Gc are definitely the TI-line and co-axial. TI will furnish devices in any of these packages on special request.

Co-axial Package. The co-axial package is suitable for co-axial circuit configurations. It is the smallest and best performing co-axial package in the industry. The base connection is the center flange, whose area provides an excellent means of grounding the base. The emitter contact (short stud) is a heavy low-inductance

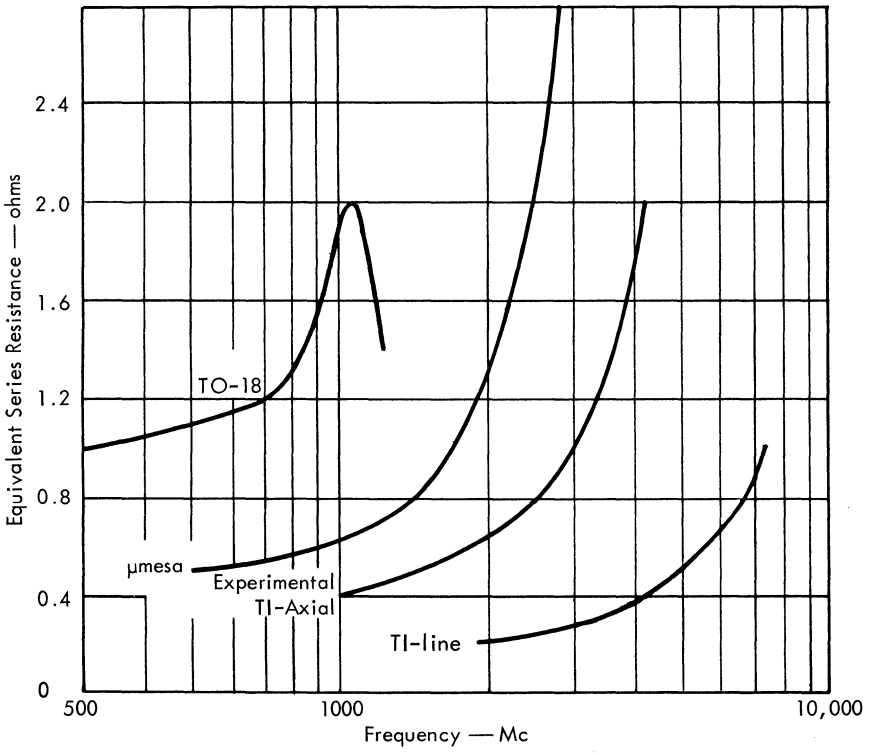


Figure 3

copper contact to the emitter strip. The chip is mounted directly on the longer copper stud, providing excellent heat conductivity.

The flange, being of larger diameter than the ceramic, allows the unit to be placed in a hole cut in a ground plane and to be clamped around its periphery to attain an excellent RF ground. The co-axial package is still being improved, and ultimately should have as low an equivalent series resistance as the TI-line package.

TI-line Package. This package is similar to the μmesa package only in appearance and dimensions. An exploded view is shown in Fig. 4; the basing is as shown

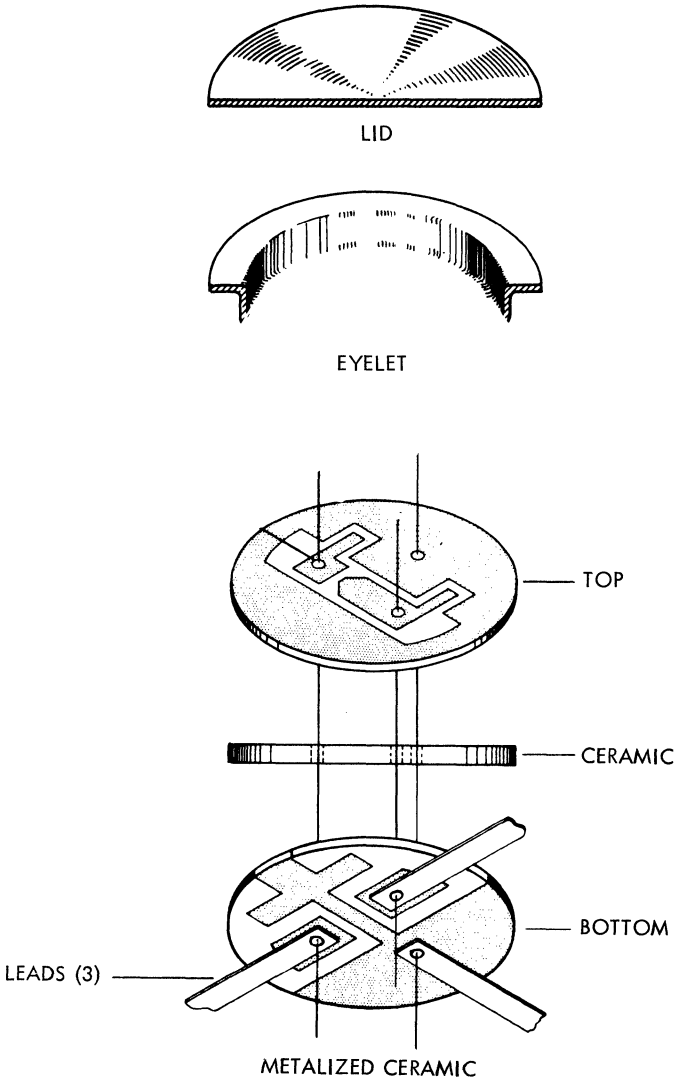


Figure 4

in Fig. 5. This revised basing gives better separation of the input and output circuits (E&C leads are adjacent in the μmesa package). The emitter and collector lines of this package can be controlled to have a 50-ohm impedance to the wafer. (A TI patent disclosure has been filed on this package.)

Chief advantages of the TI-line package are its low equivalent series resistance, its controlled 50-ohm impedances, and its suitability to strip-line configurations. The leads are gold-plated silver, giving excellent electrical and heat conductivity. In the future, this will allow us to increase the dissipation rating of devices in this package.

INTEGRATED CIRCUITS

Potted modules, thin-film circuits, and SOLID CIRCUIT® semiconductor networks all offer added value:

- Significant savings result from sharp decrease in number of components in inventory
- Procurement procedures can be streamlined
- Incoming inspection costs are reduced
- Automatic assembly techniques can be used
- In-house engineering capabilities can be better utilized
- Entire circuit function is guaranteed
- Size and weight are usually reduced dramatically
- Significant reliability advantages

We welcome your inquiries; we are always happy to submit quotations to satisfy your needs.

Modules. TI is a leader in discrete amplifier capability. These devices can be coupled with our other component products to provide a packaged circuit, possibly with an economic advantage for you.

Thin-film Circuits. We have fabricated 20-mc linear thin-film chip circuits, and a 60-mc log IF circuit. The high-frequency capabilities of our silicon chips, or germanium and silicon units packaged in μmesa or TI-line packages, coupled with our nichrome and tantalum thin-film chip linear circuits, offer you great versatility of circuit manufacture.

What is more natural than to fabricate extremely-high-frequency circuits by this technology and later translate these circuits into monolithic silicon form (SOLID CIRCUIT® semiconductor networks)?

SOLID CIRCUIT® Semiconductor Networks. Texas Instruments Series 52 differential amplifiers were the only linear semiconductor networks shown at IEEE 1964. Work is progressing on higher-frequency linear amplifiers which will be announced at a later date.

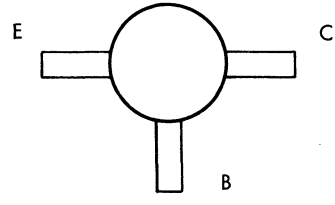


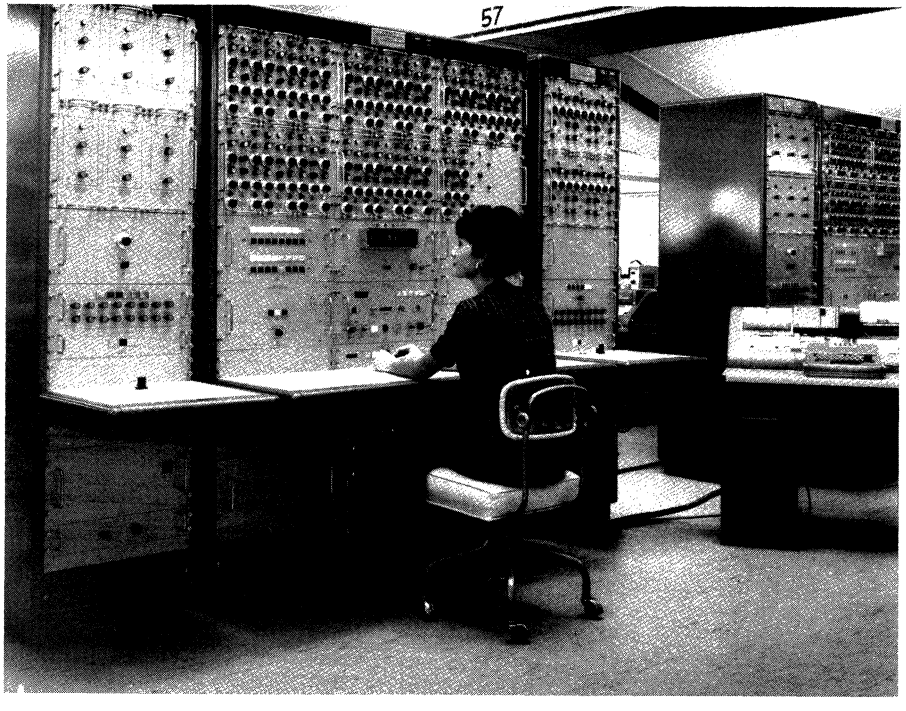
Figure 5

POWER COMMUNICATIONS PRODUCTS

We have available a microwave power source in module form. The unit consists of:

1st stage: a 45-watt 50-mc source
1st tripler: a varactor tripler that delivers approximately 37 watts at 150 mc
2nd tripler: a single varactor that delivers 25 watts at 450 mc

Overall efficiency is approximately 50%



"SMART," the TI-developed and TI-built Sequential Mechanism for Automatic Recording and Testing. Each SMART automatically measures 16 parameters in a few seconds, recording the data on punched cards.

Typical of the fine communications equipment employing TI components is this citizens band transceiver manufactured by Osborne Electronics, Hawthorne, California.

2

Dependence of Transistor y Parameters on Bias, Frequency, and Temperature

by George Johnson

INTRODUCTION

The application of two-port theory to linear active networks is not new.[1-3]* The vacuum tube has been treated in this way and tabulations of its two-terminal properties are recorded in the literature.[4,6] Many authors have used these techniques in the analysis of electric networks that have linear active networks buried within the structure.[6-8] Lately these methods have been applied to transistors.[9-11] Notable among these references is the work done by Cote and Oakes[7] and Pettit and McWhorter.[11] Both of these references use modern network theory as a foundation for a unified treatment of linear active circuits with equal emphasis on tubes and transistors.

Since the theoretical analysis has been well developed, one logical extension is to apply it to modern high-frequency transistor circuit design. As a first step, we briefly define the two-port parameters and discuss measuring instruments used to develop the parameters. The effects of bias, frequency, and temperature on the y parameters of a germanium mesa transistor are then presented.

TWO-PORT PARAMETERS

Since emphasis will be placed on the two-terminal y parameters and h parameters, only these will be mentioned. It should be stated however that, in general, any set of two-port parameters (z, y, h, or g) may be used.

A complete description of the small-signal a-c behavior of any two-terminal structure can be accomplished by specifying its y parameters, defined as follows:

y_{11} = input admittance for a-c short-circuited output
y_{12} = reverse transfer admittance for a-c short-circuited input
y_{21} = forward transfer admittance for a-c short-circuited output
y_{22} = output admittance for a-c short-circuited input

*Superscript numbers refer to bibliography entries at end of chapter.

These parameters, which may or may not be complex, may be grouped into an array called the y matrix:

$$[y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$$

In a similar manner a set of small-signal hybrid parameters may be defined as follows:

h_{11} = input impedance for a-c short-circuited output
h_{12} = reverse voltage transfer ratio for a-c open-circuited input
h_{21} = forward current transfer ratio for a-c short-circuited output
h_{22} = output admittance for a-c open-circuited input

These parameters may also be grouped into a square array called the h matrix:

$$[h] = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix}$$

Numerical subscripts are customarily used in passive network analysis, and refer to Fig. 1. When *active* networks are used, the subscripts are changed to indicate more clearly the meaning of the parameter. For instance, if the common-emitter configuration is considered, then the admittance matrix is

$$[y_e] = \begin{bmatrix} y_{ie} & y_{re} \\ y_{fe} & y_{oe} \end{bmatrix}$$

Table 1 is provided to facilitate conversion between y and h parameters. The two-port equivalent circuits corresponding to the parameters defined are shown in Fig. 2. The polarities are defined in Fig. 1.

Table 1. Conversion between h and y parameters for a like common terminal

y_i	y_r	$\frac{1}{h_i}$	$\frac{-h_r}{h_i}$
y_f	y_o	$\frac{h_f}{h_i}$	$\frac{\Delta h}{h_i}$
h_i	h_r	$\frac{1}{y_i}$	$\frac{-y_r}{y_i}$
h_f	h_o	$\frac{y_f}{y_i}$	$\frac{\Delta y}{y_i}$

$$\Delta y = y_i y_o - y_f y_r = \frac{h_o}{h_i}$$

$$\Delta h = h_i h_o - h_f h_r = \frac{y_o}{y_i}$$

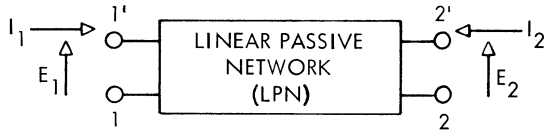


Fig. 1. A passive two-port.

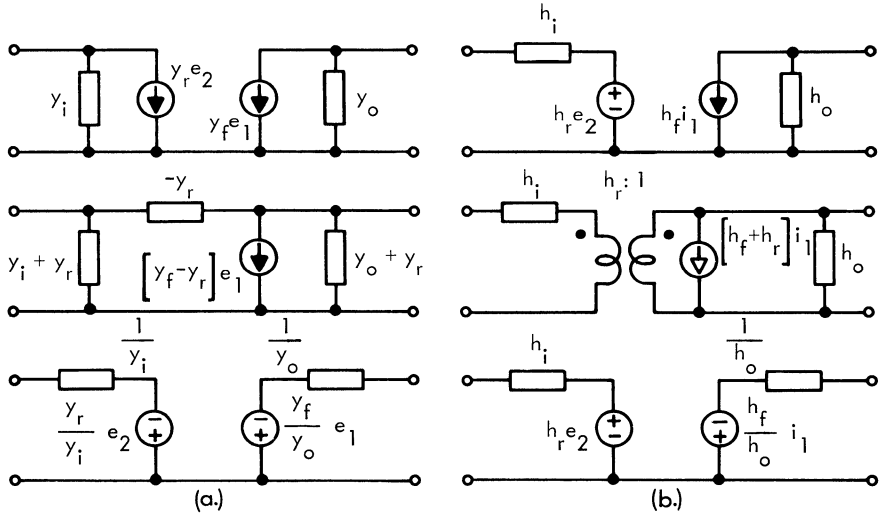


Fig. 2. One- and two-generator equivalent circuits in terms of: (a) y parameters; (b) h parameters.

MEASUREMENT OF THE y PARAMETERS

The measurement of high-frequency transistor two-port (or for that matter, internal) parameters is a technology in itself. Basically, two problems are encountered when any high-frequency two-port measurements are contemplated:

1. Which two-port parameters are best to measure?
2. Which instrument will most accurately measure these parameters?

In order to answer the first question, consider the elements of the admittance matrix for a transistor as shown in Fig. 3. A set of equations describing this network is given in Eqs. (1), (2), and (3).

$$I_b = y_{bb}V_b + y_{be}V_e + y_{bc}V_c \quad (1)$$

$$I_e = y_{eb}V_b + y_{ee}V_e + y_{ec}V_c \quad (2)$$

$$I_c = y_{cb}V_b + y_{ce}V_e + y_{cc}V_c \quad (3)$$

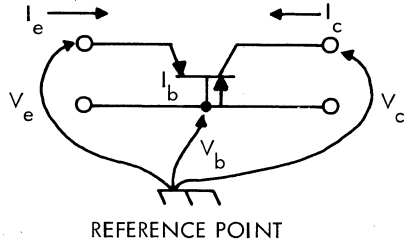


Fig. 3. A three-terminal network.

The matrix of the elements y_{ij} is called the indefinite admittance matrix because the reference node is unspecified. The elements y_{ij} of the indefinite matrix may be identified as the current flowiing into node i when one volt is applied between node j and ground, with all nodes but node j short-circuited to ground. Therefore, y_{eb} is the current flowing into terminal e from ground when one volt is impressed between the base and ground and all other terminals are grounded. Figure 4 defines the various currents for each orientation.

Consider Eqs. (1), (2), and (3). Strike out all b's. The remaining set [Eqs. (4) and (5)] defines the common-base matrix:

$$I_e = y_{ee}V_e + y_{ec}V_c \tag{4}$$

$$I_c = y_{ce}V_e + y_{cc}V_c \tag{5}$$

When we repeat the same process for the e's and c's, the following sets result. [Eqs. (6) through (9).]

$$I_b = y_{bb}V_b + y_{bc}V_c \tag{6}$$

$$I_c = y_{cb}V_b + y_{cc}V_c \tag{7}$$

$$I_b = y_{bb}V_b + y_{be}V_e \tag{8}$$

$$I_e = y_{eb}V_b + y_{ee}V_e \tag{9}$$

Now when we compare Eqs. (6) and (8), it is evident that y_{11} for the common-emitter set is equal to y_{11} for the common-collector set. Further comparisons result in Table 2. Now consider Fig. 3 again. Using Kirchoff's current rule, the sum of the currents I_b, I_e, and I_c must be zero for a specified voltage. Since V_e and V_c are zero for the common-base condition, Eq. (10) may be written:

$$I_b + I_e + I_c = 0 = V_b(y_{bb} + y_{cb} + y_{eb}) \tag{10}$$

Since

$$V_b \neq 0$$

then

$$y_{bb} + y_{cb} + y_{eb} = 0$$

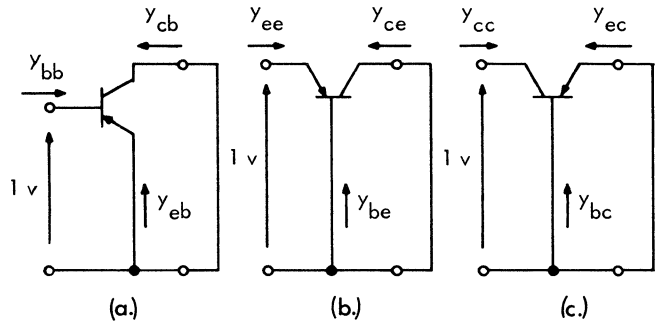


Fig. 4. Orientations: (a) common emitter; (b) common base; (c) common collector.

Table 2. Relationship among the parameters of the indefinite matrix

$y_{bb} = y_{ie} = y_{ic}$	$y_{be} = y_{rc}$	$y_{bc} = y_{re}$
$y_{eb} = y_{fc}$	$y_{ee} = y_{ib} = y_{oc}$	$y_{ec} = y_{rb}$
$y_{cb} = y_{fe}$	$y_{ce} = y_{fb}$	$y_{cc} = y_{ob} = y_{oe}$

In other words, the sum of the admittances in any row or column of the matrix of the coefficients of Eqs. (1) through (3) must add to zero. It is therefore evident that, in general, four parameters of the indefinite matrix set will be sufficient to allow calculation of all the parameters. From a practical standpoint, certain parameters are more desirable to measure than others, and considering such things as bridge loading and resolution we can eliminate some of the parameters. Probably the best set to choose is: y_{ie}, y_{ib}, y_{oe}, and y_{re}; this answers our first question.

Before the second question is discussed it should be mentioned that the y data presented in this chapter are for a consistent set of parameters. This yields a usable set of data as measured, without conversion.

The problem of determining the most accurate and practical measuring instrument is not answerable directly. The value of the two-port parameters and the frequency range are only two of the considerations that influence this choice. Two of the more popular bridges in use are the General Radio transfer function and immittance bridge and the Wayne Kerr bridge. Figures 5, 6, 7, and 8 show schematically each of these bridges.

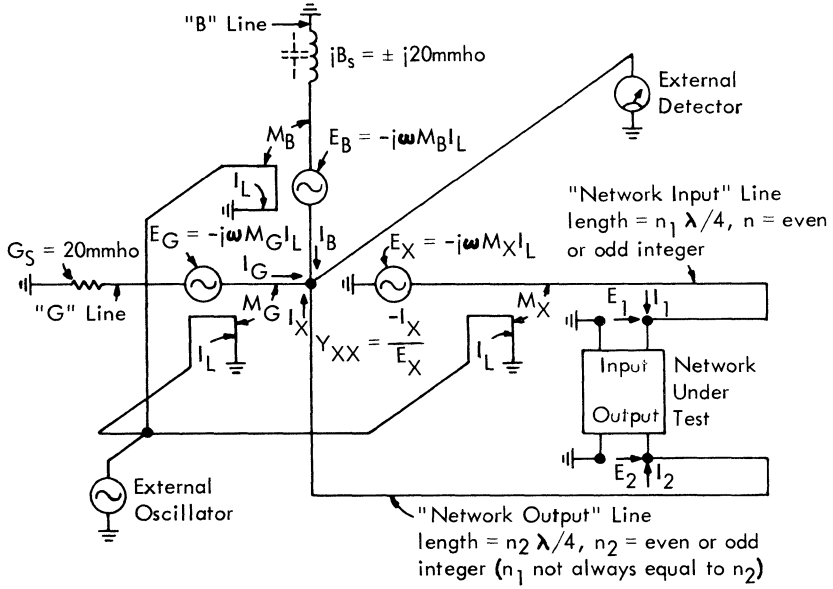


Figure 5

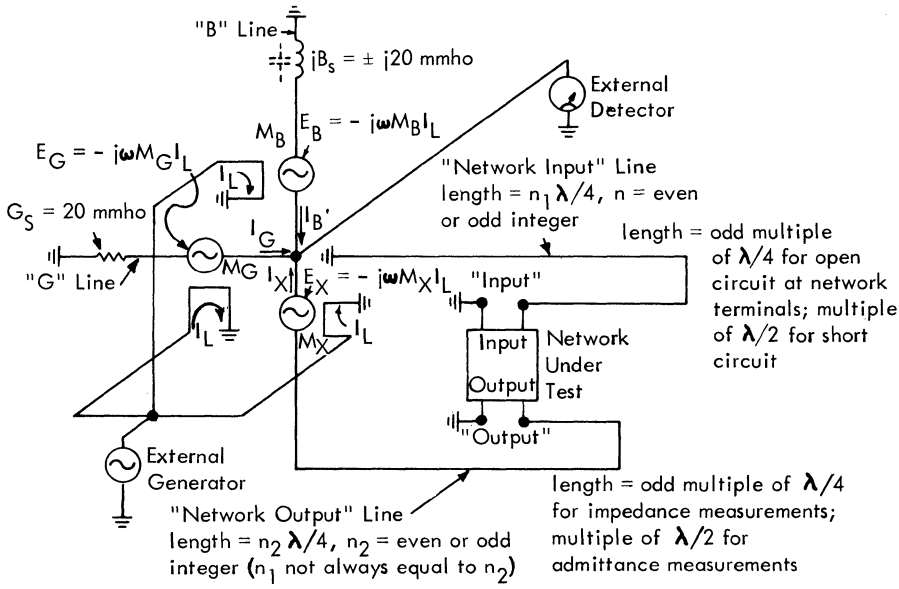


Figure 6

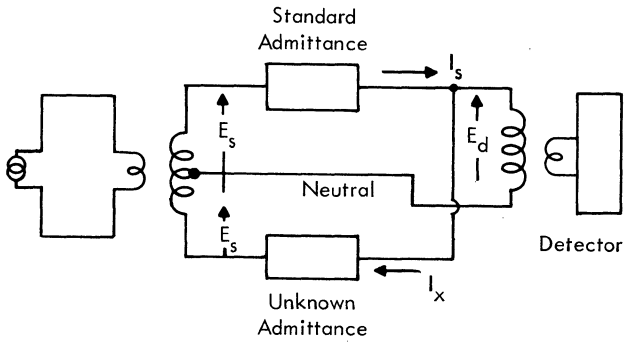


Fig. 7. Simplified diagram of Wayne Kerr bridge used for two-terminal measurements.

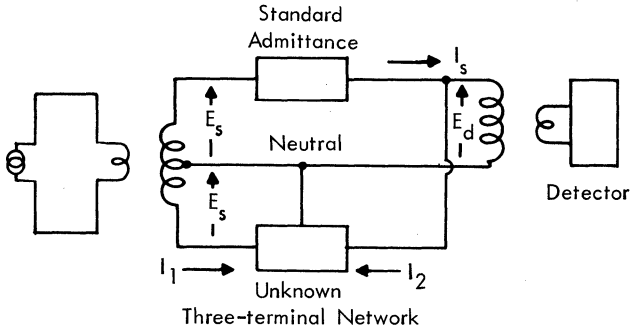


Fig. 8. Simplified diagram of Wayne Kerr bridge as used to measure the transfer admittance of a three-terminal network.

The bridge chosen for the measurement of the y parameters presented here is the General Radio bridge, because it covers a broader frequency range, and it does not require a separate jig as does the Wayne Kerr bridge.

SENSITIVITY OF y PARAMETERS

This section displays graphically the change in the y parameters of a high-performance germanium transistor with changes in bias, frequency, and temperature. The transistor selected is the 2N2415. No effort is made to relate these changes to any particular internal parameter change. The primary objective is to present accurately measured two-port data for use in practical designs. The curves of Figs. 9 through 26 contain these data.

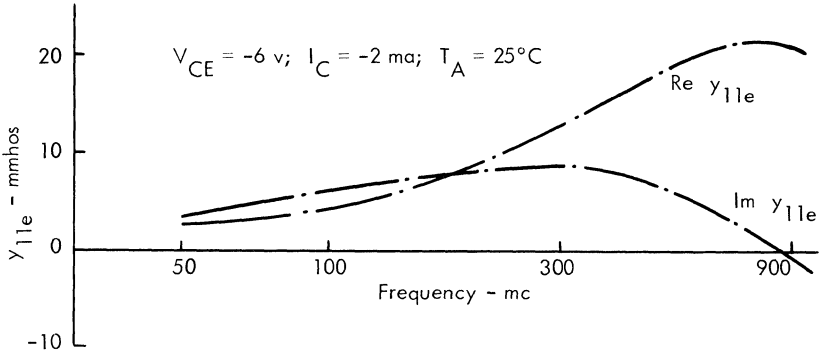


Figure 9

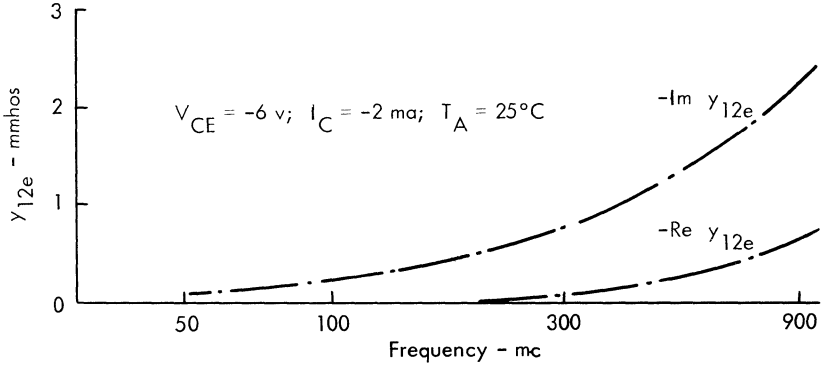


Figure 10

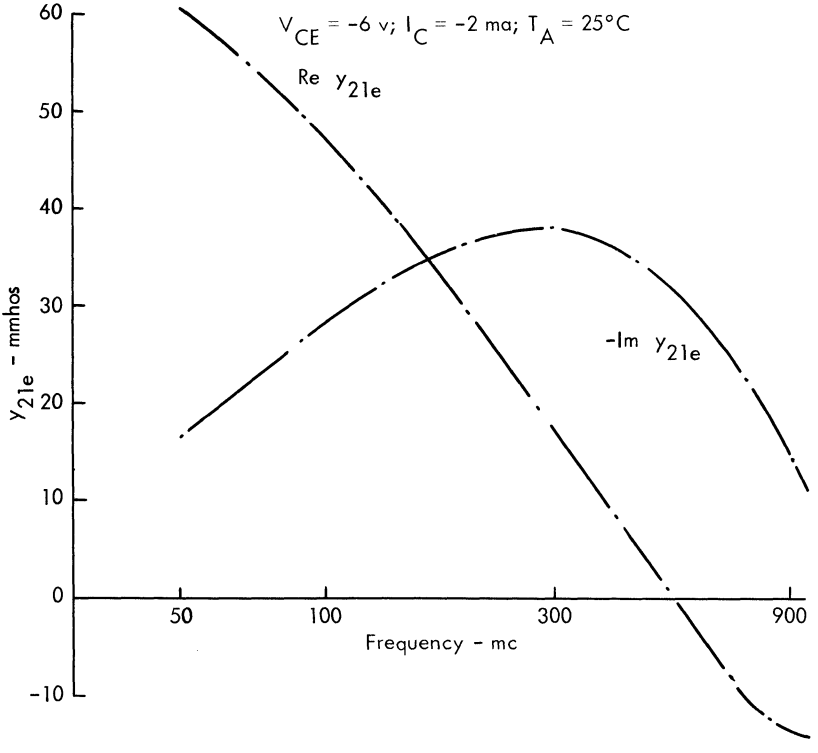


Figure 11

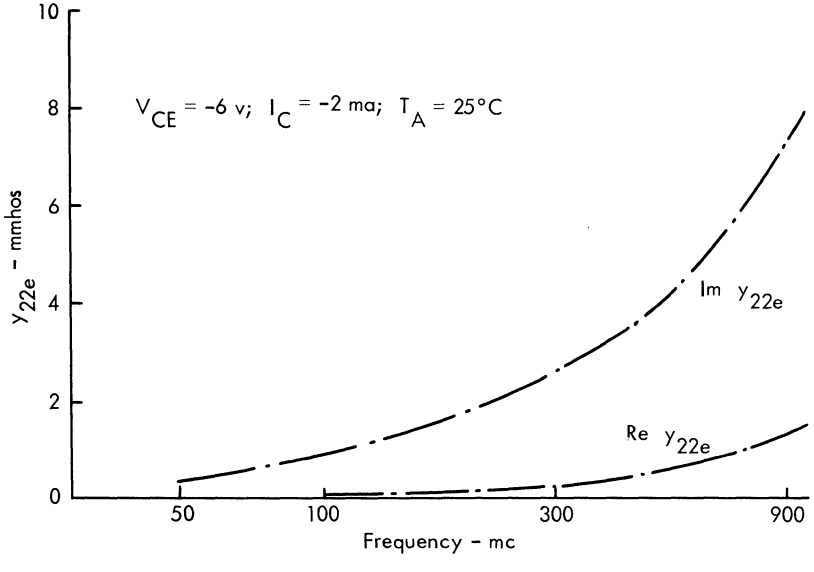


Figure 12

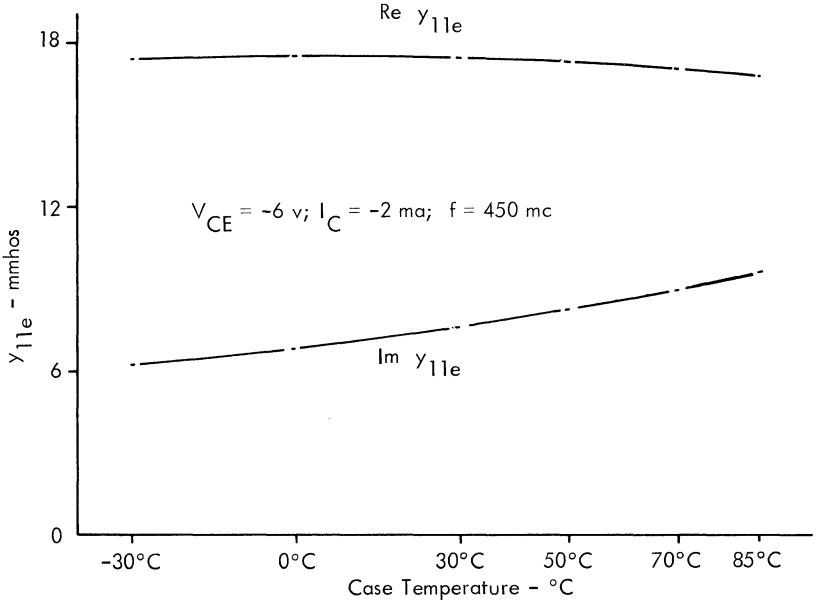


Figure 13

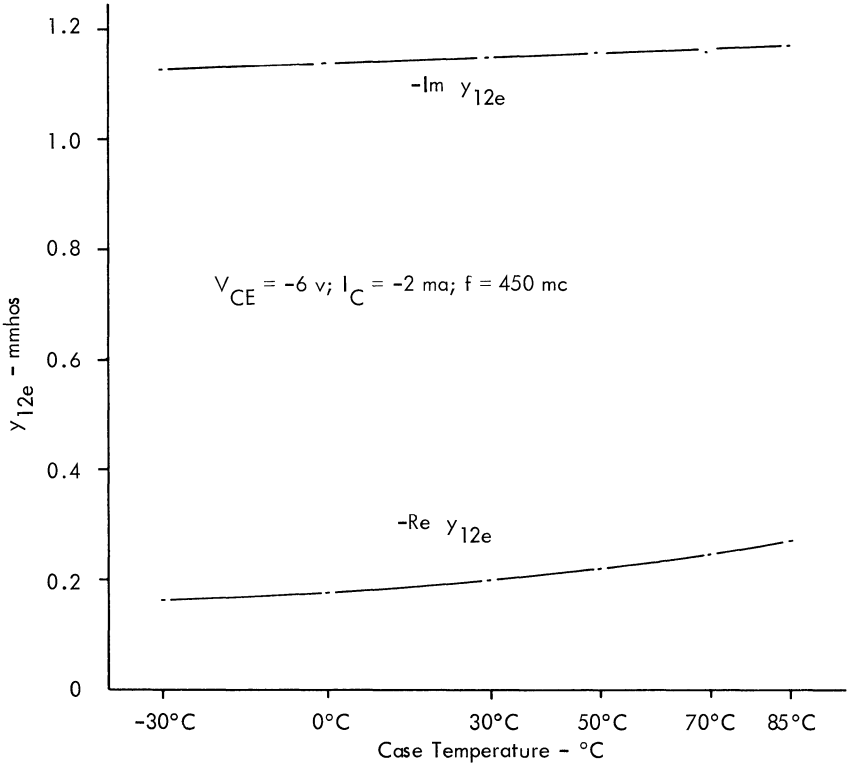


Figure 14

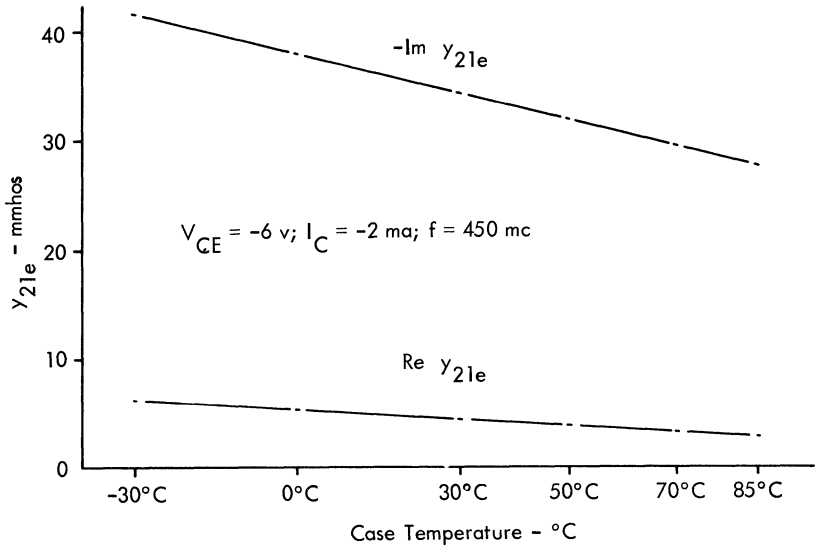


Figure 15

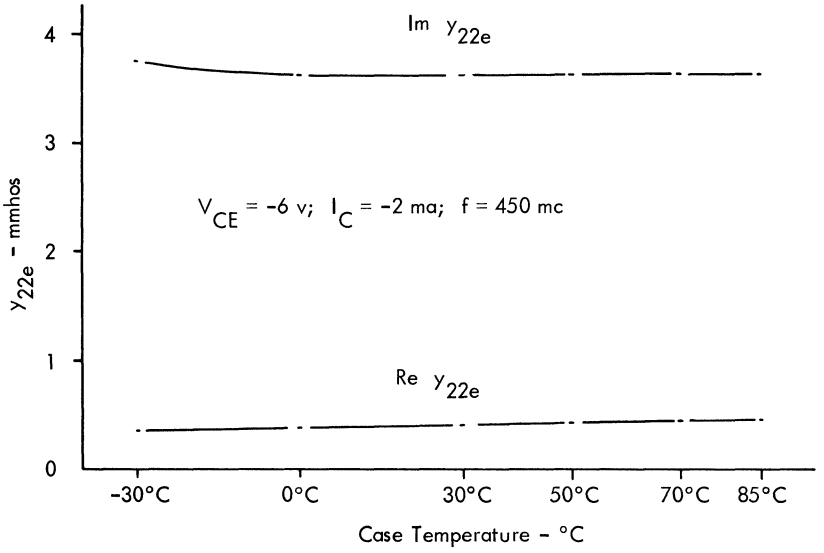


Figure 16

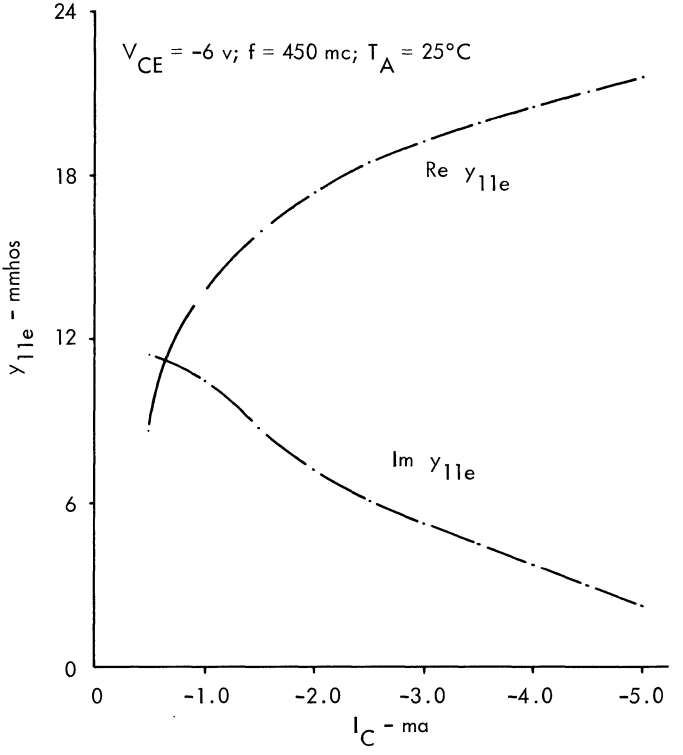


Figure 17

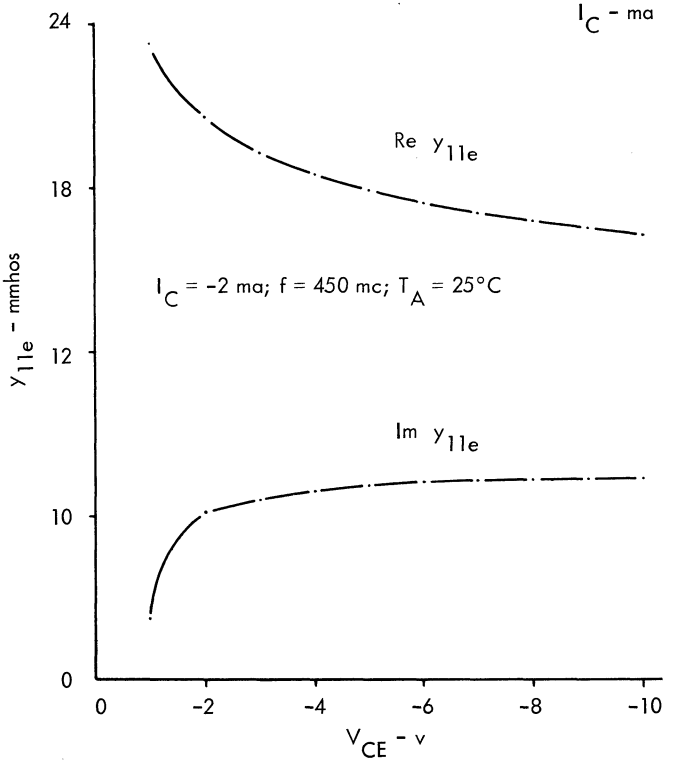


Figure 18

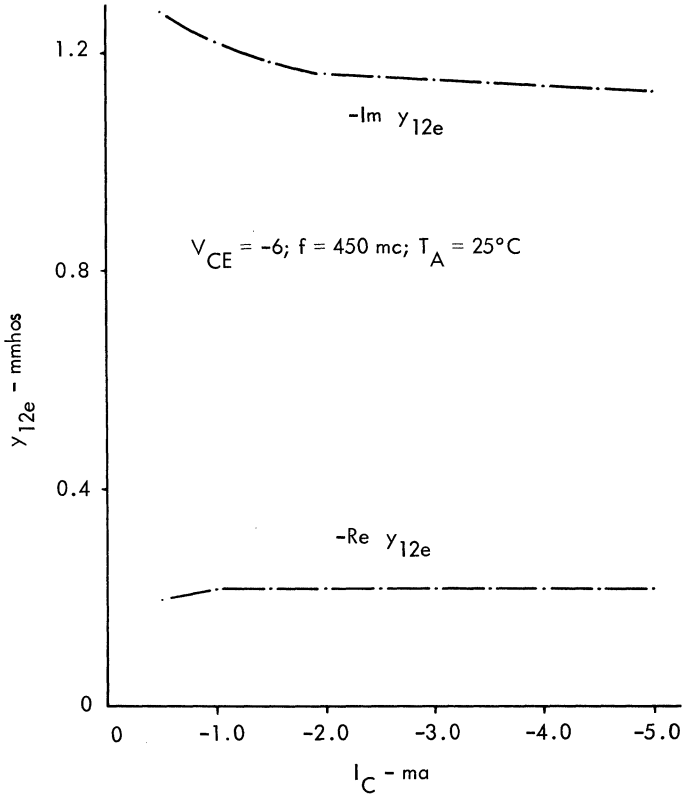


Figure 19

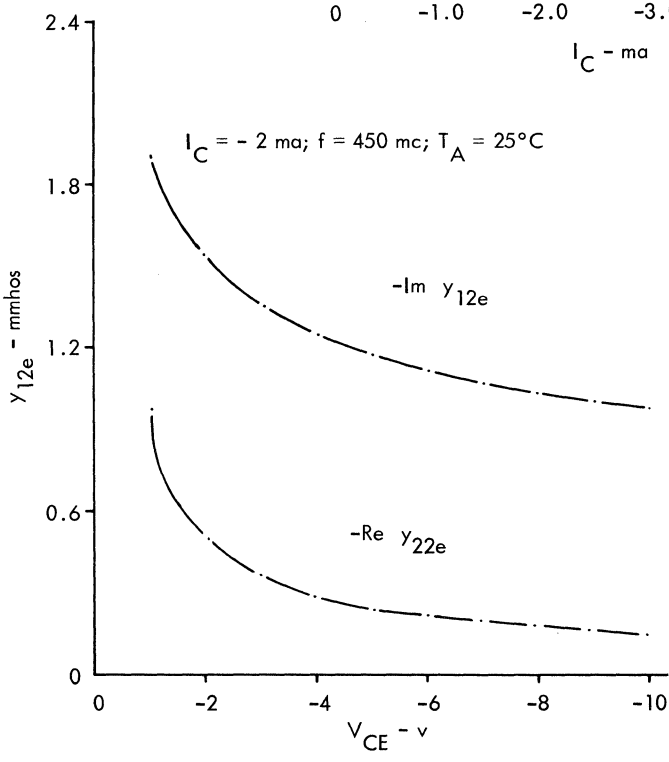


Figure 20

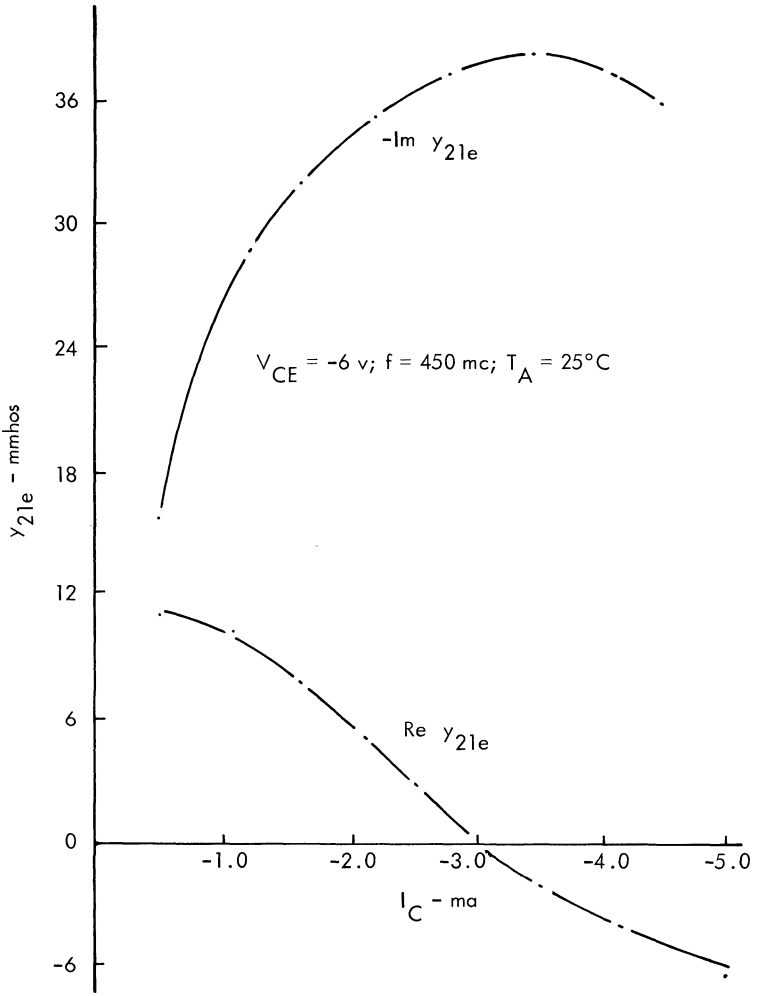

36
30
24
18
12
6
0
-6
y_{21e} - mmhos
-Im y_{21e}
V_{CE} = -6 v; f = 450 mc; T_A = 25°C
Re y_{21e}
-1.0
-2.0
-3.0
-4.0
-5.0
I_C - ma

Figure 21

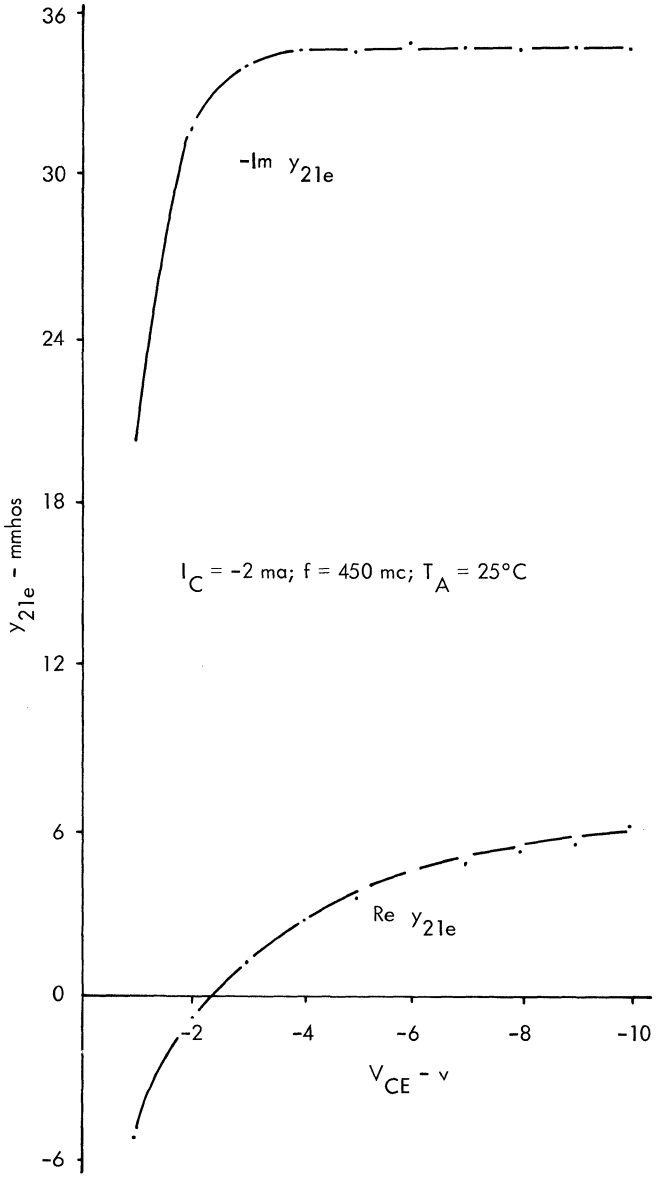

36
30
24
18
12
6
0
-6
y_{21e} - mmhos
-Im y_{21e}
I_C = -2 ma; f = 450 mc; T_A = 25°C
Re y_{21e}
-2
-4
-6
-8
-10
V_{CE} - v

Figure 22

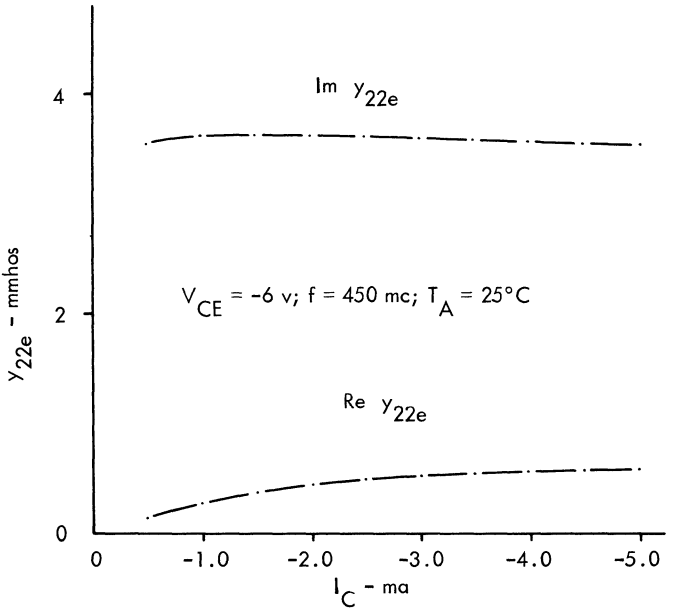


Figure 23

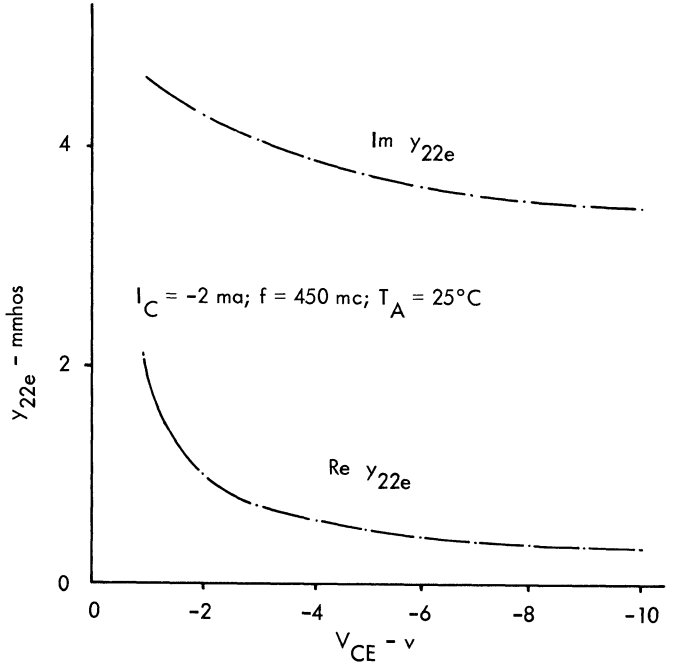


Figure 24

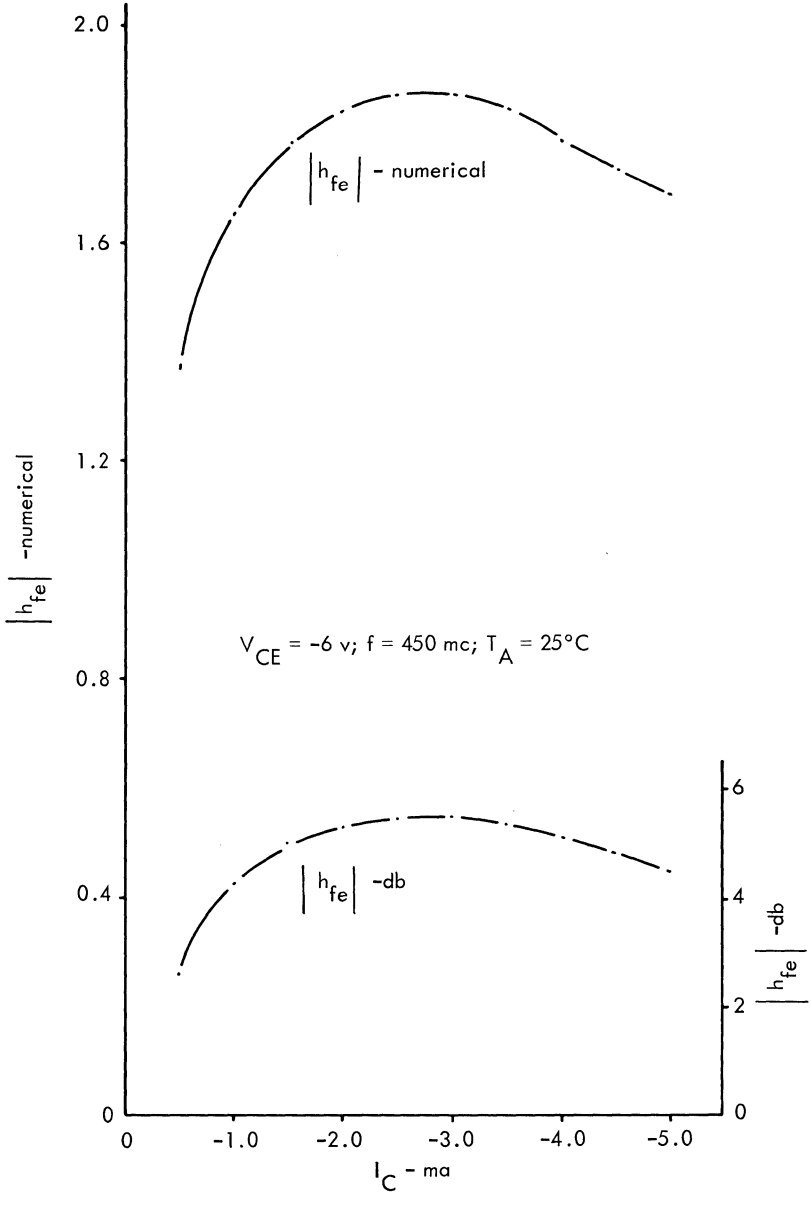

2.0
1.6
1.2
0.8
0.4
0
$|h_{fe}|$ - numerical
V_{CE} = -6 v; f = 450 mc; T_A = 25°C
$|h_{fe}|$ -db
$|h_{fe}|$ -numerical
6
4
2
0
$|h_{fe}|$ -db
0
-1.0
-2.0
-3.0
-4.0
-5.0
I_C - ma

Figure 25

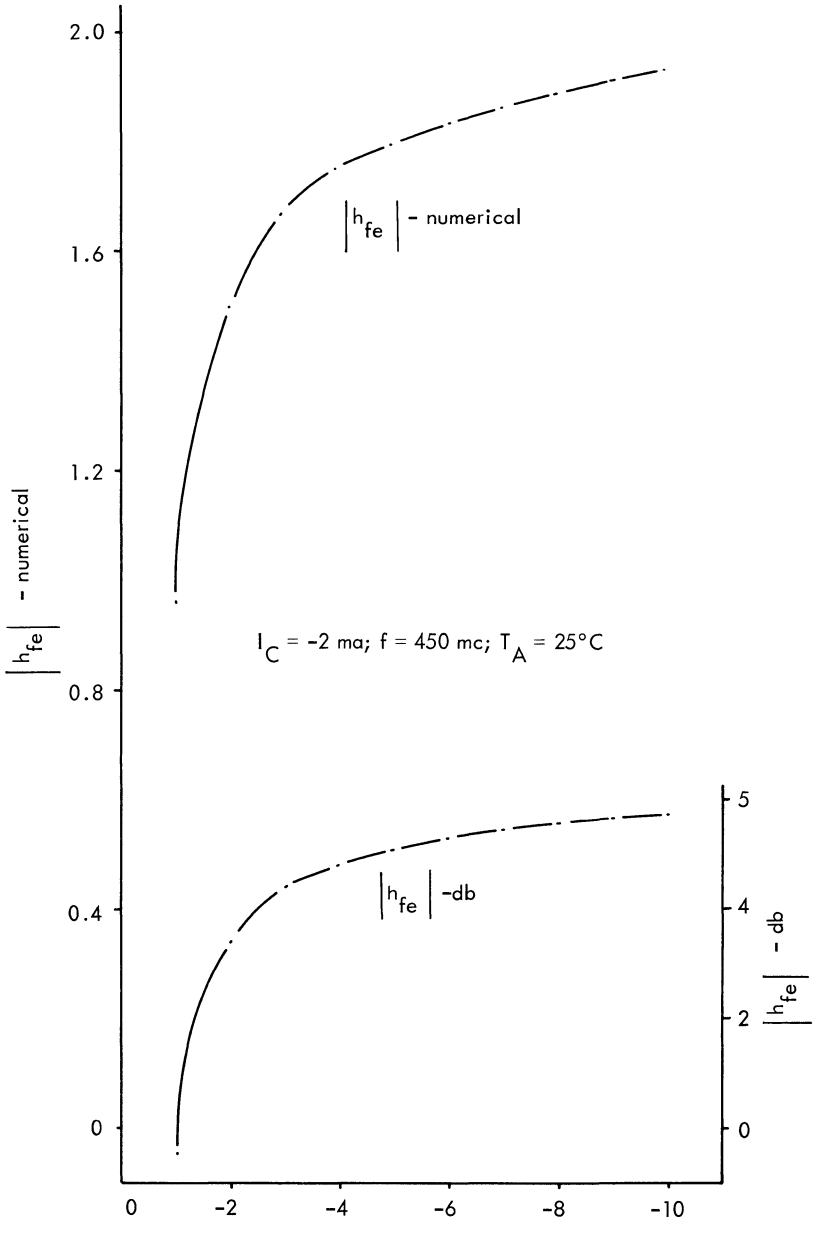

2.0
1.6
1.2
0.8
0.4
0
$|h_{fe}|$ - numerical
$|h_{fe}|$ - numerical
I_C = -2 ma; f = 450 mc; T_A = 25°C
$|h_{fe}|$ -db
5
4
2
0
$|h_{fe}|$ - db
0
-2
-4
-6
-8
-10

Figure 26

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3

Typical y Parameter Data

prepared by George Johnson

INTRODUCTION

The following two-port parameters and data are provided as an aid to the design of high-frequency circuits.

The y-parameters were obtained, in general, from a typical sample selected from a larger lot. Therefore, they represent the typical terminal properties of the

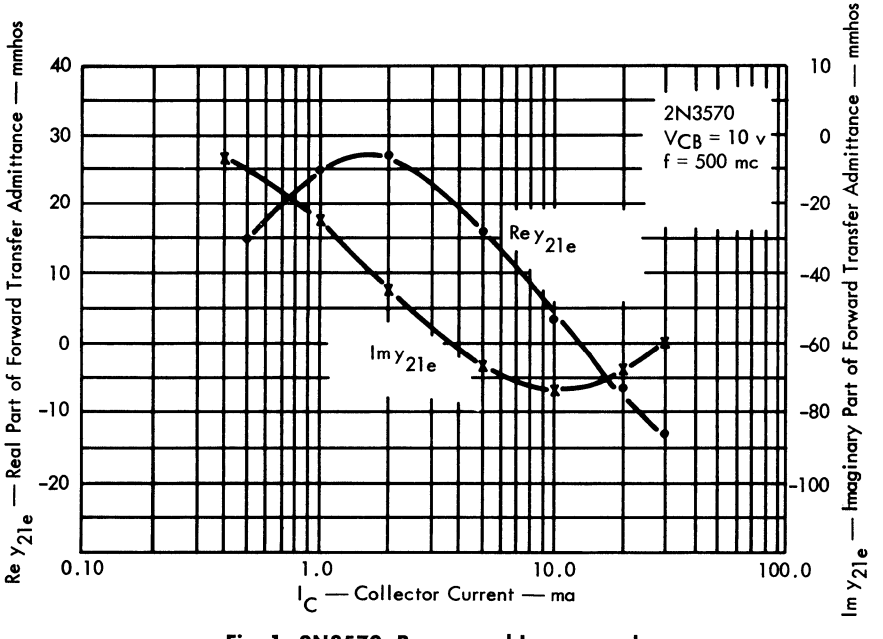

Fig. 1. 2N3570: Re y_{21e} and Im y_{21e} vs. I_C.

transistor in question at that time. All the parameters were measured on a General Radio transfer function and immittance bridge.

The list of transistors includes both silicon and germanium. The range of f_t represented by this selection of transistors is from 200 mc to 1.6 Gc. For further information on both a-c and d-c parameters, see the pertinent TI data sheets.

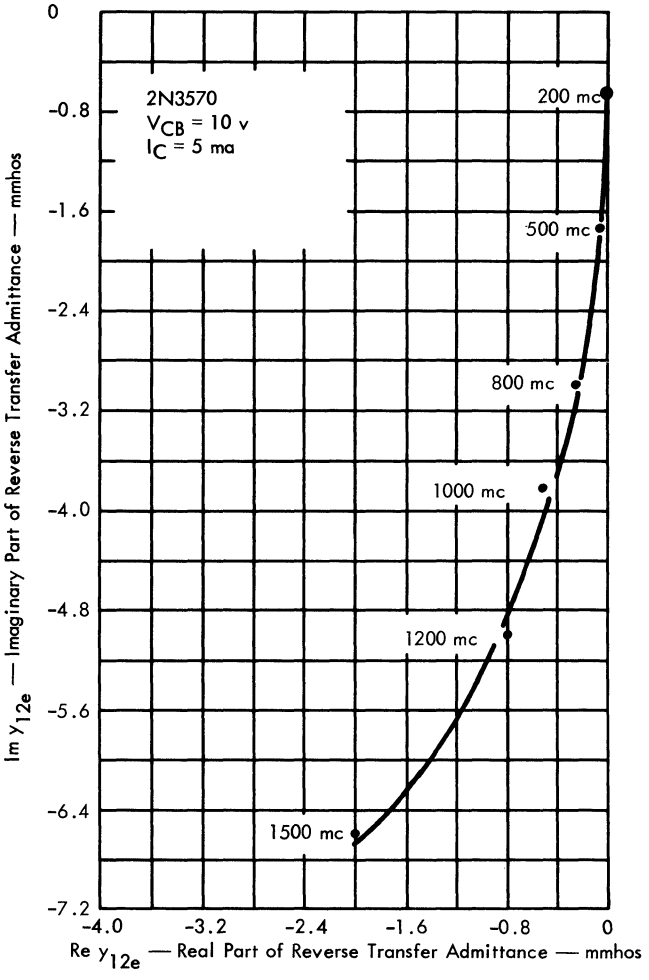

Fig. 2. 2N3570: Im y_{12e} vs. Re y_{12e}.

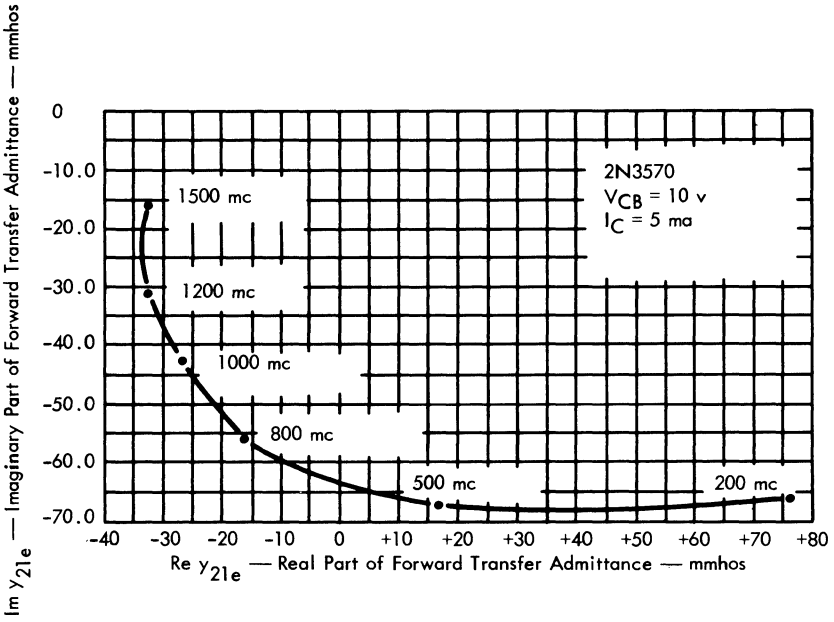

Fig. 3. 2N3570: Im y_{21e} vs. Re y_{21e}.

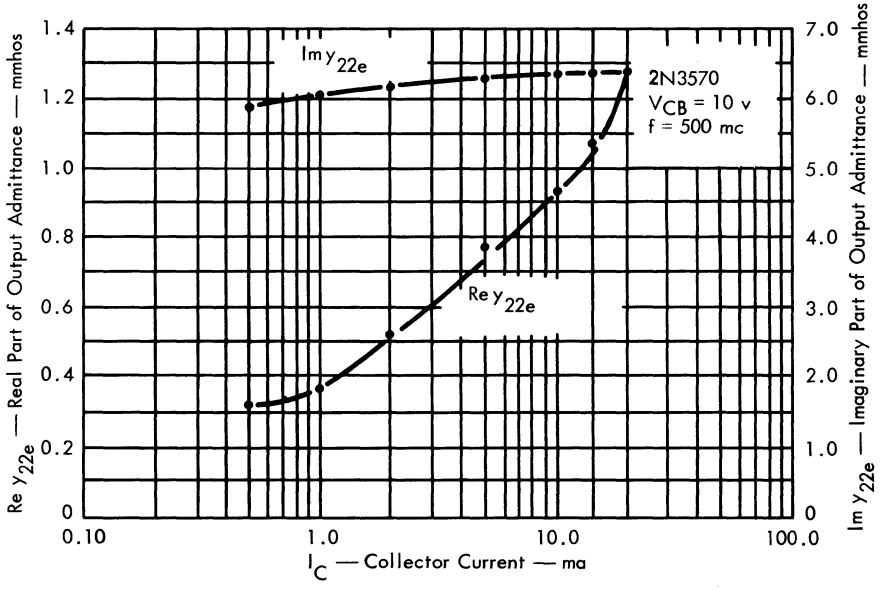

Fig. 4. 2N3570: Re y_{22e} and Im y_{22e} vs. I_C.

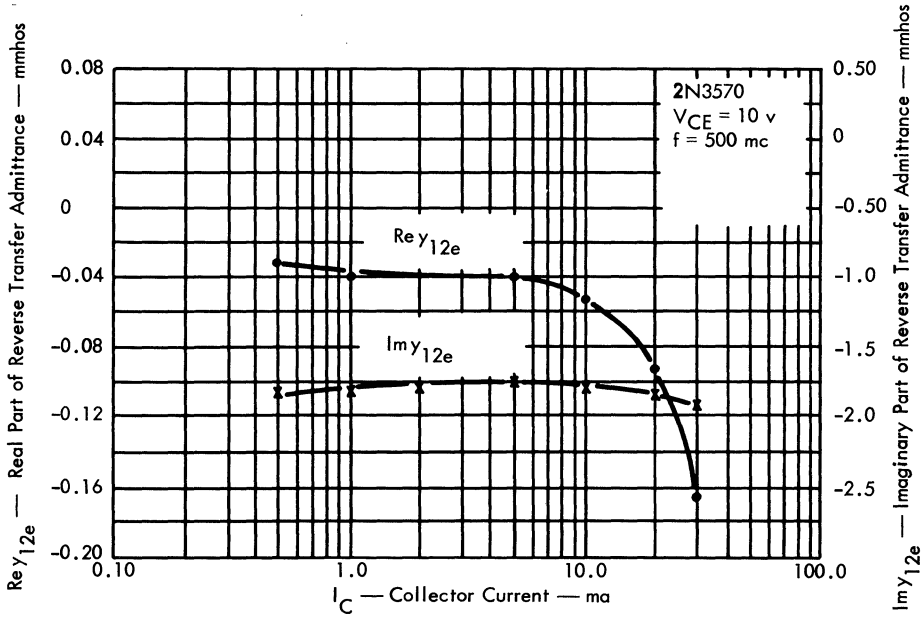

Fig. 5. 2N3570: Re y_{12e} and Im y_{12e} vs. I_C.

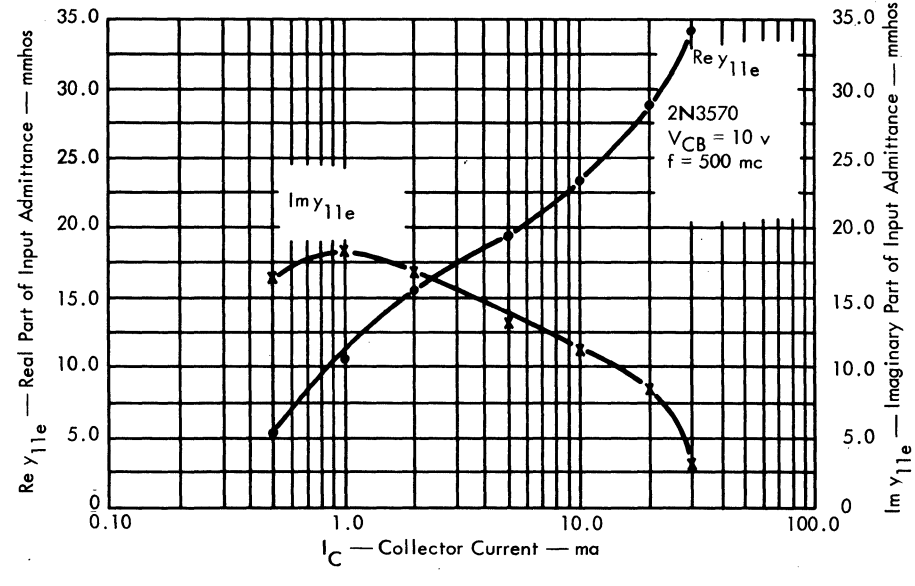

Fig. 6. 2N3570: Re y_{11e} and Im y_{11e} vs. I_C.

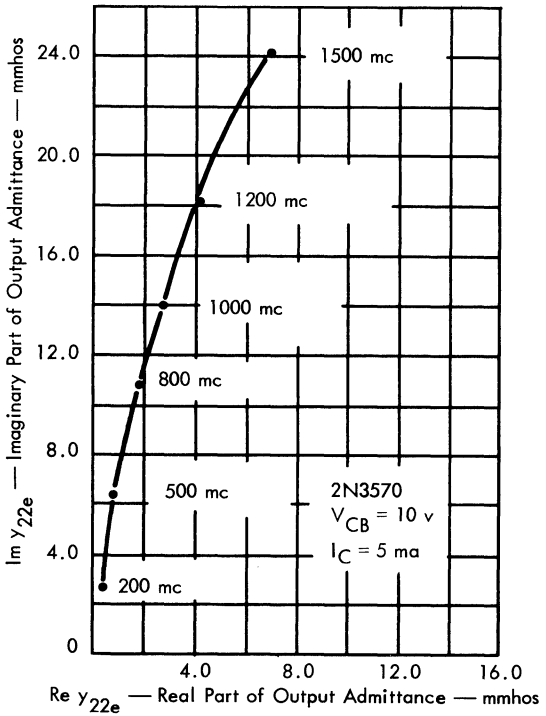

Fig. 7. 2N3570: Im y_{22e} vs. Re y_{22e}.

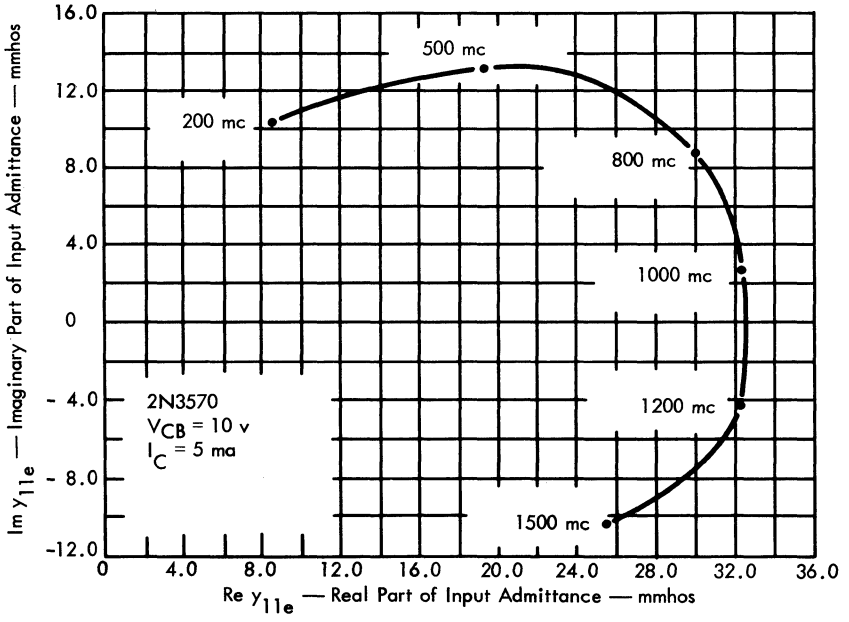

Fig. 8. 2N3570: Im y_{11e} vs. Re y_{11e}.

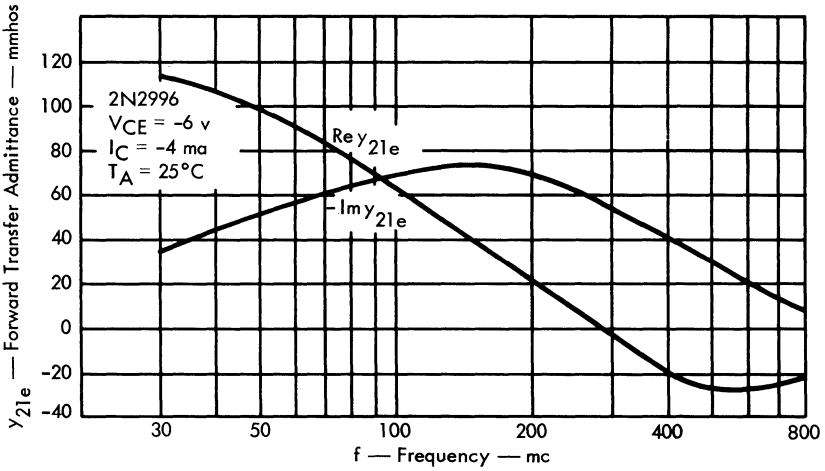

Fig. 9. 2N2996: y_{21e} vs. f.

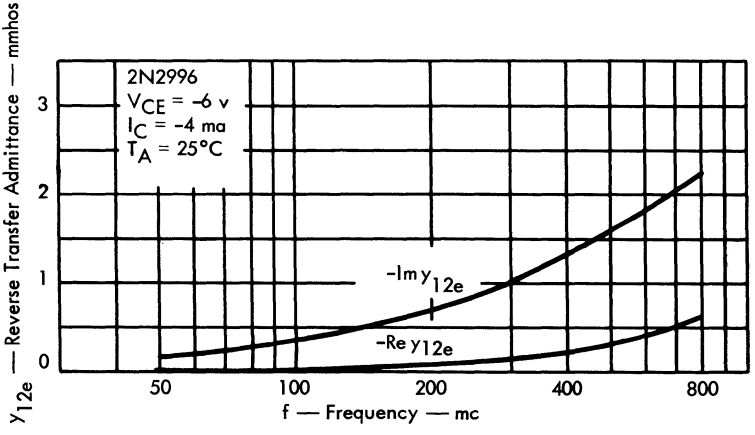

Fig. 10. 2N2996: y_{12e} vs. f.

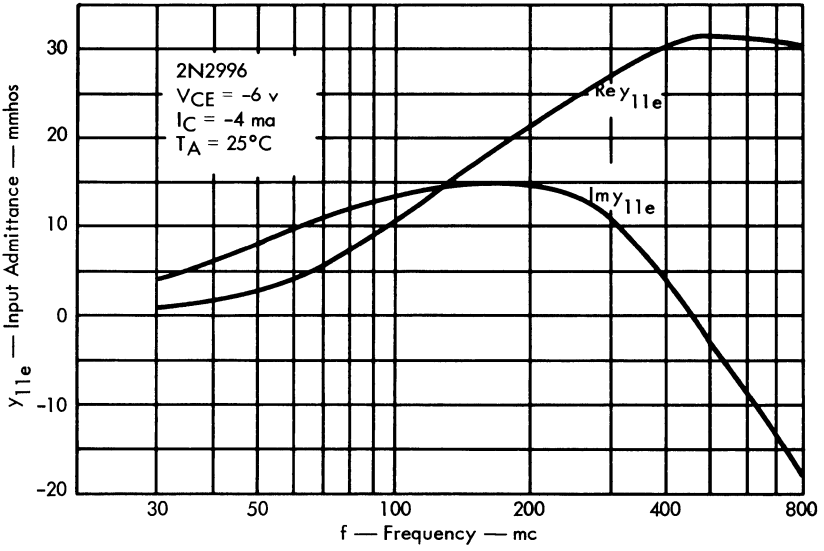

Fig. 11. 2N2996: y_{11e} vs. f.

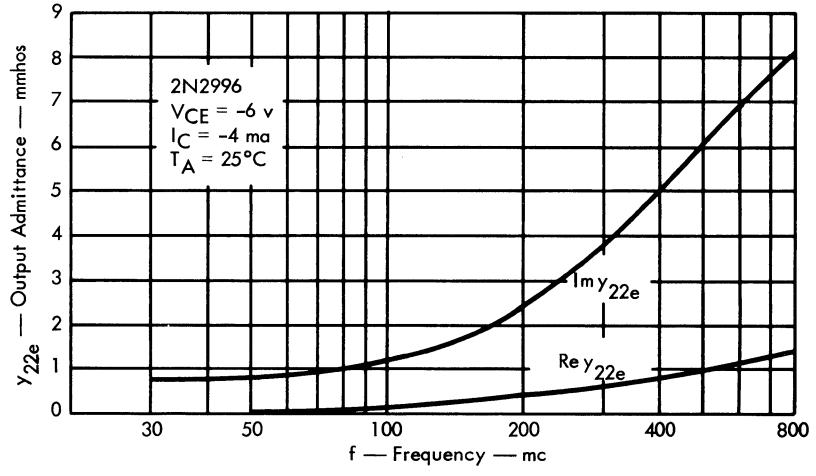

Fig. 12. 2N2996: y_{22e} vs. f.

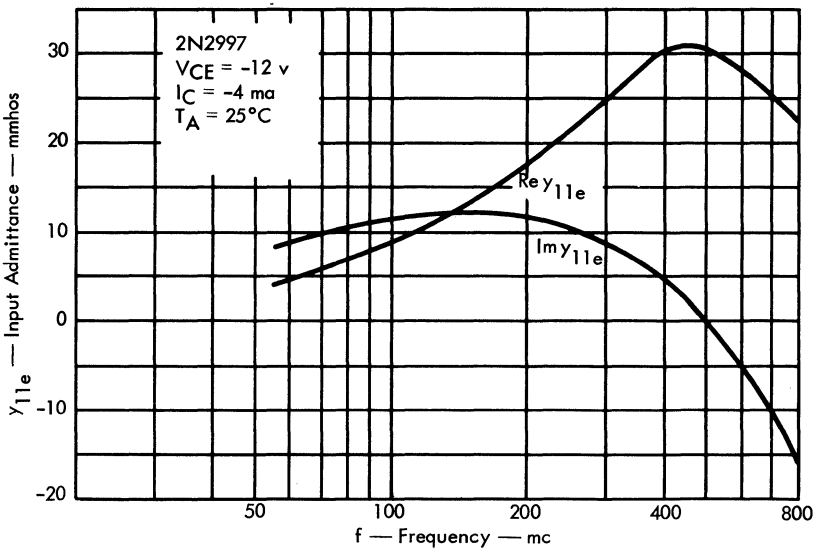

Fig. 13. 2N2997: y_{11e} vs. f.

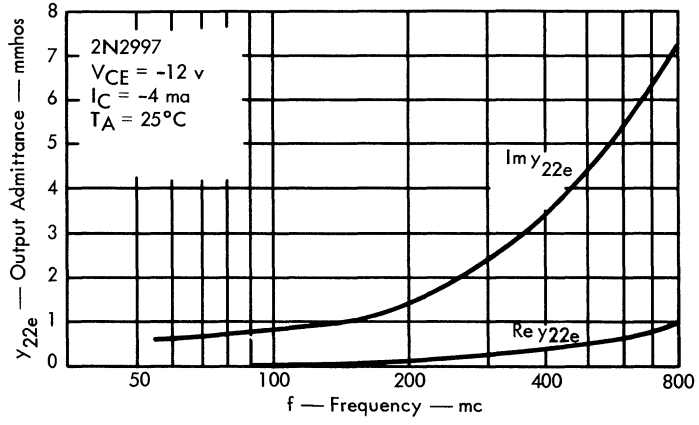

Fig. 14. 2N2997: y_{22e} vs. f.

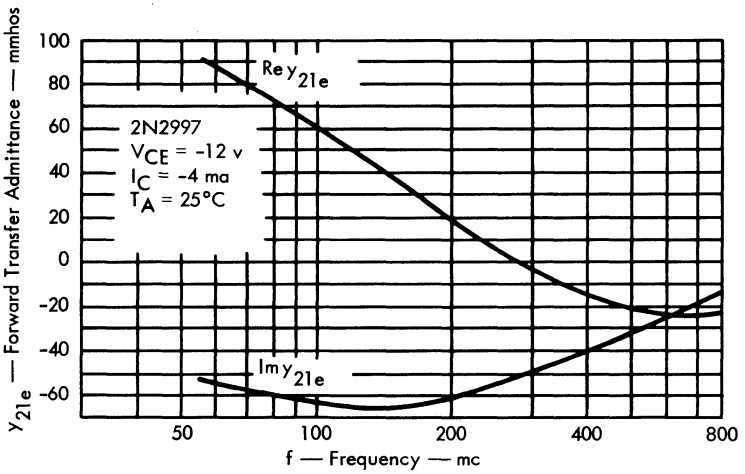

Fig. 15. 2N2997: y_{21e} vs. f.

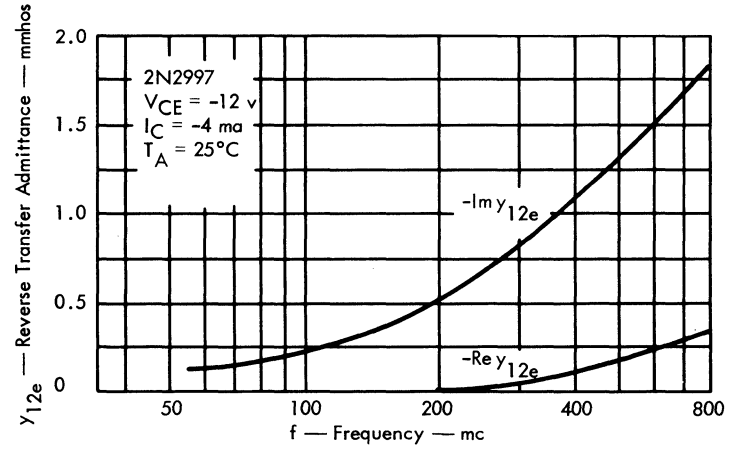

Fig. 16. 2N2997: y_{12e} vs. f.

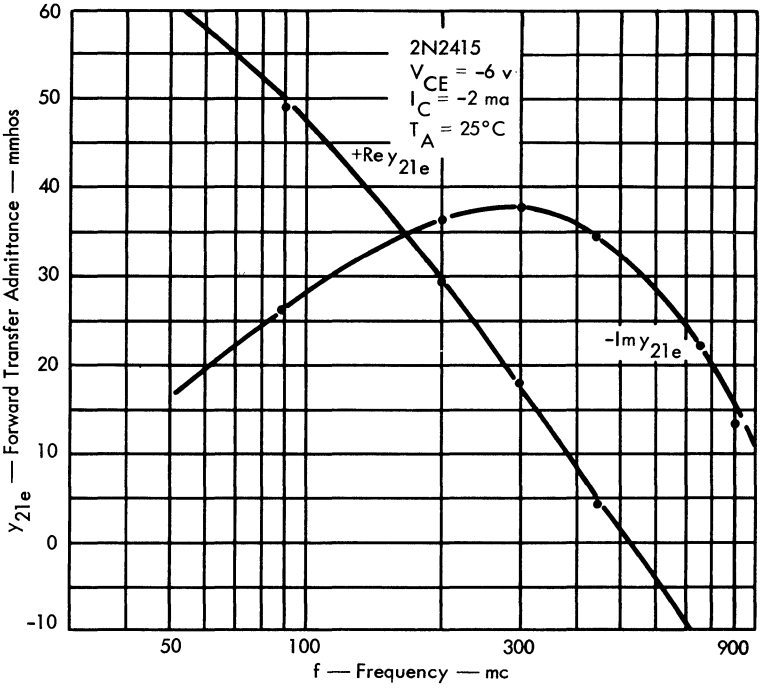

Fig. 17. 2N2415: y_{21e} vs. f.

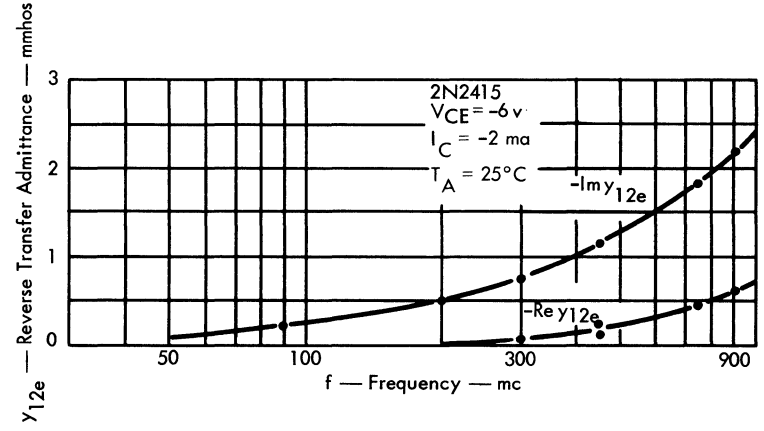

Fig. 18. 2N2415: y_{12e} vs. f.

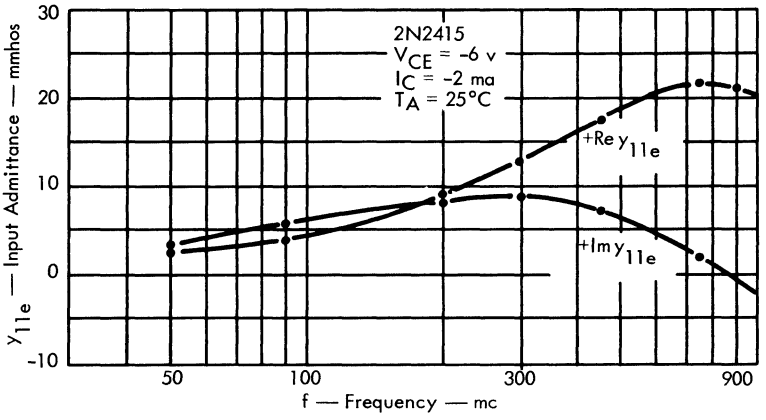

Fig. 19. 2N2415: y_{11e} vs. f.

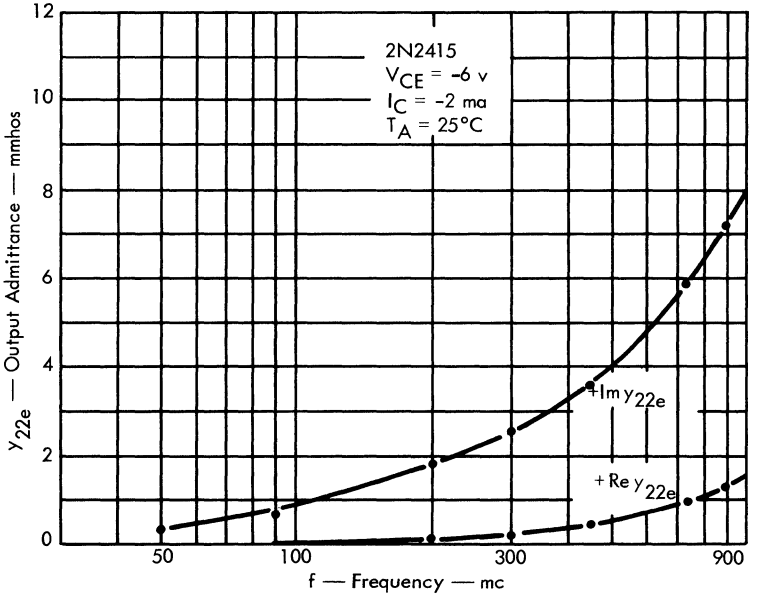

Fig. 20. 2N2415: y_{22e} vs. f.

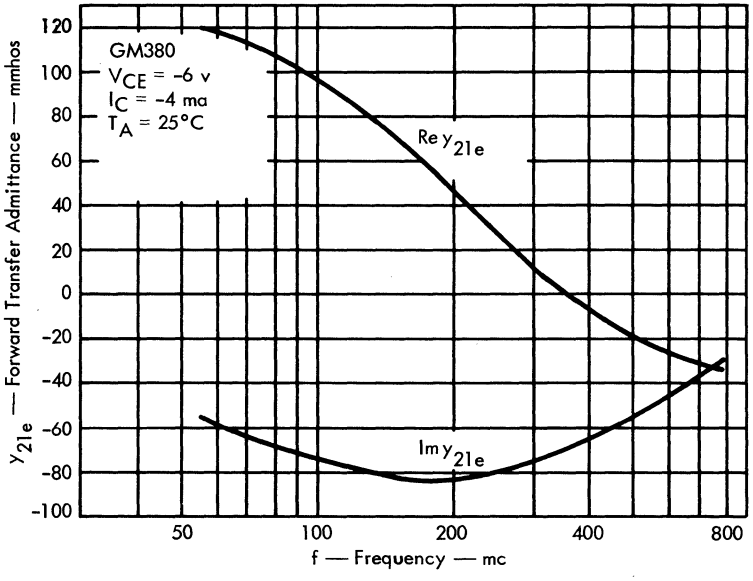

Fig. 21. GM380: y_{21e} vs. f.

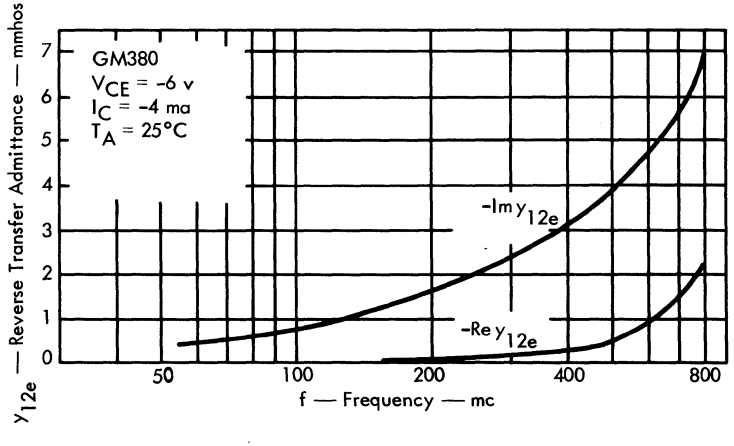

Fig. 22. GM380: y_{12e} vs. f.

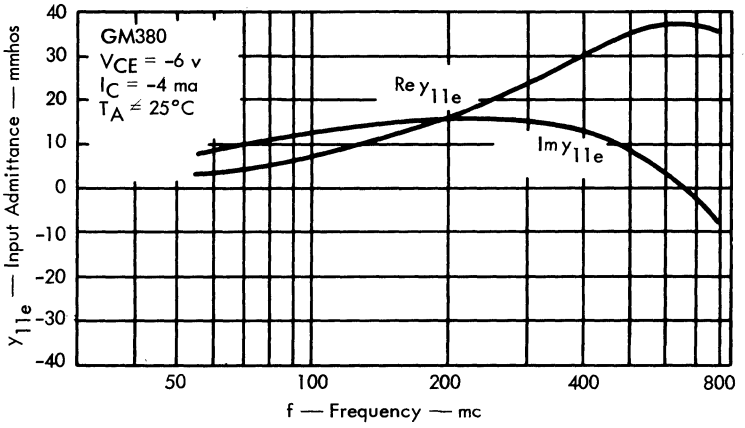

Fig. 23. GM380: y_{11e} vs. f.

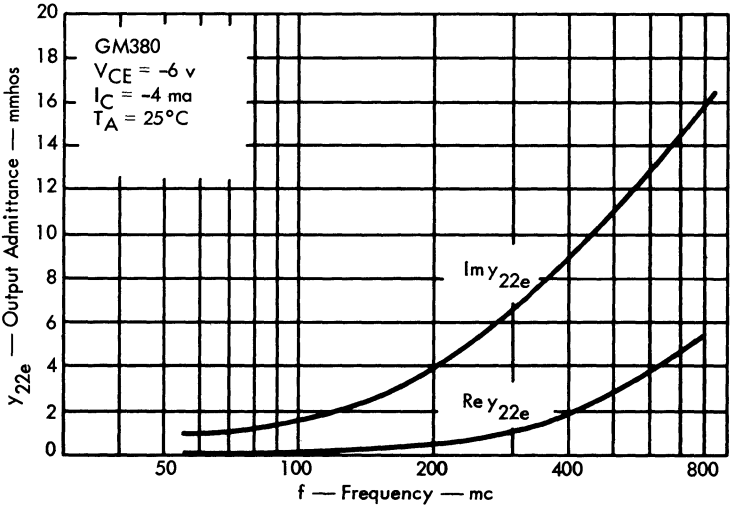

Fig. 24. GM380: y_{22e} vs. f.

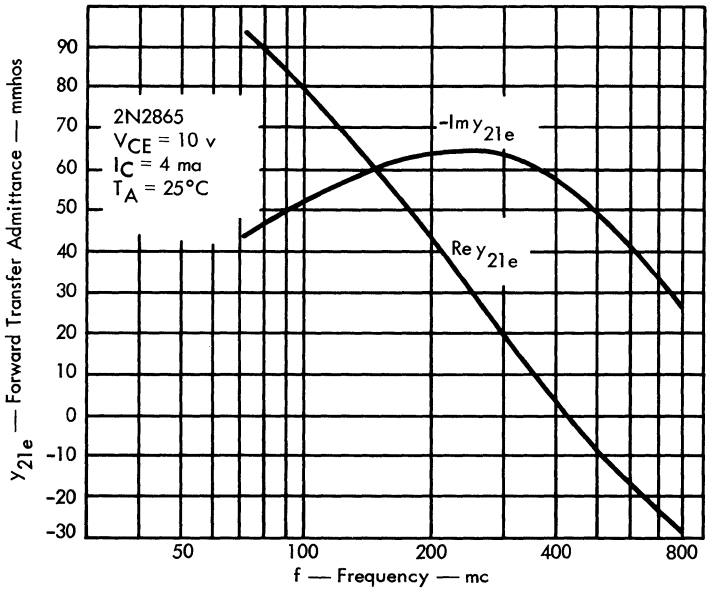

Fig. 25. 2N2865: y_{21e} vs. f.

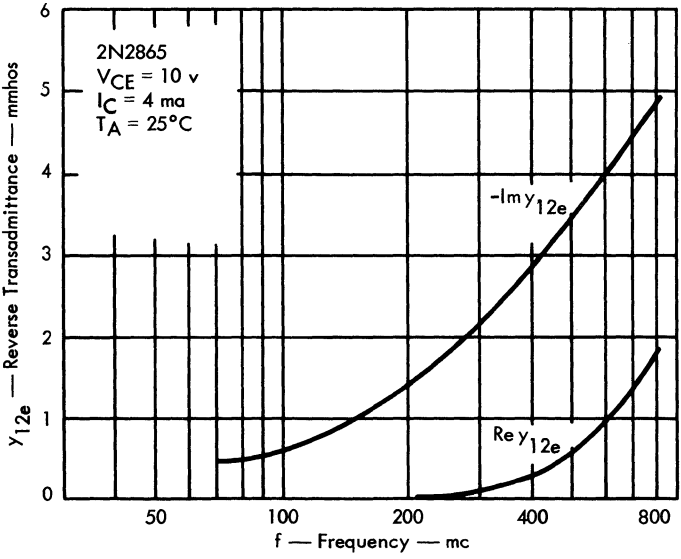

Fig. 26. 2N2865: y_{12e} vs. f.

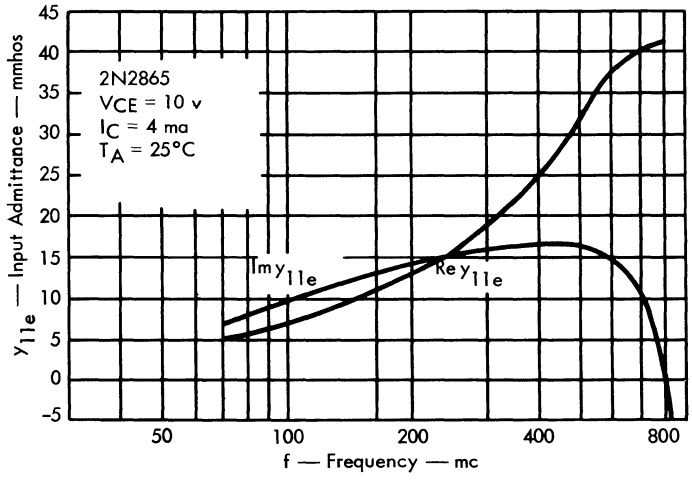

Fig. 27. 2N2865: y_{11e} vs. f.

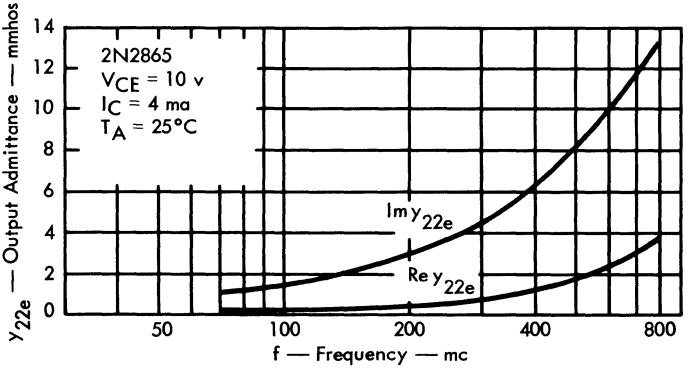

Fig. 28. 2N2865: y_{22e} vs. f.

This Central Automatic Recording and Testing facility (CART), designed and built by TI, automatically reads and records 10 parameters at two temperature levels on 1200 devices per hour.

4

Power Gain and Stability in Linear Active Two-ports

by George Johnson

INTRODUCTION

Characterization of high-frequency transistors may be accomplished by either of two methods. The first is based on a set of transistor internal parameters; they are derived from a suitable model, and can be related directly to the physical properties of the transistor. High-frequency circuit design based on this internal parameter method of transistor characterization has been well documented in the literature. The advantages of this method are ease of measurement of the internal parameters, speed and simplicity of analysis, and strong relationship to the physical device. One of the major disadvantages is that the equivalent circuit chosen may not be an accurate representation of the physical device over a particular high-frequency range because of simplifying approximations.

The second method is the two-port method. Because it emphasizes the measured terminal parameters rather than internal parameters in a specific structure, it exactly characterizes the linear active network. Principal advantages of this method are its applicability to any two-port active device, its freedom from any approximations that may have been made in arriving at a simple equivalent circuit model for the device, and all of the advantages of matrix analysis. The principal disadvantage is that information about the physical structure of the transistor is lost.

EQUIVALENT CIRCUITS

To establish a relationship between terminal parameters and internal parameters, consider the Giacoletta hybrid-π equivalent circuit shown in Fig. 1. This equivalent circuit is not necessarily a true representation of any given transistor at any given frequency, but it may be used to establish relationships between terminal parameters and internal parameters. The h and y parameters for this equivalent circuit are presented in Tables 1 and 2.

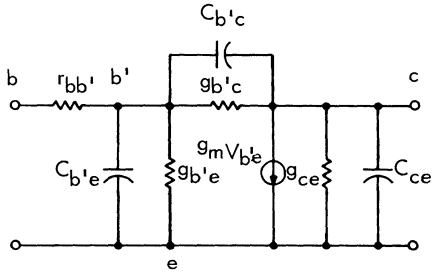

Fig. 1. Hybrid-π equivalent circuit.

These equations present the two-port parameters in terms of internal parameters of an equivalent circuit which has good correlation to the physical model. The base spreading resistance is accounted for by $r_{b'b}$, and the remaining structure represents the behavior of the intrinsic transistor. It is possible to establish still closer identity to the physical model by deriving the hybrid-π components in terms of the basic physical quantities such as diffusion lengths, base widths, doping densities, etc. However, for most purposes, the identities presented here will be quite satisfactory.

Pritchard has made certain simplifications to the equivalent circuit of Fig. 1. Figure 2 shows the approximate high-frequency equivalent circuit for junction transistors in the common-emitter configurations. The h parameters may be written by inspection when the condition $c_c << 1/\omega_t r_e'$ is used.

$$h_{ie} = \left(r_b' + \frac{\omega_t r_e'}{j\omega}\right) \text{ ohms} \tag{1}$$

$$h_{re} = \omega_t r_e' c_c \tag{2}$$

$$h_{fe} = -j\,\frac{\omega_t}{\omega} \tag{3}$$

$$h_{oe} = (\omega_t c_c + j\omega c_c) \text{ mhos} \tag{4}$$

The resulting y parameters are

$$y_{ie} = \frac{1}{r_b' - j(\omega_t/\omega) r_e'} \tag{5}$$

$$y_{re} = \frac{-\omega_t r_e' c_c}{r_b' - j(\omega_t/\omega) r_e'} \tag{6}$$

$$y_{fe} = -\frac{j(\omega_t/\omega)}{r_b' - j(\omega_t/\omega) r_e'} \tag{7}$$

$$y_{oe} = \frac{\omega_t c_c (r_b' + r_e') + j\omega c_c (r_b')}{r_b' - j(\omega_t/\omega) r_e'} \tag{8}$$

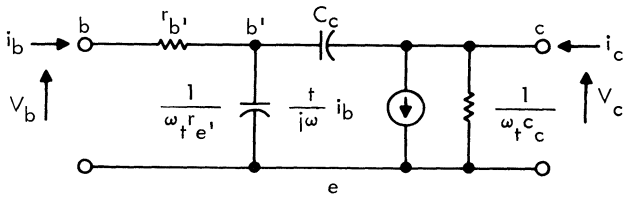

Fig. 2. Approximate high-frequency equivalent circuit of a junction transistor.

Table 1. h Parameters for the Hybrid- π Equivalent Circuit

$$h_{ie} = h'_{ie}\frac{1+\tau_1 s}{1+\tau_2 s}$$

where:

$$h'_{ie} = \frac{g_{bb'} + g_{b'e} + g_{b'c}}{g_{bb'}(g_{b'e} + g_{b'c})}$$

$$\tau_1 = \frac{C_{b'e} + C_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}}$$

$$\tau_2 = \frac{C_{b'e} + C_{b'c}}{g_{b'e} + g_{b'c}}$$

$$h_{re} = h'_{re}\frac{1+\tau_3 s}{1+\tau_4 s}$$

where:

$$h'_{re} = \frac{g_{b'c}}{g_{b'e} + g_{b'c}}$$

$$\tau_3 = \frac{C_{b'c}}{g_{b'c}}$$

$$\tau_4 = \frac{C_{b'e} + C_{b'c}}{g_{b'e} + g_{b'c}} = \tau_2$$

$$h_{fe} = h'_{fe}\frac{1-\tau_5 s}{1+\tau_6 s}$$

where:

$$h'_{fe} = \frac{g_m - g_{b'c}}{g_{b'e} + g_{b'c}}$$

$$\tau_5 = \frac{C_{b'c}}{g_m - g_{b'c}}$$

$$\tau_6 = \frac{C_{b'e} + C_{b'c}}{g_{b'c} + g_{b'e}} = \tau_4 = \tau_2$$

$$h_{oe} = h'_{oe1}\left(\frac{1+\tau_7 s}{1+\tau_8 s}\right) + h'_{oe2}(1+\tau_9 s)$$

where:

$$h'_{oe1} = \frac{(g_{b'e} + g_m)\, g_{b'c} + s^2\,(C_{b'c} C_{b'e})}{g_{b'e} + g_{b'c}}$$

$$h'_{oe2} = g_{ce}$$

$$\tau_7 = \frac{C_{b'c}(g_{b'e} + g_m) + C_{b'e} g_{b'c}}{(g_{b'e} + g_m)(g_{b'e}) + s^2\,(C_{b'c} C_{b'e})}$$

$$\tau_8 = \frac{C_{b'e} + C_{b'c}}{g_{b'e} + g_{b'c}}$$

$$\tau_9 = \frac{C_{ce}}{g_{ce}}$$

Table 2. y Parameters for the Hybrid- π Equivalent Circuit

$$y_{ie} = y'_{ie}\frac{1+\tau_2 s}{1+\tau_{10} s}$$

where:

$$y'_{ie} = \frac{g_{bb'}(g_{b'e} + g_{b'c})}{g_{bb'} + g_{b'e} + g_{b'c}}$$

$$\tau_2 = \frac{C_{b'e} + C_{b'c}}{g_{b'e} + g_{b'c}}$$

$$\tau_{10} = \frac{C_{b'e} + C_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}} = \tau_1$$

$$y_{re} = -y'_{re}\frac{1+\tau_3 s}{1+\tau_{10} s}$$

where:

$$y'_{re} = \frac{g_{bb'}\, g_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}}$$

$$\tau_3 = \frac{C_{b'c}}{g_{b'c}}$$

$$\tau_{10} = \frac{C_{b'e} + C_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}} = \tau_1$$

$$y_{fe} = \frac{y'_{fe1}}{(1+\tau_{10} s)} - y'_{fe2}\frac{(1+\tau_3 s)}{(1+\tau_{10} s)}$$

where:

$$y'_{fe1} = \frac{g_{bb'}\, g_m}{g_{bb'} + g_{b'e} + g_{b'c}}$$

$$y'_{fe2} = \frac{g_{bb'}\, g_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}}$$

$$\tau_3 = \frac{C_{b'c}}{g_{b'c}}$$

$$\tau_{10} = \frac{C_{b'e} + C_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}} = \tau_1$$

$$y_{oe} = y'_{oe1}(1+\tau_9 s) + y'_{oe2}\frac{(1+\tau_3 s)(1+\tau_{11} s)}{(1+\tau_{10} s)}$$

where:

$$y'_{oe1} = g_{ce}$$

$$y'_{oe2} = \frac{(g_{bb'} + g_m + g_{b'e})\, g_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}}$$

$$\tau_9 = \frac{C_{ce}}{g_{ce}}$$

$$\tau_{10} = \frac{C_{b'e} + C_{b'c}}{g_{bb'} + g_{b'e} + g_{b'c}}$$

$$\tau_{11} = \frac{C_{b'e}}{g_{bb'} + g_m + g_{b'e}}$$

These equations establish the approximate correlation between internal parameters and terminal parameters. Since most of these expressions are rather involved, it is simpler to express circuit design equations in terms of the terminal parameters. The discussion of stability and power gain that follows is therefore based on these terminal parameters.

POWER GAIN EQUATIONS

The power gain of a Linear Active Network (LAN) may be specified in many ways. This section defines some of the more important power gain expressions and shows their derivations.

Power Gain. The term G_p is defined as:

$$G_p = \text{Power gain} = \frac{\text{Power delivered to load}}{\text{Power delivered to input of LAN}}$$

$$G_p = \frac{|I_2|^2 \operatorname{Re}(Z_L)}{|I_1|^2 \operatorname{Re}(Z_{in})} \tag{9}$$

This power gain is independent of the generator impedance and allows the gain of a LAN to be evaluated as a function of load. It is derived as follows: from two-port theory,

$$\frac{I_2}{I_1} = \frac{Y_L h_{21}}{Y_L + h_{22}} \tag{10}$$

$$\operatorname{Re}(Z_L) = R_L \tag{11}$$

$$\operatorname{Re}(Z_{in}) = \operatorname{Re}\left(h_{11} - \frac{h_{12} h_{21}}{h_{22} + Y_L}\right) \tag{12}$$

Combining these gives

$$G_p = \frac{|(Y_L)|^2 |h_{21}|^2 \operatorname{Re}(Z_L)}{|Y_L + h_{22}|^2 \operatorname{Re}\left(h_{11} - \frac{h_{12} h_{21}}{h_{22} + Y_L}\right)} = \frac{|h_{21}|^2 \operatorname{Re}(Y_L)}{|Y_L + h_{22}|^2 \operatorname{Re}\left(h_{11} - \frac{h_{12} h_{21}}{h_{22} + Y_L}\right)} \tag{13}$$

As with all the power gain terms to be derived later, this expression is general in form. Therefore, Eq. (14) may be written

$$G_p = \frac{|y_{21}|^2 \operatorname{Re}(Y_L)}{|Y_L + y_{22}|^2 \operatorname{Re}\left(y_{11} - \frac{y_{12} y_{21}}{y_{22} + Y_L}\right)} \tag{14}$$

The general expression is given by Eq. (15)

$$G_p = \frac{|K_{21}|^2 M_{Lr}}{|K_{22} + M_L|^2 \operatorname{Re}\left(K_{11} - \frac{K_{12} K_{21}}{K_{22} + M_L}\right)} \tag{15}$$

A special form of this power gain is obtained by conjugately matching the load Y_L to y_{22}. Using

$$Y_L^* = y_{22} \tag{16}$$

in the G_p expression gives:

$$G_p' = \frac{|y_{21}|^2 M_{Lr}}{|Y_{Lr} - \text{Im}(Y_L) + y_{22r} + \text{Im}(y_{22})|^2 \text{Re}\left(y_{11} - \frac{y_{12}y_{21}}{\text{Re}(y_{22}) + \text{Im}(y_{22}) + \text{Re}(Y_L) - \text{Im}(Y_L)}\right)} \quad (17)$$

$$G_p' = G_{oo} = \frac{|y_{21}|^2}{4g_{11}g_{22} - 2\text{Re}(y_{12}y_{21})} \quad (18)$$

The term G_{oo} is the basic gain expression in the Linvill method. It serves as a useful figure of merit.

Transducer Gain. The transducer gain is the ratio of the power the LAN delivers to a load, divided by the power the generator would deliver to that load, if the load were conjugately matched to the generator. The maximum available power from the generator is

$$P_{AVS} = \frac{|E_g|^2}{4\text{Re}(Zg)} \quad (19)$$

The output power is

$$P_{out} = |V_2|^2 \text{Re}(Y_L) \quad (20)$$

Therefore, the transducer gain is

$$G_T = \frac{4\text{Re}(Z_g)\text{Re}(Y_L)|V_2|^2}{|E_g|^2} \quad (21)$$

Consider the LAN shown in Fig. 3. From two-port theory,

$$E_g = (h_{11} + Z_g)I_1 + h_{12}V_2 \quad (22)$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \quad (23)$$

$$V_2 = \frac{\begin{vmatrix} h_{11} + Z_g & E_g \\ h_{21} & I_2 \end{vmatrix}}{\begin{vmatrix} h_{11} + Z_g & h_{12} \\ h_{21} & h_{22} \end{vmatrix}} = \frac{h_{11} + Z_g}{\Delta h} I_2 - \frac{h_{21}}{\Delta h} E_g \quad (24)$$

But $-I_2 = V_2 Y_L$, so that

$$V_2 = -\left(\frac{h_{11} + Z_g}{\Delta h}\right)(V_2 Y_L) - \left(\frac{h_{21}}{\Delta h}\right) E_g \quad (25)$$

$$V_2\left[1 + \frac{(h_{11} + Z_g)}{\Delta h} Y_L\right] = -\left(\frac{h_{21}}{\Delta h}\right) E_g \quad (26)$$

$$V_2\left[\frac{\Delta h + (h_{11} + Z_g) Y_L}{\Delta h}\right] = -\left(\frac{h_{21}}{\Delta h}\right) E_g \quad (27)$$

$$\frac{V_2}{E_g} = \frac{-h_{21}}{(h_{11} + Z_g) Y_L + \Delta h} = \frac{-h_{21}}{(h_{11} + Z_g)(h_{22} + Y_L) - h_{12}h_{21}} \quad (28)$$

$$\left|\frac{V_2}{E_g}\right|^2 = \frac{|h_{21}|^2}{|(h_{11} + Z_g)(h_{22} + Y_L) - h_{12}h_{21}|^2} \quad (29)$$

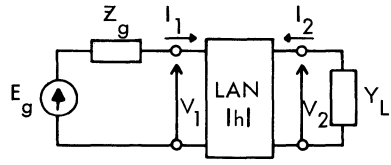

Fig. 3. General two-port.

Therefore
$$G_T = \frac{4\mathrm{Re}(Z_g)\,\mathrm{Re}(Y_L)\,|\,h_{21}\,|^2}{|\,(h_{11}+Z_g)(h_{22}+Y_L)-h_{12}h_{21}\,|^2} \tag{30}$$

The general form is given by Eq. (31)

$$G_T = \frac{4\,|\,K_{21}\,|^2\,\mathrm{Re}(M_L)\,\mathrm{Re}(M_g)}{|\,(K_{11}+M_g)(K_{22}+M_L)-K_{12}K_{21}\,|^2} \tag{31}$$

Maximum Available Power Gain. The term "maximum available power gain" cannot be discussed without discussing stability. Certain terminations may cause a linear active two-port that is not unilateral to oscillate. Such a two-port is therefore termed potentially unstable. If no such terminations are possible, then it is unconditionally stable. If it is unconditionally stable the maximum available gain G_{max} may be achieved by conjugately matching the generator to the input immittance of the terminated LAN and conjugately matching the load to the output immittance with the input network in place. If the LAN is potentially unstable, the value of G_{max} is unbounded, and the term becomes meaningless. The variation of G_{max} vs frequency is shown in Fig. 4.

To derive the expression for G_{max}, the expression for transducer gain must be differentiated with respect to the real and imaginary parts of the generator and load immittance and the four derivatives set equal to zero. They may then be substituted into the transducer gain equation to give the maximum available power gain. This is not a difficult operation, but since the technique of obtaining G_{max} by the Linvill method is the one used in later design examples, only the results of the differentiation are presented now.

The imaginary parts of the generator and load that maximize the power gain of an unconditionally stable two-port are:

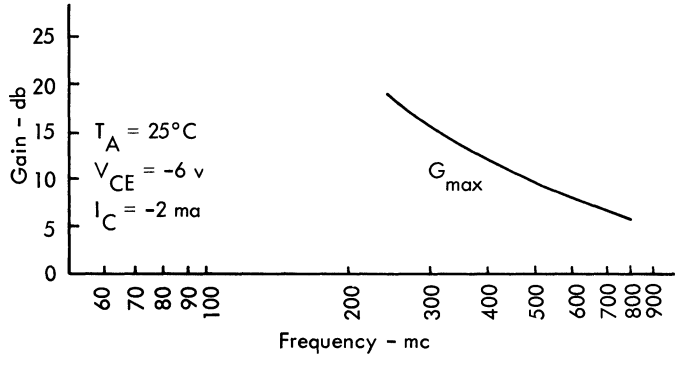

Fig. 4. G_{max} versus frequency.

$$B_g = -\mathrm{Im}(y_{11}) + \frac{\mathrm{Im}(y_{12}y_{21})}{2\mathrm{Re}(y_{22})} \tag{32}$$

$$B_L = -\mathrm{Im}(y_{22}) + \frac{\mathrm{Im}(y_{12}y_{21})}{2\mathrm{Re}(y_{11})} \tag{33}$$

The real parts of the generator and load that maximize the power gain of an unconditionally stable two-port are:

$$G_g = \frac{1}{2\mathrm{Re}(y_{22})}\left\{[2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2\right\}^{1/2} \tag{34}$$

$$G_L = \frac{1}{2\mathrm{Re}(y_{11})}\left\{[2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2\right\}^{1/2} \tag{35}$$

Substituting these values in the equation for transducer gain gives the expression for G_{max}:

$$G_{max} = \frac{|y_{21}|^2}{2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) + \left\{[2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2\right\}^{1/2}} \tag{36}$$

Maximum Available Gain. If the effect of the inverse feedback of the two-port is neglected, then the power gain obtained when the input and output are conjugately matched to the generator and load is the maximum available gain MAG. As might be expected, the expression G_{max} is meaningless unless the active device is unconditionally stable. Since the effect of the inverse feedback ratio will be neglected, the condition of unconditional stability is already satisfied. And, since G_{max} was obtained under the conditions of conjugate match at both ports, it is only necessary to substitute $y_{12} = 0$ in the G_{max} expression to obtain the equation for MAG. This substitution into Eq. (36) yields:

$$\mathrm{MAG} = \frac{|y_{21}|^2}{4\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22})} = \frac{|h_{21}|^2}{4\mathrm{Re}(h_{11})\,\mathrm{Re}(h_{22})} \tag{37}$$

This term, because it involves easily measurable parameters, is used as a figure of merit for transistor performance. It is best to use MAG only in this sense.

To relate this form of power gain back to the device parameters, the equivalent circuit of Fig. 5 is used. As is evident from this equivalent circuit, the common-emitter input impedance at high frequencies is essentially r_b'. Since the effect of internal feedback is neglected, the following derivation may be performed:

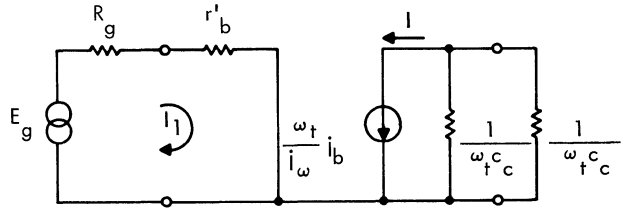

Fig. 5. High-frequency simplified equivalent circuit neglecting reverse internal feedback.

$$P_{AVS} = \frac{E_g^2}{4R_g} = \frac{E_g^2}{4r_b'} \tag{38}$$

where $R_g = r_b'$ under the condition of conjugate match.

but $$I_1 = \frac{E_g}{2r_b'} \tag{39}$$

and $$E_g^2 = 2r_b'^2 I_1^2 = 4r_b'^2 I_1^2 \tag{40}$$

so $$P_{AVg} = \frac{I_1^2 4(r_b')^2}{4r_b'} = I_1^2 r_b' \tag{41}$$

The maximum available output power is:

$$E_{Load} = \frac{-I}{2\omega_t C_c} \tag{42}$$

$$P = E_L^2 \omega_t C_c = \frac{I^2(\omega_t C_c)}{4(\omega_t C_c)^2} \tag{43}$$

The resulting power gain is

$$MAG = \frac{I^2}{4\omega_t C_c} \frac{1}{I_1^2 r_b'} = \frac{\left(\frac{I}{I_1}\right)^2}{4r_b'\omega_t C_c} \tag{44}$$

But $(I/I_1)^2$ is actually the current gain squared, which according to Fig. 5 is:

$$\frac{|\omega_t|^2}{|j\omega|} = \frac{\omega_t^2}{\omega^2} \tag{45}$$

Substituting Eq. (45) into Eq. (44) gives

$$MAG = \frac{\omega_t}{\omega^2 4r_b' C_c} \tag{46}$$

The familiar expression for f_{max} is easily obtained from MAG; at f_{max}, MAG = 1, so:

$$1 = \frac{\omega_t}{\omega^2 4r_b' C_c} = \frac{f_t}{(2\pi) f^2 4r_b' C_c} = \frac{f_t}{8\pi r_b' C_c f^2} \tag{47}$$

Solving for f, and calling this f_{max}:

$$f_{max} = \sqrt{\frac{f_t}{8\pi r_b' C_c}} \tag{48}$$

Forward-to-reverse Gain Ratio. Before leaving the subject of MAG it is well to mention another interesting and very similar expression called the forward-to-reverse gain ratio. It has just been shown that the MAG in the forward direction is:

$$MAG_F = \frac{|y_{21}|^2}{4g_{11}g_{22}} \tag{49}$$

The subscript F is used to denote forward MAG. A similar expression exists in the reverse direction:

$$MAG_R = \frac{|y_{12}|^2}{4g_{22}\,g_{11}} \tag{50}$$

The ratio of these two equations yields the forward-to-reverse gain ratio.

$$MAG_{F\text{-}R} = \frac{|y_{21}|^2}{|y_{12}|}$$

This expression is useful in specifying an upper bound on the useful frequency range. For example, on the 2N2415 this is set at $MAG_{F\text{-}R} = 20$ db at 800 mc. This means that the difference in the forward and reverse gain has degenerated to 20 db at 800 mc, a ratio of 100 to 1. This limit is completely arbitrary and could have been set at any desired value. Any higher-frequency application for the 2N2415 would mean:

1. the gain is essentially impedance gain only, and
2. the noise figure is becoming equal to the gain.

These conditions will not, in general, be true for other transistors, but the concept of limiting the upper frequency of *primary application* in this way is a simple and useful way to compare transistors in the upper-frequency regions.

Unilateral Power Gain. Neutralization of internal reverse feedback can be achieved by an external network as shown in Fig. 6. The a and p subscripts denote active and passive parameters. The composite network will have these terms:

$$y_{11c} = y_{11a} + y_{12p} \tag{51}$$

$$y_{22c} = y_{22a} + y_{12p} \tag{52}$$

$$y_{21c} = y_{21a} - y_{12p} \tag{53}$$

$$y_{12c} = y_{12a} - y_{12p} \tag{54}$$

When $|y_{12a}| = |y_{12p}|$, the value of y_{12c} is 0, and with a conjugate match of source and load to y_{11c} and y_{22c} respectively, the value of power gain is:

$$G_U = \frac{|y_{21a} - y_{12p}|^2}{4(g_{11a} + g_{12p})(g_{22a} + g_{12p})} \tag{55}$$

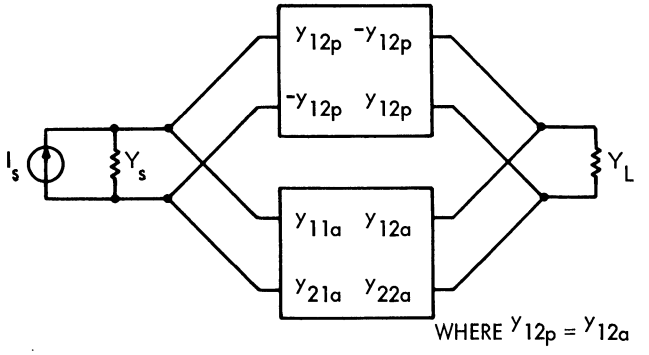

Fig. 6. A unilateralized two-port.

In other words, G_U is the power gain obtained when a network is used to just offset the internal feedback to develop a unilateral composite structure. The transducer gain can be treated in the same way. It is easy to see this expression as the unilateral transducer gain G_{TU}.

$$G_{TU} = \frac{4 \mid y_{21a} - y_{12p} \mid^2 G_S G_L}{\mid (Y_S + y_{11a} + y_{12p})(Y_L + y_{22a} + y_{12p}) \mid^2} \tag{56}$$

Neutralized Power Gain. If the condition

$$\mid y_{12a} \mid = \mid y_{12p} \mid \tag{57}$$

is not completely established, the resulting structure will be only partially unilateral because only part of the internal feedback is compensated. Under these conditions the composite admittance parameters are substituted into any of the previous power gain expressions and the gain is referred to as neutralized gain G_N.

Maximum Stable Power Gain. A special type of power gain term should be mentioned. It has been shown that G_{max} is only defined when the transistor is unconditionally stable. It is unconditionally stable if $C < 1$, where the inherent stability factor C is defined by

$$C = \frac{\mid y_{12}y_{21} \mid}{2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21})} \tag{58}$$

C is shown vs frequency in Fig. 7. At the exact frequency where $C = 1$, the transistor is on the threshold between potential instability and unconditional stability. The following derivation illustrates the interesting fact that G_{max} at this point $(C = 1)$ is given by

$$G_C = \frac{\mid y_{21} \mid}{\mid y_{12} \mid} \tag{59}$$

The derivation is as follows:

$$G_{max} = \frac{2[1 - (1 - C^2)^{1/2}] \mid y_{21} \mid^2}{[4g_{11}g_{22} - 2\mathrm{Re}(y_{12}y_{21})]C^2} = \frac{\mid y_{21} \mid^2}{2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21})} \tag{60}$$

But if $C = 1$, then

$$2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) = \mid y_{12}y_{21} \mid \tag{61}$$

Substituting this into the previous expression gives:

$$G_C = \frac{\mid y_{21} \mid}{\mid y_{11} \mid} = G_{max} \text{ at the frequency where } C = 1$$

This gain factor serves as a useful figure of merit when specified with the frequency at which $C = 1$. Figure 8 shows that the 2N2415 has a $G_C = 18.5$ db at 245 mc.

POWER GAIN CONSIDERATIONS

Consider the comparison of the power gain G_p and the transducer gain G_T. The transducer gain is the ratio of power the transistor delivers to the load over the power the generator would deliver to that load, were the load conjugately matched to the generator. If we conjugately match the input of the LAN to the generator, then G_p becomes G_T. If the input and source are not quite conjugately matched, then G_p will be slightly greater than G_T for identical output levels.

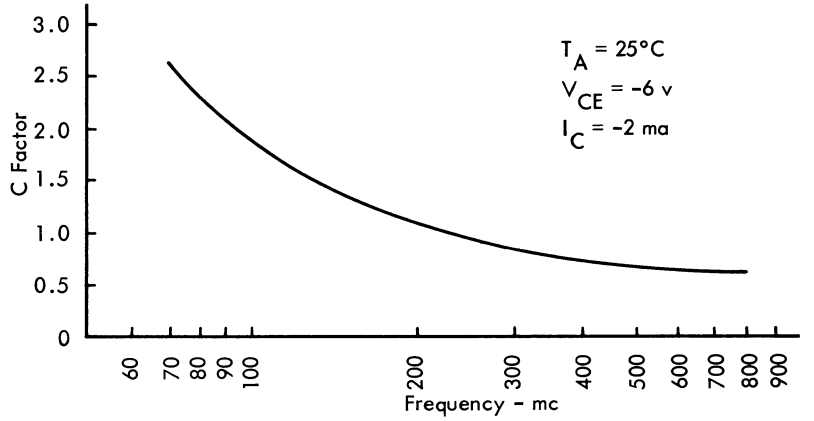

Figure 7

Power gain G_p is dependent on the transistor two-port parameters and the load. Therefore, to be complete, a specification of G_p must be accompanied by the value of M_L, the general form of the real part of the load immittance. Transducer gain must have the source and load specified to be meaningful.

The value of G_{max} is dependent only on the device parameters and, when the device is unconditionally stable, gives an accurate indication of the upper gain limit of a transistor. It should be possible to achieve this value minus insertion loss of interstages. However, as the gain y_{21}/y_{12} is approached, the inherent stability decreases. In other words, moving back in frequency along the G_{max} line of Fig. 8, the inherent stability is decreasing so that at the value y_{21}/y_{12}, the critical factor is unity.

The transistor is then on the threshold of potential instability. Since G_{max} requires a conjugate match to input and output it is quite clear that if any change anywhere in the circuit occurs then actual oscillation will occur. Therefore, because of the random nature of these disturbances in any parameter of the system, there is a practical limit to how close y_{21}/y_{12} may be approached. Figure 8 shows the

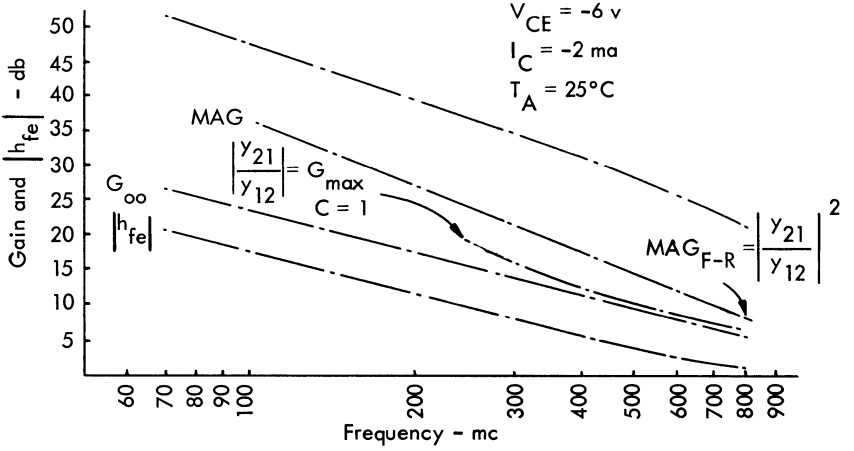

Figure 8

comparison of $|h_{fe}|$, G_{oo}, G_{max}, MAG, and $MAG_{F\text{-}R}$ for the common-emitter 2N2415. Curves for the common-base connection may be developed in a similar way.

STABILITY CONCEPTS

There are many approaches to the analysis of amplifier stability. One approach is based on the study of the conditions that cause the (transducer) gain to become infinite. Another approach is to examine the nature of the components of the transient response of the system; in other words, we are interested in whether the system has any natural frequencies. Still another technique is due to Nyquist. Each of these approaches has its own advantages, yet all are common because all the information about the stability of a system is contained in the characteristic equation describing that system.

In the case of the gain analysis, the characteristic equation (or a form of it) appears in the denominator of the gain equation. The examination of the transient response resolves to a problem of locating the roots of the system equation (characteristic equation) and deciding on the basis of the location of the roots whether the response to a transient will die out or not. When the Nyquist technique is used, one examines the locus of the value of E_{out}/E_{source} corresponding to the locus of s in the complex frequency plane. However, the denominator of E_{out}/E_{source} is the familiar characteristic equation of the system. Therefore, one of the most natural ways of examining stability is to examine the characteristic equation describing the system.

SYSTEM STABILITY

There are many ways of obtaining the characteristic equation of a system. Consider the active two-terminal pair shown in Fig. 9. Assume that we characterize this network by y parameters. The matrix is:

$$I_1 = y_{11} E_1 + y_{12} E_2 \tag{62}$$

$$I_2 = y_{21} E_1 + y_{22} E_2 \tag{63}$$

$$I_1 = -Y_g E_1 \tag{64}$$

$$I_2 = -Y_L E_2 \tag{65}$$

Now substituting these back into the matrix set

$$0 = (y_{11} + Y_g)\, E_1 + y_{12} E_2 \tag{66}$$

$$0 = y_{21} E_1 + (y_{22} + Y_L)\, E_2 \tag{67}$$

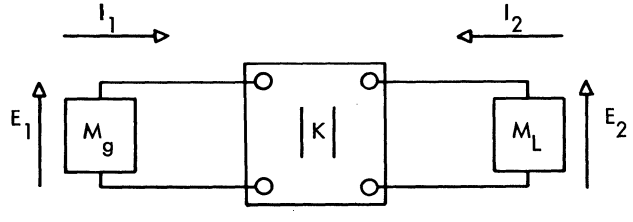

Fig. 9. A general active two-terminal pair with no external signal.

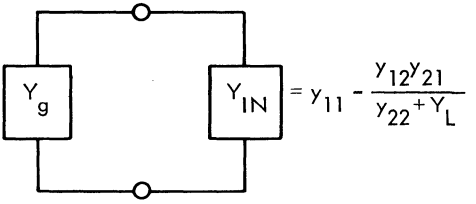

Fig. 10. Input node immittance.

Now, for the condition in which $E_1 = E_2 \neq 0$, the solution of this set is

$$(y_{11} + Y_g)(y_{22} + Y_L) - y_{12}y_{21} = 0 \qquad (68)$$

This is the system determinant or characteristic equation. It should be obvious that this is also the sum of the input admittance from the input node equated to zero. See Fig. 10.

TESTS FOR STABILITY

If a testing procedure is to be effective in determining whether a characteristic equation represents a stable system or not, it must be simple, quick, and not yield any more information than necessary. It can be shown that if any roots of the characteristic equation exist in the right half of the complex frequency plane, the system will be unstable. Since the terms y_{11}, y_{12}, y_{21}, y_{22}, Y_g, and Y_L may all be expressed as functions of the complex frequency variable s, the characteristic equation is of the form $F(s) = 0$. Now if the system represented by $F(s)$ is stable, then $F(s)$ must have no roots in the right-half plane. In other words, it must be a Hurwitz polynomial. A polynomial of the form

$$F(s) = A_0 + A_1s + A_2s^2 + A_3s^3 + \ldots A_{n-1}s^{n-1} + A_ns^n \qquad (69)$$

is Hurwitz if:

1. all the coefficients are positive and real,
2. there are no missing terms in s, and
3. it contains no roots on the j-axis or in the right-half plane.

The first two conditions may be checked by inspection. If these are satisfied, then testing may be continued to determine whether there are any right-half plane roots.

One way to test a polynomial for Hurwitz character is to form a determinant of its coefficients as shown in Fig. 11. The indices of the letter A in each row decrease by one, element by element from left to right. The indices of A in each column increase by two, element by element from top to bottom. Letters with negative indices or indices greater than n are replaced by zeros. If, and only if, each of the principal minors of the determinant is *positive* (if any of them is zero, imaginary roots are indicated), the polynomial is Hurwitz.

A_1	A_0	0	0	. . . 0
A_3	A_2	A_1	A_0	. . . 0
A_5	A_4	A_3	A_2	. . . 0
A_7	A_6	A_5	A_4	. . . 0
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
0	0	0	0	0

Fig. 11. Determinant of coefficients of Eq. (69).

The above tests simply indicate whether there are any roots on the $j\omega$ axis or whether there are any roots in the right-half plane. If the Hurwitz test shows all principal minors to be positive, the system is stable. If no roots are in the right-half plane and any roots are on the imaginary axis, the system is critically stable. If any roots are in the right-half plane, one of the principal minors will turn up negative and the system is unstable.

As an example of this type of test, consider the system polynomial of Eq. (70).

$$4s^2 + 5s + 1 = 0 \tag{70}$$

Forming the determinant as outlined above gives:

$$\begin{vmatrix} 5 & 1 \\ 0 & 4 \end{vmatrix} \quad \begin{matrix} \text{first minor: } 5 > 0 \\ \text{second minor: } 20 > 0 \end{matrix}$$

The principal minors are all greater than zero, so Hurwitz character is indicated. This type of test is very attractive because of its simplicity and because it offers no more information than is necessary.

A more detailed method of establishing the Hurwitz character of a given polynomial is known as the "continued fraction expansion method." The criteria for Hurwitz character are that the coefficients of the quotients are all positive, and that the process of division does not terminate prematurely. If it does terminate prematurely, j-axis zeros are indicated and the system must be considered unstable. This method of testing consists of forming the polynomial

$$Q(s) = \frac{M(s)}{N(s)}$$

where $M(s)$ = an even function of s

$N(s)$ = an even function of s

Note: If $N(s)$ is of higher power, use $\dfrac{N(s)}{M(s)}$

Testing the polynomial of Eq. (70),

$$
\begin{array}{r|l}
 & 4/5s \\
\hline
5s & 4s^2+1 \\
 & -4s^2 \\
\hline
 & 1 \\
\end{array}
\qquad
\begin{array}{r|l}
 & 5s \\
\hline
 & 5s \\
 & -5s \\
\hline
 & 0
\end{array}
$$

Hurwitz character is again indicated as all coefficients are positive and there are no j-axis zeros.

TRANSISTOR INHERENT STABILITY

It now becomes necessary to differentiate between active device stability and system stability. At least three different authors have shown that the criterion for active device stability is given by Eq. (71).

$$2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21}) > |\,y_{12}\,y_{21}\,| \tag{71}$$

This is quite obviously a necessary condition for stability since the real part of the immittance which maximizes the power gain of a two-port would be negative if

$$|\,y_{12}\,y_{21}\,| > 2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21}) \tag{72}$$

The value of the real part of the source impedance which maximizes the power gain is

$$\mathrm{Re}(Z_g) = \frac{1}{2\mathrm{Re}(y_{22})}\left\{[2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21})]^2 - |\,y_{12}\,y_{21}\,|^2\right\}^{1/2} \tag{73}$$

Recalling the expression for the maximum available power gain of an unconditionally stable two-port to be

$$G_{max} = \frac{|\,y_{21}\,|^2}{2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21}) + \left\{[2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21})]^2 - |\,y_{12}\,y_{21}\,|^2\right\}^{1/2}} \tag{74}$$

if

$$2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21}) = |\,y_{12}\,y_{21}\,| \tag{75}$$

which is the same as stating that the frequency of measurement* is f_c'' (or for that matter f_c'), then it is easy to see that G_{max} reduces to

$$G_{max} = \frac{|\,y_{21}\,|}{|\,y_{12}\,|} = G_c \tag{76}$$

It is also very obvious that the power gain†

$$G_p' = \frac{|\,y_{21}\,|^2}{2\,[2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21})\,]} \tag{77}$$

*f_c'' is defined here as the upper critical frequency at which the device is between unconditional stability and potential instability. A similar definition for the lower frequency yields f_c'. This is identical to the frequency at which Linvill's critical factor is unity

†G_p' is used here to emphasize again that this power gain is obtained from the general power gain expression by conjugate match to y_{22} (not y_{out}). It is identical to Linvill's P_{oo}/P_{io}.

at the frequency f_c'' reduces to:

$$G_p' = \frac{|y_{21}|}{2|y_{12}|} \tag{78}$$

Therefore, forming the ratio of Eqs. (76) and (78),

$$\frac{G_{max}}{G_p'} = \frac{|y_{21}|}{|y_{12}|}\frac{2|y_{12}|}{|y_{21}|} = 2 \tag{79}$$

This shows that the power gain G_p at f_c'' is exactly 3 db from the maximum available gain obtainable at f_c''. Furthermore, it will never be more than 3 db away from G_{max}.

Unconditional stability simply means that if the inequality of Eq. (71) is satisfied by the device itself, no load or source immittance can ever be found that will cause the system in which it is used to oscillate. Consequently, if this inequality is not satisfied, the device is termed potentially unstable, which means it is possible to find external immittances that will make the system oscillate. It is important to reemphasize that the terms "unconditionally" or "inherently stable" and "potentially unstable" refer to the active *device,* whereas a *system* is referred to as being either stable or unstable.

VARIOUS STABILITY FACTORS

To make clear the relationships among the stability terms that are in common usage, it is necessary to derive the terms presented by Stern and Linvill. Since Linvill approaches the problem with the aid of a unique gain chart, and since the chart will be used in the design examples that follow, his stability factor is presented first.

Linvill defines a "critical factor":

$$C = 2\frac{P_{oo}}{P_{io}}\frac{|y_{12}|}{|y_{21}|} \tag{80}$$

and shows graphically that its interpretation is as indicated in Fig. 12. It is clear from this figure that if C is > 1, then the device characterized by that particular set of y parameters has a region (oscillatory region) in which power output is possible for negative power input.

One way to discover how the equation for C came about is to consider the expression

$$2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21}) > |y_{12}\,y_{21}| \tag{81}$$

This has been shown to be the criterion for device stability. Now dividing through by $|y_{12}\,y_{21}|$ we get

$$\frac{2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21})}{|y_{12}\,y_{21}|} > 1 \tag{82}$$

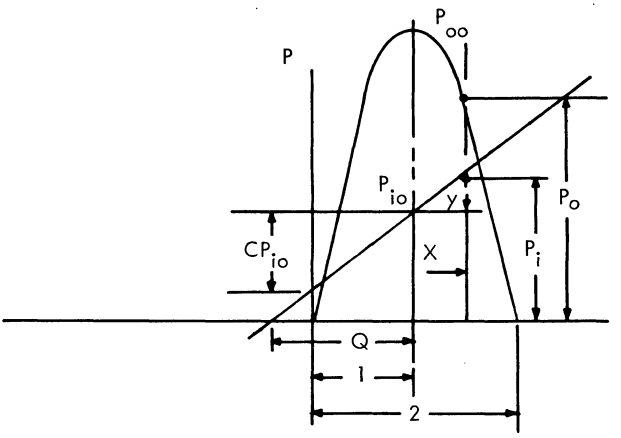

Fig. 12. Two-dimensional power gain model.

Now inverting
$$\frac{|y_{12}\,y_{21}|}{2\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}\,y_{21})} < 1 \tag{83}$$

If this expression is satisfied by the device, then it is unconditionally stable. If it is not satisfied, the device is potentially unstable. To facilitate reference to this expression, the letter C may be used and an equality substituted for the "less than" sign:

$$\frac{|y_{12}\,y_{21}|}{2\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})} = C \tag{84}$$

Recalling that:
$$G_{oo} = \frac{|y_{21}|^2}{4\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - 2\mathrm{Re}(y_{12}y_{21})} \tag{85}$$

it is clearly seen that

$$C = \frac{|y_{21}|^2}{4\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - 2\mathrm{Re}(y_{12}y_{21})} \frac{2\,|y_{12}|}{|y_{21}|} \tag{86}$$

$$= \frac{|y_{12}y_{21}|}{2\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})} \tag{87}$$

$$= 2G_{oo}\frac{|y_{12}|}{|y_{21}|} \tag{88}$$

Stern defines a stability factor that includes the effect of the load and source and is customarily presented as in Fig. 13. The modified y matrix will now be

$$y = \begin{vmatrix} y_{11} + Y_g & y_{12} \\ y_{21} & y_{22} + Y_L \end{vmatrix}$$

The stability criterion equation will now be of the form

$$2(g_{11} + G_g)(g_{22} + G_L) - \mathrm{Re}(y_{12}y_{21}) > |y_{12}y_{21}| \tag{89}$$

Now let
$$L = |y_{12}y_{21}|$$
$$M = \mathrm{Re}(y_{12}y_{21})$$

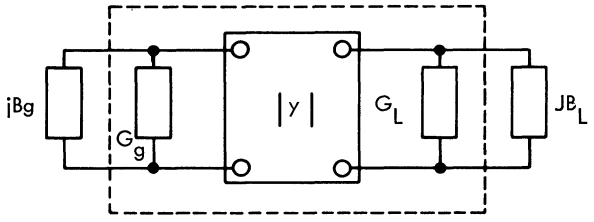

Fig. 13. Model used to demonstrate Stern's K factor.

Eq. (89) becomes

$$2(g_{11} + G_g)(g_{22} + G_L) - M > L \tag{90}$$

$$(g_{11} + G_g)(g_{22} + G_L) > \frac{L + M}{2} \tag{91}$$

Now the inequality sign may be disposed of in the same way as before, as shown in Eq. (92):

$$(g_{11} + G_g)(g_{22} + G_L) = K\left(\frac{L + M}{2}\right) \tag{92}$$

In Eq. (92):

if $K > 1$, the system as loaded is unconditionally stable

if $K < 1$, the system as loaded is potentially unstable

Stern's stability factor K has the same implication as Linvill's factor C (although they are inverse) as far as the terms "potential instability" and "unconditional stability" go, except that Stern brings the real part of the load and source into the stability equation. Thus, his K factor is not entirely a property of the device. On the other hand, the real part of the load and source are usually not varied when tuning the circuit. Thus, including them in the stability expression is a practical thing to do and K might more logically be called the actual stability factor of the circuit, while Linvill's C factor could be called an intrinsic stability factor of the device. Comparison of Eqs. (93), (94), and (95) clearly shows the interrelationships of these concepts:

stability criterion: $$2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) > |y_{12}y_{21}| \tag{93}$$

Linvill's C factor: $$2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) = \frac{1}{C}|y_{12}y_{21}| \tag{94}$$

Stern's K factor: $$2(g_{11} + G_g)(g_{22} + G_L) - K\mathrm{Re}(y_{12}y_{21}) = K|y_{12}y_{21}| \tag{95}$$

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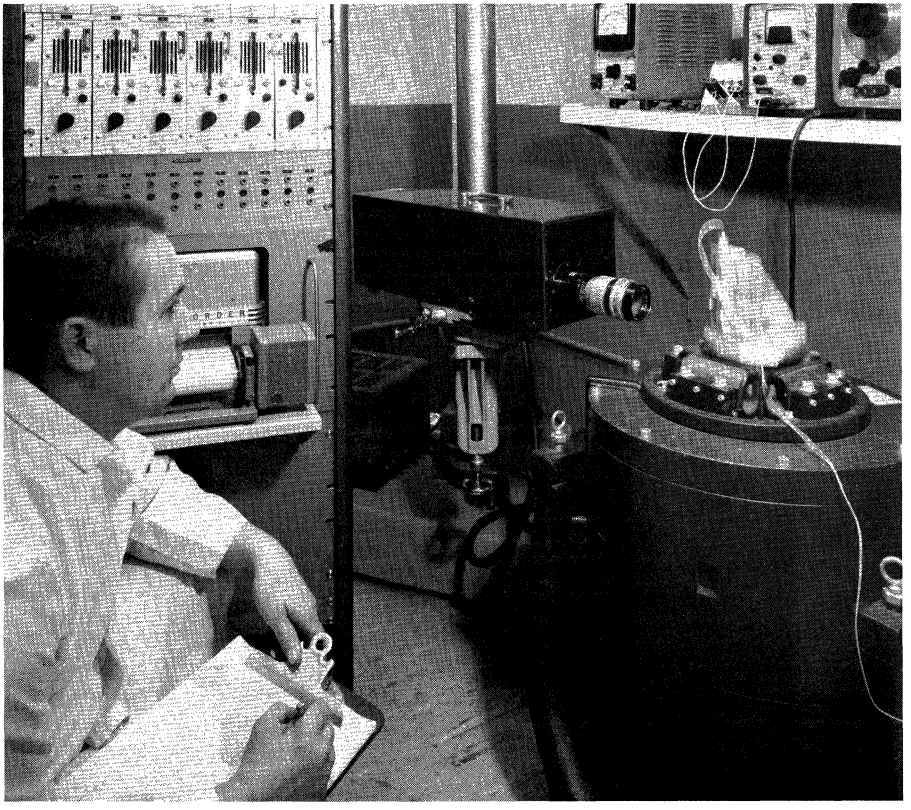


Vibration table and displacement recorder in TI's Environmental Test Laboratory, one of the most extensive facilities of its kind in the world.

5

High-frequency Amplifier Design Using Admittance Parameters

by George Johnson, Peter Norris, Frank Opp

INTRODUCTION

High-frequency amplifier design using two-port theory is demonstrated by measuring the y parameters of a silicon epitaxial mesa transistor. Since the two-port parameters of any Linear Active Network (LAN) completely describe its power gain and stability, curves of inherent stability and power gain are developed and presented. This information satisfies the first need of a designer: a complete and accurate description of the gain capability of the linear active network over the frequency range of interest.

A design technique, originated by J. G. Linvill, is described in some detail. This technique includes unique charts* and graphical representations useful in the analysis of relationships among power gain, stability, and sensitivity. A numerical example is presented which uses this design technique.

ADMITTANCE PARAMETER CHARACTERIZATION

In general, any of the six sets of two-port parameters may be used to describe the linear active network. Most common of these, of course, are the h and y parameters. In high-frequency work the y parameters are generally accepted as the most useful description of LAN; at lower frequencies the h parameters are commonly used. The parameter choice is also influenced by the type of measuring instrument and the accuracy with which it can measure the parameter in question. For this discussion a consistent set of y_e data was measured and is contained in Figs. 3 through 6 which are found later in this chapter.

The General Radio Type 1607-A Transfer Function and Immittance Bridge, a coaxial null-type instrument, was selected because of its wide range of frequency

*These charts are adapted from J. G. Linvill and L. G. Schimpf, "The Design of Tetrode Transistor Amplifiers," Bell System Tech. J., vol. 35, pp. 813–840, July 1956, with permission of the authors and the Bell Telephone Laboratories.

applicability, its accuracy, and because no test jigs are required for the measurements. The measuring procedure and bridge description along with its line losses and other error sources are described in the GR Instruction Manual and will not be described here. Accuracy equations found in the instruction book are repeated in Table 1 for convenience. The fixed error may be reduced approximately one order of magnitude by the use of appropriate accessories and line-loss corrections.

Table 1. Bridge Accuracy

Parameter	Accuracy
y_{11} or y_{22}	$2(1 + \sqrt{y_{11}/20})\ \% + 0.4$ mmhos
y_{21} or y_{12}	$2.5(1 + \sqrt{y_{21}/20})\ \% + 0.5$ mmhos

POWER GAIN AND STABILITY

Before developing the power flow concepts, it is necessary to review the various forms of power gain and to describe in general the concept of stability. This will establish the proper perspective for the material that follows.

Figure 1 shows a general four-terminal network. Although the network is characterized in terms of y parameters, any consistent set of parameters will work. Table 2 shows the various power ratios which may be defined for this network. Note that the term "power gain" has a definite meaning. Notice also that the term "maximum available gain" is meaningful only when the transistor is unconditionally stable. This is obvious since the gain obtainable from a transistor that is potentially unstable is unbounded.

Neutralization can be achieved by modifying the y_{12} parameter with a parallel network, as shown in Fig. 2. The a and p subscripts denote active and passive parameters.

Neutralized power gain is not described by any particular ratio in Table 2 and no specific equation is given since any of the above gains can be neutralized gains. In many amplifier circuits, neutralization of inverse feedback is applied only as far as necessary to achieve the stability figure desired, to reduce the input variation for a given output variation, or to achieve a specified power gain. Therefore, any of the gain equations are applicable if the composite parameters of the networks are used. These parameters are defined by the following equations:

$$y_{12c} = y_{11a} + y_{12p}$$

$$y_{22c} = y_{22a} + y_{12p}$$

$$y_{21c} = y_{21a} - y_{12p}$$

$$y_{12c} = y_{12a} - y_{12p}$$

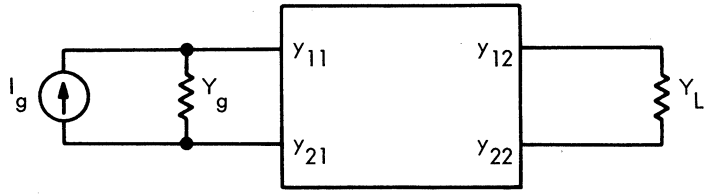


Fig. 1. A general two-port.

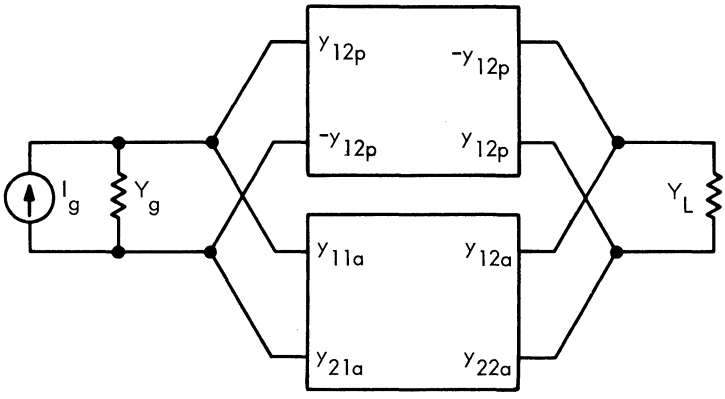


Fig. 2. A neutralized two-port.

When external feedback is applied to the point of reducing y_{12c} to zero, the following expression results:

$$G_U = \frac{|y_{21} - y_{12}|^2}{4(g_{11} + g_{12})(g_{22} + g_{12})}$$

It is now evident that the G_U in Table 2 is not the unilateral gain of the transistor, but the gain of the composite network. Now consider the meaning of the gain expression if the external unilateralizing network is not added. Let us assume internal feedback does not exist. The G_{max} term and G_U become equal and are expressed by:

$$G_U = \frac{|y_{21}|^2}{4g_{11}g_{22}}$$

This is a somewhat meaningless expression since at frequencies sufficiently low to make y_{12} small and difficult to measure, the effect of y_{12} is still important and causes potential instability. Furthermore, at higher frequencies it is erroneous to assume that y_{12} does not exist. Before this is demonstrated, however, another power gain term should be described. Define this gain the same way G_P was defined, except let the load be the conjugate of y_{22}, i.e., not Y_{out}. The expression will be of the following form:

$$\frac{P_{oo}}{P_{io}} = G_{oo} = \frac{|y_{21}|^2}{4g_{11}g_{22} - 2\mathrm{Re}(y_{12}y_{21})}$$

Table 2. Power Ratios for a General Two-port

EXPRESSION	SYMBOL	DESCRIPTION	EQUATION
Power Gain	G_P	Pwr. Delivered to Load / Pwr. Delivered to Input	$\dfrac{\lvert y_{21}\rvert^2 \operatorname{Re}(Y_L)}{\lvert Y_L + y_{22}\rvert^2 \operatorname{Re}\left(y_{11} - \dfrac{y_{12}y_{21}}{y_{22}+Y_L}\right)}$
Transducer Gain	G_T	Pwr. Delivered to Load / Max. Pwr. Available from source	$\dfrac{4\operatorname{Re}(Y_g)\operatorname{Re}(Y_L)\lvert y_{21}\rvert^2}{\lvert (y_{11}+Y_g)(y_{22}+Y_L) - y_{12}y_{21}\rvert^2}$
Max. Available Gain	G_{max}	Max. Pwr. Available at output / Max. Pwr. Available from source	$\dfrac{*\quad \lvert y_{21}\rvert^2}{2g_{11}g_{22} - \operatorname{Re}(y_{12}y_{21}) + \{[2g_{11}g_{22} - \operatorname{Re}(y_{12}y_{21})]^2 - \lvert y_{12}y_{21}\rvert^2\}^{1/2}}$
Neutralized Pwr. Gain	G_N	(See Text)	(See Text)
Unilateral Pwr. Gain	G_U	(See Text)	$\dfrac{\dagger\lvert y_{21c}\rvert^2}{4g_{11c}g_{22c}}$

*g_{11} is the $\operatorname{Re}(y_{11})$ and has no relation to the two-port parameter G_{11}.
†The subscript c implies "composite."

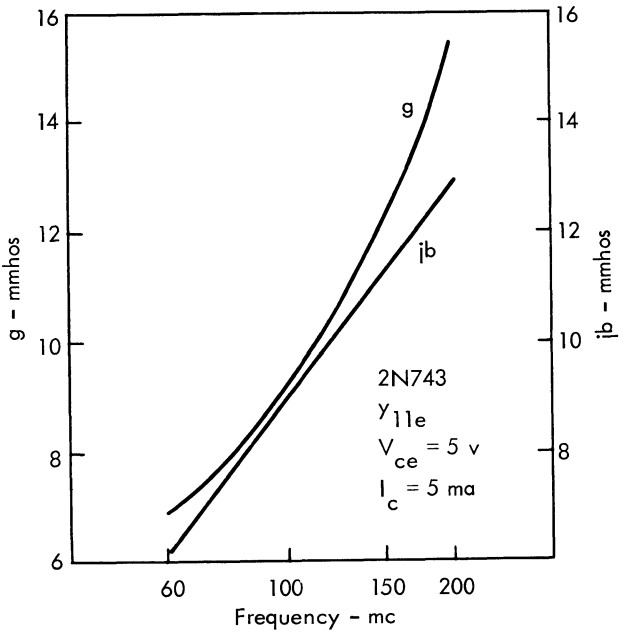


Fig. 3. y_{11e} vs. frequency (typical data).

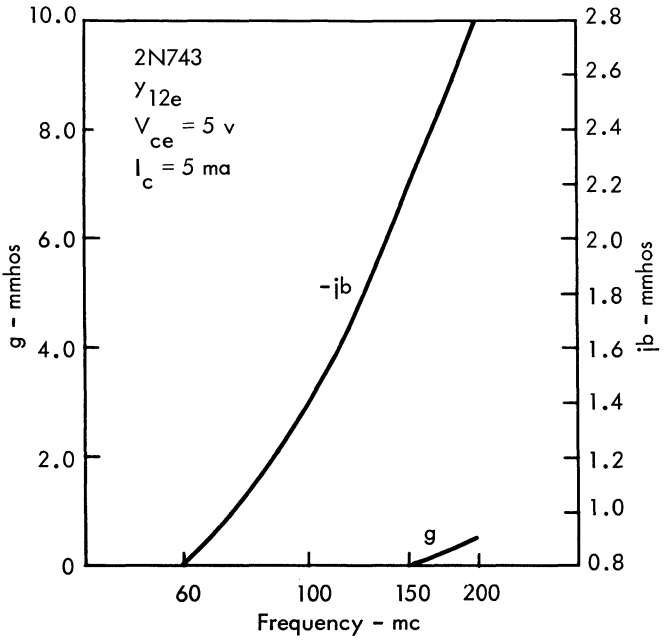


Fig. 4. y_{12e} vs. frequency (typical data).

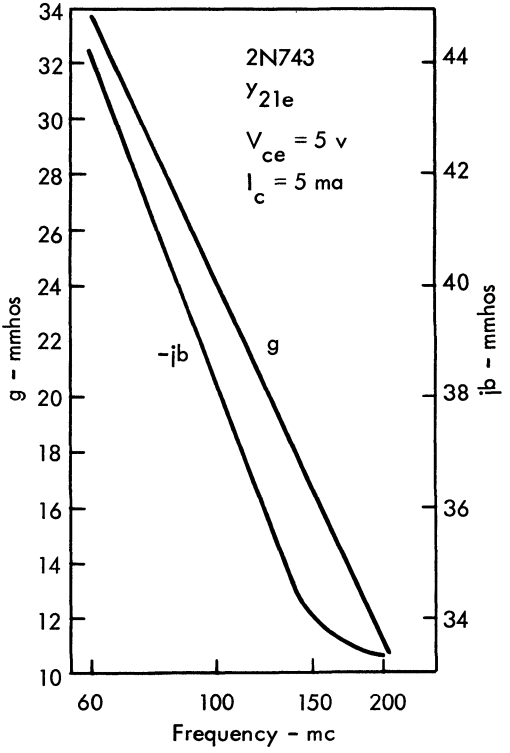


Fig. 5. y_{21e} vs. frequency (typical data).

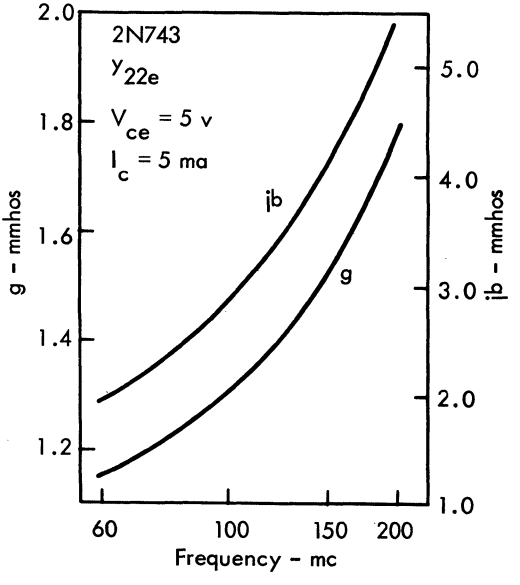


Fig. 6. y_{22e} vs. frequency (typical data).

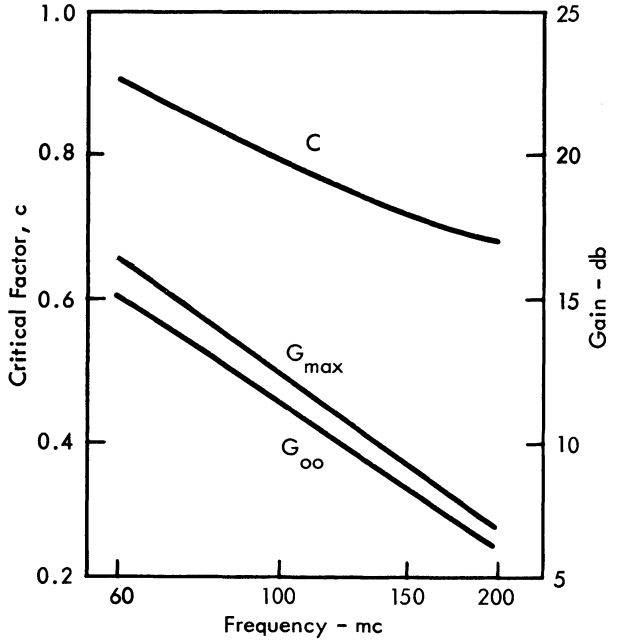


Fig. 7. 2N743 common-emitter, critical factor, and gain vs. frequency.

Note that the expression includes the existence of the y_{12} component, and just as in G_P, this expression has nothing to do with the driving source R_g. Figure 7 shows a plot of G_{oo} and G_{max}. Note that for the stage in this range G_{max} is approximately equal to G_{oo}. This will be described further in the later sections.

At least three different authors have shown the criterion for active device stability, which is expressed by:

$$2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) > |\, y_{12}y_{21} \,|$$

This may be seen by inspecting the equation for the source resistance which maximizes the power gain:

$$\mathrm{Re}(Z_g) = \frac{1}{2\mathrm{Re}(y_{22})}\left\{[2(g_{11})(g_{22}) - \mathrm{Re}(y_{12}y_{21})]^2 - |\, y_{12}y_{21} \,|^2\right\}^{1/2}$$

Now, if

$$2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) < |\, y_{12}y_{21} \,|$$

then the $\mathrm{Re}(Z_g)$ is a negative quantity and forces an unstable condition.

A BRIEF DESCRIPTION OF THE LINVILL TECHNIQUE

The need for a more comprehensive description of the general process of power flow through a two-port has been clearly indicated by the fact that active devices can be potentially unstable. To describe this power flow process, the following section shows that the equation for output power in mathematical form is sufficient to describe the geometric shape of a parabola of revolution. Similarly, the

input power equation is shown to be a geometric plane. Using this representation, we show how these geometrical representations may be combined to evaluate graphically the power gain of the two-port. A unique aspect of this interpretation is that both positive and negative input power flow are indicated. Thus device stability is explicitly indicated, and the region of instability is clearly defined.

A stability term called the critical factor c is related to this combined geometric concept of power gain and indicates the slope of the input power plane. If this slope is too great, there is a region of instability. The c factor is thus an indication of inequality of the familiar stability criterion:

Stability criterion: $2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) > |y_{12}y_{21}|$

The new stability equation: $2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) = \frac{1}{c}|y_{12}y_{21}|$

Values of c simply show the degree of unconditional stability ($c < 1$), or potential instability ($c > 1$). When $c > 1$, there is a source or load termination which causes the transistor to oscillate. It is clear the c factor is an important characteristic "parameter" of the transistor because:

a. The frequencies at which $c > 1$ define the frequency range of potential instability.
b. Its manifestation on the Linvill chart allows a load selection which will always result in stable amplifier operation.
c. When $c < 1$, the factor

$$K_G = 2\left[\frac{1-\sqrt{1-c^2}}{c^2}\right]$$

when multiplied by G_{oo} gives G_{max}, which is the maximum available gain obtainable in an unneutralized circuit.

There are other attractive properties of this analysis procedure. First, it is possible to construct sensitivity curves on the Linvill chart. Sensitivity δ is defined as the percent change in input immittance to the percent change in output immittance and indicates the degree of "non-unilateralness." This has great significance in multi-stage, i-f strip design. When these δ contours are constructed they define an area in which a given load can be placed that satisfies gain and sensitivity requirements. Other methods relating mismatch to gain loss require a few calculations, but sensitivity contours and gain curves on a Linvill chart neatly relate gain, stability, alignability, and bandwidth in one picture. A second advantage of this method is that an input immittance chart or overlay may be used to read input immittance for a given load. Although it is easily calculated, the use of this overlay speeds up the analysis of input immittance brought about by varying loads, and reduces complex algebraic manipulation.

Although sensitivity contours and input immittance overlays are not discussed here to any great extent, it should be made clear that they exist and provide the circuit designer with a powerful analytic tool as well as a complete picture of tuned amplifier performance.

The following section presents a brief development of the charts and concepts, a step-by-step design procedure, and an example design using a silicon epitaxial mesa transistor in a single-tuned 60-mc i-f amplifier stage.

GRAPHICAL PRESENTATION OF POWER GAIN

For the four-terminal network shown in Fig. 8, the power P_o delivered to the load, and the network input power P_i, are expressed as functions of the load Y_L. Working from the network equations:

$$I_1 = y_{11}E_1 + y_{12}E_2 \tag{1}$$

$$I_2 = y_{21}E_1 + y_{22}E_2 \tag{2}$$

and defining:

$$E_1 = 1 + jO$$

$$E_2 = (L + jM)\frac{-y_{21}}{2\mathrm{Re}(y_{22})}$$

Now P_o and P_i may be obtained as functions of the network parameters, and L and M may be obtained by substituting the expression for E_1 and E_2 into the network equations:

$$P_o = L\frac{|y_{21}|^2}{2\mathrm{Re}(y_{22})} - \frac{(L^2 + M^2)|y_{21}|^2}{4\mathrm{Re}(y_{22})} \tag{3}$$

$$P_i = \mathrm{Re}(y_{11}) + L\,\mathrm{Re}\left[\frac{y_{21}y_{12}}{2\mathrm{Re}(y_{22})}\right] + M\,\mathrm{Im}\left[\frac{y_{21}y_{12}}{2\mathrm{Re}(y_{22})}\right] \tag{4}$$

L, M, and Y_L are related by:

$$I_2 = -Y_L E_2$$

and Eq. (2):

$$I_2 = y_{21}E_1 + y_{22}E_2 = -Y_L E_2$$

Again using the E_1 and E_2 expressions, we have:

$$Y_L + y_{22} = \frac{2\mathrm{Re}(y_{22})}{L + jM} = G_2 + jB_2 \tag{5}$$

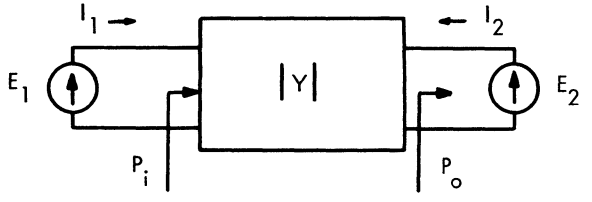


Fig. 8. Power flow directions.

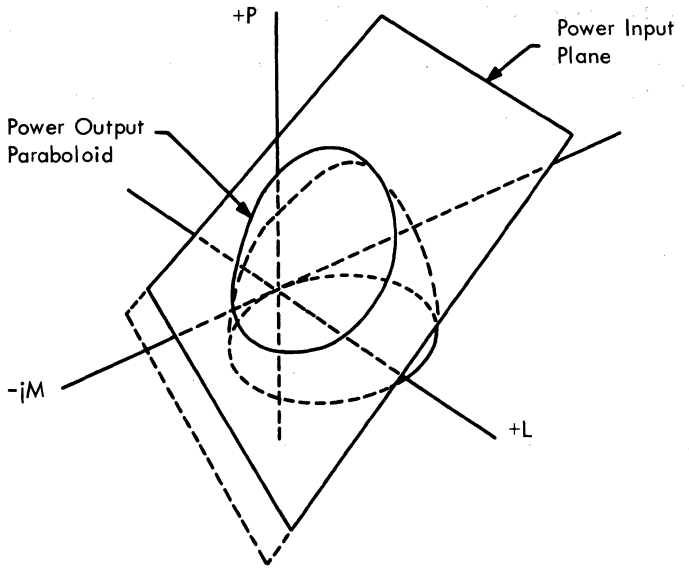


Fig. 9. Power surfaces.

Therefore, any value of Y_L can be simulated by varying L and M. If these expressions are plotted in the LMP coordinate system, the surface P_o is a paraboloid and P_i is a plane. These surfaces are shown in Fig. 9.

Since we are only concerned with passive load admittance, only the positive P_o surface is shown. The intersection of P_o and the L-M plane is a circle centered at L = 1, M = 0, of radius 1. This circle represents zero output power. The input plane can assume any position relative to P_o, its exact position determined by the parameter values used. The P_i and the L-M plane intersect in a straight line at $P_i = 0$. The amplifier gain, stability, and bandwidth can be determined by examining the relative positions of P_o and P_i. All of the necessary design information can be placed within the $P_o = 0$ circle in the L-M plane. No attempt is made to prove any of the procedures or statements given. For those who are interested, the references given provide a complete mathematical development.

At this point several quantities should be defined. To clarify these definitions, Fig. 10 shows a section of the two surfaces in question.

1. The input power plane is defined by its gradient and elevation at L = 1, M = 0. P_i at this point is labeled

$$P_{io} = \frac{2\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})}{2\mathrm{Re}(y_{22})} \tag{6}$$

The gradient is equal to

$$\mathrm{Gr} = \left| \frac{y_{12}y_{21}}{2\mathrm{Re}(y_{22})} \right| e^{j\theta} \tag{7}$$

where $\theta = \arg\ (-y_{12}y_{21})$*.

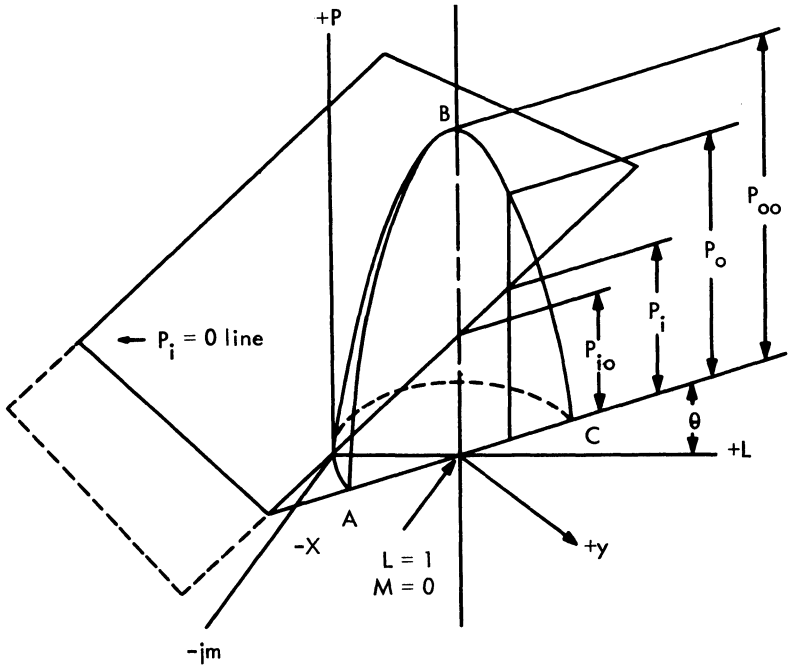


Fig. 10. Dimensions of power surface.

The ABC plane used in Fig. 10 contains the centerline of the paraboloid and makes an angle θ with the L-M plane. The intersection of this cutting plane and the L-M plane is called the gradient line. This line orients the input power in the L-M plane.

2. P_{oo} is the maximum output power and occurs at L = 1, M = 0, which corresponds to $Y_L = y_{22}$.
3. P_o is any output power and P_i is any input power.
4. A new coordinate system xy in the L-M plane has x along the gradient line and y normal to it with the origin at L = 1, M = 0.
5. The critical factor c is a measure of the transistor inherent stability. If the surfaces in Fig. 10 are viewed with a line of sight along y, the coordinate system can be reduced to two dimensions as shown in Fig. 11.

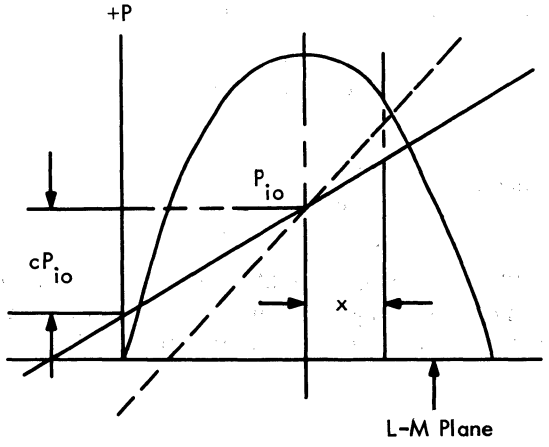


Fig. 11. Two-dimensional projection.

As long as $c < 1$, P_i is positive for all positive values of P_o and the device is stable. If the input power plane is positioned such that it intersects the L-M plane as indicated by the dotted line in Fig. 11, negative P_i's are possible for positive P_o's. In this region both P_o and P_i flow from the network, and it, therefore, must be generating power. This condition can only occur if $c > 1$. Therefore, for $c < 1$, the transistor is unconditionally stable and there are no passive terminations which can cause the transistor to oscillate. For $c > 1$, the system is potentially unstable and certain passive terminations can cause oscillations. The c factor in terms of the network y parameters is:

$$c = \frac{|y_{21}y_{12}|}{2\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{21}y_{12})}$$

$$= 2\left(\frac{P_{oo}}{P_{io}}\right)\left|\frac{y_{12}}{y_{21}}\right| \tag{8}$$

6. Constant gain contours appear as circles in the L-M plane. In terms of x and y:

$$\frac{P_i}{P_{io}} = 1 + cx$$

$$1 - \frac{P_o}{P_{oo}} = x^2 + y^2$$

Letting:

$$g = \frac{P_o/P_i}{P_{oo}/P_{io}}$$

the constant gain equation becomes:

$$1 - g + \left(\frac{g_c}{2}\right)^2 = \left(x + \frac{g_c}{2}\right)^2 + y^2 \tag{9}$$

For $c < 1$, g can have any value between 0 and K_G:

$$K_G = 2\frac{1 - \sqrt{1 - c^2}}{c^2} \tag{10}$$

The maximum gain will occur at a point $x = -\frac{cK_G}{2}$ along the gradient line. For $c > 1$, g can have any value between 0 and infinity.

The sensitivity is expressed by:

$$\delta = \frac{dY_{in}/Y_{in}}{dY_L/Y_L} = \left|\frac{Y_L}{y_{22} + Y_L}\right| \cdot \left|\frac{g_{11}}{y_{11}}\right| \cdot \frac{K}{\left|\frac{y_{22} + Y_L}{g_{22}} + \frac{g_{11}}{y_{11}}Ke^{j\theta}\right|} \tag{11}$$

where: $K = \dfrac{y_{12}y_{21}}{g_{11}g_{22}}$

$\theta = \arg(-y_{12}y_{21})$ *

The portion of the L-M plane contained within the $P_o = 0$ circle is called the Linvill chart. Any point on this chart represents a gain and value of Y_L. This chart is similar to a Smith chart in the manner of the Y_L presentation. In fact, just three

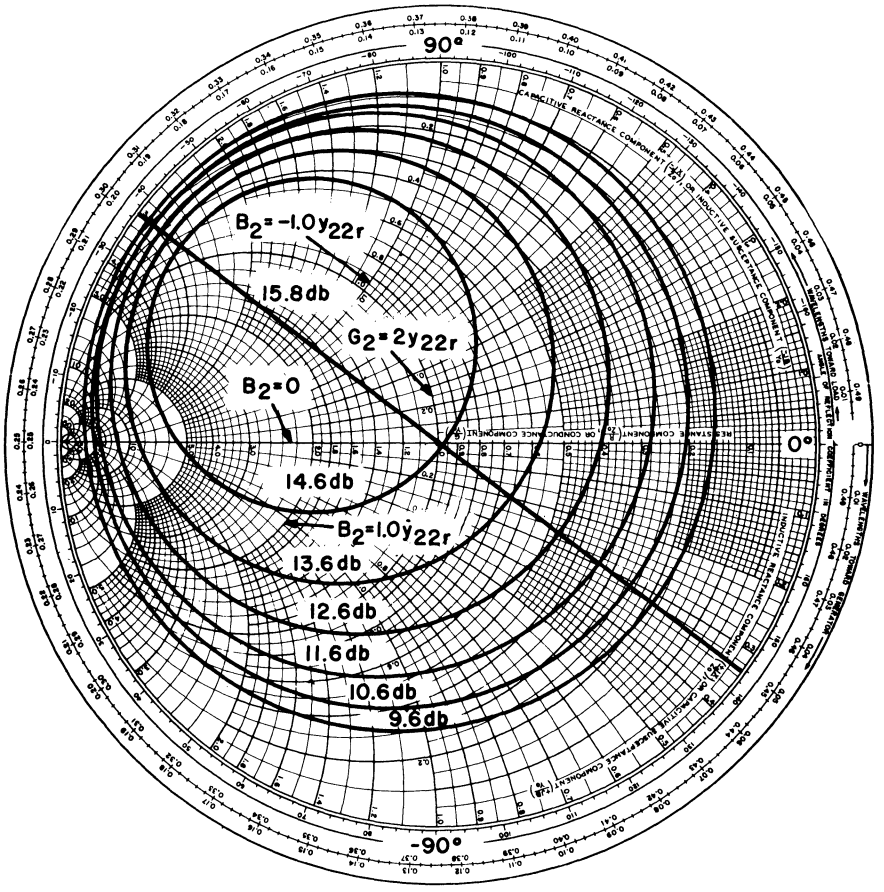


Fig. 12. 2N743 60-mc Linvill chart.

modifications convert the Smith to the Linvill chart, Fig. 12. First, a 180° rotation is required; second, the conductance-susceptance normalization factor is now the real part of the output admittance; and third, the wavelength and reflection angle graduations are replaced by angular graduations as shown in Fig. 12. A general admittance point on this chart is:

$$G_2 + jB_2 = Y_L + y_{22}$$

Therefore, as stated before, all passive Y_L values are displayed.

LINVILL CHART PREPARATION

The preparation of the Linvill chart to show transistor performance at a particular frequency requires these steps:

1. Obtain the real and imaginary parts of y_{11}, y_{22}, y_{21}, and y_{12}.

2. Complete:

$$\frac{P_{oo}}{P_{io}} = \frac{|y_{21}|^2}{4Re(y_{11})Re(y_{22}) - 2Re(y_{12}y_{21})}$$

$$C = 2\left(\frac{P_{oo}}{P_{io}}\right)\left|\frac{y_{12}}{y_{21}}\right|$$

$$\theta = \arg(-y_{21}y_{12})\ *$$

3. Draw the gradient line at the angle θ from the $B_2 = 0$ line.
4. If $c > 1$, draw a line perpendicular to the gradient through a point a distance $x = -1/c$ from the center of the circle. This line represents $P_i = 0$ and divides those terminations that cause oscillation from those that allow stable performance. If $c < 1$, this line is outside the chart.
5. If $c < 1$, calculate:

$$K_G = 2\frac{1-\sqrt{1-c^2}}{c^2}$$

the equation:

$$G_{max} = K_G\left(\frac{P_{oo}}{P_{io}}\right) \qquad (12)$$

yields the maximum mismatch gain. Using:

$$1-g+\left(\frac{cg}{2}\right)^2 = \left(x+\frac{cg}{2}\right)^2 + y^2$$

calculate and plot other constant-gain contours of interest.

LINVILL CHART CALCULATIONS EXAMPLE

To show the 2N743 60-mc performance, a Linvill chart, Fig. 12, has been prepared following the steps previously outlined:

1. The common-emitter y parameters at this frequency are:

$$y_{ie} = (6.8 + j\,6.1)10^{-3} = 9.13 \times 10^{-3} \angle 41.9°$$

$$y_{oe} = (1.24 + j\,1.92)10^{-3} = 2.28 \times 10^{-3} \angle 57.15°$$

$$y_{fe} = (33.6 - j\,44.2)10^{-3} = 55.5 \times 10^{-3} \angle -52.75°$$

$$y_{re} = (-j\,0.81)10^{-3} = 0.81 \times 10^{-3} \angle -90°$$

2. Calculate the following:

$$\frac{P_{oo}}{P_{io}} = \frac{|y_{fe}|^2}{4Re(y_{ie})Re(y_{oe}) - 2Re(y_{fe}y_{re})}$$

$$= \frac{55.5^2}{4(6.8)(1.24) - 2Re(33.6 - j\,44.2)(-j\,0.81)}$$

$$= \frac{(55.5)^2}{33.72 + 71.5}$$

$$= 29.2, \text{ or } 14.65\text{db}$$

$$c = 2\left(\frac{P_{oo}}{P_{io}}\right)\left|\frac{y_{re}}{y_{fe}}\right|$$

$$= 2(29.2)\left(\frac{0.81}{55.5}\right)$$

$$= 0.854$$

The angle θ is easily found by the following steps:

$$y_{fe}y_{re} = (33.6 - j\,44.2)(-j\,0.81)10^{-6}$$

$$= (-35.8 - j\,27.2)10^{-6}$$

$$-(y_{fe}y_{re}) = (35.8 + j\,27.2)10^{-6}$$

$$(-y_{fe}y_{re})^* = (35.8 - j\,27.2)10^{-6}$$

$$= 45 \times 10^{-6} \angle -37.2°$$

$$\theta = -37.2°$$

3. The gradient line is therefore drawn at an angle of $\theta = -37.2°$ to the $B_2 = 0$ line.
4. Since $c < 1$, the $P_i = 0$ line lies outside the chart boundaries.
5. The constant gain circles can now be calculated and plotted. If $c < 1$, which it is in this case, the first calculation should be with $g = K_G$.

   From Eq. (10),

$$K_G = 2\frac{1 - \sqrt{1 - (0.854)^2}}{(0.854)^2}$$

$$= 1.31$$

   Therefore from Eq. (12),

$$G_{max} = (1.31)(29.2)$$

$$= 38.4, \text{ or } 15.8\text{db}$$

Table 3 contains information for plotting other gain circles.

Table 3. Constant Gain Circles

g		Center	Radius
Numeric	db	$gc/2$	$\sqrt{1 - g + (gc/2)^2}$
1.31	+1.17	–0.569	0
1.0	0	–0.427	0.427
0.793	–1	–0.342	0.569
0.63	–2	–0.269	0.662
0.5	–3	–0.215	0.739
0.398	–4	–0.170	0.794
0.318	–5	–0.137	0.837

The gain circles can now be plotted on the Linvill chart. For example, to plot the 0.793 (P_{oo}/P_{io}) circle, locate the center on the gradient line at a distance of –0.342 from the center of the chart. With this center and a radius of 0.569, draw the circle. All distances are normalized to the unity radius circle. For $c > 1$, a portion of the gain circles will be off the chart, but this fact does not change the above procedure.

GAIN DESIGN PROCEDURES

1. Select Y_L based on a specified value of δ. Equation (11) can be simplified if $Y_L >> y_{22}$:

$$\delta = \frac{|y_{21}y_{12}|}{|y_{11}Y_L - y_{21}y_{12}|} \tag{13a}$$

If $\delta << 1$,

$$\delta = \frac{|y_{21}y_{12}|}{|y_{11}|\,|Y_L|} \tag{13b}$$

2. Locate the G_2 circle on the Linvill chart corresponding to the above Y_L value.
3. Find the maximum gain on this G_2 circle. This gain will occur at the point of tangency of the G_2 and a gain circle and indicates the jB_2 value necessary.
4. Draw a gain circle 3 db lower than the gain indicated in step 2. The intersections of this circle with the G_2 circle represent the half-power points.
5. Move along the G_2 circle and find the total susceptance change necessary to move from one intersection to the other.
6. To produce the required output stage bandwidth, let:

$$\frac{\Delta B}{\Delta \omega} = 2C_L$$

Select the inductance to produce the required load using the above capacitance from:

$$B_L = \omega C_L - \frac{1}{\omega L}$$

7. Calculate the Y_{in} for the collector load which yields maximum gain.
8. Match the generator admittance to the complex conjugate of Y_{in}.
9. Calculate Y_{out}, the output admittance, for this match at the input. Solve for C_{out}.
10. Transform the amplifier load to yield the required Y_L as specified by the sensitivity requirement.

GAIN DESIGN EXAMPLE

Using the 60-mc y parameters given previously, design a stage for maximum gain under the conditions:

$$\delta \leqq 0.3$$

$$R_2 = R_1 = 50\Omega$$

$$BW_{3db} \geqq 10 \text{ mc}$$

where R_2 and R_1 are the load and source impedances, respectively, not to be confused with the Y_L determined from the charts, or Y_{in}*.

1. Select the $|Y_L|$ necessary for δ less than 0.3. Solving for $|Y_L|$ from Eq. (13),

$$|Y_L| \geq \frac{|y_{21}y_{12}|}{|y_{11}|\,\delta}$$

Using the y parameters given previously and $\delta = 0.3$,

$$|Y_L| \geq \frac{4.93 \times 10^{-3}}{0.3} \geq 16.4 \times 10^{-3} \text{ mhos}$$

2. Locate the G_2 circle:

$$G_2 \geq \left(1 + \frac{|Y_L|}{y_{22r}}\right) y_{22r}$$

$$\geq \left(1 + \frac{16.4}{1.24}\right) y_{22r}$$

$$\geq 14.2y_{22r}$$

3. The Linvill chart shows that the highest possible gain is about 2 db less than P_{oo}/P_{io} and that the G_2 and B_2 values necessary are:

$$G_2 = 14.2y_{22r}$$

$$B_2 = -2y_{22r}$$

4. Draw a gain circle 3 db below the circle tangent to the $14.2y_{22r}$ point found above. This is the 0.318 (P_{oo}/P_{io}) circle.
5. Figure 13 shows an enlarged picture of the G_2 gain circles. The total

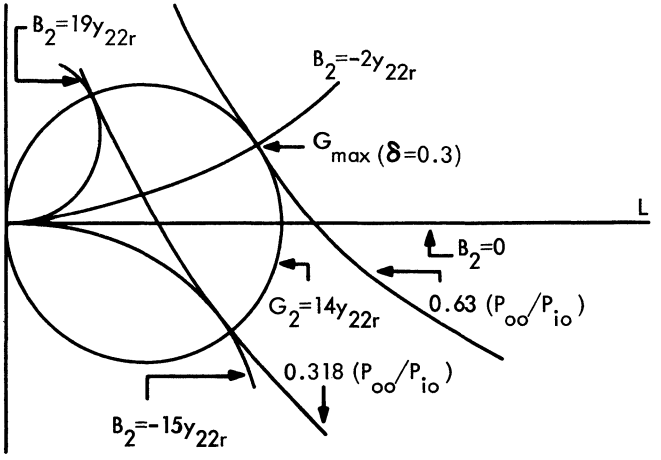


Fig. 13. Gain diagram.

susceptance change is:

$$\Delta B = 15y_{22r} - (-19y_{22r})$$
$$= 34y_{22r}$$
$$= (34)(1.24)10^{-3}$$
$$= 42.2 \times 10^{-3} \text{ mhos}$$

6. Assuming a BW_{3db} of 20 mc for both the input and the output network, let:

$$\Delta\omega = BW_{3db} = (2\pi)(20 \text{ mc})$$
$$C_L = \frac{1}{2}\frac{\Delta B}{\Delta\omega} = \frac{42.2 \times 10^{-3}}{40\pi \times 10^6} = 168 \text{ pf}$$

Solve for B_L:

$$B_2 = -2y_{22r} = y_{22i} + B_L$$
$$B_L = -2y_{22r} - y_{22i} = (-2.48 - 1.92)10^{-3}$$
$$= -4.40 \times 10^{-3}$$
$$= \omega C_L - \frac{1}{\omega L}$$

Substituting into this expression $C_L = 168$ pf, $\omega = (2\pi)$ (60 mc), and $B_L = -4.4 \times 10^{-3}$ yields:

$$L_2 = 0.04 \ \mu h$$

7. The input admittance is:

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}$$
$$Y_{in} = \left\{6.8 + j6.1 - \left[\frac{(33.6 - j44.2)(-j0.81)}{1.24 + j1.92 + (13.2)1.24 - j4.4}\right]\right\} 10^{-3}$$
$$= (8.6 + j7.9)10^{-3}$$

8. Therefore $Y_g = (8.6 - j7.9)10^{-3}$

9. The output admittance for this Y_g is:

$$Y_{out} = y_{22} - \frac{y_{12}y_{11}}{y_{11} + Y_g}$$
$$= \left\{1.24 + j1.92 - \left[\frac{(33.6 - j44.2)(-j0.81)}{6.8 + j6.1 + 8.6 - j7.9}\right]\right\} 10^{-3}$$
$$= (3.3 + j4.0)10^{-3} \text{ mhos}$$
$$C_{out} = \frac{B_{out}}{\omega}$$
$$= \frac{4.0 \times 10^{-3}}{(2\pi)(60 \times 106)}$$
$$= 10.6 \text{ pf}$$

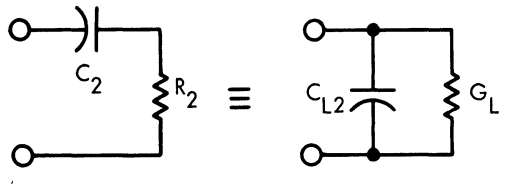


Figure 14

10. The load R_2 must now be transformed as shown in Figs. 14 and 15 below:

$$C_{L2} = C_2 \frac{1}{1 + 1/Q^2}$$

Solving for Q,

$$Q = \sqrt{1/G_L R_2 - 1}$$

$$= \frac{1}{\omega C_2 R_2}$$

$$= \sqrt{\frac{1}{(16.4 \times 10^{-3})(50)} - 1}$$

$$= 0.469$$

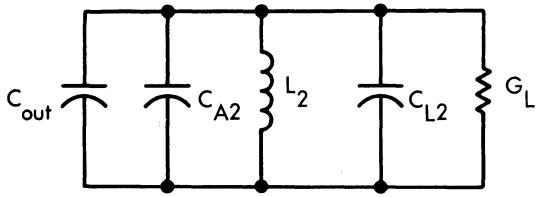
$$\omega C_2 = \frac{1}{(0.469)(50)} = 0.0426 \text{ mhos}$$

$$C_2 = 113 \text{ pf}$$

$$\text{Use } C_2 = 110 \text{ pf}$$

$$C_{L2} = 110 \left(\frac{1}{1 + 1/0.22}\right)$$

$$= 19.8 \text{ pf}$$



$$\frac{1}{G_L} = (1 + Q^2)R_2$$

Figure 15

The total load capacitance C_L which was determined from the selectivity requirement is:

$$C_L = C_{A2} + C_{L2} + C_{out}$$

where C_{A2} is additional capacitance required to give C_L. Then:

$$\begin{aligned} C_{A2} &= C_L - C_{L2} - C_{out} \\ &= 168 - 19.8 - 10.6 \\ &= 138 \text{ pf} \end{aligned}$$

A variable capacitor supplies this additional capacitance.

The 50-ohm generator impedance is matched to Y_{in}^* in the same manner.

$$Y_{in} = (8.5 + j7.4)\,10^{-3}$$

$$\begin{aligned} Q &= \sqrt{\left(\frac{1}{(8.5)\,(50) \times 10^{-3}}\right) - 1} \\ &= 1.16 \end{aligned}$$

$$\begin{aligned} \omega C_1 &= \frac{1}{(1.16)\,(50)} \\ &= 0.0173 \text{ mhos} \\ C_1 &= 45.7 \text{ pf} \end{aligned}$$

Use $C_1 = 47$ pf;

$$\begin{aligned} C_2 &= 47\frac{1}{1 + 1/(1.16)^2} \\ &= 26.9 \text{ pf} \end{aligned}$$

The transistor capacitance is:

$$\begin{aligned} C_{in} &= \frac{B_{in}}{\omega} \\ &= 20 \text{ pf} \end{aligned}$$

Choosing an input circuit $Q = 3$ will result in an amplifier bandwidth of approximately 13 mc. For this circuit:

$$Q = \frac{B_T}{2G_{in}}$$

where:

$$B_T = \omega(C_{in} + C_2 + C_{A1})$$

and C_{A1} is the additional capacitance.

$$\begin{aligned} B_T &= 2QG_{in} \\ &= (2)\,(3)\,(8.6 \times 10^{-3}) \\ &= 51.6 \times 10^{-3} \\ \omega C_{A1} &= B_T - \omega(C_{in} + C) \\ &= 51.6 \times 10^{-3} - (3.77 \times 10^8)\,(26.9 + 20)\,10^{-12} \\ C_{A1} &= 89.5 \text{ pf} \end{aligned}$$

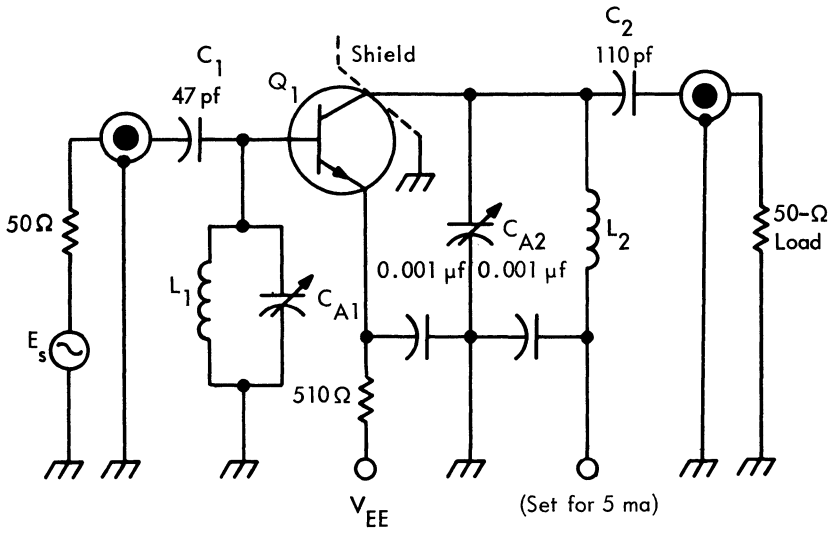
Again use a variable capacitor to supply this capacitance.

$$L_1 = \frac{1}{\omega^2 C_T}$$

$$= \frac{1}{(3.77 \times 10^8)^2 (1.35 \times 10^{-10})}$$

$$= 0.052\ \mu h$$

The circuit diagram is shown in Fig. 16 and the measured performance is given in Table 4. Measured gain, bandwidth, and input admittance agree very well with the computed values. The input admittance was also measured for $G_L = 24$ mmhos to indicate the input-output isolation. Single-stage amplifiers do not generally require this much isolation, but multi-stage amplifiers demand it. Multi-stage design follows the same general procedure with the exception that Y_{in} calculated at maximum gain must now be transformed by an appropriate matching network to the correct collector load. This procedure is followed for as many stages as required. The input stage is then matched to the generator impedance.



Components

L_1=1 1/2T, #14 wire, 1/4" dia

L_2=2T, #14 wire, 1/4" dia

C_{A1}, C_{A2}=Arco 465 (or equivalent) 45-380 pf

Q_1=2N743

δ(alignability)=0.3

Typical performance

G_T=11.5 db

BW≅10 mc

Fig. 16. 2N743 60-mc amplifier.

Table 4. Amplifier Performance

2N743 60-mc AMPLIFIER $I_c = 5$ ma $V_{ce} = 5$ volts				$G_L = 16$ mmhos		$G_L = 24$ mmhos	
UNIT	GAIN db	f_{HIGH} mc	f_{LOW} mc	G_{in} mmhos	B_{in} mmhos	G_{in} mmhos	B_{in} mmhos
81	12.2	64.8	55.2	5.53	5.84	5.13	5.35
82	12.1	64.8	55.2	8.55	8.2	8.0	7.61
83	11.2	64.8	55.0	9.53	9.45	8.93	8.85
85	12.0	64.8	54.9	6.95	7.46	6.92	6.75
86	11.2	64.8	54.9	8.93	7.73	8.34	7.35
88	12.1	64.8	54.3	9.62	8.2	9.17	7.68
93	11.2	64.8	54.8	10.62	8.85	10.3	8.33
95	10.8	64.8	55.2	7.8	5.46	7.46	5.2
96	10.0	65.0	55.2	8.85	5.82	8.4	5.65
98	11.3	64.9	55.2	7.7	6.1	7.4	5.8

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6

Small-signal UHF Amplifier Design

by George Johnson

INTRODUCTION

This chapter describes the design procedure for a 450-mc RF amplifier. Admittance parameters are used to describe the linear active network (LAN). A Linvill Chart of the LAN is used to select load and source terminations for a specified gain. Admittance-impedance charts are used to design coupling networks. Amplifier construction is discussed and experimental results of gain measurements are shown to compare well with predicted values.

POWER GAIN-STABILITY DESCRIPTION OF THE LAN

In order to get a complete description of the LAN at 450 mc, a set of y data was measured using the General Radio Transfer Function Bridge. Since the full set of y data completely characterized the LAN, its gain and stability properties may be accurately indicated. The accuracy of the y data is determined by "T-bridge" and is not subject to jig errors* (as such) because no jig is required with the T-bridge. The admittance parameters that are used in the design example are those of a germanium epitaxial mesa transistor.

$$y_{ie} = 29.7 + j14.3 = 33 \angle 25.8^\circ \text{ mmhos}$$

$$y_{re} = -0.38 - j2.0 = 2.0 \angle 259.2^\circ \text{ mmhos}$$

$$y_{fe} = -10.3 - j50.2 = 51.3 \angle 258.4^\circ \text{ mmhos}$$

$$y_{oe} = 0.93 + j5.31 = 5.39 \angle 80.0^\circ \text{ mmhos}$$

*There are, however, certain precautions which should be taken in nulling the bridge and minimizing lead length between the header and the face of the T-bridge socket. Lead length for the above data was $\cong$ 1.7 millimeters. Data above were taken with the fourth lead grounded.

One of the most important properties of the device is its inherent stability.* The device may be either potentially unstable or unconditionally stable. The criterion for unconditional stability is given by Eq. (1).

$$2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) > |y_{12}y_{21}| \tag{1}$$

where g_{11} is $\mathrm{Re}(y_{11})$

This expression may be modified slightly to make it more explicit. The quantity C is defined as a degree of inequality and is called the stability factor. Equation (2) shows this relation.

$$2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21}) = \frac{1}{C}|y_{12}y_{21}| \tag{2}$$

If the value of C is less than unity, then Eq. (1) is satisfied and the device is unconditionally stable. This means that no complex input or output termination may be found which will cause the LAN to oscillate. If C is greater than unity, then the converse is true. The value of C for the device described by the above y parameters is:

$$\begin{aligned} C &= \frac{|y_{21}y_{12}|}{2g_{11}g_{22} - \mathrm{Re}(y_{12}y_{21})} \\ &= \frac{105}{2(29.5)(0.93) - (-97)} \\ &= \frac{105}{152.1} \\ &= 0.69 \end{aligned}$$

The stability factor is less than unity; therefore, the device is unconditionally stable at 450 mc. And because C is considerably less than unity, the amplifier will be very stable. Now consider the gain of the LAN. The value of h_{fe} at 450 mc is:

$$\begin{aligned} h_{fe} &= \frac{y_{fe}}{y_{ie}} \\ &= \frac{51.3 \angle 258.4^\circ}{33 \angle 25.8^\circ} \\ &= 1.56 \angle 232.6^\circ \\ &= 3.87 \text{ db} \end{aligned}$$

The resulting value of f_t (assuming 6 db/octave roll-off)† is:

$$\begin{aligned} f_t &= (1.56)(450) \\ &= 700 \text{ mc} \end{aligned}$$

*Inherent stability refers specifically to the device stability without external circuitry. Actual stability, on the other hand, takes into consideration the total external shunt conductances of g_{11} and g_{22}. It is therefore not independent of the circuit as is the inherent stability factor C.

†This is a good assumption since the numeric value of h_{fe} at the frequency is almost 2.

The power gain G_{oo} is defined in the following way:

$$G_{oo} = \frac{\text{Power delivered to Re } (Y_L)}{\text{Power delivered to input of two-port}}$$

where Y_L is conjugately matched to y_{22}

The value of G_{oo} may be calculated for the LAN by using the following expression:

$$G_{oo} = \frac{|y_{21}|^2}{4g_{11}g_{22} - 2\text{Re}(y_{12}y_{21})}$$

$$= \frac{C}{2}\left|\frac{y_{21}}{y_{12}}\right|$$

$$= \frac{0.69}{2}\left|\frac{51.3}{2.0}\right|$$

$$= 8.7 \text{ or } 9.4 \text{ db}$$

Had C been greater than unity, the value of G_{max} would have been unbounded. However, since $C = 0.69$, G_{max} is finite and may be calculated by evaluating K_G and multiplying by G_{oo}:

$$K_G = \frac{2(1 - \sqrt{1 - c^2})}{c^2}$$

$$= 1.15$$

$$G_{max} = (K_G)(G_{oo})$$
$$= (1.15)(8.7)$$
$$= 10 \text{ db}$$

These calculations indicate that the LAN at 450 mc will be unconditionally stable, will have an h_{fe} of about 4 db ($f_t \cong 700$ mc), and will have a G_{max} of 10 db.

The display of the gain and stability of the LAN is uniquely combined in a graphic representation devised by Linvill. The calculations and constructions of this system are presented in Appendix I to this chapter. The finished Linvill Chart is shown in Fig. 5. It is essentially a plot of gain on a field of output admittance (in terms of $G_2 \pm jB_2$). The utility of such a chart is two-fold. First, it shows exactly what complex load will result in G_{max}. Second, it shows that no load which may be selected would cause instability.

LOAD CALCULATION

The evaluation of the load to obtain G_{max} of 10 db is done as follows:

$$G_2 + jB_2 = G_L + jB_L + y_{22}$$

Solving for G_L:

$$G_L = G_2 - y_{22r}$$
$$= 3y_{22r} - y_{22r}$$
$$= 1.86 \times 10^{-3} \text{ mhos}$$

Now, evaluating the reactive part:

$$\begin{aligned} B_L &= B_2 - y_{22i} \\ &= 0.7y_{22r} - y_{22i} \\ &= -4.65 \times 10^{-3} \text{ mhos} \end{aligned}$$

The load should be $1.86 - j4.65$ mmhos to yield 10 db gain.

OUTPUT NETWORK DESIGN

The load of 50 ohms must be transformed to $1.86 - j4.65$ mmhos. This may be done with the aid of an admittance-impedance chart. Appendix II discusses this type of chart and its use. One possible form of the network is shown in Fig. 1. It was chosen because the capacitor offers d-c isolation and impedance matching.

Locate the 50-ohm load on the impedance coordinate system, using a scale factor of one unit as 200 ohms or 0.5×10^{-2} mhos. This is located on the horizontal axis at R = 0.25. The value of the series capacitive reactance is added as a vertical line down from 0.25. The amount of reactance necessary to transform 50 ohms to 540 ohms is obtained by moving down from 50 ohms to the constant conductance circle marked G = −0.37.

$$\begin{aligned} G &= \frac{200\,\Omega}{0.37} \\ &= 540\,\Omega \end{aligned}$$

At this point the transformation from 50 to 540 ohms is completed, but as can be seen, the terminal value is rather capacitive. In order to neutralize this it is clearly necessary to add $-jB$ to the $+jB$ already present due to the transformed value of the series capacitor. If a transformation from 50 ohms to 1.86 mmhos instead of $1.86 - j4.65$ mmhos had been desired, the amount of shunt inductance would have been indicated by:

$$\begin{aligned} B &= (-1.1)(0.5 \times 10^{-2}) \\ &= -0.55 \times 10^{-2} \text{ mhos} \end{aligned}$$

However, the Linvill Chart indicates that a complex load is necessary to achieve the value G_{max}, so locating the desired load point:

$$\text{Real part: } \frac{1.86 \times 10^{-3}}{0.5 \times 10^{-2}} = 0.37 \text{ units}$$

$$\text{Imaginary part: } \frac{-4.65 \times 10^{-3}}{0.5 \times 10^{-2}} = -0.93 \text{ units}$$

Now instead of stopping at the horizontal axis, the process is continued until the point $0.37 - j0.93$ is reached. The above discussion is made clearer by Fig. 2.

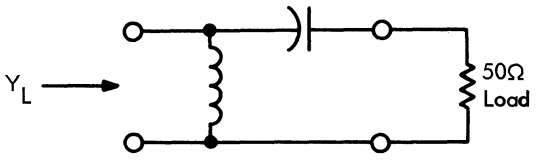


Fig. 1. Load resistance transforming network.

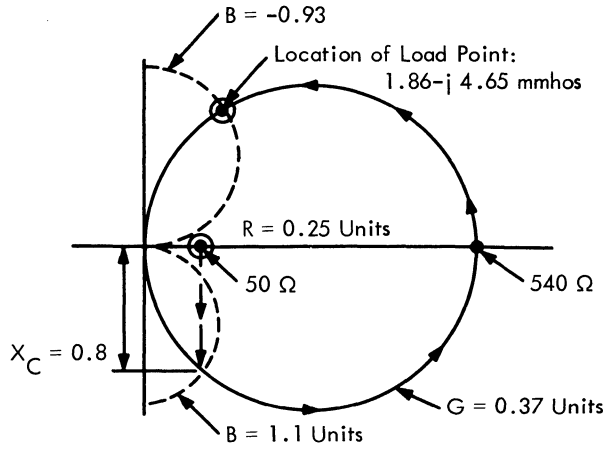


Fig. 2. Impedance-admittance chart for output network.

Solving for the value of X_c gives:

$$X_c = (0.8)(200)$$
$$= 160\,\Omega$$
$$C = 2.2 \text{ pf at } 450 \text{ mc}$$

Now solving for the amount of shunt inductance necessary to move to desired load point on the constant-conductance circle, G = 0.37.

$$X_L = \frac{200}{2.03} = 98\,\Omega \quad (\text{where } 2.03 = 1.1 + 0.93)$$

$$L = 0.034\ \mu\text{h at } 450 \text{ mc}$$

The resulting network shown in Fig. 3 performs the desired impedance transformation at 450 mc.

To allow tuning of the above network, a shunt capacitance is added. It is calculated by selecting a fractional bandwidth of 0.1.

$$\text{FBW} = 0.1 \qquad (45 \text{ mc})$$
$$Q_L = 10$$
$$= (540)(6.28)(450 \times 10^6)C$$

$$C = \frac{10}{(540)(6.28)(450 \times 10^6)}$$

$$= 6.5 \text{ pf}$$

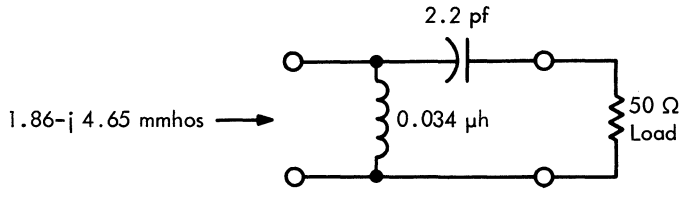


Fig. 3. Load resistance transforming network.

The inductance required to resonate with 6.5 pf is 0.02 μh at 450 mc. The network appears as in Fig. 4.

INPUT NETWORK DESIGN

Before designing the input networks, the value of the input immittance must be obtained for the specified load. This may be calculated using Eq. (3).

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \tag{3}$$

where $Y_L = 1.86 - j4.65$ mmhos

However, a quicker way has been devised which not only reduces the amount of complex algebra but allows a much more rapid analysis of input immittance for changing load conditions. Its application is discussed in Appendix III so that the design sequence presented so far will not be interrupted.

As demonstrated in Appendix III,

$$Y_{in} - y_{11} = G_1 + jB_1 \tag{4}$$

By placing a quadrant chart over the Linvill Chart (Fig. 5) and rotating it so that its real axis lies along the gradient line, we may evaluate the input impedance. Reading the values of:

$$\frac{G_1}{\left|\frac{y_{12}y_{21}}{2y_{22r}}\right|} = 0.52$$

and

$$\frac{B_1}{\left|\frac{y_{12}y_{21}}{2y_{22r}}\right|} = -0.39$$

$$\left|\frac{y_{12}y_{21}}{2y_{22r}}\right| = \frac{105 \times 10^{-6}}{(2)(0.93 \times 10^{-3})}$$

$$= 56.5 \times 10^{-3}$$

which are indicated by the point of maximum gain, we may calculate the value of Y_{in}. Substituting in Eq. (4):

$$Y_{in} = (0.52)(56.5 \times 10^{-3}) - j(0.39)(56.5 \times 10^{-3}) + 29.7 \times 10^{-3} + j14.3 \times 10^{-3}$$
$$= 59.1 \times 10^{-3} - j7.7 \times 10^{-3}$$

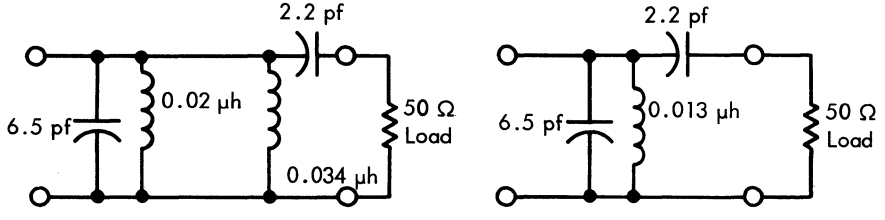


Fig. 4. Complete output network.

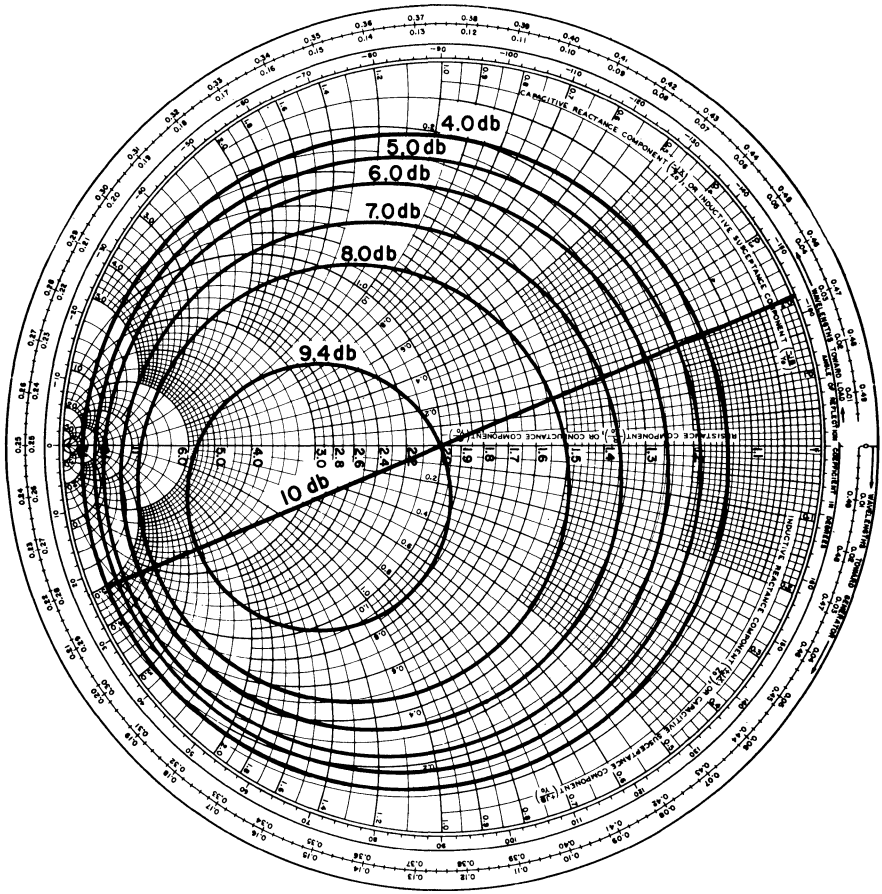


Fig. 5. Linvill chart.

Therefore the input admittance of the terminated stage at 450 mc is as shown in Fig. 6. The input network to match the generator to this admittance will be as shown in Fig. 7. And the complete input circuit with d-c return for the base and d-c block for the input will take the form shown in Fig. 8.

In designing the input network, use 1 unit = 50 ohms or 0.02 mmhos. The input admittance is $59.1 - j7.7$ mmhos, which becomes $2.9 - j0.385$ units. Locating this on the admittance chart establishes the starting point. Notice that the input admit-

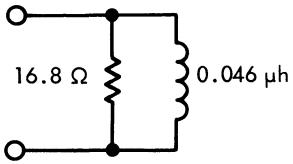


Figure 6

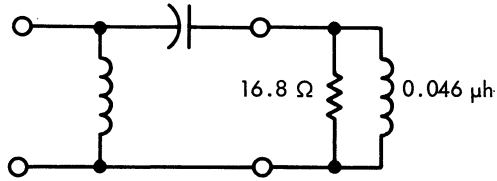


Figure 7

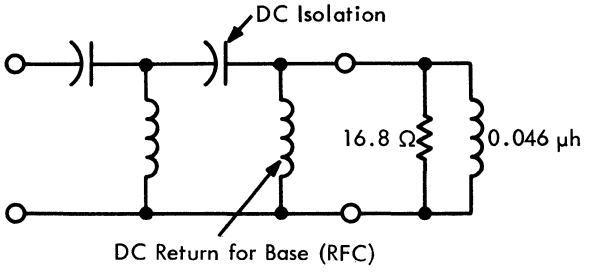


Figure 8

tance is automatically converted to a series combination simply by reading the rectangular coordinates at this point.

The first component in the desired network is a series C which requires a move straight down the chart from 2.9 − j0.385 until the constant-conductance circle of 1 is intersected. This is the value to which 16.8 ohm is transformed. The value of X_c required is:

$$X_c = (0.58)(50)$$
$$= 29\,\Omega$$
$$C = 12 \text{ pf at } 450 \text{ mc.}$$

Moving around the constant-conductance circle from B = 1.25 to B = 0 requires a shunt inductance to be added to the network. Its value is:

$$X_L = \frac{50}{1.25}$$
$$= 40\,\Omega$$
$$L = 0.014\ \mu\text{h at } 450 \text{ mc.}$$

The admittance-impedance chart of Fig. 9 pictures the above discussion. The completed network is as shown in Fig. 10. The completed circuit is shown in Fig. 11.

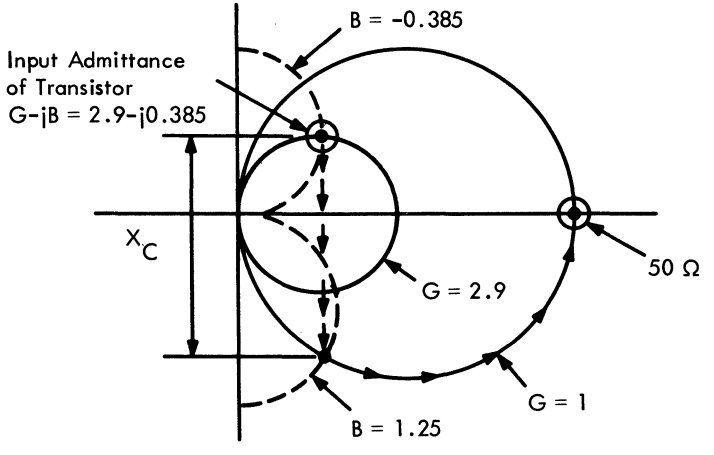


Figure 9. Input circuit design.

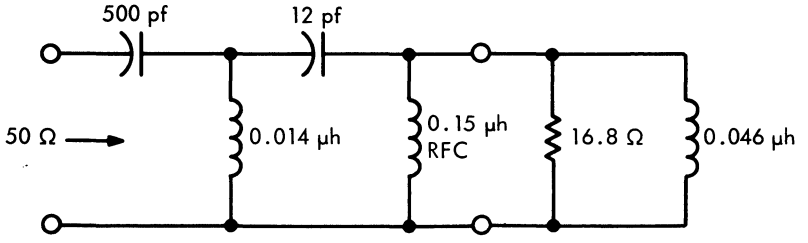


Fig. 10. Input network.

EXPERIMENTAL RESULTS

Average power gain was measured at 8.6 db. The output tank Q_L is 10 and the Q_U of the inductor is 100, so the insertion loss of the network is 1 db. Since G_{max} was 10 db, this indicates that the typical power gain should have been about 9 db. The difference between 8.6 db and 9 db is probably due to small but finite losses in the input network and to experimental and measurement errors. Bandwidth measured on the amplifier was 48 mc. This compared to the design bandwidth of 45 mc. The difference is probably due to the slight differences in actual Y_{Yr} value in the output circuit because of the tolerances of standard value capacitances used in the transforming networks.

Noise figure was about 6 db. The coincidence of best noise figure and best gain was quite close.

The construction of this circuit was straightforward. A brass two-section box approximately 3" x 2" x 1" was used. The coils were made of copper strips approximately ½" wide, 1/32" thick and 1" long. Silvered miniature air-variable capacitors were used in the tanks. Care was taken to minimize the lead inductance by modifying the TO-18 Teflon* socket. Most of the Teflon was removed so that only a thin disc, approximately the chassis thickness, remained. The bypass and decoupling 500-pf capacitors were high-quality r-f ribbon types.

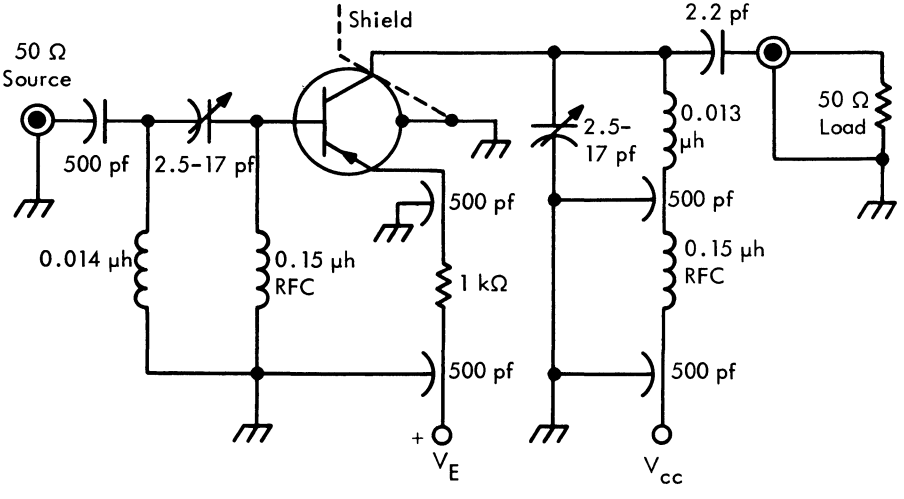


Figure 11

*Trademark of DuPont Corporation.

APPENDIX I: POWER FLOW IN A GENERAL TWO-PORT

A general two-port is defined and used to demonstrate power flow. The input power is derived and shown to be a plane. The output power is derived and shown to be a paraboloid. The combination of these two surfaces describes power gain. Potential instability and unconditional stability are defined and demonstrated graphically.

Consider the general two-port of Fig. 12. The choice of h parameters is arbitrary; any consistent set of parameters could be used. The choice of generators shown in Fig. 12 is for h parameters. Had y parameters been used, the output generator would have been a current generator but its complex identity would have been of the same form. The input current generator may be normalized to $1 + j0$ amps. The value of the output generator may be changed by varying a or b. In this way any load condition may be simulated.

Define the system of coordinates as shown in Fig. 13. The term P_o is output power. The form of the mathematical equation representing output power is a paraboloid. It is convenient to choose a new set of rectangular coordinates L and M to describe this paraboloid.

Define P_{oo} as the maximum power output from the model of Fig. 12 if the effect of h_{12} is neglected. It occurs as shown in Fig. 13 at L, M = 1, 0. Under these conditions it is obvious that:

$$P_o = \mathrm{Re}(-E_2{}^*I_2)$$

The general form of the power to the load is:

$$P_o = \mathrm{Re}(-E_2{}^*1_2)$$

where

$$-E_2 = (L + jM)\left(\frac{h_{21}}{2h_{22r}}\right)$$

Therefore the dimension for $(L + jM)$ is amps, and of course the dimension of $h_{21}/2h_{22r}$ is ohms.

Thus

$$-E_2 = (L + jM)\left(\frac{h_{21}}{2h_{22r}}\right)$$

$$= (\text{amps})(\text{ohms}) = \text{volts}$$

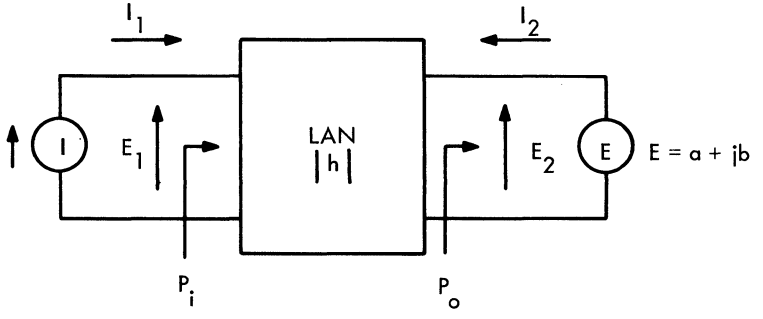


Fig. 12. Two-port power flow model.

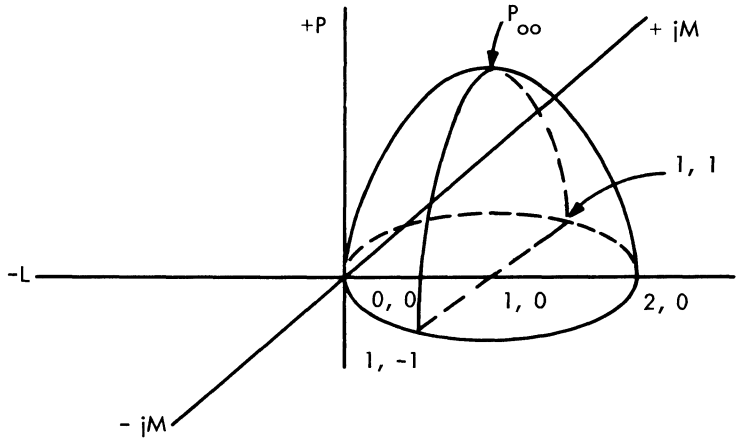


Fig. 13. Power out description.

If E_2, the "generator-load" component, is less than the output voltage produced at the output port by the signal at the input port, then the generator actually represents an IR drop rather than an EMF. If it is an IR drop it may be considered as being identical to a passive immittance.

Now writing the expression for P_o,

$$I_2 = h_{21}(1 + jO) + h_{22}(L + jM)\left(-\frac{h_{21}}{2h_{22r}}\right)$$

and

$$P_{oo} = \frac{|h_{21}|^2}{4h_{22r}}$$

Since

$$P_{oo} = |E_2|^2 Y_{Lr} = E_2^2 h_{22r} = \frac{|h_{21}|^2}{4h_{22r}}$$

then $|E_2|^2$ must be:

$$|E_2|^2 = \frac{|h_{21}|^2}{4(h_{22r})^2}$$

$$|E_2| = \frac{|h_{21}|}{2h_{22r}}$$

The value P_{oo} occurs at $L + jM = 1 + j0$ so it is clear that an appropriate choice for the variables a and jb is:

$$E_2 = a + jb = (L + jM)\left(-\frac{h_{21}}{2h_{22r}}\right)$$

Therefore

$$P_o = \mathrm{Re}(E_2^*)(I_2)$$

$$= \mathrm{Re}\left\{\frac{(h_{21})^*(L - jM)}{2h_{22r}}\left[h_{21} - \frac{(L + jM)(+h_{21})h_{22}}{2h_{22r}}\right]\right\}$$

$$= \frac{L|h_{21}|^2}{2h_{22r}} - \frac{(L^2 + M^2)|h_{21}|^2}{4h_{22r}}$$

The input power is given by:

$$P_i = \mathrm{Re}(E_1^*)(I_1)$$

$$E_1 = h_{11}I_1 + h_{12}E_2$$

$$= h_{11}(1 + j0) + h_{12}(L + jM)\left(\frac{-h_{21}}{2h_{22r}}\right)$$

$$P_i = h_{11}(1 + j0)(1 + j0) + h_{12}(1 + j0)(L + jM)\left(\frac{-h_{21}}{2h_{22r}}\right)$$

$$= h_{11r} - L\,\mathrm{Re}\left(\frac{h_{12}h_{21}}{2h_{22r}}\right) + M\mathrm{Im}\left(\frac{h_{12}h_{21}}{2h_{22r}}\right)$$

This is the equation of a plane in the coordinate system of Fig. 13. Figure 14 shows this general relationship. Cutting the model of Fig. 14 along the plane ABC yields Fig. 15.

It is quite apparent from this figure that the maximum power gain occurs at a distance d to the left of the 1.0 point. The following derivations can be made using geometry and Fig. 15.

$$\frac{f}{e} = 2\left(\frac{1 - \sqrt{1 - c^2}}{c^2}\right) = K_G$$

$$d = \frac{CK_G}{2}$$

$$C = 2\frac{P_{oo}}{P_{io}}\left|\frac{h_{12}}{h_{21}}\right| = \frac{|h_{21}|\,|h_{12}|}{2h_{11r}h_{22r} - \mathrm{Re}(h_{12}h_{21})}$$

and when $C < 1$:

$$G_{max} = K_G\frac{P_{oo}}{P_{io}}$$

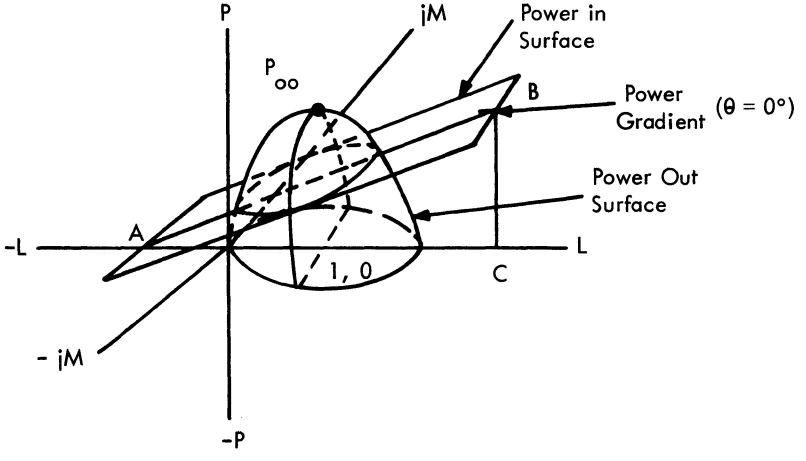


Fig. 14. Power gain model.

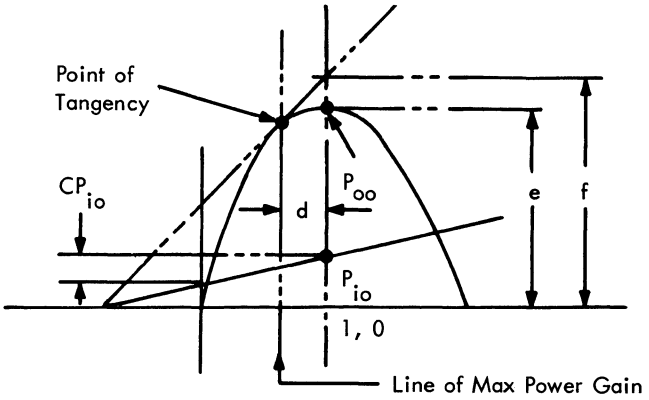


Fig. 15. Two-dimensional view of power gain model.

The Linvill Chart. The L-M plane has been discussed and shown to be a way of representing a wide variety of load conditions for the two-port. The actual load admittance must be related to this L-M plane. This may be done by considering the following expressions:

$$I_2 = I_1 h_{21} + E_2 h_{22}$$

$$= (1 + j0)h_{21} - (L + jM)\left(\frac{+h_{21}}{2h_{22r}}\right)h_{22}$$

$$= -Y_L E_2$$

$$Y_L E_2 = Y_L \frac{L + jM}{2h_{22r}} h_{21}$$

$$Y_L \frac{L + jM}{2h_{22r}} h_{21} + \frac{L + jM}{2h_{22r}} h_{22} h_{21} = h_{21}$$

$$Y_L + h_{22} = \frac{2h_{22r}}{L + jM} = G_2 + jB_2$$

In the L-M plane the real and imaginary parts, G_2 and jB_2, are mutually orthogonal circles. This kind of a plot is shown in Fig. 16.

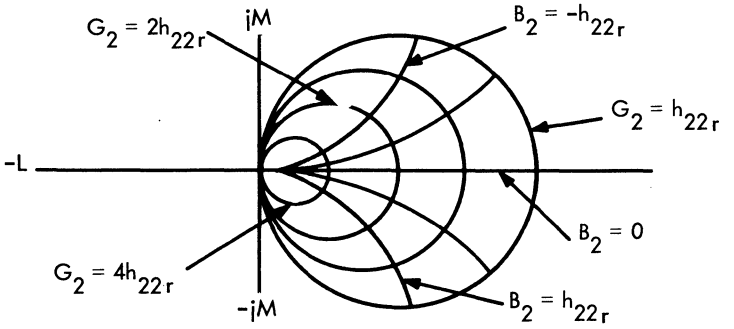


Fig. 16. $G_2 + jB_2$ in the LM plane.

APPENDIX II: LOSSLESS MATCHING TECHNIQUES

There are many ways to realize practical matching networks. The efficiency of modern synthesis is astounding, but in many cases its realization techniques are too detailed for simple matching problems. The method described here deals with coupling networks that are made from lumped, linear, constant-valued elements. It makes use of immittance charts which reduce the calculations of components to simple evaluation of reactance into inductance or capacitance. With a reactance-frequency chart or reactance slide rule, these calculations are eliminated and the whole problem reduces to simply reading the values of the network components.

The Admittance-Impedance Chart. Consider the Cartesian coordinate system of Fig. 17. This system defines all impedance functions that have positive real parts. This chart may be transformed into a system of orthogonal circles that have a common tangent point at 0. This transformed system represents all admittance functions which have positive real conductance values, and is shown in Fig. 18. Superimposing these charts results in Fig. 19.

From these charts it is obvious that

$$Z = R + jX = \frac{1}{Y} = \frac{1}{G + jB}$$

As a result it is also obvious that the problem of converting a series combination to a parallel combination of real and imaginary terms is accomplished simply by locating the parallel combination on the appropriate orthogonal circles and reading the R and X values indicated. A general chart of this type is shown in Fig. 19.

The Real Source-Load Transformation. Consider the problem of transforming 50 ohms to 450 ohms. The procedure is to systematically "build" the immittance matching network by first adding a series component of the appropriate value and then adding a shunt component of the appropriate value. The dual chart shown in Fig. 19 is used to decide what these values are. When a series component is added, the R-X part of the chart is used. Then when a shunt element is added, the orthogonal admittance coordinate system is used. Since they are superimposed as in Fig. 19, the change from one chart to the other is simply a change in the type of motion, either rectangular or circular. Since it is in normalized form, the first step is to decide on a scale factor which will put both the load and source on the

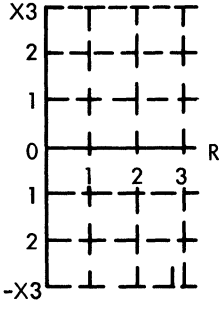


Fig. 18. Orthogonal admittance coordinate system.

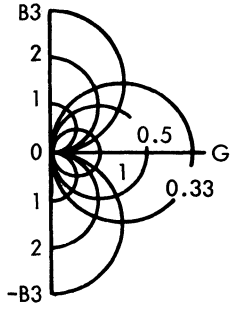


Fig. 17. Rectangular impedance coordinate system.

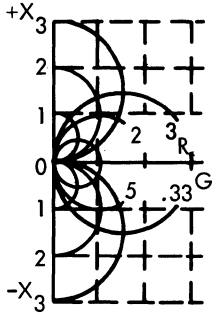


Fig. 19. Admittance impedance system.

chart. For the above values of 50 ohms and 450 ohms this scale factor may be chosen as

$$1 \text{ unit} = 100\ \Omega \text{ (or } 0.01 \text{ mhos)}$$

Starting with the 50-ohm load and using the rectangular system of coordinates, locate the point 0.5, which is:

$$\frac{50\,\Omega}{100\,\Omega/\text{unit}} = 0.5 \text{ units}$$

This point is located at (1) in Fig. 20. A value of series capacitive reactance may be added to 50 ohms by moving straight down from the 50 ohms point, (1), to point (2) The amount of this capacitive reactance determines the resistance transformation. Since 450 ohms or 4.5 units is the desired value, the amount of X_c must extend down to the constant-conductance circle of 0.22 units. Point (2) is then considered as being on the circle system shown in Fig. 18. This converts the series combination of R and C to a parallel combination. Adding shunt inductance to resonate with this shunt capacitance will not change the shunt real part, so going from (2) to (3) must be along the constant-conductance circle (0.22 units). Of course, this circle was chosen so that (3) would be 450 ohms. Notice that moving

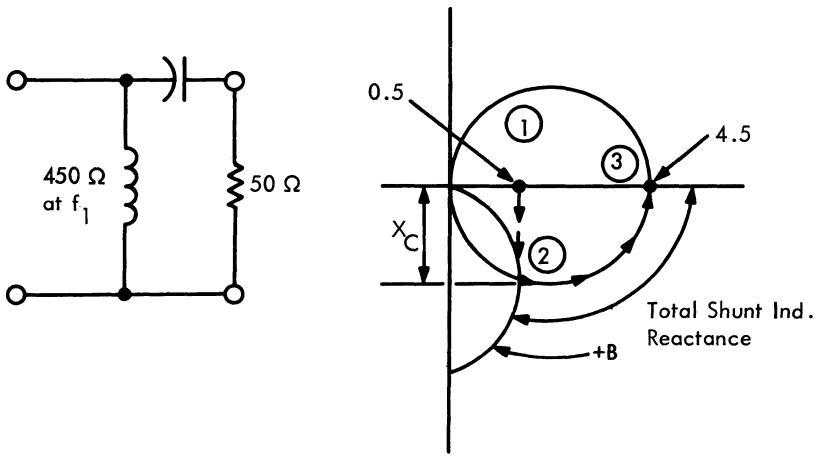


Fig. 20. Series capacitance L-section.

from (2) to (3) on the constant-conductance circle requires the addition of a shunt $-B$ to counteract the value of $+B$ at (2). This is an inductive susceptance. Addition of such a susceptance completes the transformation.

Another network will also perform this transformation. Figure 21 shows the path followed when a series coil is used rather than a series capacitor.

Complex Load-Source Transformation. There is no essential difference in the technique if both load and source are complex. Consider the following example:

$$\text{Input} = R_s + jX_s$$
$$\text{Load} = G + jB$$

The chart looks like Fig. 22.

APPENDIX III: INPUT IMMITTANCE

It is evident that a relation between the input impedance of the general two-port and the L-M plane exists. This may be shown by:

$$E_1 = I_1 h_{11} + E_2 h_{12} = Z_{in}$$

Since the general current is $1 + j0$, then $E_1/1 + j0$ is Z_{in}.

$$Z_{in} = (1 + j0)h_{11} + (L + jM)\frac{-h_{21}}{2h_{22r}} h_{12}$$

$$Z_{in} - h_{11} = R_1 + jX_1 = (L + jM)\frac{-h_{12}h_{21}}{2h_{22r}}$$

$$\frac{R_1 + jX_1}{Gr} = (L + jM)e^{-\theta}$$

where Gr is the gradient and θ is the angle of the gradient.

The values $\frac{R_1}{Gr}$ and $\frac{jX_1}{Gr}$ can be conveniently thought of as the coordinates

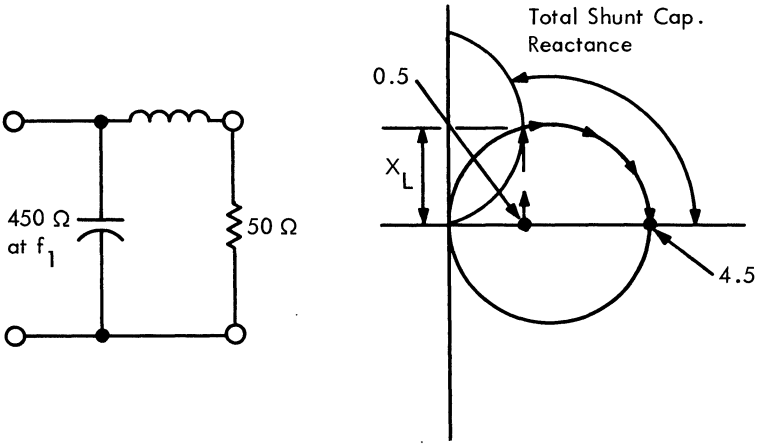


Fig. 21. Series inductance L-section.

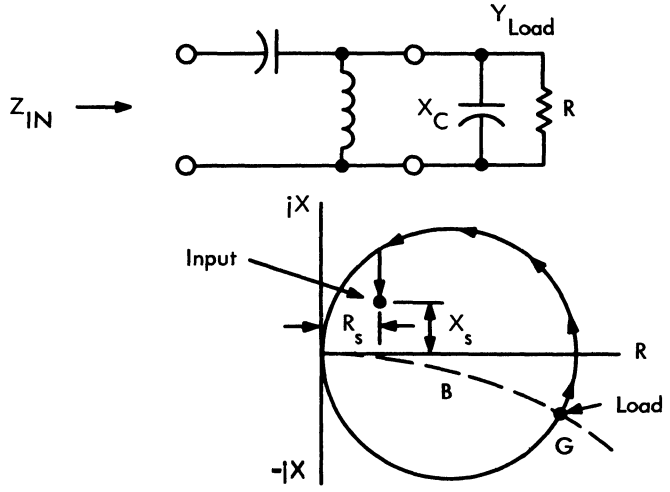


Fig. 22. Complex load-source chart.

of a rectangular grid which can be put over the L-M plane. Reading the value of $R_1/|\,Gr\,|$ and $jX_1/|\,Gr\,|$ it is possible to solve for Z_{in} using

$$Z_{in} - h_{11} = R_1 + jX_1$$

This equation is perfectly general. Had the characterization of the LAN been in y parameters, the equation would have been written

$$Y_{in} - y_{11} = G_1 + jB_1$$

The rectangular grid is shown in Fig. 23.

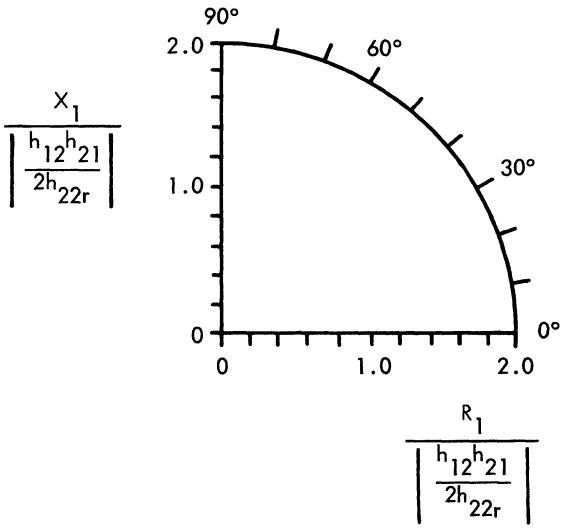


Fig. 23. Input immittance chart.

First transistorized TV receiver produced and priced for the high-volume market was introduced by Emerson Radio and Phonograph in 1964. The all-channel set uses 35 TI components.

7

Field-effect Transistors for Low-level Circuits

by L. J. Sevin and Stan Holcomb

A SIMPLIFIED THEORY

A Field-effect Transistor (FET) is essentially a semiconductor current path whose resistance is controlled by applying an electric field perpendicular to the current. The electric field results from reverse biasing a P-N junction.

When a P-N junction is reverse biased a "depletion" or space-charge layer develops on both sides of the junction. That is, the current carriers on either side of the junction are swept across and away from the junction, leaving regions that contain a net charge but no free current carriers except those generated by heat. The current-carrier density determines how well a semiconductor will conduct current; therefore, the space-charge region on either side of a P-N junction will be very low in conductivity.

Resistance of a Semiconductor Bar. Consider a bar of semiconductor silicon crystal having the dimensions shown in Fig. 1, excess impurity concentration P, and ohmic (non-rectifying) contacts at each end. The approximate resistance

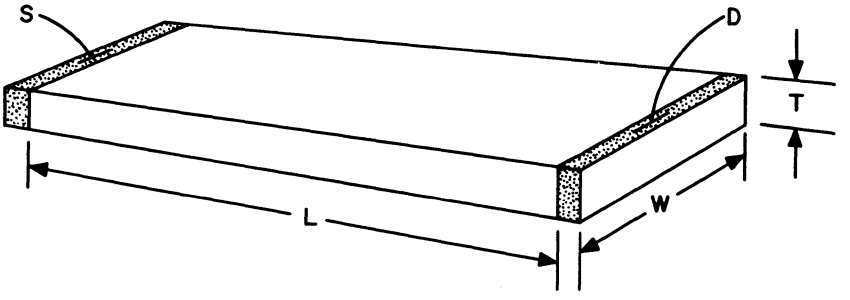


Figure 1

R_o between terminals S and D is:

$$R_o = \frac{L}{(q\mu)PWT}$$

where q = electron charge
μ = majority carrier mobility

The factor $q\mu P$ in the denominator is a good approximation for the conductivity σ of the semiconductor material if the doping level is such that the minority carrier density is negligible. Since the dimensions of the bar are fixed, the resistance of the bar must be controlled by controlling the conductivity.

Silicon Bar with P-N Junctions. Figure 2 shows a P-type bar of silicon which has had N-type impurities introduced into opposite sides, forming P-N junctions. The two N regions are electrically connected and a bias voltage (V_{GS}) is applied to the two junctions. The N regions are called gates and the space between the gates is called the channel. The resistance R_o is modulated by depleting carriers from parts of the channel.

Another view is that the effective thickness of the bar in Fig. 1 can be changed by a transverse electric field produced by the bias voltage V_{GS}. If the doping level in the gates is purposely very large compared to that in the channel, the carrier-depleted or "space-charge" zone will extend principally into the channel. Figure 3 is a graph of the net charge density, electric field, and potential through a cross-section of the channel for a given V_{GS}. Uniform charge density and ideal step junctions are assumed. The shaded areas above and below the zero concentration axis are equal, because the depleted regions on either side of the junction must contain equal net charge. The electric field and potential plots shown in Fig. 3 are obtained by performing successive integrations.

Behavior of Space-charge Layer With Channel Current. The simple field-effect structure of Fig. 2 is reproduced in Figs. 4(a) and (b) with an expanded vertical scale to allow a more graphic description of the behavior of the space-charge layer with an applied drain-to-source voltage. In Fig. 4(a), as the voltage V_{DD} is increased from zero to small values, the current rises linearly with V_{DS}. At small currents, the channel between the drain and source behaves as a linear resistor, but as current increases the parts of the channel near the junctions become significantly negative with respect to the source terminal. Since the N gates are connected externally to the source, the junctions are reverse biased and the space-charge

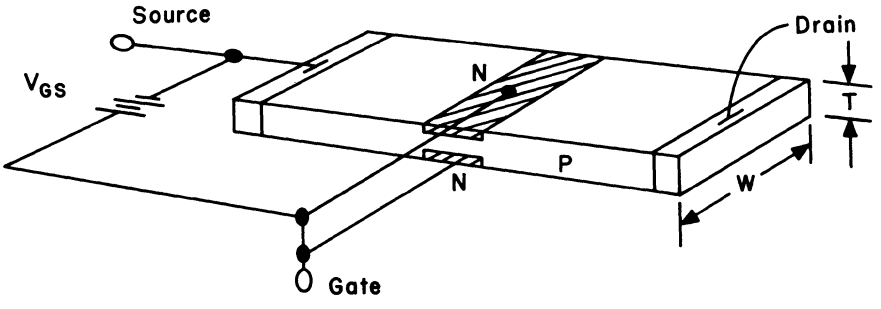


Figure 2

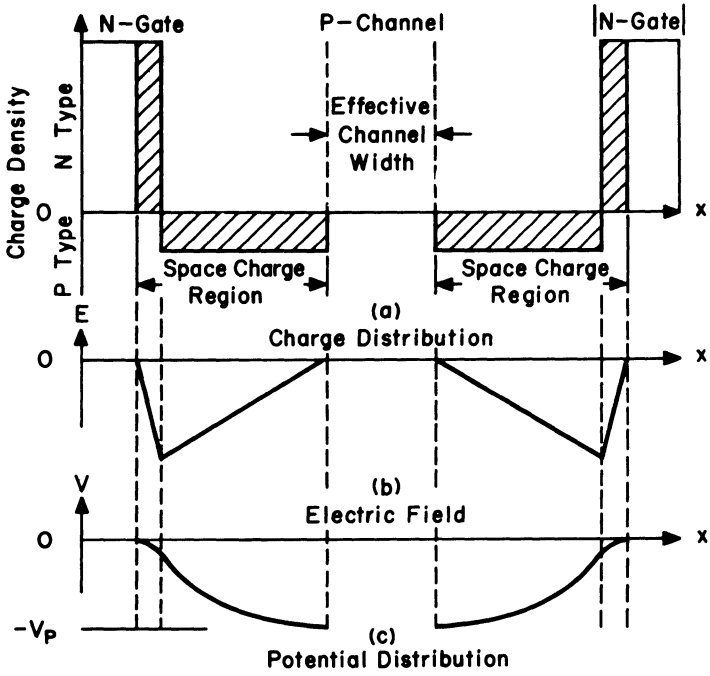


Figure 3

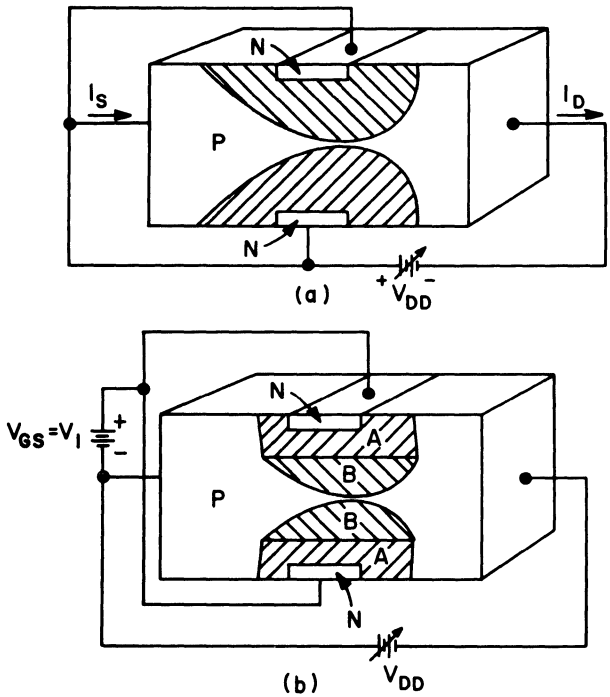


Figure 4

layers are extended into the channel, lowering the channel conductance. The electrical behavior of Fig. 4(a) is plotted in Fig. 5; note that the relatively constant slope at low voltages becomes less linear with increasing applied voltage. At some V_{DS} the space-charge layers extend into the channel until they almost meet, as shown by the shaded areas in Fig. 4(a); this corresponds approximately to the voltage at the "knee" of the $V_{GS} = 0$ curve in Fig. 5. Shockley[1] called this voltage the pinch-off voltage. Above the pinch-off voltage the drain current saturates; i.e., it increases very little for further increases in drain-to-source voltage. The fact that reverse bias on the P-N junction is greatest at the drain end gives the space-charge layers their characteristic wedge shape. Most of the potential drop in the channel is confined to the short span where the space-charge layers nearly meet; this is the active or control part of the device. The remainder of the drain-to-source voltage is dropped across the bulk channel resistance between the two terminals and this active part.

In Fig. 4(b) a fixed reverse bias, $V_{GS} = V_1$, is applied to the gates. With no channel current, there is no electric field component tangent to the junction and the space-charge layer extends uniformly part of the way into the channel (region A). When a drain current flows, both tangential and normal components of electric field are present, creating the wedge-shaped space-charge region B. The ratio of the thicknesses of regions A and B depends on the magnitude of the external reverse bias; higher values of V_{GS} increase the thickness of A relative to B. Obviously, less channel current is required to produce pinch-off as V_{GS} increases. In Fig. 5, the $V_{GS} = V_1$ curve has the same shape as the zero bias curve except that pinch-off occurs at a lower drain-to-source voltage and a lower drain current. The reverse bias on the junction required to bring the two space-charge layers together is the sum of the externally applied bias V_{GS} and the internal self bias due to current flow through the channel resistance. From this it seems that the external bias required to bring the two space-charge layers together should be capable of reducing the drain current to the reverse saturation current of the P-N junction. However, this pinch-off condition never occurs. In practice, the drain current approaches some irreducible minimum greater than the diode reverse saturation current.

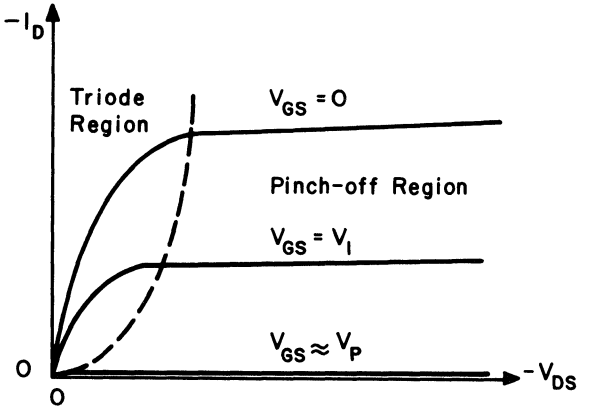
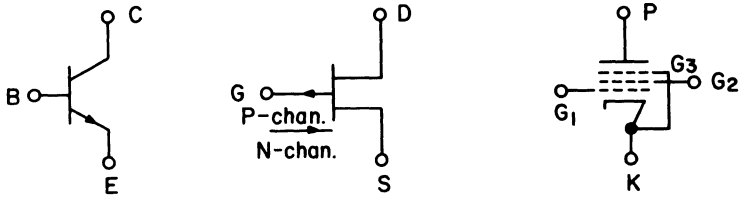


Figure 5



Junction Transistor | Field Effect Transistor | Vacuum Tube

Figure 6

Figure 5 is a set of curves that look remarkably like the output characteristics of a pentode vacuum tube, the drain, source, and gate terminals being analogous to the plate, cathode, and grid terminals respectively. The symbol adopted for the field-effect transistor is compared to those of the junction transistor and the triode vacuum tube in Fig. 6. Although the FET has only three terminals, its electrical behavior is closer to the pentode tube than to the triode tube.

Operation in the Pinch-Off Region. Aside from some suggested gain-control applications (which apparently have not been fully explored at this time) little use has been found for the FET operation in the triode or voltage saturation region. Because of the relatively high saturation voltage of the present device, it has not made an efficient switch. It has so far been most useful as an active element operating in the pinch-off region in linear applications, and it is here that we will place our emphasis.

At this point it is convenient to re-define the pinch-off voltage V_p as that gate-to-source voltage which should reduce the drain current to the reverse saturation current of the gate-channel diode. In practice, this voltage must be extrapolated from the behavior of drain current with gate-to-source voltage at drain currents significantly greater than zero.

The expression for the saturation drain current as a function of gate-to-source voltage derived by Shockley[1] is:

$$I_D = I_{DSS}\left[1 - 3\frac{V_{GS}}{V_p} + 2\left(\frac{V_{GS}}{V_p}\right)^{3/2}\right] \qquad (1)$$

The term I_{DSS} (per 56 IRE 28.S1) is the saturation drain current with zero gate-to-source bias voltage at any drain-to-source voltage in the pinch-off region below breakdown. Equation (1) was derived assuming a step junction, and is correct for both P-channel and N-channel devices since V_{GS} and V_p carry the same sign. The plot of Eq. (1) in Fig. 7 is the common-source forward transfer characteristic of the FET analogous to the common-cathode transconductance curve of a vacuum tube. This curve is in good agreement (except at low I_D) with transfer curves of practical field effects made by the alloy process; alloy junctions closely approximate step junctions.

Equation (1) must be modified to take into account the diode reverse saturation and leakage current, I_{GSS}:

$$I_D = (I_{DSS} + I_{GSS})\left[1 - 3\frac{V_{GS}}{V_p} + 2\left(\frac{V_{GS}}{V_p}\right)^{3/2}\right] - I_{GSS} \qquad (2)$$

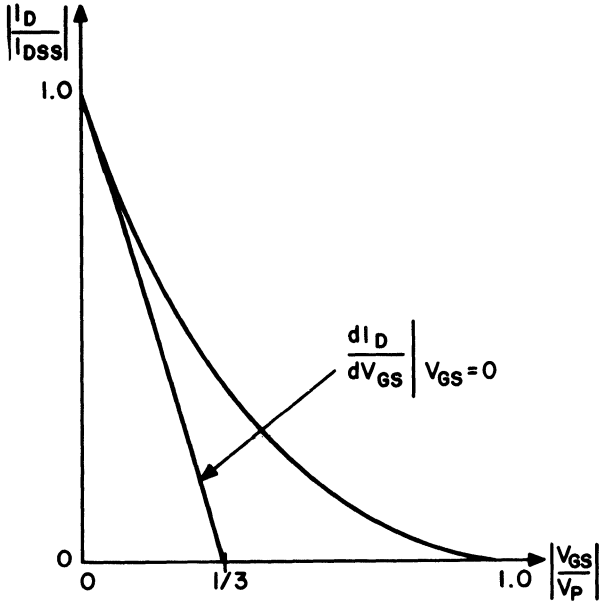


Figure 7

The disagreement between this expression and the behavior of practical devices is most marked at very low values of I_D. In practice, I_D cannot be reduced to I_{GSS} by the reverse bias on the gate-to-channel diode; as a result, D_p can be extrapolated from the measurement of V_{GS} at two or more values of I_D, or by measurement of the slope dI_D/dV_{GS} (forward transconductance), of the transfer curve at some value of V_{GS} (preferably $V_{GS} = 0$).

From Eq. (2):

$$\left.\frac{dI_D}{dV_{GS}}\right|_{V_{GS}=0} = -\frac{3}{V_p}(I_{DSS} + I_{GSS}) \qquad (3)$$

I_{GSS} can usually be neglected when compared to I_{DSS}. Equation (3) implies that a tangent drawn to a transfer curve at $V_{GS} = 0$ as in Fig. 7 will intersect the $I_D = 0$ axis at $1/3\ V_p$.

The derivation of Eq. (1) was done with the assumption that carrier mobility remains constant with reverse gate bias, i.e., the longitudinal electric field in the channel does not exceed a critical value (around 1000 v/cm) above which Ohm's law no longer holds.[2] This assumption is apparently valid for alloy field-effect transistors, but not for FET's made by a diffusion process. The longitudinal electric field in the channel of diffused types can exceed 1000 v/cm, and the carrier mobility then becomes proportional to the square root of the electric field. Dacey and Ross[3] derived an expression for the drain current behavior with gate-to-source voltage in the pinch-off region for the "square root" mobility case:

$$I_D = I_{DSS}\left\{4\left[1-\left(\frac{V_{GS}}{V_p}\right)^{1/2}\right]^3 - 3\left[1-\left(\frac{V_{GS}}{V_p}\right)^{1/2}\right]^4\right\}^{1/2} \qquad (4)$$

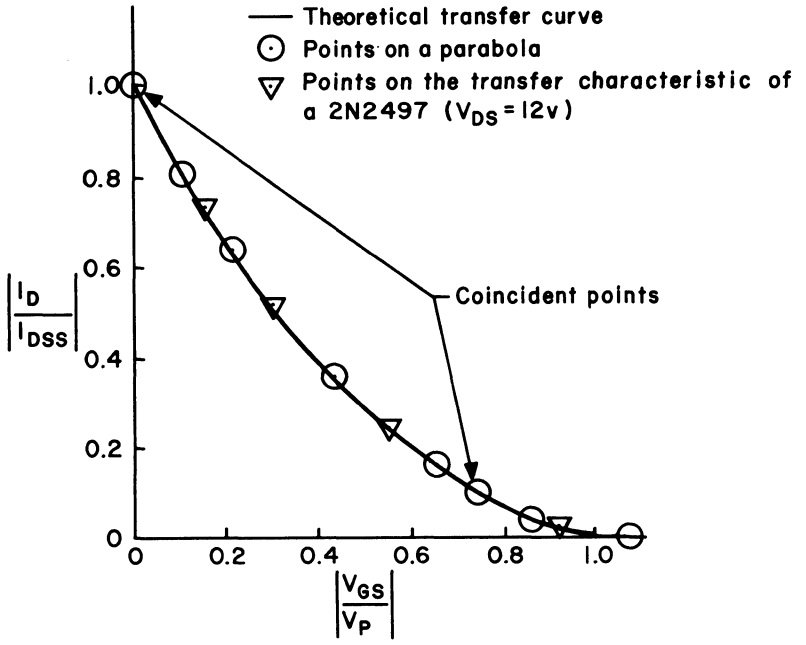


Fig. 8. Approximating the transfer curve with a parabola.

This is a more complicated expression than Eq. (1), but it agrees very well with the transfer characteristics of practical diffused type FET's. As in the case of Eq. (1), it fails at very low drain currents. An even better approximation to measured transfer curves is given by a simple parabola, properly "force-fitted" to Eq. (4). Figure 8 shows a plot of Eq. (4) with the points describing a force-fitted parabola superimposed. The force-fitting technique consists of selecting two points at which parabola and Eq. (4) are forced to coincide. The particular points selected, $I_D = I_{DSS}$ and $I_D = 0.1\ I_{DSS}$, give excellent results and are convenient for measurement. The parabola yields a slightly higher V_p than Eq. (4), i.e., 1.06/1, but the normalized transfer curve of a 2N2497 P-channel planar (diffused) FET plotted in Fig. 8 shows that the parabola is a better approximation at low currents.

The equation of the parabola in Fig. 8 is:

$$I_D = I_{DSS}\left(\frac{V_{GS}}{V_p} - 1\right)^2 \tag{5}$$

Taking into account the effect of I_{GSS}:

$$I_D = (I_{DSS} + I_{GSS})\left(\frac{V_{GS}}{V_p} - 1\right)^2 - I_{GSS} \tag{6}$$

Because virtually all of the FET's presently being marketed are made by some type of diffusion, this simple approximation can be a very powerful engineering tool for circuit design.

STATIC CHARACTERISTICS

Gate Cutoff Current. By connecting the drain to the source and reverse biasing the gate-channel diode, a measure of the direct-current input impedance and an indication of the quality of the diode can be obtained. A circuit for the measurement of this gate cutoff current I_{GSS} is shown in Fig. 9. The voltage used in this measurement is 10 volts, the gate being positive with respect to the channel for a P-channel device. If this voltage were increased in magnitude, a point would be reached at which the gate-channel diode would break down. Figure 10 shows the typical exponential variation of I_{GSS} with temperature. Static values of short-circuit input impedance are in the thousands of megohms near zero degrees centigrade.

Breakdown Voltages. For a better understanding of breakdown voltage terminology, consider the typical drain characteristics presented in Figs. 11, 12, and 13 for the 2N2497, 2N2498, and 2N2499 respectively. These are curves of drain current I_D as a function of drain-source voltage V_{DS} for the common-source configuration with gate-to-source voltage V_{GS} as a running parameter. It will be noted that the gate bias voltage is of opposite polarity to that of the drain supply voltage; hence, for ordinary bias conditions, a greater potential difference exists across the gate-drain diode than exists across the gate-source diode. This implies that gate-drain diode breakdown will occur before gate-source diode breakdown. By disconnecting the source from the drain in Fig. 9 and applying a current source of $-10\ \mu a$ to the drain, the drain-gate breakdown voltage BV_{DGO} can be determined under the conditions stated on the data sheet. The smallest voltage specified for the three types of units mentioned above is -20 volts.

Since the point at which the source is connected to the channel is physically removed from the drain connection, the source can be connected to the gate in the latter measurement without appreciably changing the value of the breakdown voltage. This connection yields BV_{DSS}, the breakdown voltage from drain to source with the gate shorted to the source. Typical values of BV_{DSS} for the three units are obvious from the break on the $V_{GS} = 0$ curves in Figs. 11, 12, and 13.

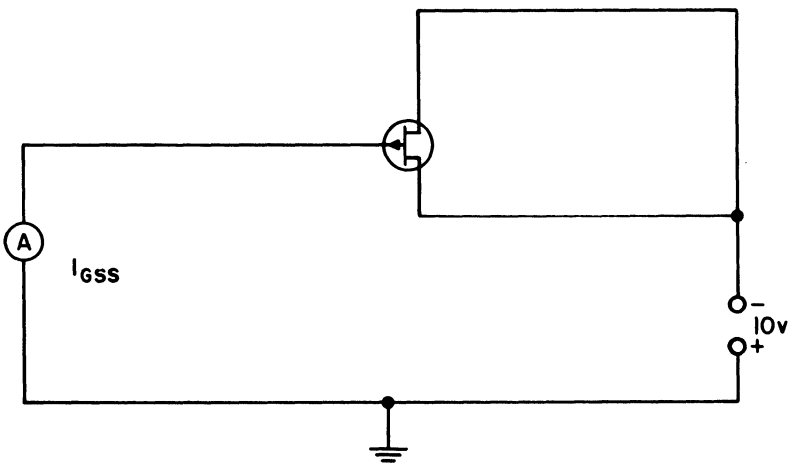


Fig. 9. Gate cutoff current test circuit.

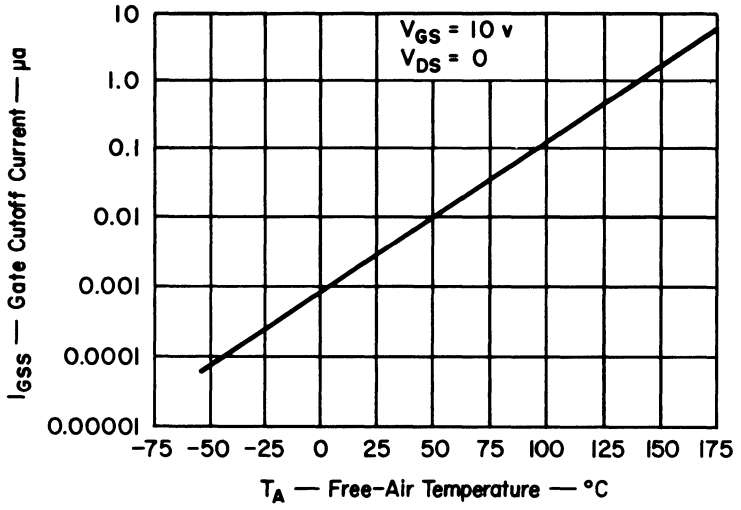


Fig. 10. Gate cutoff current vs. free-air temperature.

The break in the drain characteristic curves occurs at lower drain voltages as the gate voltage is increased; that is, the drain-gate breakdown voltage is almost constant and independent of drain-source current. Equation (7) states the relationship suggested above:

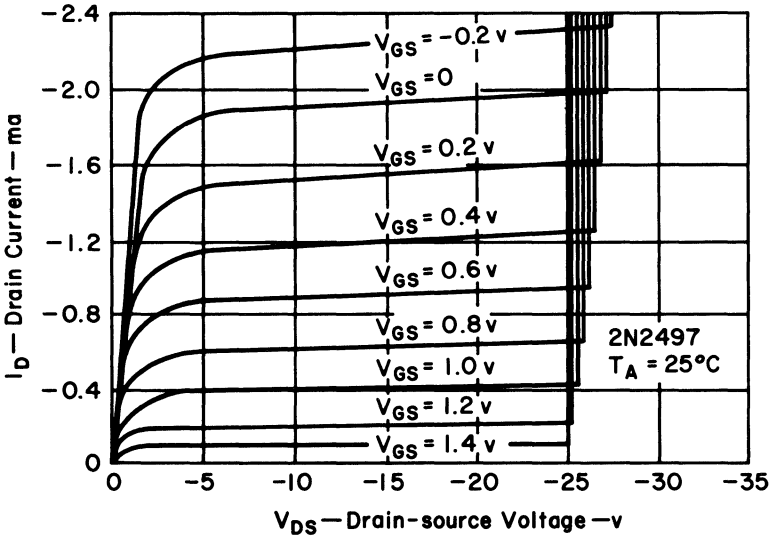


Fig. 11. Common-source drain characteristics.

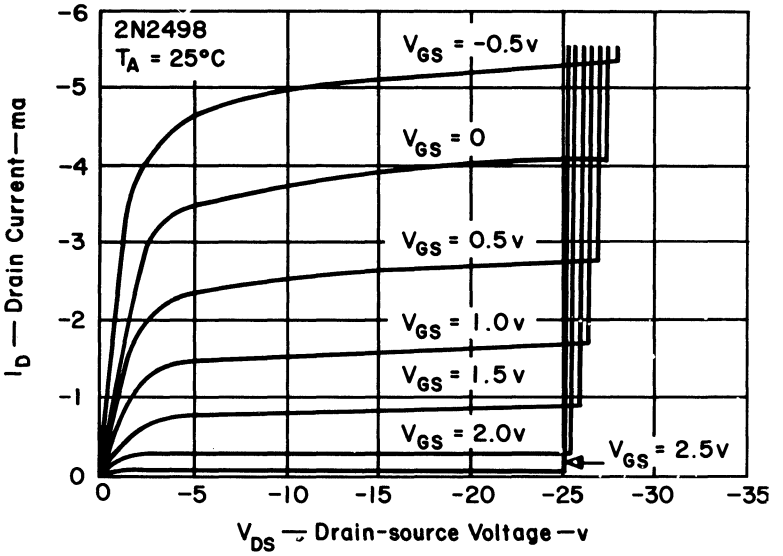


Fig. 12. Common-source drain characteristics.

$$BV_{DG} = BV_{DSX} + V_{GS} \cong \text{a constant} \tag{7}$$

where the subscript X denotes the value of BV_{DS} for a particular value of V_{GS}. Substituting BV_{DGO} for the constant, Eq. (7) becomes

$$BV_{DSX} = BV_{DGO} - V_{GS} \tag{8}$$

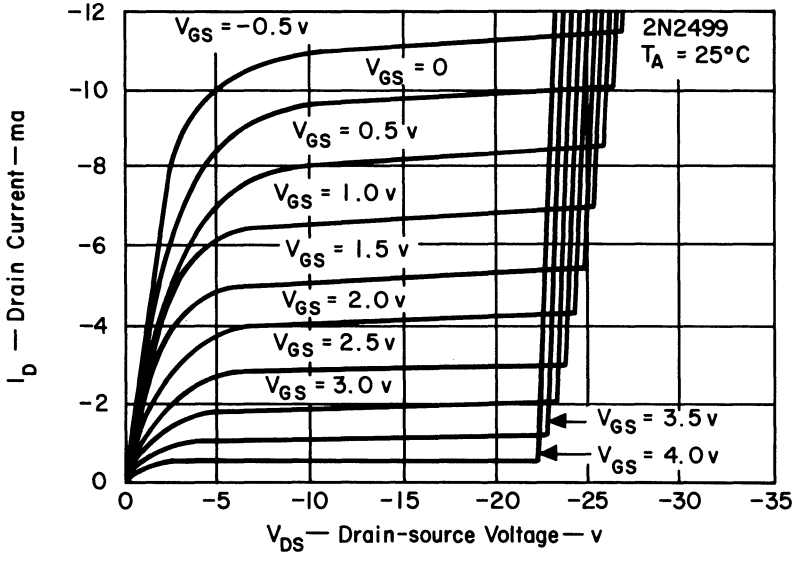


Fig. 13. Common-source drain characteristics.

Using the specified minimum BV_{DGO} and values of gate voltage, a curve can be plotted on the drain characteristic as suggested in Fig. 14. In the area to the right of this curve, breakdown is likely to occur. The useful area on the drain characteristic lies, therefore, between this curve and some characteristic curve resulting from a slight forward gate bias. Signals on the gate which cause the gate-source diode to go into forward conduction are clipped because of the sudden drop in input impedance, but the drain current is not severely affected. If the signal causes the drain-gate diode to break down, the signal is again clipped by conduction between the drain and the gate.

Saturation Drain Current $I_{D(on)}$. I_{DSS} is the IEEE standard symbol for the drain current at zero gate-to-source bias at any drain voltage (see the $V_{GS} = 0$ curve in Fig. 14). I_{DSS}, when measured at a specified drain voltage in the pinch-off or current saturation region, is called $I_{D(on)}$. If the output characteristics are relatively flat in the pinch-off region (i.e. the output impedance is very high), I_{DSS} can be approximated by $I_{D(on)}$.

The first page of the 2N2497 series data sheet is reproduced in Fig. 15 to aid this discussion. The test conditions given for $I_{D(on)}$ are $V_{DS} = 10$ and $V_{GS} = 0$. Notice that there is a 3-to-1 variation in $I_{D(on)}$ at 25°C for a given type number. $I_{D(on)}$ is strongly temperature dependent; the temperature dependence for the 2N2497 series is shown in Fig. 16. The silicon channel has a positive temperature coefficient of resistance due to decreased carrier mobility as temperature rises, but the carrier concentration at the doping levels involved remains fairly constant with temperature.[4] The total charge removed from the depletion regions depends only on the transverse electric field. Therefore, as temperature rises, it takes less current to cause sufficient voltage drop in the channel to produce pinch-off.

Pinch-off Voltage V_p. The data sheet gives a parameter $I_{D(off)}$, called the "pinch-off current," which is a measure of how much gate bias is required to reduce the drain current below a specified value. For example, the data sheet guarantees that a 2N2497 with a reverse gate bias of 5 volts will have a drain current of not

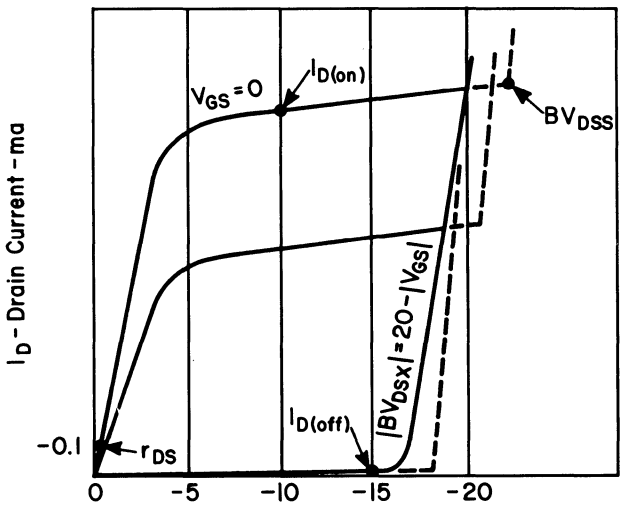


Figure 14

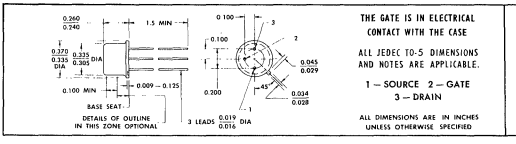
TYPES 2N2497, 2N2498, 2N2499, 2N2500
P-CHANNEL DIFFUSED PLANAR SILICON FIELD-EFFECT TRANSISTORS

TYPES 2N2497, 2N2498, 2N2499, 2N2500
BULLETIN NO. DL-S 633519, MAY 1963
REPLACES BULLETINS NO. DL-S 622727 AND DL-S 622749, JUNE 1962

FOR SMALL-SIGNAL, LOW-NOISE APPLICATIONS

- Guaranteed 10 cps Noise Figure (2N2500)
- High Input Impedance (>5 megohms at 1 kc)
- High Nuclear Radiation-Damage Resistance

***mechanical data**



***absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

Gate Current	10 ma
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	0.5 w
Total Device Dissipation at (or below) 25°C Case Temperature (See Note 2)	1.5 w
Storage Temperature Range	−195°C to +300°C

***electrical characteristics at 25°C free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	2N2497		2N2498		2N2499		2N2500		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
BV_{DGO}	Drain-Gate Breakdown Voltage (See Note 3)	$I_D = -10\ \mu a$, $I_S = 0$	−20		−20		−20		−20		v
I_{GSS}	Gate Cutoff Current	$V_{GS} = 10$ v, $V_{DS} = 0$		0.01		0.01		0.01		0.01	μa
I_{GSS}	Gate Cutoff Current	$V_{GS} = 10$ v, $V_{DS} = 0$, $T_A = 150°C$		10		10		10		10	μa
$I_{D(on)}$	Zero-Gate-Voltage Drain Current	$V_{DS} = -10$ v, $V_{GS} = 0$	−1	−3	−2	−6	−5	−15	−1	−6	ma
$I_{D(off)}$	Pinch-Off Drain Current	$V_{DS} = -15$ v, $V_{GS} =$ (See Note 4)		−10		−10		−10		−10	μa
r_{DS}	Static Drain-Source Resistance	$I_D = -100\ \mu a$, $V_{GS} = 0$		1000		800		600			ohm
$\lvert Y_{is}\rvert$	Small-Signal Common-Source Input Admittance	$V_{DS} = -10$ v, $I_D =$ (See Note 5), f = 1 kc		0.2		0.2		0.2		0.2	μmho
$\lvert Y_{fs}\rvert$	Small-Signal Common-Source Forward Transfer Admittance		1000	2000	1500	3000	2000	4000	1000	2200	μmho
$\lvert Y_{rs}\rvert$	Small-Signal Common-Source Reverse Transfer Admittance			0.1		0.1		0.1		0.1	μmho
$\lvert Y_{os}\rvert$	Small-Signal Common-Source Output Admittance			20		40		100		20	μmho
$\lvert Y_{fs}\rvert$	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = -10$ v, $I_D =$ (See Note 5), f = 10 mc	900		1350		1800		900		μmho
C_{iss}	Common-Source Short-Circuit Input Capacitance	$V_{GS} = 0$, $V_{DS} = -10$ v, f = 140 kc		32		32		32		32	pf

***operating characteristics at 25°C free-air temperature**

NF	Spot Noise Figure	$V_{DS} = -5$ v, $I_D = -1$ ma, f = 1 kc, $R_G = 1$ MΩ	3	3	4	1	db
		$V_{DS} = -5$ v, $I_D = -1$ ma, f = 10 cps, $R_G = 10$ MΩ				5	db

NOTES: 1. Derate linearly to 175°C free-air temperature at the rate of 3.3 mw/C°.
2. Derate linearly to 175°C case temperature at the rate of 10 mw/C°.
3. This parameter corresponds closely to BV_{DSS} (the Drain-Source Breakdown Voltage for $V_{GS} = 0$). BV_{DSX} (the Drain-Source Breakdown Voltage for other values of V_{GS}) may be calculated from: $|BV_{DSX}| \cong |BV_{DGO}| - |V_{GS}|$.

	2N2497	2N2498	2N2499	2N2500
NOTE 4: $V_{GS} =$	5 v	6 v	8 v	6 v
NOTE 5: $I_D =$	−1 ma	−2 ma	−5 ma	−1 ma

*Indicates JEDEC registered data.

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Figure 15

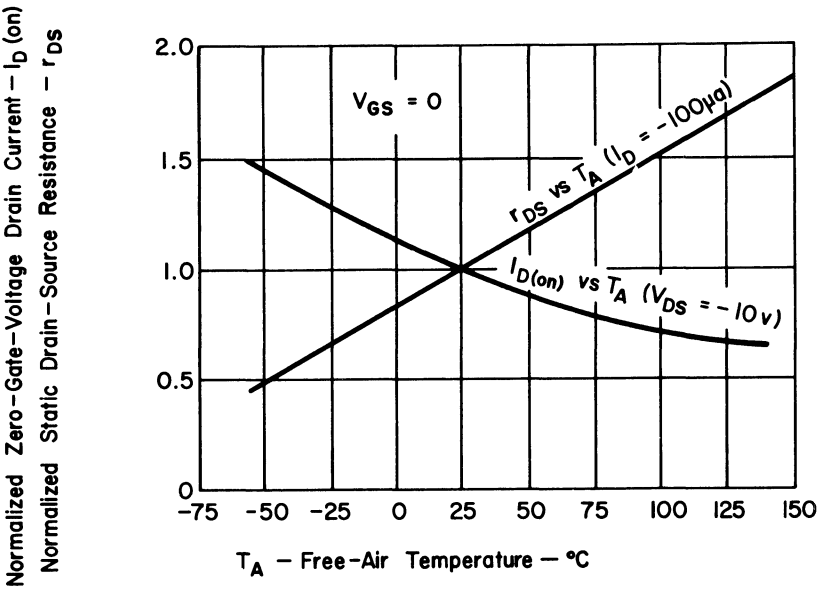


Fig. 16. Normalized zero-gain-voltage drain current and static drain-source resistance vs. free-air temperature.

more than 10 microamps. While the values of $I_{D(on)}$ and $I_{D(off)}$ give information about the transfer curves near its end points, they do not necessarily convey any useful information about the region between. And after all, this is the region in which the FET is usually operated. It is essential, then, to be able to describe the behavior of the field-effect, particularly its forward transfer characteristic, in the pinch-off region. To use a parabola for the transfer curve as described in the previous section, one must know the limits on extrapolated pinch-off voltage for each device number. Some TI data sheets do not specifically state extrapolated pinch-off voltages, but the necessary data for extracting this information are provided.

Consider the transfer curves in Fig. 17, which show parts of parabolas having as end points the maximum and minimum I_{DSS} given by the data sheet, and the maximum and minimum extrapolated pinch-off voltages, as yet undetermined. The curves are correct for P-channel devices at room temperature. The data sheet also guarantees maximum and minimum values of $|Y_{fs}|$, the small-signal forward transconductance (measured at 1 kc), which is simply dI_D/dV_{GS} when $\Delta V_{DS} = 0$. The test conditions given for $|Y_{fs}|$ show that the measurement is made at a drain current corresponding to the minimum I_{DSS} for each type, these points being intersected by the dotted line drawn from $I_{DSS(min)}$ in Fig. 17.

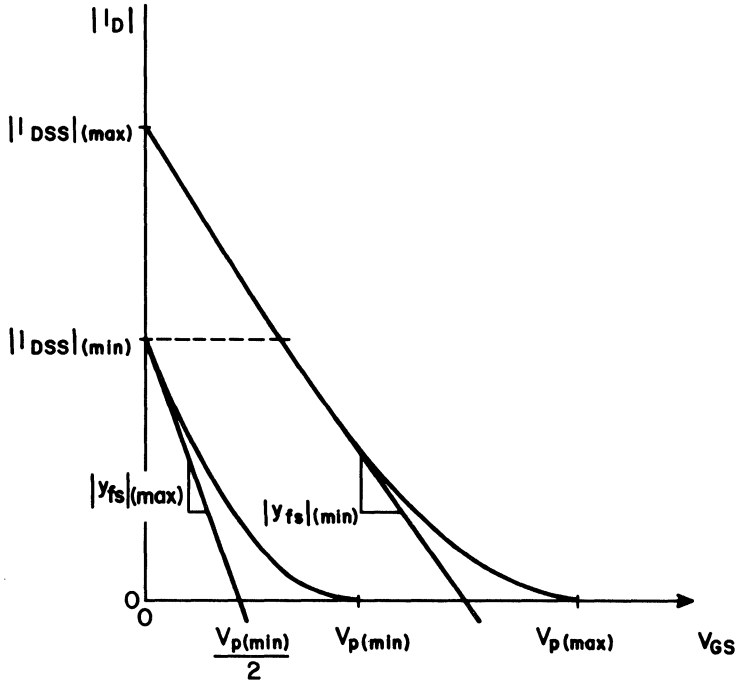


Figure 17

From Eq. (5):

$$\frac{dI_D}{dV_{GS}} = \frac{2I_{DSS}}{V_p}\left(\frac{V_{GS}}{V_p} - 1\right) = Y_{fs} \tag{9}$$

Evaluated at $I_D = I_{DSS}$:

$$\left.\frac{dI_D}{dV_{GS}}\right|_{I_D = I_{DSS}} = -\frac{2I_{DSS}}{V_p} \tag{10}$$

Equation (10) implies that the tangent drawn to the transfer curve at $I_D = I_{DSS}$ intersects the $I_D = 0$ axis at $1/2\ V_p$; this is analogous to Eq. (3) for alloy field-effects. Equation (10) can be used to determine the minimum pinch-off voltage:

$$|V_{p(min)}| = \frac{2\,|I_{DSS}|_{(min)}}{|Y_{fs}|_{(max)}} \tag{11}$$

In Fig. 18, the maximum $|Y_{fs}|$ tangent to the left-hand characteristic curve at $I_D = I_{DSS(min)}$ is shown intersecting the abscissa at $V_{GS} = 1/2\ V_{p(min)}$. To determine $V_{p(max)}$, Eq. (9) must be evaluated for the right-hand curve at $I_D = I_{DSS(min)}$. To do this, V_{GS} at this current must be found from Eq. (5):

$$\left.V_{GS}\right|_{I_D = |I_{DSS}|_{(min)}} = V_{p(max)}\left(1 - \sqrt{\frac{I_{DSS(min)}}{I_{DSS(max)}}}\right) \tag{12}$$

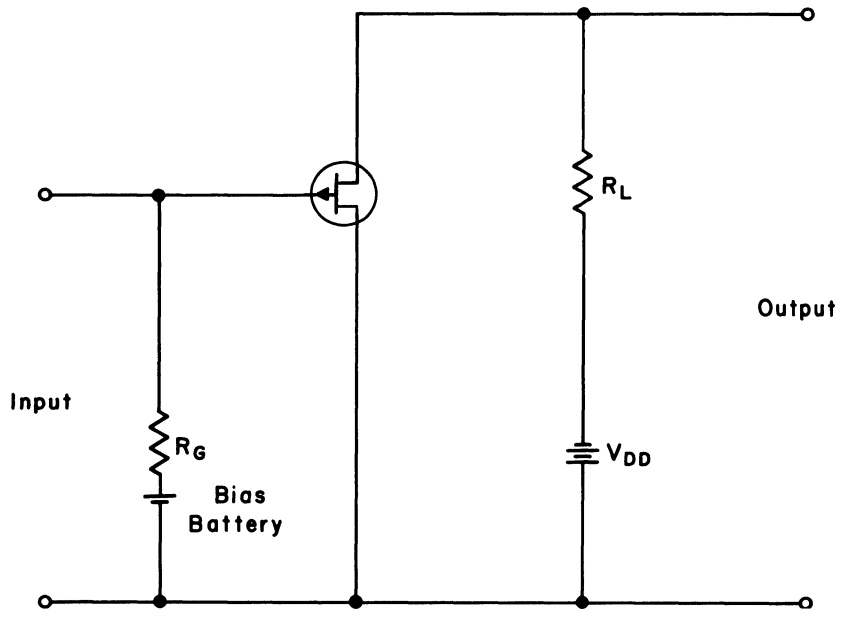


Figure 18

Substituting into Eq. (9) and solving for $|V_{p(max)}|$:

$$|V_p|_{(max)} = \frac{2\,|I_{DSS}|_{(max)}}{|Y_{fs}|_{(min)}} \sqrt{\frac{I_{DSS(min)}}{I_{DSS(max)}}} \qquad (13)$$

When these pinch-off voltages are to be evaluated from the data sheet parameters at data sheet test conditions, $I_{D(on)}$ is substituted everywhere for I_{DSS} in Eqs. (11) and (13).

BIASING FOR STABLE A-C OPERATION

The simplest method of biasing a device is to employ a fixed bias, which consists of determining from the d-c characteristics of the device what value of bias voltage or current is required to establish the desired operating conditions. This type of bias is shown in Fig. 18. Fixed bias is only useful if the temperature is going to be held nearly constant (room temperature) and if some provision is made for readjustment when the original device is replaced.

A type of bias that offers some relief from the restrictions imposed by the fixed-bias method is the self-bias method, shown in Fig. 19. With this type of biasing, the bias voltage is the drop in a resistor placed in series with the source. The drop is produced by the device's own operating current, hence the term self-bias. Since self-bias is a form of negative feedback, the operating conditions are stabilized by the device's own gain and reasonable stability is achieved for a three-to-one $I_{D(on)}$ variation if the drain current I_D is selected about half the minimum $I_{D(on)}$. Stability is usually good enough for the average small-signal stage if the temperature variation is restricted to $\pm$ 20°C, about room temperature.

But when large-temperature-range operation, or large-signal operation, or small-signal operation from a high-voltage supply, or any combination thereof is required,

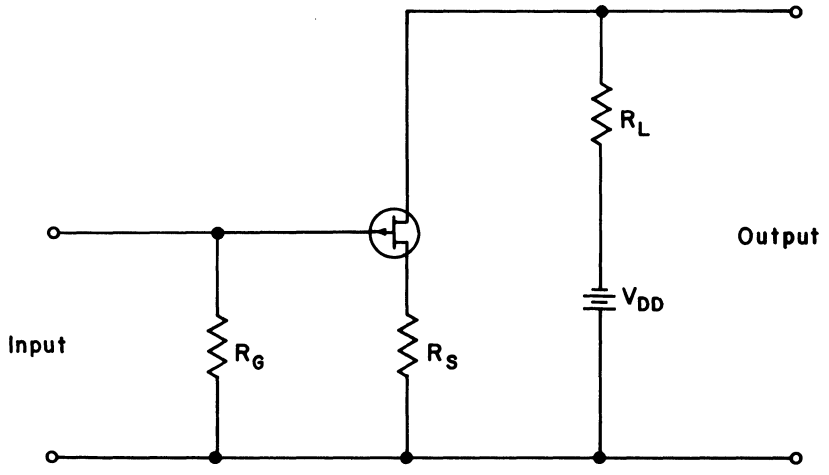


Figure 19

greater stability can be obtained from the circuit in Fig. 20. This increased stability is achieved without loss in device dynamic operating range by forward-biasing the gate and compensating by adding more source resistance, thus increasing the negative feedback. The fixed forward bias is achieved economically with the resistive divider R_1 and R_2.

By using a parabola to approximate the forward transfer characteristic of the FET, a graphical design procedure can be worked out that ensures stable operation of the circuit in Fig. 20 under "worst case" conditions arising from either environmental changes or device substitution.

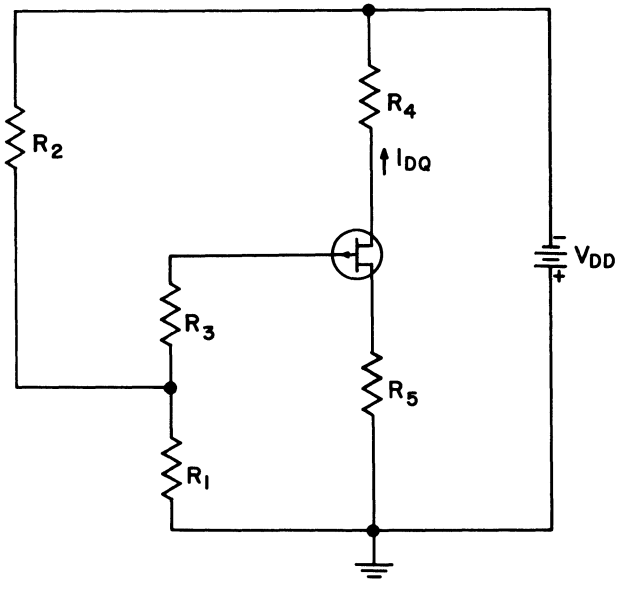


Figure 20

To determine the quiescent drain current I_{DQ} in an amplifier circuit like that in Fig. 20 it is only necessary to sum the voltage around the loop containing the gate and source terminals of the FET; the equation thus obtained will yield the operating point when it is plotted on a graph of the forward transfer characteristic. The circuit of Fig. 20 can be reduced to an equivalent circuit as in Fig. 21 by making the following substitutions:

$$R_D = R_4$$

$$R_S = R_5$$

$$R_G = R_3 + \frac{R_1 R_2}{R_1 + R_2}$$

$$V_A = V_{DD} \frac{R_1}{R_1 + R_2}$$

Writing Kirchoff's law around the gate-source loop and solving for I_D,

$$I_D = \frac{V_A + I_{GSS}(R_G + R_S) + V_{GS}}{R_S} \tag{14}$$

Figure 22 shows Eq. (14) plotted onto a typical transfer curve to locate I_{DQ}. If all devices were identical and their parameters independent of temperature, Eq. (14) would contain all the information necessary for bias design, and that would be that. But rather wide variation in parameters must be taken into account, especially where circuits are to be mass produced. Of course, this problem is not unique to FET's; it arises with all active electronic devices.

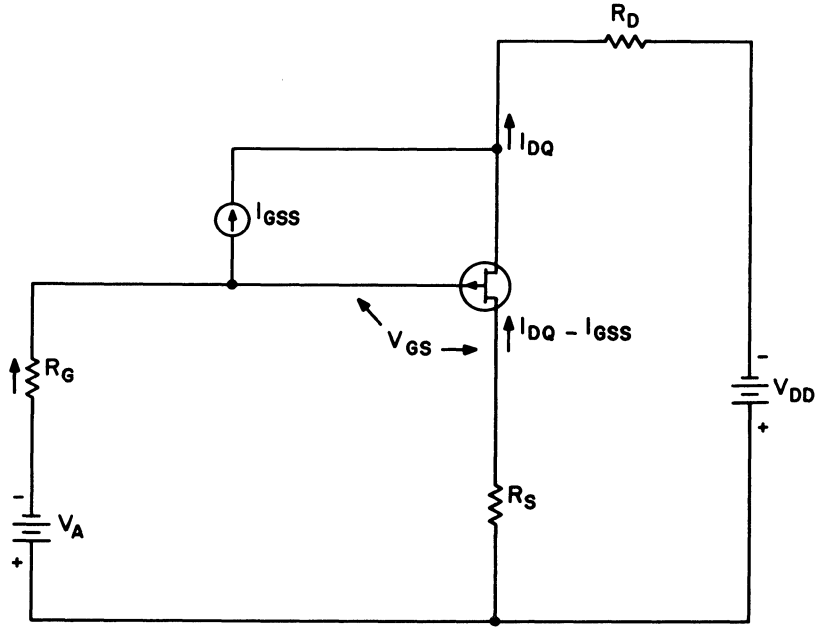


Figure 21

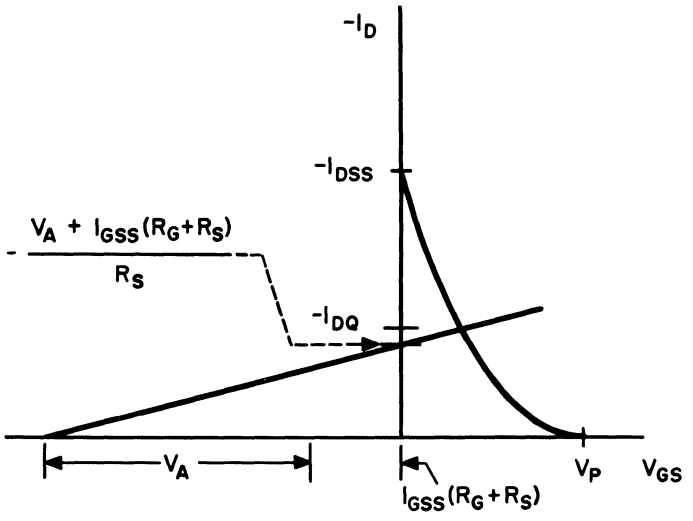


Figure 22

The effect of parameter variations on the operating point is shown by Fig. 23. These two transfer curves have the worst-case maximum and minimum values of I_{DSS} and V_p as their end points. The temperature variation of I_{DSS} must be taken into account, so that the worst-case maximum I_{DSS} would occur at the lowest ambient temperature (see Fig. 16), while the worst-case minimum occurs at the highest channel temperature. The overlines and underlines on the quantities in Fig. 23 indicate the worst-case maximum and minimum values, respectively.

From Fig. 23 and Eq. (14), the maximum I_{DQ} is:

$$|\bar{I}_{DQ}| \leq \frac{V_A + I_{GSS}(R_G + R_S) + V_{GS}}{\underline{R}_S} \tag{15}$$

The conservative minimum I_{GSS} is, of course, zero, so that the minimum value of I_{DQ} is:

$$\underline{I}_{DQ} \geq \frac{\underline{V}_A + \underline{V}_{GS}}{\bar{R}_S} \tag{16}$$

The resistor tolerances and the tolerance on V_A can be written into the equations with the following substitutions:

$$\bar{R}_S = R_S(1 + m)$$

$$\underline{R}_S = R_S(1 - n)$$

$$\bar{V}_A = V_A(1 + p)$$

$$\underline{V}_A = V_A(1 - q)$$

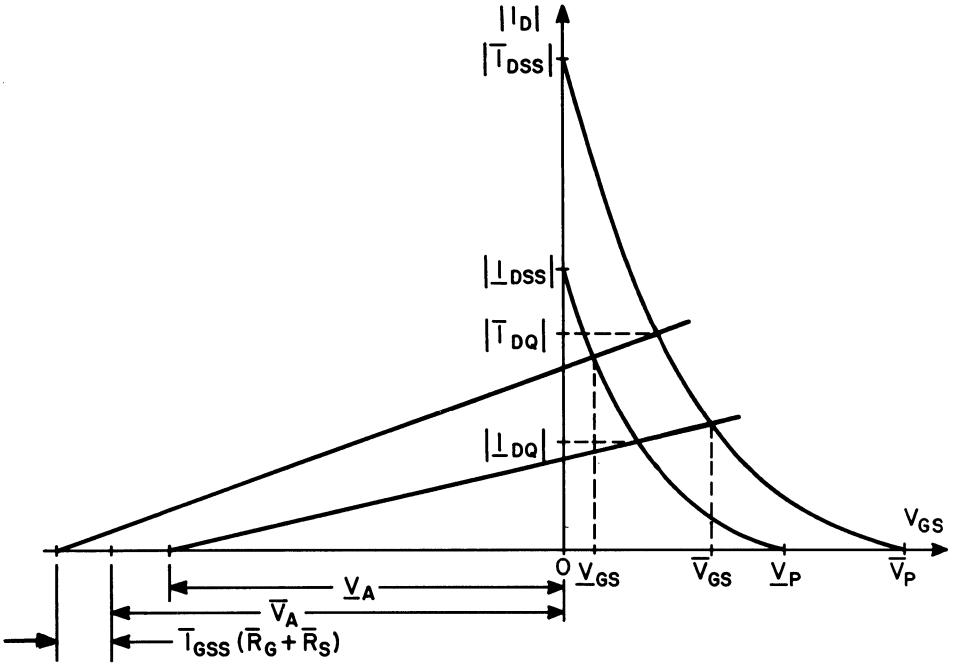


Figure 23

Combining Eq. (15) and (16) and solving for V_A:

$$V_A \geq \frac{\bar{I}_{GSS}(R_G + R_S)(1+m)^2 + \bar{V}_{GS}(1+m) - \underline{V}_{GS}K(1-n)}{(1-q)(1-n)K - (1+p)(1+m)} \qquad (17)$$

where:

$$K = \frac{\bar{I}_{DQ}}{\underline{I}_{DQ}}$$

For Eq. (17) to have any solution at all,

$$K > \frac{(1+p)(1+m)}{(1-q)(1-n)} \qquad (18)$$

This is the minimum variation to which the quiescent drain current can possibly be held with these resistor tolerances and power supply variations. How severe a limitation this is can be seen by evaluating p and q from the resistive divider (R_1 and R_2) in Fig. 20.

For $R_1 << R_2$

$$V_A(1+p) = V_{DD}(1+r)\frac{R_1(1+m)}{(R_1+R_2)(1-n)} \qquad (19)$$

$$V_A(1-q) = V_{DD}(1-r)\frac{R_1(1-n)}{(R_1+R_2)(1+m)} \qquad (20)$$

where r is the plus and minus power supply tolerance; e.g., for $V_{DD} = 28 \pm 10\%$, $r = 0.1$. Dividing Eq. (19) by Eq. (20):

$$\frac{1+p}{1-q} = \frac{1+r}{1-r}\left(\frac{1+m}{1-n}\right)^2 \tag{21}$$

And finally, substituting Eq. (21) back into Eq. (18),

$$K > \frac{1+r}{1-r}\left(\frac{1+m}{1-n}\right)^3 \tag{22}$$

This is a rather startling result. Of course, the possibility of all worst-case conditions occurring simultaneously is rather remote, but it is easy to see how the use of 10 per cent composition resistors can lead to trouble. The best (but not the most economical) solution is to use precision resistors with equal temperature coefficients, at least for R_1 and R_2.

Equation (17) demonstrated in no uncertain manner the need for the gate bias voltage, V_A. Without this external forward bias, one might as well use a potentiometer for R_S and encase the whole circuit in an oven.

The biasing problems implied by Eqs. (17) and (22) are not peculiar to field-effect transistors, but also occur with equal severity in junction transistors and to a lesser extent in vacuum tubes. Competent circuit design using any of these devices requires about the same amount of care and effort.

Equation (17) yields the value of V_A necessary to maintain the quiescent drain current within specified limits in terms of transistor parameters and resistance and supply tolerances. These limits are usually dictated by the nature of the application (or sometimes by a specification writer's whim); whether the limits are realistic or not can be checked quickly with Eq. (18). The minimum quiescent drain current can be determined if the minimum allowable output peak signal swing ($V_{pk(min)}$) is known:

$$\underline{I}_{DQ} \geq \frac{V_{pk(min)}}{R'_L} \tag{23}$$

where

$$R'_L = \frac{R_D R_L}{R_D + R_L}$$

R_L is the equivalent output load resistor and R_D is the drain load resistor in Fig. 20.

The maximum drain current I_{DQ} must not cause the FET to operate in the triode region; that is,

$$\underline{V}_{DQ} = \underline{V}_{DD} - \underline{I}_{DQ}\,(\overline{R}_D + \overline{R}_S) \text{ must not be less than } \overline{V}_p - \underline{V}_{GS} + V_{pk(min)} \tag{24}$$

On a plot of V_{DS} vs I_D characteristics, a drain-to-source voltage equal to $V_p - V_{GS}$ marks the boundary between the triode and the pinch-off region at every drain current. A conservative minimum value of V_{GS} in Eq. (24) is zero; its value at $I_D = I_{DSS}$.

Another consideration in biasing an FET is that the maximum drain-to-gate voltage must not exceed BV_{DGO}, the drain-to-gate breakdown voltage. This condition can be expressed using Fig. 21 and noting that the drain-to-gate voltage is the

sum of the drain-to-source and source-to-gate voltages:

$$\overline{V}_{DD} - \underline{I}_{DQ}(R_D + R_S)(1-n) + V_{pk(min)} - \underline{V}_{GS} \leq \underline{B}V_{DGO} \qquad (25)$$

A more useful form of this equation results from solving for $(R_D + R_S)$:

$$R_D + R_S \geq \frac{\overline{V}_{DD} - \underline{B}V_{DGO} + V_{pk(min)} - \underline{V}_{GS}}{\underline{I}_{DQ}(1-n)} \qquad (26)$$

Let us illustrate the use of this information by biasing an FET amplifier stage. An arbitrary set of conditions and requirements will be set down. These in turn will dictate the order of steps in the design procedure; the order will not necessarily remain the same under different conditions and requirements.

BIAS DESIGN EXAMPLE

1. *Conditions and requirements:*
   Supply voltage: 28 vdc ± 5%
   A-C load resistance: 10 kilohms
   Operating temperature range: −55 to + 100°C
   Minimum output signal: 1 volt rms
2. *Determination of* $\underline{I}_{DQ}$*:*

A drain load resistor can often be chosen arbitrarily, especially if (as here) no output resistance requirement is made of the amplifier. It is common practice in transistor circuitry to use a value twice the a-c load, or 20 kilohms. The equivalent a-c load resistor R_L is 6.7 ohms.

Then from Eq. (23):

$$\underline{I}_{DQ} \geq \frac{1.41\text{ v}}{6.67\text{ K}\Omega} = 0.21\text{ ma}$$

To prevent the FET from operating near cut-off, and hence in a high-distortion region when I_{DQ} approaches $\underline{I}_{DQ}$, about 50% will be added to this value. That is, $I_{DQ} = 0.3$ ma.

3. *Device selection:*

Device selection at this point is mostly an educated guess, but it must be done now to keep the procedure relatively simple. The procedure is then continued on a trial basis; if the design does not prove to be practical, another device must be selected and the procedure must be repeated, beginning with this step. The value of $\underline{I}_{DQ}$ solved for in the previous step provides some basis for device selection. It seems reasonable to expect at this point that the quiescent drain current should not have to exceed the minimum value of $I_{D(on)}$ given for the 2N2497, which we will select.

4. *Resistor selection:*

Equation (22) indicates that the use of precision resistors is in order in a "worst case" design. The temperature coefficient of resistance of TI deposited carbon resistors depends on the resistance, but for values up to 150 kilohms in the CD 1/2 MR type, a conservative value of −0.03%/C° can be used; for values from 150 kilohms to 2 megohms, −0.04%/C° is a good approximation.

R between 0 and 150 k:

$$1 + m = 1.025$$
$$1 - n = 0.975$$

R between 150 kilohms and 2 megohms:

$$1 + m = 1.03$$
$$1 - n = 0.97$$

Assuming that both resistors to be used in the voltage divider for V_A will be less than 150 kilohms:

$$1 + p = 1.12$$
$$1 - q = 0.88$$

5. *Determination of R_S:*

Having made the device and resistor selections, the next step is to find the lower limit on R_S imposed by Eq. (26). BV_{DGO} is given directly by the data sheet, while V_{GS} will be assumed to be zero.

$$R_S \geq \frac{29.4 - 20 + 1.41}{0.3(0.975)} - 20 \text{ kilohms} = 17 \text{ kilohms}$$

$R_S = 18$ kilohms will be used.

6. *Determination of $\bar{I}_{DQ}$:*

Solving Eq. (24) for $\bar{I}_{DG}$:

$$I_{DQ} < \frac{V_{DD} - \bar{V}_p - V_{pk(min)}}{(R_D + R_S)(1 + m)}$$

$\bar{V}_p$ can be evaluated using Eq. (13) and information supplied by the data sheet. For the 2N2497, $\bar{V}_p = 3.46$ volts.

$$\bar{I}_{DQ} \leq 0.55 \text{ ma}$$

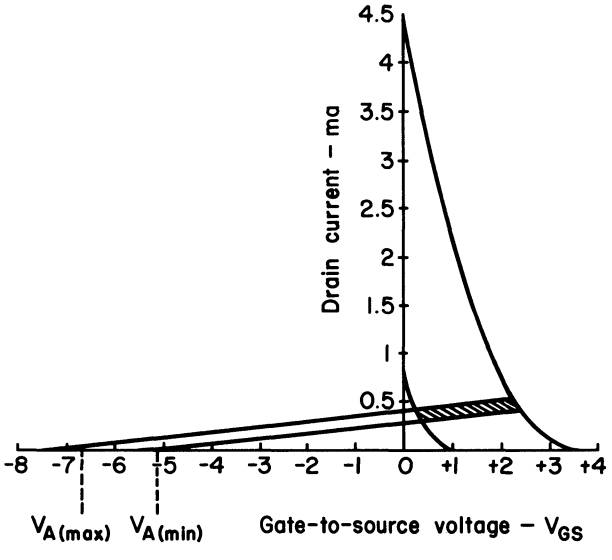


Figure 24

7. *V_A and R_G:*

In Fig. 24 two transfer curves obtained using the parabola approximation are plotted. The end points of the lower curve are V_p from Eq. (11) and $I_{D(on)}$. $I_{D(on)}$ for the 2N2497 at $V_{DS} = 10$ volts and 25°C is 1 ma; at 100°C it drops to 0.75 ma (see Fig. 18). The end points of the upper curve are $\bar{I}_{D(on)}$ and $\bar{V}_p$. $I_{D(on)}$ at −55°C is 4.5 ma. Equations (15) and (16) are plotted on these transfer curves as load lines. The slope of the upper load line is $\frac{1}{R_S(1+m)}$. The shaded area includes all possible operating points for any device type 2N2497 operating in this circuit within these ambient temperature extremes.

The intersection of the lower load line with the zero drain current axis yields the lower limit on V_A:

$$V_A \geq \frac{5.2\text{ v}}{1-q} = 5.9\text{ v}$$

The upper load line intersects the $I_D = 0$ axis at the upper limit of V_A plus the maximum allowable voltage drop across R_G and R_S due to $\bar{I}_{GSS}$:

$$V_A(1+p) + \bar{I}_{GSS}(R_G + R_S)(1+m) \leq 7.3\text{ v}$$

I_{GSS} at 100°C is 0.75 μamps. Solving for R_G:

$$R_G \leq 887 \text{ kilohms}$$

The resistance values of the completed circuit (Fig. 20) are:

R_1 – 6.49 k, CD 1/2 MR
R_2 – 24 k, CD 1/2 MR
R_3 – 820 k, CD 1/2 MR
R_4 – 20 k, CD 1/2 MR
R_5 – 18 k, CD 1/2 MR

All or part of R_5 may be bypassed with a capacitor to obtain the desired gain and low-frequency cut-off.

The value of R_G is disappointingly low; however, this is to be expected when operating temperatures much higher than room ambient are encountered. For example, if the upper operating temperature limit had been 50°C, I_{GSS} (see Figs. 19 and 24) would have been 0.05 microamps and $R_G = 13$ megohms would have worked in the circuit.

MATCHING FOR STABLE D-C OPERATION

Since FET parameters are temperature sensitive, the best way to compensate for this effect is to use them as matched pairs in the differential amplifier connection, Fig. 25.

A simple analysis of the circuit on the basis of equivalent input drift will indicate which parameters should be matched. The total equivalent input voltage drift is

$$\frac{\Delta Vin}{\Delta T} = \frac{\Delta(V_{GS1} - V_{GS2})}{\Delta T} + \frac{\Delta(I_{G1} - I_{G2})}{\Delta T}(R_G + R_S) \qquad (27)$$

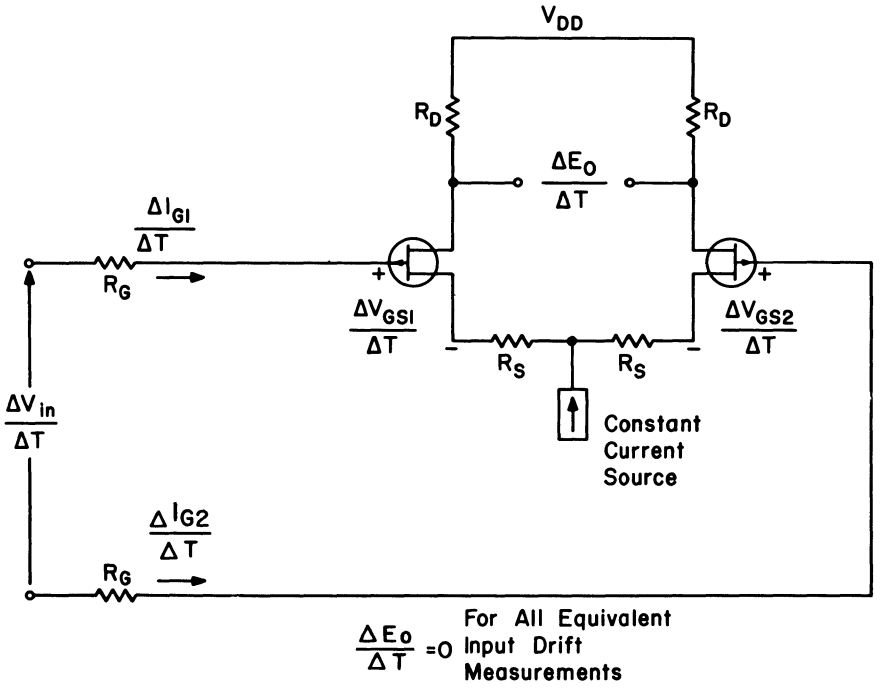


Figure 25

where $\frac{\Delta(V_{GS1}-V_{GS2})}{\Delta T}$ is the equivalent input voltage drift of the FET pair and $\frac{\Delta(I_{G1}-I_{G2})}{\Delta T}$ is the equivalent input current drift of both the circuit and the FET pair.

Thus, the equivalent input drift of the circuit will be reduced if the FET's are matched so that $\frac{\Delta(V_{GS1}-V_{GS2})}{\Delta T}$ and $\frac{\Delta(I_{G1}-I_{G2})}{\Delta T}$ are made small.

This poses the question: Which measurements or combinations of measurements will be most effective in selecting matched pairs? For the equivalent input current matching the answer is very simple since gate current is saturation current and is greatest at high temperatures. Thus, if FET's with small differences in gate current at the highest temperature needed are paired, $\frac{\Delta(I_{G1}-I_{G2})}{\Delta T}$ will be minimized. Examples of gate current vs temperature are shown in Fig. 26.

Matching of the individual equivalent input voltage drifts $\frac{\Delta V_{GS}}{\Delta T}$ may be accomplished for one drain current by holding the drain current constant, varying the temperature, and recording the change in V_{GS} for each unit.

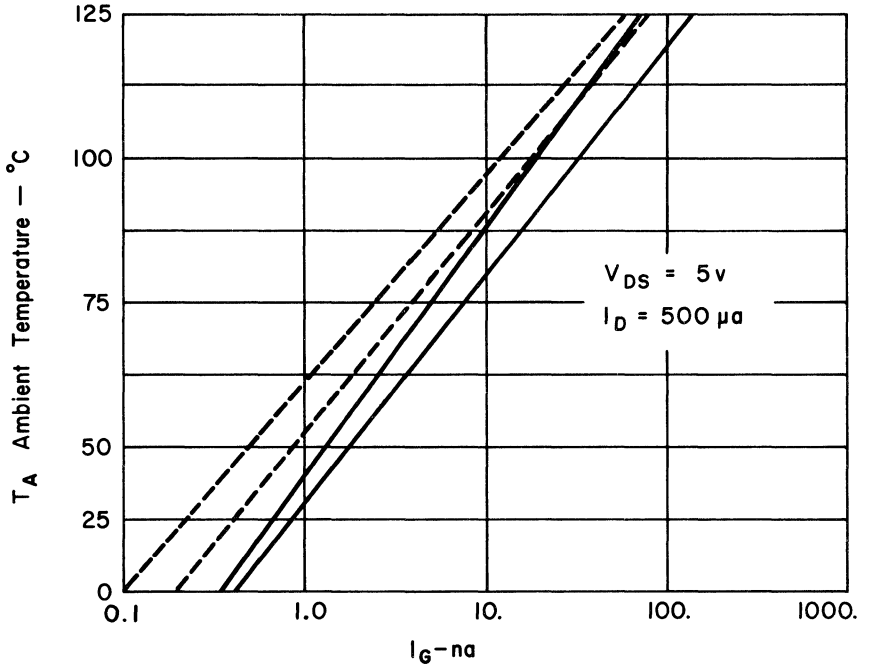


Figure 26

This method would guarantee the paired FET's to be matched at only one set of operating conditions, i.e., V_{DS} and I_D. Also, all transistors would have to be checked vs temperature; and after pairing, they would have to be checked again to accurately determine their tracking because of the inherent reading uncertainties in the individual measurements.

In view of the difficulties and shortcomings of this matching procedure, a simpler and more perfect method was sought. This better method for matching was determined from a combination of FET theory and practical measurements by the following line of reasoning: Measurement of the equivalent input voltage drift is the measurement of the change of the d-c forward transfer characteristics with temperature and referring it to the input. This then suggests that if the d-c forward transfer characteristics of a pair of FET's can be matched, the chances are good that the temperature characteristics will be matched. To do this, more must be known about the characteristics of the forward transfer curve, i.e., I_D vs V_{GS}. This additional information is of course supplied by parabolic approximation to the static transfer characteristic introduced earlier. Thus, a hypothesis can be set forth, that if $I_{D(on)}$ matches and V_{GS} at 0.1 $I_{D(on)}$ also matches, the FET will in general match and track over a range of drain currents and temperatures.*

This scheme was used to select matched pairs from a group of FET's. The differential V_{GS} vs temperature data at drain currents of 0.5 ma, 1.0 ma, and 2 ma for five pairs were taken over a $-50°C$ temperature range and are summarized in Fig. 27. One match turned out badly, but it appears possible to match to 75 mv V_{GS} difference and obtain V_{GS} tracking of less than 300 $\mu v/°C$.

*Proof of this statement is supplied in the next chapter, "The Behavior of Field-effect Transistor Characteristics with Temperature."

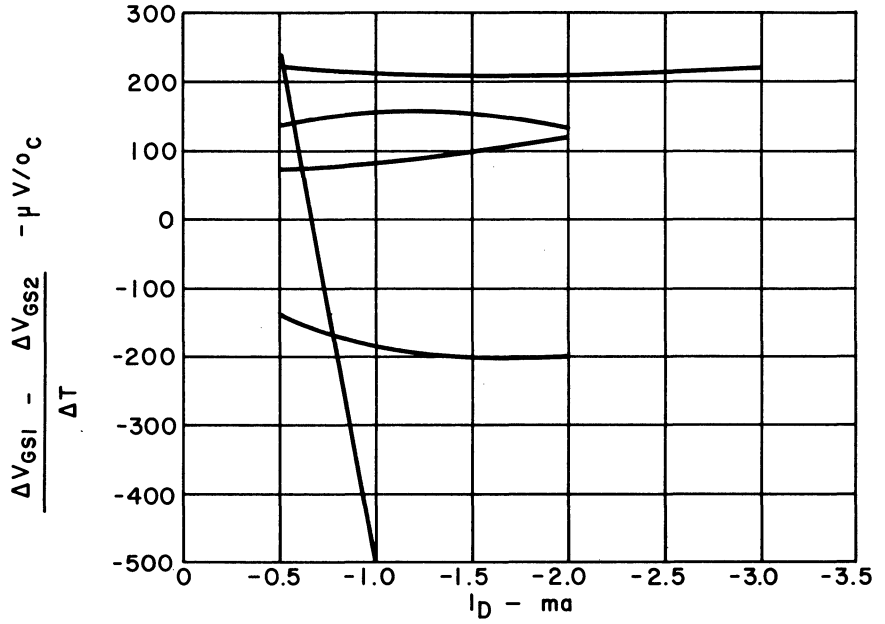


Fig. 27. Differential gate voltage tracking vs. drain current.

NOISE CHARACTERISTICS

Field-effect transistors exhibit excellent low-noise characteristics. According to Van der Ziel[5] their equivalent noise resistance is "about a factor of four better than the shot-noise resistance of a vacuum tube with comparable transconductance."

Van der Ziel lists two main sources of noise: the thermal noise of the conducting channel and the shot noise caused by the gate leakage current I_{GSS}. Figure 28 gives his noise equivalent circuit. The two voltage generators, e_s and e_d, represent the thermal noise generated in the bulk resistances, r_s and r_d, between the terminals and the active channel.

The 1/f noise break frequency is less than 100 cps, about half an order of magnitude lower than that of most transistors. Figure 29 is a graph of spot noise figure vs frequency for the 2N2497. The one-megohm generator resistance is not optimum at all frequencies. At lower frequencies the optimum generator resistance is higher; e.g., see Fig. 30. Figure 31 shows that, contrary to operation with junction transistors, noise figure is independent of operating current over a very wide range, and the change with drain-to-source voltage is slight.

APPLICATIONS

Since the outstanding low-level characteristics of field effects are high input impedance and low noise, they are naturally most useful at the input of a semiconductor circuit. Also, once the impedance level is reduced to that of conventional transistors, there is no reason to use FET's unless a high-impedance point recurs in the circuit. Further, it is interesting to note that the combination of field effects

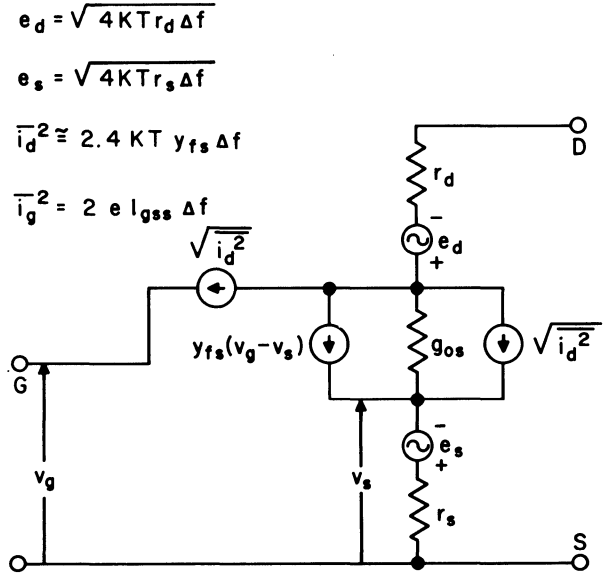


Figure 28

and conventional transistors produces more power gain than either type alone, because FET's have almost infinite current gain and transistors have very large forward transfer admittance (g_m), e.g., 0.1 mho. Accordingly, all the following applications are based upon circuit combinations with conventional transistors.

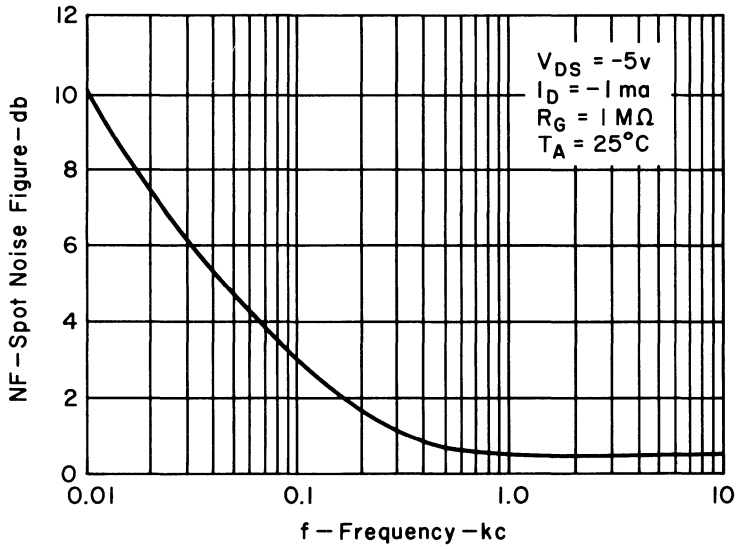


Figure 29

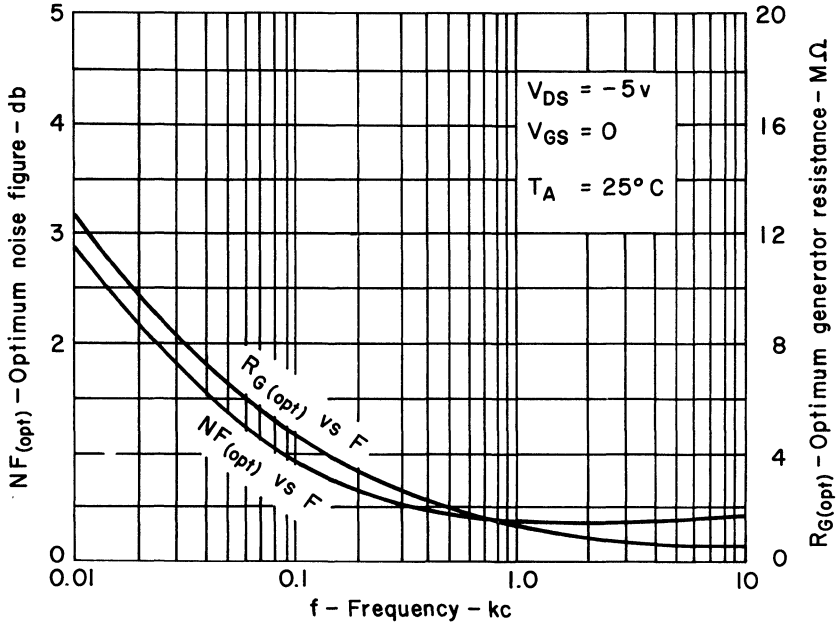


Figure 30

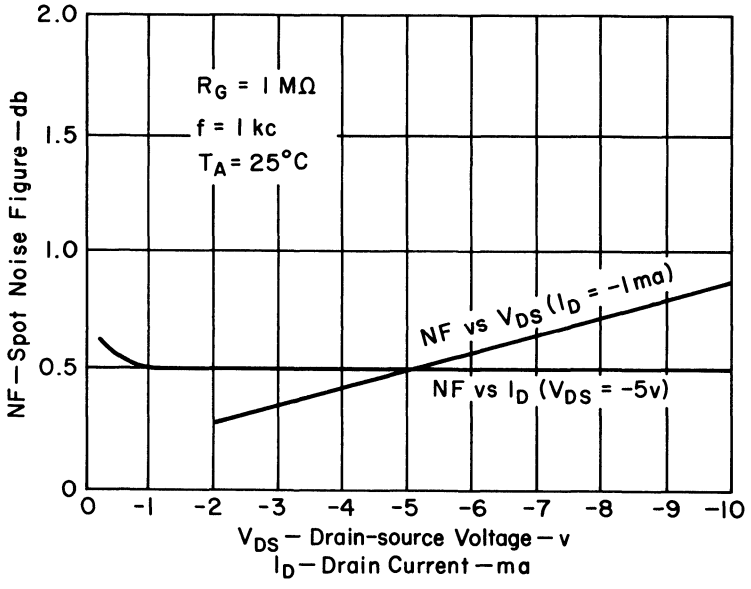


Figure 31

COMBINING CONVENTIONAL TRANSISTORS

The simple compound connection using a P-channel FET combined with a PNP transistor in Fig. 32a is equivalent to the Darlington connection. This circuit is simple and straightforward and nothing more need be said of it. The use of the circuit in Fig. 32b is somewhat obscure and requires explanation. As it stands, the source is connected to the collector so that signals applied to the gate will appear at the collector without phase inversion and near unity gain, depending upon the μ of the field effect. Thus, the connection is a simple feedback amplifier. Use has been made of this feedback in a 6-db low-noise transducer amplifier (Fig. 33) for use with very high-input-impedance low-frequency transducers. The input impedance and spot noise figure at 0.01, 0.1, 1.0, and 10 kc are shown in the accompanying table. The broad-band noise figures from 10 cycles to 10 kc with a 200-kilohm generator resistance is 1.7 db.

A simple electronic d-c millivoltmeter, Fig. 34, shows application of this compound circuit to a high-impedance low-drift d-c amplifier. The differential amplifier is made up of a pair of the simple feedback amplifiers with an approximate voltage gain of three. The field effect's operating conditions are 10 volts V_{DS} and 1 ma I_D. These conditions were selected to give a forward transconductance of 1000 to 1500 micromhos and an output impedance greater than 50 kilohms. A PNP transistor constant-current source is used to improve operating-condition stability for FET's with $I_{D(on)}$'s ranging from 1 ma to 6 ma, and to improve the common-mode rejection ratio. The circuit, when used as a d-c millivoltmeter, has an input sensitivity of 20 megohms per volt with a common-mode rejection ratio of 1000 to 1. When matched FET's are selected by the method previously discussed,

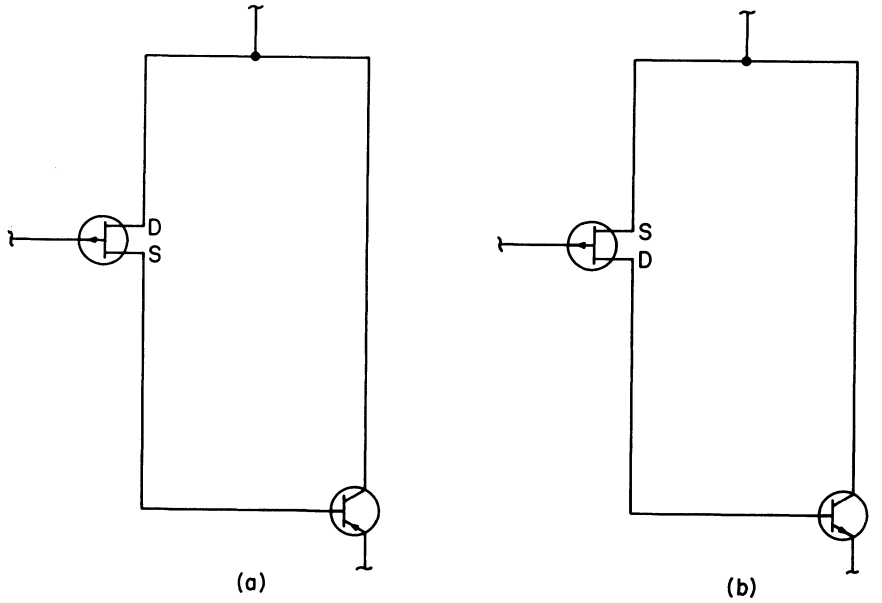
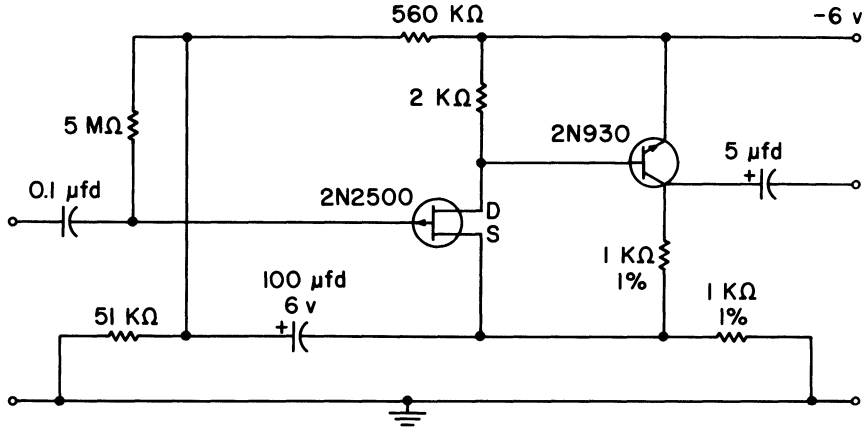


Fig. 32. Compound connection.



Freq. (kc)	Zin (MΩ)
0.01	180
0.1	180
1.0	27
5.0	14
10.0	3

Freq. (kc)	R_g (MΩ)	Spot Noise Figure (db)
0.01	20.0	7.0
0.1	2.0	3.0
1.0	0.2	1.5
10.0	00.02	1.2

Figure 33

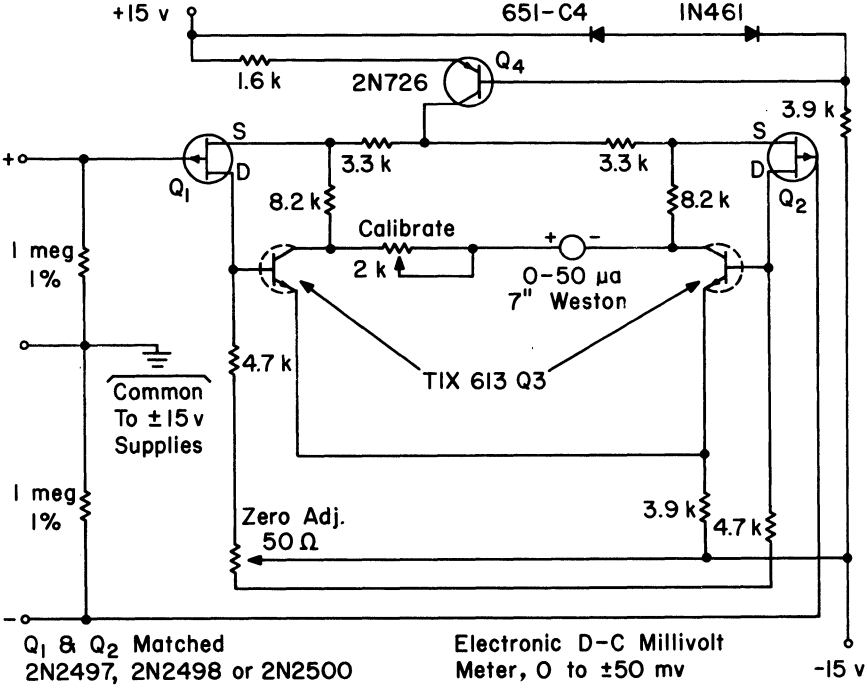


Figure 34

reasonably good temperature characteristics can be expected even from 20-megohm gate resistors if the gate current is well matched and below 0.5 na at room temperature.

A combination of an FET and a conventional transistor to give the highest possible input impedance is the bootstrapped source follower, Fig. 35. The drain as well as the gate divider are bootstrapped in phase with the source. The primary purpose is to reduce the FET's input capacitance to a minimum so that the real part of the input impedance is all that is seen at high frequencies. Application of this combination is shown in a unity-gain high-input-impedance wideband preamplifier, Fig. 36. In this circuit, the single transistor of the preceding figure is replaced by a two-stage feedback amplifier, and the source bias resistor is replaced by a common-base current source. The typical low-frequency input impedance is approximately 100 megohms. Frequency response for various values of generator resistance is shown in Fig. 37.

A second application of the bootstrapped source follower is shown in a unity-gain temperature-stable d-c amplifier, shown in Fig. 38. Here, two of the circuits of Fig. 35 are combined to form a differential input stage where one gate serves as the feedback input and the other as the signal input. Note that driven shields are placed around the signal input FET and resistors to further reduce input capacitance. A current source is used to bias the FET's so that the circuit can accommodate a 2- to 6-ma $I_{D(on)}$ range. For good temperature stability, Q_1 and Q_2 are matched. The gain accuracy is maintained at better than 2 per cent within the band pass. The input impedance at very low frequencies is limited to 42 megohms

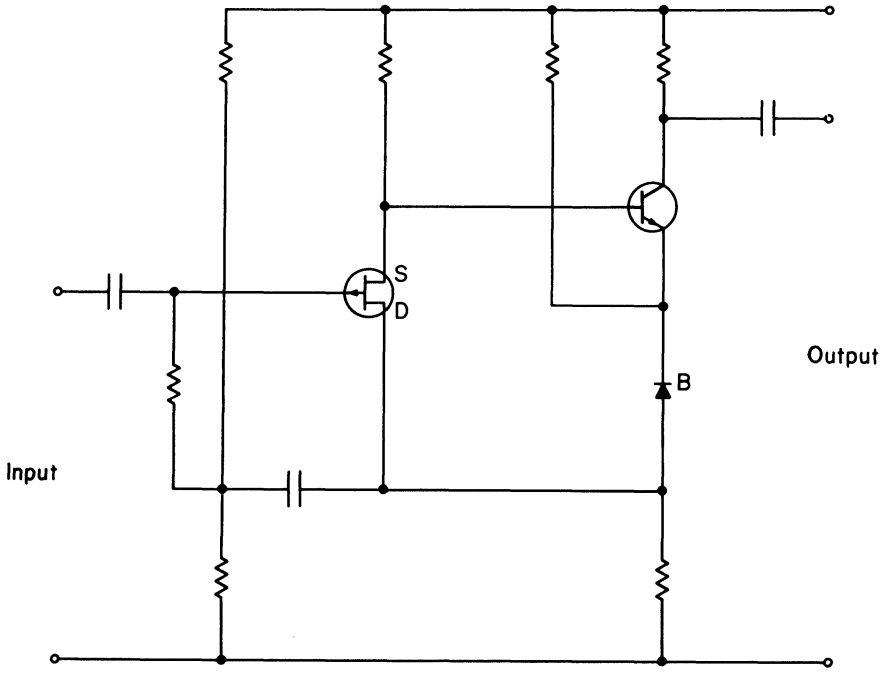


Figure 35

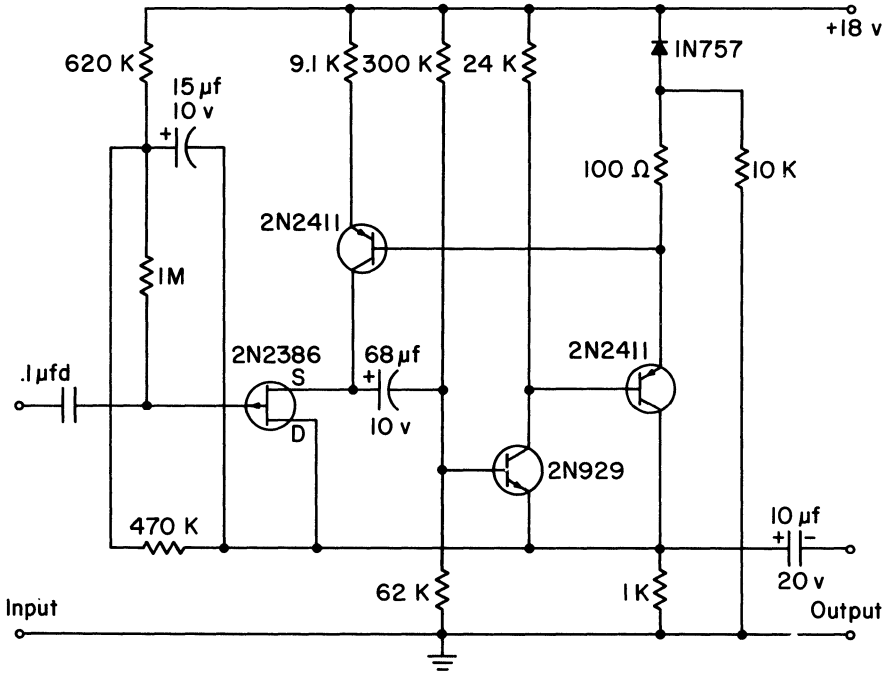


Figure 36

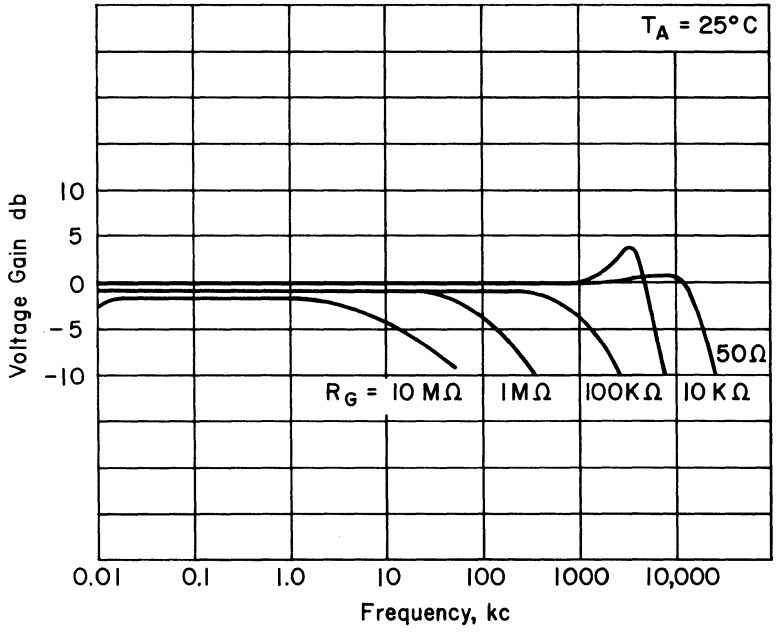
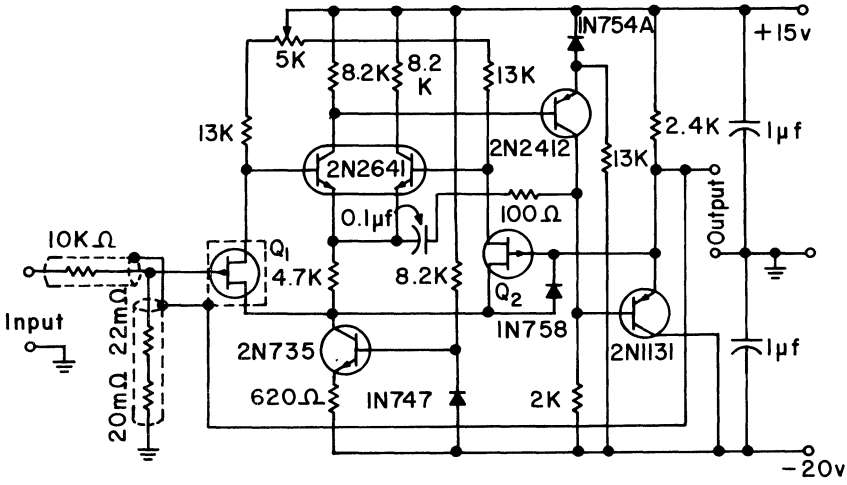


Fig. 37. Amplifier voltage gain vs. frequency.



Notes: (1) Input shields are the outer conductors of RG-114/u.
(2) Q_1 and Q_2 are Field Effect Transistors matched for $I_{D(on)}$ between 2 and 6 ma, V_{PO} <6v, and I_{GSS} <10na: all with 10%.

Figure 38

by the two resistors connecting the gate of the input field-effect transistor to ground. These resistors can be removed if the generator impedance provides a d-c return to ground. The input impedance will then be greater than a thousand megohms at several cycles per second.

Figure 39 contains response curves for generator resistance of 51 ohms, 33 kilohms, 100 kilohms, and 1 megohm.

Reasonably high input impedance is obtained by the direct-coupled cascode circuit, Fig. 40, but its outstanding characteristic is that the combination can be used as a single stage, having low reverse transfer and high output impedance. The low reverse transfer gives rise to a high input impedance, and its high output impedance makes possible a very large voltage gain.

An application that shows both these characteristics is the simple unity-gain high input impedance d-c amplifier, Fig. 41. Feedback is accomplished by connecting the source to the output so that for the condition of zero output for zero input voltage, the FET must operate at $I_{D(on)}$ where the output impedance of the FET alone is lowest and hence the μ is low. Feedback theory requires that the μ of the input stage be large to give this type of amplifier good gain accuracy. Thus, by using this cascode stage to replace the FET, this difficulty is corrected. At the same time, reverse transfer between drain and gate is minimized so that the input capacitance is not increased by the Miller effect; this makes possible high input impedance at high frequency. Figure 42 shows the upper cut-off frequencies for various generator resistances.

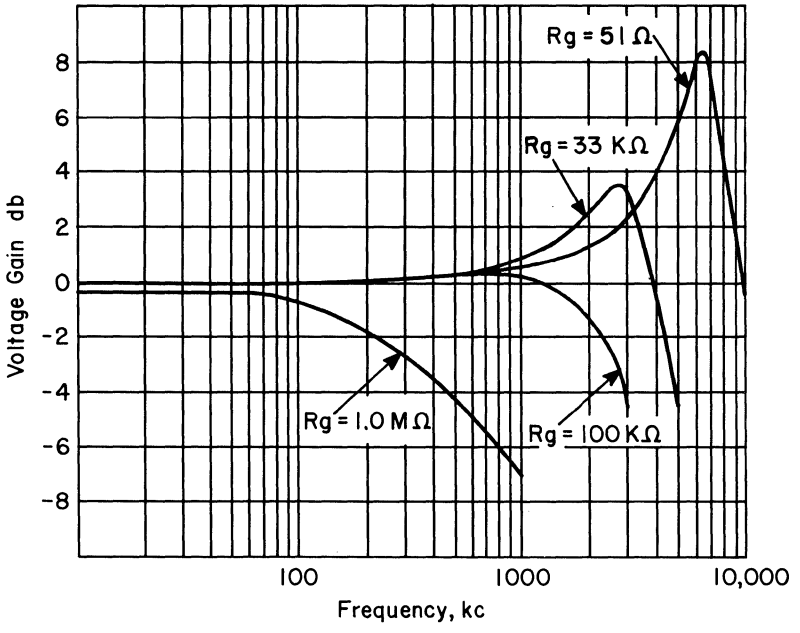


Figure 39

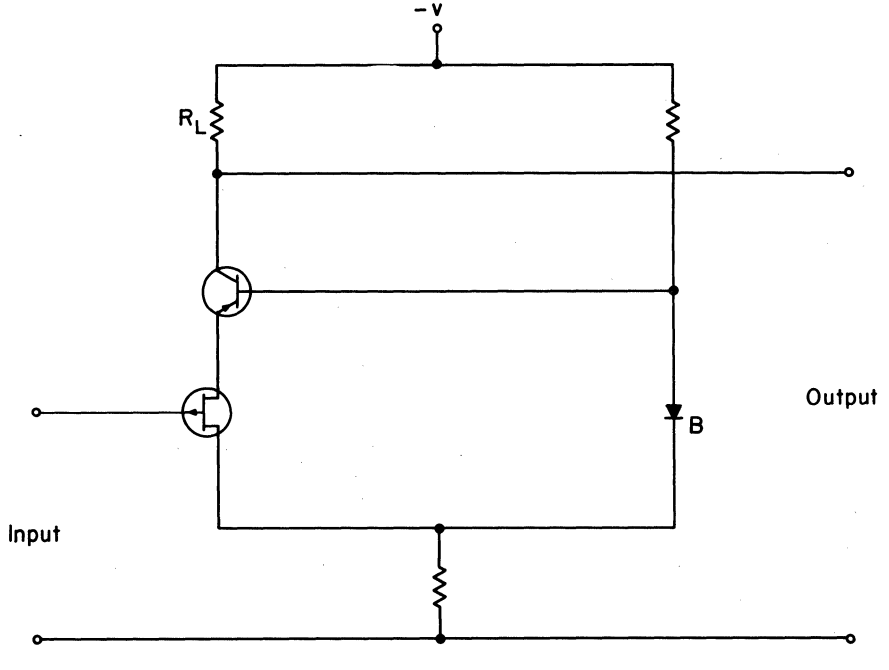


Fig. 40. Direct-coupled cascode circuit.

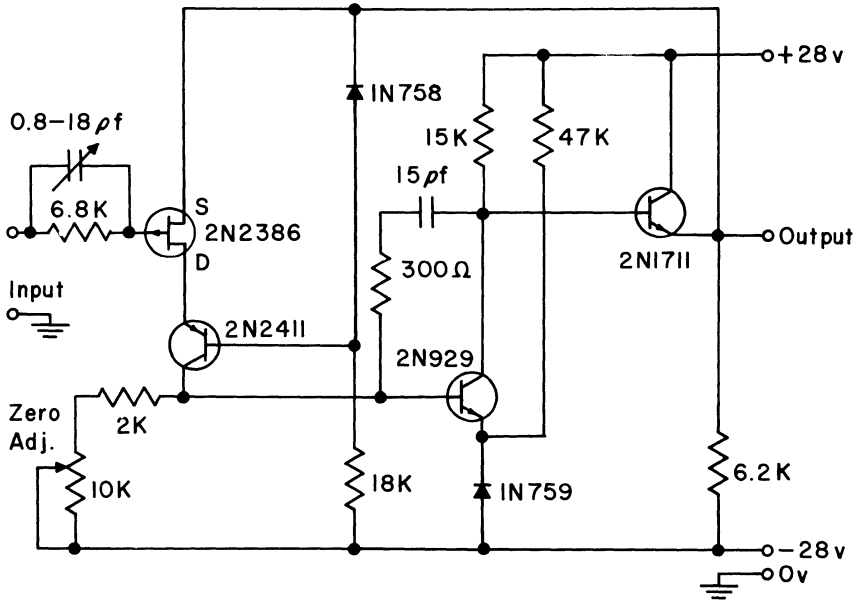


Figure 41

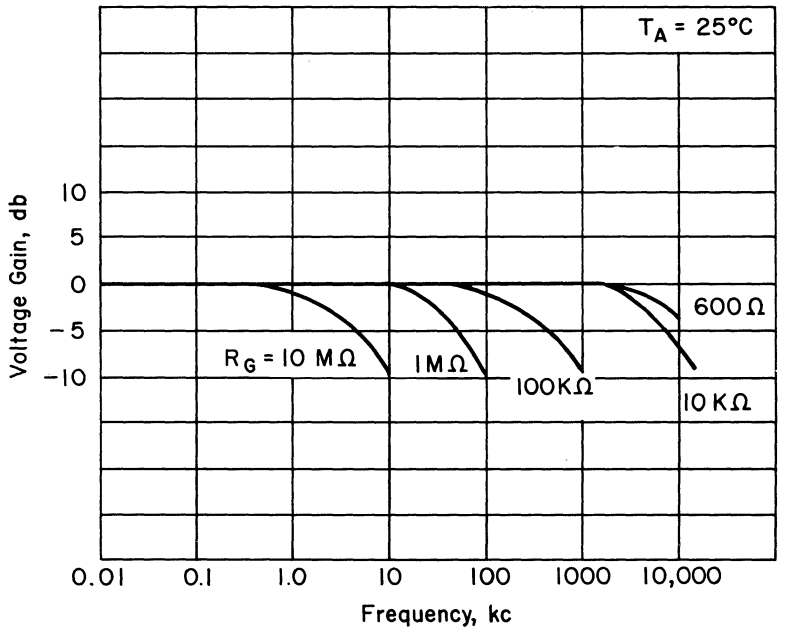
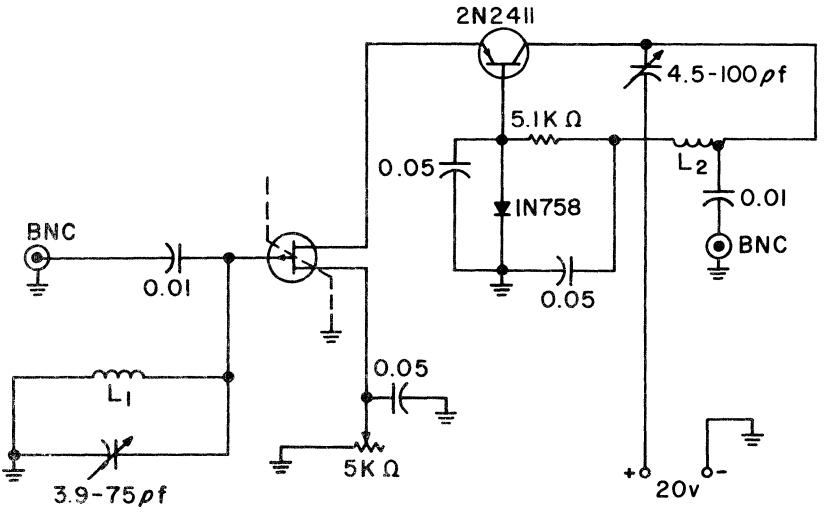


Fig. 42. Amplifier voltage gain vs. frequency.



L_1, L_2 18 turns B&W 3004 Minductor; L_2 tapped 1 3/4 turns from ground.

Figure 43

The low reverse transfer of the cascode connection makes possible stable operation of a common-source FET at 10 mc in a tuned amplifier without neutralization. The tuned amplifier in Fig. 43 has measured transducer gains of 20.6 db and 25.3 db for the 2N2497 and 2N2499 respectively. The gain measurements were made for a generator resistance of 3.3 kilohms because it is very near optimum for low-noise performance as shown in Fig. 44. Note that the optimum noise figure at 10 mc is 3 db; at present, this is too large to consider FET's as low-noise devices

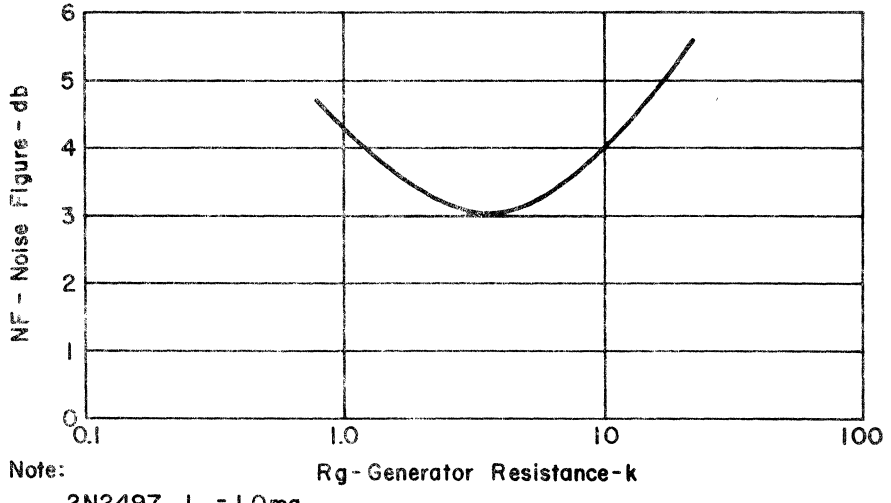


Fig. 44. Silicon P-channel field-effect transistors compound connection.

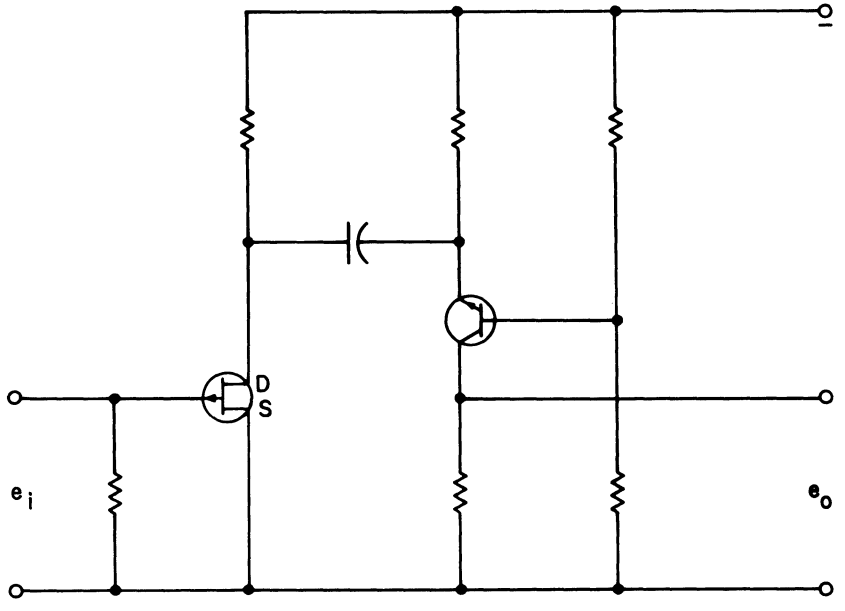


Figure 45

at radio frequencies.

The a-c coupled cascode connection, Fig. 45, has similar advantages and is uniquely suited to increasing the bandwidth of a low-noise amplifier by reducing Miller effect and permitting independent adjustment of the devices' operating conditions for optimum noise performance. In the 40-db low-noise high-input-impedance amplifier, Fig. 46, a 2N2498 is operated at 1-ma drain current while

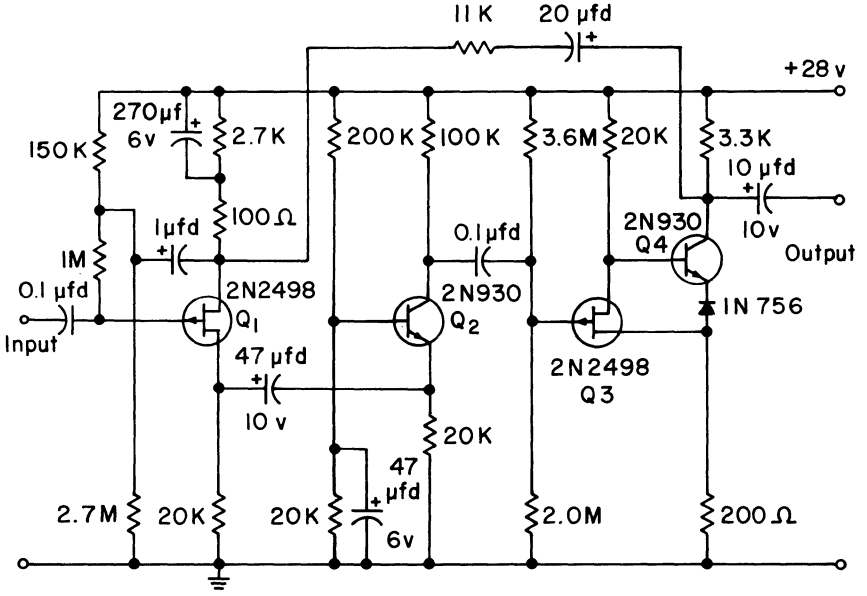


Figure 46

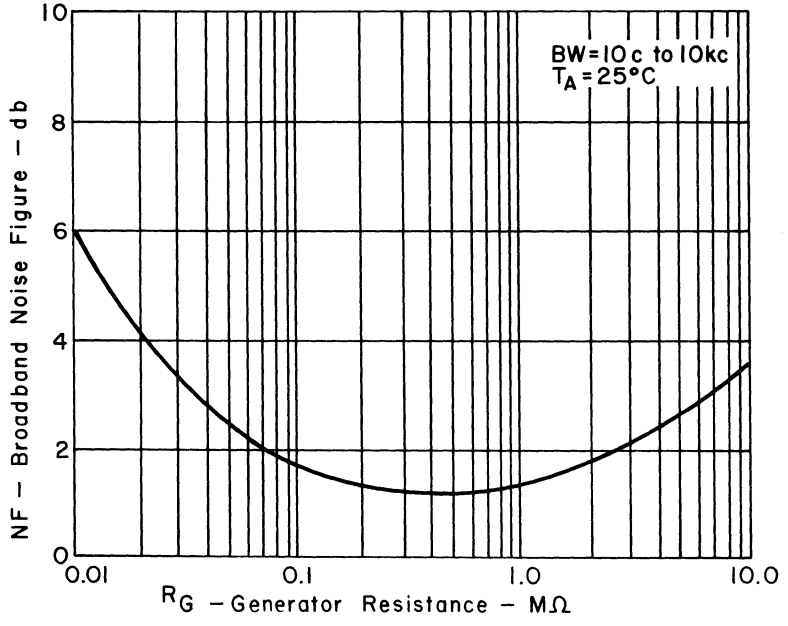


Fig. 47. Amplifier broadband noise figure vs. generator resistance.

a 2N930 is operated at 100-μa collector current. Both operating currents are optimum for the respective devices. Since the optimum generator for common-base operation is the same as for common-emitter operation, the 20-kilohm drain resistor in parallel with the 20-kilohm emitter resistor provides the 10-kilohm

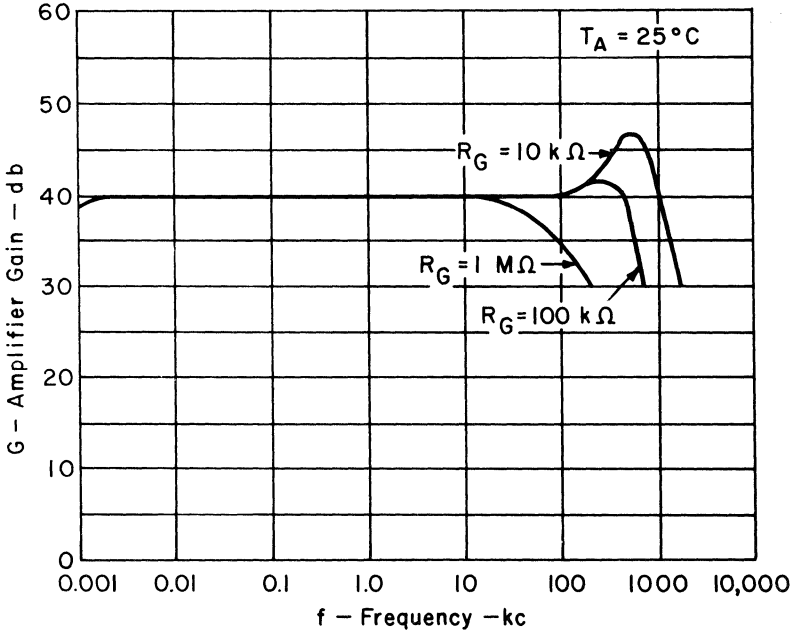


Fig. 48. Amplifier gain vs. frequency

optimum generator for the 2N390. The broadband noise figure vs generator resistance, Fig. 47, shows that the noise figure is less than 3 db over a generator resistance range of 50 kilohms to 5 megohms. The amplifier's response for generator resistances from 10 kilohms to 1 megohm is shown in Fig. 48.

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8

Dependence of Field-effect Transistor Characteristics on Temperature

by L. J. Sevin

INTRODUCTION

The wide variation of the drain characteristics of field-effect transistors with temperature has been a serious problem in some applications, notably in d-c amplifiers. Some manufacturers' data sheets show graphs of the various FET electrical characteristics versus temperature, particularly those of the gate leakage currents I_{GSS} (not applicable to induced-channel FET's), the zero-bias drain current I_{DSS} (again not applicable to the I/C FET), the transconductance y_{fs} (or g_m), and the triode-region zero-bias channel resistance $r_{D(ON)}$. The temperature dependence of I_{GSS} is quite well understood, being the thermal saturation current of a reverse-biased P-N junction. The same can be said for g_m (with minor reservations to be explained later) and $r_{D(ON)}$: conductance varies directly and resistance inversely, with carrier mobility.

The temperature variation of I_{DSS} is another matter. Individual FET's may deviate alarmingly from the published typical behavior. For example, the TI 2N2497 data sheet shows that I_{DSS} has a negative temperature coefficient about equal to that expected of the mobility of P-type silicon (the 2N2497 is a P-channel transistor), but individual units have been found that exhibit positive temperature coefficients of I_{DSS}. Some FET's have even been found whose I_{DSS} is independent of temperature! Such loss of predictability tends to have a demoralizing influence on already harassed circuit designers.

The apparent conflict is resolved when the effect of temperatures on the barrier contact potential is taken into account. Then predictability returns, and order is restored.

THE SQUARE-LAW BEHAVIOR OF FET'S

Integrated-circuit FET's and certain P-N junction FET's exhibit very nearly a "square-law" dependence of the transfer characteristic[1,2]; the relationship describing P-N FET's is:

$$I_D = I_{DSS}\left(\frac{V_{GS}}{V_p} - 1\right)^2 \tag{1}$$

where, by implication, V_p is the V_{GS} necessary to reduce the drain current to zero, I_D and V_{GS} are defined in Fig. 1. The effects of gate leakage current are not included in Eq. (1) and will not be considered in this discussion. V_p is related to the junction contact potential ϕ by:

$$V_p = V_{pi} - \phi \tag{2}$$

where V_{pi} is the internal voltage necessary to deplete the channel. This term is temperature independent, at least in the temperature range under consideration (250 to 400°K), since the strong electric field in the depletion region will ensure that all the donor atoms (in the P-channel) are ionized, eliminating any carrier "freeze out" as temperature lowers. The temperature dependence of V_p is determined by ϕ alone:

$$\frac{dV_p}{dT} = \frac{-d\phi}{dT} \tag{3}$$

According to Shockley[3], I_{DSS} is proportional to the square of the channel charge density and the first power of mobility, while V_p and V_{pi} are proportional to the first power of channel charge density:

$$I_{DSS} \propto \mu p^2 \tag{4a}$$

$$V_p, V_{pi} \propto p \tag{4b}$$

Since I_{DSS} is defined for $V_{GS} = 0$, then in order to cause I_{DSS} to flow it is necessary to deplete only that part of the channel not already depleted by ϕ. Therefore, I_{DSS} is proportional to V_p^2, not V_{pi}^2, or:

$$I_{DSS} = B\mu V_p^2 \tag{5}$$

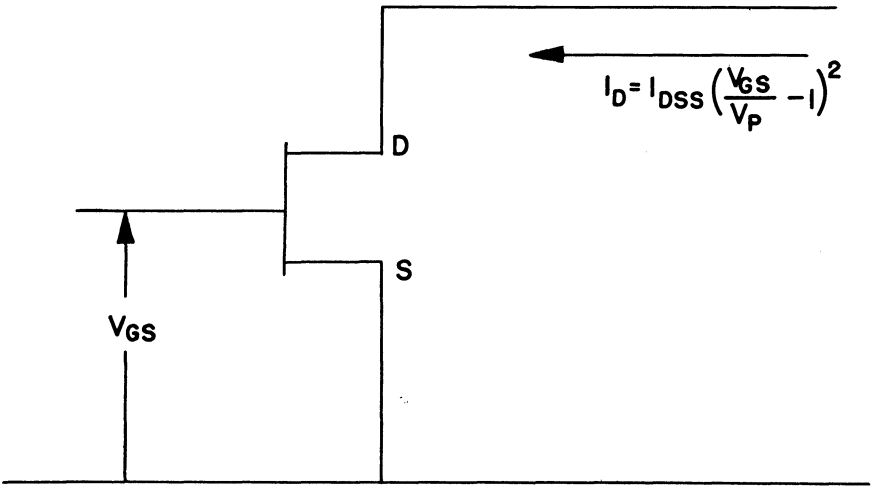

Fig. 1. A simple model.

where B encompasses the dielectric and geometry constants. Thus, there are two temperature-dependent factors in I_{DSS}, μ and V_p. For I_{DSS} to be capable of having either negative or positive temperature coefficients, the temperature dependencies of μ and V_p must be compensating, as in fact and in deed they are.

MOBILITY AND CONTACT POTENTIAL

Drift mobility exhibits an inverse power law behavior with temperature:

$$\mu = \mu_o \left(\frac{T}{T_o}\right)^{-n} \tag{6}$$

where μ_o is measured at T_o. Prince's data[4] shows that n = 2.3 for holes in silicon, and n = 1.5 for electrons in silicon.

The contact potential as a function of temperature[5] is:

$$\phi = \frac{KT}{q} \ln \left(\frac{N_a N_d}{n_i^2}\right) \tag{7}$$

where: K = Boltzmann's constant, $8.616 \times 10^{-5} \frac{eV}{K^\circ}$

q = electronic charge, 1.6019×10^{-19} coulomb
N_a = acceptor density on the P side of the junction, cm^{-3}
N_d = donor density on the N side, cm^{-3}
n_i^2 = the PN product

Now:
$$n_i^2 = 4U^2T^3 e^{\frac{-E_G}{KT}} \tag{8}$$

where: U = a constant, 2.42×10^{-15} cm^{-3} $(K^\circ)^{-3/2}$
E_G = gap energy, about 1.1 ev at room temperature for silicon

Substituting Eq. (8) back into Eq. (7):

$$\phi = \frac{KT}{q}\left[\ln\left(\frac{N_a N_d}{4U^2}\right) - 3\ln T\right] + \frac{E_G}{q} \tag{9}$$

Differentiating with respect to temperature:

$$\frac{d\phi}{dT} = -3\frac{K}{q}\left[1 + \ln T - \frac{1}{3}\ln\left(\frac{N_a N_d}{4U^2}\right)\right] + \frac{1}{q}\frac{dE_G}{dT} \tag{10}$$

dE_G/dT for silicon is nearly constant above 200°K and has an approximate value of -0.28×10^{-3} ev/K° (Ref. 6). Note that $d\phi/dT$ is not a strong function of donor and acceptor densities nor of the absolute temperature, but varies as the natural logarithm of both quantities. Furthermore at the donor and acceptor densities presently used in FET's — about 2×10^{16} (or higher) for the gate impurity (N_d or N_a) and 10^{15} for the channel impurity — the term $1/3 \ln \left(\frac{N_a N_d}{4U^2}\right)$ in Eq. (10) will be small compared to 1 + ln T. An approximate value of $d\phi/dT$ under this condition at T = 300°K is −2.0 mv/K°. Then from Eq. (3), dV_p/dT is positive, and a log function of the absolute temperature; from this it is readily seen that temperature effects of mobility and contact potential on I_{DSS} oppose each other.

THE FORWARD TRANSFER CHARACTERISTICS OF FET'S VS TEMPERATURE

Figure 2 is a graph of the transfer characteristic of a P-channel FET, with centigrade temperature as the running parameter. I_{DO} and V_{po} are reference temperature values of I_{DSS} and V_p where 25°C is the reference temperature (T_o). The temperature coefficient of I_{DSS} is negative and that of V_p is positive; it is therefore to be expected that the I_D vs V_{GS} curves at two different temperatures should cross at some point. This expectation is fulfilled by the existence of the point Q in Fig. 2. What does not necessarily follow, however, is that the curves at three different temperatures should cross at the same point, as they apparently do in Fig. 2. The type of behavior shown in Fig. 2 is typical of most P-channel devices, but Figs. 3 and 4 show two seemingly anomalous devices; neither has a cross-over point, and one (Fig. 3) has a negative coefficient of I_{DSS} while the other (Fig. 4) has a positive coefficient.

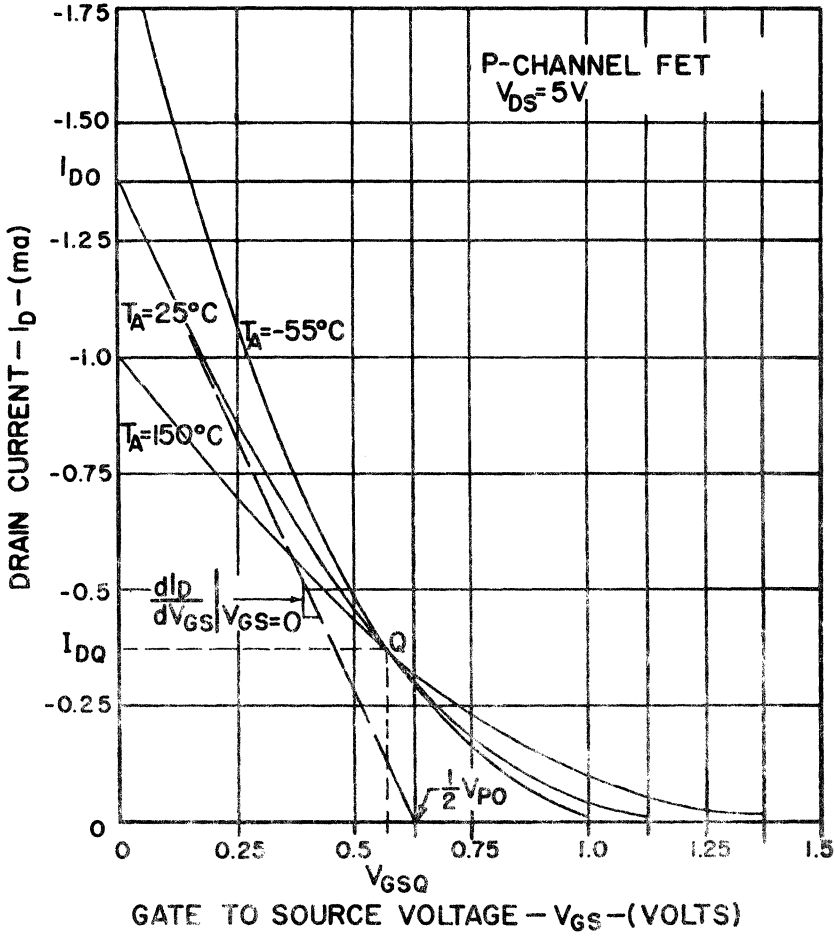

Fig. 2. Transfer characteristics with zero crossing.

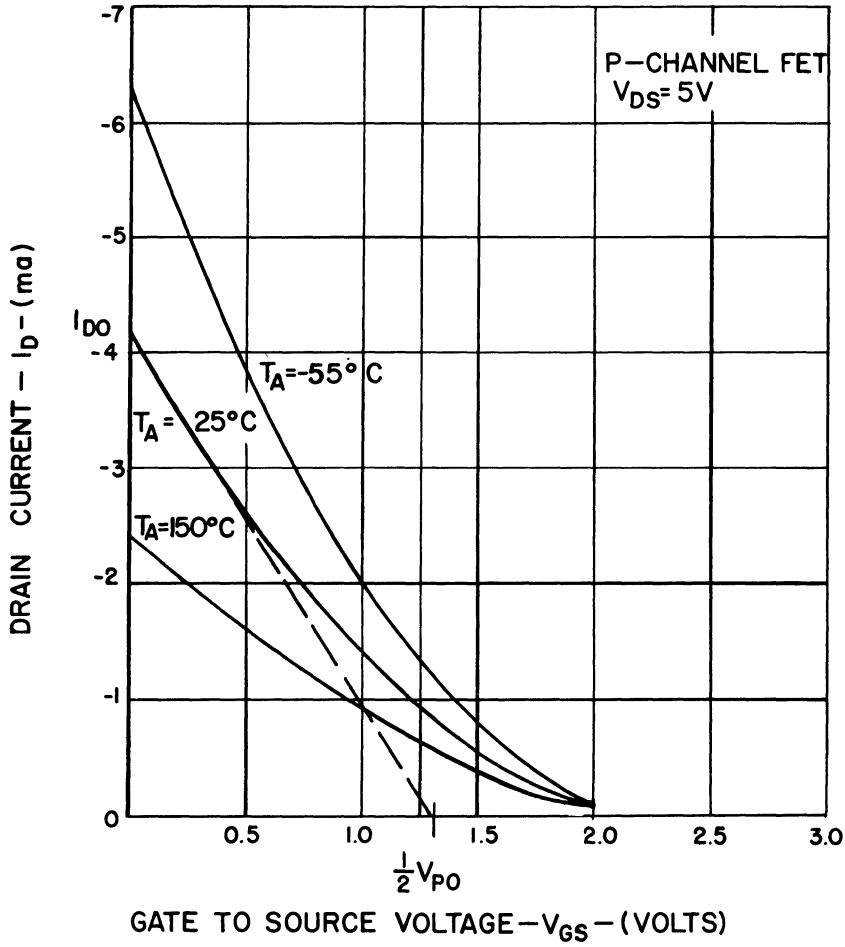

Fig. 3. Transfer characteristic with negative coefficient.

Some clue to the reasons for this behavior can be obtained by noting that the pinch-off voltage (at $T_A = T_o = 25°C$) of the device with a cross-over point (Fig. 2) lies between the pinch-off voltages of the other two devices. Admittedly, the above observation has no justification on the basis of the small sample presented, but Figs. 2, 3, and 4 are used only as an illustrative example. The observation is based on data from a much larger sample (24 devices) and at more than three temperatures, but all the data cannot be presented here for obvious reasons. The method of obtaining the pinch-off voltage from the three graphs is suggested by the square-law approximation. The tangent drawn to the transfer curves at $V_{GS} = 0$ represents the transconductance (dI_D/dV_{GS}) evaluated at $V_{GS} = 0$. By differentiating Eq. (1) with respect to V_{GS} and setting $V_{GS} = 0$, it is clear that

$$g_m = g_{max} = \frac{2\, I_{DSS}}{V_p} \tag{11}$$

This implies that the tangent drawn at $V_{GS} = 0$ will intersect the V_{GS} axis at $V_{GS} = V_p/2$.

In Fig. 2 a bias point, Q, exists where the d-c drain current and d-c gate voltage appear to be independent of temperature. It is a simple matter to derive this bias point by differentiating Eq. (1) with respect to temperature and setting the derivative equal to zero. Proceeding in this manner:

$$\frac{dI_D}{dT} = \left(\frac{V_{GS}}{V_p} - 1\right)\left[\frac{dI_{DSS}}{dT}\left(\frac{V_{GS}}{V_p} - 1\right) - 2\frac{I_{DSS}}{V_p^2}\right] \tag{12}$$

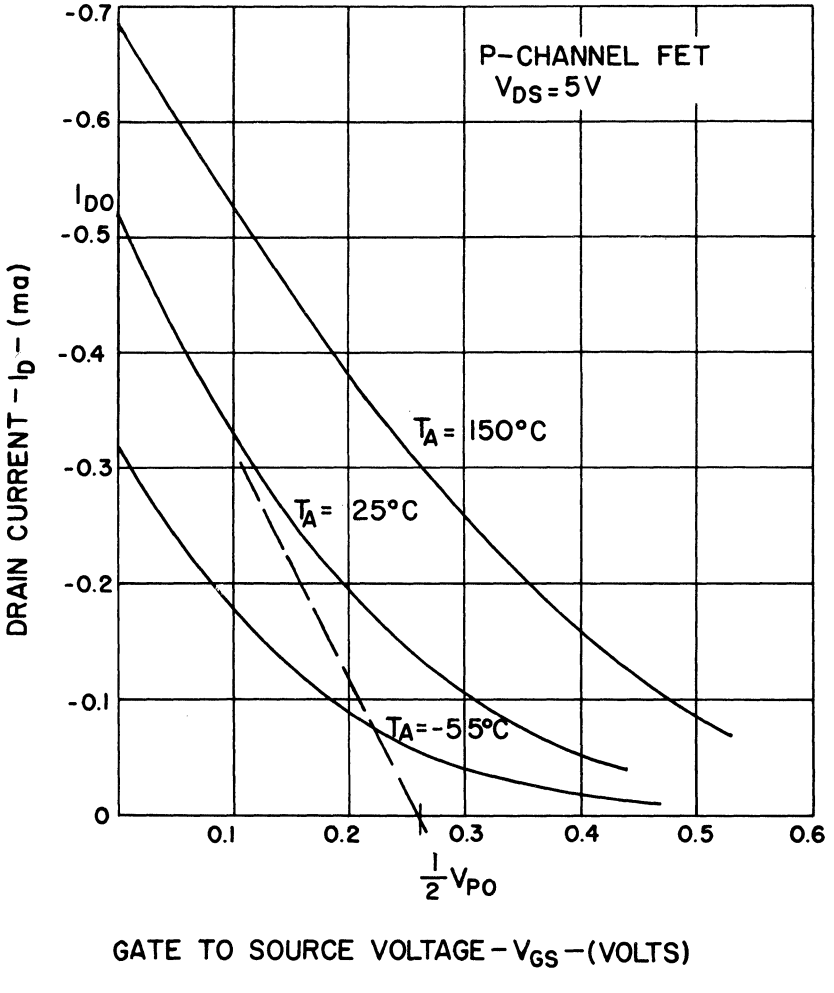

Fig. 4. Transfer characteristic with positive coefficient.

Setting Eq. (12) equal to zero, we find that

$$\frac{V_{GSQ}}{V_p} = \frac{\dfrac{dI_{DSS}}{dT}}{\dfrac{dI_{DSS}}{dT} - 2\dfrac{I_{DSS}}{V_p}\dfrac{dV_p}{dT}} \tag{13}$$

V_{GSQ} is the bias voltage from gate to source, where the temperature coefficient of the uniquely determined drain bias point current, I_{DQ}, is zero; in Eq. (13) the bias point is expressed as a fraction of the pinch-off voltage. It is generally more convenient to work with the drain current rather than the gate voltage, since good circuit practice dictates biasing with constant currents rather than with constant voltages. By subtracting one from both sides of Eq. (13) and solving for $(V_{GSQ}/V_p - 1)$ in Eq. (1) we get:

$$-\sqrt{\frac{I_{DQ}}{I_{DSS}}} = \frac{2\dfrac{I_{DSS}}{V_p}\dfrac{dV_p}{dT}}{\dfrac{dI_{DSS}}{dT} - 2\dfrac{I_{DSS}}{V_p}\dfrac{dV_p}{dT}} \tag{14}$$

The minus sign is used with the radical in Eq. (14) because the plus sign yields the wrong half of the parabola; remember that Eq. (1) is a parabola with its vertex at V_p, and it is double-valued over the I_D axis. This is a snare one must always be wary of when using Eq. (1).

From Eqs. (5) and (6):

$$I_{DSS} = B\,\mu_o \left(\frac{T}{T_o}\right)^{-n} V_p^2 \tag{15}$$

then,

$$\frac{dI_{DSS}}{dT} = B\mu_o \left(\frac{T}{T_o}\right)^{-n} V_p \left(\frac{2dV_p}{dT} - \frac{n}{T}V_p\right) \tag{16}$$

Substituting Eqs. (3), (15), and (16) into Eq. (14) and squaring both sides:

$$\frac{I_{DQ}}{I_{DSS}} = \frac{4T^2}{n^2 V_p^2}\left(\frac{d\phi}{dT}\right)^2 \tag{17}$$

Now both I_{DSS} and V_p are functions of temperature; when referenced to T_o, they become I_{DO} and V_{po} respectively. That is:

$$I_{DSS} = I_{DO}\left(\frac{T}{T_o}\right)^{-n}\left[1 - \frac{\Delta\phi}{\phi_o \Delta T}(T - T_o)\right]^2 \tag{18}$$

where:

$$\left[1 - \frac{\Delta\phi}{\phi_o \Delta T}(T - T_o)\right]^2 = \left(\frac{V_p}{V_{po}}\right)^2 \tag{19}$$

Substituting Eq. (10), (18), and (19) into Eq. (17), we have finally:

$$\frac{I_{DQ}}{I_{DO}} = \frac{4T_o{}^n T^{2-n}}{n^2 V_{po}{}^2}\left[\frac{3K}{q}(1 + \ln T) + 0.28 \times 10^{-3}\right]^2 \tag{20}$$

Equation (20) is the bias point, expressed as a fraction of I_{DO}, which is the reference temperature value of I_{DSS}, where the rate of change of gate bias voltage is zero. Note that Eq. (20) is a function of temperature, but only weakly so. When I_{DQ}/I_{DO} is equal to one, the rate of change of I_{DSS} with temperature is zero, or in other words, the cross-over point is at or near $I_D = I_{DSS}$ and $V_{GS} = 0$. For P-channel FET's, using $n = 2.3$, the cross-over point will be at $I_D = I_{DSS}$ at $T = 25°C$ (298°K) on any FET having a pinch-off voltage of 0.53 volts. Equation (20) is plotted and compared to experimental data in Fig. 5. The discrepancy can be explained if it is assumed that the value of n is 2 and not 2.3. Figure 6 shows I_{DSS} vs temperature for three devices with pinch-off voltages greater than 1.5 volts, where, according to the experimental data in Fig. 5, the mobility effects should dominate I_{DSS}. The drain voltage for these measurements was 0.5 volts, so that

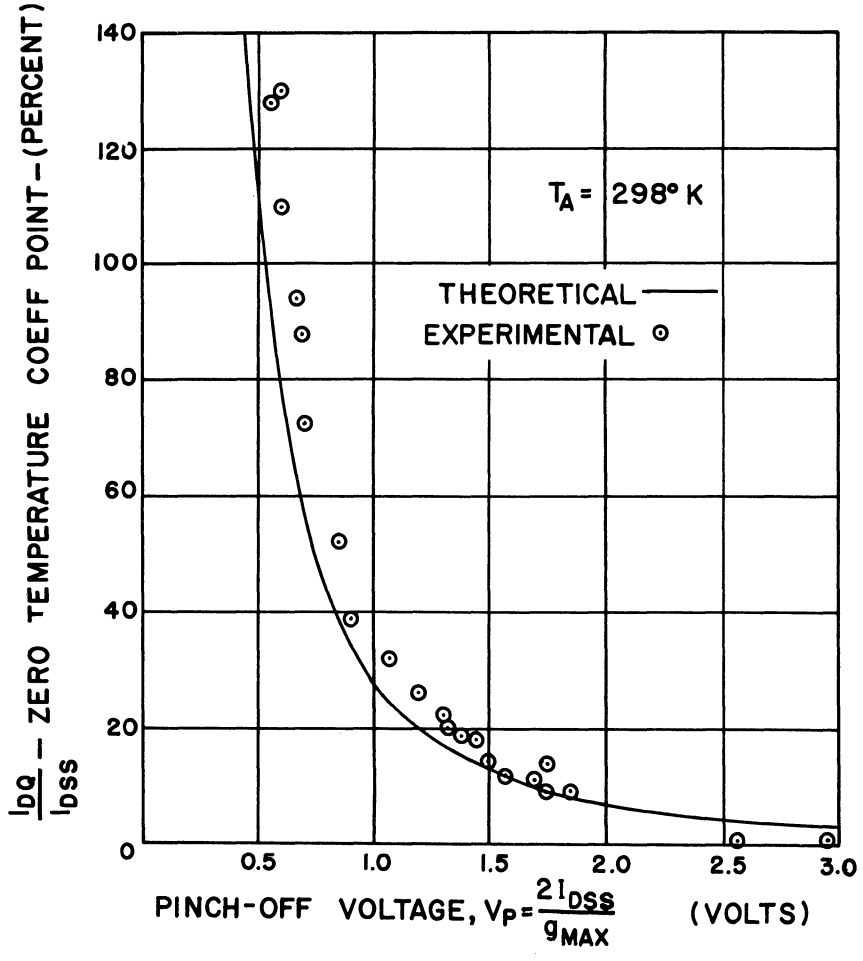

Fig. 5. Comparison of Eq. (20) with experiment.

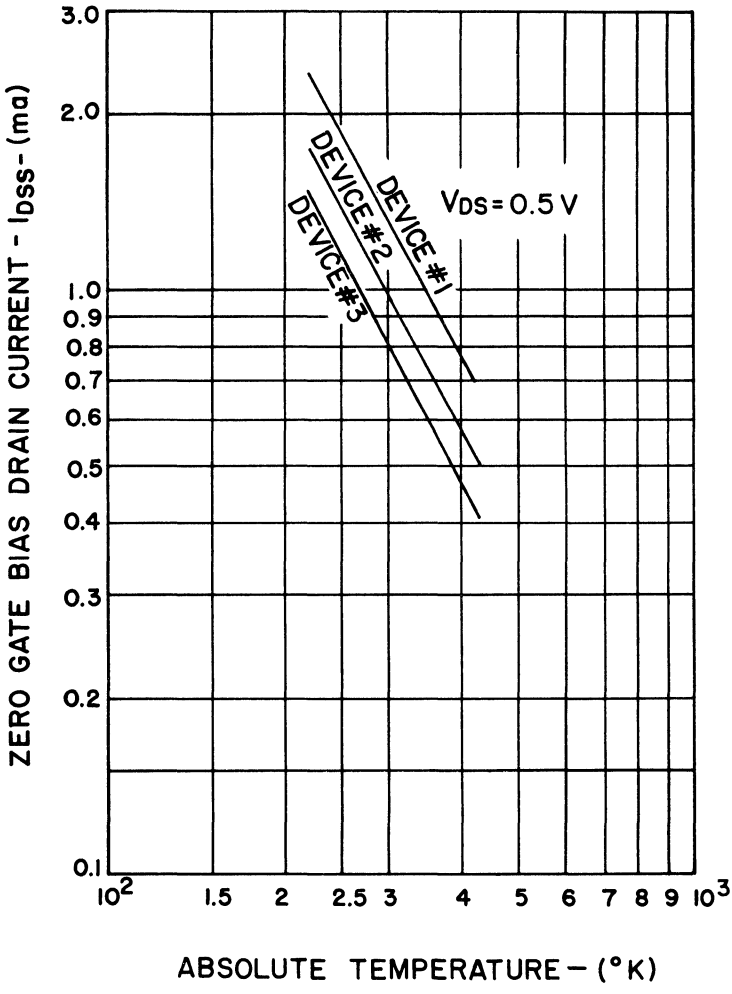

Figure 6

the field dependence of mobility[7] should be negligible. The slope of each ot these three graphs is about 2. Figure 7 shows Eq. (20) plotted with $n = 2$; compared to the experimental data, the "fit" is much better. The curve for $n = 1.5$ in Fig. 7 shows the anticipated behavior of N-channel FET's, though all devices used in the experiment were P-channel. Figure 8 shows Eq. (20) plotted for $n = 2$, with centigrade temperature as the running parameter. The almost negligible shift explains why the three curves in Fig. 2 cross-over at virtually the same bias point.

The only assumption made about the FET in deriving Eq. (20) is that it obeys the square law. The curves in Fig. 7 should then be applicable to any FET that obeys the square law, regardless of construction (subject of course, to variations of n with carrier densities); this includes induced-channel FET's.

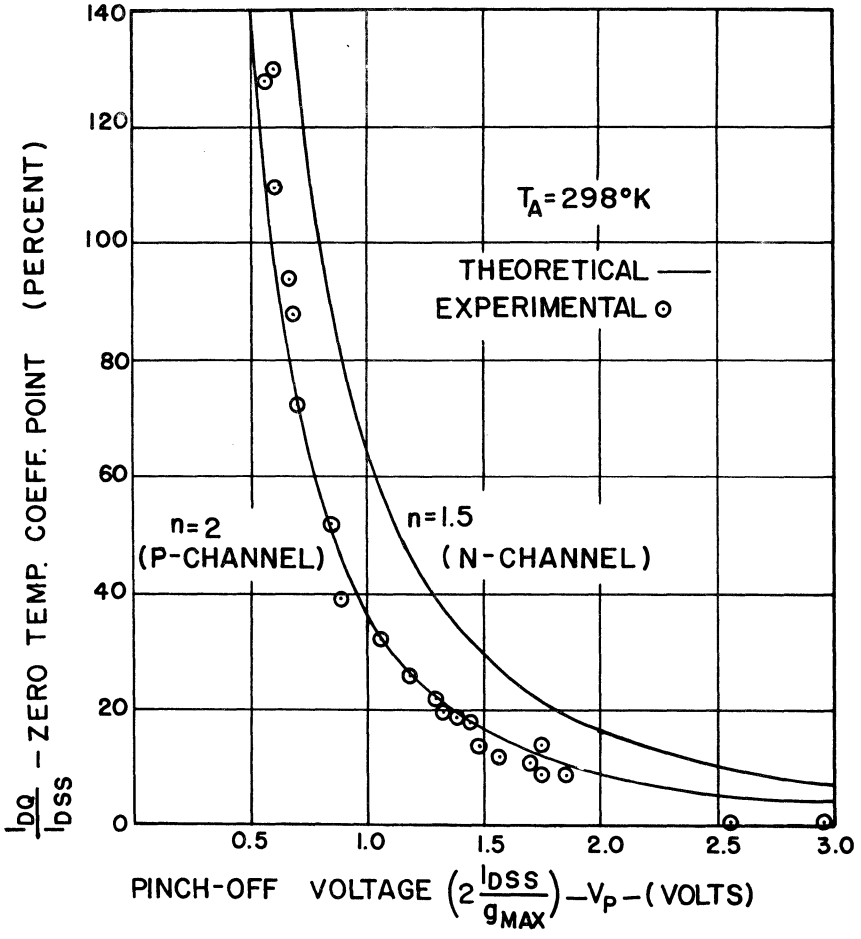

Fig. 7. Equation (20) replotted for n = 2, 1.5.

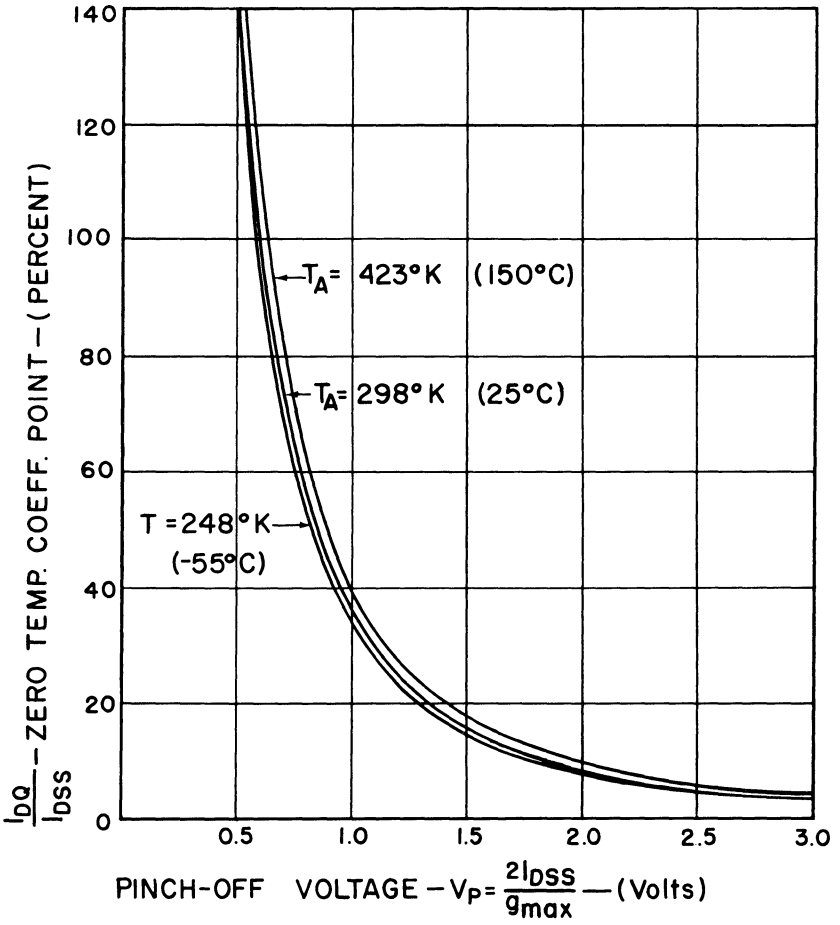

Fig. 8. Equation (20) vs. temperature.

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9

Dual Transistors in Low-level Circuits

by Stan Holcomb

INTRODUCTION

The noise problems encountered in a differential direct-coupled amplifier must be considered over a frequency range that extends from dc to the upper cutoff frequency of the amplifier. The noise problems encountered at the low frequencies and at the upper cut-off frequencies have been explained, but the noise at dc, commonly called "drift," requires singular consideration. Drift is primarily a function of the transistor's temperature sensitivity characteristics and operating conditions. It can be reduced considerably by using two matched transistors in a differential connection. Therefore, the major reason for placing two transistors in one package is to improve the matching and tracking characteristics.

To explain the usefulness of dual transistors, we present the drift performance of a generalized differential amplifier as related to the matching-tracking characteristics and operating conditions of dual transistors. Then, a high-quality low-drift circuit is presented to illustrate a practical application of dual transistors.

MATCHING-TRACKING CHARACTERISTICS AND OPERATING CONDITIONS RELATED TO AMPLIFIER DRIFT

The drift in a direct-coupled d-c amplifier that has differentially connected first and second stages is primarily caused by the first stage. The magnitude of this drift is determined by the matching characteristics and the operating conditions of the dual differential transistor used in the first stage. The operating conditions have an important effect on drift even when there are very tight V_{BE} tracking and 10% h_{FE} matching specifications.

The circuit for a general direct-coupled d-c amplifier is shown in Fig. 1. A dual differential transistor is used in the first stage. The remaining stages are represented by box A. The equivalent input voltage Δv_{in}* and current drift Δi_{in} of the amplifier

*The symbol Δ is used to denote $\frac{\Delta f(T)}{\Delta T}$

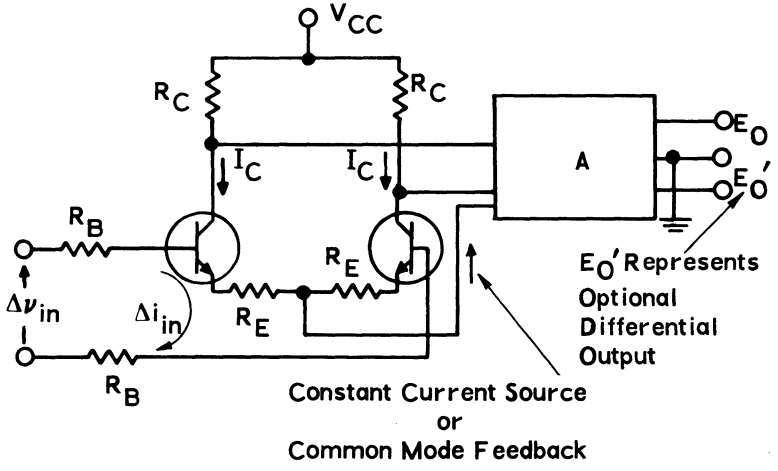


Figure 1

are related to the equivalent input voltage Δv_i and current drift Δi of the dual differential transistor by the following equations:

$$\Delta v_{in} = \Delta v + \Delta i(R_B + R_E)$$
$$\Delta i_{in} = \Delta i \qquad (1)$$

The equivalent input voltage drift Δv of the dual differential transistor is exactly equal to V_{BE} tracking or $\Delta V_{BE1} - \Delta V_{BE2}$. At this time there is no h_{FE} tracking specification in the industry which may be used to determine ΔI or $(\Delta I_{B1} - \Delta I_{B2})$. Therefore, there is no way to determine logically the exact drift performance of a

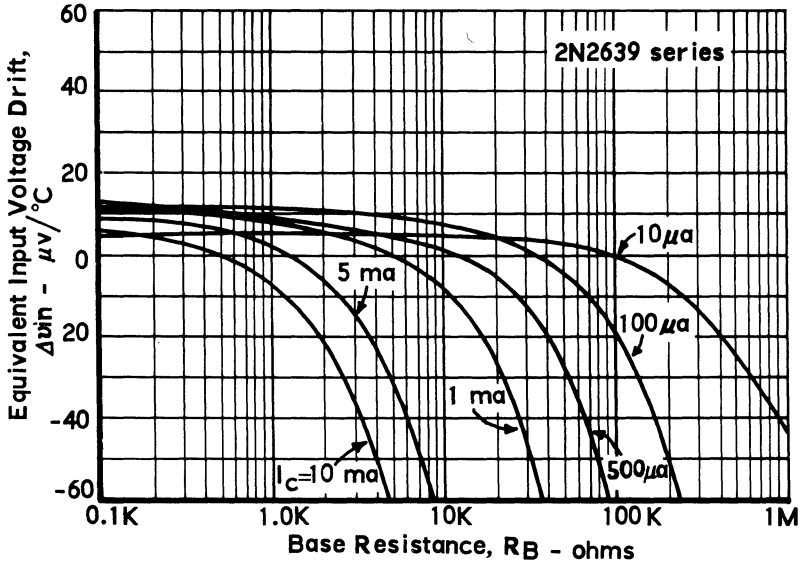


Figure 2

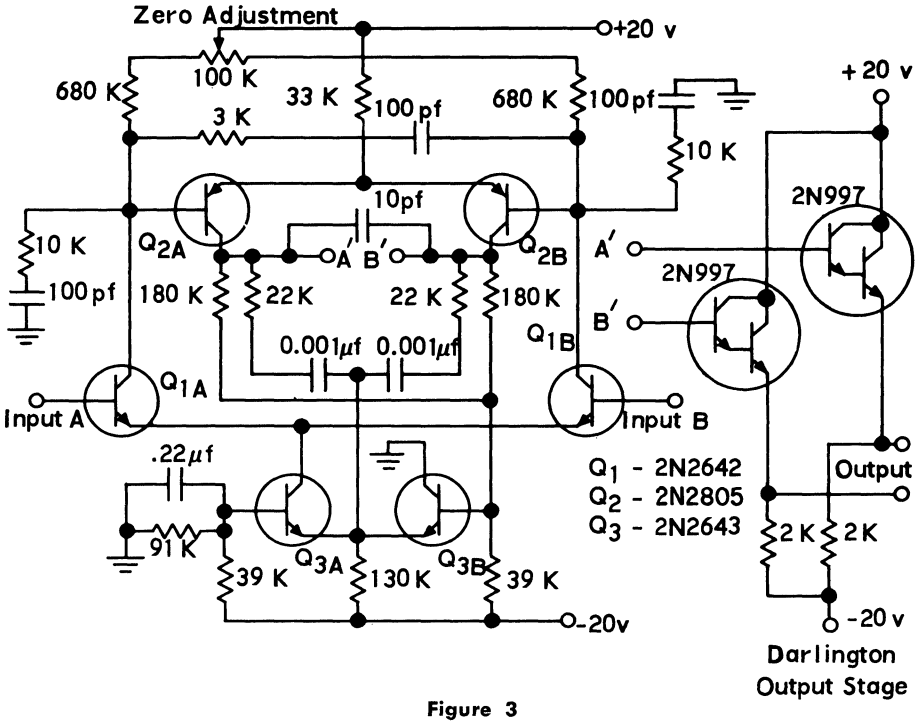


Figure 3

d-c amplifier from the guaranteed specifications, especially when there is a large base resistance. When there is no base or emitter resistance, the equivalent input voltage drift is represented by the equation:

$$\Delta v_{in} = \Delta v = \Delta V_{BE1} - \Delta V_{BE2} \qquad (2)$$

This is an unusual case, and more often the d-c source resistance, or base resistance R_B, is from 10 K to 500 K. In Eq. (1) the predominant effect of ΔI or base current tracking is illustrated. It appears that the circuit engineer has no guaranteed specification to determine the drift. This is not true with the 2N2639 series transistors or any other high-beta transistor. Because the base current is so small for a high-beta low-current transistor, the difference base resistor voltage drop is still relatively small for large base resistance, as shown in Fig. 2. Careful examination of Fig. 2 shows that input voltage drift increases rapidly as collector current increases, even at lower base resistance. Also, note that the input voltage drift is equal to the V_{BE} tracking for very small base resistances.

APPLICATION: A HIGH-QUALITY DIRECT-COUPLED DIFFERENTIAL AMPLIFIER

The circuit in Fig. 3 has been designed for general use either as a complete amplifier with a Darlington output stage or as the first two stages of a low-drift high-gain amplifier without the output stage. The circuit provides both low and high common-mode rejection for either differential or single-ended outputs: high

common-mode rejection is achieved by use of a common-mode feedback loop; low drift is achieved by using a dual transistor Q_3 as the first stage of the common-mode feedback loop. The functions of the loop and of the dual transistor Q_3 can be better understood by observing the amplifier circuit as shown in Fig. 4; here, transistors Q_1 and Q_2 act in parallel for common-mode signals. The average value of points A′ and B′ is compared with the ground or zero potential by Q_3 and its balanced resistive base divider network. By adjusting the ratio of either base divider with respect to the other, the average value of points A′ and B′ can be set precisely to the desired value. The dual transistor Q_1 acts as a common-base stage transferring with very little loss the amplified common-mode error signal, while it acts like a common-emitter stage with a very large emitter resistor (the output impedance of Q_3 operated at 20 μa) to the common-mode input source R_s and e_s, thus greatly attenuating it.

Low drift, large gain bandwidth, and low noise are obtained when duals with high gain, large bandwidth and tight matching are used throughout the circuit. Drift performance may be exchanged for economy if we know the effect of the matching parameters of each dual upon the performance. The matching of Q_1 is of utmost importance. If the amplifier is to perform well from a large d-c source (10 K to 1 M), Q_1 must be high in current gain. The input current tracking of Q_2 is the next most important characteristic for drift reduction, and the V_{BE} tracking of Q_2 is least important. The effect of high current gain in Q_3 is to improve common-mode rejection, and Q_3's ($V_{BE} - h_{FE}$) tracking affects the single-ended output common-mode rejection.

The drift and common-mode rejection performances are affected by the operating conditions of the transistors. The operating conditions of Q_1 are fixed at $I_c = 10$ μa and $V_{CE} = 15$ volts; the 10μa collector current helps reduce drift and

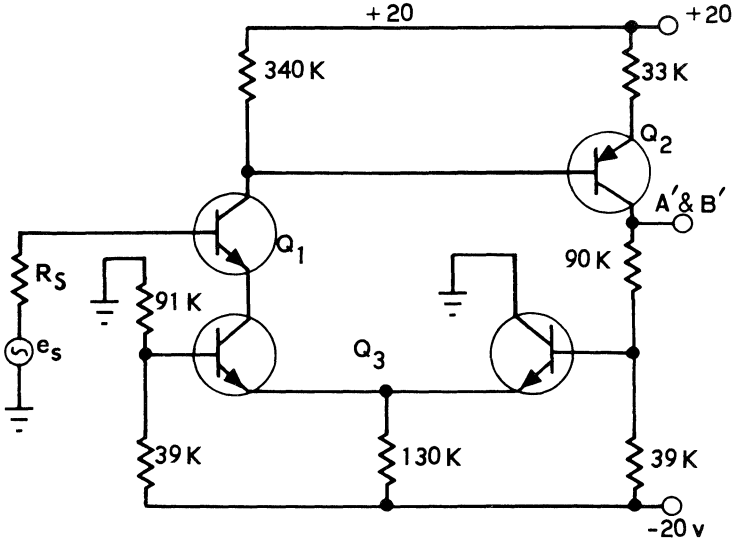


Figure 4

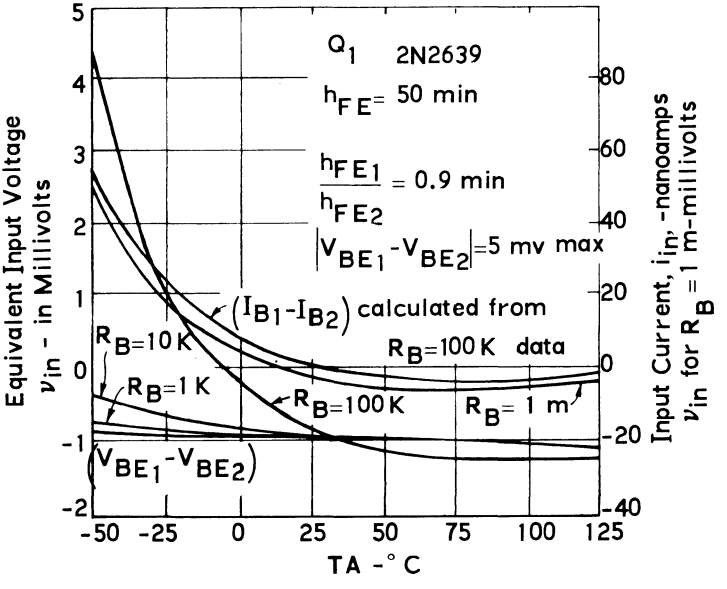


Figure 5

noise; the 15-volt collector-emitter voltage makes possible a positive 10-volt common-mode input voltage. The operating conditions of Q_2 are $I_c = 80$ μa and $V_{CE} = 15$ volts; these give a stable circuit current gain of 10 and a conservative positive 10-volt output swing, respectively. The collector-emitter voltage of Q_3 is set at -13 volts to accommodate a negative 10-volt common-mode input signal and to give maximum possible gain in the common-mode feedback loop. The output stage is operated at 10-ma collector current to give low output impedance.

PERFORMANCE CHARACTERISTICS

From the theory of amplifier drift as related to transistor matching, and from the foregoing circuit design, certain performance characteristics have been predicted and they should be evident in the following experimental results. The amplifier's equivalent input voltages v_{in} for zero output voltage vs temperature for four values of base resistance R_B are plotted in Fig. 5. The base-emitter difference ($V_{BE1} - V_{BE2}$) and base-current difference ($I_{B1} - I_{B2}$) vs temperature for a 2N2639 dual are also plotted in Fig. 5. A similar graph is given for a 2N2640 in Fig. 6, a 2N2642 in Fig. 7, and a 2N2643 in Fig. 8. In each case, the v_{in} for a small value of base resistance is almost identical to the V_{BE} difference voltage and for $R_B = 1$ M the input voltage is large and its variation with temperature approaches the shape of the base-current difference curve. The base-current difference was calculated from the $R_B = 100$ K data and the difference between the $R_B = 1$ M curve is approximately the V_{BE} difference showing that the experimental data are consistent with theory. The remaining results show that the input current is lower

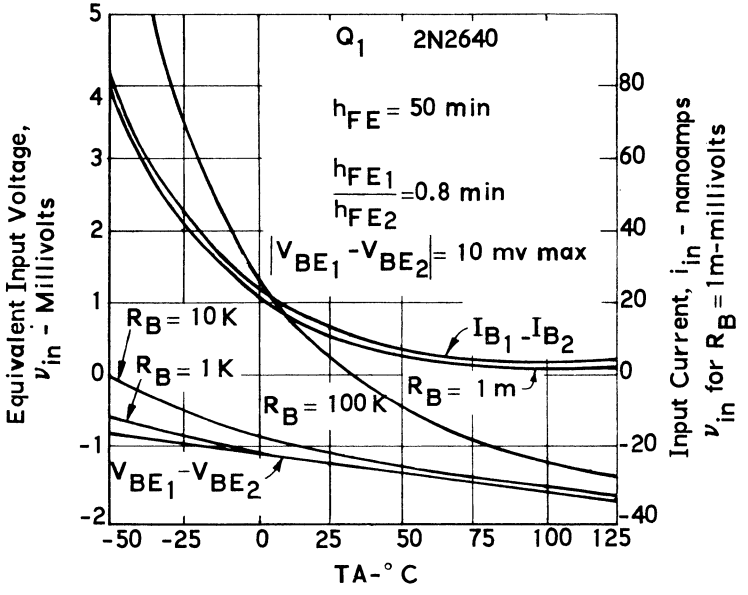


Figure 6

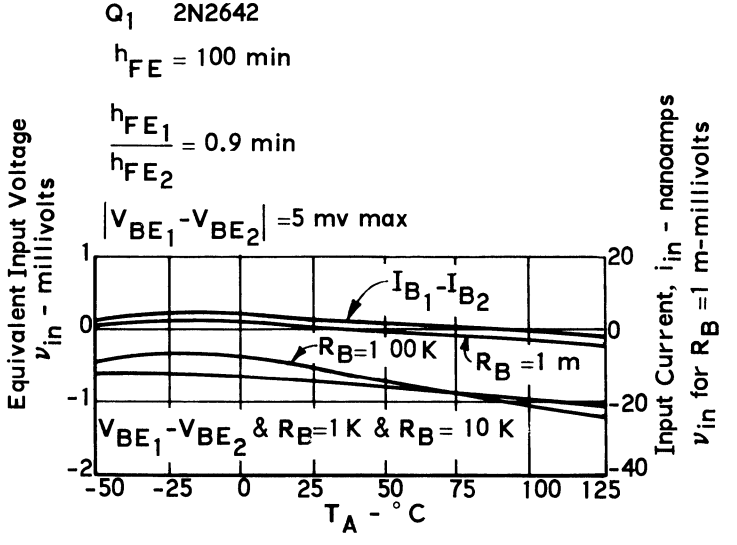


Figure 7

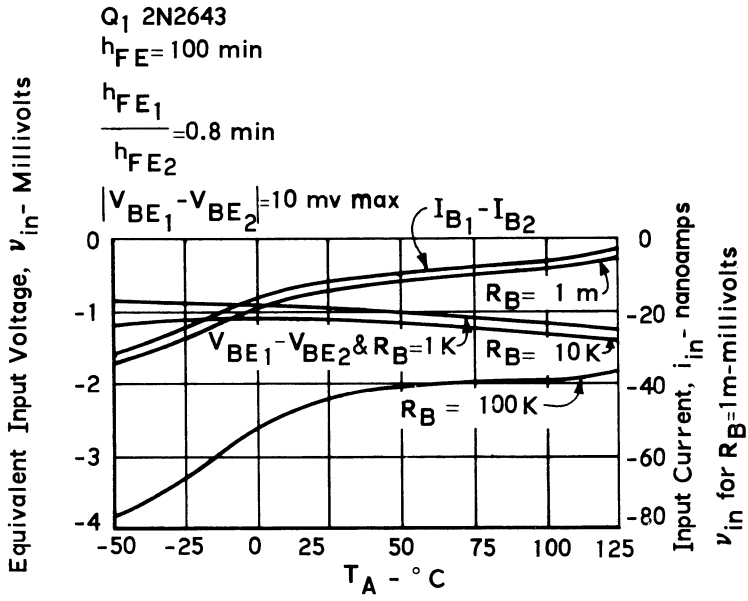


Figure 8

and more linear for duals with high current gain and tighter matched h_{FE}'s, e.g., 2N2642. Drift data as a function of the other transistor matchings were not taken, but data were taken on gain, frequency response, and common-mode rejection, since they are included in the design features.

Both the open-loop and the closed-loop single-ended voltage gains shown in Fig. 9 were made in the appropriate test circuits with one of the differential inputs grounded. Since the open-loop voltage-gain roll-off holds a constant −20 db per decade slope from its 850-cps break to beyond its 5-mc crossover, the amplifier is stable for output shorted to input (i.e., zero feedback resistance) and for operational integrator use.

Both open-loop and closed-loop common-mode rejection (CMR) data were taken in the appropriate test circuits with 20 volts peak-to-peak applied to both inputs. The very large CMR ratio even for a single-ended output is a result of the large amount of common-mode feedback and the close differential match of the first-stage parameters.

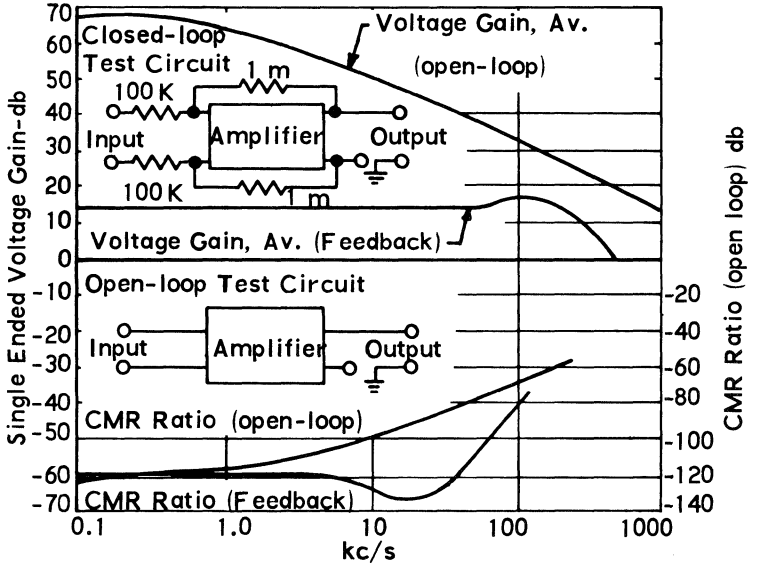

Closed-loop
Test Circuit
1 m
100 K
Input
Amplifier
Output
100 K
1 m
Voltage Gain, Av.
(open-loop)
Voltage Gain, Av. (Feedback)
Open-loop Test Circuit
Input
Amplifier
Output
CMR Ratio (open-loop)
CMR Ratio (Feedback)
Single Ended Voltage Gain-db
CMR Ratio (open loop) db
70
60
50
40
30
20
10
0
-10
-20
-30
-40
-50
-60
-70
-20
-40
-60
-80
-100
-120
-140
0.1
1.0
10
100
1000
kc/s

Figure 9

10

Low-level Operation of the 2N929 and 2N930

The 2N929 and 2N930 represent a considerable aid to the designer of low-level and low-noise circuitry. By rigid exclusion of all contaminants from the crystal surface, room temperature leakage currents are held to near theoretical minimum values. Because the number of surface recombination centers is low, careful control of the diffusion processes results in h_{FE}'s that remain high even at very low current levels.

This paper presents circuit suggestions and typical parameter curves to permit the designer to predict the performance of these transistors in his circuit. Curves shown are typical of both the 2N929 and the 2N930 unless otherwise noted.

LOW-FREQUENCY LOW-NOISE APPLICATIONS

Two types of low-frequency low-noise applications will be considered. The first is an amplifier which must respond to only one frequency, or at most, to a narrow band of frequencies. An index of noise performance under these conditions is the amplifier's spot noise figure NF. Loosely speaking, a noise figure is a measure, in decibels, of the amount by which the signal-to-noise power ratio is degraded when the signal passes through the amplifier. From another viewpoint, it relates the noise power output of the actual amplifier, fed from a resistive source impedance, to the noise power output of a perfect (i.e., noiseless) amplifier having the same gain and fed from the same source. For spot noise figures, only the power contained in the noise signal frequencies within a very narrow passband (e.g., 1 cps) is considered.

The second type of low-frequency low-noise application concerns an amplifier that must respond to a wide band of frequencies. A typical example is the high-fidelity audio amplifier. To evaluate noise performance in this application, the so-called "broadband" noise figure is useful. In this paper, broadband noise figure will be denoted by NF, and it may be thought of as an averaged noise figure over a passband with 10 and 10,000 cps half-power frequencies.

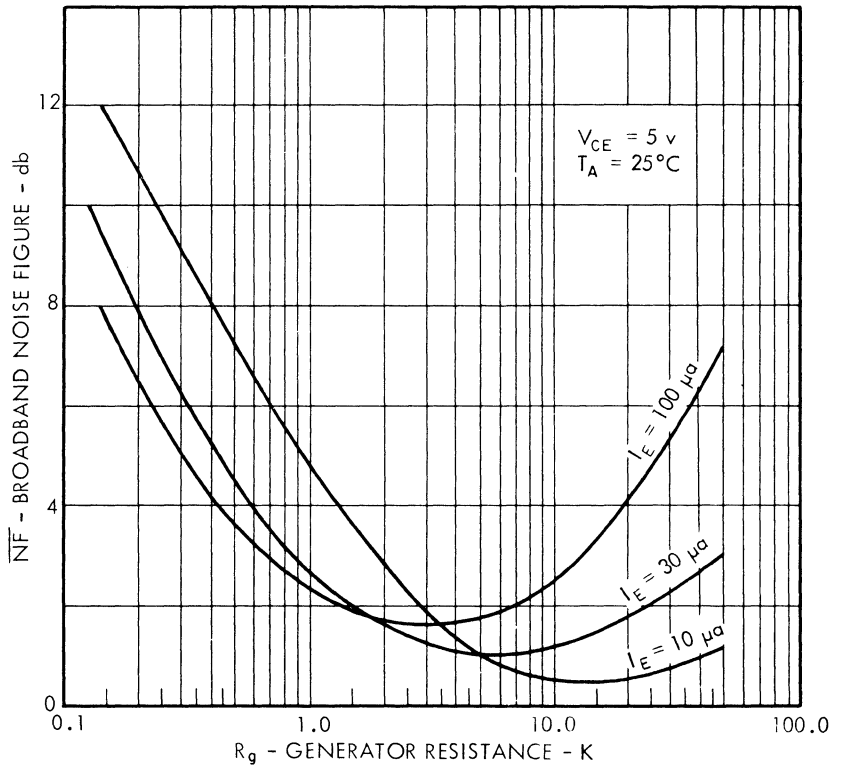


Fig. 1. Broadband noise figure vs. source impedance.

So long as the first-stage available power gain is greater than unity, the ultimate design objective is to minimize the noise figure. In theory, additional stages can always be added to provide any designed gain. Practically, however, good gain in the first stage simplifies the design problem by permitting RC coupling rather than transformer coupling and by reducing the effective noise contribution of the second stage.

The NF given by a particular transistor will vary with the emitter current, the signal source impedance and, to a lesser extent, the collector-emitter voltage. Typical NF's shown in Fig. 1 illustrate this. For this transistor series, optimum operating conditions for minimum NF will be about $I_E = 10$ μa, $R_g = 10$ K, and $V_{CE} = 5$ volts. However, it may sometimes be necessary to compromise the noise figure in order to accept a wider dynamic range of signals.

Typical NF's under these optimum conditions are displayed in Fig. 2.

High-frequency Low-noise Application. Over a frequency range of 2 kc to 1 mc, the NF's of the typical 2N929 and 2N930 remain 1 db or less. Above 1 mc, the NF rises, but the transistor remains useful to as high as 70 mc. Figure 3 illustrates this variation.

Figure 3 differs from the high-frequency spot noise curve shown on the transistor data sheet. This difference is due to a change in operating conditions. Data sheet curves were run at a constant emitter current of 1 ma, but this value is not optimum

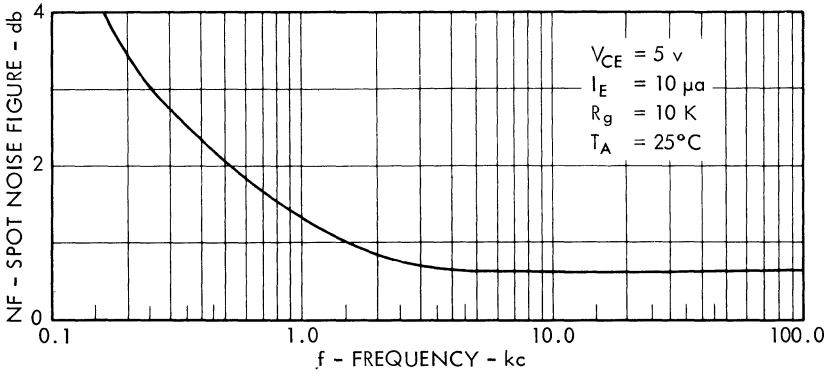


Fig. 2. Typical spot noise figure vs. frequency.

for the whole frequency range covered. To create the curve in Fig. 3, the source impedance and emitter current were varied with frequency as shown in Fig. 4.

To test the accuracy of Fig. 3, a 70-mc amplifier stage was constructed; details of this design are shown in Fig. 5. Averaged results for five units are given in Fig. 6. Optimum emitter currents and source impedances are well within the predicted range. NF is 0.6 db higher than predicted, probably due to differences in circuit losses or to measurement errors.

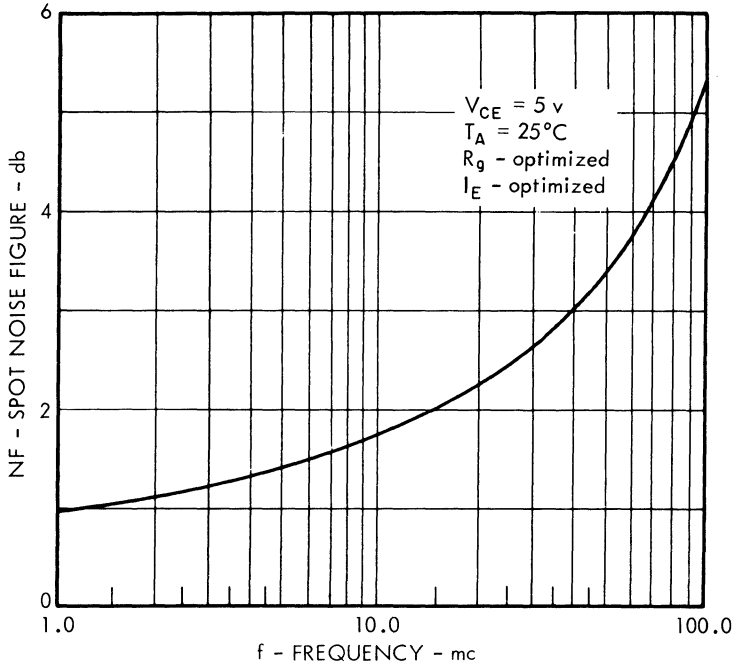


Fig. 3. Typical spot noise figure vs. frequency.

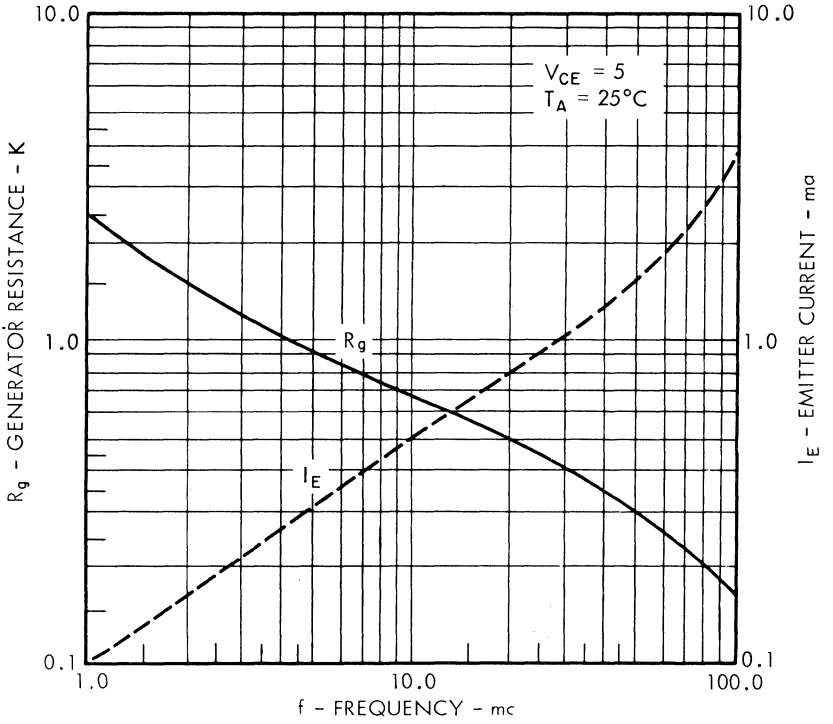


Fig. 4. Optimum source impedance and emitter current vs. frequency.

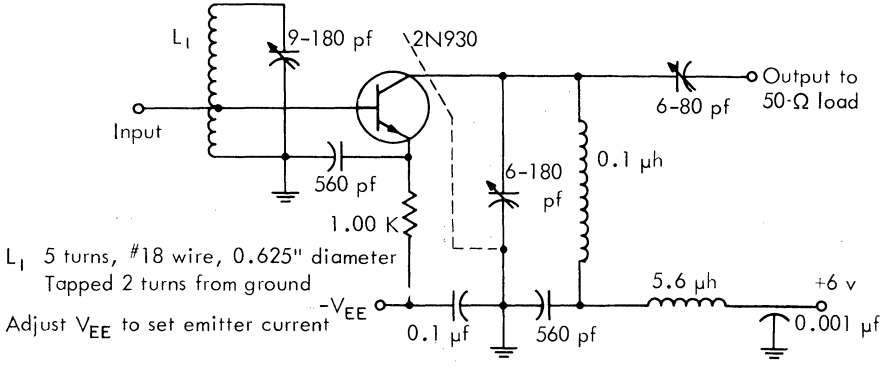


Fig. 5. 70-mc noise test amplifier.

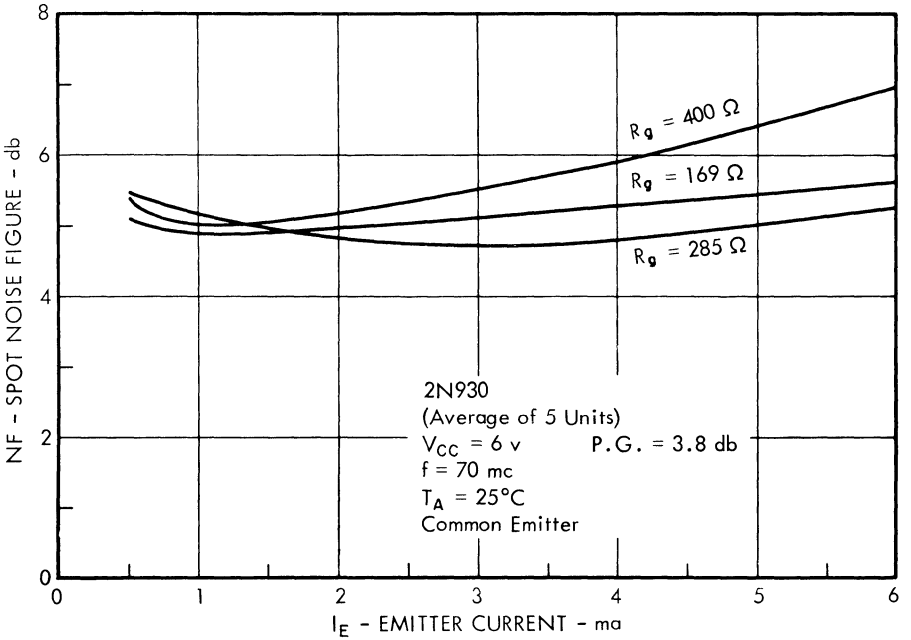
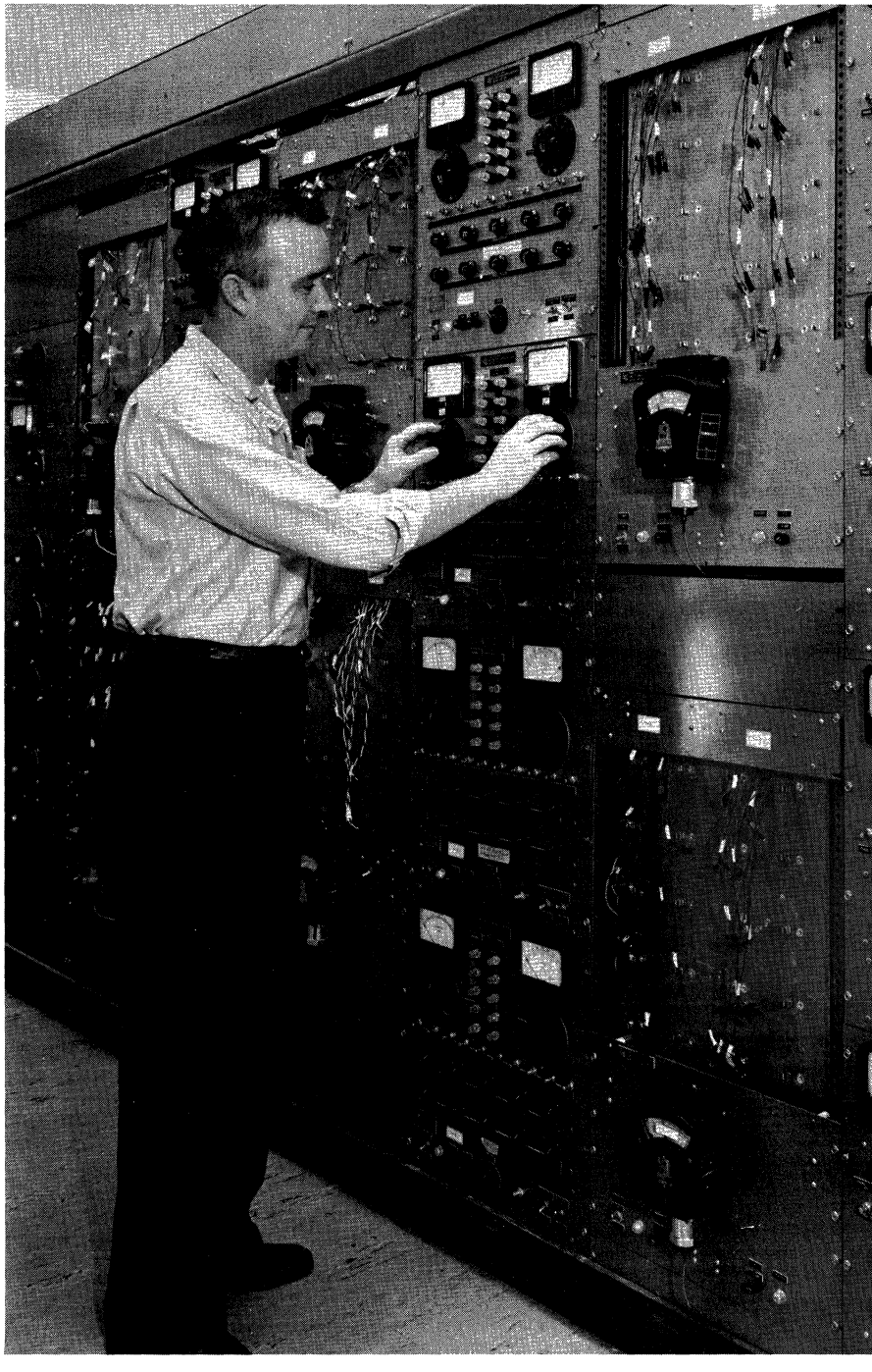


Fig. 6. Spot noise figure vs. I_E and R_g.



One small corner of TI's life-testing facilities, where more than 100,000 transistors can simultaneously be subjected to operating life tests.

11

High Input Impedance Techniques

by Ralph Dean

INTRODUCTION

The bipolar transistor, being current controlled, is inherently a low input impedance device. Many transistor circuits perform very satisfactorily at input impedance levels of a few kilohms or less. Other applications, however, require input impedances in the hundreds of megohms. The field-effect (unipolar) transistor, being a voltage-controlled device, has an inherently high input resistance in the order of 10^{12} ohms. But the shunting effects of bias networks and junction capacitances necessitate the use of special techniques in order to obtain high impedances over a wide frequency range. Techniques presented here can yield hundreds of megohms input impedance using either bipolar or unipolar transistors.

METHODS

All impedance multiplying techniques involve some form of feedback. Positive feedback, negative feedback, or combinations of both can be used. There seems to be no standard for describing feedback in general terms, so this subject will be discussed briefly. In Figs. 1a through 1d, each basic amplifier and its associated feedback network is represented by a four-terminal network. The manner in which the networks are interconnected determines the effect of the feedback on gain, and output impedance. In describing these configurations, the words "shunt" and "series" will be used to describe the manner of interconnection. For example, the configuration of Fig. 1c would be described as "series-shunt." The first term describes the interconnection at the input to the amplifier; the second term describes the interconnection at the output terminals. This configuration is also designated "h-type" because the respective h-parameters of the networks are simply added to obtain the composite h-parameters. The other configurations are called shunt-shunt, (y); shunt-series, (g); and series-series, (z). In each case the parameter system is such that composite parameters are obtained simply by the addition of corresponding parameters.

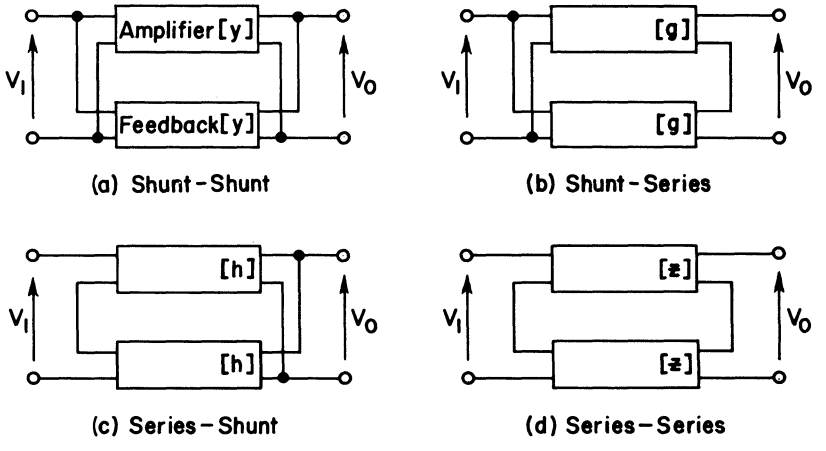


Fig. 1. Feedback configuration.

It is easily shown that series negative feedback at the input increases Z_{in} and reduces the voltage gain. It can also be shown that shunt negative feedback decreases Z_{in} and the current gain. Negative feedback taken in series from the output increases Z_o; if taken in shunt, it decreases Z_o. The opposite behavior is observed for positive feedback in all the above configurations.

When considering Z_{in}, the input terminals are of primary interest. Further references to feedback in this chapter will refer to the input terminals only, unless otherwise specified.

BASIC IMPEDANCE MULTIPLIERS

Perhaps the most common impedance multiplier is the negative series-shunt configuration shown in Fig. 2. The input impedance is $Z_{in} = Z_1 (1 + A\beta_f)$. If $A\beta_f$ is positive, the feedback is negative and causes the input impedance to increase.

The familiar emitter follower is illustrated in Fig. 3. The h-parameter matrix of the transistor is:

$$[h]_t = \begin{bmatrix} h_{ie} & -h_{re} \\ -h_{fe} & h_{oe} \end{bmatrix}$$

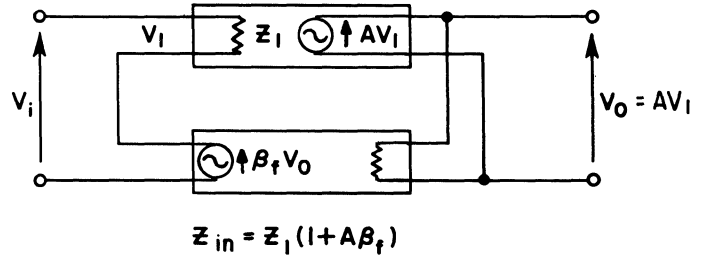


Fig. 2. Series-shunt connection.

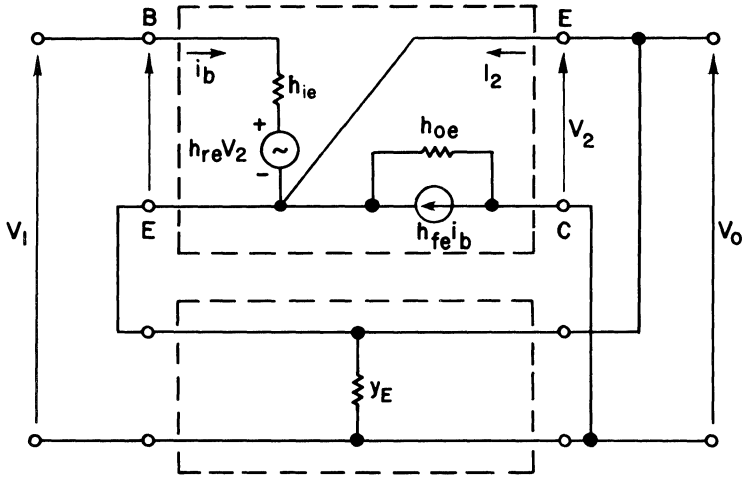


Fig. 3. h-parameter representation of emitter follower.

Negative signs are associated with h_{re} and h_{fe} because V_2 and I_2 are reversed from their normal sense. The h-matrix of the feedback network is

$$[h]_f = \begin{bmatrix} 0 & 1 \\ -1 & Y_E \end{bmatrix}$$

The composite matrix is

$$[h]_c = \begin{bmatrix} h_{ie} & (1-h_{re}) \\ -(h_{fe}+1) & (h_{oe}+Y_E) \end{bmatrix}$$

Substituting these parameters into the general input impedance equation,

$$Z_{in} = h_{11} - \frac{h_{12}h_{21}}{h_{22}+Y_L} \tag{1}$$

we obtain

$$Z_{in} = h_{ie} + \frac{(h_{fe}+1)(1-h_{re})}{h_{oe}+Y_E} \tag{2}$$

$$Z_{in} \cong h_{ie} + \frac{h_{fe}+1}{h_{oe}+Y_E} \tag{3}$$

Z_{in} is shown in this form to illustrate the ease of finding the composite h-parameters and hence the characteristic performance equations of such a composite network. For our present purposes however, it is more illustrative to write Eq. (2) in terms of the common-base T parameters

$$Z_{in} = r_b + \frac{(\beta+1)(R_E+r_e)r_c}{(\beta+1)(R_E+r_e)+r_c} \tag{4}$$

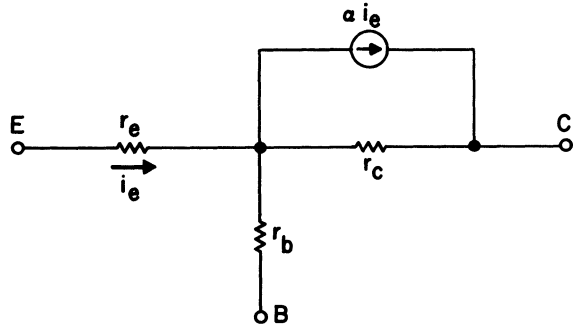


Fig. 4. Common-base T-equivalent circuit.

Equation (4) may be obtained by transformation from Eq. (2) or by direct derivation from the T-equivalent circuits of Figs. 4 and 5.

Note that the collector shunt resistance in the common-emitter configuration, Fig. 5, is less than the common-base value by the factor $(1-\alpha)$. The value of the common-emitter current gain is greater than the common-base gain by $1/(1-\alpha)$. The term $\beta = \alpha/(1-\alpha)$ should not be confused with β_f which was used previously for feedback factor. Typical values for the T parameters are:

α = 0.9 to 0.995
β = 10 to 200
r_c = 1 to 20 megohms
r_b = 500 ohms
r_e = $26/I_E$ ohms/milliampere

where I_E is the emitter bias current.

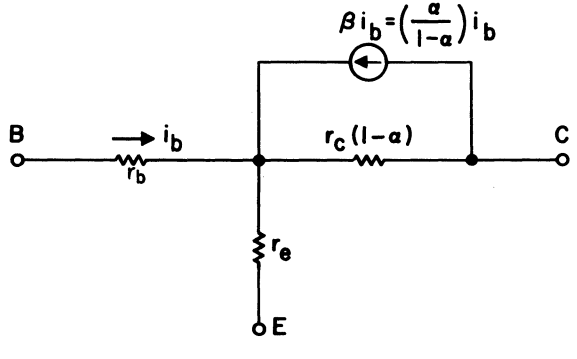


Fig. 5. Common-emitter T-equivalent circuit.

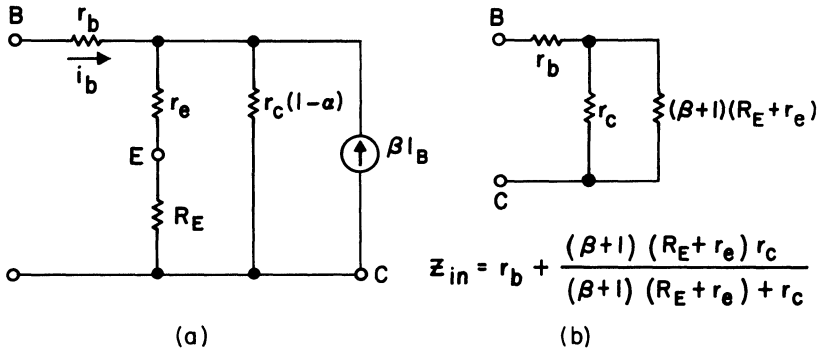


Fig. 6. Common-emitter T representation of emitter follower.

The term "current multiplication" has been applied to the type of impedance multiplier being discussed. This is illustrated in Fig. 6, where the common-emitter T equivalent is used with an emitter-follower amplifier. Here the input current is multiplied by the current gain β. Then the current which flows through the parallel combination of $r_e + R_E$ and $r_c(1-\alpha)$ is $(\beta + 1)\, i_b$. This current passing through $(r_e + R_E)$ provides the negative series feedback which multiplies the feedback resistance by the current gain plus one. The input impedance is:

$$Z_{in} = r_b + \frac{(\beta + 1)(R_E + r_c) r_c}{(\beta + 1)(R_E + r_e) + r_c} \tag{5}$$

Both the series emitter resistance and the collector shunt resistance are multiplied by $\beta + 1$, but since the collector shunt resistance is $r_c(1-\alpha)$, and $(1-\alpha)(\beta+1) = 1$, this term reduces to r_c. The equivalent input network is shown in Fig. 6. The same result would have been obtained if the common-base equivalent had been used. This concept is illustrated in general terms in Fig. 7. In general,

$$Z_{in} = Z_1 + (A_I + 1) R_F \tag{6}$$

Several current amplifiers can be cascaded to obtain very large current multiplications. The Darlington configuration shown in Fig. 8 achieves a large current multiplication. However, the input impedance of the Darlington current multiplier is limited by the shunting effect of the collector resistance of Q_1. Circuits of this type can achieve input impedances in the order of a megohm. Techniques for reducing the effects of shunt resistance are discussed next.

$$\bar{Z}_{in} = \bar{Z}_I + (A_i + 1)\, R_F$$

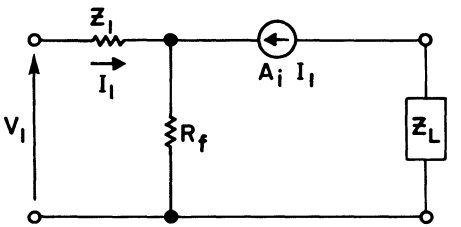


Fig. 7. Current multiplier.

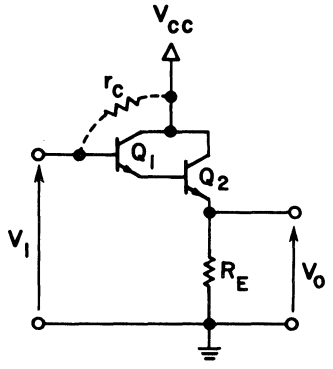


Fig. 8. Darlington emitter-follower configuration.

In Fig. 9, an idealized voltage amplifier is shown with shunt-shunt positive feedback. Although y-parameters would be used with a more complex system, for the simple amplifier shown it is more illustrative to use loop equations to obtain

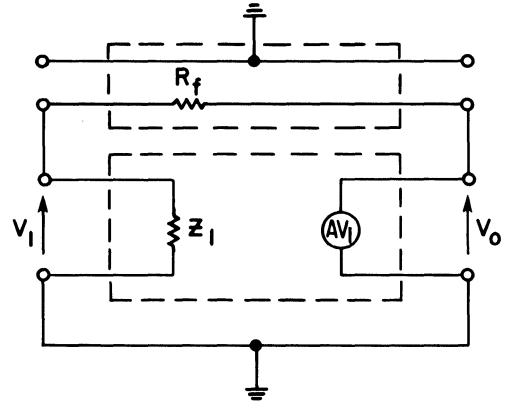
$$Z_{in} = \frac{R_f Z_1}{R_f + (1-A)Z_1} = \frac{1}{\frac{1}{Z_1} + \frac{1-A}{R_F}} \tag{7}$$

Z_{in} approaches infinity as A approaches

$$\frac{R_f + Z_1}{Z_1}$$

Obviously, if A is made to approach this value, A and the circuit impedance must be carefully controlled to prevent negative impedances from occurring. If $A = 1$, Eq. (7) reduces to Z_1. That is, the R_f term vanishes. The use of shunt positive feedback to reduce the effect of a shunt impedance is known as bootstrapping. If the gain A is unity, the bootstrapping is complete. If A is less than unity, the bootstrapping is partial. In general, a shunt impedance such as R_f in Fig. 8 is magnified by the gain A such that

$$R_{equivalent} = \frac{R_f}{1-A} \tag{8}$$



$$Y_{in} = \frac{1}{Z_1} + \frac{(1-A)}{R_f}$$

Fig. 9. Shunt feedback.

$$\lim_{A \to 1} Z_{in} = \frac{(R_E + r_e)(r_c + r_b)}{(1-\alpha) r_c} \approx (\beta+1)(R_E + r_e)$$

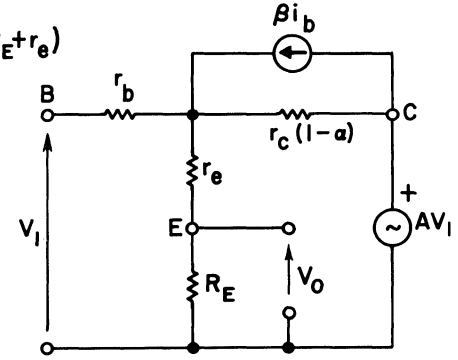


Fig. 10. Emitter follower with collector bootstrapping.

Now consider the bootstrapped emitter follower shown in Fig. 10. Since the collector of the transistor presents a fairly high impedance, it is easily driven from a low-impedance source. The exact manner in which this is done is not important at the moment. It is easily shown that

$$Z_{in} = \frac{(R_E + r_e)(r_c + r_b) + (1-A) r_c r_b}{(1-\alpha) r_c + (1-A)(R_E + r_e)} \tag{9}$$

if A = 1,
$$Z_{in} = r_b + \frac{R_E + r_e}{(1-\alpha)} \left(1 + \frac{r_b}{r_c} \right) \cong r_b + \frac{R_E + r_e}{1-\alpha} \tag{10}$$

The shunting effect of r_c has been virtually eliminated by bootstrapping.

To this point, nothing has been said about input capacitance. Normally, at low frequencies this is of no concern. However, as the resistive component of input impedance is increased the capacitive component quickly becomes significant. Fortunately the bootstrapping technique can be used to reduce the effective collector capacitance in the same manner as the shunt conductance can be reduced. Another way to view bootstrapping is to consider it as the reverse of Miller effect. For example, the common-emitter amplifier shown in Fig. 11 has a voltage gain A. The value of C_{in} then is $C_{OB}(1-A)$. Since A is negative in this case, C is effectively

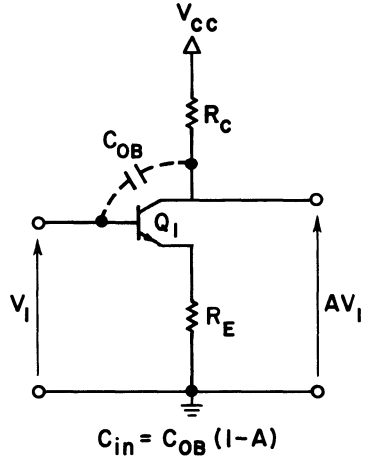


Fig. 11. Miller effect.

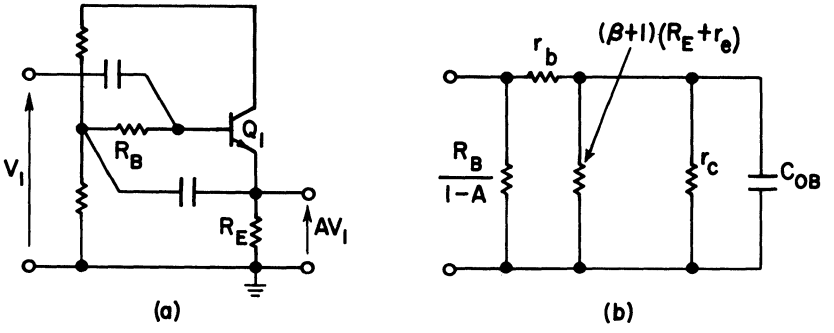


Fig. 12. Emitter follower with bias bootstrapping.

increased. If A is positive and unity, as in the case of perfect bootstrapping, the shunting effect of C_{OB} is eliminated.

The bootstrapping technique can also be applied to external impedances such as bias networks. Such an arrangement is shown in Fig. 12. In this case, the gain A is the gain of the emitter follower. Since $A < 1$, the effect of R_B cannot be completely eliminated. The series element r_b is usually a few hundred ohms, and may be neglected. The next shunt element $(\beta + 1)(R_E + r_e)$ is affected by the permissible values of R_E and current level. These in turn are related to the stability factor. The last shunt element r_c cannot be bootstrapped because a capacitor between the collector and emitter would short the collector generator. Input impedances of about a megohm can be obtained from this configuration.

In the circuit of Fig. 13, the second transistor increases the current multiplication, and allows the collector of Q_1 to be bootstrapped by isolating the output voltage from Q_1. An input impedance of several megohms can be obtained with this circuit.

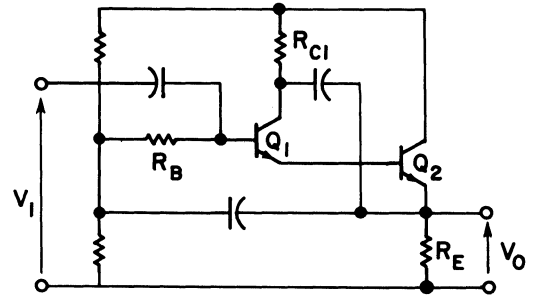


Fig. 13. Darlington emitter follower with collector and bias bootstrapping.

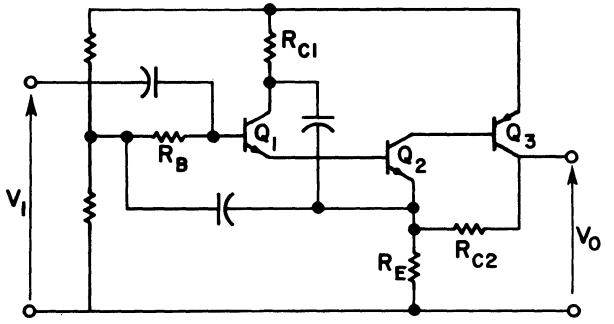


Fig. 14. Darlington complementary amplifier.

The circuit of Fig. 14 offers further current multiplication and higher gain for more effective bootstrapping. Frequency response is rather low in the circuits of Figs. 13 and 14 because the low-current level of Q_1 causes the frequency response of this transistor to be low.

Frequency response of these circuits can be improved by biasing Q_1 with a current generator in its emitter leg as shown in Fig. 15a. This raises I_E to a level where

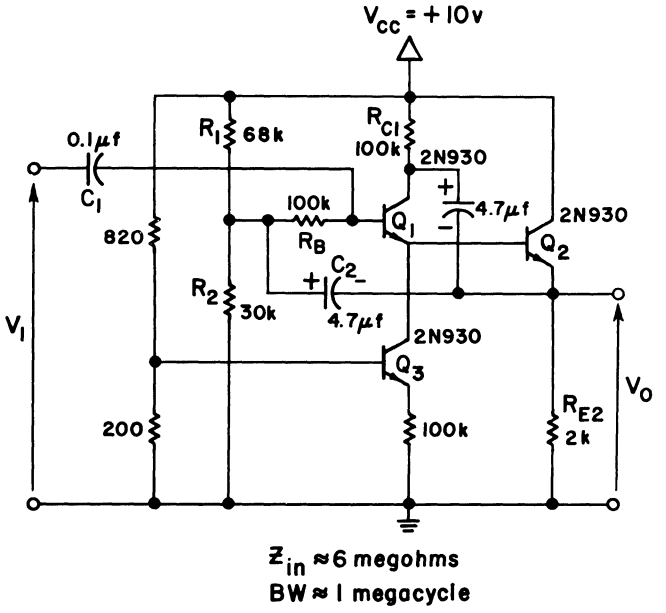


Fig. 15a. Cascaded emitter follower with current bias.

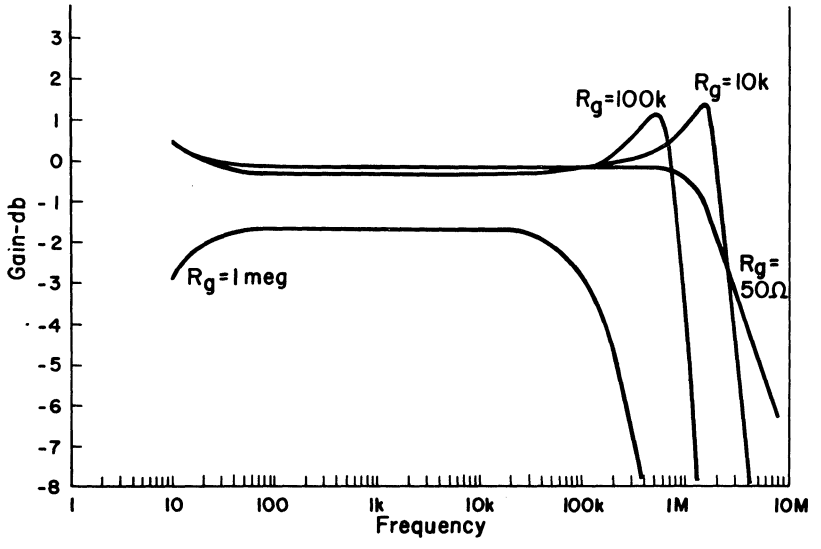


Fig. 15b. Frequency response curves of cascaded emitter follower.

the cutoff frequency of Q_1 is reasonably high, yet the external emitter impedance is maintained at a high level. An input impedance of 6 megohms was measured on this circuit. Frequency response curves are shown in Fig. 15b. The peak at high frequencies is caused by the normal phase shifts within the amplifier. The low-frequency peak is caused by resonance between the input capacitor C_1 and the effective inductance of R_B. This phenomenon is caused by phase shift within the bootstrap network, C_2, R_1, R_2. It can be shown that the resistor R_B appears to be inductive at low frequencies.

Increasing values of R_g lower the Q of the resonant circuit to a point where the peak is no longer seen.

In the circuit of Fig. 16a, a complementary transistor Q_4 has been added to increase current multiplication. This also increases the gain at the emitter of Q_2 by raising the effective value of R_{E2}. This higher gain makes the bootstrapping more effective. An input impedance of 25 megohms was obtained with this circuit. Response curves are shown in Fig. 16b. These curves are very similar to the curves of Fig. 15b.

In the circuit of Fig. 17a, positive shunt feedback is used to cancel the shunt impedance of the bias network and the transistor. Theoretical input impedances of $(h_{fe1}h_{fe2}R_{E1})$ can be obtained. In the illustration, R_{E1} is made small in order to obtain a gain of 10. As a result, Z_{in} is limited to about 1.5 megohms. Higher values can be obtained by increasing the ratio R_{E1}/R_{E2}. The feedback impedance R_f, and C_f could be further adjusted to cancel the impedance $(h_{fe1}\,h_{fe2}\,R_{E1})$, but since this term is by no means constant, instability would result. The major advantage of this circuit is that excellent bias stability is obtained. The three diodes, D_1, D_2, and D_3 compensate for variations in V_{BE1}, and the negative d-c feedback from R_{E2} further increases bias stability. Response curves for this circuit are shown in Fig. 17b. Voltage gain was observed to increase 1% over the temperature range -25 to 125°C. The quiescent collector voltage of Q_2 decreased 6% over the same range.

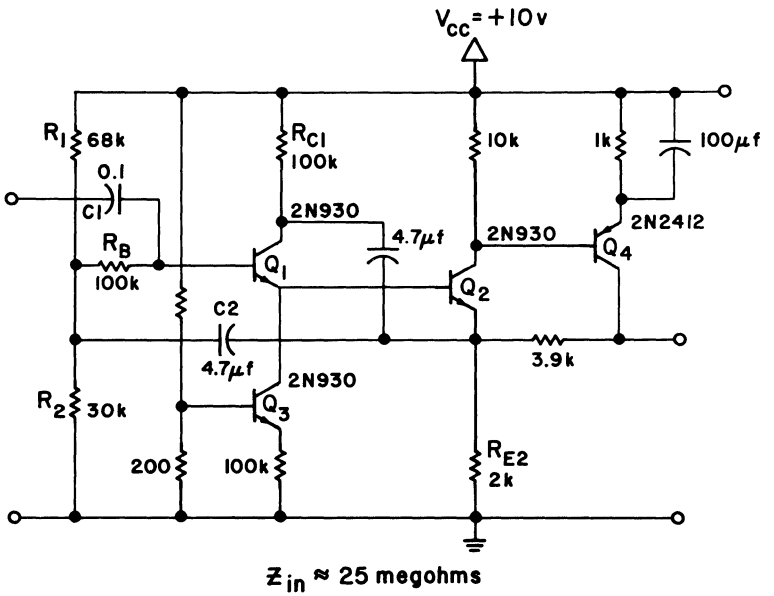


Fig. 16a. Complementary current multiplier.

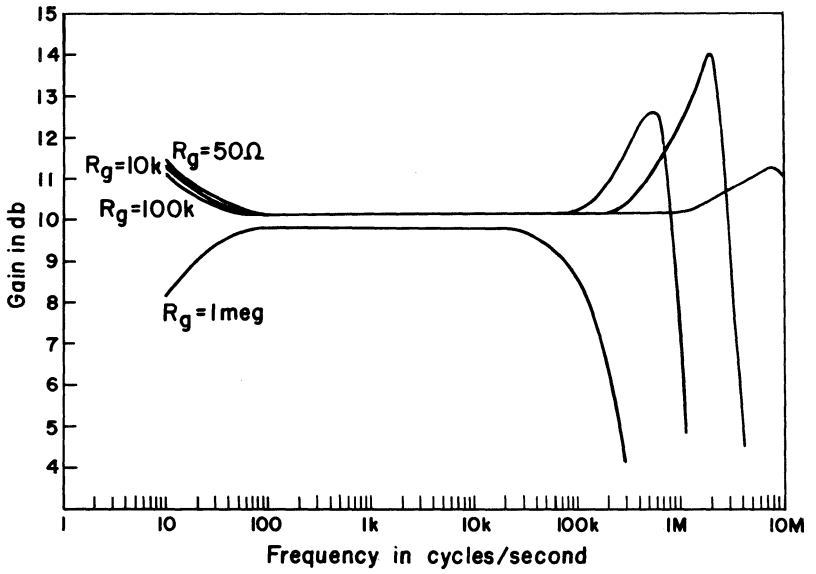
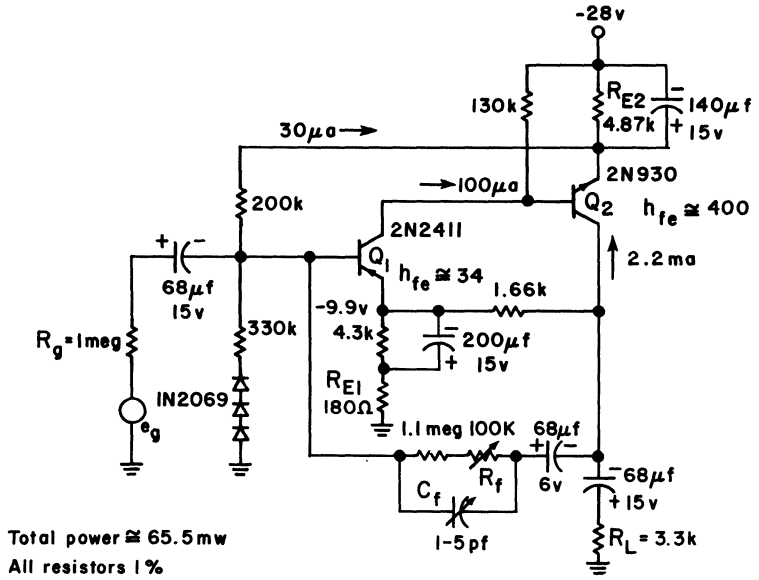


Fig. 16b. Complementary emitter-follower frequency response curves.



Total power ≅ 65.5mw
All resistors 1%
Midband input |Z| ≅ 1.5 megohm
Maximum power out without clipping = 1mw into 3.3 k
power gain ≅ 4.3×10^4
d-c output bias voltage stable within 6% from −25°C to +125°C

Figure 17a

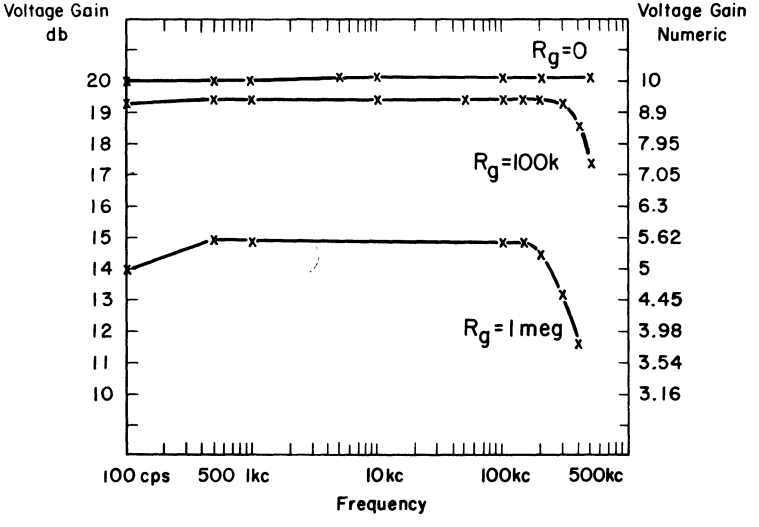


Fig. 17b. Voltage gain vs. frequency.

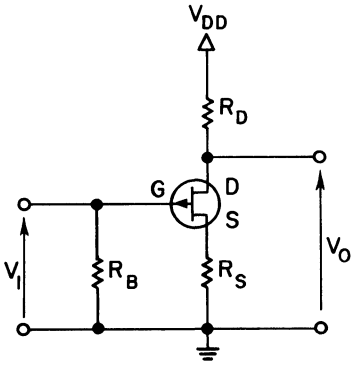


Fig. 18. Basic FET amplifier.

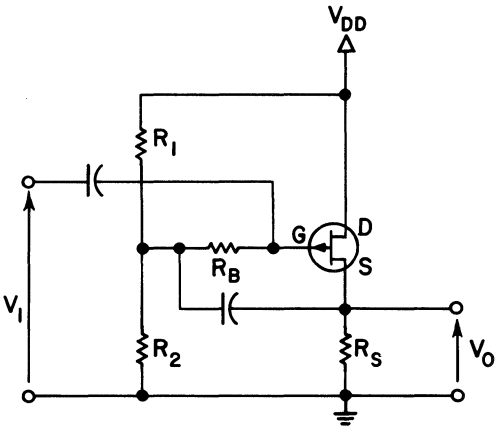
FIELD-EFFECT TRANSISTORS

The special techniques demonstrated thus far apply to increasing the input impedance of junction (bipolar) transistors. But the field-effect (unipolar) transistor exhibits an inherently high input resistance. Its behavior is very much like that of the vacuum pentode. Fig. 18 shows a very rudimentary FET amplifier. The G or gate terminal is the control electrode corresponding to the grid of a tube, the D or drain terminal corresponds to the plate, and the S or source terminal corresponds to the cathode. The FET illustrated is a P-channel device; the bias polarities are opposite those of the vacuum tube. The gate electrode is in this case one side of a P-N junction. In normal operation this junction is reverse biased, and it exhibits a finite junction capacitance.

The input impedance of the circuit shown is approximately 1000 megohms shunted by 9 pf. This capacitive component becomes significant at a rather low frequency, making it necessary to use bootstrapping to reduce the effective input capacitance. Consider now the source follower shown in Fig. 19. The gain is:

$$A_v = \frac{1}{1 + \frac{1}{g_m R_s}}$$

The transconductance g_m of the FET may be near 1000 micromhos at its maximum current. Then, to obtain $A_v = 0.98$, R_s must be greater than 50 kilohms. This conflicts with the requirement that the quiescent current should be large to obtain high g_m. This problem is alleviated in the circuit of Fig. 20 by obtaining the bias current from the current generator Q_2. The effective source resistance is now r_{c2} since Q_2 is effectively a common-base stage. This scheme is used in the circuit of Fig. 21. Q_1 is the FET and Q_2 is the current generator. Q_3 and Q_4 function as a complementary current multiplier. Bootstrapping for R_B is obtained directly from the emitter of Q_3. An adjustment R_{10} is provided in order to obtain greater than unity gain at the drain of Q_1. This allows the response to be peaked for high values of R_g. Voltage gain is 2 and input impedance is 200 megohms. Response curves are shown in Fig. 21a. The dashed curve (R_g = 10 megohms) was obtained using the peaking adjustment just described.



$$A_V = \frac{1}{1 + \frac{1}{g_m R_s}}$$

Fig. 19. Source follower.

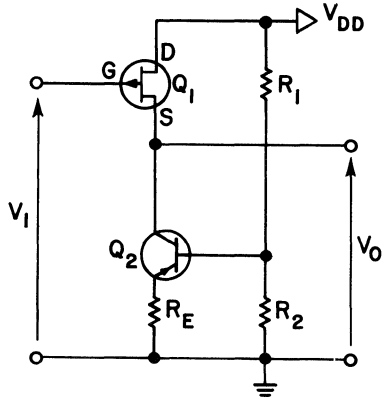


Fig. 20. Source follower with current-generator bias.

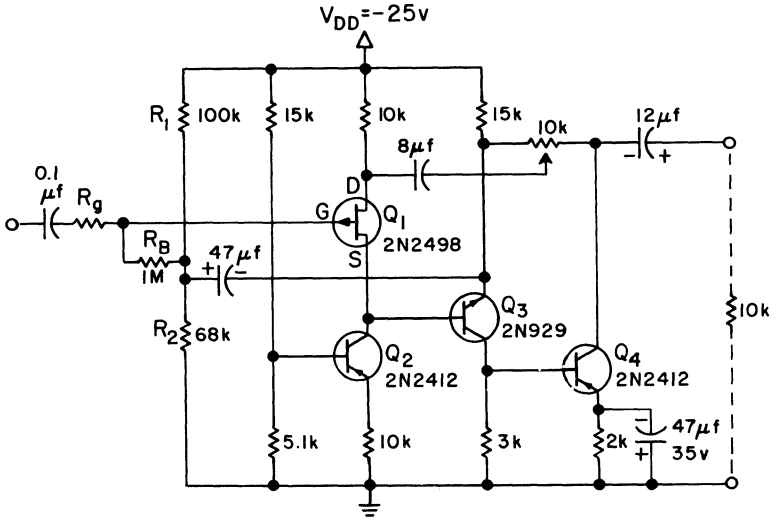


Fig. 21. 6-db high input Z FET amplifier.

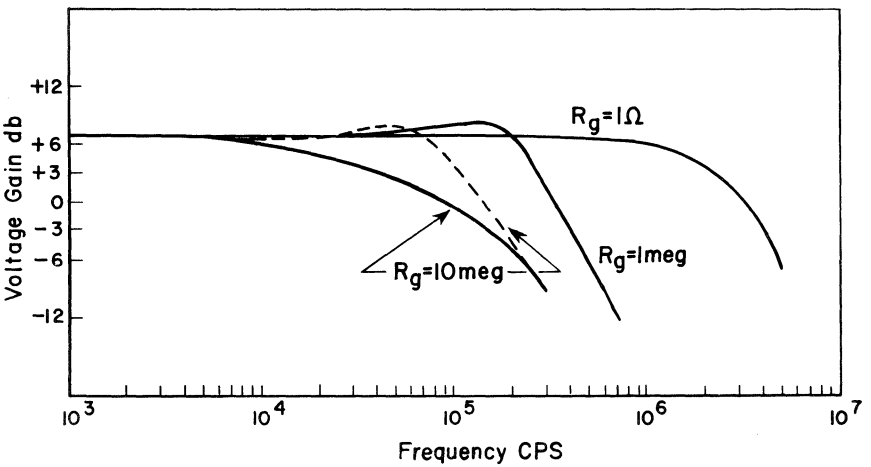


Fig. 21a. FET amplifier response curves.

CONCLUSIONS

The concepts of current multiplication and bootstrapping that have been defined and illustrated are those most widely used in high impedance circuits. The shunt positive feedback method, which has also been illustrated, has the advantage that very good stability factors can be obtained. Although the circuits presented exhibit relatively moderate input impedances, extension of the techniques involved can yield extremely high input impedances. Since all of these techniques involve feedback, it is well to do careful a-c and d-c stability analyses on any such circuit before adopting the design. In such analyses, the bias and temperature dependence of transistor parameters should be considered. A detailed treatment of such topics is too lengthy to include here; excellent treatments can be found in the literature. Some of these techniques can be extended to d-c amplifiers, but this subject is also a field in itself and will not be covered here.

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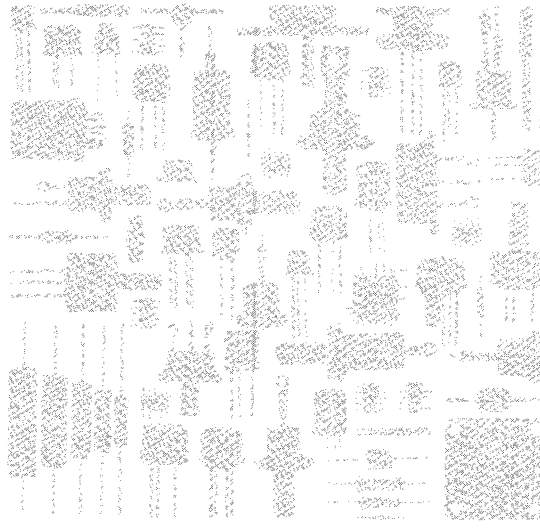

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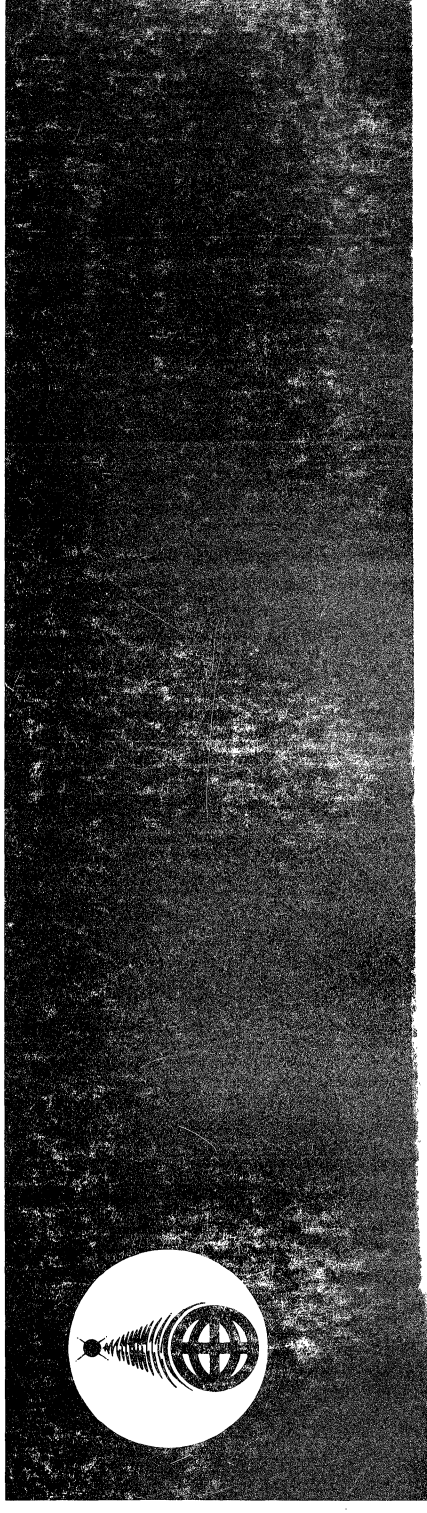

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