Total Access 1500
System Release 3.1
Release Notes

Module	Description	Firmware Issue
1180008L1	TA 1500 SCU	V10
1180008L2	TA 1500 SCU COT w/MLT	V10
1180008L3	TA 1500 SCU RT w/MLT	V10
1180008L22	TA 1500 SCU COT w/VF Test Access	V10
1180008L23	TA 1500 SCU RT, w/VF Test Access	V10
1180009L1	TA 1500 Dual LIU	T10
1180109L1	TA 1500 Quad LIU	T10
1180109L2	TA 1500 Quad LIU, L2 (Mode II)	T10

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Revision History

The history of this document is as follows:

Revision	Release Date	Initiator/Title	Description
A	December 2005	Wayne Cranford Product Manager	This is the initial issue of this document

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1. OVERVIEW

This document provides information relating to changes made to Total Access 1500 System components for System Release 3.1.

System Release 3.1 consists of software changes to the System Control Units (SCUs), Dual Line Interface (Dual LIU), and Quad Line Interface Units (Q-LIUs). The software can be uploaded in the field by using the local craftport on the SCU, or using TFTP. This software was developed to be used by all existing hardware, and from any previous software.

The SCU software is intended to be uploaded to all Total Access 1500 SCUs. The software for the Quad LIU is intended to be uploaded to both versions of Quad LIU.

Software enhancements of modules are detailed in *Software Changes by Module*, beginning on page 1-3.

While not released to production, some customer had previously upgraded the SCU to V08, Dual LIU to T07, and/or the Quad LIU to T09. We recommend upgrading all of these systems to this System Release. Items addressed specifically from the interim software are noted in the following applicable sections.

2. Software Changes By Modules

The following sections provide detailed information regarding feature enhancements, and fixes for each of the above listed components:

2.1 System Control Units (Software V10, checksum 8B50)

1180008L1
1180008L2
1180008L3
1180008L22
1180008L23

General

- Incorporated a change such that when an 1180008L22 or 1180008L23, is deployed with a L2 Q-LIU (1180109L2), the SCU only provides Primary/Secondary Power Alarms when deployed in the 19-inch chassis (1180019L1).
- Add support for Y-Modem uploads over the RS-485.
  Previously the TA 1500 only supported remote upgrade using TFTP. This added feature allows download from either a Host TA 1500 SCU, or another ADTRAN units (TA 3000, OP-6100). Download time estimates for Y-Modem can be between 19 to 25 minutes, based on the activity of the RS-485 bus.
  This change may require increasing the timeout of the TFTP server, as there will be additional delay between receipt of the 1st block of data while the erase function is performed.
- Added support for the Total Access 1500 19-inch Chassis when deployed with List 2 Quad LIU (1180109L2). See Figure 4.
  Previous SCU/LIU software would operate properly in the 19-inch Chassis but would display all 24 Access Modules slots. Requires List 2 Quad LIU with software T09Q or later to work properly.
- Incorporated a change to insure Host SCU will update a new client shelf with the time and date stamp.

Menus

- Modified menu header to display the TID field in Top line on the left-hand corner of the screen. The “Slot” field was moved to the 2nd line in the left-hand corner, replacing “Active Alarms:” nomenclature. Alarm notification remains on the 2nd line in the center of the screen. See Figure 1. This change will allow remote user to have the TID always present on the screen, whether locally or remotely logged in.
- Incorporated change to the SCU Management Configuration Menu whether the Ethernet Link is either "Up" or "Down". See Figure 2.
- Incorporated a change to the TFTP Application Menu to add, “Reset the TA1500 Commons” as a menu option. See Figure 3.
- Incorporated a change to the Restore Factory Default menu to challenge with a “Setting this item will affect service” notice and require the user to select either “Yes” or ”No”.

- Incorporated support for NMA logging channel.
  This new feature allows an active user with TL1 Logging privileges to receive TL1 commands

and responses for all active TL1 sessions, including autonomous alarms. Additionally, the User Name and Password will sent logged for those local or remote Menu users. Privileges are established in the Security/User Information menu. See Figure 5.

SMNP

- Added SNMP Support for SCU LED status.

TL1

- Modified TL1 response to RTRV-USER-SECU to return the ASCII character instead of the hex value.
- Incorporated a one-hour inactivity timer for TL1 sessions to Client shelves over the RS-485. Previously the TCP/IP Inactivity Timer in the SCU Management Menu would timeout any TL1 session to the Host or Client shelves. However, unless the user terminated the TL1 session to the Client, the Client would maintain that TL1 session. This TL1 Inactivity timer is not user selectable, and is independent of whether the TL1 session is via TCP/IP or X.25 to the Host shelf.

Fixes

- Modified Y-Modem download to erase SCU or LIU flash after receiving a valid Y-Modem file header.
  Previously the SCU would erase the Application Flash code, and if a file were never sent – a reset of the SCU would result in the SCU or LIU powering up in a Boot Mode.
- Modified local and remote TFTP upload to erase the flash following receipt of the first good block.
  Previously the SCU and LIU would erase Application Flash code before the file transfer was initiated. If a file were never sent, (wrong file name or TFTP server Location) a reset of the SCU or LIU would result in the units to power-up in a Boot Mode.
- Incorporated a change where a RS485 client will be rediscovered following a loss of the physical connection. While not expected to be a field-related issue, this change could help in lab or otherwise temporary installations where the user has not wire-wrapped the RS-485.
- Incorporated change such that a corrupted auto logoff menu would provide an “error”, allowing the user to select either enable or disabled.
  During software upgrade in a lab environment, it was noted on one occasion that the Auto Logoff selection in the SCU Provisioning Menu was not present.
- Implemented a change where the 4W ETO was not always properly recognized in the menu.
- Implemented a change where the SCU would update the LIU provisioning items following a failover, when the LIUs are at different software revision.
  Previously, the SCU would not download the provisioning information of the Online LIU to the Offline LIU prior to performing the failover, if the LIU software were not the same.
- Implemented a change to the TCP/IP Inactivity Timer. Sessions would timeout immediately for some back-to-back connections as well as with Tollgrade’s Loopcare OSS.
- Implemented a change so 1180008L22 and 1180008L23, SCU with Voice Frequency Test Access would send the correct Signaling States to the Dual FXO/TO (1180207L4) and Dual FXO GT (1180215L2). Previously the Test Access feature would not work properly with the Access Modules. ***(Updated since V08)***

2.2 Dual Line Interface Unit (Software T10, checksum BF53) 1180009L1

ALARMS

- Implemented a change to disabled the External Clock OOS alarms in the SCU Alarm menu by default.

GENERAL

- Incorporated a Mode in Dual T1 where DS0 assignment for a 2B+D U-BR1TE will be automatically mapped in tri-slot arrangement, following the same guidelines of an SLC-96 or SLC-5.
  In D4 counting (See Table 6):
  Slots 1, 4, 7, 10, 13, 16, 19, 22, the LIU will automatically assign the two DS0s of the physical slot, along with the odd DS0 from the adjacent physical slot immediately to the right. This is dependent on adjacent slot being unoccupied, or containing a 2B+D U-BR1TE. Example: a 2B+D U-BR1TE in Slot 1 would be assigned DS0-1, DS0-2, and DS-3 from T1-A.
  Slots 2, 5, 8, 11, 14, 17, 20, and 23, the LIU will automatically assign for a 2B+D U-BR1TE the even DS0 from that physical slot, along with the two DS0s from the adjacent physical slot immediately to the right. This is dependent on the adjacent slot being unoccupied. Example, a U-BR1TE in Slot 5 would be assigned DS0-10, DS0-11, and DS0-12 from T1 A.
  In slots 3, 6, 9, 12, 15, 18, 21 and 24, a 2B+D U-BR1TE will not be automatically assigned DS0s.

SNMP

- Added support for retrieving signal bits via SNMP
- Added support for retrieving LIU status LED via SNMP
- Added support for retrieving Access Module LED status via SNMP.
- Added SNMP support to Enable/Disable T1 select.
- Add SNMP support for "Manufactured By" and "Date of Manufacture". This will only be available on those access modules with this capability to be displayed.

FIXES

- Removed Signaling Bits from the Status Screen of the 4W TO.
- Implemented a change for the 2nd port of the Dual FXS GT to display the signaling bits in the Status Menu.
- Implemented a change to FXS and FXS GT LEDs such that exiting a test while provisioned for TO (ETO) mode would allow the LEDs return to the proper state. Previously, when exiting a test the Status LED would go from Amber to off, instead of Green. (Fixed in R36)
- Implemented a change to the 1004Hz Test Tone on 2-wire analog access modules that disables the analog-to-digital path when sending a 1004 Hz towards the loop. Previously the 1004Hz tone was also received in T1 DS0 about -23 dB. This was due to reflection from the access Modules.
- Implemented a change to insure the SCU could reliably read which LIU was Online, and which was Offline. In a lab environment it was noted on several occasions LIU-A would not operate as the Online LIU.
- Implemented a change on the Dual LIU to allow for Manual Timeslot assignment by T1-B.
- Implemented a change to correct a problem with the tone generation of the LIU. Previously the LIU could corrupt the 1004Hz, Ringback and other tones generate by the LIU for use within the system. This intermittent anomaly was not service affecting however the 1004Hz Menu Tests would not operate properly. ***(Updated since T07)***

KNOWN ERRATA

- A range of DS0 cannot be manual mapped for the Total Access 1500 Fractional T1 Dataport (P/N 1180405L1).
  Work Around – manual map each DS0

2.3 Quad Line Interface Unit (Software T10, checksum 48D7)

1180109L1
1180109L2

ALARMS

- Implemented a change to disabled the External Clock OOS alarms in the SCU Alarm menu by default.
- Implemented a change for the PHTL and ATB alarms to be assigned the appropriate T1 for the List 2 Q-LIU (P/N 1180109L2). PHTL or ATB are specific to SLC Mode II operation. Previously the AID in the TL1 report for these alarms used a "0" instead of a "1" or "2", indicating the specific T1 with this alarm condition.

GENERAL

- Incorporated a Mode in Dual T1 where DS0 assignment for a 2B+D U-BR1TE will be automatically mapped in tri-slot arrangement, following the same guidelines of an SLC-96 or SLC-5.
  In D4 counting (See Table 6):
  Slots 1, 4, 7, 10, 13, 16, 19, 22, the LIU will automatically assign the two DS0s of the physical slot, along with the odd DS0 from the adjacent physical slot immediately to the right. This is dependent on adjacent slot being unoccupied, or containing a 2B+D U-BR1TE. Example: a 2B+D U-BR1TE in Slot 1 would be assigned DS0-1, DS0-2, and DS-3 from T1-A.
  Slots 2, 5, 8, 11, 14, 17, 20, and 23, the LIU will automatically assign for a 2B+D U-BR1TE the even DS0 from that physical slot, along with the two DS0s from the adjacent physical slot immediately to the right. This is dependent on the adjacent slot being unoccupied. Example, a U-BR1TE in Slot 5 would be assigned DS0-10, DS0-11, and DS0-12 from T1 A.
  In slots 3, 6, 9, 12, 15, 18, 21 and 24, a 2B+D U-BR1TE will not be automatically assigned DS0s.

- Incorporated a "DLC" counting sequence to the Quad LIU Bank Provisioning menu when the Quad LIU is provisioned for Quad T1 Bank Mode.
  When selected, the LIU will automatically assign the DS0s such that all DS0 from a T1 will appear on the 50-pin amphenol connectors on the rear of the chassis. T1-A will appear on P1 (T/R), T1-B will appear on P2 (T1/R1), T1-C will appear on P3 (E/SG), and T1-D will appear on P4 (M/SB). Tables1-7 provides the T1/DS0 timeslot and amphenol connector information.

MENUS

- Added support for the 19-inch chassis in List 2 Quad LIU (1180109L2).
  Previously the LIU would not detect a 19-inch chassis and would display all 24 Access Modules slots. Requires upgraded SCU software V08 or later to work properly. See Figure 5.
- Fixed PHTL alignment in the Alarm Menu of the List 2 Quad LIU (P/N 1180109L2). This selection only appears in the menu when the LIU is provisioned for SLC-96 Mode II.

SNMP

- Added support for retrieving signal bits via SNMP
- Added support for retrieving LIU status LED via SNMP
- Added support for retrieving Access Module LED status via SNMP.
- Added SNMP support to Enable/Disable T1 select.
- Add SNMP support for "Manufactured By" and "Date of Manufacture". This will only be available on those access modules with this capability to be displayed.

FIXES

- Removed Signaling Bits from the Status Screen of the 4W TO.
- Implemented a change for the 2nd port of the Dual FXS GT to display the signaling bits in the Status Menu.
- Implemented a change to FXS and FXS GT LEDs such that exiting a test while provisioned for TO (ETO) mode would allow the LEDs return to the proper state. Previously, when exiting a test the Status LED would go from Amber to off, instead of Green. (Fixed in R36)
- Implemented a change to the 1004Hz Test Tone on 2-wire analog access modules that disables the analog-to-digital path when sending a 1004 Hz towards the loop. Previously the 1004Hz tone was also received in T1 DS0 about -23 dB. This was due to reflection from the access Modules.
- Implemented a change to insure the SCU could reliably read which LIU was Online, and which was Offline. In a lab environment it was noted on several occasions LIU-A would not operate as the Online LIU.
- Implemented a change to correct a problem with the tone generation of the LIU. Previously the LIU could corrupt the 1004Hz, Ringback and other tones generate by the LIU for use within the system. This intermittent anomaly was not service affecting however the 1004Hz Menu Tests would not operate properly and MLT test would not function. ***(Updated since T09)***

KNOWN ERRATA

- A range of DS0 cannot be manual mapped for the Total Access 1500 Fractional T1 Dataport (P/N 1180405L1).
  Work Around – manual map each DS0

```
TID: HTVLALEX0101          TOTAL ACCESS SYSTEM 1500            01/01/05 20:16
Slot: SCU                       Major    Minor




                              TA1500 Main Menu

                            1.  System Controller
                            2.  Online LIU  - [LIU A]
                            3.  Offline LIU - [.....]
                            4.  Access Modules
                            5.  Alarm Log
                            6.  Logoff




                                  Selection:



                           '?' - System Help Screen
```

Figure 1. TID and Shelf/Slot information

```
TID: HTVLALEX0101          TOTAL ACCESS SYSTEM 1500            01/01/05 20:17
Slot: SCU                       Major    Minor




                             Management Configuration

                    1.  IP Address
                    2.  IP Subnet Mask
                    3.  IP Default Gateway
                    4.  TELNET Port Number           2000
                    5.  TCP/IP Port Number           2001
                    6.  TCP/IP Inactivity Timeout    30 min
                    7.  SNMP Configuration
                        Ethernet Link                Down


                                  Selection:



                           '?' - System Help Screen
```

Figure 2. Ethernet Link Status

```
TID: HTVLALEX0101          TOTAL ACCESS SYSTEM 1500            01/01/05 20:18
Slot: SCU                       Major    Minor



                          TFTP Application

        1.  TFTP Upload Destination         SCU
        2.  TFTP Host IP Address
        3.  SCU Application Filename
        4.  LIU Application Filename
        5.  Start TFTP Upload
        6.  Modify Checksum                 6D26
        7.  Compute Checksum and Store
        8.  Reset the TFTP Destination
        9.  Reset the TA1500 Commons


                               Selection:


                         '?' - System Help Screen
```

Figure 3. Reset TA 1500 Commons Addition

```
TID: HTVLALEX0101          TOTAL ACCESS SYSTEM 1500            01/01/05 20:19
Slot: SCU                       Major    Minor


                               Access Modules

           1.  Quad R-POTS                  10.  ....................
           2.  DS0DP                        11.  ....................
           3.  ....................         12.  ....................
           4.  ....................         13.  ....................
           5.  ....................         14.  ....................
           6.  ....................         15.  ....................
           7.  ....................         16.  ....................
           8.  ....................         17.  ....................
           9.  ....................         18.  ....................




                               Selection:


                         '?' - System Help Screen
```

Figure 4. 19-Inch Chassis Access Module Menu with L2 Q-LIU

```
TID: HTVLALEX0101          TOTAL ACCESS SYSTEM 1500           01/01/05 20:20
Slot: SCU                       Major    Minor




                                User Information

                          1.  User Name            USER
                          2.  Password             ********
                          3.  R/W                  Read/Write
                          4.  Test                 Enabled
                          5.  Admin                Enabled
                          6.  TL1 Logging          Enabled
                          7.  Delete this User




                                 Selection:



                              '?' - System Help Screen
```

Figure 5. TL1 Logging Privilege

```
TID: HTVLALEX0101          TOTAL ACCESS SYSTEM 1500           01/01/05 20:20
Slot: Online LIU                Major    Minor
                          LIU Time Slot Assignment by Card
Card Card                                Card Card
Slot Name                                Slot Name
--------------------------------------+----------------------------------------
 1.  Quad R-POTS      A01 --- --- --- |10.
 2.  DS0DP            A02 N/A N/A N/A |11.
 3.                                   |12.
 4.                                   |13.
 5.                                   |14.
 6.                                   |15.
 7.                                   |16.
 8.                                   |17.
 9.                                   |18.



--------------------------------------+----------------------------------------

                               Select Card (1..18):


                              '?' - System Help Screen
```

Figure 6. 19-Inch Chassis Access Module Menu with L2 Q-LIU

Table 1. Automatic Time Slot Assignment and Wiring Interconnect for Quad C & R-POTS

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23- Inch Chassis	19- Inch Chassis	
1	1	A1	A1	A1	A1	P1 - 26/1	P1 - 26/1	T/R
	2	A2	A2	A3	B1	P2 - 26/1	P1 - 27/2	T/R
	3	N/A	A3	A5	C1	P3 - 26/1	P1 - 28/3	T/R
	4	N/A	A4	A7	D1	P4 - 26/1	P1 - 29/4	T/R
2	1	A5	A5	A9	A2	P1 - 27/2	P1 - 30/5	T/R
	2	A6	A6	A11	B2	P2 - 27/2	P1 - 31/6	T/R
	3	N/A	A7	A13	C2	P3 - 27/2	P1 - 32/7	T/R
	4	N/A	A8	A15	D2	P4 - 27/2	P1 - 33/8	T/R
3	1	A9	A9	A17	A3	P1 - 28/3	P1 - 34/9	T/R
	2	A10	A10	A19	B3	P2 - 28/3	P1 - 35/10	T/R
	3	N/A	A11	A21	C3	P3 - 28/3	P1 - 36/11	T/R
	4	N/A	A12	A23	D3	P4 - 28/3	P1 - 37/12	T/R
4	1	A13	A13	A2	A4	P1 - 29/4	P1 - 38/13	T/R
	2	A14	A14	A4	B4	P2 - 29/4	P1 - 39/14	T/R
	3	N/A	A15	A6	C4	P3 - 29/4	P1 - 40/15	T/R
	4	N/A	A16	A8	D4	P4 - 29/4	P1 - 41/16	T/R
5	1	A17	A17	A10	A5	P1 - 30/5	P1 - 42/17	T/R
	2	A18	A18	A12	B5	P2 - 30/5	P1 - 43/18	T/R
	3	N/A	A19	A14	C5	P3 - 30/5	P1 - 44/19	T/R
	4	N/A	A20	A16	D5	P4 - 30/5	P1 - 45/20	T/R
6	1	A21	A21	A18	A6	P1 - 31/6	P1 - 46/21	T/R
	2	A22	A22	A20	B6	P2 - 31/6	P1 - 47/22	T/R
	3	N/A	A23	A22	C6	P3 - 31/6	P1 - 48/23	T/R
	4	N/A	A24	A24	D6	P4 - 31/6	P1 - 49/24	T/R
7	1	B1	B1	B1	A7	P1 - 32/7	P2 - 26/1	T/R
	2	B2	B2	B3	B7	P2 - 32/7	P2 - 27/2	T/R
	3	N/A	B3	B5	C7	P3 - 32/7	P2 - 28/3	T/R
	4	N/A	B4	B7	D7	P4 - 32/7	P2 - 29/4	T/R
8	1	B5	B5	B9	A8	P1 - 33/8	P2 - 30/5	T/R
	2	B6	B6	B11	B8	P2 - 33/8	P2 - 31/6	T/R
	3	N/A	B7	B13	C8	P3 - 33/8	P2 - 32/7	T/R
	4	N/A	B8	B15	D8	P4 - 33/8	P2 - 33/8	T/R
9	1	B9	B9	B17	A9	P1 - 34/9	P2 - 34/9	T/R
	2	B10	B10	B19	B9	P2 - 34/9	P2 - 35/10	T/R
	3	N/A	B11	B21	C9	P3 - 34/9	P2 - 36/11	T/R
	4	N/A	B12	B23	D9	P4 - 34/9	P2 - 37/12	T/R
10	1	B13	B13	B2	A10	P1 - 35/10	P2 - 38/13	T/R
	2	B14	B14	B4	B10	P2 - 35/10	P2 - 39/14	T/R
	3	N/A	B15	B6	C10	P3 - 35/10	P2 - 40/15	T/R
	4	N/A	B16	B8	D10	P4 - 35/10	P2 - 41/16	T/R
11	1	B17	B17	B10	A11	P1 - 36/11	P2 - 42/17	T/R
	2	B18	B18	B12	B11	P2 - 36/11	P2 - 43/18	T/R
	3	N/A	B19	B14	C11	P3 - 36/11	P2 - 44/19	T/R
	4	N/A	B20	B16	D11	P4 - 36/11	P2 - 45/20	T/R

Table 1. (continued) Automatic Time Slot Assignment and Wiring Interconnect for Quad C and R-POTS

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23- Inch Chassis	19- Inch Chassis	
12	1	B21	B21	B18	A12	P1 - 37/12	P2 - 46/21	T/R
	2	B22	B22	B20	B12	P2 - 37/12	P2 - 47/22	T/R
	3	N/A	B23	B22	C12	P3 - 37/12	P2 - 48/23	T/R
	4	N/A	B24	B24	D12	P4 - 37/12	P2 - 49/24	T/R
13	1	C1	C1	C1	A13	P1 - 38/13	P3 - 26/1	T/R
	2	C2	C2	C3	B13	P2 - 38/13	P3 - 27/2	T/R
	3	N/A	C3	C5	C13	P3 - 38/13	P3 - 28/3	T/R
	4	N/A	C4	C7	D13	P4 - 38/13	P3 - 29/4	T/R
14	1	C5	C5	C9	A14	P1 - 39/14	P3 - 30/5	T/R
	2	C6	C6	C11	B14	P2 - 39/14	P3 - 31/6	T/R
	3	N/A	C7	C13	C14	P3 - 39/14	P3 - 32/7	T/R
	4	N/A	C8	C15	D14	P4 - 39/14	P3 - 33/8	T/R
15	1	C9	C9	C17	A15	P1 - 40/15	P3 - 34/9	T/R
	2	C10	C10	C19	B15	P2 - 40/15	P3 - 35/10	T/R
	3	N/A	C11	C21	C15	P3 - 40/15	P3 - 36/11	T/R
	4	N/A	C12	C23	D15	P4 - 40/15	P3 - 37/12	T/R
16	1	C13	C13	C2	A16	P1 - 41/16	P3 - 38/13	T/R
	2	C14	C14	C4	B16	P2 - 41/16	P3 - 39/14	T/R
	3	N/A	C15	C6	C16	P3 - 41/16	P3 - 40/15	T/R
	4	N/A	C16	C8	D16	P4 - 41/16	P3 - 41/16	T/R
17	1	C17	C17	C10	A17	P1 - 42/17	P3 - 42/17	T/R
	2	C18	C18	C12	B17	P2 - 42/17	P3 - 43/18	T/R
	3	N/A	C19	C14	C17	P3 - 42/17	P3 - 44/19	T/R
	4	N/A	C20	C16	D17	P4 - 42/17	P3 - 45/20	T/R
18	1	C21	C21	C18	A18	P1 - 43/18	P3 - 46/21	T/R
	2	C22	C22	C20	B18	P2 - 43/18	P3 - 47/22	T/R
	3	N/A	C23	C22	C18	P3 - 43/18	P3 - 48/23	T/R
	4	N/A	C24	C24	D18	P4 - 43/18	P3 - 49/24	T/R
19	1	D1	D1	D1	A19	P1 - 44/19	N/A	T/R
	2	D2	D2	D3	B19	P2 - 44/19	N/A	T/R
	3	N/A	D3	D5	C19	P3 - 44/19	N/A	T/R
	4	N/A	D4	D7	D19	P4 - 44/19	N/A	T/R
20	1	D5	D5	D9	A20	P1 - 45/20	N/A	T/R
	2	D6	D6	D11	B20	P2 - 45/20	N/A	T/R
	3	N/A	D7	D13	C20	P3 - 45/20	N/A	T/R
	4	N/A	D8	D15	D20	P4 - 45/20	N/A	T/R
21	1	D9	D9	D17	A21	P1 - 46/21	N/A	T/R
	2	D10	D10	D19	B21	P2 - 46/21	N/A	T/R
	3	N/A	D11	D21	C21	P3 - 46/21	N/A	T/R
	4	N/A	D12	D23	D21	P4 - 46/21	N/A	T/R
22	1	D13	D13	D2	A22	P1 - 47/22	N/A	T/R
	2	D14	D14	D4	B22	P2 - 47/22	N/A	T/R
	3	N/A	D15	D6	C22	P3 - 47/22	N/A	T/R
	4	N/A	D16	D8	D22	P4 - 47/22	N/A	T/R

Table 1. (continued) Automatic Time Slot Assignment and Wiring Interconnect for Quad C and R-POTS

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23- Inch Chassis	19- Inch Chassis	
23	1	D17	D17	D10	A23	P1 - 48/23	N/A	T/R
	2	D18	D18	D12	B23	P2 - 48/23	N/A	T/R
	3	N/A	D19	D14	C23	P3 - 48/23	N/A	T/R
	4	N/A	D20	D16	D23	P4 - 48/23	N/A	T/R
24	1	D21	D21	D18	A24	P1 - 49/24	N/A	T/R
	2	D22	D22	D20	B24	P2 - 49/24	N/A	T/R
	3	N/A	D23	D22	C24	P3 - 49/24	N/A	T/R
	4	N/A	D24	D24	D24	P4 - 49/24	N/A	T/R

Table 2. Automatic Time Slot Assignment and Wiring Interconnect for Dual 4-wire Access Modules

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1 (D4)	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23-Inch Chassis	19-Inch Chassis	
1	1	A1	A1	A1	A1	P1 - 26/1	P1 - 26/1	T/R
						P2 - 26/1	P1 - 27/2	T1/R1
	2	A2	A2	A3	B1	P3 - 26/1	P1 - 28/3	T/R
						P4 - 26/1	P1 - 29/4	T1/R1
2	1	A3	A5	A9	A2	P1 - 27/2	P1 - 30/5	T/R
						P2 - 27/2	P1 - 31/6	T1/R1
	2	A4	A6	A11	B2	P3 - 27/2	P1 - 32/7	T/R
						P4 - 27/2	P1 - 33/8	T1/R1
3	1	A5	A9	A17	A3	P1 - 28/3	P1 - 34/9	T/R
						P2 - 28/3	P1 - 35/10	T1/R1
	2	A6	A10	A19	B3	P3 - 28/3	P1 - 36/11	T/R
						P4 - 28/3	P1 - 37/12	T1/R1
4	1	A7	A13	A2	A4	P1 - 29/4	P1 - 38/13	T/R
						P2 - 29/4	P1 - 39/14	T1/R1
	2	A8	A14	A4	B4	P3 - 29/4	P1 - 40/15	T/R
						P4 - 29/4	P1 - 41/16	T1/R1
5	1	A9	A17	A10	A5	P1 - 30/5	P1 - 42/17	T/R
						P2 - 30/5	P1 - 43/18	T1/R1
	2	A10	A18	A12	B5	P3 - 30/5	P1 - 44/19	T/R
						P4 - 30/5	P1 - 45/20	T1/R1
6	1	A11	A21	A18	A6	P1 - 31/6	P1 - 46/21	T/R
						P2 - 31/6	P1 - 47/22	T1/R1
	2	A12	A22	A20	B6	P3 - 31/6	P1 - 48/23	T/R
						P4 - 31/6	P1 - 49/24	T1/R1
7	1	A13	B1	B1	A7	P1 - 32/7	P2 - 26/1	T/R
						P2 - 32/7	P2 - 27/2	T1/R1
	2	A14	B2	B3	B7	P3 - 32/7	P2 - 28/3	T/R
						P4 - 32/7	P2 - 29/4	T1/R1
8	1	A15	B5	B9	A8	P1 - 33/8	P2 - 30/5	T/R
						P2 - 33/8	P2 - 31/6	T1/R1
	2	A16	B6	B11	B8	P3 - 33/8	P2 - 32/7	T/R
						P4 - 33/8	P2 - 33/8	T1/R1
9	1	A17	B9	B17	A9	P1 - 34/9	P2 - 34/9	T/R
						P2 - 34/9	P2 - 35/10	T1/R1
	2	A18	B10	B19	B9	P3 - 34/9	P2 - 36/11	T/R
						P4 - 34/9	P2 - 37/12	T1/R1
10	1	A19	B13	B2	A10	P1 - 35/10	P2 - 38/13	T/R
						P2 - 35/10	P2 - 39/14	T1/R1
	2	A20	B14	B4	B10	P3 - 35/10	P2 - 40/15	T/R
						P4 - 35/10	P2 - 41/16	T1/R1
11	1	A21	B17	B10	A11	P1 - 36/11	P2 - 42/17	T/R
						P2 - 36/11	P2 - 43/18	T1/R1
	2	A22	B18	B12	B11	P3 - 36/11	P2 - 44/19	T/R
						P4 - 36/11	P2 - 45/20	T1/R1

Table 2. (continued) Automatic Time Slot Assignment and Wiring Interconnect for Dual 4-wire Access Module

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1 (D4)	23-Inch Chassis	19-Inch Chassis	Quad T1 (DLC)	23-Inch Chassis	19Inch Chassis	
12	1	A23	B21	B18	A12	P1 - 37/12	P2 - 46/21	T/R
						P2 - 37/12	P2 - 47/22	T1/R1
	2	A24	B22	B20	B12	P3 - 37/12	P2 - 48/23	T/R
13	1	B1	C1	C1	A13	P1 - 38/13	P3 - 26/1	T/R
						P2 - 38/13	P3 - 27/2	T1/R1
	2	B2	C2	C3	B13	P3 - 38/13	P3 - 28/3	T/R
						P4 - 38/13	P3 - 29/4	T1/R1
14	1	B3	C5	C9	A14	P1 - 39/14	P3 - 30/5	T/R
						P2 - 39/14	P3 - 31/6	T1/R1
	2	B4	C6	C11	B14	P3 - 39/14	P3 - 32/7	T/R
						P4 - 39/14	P3 - 33/8	T1/R1
15	1	B5	C9	C17	A15	P1 - 40/15	P3 - 34/9	T/R
						P2 - 40/15	P3 - 35/10	T1/R1
	2	B6	C10	C19	B15	P3 - 40/15	P3 - 36/11	T/R
						P4 - 40/15	P3 - 37/12	T1/R1
16	1	B7	C13	C2	A16	P1 - 41/16	P3 - 38/13	T/R
						P2 - 41/16	P3 - 39/14	T1/R1
	2	B8	C14	C4	B16	P3 - 41/16	P3 - 40/15	T/R
						P4 - 41/16	P3 - 41/16	T1/R1
17	1	B9	C17	C10	A17	P1 - 42/17	P3 - 42/17	T/R
						P2 - 42/17	P3 - 43/18	T1/R1
	2	B10	C18	C12	B17	P3 - 42/17	P3 - 44/19	T/R
						P4 - 42/17	P3 - 45/20	T1/R1
18	1	B11	C21	C18	A18	P1 - 43/18	P3 - 46/21	T/R
						P2 - 43/18	P3 - 47/22	T1/R1
	2	B12	C22	C20	B18	P3 - 43/18	P3 - 48/23	T/R
						P4 - 43/18	P3 - 49/24	T1/R1
19	1	B13	D1	D1	A19	P1 - 44/19	N/A	T/R
						P2 - 44/19	N/A	T1/R1
	2	B14	D2	D3	B19	P3 - 44/19	N/A	T/R
						P4 - 44/19	N/A	T1/R1
20	1	B15	D5	D9	A20	P1 - 45/20	N/A	T/R
						P2 - 45/20	N/A	T1/R1
	2	B16	D6	D11	B20	P3 - 45/20	N/A	T/R
						P4 - 45/20	N/A	T1/R1
21	1	B17	D9	D17	A21	P1 - 46/21	N/A	T/R
						P2 - 46/21	N/A	T1/R1
	2	B18	D10	D19	B21	P3 - 46/21	N/A	T/R
						P4 - 46/21	N/A	T1/R1
22	1	B19	D13	D2	A22	P1 - 47/22	N/A	T/R
						P2 - 47/22	N/A	T1/R1
	2	B20	D14	D4	B22	P3 - 47/22	N/A	T/R
						P4 - 47/22	N/A	T1/R1

Table 2. (continued) Automatic Time Slot Assignment and Wiring Interconnect for Dual 4-wire Access Module

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23-Inch Chassis	19-Inch Chassis	
23	1	B21	D17	D10	A23	P1 - 48/23	N/A	T/R
						P2 - 48/23	N/A	T1/R1
	2	B22	D18	D12	B23	P3 - 48/23	N/A	T/R
						P4 - 48/23	N/A	T1/R1
24	1	B23	D21	D18	A24	P1 - 49/24	N/A	T/R
						P2 - 49/24	N/A	T1/R1
	2	B24	D22	D20	B24	P3 - 49/24	N/A	T/R
						P4 - 49/24	N/A	T1/R1

Table 3. Automatic Time Slot Assignment and Wiring Interconnect for Dual 2-wire Access Modules

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23-Inch Chassis	19-Inch Chassis	
1	1	A1	A1	A1	A1	P1 - 26/1	P1 - 26/1	T/R
	2	A2	A2	A3	B1	P3 - 26/1	P1 - 28/3	T/R
2	1	A5	A5	A9	A2	P1 - 27/2	P1 - 30/5	T/R
	2	A6	A6	A11	B2	P3 - 27/2	P1 - 32/7	T/R
3	1	A9	A9	A17	A3	P1 - 28/3	P1 - 34/9	T/R
	2	A10	A10	A19	B3	P3 - 28/3	P1 - 36/11	T/R
4	1	A13	A13	A2	A4	P1 - 29/4	P1 - 38/13	T/R
	2	A14	A14	A4	B4	P3 - 29/4	P1 - 40/15	T/R
5	1	A17	A17	A10	A5	P1 - 30/5	P1 - 42/17	T/R
	2	A18	A18	A12	B5	P3 - 30/5	P1 - 44/19	T/R
6	1	A21	A21	A18	A6	P1 - 31/6	P1 - 46/21	T/R
	2	A22	A22	A20	B6	P3 - 31/6	P1 - 48/23	T/R
7	1	B1	B1	B1	A7	P1 - 32/7	P2 - 26/1	T/R
	2	B2	B2	B3	B7	P3 - 32/7	P2 - 28/3	T/R
8	1	B5	B5	B9	A8	P1 - 33/8	P2 - 30/5	T/R
	2	B6	B6	B11	B8	P3 - 33/8	P2 - 32/7	T/R
9	1	B9	B9	B17	A9	P1 - 34/9	P2 - 34/9	T/R
	2	B10	B10	B19	B9	P3 - 34/9	P2 - 36/11	T/R
10	1	B13	B13	B2	A10	P1 - 35/10	P2 - 38/13	T/R
	2	B14	B14	B4	B10	P3 - 35/10	P2 - 40/15	T/R
11	1	B17	B17	B10	A11	P1 - 36/11	P2 - 42/17	T/R
	2	B18	B18	B12	B11	P3 - 36/11	P2 - 44/19	T/R
12	1	B21	B21	B18	A12	P1 - 37/12	P2 - 46/21	T/R
	2	B22	B22	B20	B12	P3 - 37/12	P2 - 48/23	T/R
13	1	C1	C1	C1	A13	P1 - 38/13	P3 - 26/1	T/R
	2	C2	C2	C3	B13	P3 - 38/13	P3 - 28/3	T/R
14	1	C5	C5	C9	A14	P1 - 39/14	P3 - 30/5	T/R
	2	C6	C6	C11	B14	P3 - 39/14	P3 - 32/7	T/R

Table 3. (continued) Automatic Time Slot Assignment and Wiring Interconnect for Dual 2-wire Access Modules

Physical Slot	Module Circuit	Associated T1/DS0				Connections		Interconnect Wiring
		Dual T1	Quad T1 (D4)	Interconnect Wiring	Quad T1 (DLC)	23-Inch Chassis	19-Inch Chassis	
15	1	C9	C9	C17	A15	P1 - 40/15	P3 - 34/9	T/R
	2	C10	C10	C19	B15	P3 - 40/15	P3 - 36/11	T/R
16	1	C13	C13	C2	A16	P1 - 41/16	P3 - 38/13	T/R
	2	C14	C14	C4	B16	P3 - 41/16	P3 - 40/15	T/R
17	1	C17	C17	C10	A17	P1 - 42/17	P3 - 42/17	T/R
	2	C18	C18	C12	B17	P3 - 42/17	P3 - 44/19	T/R
18	1	C21	C21	C18	A18	P1 - 43/18	P3 - 46/21	T/R
	2	C22	C22	C20	B18	P3 - 43/18	P3 - 48/23	T/R
19	1	D1	D1	D1	A19	P1 - 44/19	N/A	T/R
	2	D2	D2	D3	B19	P3 - 44/19	N/A	T/R
20	1	D5	D5	D9	A20	P1 - 45/20	N/A	T/R
	2	D6	D6	D11	B20	P3 - 45/20	N/A	T/R
21	1	D9	D9	D17	A21	P1 - 46/21	N/A	T/R
	2	D10	D10	D19	B21	P3 - 46/21	N/A	T/R
22	1	D13	D13	D2	A22	P1 - 47/22	N/A	T/R
	2	D14	D14	D4	B22	P3 - 47/22	N/A	T/R
23	1	D17	D17	D10	A23	P1 - 48/23	N/A	T/R
	2	D18	D18	D12	B23	P3 - 48/23	N/A	T/R
24	1	D21	D21	D18	A24	P1 - 49/24	N/A	T/R
	2	D22	D22	D20	B24	P3 - 49/24	N/A	T/R

Table 4. Automatic Time Slot Assignment and Wiring Interconnect for Single 4-wire Access Modules

Physical Slot	Associated T1/DS0				Connections		Interconnect Wiring
	Dual T1 (D4)	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23-Inch Chassis	19-Inch Chassis	
1	A1	A1	A1	A1	P1 - 26/1	P1 - 26/1	T/R
					P2 - 26/1	P1 - 27/2	T1/R1
2	A3	A5	A9	A2	P1 - 27/2	P1 - 30/5	T/R
					P2 - 27/2	P1 - 31/6	T1/R1
3	A5	A9	A17	A3	P1 - 28/3	P1 - 34/9	T/R
					P2 - 28/3	P1 - 35/10	T1/R1
4	A7	A13	A2	A4	P1 - 29/4	P1 - 38/13	T/R
					P2 - 29/4	P1 - 39/14	T1/R1
5	A9	A17	A10	A5	P1 - 30/5	P1 - 42/17	T/R
					P2 - 30/5	P1 - 43/18	T1/R1
6	A11	A21	A18	A6	P1 - 31/6	P1 - 46/21	T/R
					P2 - 31/6	P1 - 47/22	T1/R1
7	A13	B1	B1	A7	P1 - 32/7	P2 - 26/1	T/R
					P2 - 32/7	P2 - 27/2	T1/R1
8	A15	B5	B9	A8	P1 - 33/8	P2 - 30/5	T/R
					P2 - 33/8	P2 - 31/6	T1/R1
9	A17	B9	B17	A9	P1 - 34/9	P2 - 34/9	T/R
					P2 - 34/9	P2 - 35/10	T1/R1
10	A19	B13	B2	A10	P1 - 35/10	P2 - 38/13	T/R
					P2 - 35/10	P2 - 39/14	T1/R1
11	A21	B17	B10	A11	P1 - 36/11	P2 - 42/17	T/R
					P2 - 36/11	P2 - 43/18	T1/R1
12	A23	B21	B18	A12	P1 - 37/12	P2 - 46/21	T/R
					P2 - 37/12	P2 - 47/22	T1/R1
13	B1	C1	C1	A13	P1 - 38/13	P3 - 26/1	T/R
					P2 - 38/13	P3 - 27/2	T1/R1
14	B3	C5	C9	A14	P1 - 39/14	P3 - 30/5	T/R
					P2 - 39/14	P3 - 31/6	T1/R1
15	B5	C9	C17	A15	P1 - 40/15	P3 - 34/9	T/R
					P2 - 40/15	P3 - 35/10	T1/R1
16	B7	C13	C2	A16	P1 - 41/16	P3 - 38/13	T/R
					P2 - 41/16	P3 - 39/14	T1/R1
17	B9	C17	C10	A17	P1 - 42/17	P3 - 42/17	T/R
					P2 - 42/17	P3 - 43/18	T1/R1
18	B11	C21	C18	A18	P1 - 43/18	P3 - 46/21	T/R
					P2 - 43/18	P3 - 47/22	T1/R1
19	B13	D1	D1	A19	P1 - 44/19	N/A	T/R
					P2 - 44/19	N/A	T1/R1
20	B15	D5	D9	A20	P1 - 45/20	N/A	T/R
					P2 - 45/20	N/A	T1/R1
21	B17	D9	D17	A21	P1 - 46/21	N/A	T/R
					P2 - 46/21	N/A	T1/R1
22	B19	D13	D2	A22	P1 - 47/22	N/A	T/R
					P2 - 47/22	N/A	T1/R1

Table 4. (continued) Automatic Time Slot Assignment and Wiring Interconnect for Single 4-wire Access Modules

Physical Slot	Associated T1/DS0				Connections		Interconnect Wiring
	Dual T1 (D4)	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23-Inch Chassis	19-Inch Chassis	
23	B21	D17	D10	A23	P1 - 48/23	N/A	T/R
					P2 - 48/23	N/A	T1/R1
24	B23	D21	D18	A24	P1 - 49/24	N/A	T/R
					P2 - 49/24	N/A	T1/R1

Table 5. Automatic Time Slot Assignment and Wiring Interconnect for Single 2-wire and 1 DS0 ISDN Access Modules

Physical Slot	Associated T1/DS0				Connections		Interconnect Wiring
	Dual T1 (D4)	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)	23-Inch Chassis	19-Inch Chassis	
1	A1	A1	A1	A1	P1 - 26/1	P1 - 26/1	T/R
2	A3	A5	A9	A2	P1 - 27/2	P1 - 30/5	T/R
3	A5	A9	A17	A3	P1 - 28/3	P1 - 34/9	T/R
4	A7	A13	A2	A4	P1 - 29/4	P1 - 38/13	T/R
5	A9	A17	A10	A5	P1 - 30/5	P1 - 42/17	T/R
6	A11	A21	A18	A6	P1 - 31/6	P1 - 46/21	T/R
7	A13	B1	B1	A7	P1 - 32/7	P2 - 26/1	T/R
8	A15	B5	B9	A8	P1 - 33/8	P2 - 30/5	T/R
9	A17	B9	B17	A9	P1 - 34/9	P2 - 34/9	T/R
10	A19	B13	B2	A10	P1 - 35/10	P2 - 38/13	T/R
11	A21	B17	B10	A11	P1 - 36/11	P2 - 42/17	T/R
12	A23	B21	B18	A12	P1 - 37/12	P2 - 46/21	T/R
13	B1	C1	C1	A13	P1 - 38/13	P3 - 26/1	T/R
14	B3	C5	C9	A14	P1 - 39/14	P3 - 30/5	T/R
15	B5	C9	C17	A15	P1 - 40/15	P3 - 34/9	T/R
16	B7	C13	C2	A16	P1 - 41/16	P3 - 38/13	T/R
17	B9	C17	C10	A17	P1 - 42/17	P3 - 42/17	T/R
18	B11	C21	C18	A18	P1 - 43/18	P3 - 46/21	T/R
19	B13	D1	D1	A19	P1 - 44/19	N/A	T/R
20	B15	D5	D9	A20	P1 - 45/20	N/A	T/R
21	B17	D9	D17	A21	P1 - 46/21	N/A	T/R
22	B19	D13	D2	A22	P1 - 47/22	N/A	T/R
23	B21	D17	D10	A23	P1 - 48/23	N/A	T/R
24	B23	D21	D18	A24	P1 - 49/24	N/A	T/R

Table 6. Automatic Time Slot Assignment and Wiring Interconnect for 2B+D ISDN

Physical Slot	Associated T1/DS0					Connections		Interconnect Wiring
	Single T1 (D4)	Dual T1 (D4)	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC)[Note 1]	23-Inch Chassis	19-Inch Chassis	
1	A1, A2, A3	A1, A2, A3	A1, A2, A3	A1, A3, A5	A1, B1, C1	P1 - 26/1	P1 - 26/1	T/R
2	Blank	A4, A5, A6	A5, A6, A7	A9, A11, A13	A2, B2, C2	P1 - 27/2	P1 - 30/5	T/R
3	Blank	Blank	A9, A10, A11	A17, A19, A21	A3, B3, C3	P1 - 28/3	P1 - 34/9	T/R
4	A4, A5, A6	A7, A8, A9	A13, A14, A15	A2, A4, A6	A4, B4, C4	P1 - 29/4	P1 - 38/13	T/R
5	Blank	A10, A11, A12	A17, A18, A19	A10, A12, A14	A5, B5, C5	P1 - 30/5	P1 - 42/17	T/R
6	Blank	Blank	A21, A22, A23	A18, A20, A22	A6, B6, C6	P1 - 31/6	P1 - 46/21	T/R
7	A7, A8, A9	A13, A14, A15	B1, B2, B3	B1, B3, B5	A7, B7, C7	P1 - 32/7	P2 - 26/1	T/R
8	Blank	A16, A17, A18	B5, B6, B7	B9, B11, B13	A8, B8, C8	P1 - 33/8	P2 - 30/5	T/R
9	Blank	Blank	B9, B10, B11	B17, B19, B21	A9, B9, C9	P1 - 34/9	P2 - 34/9	T/R
10	A10, A11, A12	A19, A20, A21	B13, B14, B15	B2, B4, B6	A10, B10, C10	P1 - 35/10	P2 - 38/13	T/R
11	Blank	A22, A23, A24	B17, B18, B19	B10, B12, B14	A11, B11, C11	P1 - 36/11	P2 - 42/17	T/R
12	Blank	Blank	B21, B22, B23	B18, B20, B22	A12, B12, C12	P1 - 37/12	P2 - 46/21	T/R
13	A13, A14, A15	B1, B2, B3	C1, C2, C3	C1, C3, C5	A13, B13, C13	P1 - 38/13	P3 - 26/1	T/R
14	Blank	B4, B5, B6	C5, C6, C7	C9, C11, C13	A14, B14, C14	P1 - 39/14	P3 - 30/5	T/R
15	Blank	Blank	C9, C10, C11	C17, C19, C21	A15, B15, C15	P1 - 40/15	P3 - 34/9	T/R
16	A16, A17, A18	B7, B8, B9	C13, C14, C15	C2, C4, C6	A16, B16, C16	P1 - 41/16	P3 - 38/13	T/R
17	Blank	B10, B11, B12	C17, C18, C19	C10, C12, C14	A17, B17, C17	P1 - 42/17	P3 - 42/17	T/R
18	Blank	Blank	C21, C22, C23	C18, C20, C22	A18, B18, C18	P1 - 43/18	P3 - 46/21	T/R
19	A19, A20, A21	B13, B14, B15	D1, D2, D3	D1, D3, D5	A19, B19, C19	P1 - 44/19	N/A	T/R
20	Blank	B16, B17, B18	D5, D6, D7	D9, D11, D13	A20, B20, C20	P1 - 45/20	N/A	T/R
21	Blank	Blank	D9, D10, D11	D17, D19, D21	A21, B21, C21	P1 - 46/21	N/A	T/R
22	A22, A23, A24	B19, B20, B21	D13, D14, D15	D2, D4, D6	A22, B22, C22	P1 - 47/22	N/A	T/R
23	Blank	B22, B23, B24	D17, D18, D19	D10, D12, D14	A23, B23, C23	P1 - 48/23	N/A	T/R
24	Blank	Blank	D21, D22, D23	D18, D20, D22	A24, B24, C24	P1 - 49/24	N/A	T/R

Note 1: Automatic mapping of 2B+D ISDN is not recommended for Quad T1/DLC counting modes. All 3 DS0s intended for ISDN applications should be mapped to the same T1.

Table 7. Automatic Time Slot Assignment and Wiring Interconnect for 2B, or 1B+D ISDN

Physical Slot	Associated T1/DS0				Connections		Interconnect Wiring
	Dual T1 (D4)	Quad T1 (D4)	Quad T1 (DID)	Quad T1 (DLC) Note 1	23-Inch Chassis	19-Inch Chassis	
1	A1, A2	A1, A2	A1, A3	A1, B1	P1 - 26/1	P1 - 26/1	T/R
2	A3, A4	A5, A6	A9, A11	A2, B2	P1 - 27/2	P1 - 30/5	T/R
3	A5, A6	A9, A10	A17, A19	A3, B3	P1 - 28/3	P1 - 34/9	T/R
4	A7, A8	A13, A14	A2, A4	A4, B4	P1 - 29/4	P1 - 38/13	T/R
5	A9, A10	A17, A18	A10, A12	A5, B5	P1 - 30/5	P1 - 42/17	T/R
6	A11, A12	A21, A22	A18, A20	A6, B6	P1 - 31/6	P1 - 46/21	T/R
7	A13, A14	B1, B2	B1, B3	A7, B7	P1 - 32/7	P2 - 26/1	T/R
8	A15, A16	B5, B6	B9, B11	A8, B8	P1 - 33/8	P2 - 30/5	T/R
9	A17, A18	B9, B10	B17, B19	A9, B9	P1 - 34/9	P2 - 34/9	T/R
10	A19, A20	B13, B14	B2, B4	A10, B10	P1 - 35/10	P2 - 38/13	T/R
11	A21, A22	B17, B18	B10, B12	A11, B11	P1 - 36/11	P2 - 42/17	T/R
12	A23, A24	B21, B22	B18, B20	A12, B12	P1 - 37/12	P2 - 46/21	T/R
13	B1, B2	C1, C2	C1, C3	A13, B13	P1 - 38/13	P3 - 26/1	T/R
14	B3, B4	C5, C6	C9, C11	A14, B14	P1 - 39/14	P3 - 30/5	T/R
15	B5, B6	C9, C10	C17, C19	A15, B15	P1 - 40/15	P3 - 34/9	T/R
16	B7, B8	C13, C14	C2, C4	A16, B16	P1 - 41/16	P3 - 38/13	T/R
17	B9, B10	C17, C18	C10, C12	A17, B17	P1 - 42/17	P3 - 42/17	T/R
18	B11, B12	C21, C22	C18, C20	A18, B18	P1 - 43/18	P3 - 46/21	T/R
19	B13, B14	D1, D2	D1, D3	A19, B19	P1 - 44/19	N/A	T/R
20	B15, B16	D5, D6	D9, D11	A20, B20	P1 - 45/20	N/A	T/R
21	B17, B18	D9, D10	D17, D19	A21, B21	P1 - 46/21	N/A	T/R
22	B19, B20	D13, D14	D2, D4	A22, B22	P1 - 47/22	N/A	T/R
23	B21, B22	D17, D18	D10, D12	A23, B23	P1 - 48/23	N/A	T/R
24	B23, B24	D21, D22	D18, D20	A24, B24	P1 - 49/24	N/A	T/R

Note 1:Automatic mapping of 1B+D ISDN is not recommended for Quad T1/DLC counting modes. Both DS0s intended for ISDN applications should be mapped to the same T1. Automatic mapping of 2B ISDN will work properly