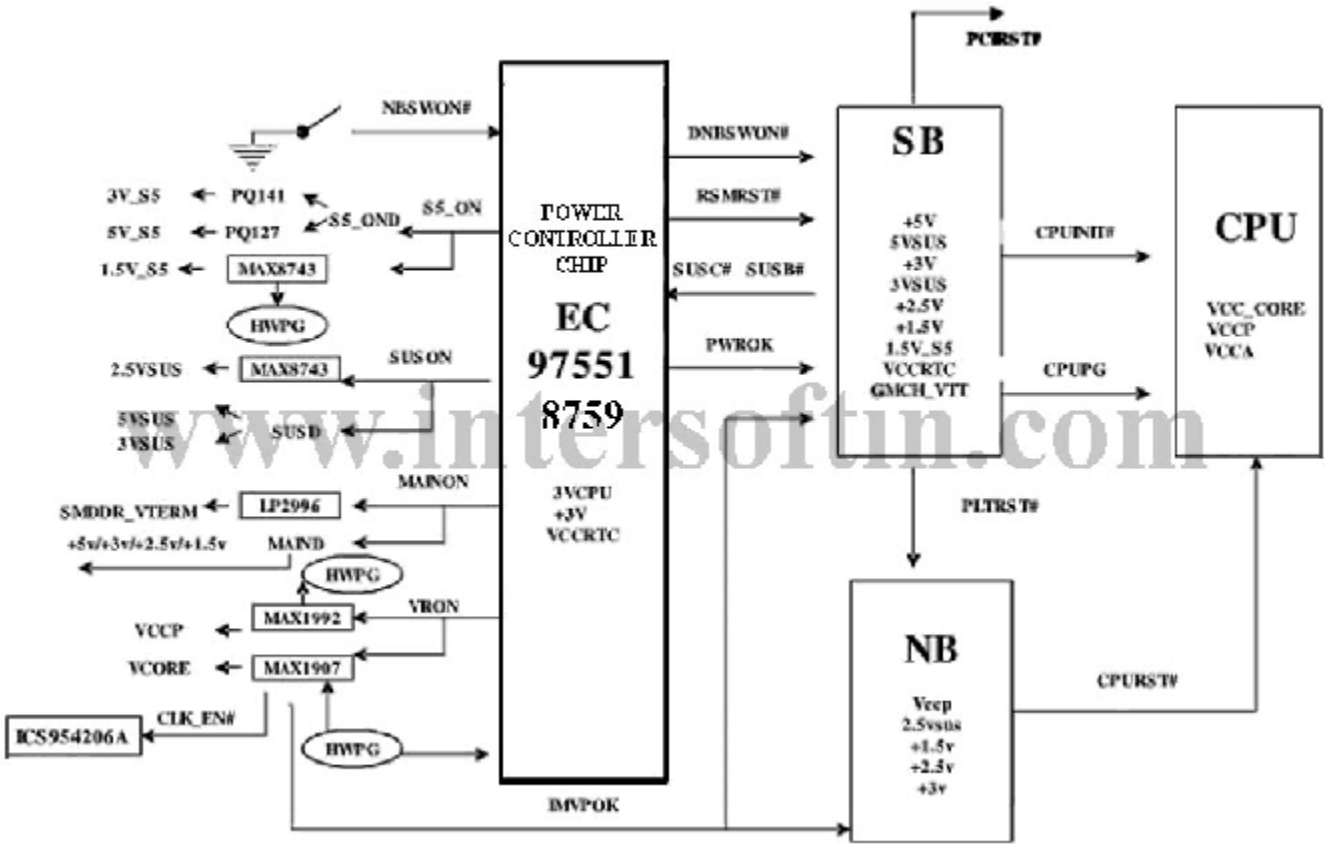
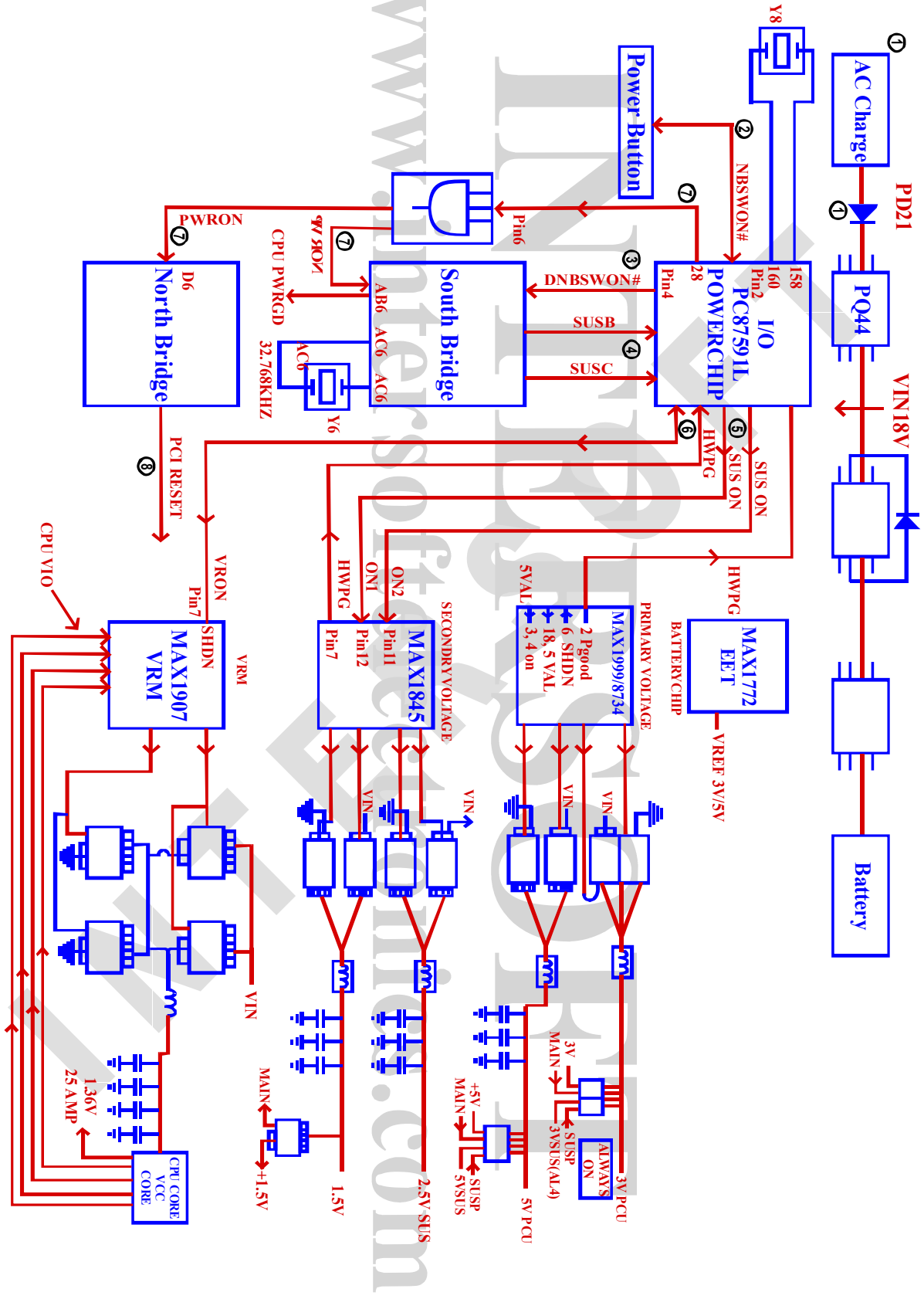
HP laptop v2000 dv1000 notebook power detail Step with timing

INTERSOFT INSTITUTE

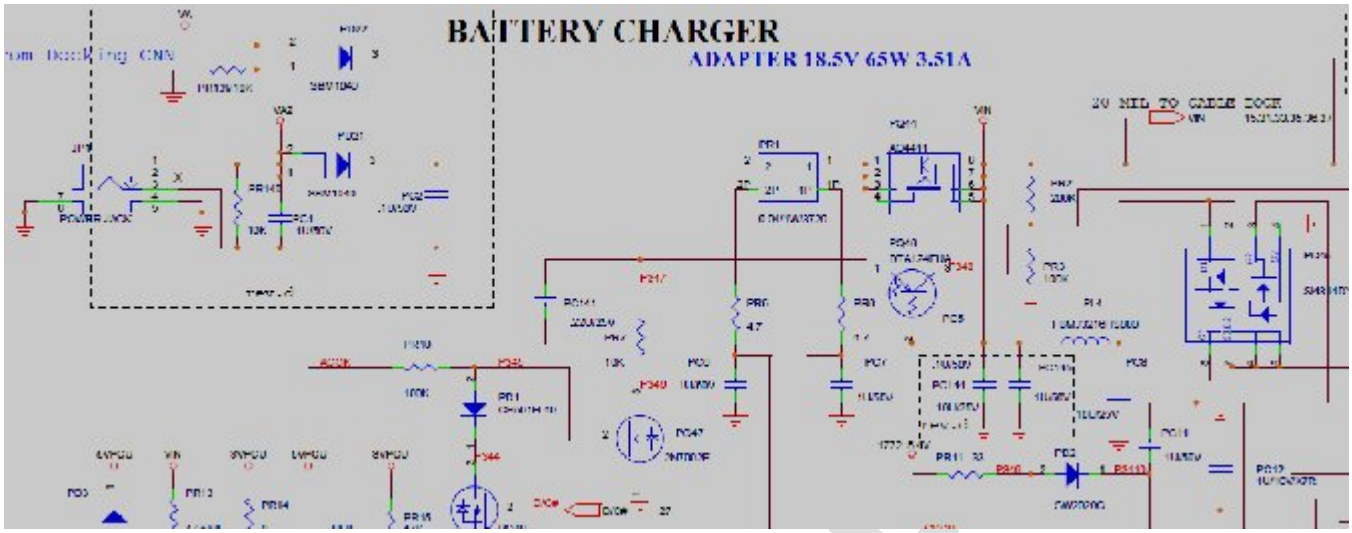
DV1000/V2000/ POWER ON DETAIL





V 2000/ DV1000/ M2000 MOTHERBOARD TRACING DETAIL

First Step is to check whether normal voltage VA is generated. (VA is the voltage through PJ1 Power Connector Adapter for Input Voltage.)If the Diode PD21, PD22 is open then VA voltage will not be generated in normal circumstance.



Second Step is to check whether the VIN voltage is normal. VIN voltage is the voltage from the VA conduction through the controlling MOSFET PQ44.

Third Step is to check 3.3/5 VPCU voltage is normal at Max 1999/8734. VIN voltage is generated as 3.3/5 VPCU in the basic premise of the system voltage. However, it only produces the two basic voltages necessary for the condition to up the power section.
Here, we take the MAX8734/1999 chip as an example :

1. Check whether the MAX 1999/8734 20 PIN has 19V input.
2. Check whether the chip's first 6 PIN SHDN has high 5V. When the pin is low, the MAX8734 /1999 will shut down and stop working.
3. Check whether the chip 5V-AL PIN 18 of MAX 1999/8734 generates a linear voltage. Here we have to note that the section of 5V-AL voltages should not be taken to mean 5VPCU voltage. As a linear voltage, it's current output is very small, which is available in the 3.3/5 VPCU voltage generator's start voltage before it. When the 3.3/ 5VPCU voltage stabilizes, the 5V-AL output PIN voltage will be 5VPCU and will take over to provide power. If the PIN has normal voltage output, then we can say that the MAX 1999/8734 internal line is up and working. If not, with the exclusion of other chip pin under exceptional circumstances, consider replacing the MAX 1999/8734 power chip.
4. Now, check chip section On PIN 3,4 the ON3 and ON5 signal should be high.
   The role of these two pins is to open the 3.3 VPCU and 5 VPCU voltages. If these 2 pins show low here then they certainly would not have 3.3/ 5 VPCU voltage.
5. Check 3.3/5VPCU output voltage, short circuit to ground to check impedance of the existence of such anomalies. If the voltage output is short circuit, MAX1999/8734 will soon be in line to protect their own state, to stop the output voltage.
6. Voltages examined on both sides of the MOS 3.3/5VPCU tube and connected to control circuit is abnormal. We can examine and control ON3 and ON5 pins.

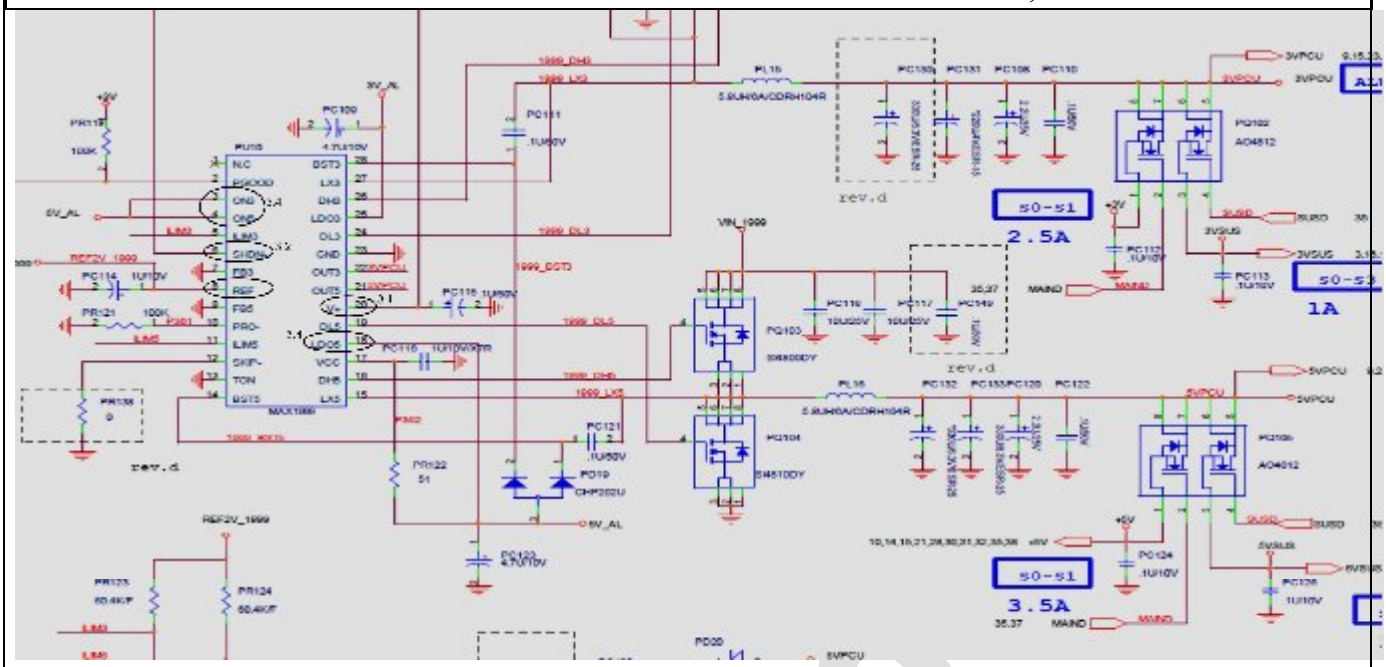
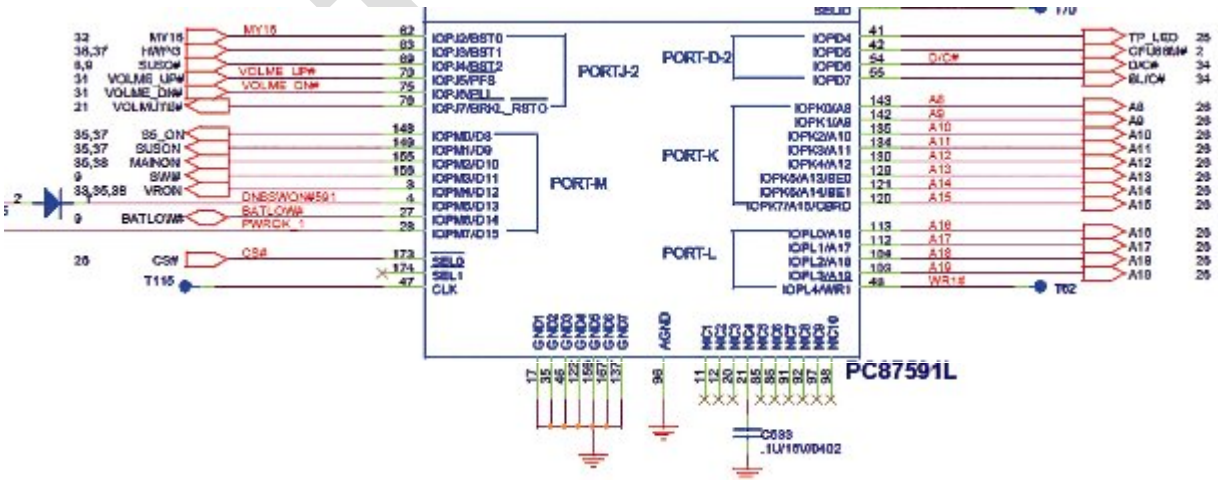


Fig. System power main 5v 3v generate max 1999 schematic diagram

Fourth Step Check the Power Management chip, IO 87591L the first 44 PIN, the ACIN input pin on the motherboard. This voltage on this pin must be high. Also check the power supply of the adapter to the motherboard.

Fifth Step Press the start button on the power board, measure whether the power management chip's first 2 PINS (ON/OFF NBSWON) high to low transition is working normally.

Sixth Step Check the power management chip to detect whether the first 4PIN (DNBSWON to South Bridge) instant boot button is pressed. A high to low negative pulse transition should be detected. If not, then this is an indication of trouble in the power management chip.



South Bridge received DNBSWON low, it occurs SUSB #, SUSC # 2 high sent to 97551/87591, South Bridge chip part of the line is always in working confition. Likewise, it is also connected to a 32.768kHz Y5, its role is to South Bridge chip modules RTC and basic detection module reference clock.

Southbridge chip power management chip receiving the boot action to issue a pulse signal, this chip will be the first 26PIN the S USB #, the first 69PIN high of SUSC # set to an invalid state, the power management chip, boot up action to provide necessary conditions. parts.

Seventh Step Check to ensure that SUSB# and SUSC# pin is in the high state from south bridge received, . If one foot is in the low state, then it will be unable to achieve power management chip boot action.

97551/87591 received SUSB #, SUSC # after have had a SUSON, MAINON #, VRON. SUSON signals into SUSD signal sent tube arises 3VSUS, 5VSUS, and SUSON sent to MAX1845 generate 2.5VSUS.

MAINON # generated by PU7 SMDDR-VTERM. At the same time and by PQ119 PQ125 into MAIND send PQ143, PQ145, PQ148, PQ153 produce +3 V, +5 V, +2.5 V, +1.5 V voltage.

VRON gave PU9 (MAX1907), PU5 (1992E) generated VCC-CORE and VCCP voltage. PU6, PU4 signals generated HWPG to 97,551, then PU3, PU5 also various feedback signals to generate a HWPG 97551/87591.

At this point the M / B of the main voltage in each group have been OK back HWPG voltage feedback signal with convergence, the equivalent of a HWPG "and" relationship, such as including any group for the low feedback HWPG this POWER OK 97551/87591 occurs

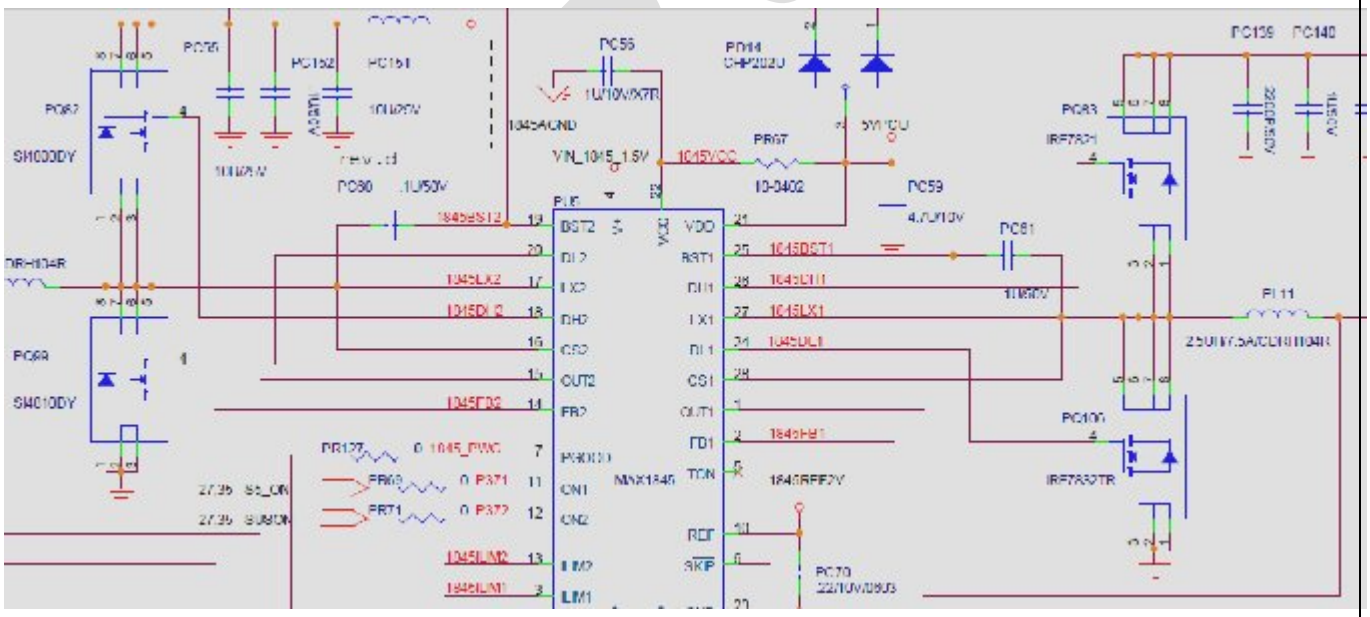


Fig. :- 2nd stage power supply block diagram

Eighth Step Measure, with a multi meter, the SUSON (from I/O to MAX1845, on signals 2nd stage 2.5 1.5 volt) power management chip149 PIN low signal, to see whether there is a high jump in the signal. This situation can be divided into two types: One is no action, the other is a jump, but without high maintenance of the signal. On focused inspection of input pin voltage, we can see that the signal generated is abnormal. The second case shows the power management chip to respond to the boot action and begin to work up. But unfortunately the control module voltage generates a problem, it cannot

generate the corresponding voltage and the voltage OK signal back to the power management chip. In this case, the 63PIN HWPG (Power Good from MAX1845, MAX1999), under normal circumstances, should send a high signal to the power management chip.

When the power management chip to the PWRGD signal received after a certain delay period, to again PWROK signal to the corresponding delay circuit. Delay circuits at different delay, the order issued by the appropriate power supply OK signal. One, SB-PWROK signal to the South Bridge chipm NB-PWROK signal to the North Bridge chip. CPU-PWROK signal to CPU. Next, the system chipset will issue a reset signal, First issued by the South Bridge PCIRST # signal to the PCI bus and other related equipment and the North Bridge chip. Meanwhile, the North Bridge chip in the receiver to the South Bridge chip issued PCIRST # reset signal, we will send CPURST# signal to the CPU.

Ninth Step in the boot power, the ultimate PWROK signal, (which is sent to the North , South and MAX 1907 vrm chip). Power Management IC's **28 PIN** is the pin we are looking for. Generally, if the pin signal maintains a high signal, it indicates the boot was successful. The mother board's power supply module and voltage stability are maintained.

Tenth Step when the instruction to turn off opening of voltage, such as the OK is HWPG constant as high as 97,551, after receiving HWPG produce PWROK signal sent to SB Southbridge, Southbridge SB produced after the PCI RST # generated through U42 PCIRST # passed to North Bridge. North Bridge before they produce the CPURST #. Signal

MAIN FOULT LIST WITH PARTICULAR ICS

Main fault: MAX 1999/8743 3VPCU or 5VPCU bad output (usually board plug 19vin, there are two voltage output)

1. VIN_1999 input 19V voltage problems.
2. Test 8 pin reference voltage is 2V.
3. Check whether PQ103 PQ101 or bad.
4. Measured with a Multimeter or 5VPCU 3VPCU ground impedance, small or short-circuit impedance for RMA board, the general line of parts for the burn. (PU10, PQ101, PQ103, PQ104, PQ102, PQ105, U23, etc.).

The IC is a voltage generated 2.5VSUS and 1.5V_S5 two groups, in 19VIN added after S5_ON, SUSON under normal circumstances, the two signals, that can generate the two voltages.

Main fault: MAX 1845 2.5VSUS or 1.5V_S5 output bad (not voltage output and low).

1. VIN_1845 input 19V voltage problems.
2. Open bad.
3. S5_ON, SUSON poor or no signals sent 1845IC.
4. 2.5 VSUS and 1.5V_S5 two smaller voltage-to-ground impedance or short circuit, for the RMA board, the general line of parts for the burn (PU5, PQ82, PQ99, PQ83, PQ106, PQ87, U16)

Signal description!
is the speed of the IC chip power management control, supply CPU CORE voltage, can automatically correct the offset, ± 0.75% output voltage accuracy, a 0.700V-1.708V to voltage output range, 2V-28V power supply input voltage range and output over-voltage protection function.

Main fault: MAX 1907 Insert CPU no voltage output.

1. VIN19V no input, PL12, PL18 bad.
2. PQ107, PQ108, PQ109, PQ110 bad.
3. 5 VPCU not enter into MAX1907IC the 30PIN.
4. Control signal VRON, SHDN, STP-CPU, DPRSLPVR, PWROK problems.
5. CPU_VID0-5 signal not sent to the MAX1907.
6. MAX1907
7. Peripheral resistance, capacitance, diode and circuit problem.

Corresponding voltage generated the following way:

CONTROLLING

1. 5 VSUS issued by PC97551/87591 SUSD signal to control PQ105 (4812IC), from the conversion over from 5VPCU
2. +5 issued by PC97551/87591 MAIND signal to control PQ105 (4812IC), conversion from 5VPCU over the.
3. 3 VSUS: PC97551/87591 issued by SUSD signal to control PQ102 (4812IC), conversion from 3VPCU them there.
4. +3 V: issued by PC97551/87591 MAIND signal to control PQ102 (4812IC), conversion from 3VPCU them there.
5. +1.5 issued by PC97551/87591 MAIND signal to control the PQ87 (4800IC), conversion from 1.5V_S5 them there.
6. 1.2 V: is the +5 V through PQ113, PQ112, PU6B and 1845REF2V signal to control the PQ89 (4800), from 1.5V_S5 convert them there.
7. VCCP is VRON by PQ91, PQ90, PU6A and 1845REF2V signal to control the PQ88 (4800), from 1.5V_S5 convert them there.

SMDDR_VTERM (1.25V issued by PC97551/87591 MAIND signal to control PU7 (LP2996IC), conversion from 2.5VSUS them there.
from the 97,551 issued S5_ON signals PQ73-PQ70-PQ70 parts produced S5_OND signal to control PQ100 the first 3 PIN, from 3VPCU conversion over the.

One main voltage: 19VIN: the total power input.
5VPCU: MAX1999IC generated.
3VPCU: MAX1999IC generated.
1.5V_S5: MAX1845IC generated.
CPU CORE: MAX1907IC generated.

Some of the main power is not the point of failure:
1. 0.001 A current fixed: generally 3VPCU, 5VPCU, 19VIN problems.

A current fixed: 3VPCU, 5VPCU, 19VPCU normal, 2.5VSUS, 1.5V_S5, +5 V, +3 V, 1.5V, 1.2V, 1.05V whether short circuit.

general short-circuit condition: 5VPCU ground short circuit, MOSFE tube, MAX1999 3VPCU ground short circuit, MOSFE tube, MAX1999, 97551/87591 chip.
On the ground a short Road, South Bridge bad.

To ground short circuit, Northbridge bad
A current fixed: 3VPCU, 5VPCU, 19VPCU normal, generally bad for the BIOS, 9 7551, South Bridge. 4, a plug power supply, current has been increased from 0.002A to zero a few amps, usually 97551/87591 chip burned. (97 551 poor, the temperature is high, hope the maintenance of attention, to avoid burns).
High-current, generally short, carefully measuring the voltage of each group on the ground impedance, replacement parts excluded failure.

POST self maintenance: self-test process

POST self-test code table:

A system does not boot: DEBUG CARD run 00 of the state.

1. The first of each group should measure the voltage supply is
2. and then check whether the circuit and chip fat, warm, odor and other anomalies, timely treatment.
3. E clock IC clock signal is sent to the pin on each chip.
4. Measure the chip RESET signal is sent or received.
5. Lace the BIOS.
6. the main signal for the

1). with empty CPU socket board installed in the machine, check the CPU to the Northbridge Block signal impedance:

3-31 address signal, HD # 0-63 data signals, ADS address status, and control signals, determine whether the CPU and North Bridge air welding, poor

2). North Bridge main signal check: HL0-10 South Bridge HUB bus interface connectivity.

Memory does not boot: DEBUG CARD running 28, 38 and so on.

1. Mainly the memory part.
2. BIOS can also cause bad run of 38.
3. The memory part of the main North Bridge Control: R_MD0-63, R_MA0-12, R_SM_DQS0-8, SM_B1-5, SM_CS0-3, M_DM0-8,
CKE0-3, CLK_SDRAM0-4 and other signals.
4. In the inspection process must be carefully measured: North Bridge - exclusive group – the memory slot of the signal, open circuit, short circuit and other undesirable phenomena.
5. Check SMDDR_VREF reference voltage is normal.
6. Northbridge, memory slots: empty and bad welding, welding or replacement material.

Shown: DEBUG CARD running 59, 69 and so on.

1. Northbridge peripheral circuits for voltage
2. Northbridge bad.
3. Clock parts and clock IC bad.
4. U15, CH7015IC bad. FUNTION poor maintenance of the

1. Battery charge and discharge bad: PQ45, PQ44, PQ42 poor more.
2. 5 IN 1CARD bad: bad need of replacement slot; slot in the foot air welding; lines and for the voltage problems; PCI7411 chip air welding and bad need of replacement.
3. Bad: Interface bad need of replacement; 1394 24.576 MHZ clock is from the vibration; PCI7411 chip problem.
4. CARDBUS bad: Interface problems; PCI7411 chip problem.
5. USB bad: Line Interface problems; Southbridge bad.
6. LAN bad: Interface loose dirt poor replacement; U18IC impedance bad; clock could not afford to vibration; chips RTL8100 bad; around bad filter capacitor leakage.
7. MODEN and sound bad: MU2 chip bad; power supply; clock; amplifier and line. MU1 and peripheral circuits.
8. HDD bad: Interface circuit; Southbridge bad.
9. CD-ROM bad: Interface circuit; Southbridge bad.
10. KEYBOARD bad: bad interface circuit; Pai Yung CP1-6 poor; 97551/87591 chip, bad; BIOS program problems, need to replace the BIOS.
11. TOUCH PAD bad: bad interface circuit; 97551/87591 chip bad.
12. FAN bad: Interface, Q11, Q12, and the 97551/87591 chip bad.

OTHER NOTES FOR IMPORTANT

Power management chips and BIOS chips, where 3.3VPCU, VC CRT C where normal electricity supply, will enter the working state. One-chip power management system can be understood as moments in the work of the monitoring status. Connected to the power management chip clock oscillator Y6 external power management chip to monitor the line to provide the basis 32.768kHz clock signal. If you do not have this clock signal, the power management chip will also be in a "paralyzed" state. -

Power Management IC 2 feet for the start signal to detect motion foot NBSWON #. Under normal circumstances, when the pin is detected over a negative pulse signal, the chip that was press the power button on the boot, and immediately turn signal through the first 4PIN of DNBSWON # "reported to the South Bridge chips."

South Bridge chip part of the line is always in working condition. Likewise, it is also connected to a 32.768 kHz external when Zhong Jingzhen Y5, its role is to South Bridge chip modules RTC and basic detection module reference clock.

Southbridge chip power management chip receiving the boot action to issue a pulse signal, this chip will be the first 26PIN the S USB #, the first 69PIN high of SUSC # set to an invalid state, the power management chip, boot up action to provide necessary conditions.

parts.

Power management chip in the receiver to the South Bridge chip SUSB #, SUSC # control signal "Reply" In the future, it began to issue secondary power control signal (S5-ON, SUSON, MAINON, and VRON) to each computer motherboard chip supply voltage generated. 3 N3 j8 H1 z I1 Z

DC / DC power supply generating circuit will have all the appropriate supply voltage to achieve stability in their output will be issued PWRGD high effective signal back to the power management chip, meaning that tell it, had now been given the task of successfully completed. Next, the power management chip control chip can be reported to the superior work.

When the power management chip to the PWRGD signal received after certain

delay period, to again PWROK signal to the corresponding delay circuit. Delay circuits at different delay, the order issued by the appropriate power supply OK signal. One, SB-PWROK signal to the South Bridge chip, NB-PWROK signal to the North Bridge chip, CPU-PWROK signal to CPU. Next, the system chipset will issue a reset signal, first issued by the South Bridge PCI RST # signal to the PCI bus and other related equipment and the North Bridge chip. Meanwhile, the North Bridge chip in the receiver to the South Bridge chip issued PCIRST # reset signal, we will send CPURST # signal to the CPU. check sequence:;)

South Bridge, the main signal checking: AD0-31 composite address data signal line, C/BE0-3 bytes to allow the signal line, the control signal line, LAD0 -3 + LDRQ0 + LFRAME # even the case in which the hard disk access 97,551 chips in the LPC bus interface.
4). MINI PCI slot on the PCI bus can be measured to check the appropriate bus plug-in circuit.
5). 97 551 chip, the signal inspection: LAD0-3 + LDRQ0 + LFRAME # signal.
6). BIOS checks on the signal: A0-19 address lines, D0-7 data lines, CS # chip select signals, RD # read the signal, WR # write signal and power ground.
7). try to make it clear fault region, to facilitate maintenance.
If the above does not find problems, from the perspective of poor parts replacement parts to repair.