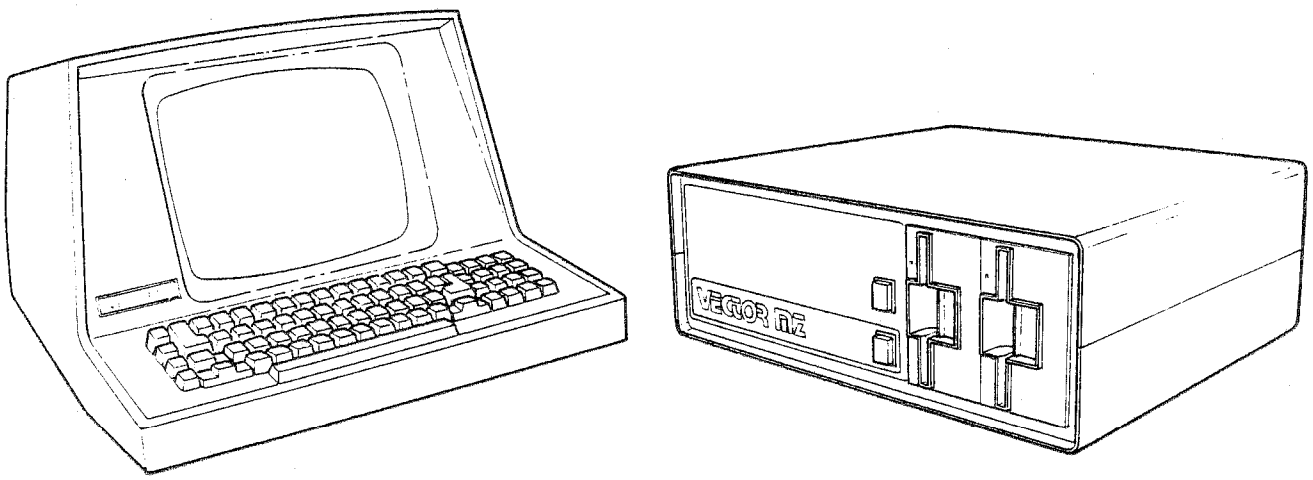
Bitstreamer
Users Manual



VECTOR GRAPHIC INC.

REPAIR AGREEMENT

The Bit Streamer Board sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any Bit Streamer Board that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the Bit Streamer Board left the VECTOR GRAPHIC, INC., factory;

2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;

3. The Bit Streamer Board is promptly returned to VECTOR GRAPHIC, INC., at customer's expense, for examination by VECTOR GRAPHIC, INC., to confirm the alleged defect, and for subsequent repair or replacement if found to be in order.

Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the Bit Streamer Board is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is $35.00 for the first hour, and $18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any Bit Streamer Board until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.

BIT STREAMER I/O BOARD

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INTRODUCTION

VECTOR GRAPHIC INC.'S "BIT STREAMER" I/O BOARD IS DESIGNED FOR EASE OF OPERATION AND MAXIMUM FLEXIBILITY. AN 8251 USART IS EMPLOYED, WHICH UNDER SOFTWARE CONTROL IS CAPABLE OF A WIDE VARIETY OF DATA CONFIGURATIONS. THE SERIAL PORT INCLUDES DRIVERS AND RECEIVERS FOR BOTH RS232C OR 20MA CURRENT LOOP OPERATION. INCLUDED IN THIS MANUAL ARE DIRECTIONS FOR A SIMPLE MODIFICATION TO PERMIT TWO SERIAL PORTS.

THE TWO PARALLEL I/O PORTS FEATURE LATCHED OUTPUT DATA LINES AND LATCHES FOR THE INPUT STROBES.

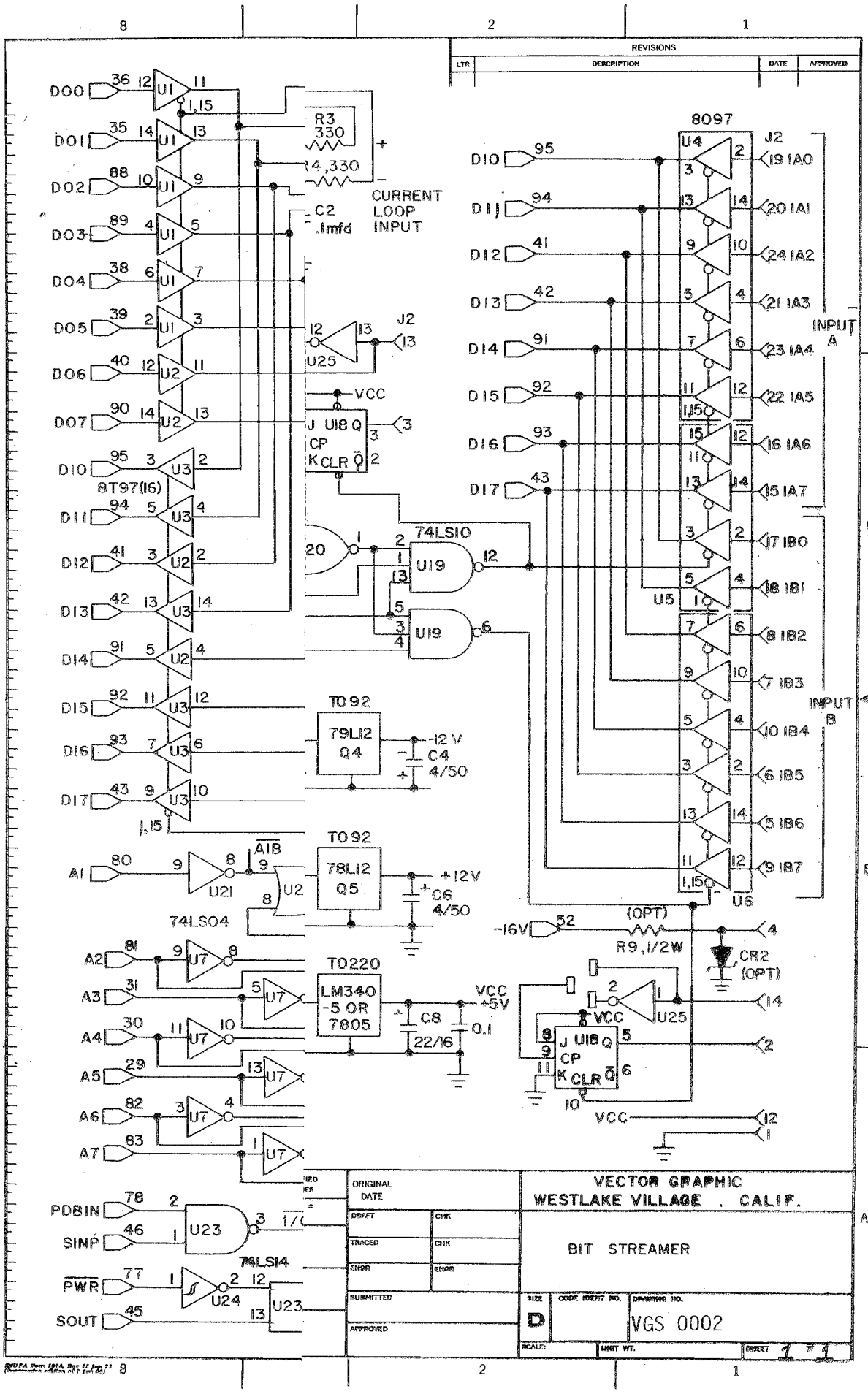
CAREFUL ATTENTION TO GOOD DESIGN PRACTICES PROVIDES THE USER WITH AN I/O BOARD THAT OPERATES RELIABLY WITHOUT CONSTANT ADJUSTMENT OR MAINTENANCE.

IF THERE IS ANYTHING YOU DO NOT UNDERSTAND, PLEASE DO NOT HESITATE TO CALL OR WRITE US.

PARTS LISTS

QTY.	DESCRIPTION
1	PRINTED CIRCUIT BOARD
1	6106B HEAT SINK
1	7805/340T-5 REGULATOR
1	78L12
1	79L12
1	8251 USART (U9)
1	7493 (U10)
3	74LS93 (U11, U12, U13)
6	74367/8097 (U1, U2, U3, U4, U5, U6)
1	74LS30 (U8)
2	74LS02 (U20, U22)
1	74LS00 (U23)
4	74LS75 (U14, U15, U16, U17)
1	74LS14 (U24)
3	74LS04 (U7, U21, U25)
1	74LS107 (U18)
1	74LS10 (U19)
1	1488 LINE DRIVER (U26)
1	1489 LINE RECEIVER (U27)
2	470 PF 50 VOLT AXIAL GLASS CAPACITORS
7	0.1 MFD 50V MONOLITHIC RADIAL CAPACITORS
4	4.0 MFD 50V AXIAL ELECTROLYTIC CAPACITORS
2	22 MFD 16V AXIAL ELECTROLYTIC CAPACITORS

QTY.		DESCRIPTION
3		330 OHM 1/4 WATT CARBON RESISTORS (STRIPES OF ORANGE, ORANGE, BROWN)
2		220 OHM 1/2 WATT CARBON RESISTORS (STRIPES OF RED, RED, BROWN)
2		4.7K 1/4 WATT RESISTOR (STRIPES OF YELLOW, VIOLET, RED)
2		1K 1/4 WATT RESISTORS (STRIPES OF BROWN, BLACK, RED)
3		2N3643 TRANSISTORS
1		1N4148 DIODE
1		MOLEX PLUG
2		24 PIN DIP PLUGS
1		8 POSITION DIP SWITCH
2		24 PIN SOCKETS
10		16 PIN SOCKETS
16		14 PIN SOCKETS
1		28 PIN SOCKET
2		EJECTORS
	OPTIONAL	
1		CABLE #ASI-1327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DESCRIPTION
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U5
U6
J2
INPUT A
INPUT B
D00
D01
D02
D03
D04
D05
D06
D07
D10
D11
D12
D13
D14
D15
D16
D17
R3
330
4,330
CURRENT LOOP INPUT
C2
.1mfd
VCC
74LS10
U19
TO92
79L12
Q4
-12 V
C4
4/50
74LS04
U21
U2
78L12
Q5
+12V
C6
4/50
-16V
(OPT)
R9, 1/2W
CR2
(OPT)
TO220
LM340
-5 OR
7805
C8
22/16
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VCC
+5V
U25
U18
PDBIN
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PWR
SOUT
74LS14
U23
U24
ORIGINAL DATE
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SUBMITTED
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VECTOR GRAPHIC
WESTLAKE VILLAGE . CALIF.
BIT STREAMER
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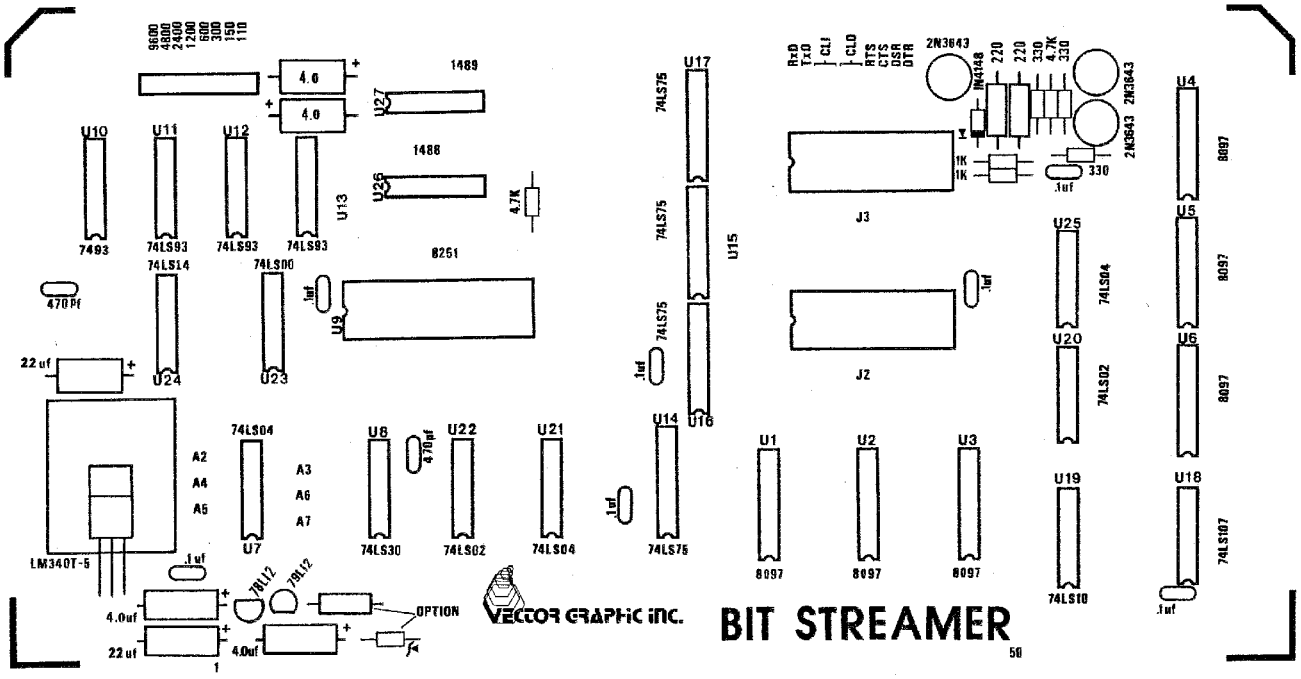
DRAWING NO.
VGS 0002
SCALE:
UNIT WT.
SHEET 1 OF 1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4800
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U10
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U12
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U27
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74LS93
74LS93
4.7K
8251
74LS14
74LS00
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U9
22 uf
U24
U23
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A2
A4
A5
A3
A6
A7
U7
U8
U22
U21
470uf
74LS30
74LS02
74LS04
LM340T-5
.1uf
78L12
79L12
OPTION
4.0uf
22 uf
4.0uf
1
VECTOR GRAPHIC INC.
BIT STREAMER
50
U17
74LS75
74LS75
74LS75
U15
U16
U14
74LS75
.1uf
R=D
T=D
CLI
CLD
RTS
CTS
DSR
DTR
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IN4148
220
220
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4.7K
330
2N3643
2N3643
1K
1K
330
.1uf
J3
J2
.1uf
U25
74LS04
U20
74LS02
U19
74LS10
U1
U2
U3
8097
8097
8097
U4
U5
U6
U18
8097
8097
8097
74LS107
.1uf

THEORY OF OPERATION

THE BIT STREAMER COMBINES TWO PARALLEL INPUT PORTS, TWO PARALLEL OUTPUT PORTS AND A SERIAL I/O PORT USING AN 8251 PROGRAMMABLE UNIVERSAL SYNCHRONOUS / ASYNCHRONOUS RECEIVER - TRANSMITTER. COMMUNICATION WITH THE CIRCUITRY ON THE BOARD IS BY MEANS OF INPUT AND OUTPUT INSTRUCTION CYCLES EXECUTED BY THE CPU.

INPUT PORTS

TO INPUT DATA, THE FOLLOWING SIGNAL CONDITIONS MUST BE MET:

1. THE LOWER EIGHT ADDRESS LINES MUST CONTAIN THE PORT ADDRESS.

2. SINP MUST BE HIGH, INDICATING AN INPUT MACHINE CYCLE.

3. PDBIN MUST BE HIGH, INDICATING THAT THE DATA BUS MAY BE ACCESSED BY THE BOARD.

THE REQUIRED SIGNALS ARE GATED TOGETHER THROUGH U8, U23, U20 AND U19 TO PRODUCE TWO ENABLE SIGNALS -- ONE FOR PORT A AND ONE FOR PORT B -- WHICH STROBE THE INPUT DATA ONTO THE DATA BUS AT THE APPROPRIATE TIME USING TRI-STATE BUS DRIVERS U4, U5 AND U6.

OUTPUT PORTS

VALID OUTPUT DATA IS PRESENT ON THE DATA BUS DURING AN OUTPUT MACHINE CYCLE WHEN THE FOLLOWING CONDITIONS ARE MET:

1. THE LOWER EIGHT ADDRESS LINES CONTAIN THE PORT ADDRESS.

2. SOUT MUST BE HIGH, INDICATING AN OUTPUT MACHINE CYCLE.

3. PWR MUST BE LOW, INDICATING THE DATA BUS CONTAINS VALID DATA.

THE APPROPRIATE SIGNALS ARE GATED TOGETHER THROUGH U8, U23, U19 AND U20 TO PRODUCE STROBES TO CAUSE THE DATA BUS SIGNALS TO BE LATCHED BY 74LS75 QUAD LATCHES U14, U15, U16 AND U17. THESE OUTPUTS REMAIN CONSTANT UNTIL THE PARTICULAR OUTPUT PORT IS AGAIN ACCESSED BY THE CPU. AN INTERNAL BI-DIRECTIONAL DATA BUS IS USED TO MINIMIZE THE LOADING ON THE S-100 BUS.

SERIAL PORT

THE HEART OF THE SERIAL I/O PORT IS THE 8251 USART CONSISTING OF INDEPENDENT RECEIVER AND TRANSMITTER. THE FUNCTION OF THE TRANSMITTER IS TO ACCEPT EIGHT BITS OF PARALLEL DATA FROM THE DATA BUS, AND CONVERT THIS TO SERIAL DATA WITH A WIDE RANGE OF ASYNCHRONOUS FORMATS. THE SPEED AT WHICH THE DATA AND SYNC BITS

ARE OUTPUT IS CALLED THE BAUD RATE (AFTER BAUDOT) AND THIS IS CONTROLLED BY A SELECTABLE CLOCK RATE DERIVED FROM THE 2 MHZ SYSTEM CLOCK BY COUNTERS U10, U11, U12 AND U13. THE CLOCK RATE IS NORMALLY SIXTEEN TIMES THE REQUIRED BAUD RATE (THIS CAN BE CHANGED WHEN THE USART IS INITIALIZED), SO A FREQUENCY OF 153.6 KHZ IS REQUIRED FOR 9600 BAUD. THIS GIVES A FREQUENCY DIVISION RATIO OF 13.02 (WHICH IS ROUNDED TO 13) RELATIVE TO THE 2 MHZ CLOCK. U10 THUS FORMS A DIVIDE BY 13 STAGE, AND THE GATED TERMINAL COUNT AT U23 PIN 8 CAN BE SELECTED BY A DIP SWITCH FOR 9600 BAUD. THE COMMON BAUD RATES, EXCEPT FOR 110 BAUD, ARE OBTAINED BY SUCCESSIVELY DIVIDING THIS FREQUENCY IN HALF USING U11 AND U12 (74LS93 BINARY COUNTERS). THE CLOCK FREQUENCY FOR 110 BAUD, THE STANDARD FREQUENCY FOR TELETYPES, IS GENERATED BY DIVIDING THE FREQUENCY FOR 2400 BAUD BY 22. THESE FREQUENCIES ARE SELECTED BY THE DIP SWITCH AND APPLIED TO TXC AND RXC OF THE USART.

THE USART IS DESIGNED TO INTERFACE EASILY TO AN 8080 BUS STRUCTURE, AND THE CONTROL SIGNALS RD, C/D, CS, WR ARE DERIVED EASILY FROM THE S-100 BUS SIGNALS. SINCE THE DEVICE WAS INTENDED TO BE USED WITH A BI-DIRECTIONAL DATA BUS, THE S-100 SPLIT DATA BUS IS RECOMBINED AS AN INTERNAL DATA BUS USING THE TRI-STATE BUS DRIVERS U1, U2 AND U3. EIA RS232C LEVEL LINE DRIVERS AND RECEIVERS U27 AND U26 INTERFACE THE RXD INPUT AND TXD OUTPUT OF THE USART TO THE OUTSIDE WORLD. THESE COMPONENTS ARE CAPABLE OF TOLERATING MORE ABUSE IN THEIR CIRCUITS AND STATIC TRANSIENTS THAN ARE TTL OR MOS DEVICES, AND PRODUCE PLUS OR MINUS 10 VOLT SIGNALS WITH HIGH NOISE IMMUNITY. IN ADDITION, DISCRETE COMPONENTS ARE USED TO INTERFACE WITH 20MA TELETYPE SIGNALS.

THE USART IS CAPABLE OF BEING CONFIGURED FOR A WIDE VARIETY OF COMMUNICATION FORMATS. THE EXACT SOFTWARE REQUIRED TO COVER PERHAPS 90% OF THE APPLICATIONS FOR PERSONAL OR BUSINESS COMPUTERS IS DESCRIBED IN THE USERS GUIDE. FOR MORE SOPHISTICATED APPLICATIONS, THE USER IS REFERRED TO THE INTEL PUBLICATIONS AP-16 AND 1977 DATA CATALOG OR ADAM OSBORNE'S "AN INTRODUCTION TO MICROCOMPUTERS" VOLUME II.

USERS GUIDE

THE BIT STREAMER I/O BOARD HAS BEEN DESIGNED TO MINIMIZE THE NEED FOR USER INSTALLED JUMPERS. WITHOUT MAKING ANY CHANGES TO THE PRE-JUMPERED OPTIONS, THE BOARD CAN BE INSTALLED IN A COMPUTER AND WILL OPERATE AS AN RS232 SERIAL PORT USING THE INITIALIZATION AND I/O SOFTWARE ON THE VECTOR GRAPHIC OPTION C MONITOR PROM. CONNECTION BETWEEN THE BOARD SOCKET J3 AND DB25 TERMINAL CONNECTOR CAN BE MADE BY MEANS OF A 24 WIRE FLAT RIBBON CABLE WITH A 24 PIN DIP PLUG ON ONE END AND A DB25 FEMALE CONNECTOR ON THE OTHER. THIS CABLE IS AVAILABLE FROM VECTOR GRAPHIC AS AN OPTION. THE PINOUT HAS BEEN CONFIGURED SO THAT THE RS232 DATA AND CONTROL LINES WILL MATCH; PIN 24 ON THE DIP PLUG CONNECTS TO PIN 1 ON THE DB25. THE PARALLEL OUTPUT PORTS ARE AVAILABLE ON THE SAME CONNECTOR, WHILE THE PARALLEL INPUT PORTS ARE AVAILABLE AT J2. FIGURE 1 GIVES THE PINOUTS FOR THE VARIOUS LINES.

IN THE STANDARD CONFIGURATION, THE BOARD OCCUPIES FOUR I/O PORT ADDRESSES AS SHOWN BELOW:

PORT	INPUT	OUTPUT
03	USART STATUS	USART COMMAND
02	USART DATA	USART DATA
01	PARALLEL PORT B	PARALLEL PORT B
00	PARALLEL PORT A	PARALLEL PORT A

THE PARALLEL PORT OPERATION IS QUITE STRAIGHTFORWARD: AN "OUT 0" INSTRUCTION EXECUTED BY THE CPU WILL CAUSE THE 8 BIT CONTENTS OF THE ACCUMULATOR TO BE LATCHED ON THE BOARD AND THE TTL LEVEL SIGNALS CORRESPONDING TO THE VARIOUS BITS WILL BE AVAILABLE AT PORT A AS SHOWN IN FIGURE 1. SIMILARLY, AN "IN 1" INSTRUCTION WILL CAUSE THE SIGNALS APPLIED TO PORT B ON J3 TO BE SAMPLED AND TRANSFERRED TO THE ACCUMULATOR. INPUT VOLTAGES SHOULD NOT EXCEED THE RANGE OF 0-5V, AND THE OUTPUTS ARE ACTIVE PULL-UP LOW POWER SCHOTTKY GATES WITH A FAN OUT OF FIVE STANDARD TTL GATES OR 20 LOW POWER SCHOTTKY GATES.

OPERATION OF THE SERIAL PORT IS CONSIDERABLY MORE COMPLEX AND WILL BE DESCRIBED IN MORE DETAIL ELSEWHERE. BRIEFLY, THE 8251 USART MUST BE CONFIGURED BY OUTPUTTING TWO COMMANDS TO PORT 3 ONCE, AND ONLY ONCE, EACH TIME THE COMPUTER IS TURNED ON OR RESET. THE VECTOR GRAPHIC CPU BOARD GENERATES A POC SIGNAL IN EITHER CASE. THE INITIALIZATION ROUTINE FOR MOST APPLICATIONS IS AS FOLLOWS:

```
INIT    MVI A, 0CEH
        OUT 3
        MVI A, 27H
        OUT 3
```

THE FIRST COMMAND CONFIGURES THE USART FOR ASYNCHRONOUS OUTPUT WITH A BAUD RATE CLOCK DIVIDE FACTOR OF 16, AN 8 BIT CHARACTER LENGTH, NO PARITY BIT AND TWO STOP BITS. THIS IS THE STANDARD FORMAT FOR 110 BAUD COMMUNICATION, BUT IT WILL WORK

SATISFACTORILY AT HIGHER BAUD RATES (I.E. WITH AN ADM-3 TERMINAL), ALTHOUGH ONLY ONE STOP BIT IS NORMALLY USED. THE EXTRA STOP BIT WILL RESULT IN A 10% TRANSMISSION SPEED REDUCTION, AND APPEARS TO THE TERMINAL AS A BRIEF MARK CONDITION BETWEEN CHARACTERS. THE SECOND COMMAND ENABLES THE TRANSMITTER AND RECEIVER TO BEGIN DATA TRANSMISSION.

RECEIPT OF A CHARACTER IS INDICATED BY TESTING THE STATUS PORT. A TYPICAL INPUT ROUTINE IS AS FOLLOWS:

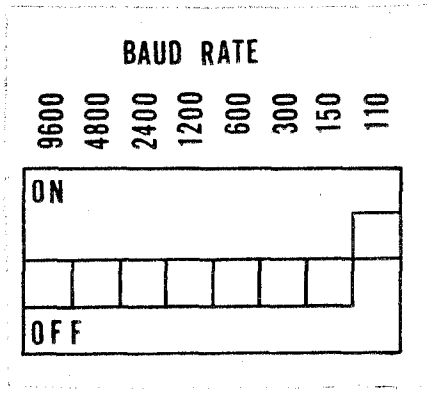
```
INPUT   IN      3       USART STATUS
        XRI     00
        ANI     2       LOOK AT D1 - RXRDY
        JZ      INPUT   LOOP UNTIL TRUE
        IN      2       READ DATA
        ANI     7FH     MASK EIGHTH BIT
        RET
```

TRANSMISSION OF A CHARACTER STARTS BY TESTING THE STATUS PORT TO SEE IF THE USART IS READY TO RECEIVE A CHARACTER.

```
OUTPUT  IN      3       USART STATUS
        XRI     00
        ANI     1       LOOK AT D0 - TXRDY
        JZ      OUTPT   LOOP UNTIL TRUE
        POP     PSW     (OR MOV A,B)
        OUT     2       OUTPUT DATA
        RET
```

OF COURSE, PRIOR TO CALLING THE OUTPUT ROUTINE, THE CHARACTER CODE TO BE OUTPUT WAS SAVED ON THE STACK OR IN ONE OF THE CPU REGISTERS.

THE BAUD RATE IS CONTROLLED BY BOTH THE BAUD RATE FACTOR SELECTED DURING INITIALIZATION, WHICH FIXES THE INTEGER BY WHICH THE USART DIVIDES THE EXTERNALLY SUPPLIED CLOCK, AND THE BAUD RATE SWITCH SETTING ON THE UPPER LEFT CORNER OF THE BOARD. THE LEFTMOST SWITCH WILL SELECT 9600 BAUD, WHILE THE RIGHTMOST SWITCH SELECTS 110 BAUD. THE X16 BAUD RATE FACTOR IS TAKEN INTO ACCOUNT. ONLY ONE SWITCH SHOULD BE ON AT ANY ONE TIME, AND THE BAUD RATE OF THE TERMINAL MUST AGREE WITH THE SWITCH SETTING.



CONNECTION TO THE TERMINAL

EITHER RS232 OR 20MA CURRENT LOOP SIGNALS CAN BE INTERFACED TO THE BIT STREAMER. THE SIMPLEST METHOD IS TO USE A FLAT RIBBON CABLE AS MENTIONED PREVIOUSLY. CABLES ARE AVAILABLE AT YOUR LOCAL COMPUTER STORE, OR YOU MAY ORDER FROM VECTOR GRAPHIC.

THE INTERCONNECTIONS BETWEEN THE PINS OF J3 ARE SHOWN IN FIGURE 2.

THE CORRESPONDENCE BETWEEN J3 AND THE DB25 CONNECTOR PINS IS AS FOLLOWS:

J3	DB25	RS232 DEFINITION RELATIVE TO TERMINAL
24	1	PROTECTIVE GROUND
23	2	TRANSMITTED DATA (TXD)
22	3	RECEIVED DATA (RXD)
21	4	REQUEST TO SEND (RTS)
20	5	CLEAR TO SEND (CTS)
19	6	DATA SET READY (DSR)
18	7	SIGNAL GROUND (GND)
7	20	DATA TERMINAL READY (DTR)

AS FAR AS THE BIT STREAMER IS CONCERNED, THE ONLY SIGNAL NEEDED FOR PROPER OPERATION IS CLEAR TO SEND (CTS), WHICH MUST BE HIGH TO ENABLE THE USART. IF NO CONNECTION IS MADE, A PULL-UP RESISTOR HOLDS THIS LINE HIGH.

FOR PROPER OPERATION OF THE TERMINAL (IN ADDITION TO SIGNAL GROUND, TRANSMITTED DATA AND RECEIVED DATA) CTS AND DSR MUST BE HELD HIGH. THIS IS DONE BY JUMPERING THEM TO RTS AND DTR RESPECTIVELY, WHICH GO HIGH WHEN THE TERMINAL IS ON. TRACES ON THE BOARD INTERCONNECT THE APPROPRIATE PINS. IF EITHER OF THESE SIGNALS IS NOT AVAILABLE, CTS AND DSR MAY BE CONNECTED TO +5V THROUGH A 4.7K PULLUP RESISTOR.

AN ALTERNATE METHOD OF CONNECTING THE TERMINAL IS TO USE A THREE WIRE CONNECTION TO THE BOARD (RXD, TXD, SIGNAL GROUND) AND CONNECT PIN 4 TO PIN 5 AND PIN 20 TO PIN 6 AT THE TERMINAL REAR PANEL.

IF FULL RS232 PROTOCOL WILL BE USED, CUT THE TRACES AS SHOWN IN FIGURE 3-1 AND ADD THE JUMPERS TO CONNECT THE CONTROL SIGNALS TO THE EIA LINE DRIVERS AND RECEIVERS. THE DSR CONTROL INPUT SIGNAL CAN BE TESTED BY LOOKING AT BIT 7 ON THE STATUS PORT, WHILE THE DTR AND RTS OUTPUTS CAN BE CONTROLLED BY OUTPUTTING THE APPROPRIATE COMMAND TO PORT 3. THESE SIGNALS ARE NOT SUPPORTED BY MOST OF THE SOFTWARE AVAILABLE TO THE HOBBYIST, AND SHOULD BE CONNECTED ONLY IN EXCEPTIONAL CASES.

20MA CURRENT LOOP

FOUR LEADS ARE REQUIRED TO CONNECT THE BOARD TO A 20MA CURRENT LOOP DEVICE SUCH AS AN ASR33 TELETYPE:

CURRENT LOOP INPUT + AND -

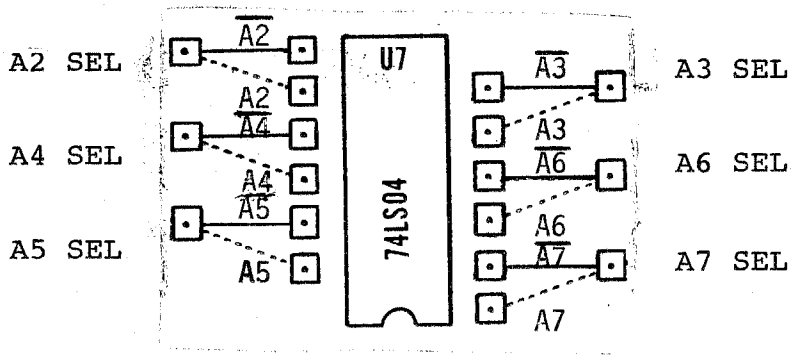
CURRENT LOOP OUTPUT + AND -

THESE SIGNALS ARE AVAILABLE ON THE PADS IMMEDIATELY ABOVE J3. REFER TO FIGURE 3-2 FOR JUMPERING ILLUSTRATION. A MOLEX CONNECTOR STRIP SOLDERED IN THESE PADS CAN BE USED FOR THE TTY CONNECTIONS, AND A JUMPER MUST BE INSTALLED IN THE UPPER RIGHT HAND CORNER OF THE BOARD TO CONNECT THE CURRENT LOOP INPUT CIRCUIT.

FOR THIS APPLICATION, THE EIA RECEIVER (1489) SHOULD REMAIN IN PLACE AS IT PROVIDES AN INTERNAL RESISTIVE PULL-UP FOR Q1. BOTH CURRENT LOOP AND RS232 TERMINALS CAN BE CONNECTED SIMULTANEOUSLY, FOR EXAMPLE, WHERE A VIDEO DISPLAY AND TELETYPE PRINTER ARE USED. THE KEYBOARD INPUTS WOULD BE IN PARALLEL DUE TO THE WIRED "OR" CONNECTION OF RXD AND BOTH OUTPUTS WOULD BE ENABLED. THE BAUD RATE COULD BE SELECTED WITH AN EXTERNAL SWITCH, AND THE TTY PRINTER COULD BE DISABLED WITH AN SPST SWITCH FROM CLO- TO GROUND.

CHANGING THE BOARD ADDRESS

ON EITHER SIDE OF U7 IN THE LOWER LEFT CORNER OF THE BOARD ARE SIX SETS OF PADS THAT CONTROL THE BOARD ADDRESS.



TO CHANGE THE ADDRESS, CUT THE TRACE BETWEEN PADS NEXT TO U7 AND THE ADDRESS BIT TO BE CHANGED AND INSTALL A JUMPER AS INDICATED BY THE DOTTED LINE TO THE INVERTED PIN ON U7. FOR EXAMPLE, TO CHANGE THE BOARD ADDRESS FROM PORT 0 TO PORT 4 CUT THE TRACE FROM A2 TO A2SEL AND ADD A JUMPER FROM A2 TO A2SEL.

EXTERNAL BAUD RATE CONTROL

IF TWO DIFFERENT BAUD RATES ARE COMMONLY USED, THE DIP SWITCH CAN BE REPLACED WITH AN SPDT SWITCH MOUNTED ON THE REAR PANEL AND CONNECTED TO THE BOARD WITH A 16 PIN DIP PLUG AND SOCKET. ALTERNATELY, THE BAUD RATE CAN BE CONTROLLED BY SOFTWARE BY SELECTING A BAUD RATE FACTOR OF 1X, 16X OR 64X WHEN THE USART

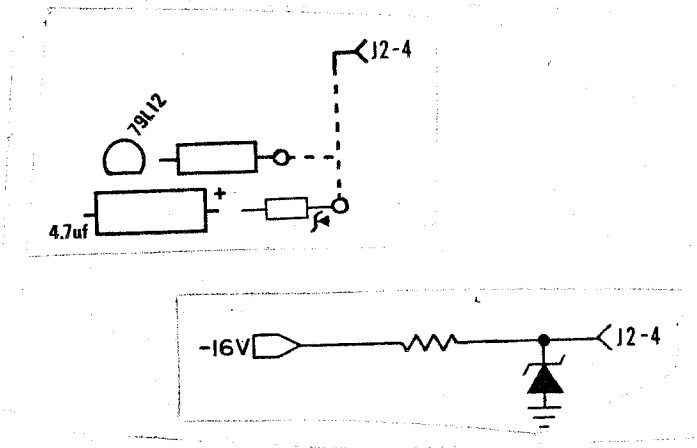
COMMAND IS ISSUED.

PATCH AREA

IMMEDIATELY TO THE RIGHT OF THE 8251 USART ARE LOCATED TWO 16 PIN PAD ARRAYS THAT CAN BE USED FOR ANY SPECIAL PURPOSE, SUCH AS CUSTOM I/O INTERFACES. THERE ARE SEVERAL UNUSED GATES AND INVERTERS ON THE BOARD WHICH HAVE 3 HOLE SOLDER PADS FOR SIMILAR PURPOSES. A BUFFERED CLK SIGNAL IS AVAILABLE AT U24-6.

KEYBOARD CONNECTION

ONE USE OF THE PARALLEL INPUT PORTS IS TO INTERFACE WITH A KEYBOARD. MANY KEYBOARDS REQUIRE A NEGATIVE SUPPLY VOLTAGE IN ADDITION TO THE +5V, AND THERE ARE PADS PROVIDED IN THE LOWER LEFT PORTION OF THE BOARD FOR AN OPTIONAL ZENER REGULATED SUPPLY.



THE ZENER VOLTAGE WILL DEPEND ON THE KEYBOARD REQUIREMENTS IF IT IS NEEDED AT ALL, AND THE RESISTOR SHOULD BE SELECTED TO BIAS THE ZENER WITH AT LEAST 10MA OF CURRENT IN ADDITION TO THE CURRENT REQUIRED BY THE KEYBOARD.

FOR EXAMPLE, WITH A KEYBOARD REQUIRING 10MA OF CURRENT AT 6V, THE ZENER COULD BE A 1N752A (5.6V) AND THE RESISTOR COULD BE 10/.02 = 500 OHMS (470 NOMINAL). THE ZENER DISSIPATION WOULD BE 60MW AND THE RESISTOR DISSIPATION WOULD BE 200MW (USE A 1/2 WATT RESISTOR TO ALLOW FOR HIGHER SUPPLY VOLTAGE).

THE DATA FROM THE KEYBOARD CAN BE CONNECTED TO INPUT PORT B, BITS 0-6. SOME KEYBOARDS HAVE POSITIVE TRUE DATA WHILE OTHERS HAVE NEGATIVE TRUE POLARITY. MOST SOFTWARE EXPECTS POSITIVE TRUE INPUTS, ALTHOUGH A CMA INSTRUCTION CAN BE USED TO INVERT THE INPUT DATA. ALTERNATELY, MANY KEYBOARDS HAVE INVERTING OUTPUT BUFFERS THAT CAN BE REPLACED WITH NON-INVERTING TYPES.

EITHER A KEYPRESS SIGNAL OR A STROBE PULSE IS GENERATED BY THE KEYBOARD TO INDICATE THAT A KEY HAS BEEN DEPRESSED AND THE DATA IS VALID (DEBOUNCED). THIS SIGNAL SHOULD BE CONNECTED TO STROBE INPUT B (J2 PIN 14). THE PROPER STROBE POLARITY SHOULD BE SELECTED BY INSTALLING A JUMPER BETWEEN U25 PIN 1 OR 2 AND THE PAD OPPOSITE THEM SO THAT THE SIGNAL APPLIED TO U18 PIN 9 GOES LOW WHEN A KEY IS PRESSED. THE Q OUTPUT OF U18 AVAILABLE AT J2 PIN 2 SHOULD BE CONNECTED TO J2 PIN 16 (A6 INPUT). THE KEYBOARD SHOULD OPERATE PROPERLY WITH THE

FOLLOWING INPUT ROUTINE:

```
INPUT   IN      0       KBD STATUS PORT A
        ANI     40H     STATUS BIT
        JZ      INPT
        IN      1       KBD DATA PORT B
        ANI     7FH     IGNORE EIGHTH BIT
        RET
```

ALTHOUGH OTHER CONFIGURATIONS ARE POSSIBLE, THE IMPORTANT THING TO REMEMBER IS THAT THE STATUS BIT LATCH U18 SHOULD NOT BE RESET UNTIL THE DATA IS READ IN FOR PROPER OPERATION WITH EXISTING SOFTWARE THAT MAY MAKE MULTIPLE TESTS OF THE STATUS BIT IN TESTING FOR A CONTROL C. THE STATUS BIT IS RESET WHEN PORT B IS INPUT. THE KEYBOARD DATA IS NOT LATCHED ON THE BOARD, AND THIS MEANS CONTROL C OR OTHER BREAK CHARACTER MUST BE HELD DOWN TO INTERRUPT PROGRAM EXECUTION UNTIL THE KEYBOARD IS POLLED. THERE ARE EXTREMELY RARE (FORTUNATELY) KEYBOARDS THAT DO NOT GENERATE STABLE OUTPUT DATA WHEN THE KEYS ARE DEPRESSED. DO NOT USE THIS TYPE OF KEYBOARD.

MOST KEYBOARDS HAVE EXTRA KEYS THAT ARE NOT CONNECTED TO THE ENCODER, BUT MAY BE USED INDEPENDENTLY. IT IS CONVENIENT TO CONNECT ONE OF THESE KEYS TO PIN 75 ON THE BUS (PRESET) TO PERMIT JUMPING TO THE MONITOR IN THE VECTOR 1 WITHOUT USING THE RESET SWITCH ON THE FRONT PANEL.

UNDERSHOOT ON THE CLOCK (PIN 49) BUS LINE CAN IN SOME CASES CAUSE INCORRECT BAUD RATES TO BE GENERATED. IF THIS OCCURS, TERMINATE THIS BUS LINE. A 220 OHM 1/4 WATT RESISTOR SOLDERED FROM THE EYELET ABOVE PIN 49 TO THE GROUND STRIP CONNECTED TO PIN 50 WILL CORRECT THE PROBLEM.

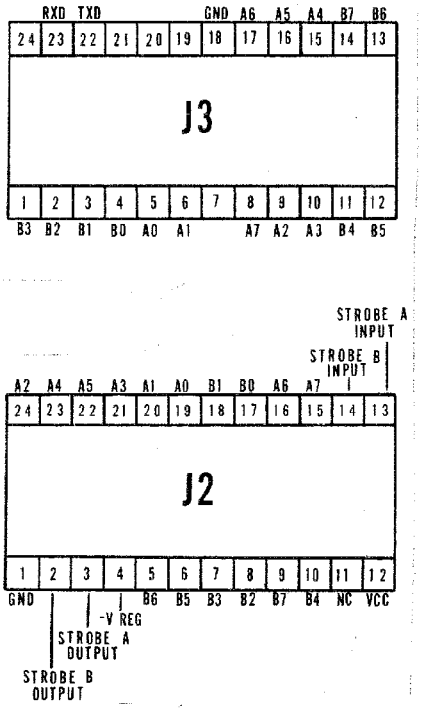


FIGURE 1

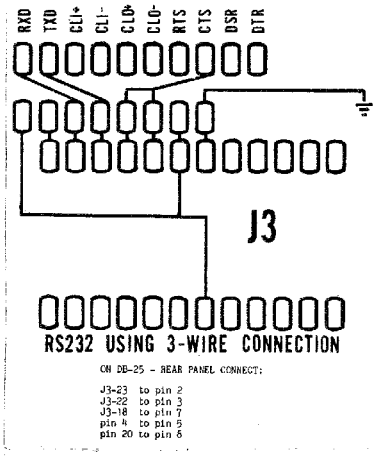


FIGURE 2

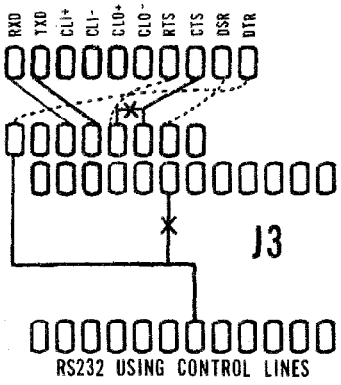


FIGURE 3-1

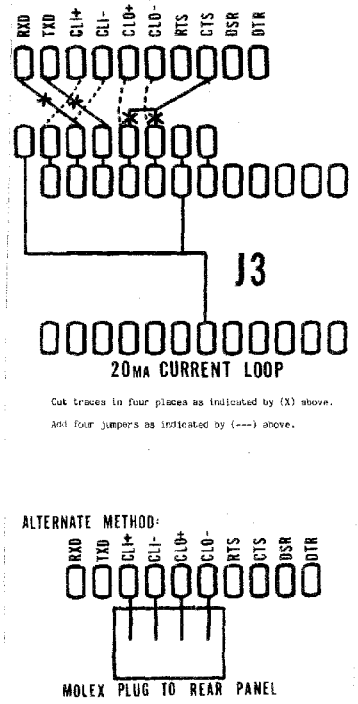
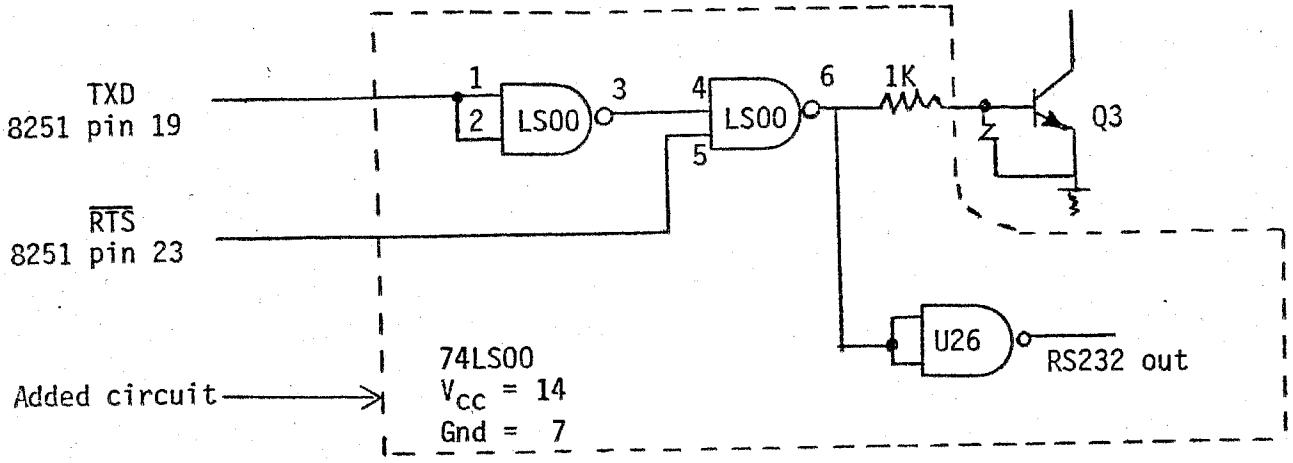


FIGURE 3-2

TTL LEVEL INPUT DEVICES SUCH AS THE TELETYPE MODEL 43 OPTION AAA (WHICH IS ABOUT $150 LESS EXPENSIVE THAN THE EQUIVALENT MODEL WITH EIA LEVEL DRIVERS) CAN BE EASILY ACCOMMODATED BY REPLACING THE EIA DRIVERS U26 AND U27 WITH JUMPERS. FOR EXAMPLE, JUMPER U27-6 TO U27-7 AND JUMPER U27-8 TO U27-10. JUMPER U26-5 TO U26-6.

MODIFICATION FOR TWO SERIAL OUTPUTS



1. REMOVE R5 CONNECTED TO THE BASE OF Q3.

2. ADD A 74LS00 IN THE KLUGE AREA OF THE BOARD.

3. WIRE UP THE CIRCUIT AS SHOWN USING THE RESISTOR REMOVED IN (1) AND AN UNUSED SECTION OF U26 (1488). A PRINTER CAN BE CONNECTED TO EITHER THE CURRENT LOOP OUTPUT OR THE RS232 OUTPUT AND IT WILL BE ENABLED BY CONTROL OF THE RTS BIT BY OUTPUTTING TO PORT 3. CARE SHOULD BE TAKEN THAT THE OTHER COMMAND BITS ARE OUTPUT CORRECTLY. SOFTWARE TO ENABLE AND DISABLE THE NEW OUTPUT WOULD BE AS FOLLOWS:

```
MVI A, 27H
OUT 3          SETS RTS LOW; DISABLES 2ND OUTPUT
```

```
MVI A, 07H
OUT 3          SETS RTS HIGH; ENABLES 2ND OUTPUT
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THE MONITOR OPTION C INITIALIZES THE USART AND SETS RTS LOW, DISABLING THE SECOND OUTPUT. THE BAUD RATE CAN BE CHANGED BY DOING A SOFTWARE RESET OF THE USART AND REINITIALIZING THE USART FOR A DIFFERENT BAUD RATE FACTOR. FOR EXAMPLE, IF A VIDEO DISPLAY IS USED AT 1200 BAUD WITH THE NORMAL X16 BAUD RATE FACTOR, REINITIALIZING WITH X64 WOULD GIVE A 300 BAUD OUTPUT. IT WOULD BE NECESSARY TO USE THE REMAINING SECTIONS OF THE 74LS00 TO DISABLE THE VIDEO OUTPUT WHILE OUTPUTTING TO THE PRINTER AT THE LOWER SPEED. CARE WOULD ALSO HAVE TO BE EXERCISED TO PREVENT THE SOFTWARE RESET FROM DUMPING THE CHARACTER BEING TRANSMITTED BY THE USART. IT IS NECESSARY TO TEST THE TXE STATUS BIT TO ENSURE THIS.

GENERAL TROUBLE SHOOTING GUIDE

BECAUSE OF THE COMPLEXITY OF THE ENTIRE COMPUTER SYSTEM, BOTH HARDWARE AND SOFTWARE, IT IS ESSENTIAL TO ISOLATE ANY PROBLEM TO AN INDIVIDUAL BOARD OR PROGRAM. FORTUNATELY, ALL OF THE COMPUTER LOGIC IS ON EASILY REMOVABLE BOARDS. IT IS EXTREMELY VALUABLE TO HAVE ACCESS TO A TESTED COMPUTER SO THAT THE BOARDS CAN BE INDIVIDUALLY TESTED. ALTHOUGH THERE IS THE POSSIBILITY OF INTERACTION BETWEEN BOARDS DUE TO MARGINAL TIMING OR DEFECTIVE COMPONENTS, THIS IS NOT THE USUAL CASE, AND IT IS BEST TO ASSUME THAT IF A BOARD WORKS IN COMPUTER "A" IT WILL ALSO WORK IN COMPUTER "B".

THE MINIMUM SYSTEM CONSISTS OF THREE BOARDS: THE CPU BOARD, THE PROM/RAM BOARD, AND EITHER A VIDEO OR SERIAL I/O BOARD. MAKE SURE THAT THE MONITOR PROGRAM HAS BEEN PROPERLY PATCHED FOR THE PARTICULAR I/O CONFIGURATION OF YOUR SYSTEM. THERE IS TOTAL CONFUSION IN THE INDUSTRY CONCERNING PORT ASSIGNMENTS, LOGIC CONVENTIONS, AND STRAPPING OPTIONS. SEVERAL TYPES OF PROGRAMMABLE USARTS ARE USED WHICH REQUIRE INITIALIZATION.

IF YOU HAVE CAREFULLY FOLLOWED THE ASSEMBLY INSTRUCTIONS FOR EACH OF THE BOARDS AND THE REGULATORS CHECK OUT, INSTALL ALL CHIPS. LET'S ASSUME YOU ARE USING A VIDEO DISPLAY. AS SOON AS YOU TURN THE COMPUTER ON, YOU SHOULD SEE A DISPLAY OF RANDOM MEMORY GARBAGE ON THE TV SCREEN. THIS WILL BE INDEPENDENT OF ANY FUNCTIONING OF THE COMPUTER OTHER THAN THE CLOCK OSCILLATOR. IF YOU DO NOT GET A PROPER DISPLAY, THE VIDEO INTERFACE MUST BE DEBUGGED FIRST. FEEL THE CHIPS ON THE BOARD. ANY THAT ARE HOT TO THE TOUCH MAY BE IN BACKWARD (PROBABLY DESTROYED IF TTL) OR MAY HAVE THEIR OUTPUTS SHORTED. THERE IS MORE THAN A FACTOR OF TEN DIFFERENCE IN THE POWER DISSIPATION OF TTL CHIPS, BUT THEY SHOULD NOT BE UNCOMFORTABLY HOT TO THE TOUCH.

REMOVE THE BOARD AND INSPECT IT CAREFULLY. ABOUT HALF OF THE PROBLEMS CAN BE FOUND SIMPLY BY VISUAL INSPECTION. LOOK WITH A MAGNIFYING GLASS OR INSPECTION SCOPE AT EACH PIN ON THE BOTTOM FOR UNSOLDERED PINS, MISSING PINS THAT MAY BE BENT UNDER OR BROKEN OFF, SOLDER BRIDGES BETWEEN PINS OR TO ADJACENT TRACES, AND ETCH BRIDGES BETWEEN TRACES (VERY HARD TO SEE). A CAREFUL EXAMINATION WILL TAKE 15 MINUTES, BUT MAY SAVE YOU A LOT OF GRIEF, AND YOU MAY DISCOVER PROBLEMS LIKE UNSOLDERED PINS THAT MAY REVEAL THEMSELVES ONLY LATER AS INTERMITTENT PROBLEMS. EXAMINE THE TOP OF THE BOARD TO BE SURE THE PROPER CHIPS ARE INSTALLED IN THE RIGHT PLACES. SIGHT ALONG THE EDGE OF THE CHIPS TO FIND BENT UNDER PINS. CHIPS ARE SOMETIMES INSERTED WITH A WHOLE ROW OF PINS THAT MISS THE SOCKET HOLES.

IF THE VISUAL INSPECTION FAILS TO GET THE VIDEO DISPLAY WORKING, A COMPONENT MAY BE BAD (USUALLY AN IC). TRY EXCHANGING IDENTICAL COMPONENTS TO SEE IF THE SYMPTOMS CHANGE. AT THIS POINT IT IS WISE TO GO BACK AND CAREFULLY REREAD THE MANUAL TO BE SURE YOU UNDERSTAND THE WAY THE BOARD WORKS AND THAT YOU HAVE SELECTED THE PROPER JUMPER OPTIONS. AFTER THIS, YOU WILL PROBABLY WANT TO TAKE THE UNIT TO A DEALER IF YOU ARE NOT FAMILIAR WITH DIGITAL TROUBLE SHOOTING PROCEDURES, OR GO THROUGH THE CIRCUIT BLOCK BY BLOCK WITH A SCOPE OR LOGIC PROBE IF YOU ARE EXPERIENCED.

AFTER THE VIDEO DISPLAY OR SERIAL I/O IS WORKING, THE RESET SWITCH SHOULD CAUSE A "*" PROMPT TO BE WRITTEN. IF THIS DOES NOT WORK, FOLLOW THE SAME PROCEDURE ON

THE CPU AND PROM/RAM BOARDS. THE CPU BOARD CONSISTS MOSTLY OF 8097 BUS DRIVERS WHICH CAN BE EXCHANGED ONE BY ONE. THE VECTORED INTERRUPT AND REAL TIME CLOCK COMPONENTS, IC A1, ARE NOT NECESSARY IN THE BOARD AT THIS TIME AND SHOULD BE REMOVED. USING A SCOPE, EXAMINE THE OUTPUT PINS OF ALL CHIPS. LOW LOGIC LEVELS ARE NORMALLY LESS THAN 0.2 VOLTS AND HIGH GREATER THAN 3.0 VOLTS. A LEVEL OF 0.4 VOLTS MAY INDICATE SHORTS BETWEEN OUTPUTS WHERE ONE IS TRYING TO PULL HIGH AND THE OTHER LOW. A LEVEL OF 1.2 VOLTS INDICATES AN OPEN CIRCUITED INPUT. NMOS CHIPS HAVE SIMILAR LOGIC LEVELS, WHILE PMOS CHIPS CAN PULL TTL INPUTS TO -0.6V WHERE THE INPUT CLAMP DIODE LIMITS THE VOLTAGE. DO NOT BE SURPRISED AT HOW STRANGE SOME OF THE WAVEFORMS ON THE BUS LOOK, SUCH AS THE DI LINES. THERE ARE PERIODS OF TIME DURING WHICH THE BUS IS NOT BEING ACTIVELY DRIVEN, AND THE VOLTAGE MAY DRIFT DUE TO RECEIVER INPUT CURRENT. ABNORMAL OPERATION IS INDICATED PRINCIPALLY BY ABNORMAL LOGIC LEVELS MAINTAINED CONSTANT FOR AT LEAST ONE CLOCK PERIOD (500 MICROSECONDS).

ONCE YOUR BASIC SYSTEM IS WORKING, CHECK OUT OF MEMORY BOARDS AND OTHER INTERFACES IS RELATIVELY STRAIGHTFORWARD USING THE MEMORY TEST PROGRAM IN THE MONITOR, OR SIMPLE DIAGNOSTIC ROUTINES YOU CAN PROGRAM IN MEMORY ON THE PROM/RAM BOARD. AFTER YOUR SYSTEM IS UP AND RUNNING, IT SHOULD BE QUITE RELIABLE. SINCE MOST MICROCOMPUTER SYSTEMS ARE MEMORY INTENSIVE, THE MEMORY IS THE MOST LIKELY SOURCE OF COMPONENT FAILURE. A SYSTEM WITH 32K OF STATIC MEMORY MAY CONTAIN 75% OF ITS COMPONETS ON THE MEMORY BOARDS. IF A PROBLEM IS EXPERIENCED RUNNING A PROGRAM, FIRST SUSPECT THE MEMORY AND USE THE MONITOR TEST PROGRAM. WE HAVE YET TO EXPERIENCE A PROBLEM WITH OUR 8K MEMORY BOARDS THAT WAS NOT REVEALED BY THE TEST PROGRAM. IF YOU DO MUCH REARRANGING OF YOUR SYSTEM, IT IS A GOOD PRACTICE TO TEST MEMORY FOR A FEW SECONDS WHEN YOU FIRST TURN ON THE COMPUTER TO MAKE SURE THE BOARDS ARE ADDRESSED PROPERLY OR THAT THEY ARE IN THE COMPUTER. THIS MAY SAVE SOME HEAD SCRATCHING WHEN THE PROGRAM YOU HAVE JUST LOADED FAILS TO RESPOND TO YOUR EAGER KEYBOARD TOUCH. IF YOU SUSPECT TEMPERATURE SENSITIVE CHIPS, REMOVE THE COVER OF THE COMPUTER TO INTERRUPT AIR FLOW BETWEEN BOARDS. WE DO NOT RECOMMEND OBSTRUCTING THE AIR FLOW THROUGH THE COMPUTER BY PLACING A SHEET OF PAPER OVER THE LEFT SIDE. A FULL COMPUTER MAY DISSIPATE OVER 300 WATTS AND REACH UNACCEPTABLE TEMPERATURES IF NO AIRFLOW IS PERMITTED.

PARALLEL PORTS
34 PIN CONNECTOR
BITSTREAMER II

1	D7 OUT	18	——— +12
2	DØ OUT	19	GND
3	D1 OUT	20	GND
4	D2 OUT	21	GND
5	D3 OUT	22	GND
6	D4 OUT	23	GND
7	D5 OUT	24	GND
8	D6 OUT	25	GND
9	———	26	GND
10	D3 IN	27	GND
11	DØ IN	28	GND
12	D1 IN	29	GND
13	D2 IN	30	GND
14	GND	31	——— +5V
15	D7 IN	32	D4 IN
16	GND	33	D5 IN
17	——— -12	34	D6 IN

RS-232 SERIAL PORTS
DB-25 TO 16 PIN DIP
BIT STREAMER II

DB-25	J1,J2,J3 16 PIN DIP	RS-232 Name	8251 FUNCTION Direction from board	
1	16	PROTECTIVE GROUND		GND
2	15	TRANSMIT DATA	(INP)	RXD
3	14	RECEIVE DATA	(OUT)	TXD
4	13	REQUEST TO SEND	(INP)	RTS*
5	12	CLEAR TO SEND	(OUT)	CTS*
6	11	DATA SET READY	(OUT)	DSR*
7	10	SIGNAL GROUND		SGND
8	9	CARRIER DETECT	(OUT)	CD*
14	1			
15	2			
16	3			
17	4			
18	5			
19	6	OPTION PAD		
20	7	DATA TERMINAL READY	(INP)	DTR
21	8			

* Depends on jumpering — See section on full RS-232-C protocol.

8251 Tx rate of 19.2 is a nominal.

PORT ADDRESSES AND SOCKETS

CHANNEL	PORT ADDRESSES (Unmodified board)	FUNCTION	CONNECTOR	
Serial - A	Ø2	Commands + Status	J3	16-pin sockets on right side
	Ø3	Data		
Serial - B	Ø4	Commands + Status	J2	"
	Ø5	Data		
Serial - C	Ø6	Commands + Status	J1	"
	Ø7	Data		
Parallel - A	Ø8	Data	J4	34-pin molex on top of board
Parallel - B	Ø9	Data	J5	"