

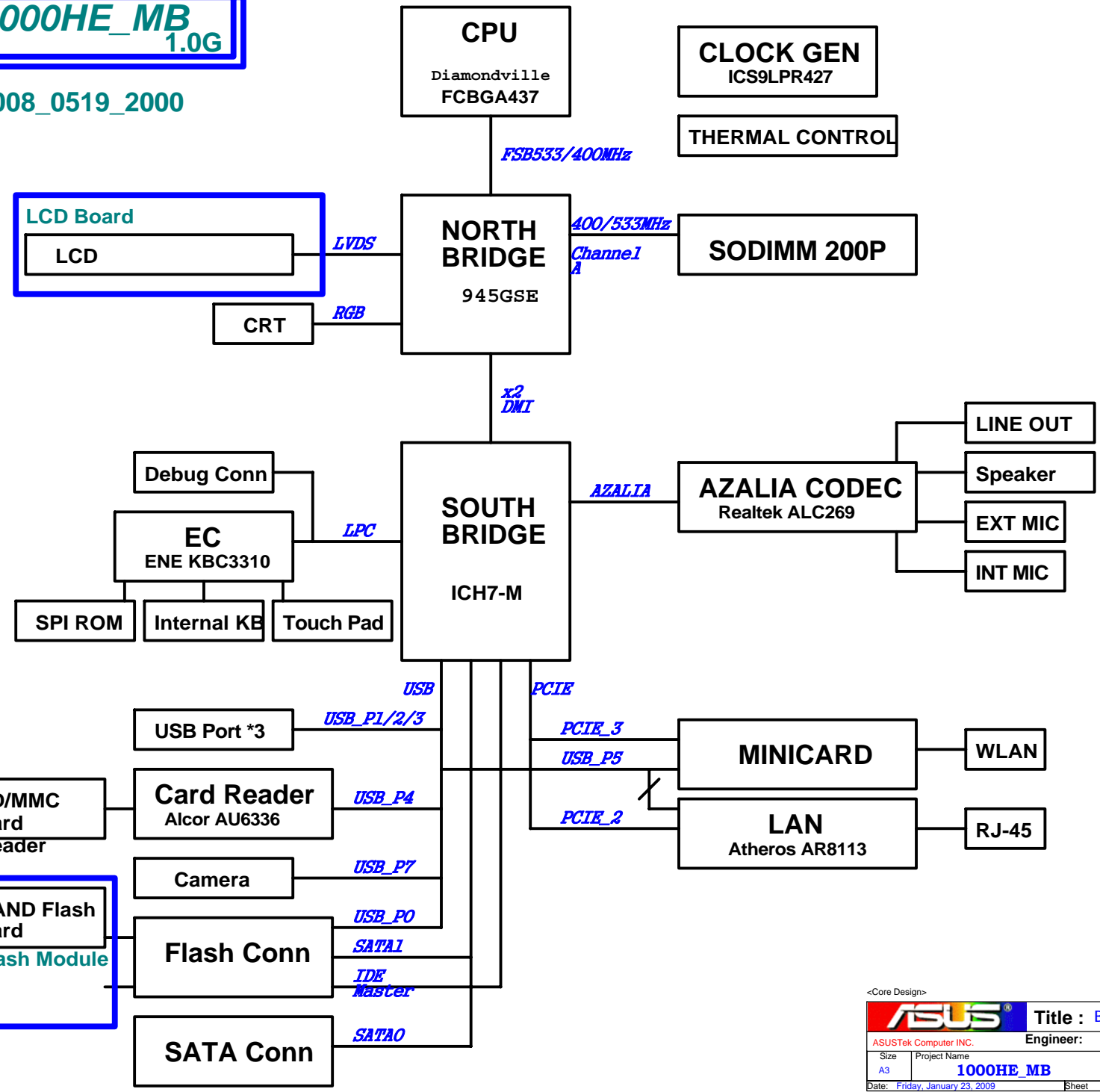
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- 06_Diamondville_PWR
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- 08_NB-945GMS(DMI)
- 09_NB-945GMS(GRAPHIC)
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1000HE_MB
1.0G

2008_0519_2000

LCD Board
LCD

NAND Flash Card
Flash Module



5

4

3

2

1


D

C

B

A

<Core Design>

		Title : History	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size	Project Name		Rev
A3	1000HE_MB		1.0G
Date: Friday, January 23, 2009		Sheet	2 of 47

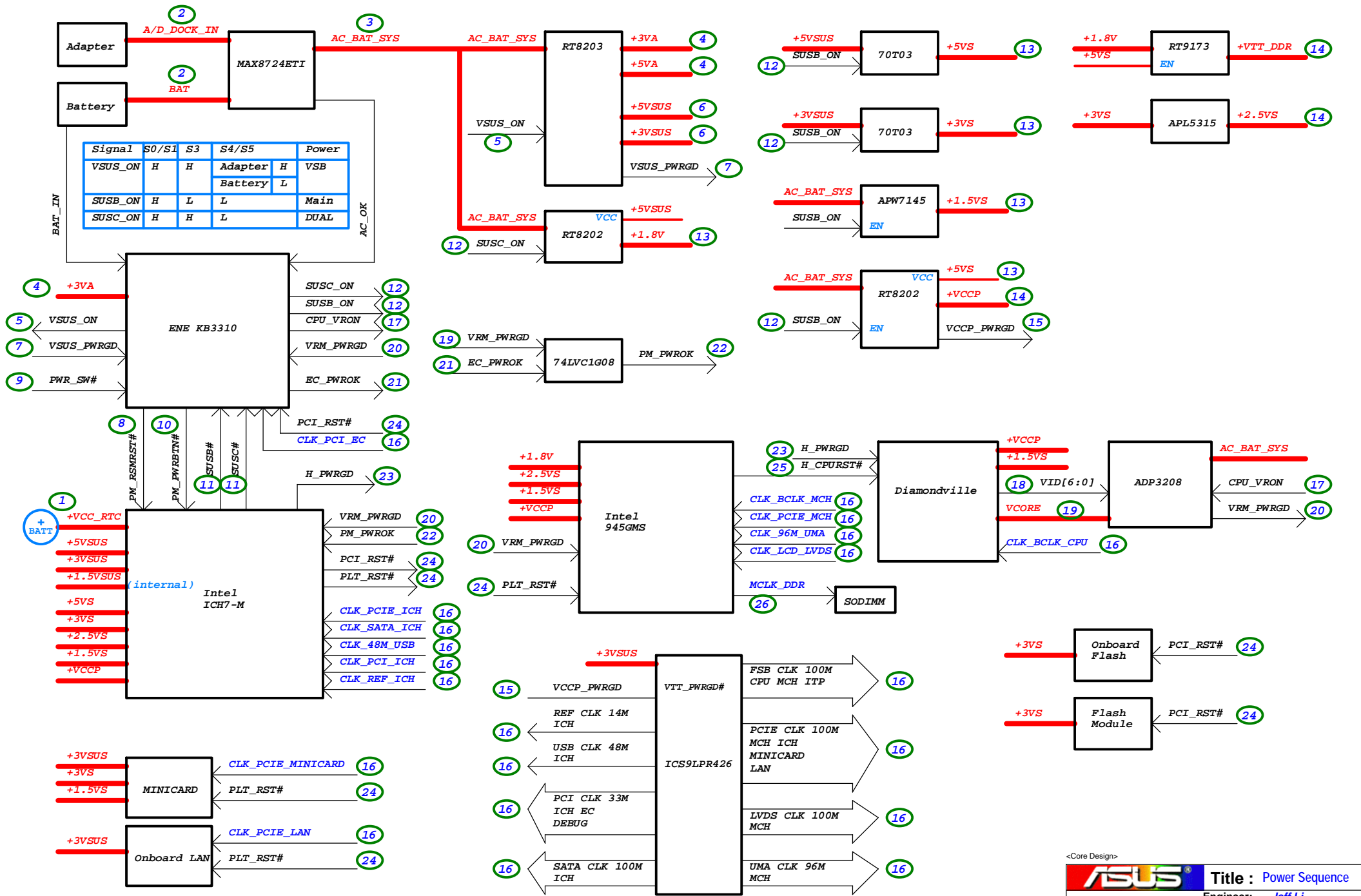
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4

3

2

1



EC KB3310 GPIO SETTING


Pin	Pin Name	Signal Name	Type	Note
1	GPIO0/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO4	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMH#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

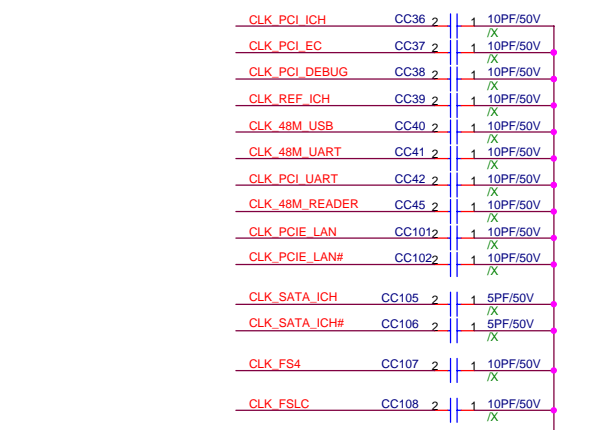
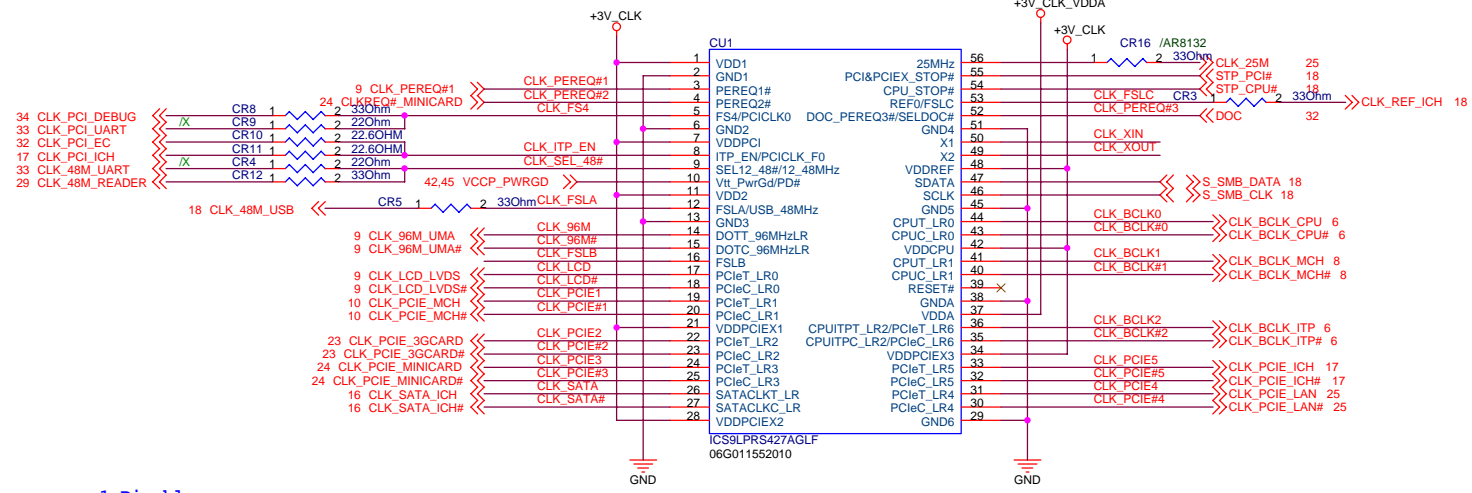
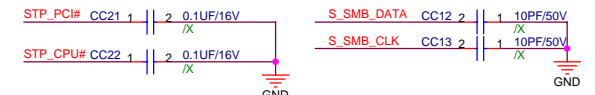
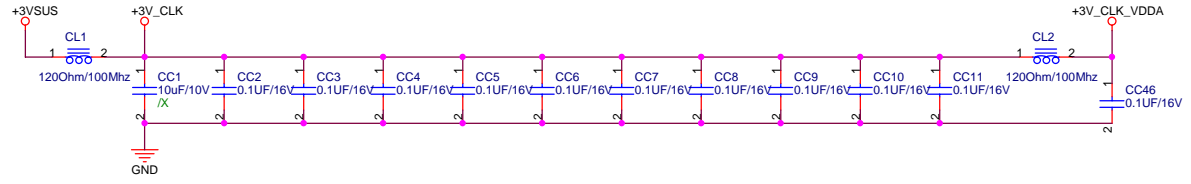
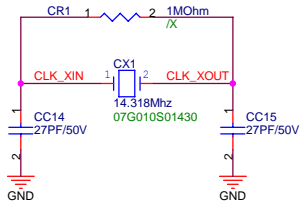
EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPL_SO	I	
120	WR#/SPIDO	SPL_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPL_CE#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCR_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

<Core Design>

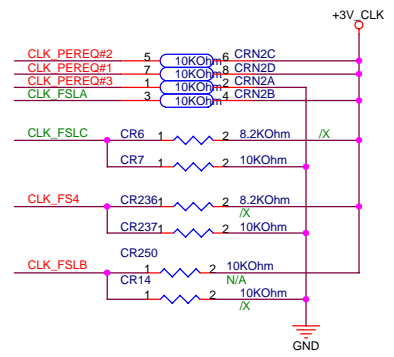
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ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000H_MB		1.0G
Date: Friday, January 23, 2009	Sheet	4	of 47

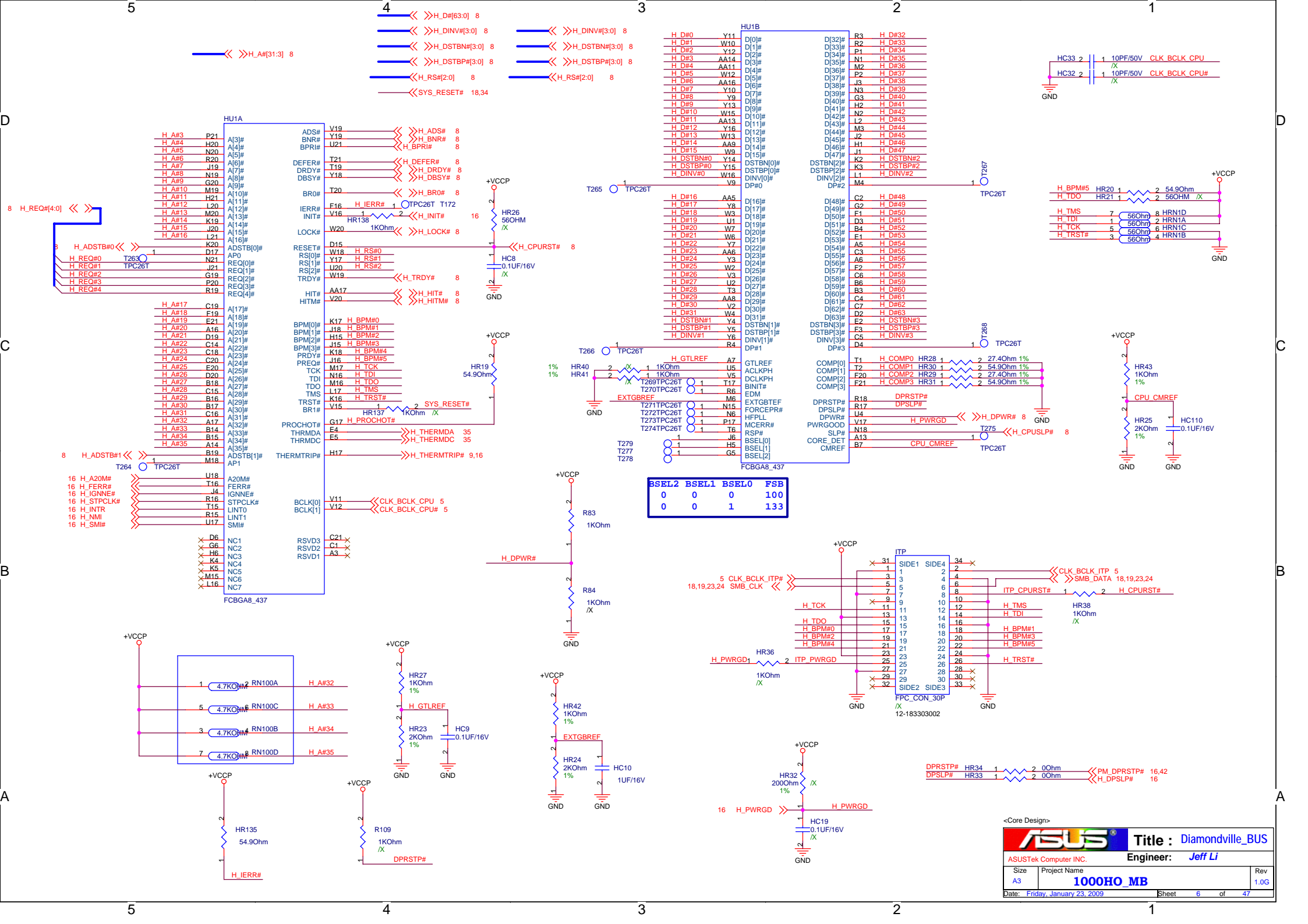


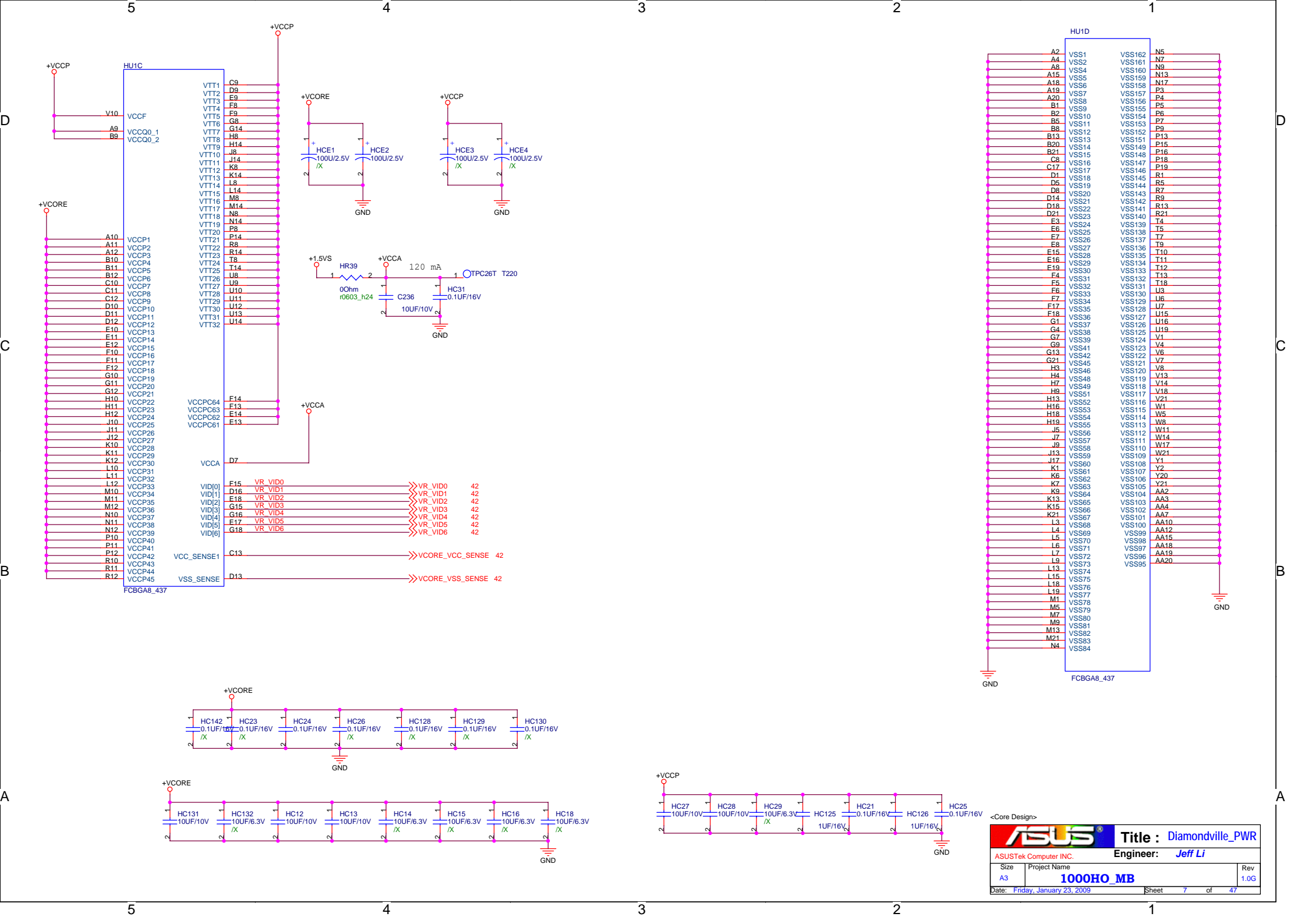
1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	1	1	166	100	100
0	0	1	133	100	100
1	0	1	100	100	100



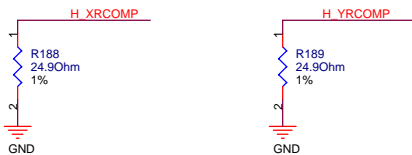




**Power:
+VCCP**

RCOMP

For Calibrating the FSB I/O Buffer



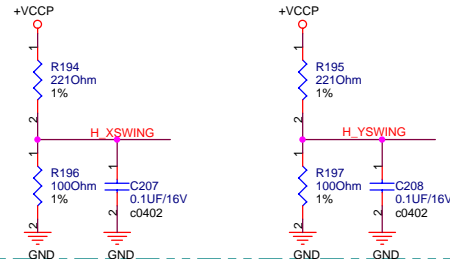
SCOMP

For Slew Rate Compensation on the FSB

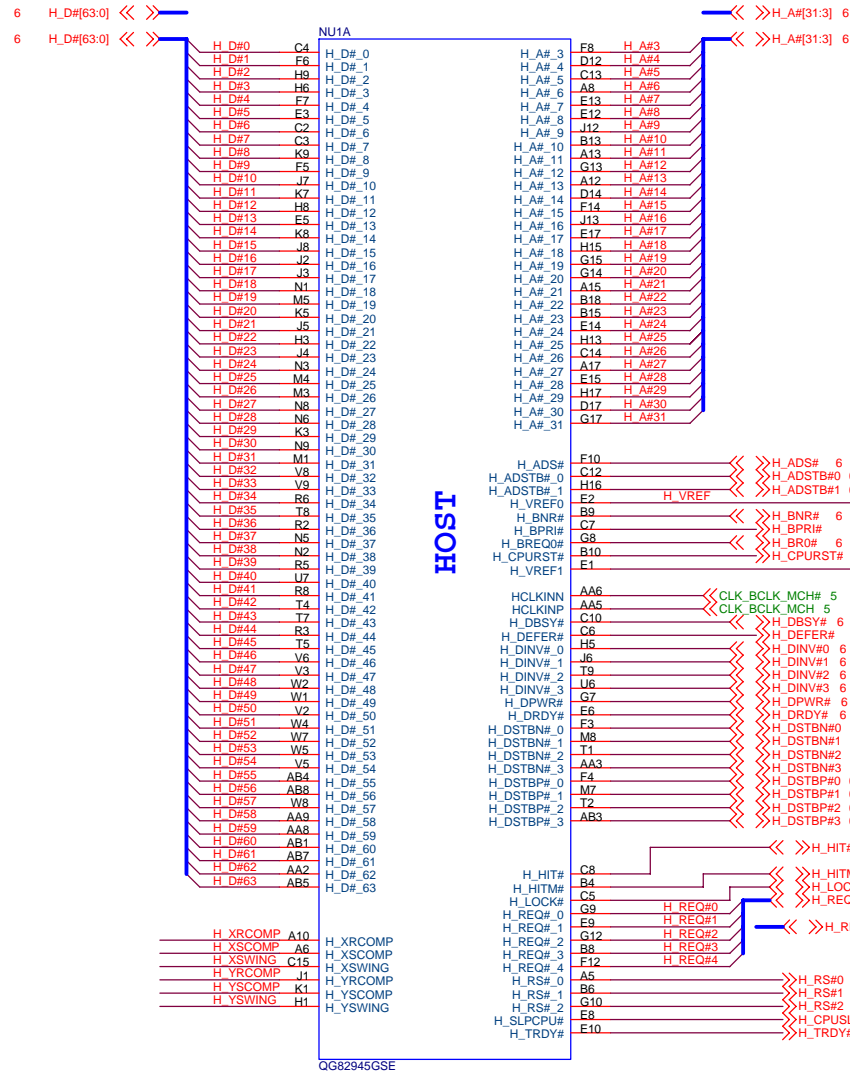


Voltage Swing

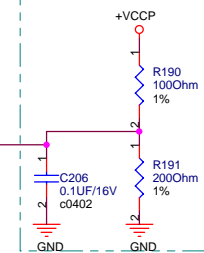
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing

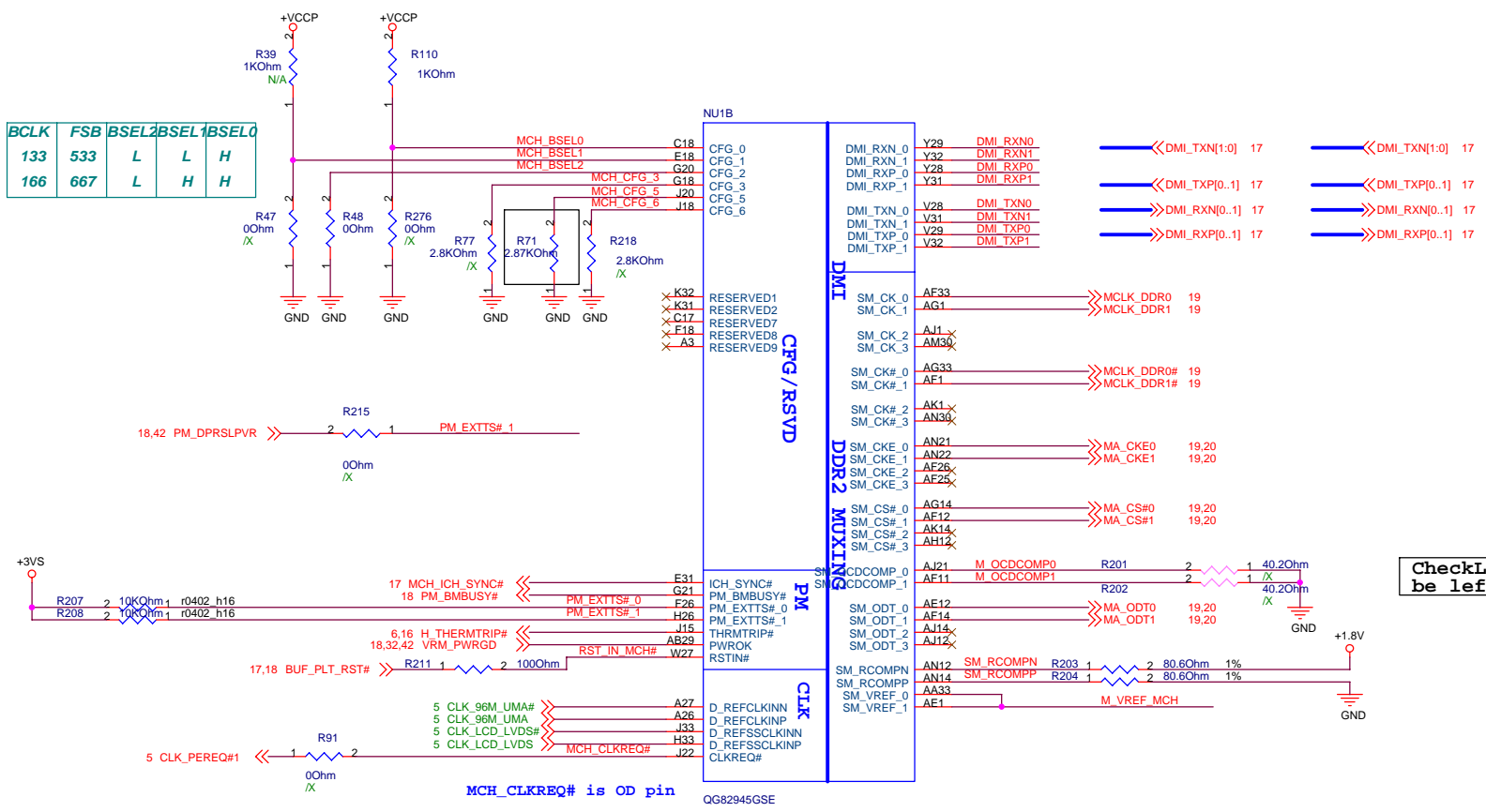


AGTL+ I/O Voltage Reference

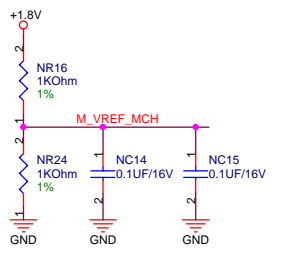


Layout Note:
0.1uF should be placed 100mils or
less from GMCH pin.

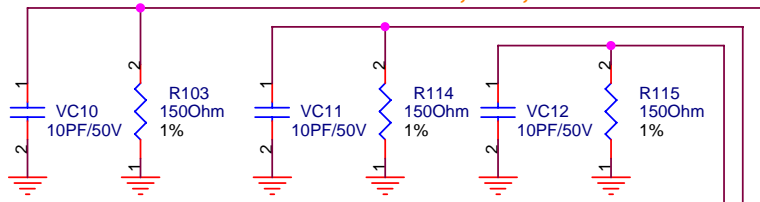
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



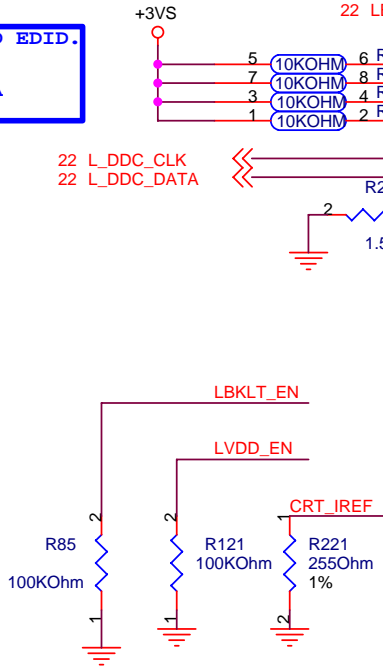
CheckList notes :Can be left as NC



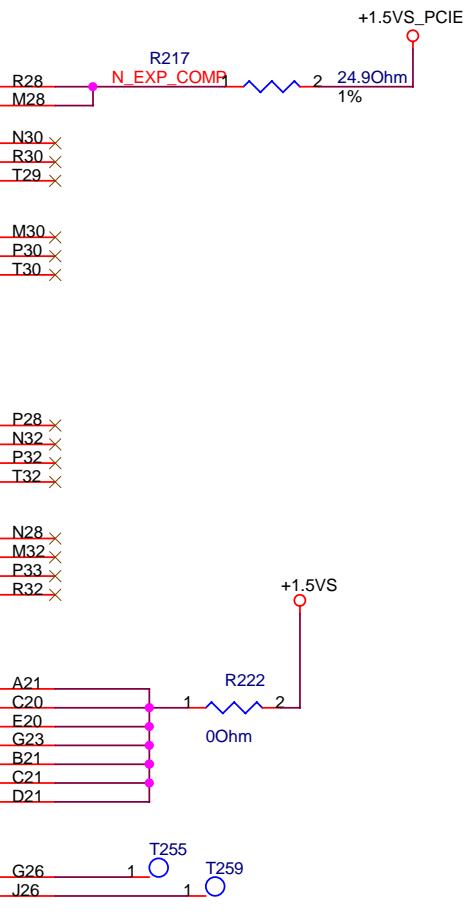
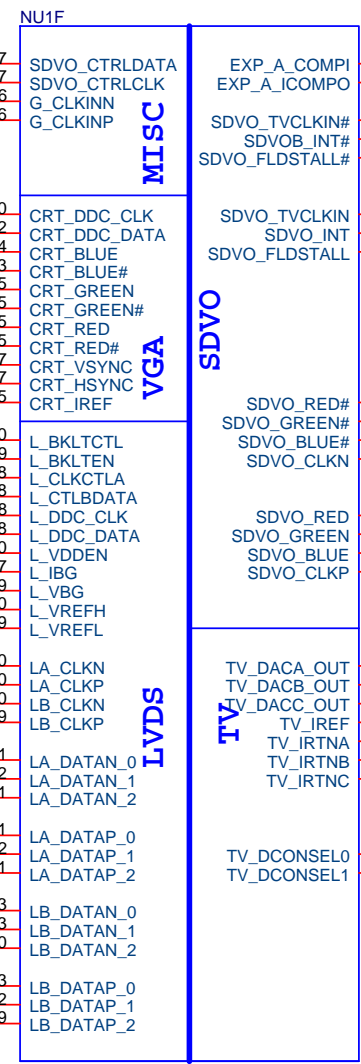
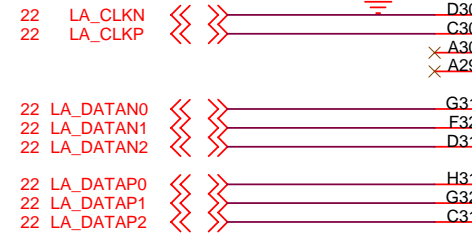
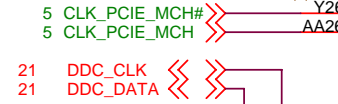
Close to GMCH
R103,R114,R115



IF USE NB READ EDID,
MUST CONNECT
L_DDC_CLK&DATA



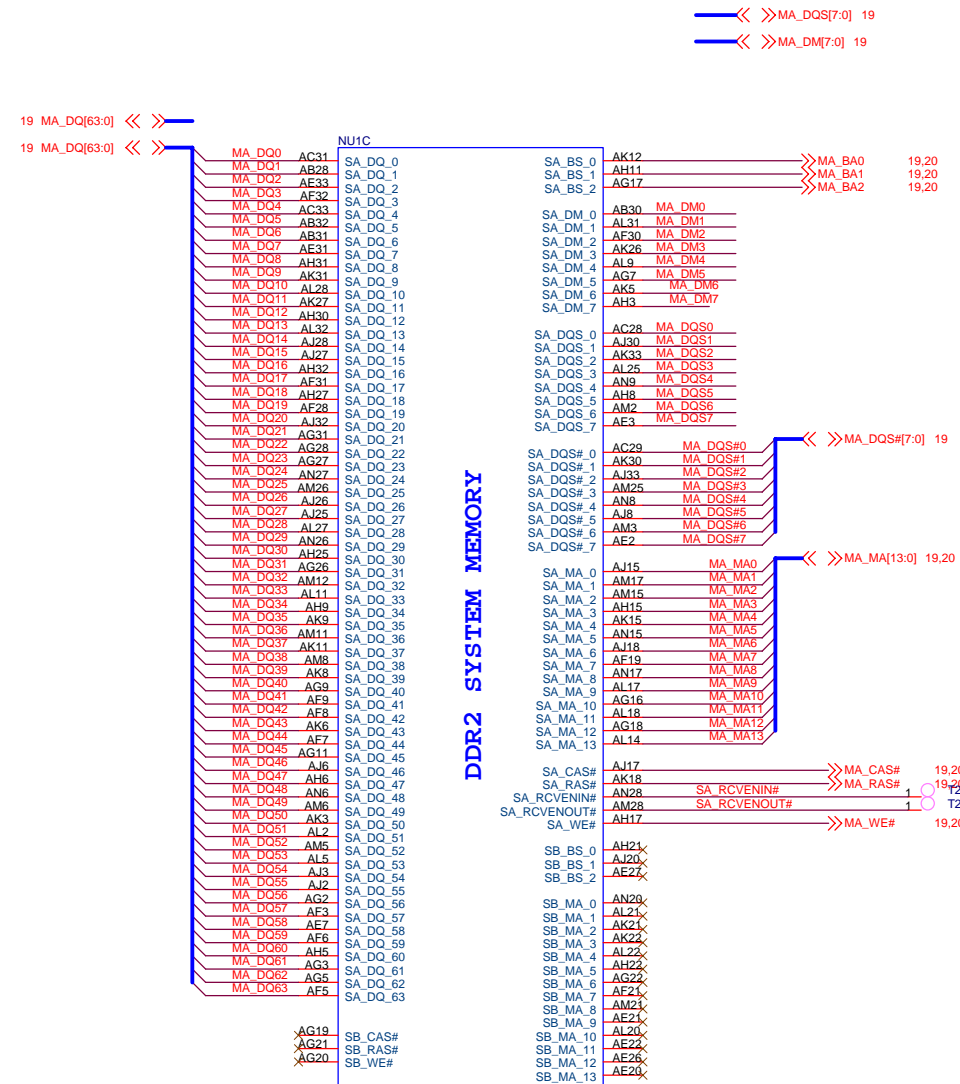
Close to GMCH



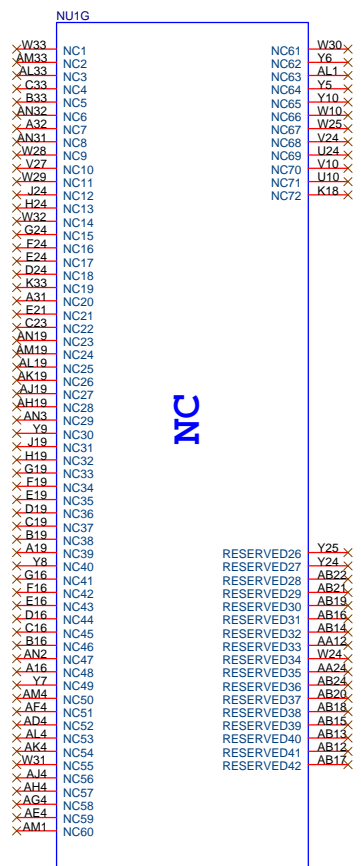
QG82945GSE

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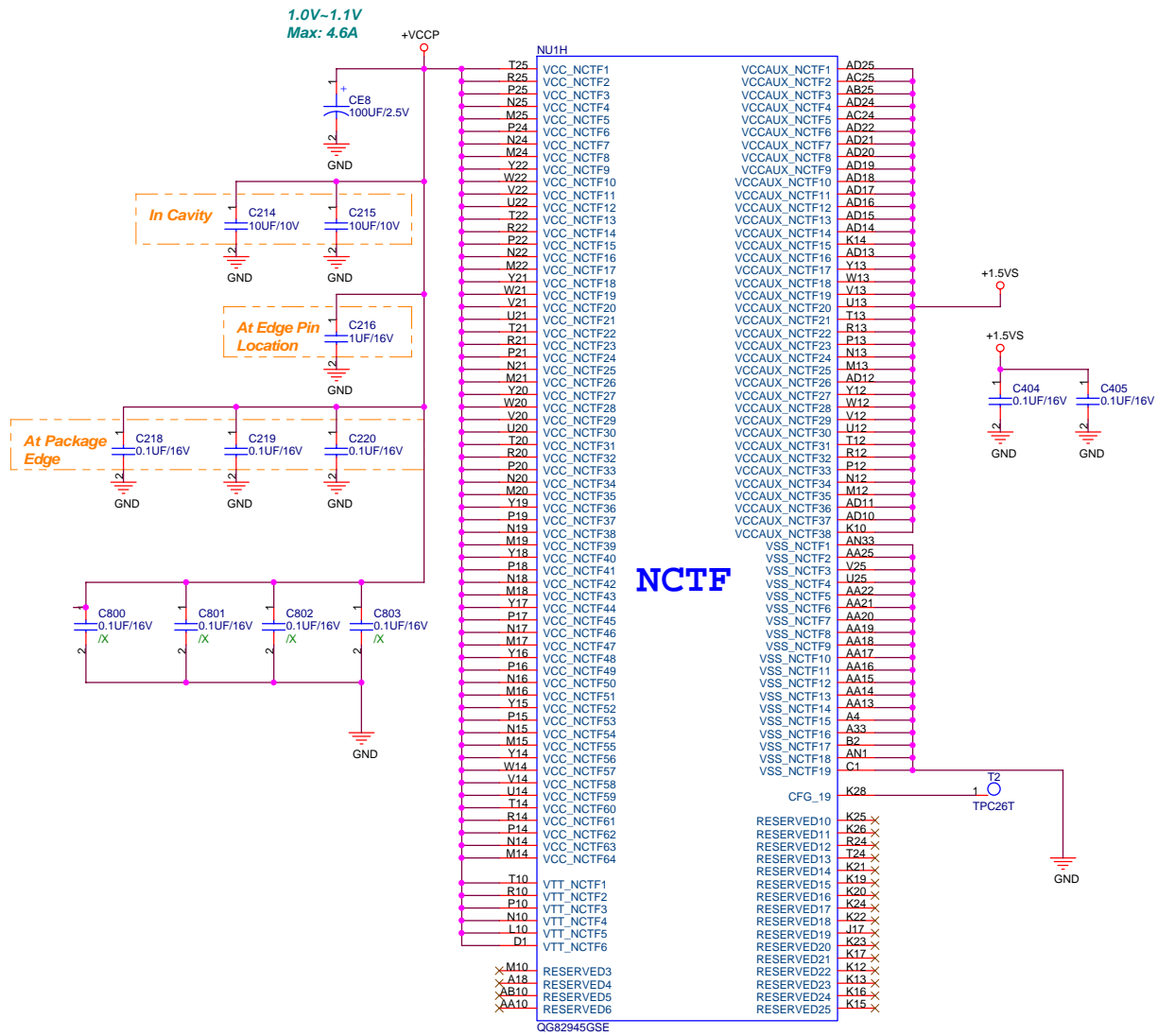
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ASUSTeK COMPUTER INC.		Engineer: <i>Jeff Li</i>	
Size A4	Project Name 1000HO_MB	Rev 1.0G	
Date: Friday, January 23, 2009	Sheet	10	of 47



QG82945GSE

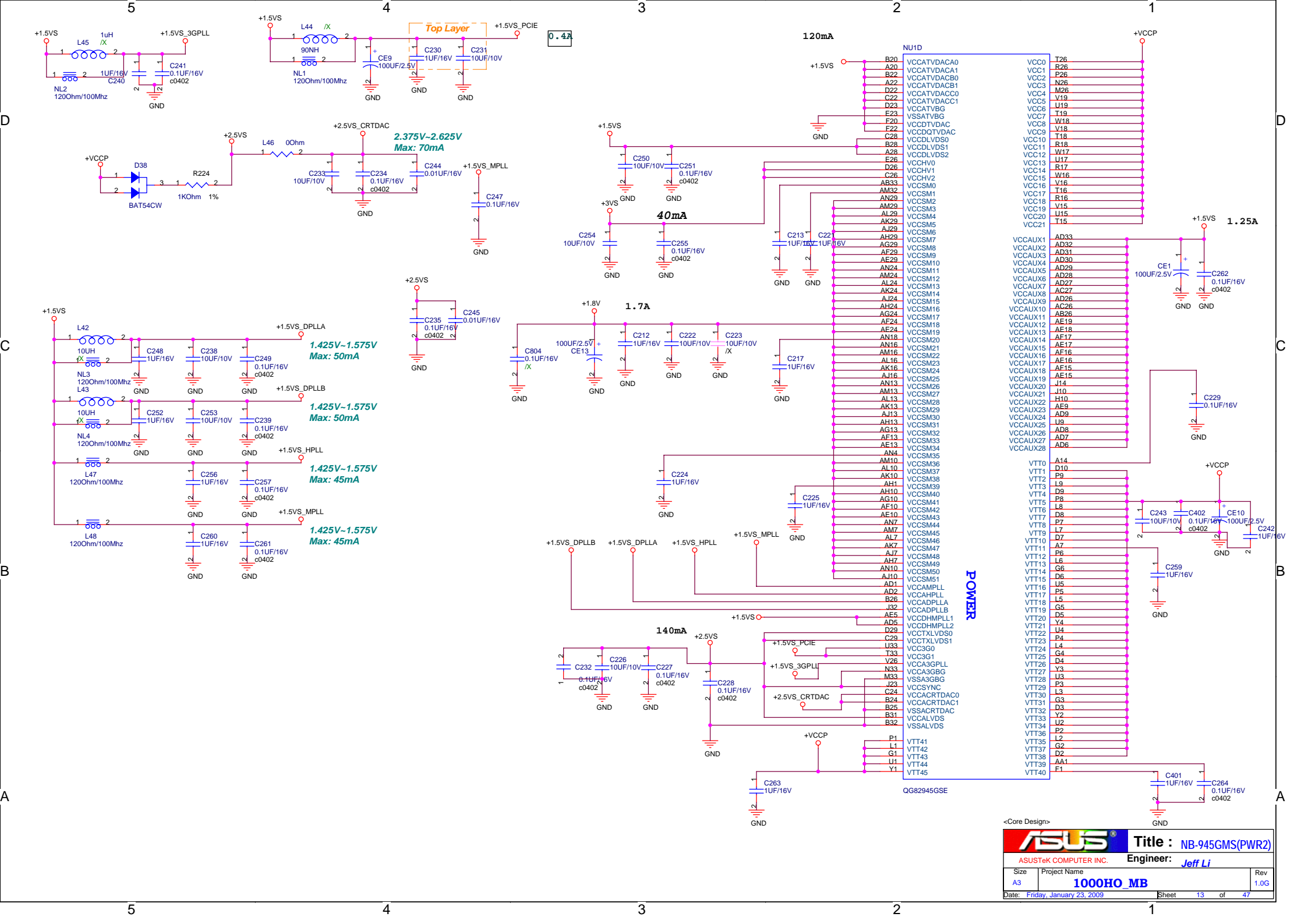


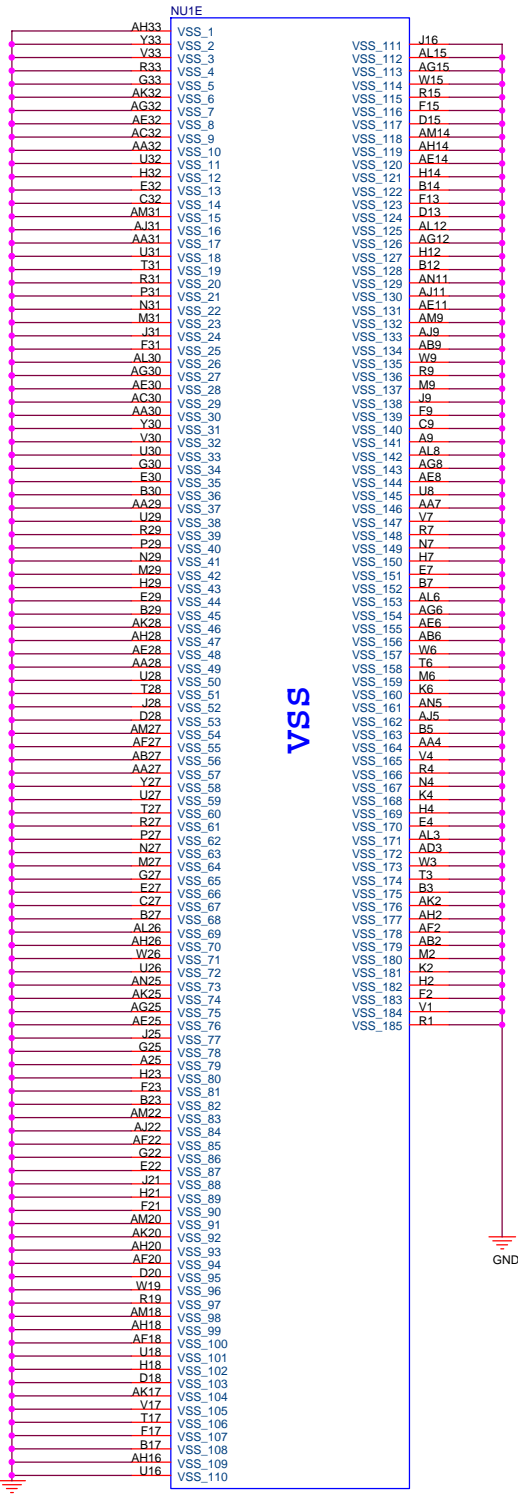
QG82945GSE



NCTF

CFG_19(K28) Strapping :
DMI LANE Reversal:
 0:Normal Operation (Default)
 1.:Reversal Lanes, 3->0,2->1..etc
 Note:945GMS doesn't support DMI Lane Reversal

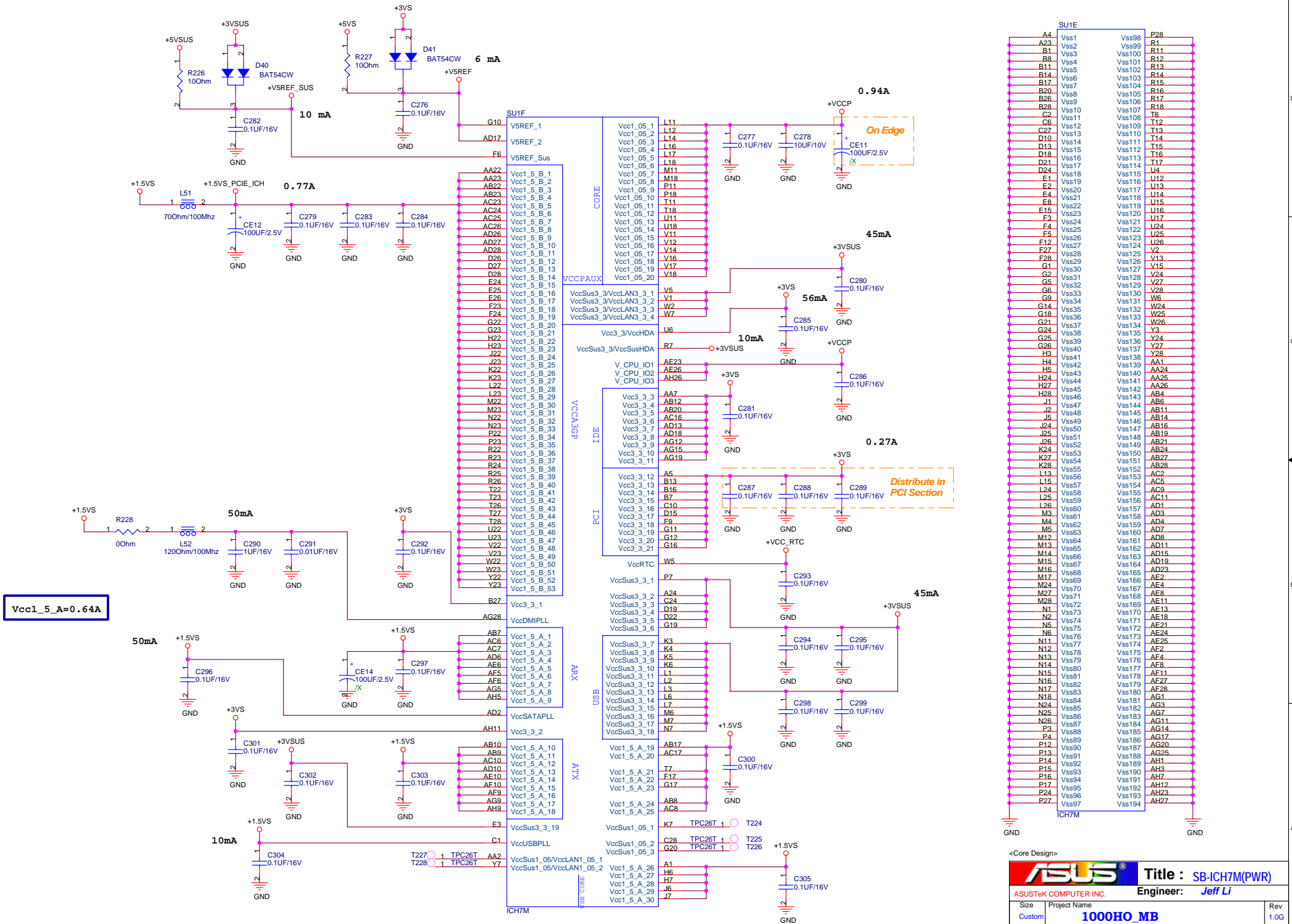




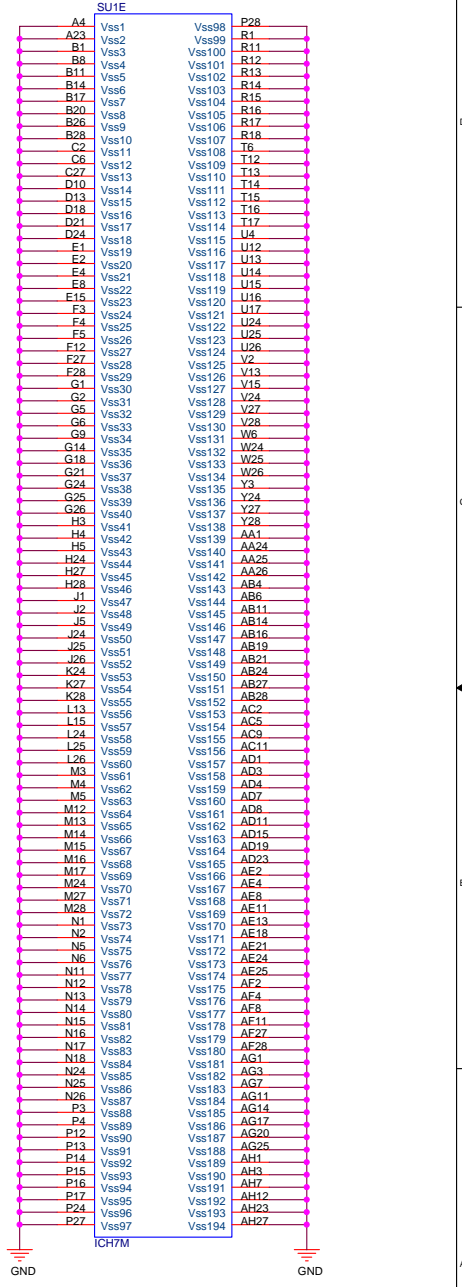
VSS

<Core Design>

		Title : NB-945PMS(GND)	
ASUSTeK COMPUTER INC.		Engineer: <i>Jeff Li</i>	
Size	Project Name	Rev	
A3	1000HO_MB	1.0G	
Date: Friday, January 23, 2009	Sheet	14	of 47

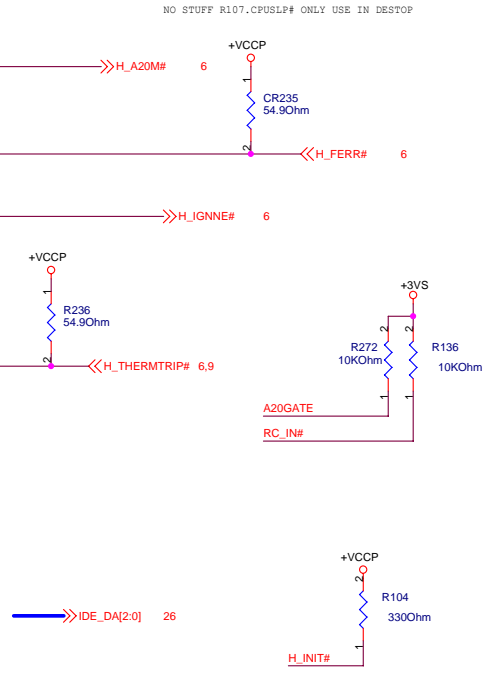
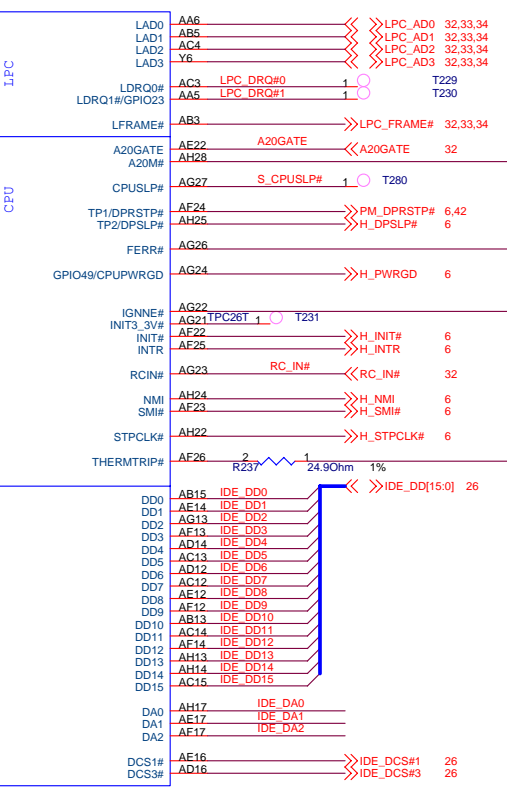
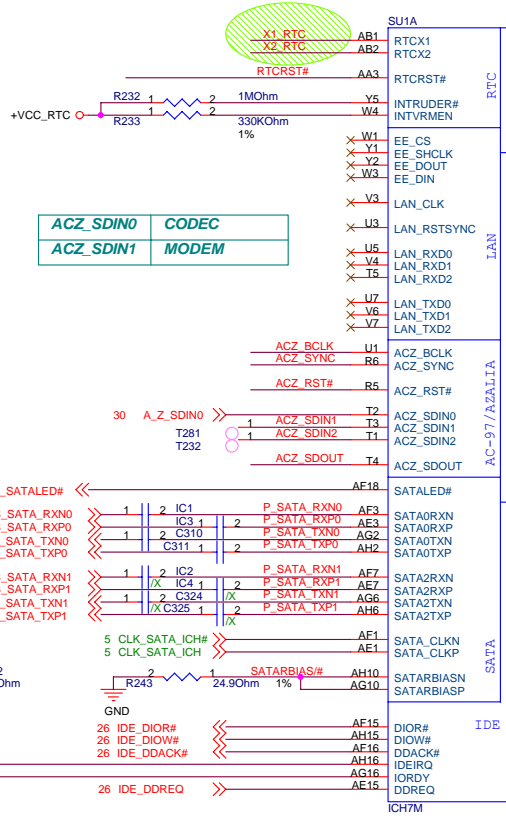
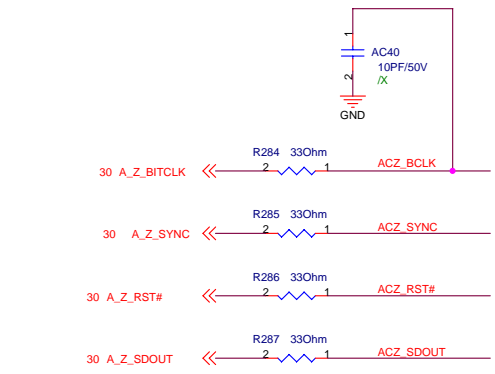
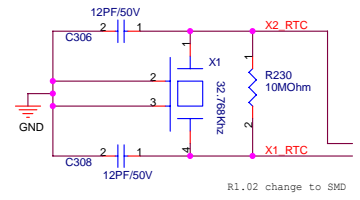
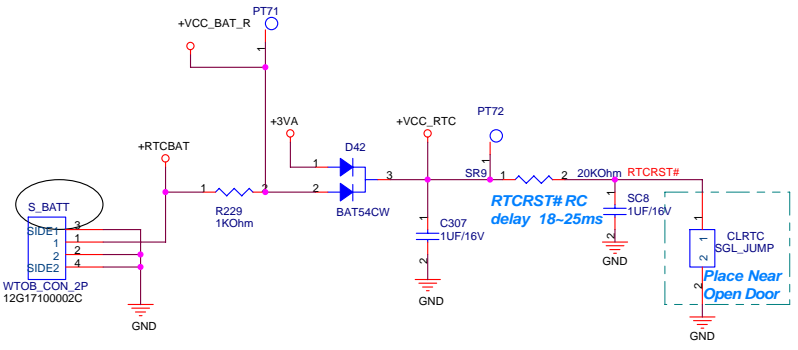


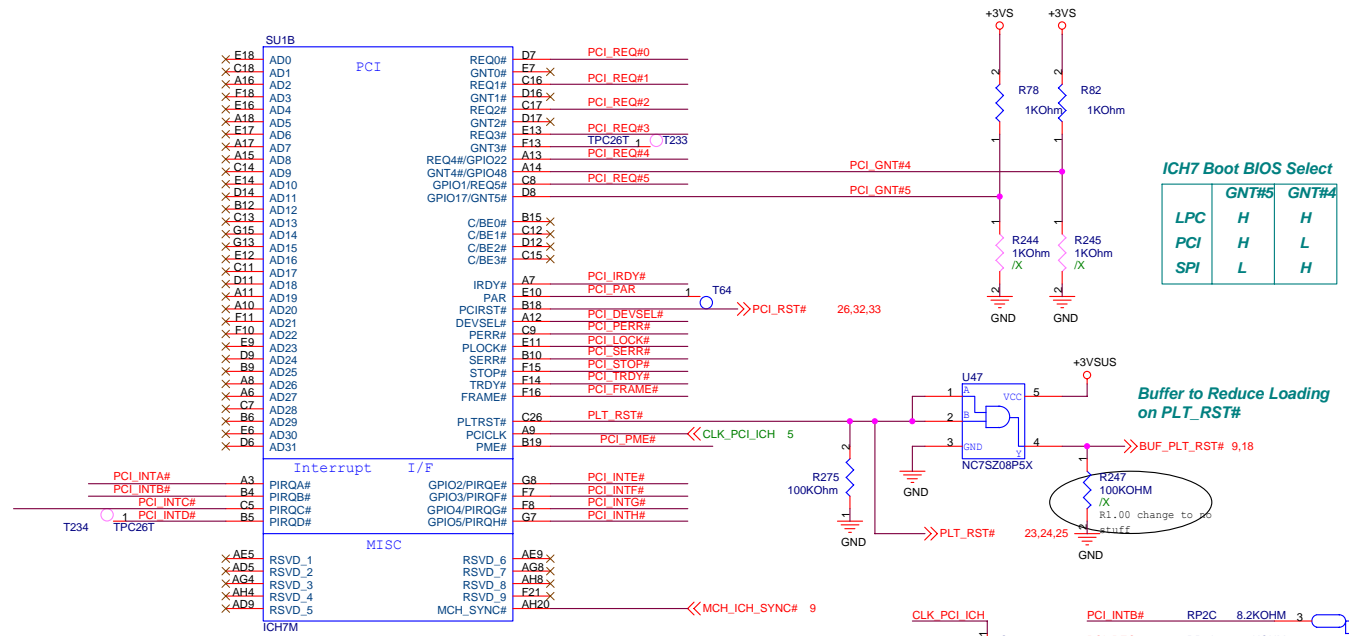
Vcc1_5_A=0.64A



<Core Design>

ASUS		Title : SB-ICH7M(PWR)
ASUSTek COMPUTER INC.		
Size		Engineer: Jeff Li
Custom		Project Name: 1000HO_MB
Date: Friday, January 23, 2009		Rev: 1.0G
Sheet		15 of 47





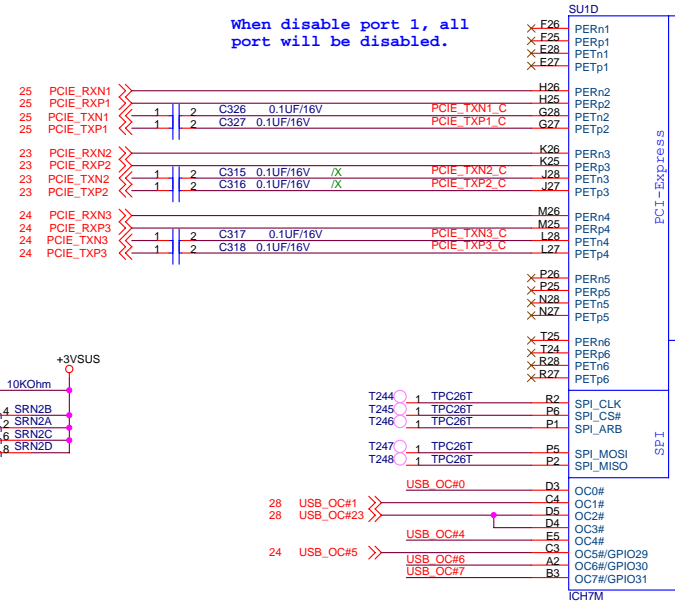
ICH7 Boot BIOS Select

	GNT#5	GNT#4
LPC	H	H
PCI	H	L
SPI	L	H

Buffer to Reduce Loading on PLT_RST#

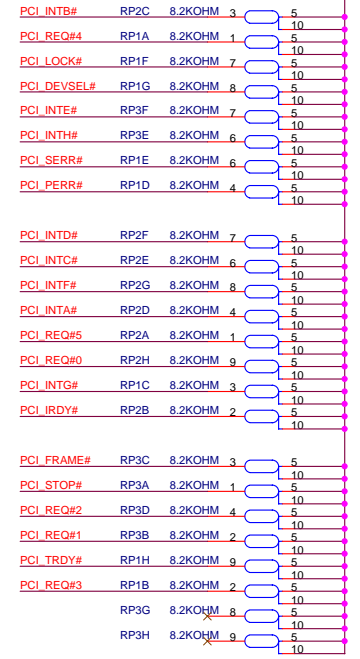
R247 100KOHM
R1.00 change to 50k
stuff

When disable port 1, all port will be disabled.

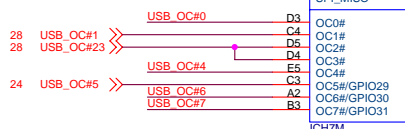
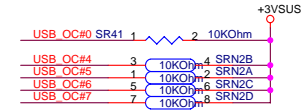


Internal Pull-Up R88

- USB 0 Flash Card
- USB 1 USB Conn
- USB 2 USB Conn
- USB 3 USB Conn
- USB 4 Card Reader
- USB 5 Minicard + 3.5G
- USB 6 Bluetooth
- USB 7 Camera



- LAN AR8113 IC
- 3.5G, GPS, DTV, Wimax
- WIFI PCIExpress Card



CRB & Checklist

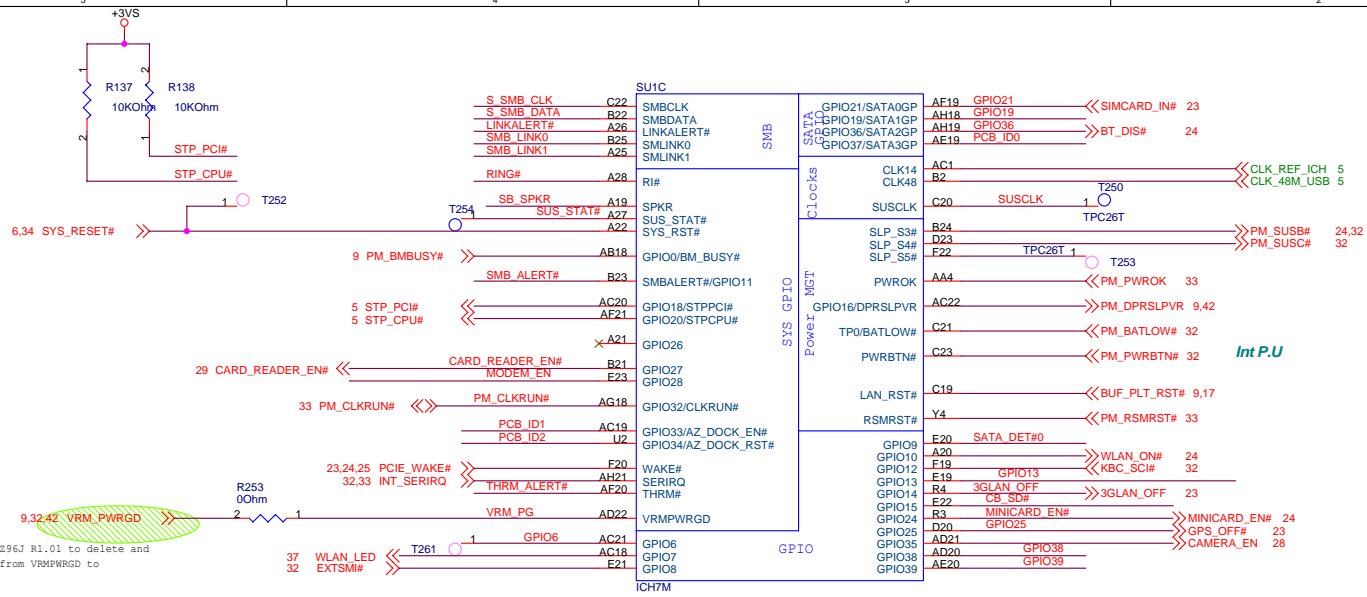
<Core Design>

ASUS Title : SB-ICH7M(2)

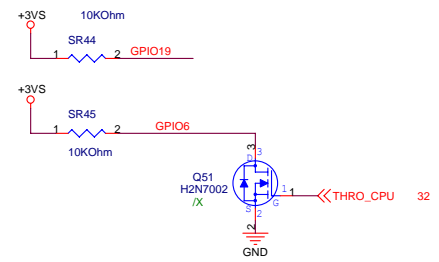
ASUSTek COMPUTER INC. Engineer: Jeff Li

Size	Project Name	Rev
Custom	1000HO_MB	1.0G

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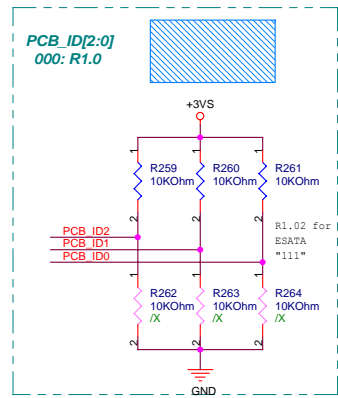
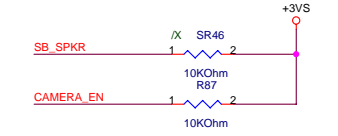
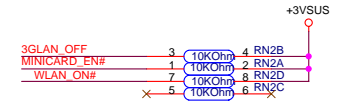
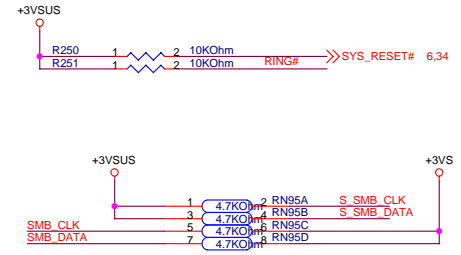
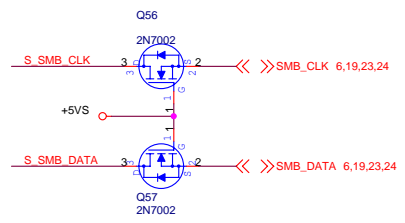


05/12/30, refer Z96J R1.01 to delete and change net name from VRMPWRGD to VRM_PWRGD.

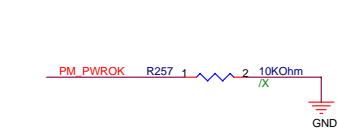
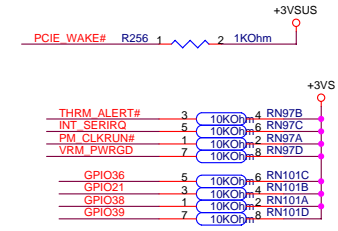
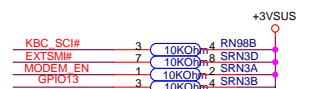
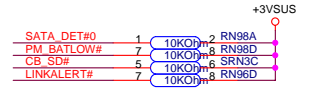
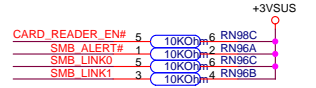


S_SMB_CLK <<< S_SMB_CLK 5
S_SMB_DATA <<< S_SMB_DATA 5

WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x

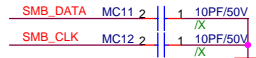
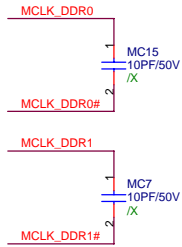


PCB_VID3 : PROJECT CODE



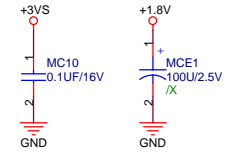
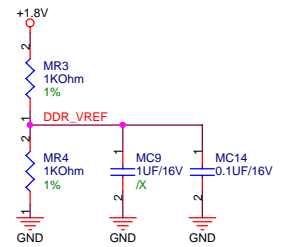
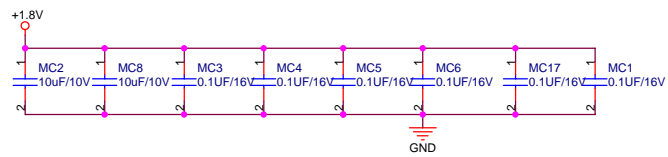
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ASUSTek COMPUTER INC		Engineer: Jeff Li	
Size	Project Name	Rev	
Custom	1000HO_MB	1.0G	
Date: Friday, January 23, 2009	Sheet 18	of 47	



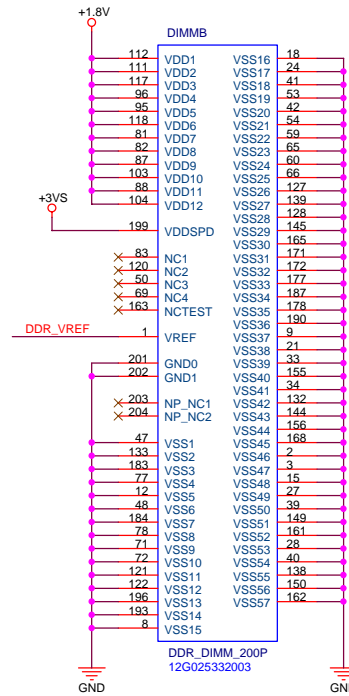
STD Type

- << >> MA_DQ[63:0] 11
- << >> MA_DQS[7:0] 11
- << >> MA_DQS#[7:0] 11
- << >> MA_DM[7:0] 11
- << >> MA_MA[13:0] 11,20
- << >> MA_BA[2:0] 11,20



DIMMA		DIMMB	
MA_MA0	102	A0	DQ0
MA_MA1	101	A1	DQ1
MA_MA2	100	A2	DQ2
MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	92	A7	DQ7
MA_MA8	93	A8	DQ8
MA_MA9	91	A9	DQ9
MA_MA10	105	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	X 86	A14	DQ14
	X 85	A15	DQ15
MA_BA2	85	A16_BA2	DQ16
MA_BA0	107	BA0	DQ17
MA_BA1	106	BA1	DQ18
	110	S0#	DQ19
9,20 MA_CS#0	X 115	S1#	DQ20
9,20 MA_CS#1	X 100	CK0#	DQ21
9 MCLK_DDR0	X 30	CK0#	DQ22
9 MCLK_DDR#	X 164	CK1#	DQ23
9 MCLK_DDR1#	X 166	CK1#	DQ24
9,20 MA_KE0	X 79	CKE0	DQ25
9,20 MA_KE1	X 80	CKE1	DQ26
11,20 MA_CAS#	X 113	CAS#	DQ27
11,20 MA_RAS#	X 108	RAS#	DQ28
11,20 MA_WE#	X 109	WE#	DQ29
	X 200	SA0	DQ30
6,18,23,24 SMB_CLK	X 197	SA1	DQ31
6,18,23,24 SMB_DATA	X 195	SCL	DQ32
	X 114	SDA	DQ33
9,20 MA_ODT0	X 114	ODT0	DQ34
9,20 MA_ODT1	X 119	ODT1	DQ35
MA_DM0	10	DM0	DQ36
MA_DM2	26	DM1	DQ37
MA_DM1	52	DM2	DQ38
MA_DM3	67	DM3	DQ39
MA_DM4	130	DM4	DQ40
MA_DM5	147	DM5	DQ41
MA_DM6	170	DM6	DQ42
MA_DM7	185	DM7	DQ43
		DM8	DQ44
		DM9	DQ45
		DM10	DQ46
		DM11	DQ47
		DM12	DQ48
		DM13	DQ49
		DM14	DQ50
		DM15	DQ51
		DM16	DQ52
		DM17	DQ53
		DM18	DQ54
		DM19	DQ55
		DM20	DQ56
		DM21	DQ57
		DM22	DQ58
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		DM26	DQ62
		DM27	DQ63



GROUP1
GROUP2
SWAP

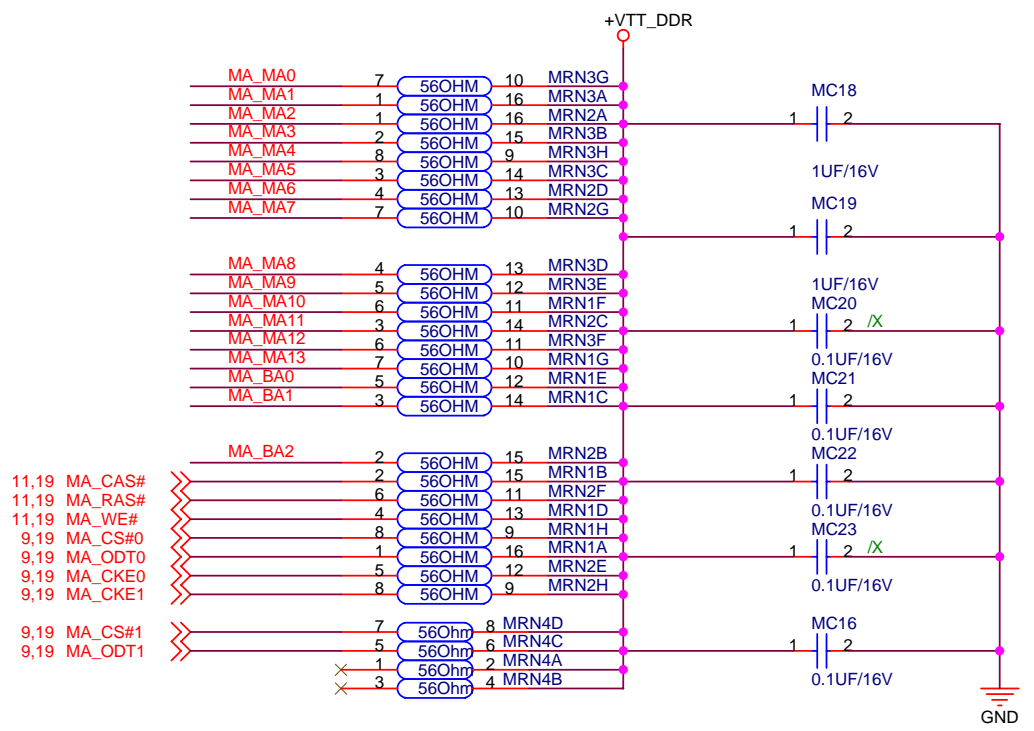


DDR_DIMM_200P
12G025332003


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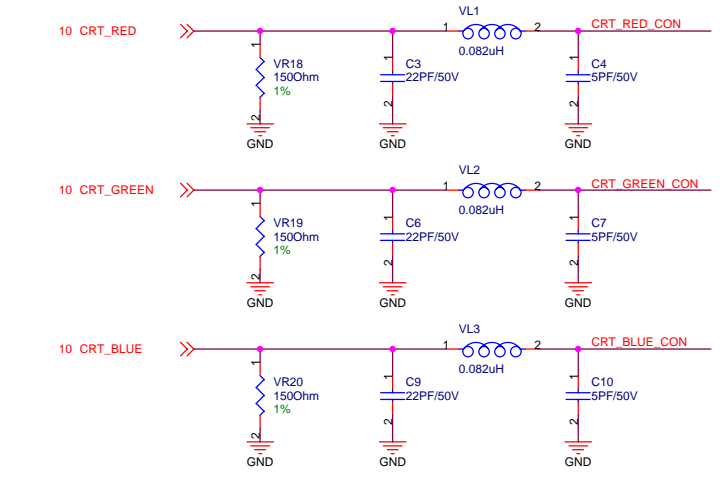
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ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000HO_MB		1.0G
Date:	Friday, January 23, 2009	Sheet	19 of 52

 << MA_MA[13:0] 11,19
 << MA_BA[2:0] 11,19

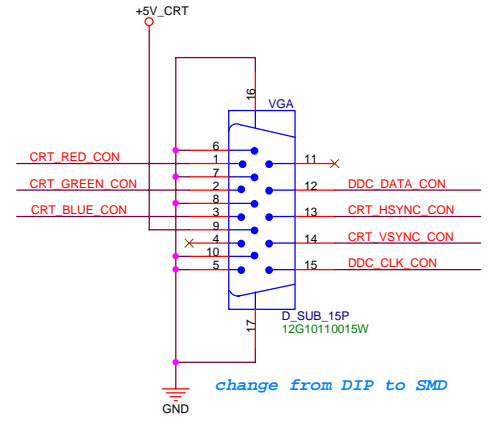
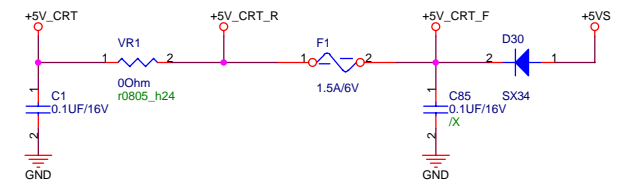
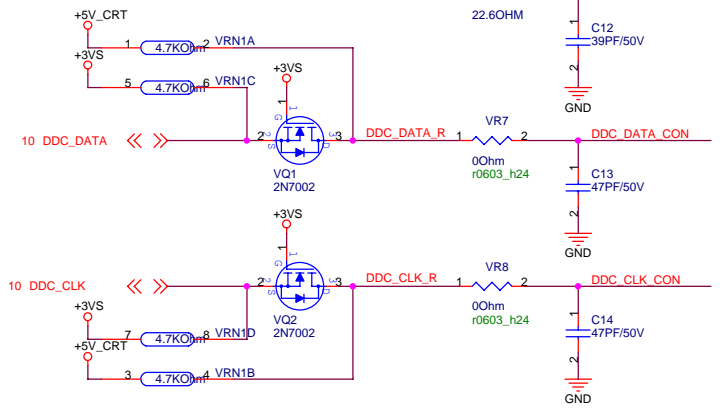


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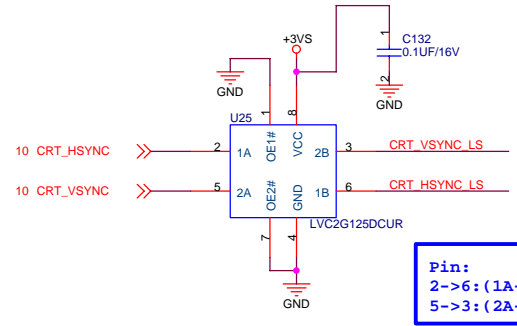
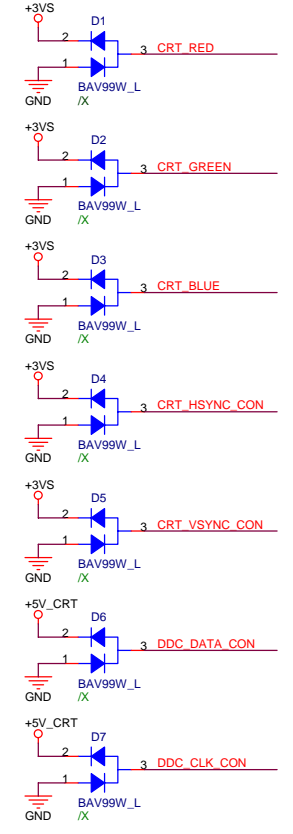
		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: <i>Jeff Li</i>	
Size A4	Project Name 1000HO_MB		Rev 1.0G
Date: Friday, January 23, 2009	Sheet	20	of 52



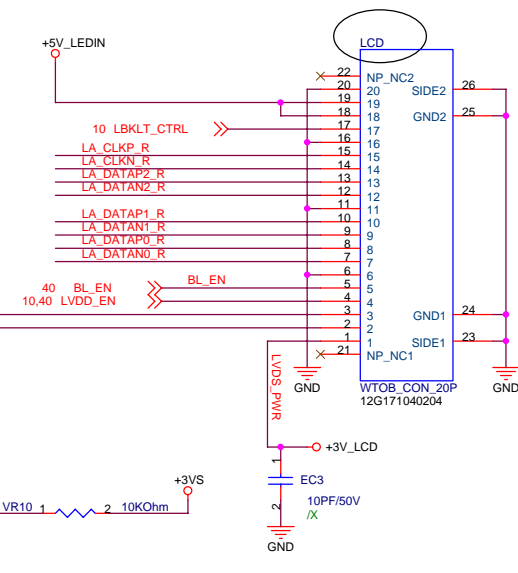
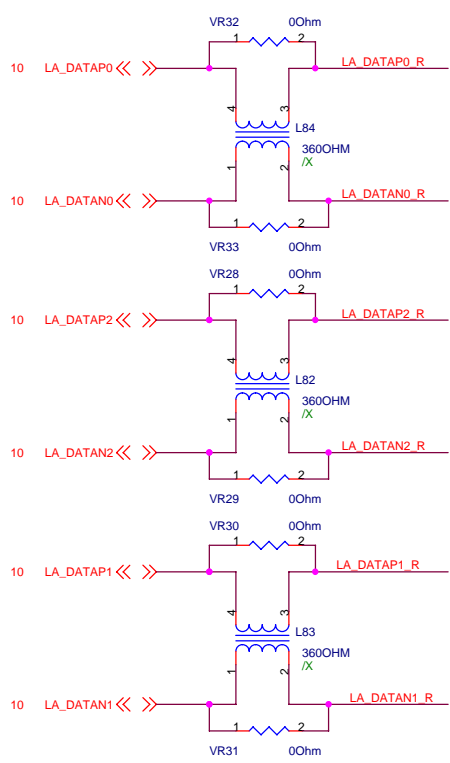
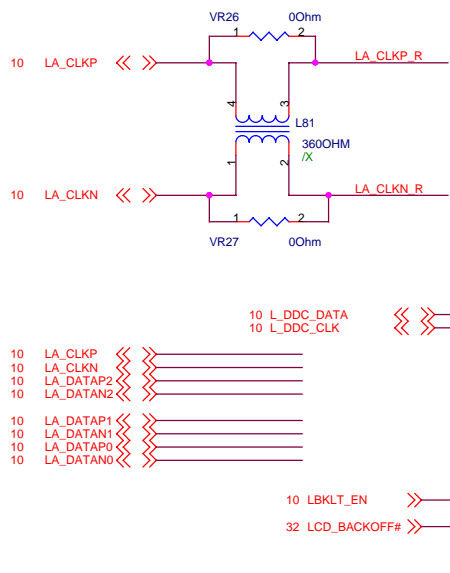
U25 : VR5 & VR6 --> 22 OHM
 U25 /X : VR5 & VR6 --> 0 OHM



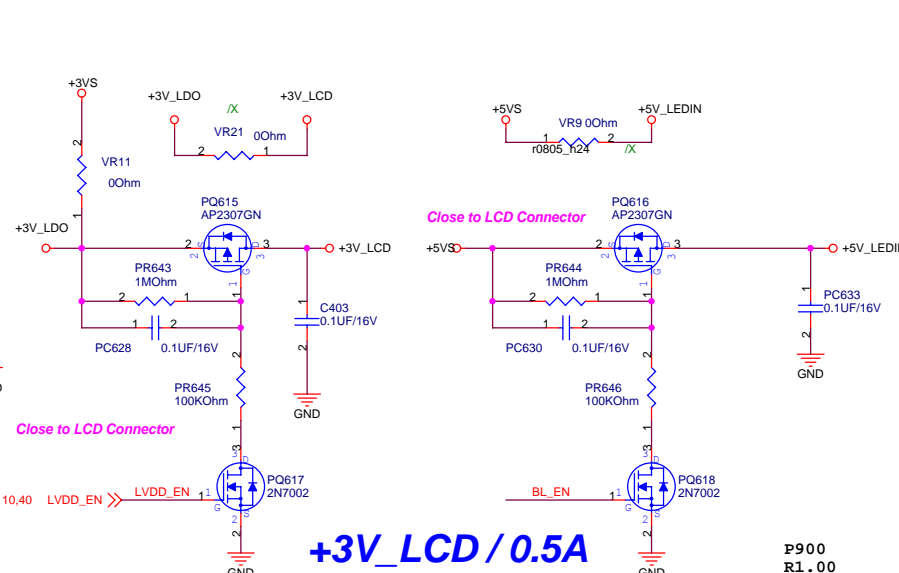
VGA use 12G10110015W & 12G10110015N



Pin:
 2->6: (1A->1B)
 5->3: (2A->2B)

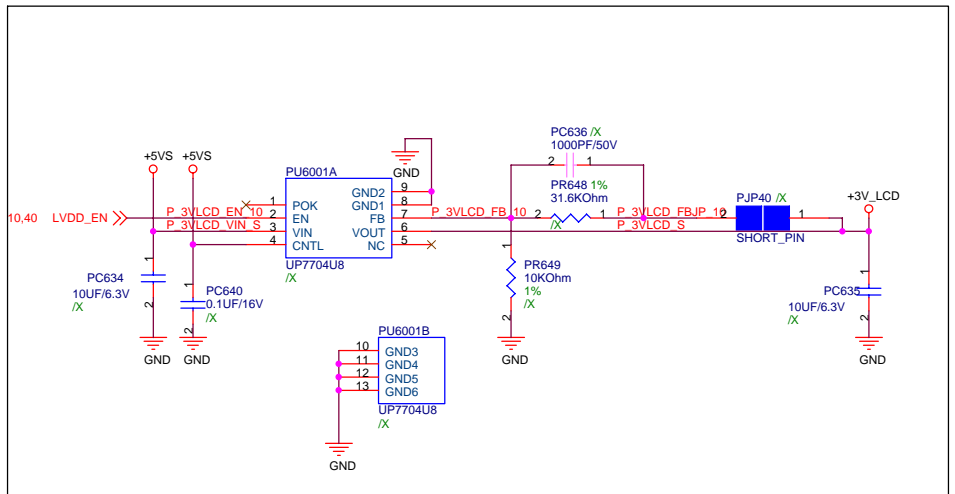
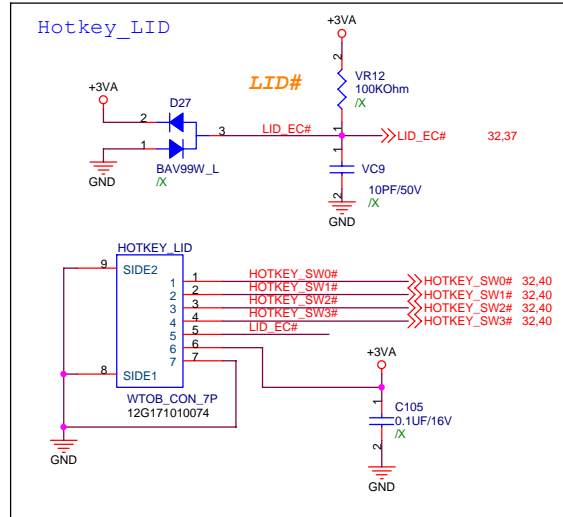


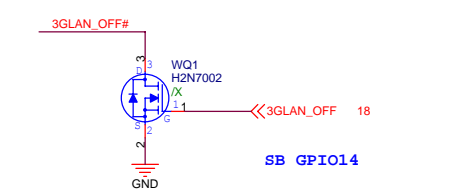
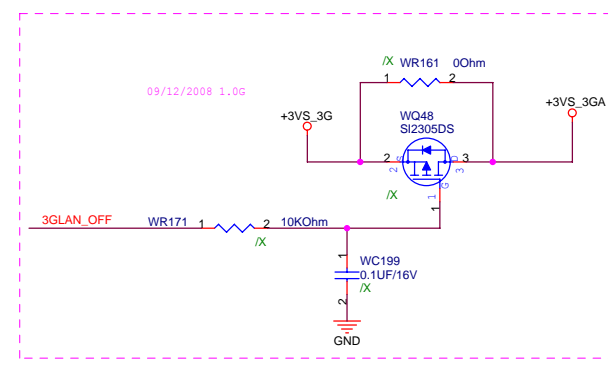
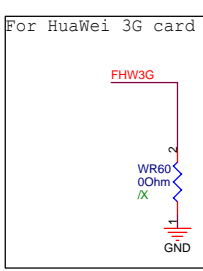
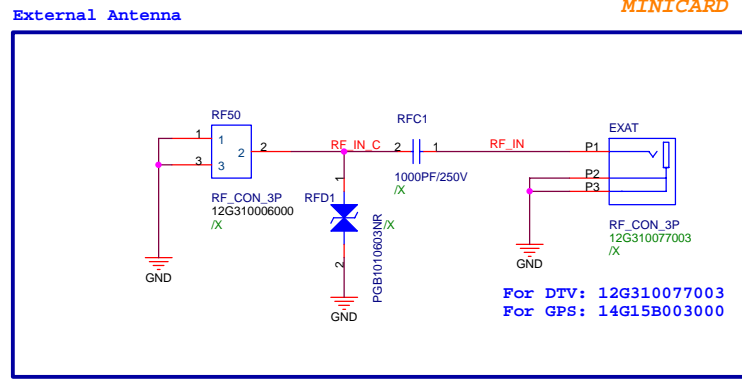
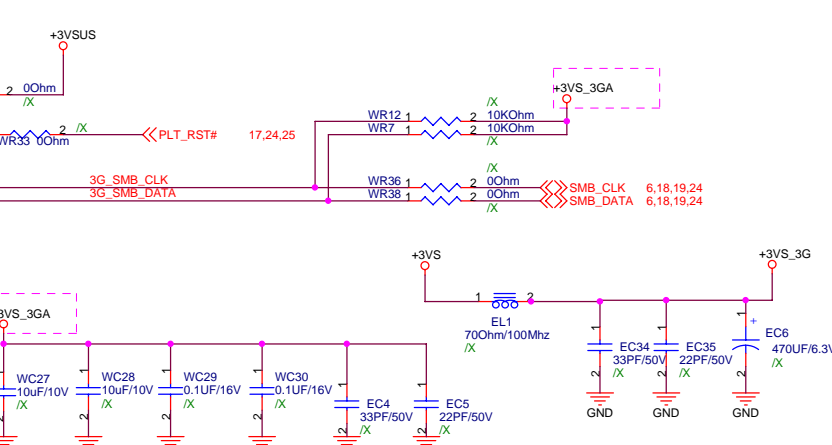
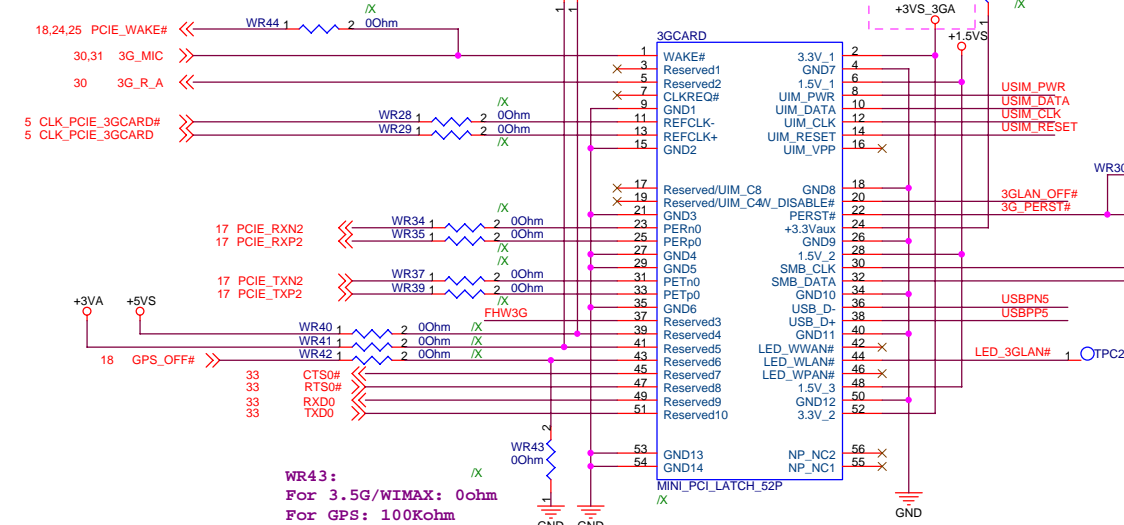
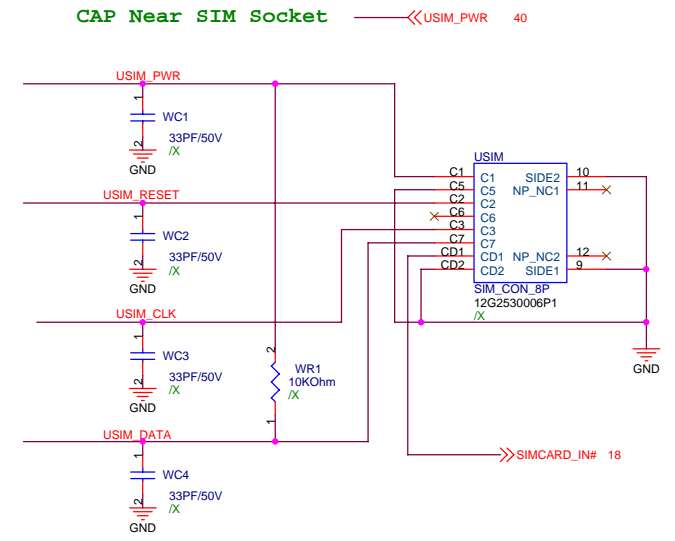
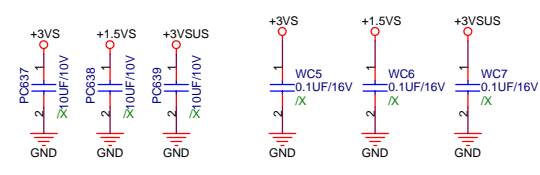
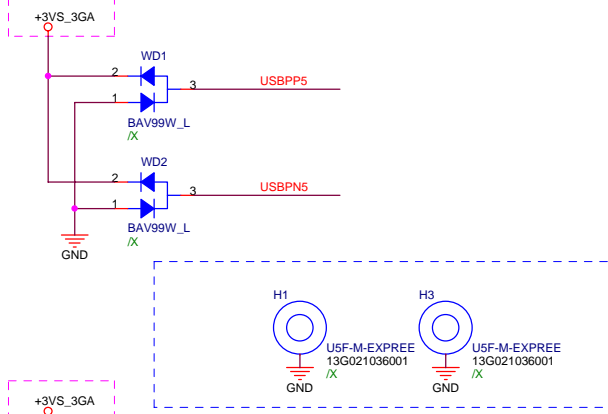
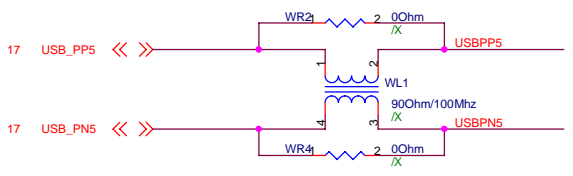
L DDC CLK	EC1	2	1	10PF/50V
L DDC DATA	EC2	2	1	10PF/50V
LA_CLKP_R	VC1	2	1	10PF/50V
LA_CLKN_R	VC2	2	1	10PF/50V
LA_DATAP2_R	VC3	2	1	10PF/50V
LA_DATAN2_R	VC4	2	1	10PF/50V
LA_DATAP1_R	VC5	2	1	10PF/50V
LA_DATAN1_R	VC6	2	1	10PF/50V
LA_DATAP0_R	VC7	2	1	10PF/50V
LA_DATAN0_R	VC8	2	1	10PF/50V



+3V_LCD / 0.5A

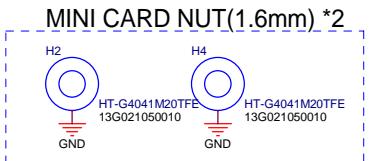
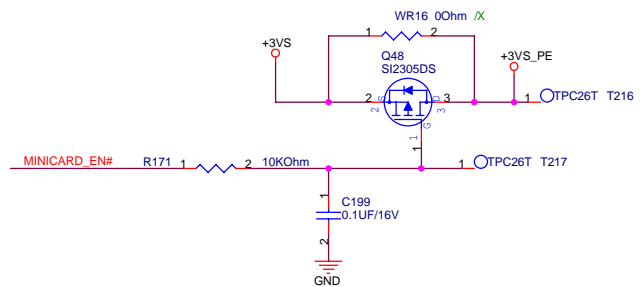
P900
R1.00



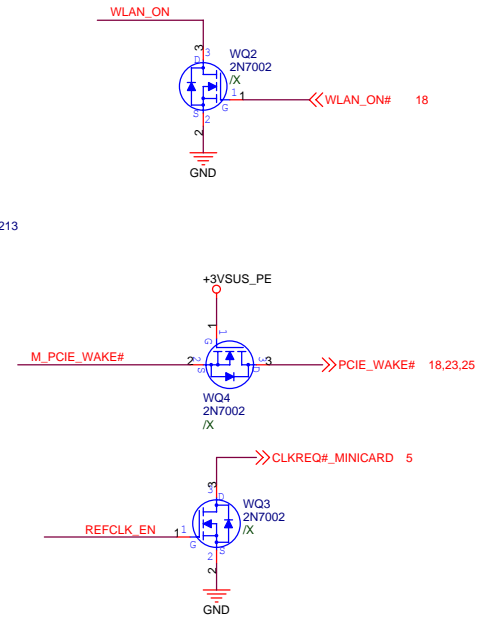
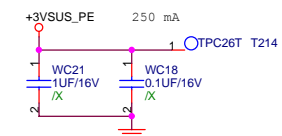
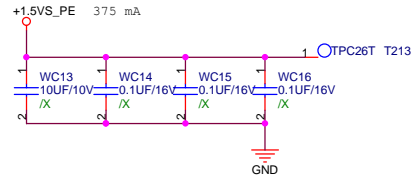
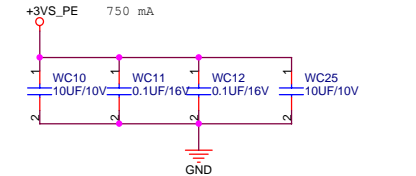
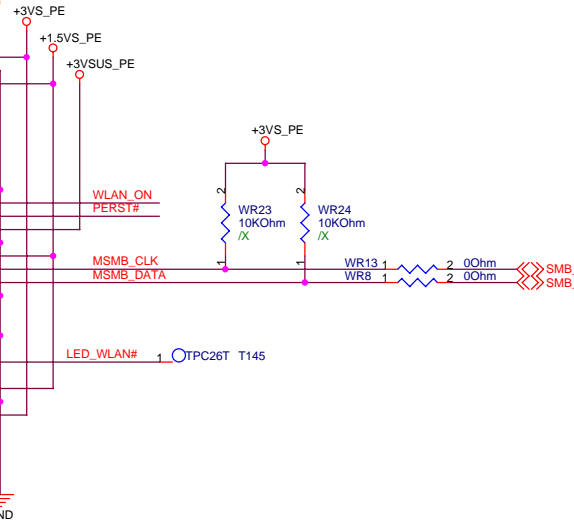
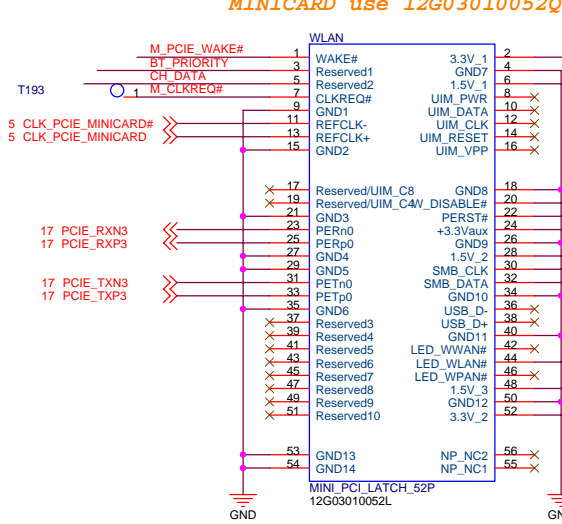


<Core Design> **3.5G Module & External Antenna**

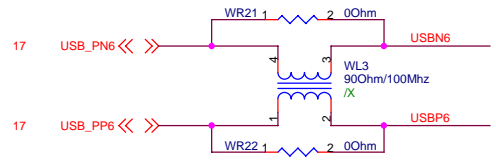
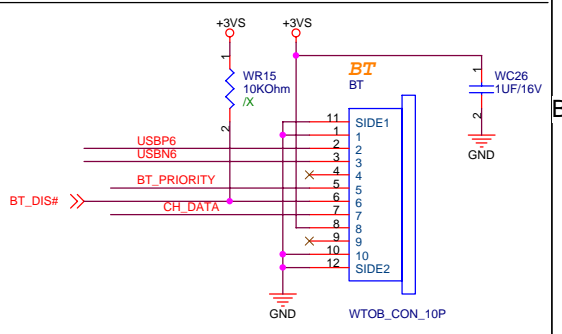
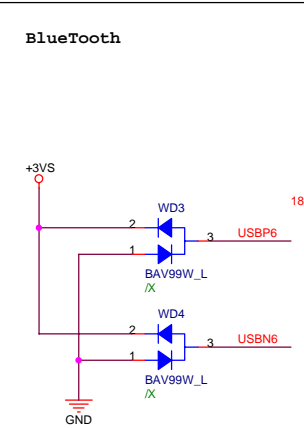
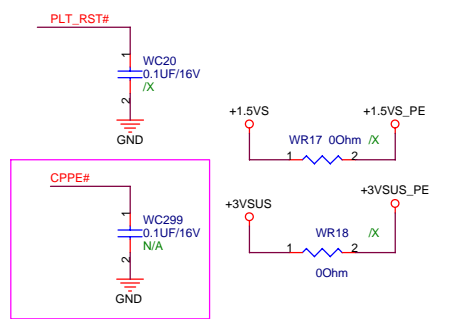
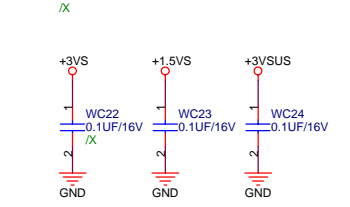
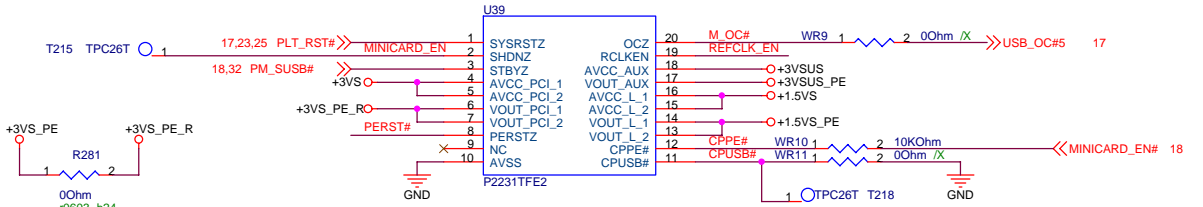
ASUS Title :	
ASUSTek Computer INC.	Engineer: Jeff Li
Size: A3	Project Name: 1000H_MB
Date: Friday, January 23, 2009	Sheet 23 of 52



MINICARD use 12G03010052Q

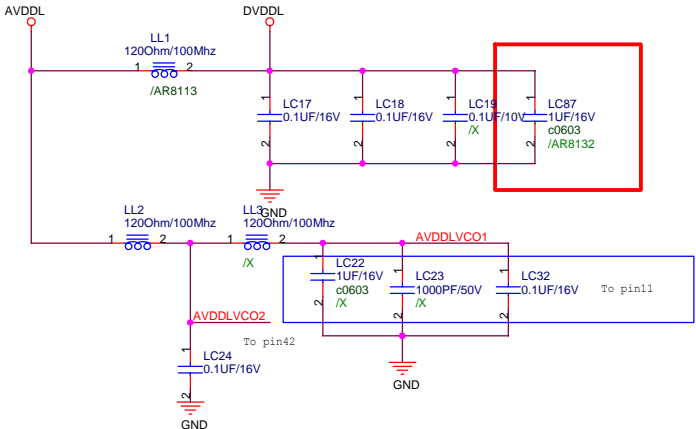
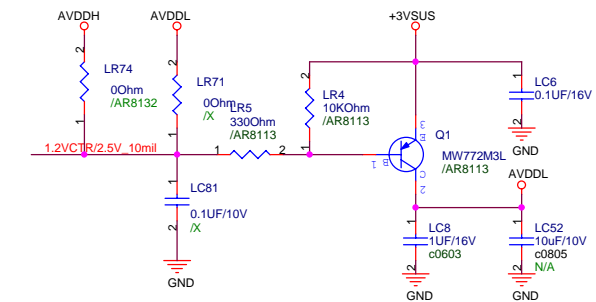
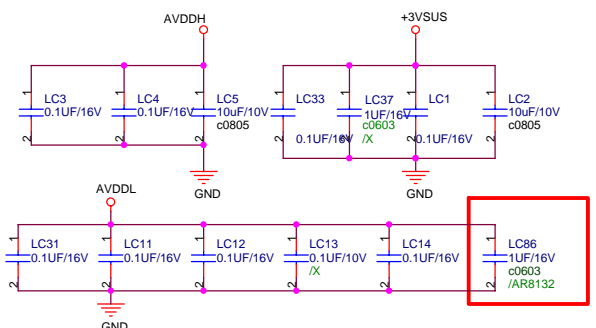


U39 use 06G030057013

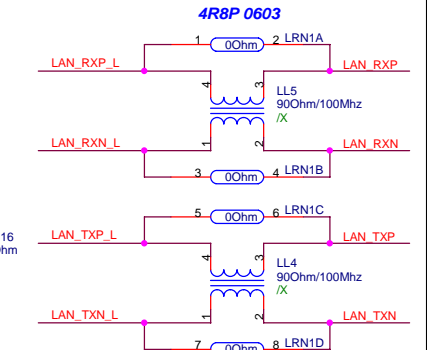
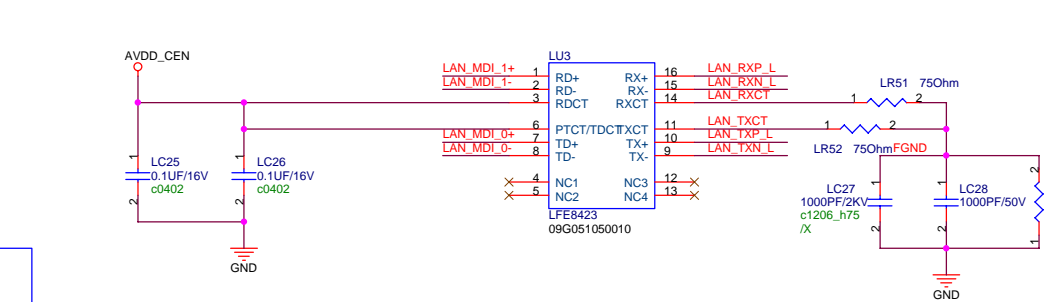
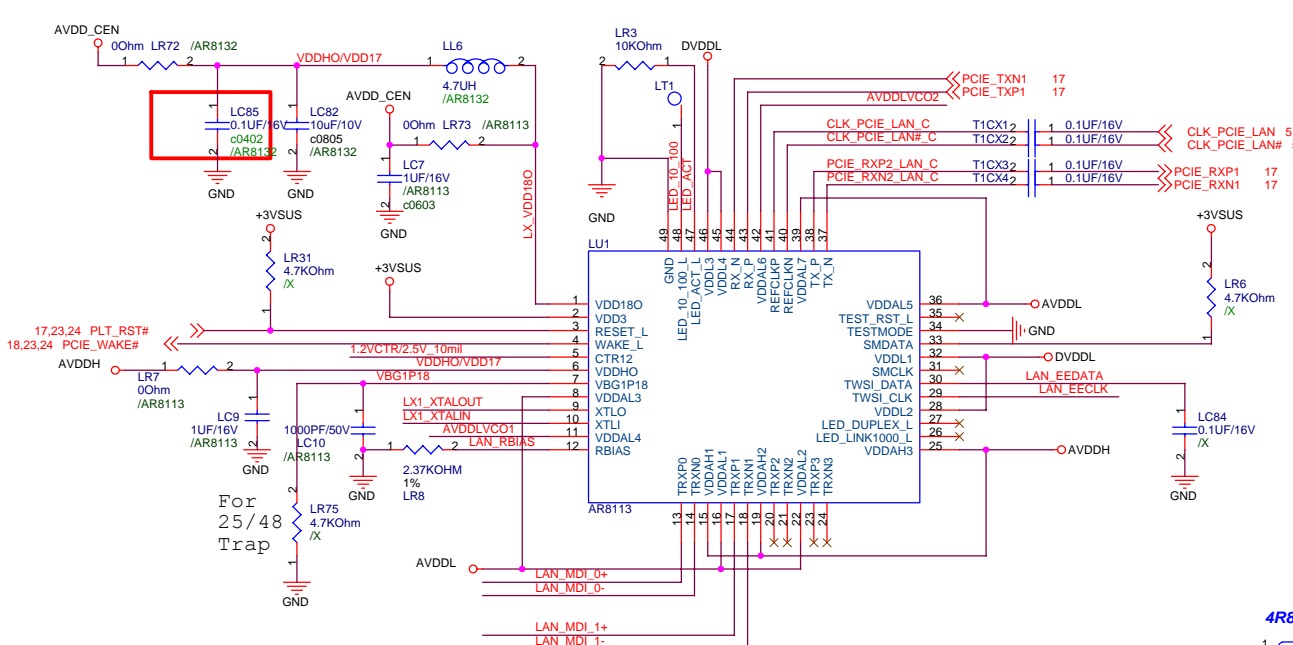
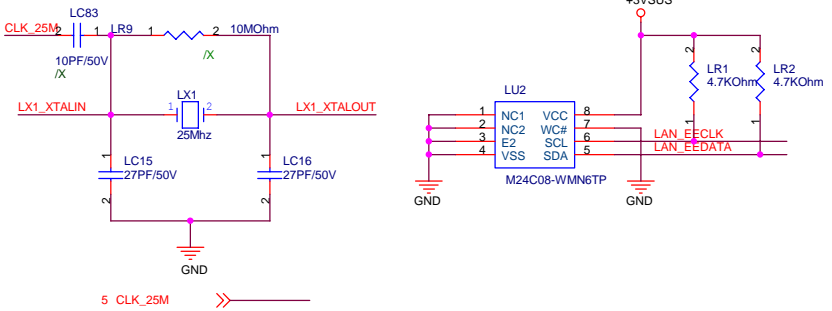


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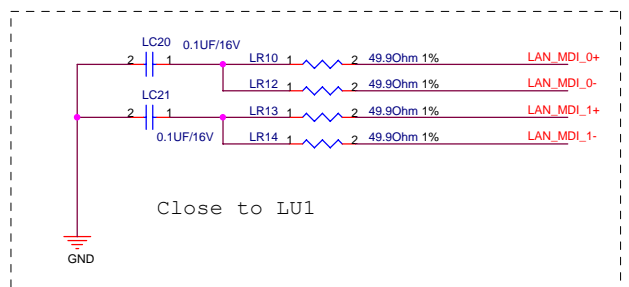
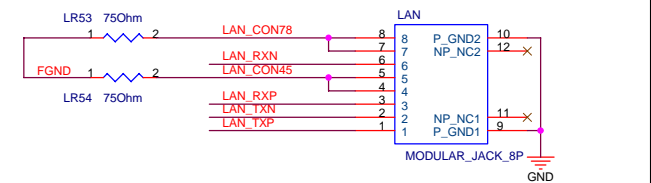
ASUS		Title : Minicard	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size A3	Project Name	1000HO_MB	Rev 1.0G
Date: Friday, January 23, 2009	Sheet	24	of 47



if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept



LAN connector: 12G148301086

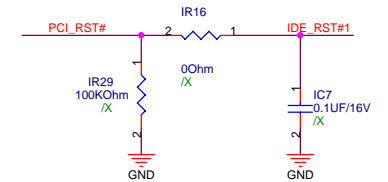
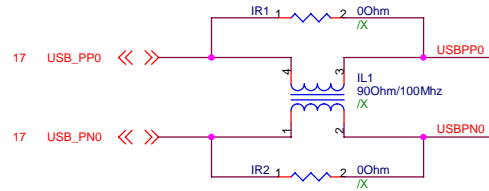
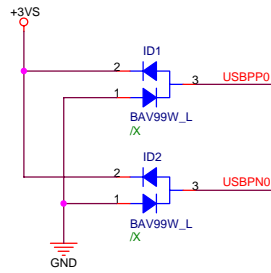
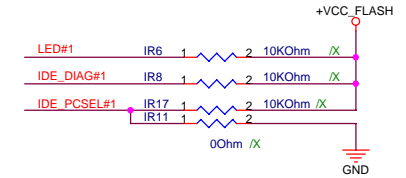
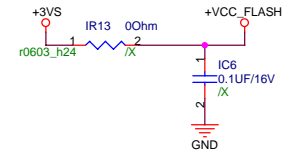
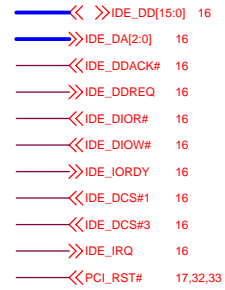
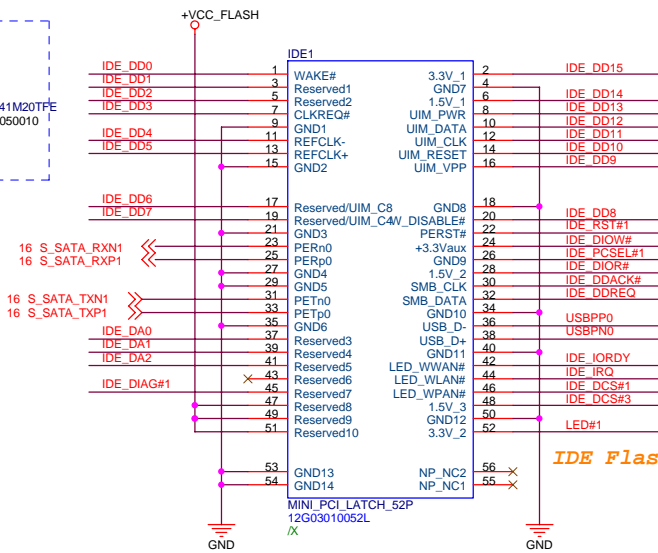
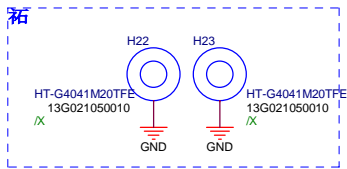


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Title : AR8113 / AR8132
Engineer: Jeff Li

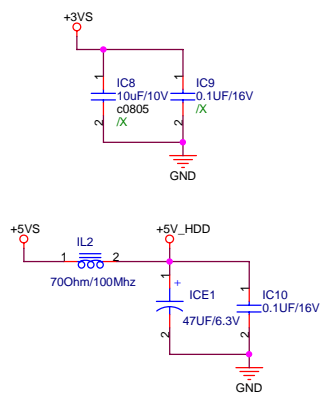
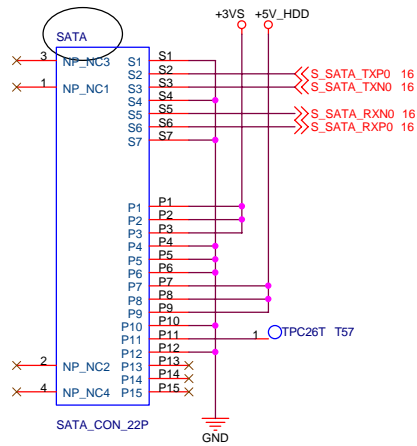
Size	Project Name	Rev
A3	1000HO_MB	1.0G

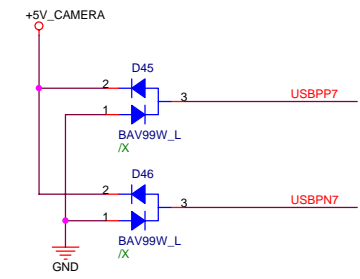
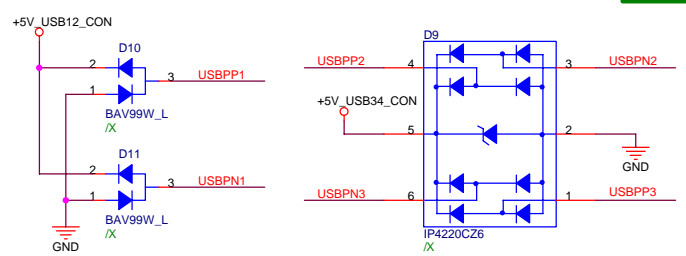
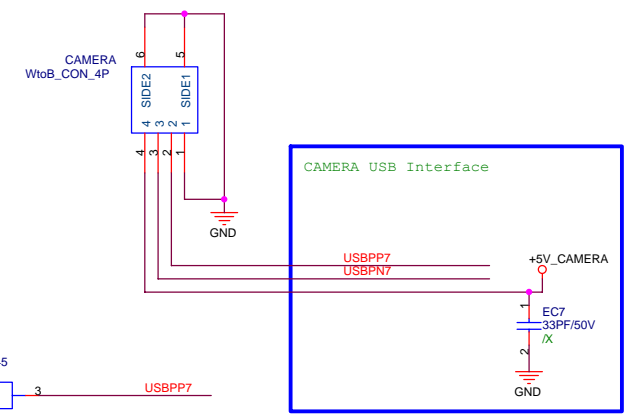
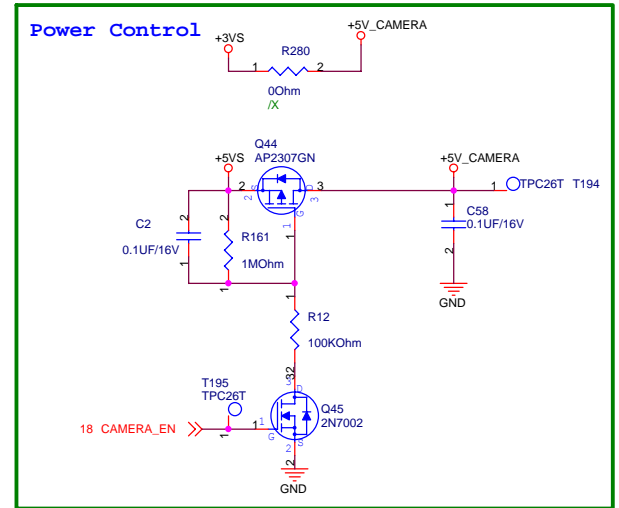
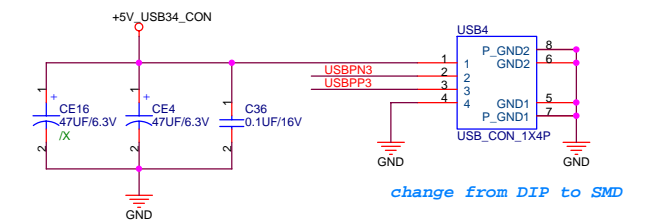
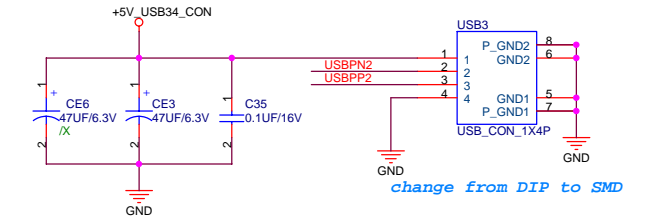
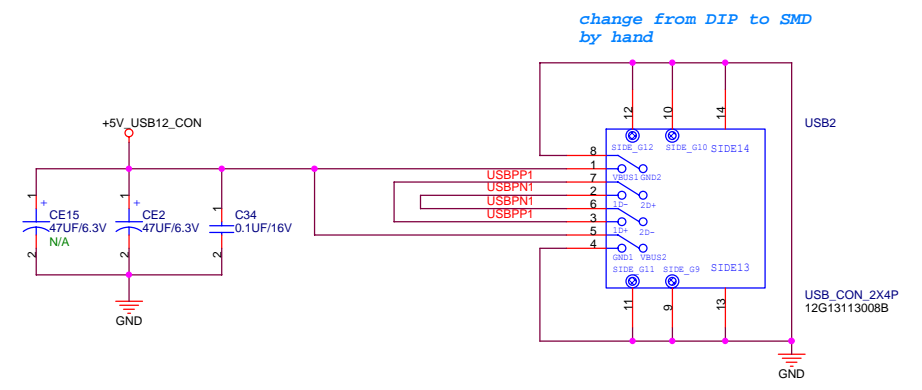
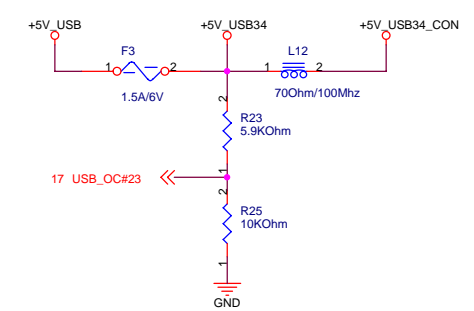
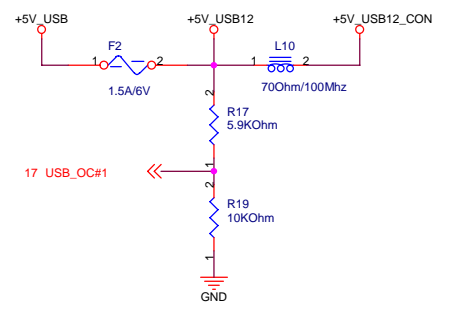
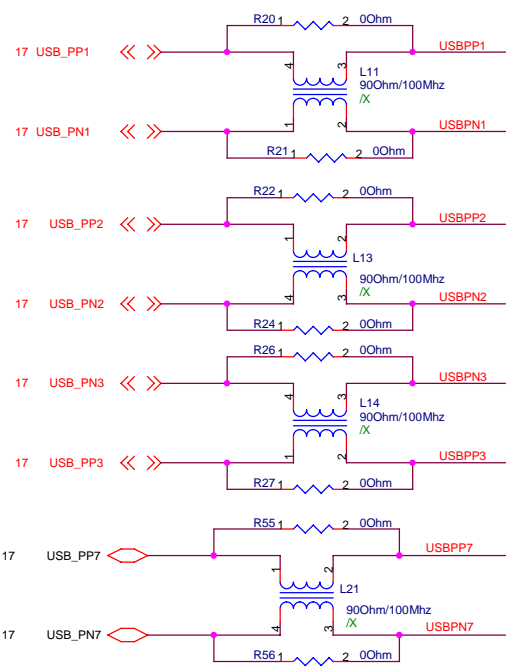
Date: Friday, January 23, 2009 Sheet 25 of 47

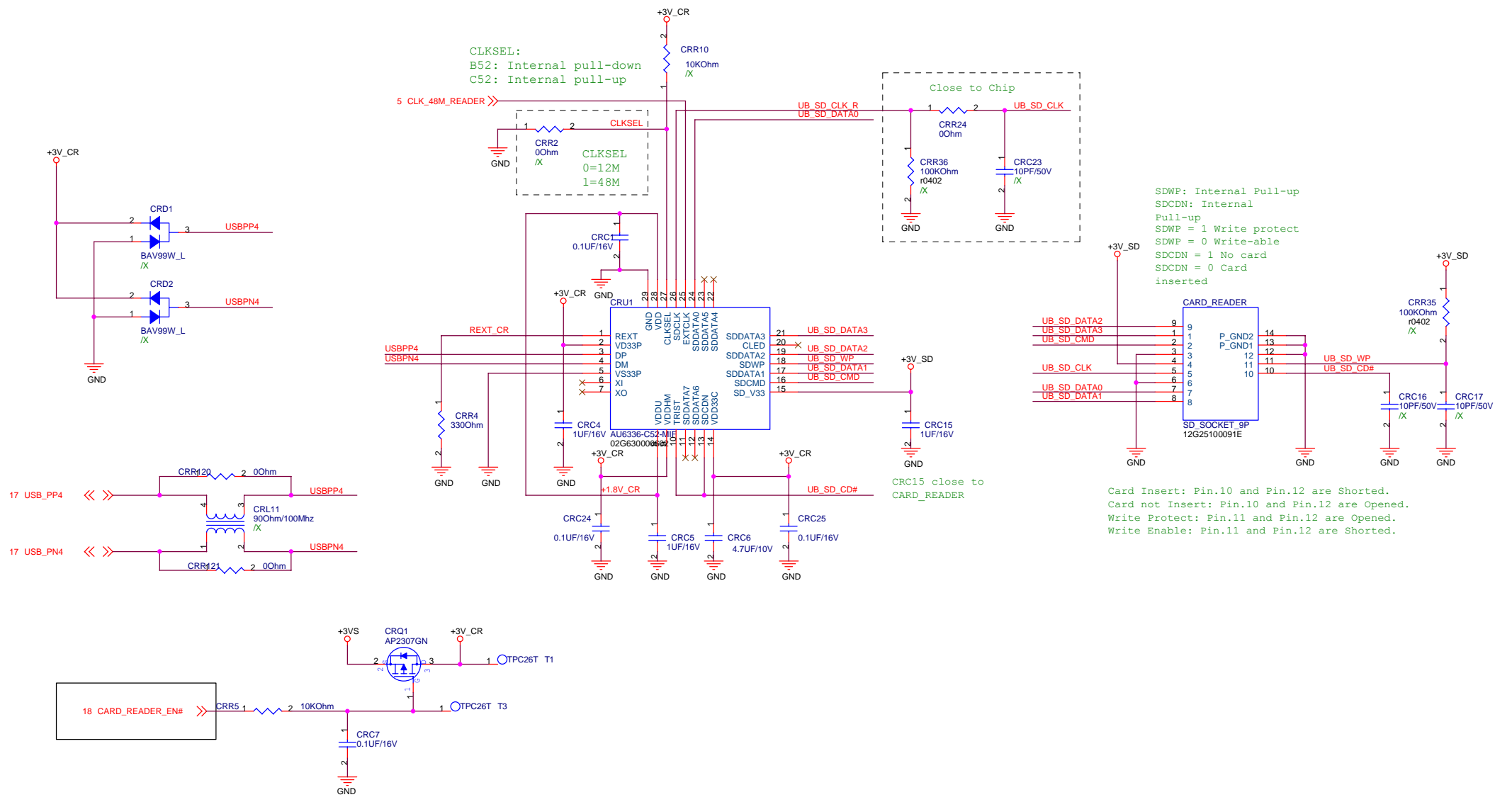


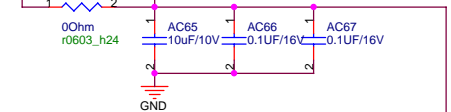
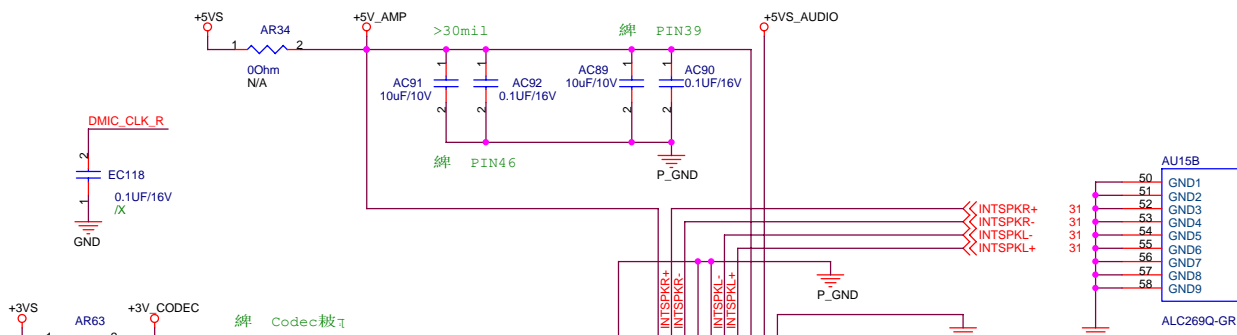
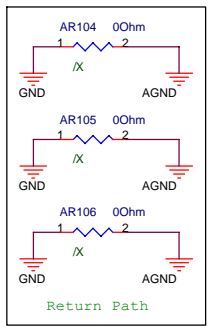
Naming Rule:
 IC: IU?
 R: IR?
 C: IC?
 L: IL?

SATA HDD Connector







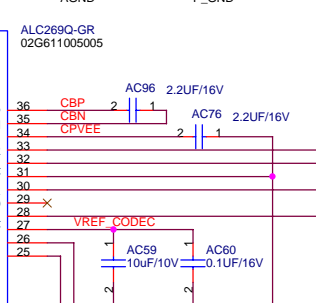
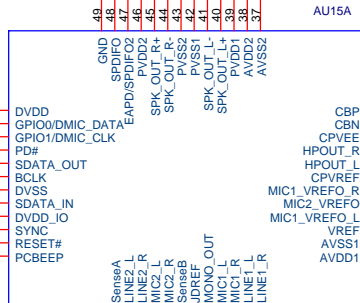
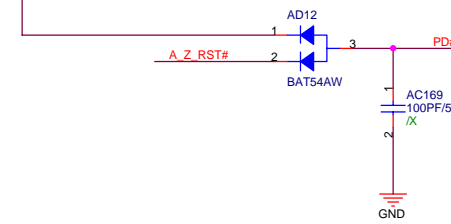


- 16 A_Z_SDOUT
- 16 A_Z_BITCLK
- 16 A_Z_SDINO
- 16 A_Z_SYNC
- 16 A_Z_RST#

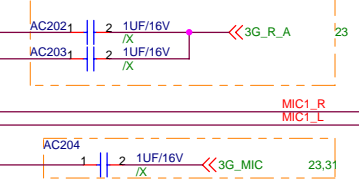
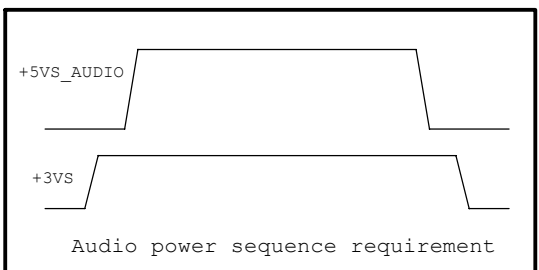
32 OP_SD#

OP_SD#: Controlled by EC to power down Class-D speaker amp.

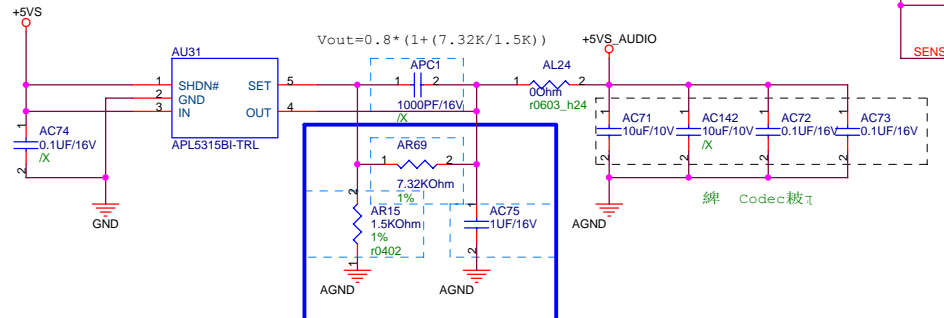
PD#: Internal Pull-up 50K to +3V



Analogue: Pin.13~Pin.38
Digital: Pin.1~Pin.12 and Pin.39~Pin.48

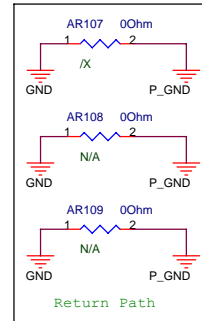
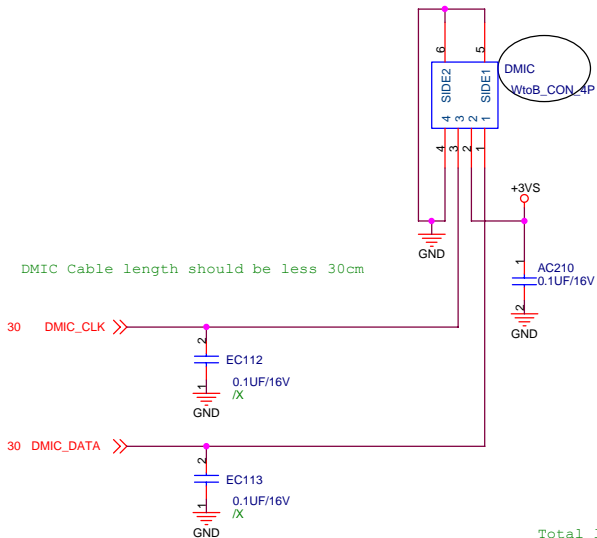


Need 4.7u/10V XSR to prevent poor THD+N

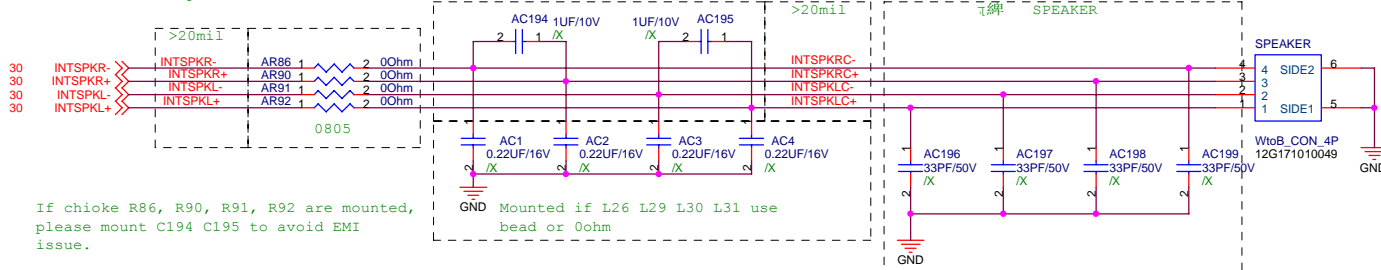


For Audio Noise Issue

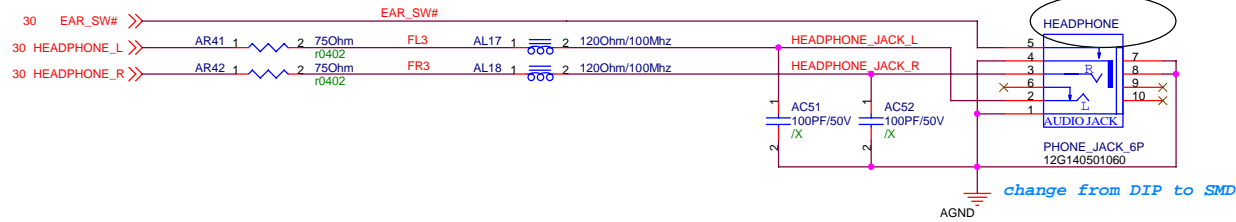
ASUS		Title : ALC269-1	
ASUSTek Computer Inc.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000HO_MB		1.0G
Date: Friday, January 23, 2009	Sheet	20 of	47



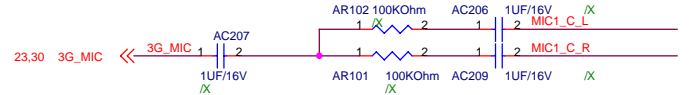
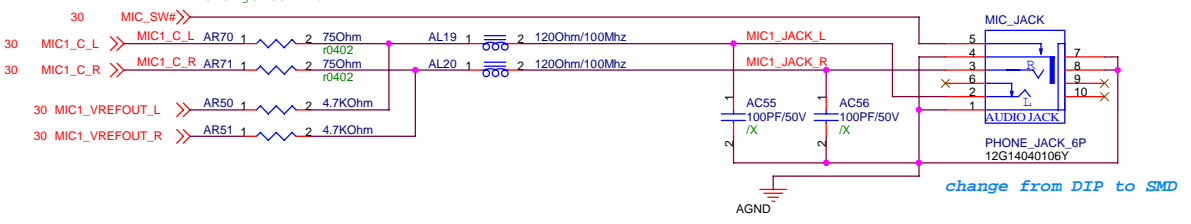
Total length from speaker+/- L+- (pin40 41 44 45) to internal speaker please as short as possible (<20cm is better)



LINE_OUT use 12G140501060



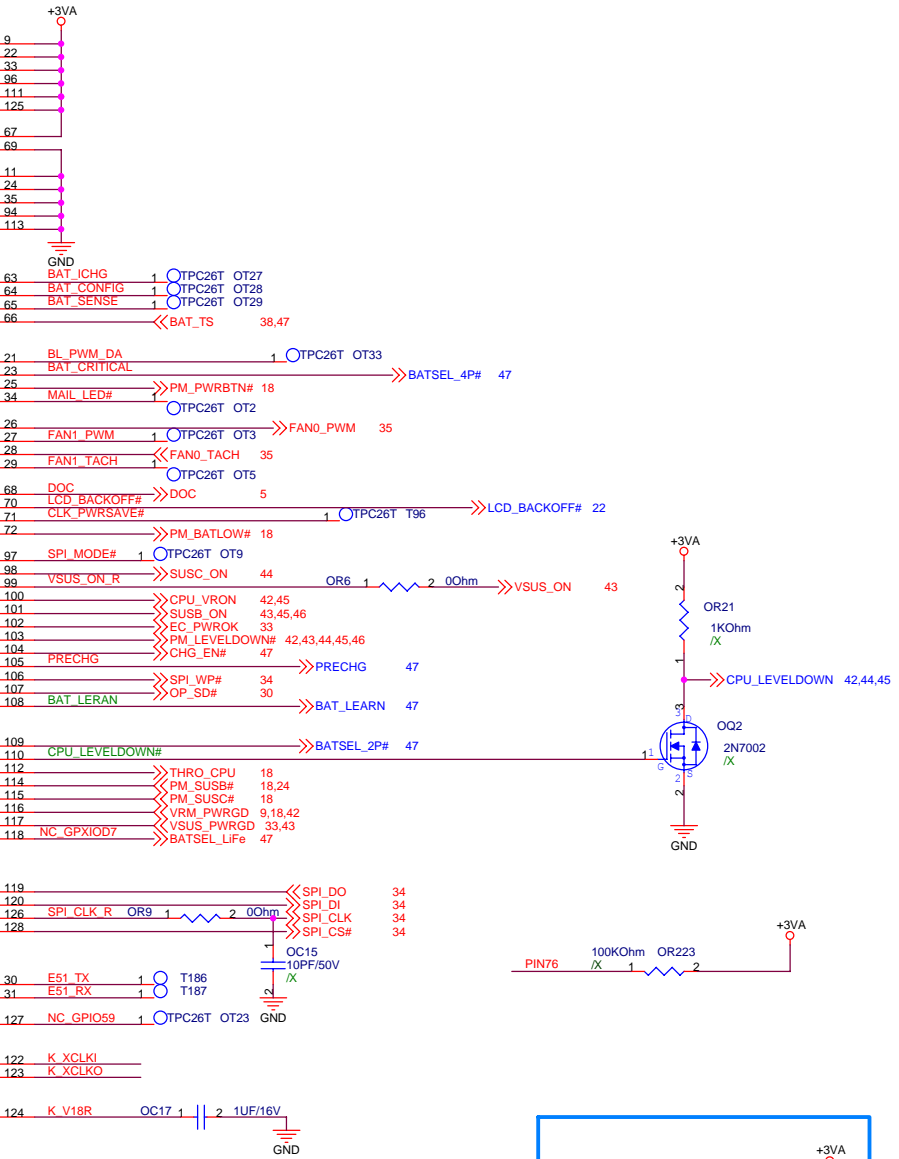
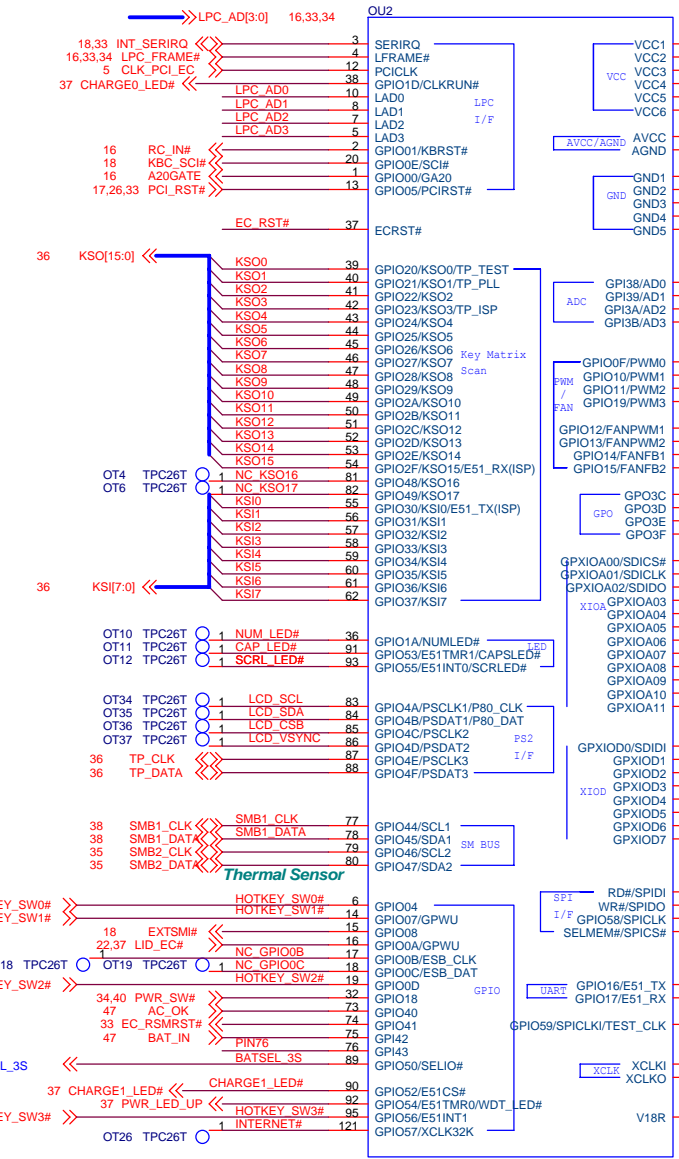
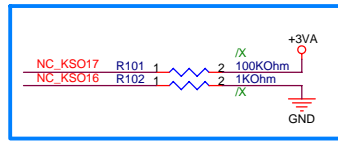
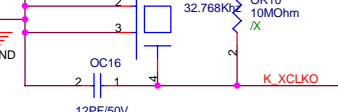
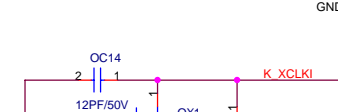
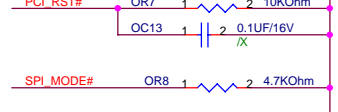
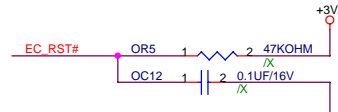
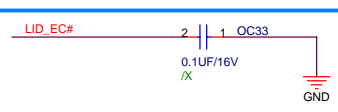
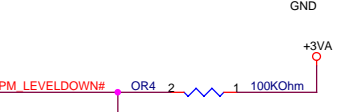
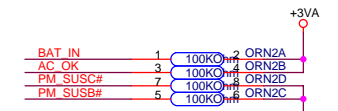
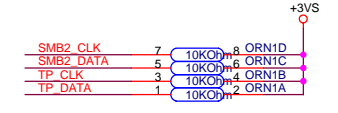
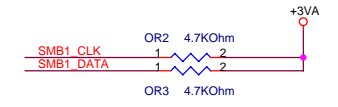
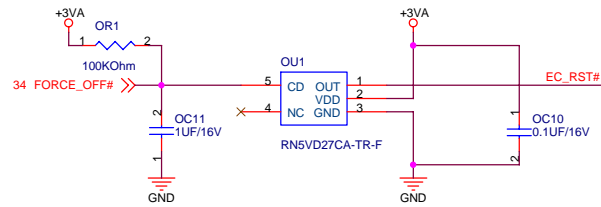
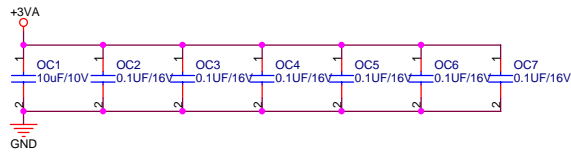
MIC_JACK use 12G14040106Y



R70 and R71: If don't need retasking function, change to 1K.

<Core Design>

ASUS		Title : ALC269-2	
ASUSTek Computer Inc.		Engineer: Jeff Li	
Size A3	Project Name 1000HO_MB		Rev 1.0G
Date: Friday, January 23, 2009	Sheet	31	of 47



<Core Design>

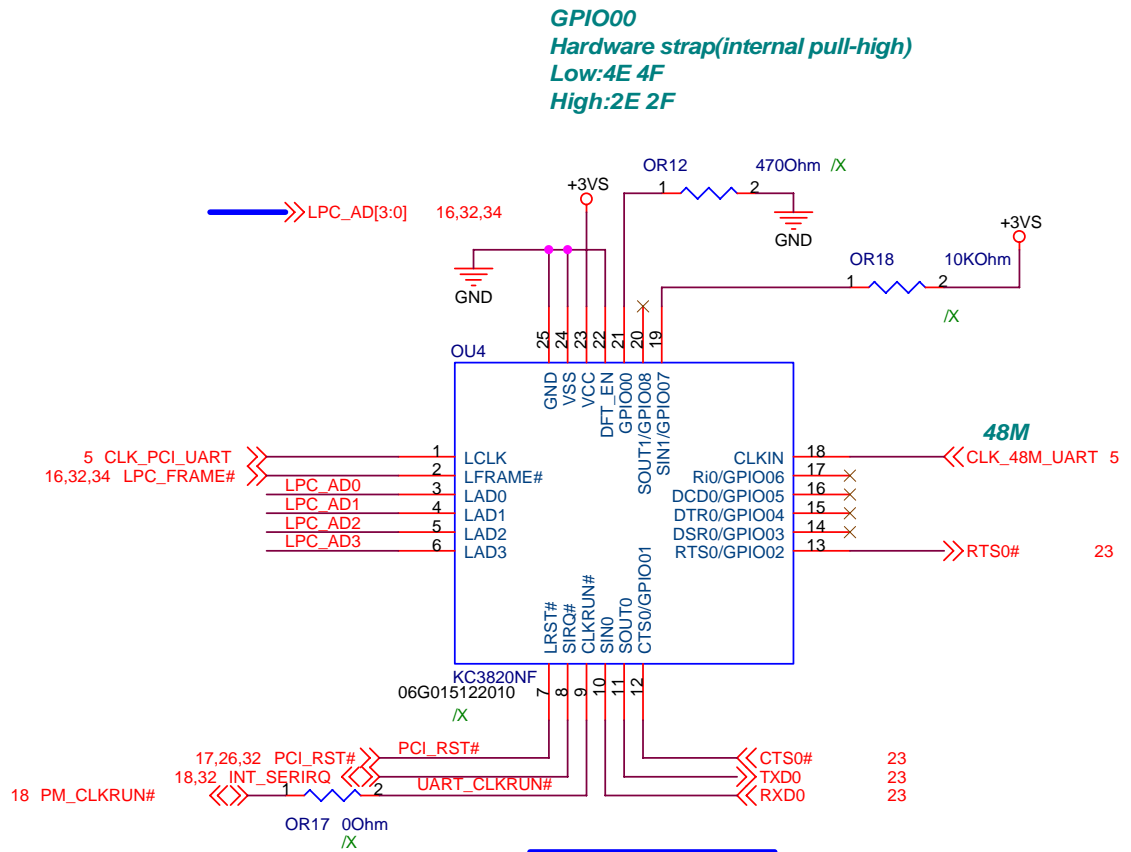
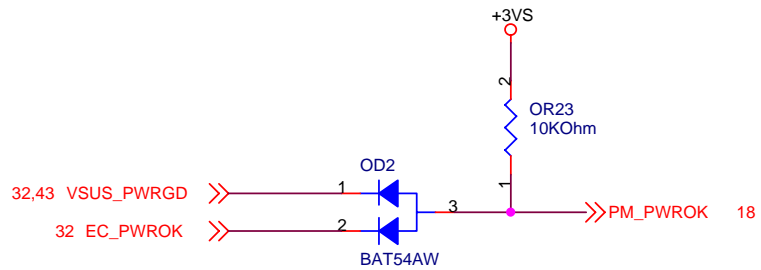
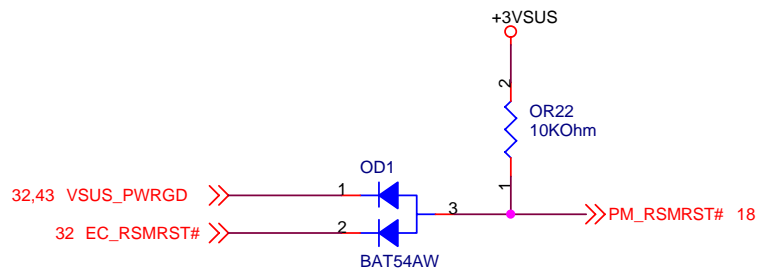
Title : EC_ENE KB3310

ASUSTek Computer INC. Engineer: **Jeff Li**

Size A3	Project Name 1000HO_MB	Rev 1.0G
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KB33100F
N/A
02G890000700

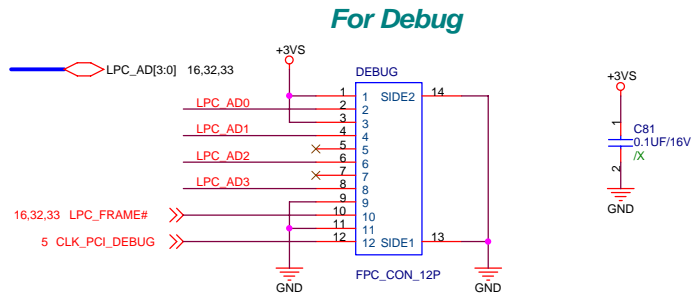
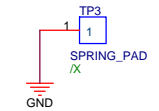
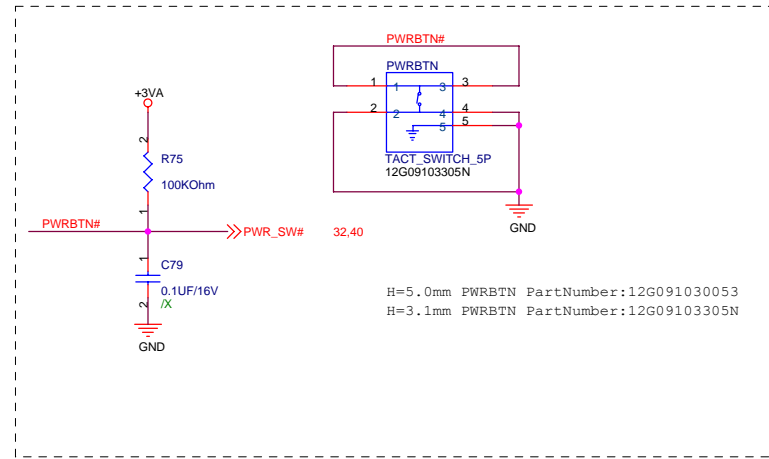
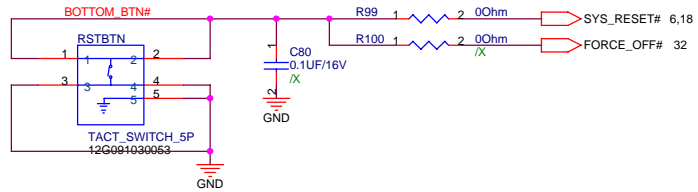


GPIO00
 Hardware strap(internal pull-high)
 Low:4E 4F
 High:2E 2F

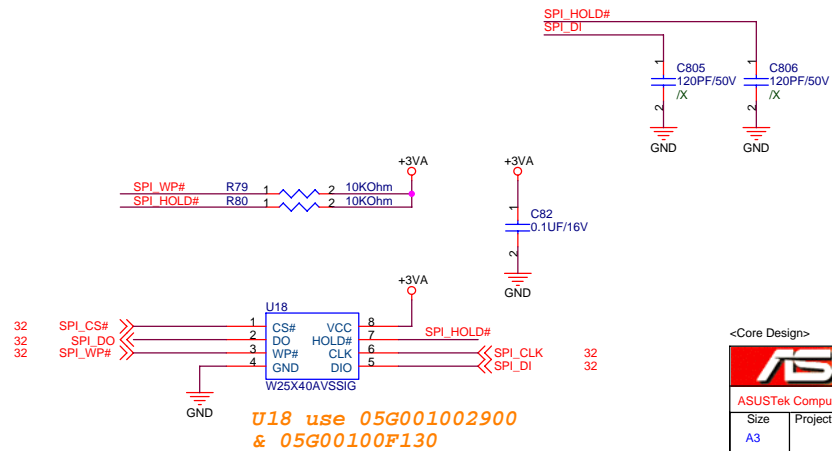
UART Control
 IC for using
 GPS module due
 to no UART on
 ENE EC

<Core Design>

		Title : EC_UART_KC3820	
ASUSTek Computer INC.		Engineer: <i>Jeff Li</i>	
Size A4	Project Name 1000HO_MB		Rev 1.0G
Date: Friday, January 23, 2009		Sheet	33 of 47

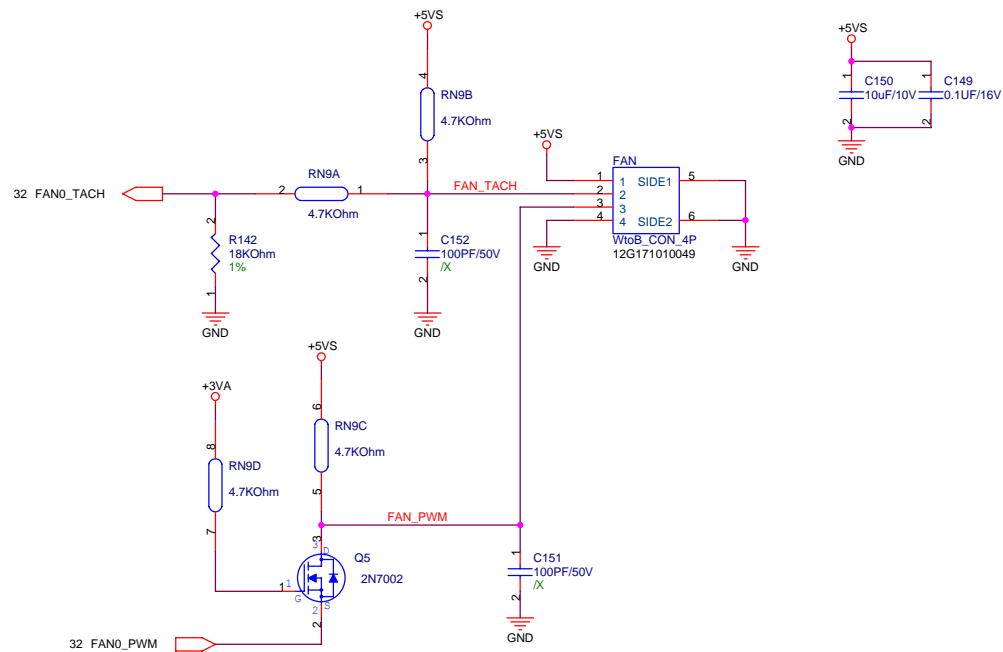
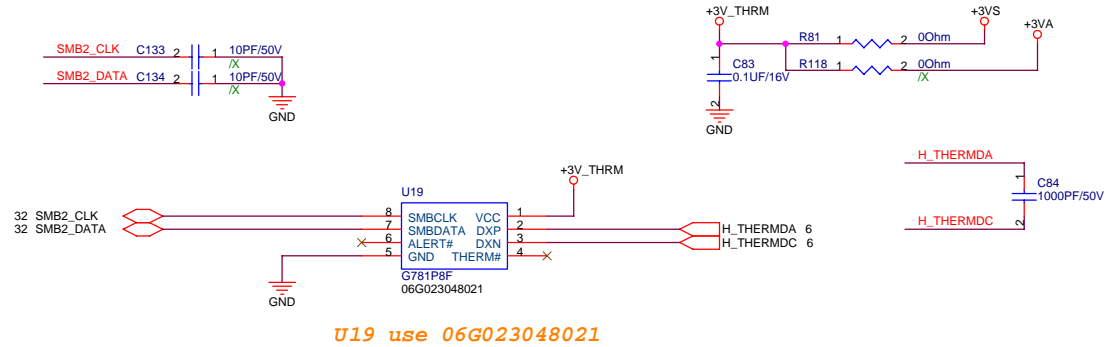


Debug Card cable use Z96 Touch Pad cable, P/N:
14G124110126, 14G124110120, 14G124110121
14G124110124, 14G124110125



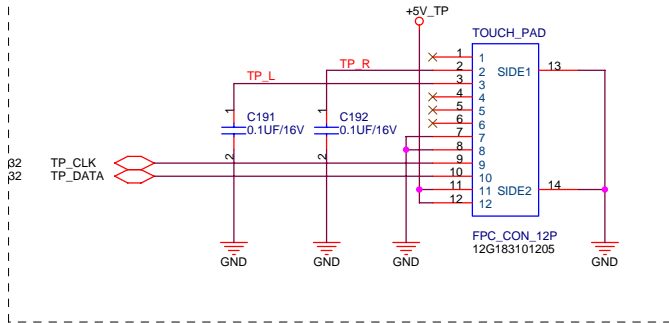
<Core Design>

ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	100HO_MB		1.0G
Date:	Friday, January 23, 2009	Sheet	34 of 52

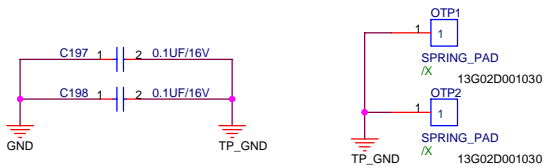
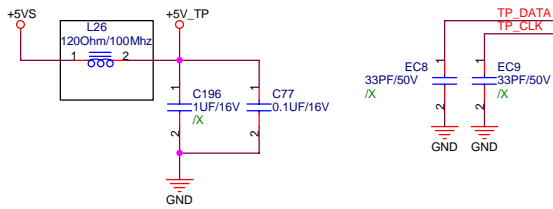
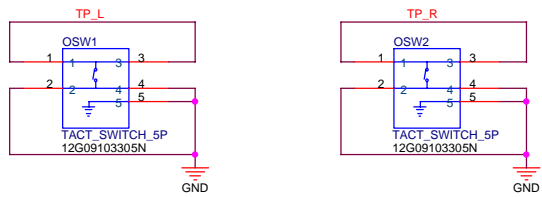


For Touch-Pad

P900 R1.0G

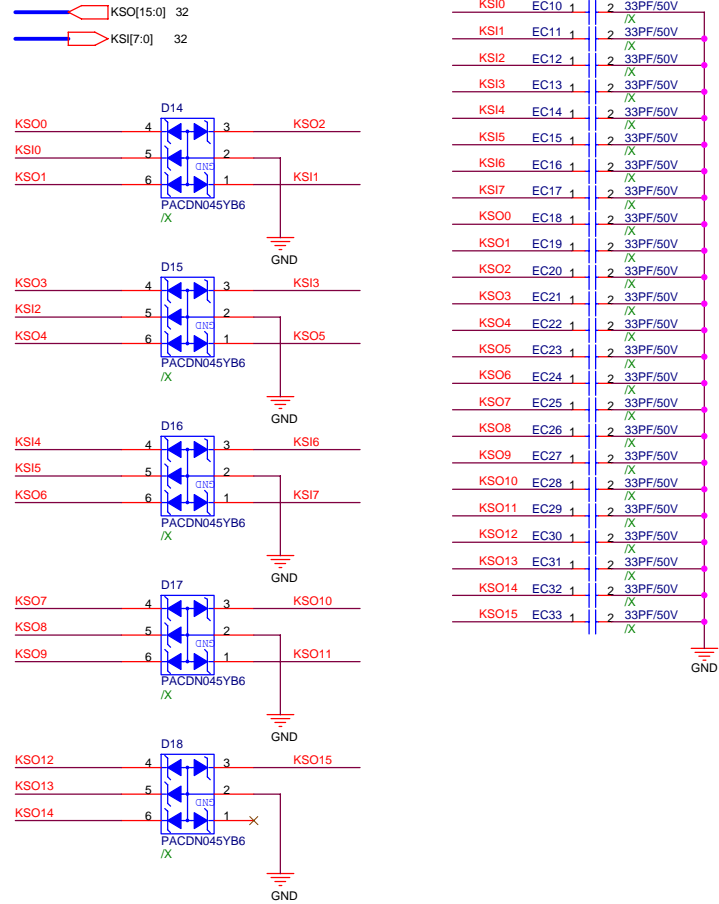
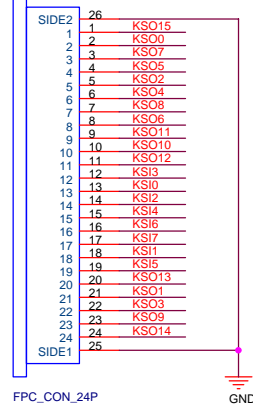


SW2, SW3 use 12G09103305N



For Keyboard Connector

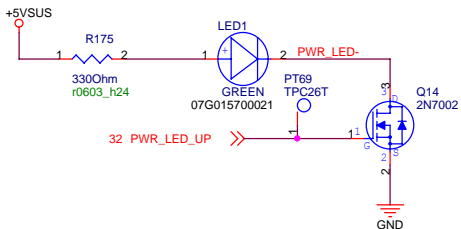
KB



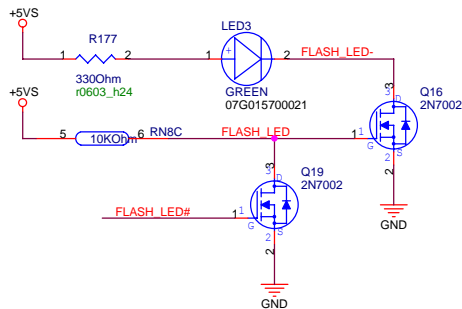
<Core Design>

ASUS		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000HO_MB		1.0G
Date: Friday, January 23, 2009	Sheet	36	of 52

for POWER LED

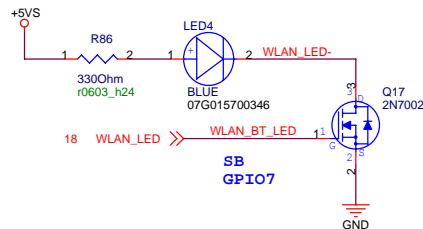


for FLASH LED

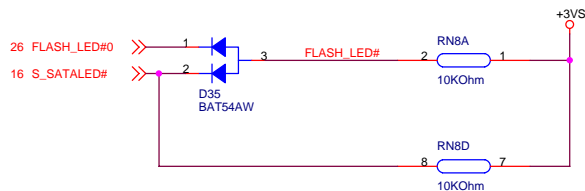
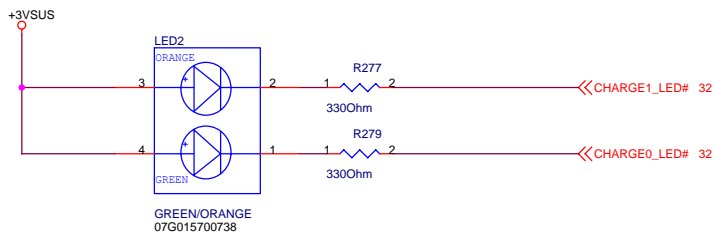


for WLAN/BlueTooth LED

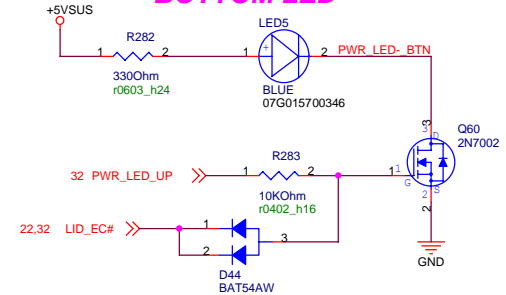
R86 use 4.7K OHm 10G213472003030



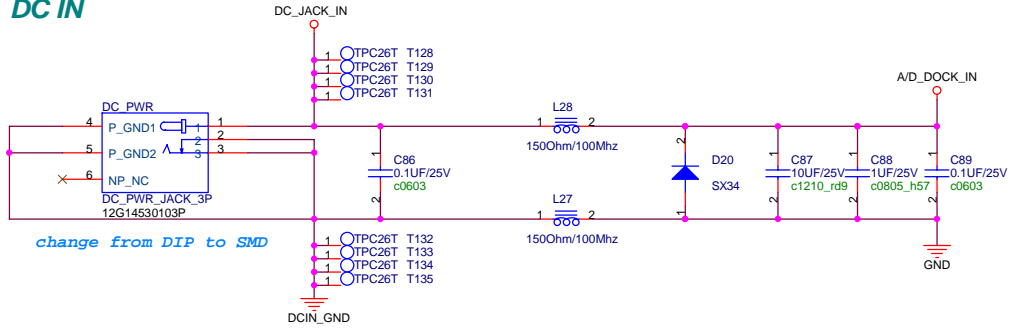
for CHARGE LED



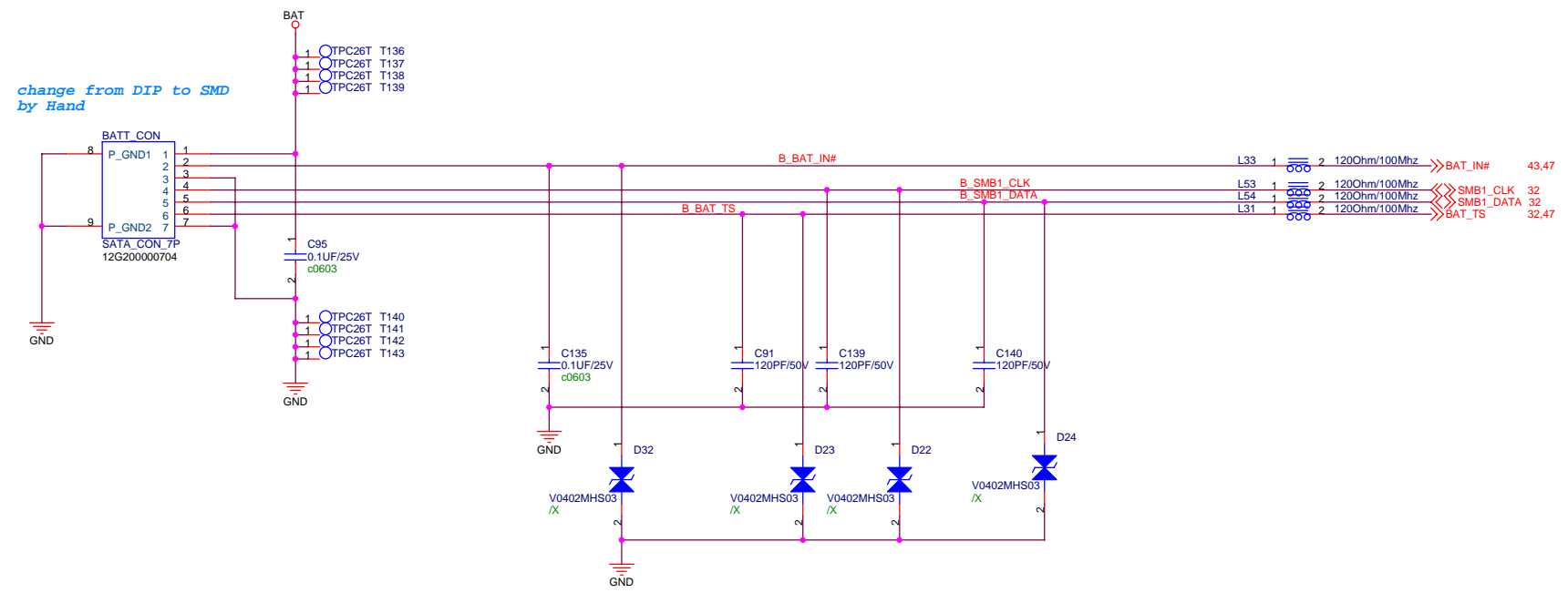
for POWER BOTTOM LED

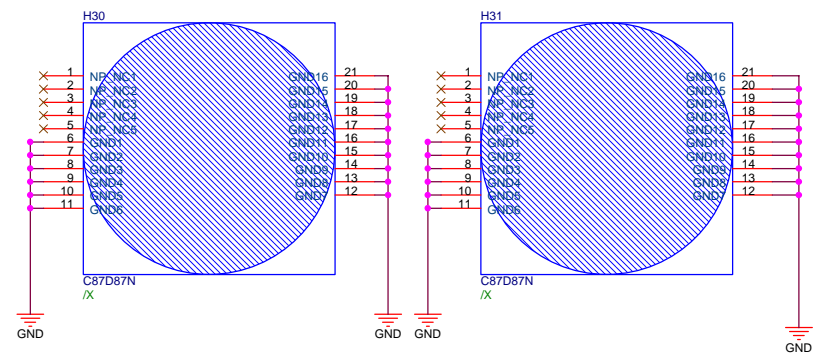
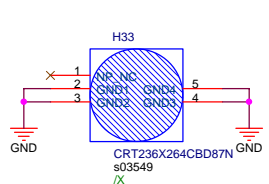
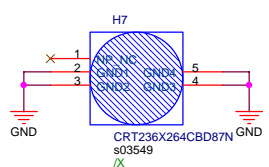
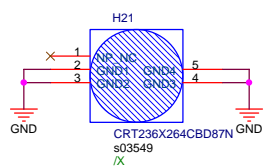
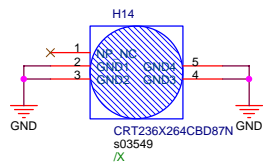
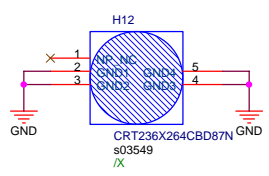
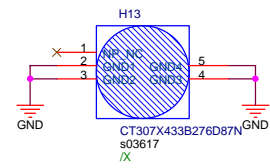
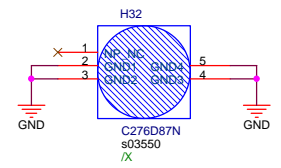
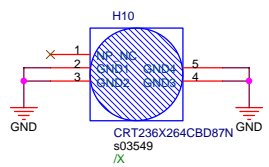
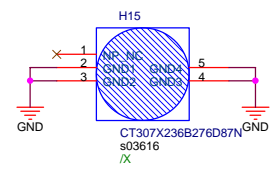
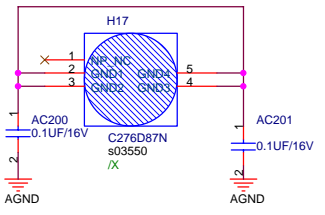
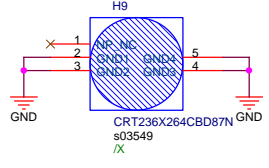
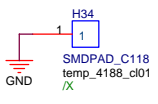
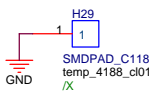
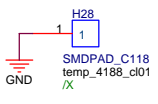
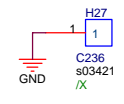
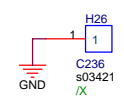
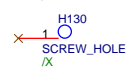
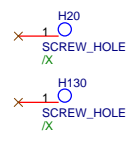
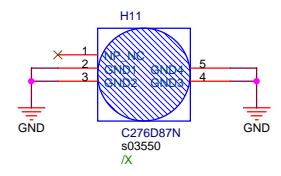
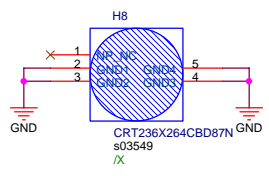


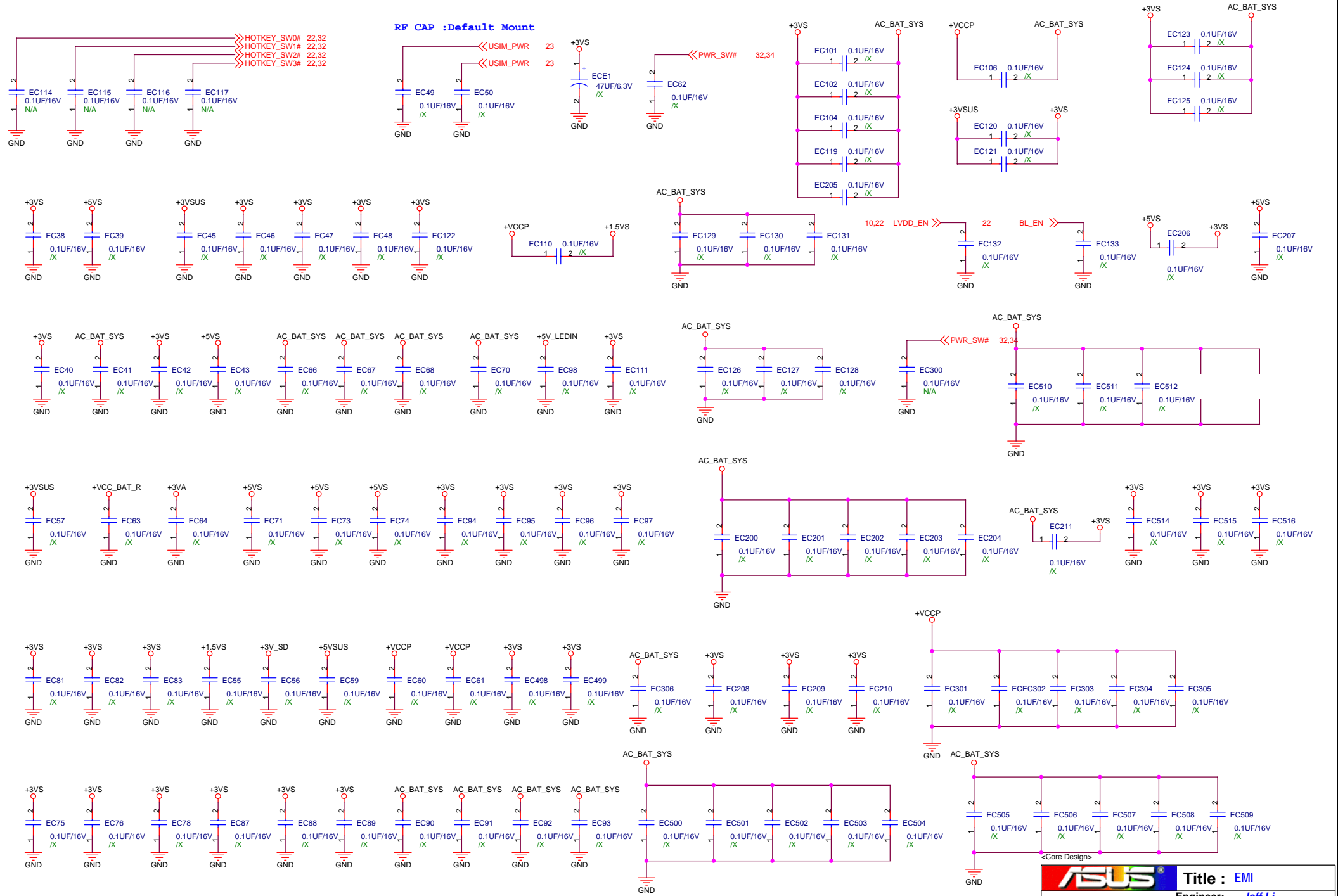
DC IN

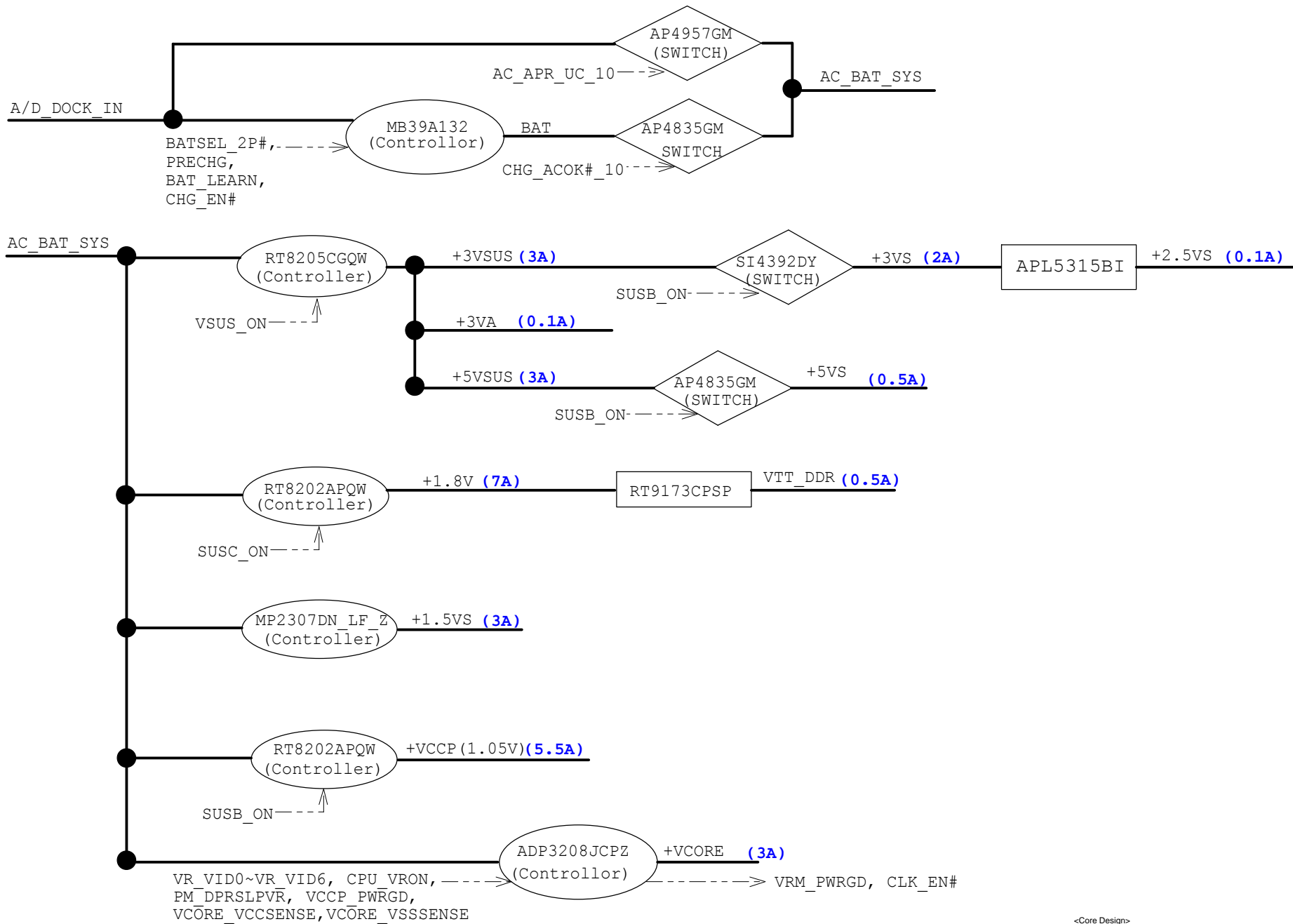


BAT IN



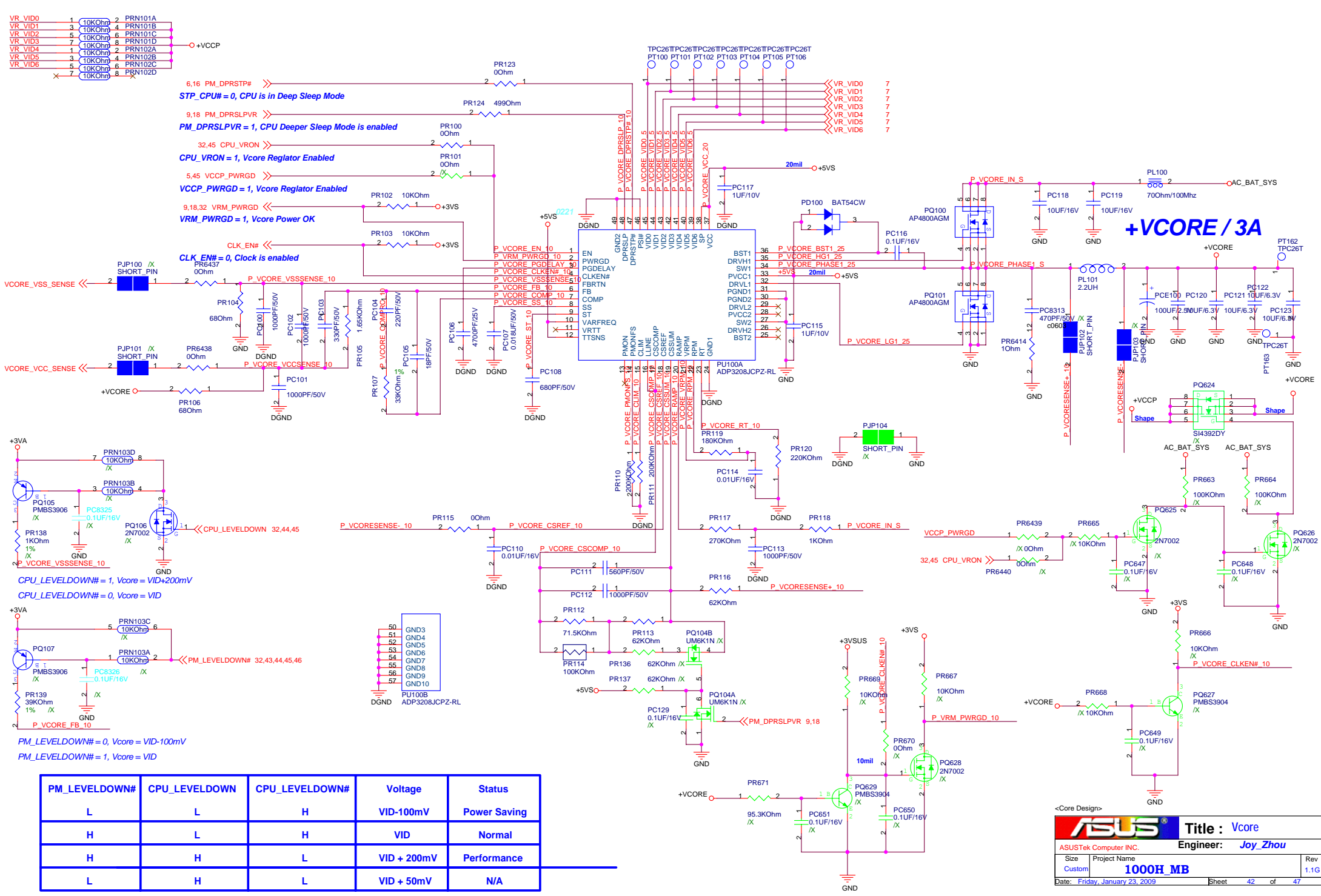






<Core Design>

ASUS		Title : Power Flow	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
Size	Project Name	Rev	
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6.16 PM_DPRSTP# >>>
STP_CPUH# = 0, CPU is in Deep Sleep Mode

9.18 PM_DPRSLPVR >>>
PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled

32.45 CPU_VRON >>>
CPU_VRON = 1, Vcore Reglator Enabled

5.45 VCCP_PWRGD >>>
VCCP_PWRGD = 1, Vcore Reglator Enabled

9.18.32 VRM_PWRGD >>>
VRM_PWRGD = 1, Vcore Power OK

CLK_EN# <<<
CLK_EN# = 0, Clock is enabled

7 Vcore_VSS_Sense <<<
 7 Vcore_VCC_Sense <<<

CPU_LEVELDOWN# = 1, Vcore = VID+200mV
 CPU_LEVELDOWN# = 0, Vcore = VID

PM_LEVELDOWN# = 0, Vcore = VID-100mV
 PM_LEVELDOWN# = 1, Vcore = VID

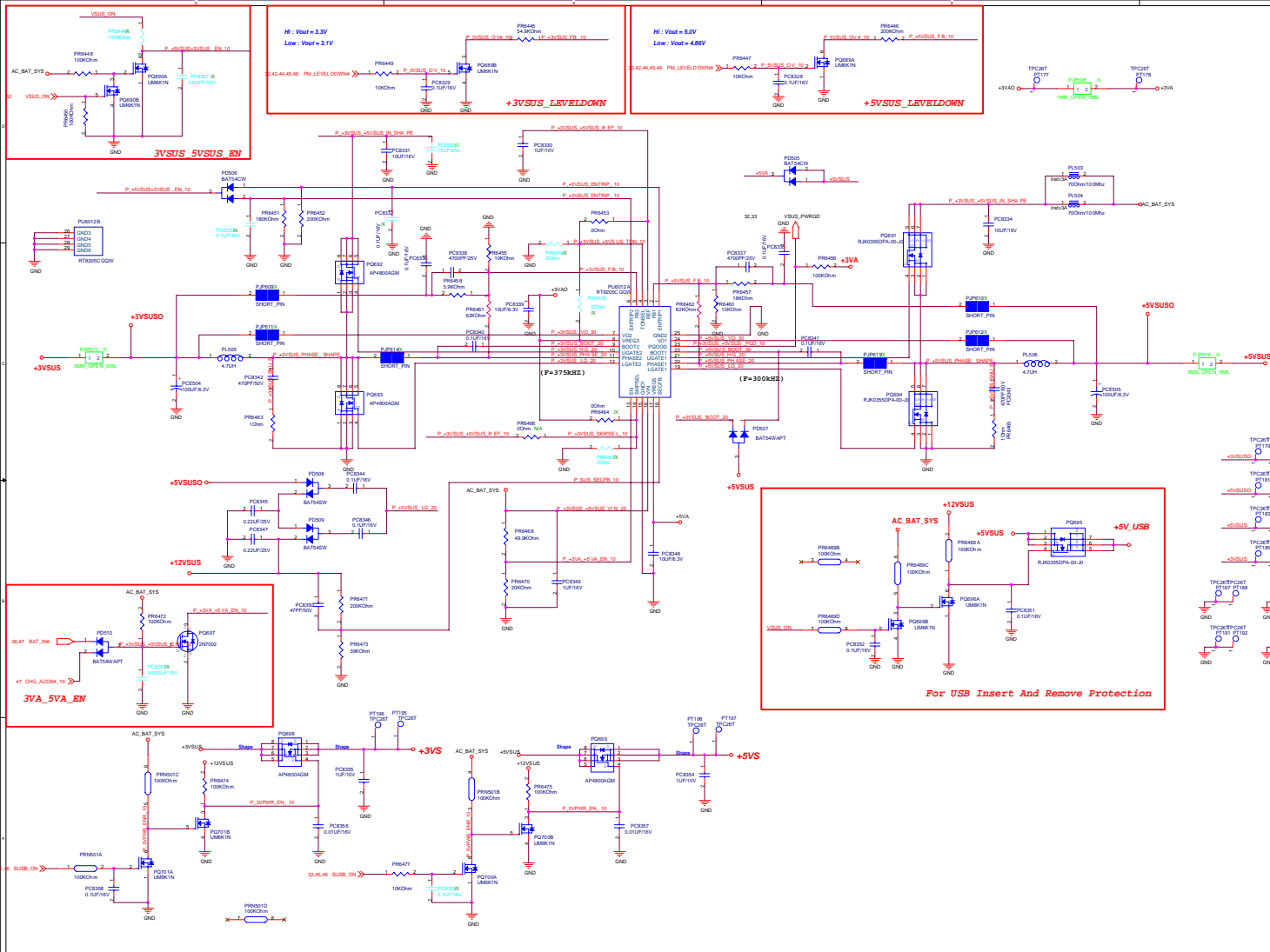
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	VID-100mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

<Core Design>

ASUS Title : Vcore
 ASUSTek Computer INC. Engineer: Joy_Zhou

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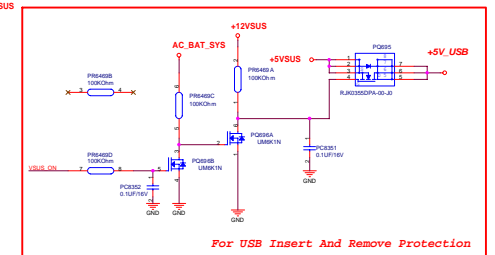


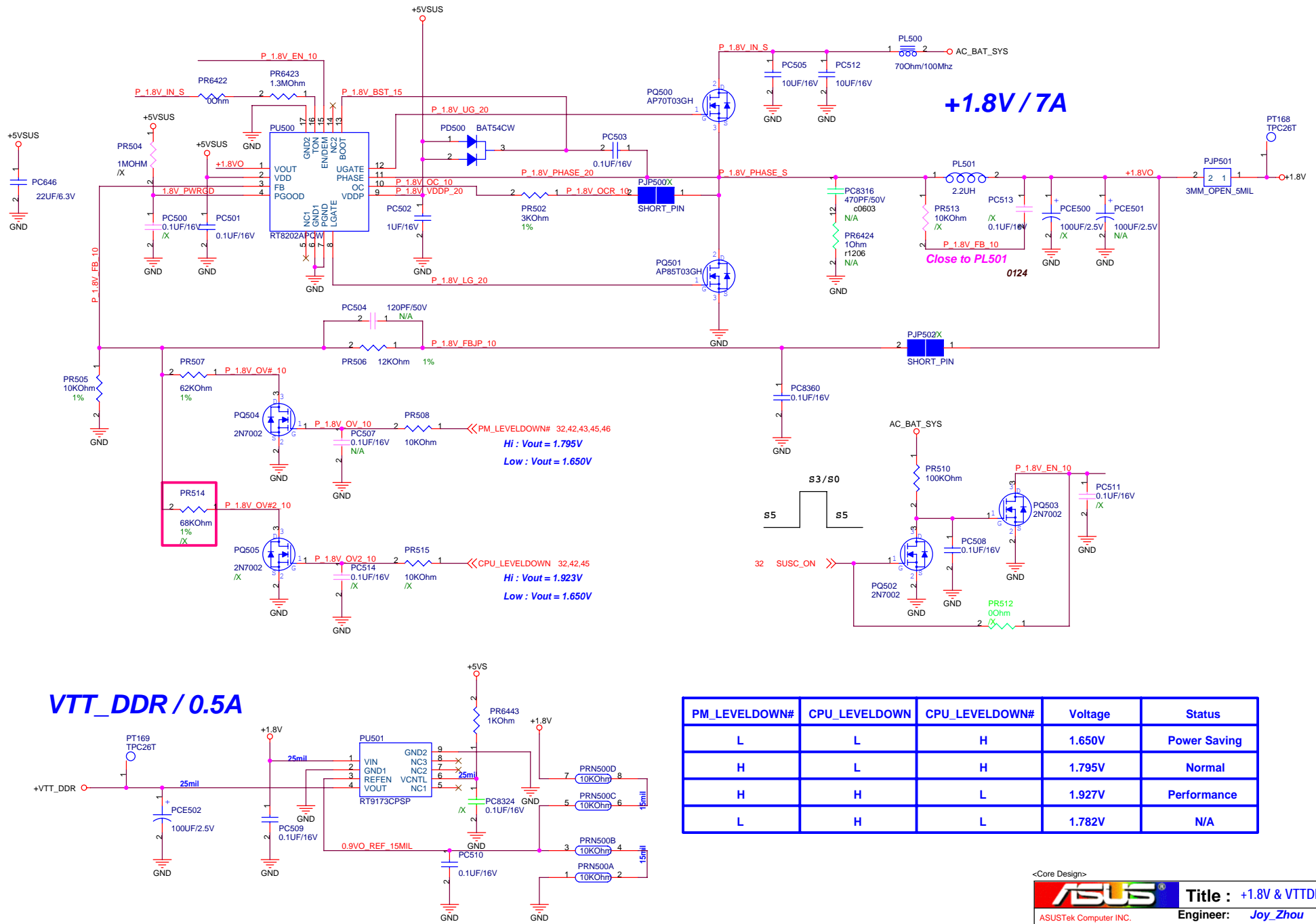
Power stage	+3VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.1A$
2. Ripple Current:	$I_{rip} = 1.36A$ $I_{spec} = 2.5A @ 1\% r_{ps}$
3. Dynamic:	$I_{peak} = 3A$ $ESR / 1\% r_{ps} = 18\text{mohm}$ $V = 54mV$
4. Inductor Spec:	$I_{sat} = 10A$ $I_{dc} = 5.5A$ $DCR = 37\text{mohm}$
5. MOSFET Spec:	H-side MOSFET: AP4800AGM $R_{ds(ON)} = 21\text{mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 9.6A$ ($T = 25^\circ C$) $I_{peak} = 40A$ L-side MOSFET: RAP4800AGM $R_{ds(ON)} = 21\text{mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 9.6A$ ($T = 25^\circ C$) $I_{peak} = 40A$

Power stage	+5VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.67A$
2. Ripple Current:	$I_{rip} = 2.07A$ $I_{spec} = 2.5A @ 1\% r_{ps}$
3. Dynamic:	$I_{peak} = 3A$ $ESR / 1\% r_{ps} = 18\text{mohm}$ $V = 54mV$
4. Inductor Spec:	$I_{sat} = 10A$ $I_{dc} = 5.5A$ $DCR = 37\text{mohm}$
5. MOSFET Spec:	H-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 10.7\text{mohm}$ ($V_{gs} = 10V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause $\geq 10\mu s$) L-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 10.7\text{mohm}$ ($V_{gs} = 10V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause $\geq 10\mu s$)

Controller	+3VSUS
1. Voltage & Current:	+3VSUS=3.3V@3A
2. Frequency:	fosc=375KHz
3. OCP:	Set PR112=10Kohm Iocp=11.1A
4. POR:	V on = 2.5V
5. UVP:	V uvp = 70% Vout
6. OVP:	V ovp = 115% Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4V
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 110 uF I inrush = 0.165 A

Controller	+5VSUS
1. Voltage & Current:	+5VSUS=5V@3A
2. Frequency:	fosc=300KHz
3. OCP:	Set PR112=10Kohm Iocp=11.1A
4. POR:	V on = 4.35-4.25V V off = 3.9-4.25V
5. UVP:	V uvp = 70% Vout
6. OVP:	V ovp = 115% Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4V
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 110 uF I inrush = 0.275 A





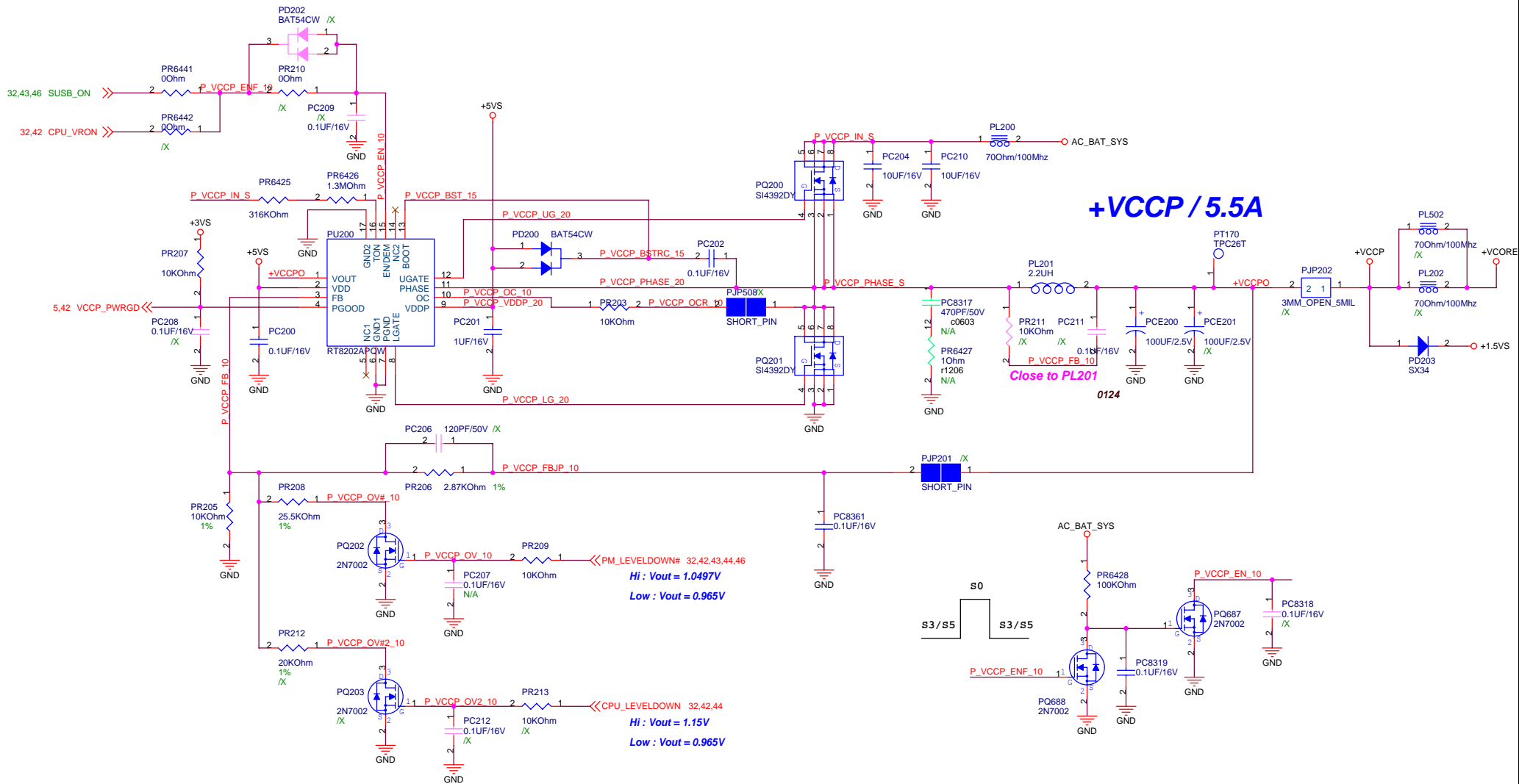
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

<Core Design>

ASUS Title : +1.8V & VTTDDR
 ASUSTek Computer INC. Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

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+VCCP / 5.5A

PM_LEVELDOWN# 32,42,43,44,46
 Hi : Vout = 1.0497V
 Low : Vout = 0.965V

CPU_LEVELDOWN# 32,42,44
 Hi : Vout = 1.15V
 Low : Vout = 0.965V

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

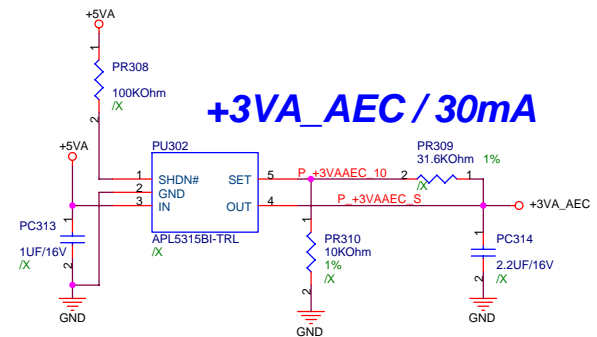
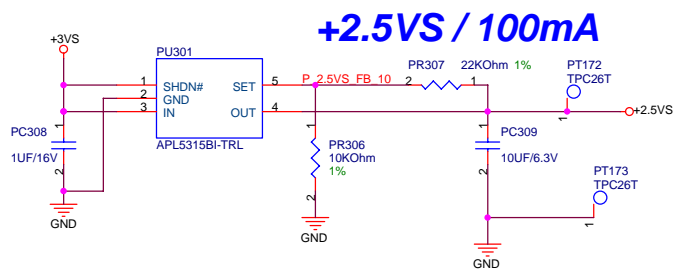
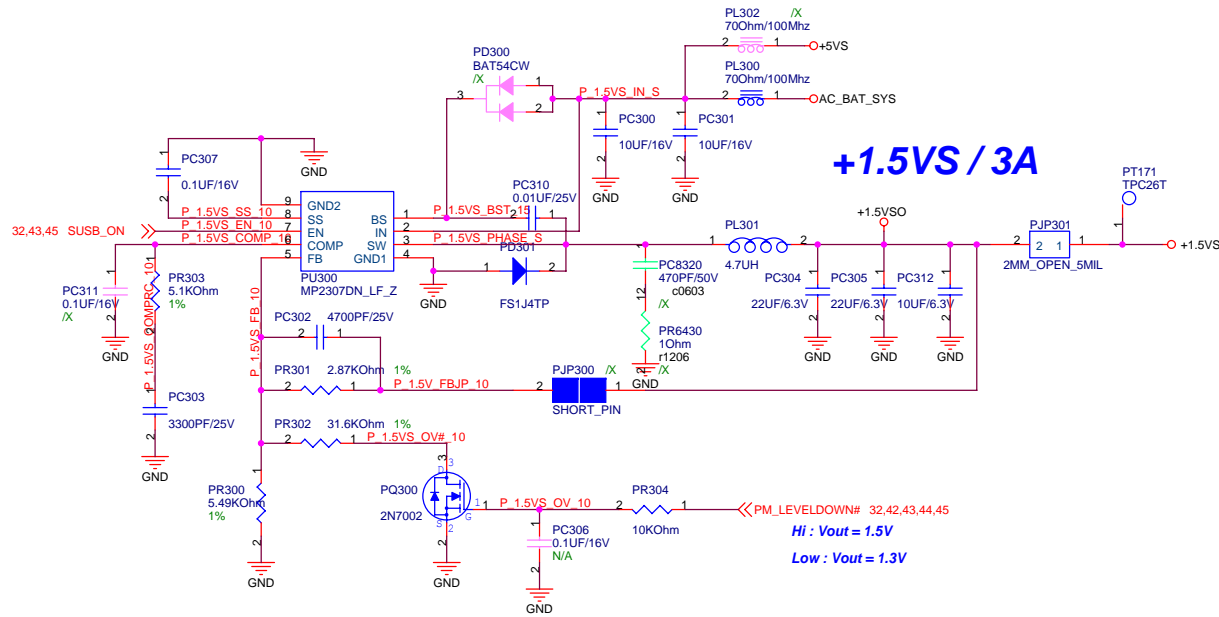
<Core Design>

ASUS Title : VCCP

ASUSTek Computer INC. Engineer: Joy_Zhou

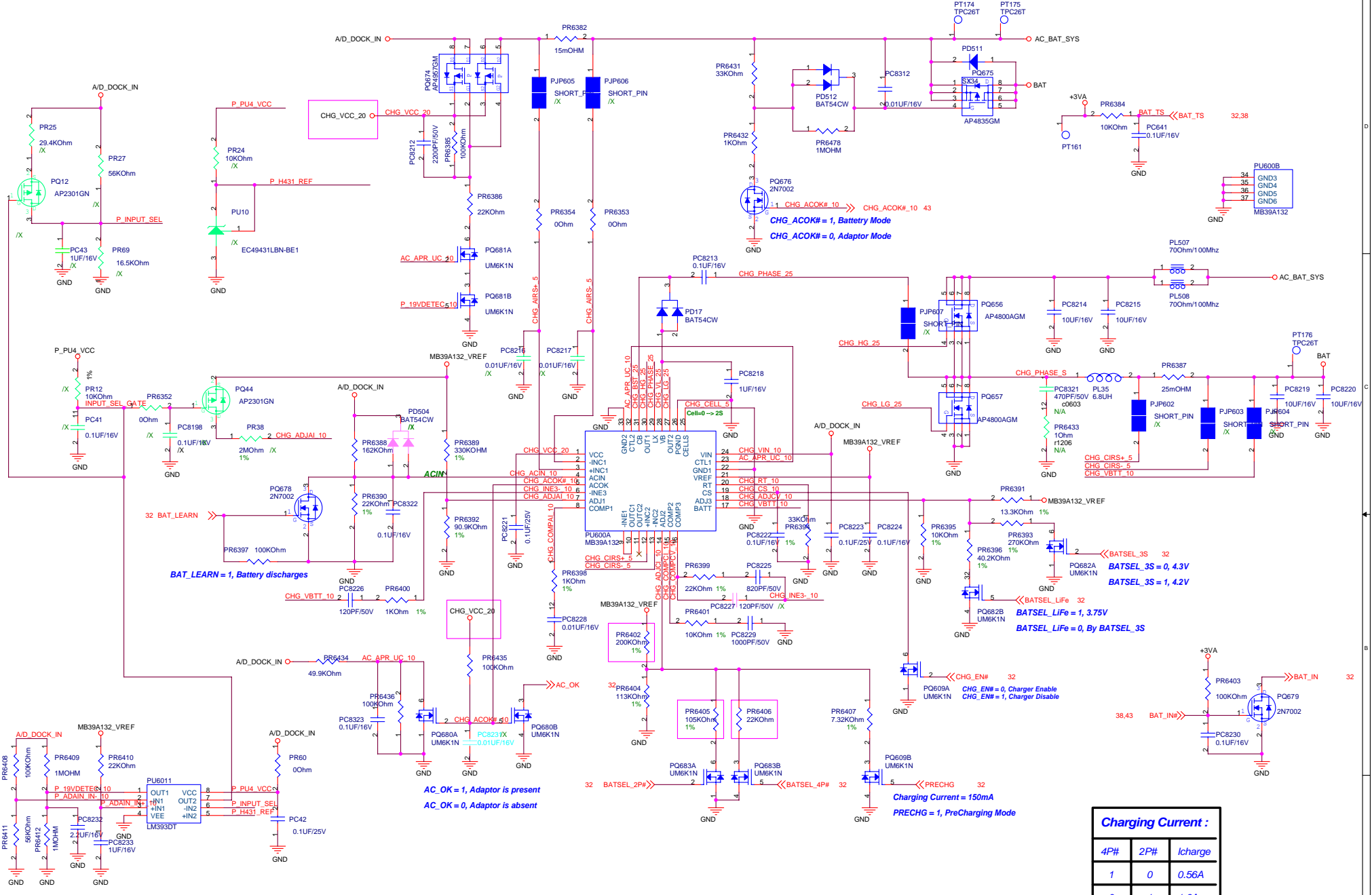
Size	Project Name	Rev
A3	1000H_MB	1.1G

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<Core Design>

ASUS		Title : +1.5V & +2.5V	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name		Rev
A3	1000H_MB		1.1G
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Battery Charging Voltage :
 $V_{adj3} > 4.1V \implies V_{bat} = 4.2V / \text{cell}$
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 * V_{adj3}$

Battery Charging Current :
 $4.4V > V_{adj2} > 0V \implies I_{chg} = (V_{adj2} - 0.075) / (25 * R_s)$

Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 * R_s)$

Pre-Charging Mode :
 Precharging current = 150mA
 $V_{adj2} = 168.75mV$

Adaptor Max. Current :
 $PR600 = 235.8K; I_{limit} = 2.170A; 20.615W (9.5V/22W)$
 $PR600 = 185.3K; I_{limit} = 2.677A; 32.124W (12V/36W)$

ACIN Threshold = 1.25V
 Adaptor > 8.63V, System Powered by Adaptor
 Adaptor < 8.63V, System Powered by Battery

Prevent Input from 19V :
 Adaptor > 13.06V, PQ603B Turn-off
 Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :
 $BAT_ID = 1, 2 \text{ Cells}; V_{adj2} = 0.998V \implies I_{charge} = 1.477A$
 $BAT_ID = 0, 4/6 \text{ Cells}; V_{adj2} = 1.648V \implies I_{charge} = 2.517A$

VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
Soft start: $t_s(s) = 0.13 * CS(uF)$

VTH of -IN1: $1.5V / 62 * (100+62) = 13.06V$


VTH of ACIN: $1.25V / 25 * (185+25) = 10.5V$
 Change PR607 and PR608 value

Charging Current :

4P#	2P#	Icharge
1	0	0.56A
0	1	1.6A
0	0	2.8A



<Core Design>

		Title : Note	
ASUSTek Computer INC.		Engineer: <i>KingCa_Jin</i>	
Size	Project Name		Rev
A3	1000HE_MB		1.0G
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