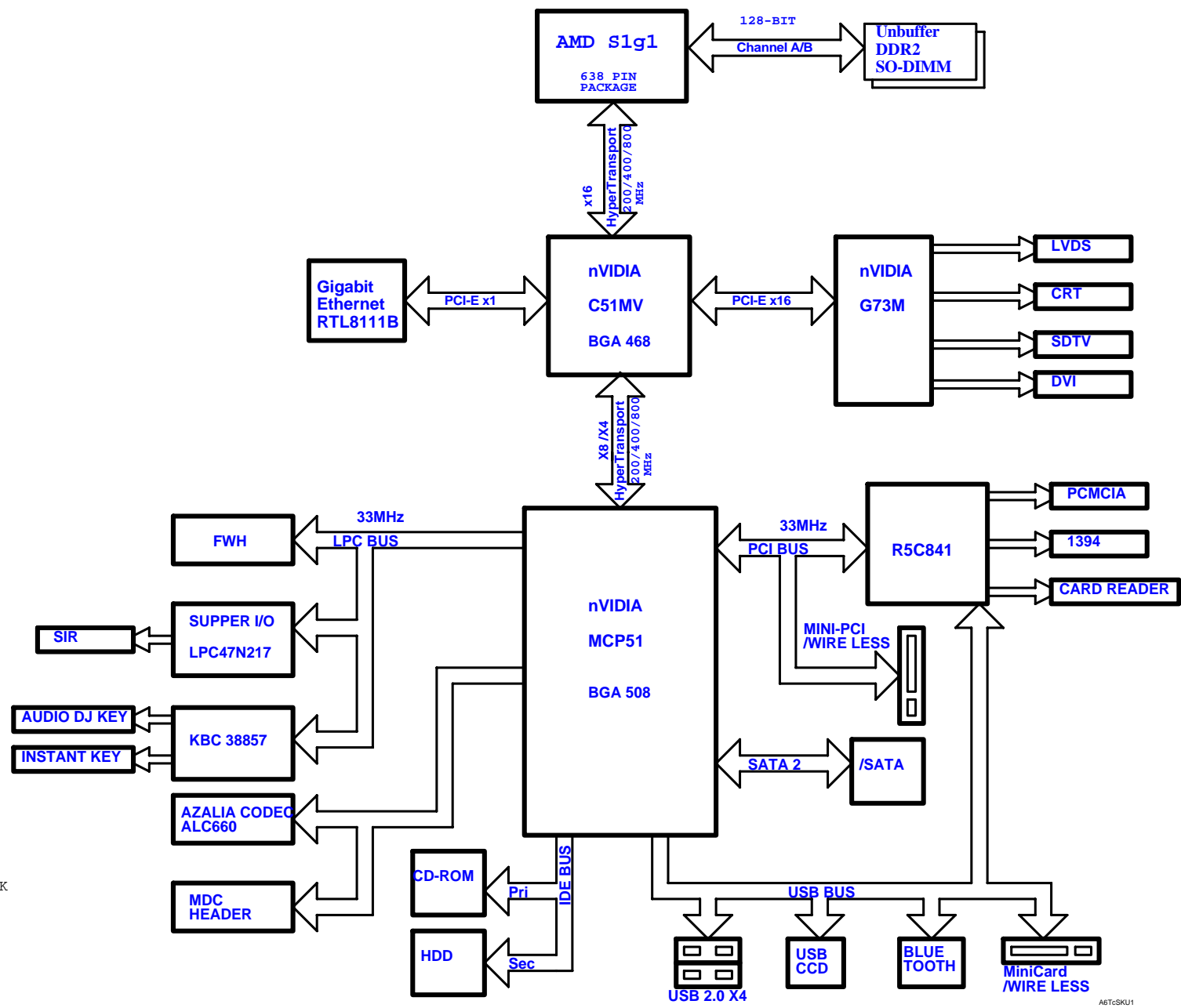


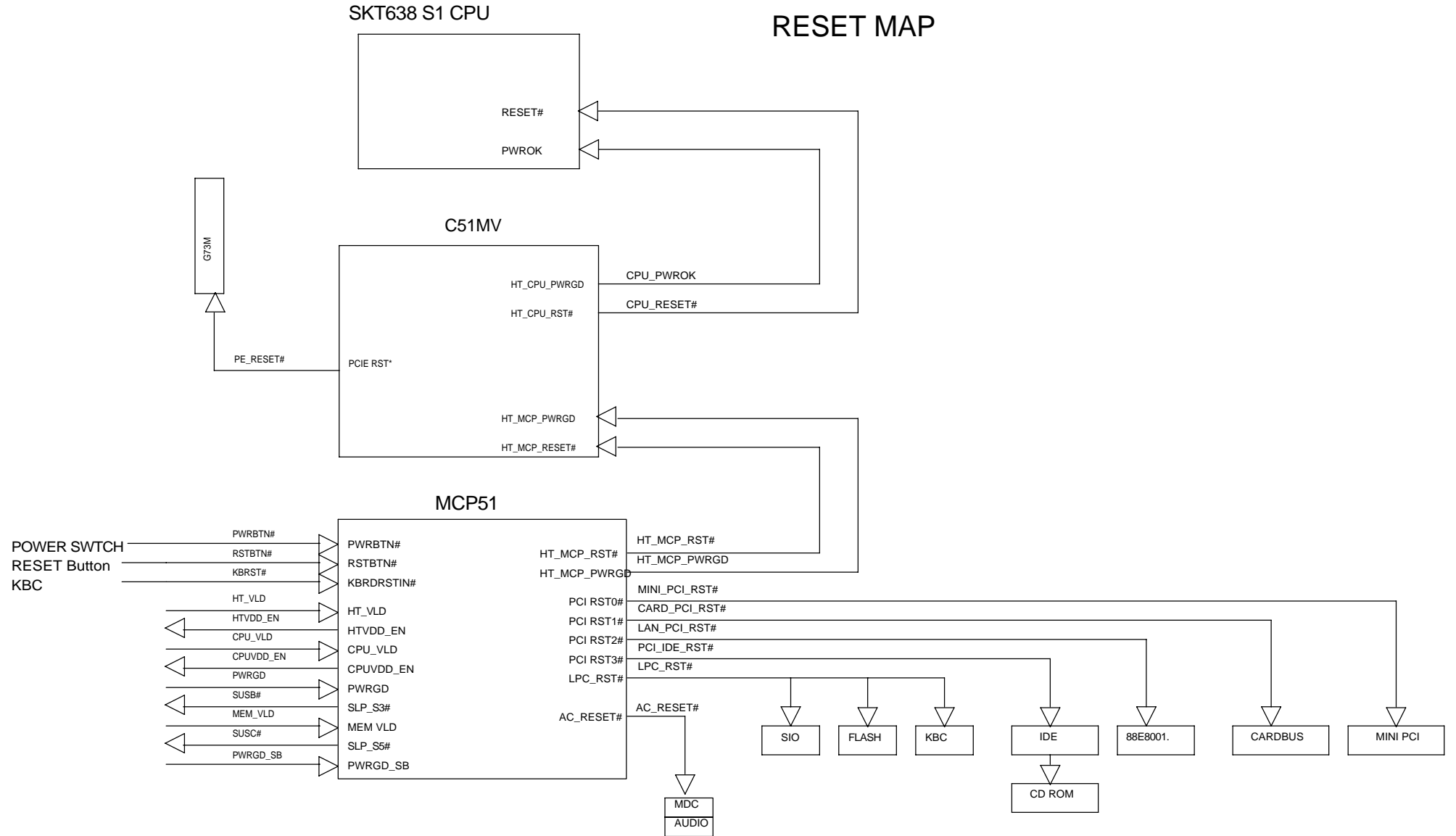
# A6T

REVISION: 1.01

- 01. BLOCK DIAGRAM
- 02. RESET MAP
- 03. CLOCK MAP
- 04. S1\_HT\_C51
- 05. S1\_DDR2
- 06. S1\_CNTL/DEBUG/THERM
- 07. S1\_POWER
- 08. DDR2\_SODIMM
- 09. DDR2\_TER/FETGAGE
- 10. C51\_HT\_CPU
- 11. C51\_HT\_MCP
- 12. C51\_PCIE
- 13. C51\_VIDEO
- 14. C51\_VCC\_GND
- 15. FAN/THERM SENSOR
- 16. MCP51\_HT
- 17. MCP51\_PCI/LPC
- 18. MCP51\_IDE/SATA
- 19. MCP51\_USB/AC97/SMB
- 20. MCP51\_RGMI/XTAL
- 21. MCP51\_VCC
- 22. G73M\_PCIE
- 23. G73M\_FB I/F
- 24. G73M\_LVDS/GND
- 25. G73M\_VGA/TV
- 26. G73M\_TMDS/GPIO
- 27. G73M\_XTAL/ROM STRAP
- 28. G73M\_STRAPS
- 29. G73M\_MEM\_PART1
- 30. G73M\_MEM\_PART2
- 31. HDD/CDROM
- 32. MINI PCI
- 33. CARD BUS
- 34. PCMCIA
- 35. 1394/SD\_CARD
- 36. SIO/SIR
- 37. FWH
- 38. KBC
- 39. USB/BLUE TOOTH
- 40. CRT/TV CON
- 41. LVDS/INVERTER
- 42. ALC880
- 43. AMP
- 44. MIC/LINE-IN JACK
- 45. RJ45/11/MDC
- 46. LAN
- 47. BLANK
- 48. FUNCTION KEY
- 49. LED
- 50. POWER SEQUENCE(1)
- 51. POWER SEQUENCE(2)
- 52. SCREW HOLE
- 53. Battery
- 54. CHARGE
- 55. BATLOW/SD#
- 56. LOAD SWITCH
- 57. BLANK
- 58. BLANK
- 59. BLANK
- 60. POWER SEQUENCE BLOK
- 61. POWER BUDGET BLOCK
- 62. BLANK



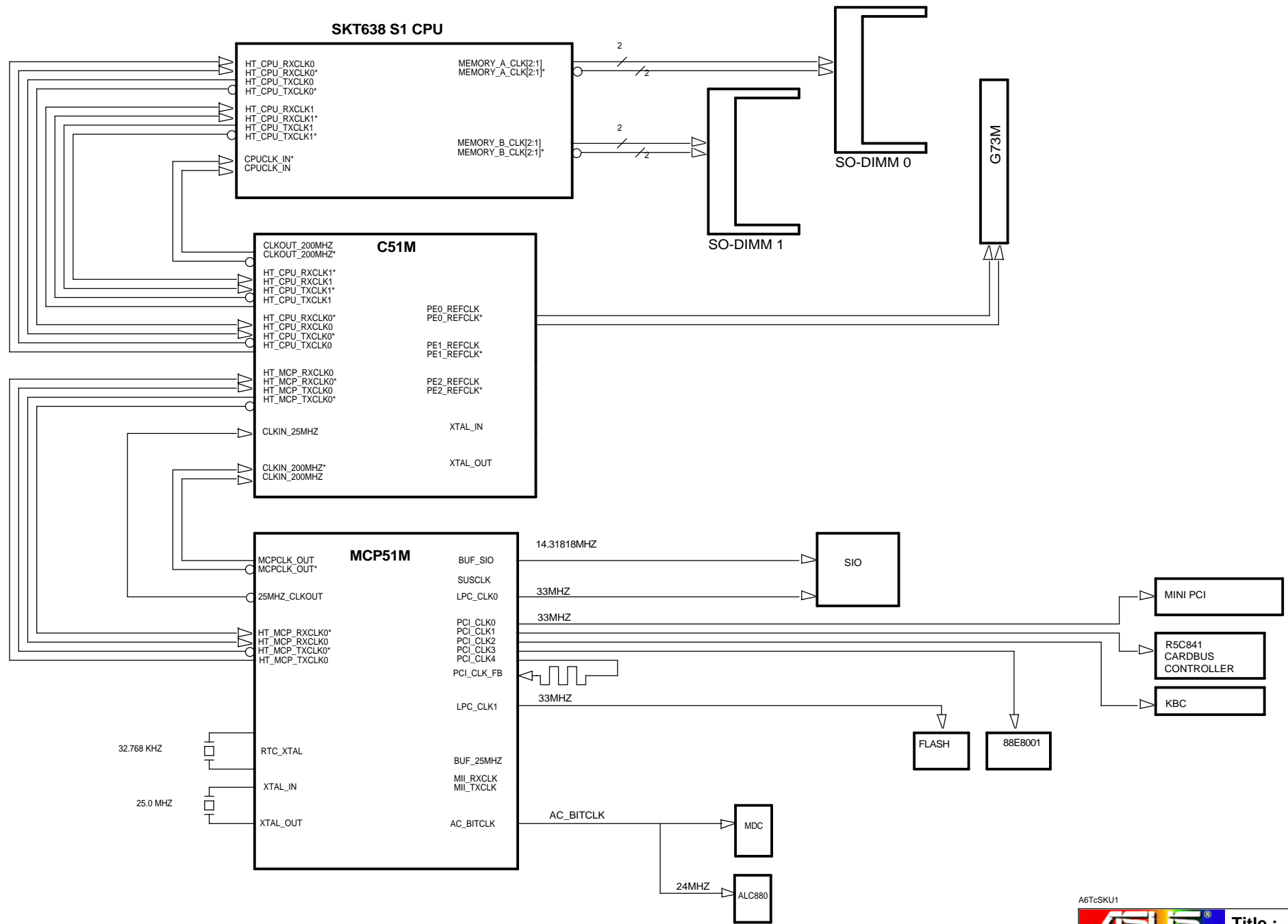
# RESET MAP

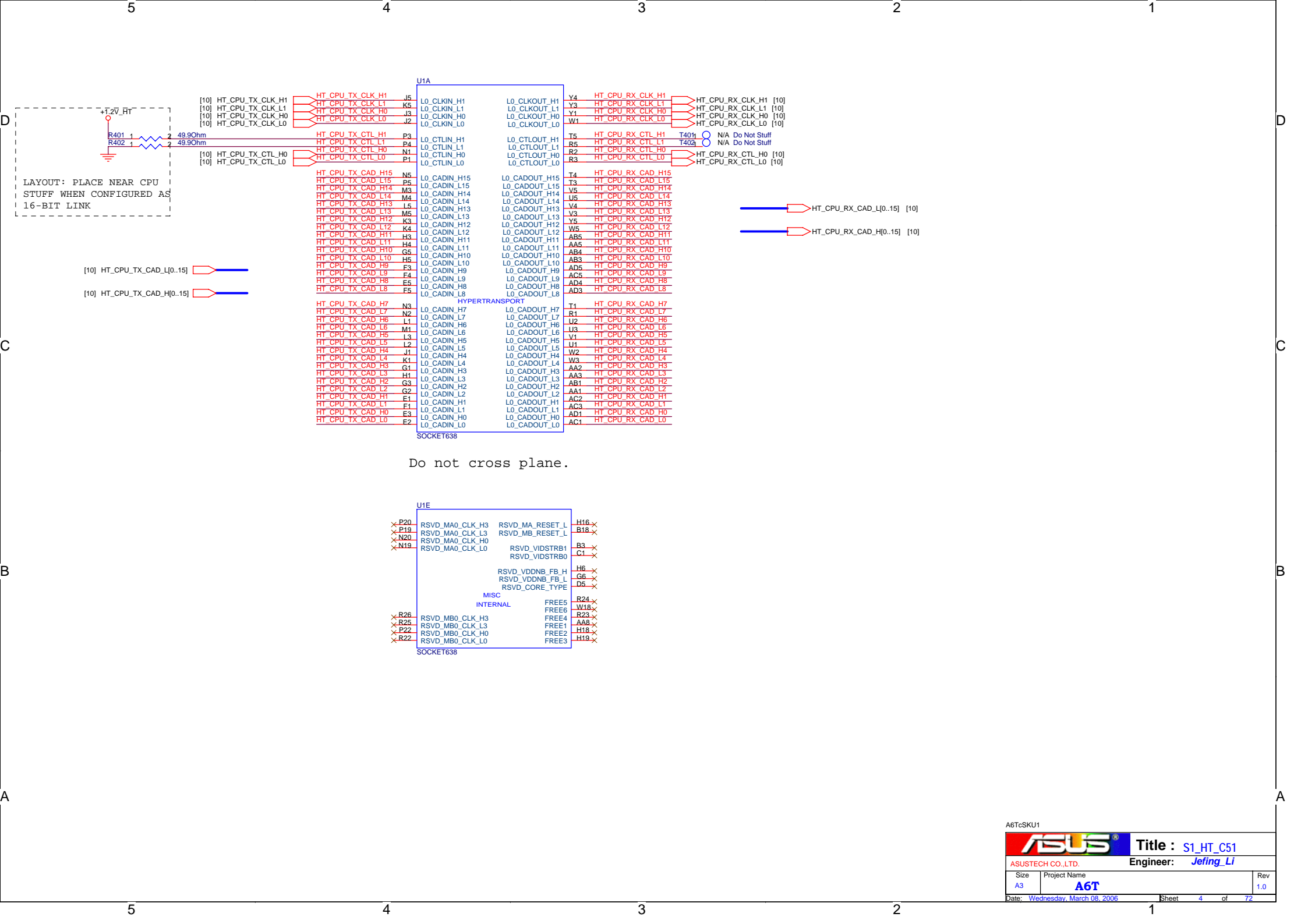


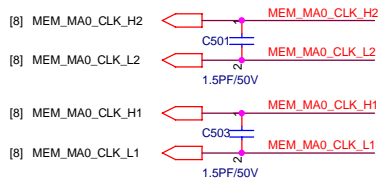
A6TcSKU1

<b>ASUS</b>		<b>Title : RESET MAP</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name	Rev	
A3	<b>A6T</b>	1.0	
Date: Wednesday, March 08, 2006	Sheet 2 of 72		

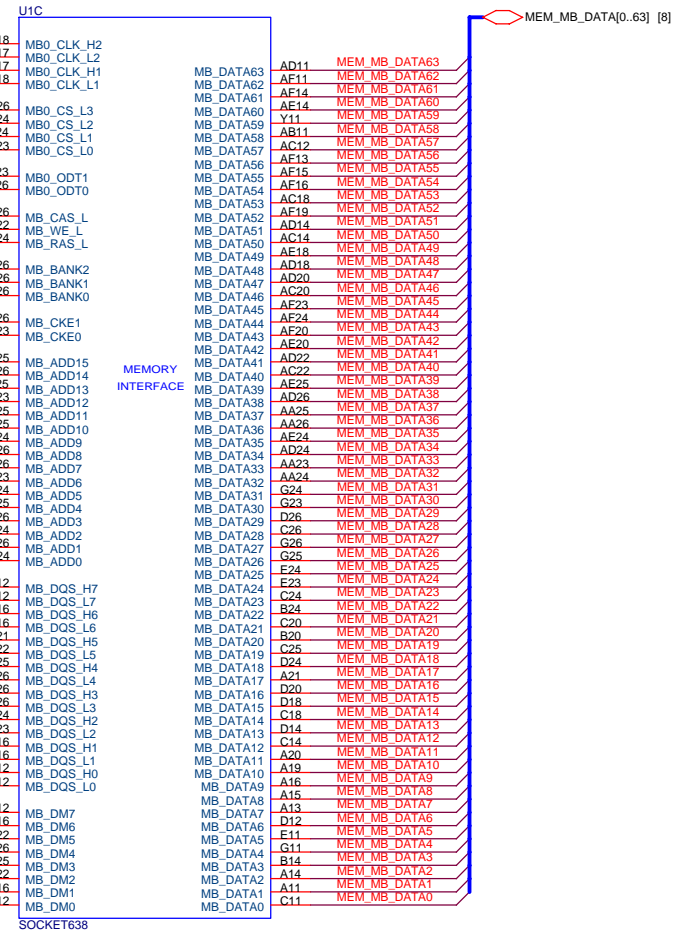
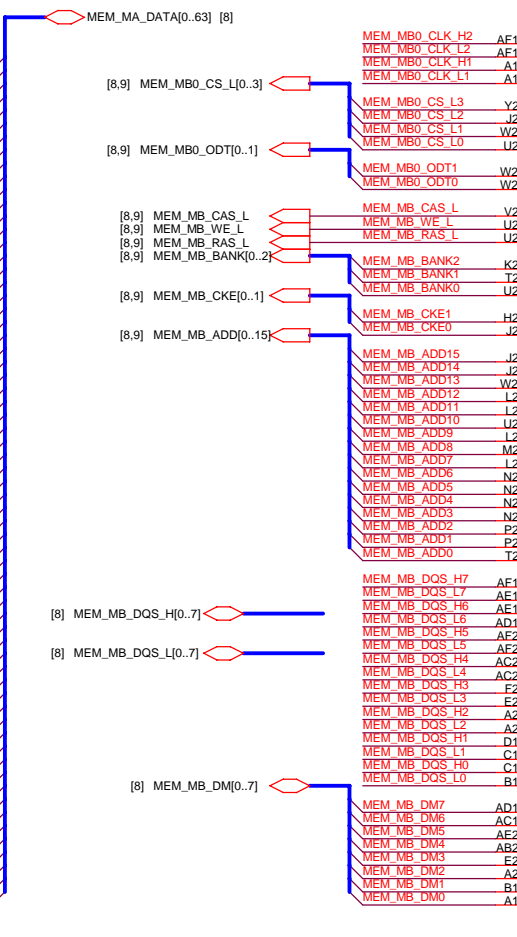
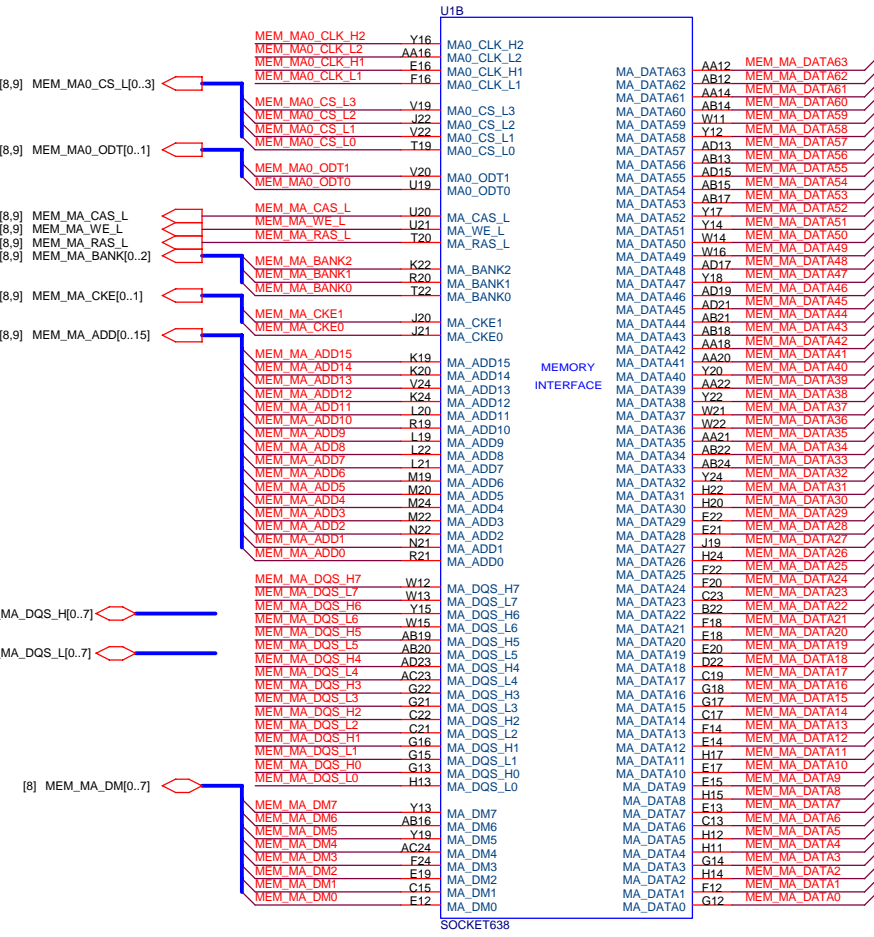
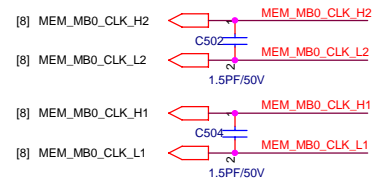
# CLOCK MAP







the cap close to cpu less than 1200mil  
max neckdown to & from caps is 500mil



MEMORY INTERFACE

MEMORY INTERFACE

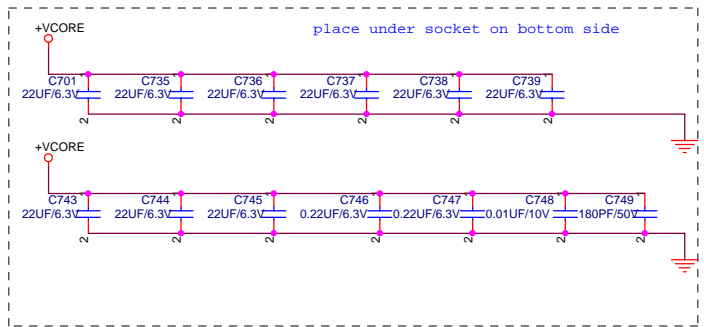
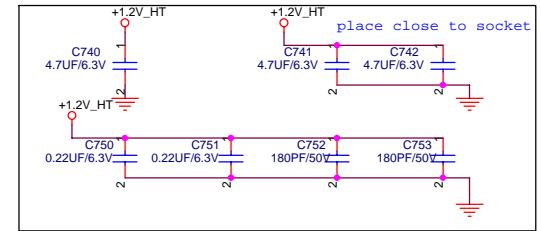
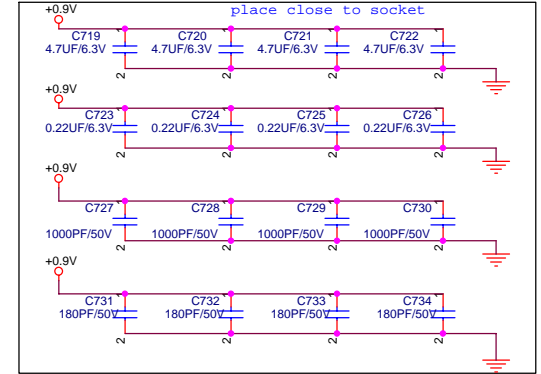
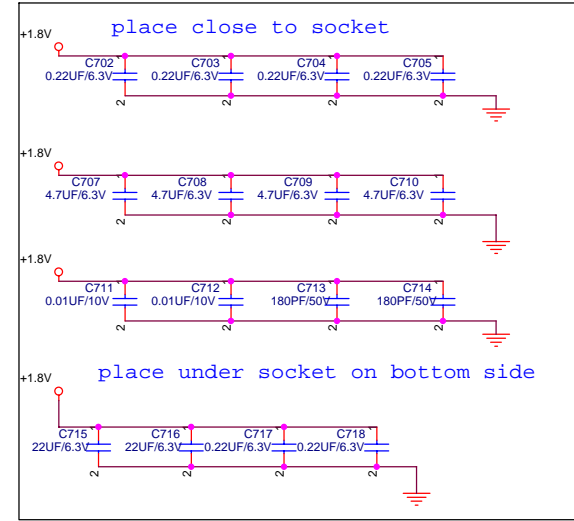
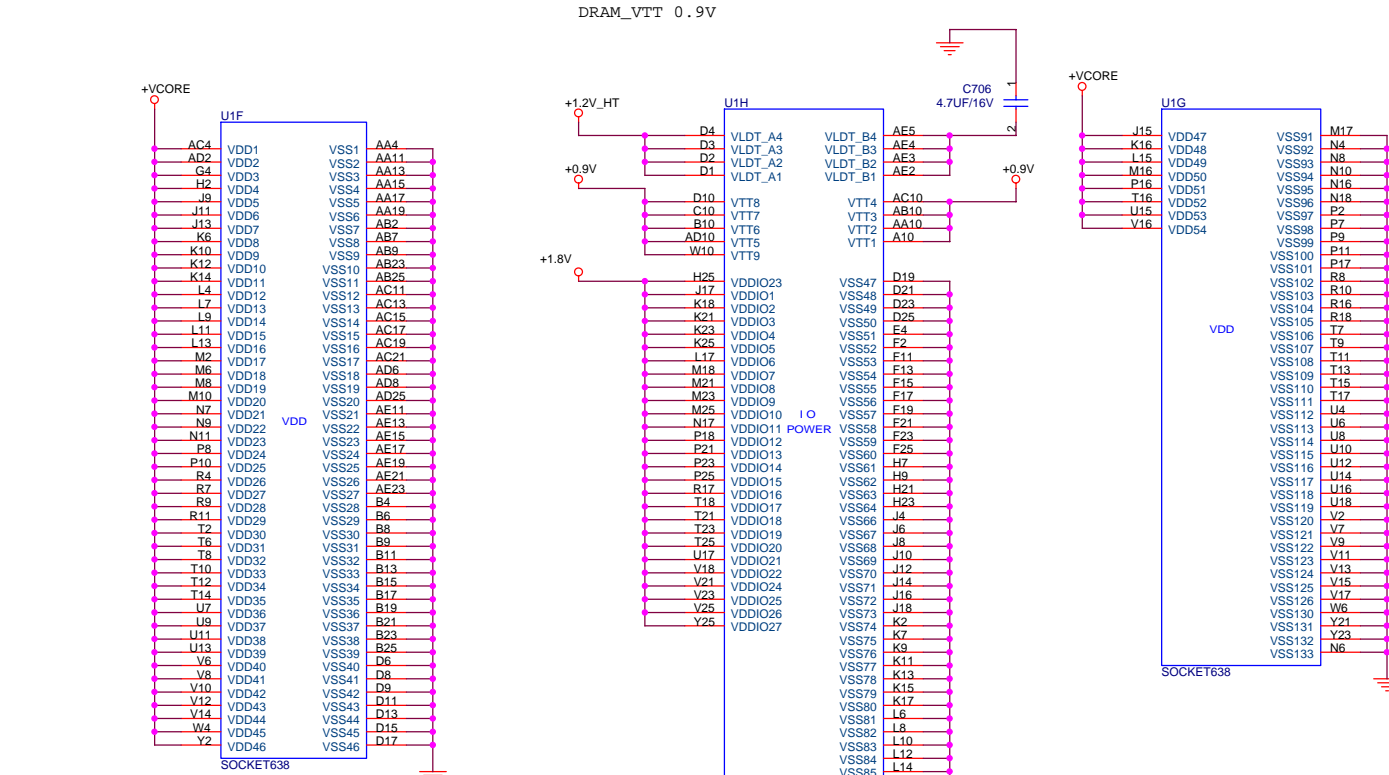
SOCKET638

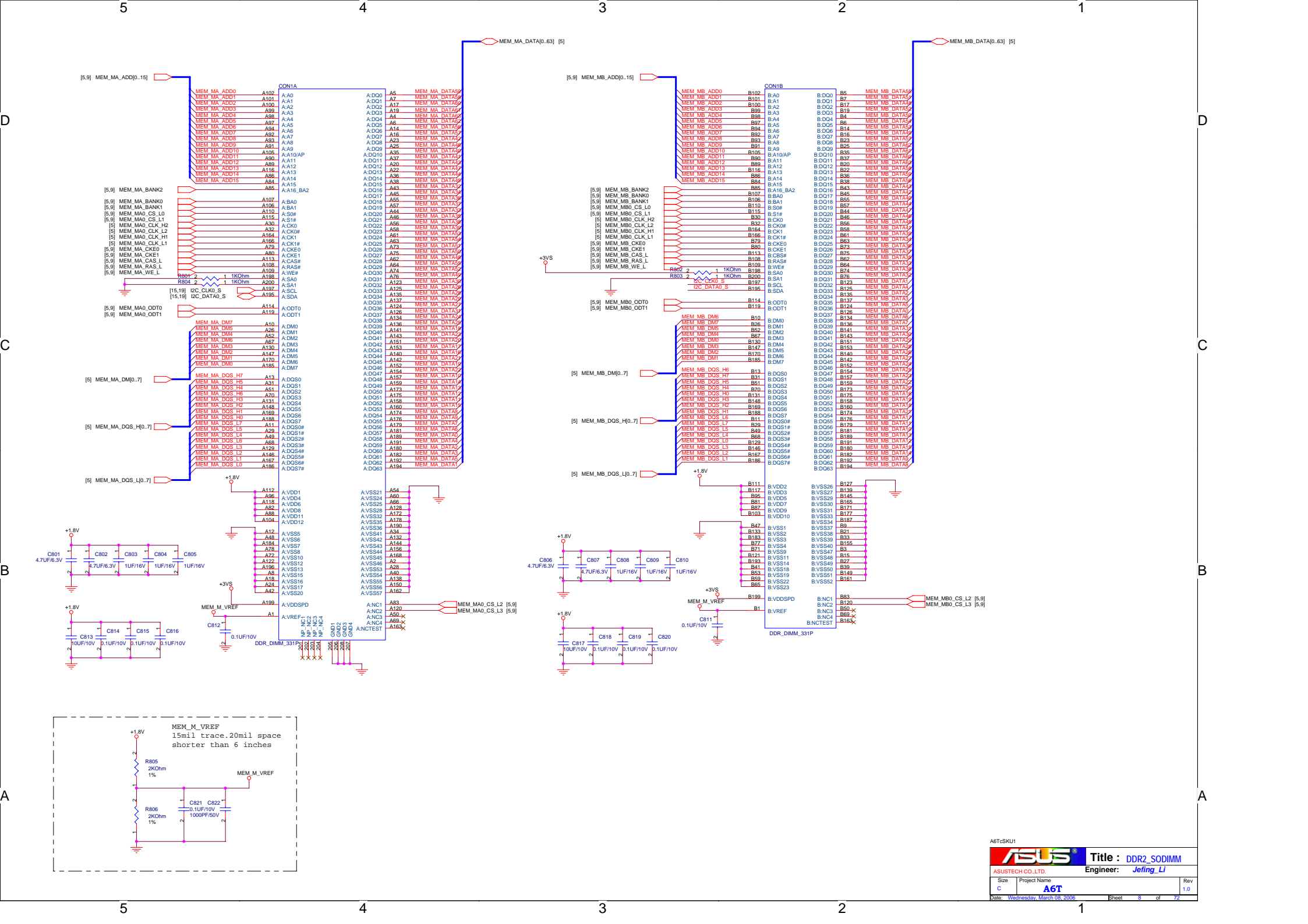
SOCKET638

A6TcSKU1

		Title : S1_DDR2	
		ASUSTECH CO.,LTD. Engineer: Jefing_Li	
Size	Project Name	Rev	
A3	A6T	1.0	
Date: Wednesday, March 08, 2006		Sheet	5 of 72

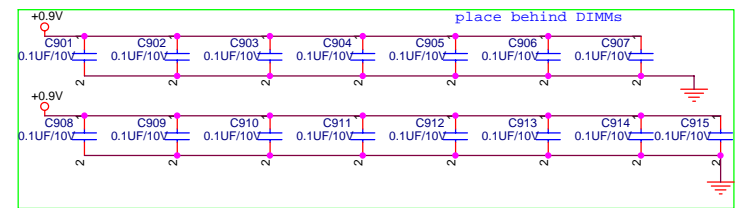
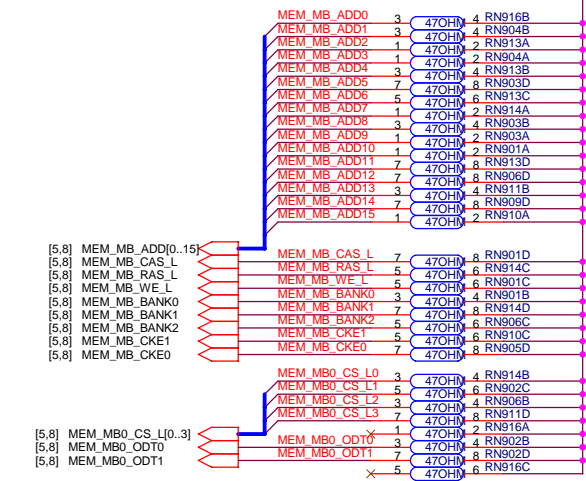
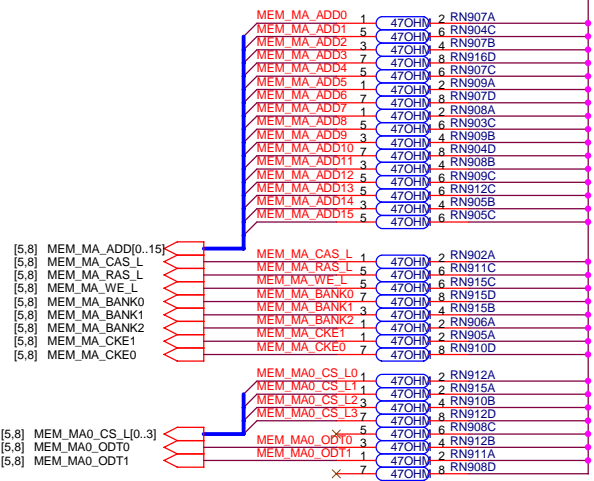




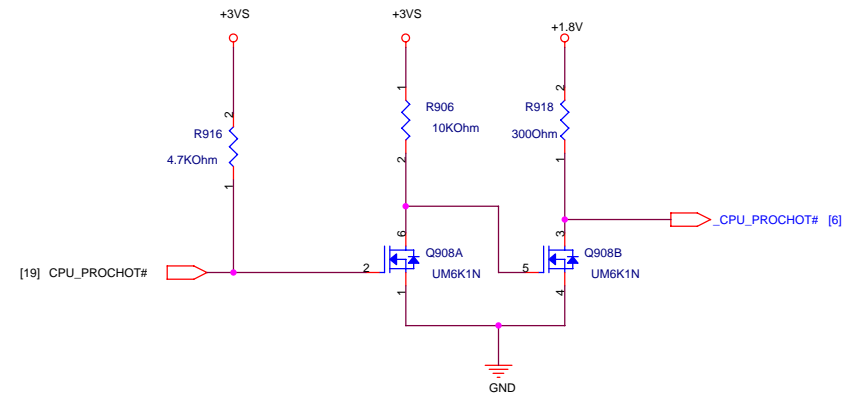
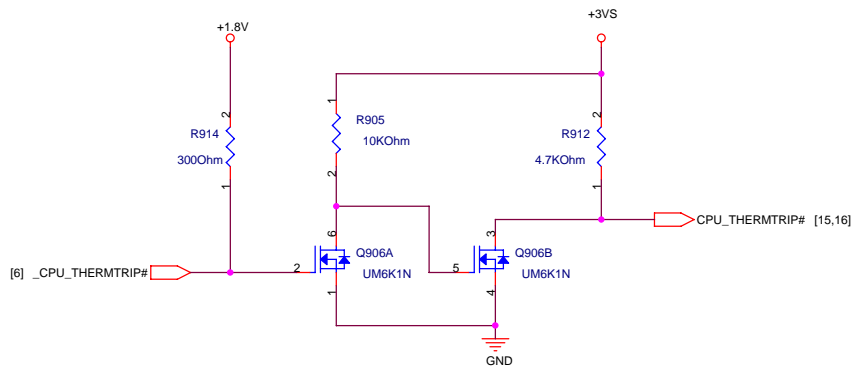


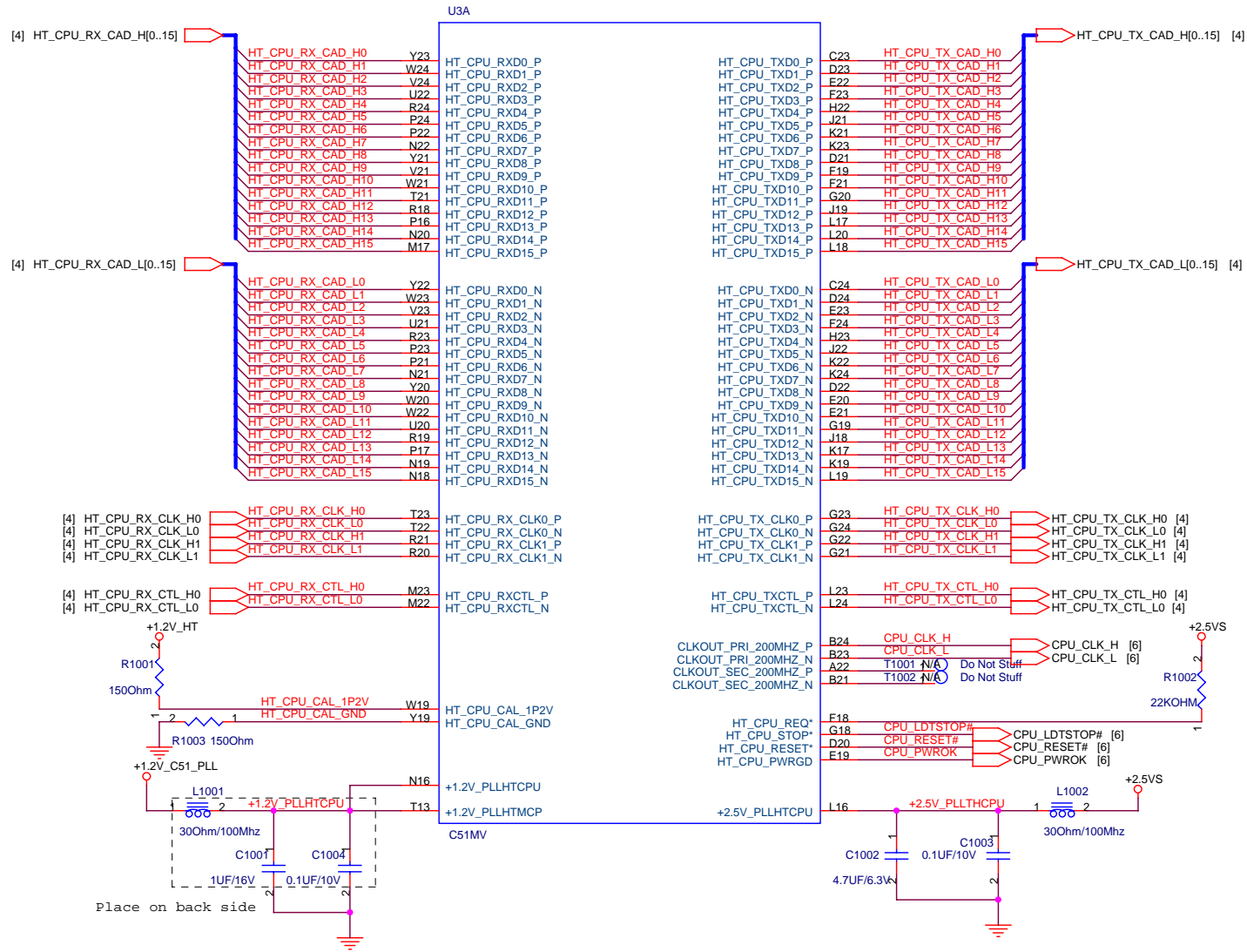


# DDR2 TERMINATION



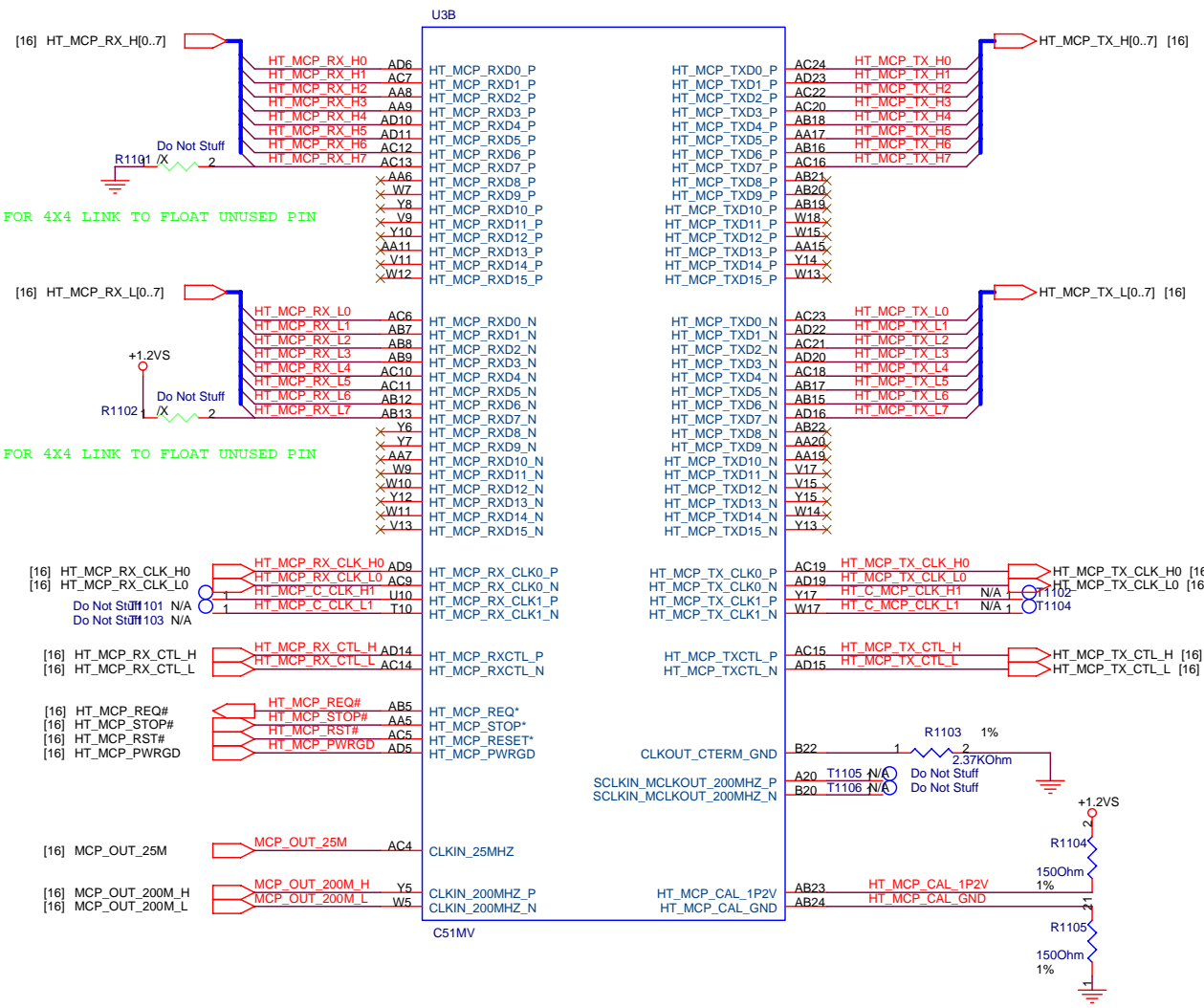
LAYOUT : COULD BE SWAP





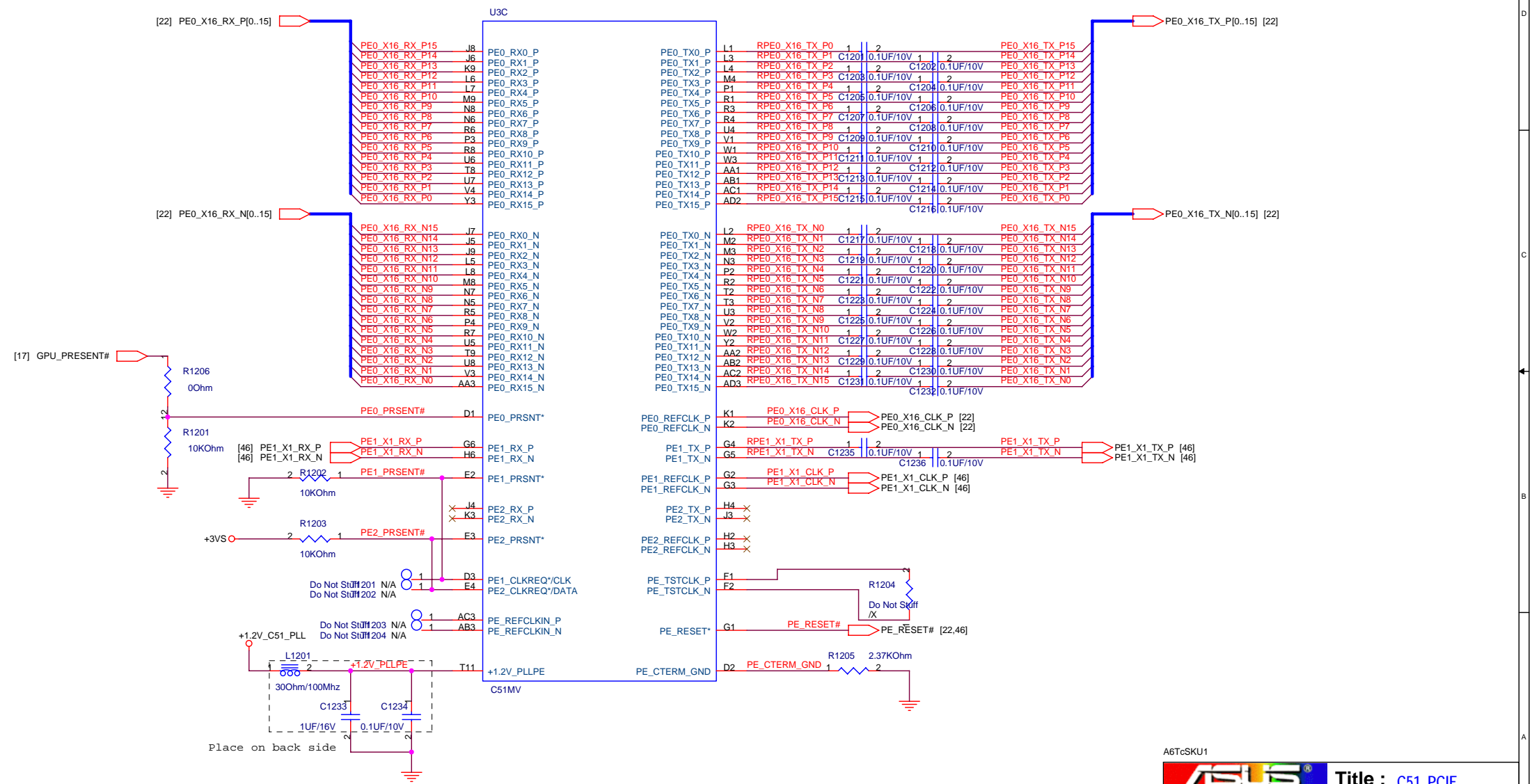
A6TcSKU1

		Title : C51_HT_CPU	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name		Rev
B	A6T		1.0
Date: Wednesday, March 08, 2006		Sheet 10 of 72	



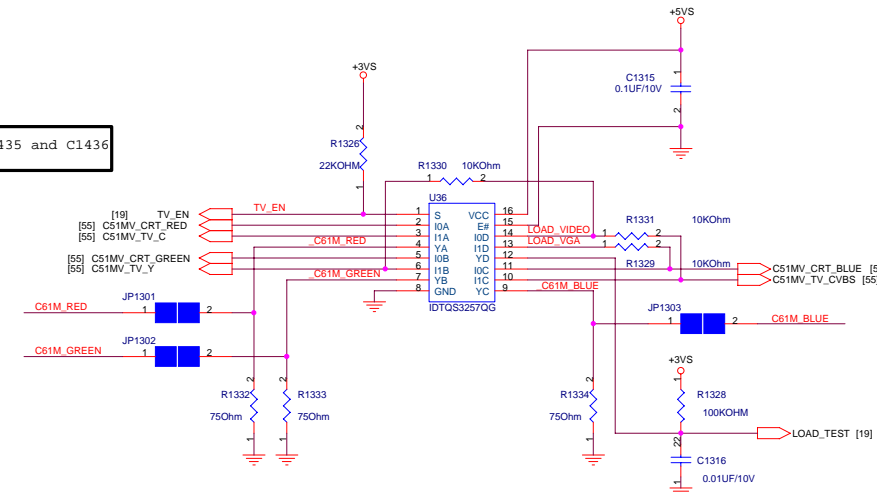
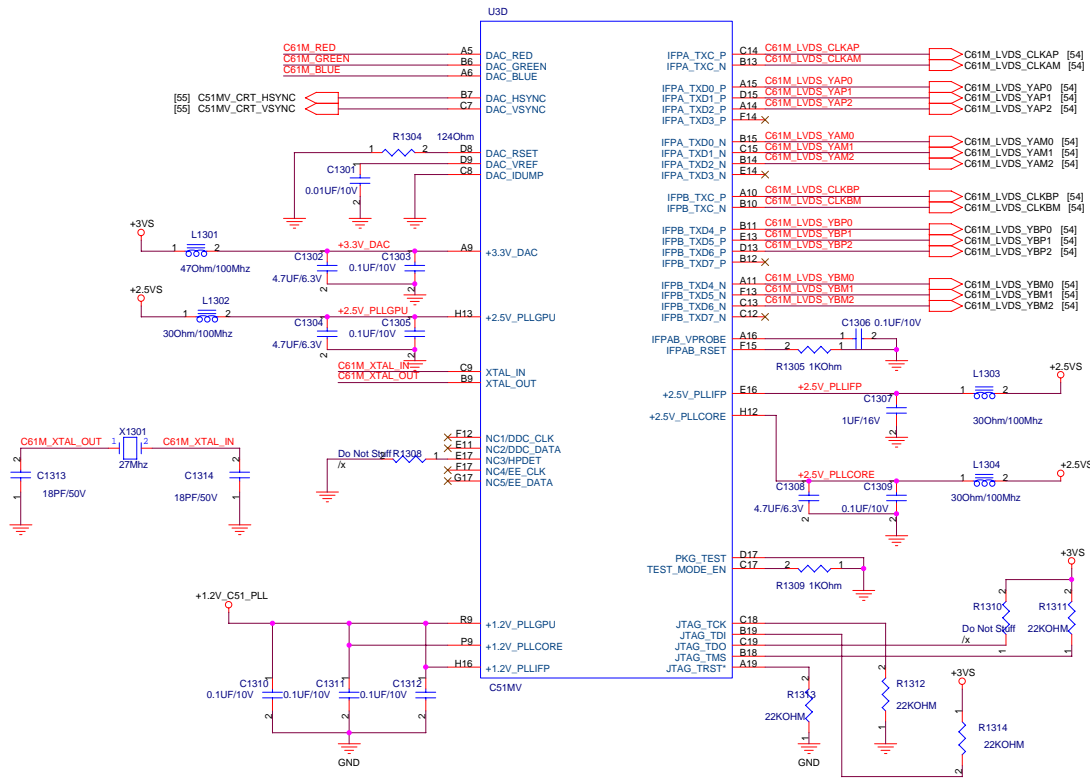
A6TcSKU1

		<b>Title :</b> C51_HT_MCP	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name		Rev
B	A6T		1.0
Date: Wednesday, March 08, 2006		Sheet 11 of 72	



A6TcSKU1

		<b>Title : C51_PCIE</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size B	Project Name <b>A6T</b>	Date: Wednesday, March 08, 2006	Rev 1.0
Date: Wednesday, March 08, 2006		Sheet 12 of 72	





# Fan Speed Control

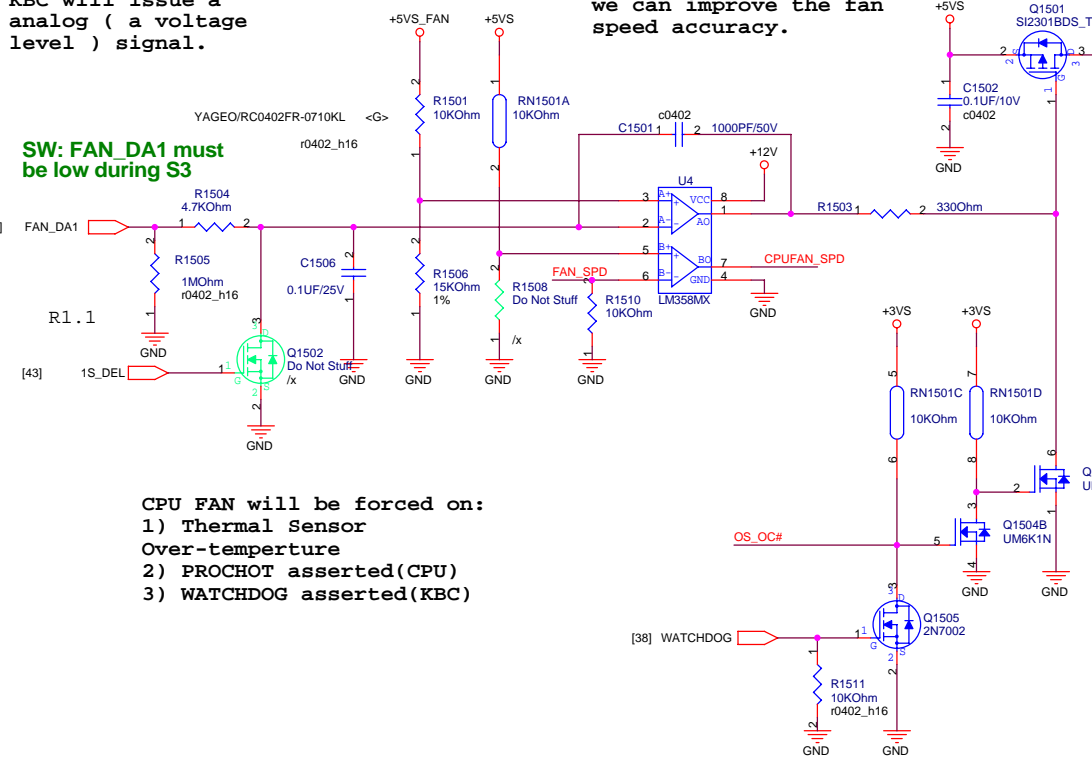
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

KBC will issue a analog ( a voltage level ) signal.

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

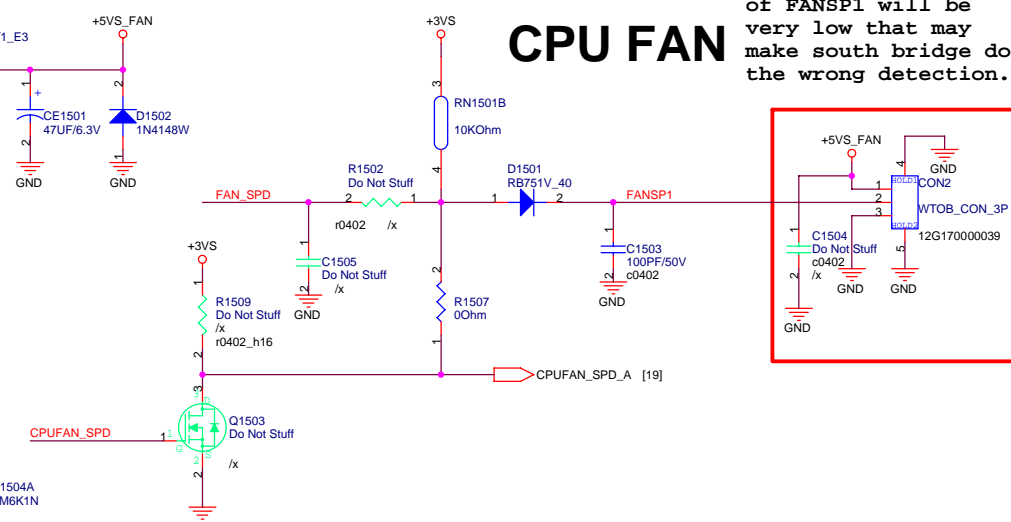
## CPU FAN

SW: FAN\_DA1 must be low during S3



CPU FAN will be forced on:

- 1) Thermal Sensor
- 2) PROCHOT asserted(CPU)
- 3) WATCHDOG asserted(KBC)

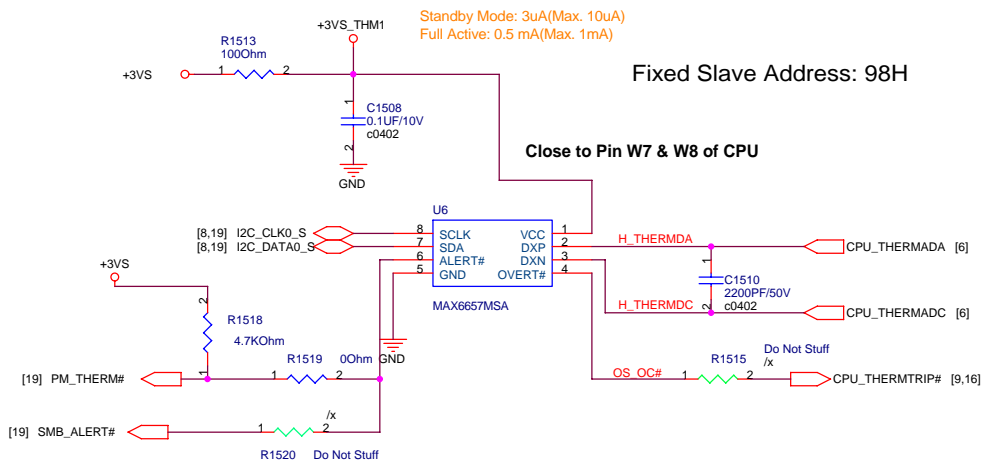


## CPU THERM SENSOR

Standby Mode: 3uA(Max. 10uA)  
Full Active: 0.5 mA(Max. 1mA)

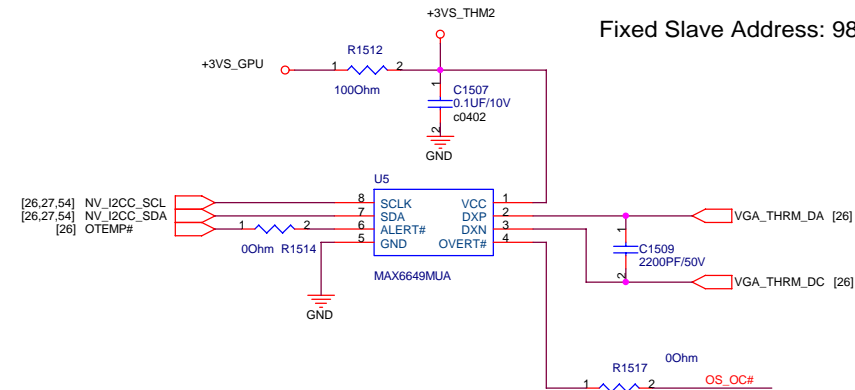
Fixed Slave Address: 98H

Close to Pin W7 & W8 of CPU



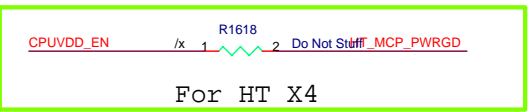
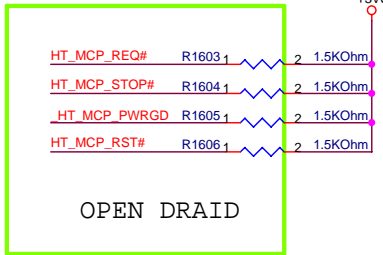
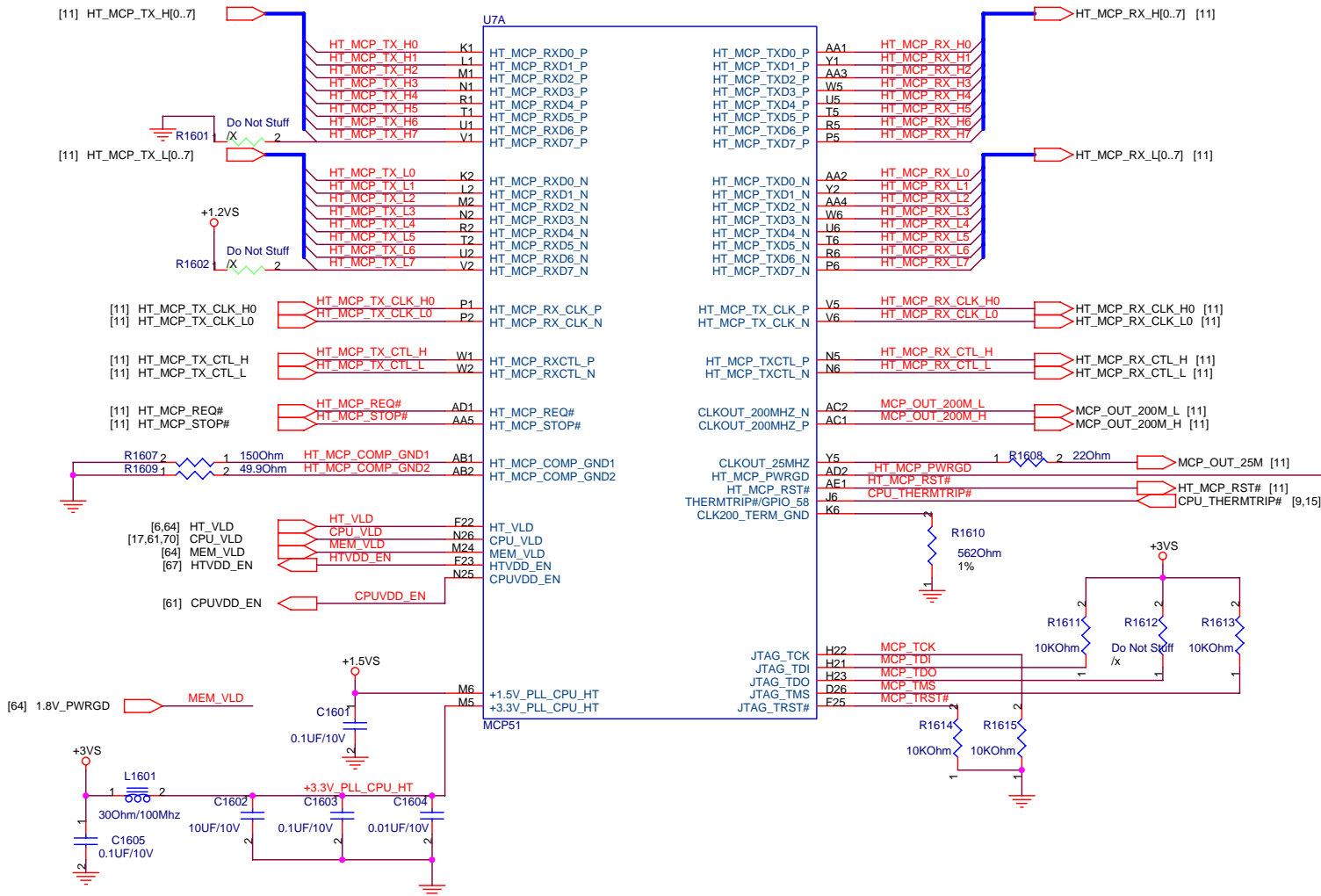
## VGA THERM SENSOR

Fixed Slave Address: 98H



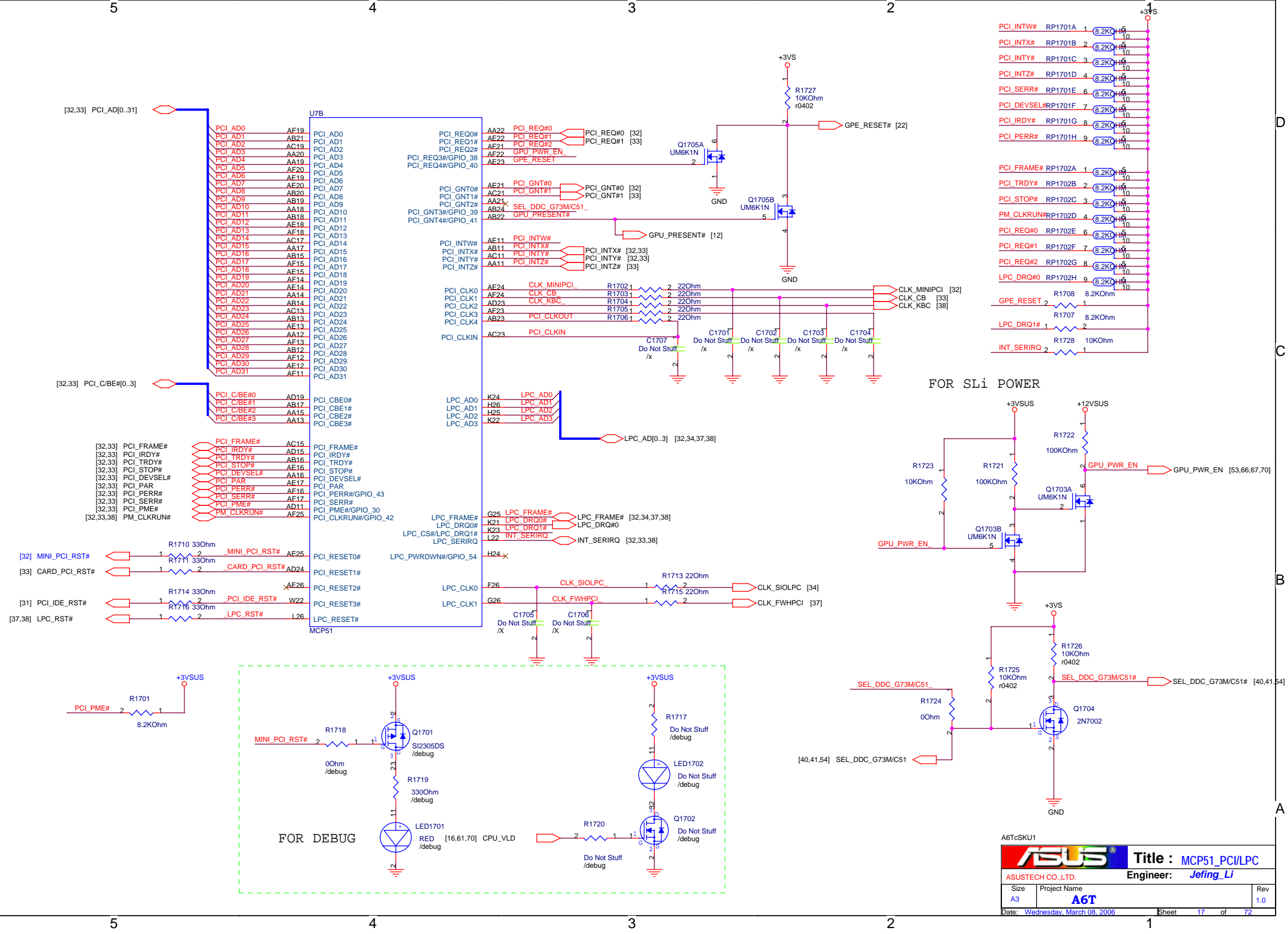
A6TcSKU1

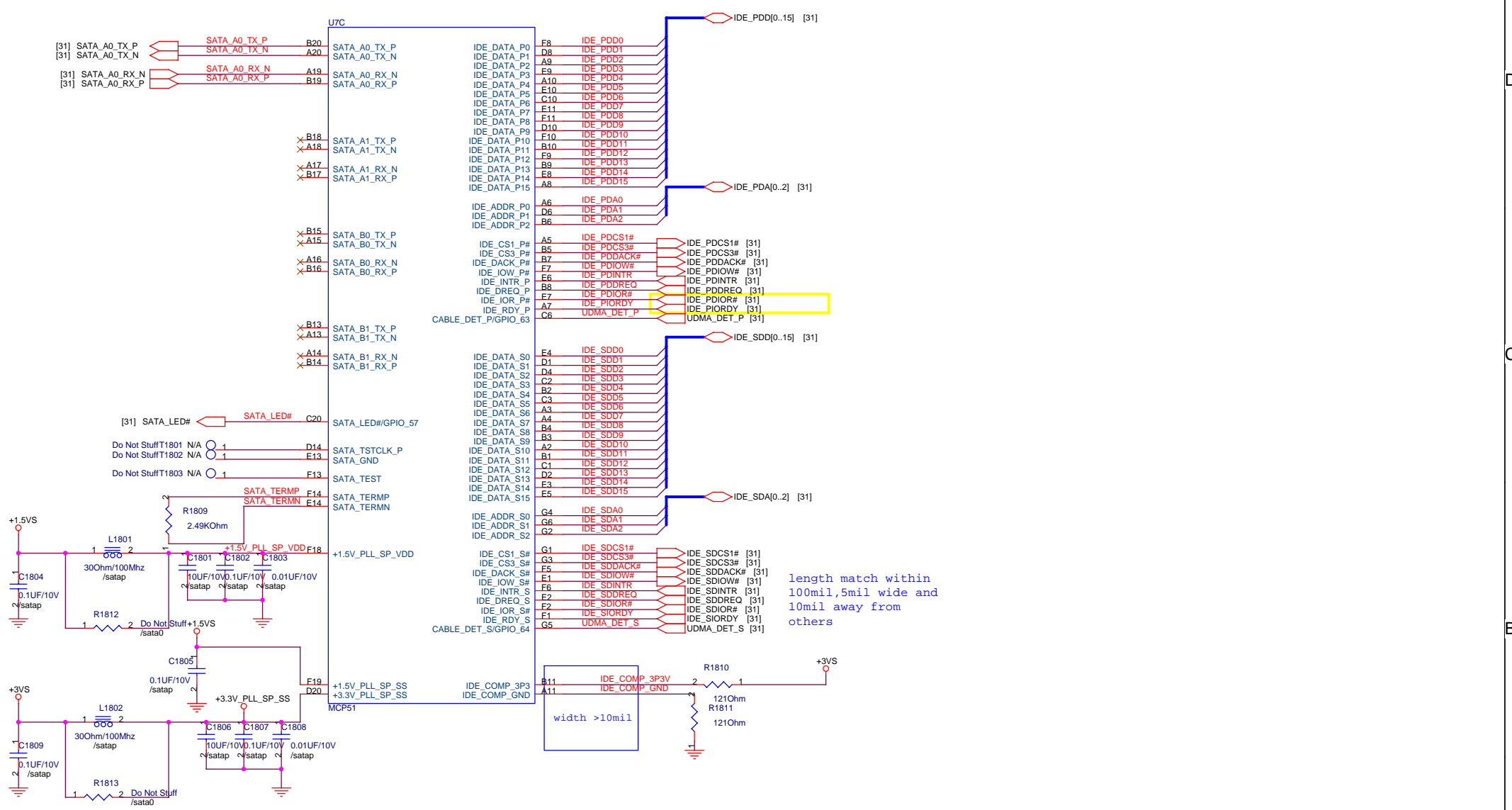
<b>ASUS</b>		<b>Title : FAN/THERM SENSOR</b>	
ASUSTECH CO.,LTD.		Engineer: <b>Jefing_Li</b>	
Size A3	Project Name <b>A6T</b>	Rev 1.0	
Date: Wednesday, March 08, 2006		Sheet	15 of 72

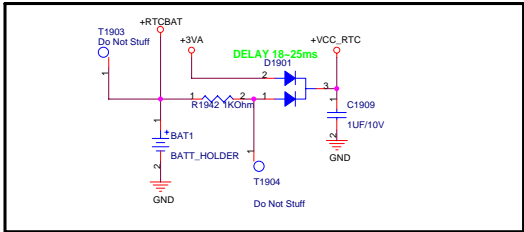
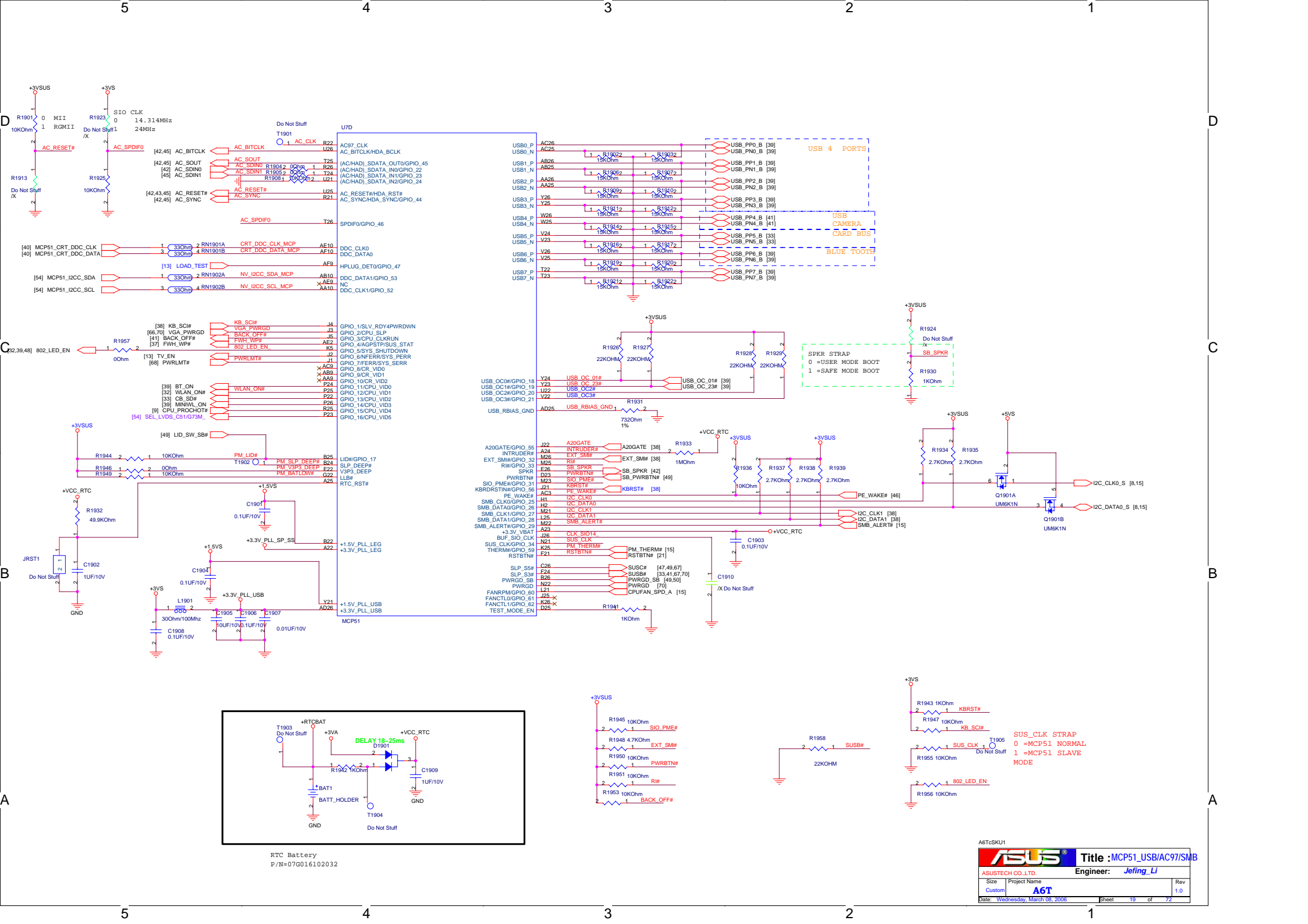


A6TcSKU1		<b>ASUS</b> Title : MCP51_HT	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name	Rev	
B	A6T	1.0	
Date: Wednesday, March 08, 2006		Sheet	16 of 72

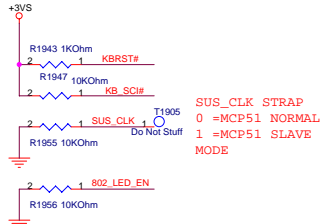




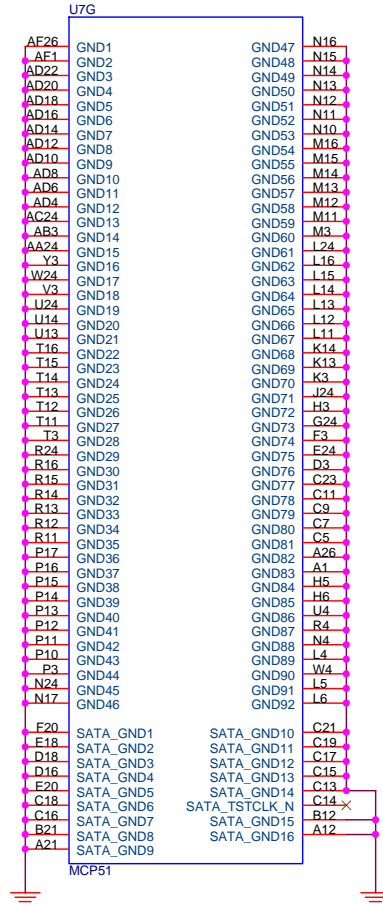
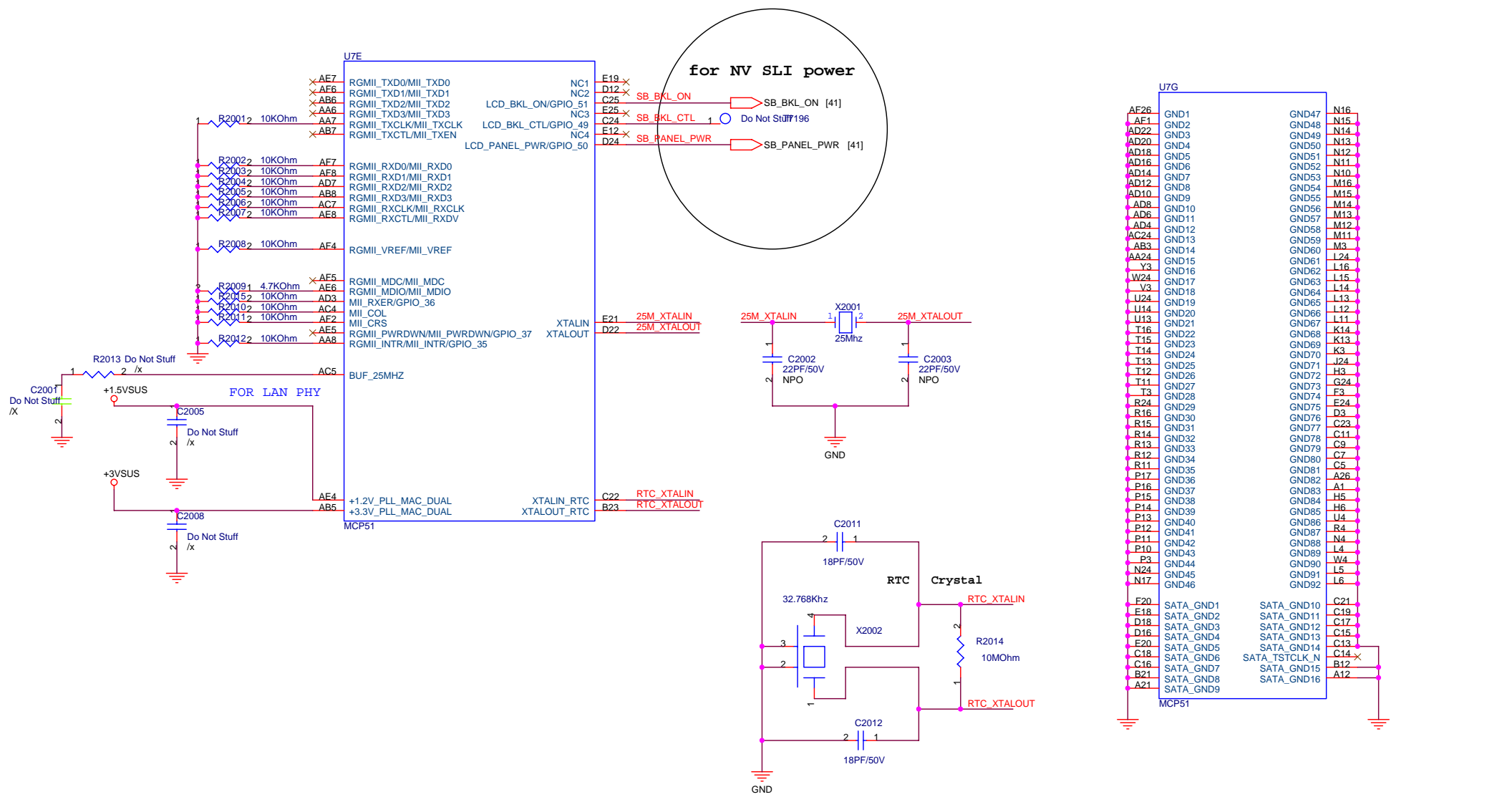




RTC Battery  
P/N=07G016102032

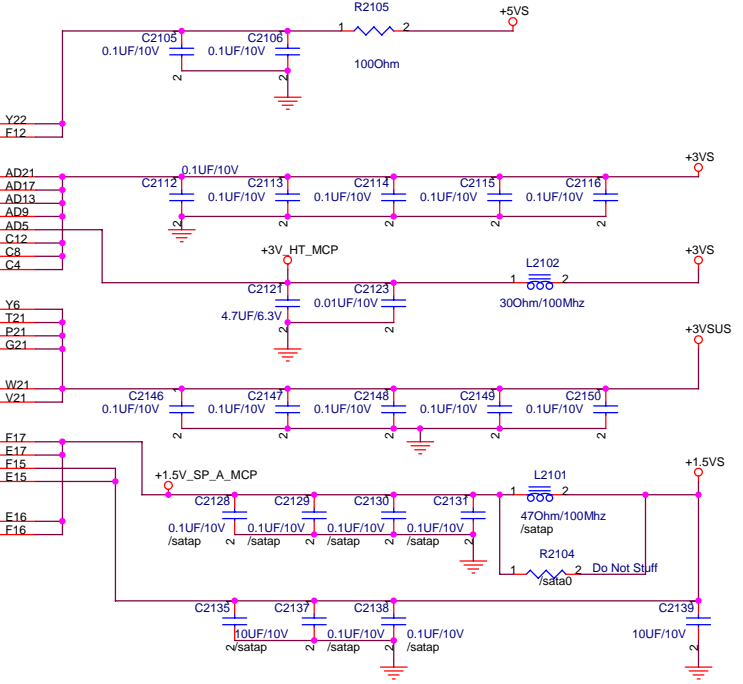
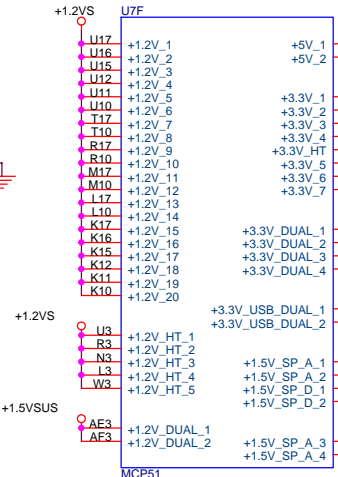
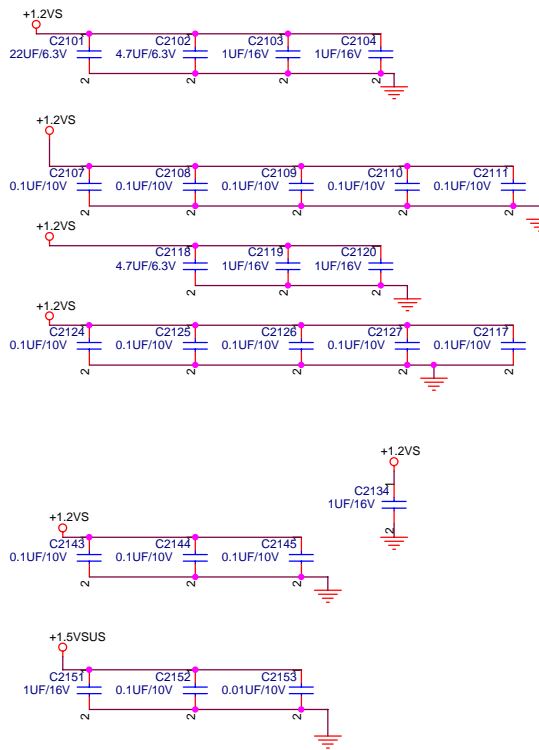


SUS\_CLK STRAP  
0 =MCP51 NORMAL  
1 =MCP51 SLAVE  
MODE

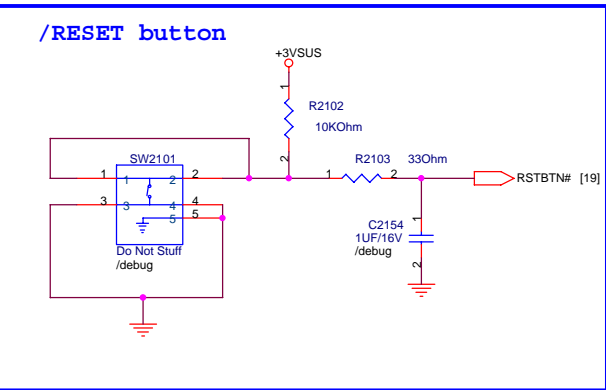


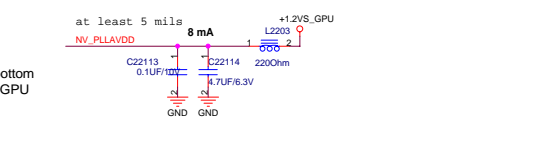
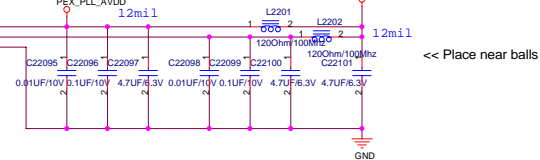
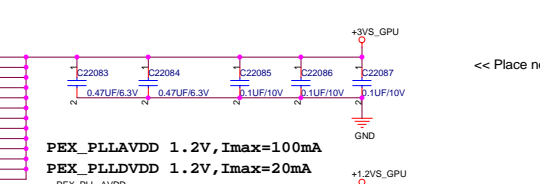
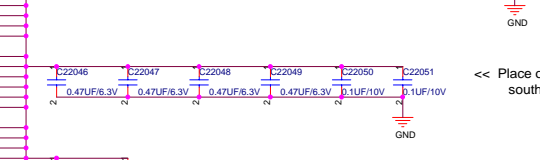
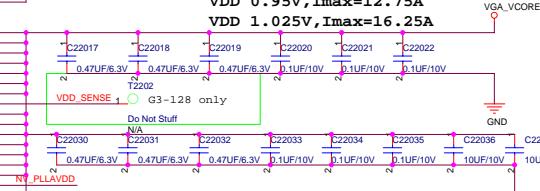
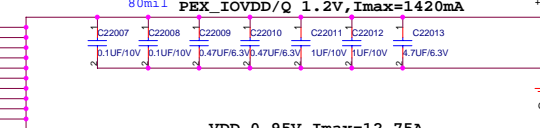
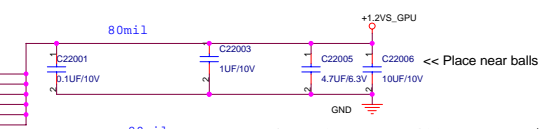
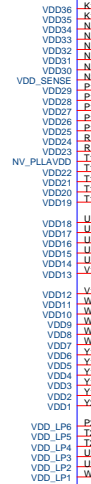
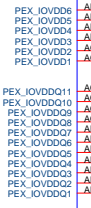
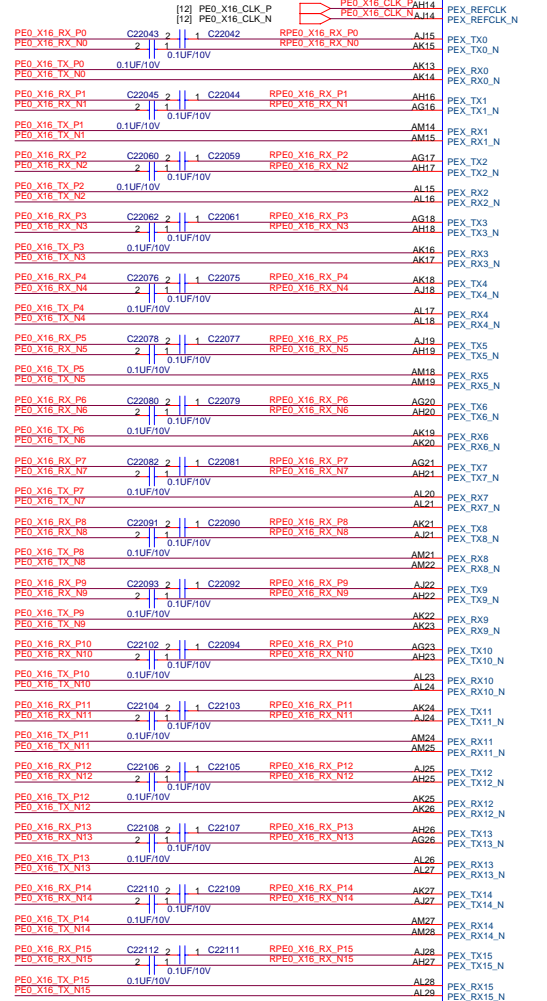
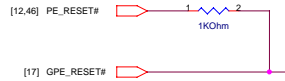
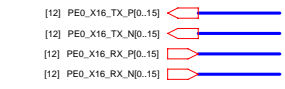
A6TcSKU1

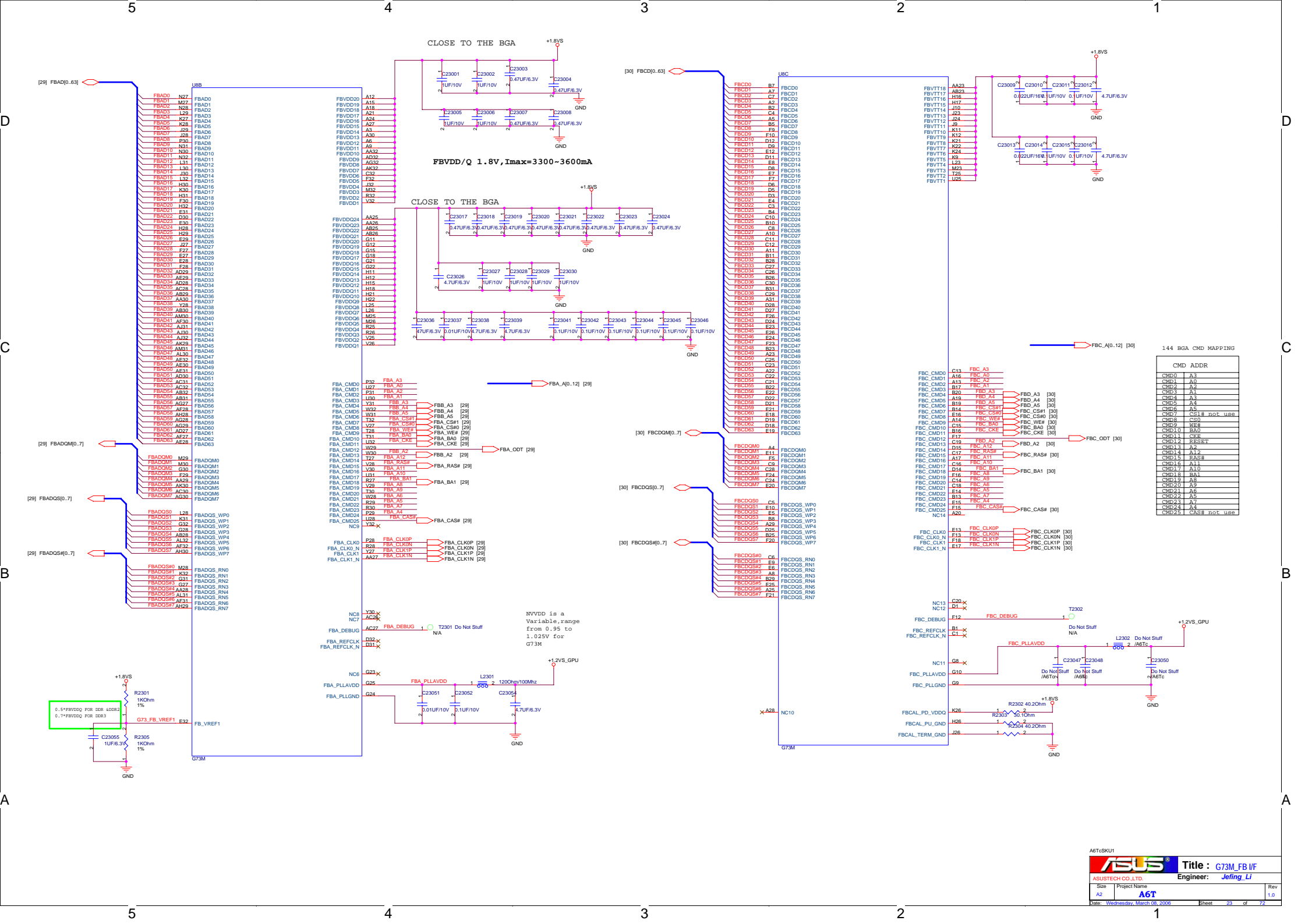
<b>ASUS</b>		Title : <b>MCP51_RGMII/XTAL</b>	
ASUSTECH CO.,LTD.		Engineer: <b>Jefing_Li</b>	
Size	Project Name		Rev
B	<b>A6T</b>		1.0
Date: <b>Wednesday, March 08, 2006</b>		Sheet	20 of 72



- 1.5V
- FOR SATA & MXM CONNECTOR
- 1.5V\_SP\_A @440MA
  - 1.5V\_SP\_D @164MA
  - 1.5V\_PLL\_SP\_DVDD @20MA
  - 1.5V\_PLL\_SP\_AVDD @160MA
  - 1.5V\_PLL\_CPU\_HT @71MA
  - 1.5V\_PLL\_SP\_SS @10MA
  - 1.5V\_PLL\_LEG @4MA
  - 1.5V\_PLL\_USB\_CORE @16MA

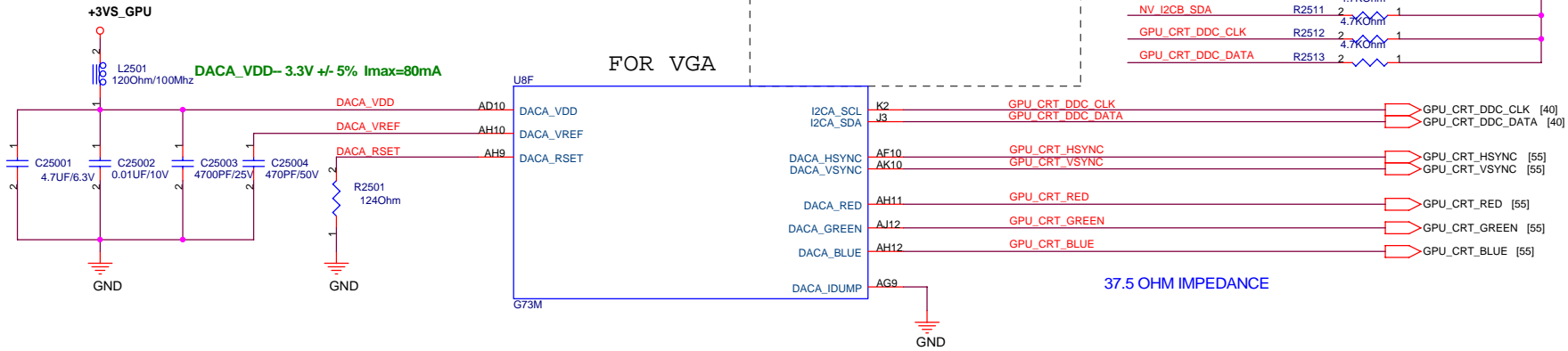




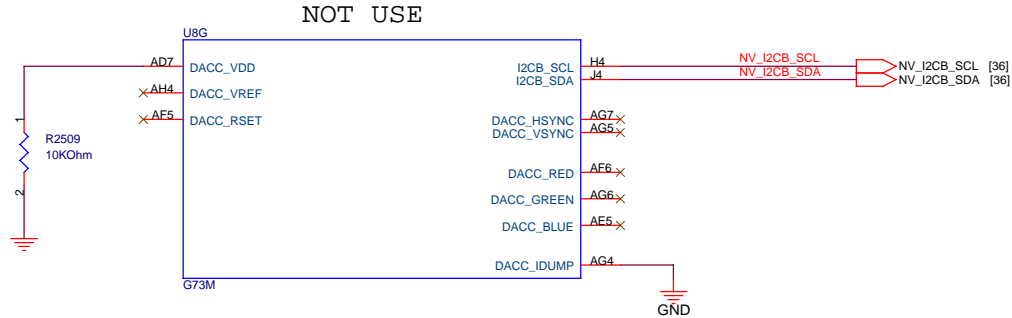
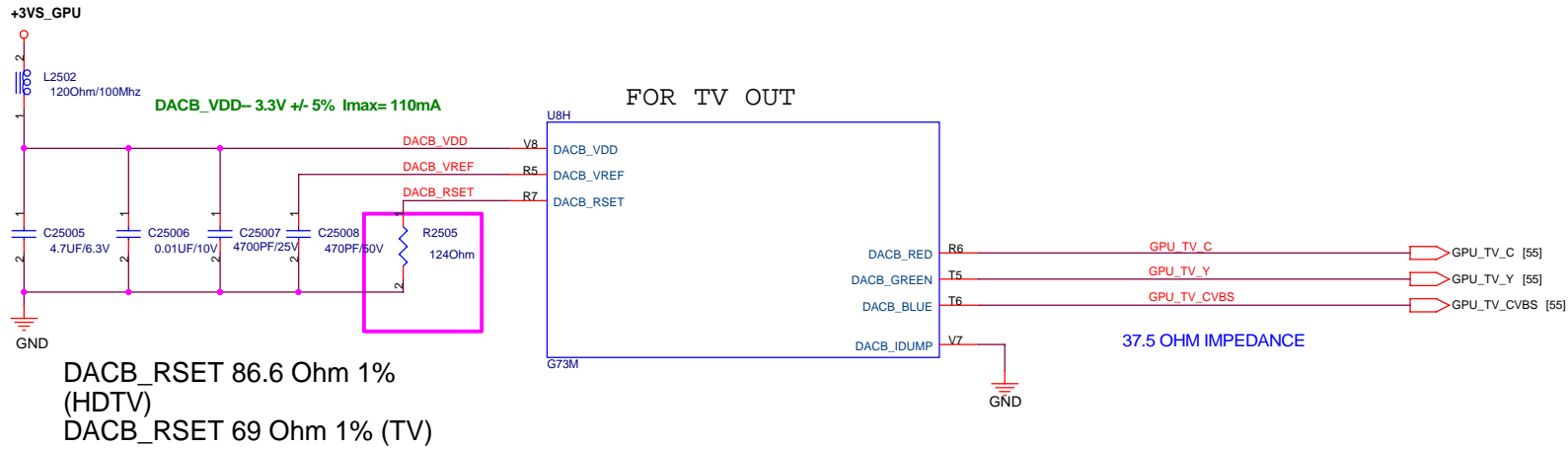




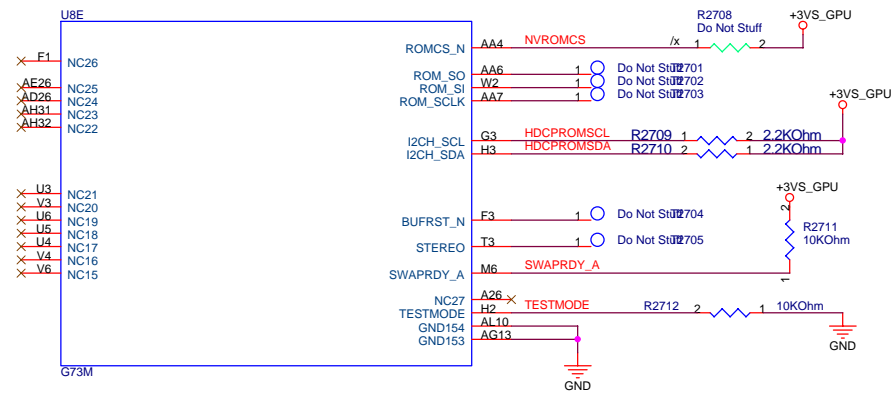
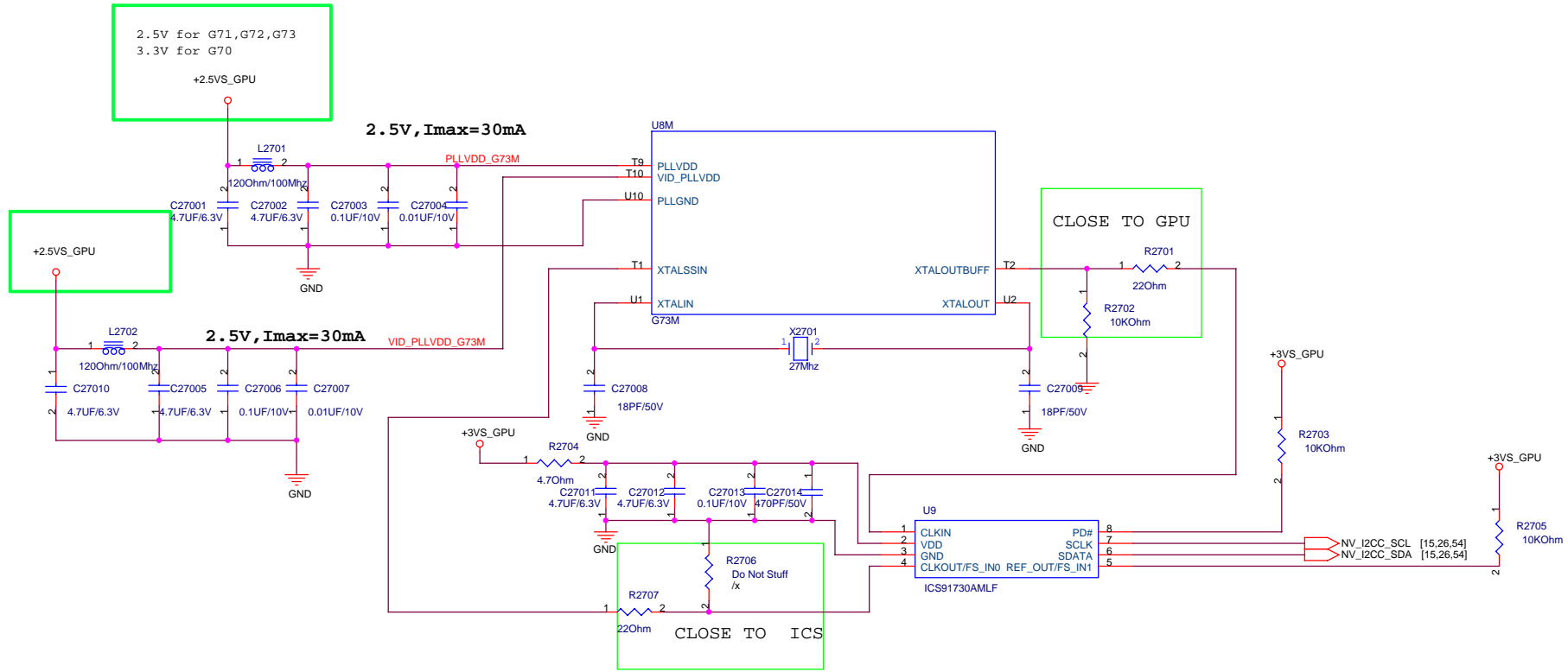




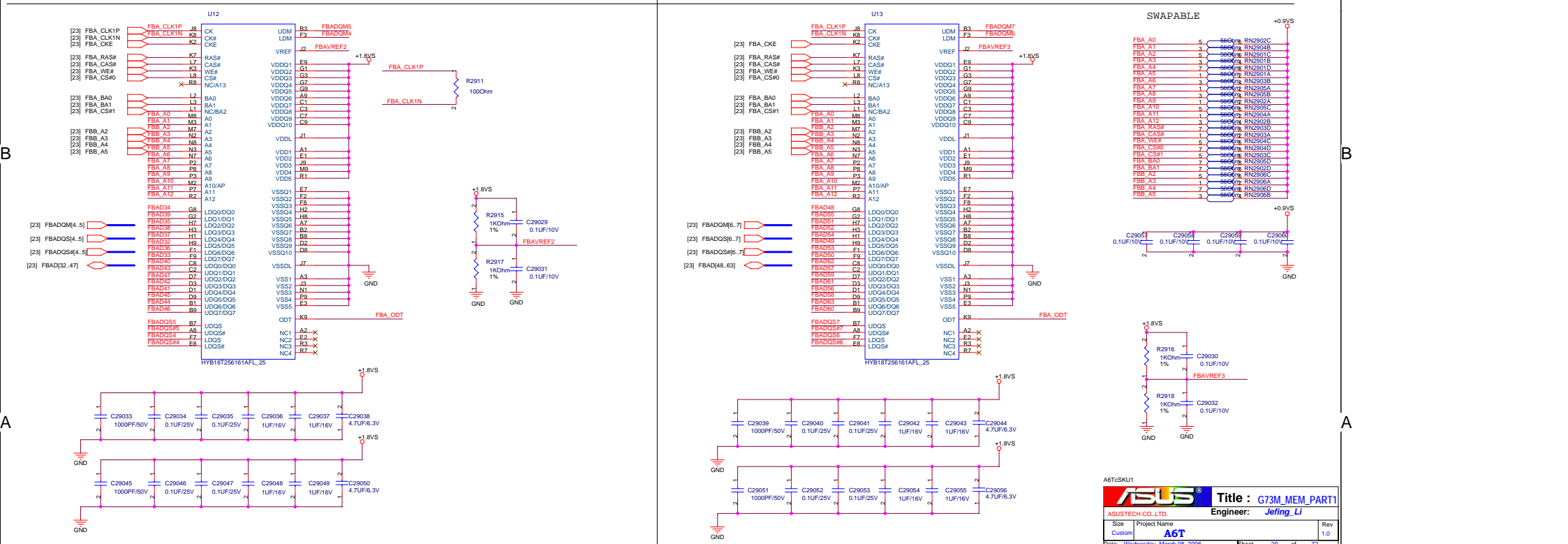
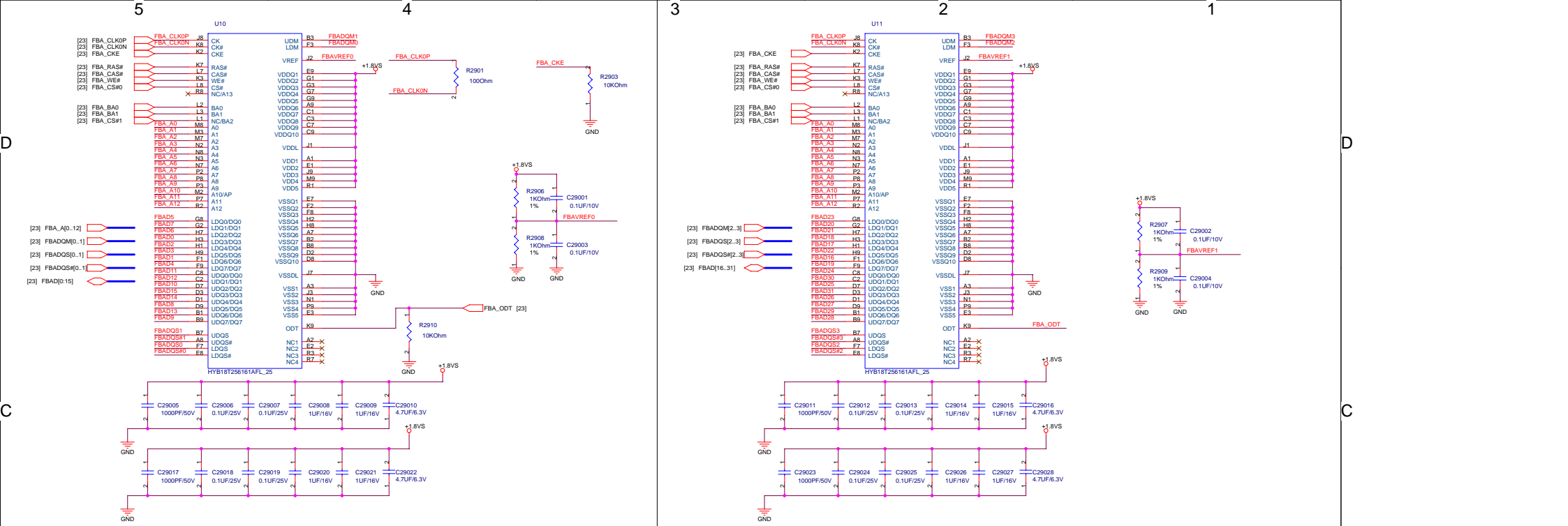
The I2C interface on the G7x devices is 5V tolerant; pull-ups may be connected to 5V directly.

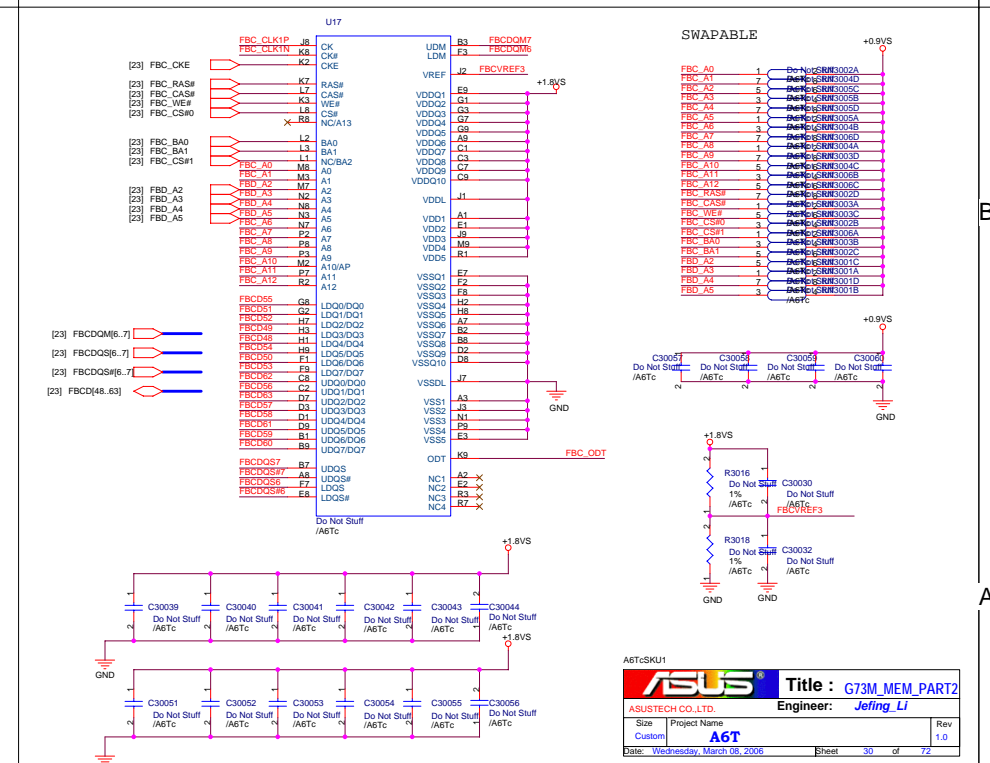
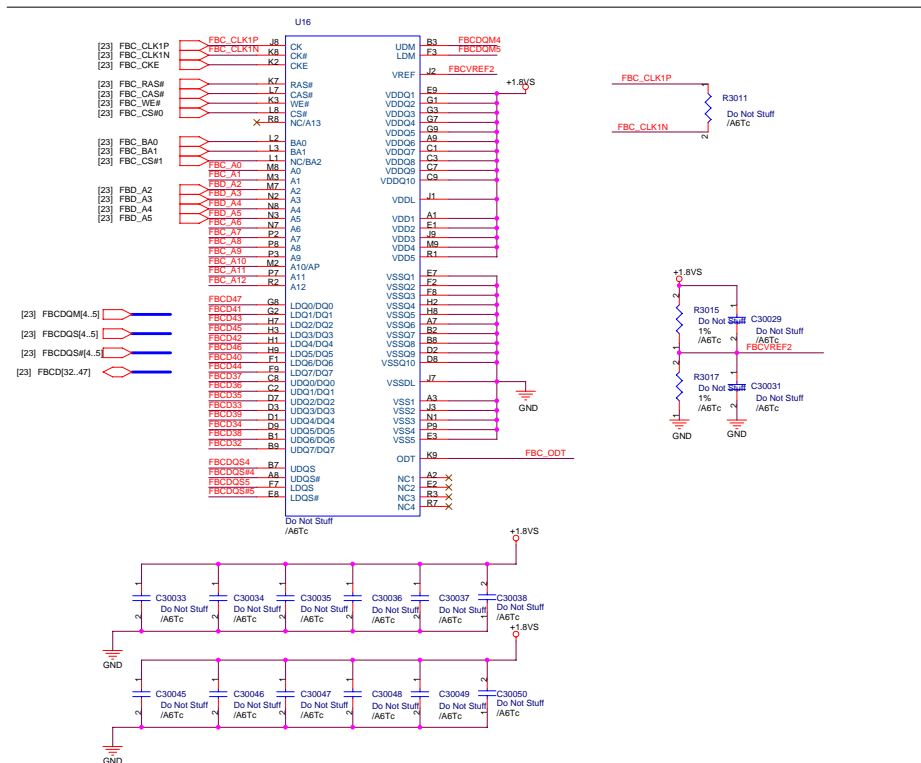
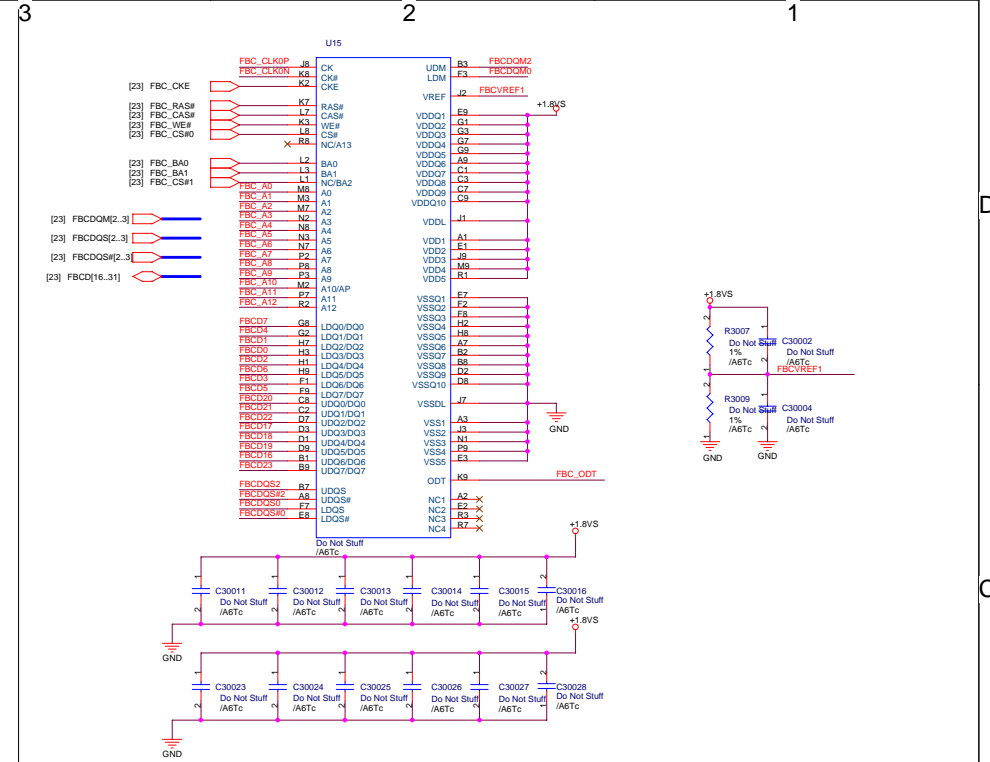
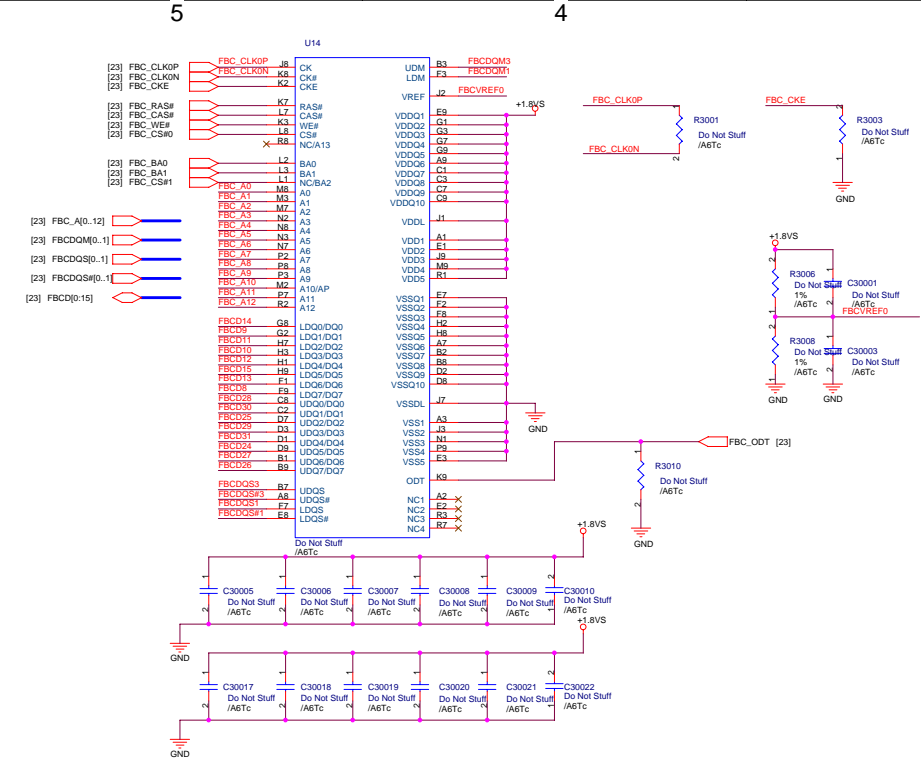


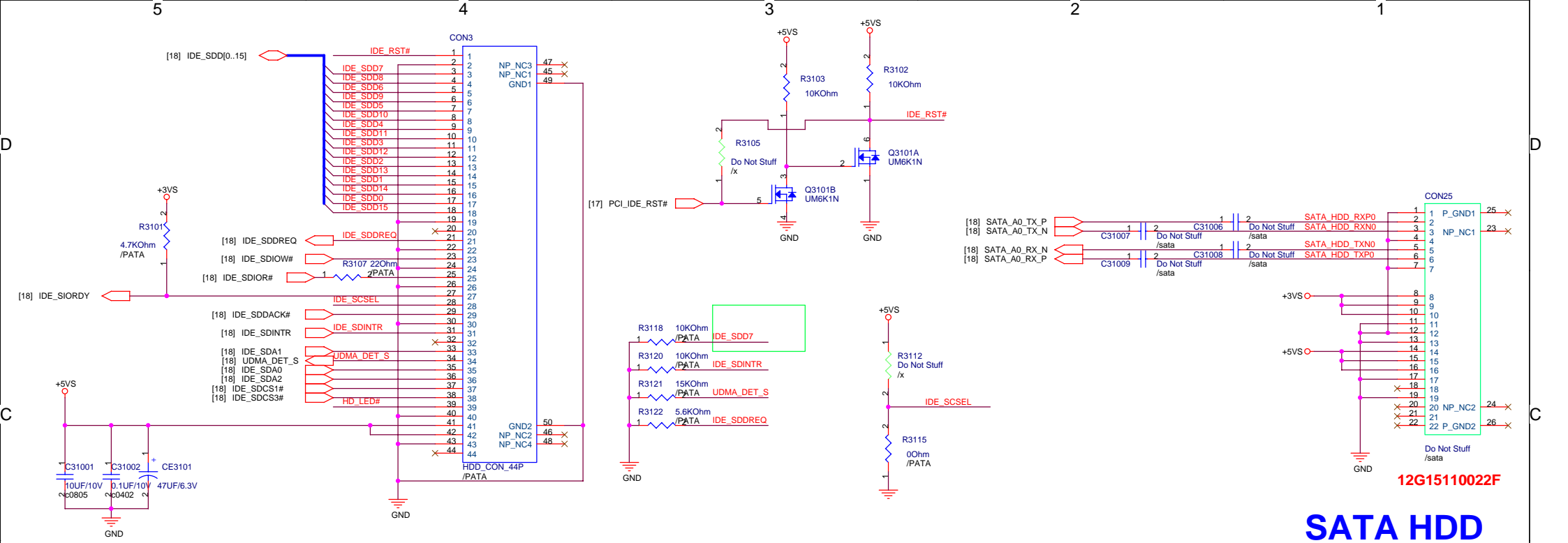






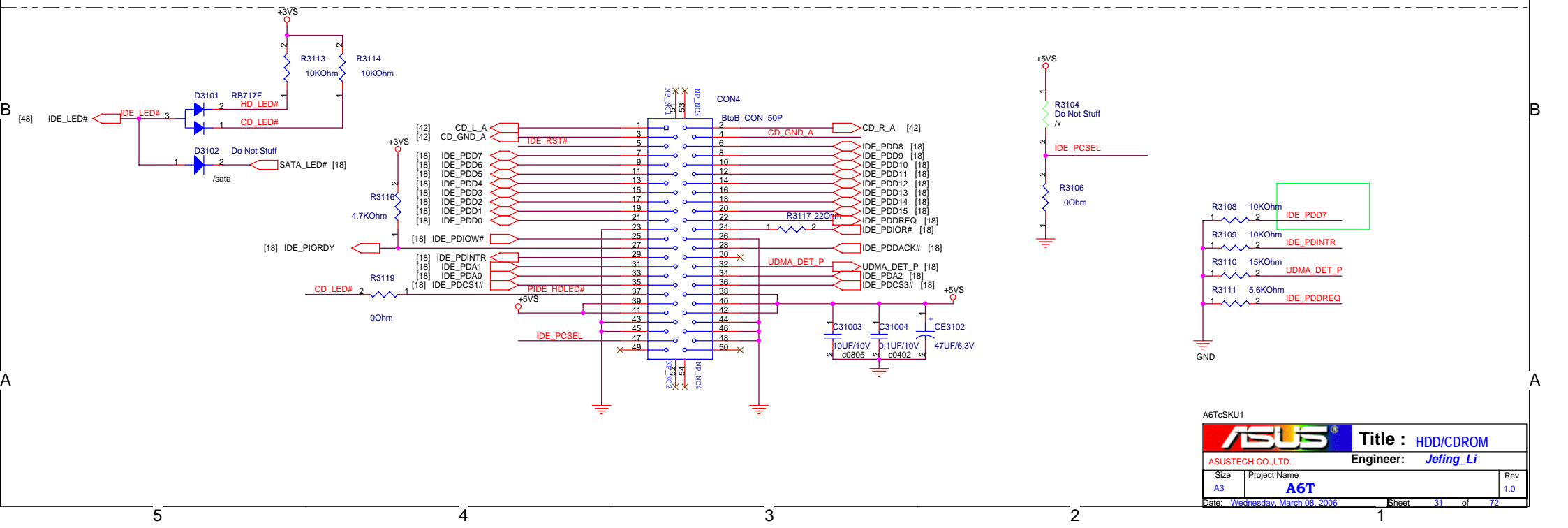






# SATA HDD

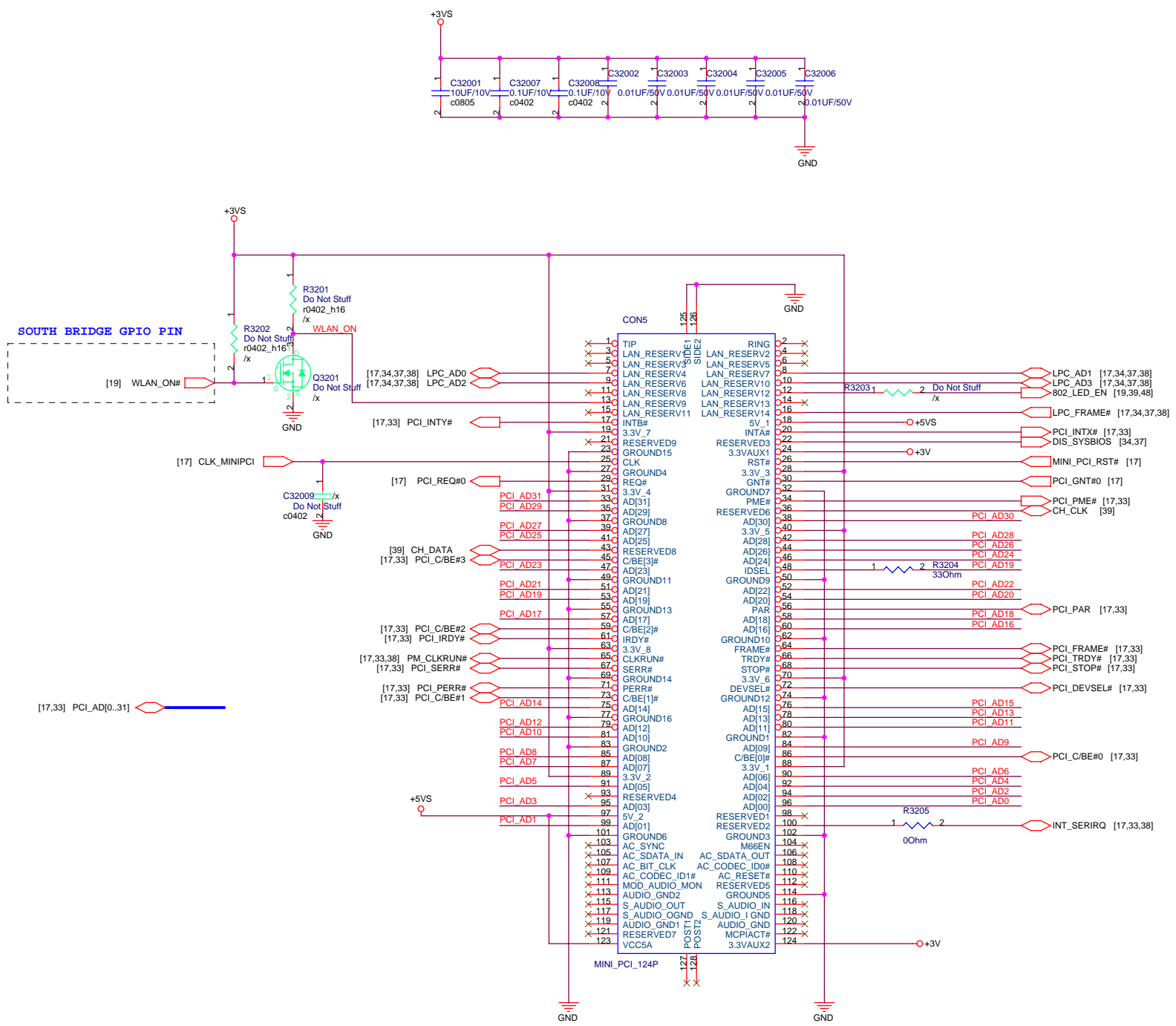
12G15110022F



A6TcSKU1

<b>ASUS</b>		Title : HDD/CDROM	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name	Rev	
A3	<b>A6T</b>	1.0	
Date: Wednesday, March 08, 2006	Sheet	31	of 72

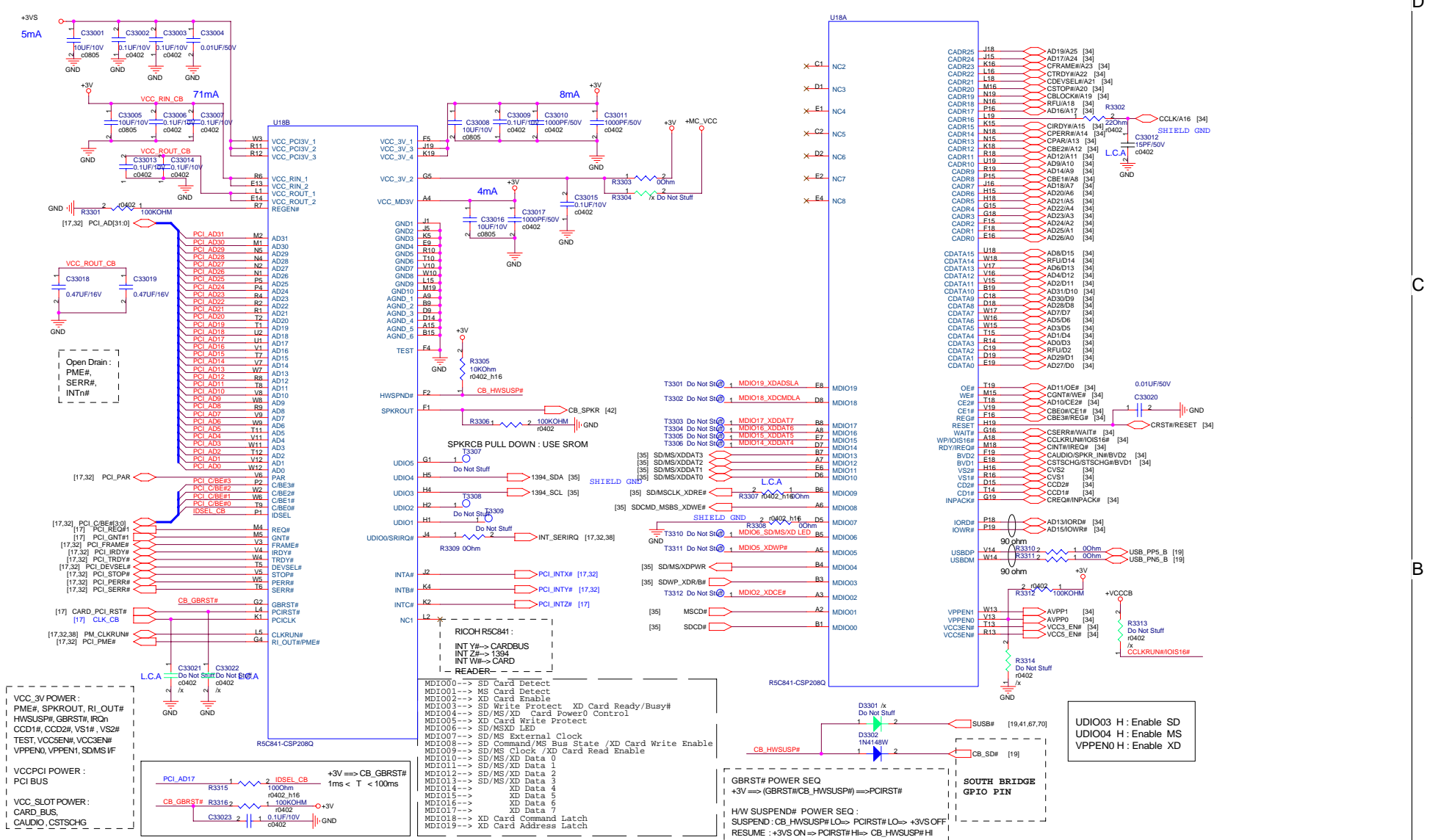
SOUTH BRIDGE GPIO PIN

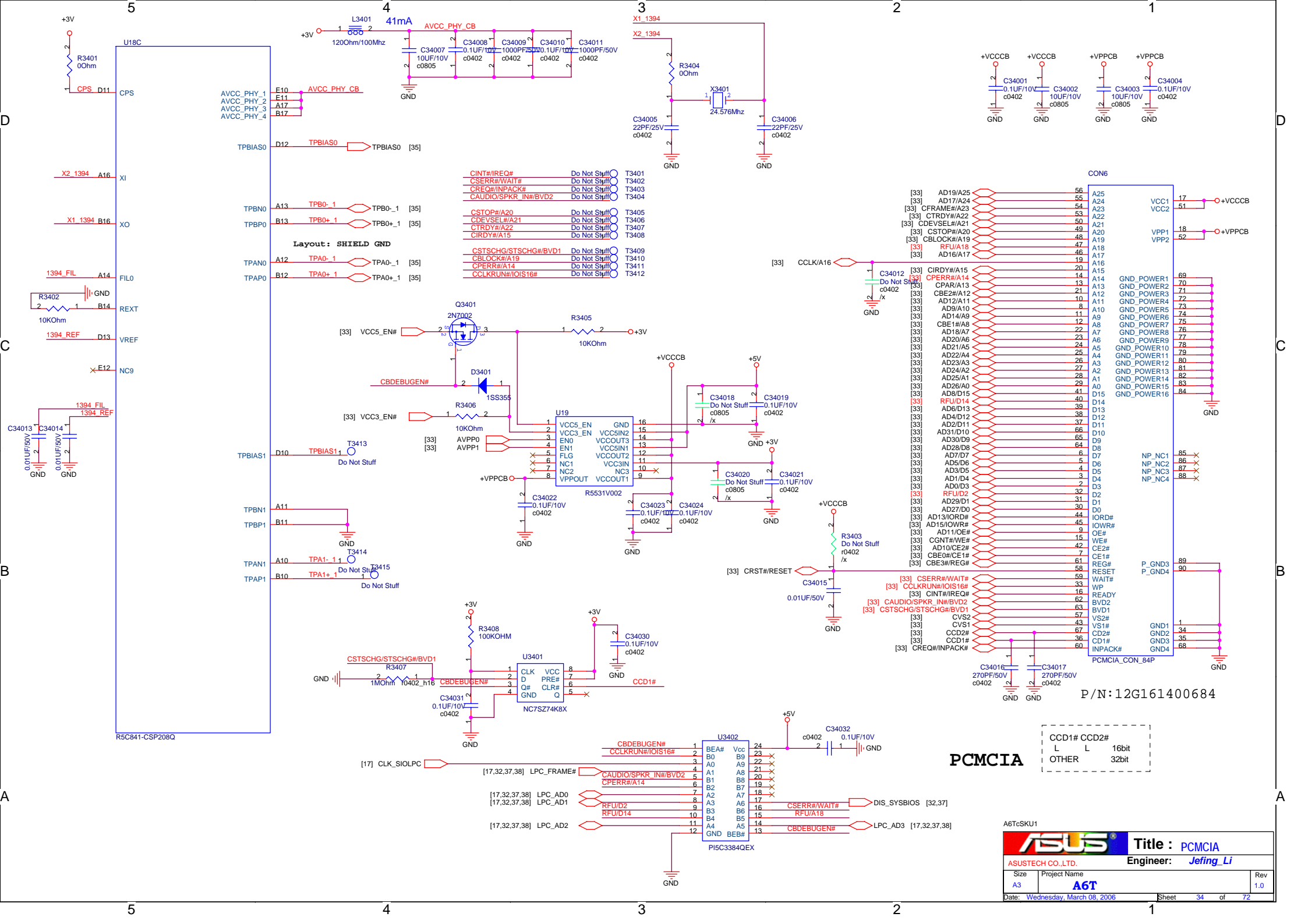


A6TcSKU1

<b>ASUS</b>		<b>Title : MINI PCI</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name	Rev	
A3	<b>A6T</b>	1.0	
Date: Wednesday, March 08, 2006		Sheet	32 of 72



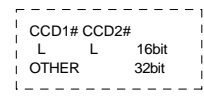


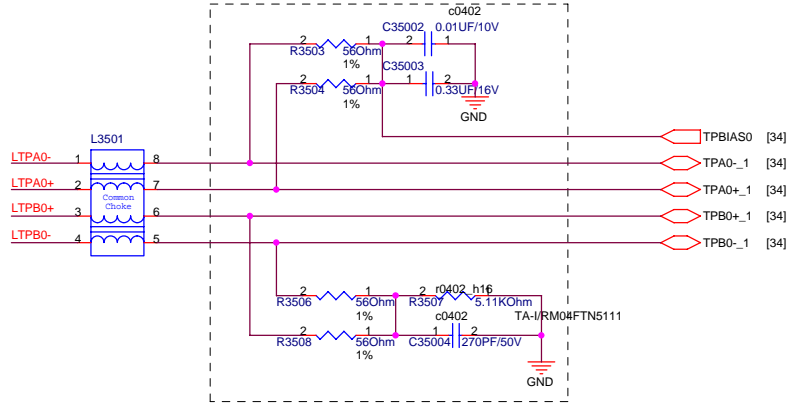
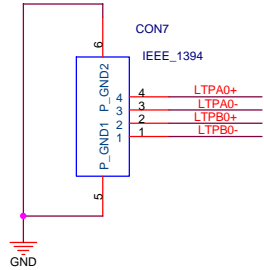


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- CSERR#/WAIT# Do Not Stuff T3402
- CREQ#/INPACK# Do Not Stuff T3403
- CAUDIO#/SPKR\_IN#/BVD2 Do Not Stuff T3404
- CSTOP#/A20 Do Not Stuff T3405
- CDESEL#/A21 Do Not Stuff T3406
- CTRDY#/A22 Do Not Stuff T3407
- CIRDY#/A15 Do Not Stuff T3408
- CSTSCHG#/STSCHG#/BVD1 Do Not Stuff T3409
- CSLOCK#/A19 Do Not Stuff T3410
- CPERR#/A14 Do Not Stuff T3411
- CCLKRUN#/IOIS16# Do Not Stuff T3412

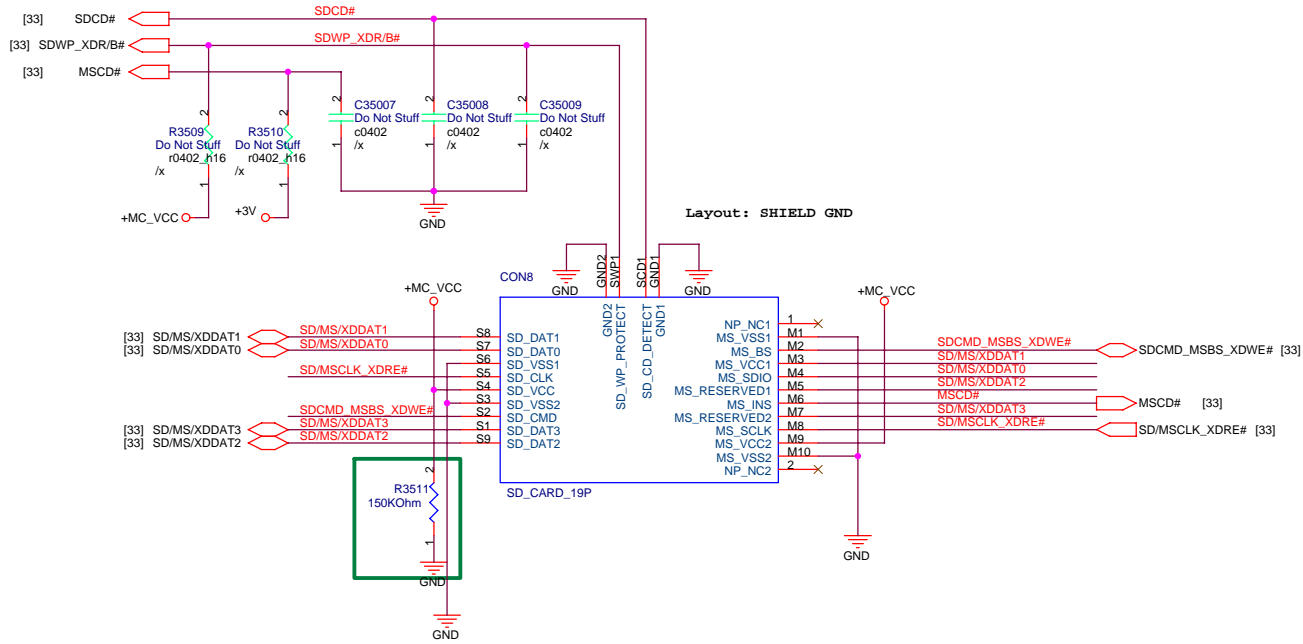
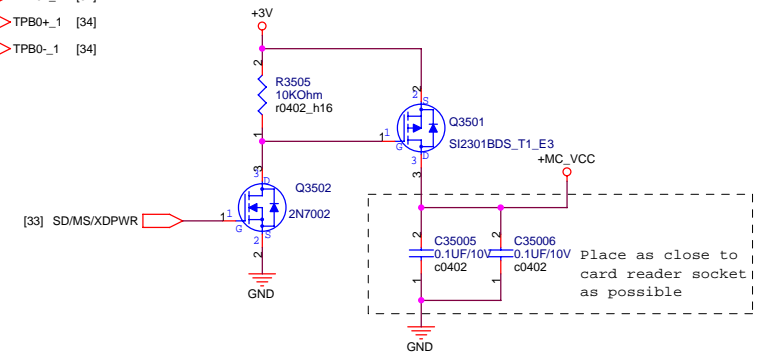
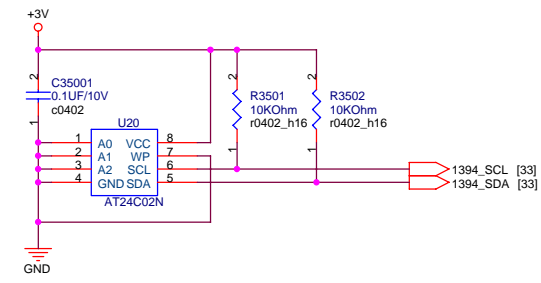
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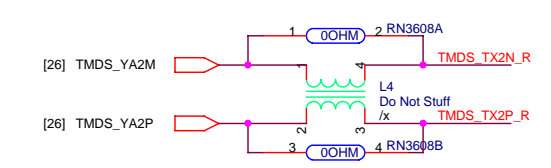
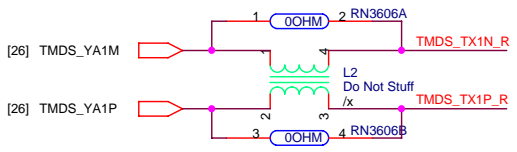
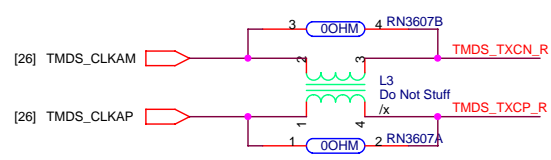
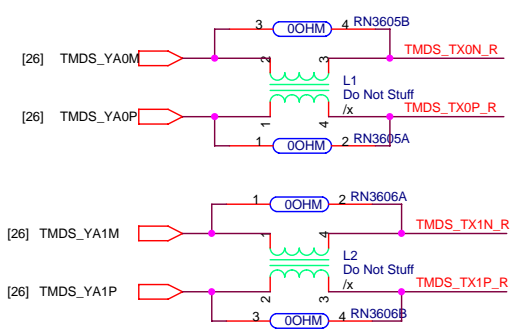
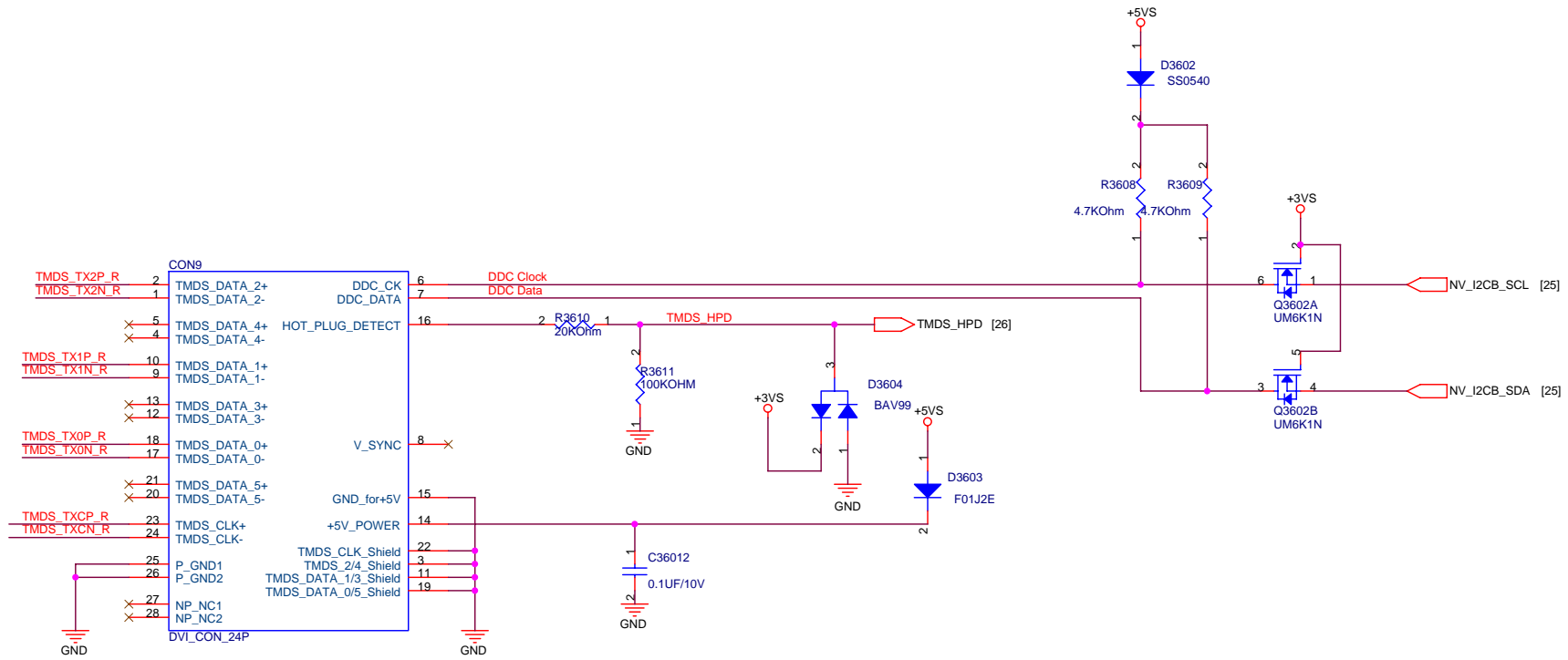
**PCMCIA**





1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend , maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

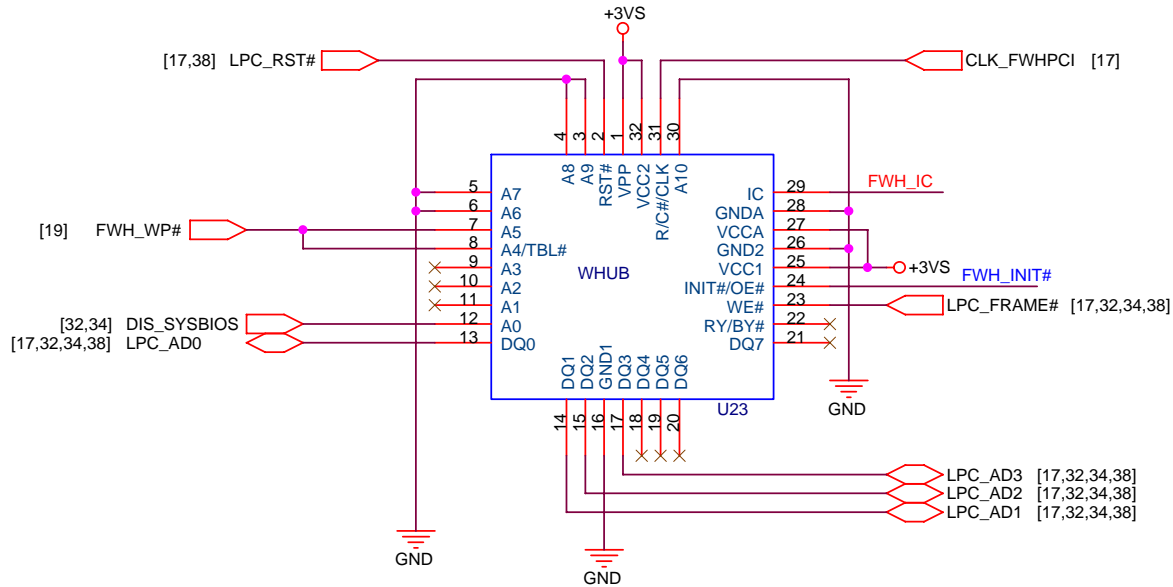




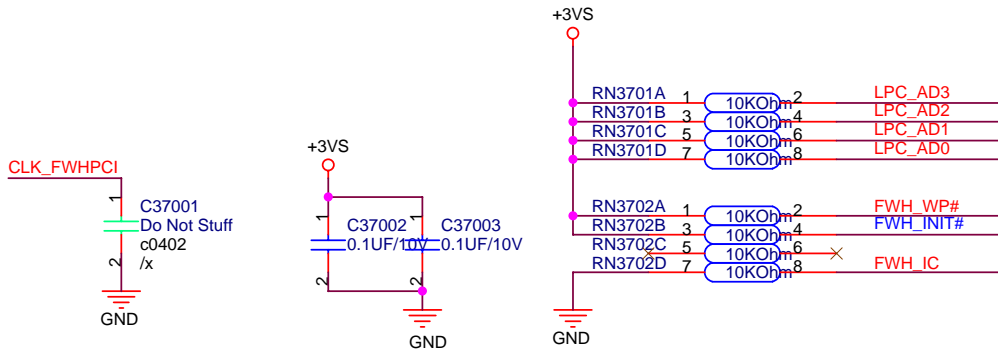
A6TcSKU1

<b>ASUS</b>		<b>Title : SIO/SIR/DVI</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size B	Project Name <b>A6T</b>	Rev 1.0	
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# FWH

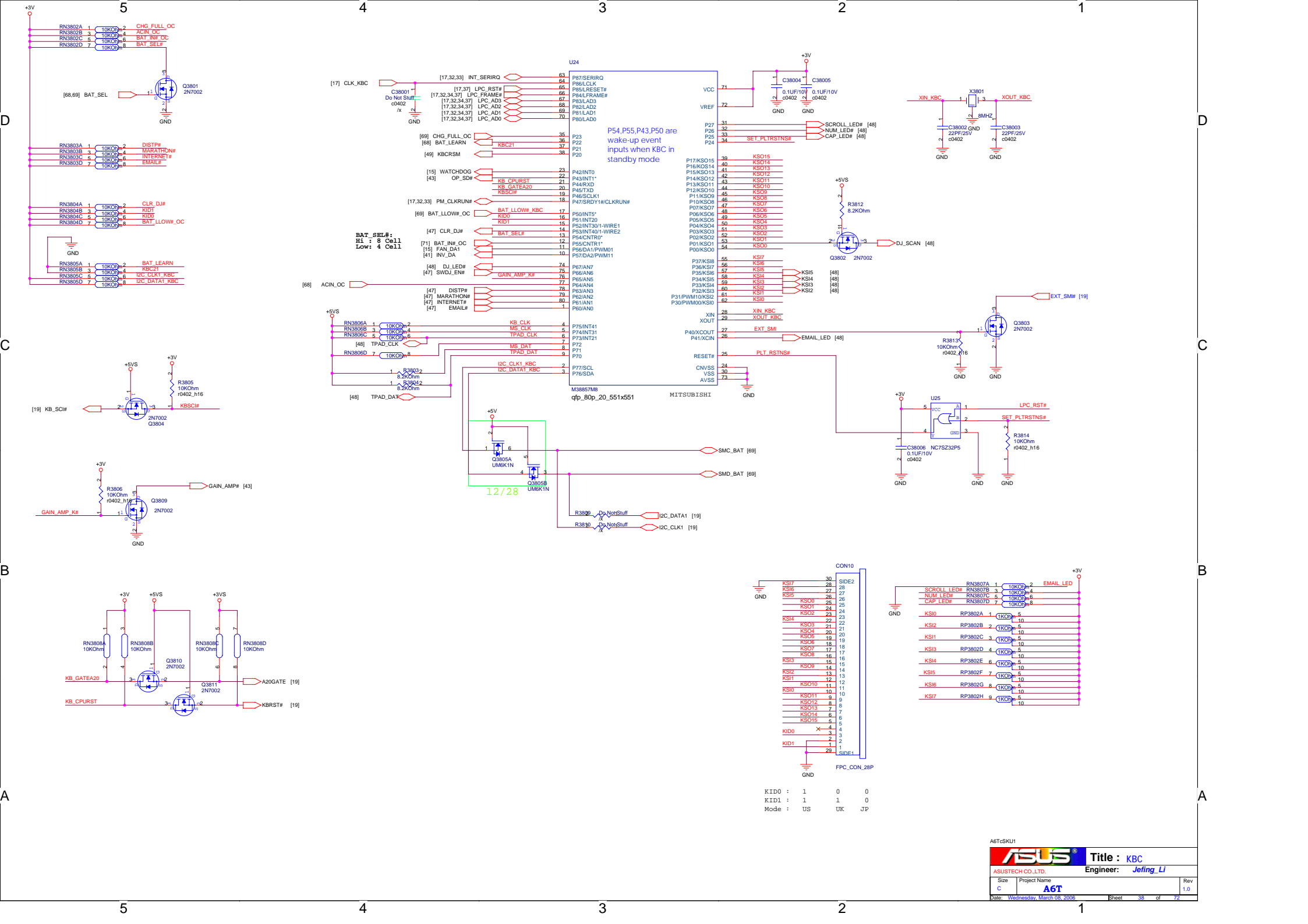


PLCC32 Socket Part Number : 12-043000323  
 SST FWH/LPC Part Number :  
 05G00101712L(燒)



A6TcSKU1

		<b>Title :</b> FWH
ASUSTECH CO.,LTD.		<b>Engineer:</b> Jefing_Li
Size A4	Project Name <b>A6T</b>	Rev 1.0
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P54, P55, P43, P50 are wake-up event inputs when KBC in standby mode

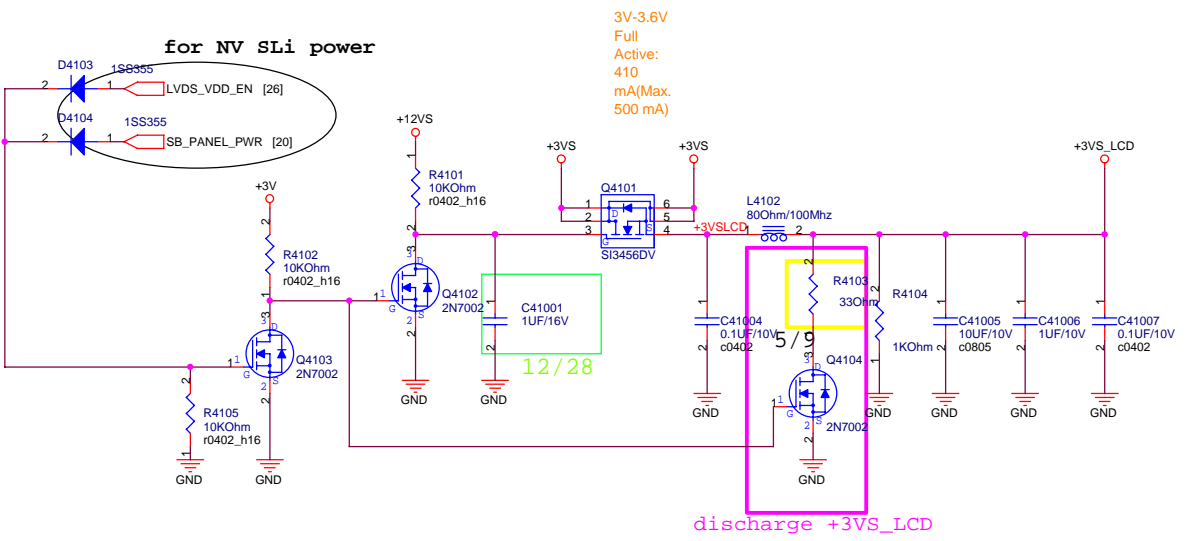
KID0 : 1 0 0  
 KID1 : 1 1 0  
 Mode : US UK JP



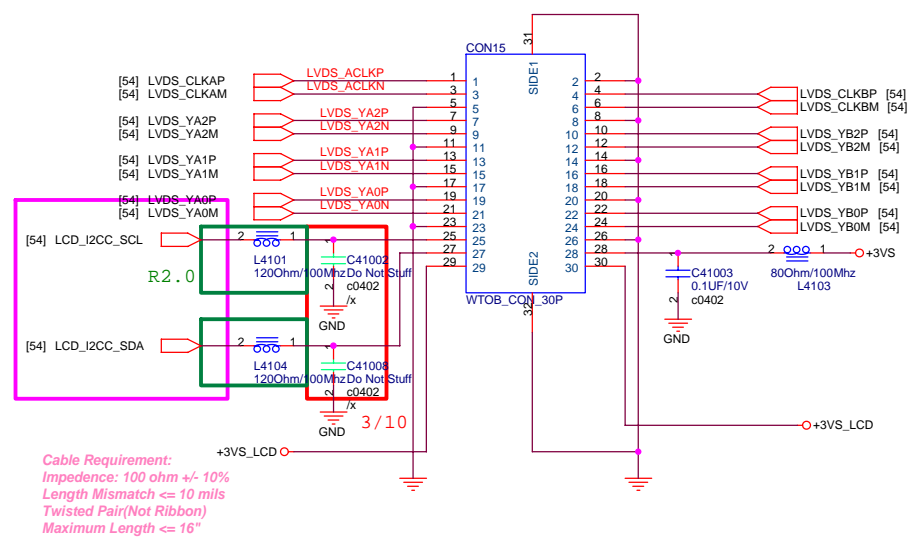




# LCD Power

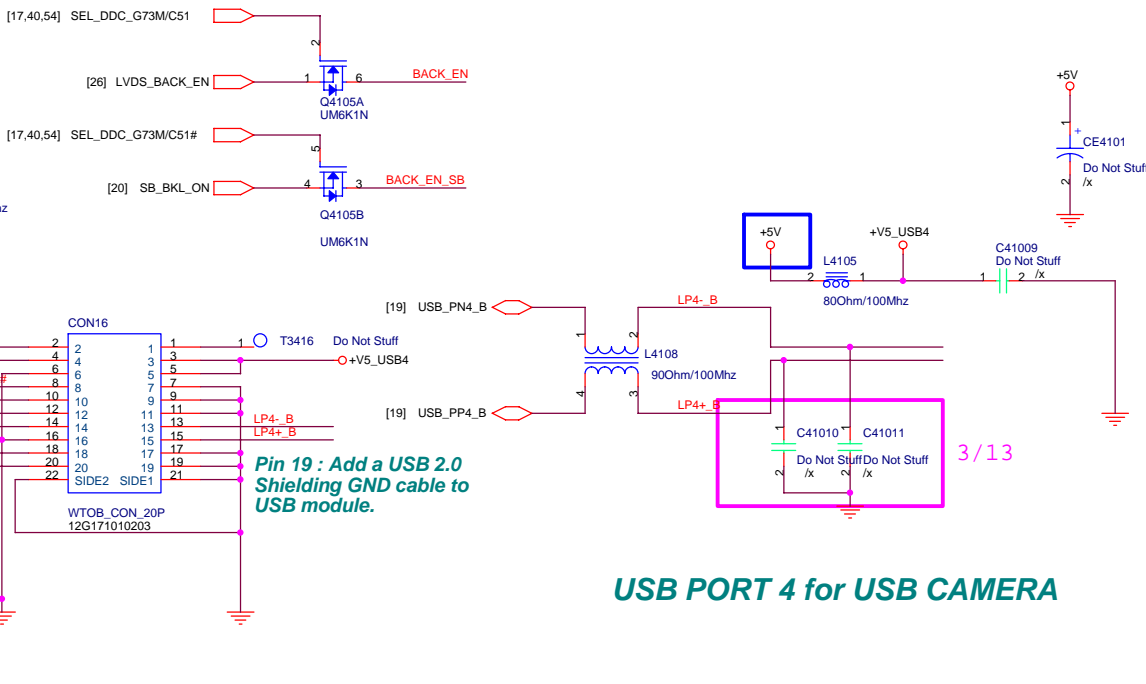
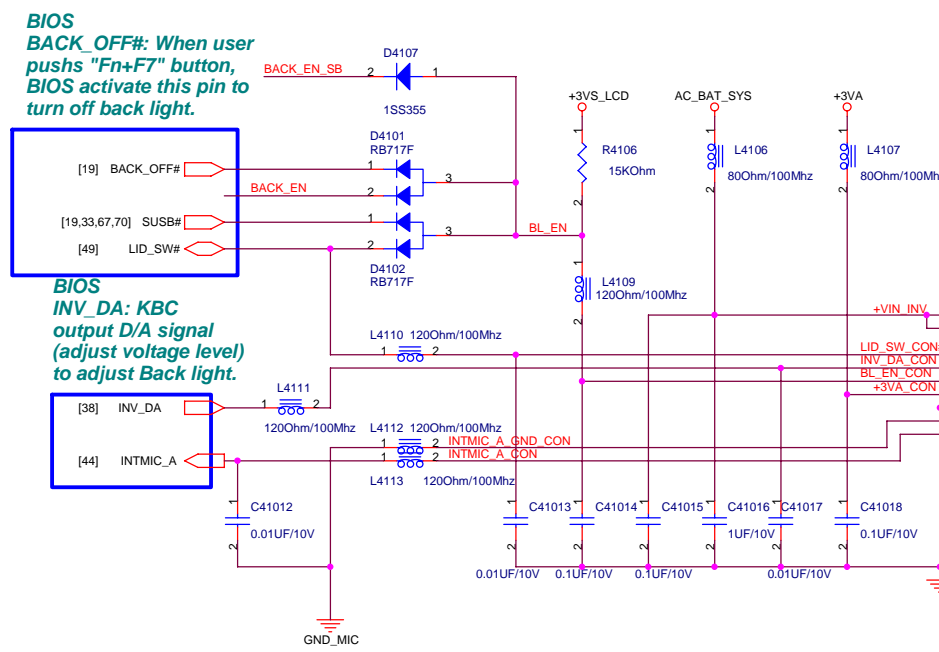


# LCD LVDS Interface

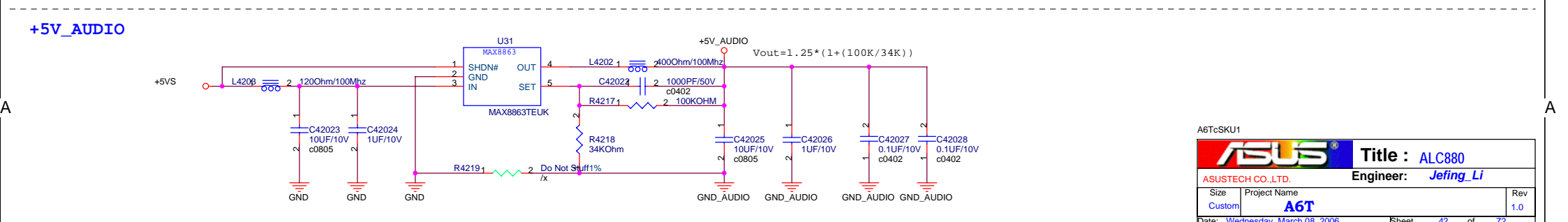
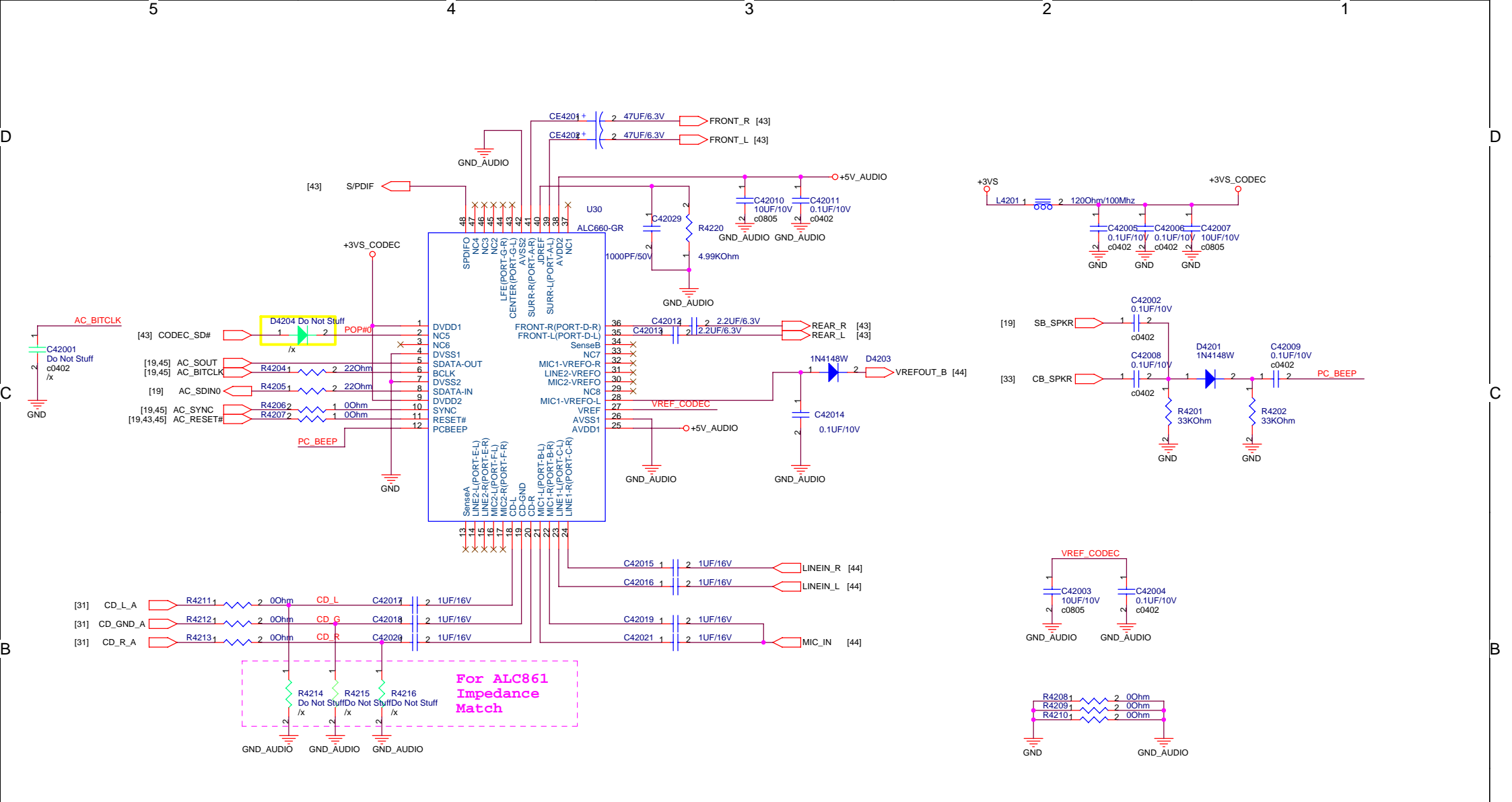


for NV SLi power

# INVERTER Interface

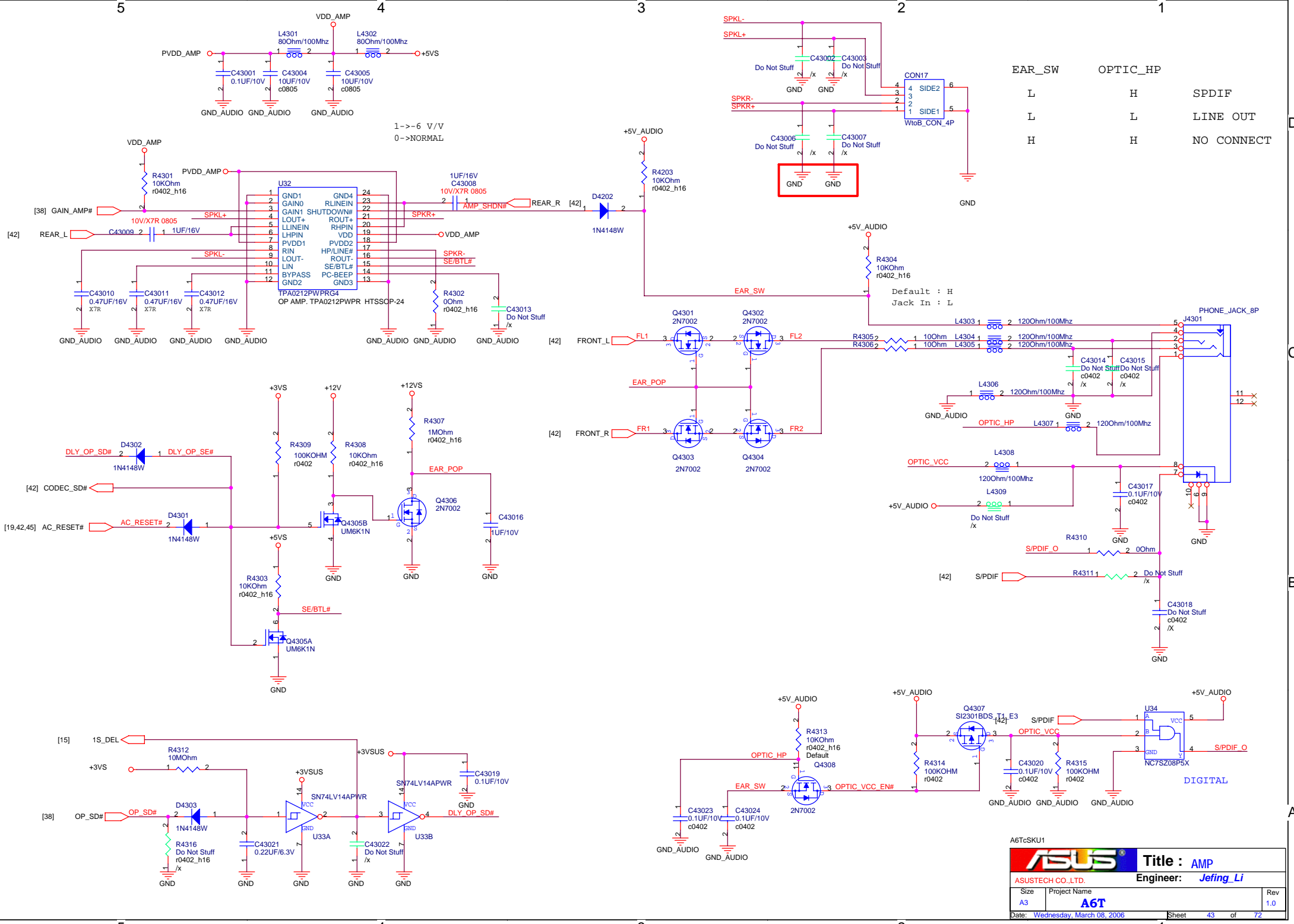


USB PORT 4 for USB CAMERA

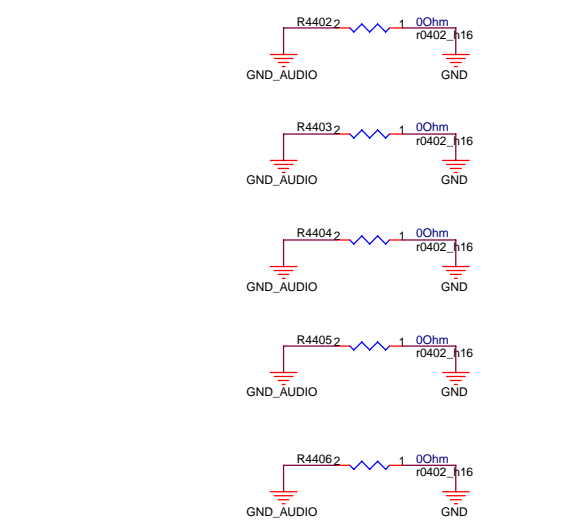
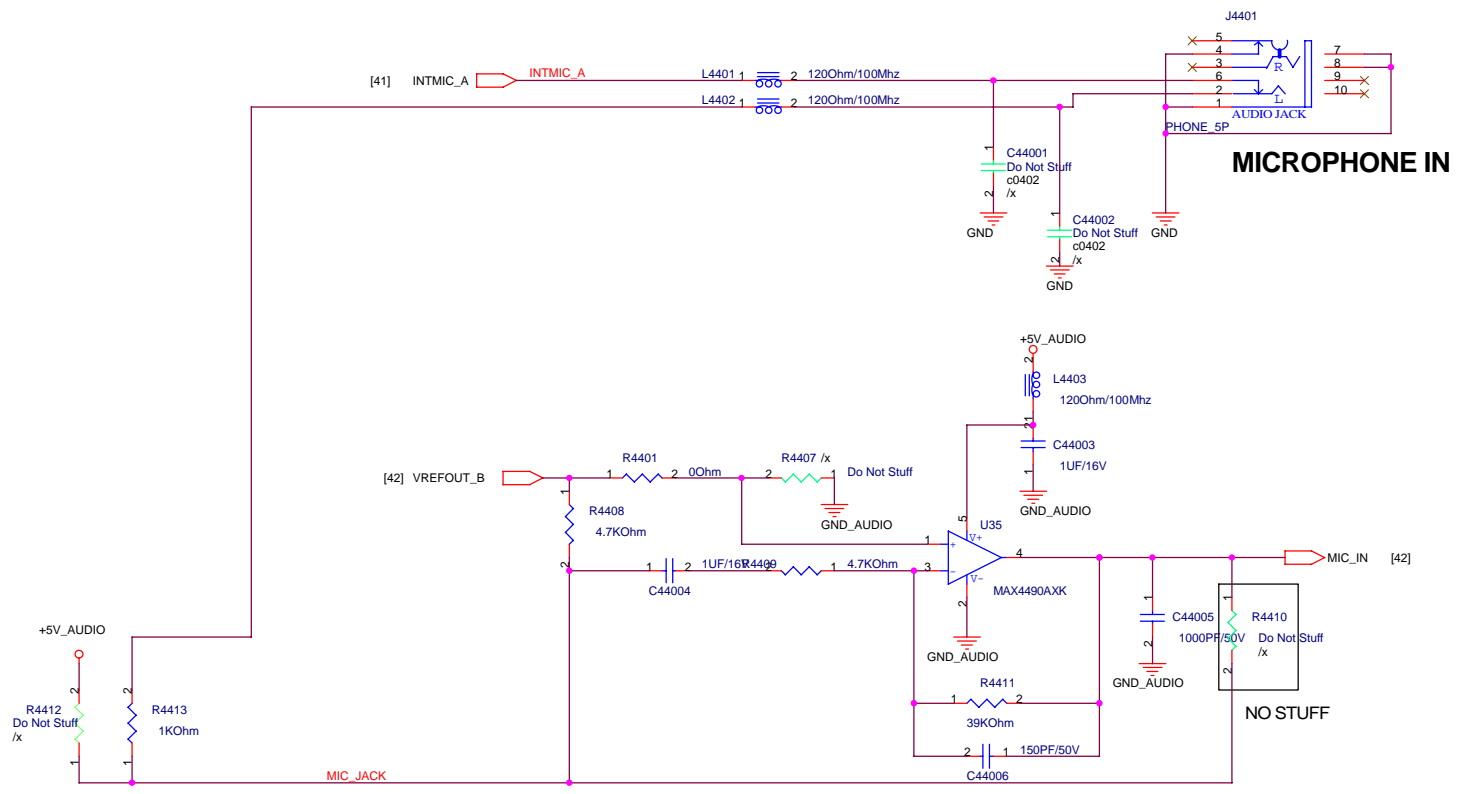


A6TcSKU1

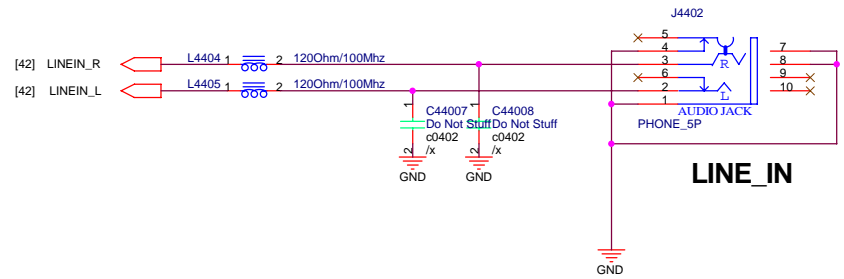
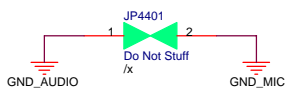
<b>ASUS</b>		<b>Title : ALC880</b>	
ASUSTECH CO.,LTD.		Engineer: <b>Jefing_Li</b>	
Size	Project Name		Rev
Custom	<b>A6T</b>		1.0
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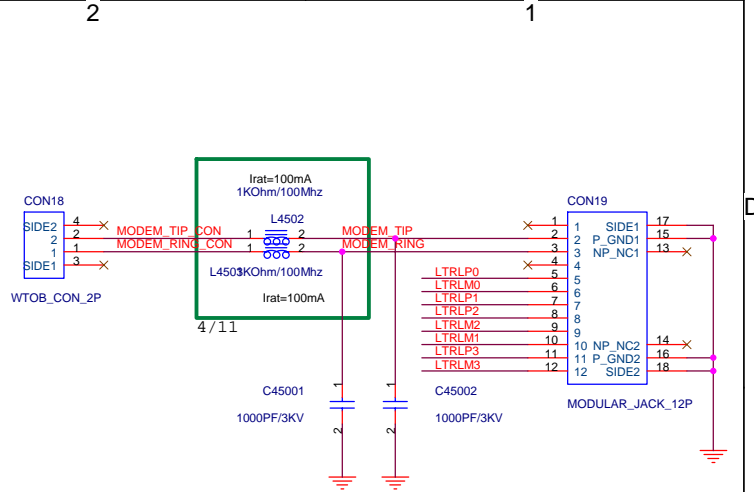
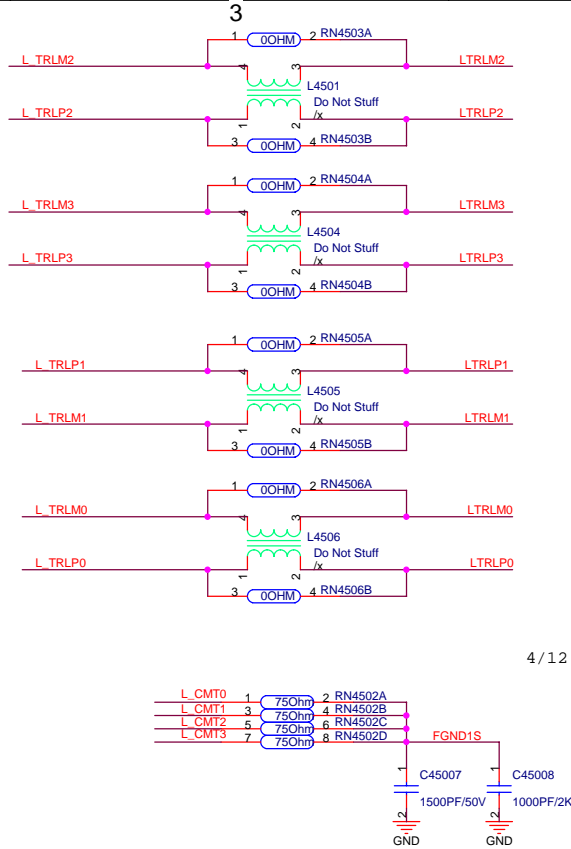
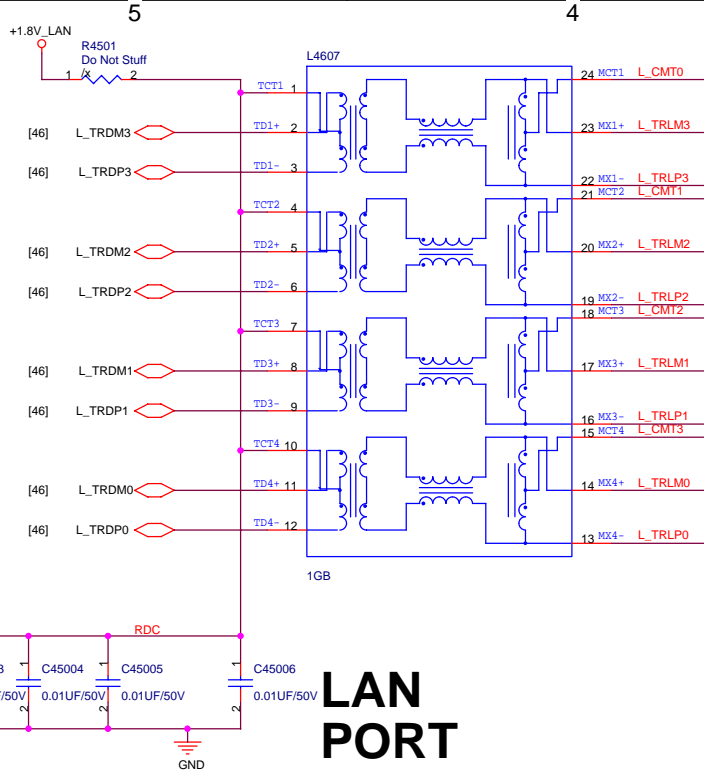


EAR_SW	OPTIC_HP	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT

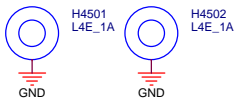
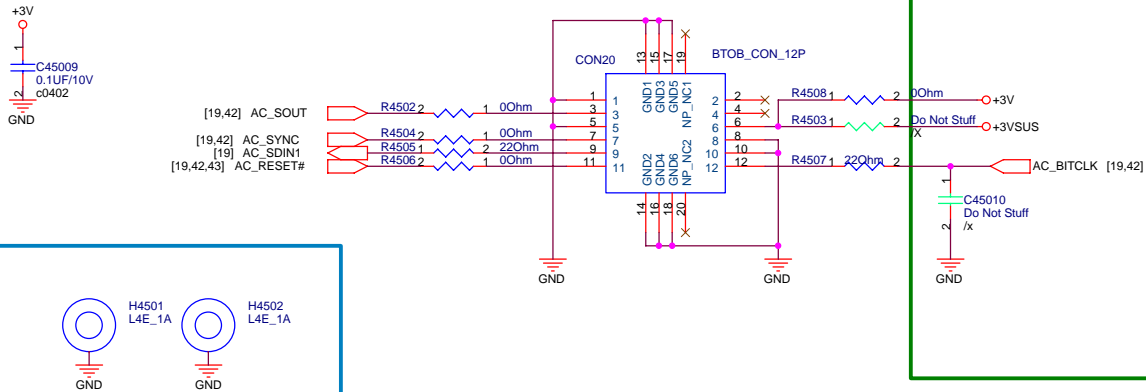


**INTMIC\_A:GND\_AUDIO**  
: W/P/X = 12/5/15mils

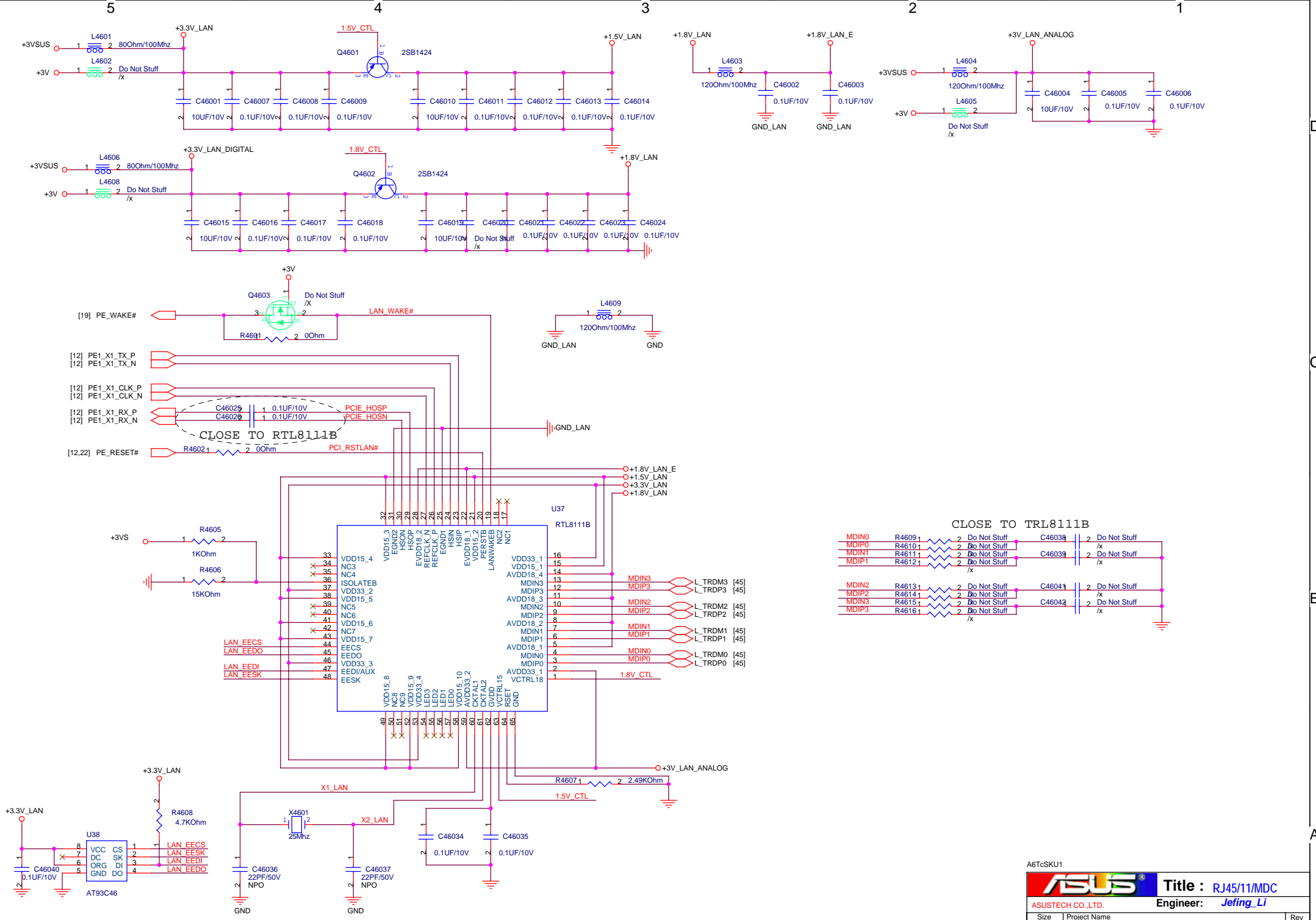




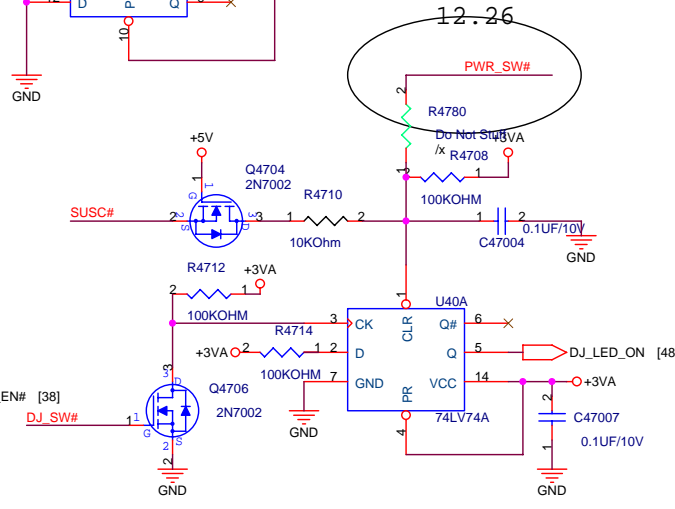
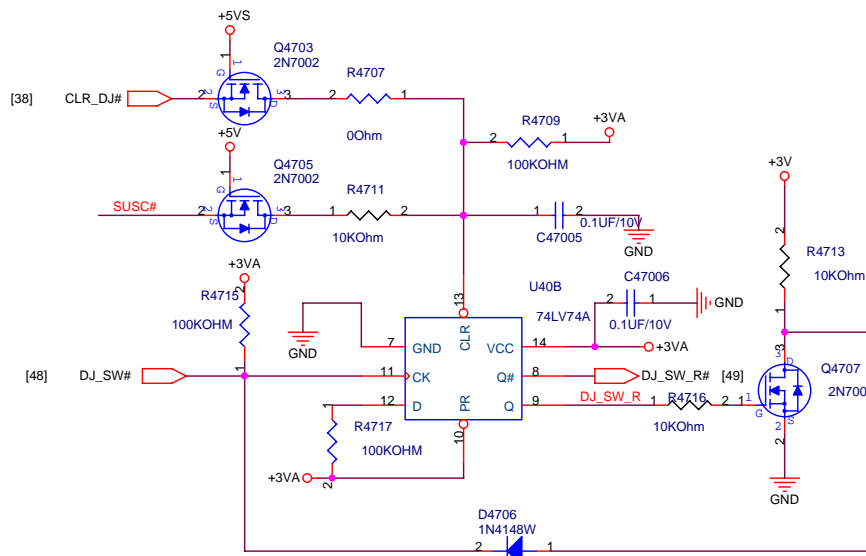
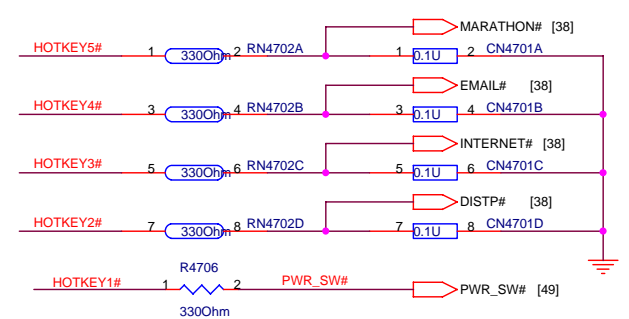
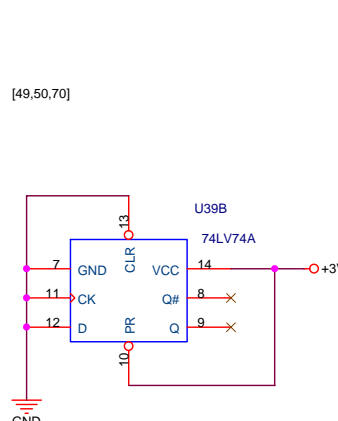
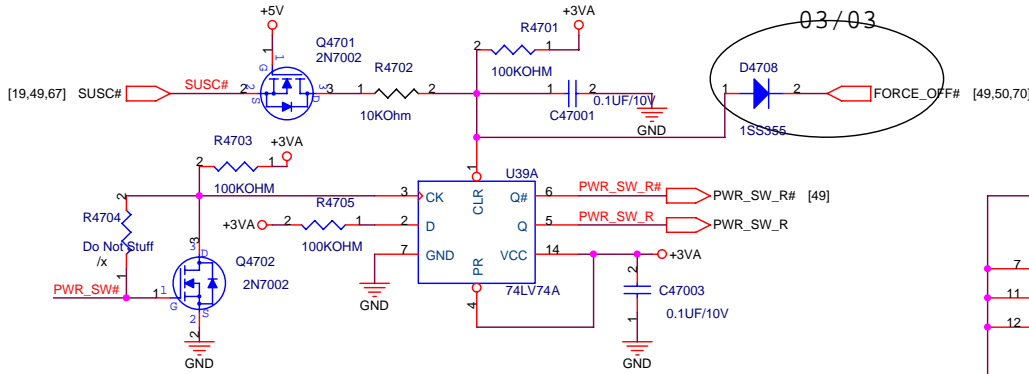
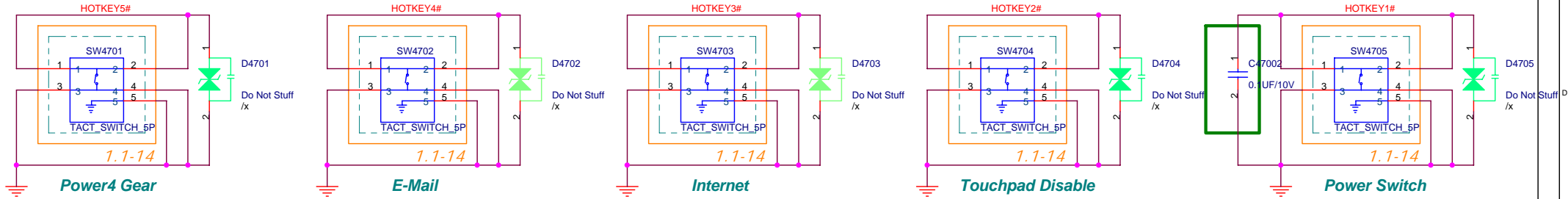
**MDC**



**Must change to 13-N7510M270**

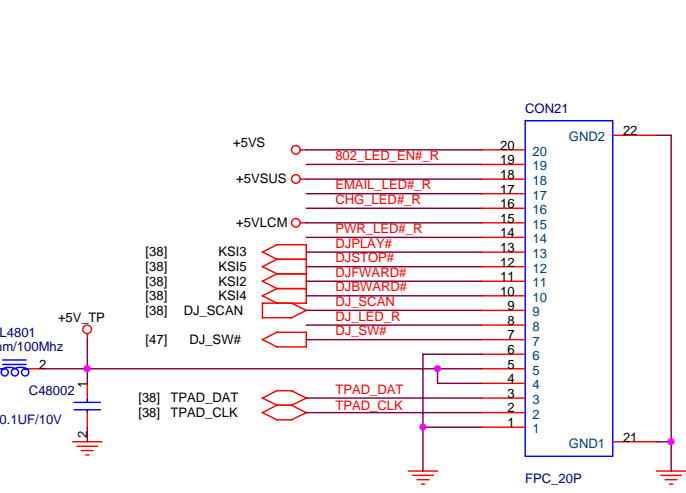
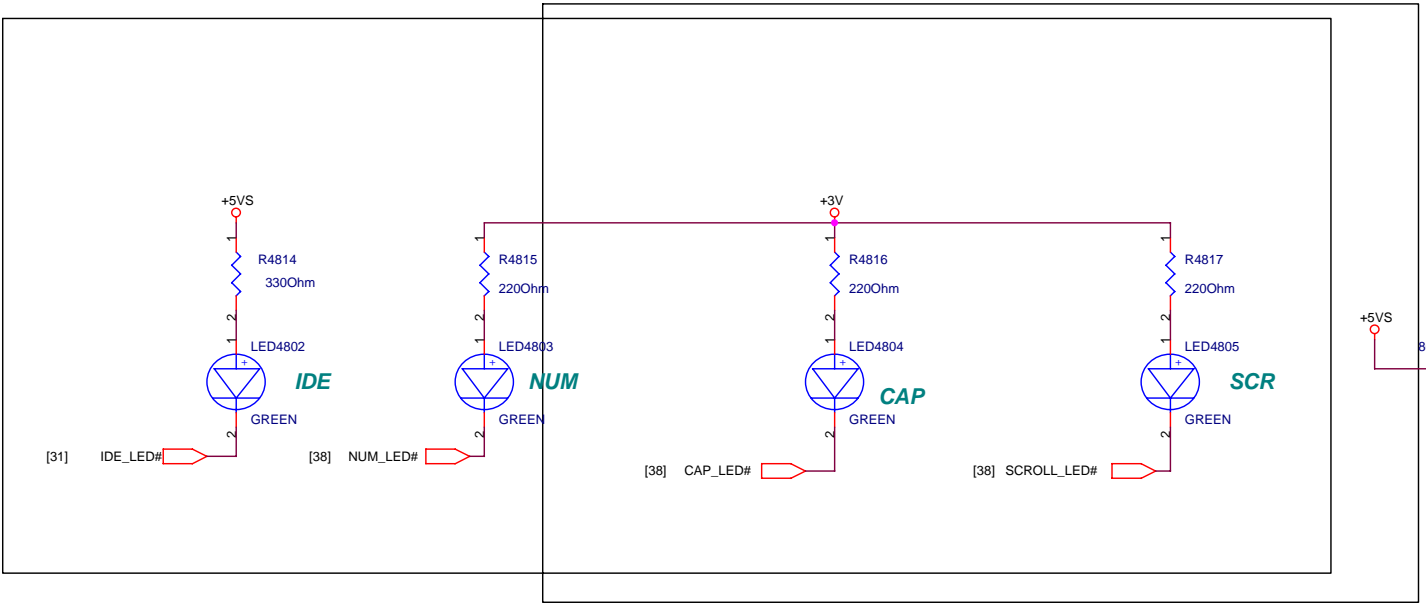
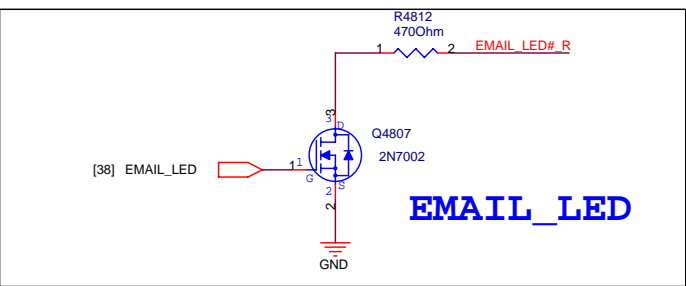
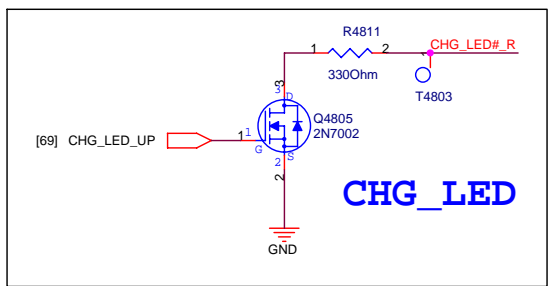
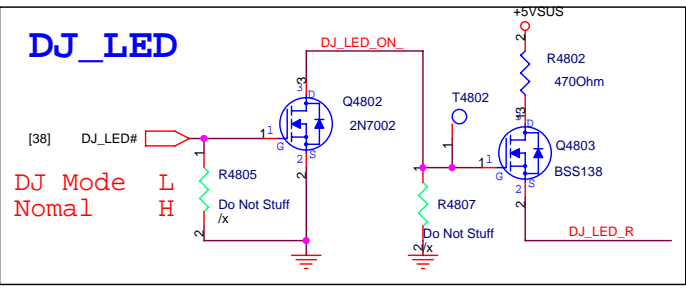
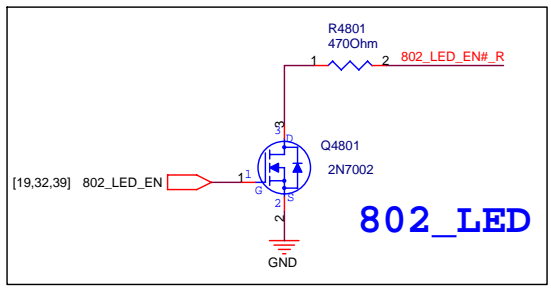
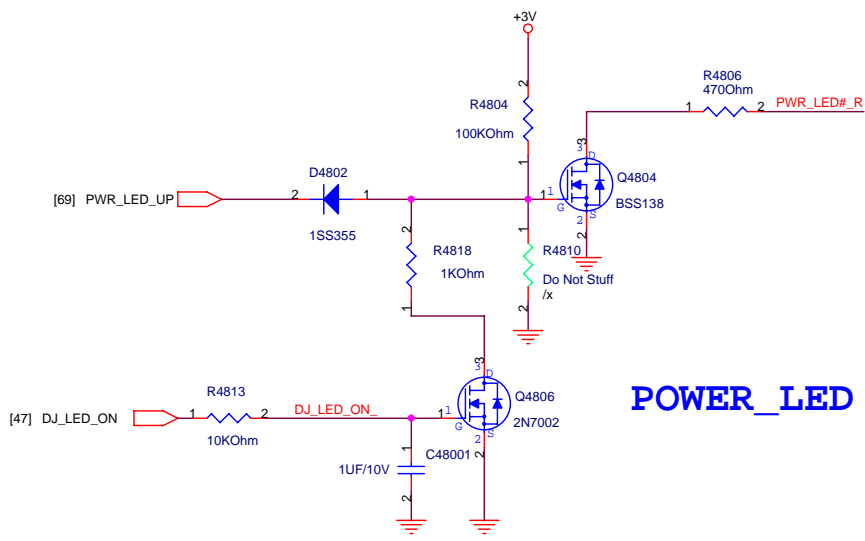


# FUNCTION KEY



A6TcSKU1

		Title : FUNCTION KEY	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size B	Project Name A6T	Date: Wednesday, March 08, 2006	Rev 1.0
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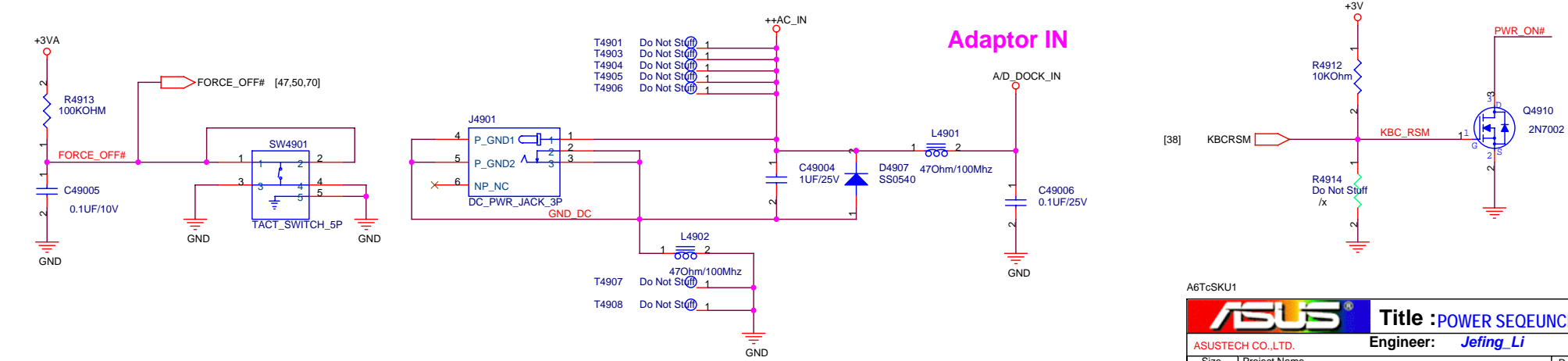
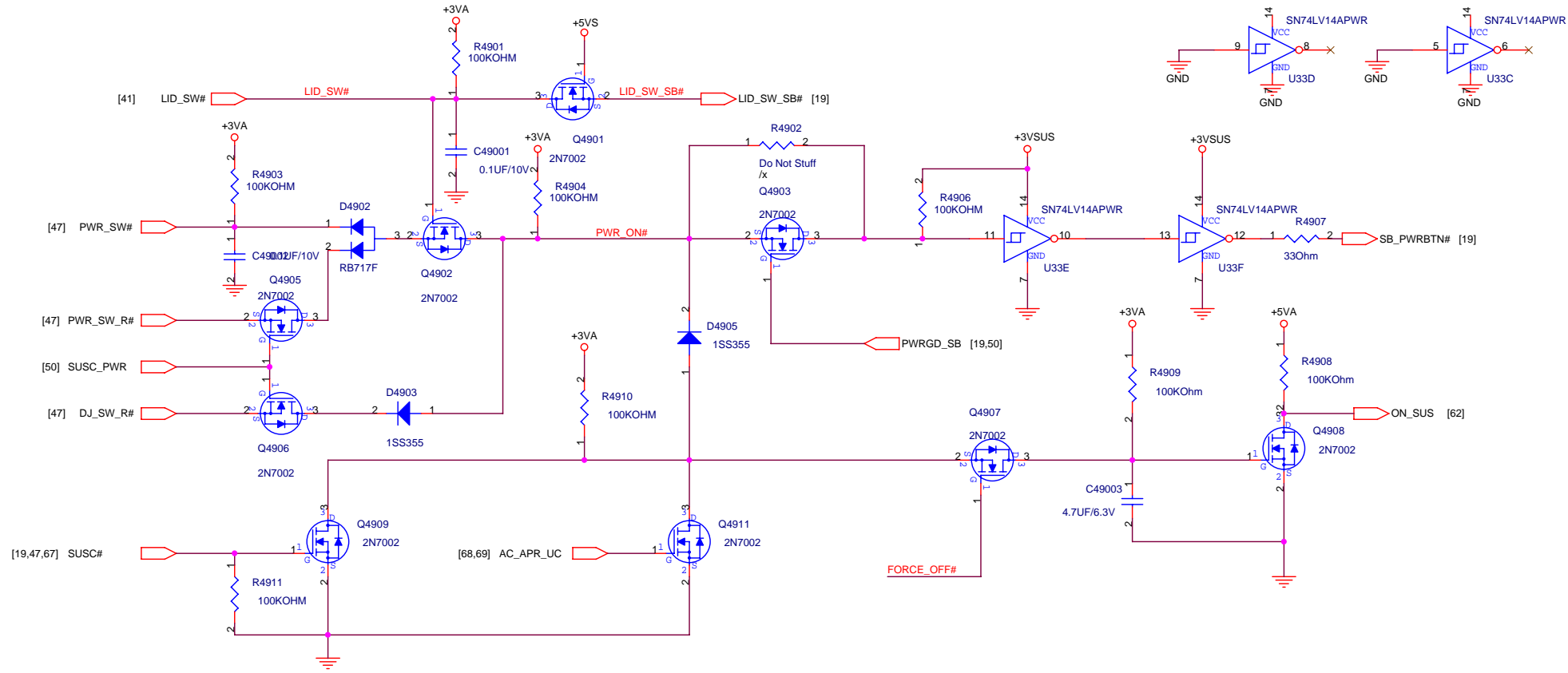
**ASUS** Title : LED

ASUSTECH CO.,LTD. Engineer: Jefing\_Li

Size	Project Name	Rev
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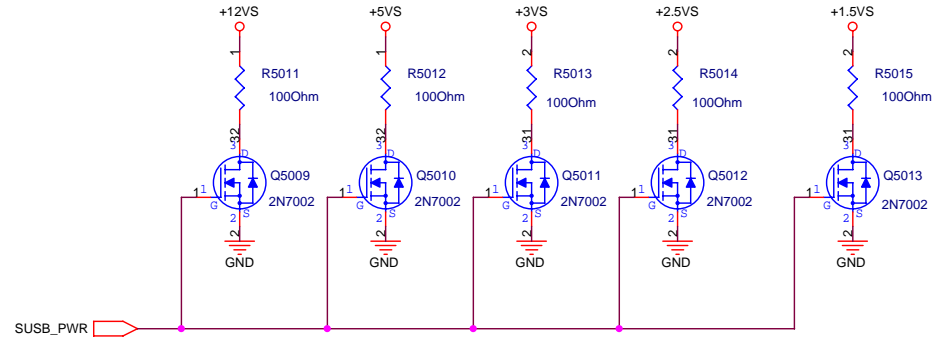
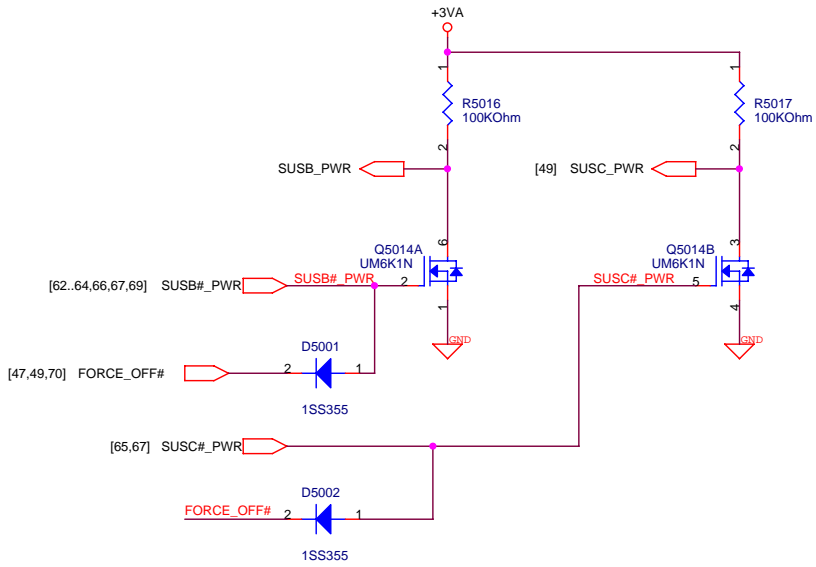
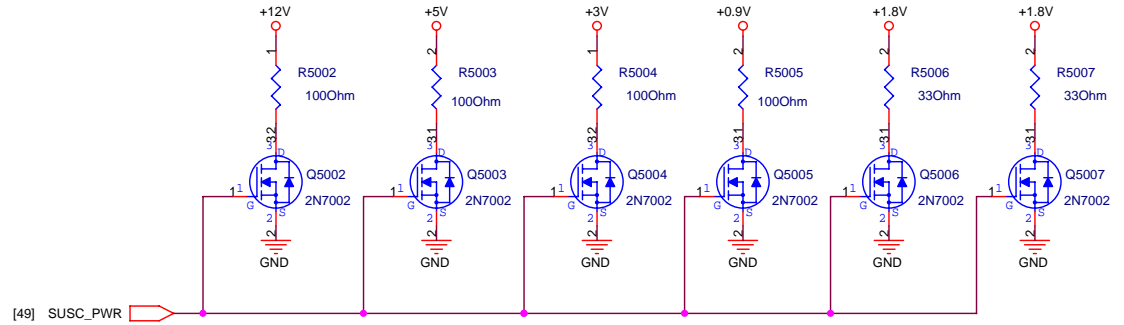
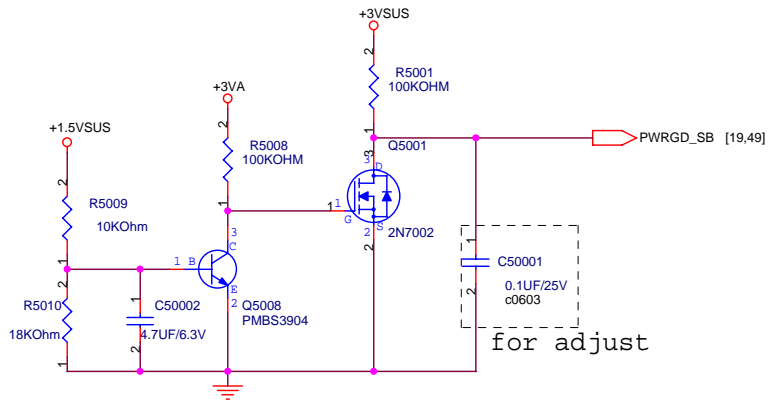
A6TcSKU1

**Title :POWER SEQUENCE(1)**

ASUSTECH CO.,LTD. Engineer: *Jefing\_Li*

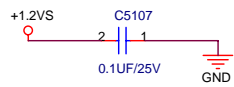
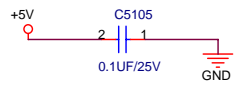
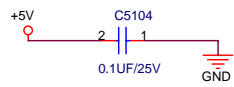
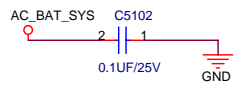
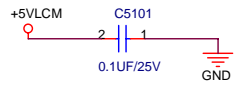
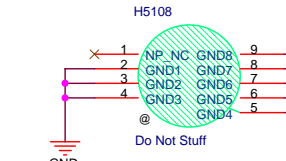
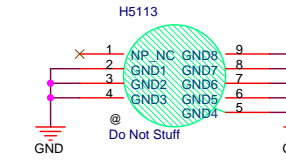
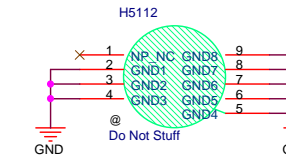
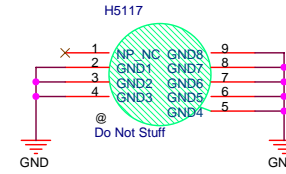
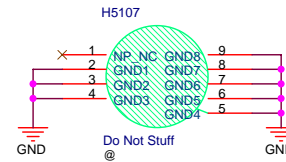
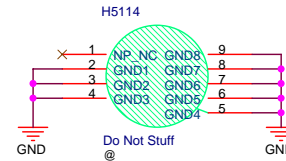
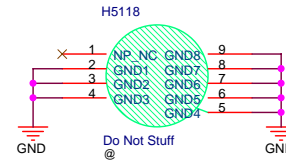
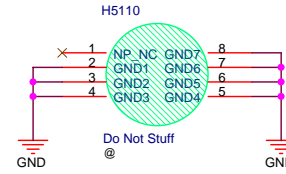
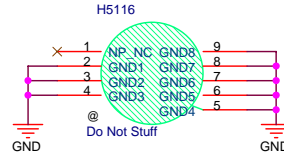
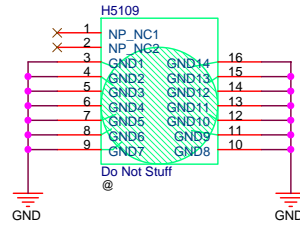
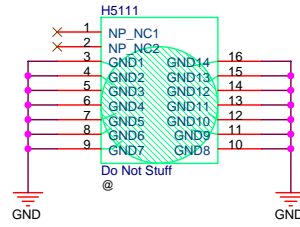
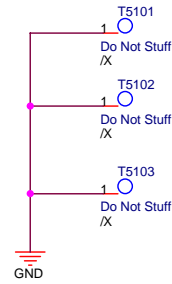
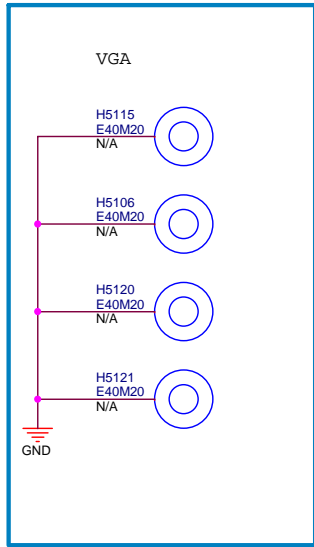
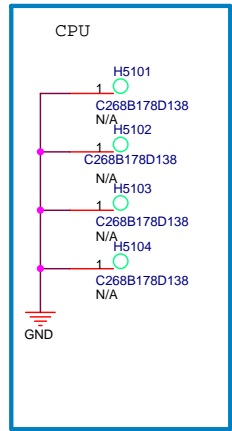
Size	Project Name	Rev
B	<b>A6T</b>	1.0

Date: Wednesday, March 08, 2006 Sheet 49 of 72



A6TcSKU1

<b>ASUS</b>		<b>Title : POWER SEQUENCE(2)</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name		Rev
B	<b>A6T</b>		1.0
Date: Wednesday, March 08, 2006		Sheet	50 of 72



A6TcSKU1

<b>ASUS</b>		<b>Title : SCREW HOLE</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name		Rev
B	<b>A6T</b>		1.0
Date: Wednesday, March 08, 2006		Sheet	51 of 72

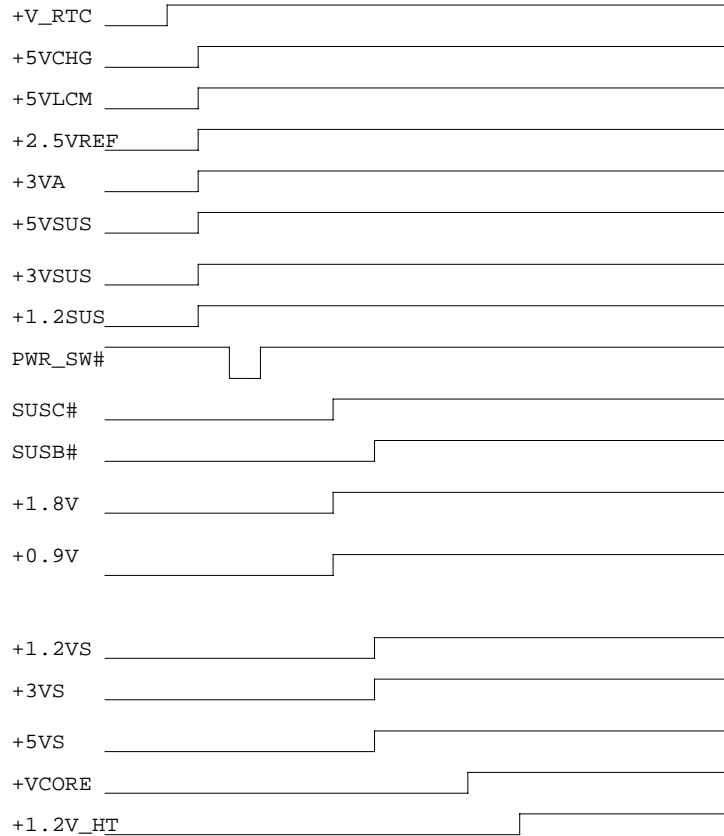
RUN S0-S1 This voltage rail is present when the system is "running"

SUS S0-S1-S3 This voltage rail is present when the system is running or in suspend-to-RAM

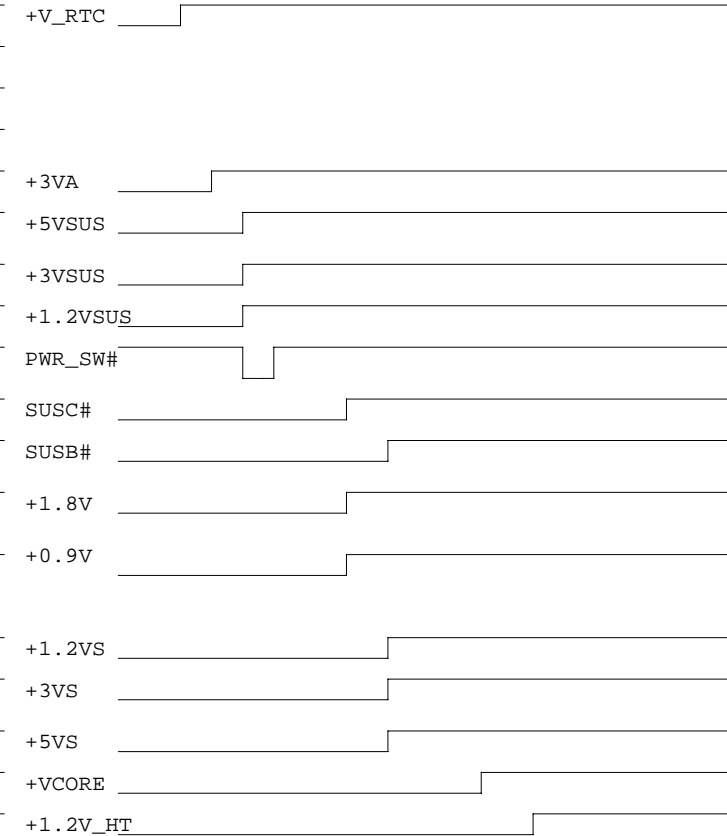
ALWAYS S0-S1-S3-S4-S5 This voltage rail is always present as long as there is main power, whether in the form of a system battery, an AC adapter, or other type of main power supply

RTC S0-S5, G3 This voltage rail is always present for the Real Time Clock and CMOS RAM circuitry even in the mechanical off state as long as the coin cell is present and not discharged.

AC MODE

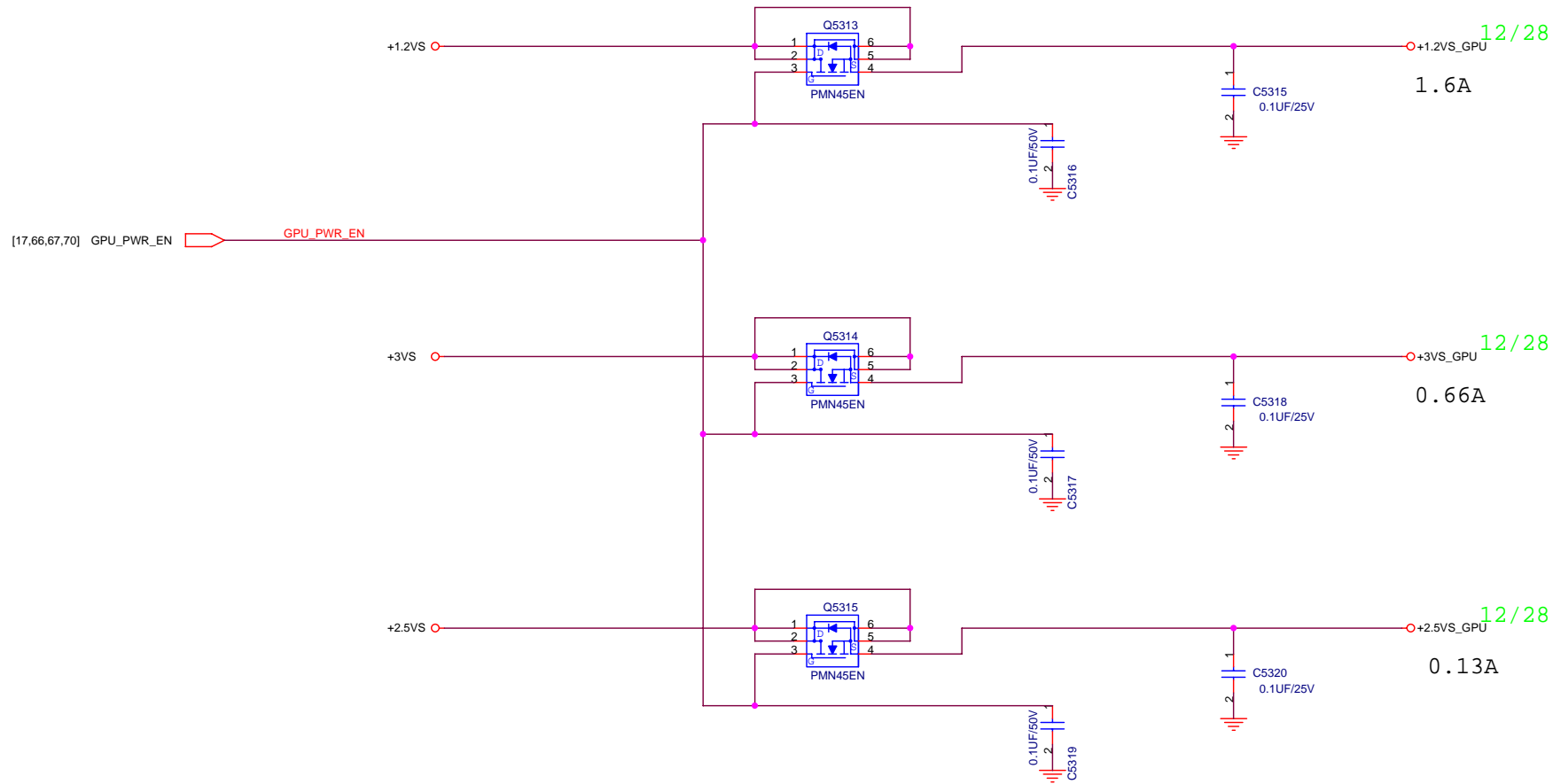


BAT MODE



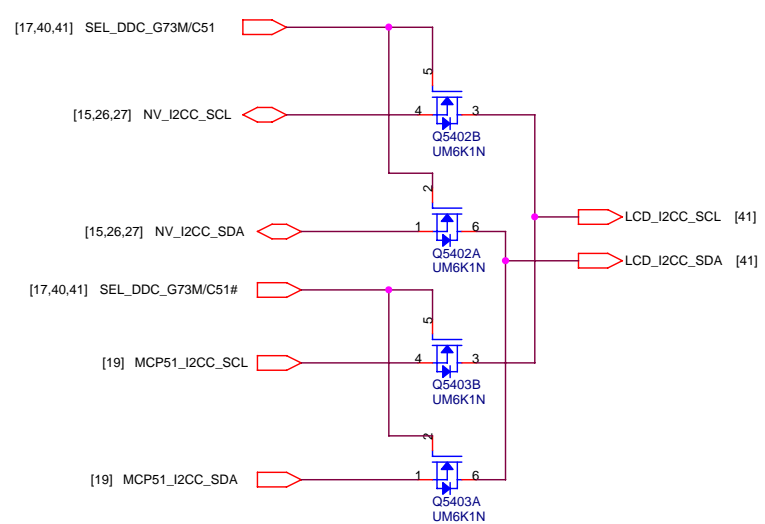
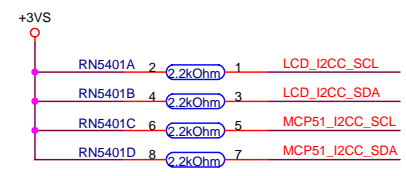
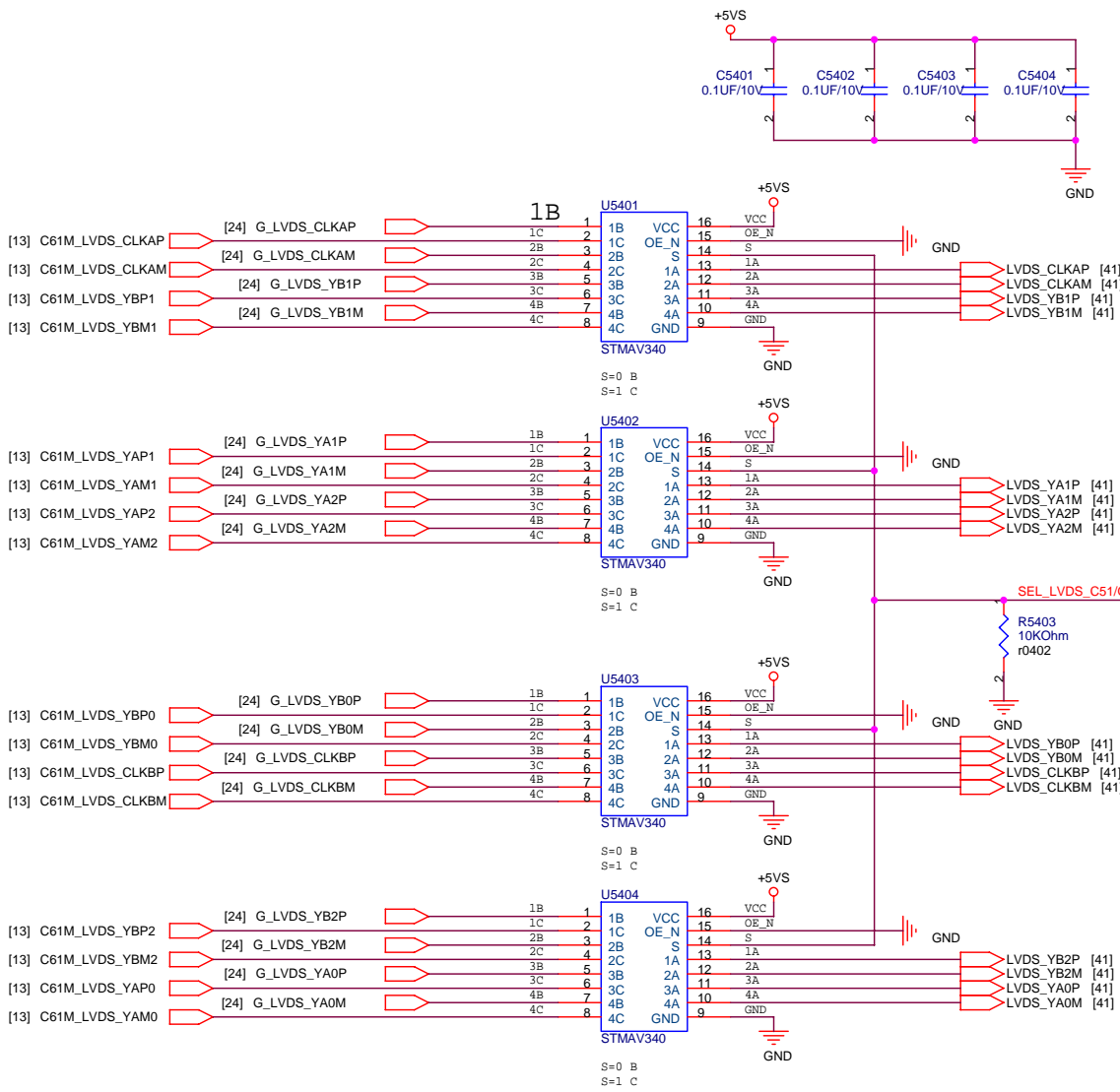
A6TcSKU1

		Title :POWER SEQUENCE BLCOK	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name	Rev	
Custom	A6T	1.0	
Date: Wednesday, March 08, 2006		Sheet	52 of 72



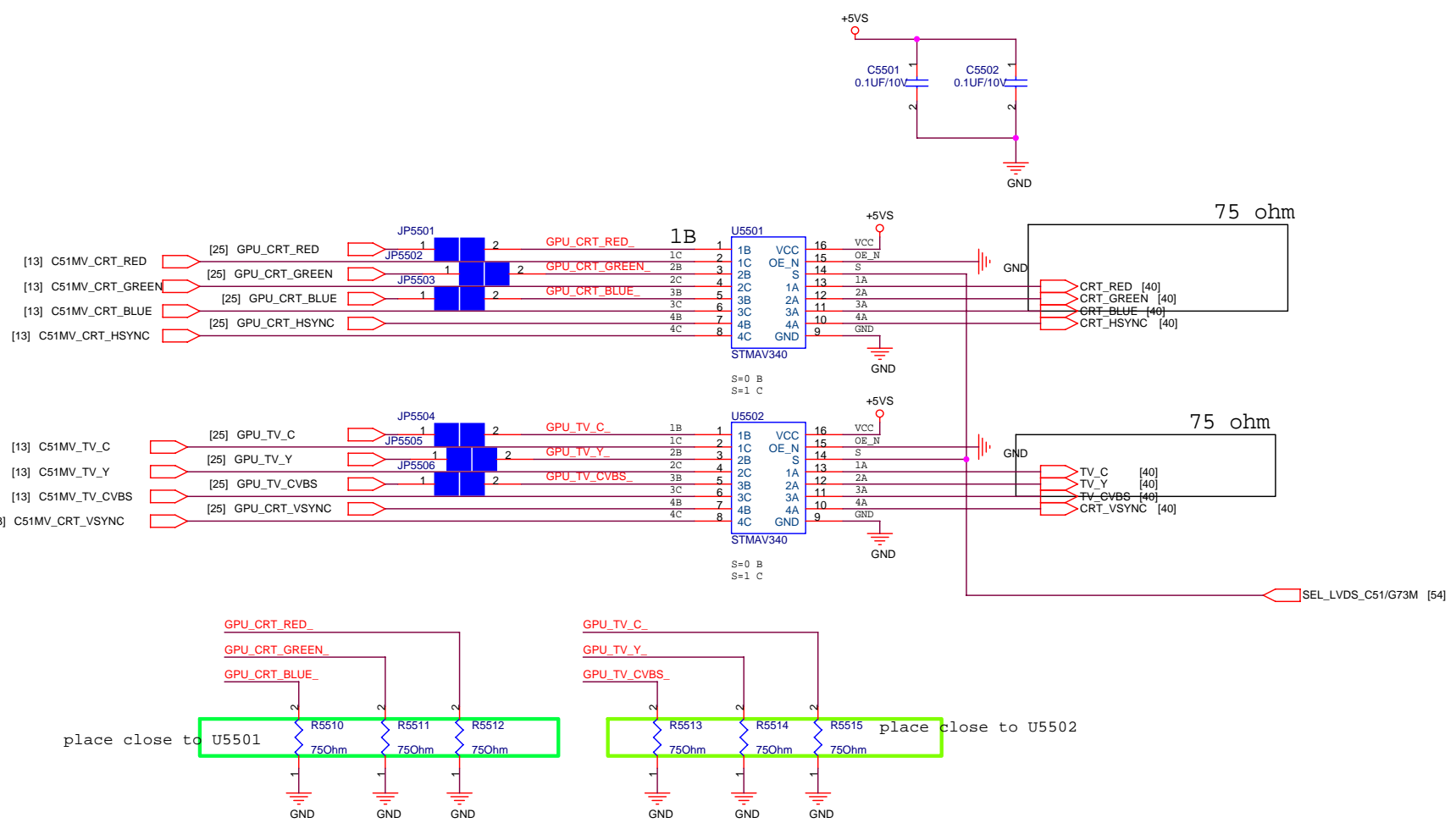
A6TcSKU1

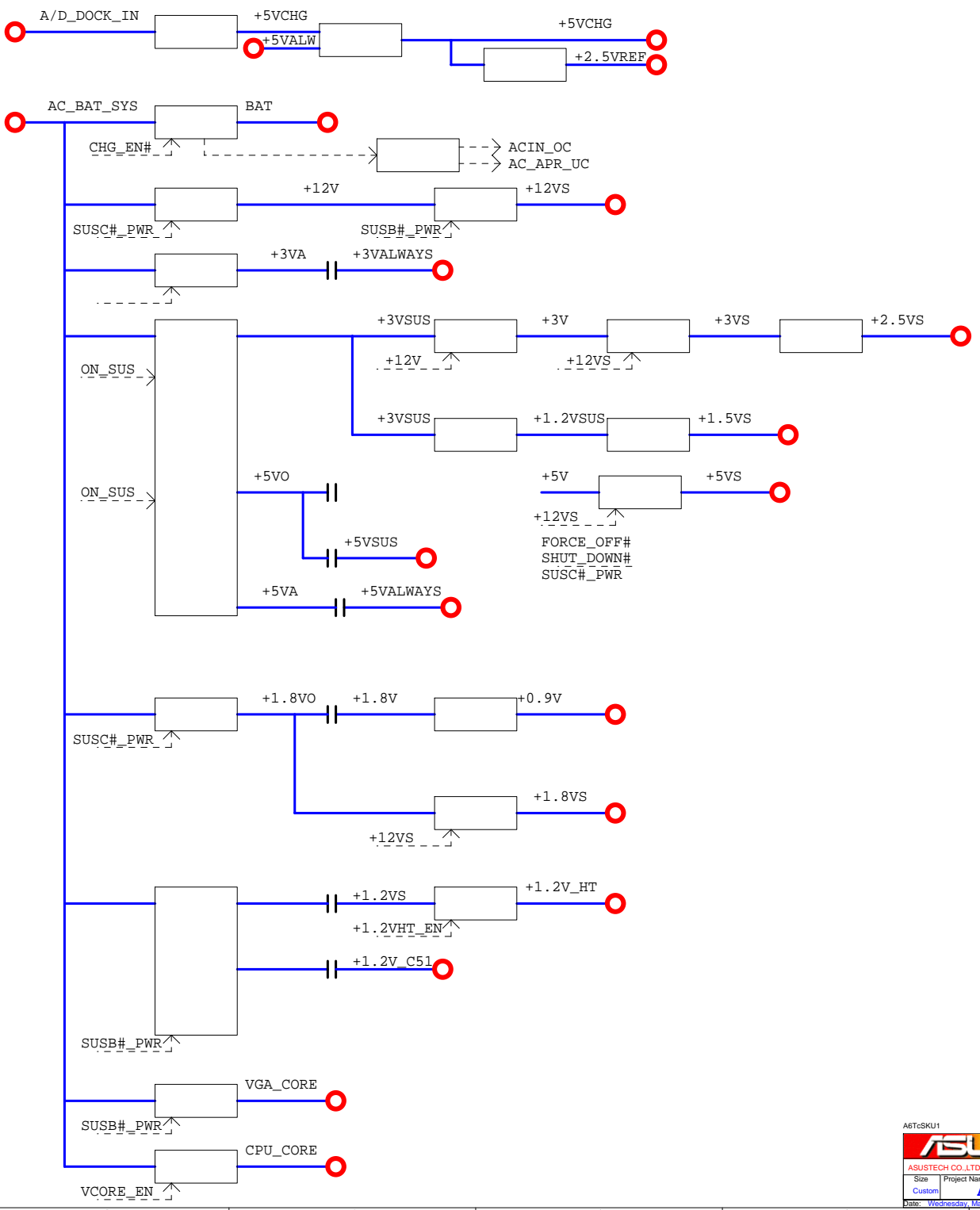
		Title : BLANK	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name		Rev
B	A6T		1.0
Date: Wednesday, March 08, 2006		Sheet 53 of 72	



A6TcSKU1

		Title : BLANK	
ASUSTECH CO.,LTD.		Engineer: Jefing_Li	
Size	Project Name		Rev
B	A6T		1.0
Date: Wednesday, March 08, 2006	Sheet	54	of 72







5

4

3

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1

D

D

C

C

B

B

A

A

A6TcSKU1

		<b>Title : BLANK</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name		Rev
B	<b>A6T</b>		1.0
Date:	Wednesday, March 08, 2006	Sheet	57 of 72

5

4

3

2

1

5

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2

1

D

D

C

C


B

B

A

A

A6TcSKU1

		<b>Title : BLANK</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name		Rev
B	<b>A6T</b>		1.0
Date: <i>Wednesday, March 08, 2006</i>		Sheet	58 of 72

5

4

3

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2

1

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D

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C

B

B

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A

A6TcSKU1

		<b>Title : BLANK</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name		Rev
B	<b>A6T</b>		1.0
Date: <i>Wednesday, March 08, 2006</i>		Sheet	59 of 72

5

4

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2

1

5

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3

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1

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D

C

C


B

B

A

A

A6TcSKU1

		<b>Title : BLANK</b>	
ASUSTECH CO.,LTD.		Engineer: <i>Jefing_Li</i>	
Size	Project Name		Rev
B	<b>A6T</b>		1.0
Date: <i>Wednesday, March 08, 2006</i>		Sheet	60 of 72

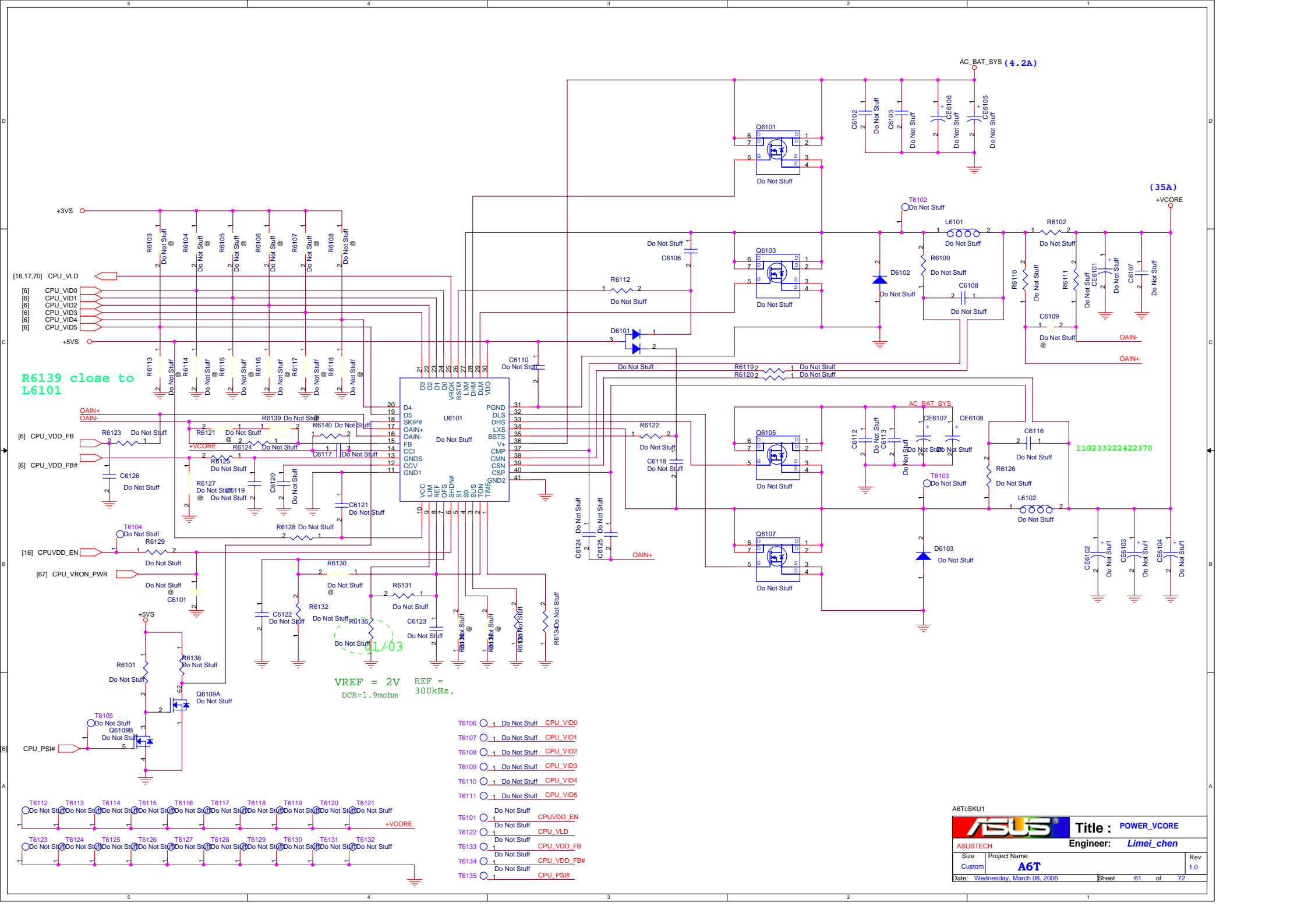
5

4

3

2

1



[16,17,70] CPU\_VLD  
 [6] CPU\_VID0  
 [6] CPU\_VID1  
 [6] CPU\_VID2  
 [6] CPU\_VID3  
 [6] CPU\_VID4  
 [6] CPU\_VID5  
 +5VS

R6139 close to L6101

[6] CPU\_VDD\_FB  
 [6] CPU\_VDD\_FB#

[16] CPUVDD\_EN  
 [67] CPU\_VRON\_PWR

CPUI\_PSI#

T6112 T6113 T6114 T6115 T6116 T6117 T6118 T6119 T6120 T6121  
 Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff  
 +VCORE

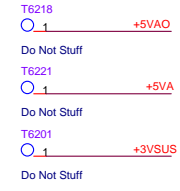
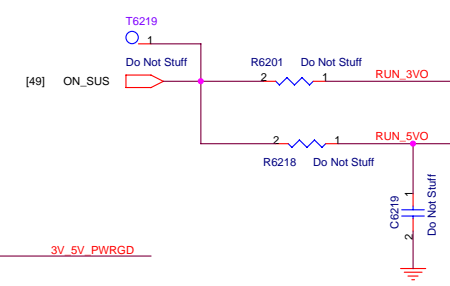
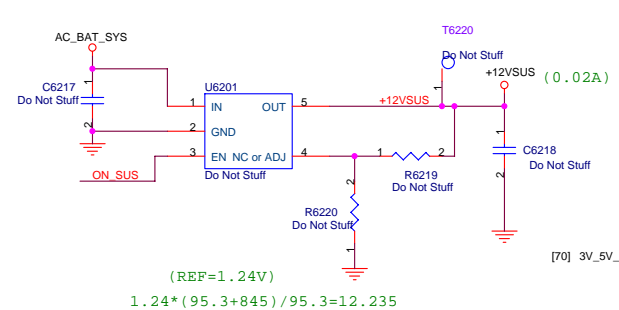
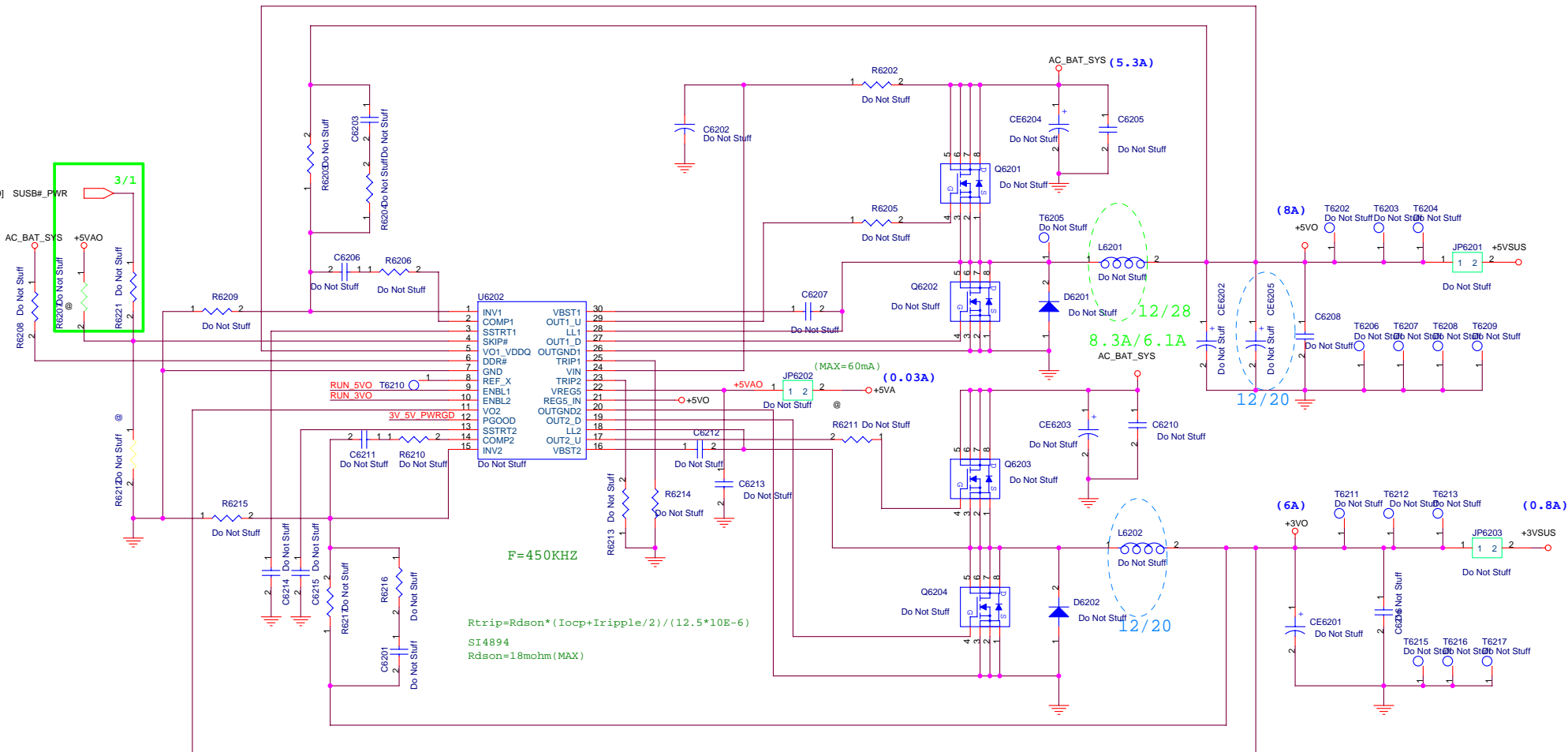
T6123 T6124 T6125 T6126 T6127 T6128 T6129 T6130 T6131 T6132  
 Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff

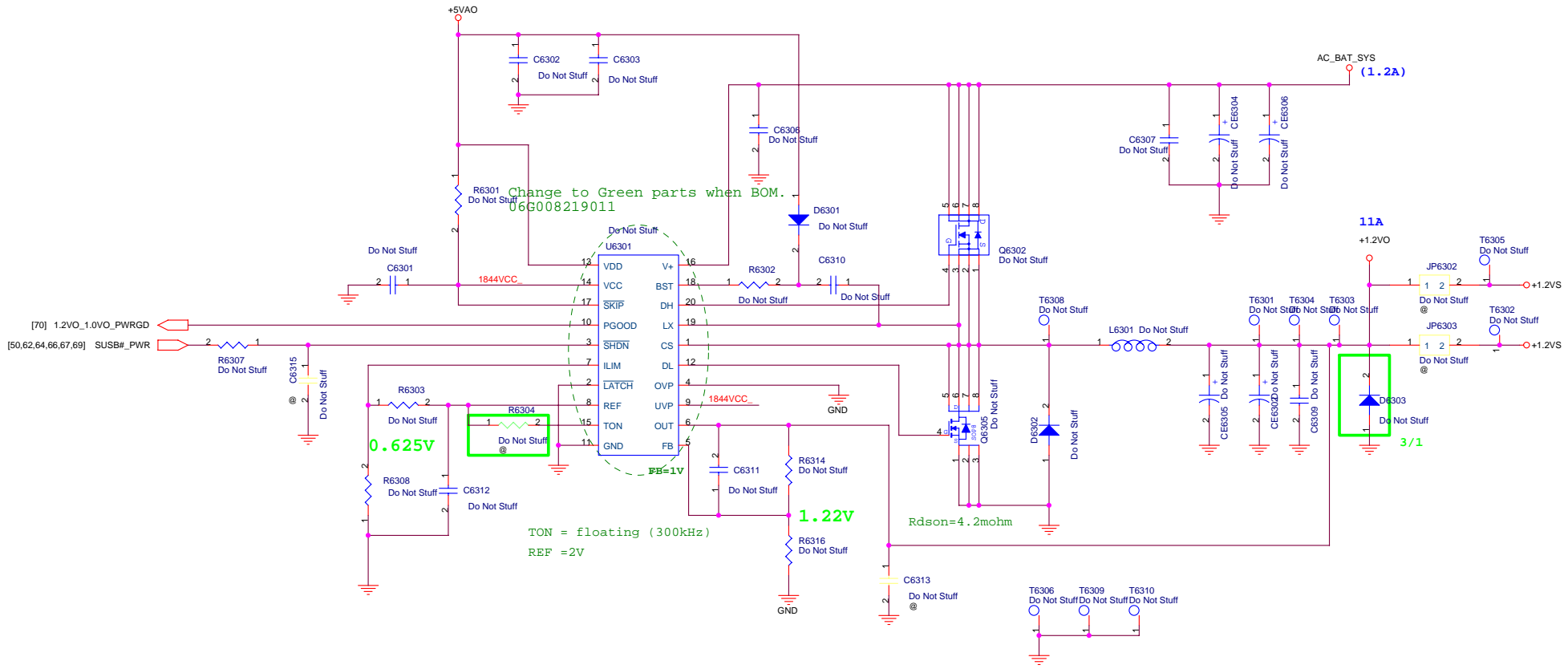
VREF = 2V REF = 300kHz,  
 DCR=1.9mohm

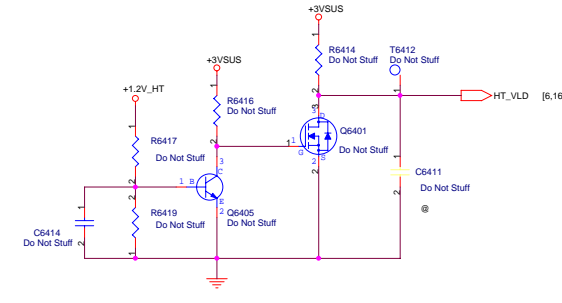
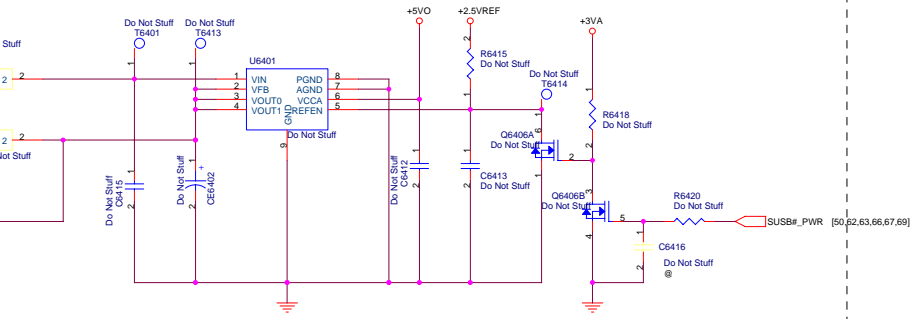
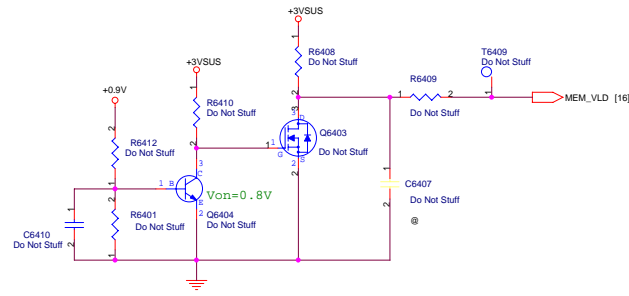
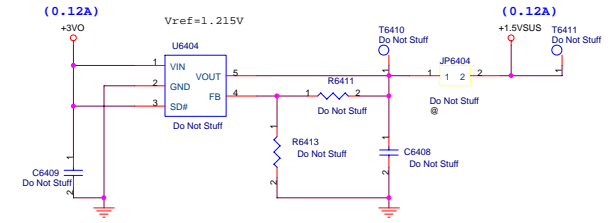
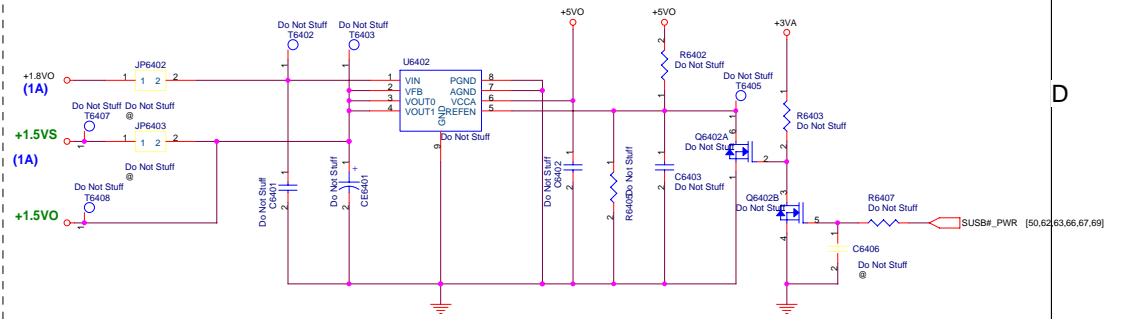
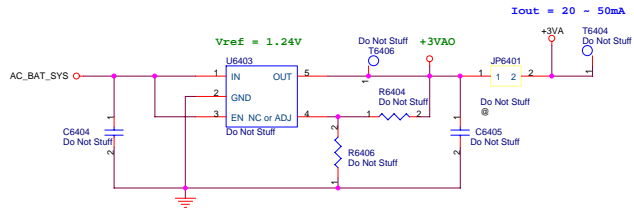
- T6106 1 Do Not Stuff CPU\_VID0
- T6107 1 Do Not Stuff CPU\_VID1
- T6108 1 Do Not Stuff CPU\_VID2
- T6109 1 Do Not Stuff CPU\_VID3
- T6110 1 Do Not Stuff CPU\_VID4
- T6111 1 Do Not Stuff CPU\_VID5
- Do Not Stuff CPUVDD\_EN
- T6122 1 Do Not Stuff CPU\_VLD
- T6133 1 Do Not Stuff CPU\_VDD\_FB
- T6134 1 Do Not Stuff CPU\_VDD\_FB#
- T6135 1 Do Not Stuff CPU\_PSI#

A6TcSKU1

		Title : POWER_VCORE	
		ASUSTECH Engineer: Limei_chen	
Size	Project Name	Rev	
Custom	A6T	1.0	
Date: Wednesday, March 08, 2006		Sheet	61 of 72

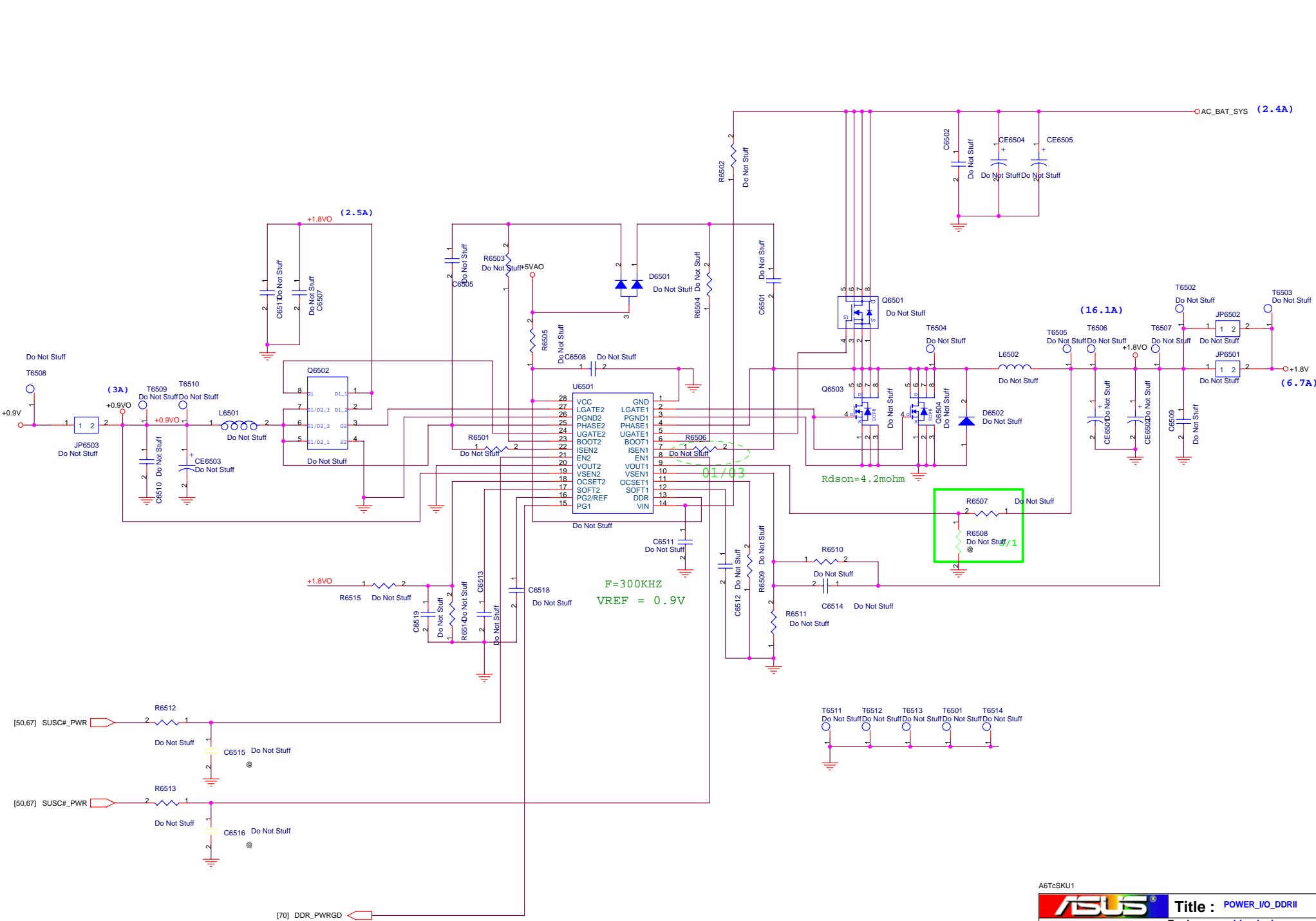


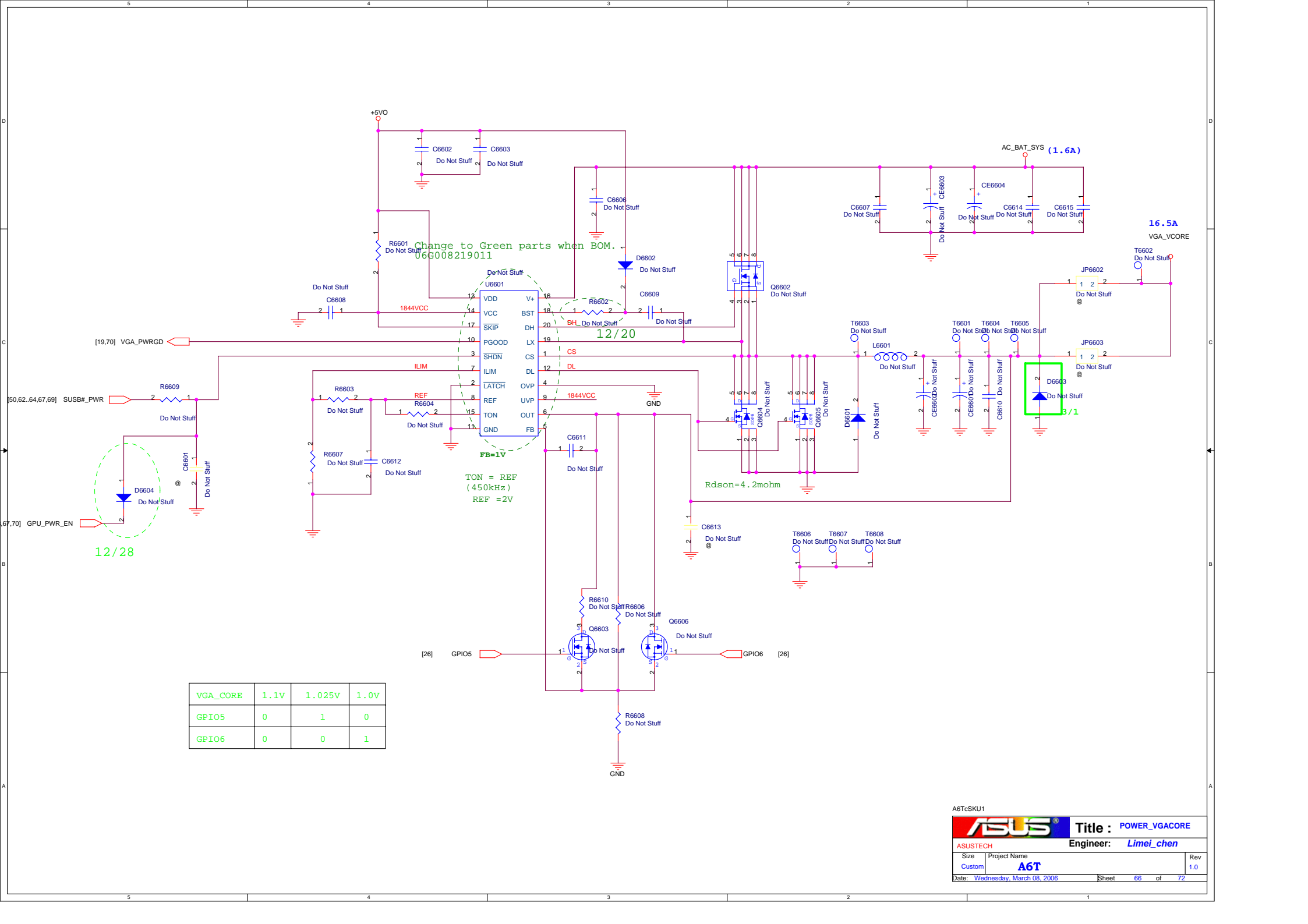




A6TcSKU1		<b>ASUS</b> Title : POWER_VO_LDO	
ASUSTECH		Engineer: Limei.chen	
Size	Project Name	Rev	
C	A6T	1.0	
Date: Wednesday, March 08, 2006		Sheet	64 of 72







Change to Green parts when BOM.  
06G008219011

12/20

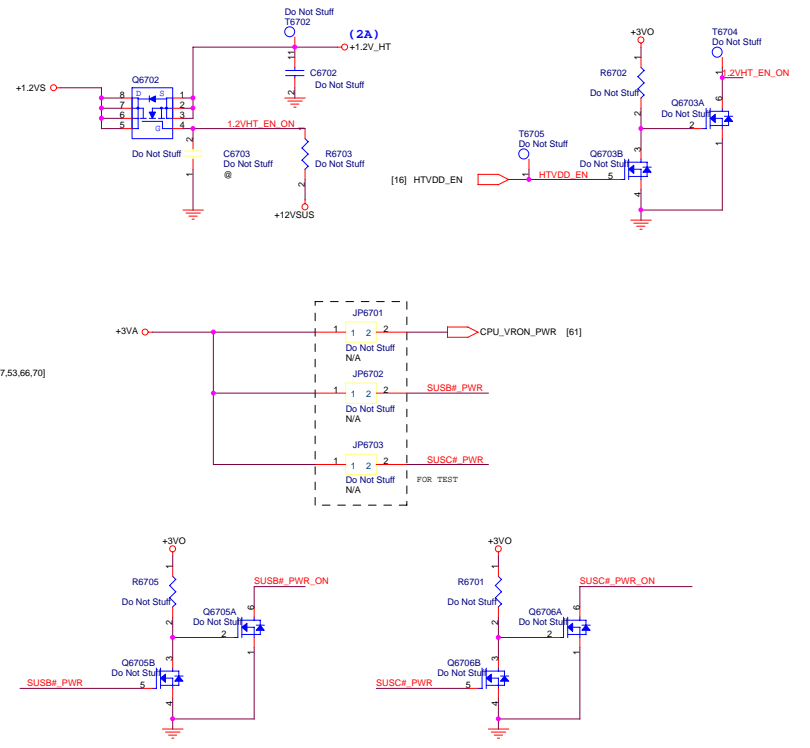
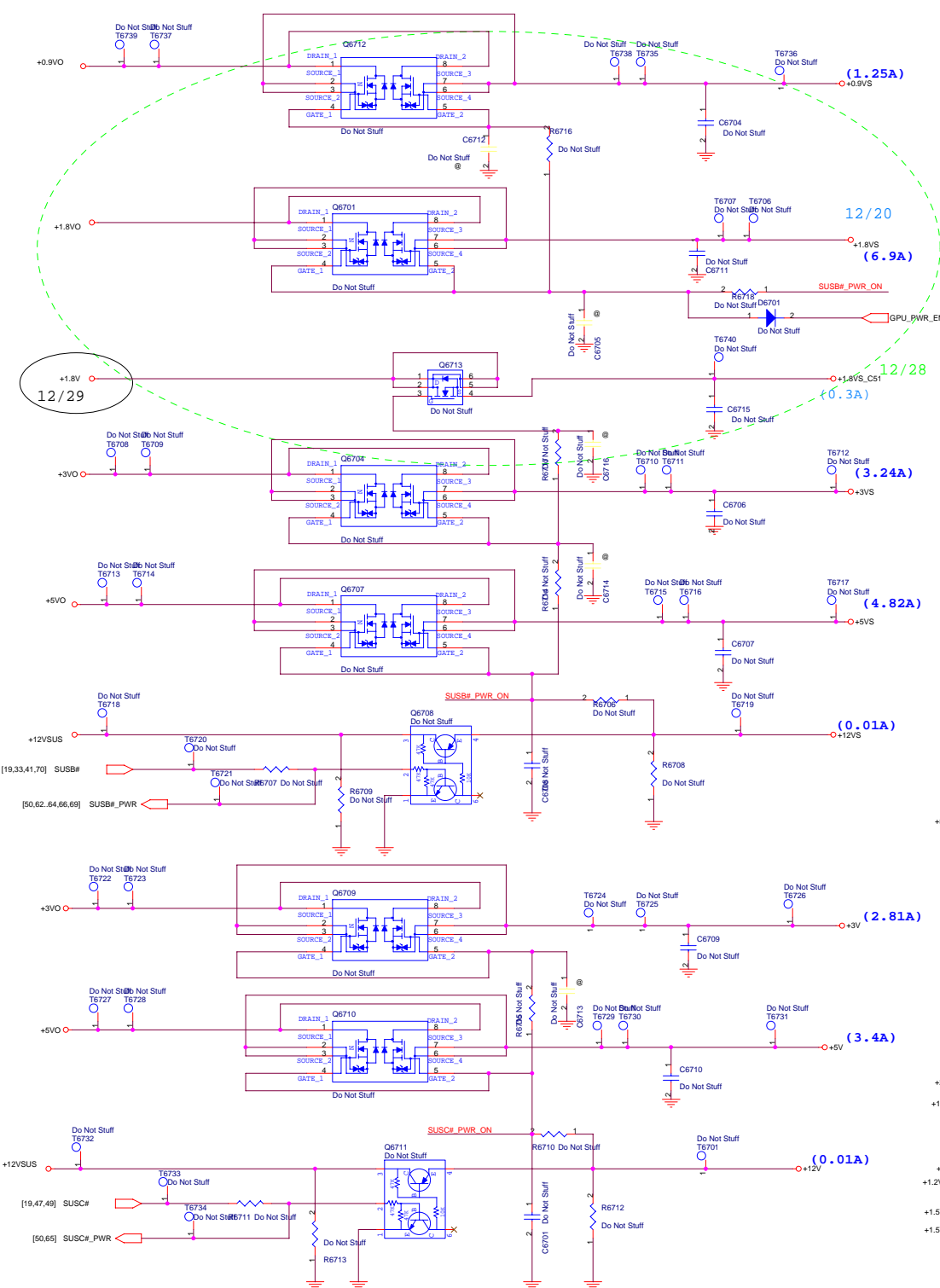
TON = REF  
(450kHz)  
REF = 2V

Rdson=4.2mohm

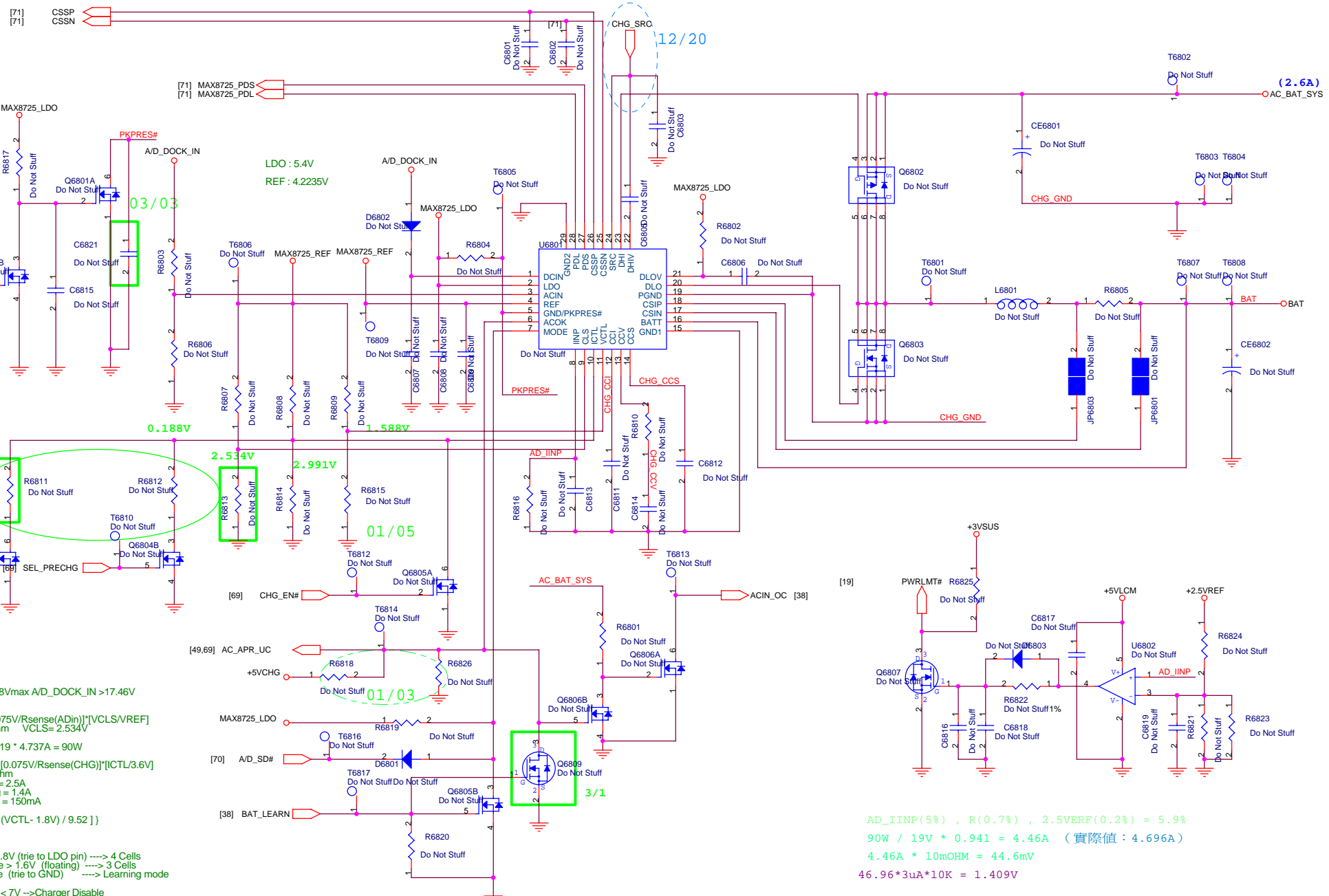
VGA_CORE	1.1V	1.025V	1.0V
GPIO5	0	1	0
GPIO6	0	0	1

A6TcSKU1

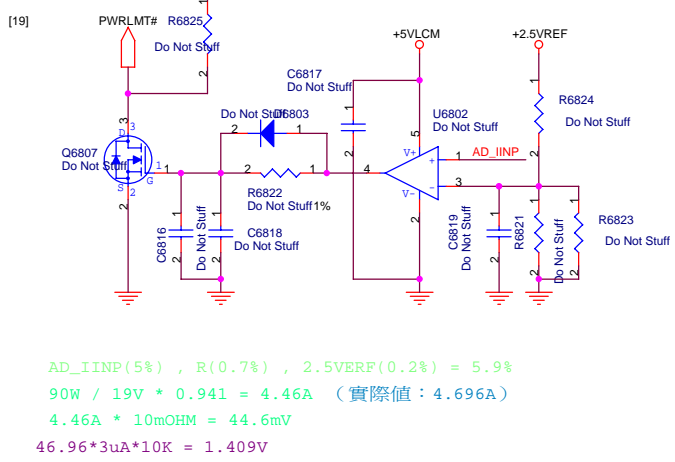
**ASUS** Title : POWER\_VGACORE  
 ASUSTECH Engineer: Limei\_chen  
 Size Project Name  
 Custom A6T  
 Date: Wednesday, March 08, 2006 Sheet 66 of 72



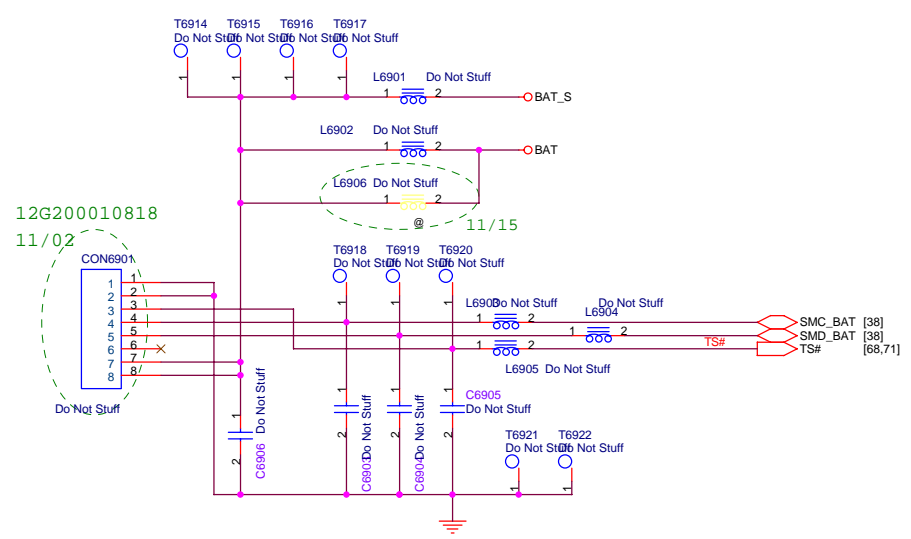
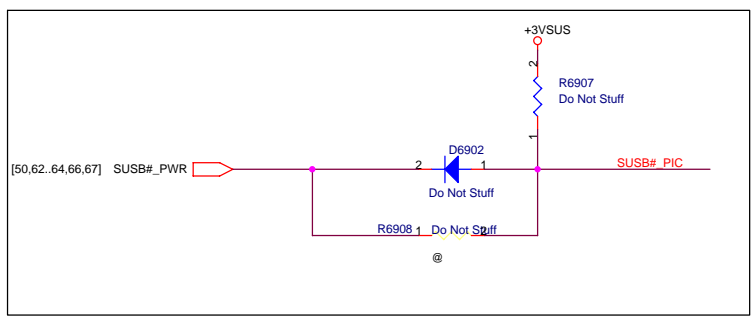
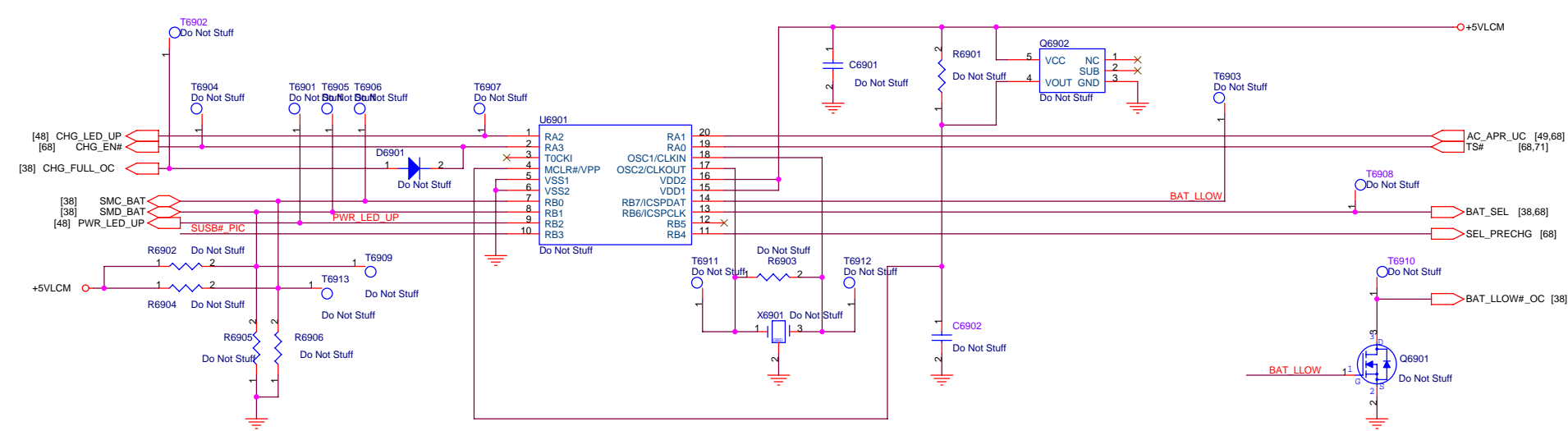
+3VA	[19,41,47,49,50,64,71]	AC_BAT_SYS	AC_BAT_SYS [41,51,61,66,68,71]
+3VSUS	[6,17,19,21,39,43,45,46,49,50,62,64,68,70]	BAT	BAT [66,69,71]
+3V0	[82,64]	+VCORE	+VCORE [7,61]
+3V	[32,35,38,39,41,45,50,64]	VGA_VCORE	VGA_VCORE [22,66]
+3VA0	[64]		
+3VS	[6,8,9,12,19,21,31,33,36,38,40,43,46,50,53,54,61]		
+5VA0	[82,63,65,70]		
+5VA	[49,62]		
+5VSUS	[48,62]		
+5V0	[82,64,66,71]		
+5V	[34,38,39,41,47,50,51]		
+5VS	[13,15,19,21,31,32,36,38,40,42,43,47,51,54,55,61]		
+5VCHG0	[68,71]		
+5VLCM0	[48,51,68,71]		
+1.8V0	[64,65]		
+1.8V	[6,9,50,65]		
+1.8VS	[23,24,29,30]		
+0.9V0	[65]		
+0.9V	[6,7,9,50,64,65]		
+0.9VS	[29,30]		
+2.5V0	[64]		
+2.5VS	[6,10,13,14,50,53,64]		
+2.5VREF	[64,68,70,71]		
+12VSUS	[17,62]		
+12V	[15,43,50]		
+12VS	[40,41,43,50]		
+1.2VS	[11,14,16,21,51,53,63]		
+1.2V_HT	[4,6,7,10,14,64]		
+1.5VSUS	[20,21,50,64]		
+1.5VS	[16,18,19,21,50,64]		

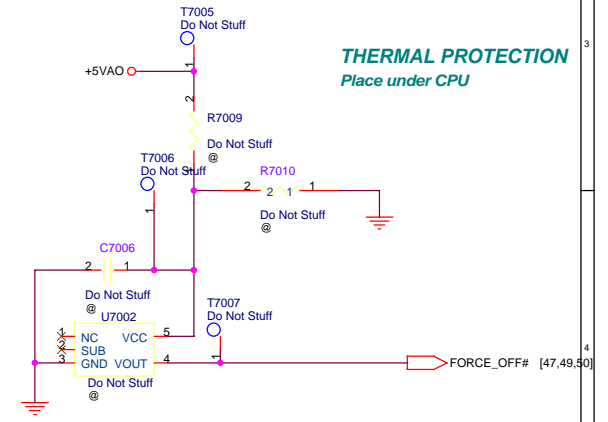
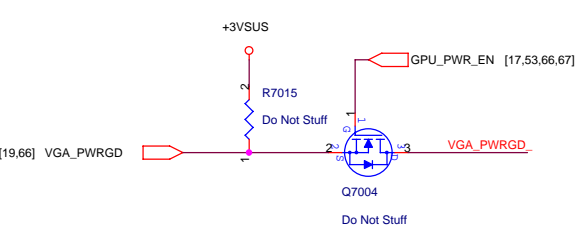
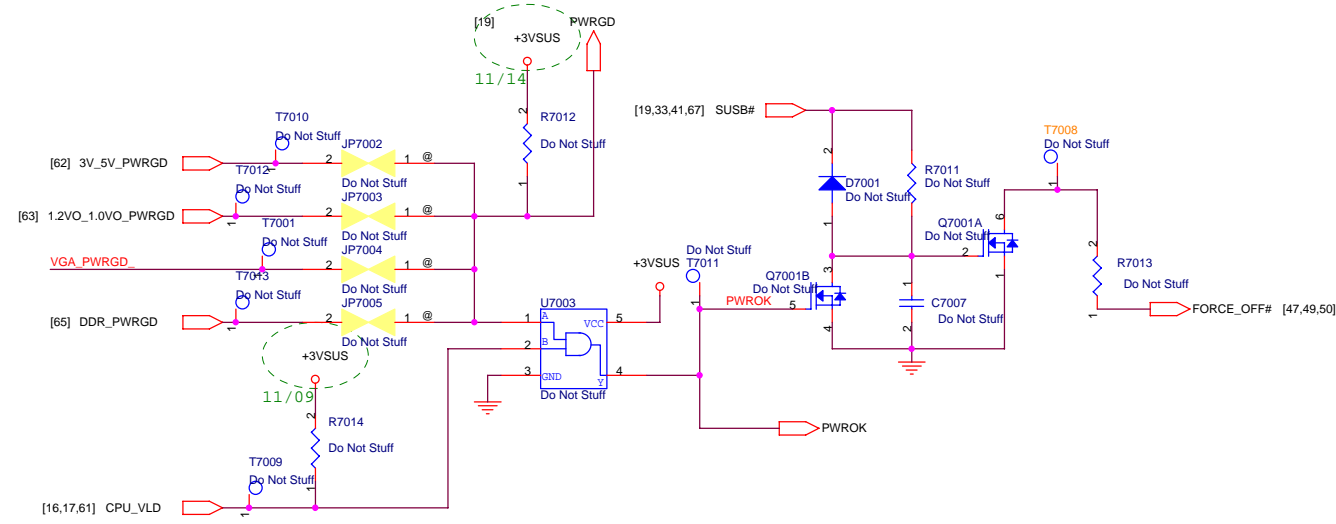
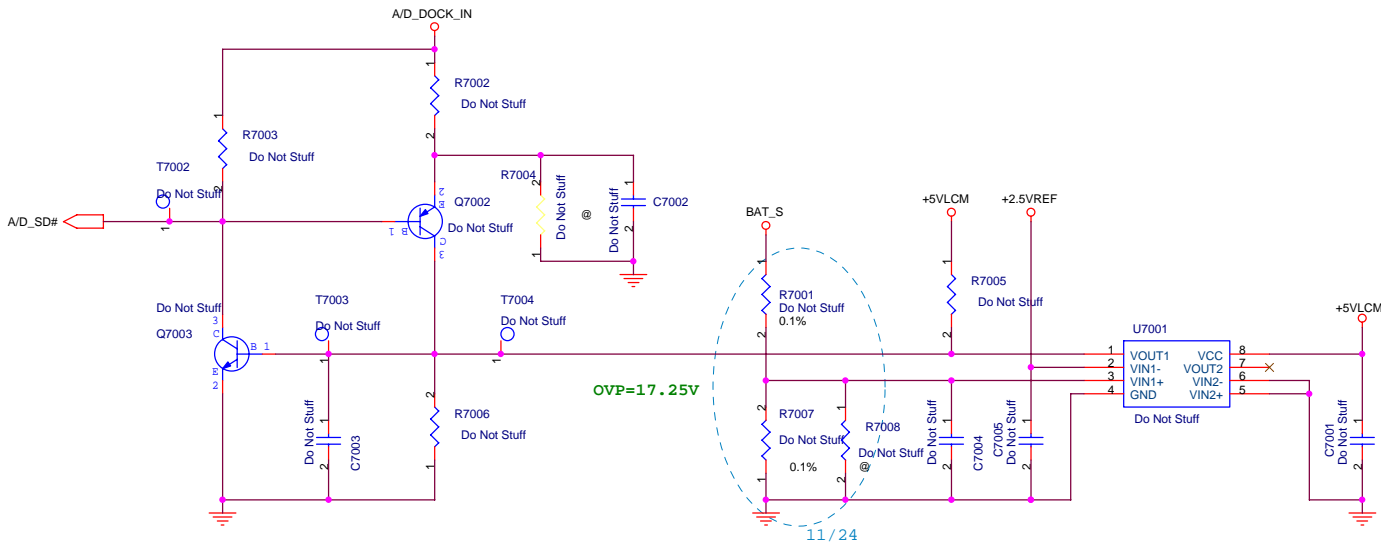


- ⊗ AC\_IN Threshold 2.048V/max A/D\_DOCK\_IN >17.46V active
- ⊗ Adapter lin(max) =  $[0.075V/R_{sense}(ADin)] \cdot [V_{CLS}/REF]$   
 $R_{sense}(ADin)=0.01 \text{ ohm}$   $V_{CLS}=2.534V$   
 $\Rightarrow \text{lin(max)}=4.5A$   
 $\Rightarrow \text{Constant Power} = 19 \cdot 4.737A = 90W$
- ⊗ Charge Current  $I_{chg} = [0.075V/R_{sense}(CHG)] \cdot [I_{CTL}/3.6V]$   
 $R_{sense}(CHG)=0.025 \text{ ohm}$   
 $V_{ICTL}=3.0V \Rightarrow I_{chg} = 2.5A$   
 $V_{ICTL}=1.68V \Rightarrow I_{chg} = 1.4A$   
 $V_{ICTL}=0.18V \Rightarrow I_{chg} = 150mA$
- ⊗  $V_{batt} = \text{Cell} \cdot (V_{ref} + [(V_{CTL} - 1.8V) / 9.52])$   
 $V_{CTL}=1.615V$   
 $\Rightarrow V_{batt} = 4.2V$
- ⊗ Mode pin :  $V_{mode} > 2.8V$  (try to LDO pin) ----> 4 Cells  
 $2.0 > V_{mode} > 1.6V$  (floating) ----> 3 Cells  
 $0.8 > V_{mode}$  (try to GND) ----> Learning mode
- ⊗  $V_{ICTL} < 0.8V$  or  $DCIN < 7V$  --> Charger Disable



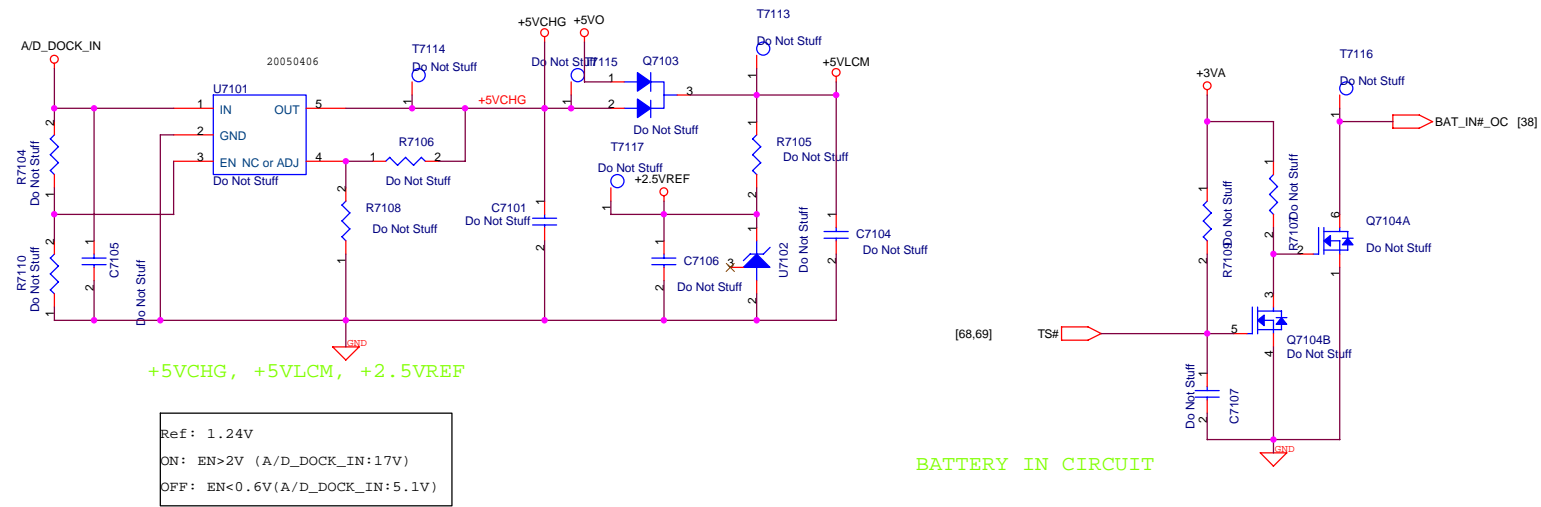
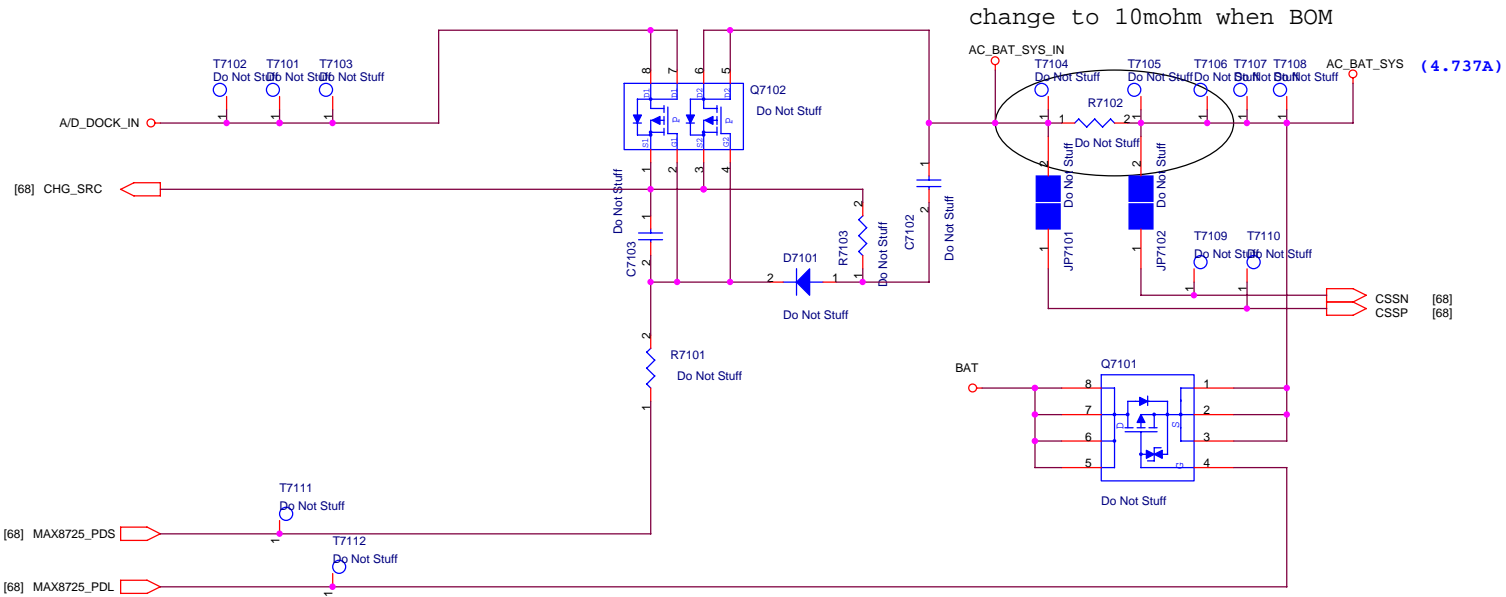
$AD\_IINP(5\%) , R(0.7\%) , 2.5V\_REF(0.2\%) = 5.9\%$   
 $90W / 19V \cdot 0.941 = 4.46A$  (實際值: 4.696A)  
 $4.46A \cdot 10m\Omega = 44.6mV$   
 $46.96 \cdot 3\mu A \cdot 10K = 1.409V$





A6TcSKU1

<b>ASUS</b>		<b>Title : POWER_PROTECT</b>	
ASUSTECH		Engineer: Limei_chen	
Size	Project Name	Rev	
Custom	<b>A6T</b>	1.0	
Date: Wednesday, March 08, 2006	Sheet	70	of 72



BATTERY IN CIRCUIT

A6TcSKU1

<b>ASUS</b>		Title: POWER_SWITCH_5VLCM	
ASUSTECH		Engineer: Limei_chen	
Size	Project Name		Rev
Custom	A6T		1.0
Date: Wednesday, March 08, 2006		Sheet 71 of 72	





12/20 P62 Add CE6205 100UF/6.3V(the high trancient ripple )  
P62 change L6202 from 1.8uh to 3.7uh (because of the low enficiency and the thermal issue)  
P63 change R6312 from 1K to 6.81K  
P63 change R6315 from 9.09K to 20K  
P66 Add C6614 1UF/25V(due to bad Highside Gate)  
P66 change R6602 from 0ohm to 2.7ohm(due to bad Highside Gate)  
P67 exchange 0.9VS &1.8VS  
P67 change Q6702 to SI4800(due to the Voltage is low)  
P67 change Q6702 from PMN45EN(Rdson=40mohm-max)to SI4800(Rdson=18.5mohm-max)  
P68 change C6807 from 1UF/25V to 4.7UF/25V  
P68 change A/D\_DOCK\_in to CHG\_SRC  
P71 change C7105 from 1UF/25V to 4.7UF/25V  
12/28 P66 Add D6604& net GPU\_PWR\_EN  
P67 Add Q6713,R6717,C6716,C6715,R6718,D6701  
P67 add net GPU\_PWR\_\_EN,+1.8VS\_C51  
P62 change L6201 from 1.8uh to 2.8uh (because of the low enficiency and the thermal issue)  
P63 change R6314 from 6.81K to 7.5K(because of the low voltage in device side )  
12/29 P67 change 1.8VO to 1.8V(EE)  
12/30 P68 Add R6826(due to D7103's leakage current is high when the tempreture is high,thermal team 49 degree)  
01/03 P61 change R6135 from 100Kohm to 120kohm(due to OCP)  
P65 change R6506 from 330ohm to 402ohm(due to OCP)  
P68 change R6818 from 49.9Kohm to 4.7Kohm  
P68 Add R6826 15Kohm  
01/04 P68 connect R6807.2,R6808.2,R6809.2 to MAX8725\_REF(due to REF+-0.5%,but LDO +-2.8%)  
P68 change R6807,R6812,R6807,R6808,R6809,R6813,R6814,R6815(due to MAX8725\_REF)

A6TcSKU1

		Title : History	
ASUSTEK COMPUTER INC		Engineer: Rui-xing	
Size	Project Name	Rev	
C	History	1.00	
Date: Wednesday, March 08, 2006		Sheet 73 of 73	

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