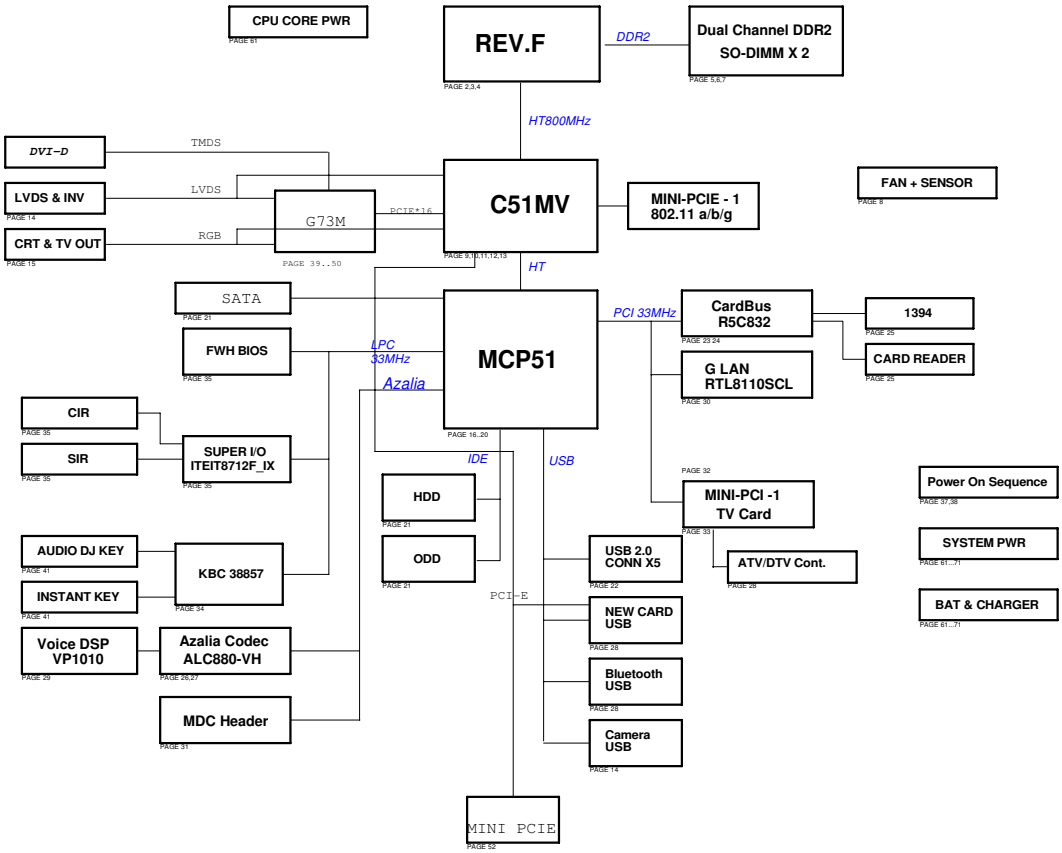
A7T/M BLOCK DIAGRAM



01_BLOCK DIAGRAM	41_G73M_PCIEX16_1
02_AMD S1 CPU(1)	42_G73M_PCIEX16_2
03_AMD S1 CPU(2)	43_G73M_DISPLAY
04_AMD S1 CPU(3)	44_G73M_BIOS&CRY
05_DDR2_SO_DIMM-1	45_G73M_GPIO
06_DDR2_SO_DIMM-2	46_G73M_STRAP
07_DDR2_SODIMMS	47_G73M_VRAM1
08_THERMAL&FAN	48_G73M_VRAM2
09_C51M HT_CPU	49_G73M_VRAM3
10_C51M HT_MCP	50_G73M_VRAM4
11_C51M PCIEx16	51_RJ11+45&MINI
12_C51M VGA OUTPUT	52_NEWCARD (802.11)
13_C51M POWER&GND	61_Vcore
14_LVDS CONNECTER	62_SYSTEM
15_CRT TV CONNECTER	63_1.2VO&+1.8VO
16_MCP51_HT I/F	64_2.5V & 0.9V_3VA
17_MCP51_PCI I/F	65_ VGACORE
18_MCP51_IDE	66_1V_C51_CORE
19_MCP51_USB	67_LOAD SWITCH
20_MCP51_POWER	68_CHARGE
21_HDD&ODD	69_PIC16C54
22_USB	70_BATCONN
23_CARDBUS R5C841	71_PWRGD_SHUTDOWN#
24_CARDBUS SOCKET	53_SYSTEM RESOURCE
25_1394 CON	54_HISTORY
26_ALC880	
27_AMP	
28_BT/FM/RF	
29_VOICE DSP	
30_LAN_RTL8100TL	
31_RJ11+45&MDC	
32_MINIPCI (802.11)	
33_MINIPCI (TV)	
34_KBC 38857	
35_SUPER I/O	
36_FUNCTION KEY	
37_PWR ON SEQ-1	
38_PWR ON SEQ-2	
39_G73M_FB_1	
40_G73M_FB_2	

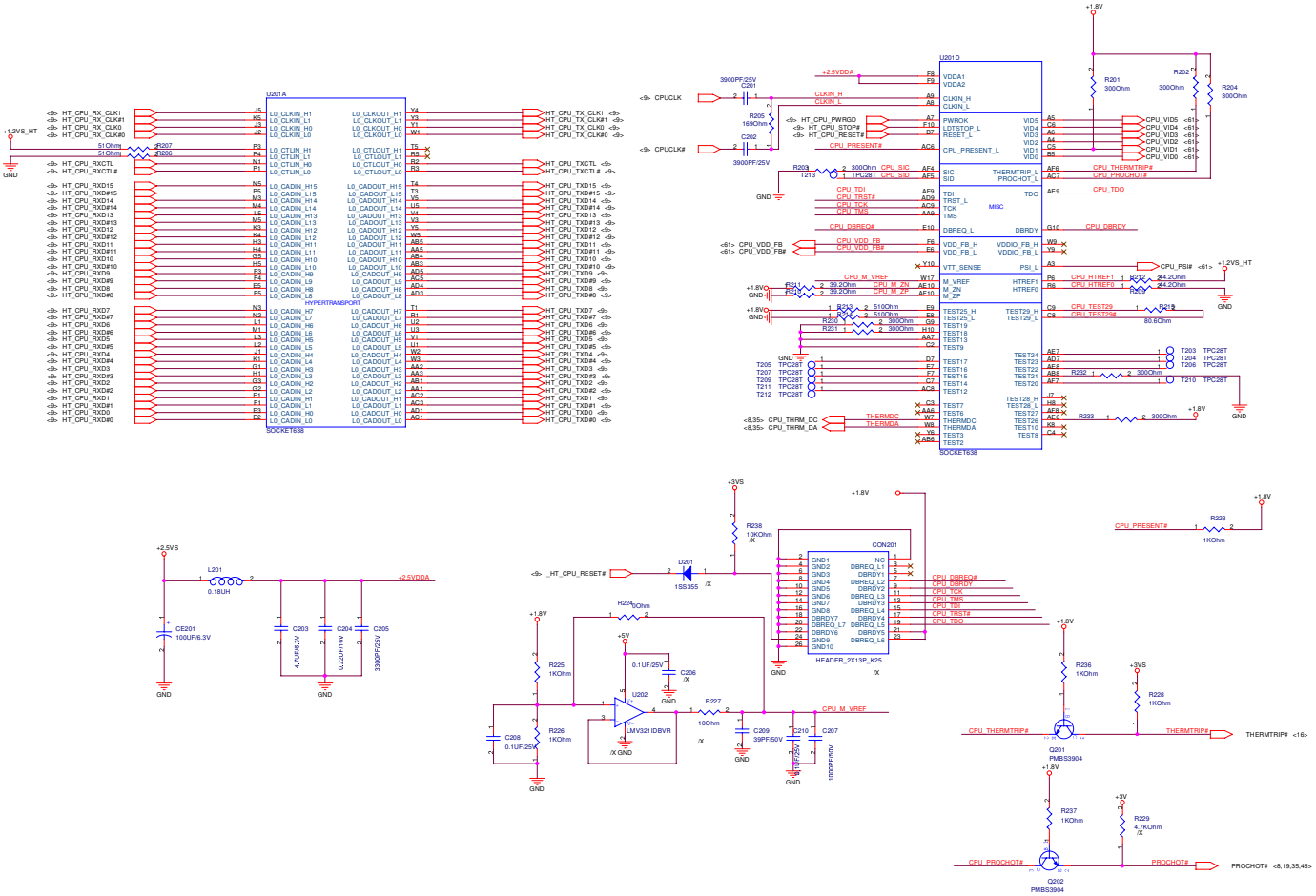
ASUSTeK

Title : BLOCK DIAGRAM

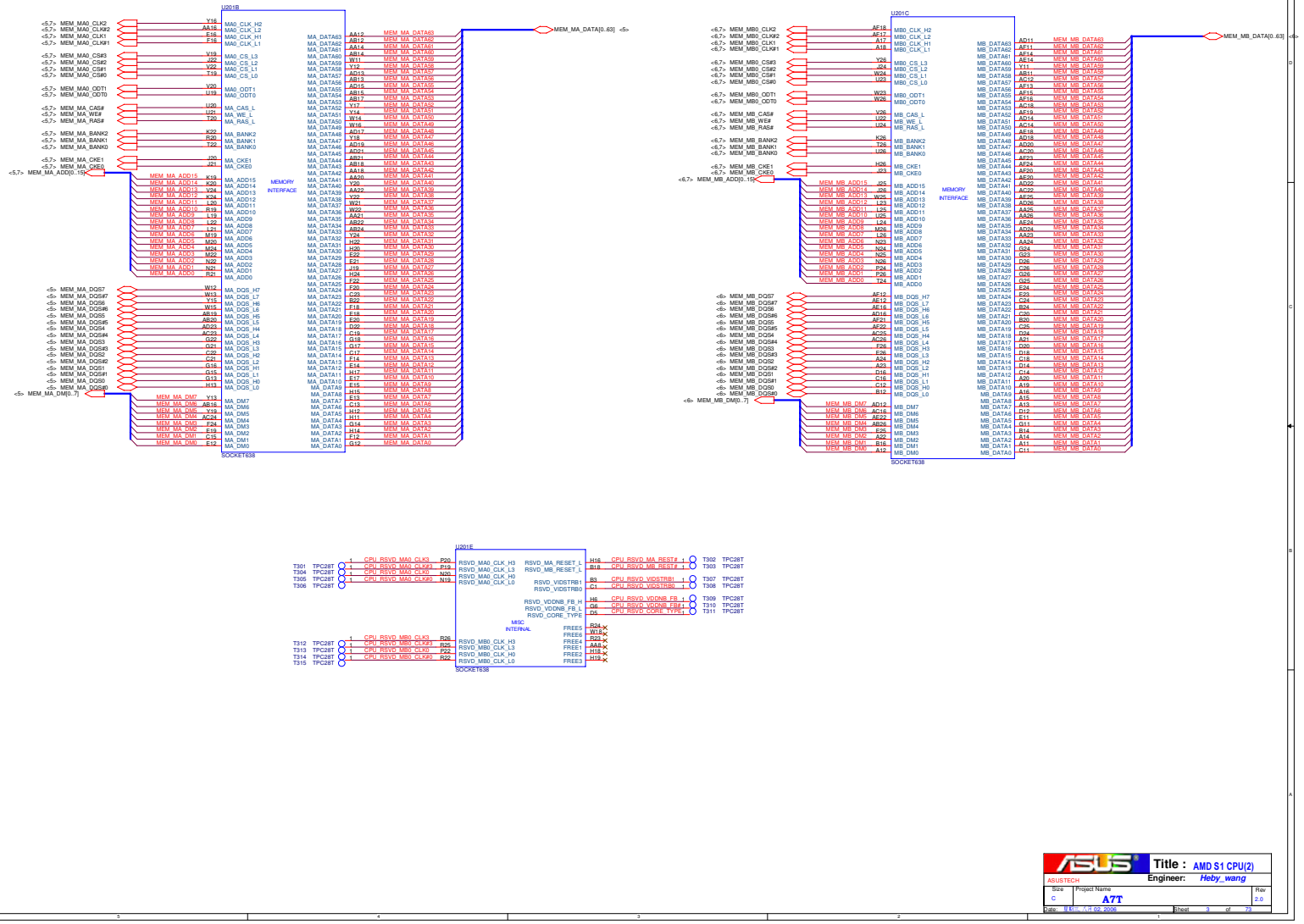
Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

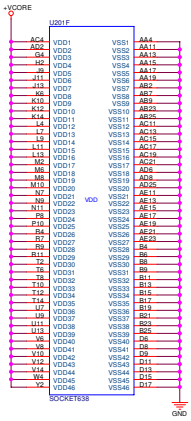
Date: 星期二, 四月 28, 2006 Sheet 1 of 73

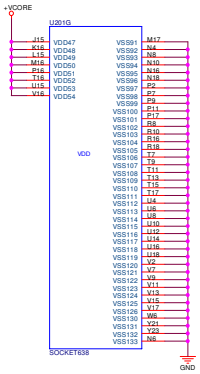


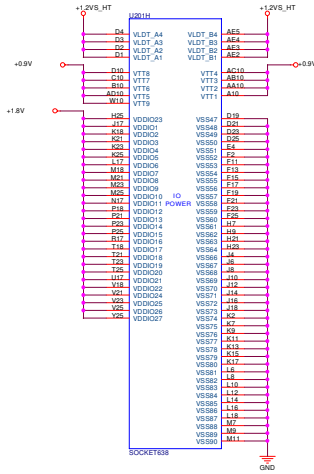
ASUSTECH	Title : AMD S1 CPU(1)		
	Engineer: Heby_wang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 2 of 79		

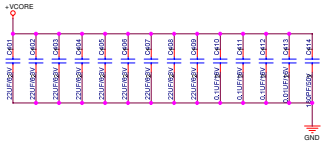


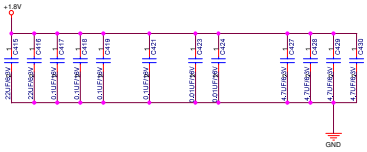
ASUSTECH	Title : AMD S1 CPU(2)		
	Engineer: Heby_wang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 3 of 79		

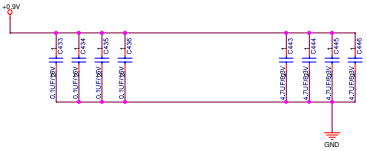


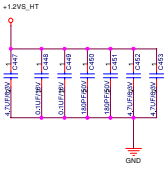












Title : AMD S1 CPU(3)

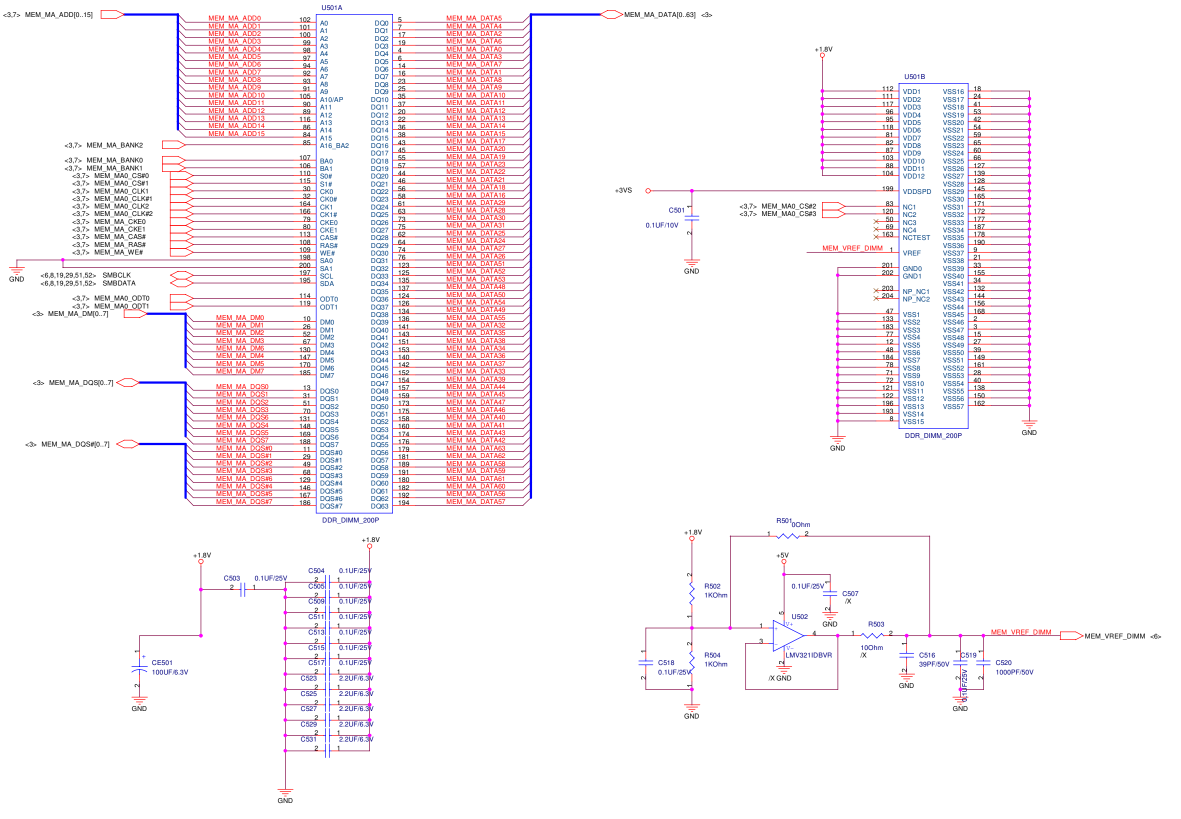
ASUSTECH

Engineer: Heby_wang

Size	Project Name	Rev
C	A7T	2.0

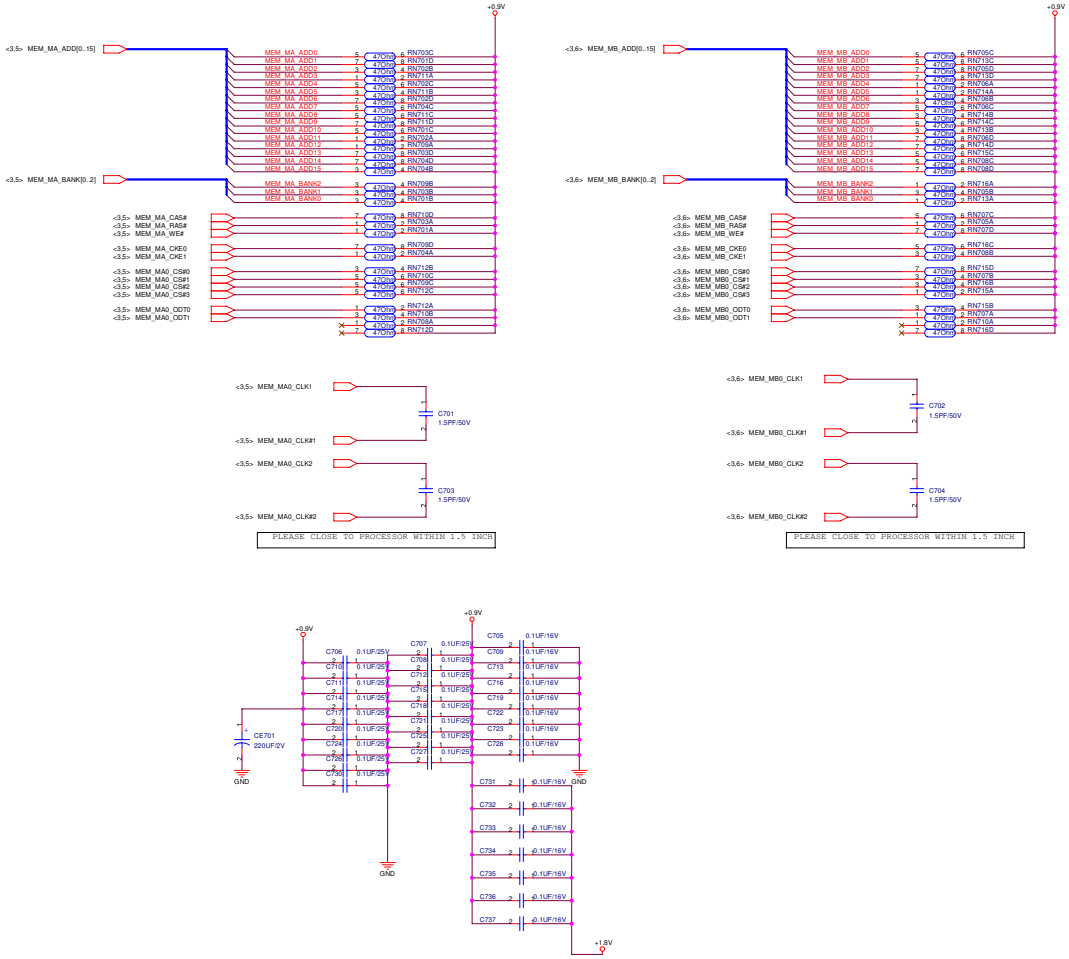
Date: 星期五, 四月 28, 2006 Sheet 4 of 79

TOP

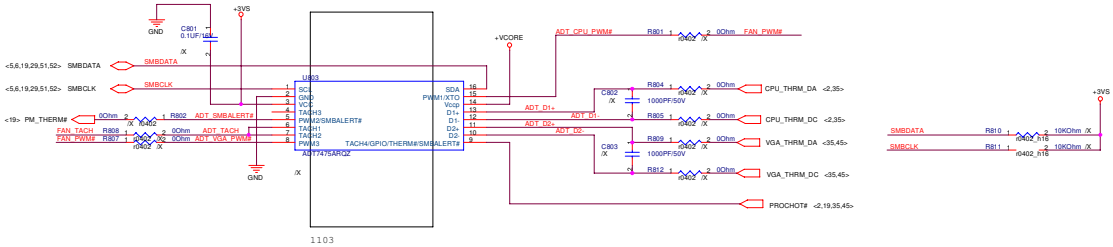


ASUSTECH	Title : DDR2_SO_DIMM(0)	
	Engineer: Heby_wang	
Size C	Project Name A7T	Rev 2.0
Date: 星期三, 八月 02, 2006	Sheet 5 of 73	

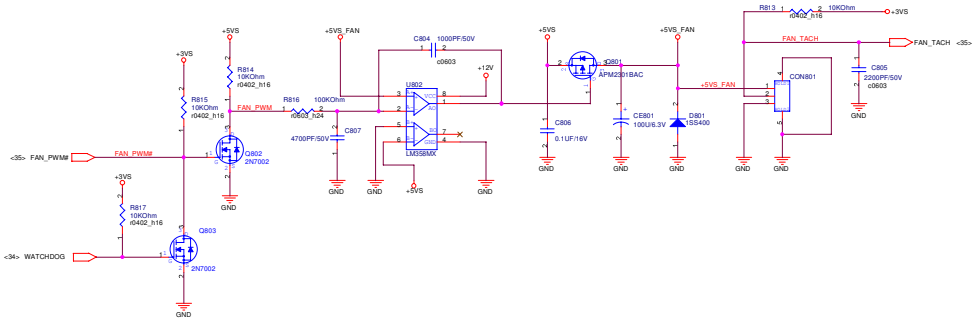
BOTTOM



ASUSTECH	Title : DDR2TERMINATIONS		
	Engineer: Heby_wang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期五, 四月 28, 2006	Sheet 7 of 79		



1103



Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pull-Up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E) (Default)

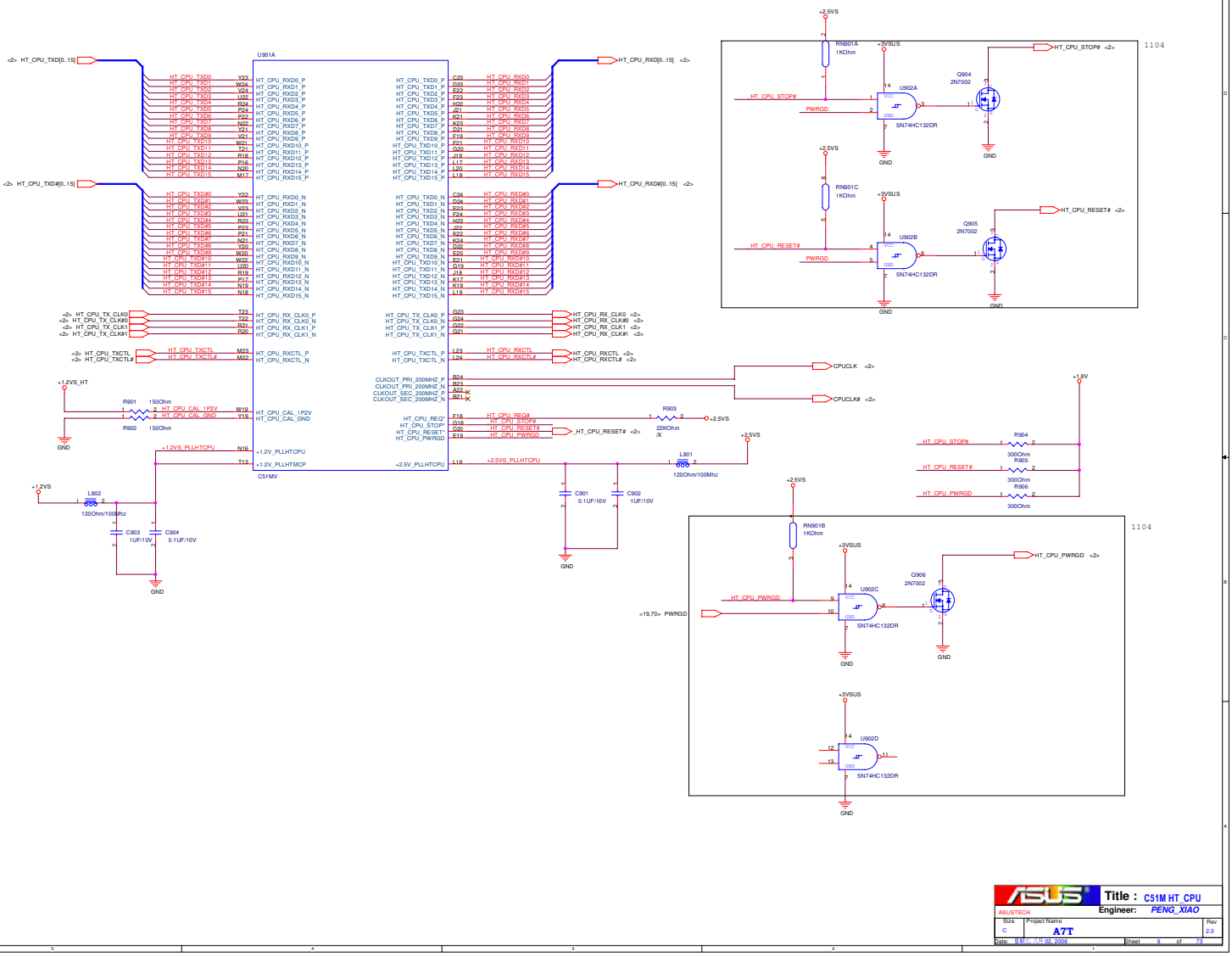
ASUSTECH

Title : THERMAL&FAN

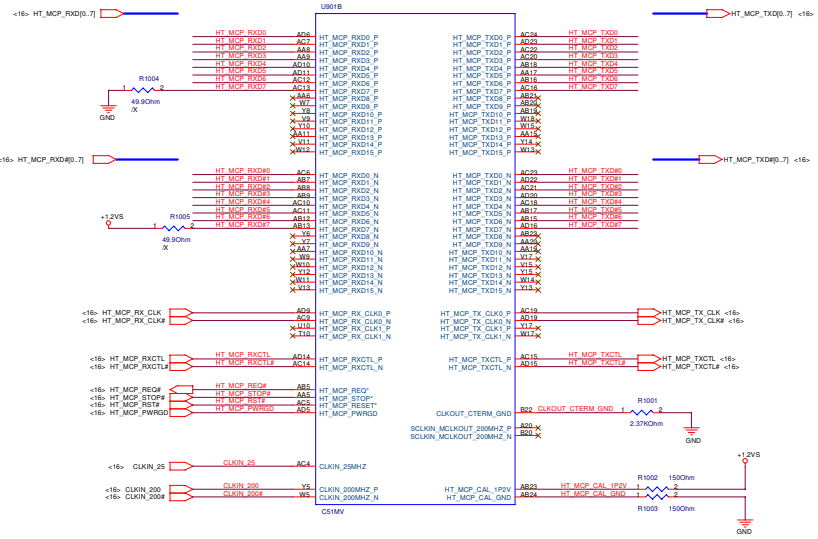
Engineer: Heby_wang

Size	Project Name	Rev
C	A7T	2.0

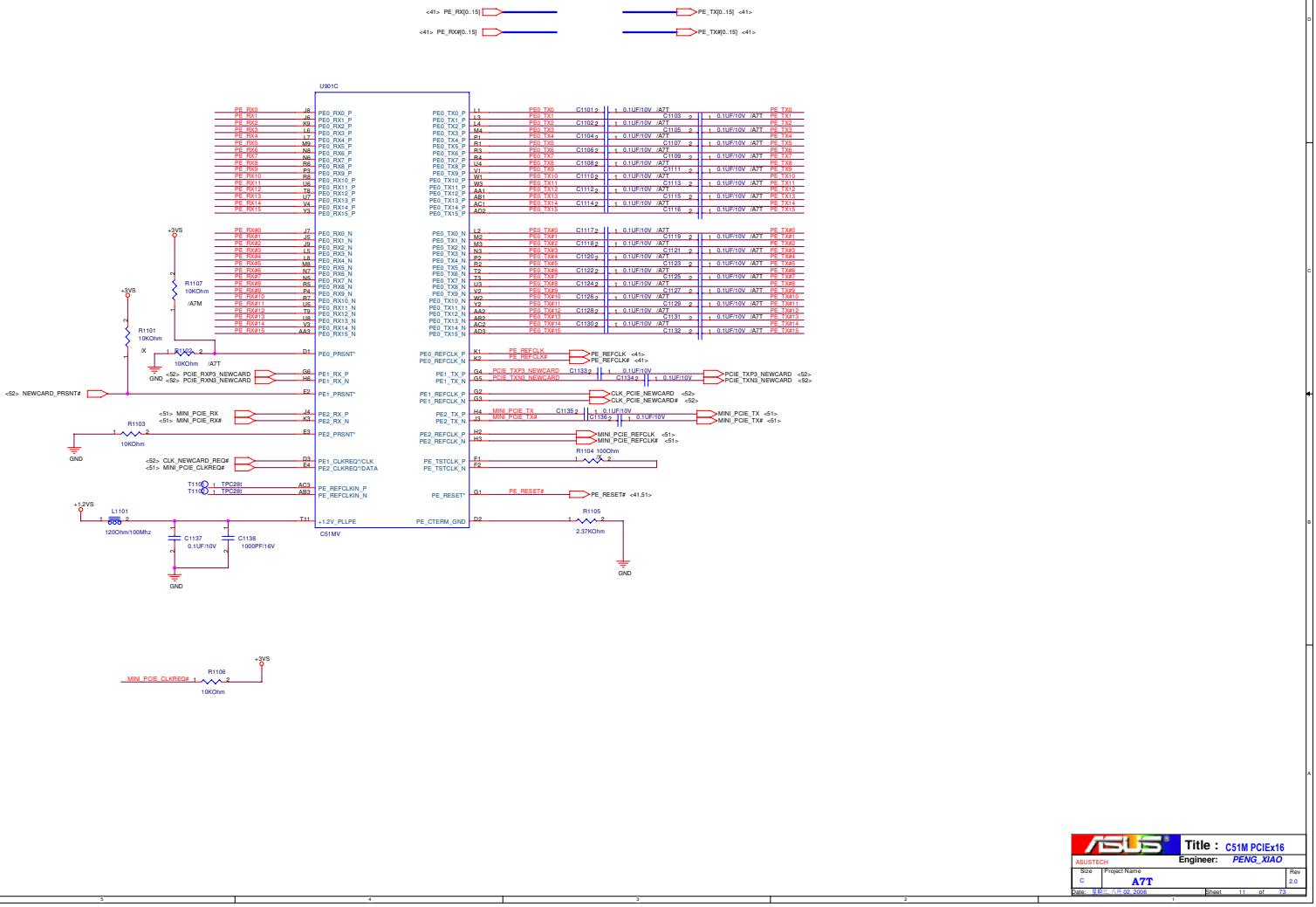
Date: 星期一, 八月 02, 2006 Sheet 8 of 79



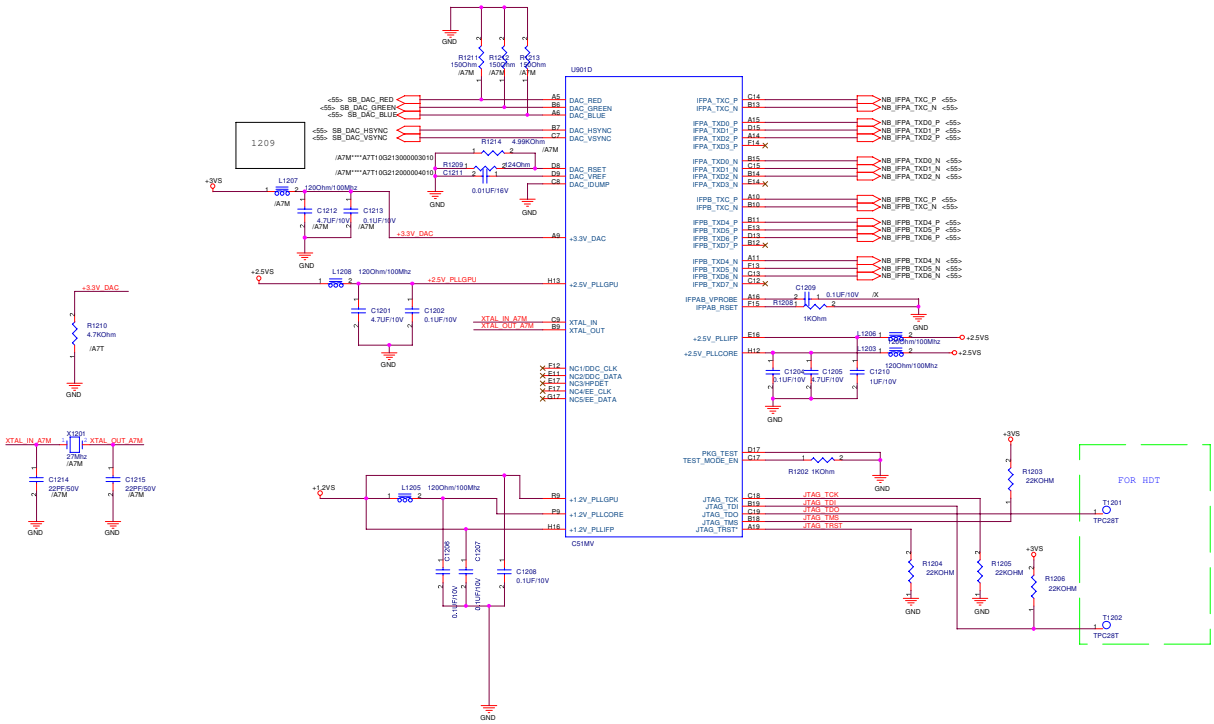
ASUSTECK	Title : C51M HT_CPU		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 9 of 73		



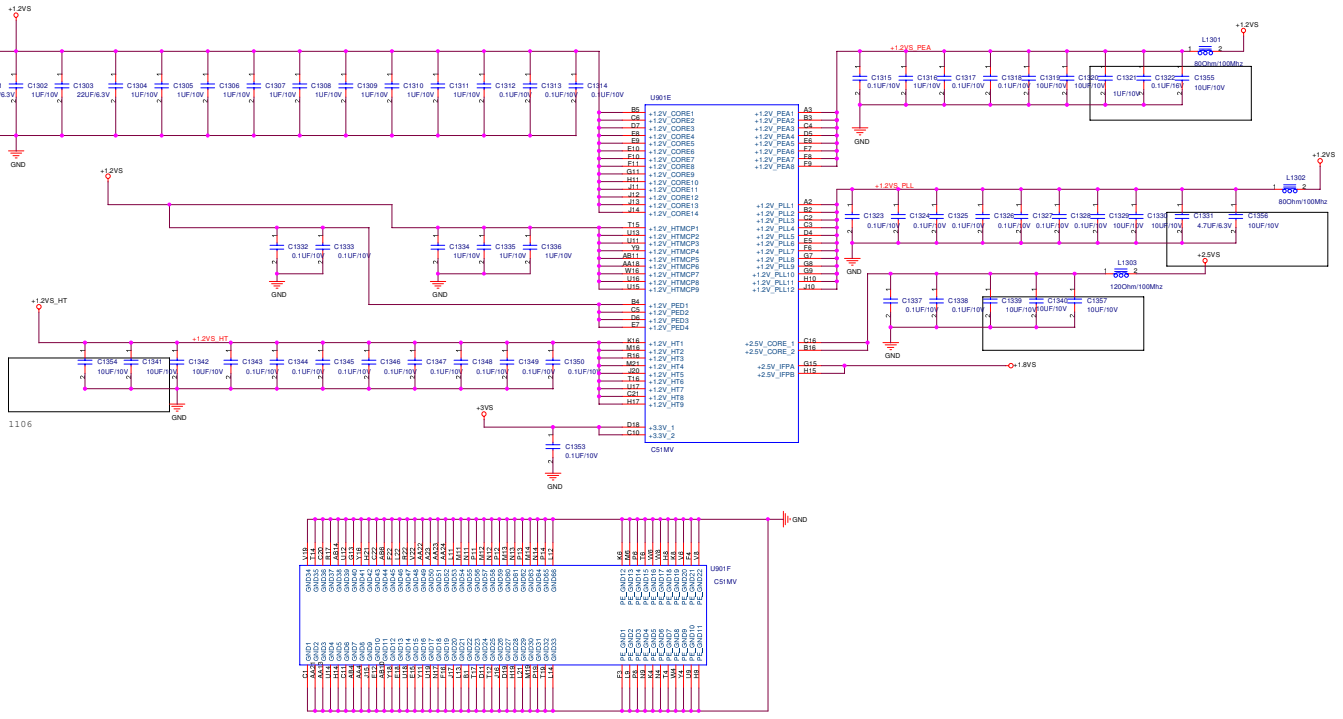
ASUSTeK	Title : C51 HT_MCP	
	Engineer: PENG_XIAO	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 10 of 73	



ASUSTeK	Title : C51M PCIEx16		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 11 of 29		



ASUSTECH	Title : C51M RGB&TV OUT		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期三, 四月 26, 2006	Sheet 12 of 29		



ASUSTeK	Title : C51M PWR&GND		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 四月 28, 2006	Sheet 13 of 73		

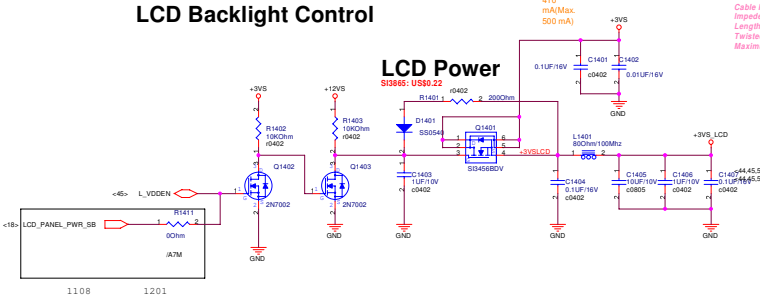
LCD Backlight Control

LCD Power

3-3.6V
S0-S1M:410 mA(500 mA Max.)

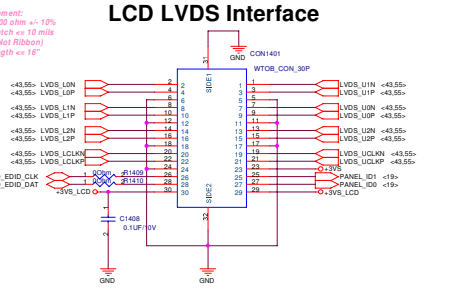
3V-3.6V
Full
Active:
410
mA(Max.
500 mA)

SI3865: US$0.22



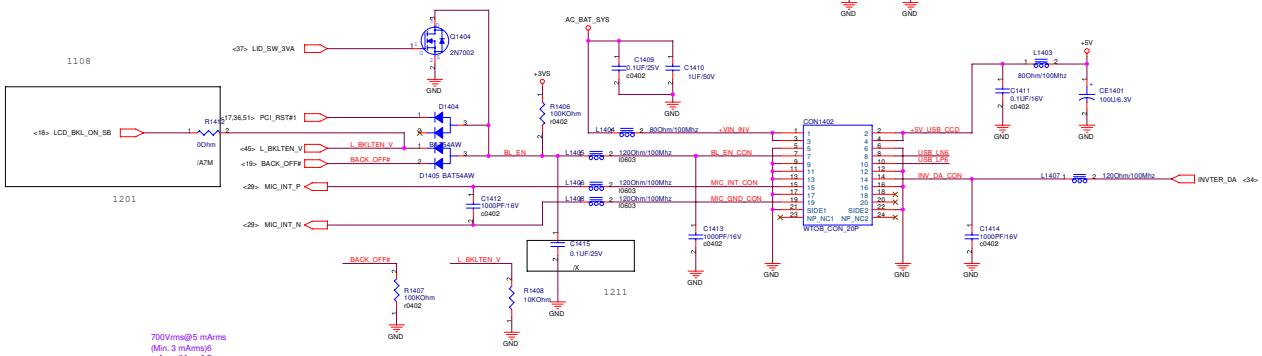
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 18"

LCD LVDS Interface



INVERTER Interface

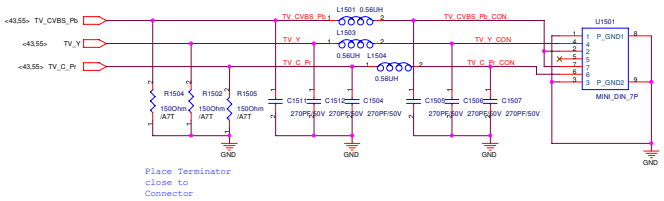
BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.



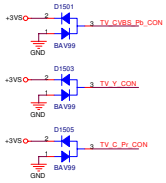
700Vrms@5 mArms
(Min. 3 mArms)6
mArms(Max. 6.5
mArms)

ASUSTeK	Title : LVDS CONNECTER		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006		Sheet 14 of 29	

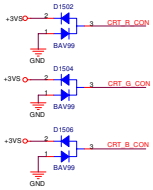
TV OUT



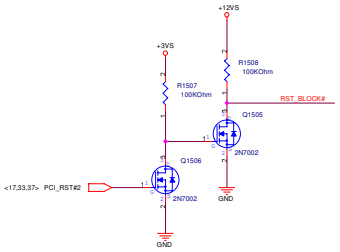
Place Terminator close to Connector

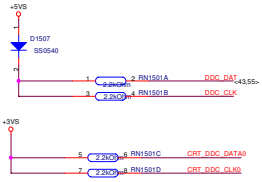


PLACE ESD Diodes near TV port



PLACE ESD Diodes near VGA port

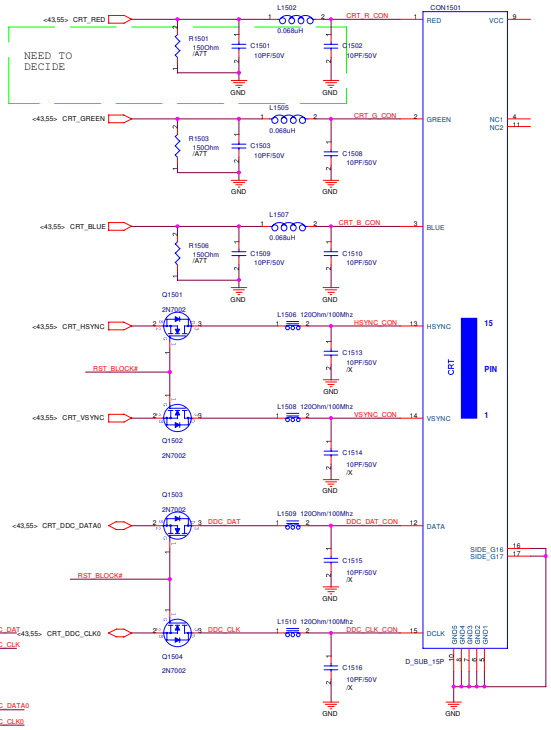




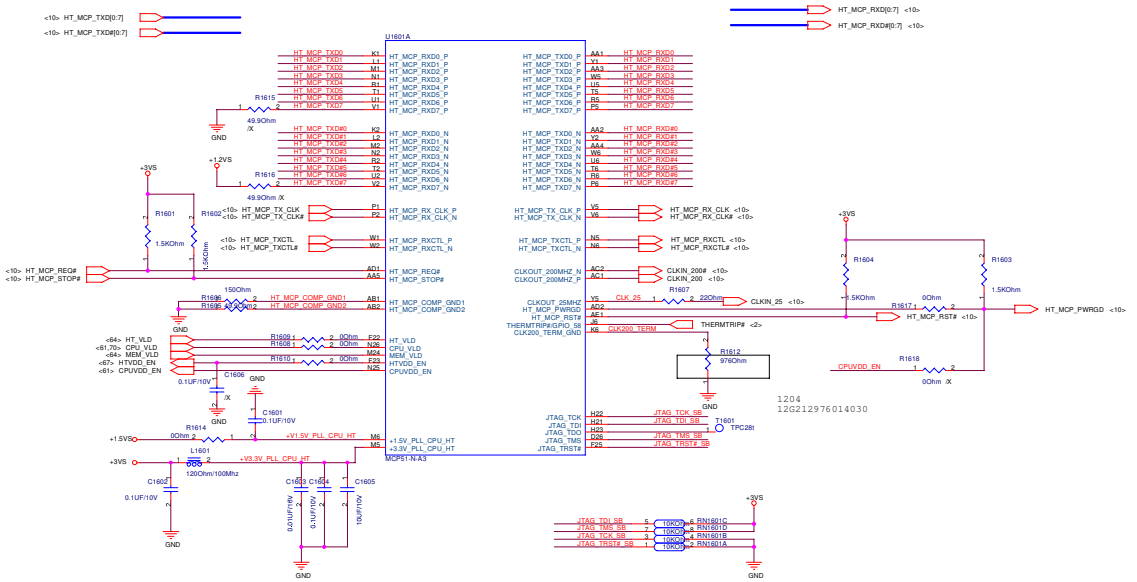
CRT OUT

1208

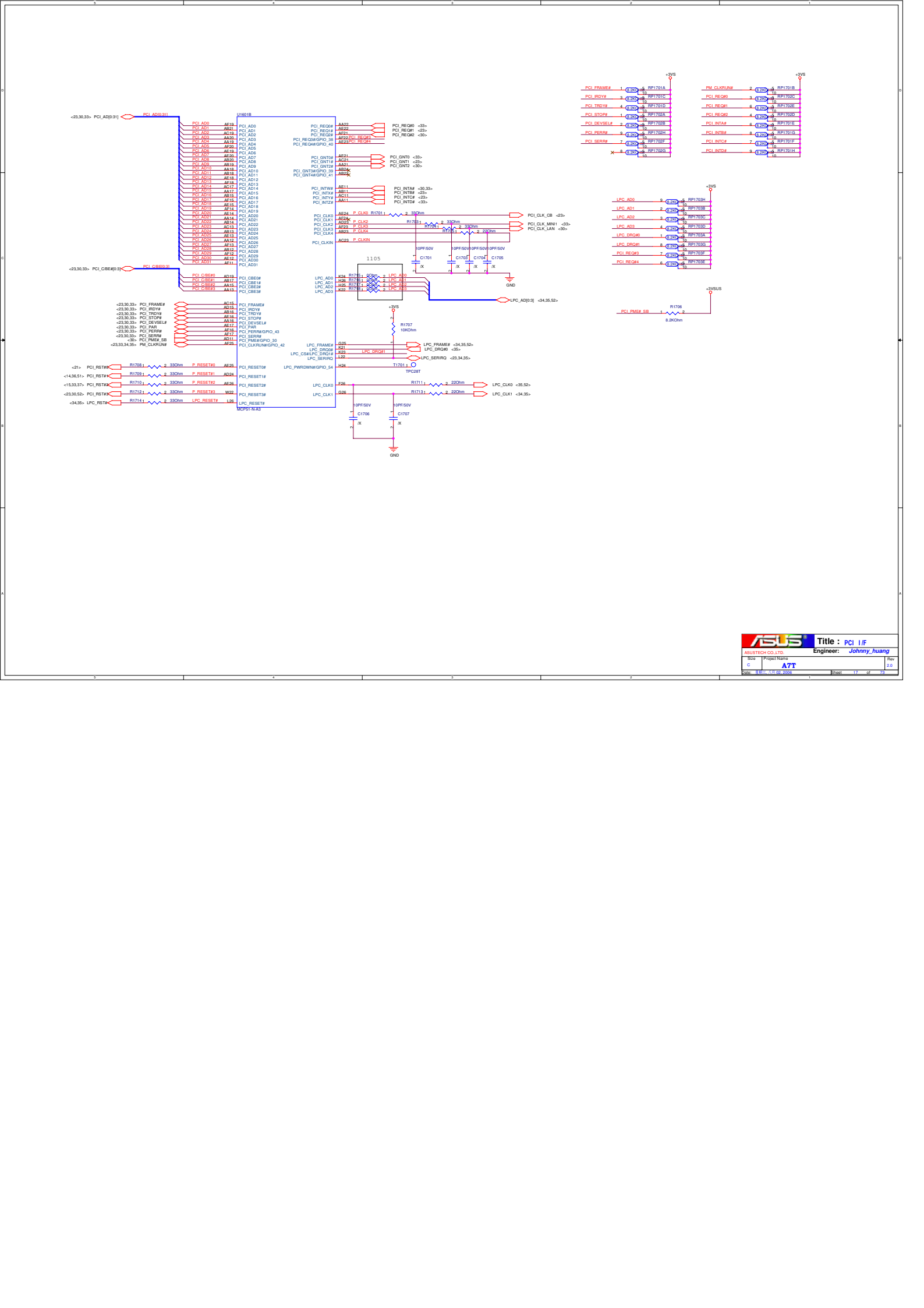
NEED TO DECIDE



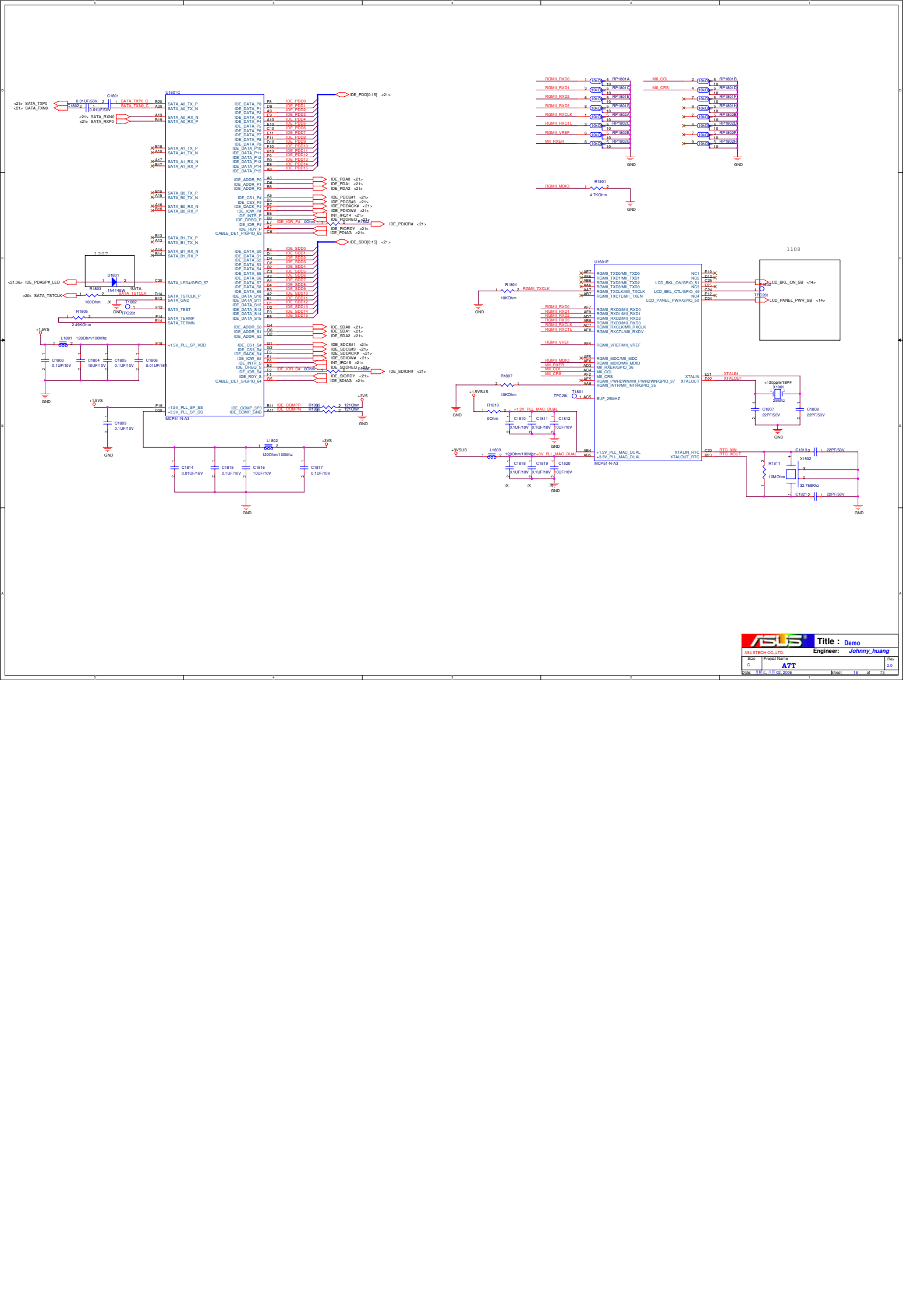
ASUSTECH	Title : CRT TV CONNECTER		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: Fri, Jul 04, 2006		Sheet 15 of 73	



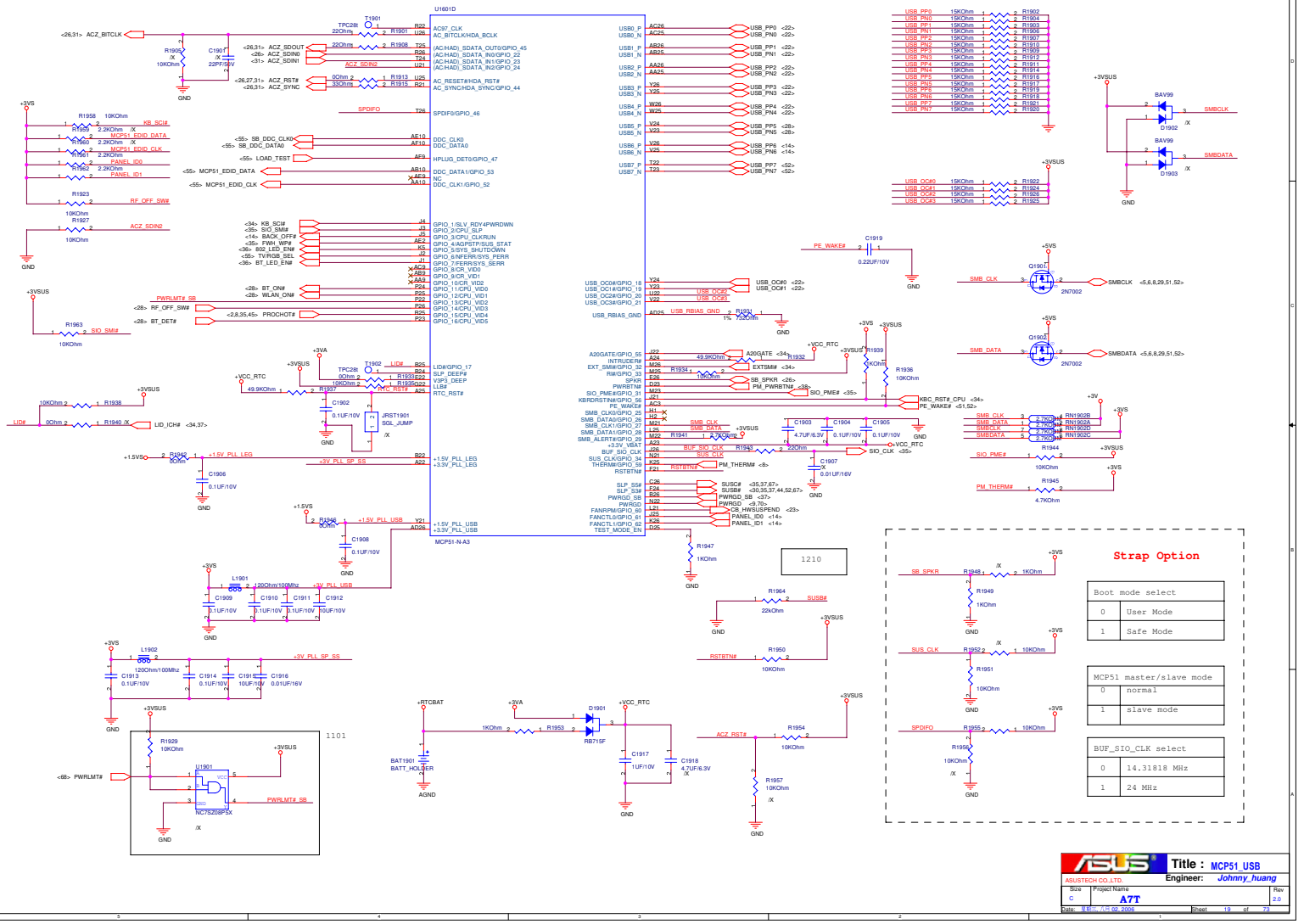
ASUSTECH CO.,LTD	Title : SB_HT_I/F		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 四月 28, 2009	Sheet 18 of 73		

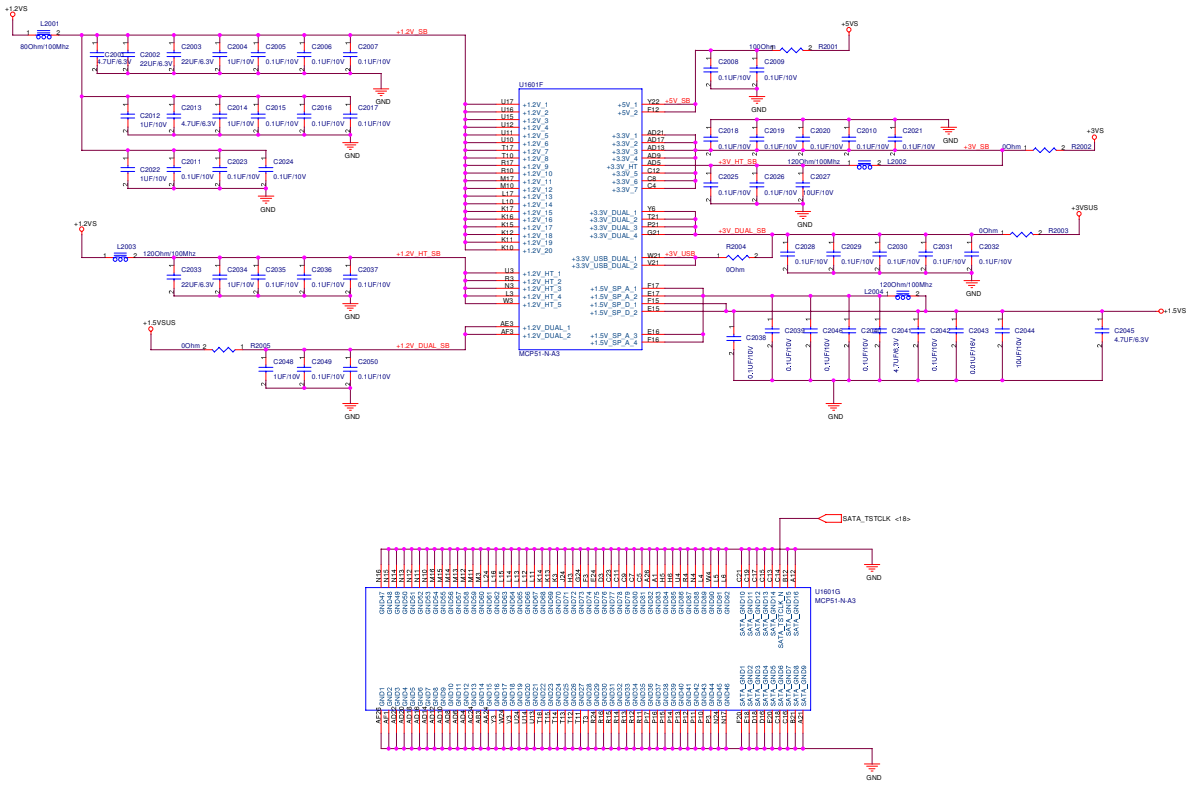


ASUSTECH CO.,LTD	Title : PCI I/F		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 17 of 73		



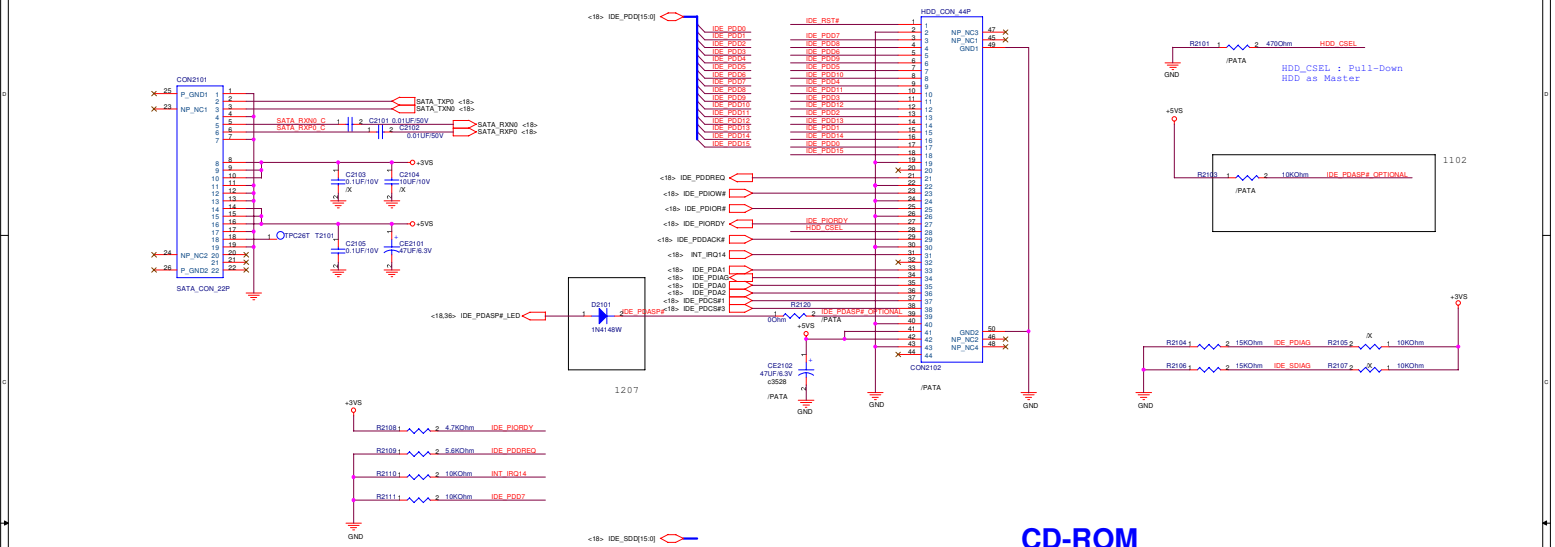
ASUSTeK COMPUTER INC.	Title : Demo		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 18 of 73		


U1601D
MCP51-N-A3
Strap Option
Boot mode select
0 User Mode
1 Safe Mode
MCP51 master/slave mode
0 normal
1 slave mode
BUF_SIO_CLK select
0 14.31818 MHz
1 24 MHz
Title : MCP51_USB
ASUSTeK COMPUTER INC.
Engineer: Johnny_huang
Size: C
Project Name: A7T
Rev: 2.0
Date: 星期二, 八月 02, 2006
Sheet 19 of 29

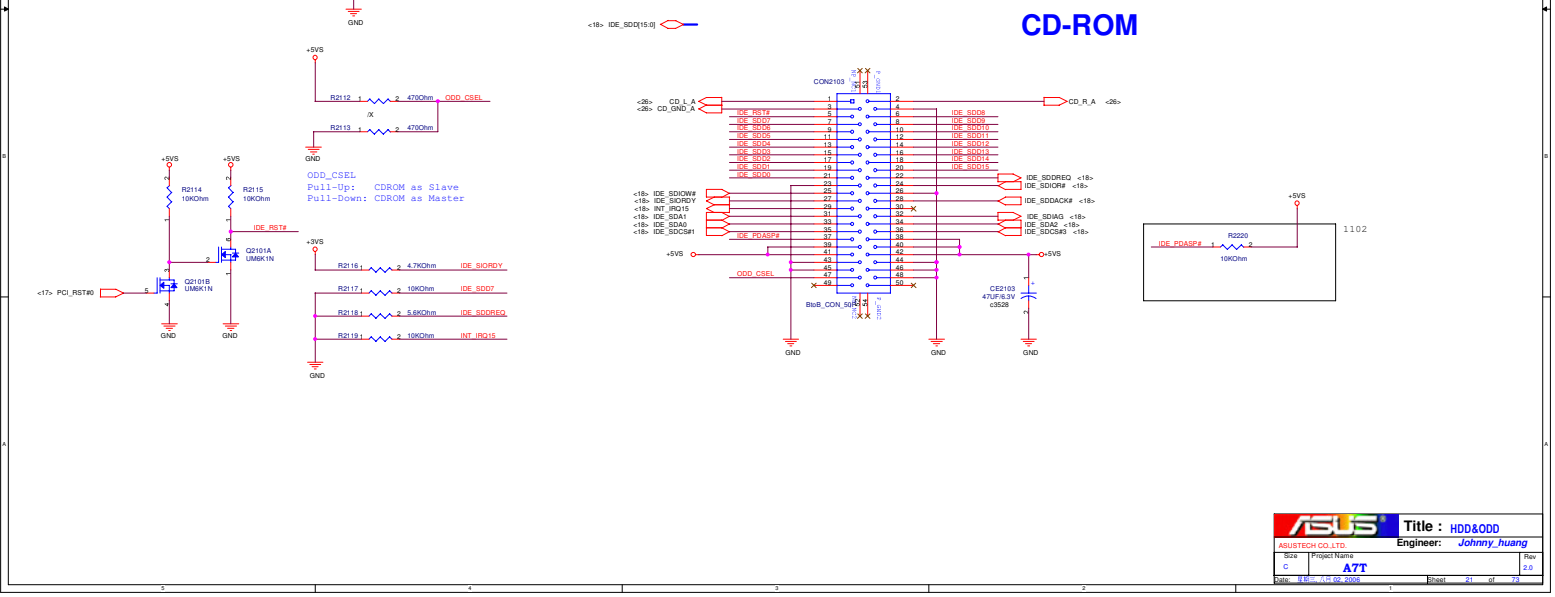


ASUSTECH CO.,LTD	Title : MCP51_PWR		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 20 of 73		

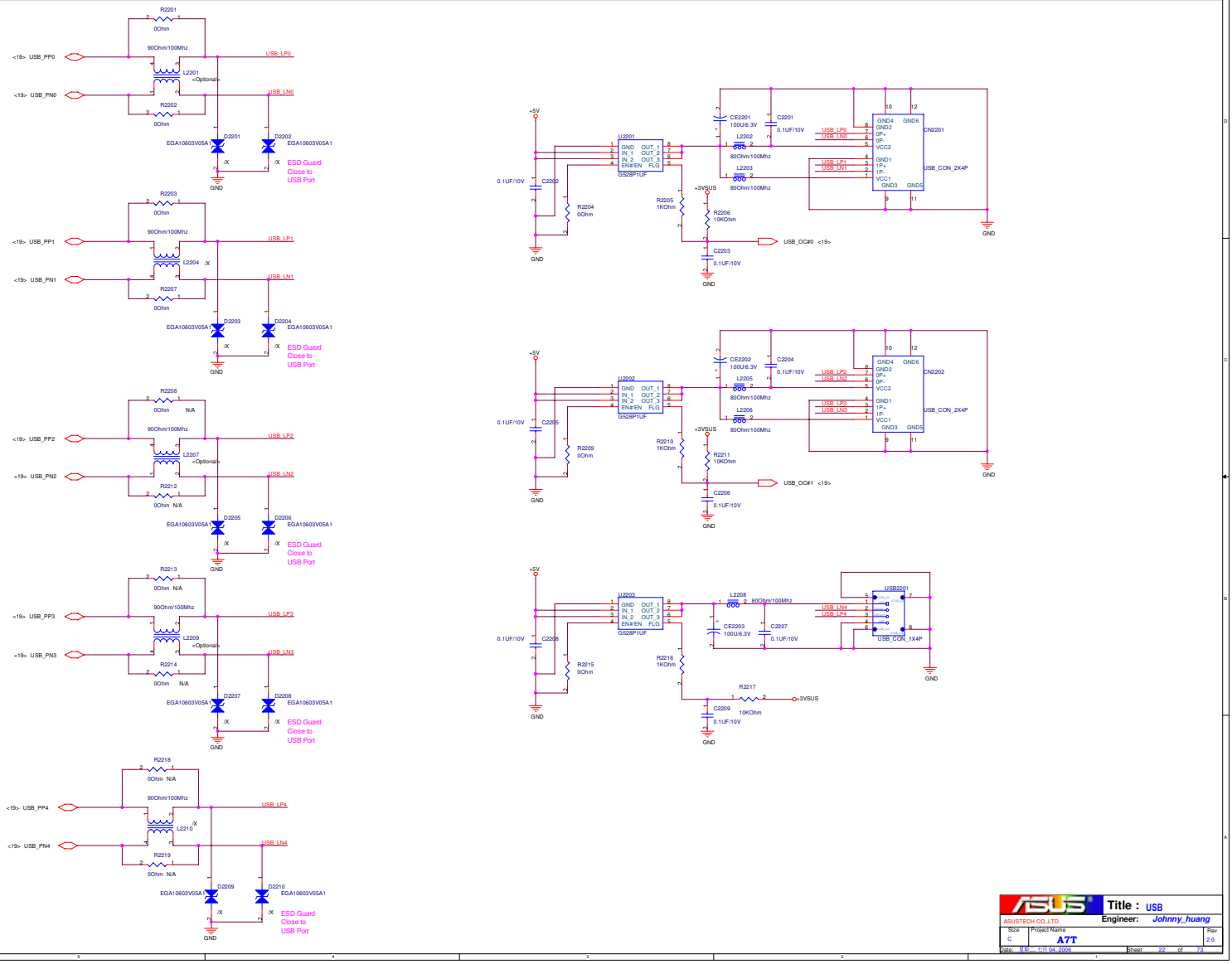
HDD



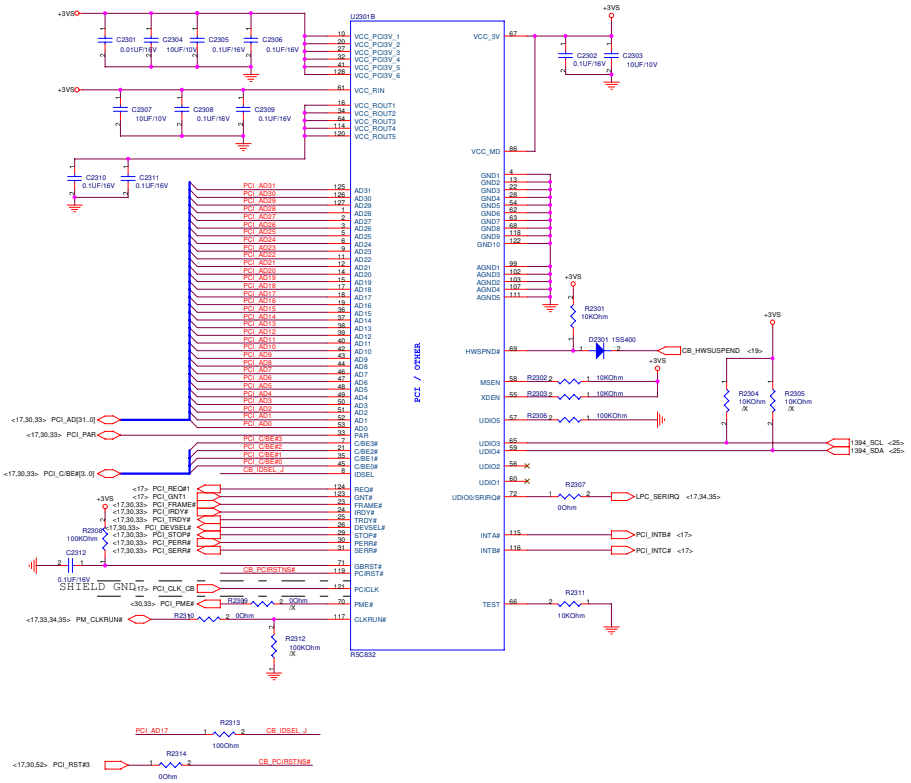
CD-ROM



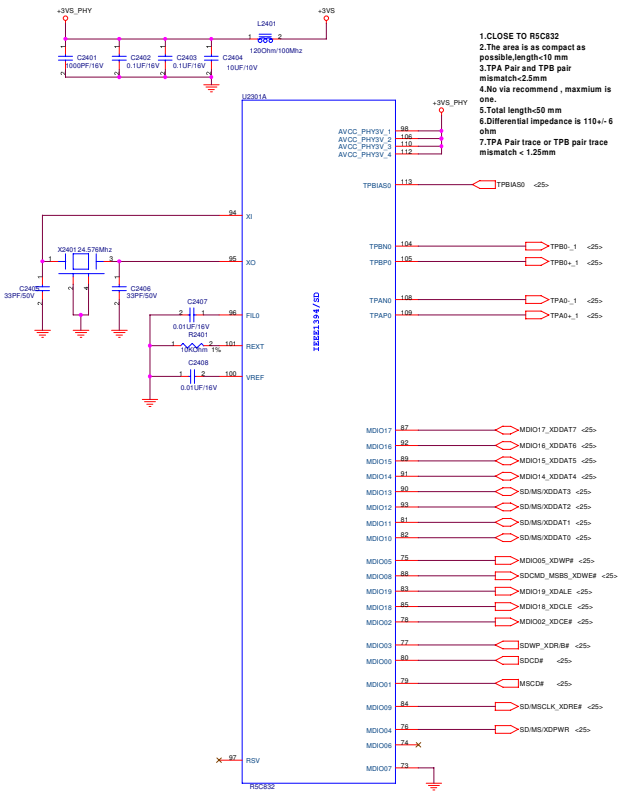
ASUSTECH COMPUTER INC.	Title : HDD&ODD		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 六月 02, 2006	Sheet 21 of 73		



ASUSTECH CO.,LTD	Title : USB	
	Engineer: Johnny_huang	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期二, 十月 04, 2005	Sheet 22 of 73	



ASUSTEK	Title : R5C832_1		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 23 of 73		



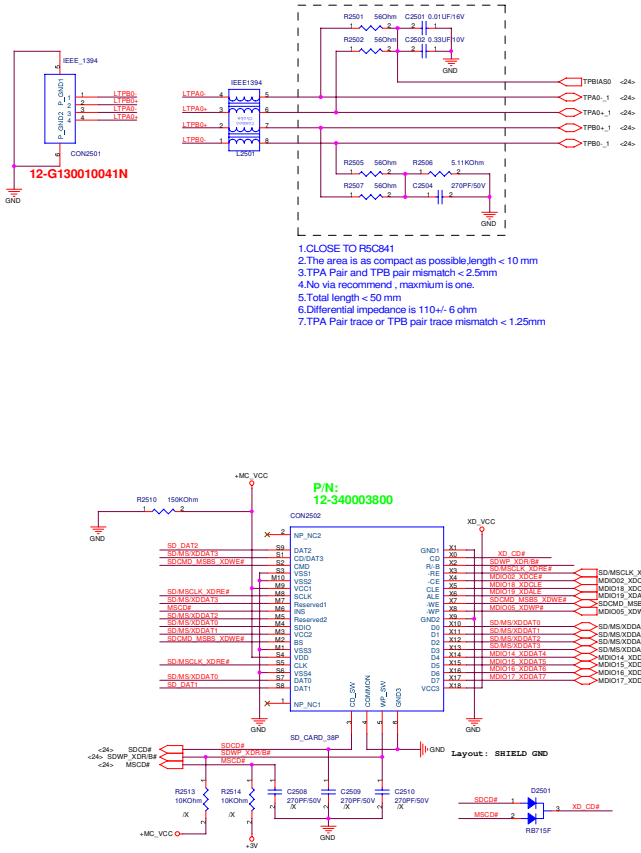
ASUSTEK

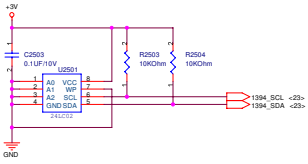
Title : R5C832_2

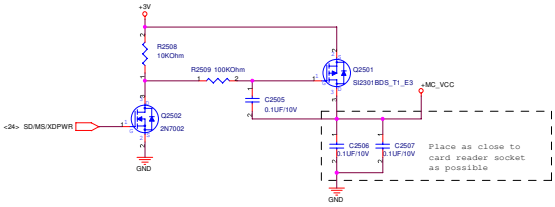
Engineer: echo_xing

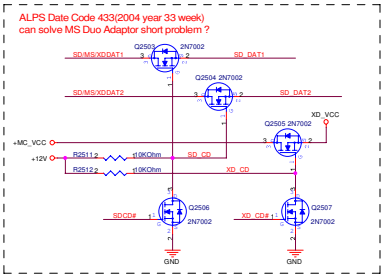
Size	Project Name	Rev
C	A7T	2.0

Date: 星期二, 八月 02, 2006 Sheet 24 of 73

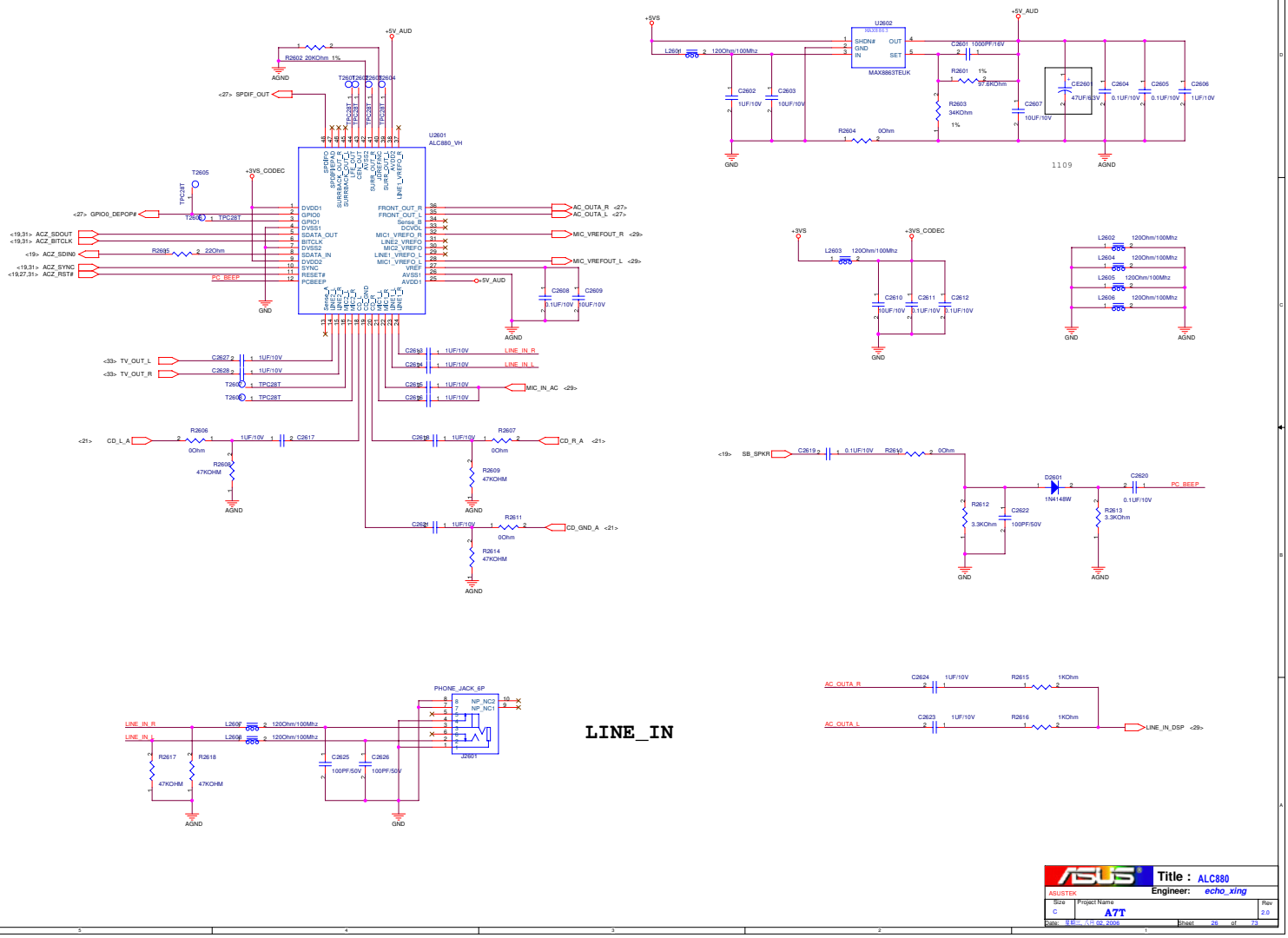








ASUSTEK	Title : 1394&IN 1 CON		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 15, 2006	Sheet 25 of 73		

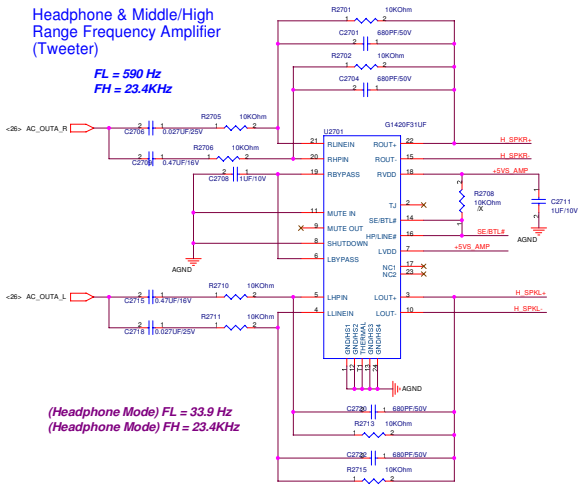


LINE_IN

ASUSTEK	Title : ALC880		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 28 of 73		

Headphone & Middle/High Range Frequency Amplifier (Tweeter)

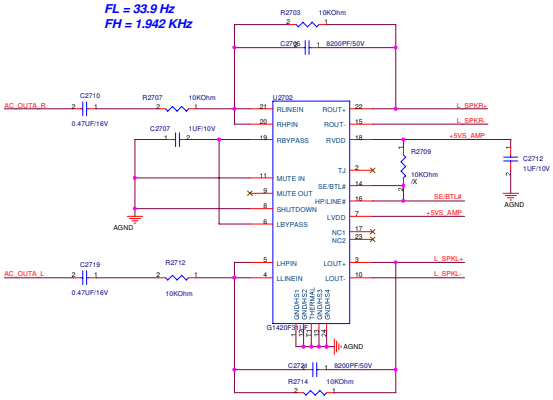
FL = 590 Hz
FH = 23.4KHz

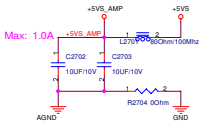


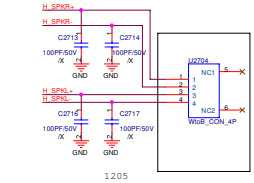
(Headphone Mode) FL = 33.9 Hz
(Headphone Mode) FH = 23.4KHz

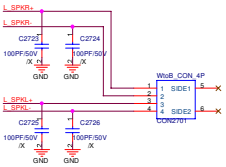
Low Range Frequency Amplifier (Woofer)

FL = 33.9 Hz
FH = 1.942 KHz

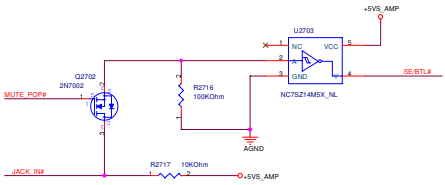


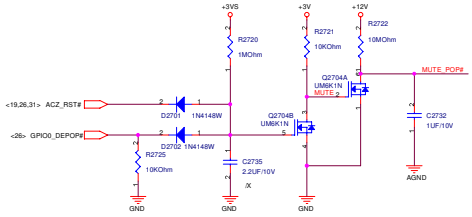




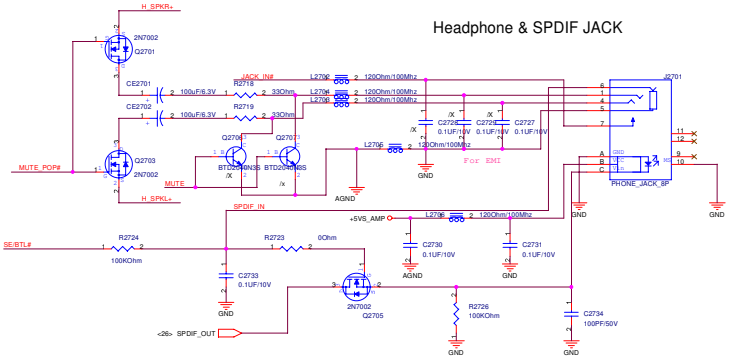


	SE/BTL#	SPDIF_IN
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X



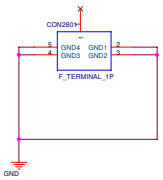


Headphone & SPDIF JACK



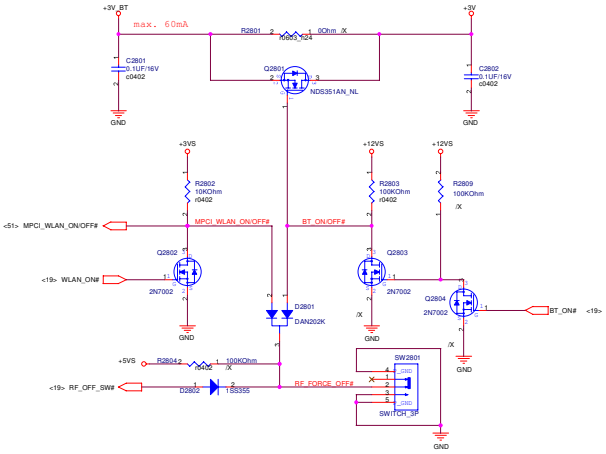
ASUSTEK	Title : AMP			
	Engineer: echo_xing			
Size: C	Project Name: A7T			Rev: 2.0
Date: 星期二, 六月 02, 2006			Sheet 27 of 73	

ATV_DTV_FM Antenna

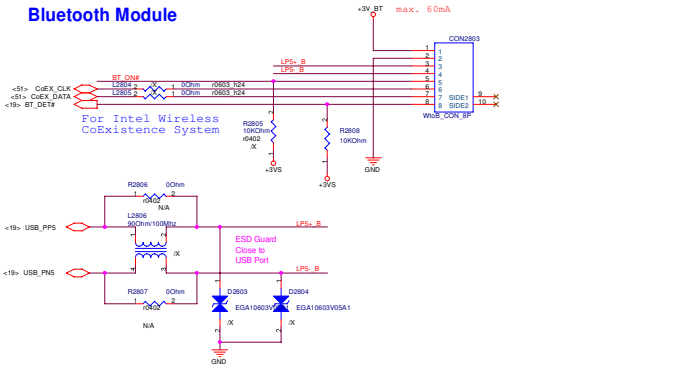


14G152075000

WLAN/BT ON/OFF Control

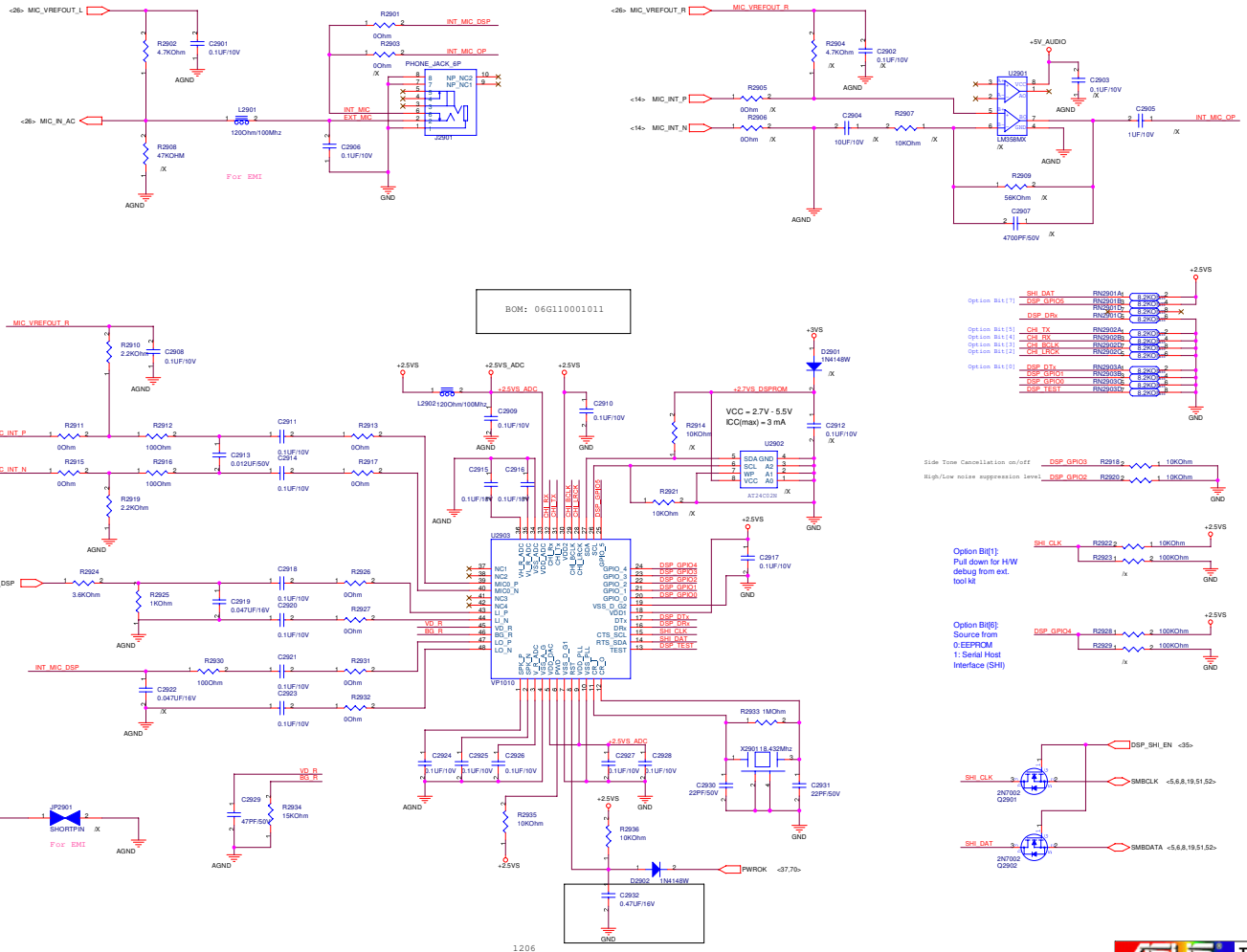


Bluetooth Module



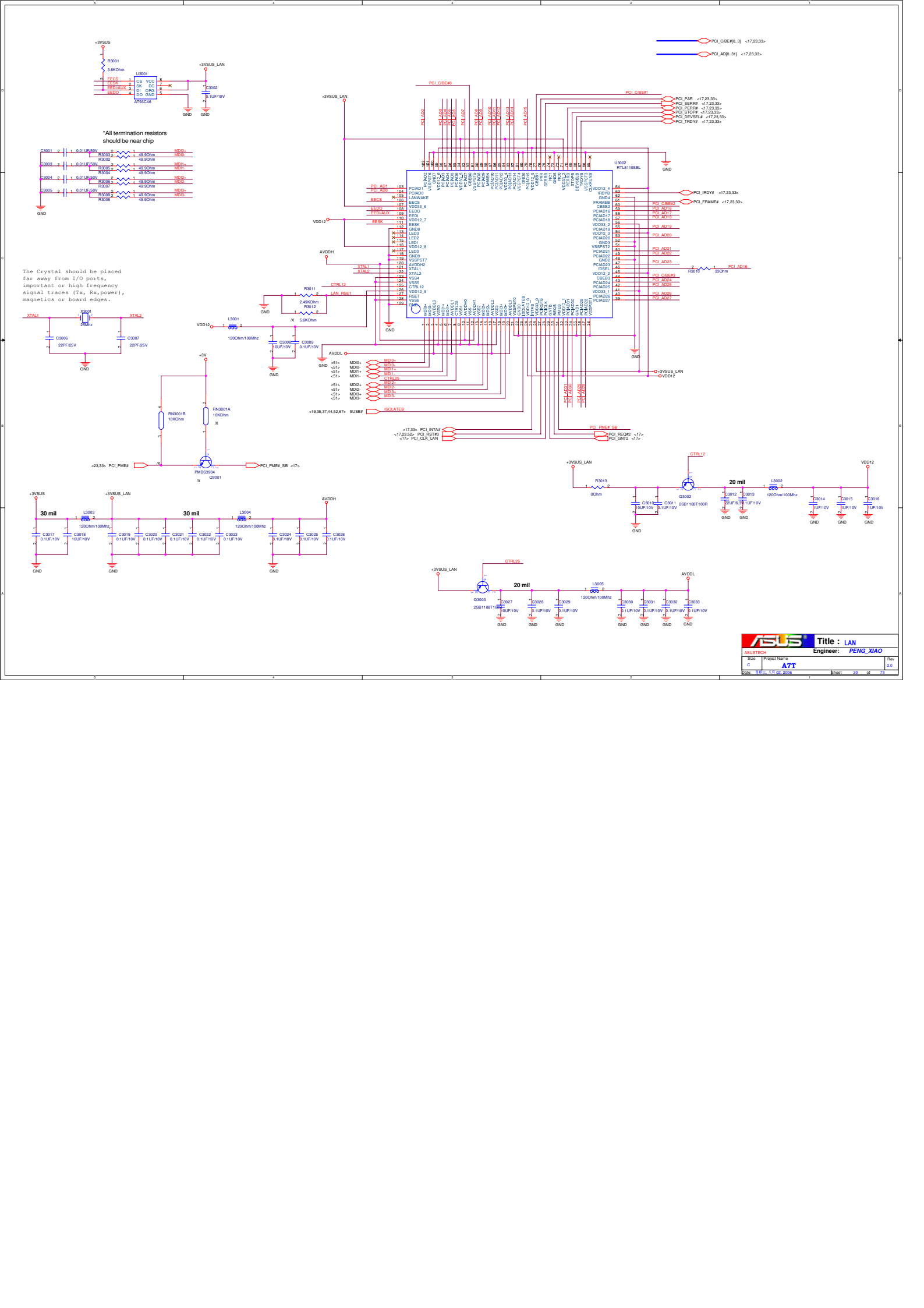
ASUSTeK	Title : BT/RF		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 28 of 73		

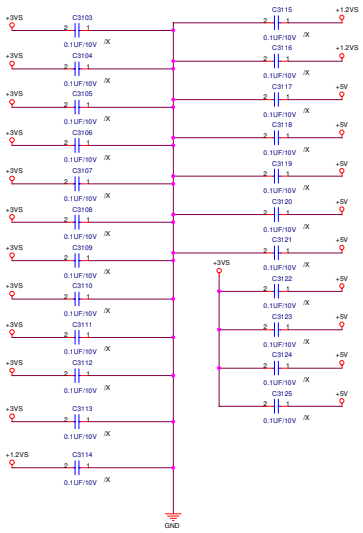
FL = TBD
FH = TBD Internal MIC Pre-Amplifier



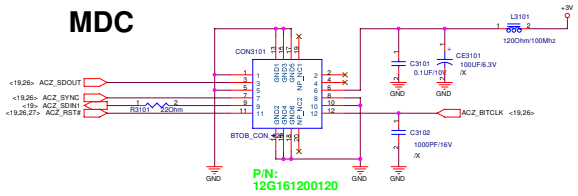
1206

ASUSTEK	Title : VOICE DSP		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 六 02, 2006	Sheet 29 of 73		

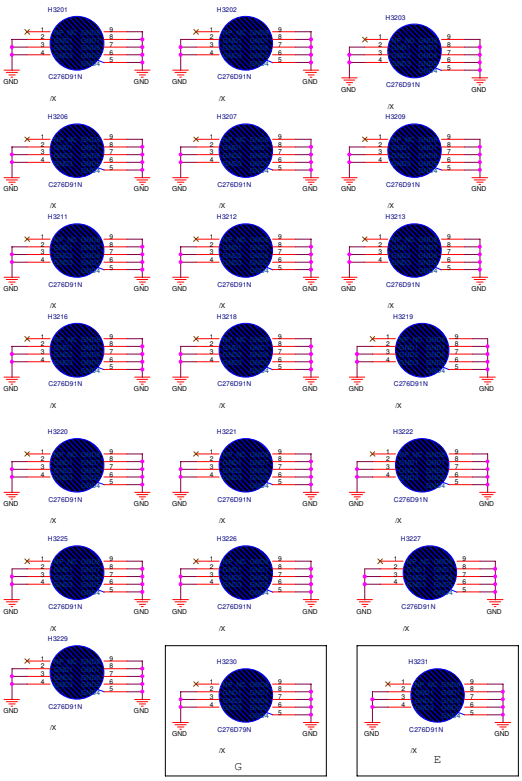

*All termination resistors should be near chip
The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx,power), magnetics or board edges.
U3002 RTL8110SBL
U3001 AT93C46
Q3001 PMBS3904
Q3002 2SB1188T100R
Q3003 2SB1188T100R
PCI_C/BE#[0..3] <17,23,33>
PCI_AD[0..31] <17,23,33>
Title : LAN
Engineer: PENG_XIAO
ASUSTeK
Size C
Project Name A7T
Rev 2.0
Date: 星期二, 八月 02, 2006
Sheet 30 of 73

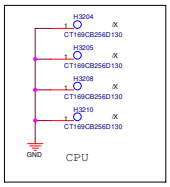


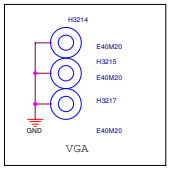
MDC

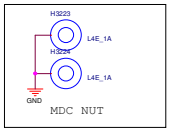


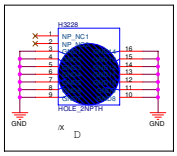
ASUSTECH	Title : MDC		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 31 of 73		



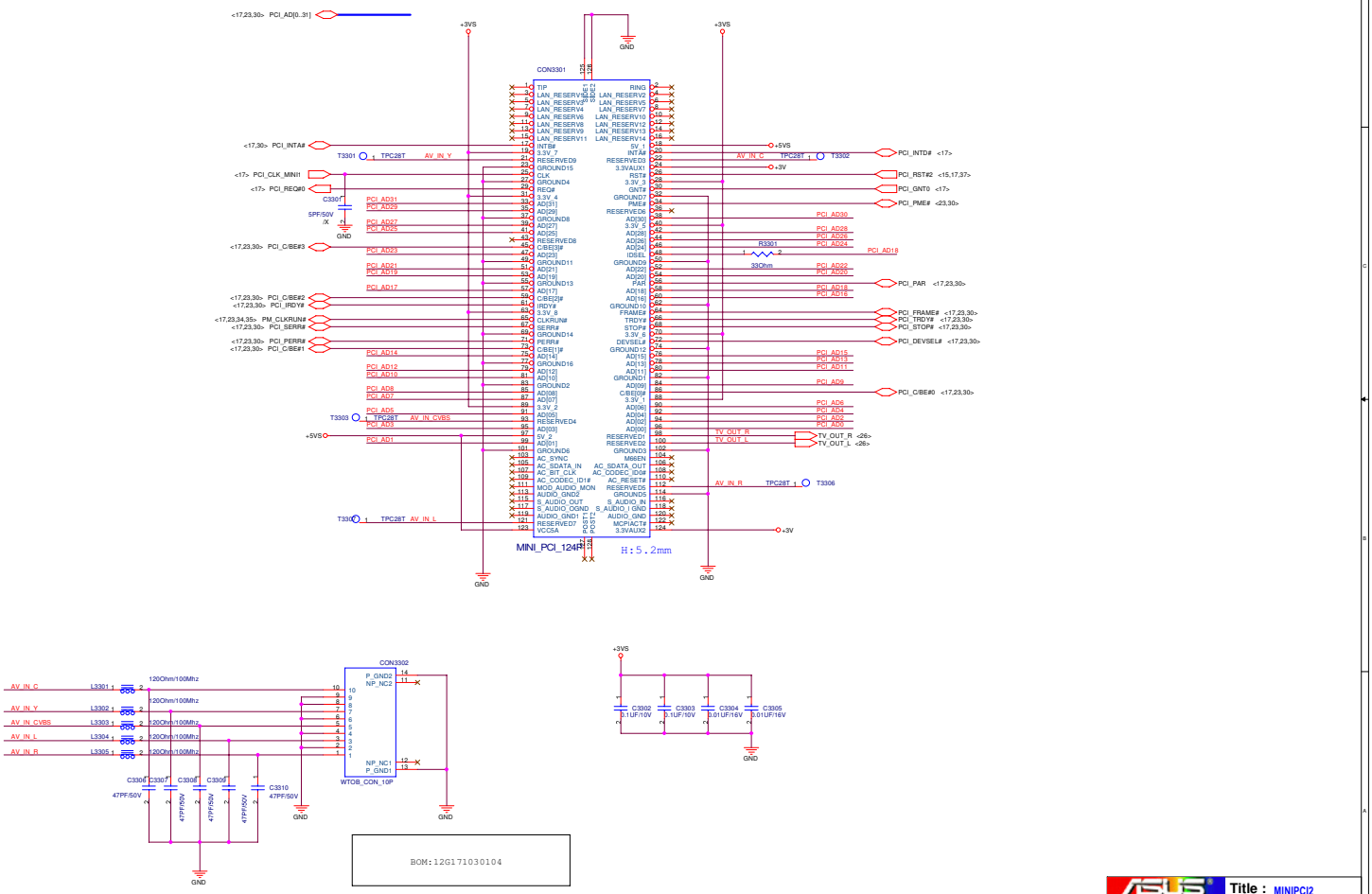






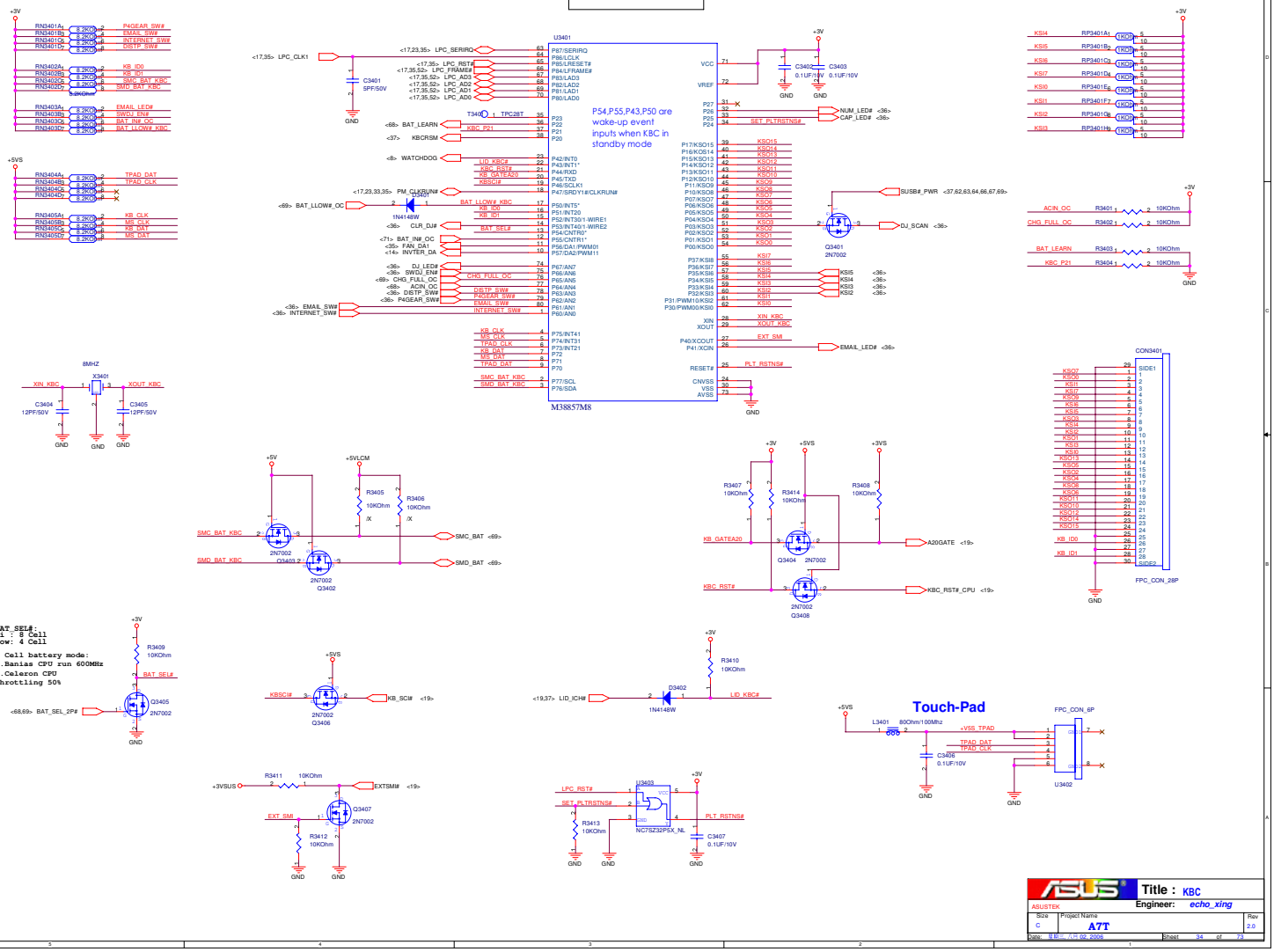


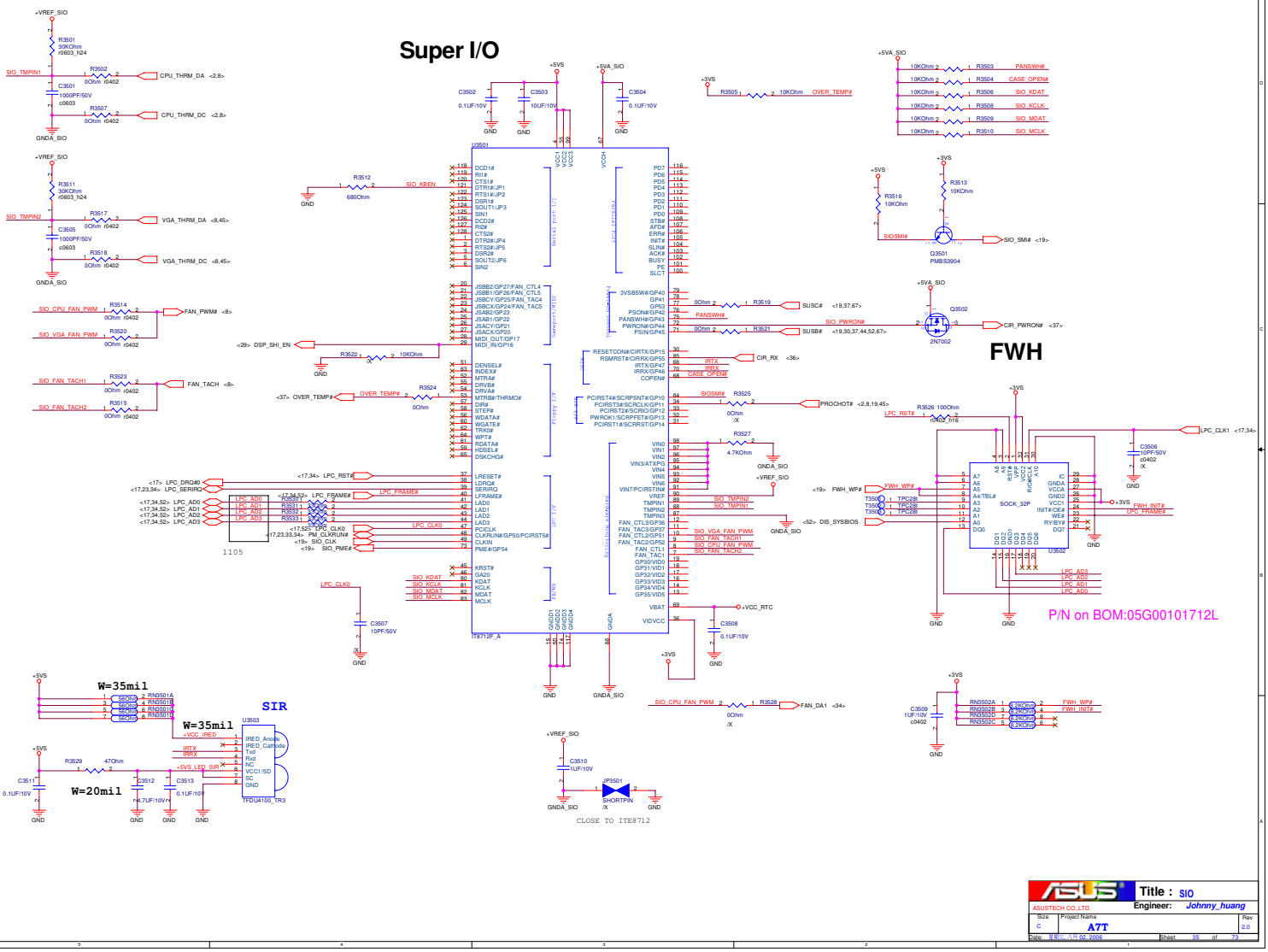
ASUSTEK	Title : Screw Hole		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 32 of 73		



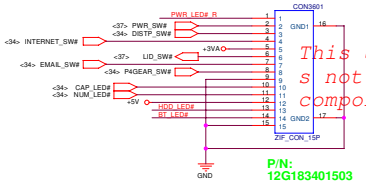
ASUSTEK	Title : MINIPCI2		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 33 of 73		

TYPE	JP	UK	US
KID0	L	L	H
KID1	L	H	H




Super I/O
FWH
P/N on BOM:05G00101712L
SIR
W=35mil
W=20mil
CLOSE TO ITE8712
1105
Title : SIO
ASUSTECH CO.,LTD
Engineer: Johnny_huang
Project Name
A7T
Rev
2.0
Sheet 35 of 73

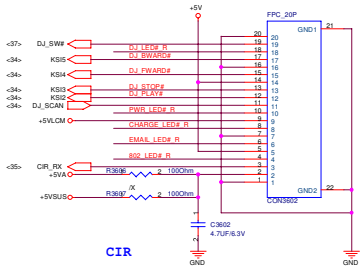
Launch Board Conn.



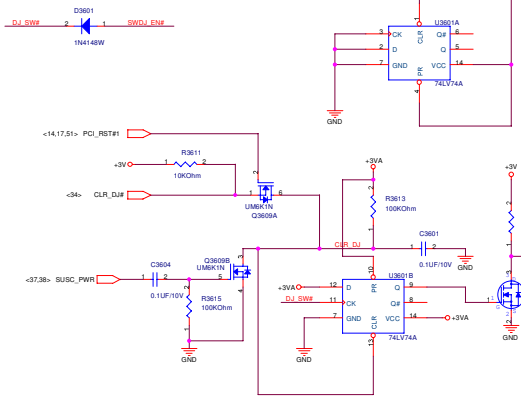
This JACK is not GREEN component

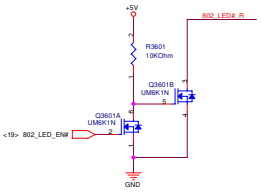
P/N:
12G183401503

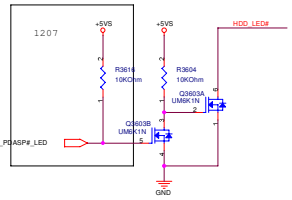
DJ Board Conn.

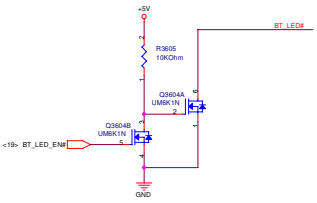


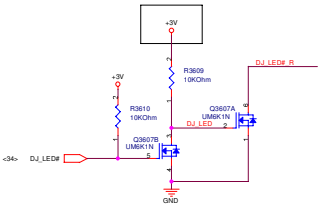
CIR

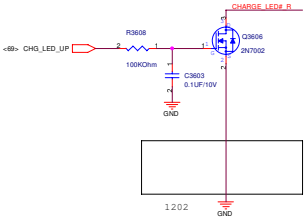


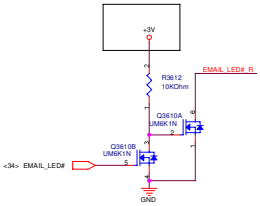


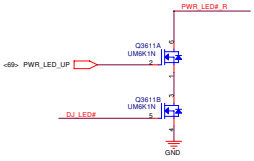


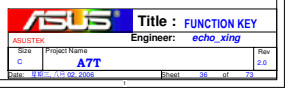


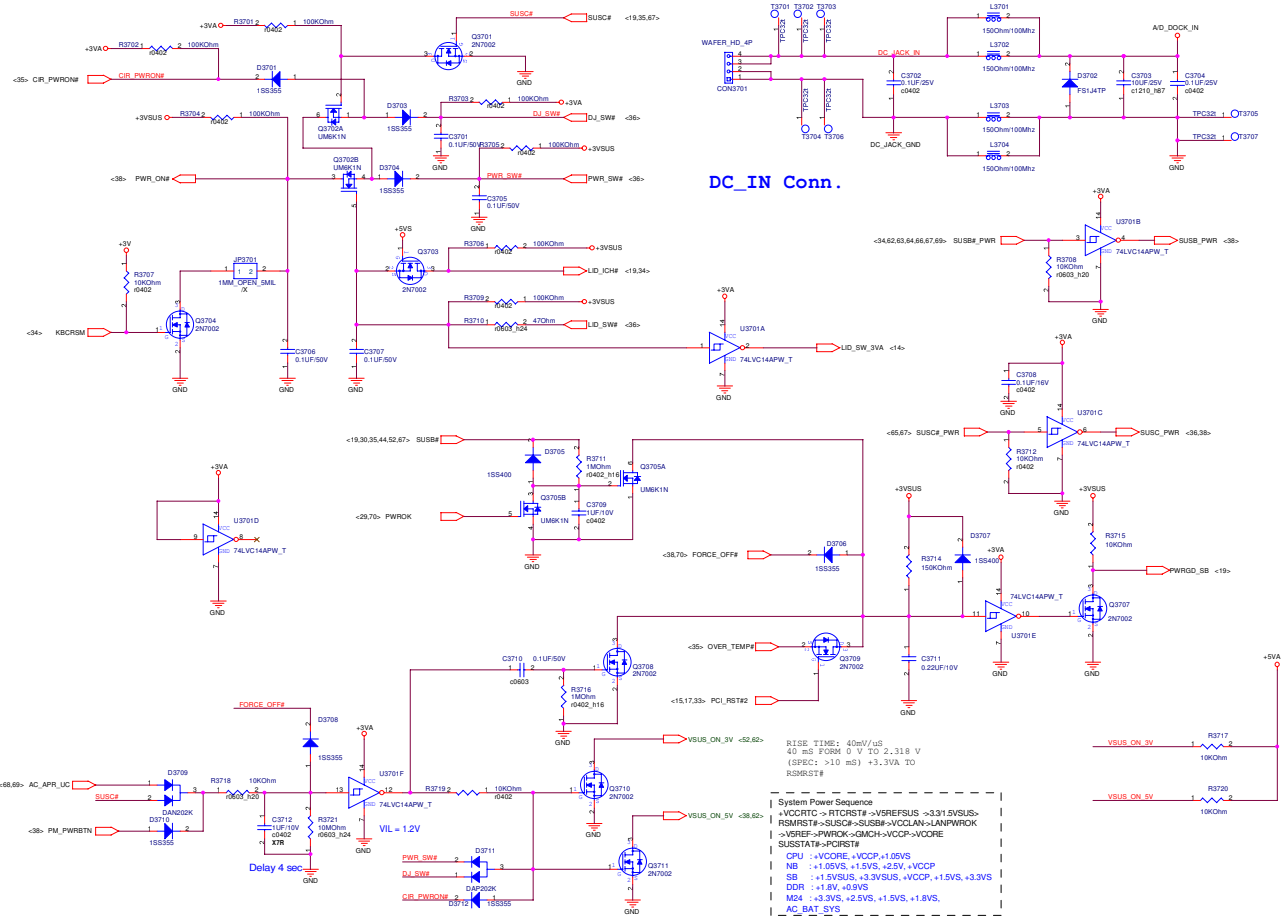






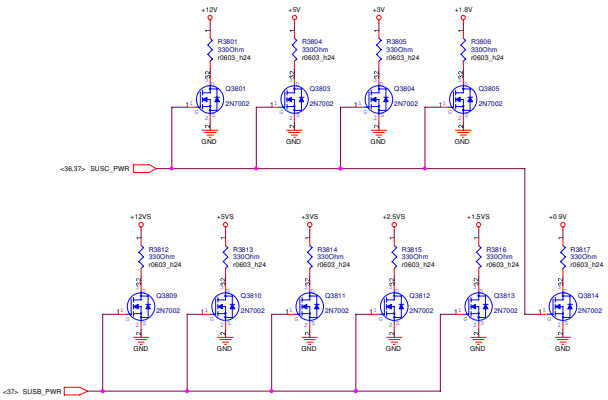


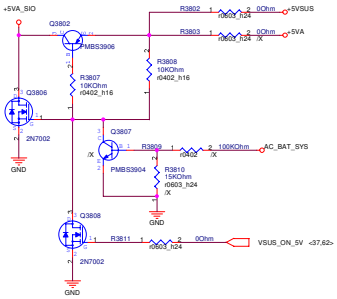


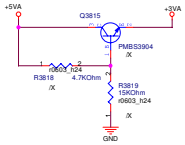


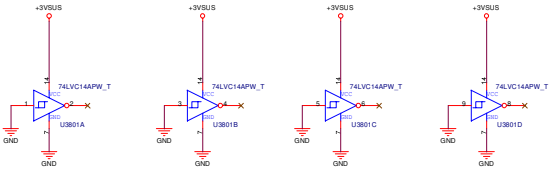
ASUSTeK	Title : POWER ON SEQ		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 37 of 73		

Discharge Ckt.

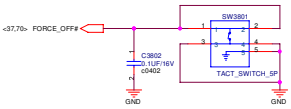


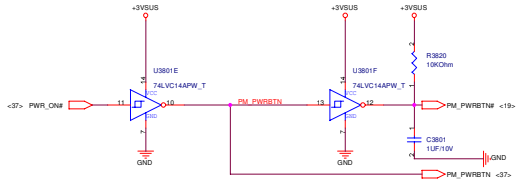




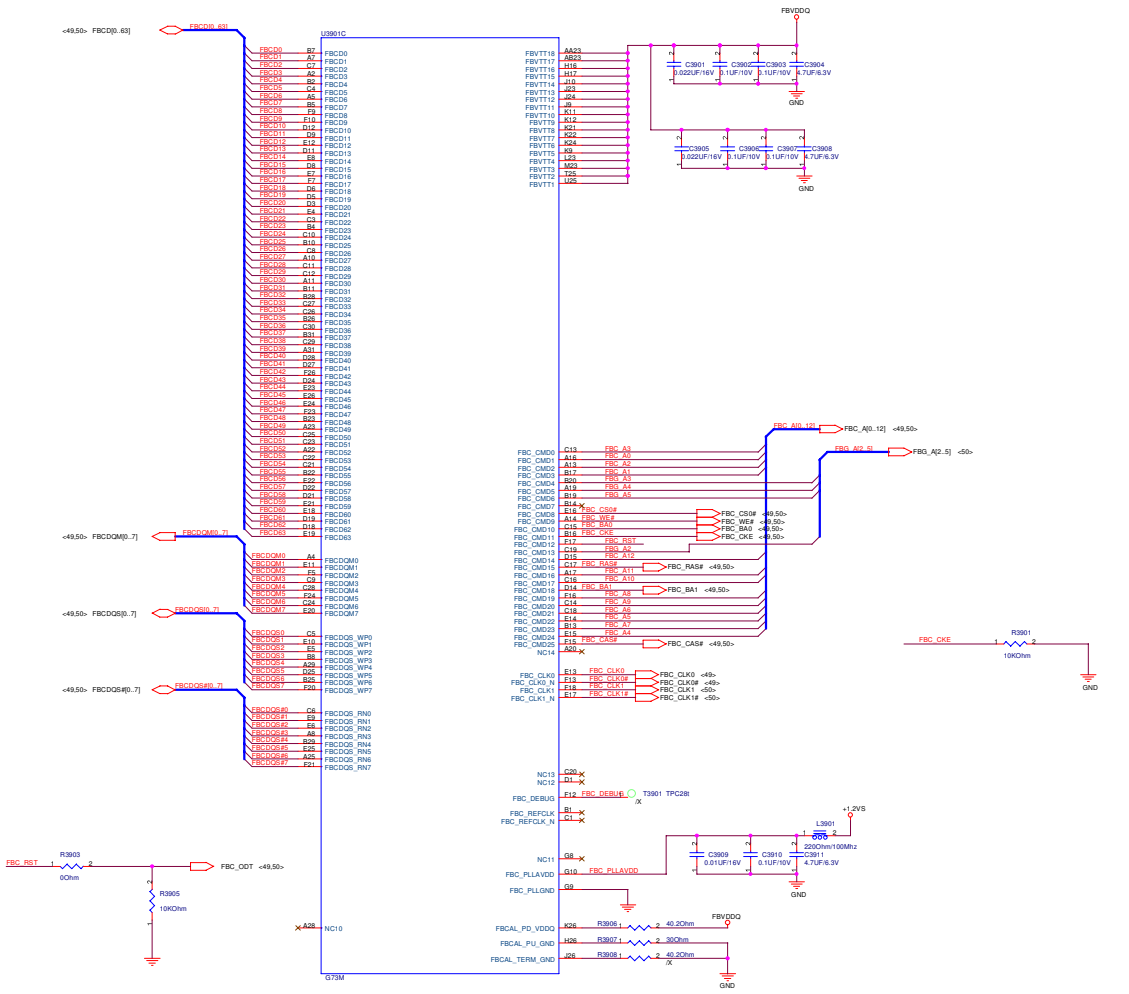


RESET SW.

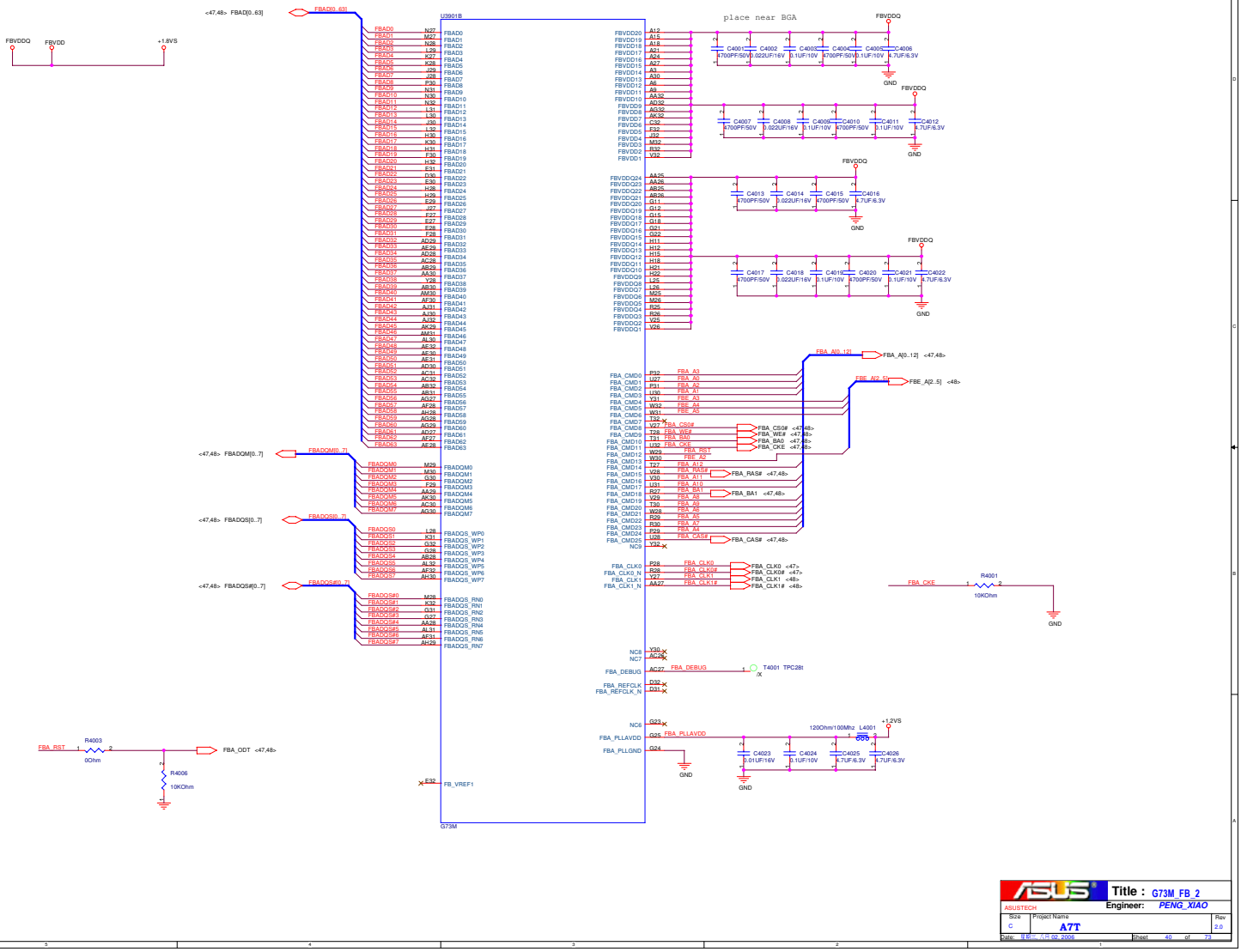




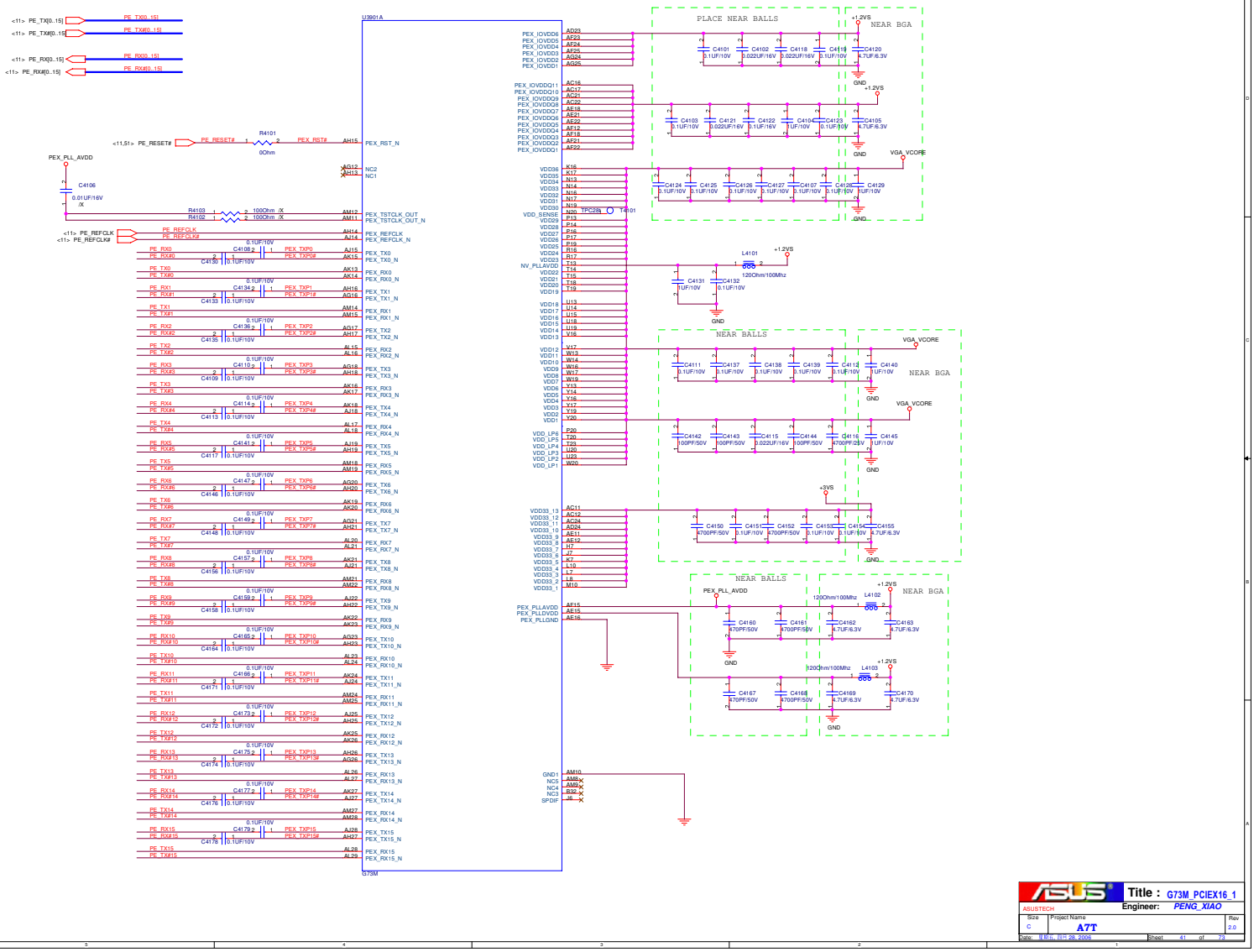
ASUSTECH	Title : PWR ON SEQ		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 38 of 73		



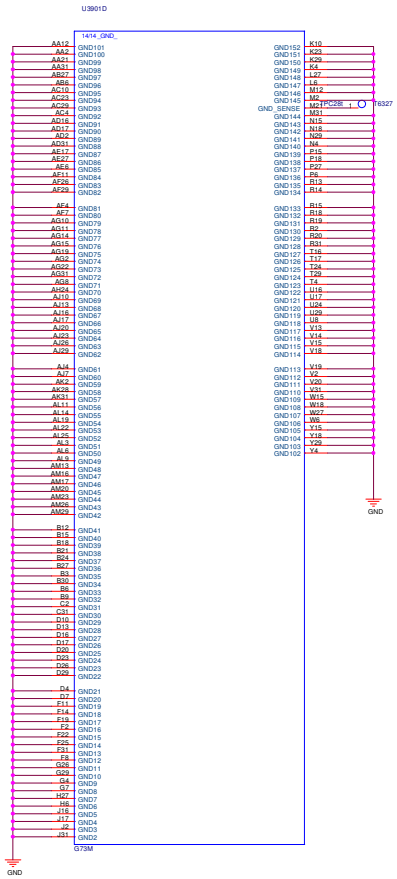
ASUSTeK	Title : G73M_FB_1		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 39 of 73		



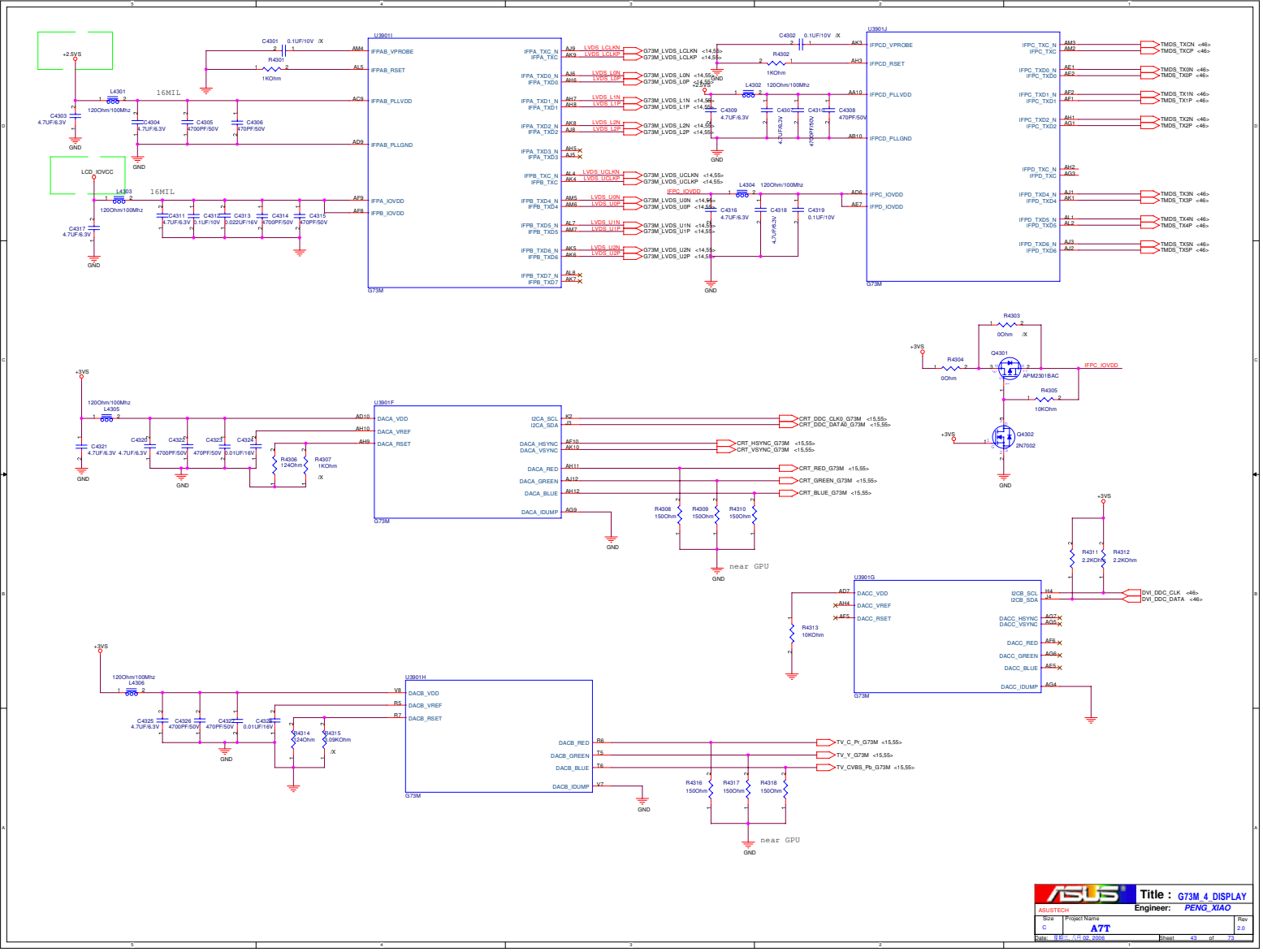
ASUSTeK	Title : G73M_FB_2		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 40 of 73		



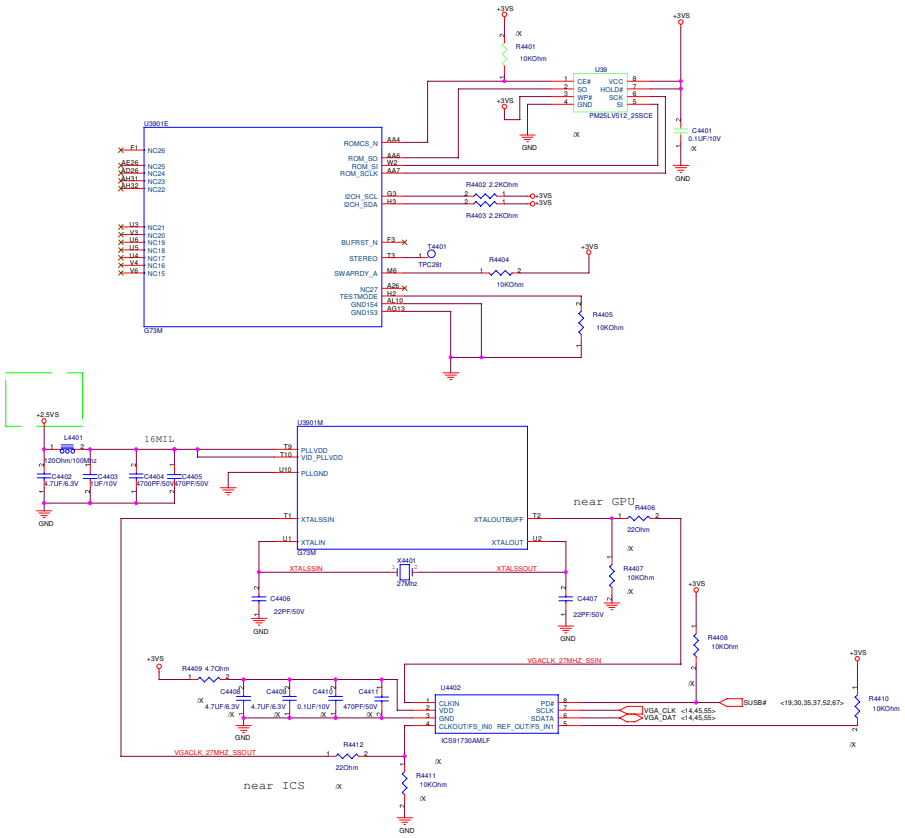
ASUSTECH	Title : G73M_PCIEX16_1		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 41 of 73		



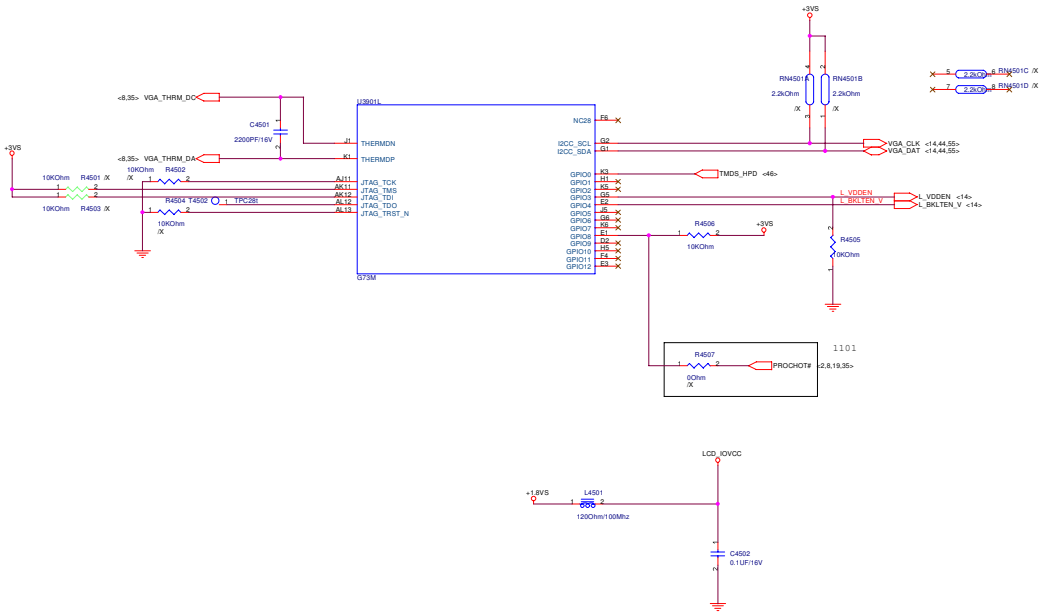
ASUSTECH	Title : G73M_PCIEX16_2		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 42 of 73		



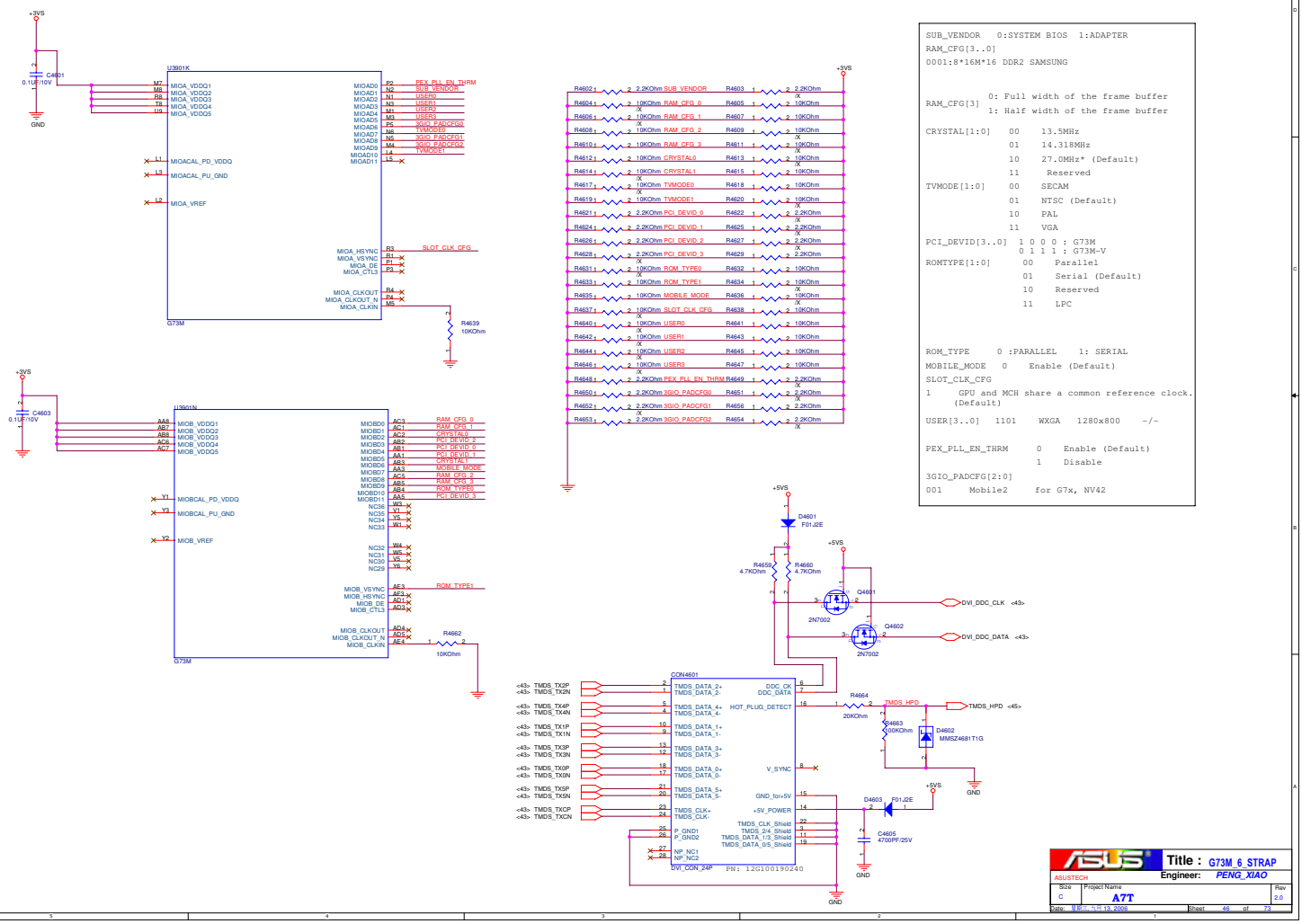
ASUSTeK	Title : G73M_4_DISPLAY		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 六月 02, 2006	Sheet 43 of 73		

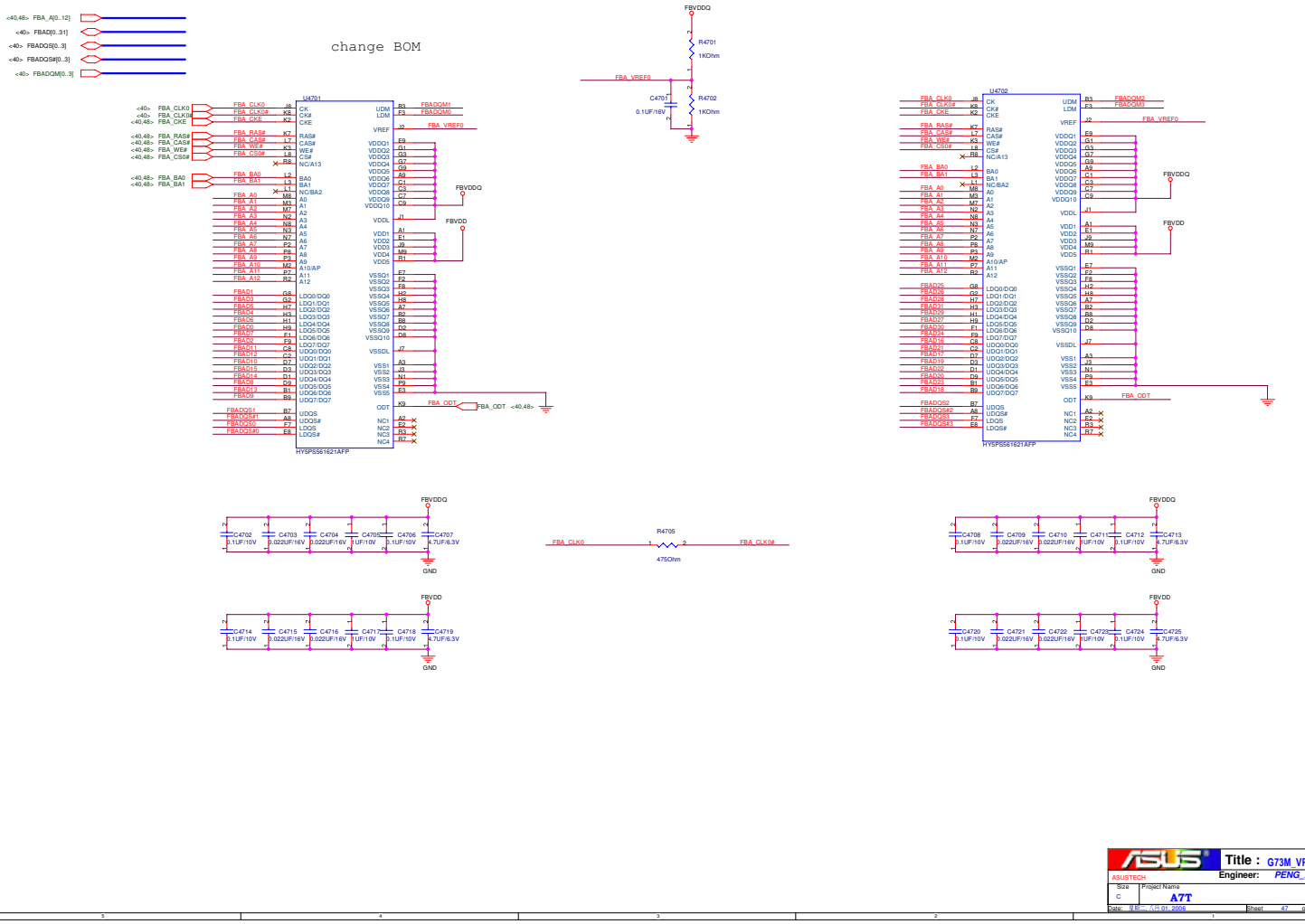


ASUSTECH	Title : G73M-BIOS&CRY		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 44 of 73		

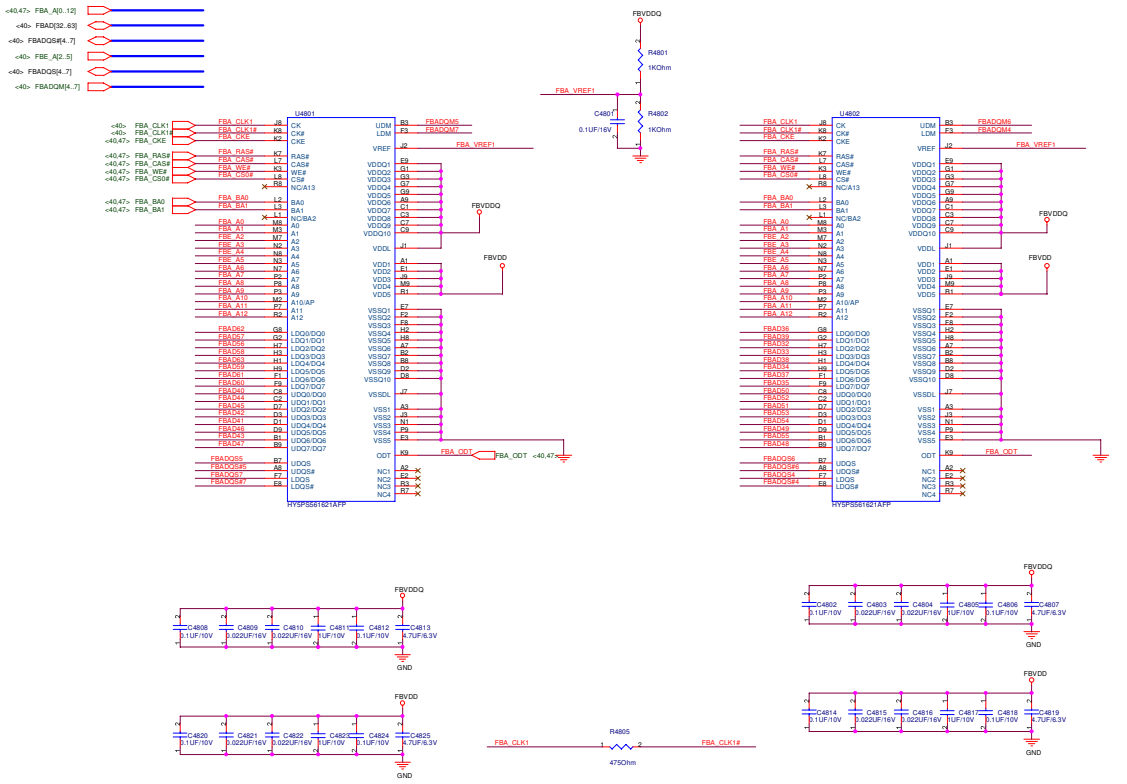


ASUSTECH	Title : G73M_5_GPIO		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006		Sheet 45 of 73	

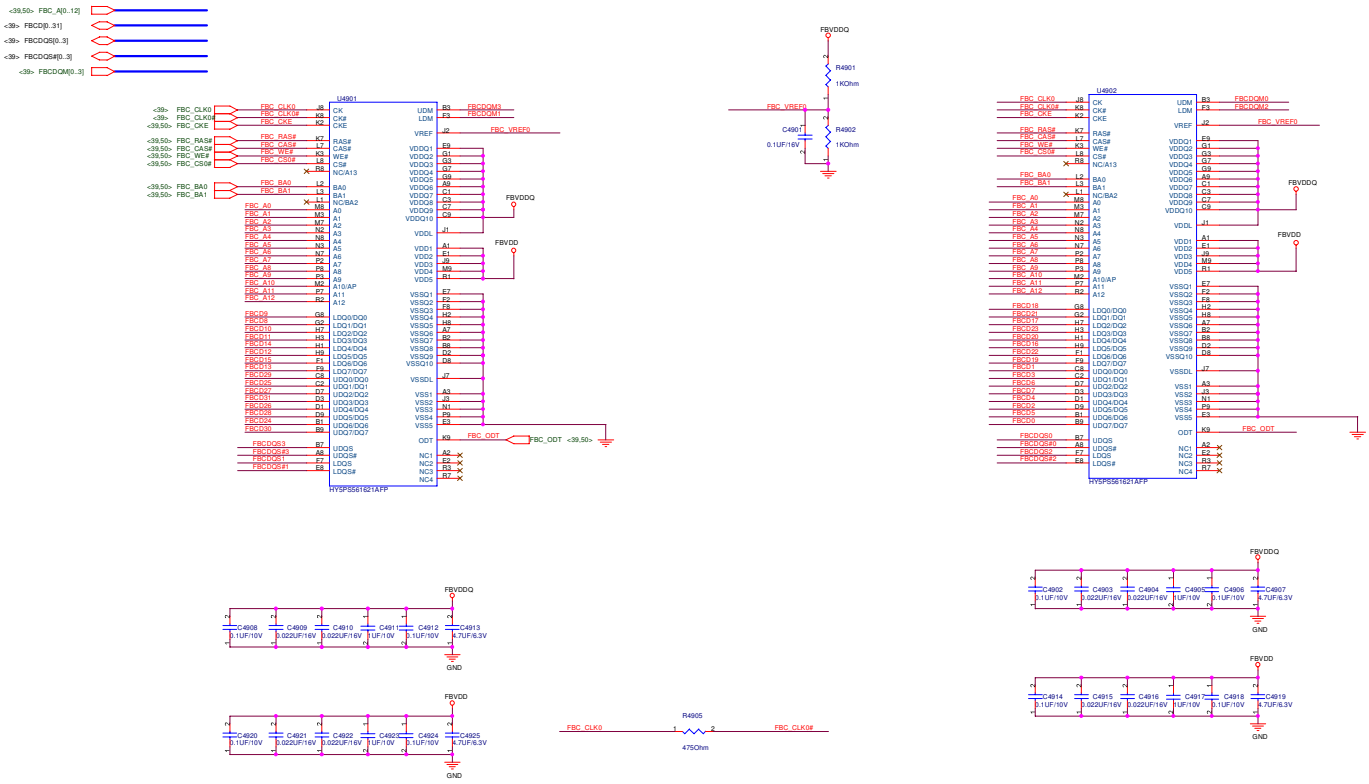

SUB_VENDOR 0:SYSTEM BIOS 1:ADAPTER
RAM_CFG[3..0]
0001:8*16M*16 DDR2 SAMSUNG
RAM_CFG[3] 0: Full width of the frame buffer
1: Half width of the frame buffer
CRYSTAL[1:0] 00 13.5MHz
01 14.318MHz
10 27.0MHz* (Default)
11 Reserved
TVMODE[1:0] 00 SECAM
01 NTSC (Default)
10 PAL
11 VGA
PCI_DEVID[3..0] 1 0 0 0 : G73M
0 1 1 1 : G73M-V
ROMTYPE[1:0] 00 Parallel
01 Serial (Default)
10 Reserved
11 LPC
ROM_TYPE 0 :PARALLEL 1: SERIAL
MOBILE_MODE 0 Enable (Default)
SLOT_CLK_CFG
1 GPU and MCH share a common reference clock. (Default)
USER[3..0] 1101 WXGA 1280x800 -/-
PEX_PLL_EN_THRM 0 Enable (Default)
1 Disable
3GIO_PADCFG[2:0]
001 Mobile2 for G7x, NV42
U3901K
G73M
U3901N
G73M
CON4601
DVI_CON_24P
PN: 12G100190240
Title : G73M_6_STRAP
Engineer: PENG_XIAO
ASUSTECH
Size C
Project Name A7T
Rev 2.0
Date: 日期, 九月 13, 2006
Sheet 46 of 73



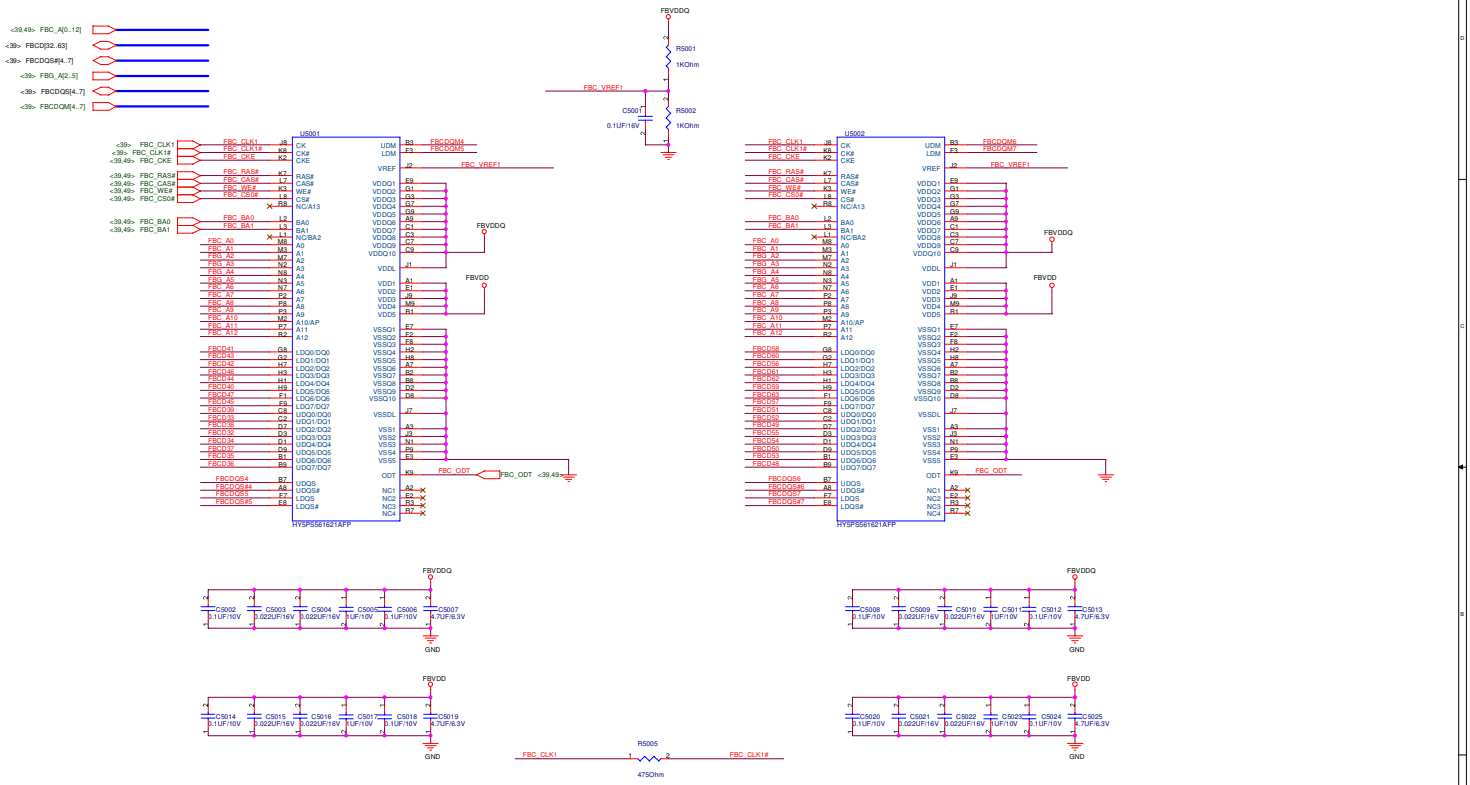
ASUSTeK	Title : G73M_VRAM1		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期一, 八月 01, 2006	Sheet 47 of 73		



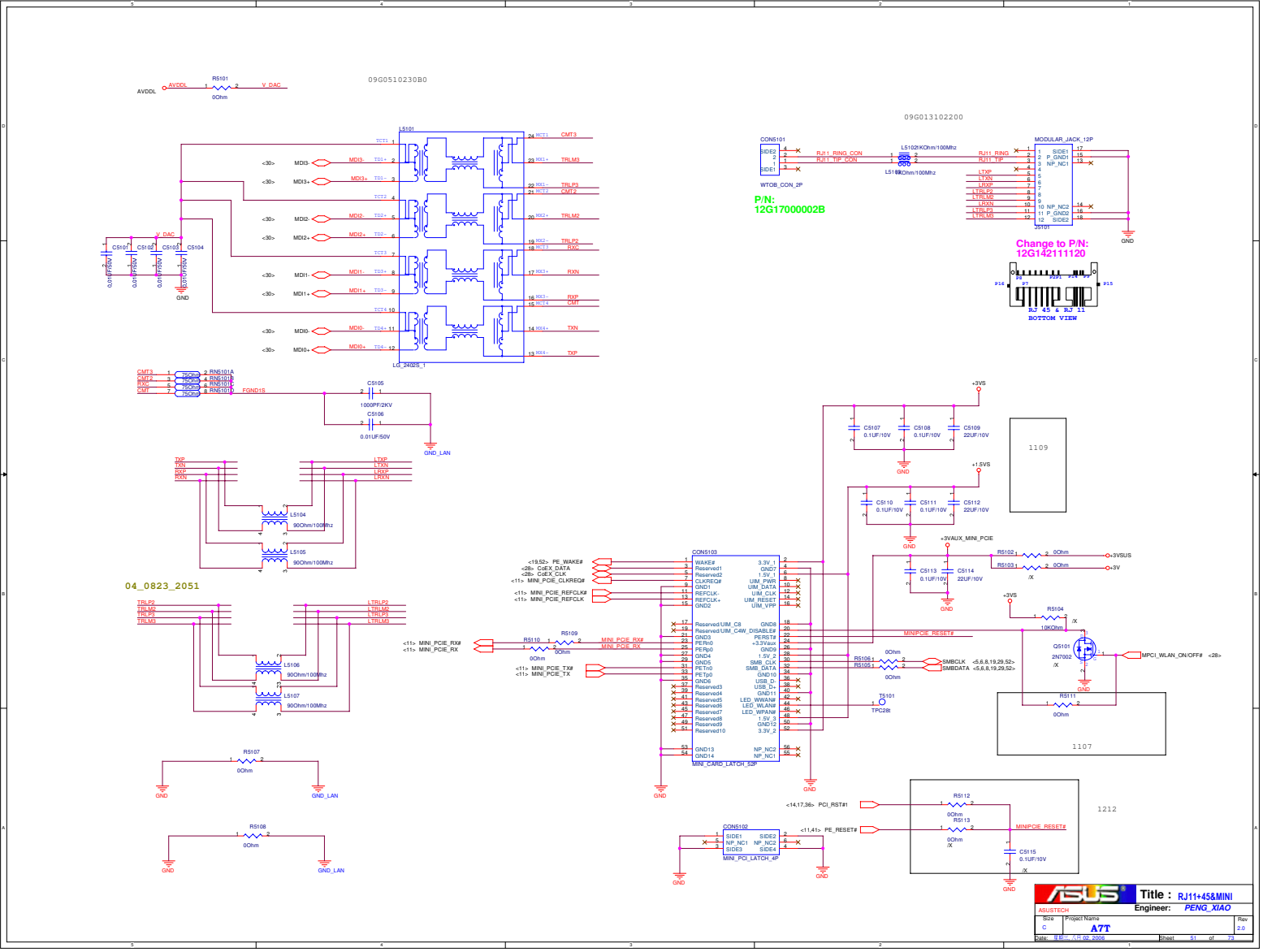
ASUSTeK	Title : G73M_VRAM2		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 01, 2006	Sheet 48 of 73		

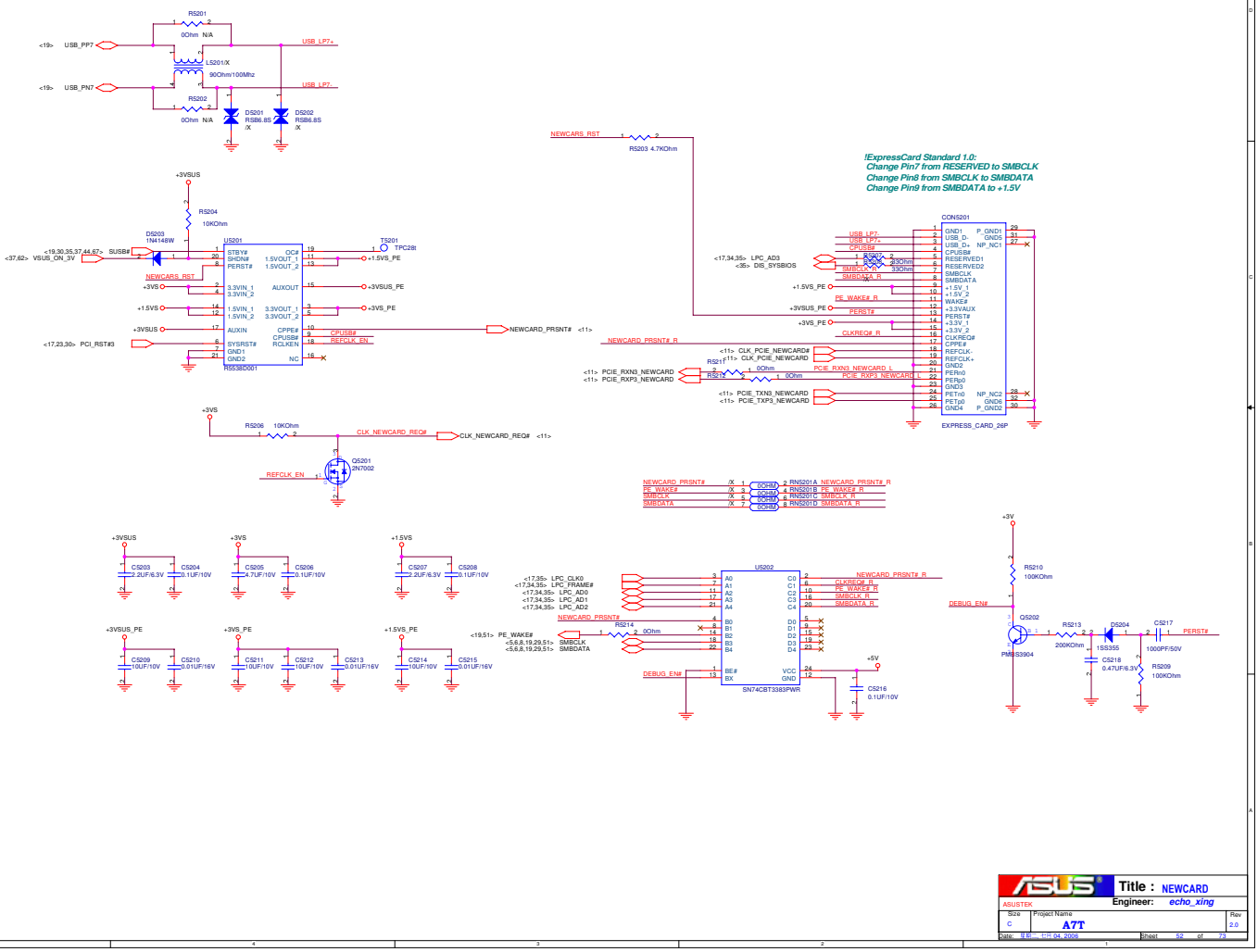


ASUSTeK	Title : G73M_VRAM3		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 01, 2006		Sheet 49 of 73	



ASUSTeK	Title : G73M-VRAM4		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期一, 八月 01, 2006	Sheet 50 of 73		


09G0510230B0
AVDDL
RS101
0Ohm
V_DAC
09G0131022OO
LS101
LG_2402S_1
CMT3
TRLM3
TRLP3
CMT2
TRLM2
TRLP2
RXC
RXN
CMT
TXP
TXN
RXP
RXN
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
RN5101A
RN5101B
RN5101C
RN5101D
75OHM
FGND1S
CS105
1000PF/2KV
CS106
0.01UF/50V
GND_LAN
CS101
CS102
CS103
CS104
0.01UF/50V
GND
LS104
LS105
LS106
LS107
90Ohm/100Mhz
04_0823_2051
LTXP
LTXN
LRXP
LRXN
LTRLP2
LTRLM2
LTRLP3
LTRLM3
RS107
RS108
0Ohm
CON5101
SIDE2
SIDE1
WTOB_CON_2P
RJ11_RING_CON
RJ11_TIP_CON
LS102
90Ohm/100Mhz
RJ11_RING
RJ11_TIP
MODULAR_JACK_12P
P/N:
12G17000002B
Change to P/N:
12G142111120
RJ 45 & RJ 11
BOTTOM VIEW
CON5103
WAKE#
Reserved1
Reserved2
CLKREQ#
GND1
REFCLK-
REFCLK+
GND2
Reserved/UIM_C8
Reserved/UIM_C4
GND3
PERn0
PERp0
GND4
GND5
PETn0
PETp0
GND6
Reserved3
Reserved4
Reserved5
Reserved6
Reserved7
Reserved8
Reserved9
Reserved10
GND13
GND14
3.3V_1
GND7
1.5V_1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
GND8
PERST#
+3.3Vaux
GND9
1.5V_2
SMB_CLK
SMB_DATA
GND10
USB_D-
USB_D+
GND11
LED_WWAN#
LED_WLAN#
LED_WPAN#
1.5V_3
GND12
3.3V_2
NP_NC2
NP_NC1
MINI_CARD_LATCH_52P
MINI_PCIE_RX#
MINI_PCIE_RX
MINI_PCIE_TX#
MINI_PCIE_TX
MINIPCIE_RESET#
SMBCLK
SMBDATA
MPCI_WLAN_ON/OFF#
RS109
RS110
RS105
RS106
RS111
RS102
RS103
RS104
RS112
RS113
RS115
10KOhm
2N7002
TS101
TPC28I
CON5102
SIDE1
SIDE2
NP_NC1
NP_NC2
SIDE3
SIDE4
MINI_PCI_LATCH_4P
PCI_RST#1
PE_RESET#
+3VS
+1.5VS
+3VAUX_MINI_PCIE
+3VSUS
CS107
CS108
CS109
CS110
CS111
CS112
CS113
CS114
0.1UF/10V
22UF/10V
1109
1107
1212
GND
/X
ASUSTeK
Title : RJ11+45&MINI
Engineer: PENG_XIAO
Size C
Project Name A7T
Rev 2.0
Date: 星期二, 八月 02, 2006
Sheet 51 of 73



ASUSTEK

Title : NEWCARD

Engineer: echo_xing

Size: C | Project Name: A7T | Rev: 2.0

Date: 星期二, 十月 04, 2006 | Sheet 52 of 73

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	A
CARD READER	AD17	1	C
1394	AD17	1	B
MINIPCI (802.11a/b/g)	AD19	3	B,C
MINIPCI (TV)	AD18	0	A,D

Host	SM-Bus Device	SM-Bus Address	Device
MCP51	Voice DSP	1100000x (C2H)	VP1010
MCP51	SO-DIMM 0	1010000x (A0H)	DDR SOCKET1
MCP51	SO-DIMM 1	1010010x (A4H)	DDR SOCKET2
MCP51	Thermal Sensor	0101110x (5CH)	ADT7463 (Optinal)
	PIC	1001001x (92H)	Charge IC
	M38857	0001000x (10H)	KBC control IC
	BQ2060	16H-17H	Battery sensor IC

MCP51 GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 1	INPUT	KB_SCI#				+3VS
GPIO 2	INPUT	SIO_SMI#				+3VS
GPIO 3	OUTPUT	BACK_OFF#	LOW	HIGH	Off	+3VS
GPIO 4	OUTPUT	FWH_WP#	LOW	LOW	Off	+3VS
GPIO 5	OUTPUT	802_LED_EN#	LOW	HIGH	Driven	+3VSUS
GPIO 6						+3VSUS
GPIO 7	OUTPUT	BT_LED_EN#	**LOW**	HIGH	Driven	+3VSUS
GPIO 8						
GPIO 9						
GPIO 10						
GPIO 11	OUTPUT	BT_ON#	LOW	LOW	Off	+3VS
GPIO 12	OUTPUT	WLAN_ON#	LOW	LOW	Off	+3VS
GPIO 13						
GPIO 14						
GPIO 15	INPUT	PROCHOT#	LOW	HIGH	Off	
GPIO 16						
GPIO 17		LID#				+3VSUS
GPIO 18		USB_OC#0				+3VSUS
GPIO 19		USB_OC#1				+3VSUS
GPIO 20		USB_OC#2				+3VSUS
GPIO 21		USB_OC#3				+3VSUS
GPIO 22		ACZ_SDIN0				+3VSUS
GPIO 23		ACZ_SDIN1				+3VSUS
GPIO 24						
GPIO 25						
GPIO 26						
GPIO 27		SMB_CLK				+3VSUS
GPIO 28		SMB_DATA				+3VSUS
GPIO 29		SMB_ALERT#				+3VSUS
GPIO 30		PCI_PME#				+3VSUS
GPIO 31		SIO_PME#				+3VSUS
GPIO 32		EXTSMI#				+3VSUS
GPIO 33		RI#				+3VSUS
GPIO 34		SUS_CLK	PULL-DOWN:Normal mode select			
GPIO 40						
GPIO 41						
GPIO 46		SPDIFO	PULL-HIGH:SIO_CLK select 24MHz			+3VS
GPIO 47	INPUT	RF_OFF_SW#	LOW	HIGH	Off	+3VS
GPIO 61	INPUT	PANEL_ID0			Off	+3VS
GPIO 62	INPUT	PANEL_ID1			Off	+3VS

KBC GPIO	I/O Mode	Signal	Active	S0 Default	S3
P23(Pin 35)					
P22(Pin 36)	OUTPUT	BAT_LEARN	HIGH	LOW	LOW
P21(Pin 37)		KBC_P21			
P20(Pin 38)	OUTPUT	KBCRSM	HIGH	LOW	LOW
P42(Pin 23)	OUTPUT	WATCHDOG	HIGH	LOW	LOW
P43(Pin 22)	INPUT	LID_KBC#			
P44(Pin 21)					
P45(Pin 20)	OUTPUT	KB_GATEA20			
P46(Pin 19)	OUTPUT	KBSCI#			
P47(Pin 18)		PM_CLKRUN#			
P50(Pin 17)	INPUT	BAT_LLOW#_OC			
P51(Pin 16)	INPUT	KB_ID0			
P52(Pin 15)	INPUT	KB_ID1			
P53(Pin 14)	OUTPUT	CLR_DJ#	LOW	LOW	Driven
P54(Pin 13)	INPUT	BAT_SEL#			
P55(Pin 12)	INPUT	BAT1_IN#_OC			
P56(Pin 11)	OUTPUT	FAN_DA1(Optinal)	Analog	Analog	Driven
P57(Pin 10)	OUTPUT	INVTER_DA	Analog	Analog	Driven
P67(Pin 74)	OUTPUT	DJ_LED#	LOW	HIGH	HIGH
P66(Pin 75)	INPUT	SWDJ_EN#			
P65(Pin 76)	INPUT	CHG_FULL_OC			
P64(Pin 77)	INPUT	ACIN_OC			
P63(Pin 78)	INPUT	DISTP_SW#			
P62(Pin 79)	INPUT	P4GEAR_SW#			
P61(Pin 80)	INPUT	**EMAIL_SW#**			
P60(Pin 1)	INPUT	**INTERNET_SW#**			
P75(Pin 4)		KB_CLK			
P74(Pin 5)		MS_CLK			
P73(Pin 6)		TPAD_CLK			
P72(Pin 7)		KB_DAT			
P71(Pin 8)		MS_DAT			
P70(Pin 9)		TPAD_DAT			
P77(Pin 2)		SMC_BAT			
P76(Pin 3)		SMD_BAT			
P27(Pin 31)					
P26(Pin 32)	OUTPUT	NUM_LED#	LOW	Define	HIGH
P25(Pin 33)	OUTPUT	CAP_LED#	LOW	Define	HIGH
P24(Pin 34)	OUTPUT	SET_PLTRSTNS#	LOW		
P40(Pin 27)	OUTPUT	EXT_SMI			
P41(Pin 26)	OUTPUT	EMAIL_LED#	LOW	HIGH	HIGH

MCP51 GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 16	OUTPUT	DSP_SHI_EN	HIGH	HIGH	Off	+5VS
GPIO 53	INPUT	SUSC#	LOW	HIGH	H/L	+5VS
GPIO 45	INPUT	SUSB#	LOW	HIGH	LOW	+5VS
GPIO 11	INPUT	PROCHOT#	LOW	HIGH	Off	+5VS

ASUSTeK

Title : SYS RESOU

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期日, 四月 29, 2006 Sheet 53 of 73

Rev	Date	Description
1.1		
	1101	add throttle circuit
	1102	add HD and ODD LED control
	1103	change therm sensor
	1104	add de-glitch circuit for NVIDIA suggestion
	1105	add damping resistor for LPC bus
	1106	change C1319,20,29,30,39,40,41,42 package, add C1354,55,56,57 for therm issue
	1107	add R5111 for wireless disable option
	1108	add MCP51 LCD control signal
	1109	modify C5109,12,14,CE2601 P/N for high limit
1.2		
	1201	swap LVDS control signal
	1202	remove Q3608 for charge LED
	1203	change R3609 and R3612's pull high power to +3V
	1204	change R1612 P/N
	1205	swap speaker
	1206	add C2936
	1207	change HDD LED control
	1208	change bead to inductor for SI
	1209	add R1214 for RGB signal
	1210	add R1964 for NVIDIA suggestion
	1211	add C1415 for LCD
	1212	add R5112 R5113 and C5115 for MINIPCIE reset sequence

Rev	Date	Description

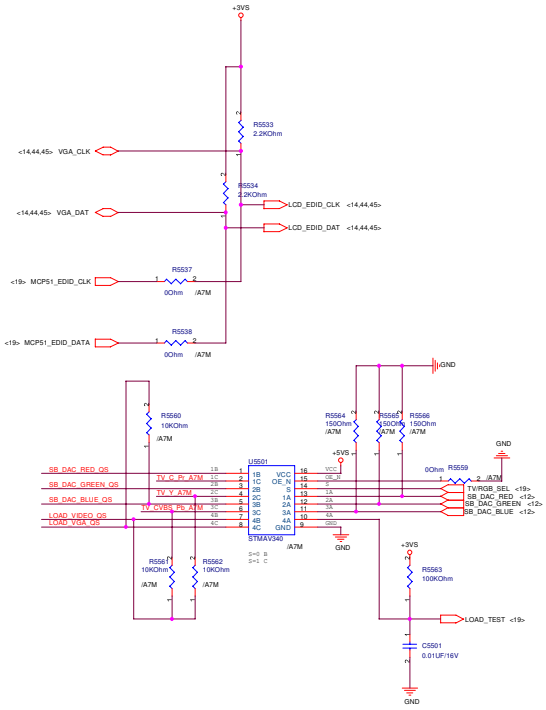
ASUSTECH

Title : HISTORY

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期日, 四月 29, 2006 Sheet 54 of 73



ASUSTeK	Title : LVDS SWITCH		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 55 of 73		

Title : HISTORY

ASUSTECH

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期三, 四月 26, 2006 Sheet 56 of 73

Title : HISTORY

ASUSTECH

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期日, 四月 29, 2006 Sheet 57 of 73

Title : HISTORY

ASUSTECH

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期三, 四月 26, 2006 Sheet 58 of 73

Title : HISTORY

ASUSTECH

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期三, 四月 26, 2006 Sheet 59 of 73

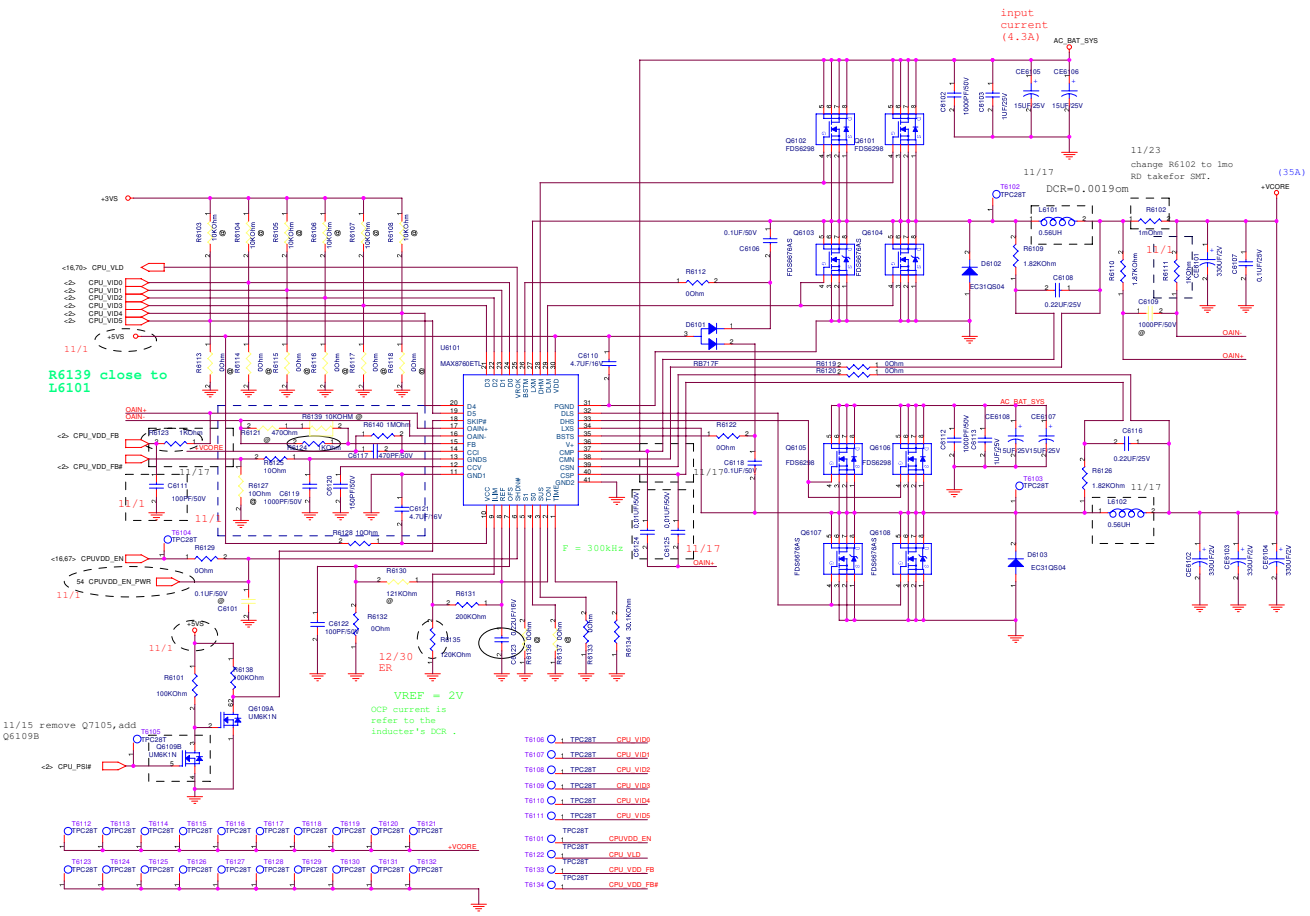
Title : HISTORY

ASUSTECH

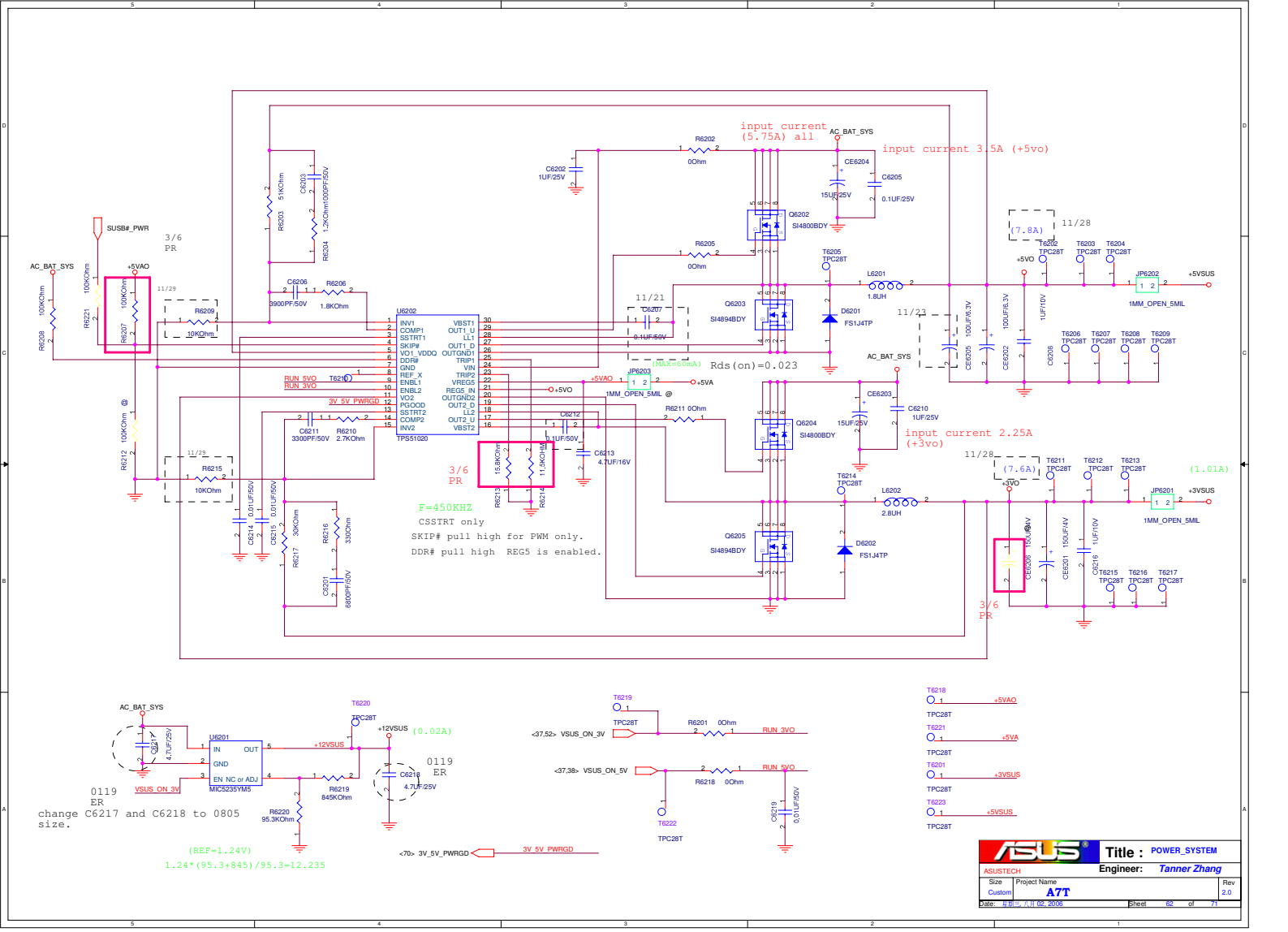
Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

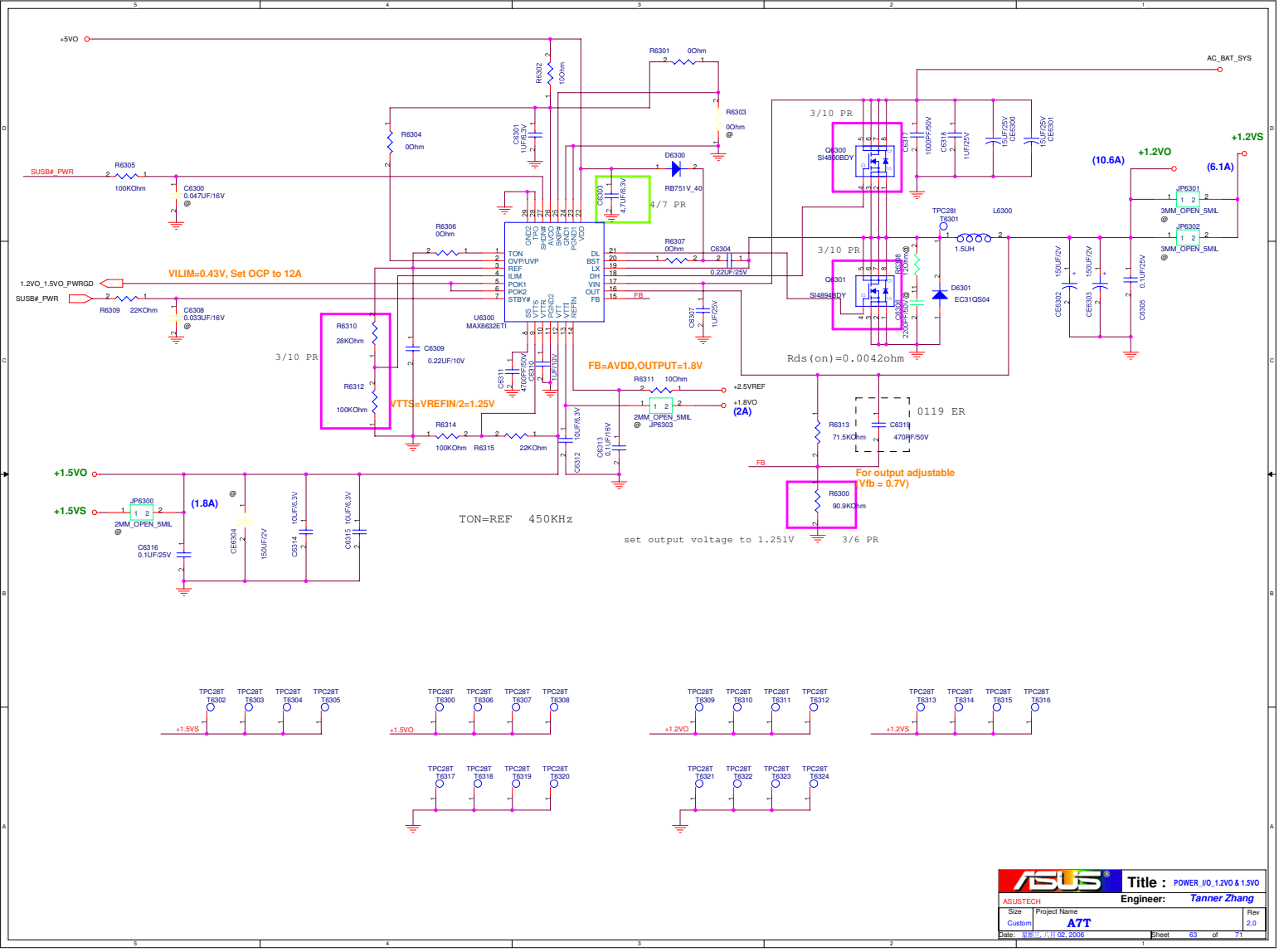
Date: 星期五, 四月 28, 2006 Sheet 60 of 73



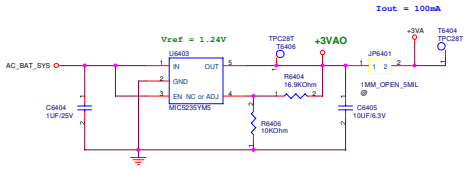
ASUSTek	Title : POWER_VCORE		
	Engineer: Tanner Zhang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 61 of 71		



ASUSTECH	Title : POWER_SYSTEM		
	Engineer: Tanner Zhang		
Size: Custom	Project Name: A77		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 62 of 71		

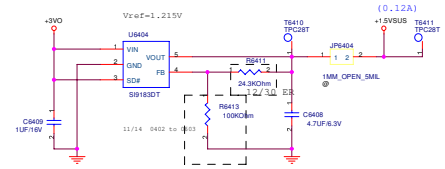


ASUSTECH	Title : POWER_I/O_1.2VO & 1.5VO		
	Engineer: Tanner Zhang		
Size: Custom	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 63 of 71		

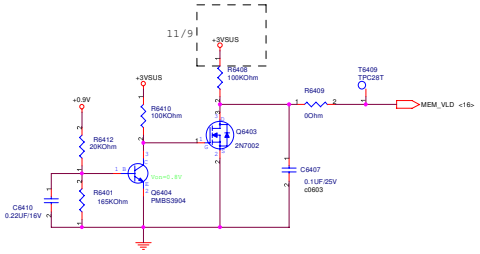


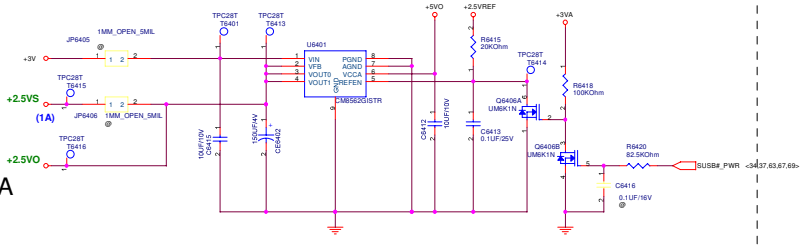
+3VA

+1.5VS

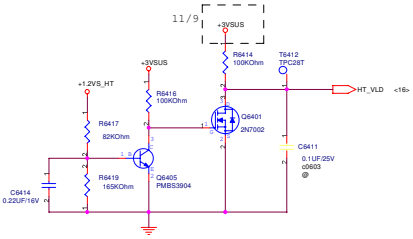


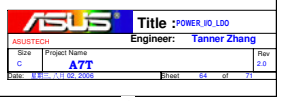
+1.5VSUS

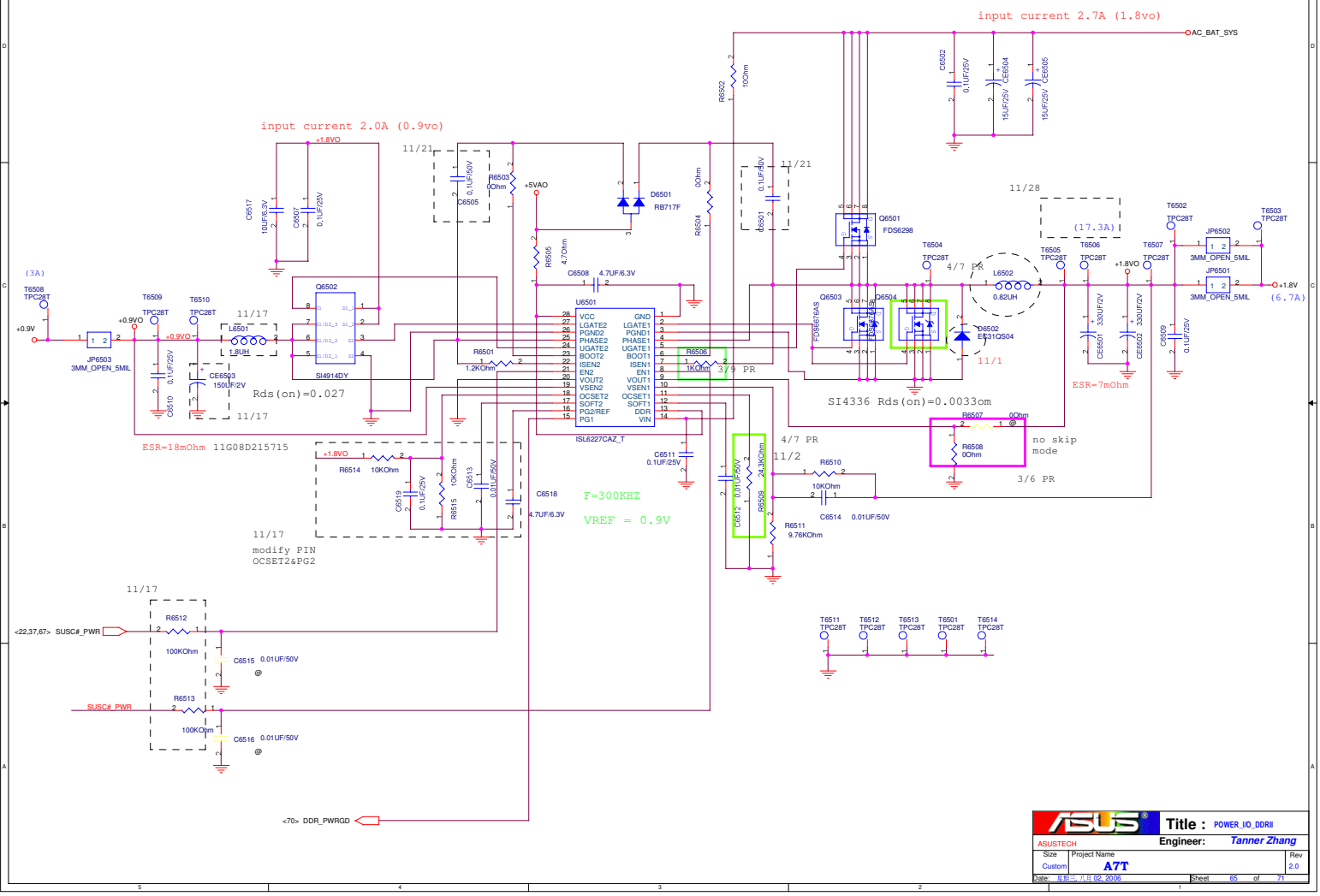


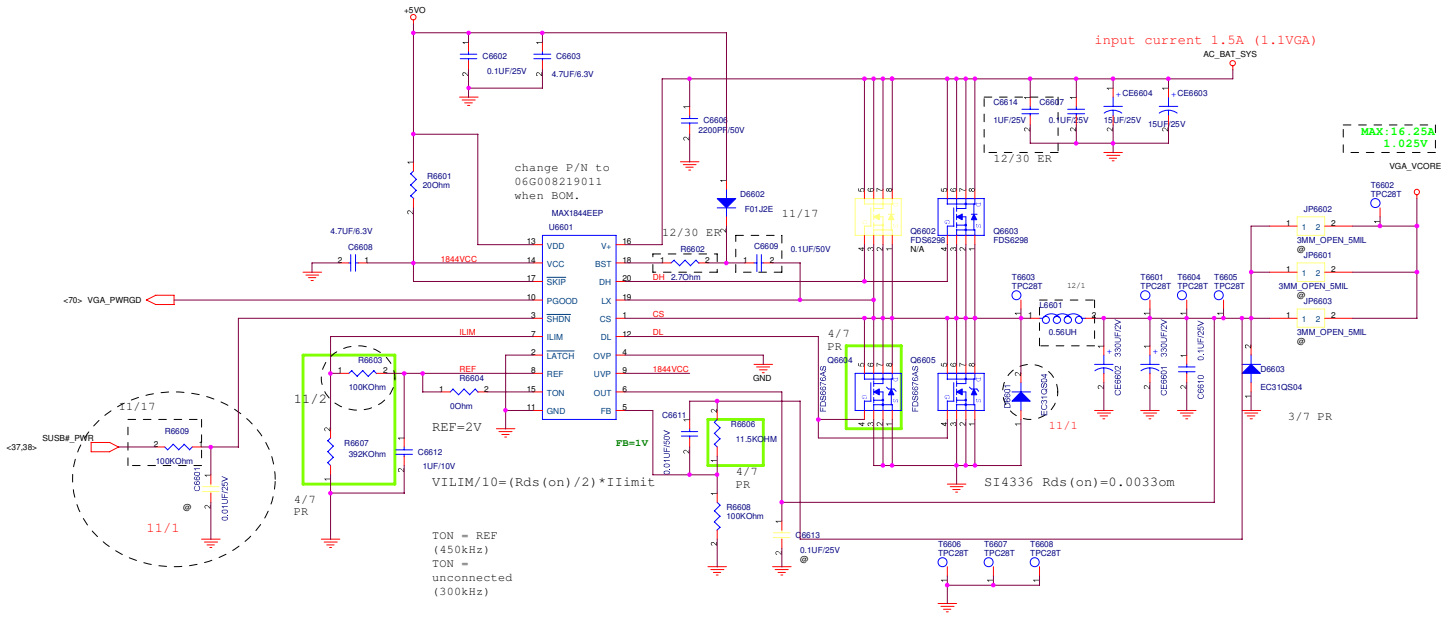


+2.5VS



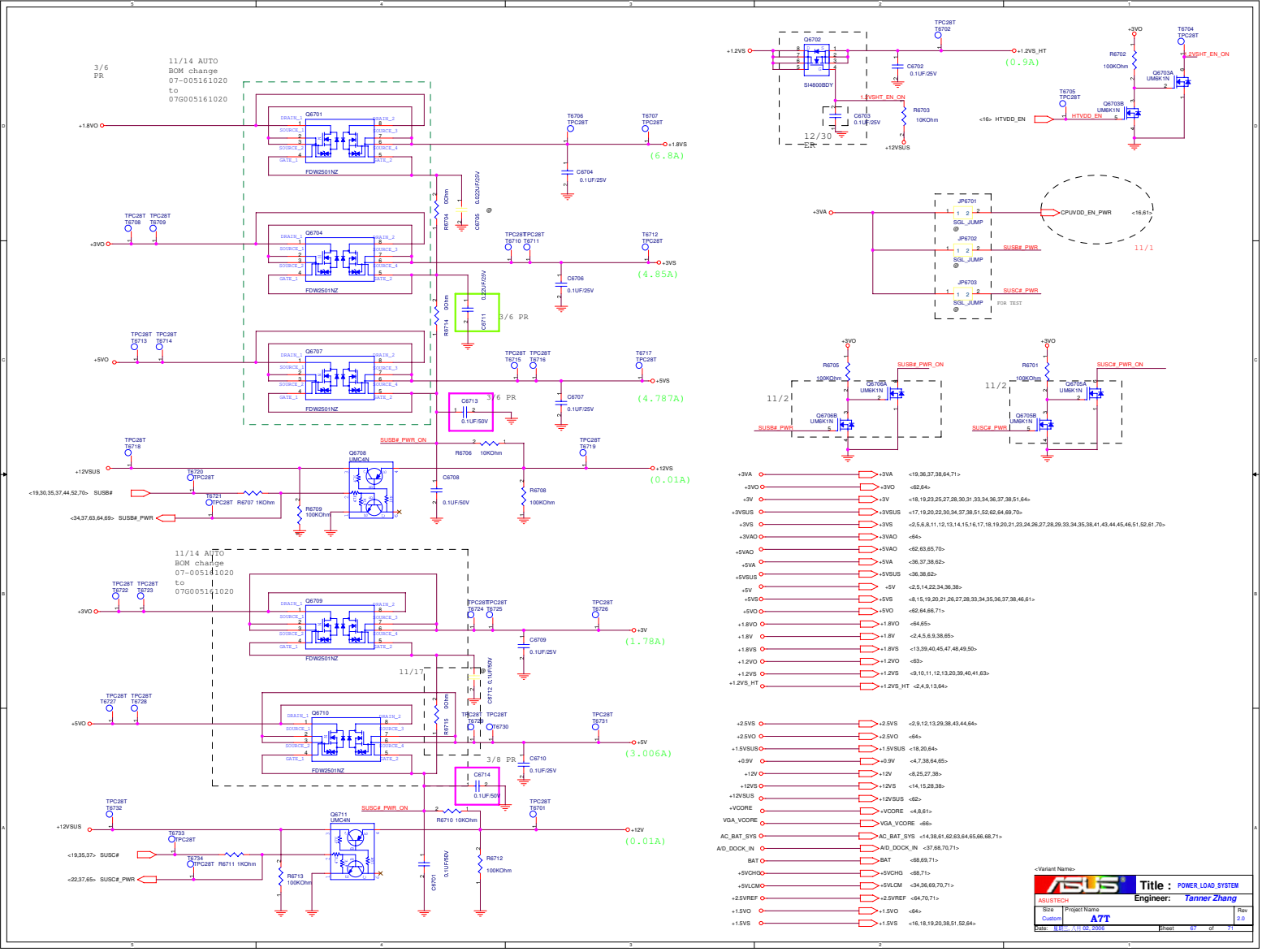


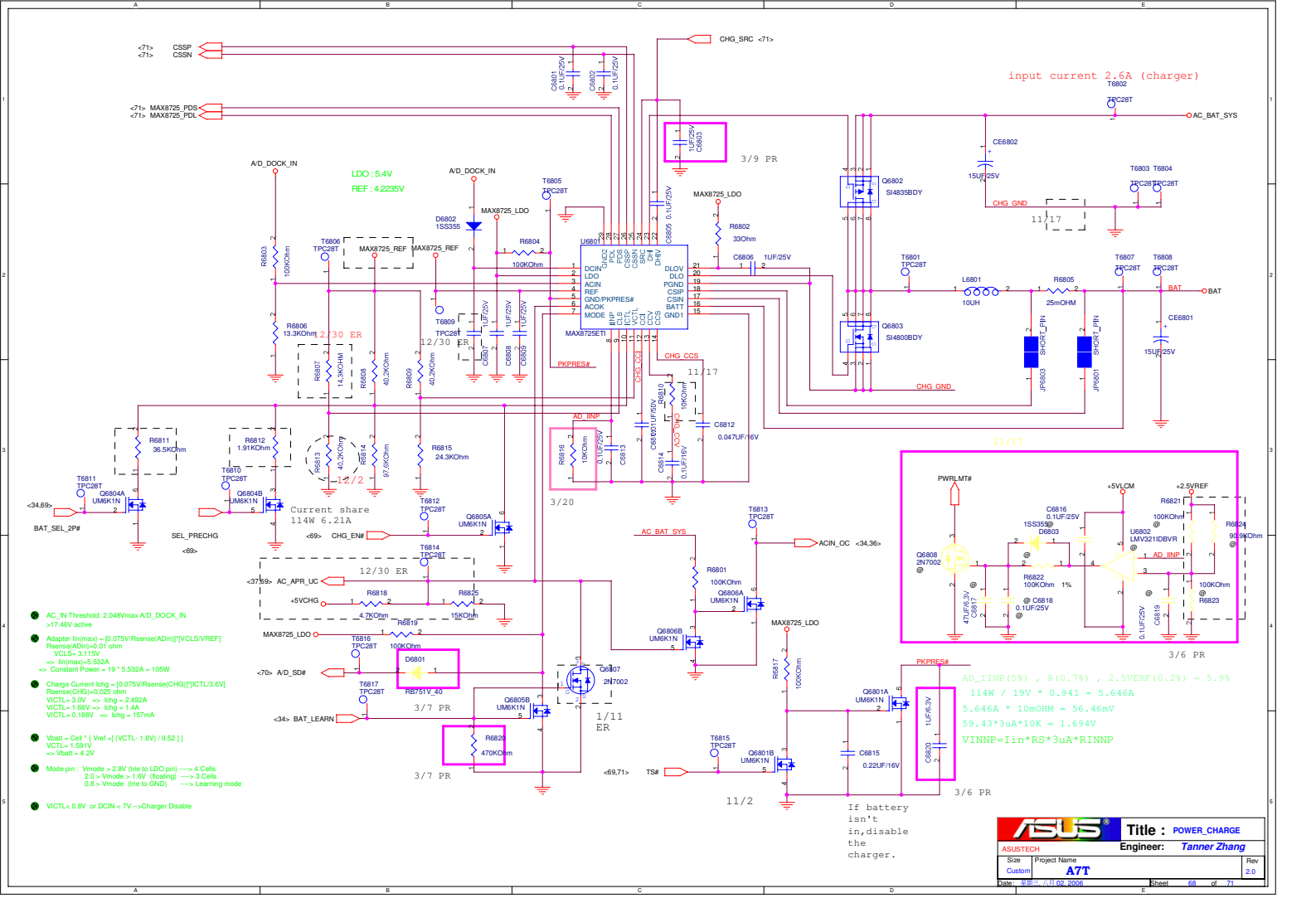

input current 2.7A (1.8vo)
AC_BAT_SYS
input current 2.0A (0.9vo)
+1.8VO
+5VAO
+0.9VO
+0.9V
+1.8V
(3A)
(6.7A)
(17.3A)
11/21
11/28
11/17
11/1
11/2
3/6 PR
4/7 PR
3/9 PR
Rds(on)=0.027
SI4336 Rds(on)=0.0033om
ESR=18mOhm 11G08D215715
ESR=7mOhm
no skip mode
F=300KHZ
VREF = 0.9V
modify PIN OCSET2&PG2
ISL6227CAZ_T
SI4914DY
FDS6298
FDS6676AS
RB717F
E0331QS04
0.82UH
1.8UH
150UF/2V
330UF/2V
3MM_OPEN_5MIL
<22,37,67> SUSC#_PWR
SUSC#_PWR
<70> DDR_PWRGD
Title : POWER_I/O_DDRII
ASUSTECH
Engineer: Tanner Zhang
Size: Custom
Project Name: A7T
Rev: 2.0
Date: 星期三, 八月 02, 2006
Sheet 65 of 71

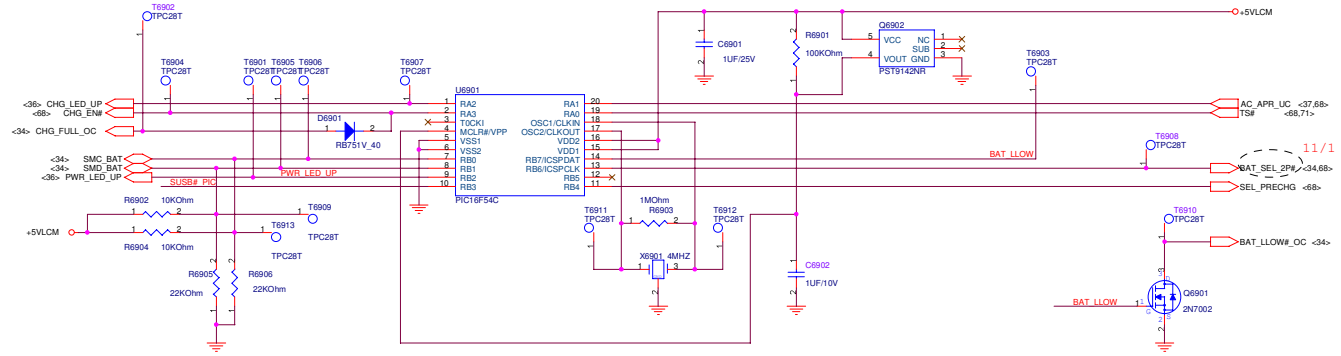


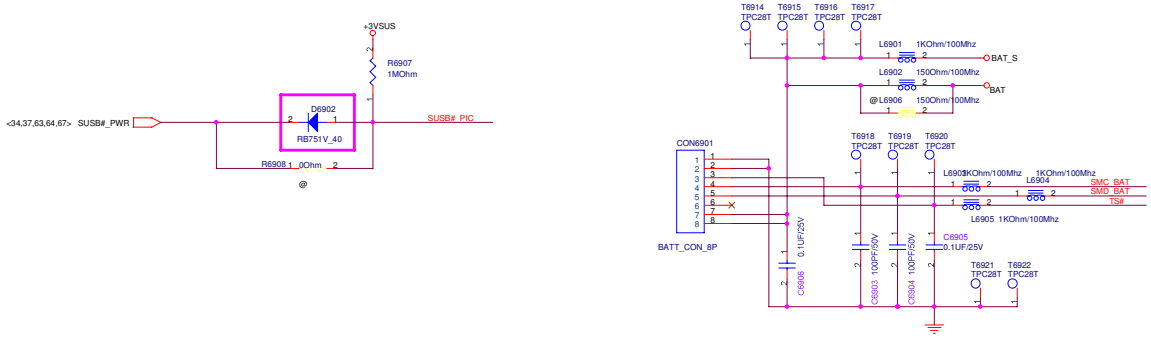
<Variant Name>

ASUSTek	Title : POWER_VGACORE	
	Engineer: Tanner Zhang	
Size: Custom	Project Name: A7T	Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 66 of 71	

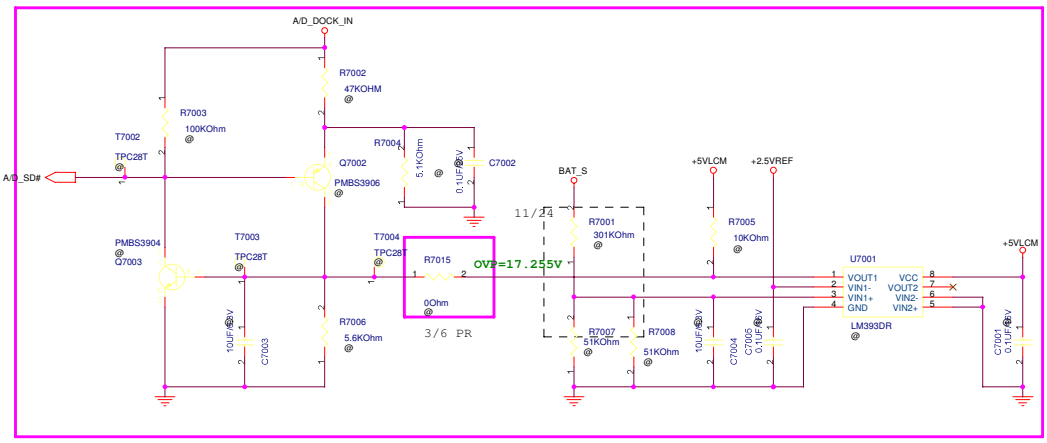

3/6 PR
11/14 AUTO BOM change 07-005161020 to 07G005161020
+1.8VO
Q6701
FDW2501NZ
T6706 TPC28T
T6707 TPC28T
+1.8VS
(6.8A)
C6704 0.1UF/25V
R6704 0Ohm
C6705 0.022UF/25V
+3VO
Q6704
T6708 TPC28T
T6709 TPC28T
T6710 TPC28T
T6711 TPC28T
T6712 TPC28T
+3VS
(4.85A)
C6706 0.1UF/25V
R6714 0Ohm
C6711 0.22UF/25V
+5VO
Q6707
T6713 TPC28T
T6714 TPC28T
T6715 TPC28T
T6716 TPC28T
T6717 TPC28T
+5VS
(4.787A)
C6713 0.1UF/50V
C6707 0.1UF/25V
T6718 TPC28T
+12VSUS
T6720 TPC28T
<19,30,35,37,44,52,70> SUSB#
T6721 TPC28T
R6707 1KOhm
<34,37,63,64,69> SUSB#_PWR
SUSB#_PWR_ON
Q6708 UMC4N
R6706 10KOhm
R6709 100KOhm
C6708 0.1UF/50V
R6708 100KOhm
T6719 TPC28T
+12VS
(0.01A)
11/14 AUTO BOM change 07-005161020 to 07G005161020
Q6709
T6722 TPC28T
T6723 TPC28T
T6724 TPC28T
T6725 TPC28T
T6726 TPC28T
+3V
(1.78A)
C6709 0.1UF/25V
11/17
C6712 0.1UF/50V
Q6710
T6727 TPC28T
T6728 TPC28T
T6729 TPC28T
T6730 TPC28T
T6731 TPC28T
+5V
(3.006A)
R6715 0Ohm
C6710 0.1UF/25V
3/8 PR
C6714 0.1UF/50V
+12VSUS
T6732 TPC28T
T6733 TPC28T
<19,35,37> SUSC#
T6734 TPC28T
R6711 1KOhm
<22,37,65> SUSC#_PWR
SUSC#_PWR_ON
Q6711 UMC4N
R6710 10KOhm
R6713 100KOhm
C6701 0.1UF/50V
R6712 100KOhm
T6701 TPC28T
+12V
(0.01A)
Q6702 SI4800BDY
+1.2VS
T6702 TPC28T
+1.2VS_HT
(0.9A)
C6702 0.1UF/25V
1.2VSHT_EN_ON
C6703 0.1UF/25V
R6703 10KOhm
+12VSUS
12/30 ECR
+3VO
T6704 TPC28T
1.2VSHT_EN_ON
R6702 100KOhm
Q6703A UMK1N
T6705 TPC28T
Q6703B UMK1N
<16> HTVDD_EN
HTVDD_EN
+3VA
JP6701 SGL_JUMP
CPUVDD_EN_PWR
<16,61>
JP6702 SGL_JUMP
SUSB#_PWR
11/1
JP6703 SGL_JUMP
SUSC#_PWR
FOR TEST
+3VO
R6705 100KOhm
SUSB#_PWR_ON
Q6706A UMK1N
11/2
Q6706B UMK1N
SUSB#_PWR
+3VO
R6701 100KOhm
SUSC#_PWR_ON
Q6705A UMK1N
11/2
Q6705B UMK1N
SUSC#_PWR
+3VA <19,36,37,38,64,71>
+3VO <62,64>
+3V <18,19,23,25,27,28,30,31,33,34,36,37,38,51,64>
+3VSUS <17,19,20,22,30,34,37,38,51,52,62,64,69,70>
+3VS <2,5,6,8,11,12,13,14,15,16,17,18,19,20,21,23,24,26,27,28,29,33,34,35,38,41,43,44,45,46,51,52,61,70>
+3VAO <64>
+5VAO <62,63,65,70>
+5VA <36,37,38,62>
+5VSUS <36,38,62>
+5V <2,5,14,22,34,36,38>
+5VS <8,15,19,20,21,26,27,28,33,34,35,36,37,38,46,61>
+5VO <62,64,66,71>
+1.8VO <64,65>
+1.8V <2,4,5,6,9,38,65>
+1.8VS <13,39,40,45,47,48,49,50>
+1.2VO <63>
+1.2VS <9,10,11,12,13,20,39,40,41,63>
+1.2VS_HT <2,4,9,13,64>
+2.5VS <2,9,12,13,29,38,43,44,64>
+2.5VO <64>
+1.5VSUS <18,20,64>
+0.9V <4,7,38,64,65>
+12V <8,25,27,38>
+12VS <14,15,28,38>
+12VSUS <62>
+VCORE <4,8,61>
VGA_VCORE <66>
AC_BAT_SYS <14,38,61,62,63,64,65,66,68,71>
A/D_DOCK_IN <37,68,70,71>
BAT <68,69,71>
+5VCHG <68,71>
+5VLCM <34,36,69,70,71>
+2.5VREF <64,70,71>
+1.5VO <64>
+1.5VS <16,18,19,20,38,51,52,64>
<Variant Name>
Title : POWER_LOAD_SYSTEM
ASUSTECH
Engineer: Tanner Zhang
Size: Custom
Project Name: A7T
Rev: 2.0
Date: Sheet 67 of 71


input current 2.6A (charger)
LDO : 5.4V
REF : 4.2235V
Current share
114W 6.21A
12/30 ER
12/30 ER
12/2
3/9 PR
11/17
11/17
3/20
12/30 ER
3/7 PR
3/7 PR
1/11
ER
11/2
3/6 PR
3/6 PR
AD_IINP(5%) , R(0.7%) , 2.5VERF(0.2%) = 5.9%
114W / 19V * 0.941 = 5.646A
5.646A * 10mOHM = 56.46mV
59.43*3uA*10K = 1.694V
VINNP=Iin*RS*3uA*RINNP
If battery isn't in,disable the charger.
AC_IN Threshold 2.048Vmax A/D_DOCK_IN >17.46V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01 ohm
VCLS= 3.115V
=> Iin(max)=5.532A
=> Constant Power = 19 * 5.532A = 105W
Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.0V => Ichg = 2.492A
VICTL= 1.68V => Ichg = 1.4A
VICTL= 0.188V => Ichg = 157mA
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.591V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (tie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Title : POWER_CHARGE
ASUSTECH
Engineer: Tanner Zhang
Size Custom
Project Name A7T
Rev 2.0
Date: 星期三, 八月 02, 2006
Sheet 68 of 71

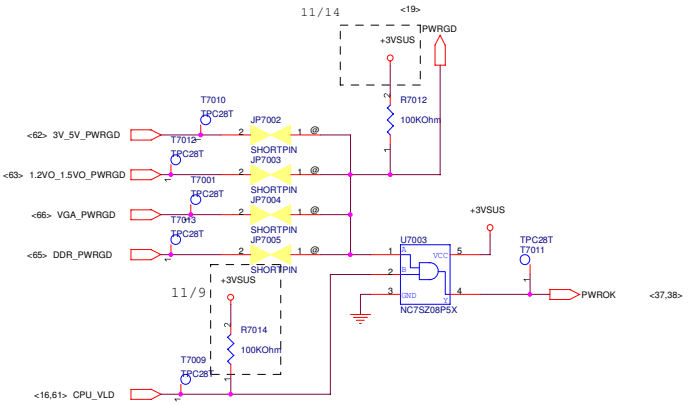


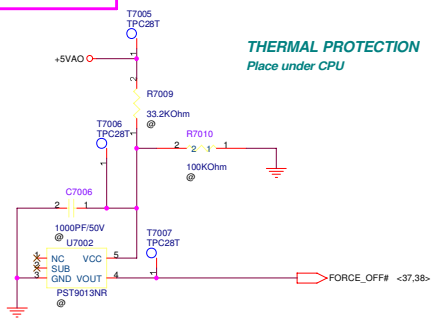


ASUSTECH	Title : Power_PI		
	Engineer: Tanner Zhang		
Size: Custom	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 69 of 71		



3/7 PR

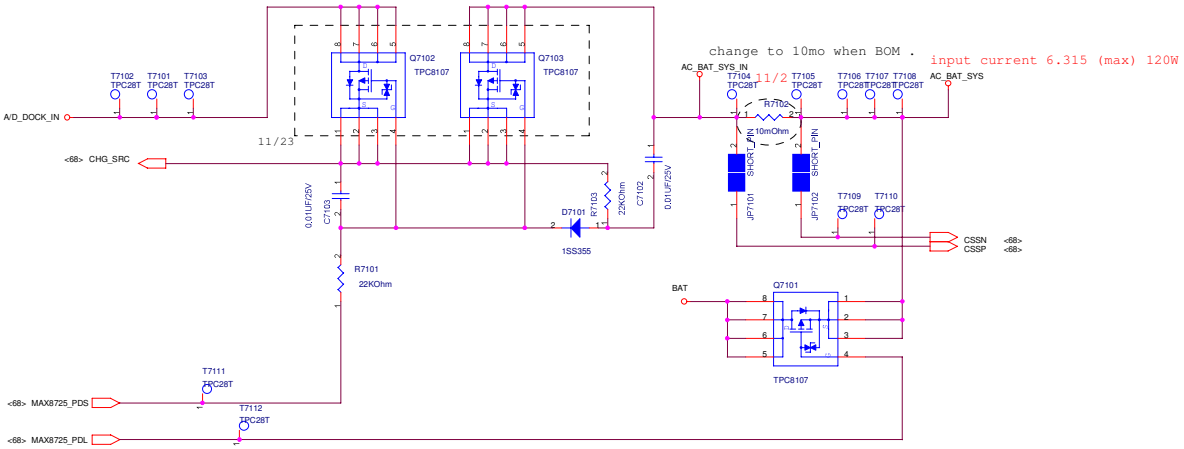


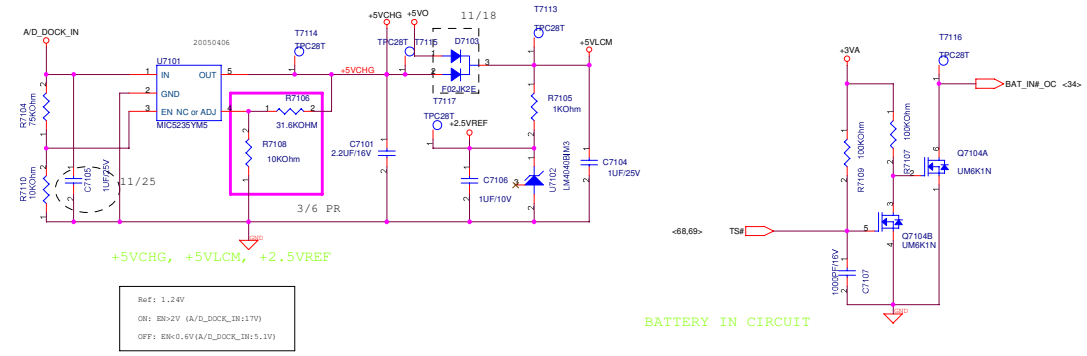


THERMAL PROTECTION

Place under CPU

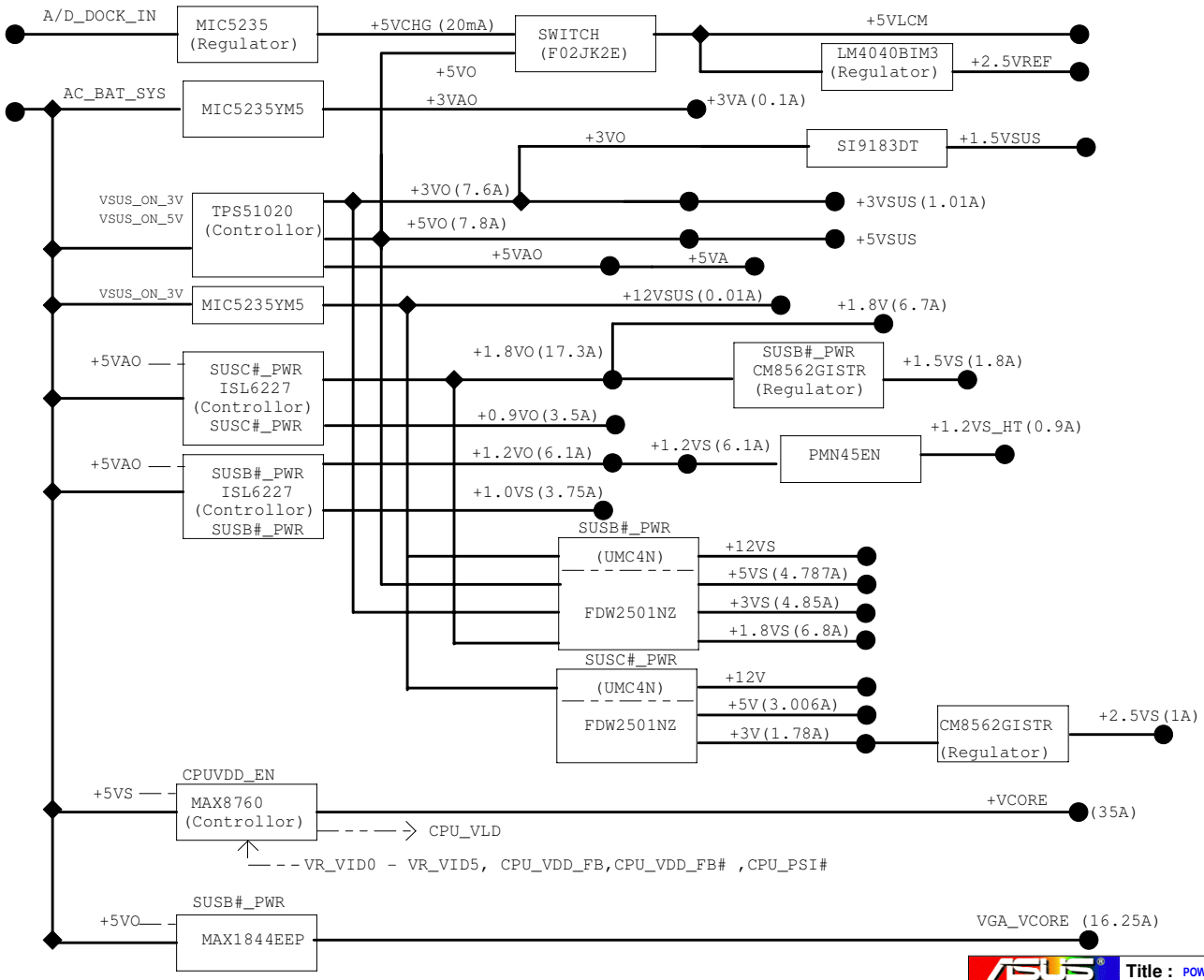
ASUSTECH	Title : POWER_PROTECT	
	Engineer: Tanner Zhang	
Size: Custom	Project Name: A7T	Rev: 2.0
Date: 星期十, 八月 02, 2006	Sheet 70 of 71	





BATTERY IN CIRCUIT

ASUSTECH	Title : POWER_SWITCH_5VLCM	
	Engineer: Tanner Zhang	
Size: Custom	Project Name: A7T	Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 71 of 71	



ASUSTECH	Title : POWER FLOWCHART		
	Engineer: Tanner_Zhang		
Size: Custom	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 72 of 73		

Revision History

Power

R1.0

2006.01.03

1.Add 150UF/4V (15mohm) to +3VO output for the gate Feq. is wrong.
2.change c6708.1 to Q6710.2 for +5vs's gate softstart.
3.change R6135 to 120K for Vcore OCP set
4.Add 1uf/25V to VGACORE input for gate noise.
5.change C6703 to N/A for load switch 1.2VS_HT gate
6.Change R6506 to 470ohm.and R6509 to 100Kohm for 1.8V ocp set
7.add R6825 15Kohm and change R6818 to 4.7Kohm for AC_IN wrong motion.
8.Change C6807 to 4.7uf/25V for AD_IN noise
9.Remove JP6303
10.Change R6602 0ohm to 2.7ohm(0603 5%) for vgacore high side gate noise
11.Change Q6702 to SI4800 for 1.2vs_HT low voltage.
12.Change R6606 to 1K (0603 1%) for VGACORE output 1.02V
13.Change R6807 to 29.4K(0603 1%) for current share point set.
14.For PWRLMT# 114w,change R6823 to 100k(0603 0.1%),and change R6824 to 90.9K(0603 1%)
15.change R6511 to 9.76K(0603 1%) for 1,8vs voltage set.
16.Change R6312 R6314 to 7.5K(0603 1%) for 1.2vs voltage set.
17.Change R6411 to 24.3K.(0603 1%) for 1.5VSUS voltage set.
18.C6411 change to @

2006.01.04

1.change C6217 to 4.7UF/25v(0805)11G235247512320
2.change C6807 to 1uF/25V(0805) 11G235310532360
3.change C7105 to 1UF/25V(1206) 11G236110512320

2006.01.05

1.Change PAGE 68 MAX8725_LDO to MAX8725_REF.
2.change R6814 (49.9K) to 97.6k(1%)10G213976213030
Change R6812(1.5K) to 1.91K(1%) 10G213191113030
Change R6811(22.6K) to 36.5k(1%) 10G213365213010
Change R6809(53.6k) to 40.2K(1%) 10G213402213030
Change R6815(22.6k) to 24.3K(1%) 10G213243213030
Change R6807(40.2k) to 14.3K(1%) 10G213143213030
Change R6813(55.1k) to 40.2K(1%) 10G213402213030

2006.01.06

1.change L6501 to 1.8UH(09G02X183100) for 0.9 transit ripple.
2.for battery OVP 17.25V, change R7001(200k 0.1%) to 301K(0.1%) 10G213301323030
Change R7007(100K 0.1%) to 51K(0.1%) 10G213510223030
Set R7008 to @ When A7M bom
3.change L6202 to 2.8uh. (09G02X183100)
4. add Q6807 for auto battery learning error.

System

R1.0

ASUSTECH	Title : HISTORY	
	Engineer: Tanner_Zhang	
Size: Custom	Project Name: A7T	Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 73 of 73	