To our valued customers

I want to express my thanks to you for being interested in our products and for having confidence in LogiFind International CO,. Ltd.

The primary aim of our company is to design and produce high quality electronic products and to constantly improve the performance thereof in order to better suit your needs. Please share your thoughts and feelings regarding our operation so that we can serve you better in the future. I thank you for your continued support and patronage.
Your Dream is our Destination!

Sincerely,

Owner and General Manager
of LogiFind International CO,. Ltd.

CONTENTS

What's AX309 Development Board

Introduction

The purpose of this manual is to describe the functionality and contents of the **AX309** development board. This document includes instructions for operating the board, descriptions of the hardware features, and explanations of the test code programmed into the on-board programmable memory. For reference design documentation and example projects, see the official website:**www.LogiFind.com**

Description

The AX309 development board provides a complete hardware environment for designers to accelerate their time to market.The kit delivers a stable platform to develop and test designs targeted to the low-cost and low-power Xilinx Spartan-6 FPGA. The installed Spartan-6 FPGA LX9 device offers a prototyping environment to effectively demonstrate the enhanced benefits of low-cost Xilinx FPGA solutions. Reference designs are included with the kit to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

The **AX309** development board contains the following individual pieces:

- ●The easyFPGA-Spartan-6 development board
- ●USB 2.0 cable
- ●Xilinx ISE® Design Suite (IDS) 14.7
- ●Example Source Code
- ●AX309 Development Board Users Manual
- ●Transparent protection board

Please note that this kit does **NOT** include a Xilinx programming cable.

Block Diagram of the Board

Figure 1 gives the block diagram of the **AX309** development board. To provide maximum flexibility for the user, all connections are made through the Xilinx Spartan-6 FPGA device. Thus, the user can configure the FPGA to implement any system design.

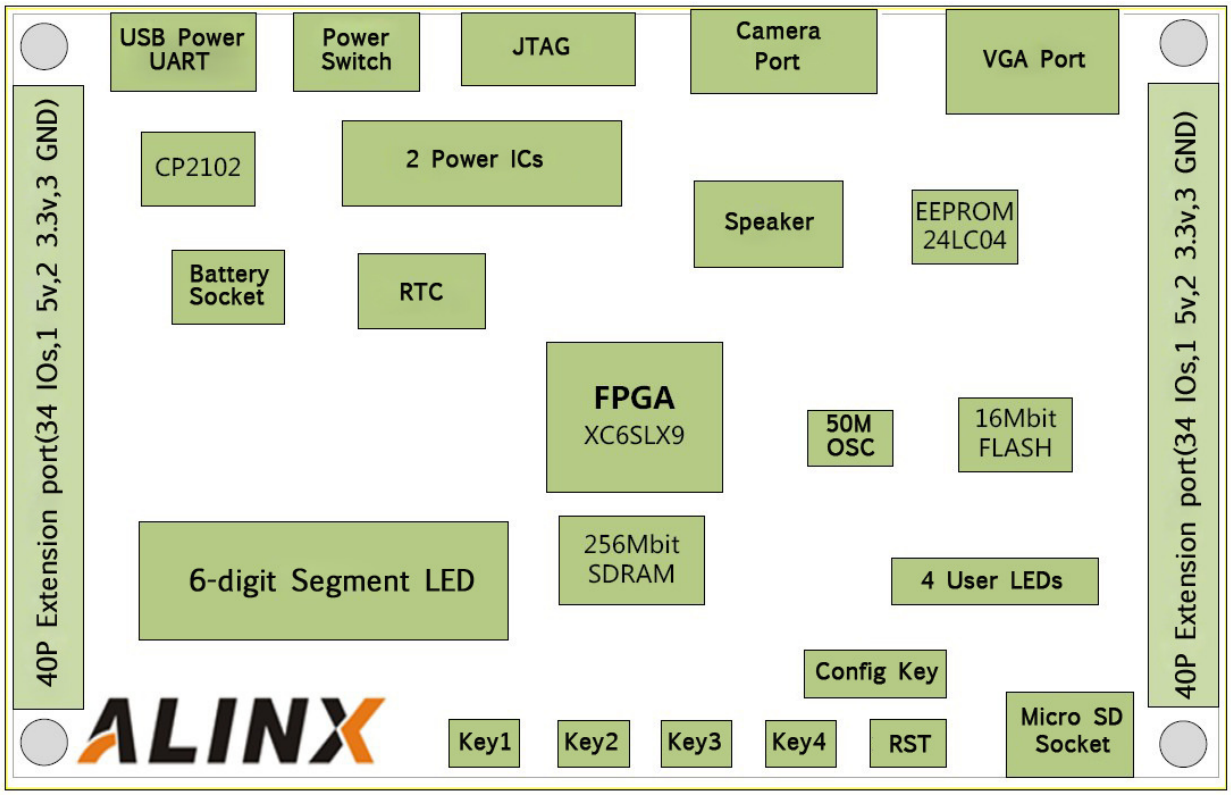

Figure 1. Block Diagram

Following is more detailed information about the blocks in **Figure 1**:

FPGA

Xilinx Spartan-6 XC6SLX9 FPGA

JTAG Port

On-board JTAG Port for programming

SDRAM

256Mbit SDRAM

SPI Flash memory

64Mbit SPI FLASH

Camera Port

Supports 5000000 pixels OV5640 module

Pushbutton switches

4 User Keys

Normally high; generates one active-low pulse when the switch is pressed

General User Interfaces

4 User LEDs

6-digit 7-segment displays

Buzzer

System Clock inputs

50MHz oscillator

RTC Module

Comes with a CR1220 battery socket

External Eeprom

Comes with a 24LC04;

VGA output

Uses a 16-bit resistor-network DAC under RGB65536 Mode

With 15-pin high-density D-sub connector

Voltage Regulator Circuit

Provides 1.2V,5V and 3.3V for system power supply

Micro SD

Equips a Micro SD card holder.

On-board USB to TTL/RS232 Module

Use cp2102 for USB-TTL/RS232 Converting (Without DB-9 serial connector)

40-PIN Expansion Headers

Two Channels 40-PIN Expansion Headers Spartan-6 I/O pins, as well as 3 power and ground lines, are brought out to the 40-pin expansion connectors. You can install 4.3"TFT module and AD/DA module by our company on this two expansion headers.

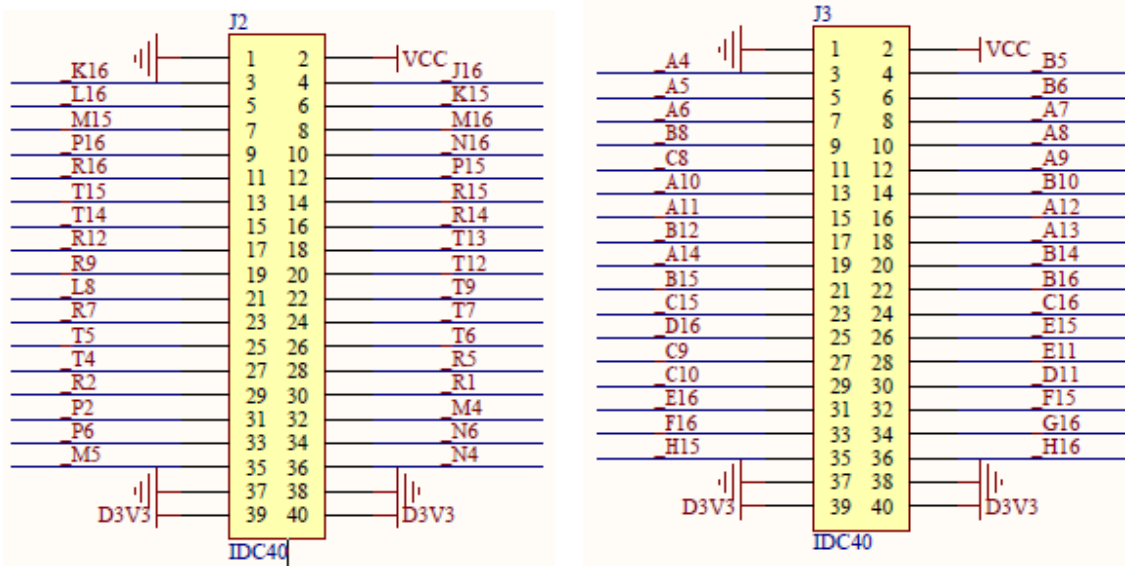

Figure 2. 40-PIN Expansion Headers

Test Files

Files that are used to factory test the **AX309** development board are available and can be found on the LogiFind Company website: **www.LogiFind.com.**

What's on Board

Figure 3. What's on Board

A photograph of the **AX309** development board is shown in following **Figure 3**. It depicts the layout of the board and indicates the location of the connectors and key components.

The following hardware is provided on the **AX309** development board:

Tab1.Baord Source

1	**Xilinx XC6SLX9**	**2**	**256Mbit SDRAM**
3	**FLASH 16Mbit**	**4**	**USB to UART cp2102**
5	**USB/USB Power**	**6**	**Power Switch**
7	**JTAG Port**	**8**	**Camera Port**
9	**VGA Port**	**10**	**SD card**
11	**RTC DS1302**	**12**	**Reset and 4 User Buttons**
13	**6-digit LED Display**	**14**	**EEPROM 24LC04**
15	**4 User LEDs**	**16**	**50Mhz System Clock**
17	**Buzzer**	**18**	**Power Circuit**
19	**40PIN Expansion Port**	**20**	**40PIN Expansion Port**

Software

ISE Installation

Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs , enabling the developer to synthesize ("compile") their designs , perform timing analysis, examine RTLdiagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

With the 14.7 release, it now moves into the sustaining phase of its product life cycle. In the future, while there are no more planned ISE major releases, you will continue to receive Xilinx's superior technical support and Xilinx may release periodic updates and patches. If you have not already done so, Xilinx recommends signing up for "My Alerts" at http://www.xilinx.com/support/answers/18683.htm to keep you informed.You can download the ISE software from the Xilinx official website: http://www.xilinx.com/support/download.html, and of course,you can contact us for this software.The ISE is a big software and we recommend 64-bit win OS,4GB memory(or higher) of your computer.The followings shows how to install it in your computer.

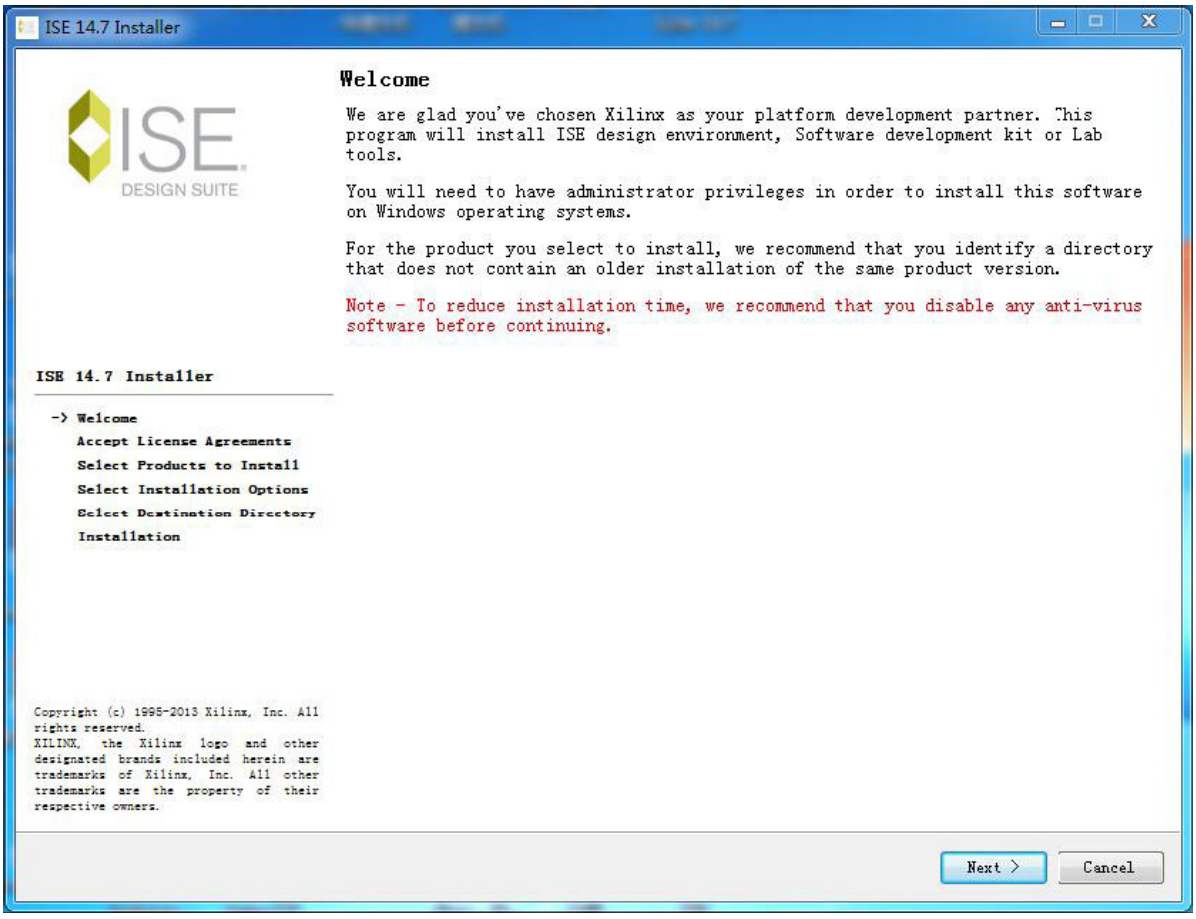

Figure 4. Run the ISE Installer

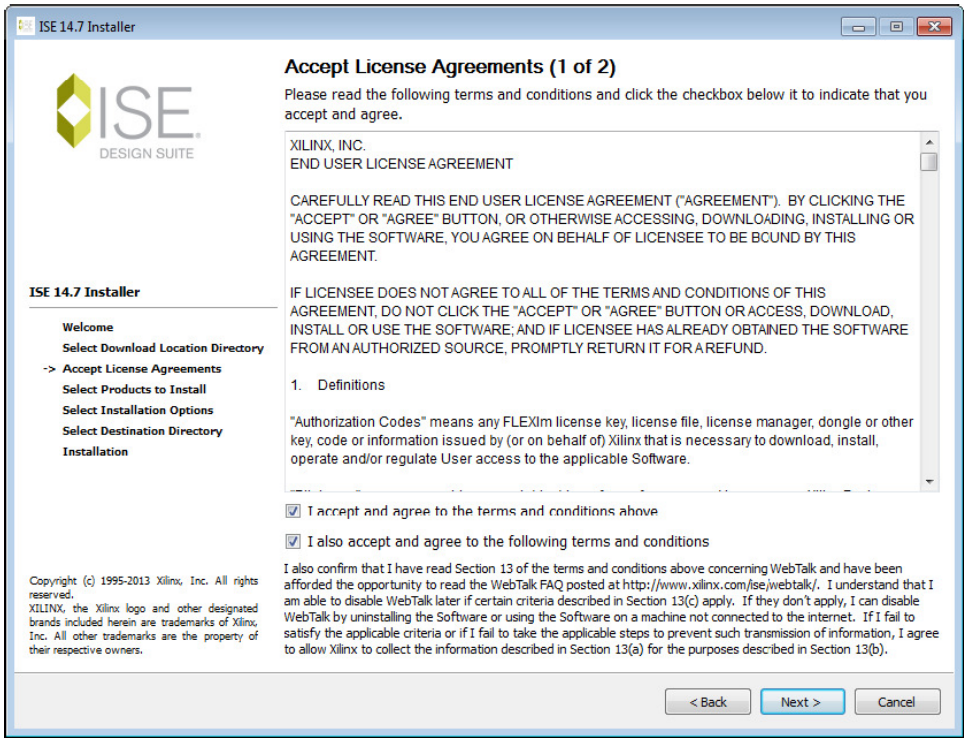

Figure 5. Accept License Agreements (1 of 2)

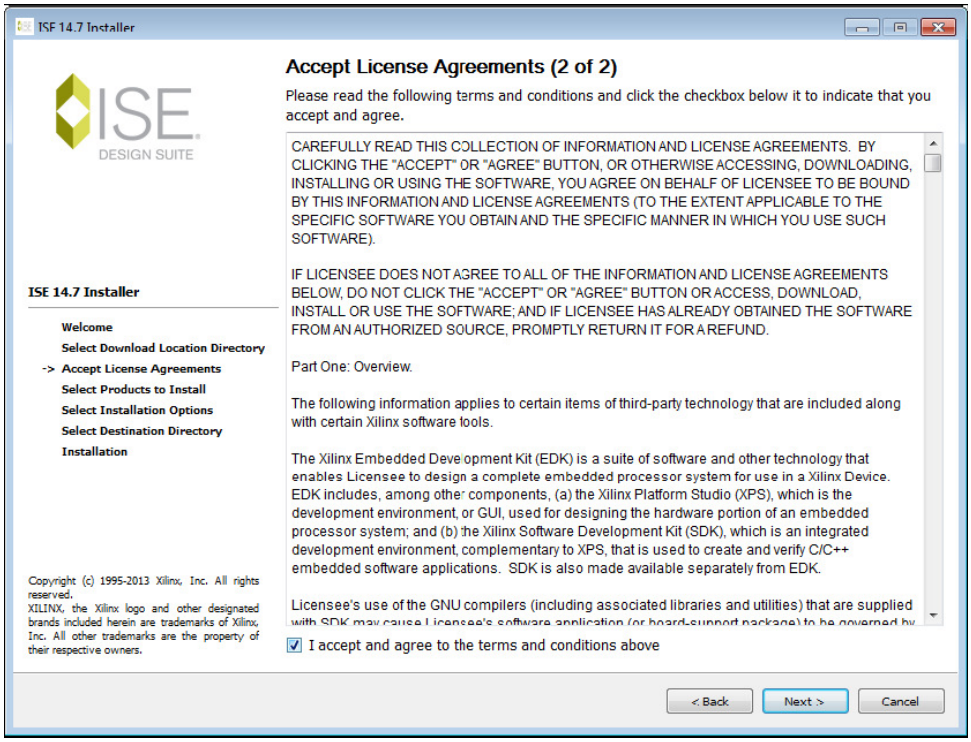

Figure 6. Accept License Agreements (2 of 2)

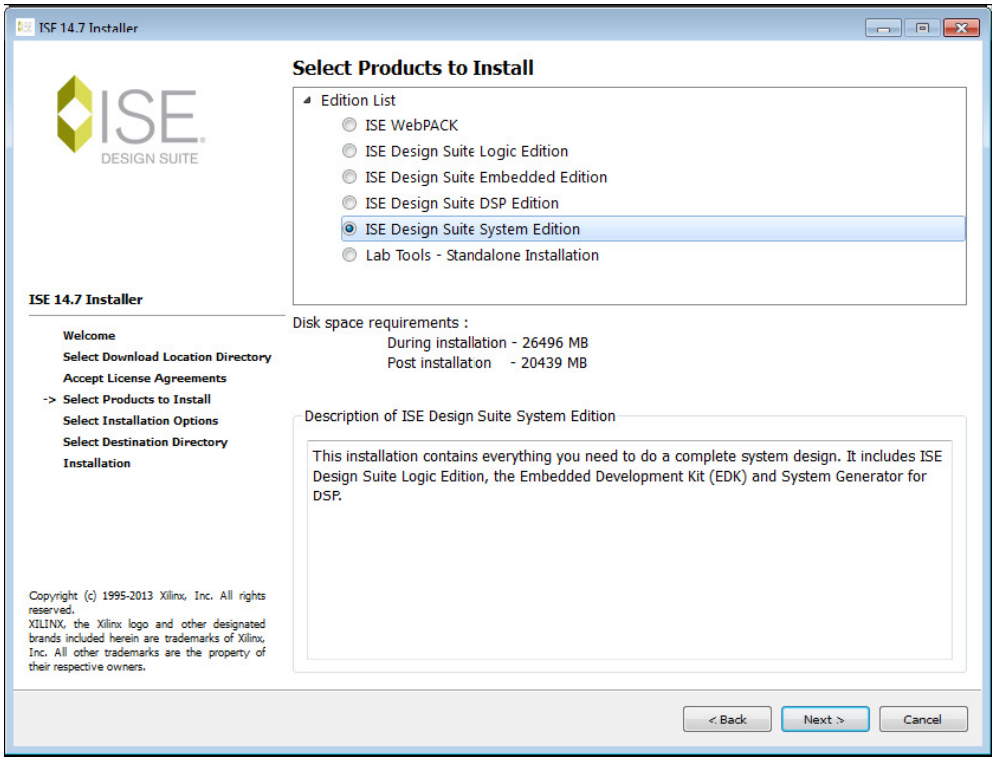

Figure 7. Select Products to Install

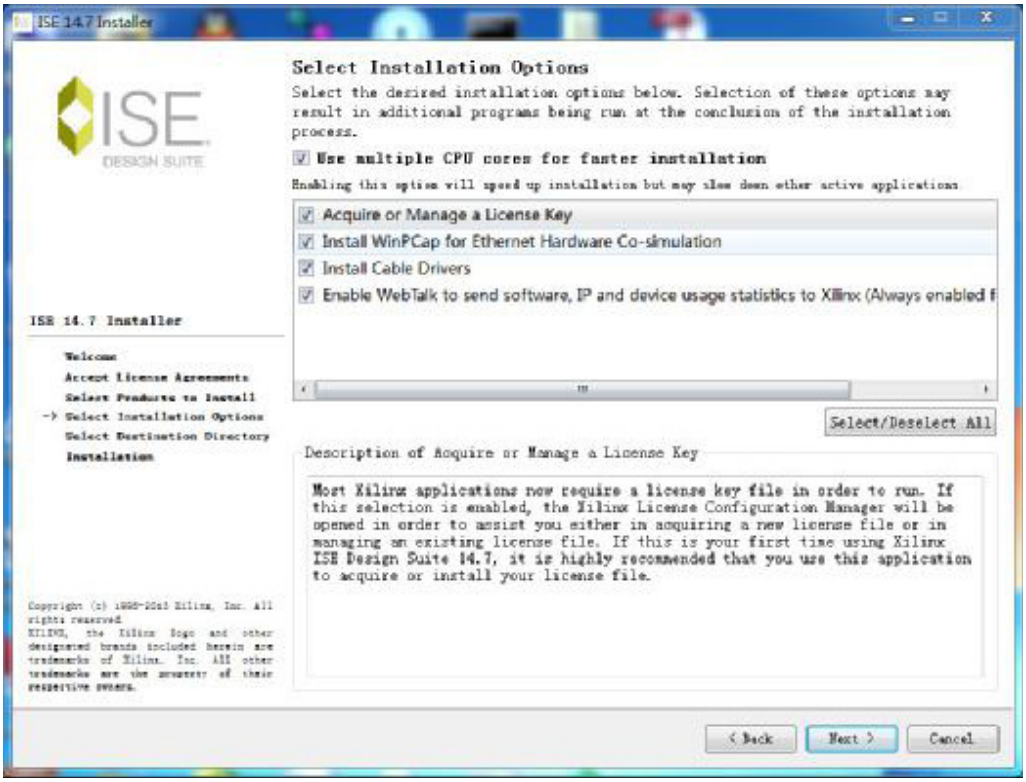

Figure 8. Select Installation Options

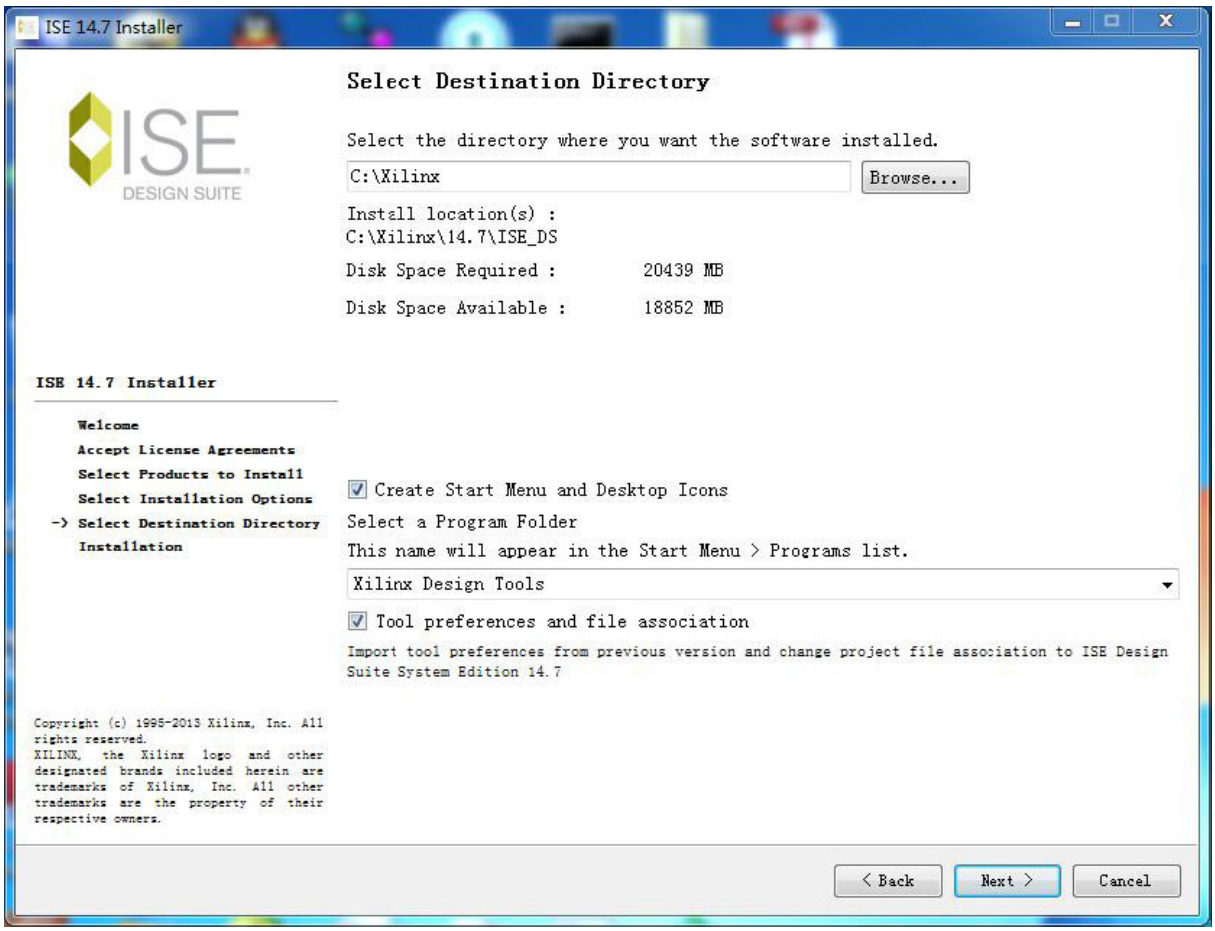

Figure 9. Select Destination Directory

Create a new project

Run the ISE "Project Navigator" software.

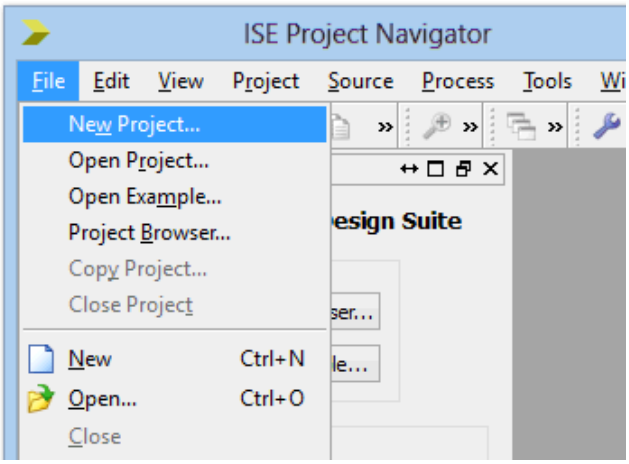

Figure 10. Select "New project"

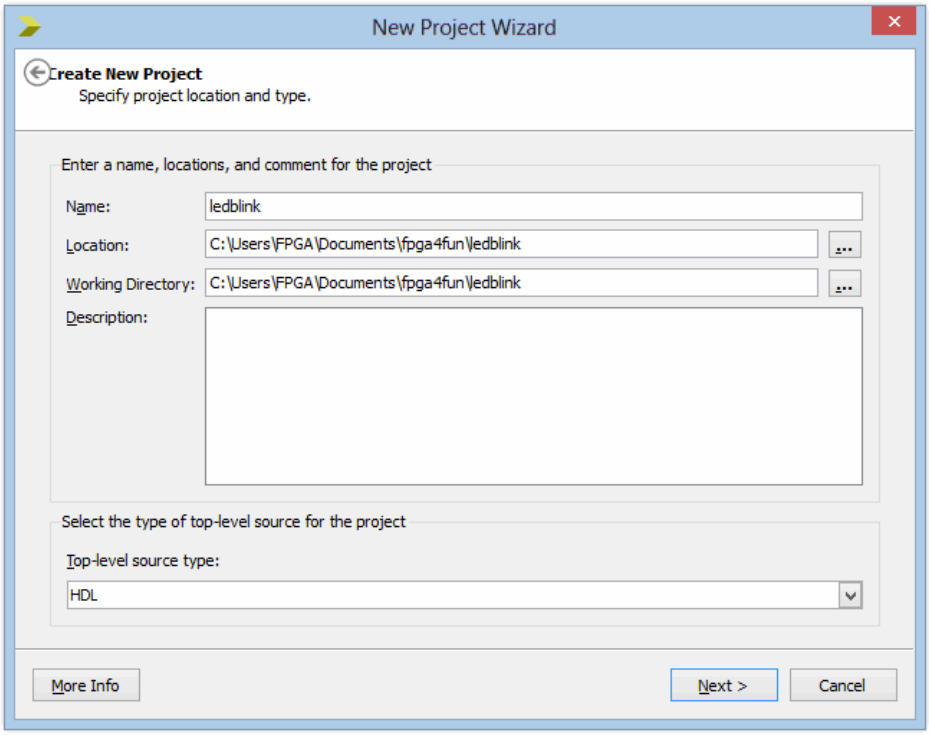

Figure 11. Choose a project name and directory,then click next

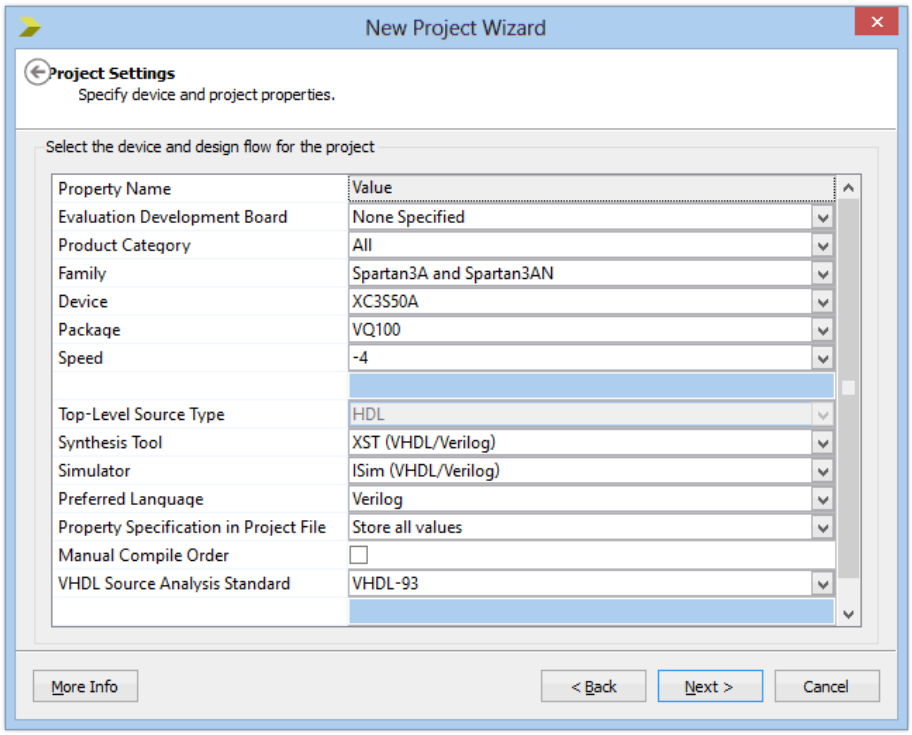

Figure 12. Select the devic,click "Next" and "Finish"

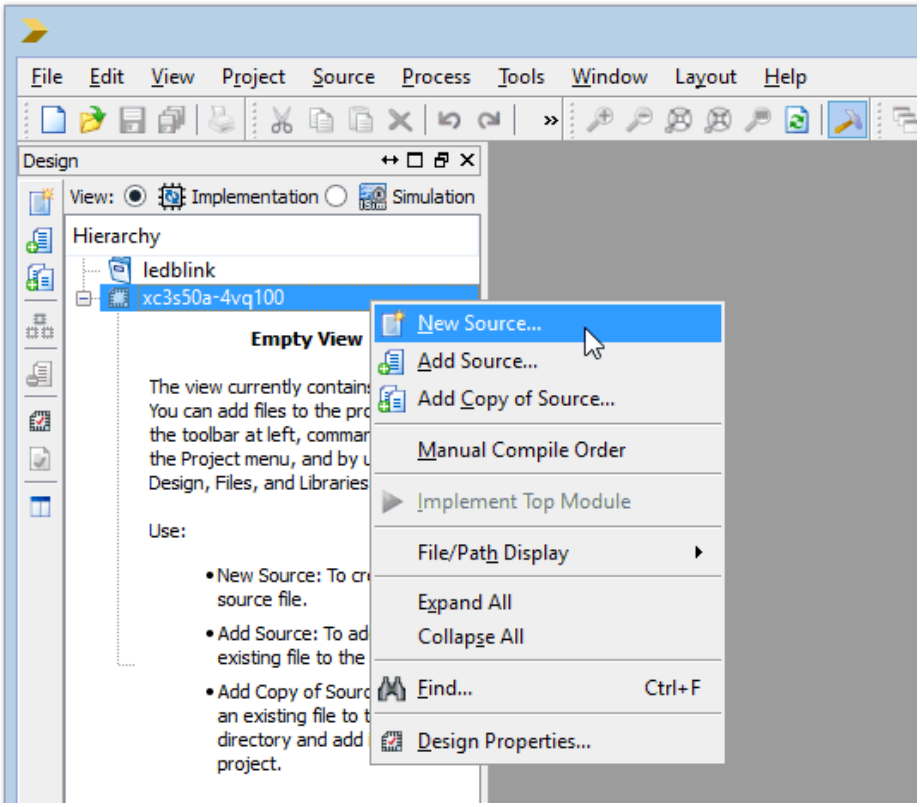

Figure 13. Click "New Source"

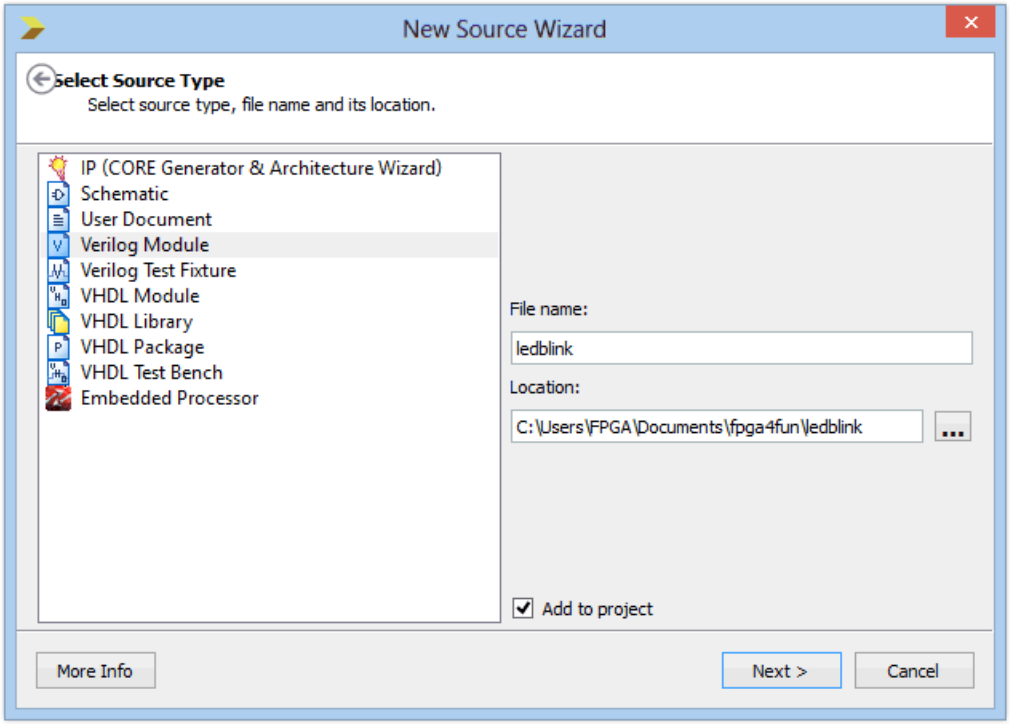

Figure 14. Select "Verilog Module" and give it a name

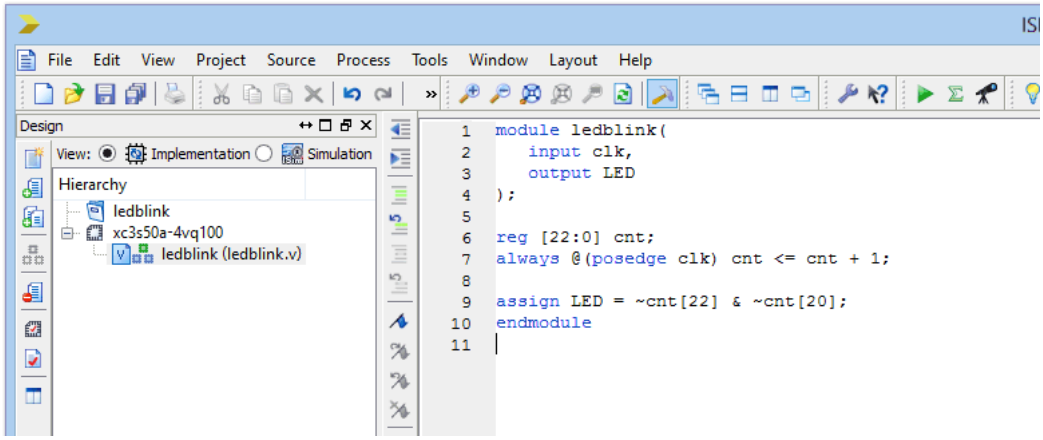

Figure 15. Type text and save

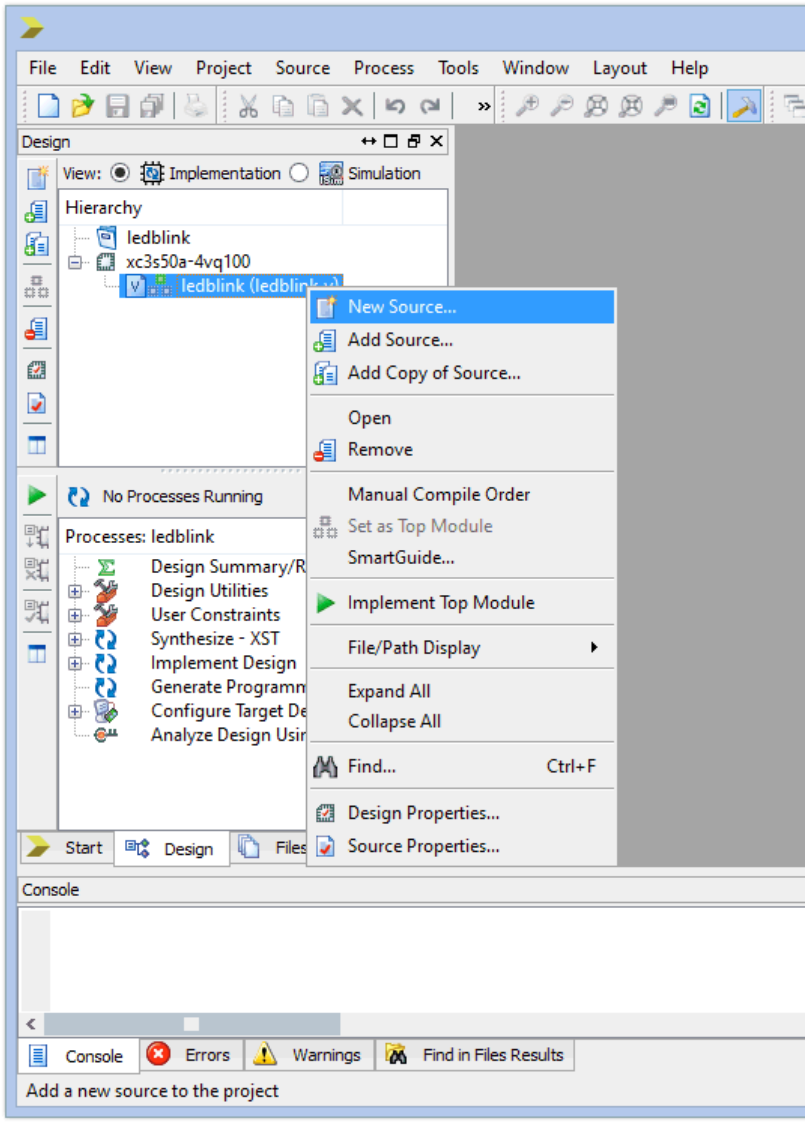

Figure 16. Click "New Source" again to Assign the pins

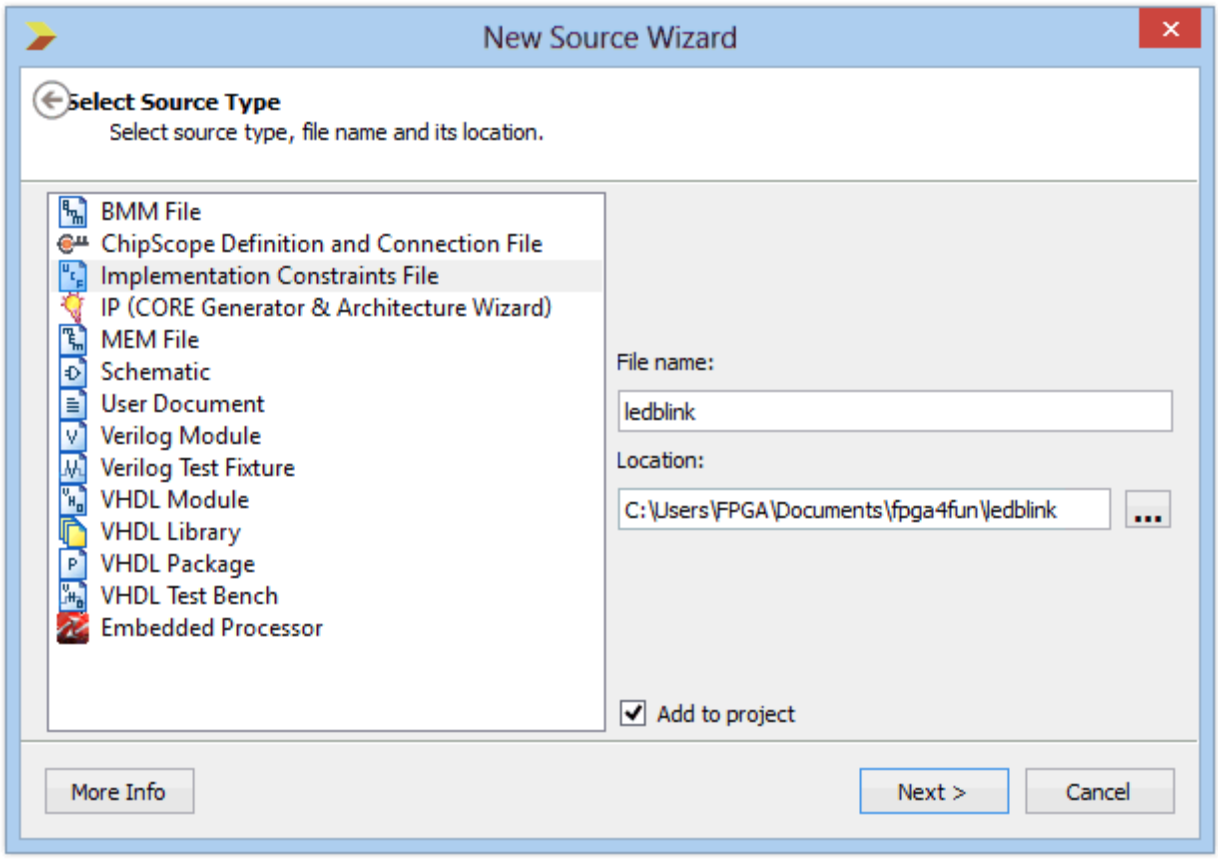

Figure 17. Select "Implementation Contraints File", give it a name

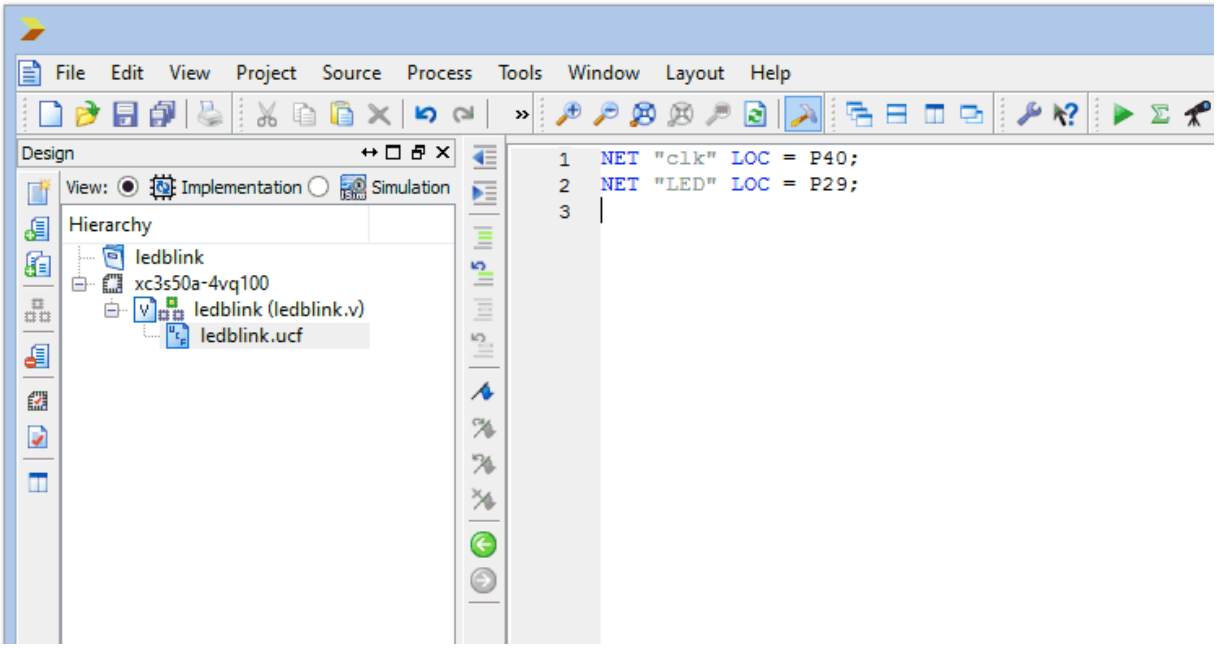

Figure 18. Type the test before saving

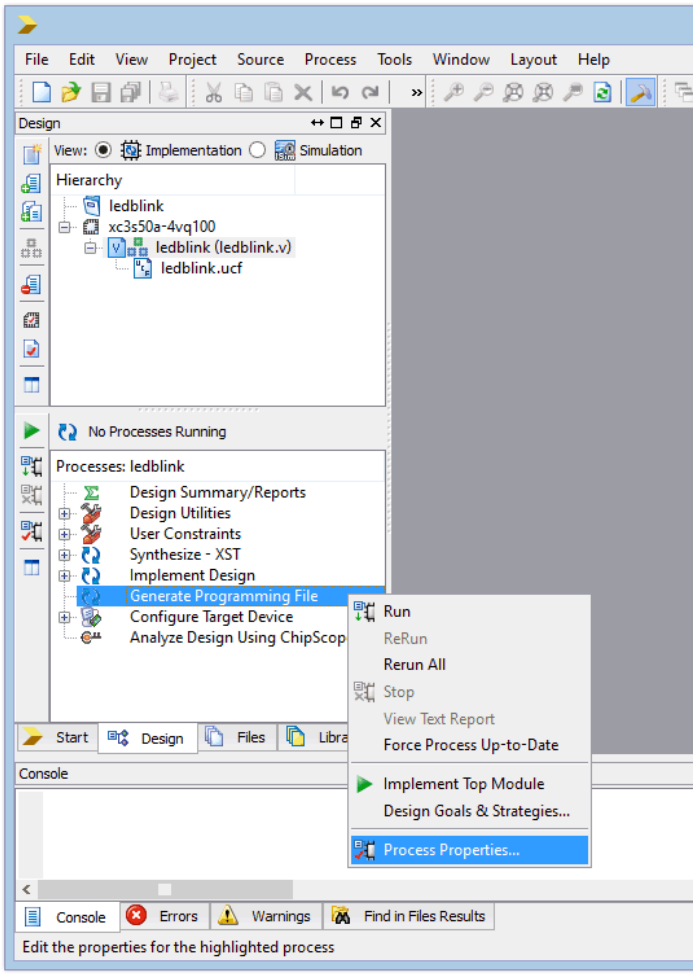

Figure 19. Select the "ledblink" top level, then get to Set the programming properties

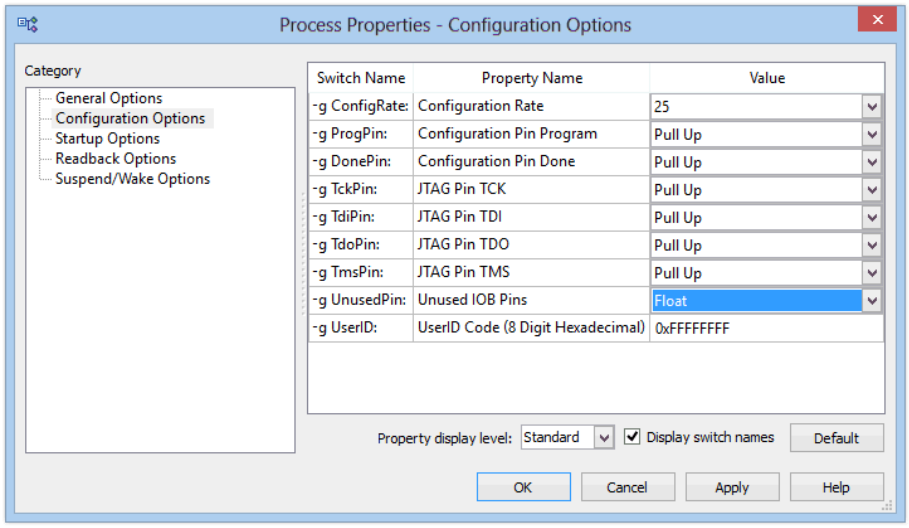

Figure 20. Make sure to float the unused pins

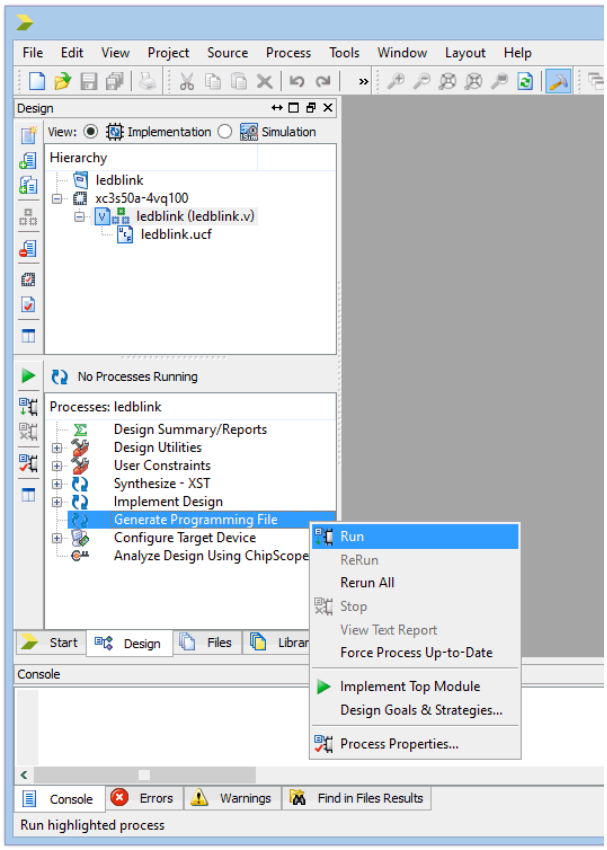

Figure 21. Select "Run" and wait a few tens of seconds

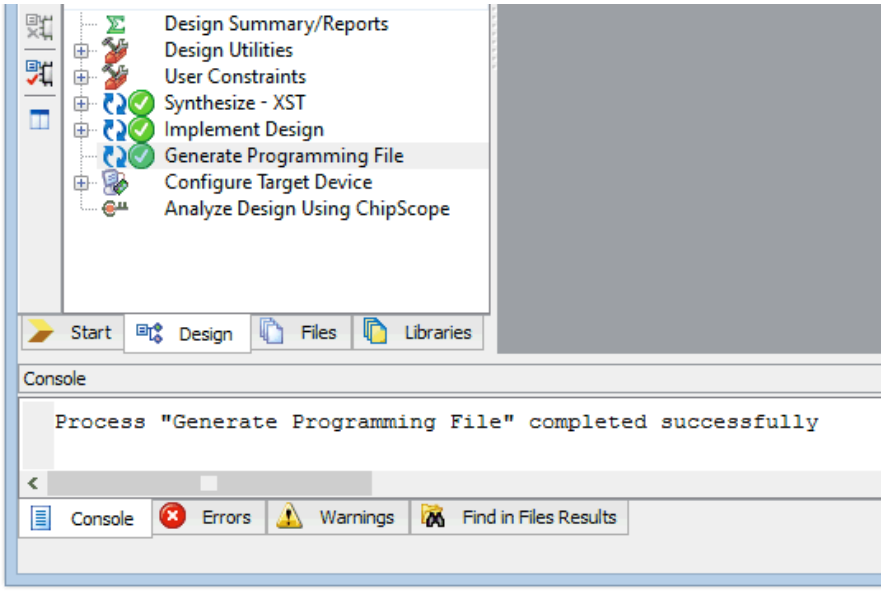

Figure 22. Generate the FPGA programming file

Hardware

Power Supply

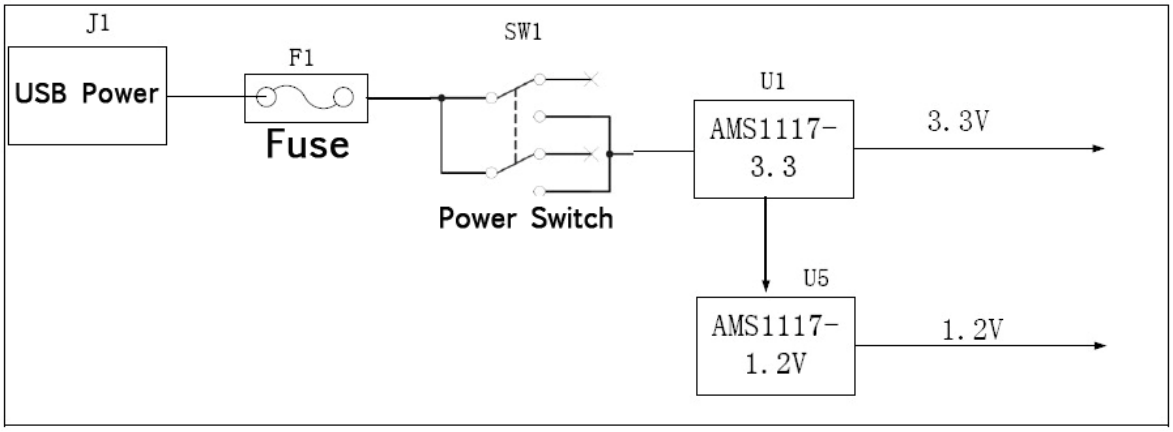

Figure 23. Power Supply

AX309 development board powered via a mini USB cable. AX309 provides two channels LDO voltage:+ 3.3V and + 1.2V, which meet the FPGA BANK voltage and core voltage requirement.

We design the PCB in 4 layer, and reserve for independent GND, so that the entire board has a whole layer for ground to ensure that the board has a very good stability. We reserve many power supply test points so that the users confirm the voltage on board very easily.

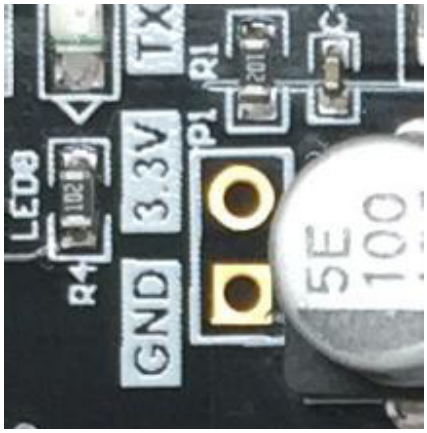

Figure 24. Power Supply Test Point

JTAG Port

AX309 equips a standard JTAG Port for uploading firmware into the Xilinx chip on board.

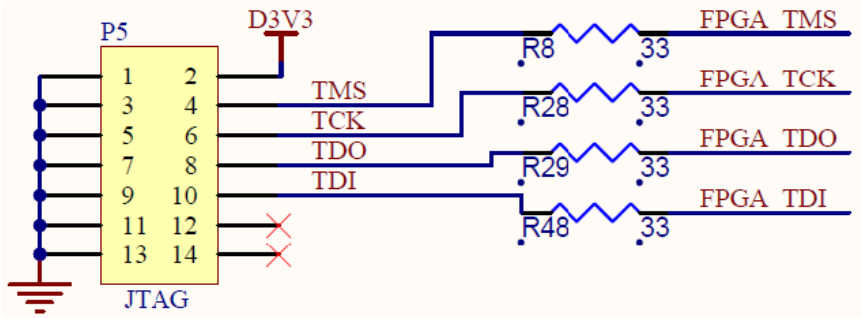

Figure 25. JTAG Port

System Clock

AX309 equips a 50MHz OSC for system clock source. The oscillator output is connected to the FPGA's global clock (GCLK Pin T8).GCLK can be used to drive the user logic unit circuit inside the FPGA. We can also get higher frequency clock via configuring the FPGA's internal PLLs and DCMs.

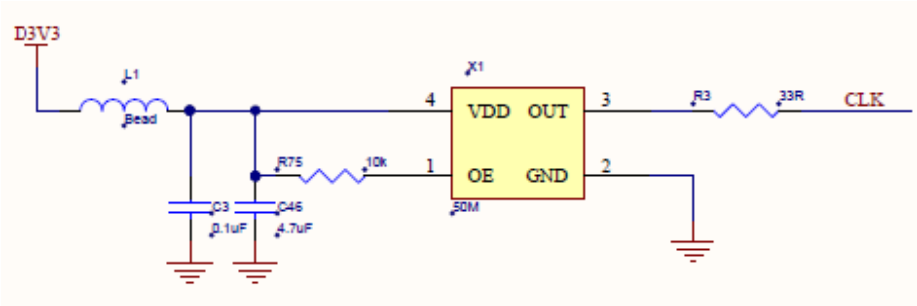

Figure 26. System Clock Source

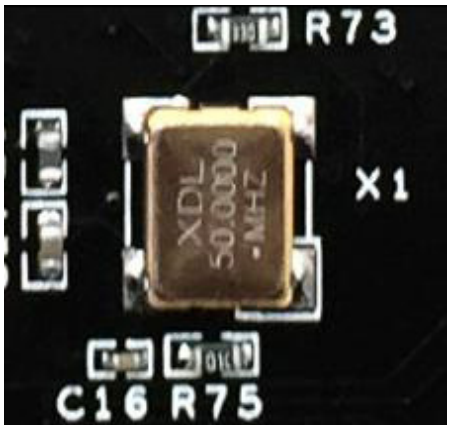

Figure 27. System Clock Source on board

QSPI Flash

AX309 Development board equips a 64Mbit SPI FLASH chip M25P16, which uses standard 3.3V CMOS voltage. Because of its non-volatile characteristics, SPI FLASH can be used as FPGA's system boot image which include bit file, soft-core application code and other user data files.

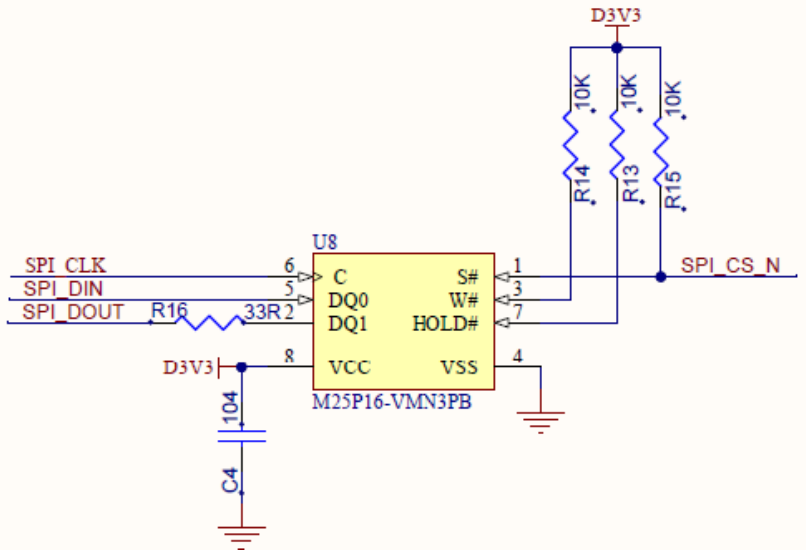

Figure 28. SPI Flash Circuit

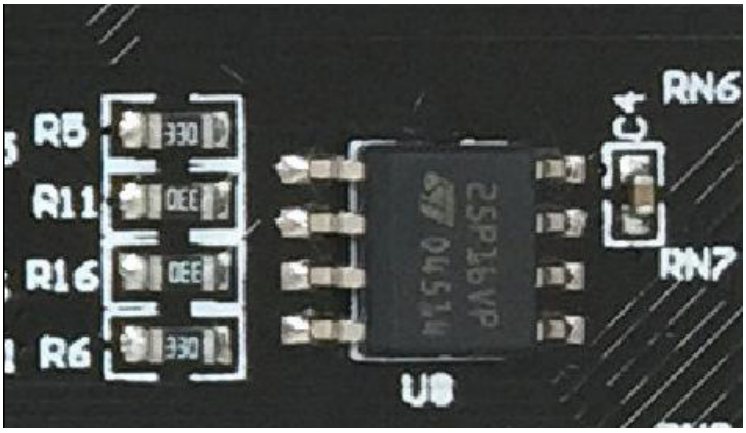

Figure 29. SPI Flash on board

Tab2. Pin Configuration for SPI Flash experiment

Signal Name	FPGA PIN
SPI_CLK	R11
SPI_CS_N	T3
SPI_DIN	T10
SPI_DOUT	P10

SDRAM

AX309 equips a 256Mbit (16M*16bit) SDRAM HY57V2562GTR, which is used for data cache.For example, we collect camera data, and temporarily stored in the SDRAM, and then display through the VGA screen.

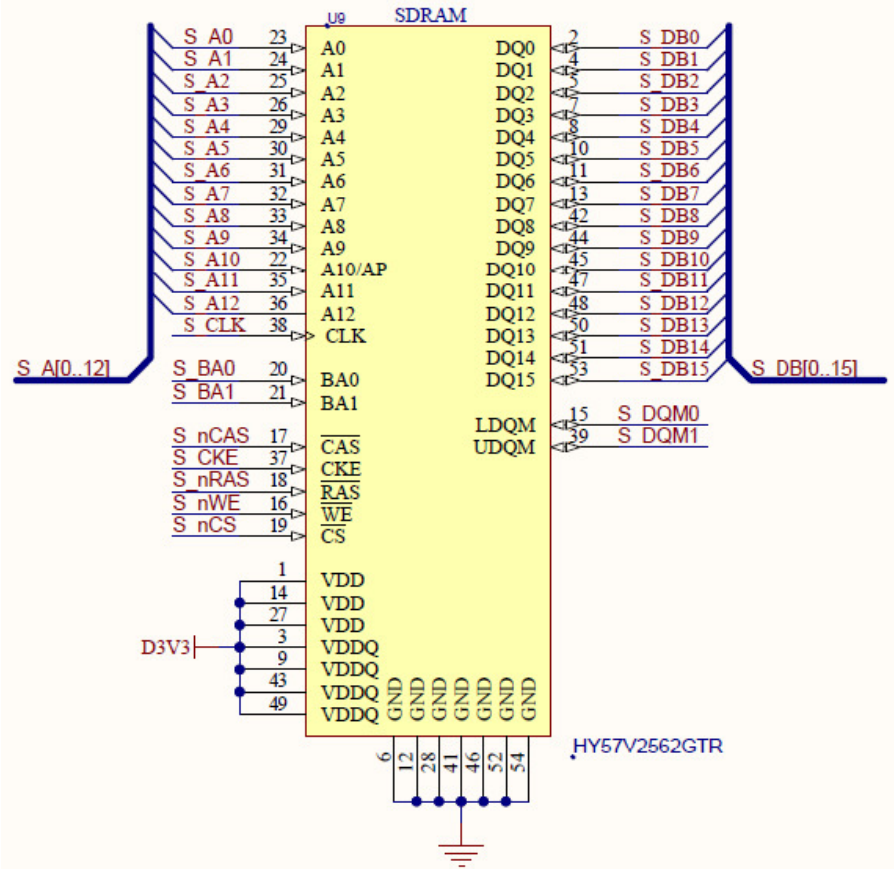

Figure 30. SDRAM module circuit

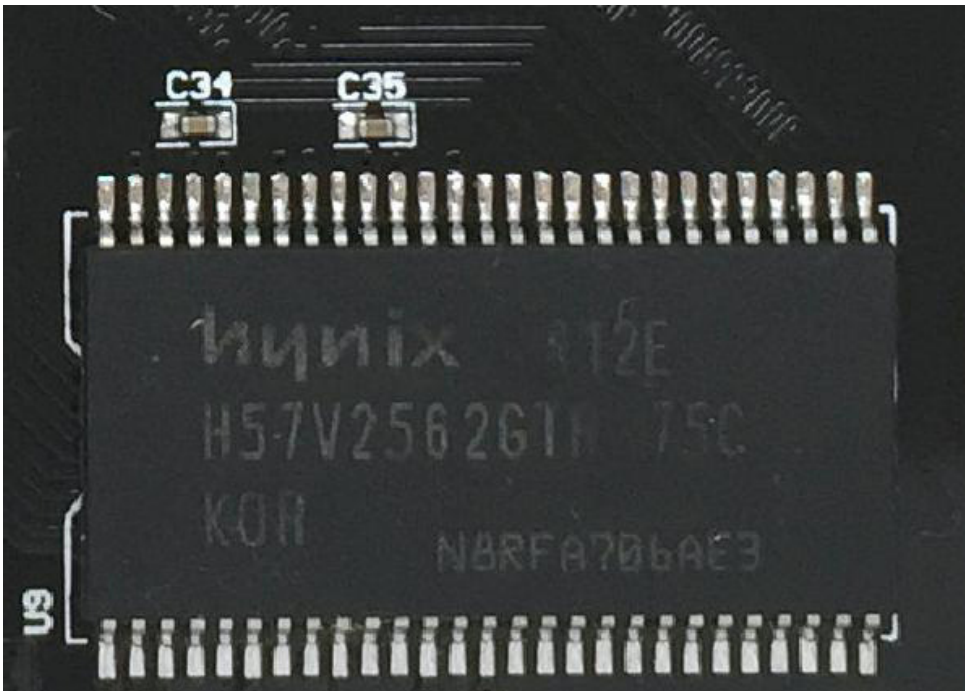

Figure 31. SDRAM module on board

Tab3. Pin Configuration for SDRAM experiment

Signal Name	FPGA PIN
S_CLK	H4
S_CKE	H2
S_NCS	G1
S_NWE	E1
S_NCAS	F2
S_NRAS	F1
S_DQM<0>	E2
S_DQM<1>	H1
S_BA<0>	G6
S_BA<1>	J6
S_A<0>	J3
S_A<1>	J4
S_A<2>	K3
S_A<3>	K5
S_A<4>	P1
S_A<5>	N1
S_A<6>	M2
S_A<7>	M1
S_A<8>	L1
S_A<9>	K2
S_A<10>	K6
S_A<11>	K1
S_A<12>	J1
S_DB<0>	A3
S_DB<1>	B3
S_DB<2>	A2
S_DB<3>	B2
S_DB<4>	B1
S_DB<5>	C2
S_DB<6>	C1

S_DB<7>	D1
S_DB<8>	H5
S_DB<9>	G5
S_DB<10>	H3
S_DB<11>	F6
S_DB<12>	G3
S_DB<13>	F5
S_DB<14>	F3
S_DB<15>	F4

EEPROM 24LC04

EEPROM is short for Electrically Erasable Programmable Read Only Memory. It is usually a secondary storage memory in devices containing data that is retained even if the device looses power supply. Because of the ability to alter single bytes of data, **EEPROM** devices are used to store personal preference and configuration data in a wide spectrum of consumer, automotive, telecommunication, medical, industrial, and PC applications. **AX309** equips a 4Kbit (2 * 256 * 8bit) **EEPROM** 24LC04.

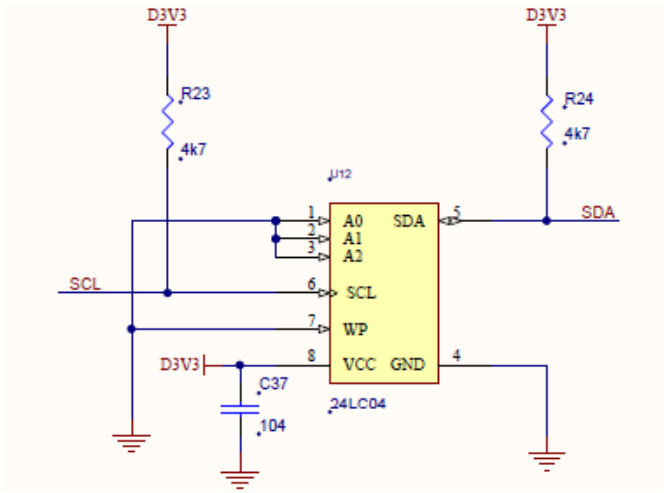

Figure 32. EEPROM module

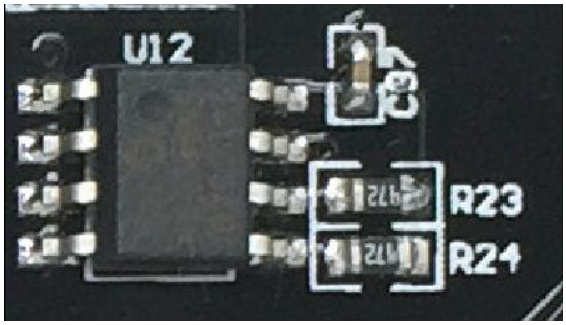

Figure 33. EEPROM module on board

Tab4. Pin Configuration for EEPROM experiment

Signal Name	FPGA PIN
SDA	P12
SCL	N12

Real Time Clock DS1302

The **DS1302** trickle-charge timekeeping chip contains a real-time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. Only three wires are required to communicate with the clock/RAM: RST, IO (data line), and SCLK (serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The **DS1302** is designed to operate on very low power and retain data and clock information on less than 1μW. The **DS1302** has dual power pins, one for primary and another for backup.

AX309 equips a **DS1302** module with a CR1220 battery holder.

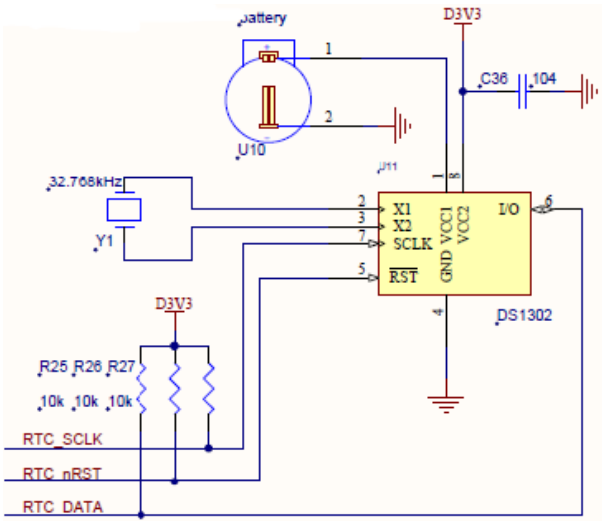

Figure 34. DS1302 module

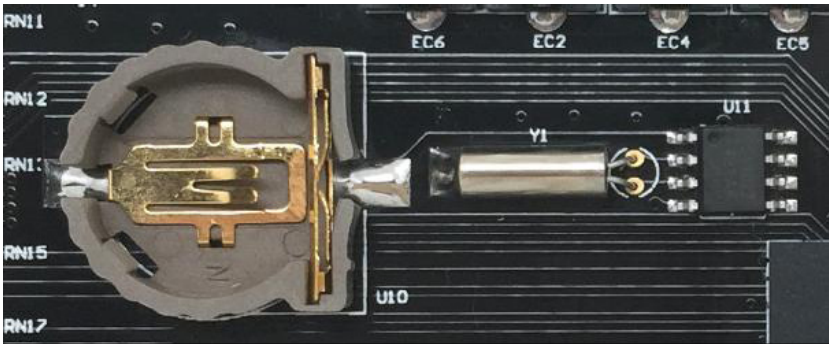

Figure 35. DS1302 module on board

Tab5. Pin Configuration for RTC experiment

Signal Name	FPGA PIN
RTC_SCIK	E13
RTC_nRST	C13
RTC_DATA	D14

CP2102 USB to UART

Modern PC computers, laptops and notebooks are no longer equipped with RS-232 connectors and UART controllers. They are nowadays replaced with USB connectors and USB controllers. Still, certain technology enables UART communication to be done via USB connection. CP2102 from SILICON® convert UART signals to the appropriate USB standard. In order to use USB-UART module on AX309, you must first install cp2102 drivers on your computer. Drivers can be found on the Product DVD and also download in this link: **https://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx**

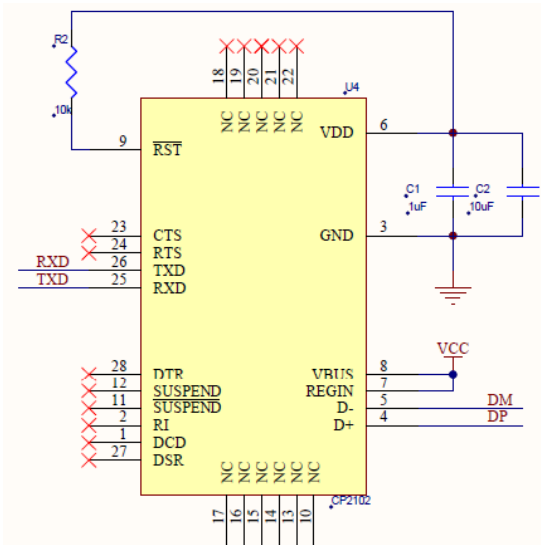

Figure 36. CP2102 module

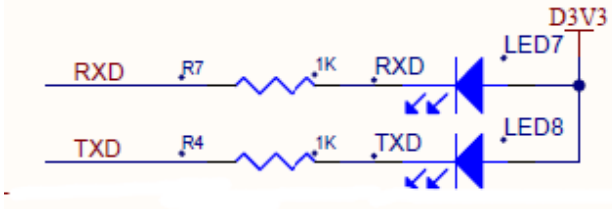

Figure 37. Two LEDs for RXD and TXD indicator

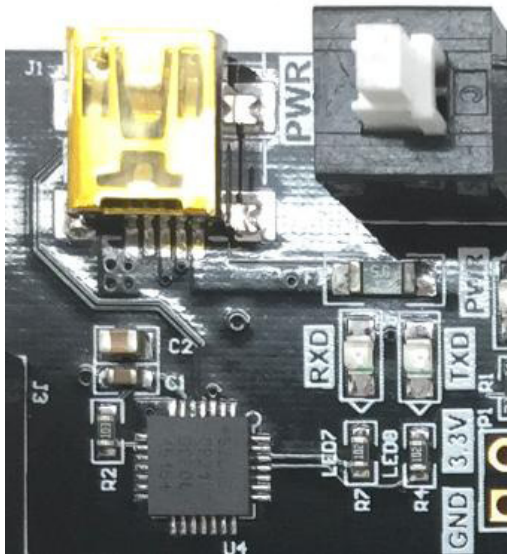

Figure 38. CP2102 module on board

Tab6. Pin Configuration for USB-UART experiment

Signal Name	FPGA PIN
RXD	C11
TXD	D12

VGA Port

A **Video Graphics Array (VGA)** connector is a three-row 15-pin DB-15 connector. The 15-pin VGA connector is found on many video cards, computer monitors, and high definition television sets. On laptop computers or other small devices, a VGA port is usually used .DB-15 is also conventionally called RGB connector.VGA connectors and cables carry analog component RGBHV (red, green, blue, horizontal sync, vertical sync) video signals, and VESA Display Data Channel (VESA DDC) data. The VGA interface is not engineered to be hot pluggable (so that the user can connect or disconnect the output device while the host is running), although in practice this can be done and usually does not cause damage to the hardware or other problems.

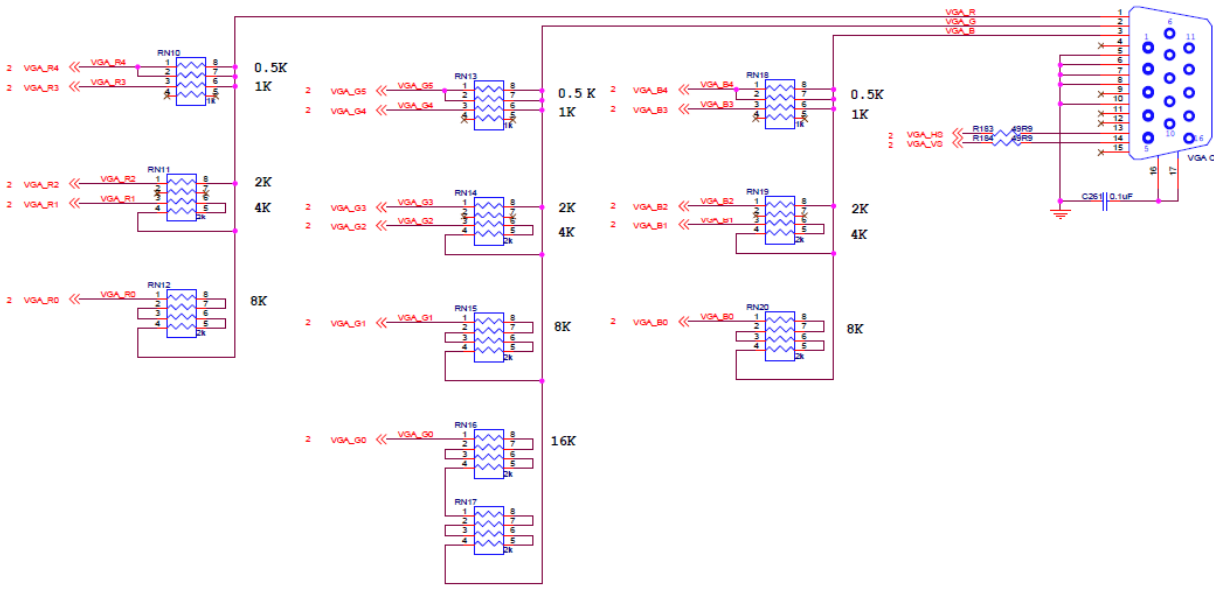

Figure 39. VGA Connector module

Figure 40. VGA Connector module on board

Tab7. Pin Configuration for VGA experiment

SIGNAL NAME	FPGA PIN	REMARKS
VGA_D<0>	P7	BLUE<0>
VGA_D<1>	M7	BLUE<1>
VGA_D<2>	P8	BLUE<2>
VGA_D<3>	N8	BLUE<3>
VGA_D<4>	L7	BLUE<4>
VGA_D<5>	M9	GREEN<0>
VGA_D<6>	N9	GREEN<1>
VGA_D<7>	P9	GREEN<2>
VGA_D<8>	L10	GREEN<3>
VGA_D<9>	M10	GREEN<4>
VGA_D<10>	P11	GREEN<5>
VGA_D<11>	M11	RED<0>
VGA_D<12>	M12	RED<1>
VGA_D<13>	L12	RED<2>
VGA_D<14>	N14	RED<3>
VGA_D<15>	M13	RED<4>
VGA_HS	M14	Horizontal Synchronous
VGA_VS	L13	Vertical Synchronous

SD Card

The SD connector enables the memory card to be interfaced to the microcontroller in order to expand microcontroller memory.To enable serial communication between the microcontroller and the memory card it is necessary to adjust their voltage levels.Memory card is powered with 3.3v power supply voltage.

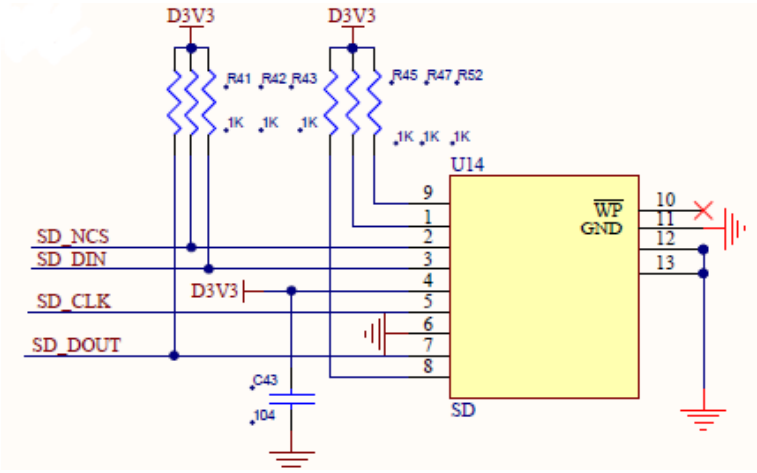

Figure 41. SD CARD module

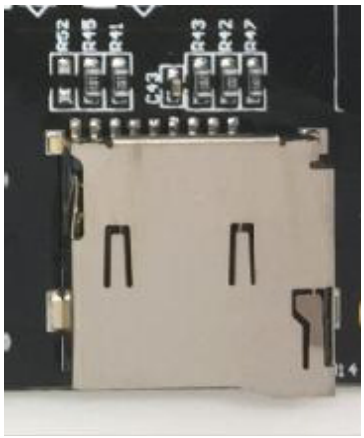

Figure 42. SD CARD module on board

Tab8. Pin Configuration for SD CARD experiment

SD MODE	
Signal Name	FPGA PIN
SD_NCS	N3
SD_DIN	L5
SD_CLK	M3
SD_DOUT	L4

Four User LEDs

LED (Light-Emitting Diode) is a highly efficient electronic light source. When connecting LEDs, it is necessary to place a current limiting resistor in series so that LEDs are provided with the current value specified by the manufacturer. The current varies from 0.2mA to 20mA, depending on the type of the LED and the manufacturer. **AX309** Development Board uses low-current LEDs with typical current consumption of 0.2mA or 0.3mA, depending of VCC voltage selection. Board contains 4 LEDs which can be used for visual indication of the logic state on IO pins. An active LED indicates that a logic low (0) is present on the pin.

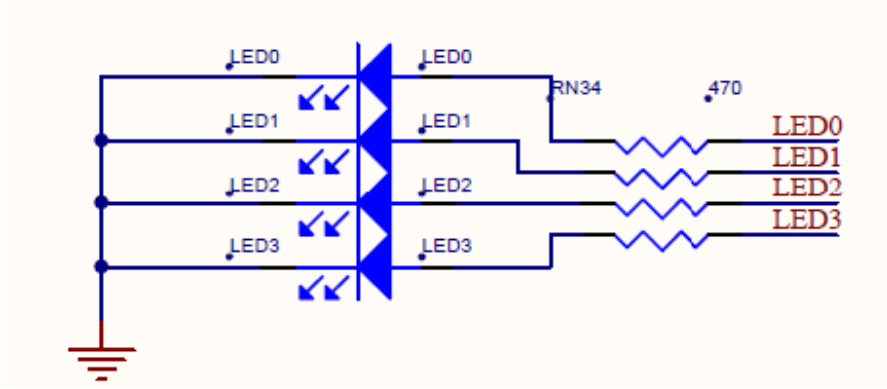

Figure 43. four LEDs module

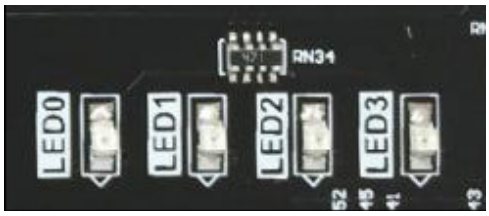

Figure 44. four LEDs module on board

Tab9. Pin Configuration for LED experiment

Signal Name	FPGA PIN
LED<0>	P4
LED<1>	N5
LED<2>	P5
LED<3>	M6

KEYs

The logic state of all microcontroller digital inputs may be changed using push buttons. In this application, 4 user keys are connected to 4 different Input/Output ports.At the same time, four pull-up resistors are added in order to apply a high level on the corresponding input pins.The four keys are used for common application.

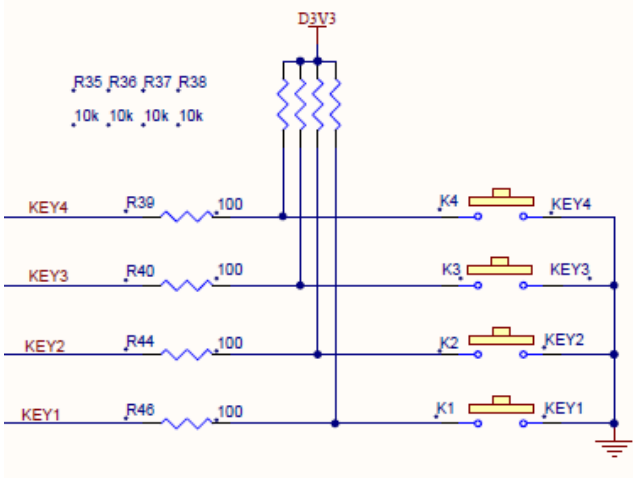

Figure 45. Four Common User Keys

In addition,There are two Keys on this board: **RESET** key for system reset, and **CONFIG** key for application re-configuring.

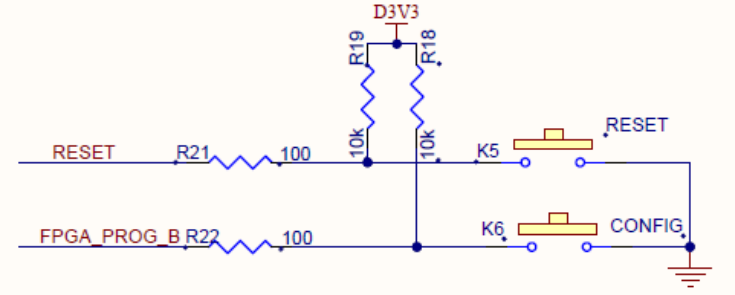

Figure 46. RESET and CONFIG keys

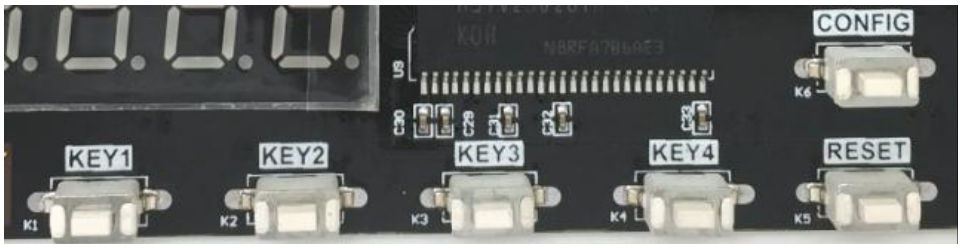

Figure 47. Keys on board

Tab10. Pin Configuration for keys experiment

Signal Name	FPGA PIN	REMARKS
KEY1	C3	KEY 1
KEY2	D3	KEY 2
KEY3	E4	KEY 3
KEY4	E3	KEY 4
RESET	L3	KEY6
PROG	T2	KEY5

Camera Port

AX309 equips a 9*2 header for the OV7670 and OV5640 camera modules by our company. The OV7670 and OV5640 camera module can capture video data and then display on TFT lcd or VGA screen. OV7670,300000 pixel, 640 * 480; OV5640,5000000 pixel,2592 * 1944.

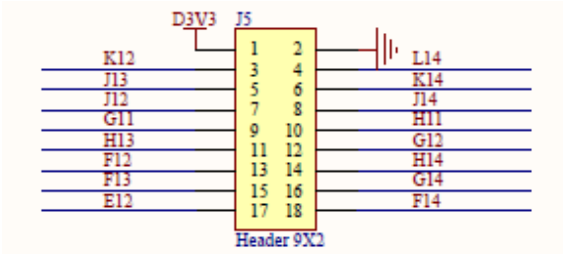

Figure 48. Camera Port

Figure 49. Camera module connected to the board

Tab11. Pin Configuration for camera experiment

Signal Name	FPGA PIN
CMOS_SCLK	K12
CMOS_SDAT	L14
CMOS_VSYNC	J13
CMOS_HREF	K14
CMOS_PCLK	J12
CMOS_XCLK	J14
CMOS_D<7>	G11
CMOS_D<6>	H11
CMOS_D<5>	H13
CMOS_D<4>	G12
CMOS_D<3>	F12
CMOS_D<2>	H14
CMOS_D<1>	F13
CMOS_D<0>	G14
CMOS_RESET	E12
CMOS_PWDN	F14

6-Digit LED Display

One seven segment digit consist of 7+1 LEDs which are arranged in a specific formation which can be used to represent digits from 0 to 9 and even some letters. One additional LED is used for marking the decimal dot, in case you want to write a decimal point in the desired segment. The AX309 development board contains 6-digit 7-segment display. Driving such a display is done using multiplexing techniques. Data lines are shared between segments, and therefore the same segment LEDs in each digit are connected in parallel. The board equips a 6-digit,0.36" LED Display.

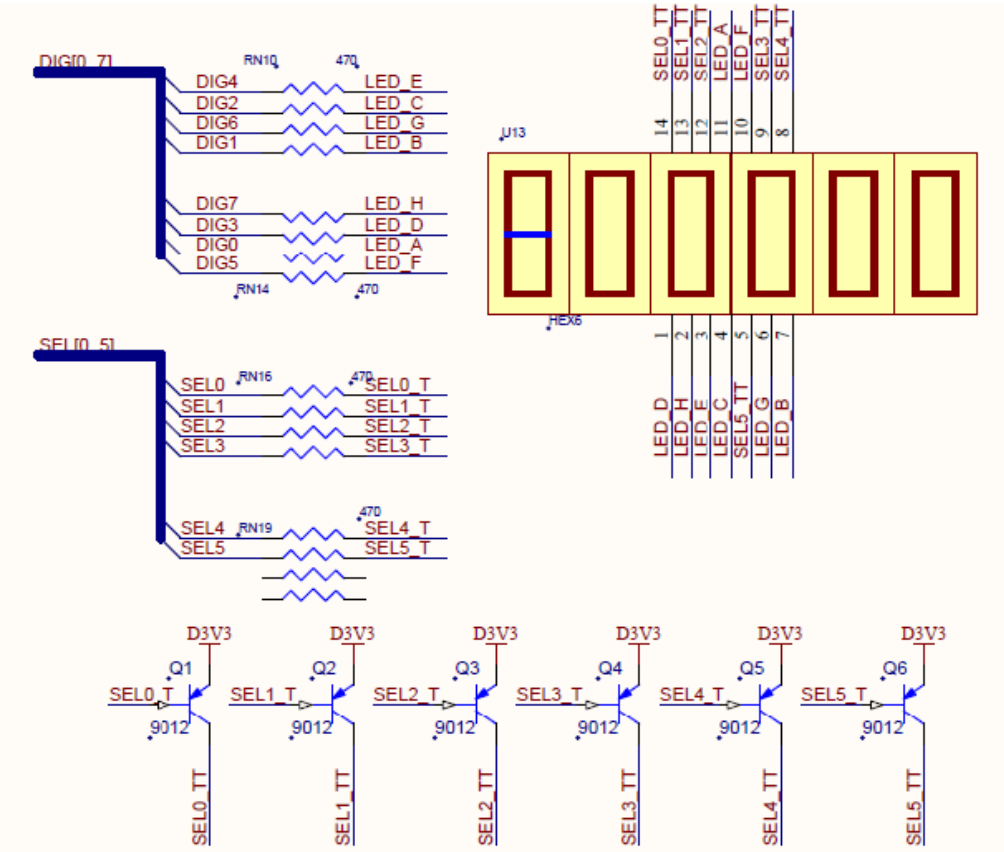

Figure 50. Segment 6-digit LED Display

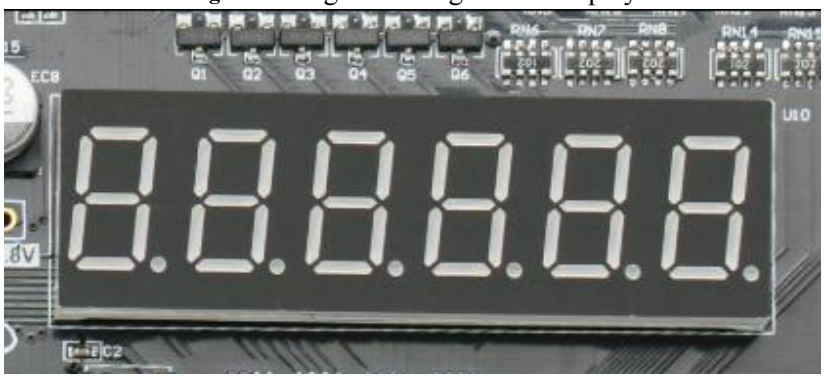

Figure 51. Segment 6-digit LED Display on board

Tab12. Pin Configuration for Segment 6-digit LED Display experiment

Signal Name	FPGA PIN	REMARKS
DIG[0]	C7	A
DIG[1]	E6	B
DIG[2]	C5	C
DIG[3]	F7	D
DIG[4]	D6	E
DIG[5]	E7	F
DIG[6]	D5	G
DIG[7]	C6	DP
SEL[0]	D8	DIGIT-1
SEL[1]	E8	DIGIT-2
SEL[2]	F9	DIGIT-3
SEL[3]	F10	DIGIT-4
SEL[4]	E10	DIGIT-5
SEL[5]	D9	DIGIT-6

Piezo Buzzer

Piezo electricity is the charge which accumulates in certain solid materials in response to mechanical pressure, but also providing the charge to the piezoelectric material causes it to physically deform. One of the most widely used applications of piezo electricity is the production of sound generators, called piezo buzzers. Piezo buzzer is an electric component that comes in different shapes and sizes, which can be used to create sound waves when provided with analog electrical signal.

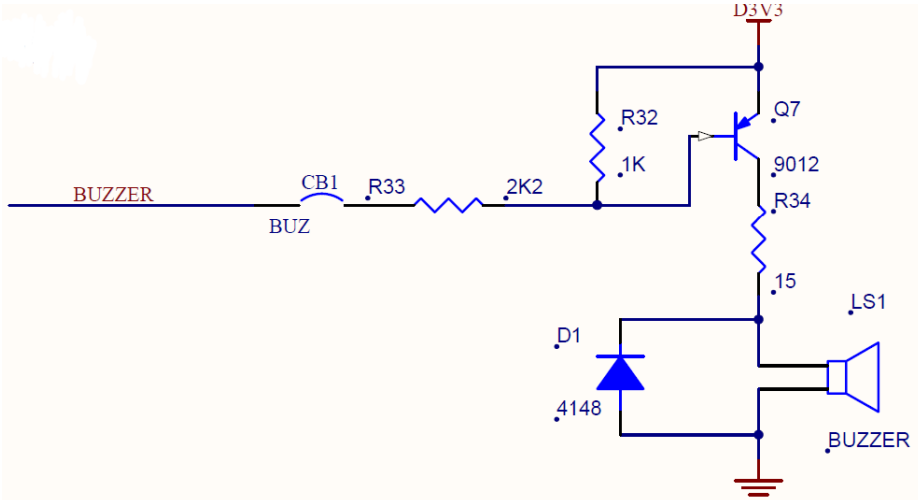

Figure 52. Buzzer Module

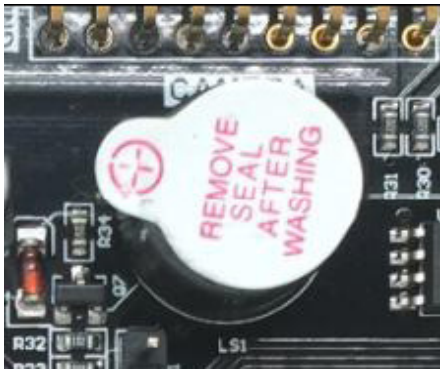

Figure 53. Buzzer Module on board

Tab13. Pin Configuration for buzzer experiment

Signal Name	FPGA PIN
BUZZER	J11

Expansion Port

AX309 equips two expansion port which are used for connecting some external module like AD/DA module and TFT LCD Display module.

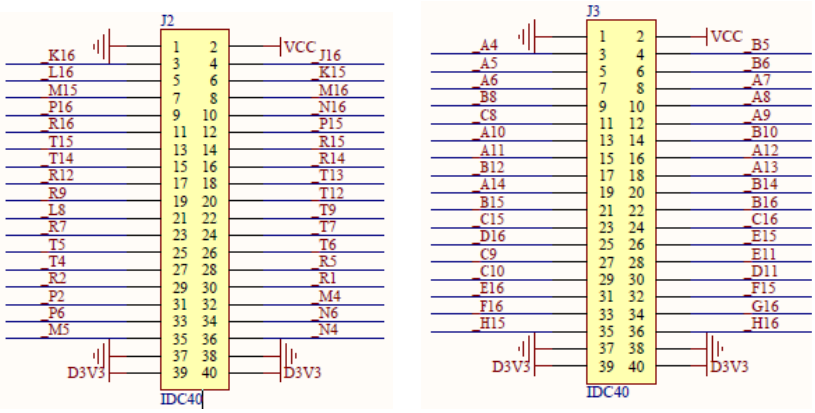

Figure 54. Expansion port J2 and J3

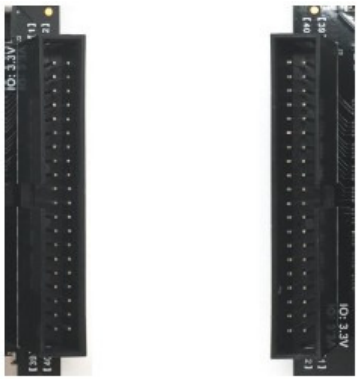

Figure 55. Expansion port J2 and J3 on board

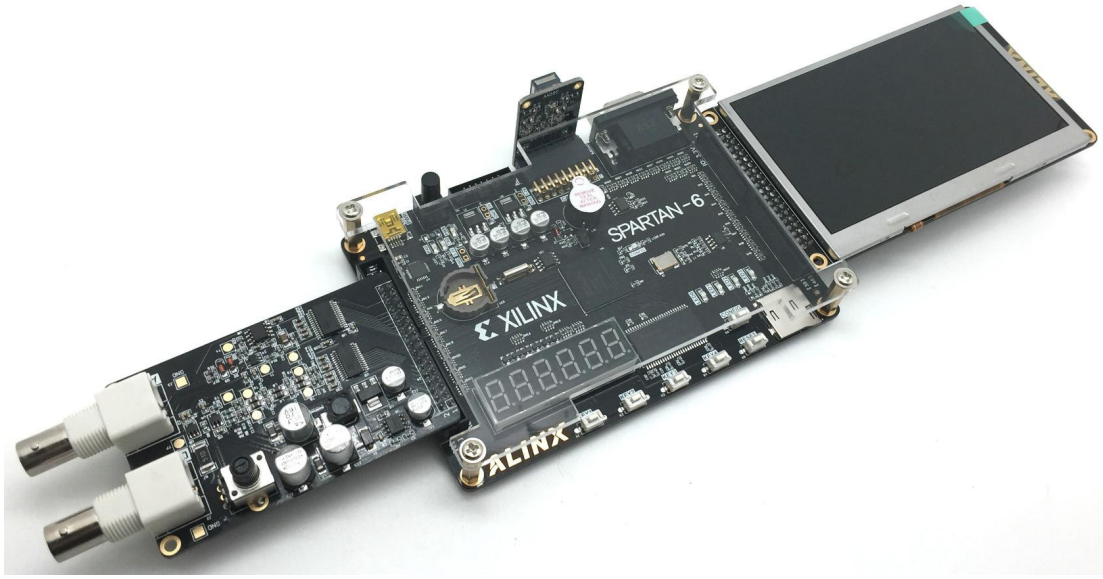

Figure 56. AD/DA module and TFT module connected to the board

Tab14. Pin Configuration for J2

PIN#	FPGA PIN	PIN#	FPGA PIN
1	GND	2	VCC5V
3	K16	4	K15
5	L16	6	K15
7	M15	8	M16
9	P16	10	N16
11	R16	12	P15
13	T15	14	R15
15	T14	16	R14
17	R12	18	T13
19	R9	20	T12
21	L8	22	T9
23	R7	24	T7
25	T5	26	T6
27	T4	28	R5
29	R2	30	R1
31	P2	32	M4
33	P6	34	N6
35	M5	36	N4
37	GND	38	GND
39	D3V3	40	D3V3

Tab15. Pin Configuration for J3

PIN#	FPGA PIN	PIN#	FPGA PIN
1	GND	2	VCC5V
3	A4	4	B5
5	A5	6	B6
7	A6	8	A7
9	B8	10	A8
11	C8	12	A9
13	A10	14	B10
15	A11	16	A12
17	B12	18	A13
19	A14	20	B14
21	B15	22	B16
23	C15	24	C16
25	D16	26	E15
27	C9	28	E11
29	C10	30	D11
31	E16	32	F15
33	F16	34	G16
35	H15	36	H16
37	GND	38	GND
39	D3V3	40	D3V3

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