

Lindbergh Schematic Document

uFCPGA Northwood

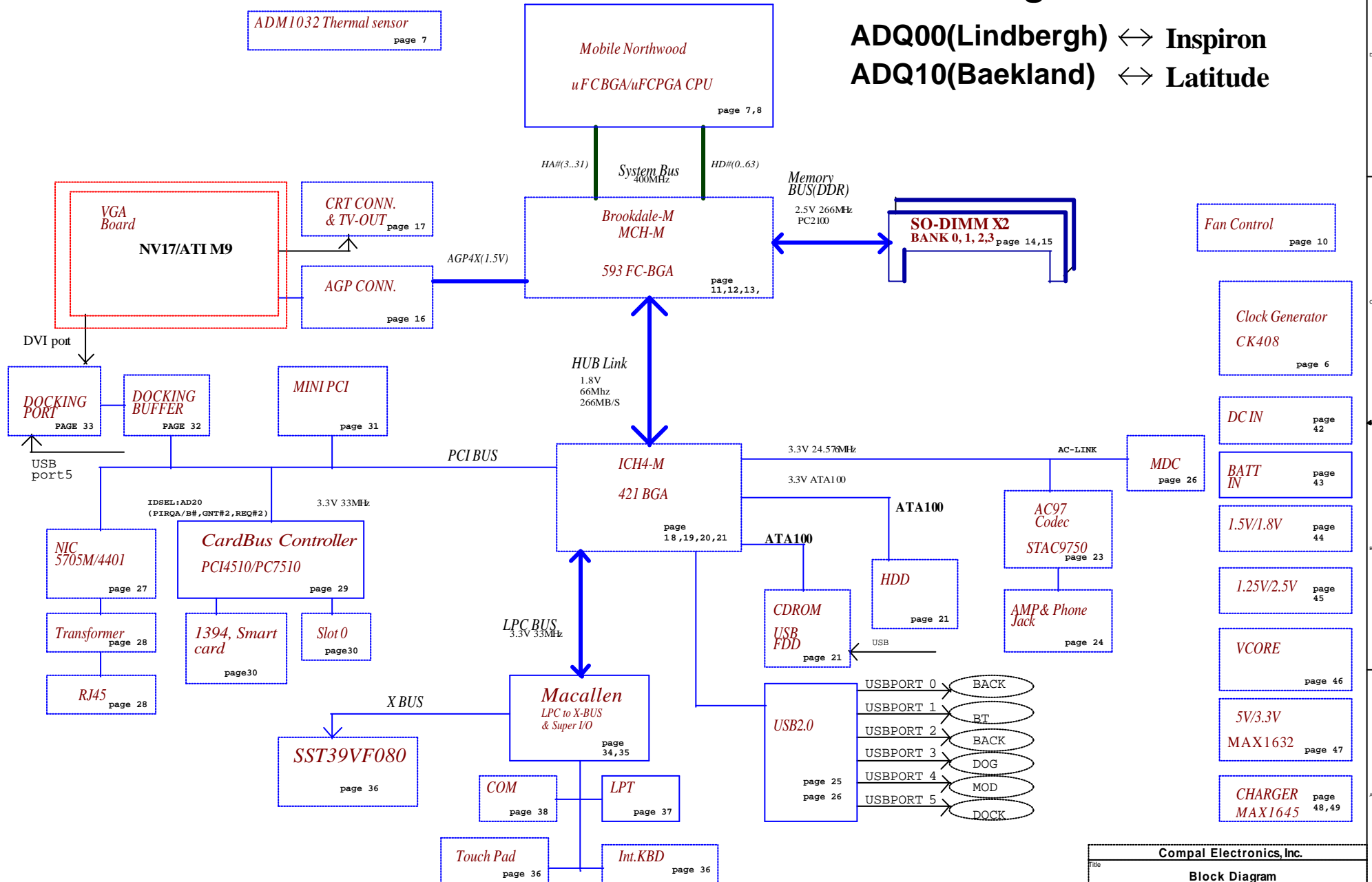
2002-10-23

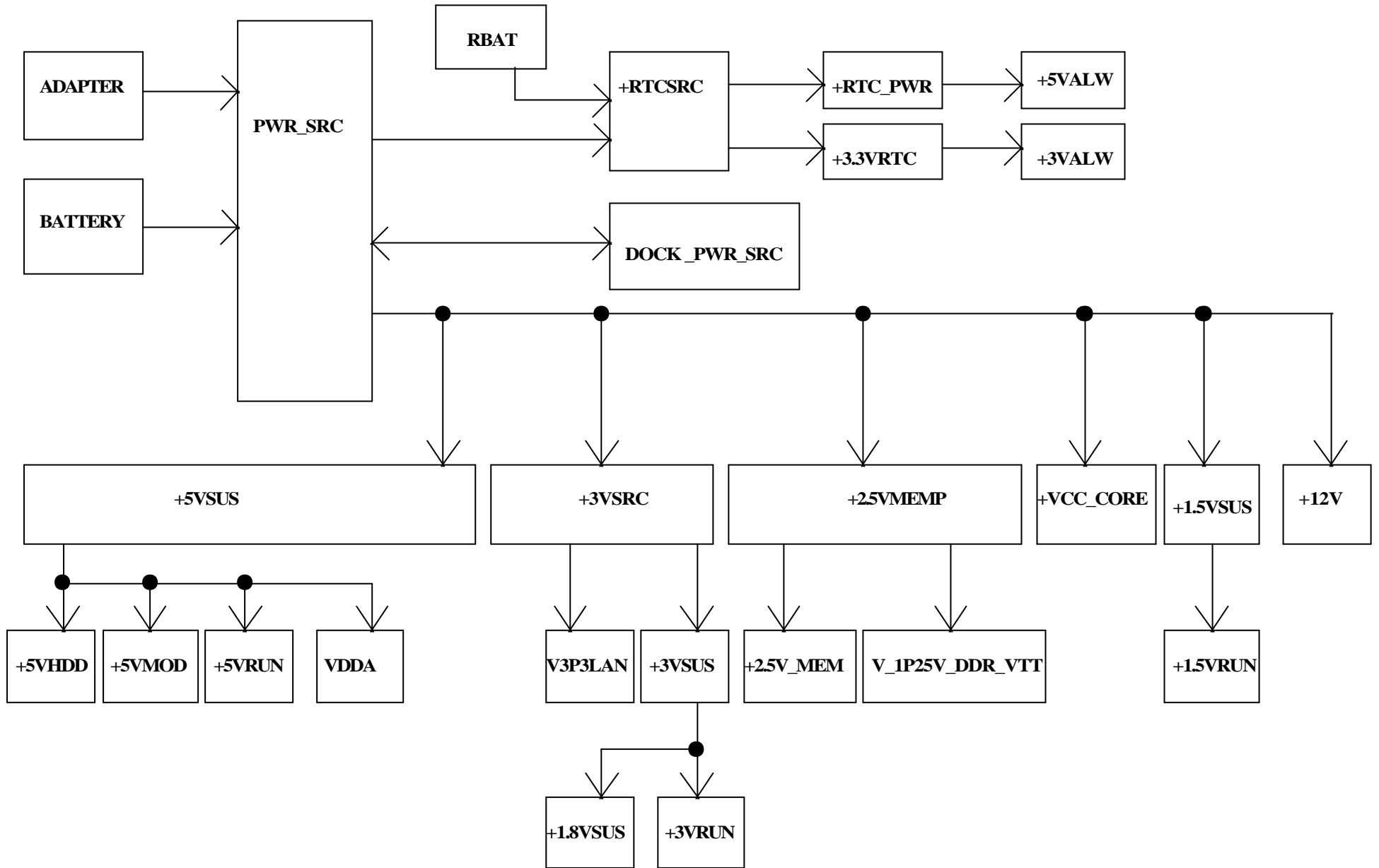
Rev:X025

Compal Electronics, Inc.		
Title	Cover Sheet	
Size	Document Number	Rev
	ADQ00/LA-1351	X025
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	Sheet	1 of 50

Block Diagram

ADQ00(Lindbergh) ↔ Inspiron
 ADQ10(Baekland) ↔ Latitude





ICH4-M

ICH_SMBCLK

ICH_SMBDATA

DIMM0

DIMM1

7002

+3VRUN

CK_SCLK

CLK GEN.

7002

CK_SDATA

V_3P3_LAN

7002

7002

LAN_SMBCLK

NIC

LAN_SMBDATA

7002

7002

MPCI

SIO
Macallen

CLK_SMB

DAT_SMB

24C05

ADM1032

7002

+3VALW

7002

DH PORT

DOCK_SMB_CLK

DOCK_SMB_DAT

+5VALW

DOCKING

SBAT_SMBCLK

SBAT_SMBDAT

+5VALW

2'nd BATTERY

VGA

Inverter & ADM1032

PBAT_SMBCLK

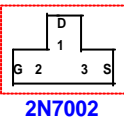
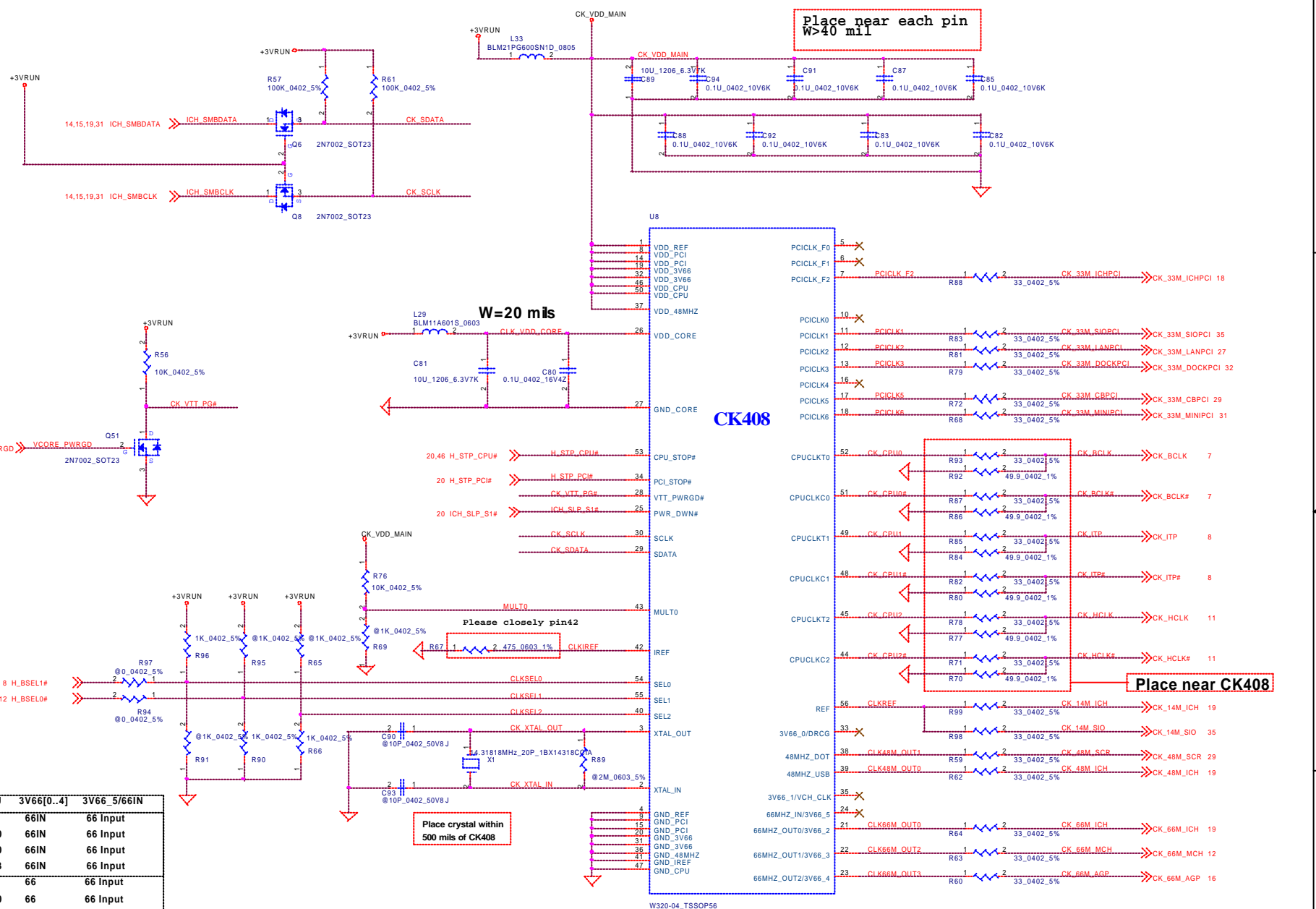
PBAT_SMBDAT

+5VALW

1'nd BATTERY

CHARGER

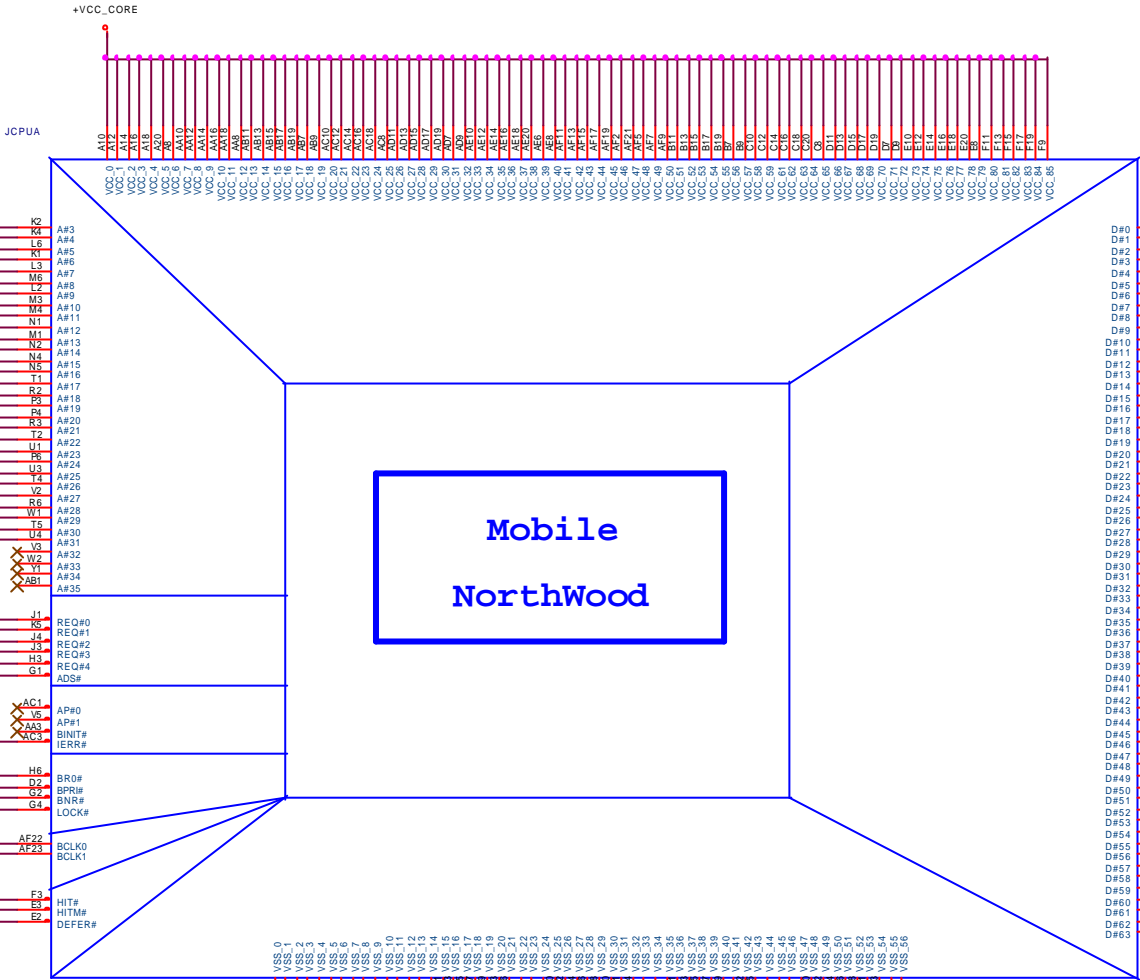
Compal Electronics, Inc.		
Title		
SMBUS TOPOLOGY		
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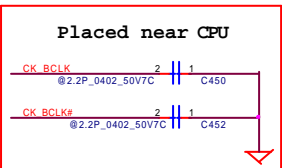
2N7002

S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input
Mid	0	0	Hi-z	Hi-z	Hi-z
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserve	Reserve	Reserve
Mid	1	1	Reserve	Reserve	Reserve

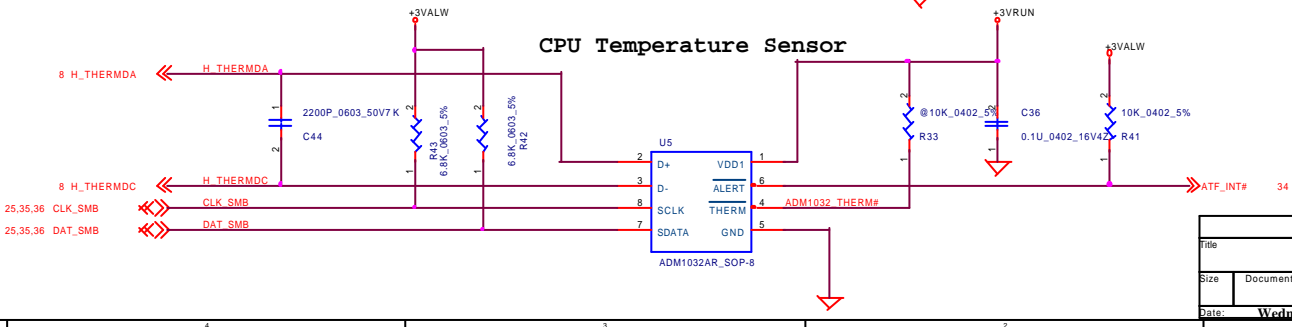
Mobile NorthWood



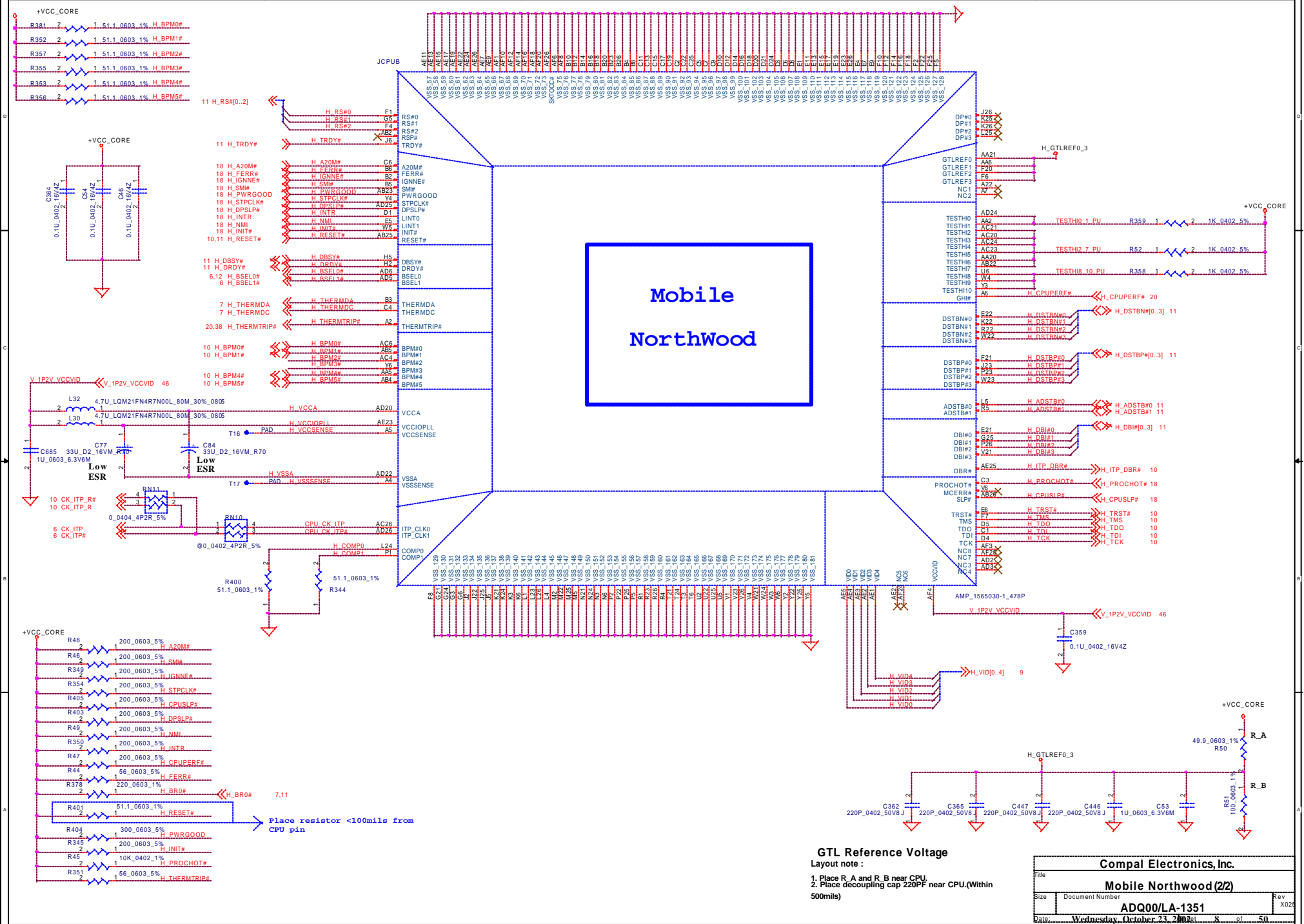
AMP_1565030-1_478P



JCPU DELL P/N changed to IM568(mobil socket)



Mobile NorthWood



GTL Reference Voltage

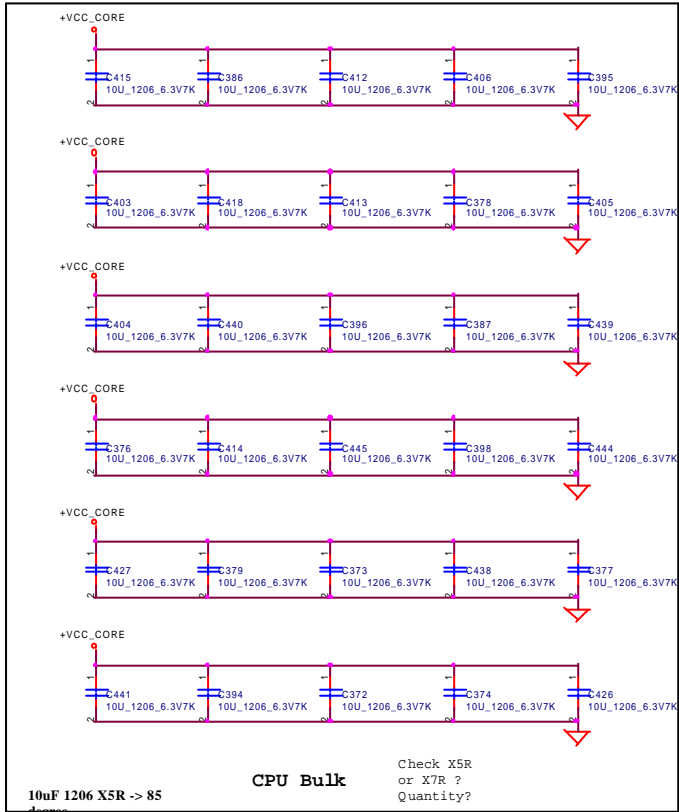
Layout note:

1. Place R_A and R_B near CPU.
2. Place decoupling cap 220PF near CPU.(Within 500mils)

Compal Electronics, Inc.		
Mobile NorthWood(2/2)		
ADQ00/LA-1351		
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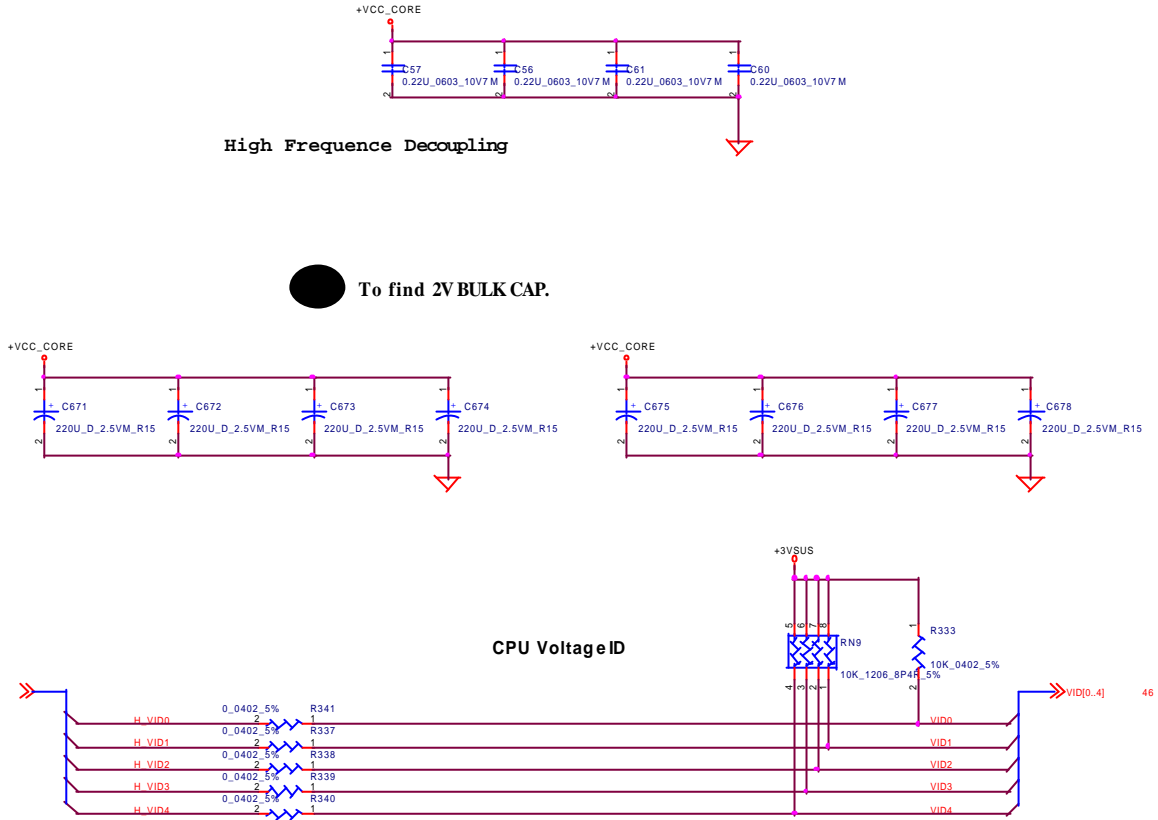
Layout note :
 Place close to CPU. Use 2-3 vias per PAD.
 Place .22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

Layout note :
 Place close to CPU power and ground pin as possible (<1inch)



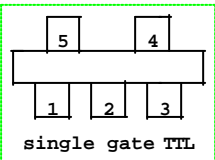
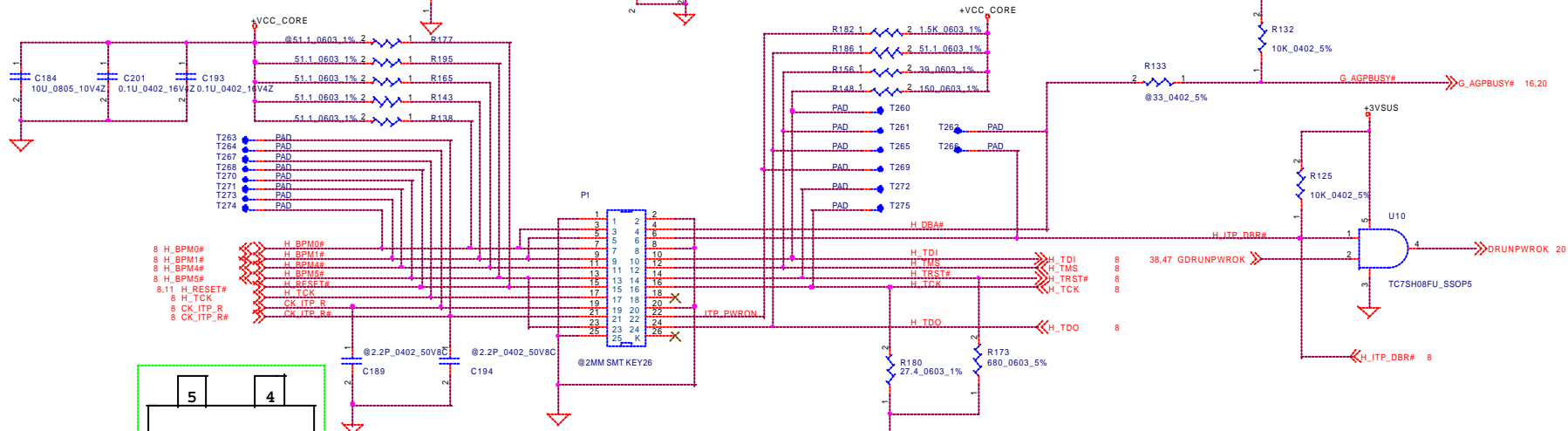
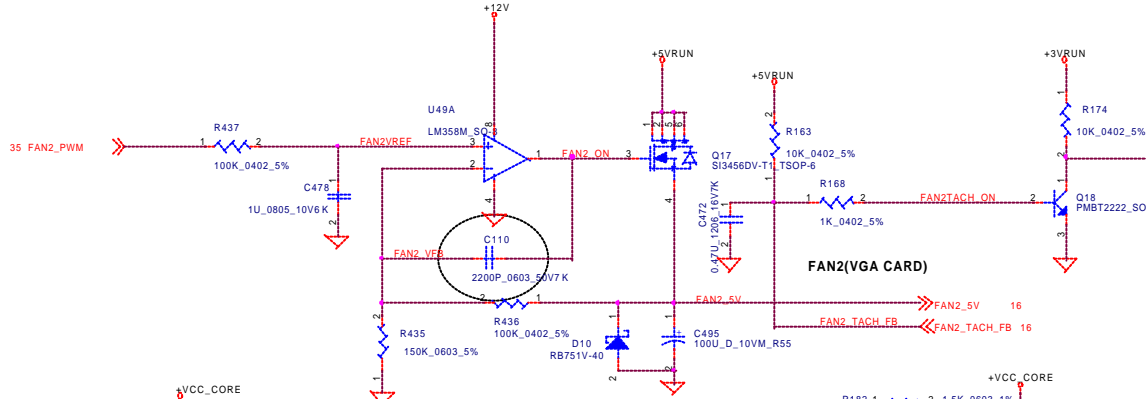
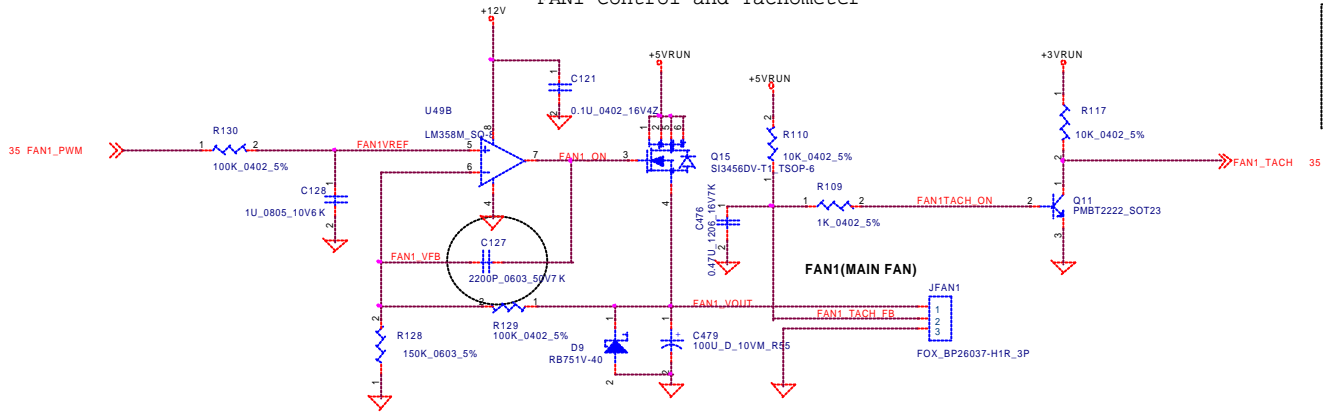
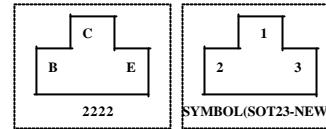
High Frequency Decoupling

To find 2V BULK CAP.



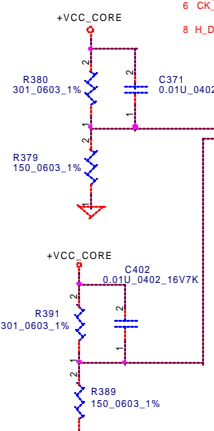
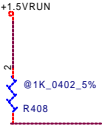
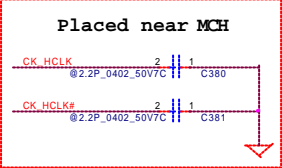
V I D					Vcore
VID4	VID3	VID2	VID1	VID0	V
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950

FAN1 Control and Tachometer

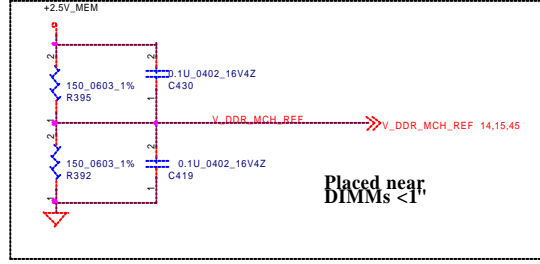
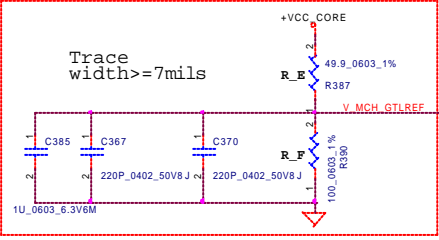


ITP Debug Connector

Compal Electronics, Inc.		
Title: ITP Debug CONN. & FAN		
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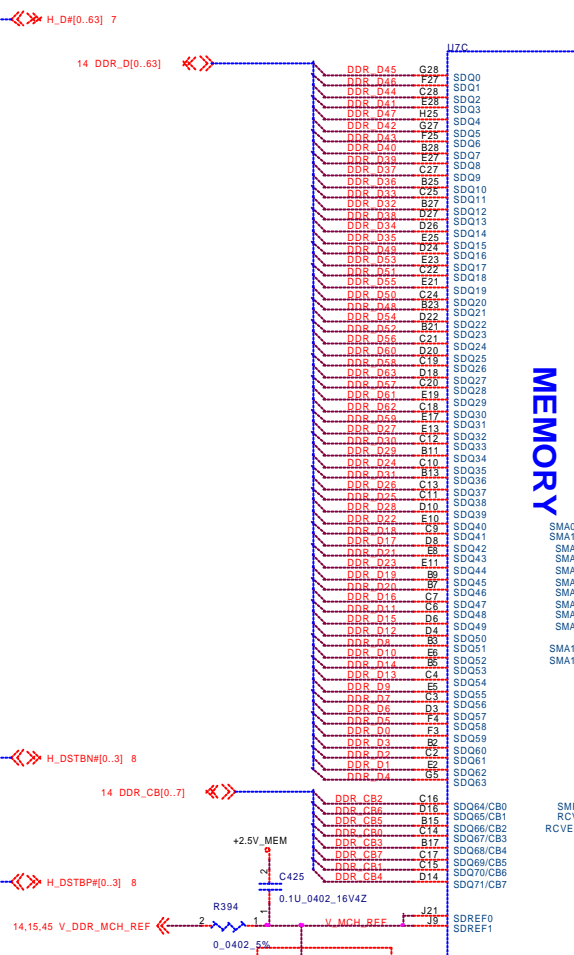


GTL Reference Voltage
Layout note:
1. Place R_E and R_F near MCH
2. Place decoupling cap 220PF near MCH pin.(Within 500mils)

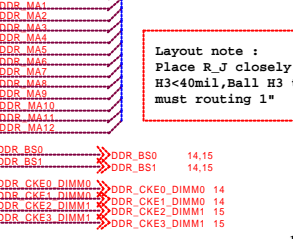
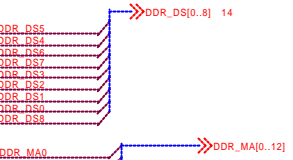
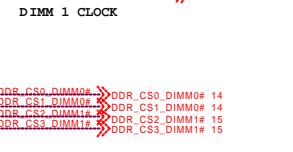
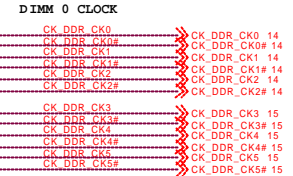


Placed near DIMMs <1"

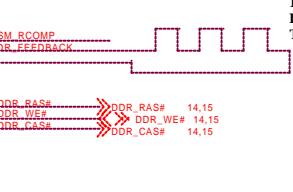
H_A#3	T4	HA#3	AD#0	AD#0	AD#0
H_A#4	T5	HA#4	AD#1	AD#1	AD#1
H_A#5	T3	HA#5	AD#2	AD#2	AD#2
H_A#6	U3	HA#6	AD#3	AD#3	AD#3
H_A#7	R3	HA#7	AD#4	AD#4	AD#4
H_A#8	P7	HA#8	AD#5	AD#5	AD#5
H_A#9	R2	HA#9	AD#6	AD#6	AD#6
H_A#10	R4	HA#10	AD#7	AD#7	AD#7
H_A#11	R6	HA#11	AD#8	AD#8	AD#8
H_A#12	P5	HA#12	AD#9	AD#9	AD#9
H_A#13	N7	HA#13	AD#10	AD#10	AD#10
H_A#14	N2	HA#14	AD#11	AD#11	AD#11
H_A#15	N3	HA#15	AD#12	AD#12	AD#12
H_A#16	R3	HA#16	AD#13	AD#13	AD#13
H_A#17	M4	HA#17	AD#14	AD#14	AD#14
H_A#18	M3	HA#18	AD#15	AD#15	AD#15
H_A#19	L5	HA#19	AD#16	AD#16	AD#16
H_A#20	L3	HA#20	AD#17	AD#17	AD#17
H_A#21	L5	HA#21	AD#18	AD#18	AD#18
H_A#22	K3	HA#22	AD#19	AD#19	AD#19
H_A#23	J2	HA#23	AD#20	AD#20	AD#20
H_A#24	J3	HA#24	AD#21	AD#21	AD#21
H_A#25	L2	HA#25	AD#22	AD#22	AD#22
H_A#26	L2	HA#26	AD#23	AD#23	AD#23
H_A#27	N5	HA#27	AD#24	AD#24	AD#24
H_A#28	S2	HA#28	AD#25	AD#25	AD#25
H_A#29	N5	HA#29	AD#26	AD#26	AD#26
H_A#30	M6	HA#30	AD#27	AD#27	AD#27
H_A#31	L7	HA#31	AD#28	AD#28	AD#28
H_ADSTB#0	R5	HADSTB#0	AD#29	AD#29	AD#29
H_ADSTB#1	R5	HADSTB#1	AD#30	AD#30	AD#30
H_RESET#	AE17	CPURST#	AD#31	AD#31	AD#31
H_TRDY#	Y4	HTRDY#	AD#32	AD#32	AD#32
H_DEFE#	Y4	HTRDY#	AD#33	AD#33	AD#33
H_BPR#	W5	BPR#	AD#34	AD#34	AD#34
H_LOCK#	W5	HLOCK#	AD#35	AD#35	AD#35
MCH_TESTIN#	H26	RSTIN#	AD#36	AD#36	AD#36
H_DBSY#	Y5	DBSY#	AD#37	AD#37	AD#37
H_DRDY#	Y5	DRDY#	AD#38	AD#38	AD#38
H_HIT#	Y5	HIT#	AD#39	AD#39	AD#39
H_HITM#	Y5	HITM#	AD#40	AD#40	AD#40
H_BRO#	Y7	BREQ#0	AD#41	AD#41	AD#41
H_BNR#	W3	BNR#	AD#42	AD#42	AD#42
H_RS#0	W2	RS#0	AD#43	AD#43	AD#43
H_RS#1	W6	RS#1	AD#44	AD#44	AD#44
H_RS#2	W6	RS#2	AD#45	AD#45	AD#45
H_REQ#0	U6	HREQ#0	AD#46	AD#46	AD#46
H_REQ#1	T7	HREQ#1	AD#47	AD#47	AD#47
H_REQ#2	U5	HREQ#2	AD#48	AD#48	AD#48
H_REQ#3	U2	HREQ#3	AD#49	AD#49	AD#49
H_REQ#4	U2	HREQ#4	AD#50	AD#50	AD#50
CK_HCLK	J8	BCLK	AD#51	AD#51	AD#51
CK_HCLK#	K8	BCLK#	AD#52	AD#52	AD#52
H_DBI#0	AD5	DBI#0	AD#53	AD#53	AD#53
H_DBI#1	AG4	DBI#1	AD#54	AD#54	AD#54
H_DBI#2	AH9	DBI#2	AD#55	AD#55	AD#55
H_DBI#3	AD15	DBI#3	AD#56	AD#56	AD#56
H_SWNG0	AAT	HSWNG0	AD#57	AD#57	AD#57
H_SWNG1	AD13	HSWNG1	AD#58	AD#58	AD#58
GMCHCOMP#	AC2	HRCOMP0	AD#59	AD#59	AD#59
GMCHCOMP1	AC13	HRCOMP1	AD#60	AD#60	AD#60
H_RSTN#	Y4	TESTIN#	AD#61	AD#61	AD#61
H_DRDY#	Y5	DRDY#	AD#62	AD#62	AD#62
H_HIT#	Y5	HIT#	AD#63	AD#63	AD#63
H_HITM#	Y5	HITM#	AD#64	AD#64	AD#64
H_BRO#	Y7	BREQ#0	AD#65	AD#65	AD#65
H_BNR#	W3	BNR#	AD#66	AD#66	AD#66



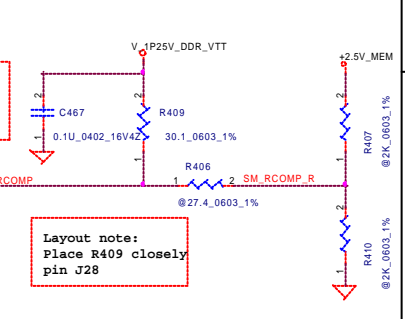
MEMORY



Layout note:
Place R_J closely ball
H3<40mil, Ball H3 to G3 trace
must routing 1"



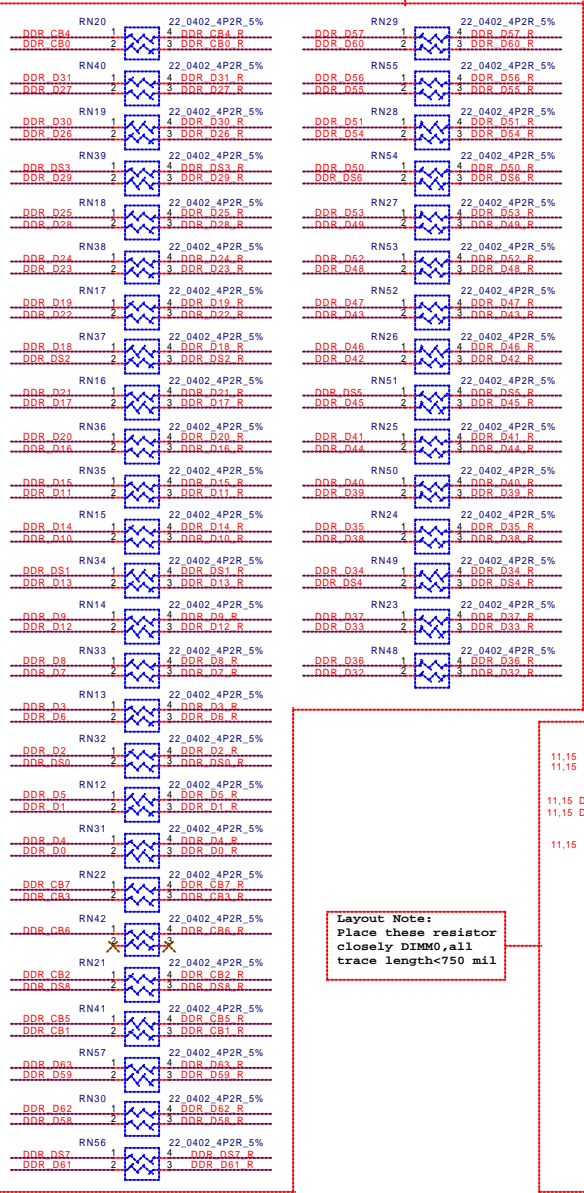
1 inch" INNER LAYER DELAY TRACE



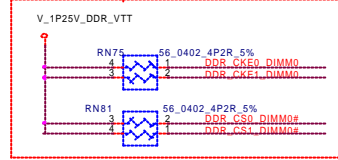
Layout note:
Place R409 closely pin J28

11 DDR_D[0..63] <<>
 11 DDR_CB[0..7] <<>
 11 DDR_DS[0..8] <<>

Layout Note:
 Place these resistor
 closely DIMM0,all
 trace length<750 mil

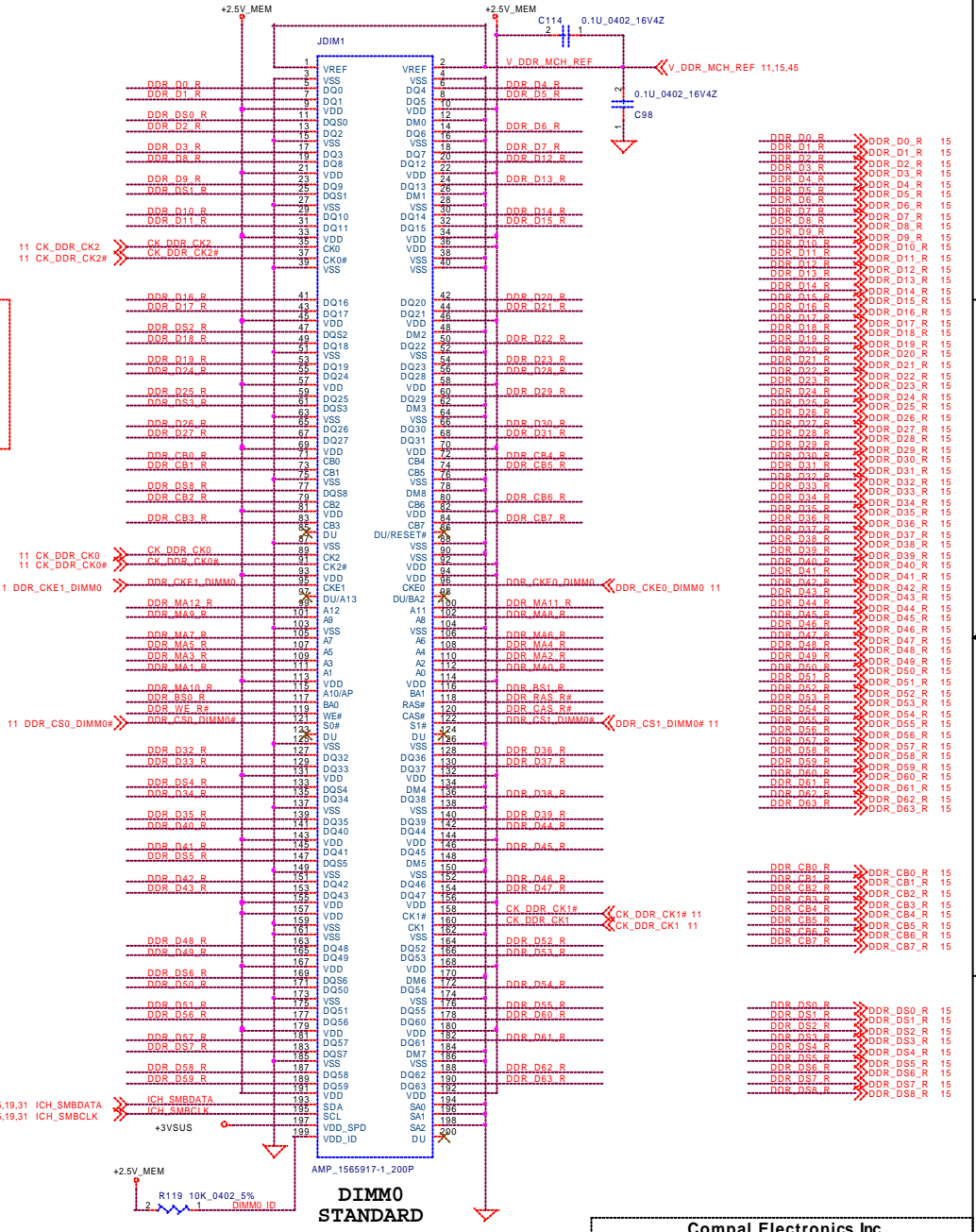
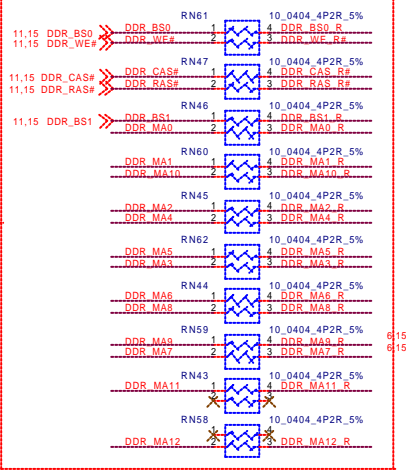


Layout Note:
 Place these resistor
 closely DIMM0,all
 trace length
 Max=1.3"



11.15 DDR_MA[0..12] <<>

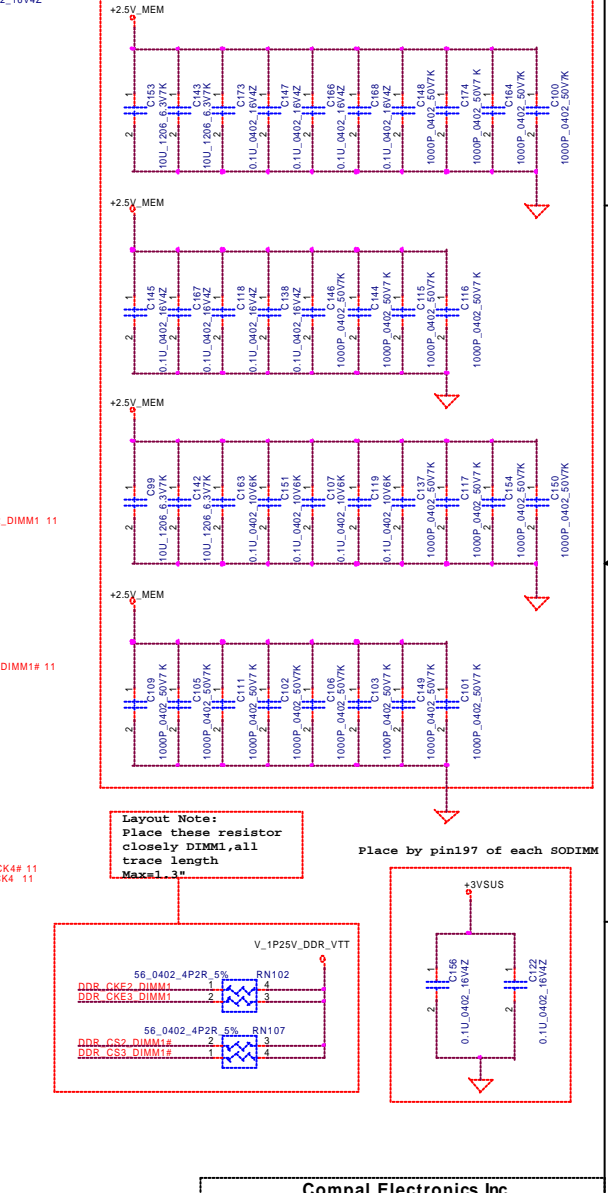
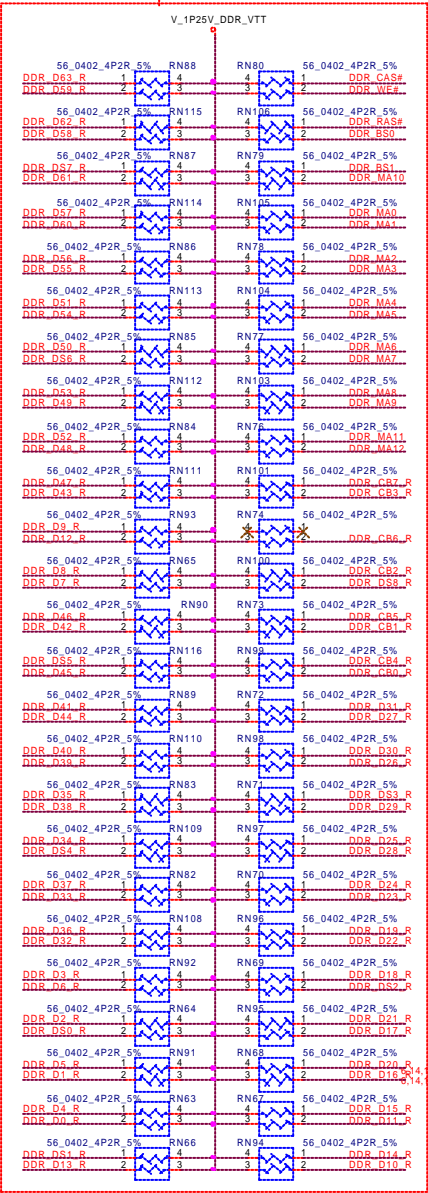
Layout Note:
 Place these resistor
 closely DIMM0,all
 trace length<750 mil



Layout Note:
Place these resistors
closely DIMM1,all
trace length<=800 mll

Layout Note:
Place CAP
near SODIMM
One .1uF cap per power pin.
Place each cap close to
pin.

- 11,14 DDR_MA0[.12]
- 14 DDR_D0_R
- 14 DDR_D1_R
- 14 DDR_D2_R
- 14 DDR_D3_R
- 14 DDR_D4_R
- 14 DDR_D5_R
- 14 DDR_D6_R
- 14 DDR_D7_R
- 14 DDR_D8_R
- 14 DDR_D9_R
- 14 DDR_D10_R
- 14 DDR_D11_R
- 14 DDR_D12_R
- 14 DDR_D13_R
- 14 DDR_D14_R
- 14 DDR_D15_R
- 14 DDR_D16_R
- 14 DDR_D17_R
- 14 DDR_D18_R
- 14 DDR_D19_R
- 14 DDR_D20_R
- 14 DDR_D21_R
- 14 DDR_D22_R
- 14 DDR_D23_R
- 14 DDR_D24_R
- 14 DDR_D25_R
- 14 DDR_D26_R
- 14 DDR_D27_R
- 14 DDR_D28_R
- 14 DDR_D29_R
- 14 DDR_D30_R
- 14 DDR_D31_R
- 14 DDR_D32_R
- 14 DDR_D33_R
- 14 DDR_D34_R
- 14 DDR_D35_R
- 14 DDR_D36_R
- 14 DDR_D37_R
- 14 DDR_D38_R
- 14 DDR_D39_R
- 14 DDR_D40_R
- 14 DDR_D41_R
- 14 DDR_D42_R
- 14 DDR_D43_R
- 14 DDR_D44_R
- 14 DDR_D45_R
- 14 DDR_D46_R
- 14 DDR_D47_R
- 14 DDR_D48_R
- 14 DDR_D49_R
- 14 DDR_D50_R
- 14 DDR_D51_R
- 14 DDR_D52_R
- 14 DDR_D53_R
- 14 DDR_D54_R
- 14 DDR_D55_R
- 14 DDR_D56_R
- 14 DDR_D57_R
- 14 DDR_D58_R
- 14 DDR_D59_R
- 14 DDR_D60_R
- 14 DDR_D61_R
- 14 DDR_D62_R
- 14 DDR_D63_R
- 14 DDR_C80_R
- 14 DDR_C81_R
- 14 DDR_C82_R
- 14 DDR_C83_R
- 14 DDR_C84_R
- 14 DDR_C85_R
- 14 DDR_C86_R
- 14 DDR_C87_R
- 14 DDR_D50_R
- 14 DDR_D51_R
- 14 DDR_D52_R
- 14 DDR_D53_R
- 14 DDR_D54_R
- 14 DDR_D55_R
- 14 DDR_D56_R
- 14 DDR_D57_R
- 14 DDR_D58_R
- 14 DDR_D59_R
- 11,14 DDR_BS0
- 11,14 DDR_BS1
- 11,14 DDR_WE#
- 11,14 DDR_CAS#
- 11,14 DDR_RAS#



Layout Note:
Place these resistor
closely DIMM1,all
trace length
Max<=1.3"

Place by pin197 of each SODIMM

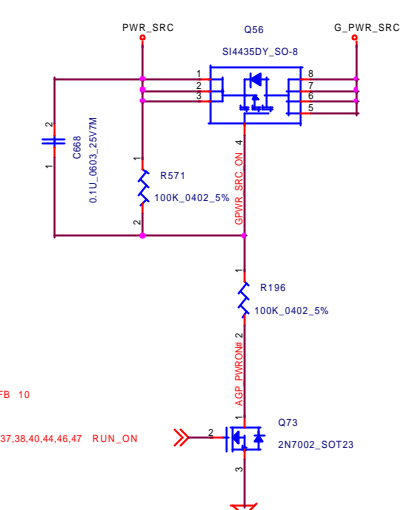
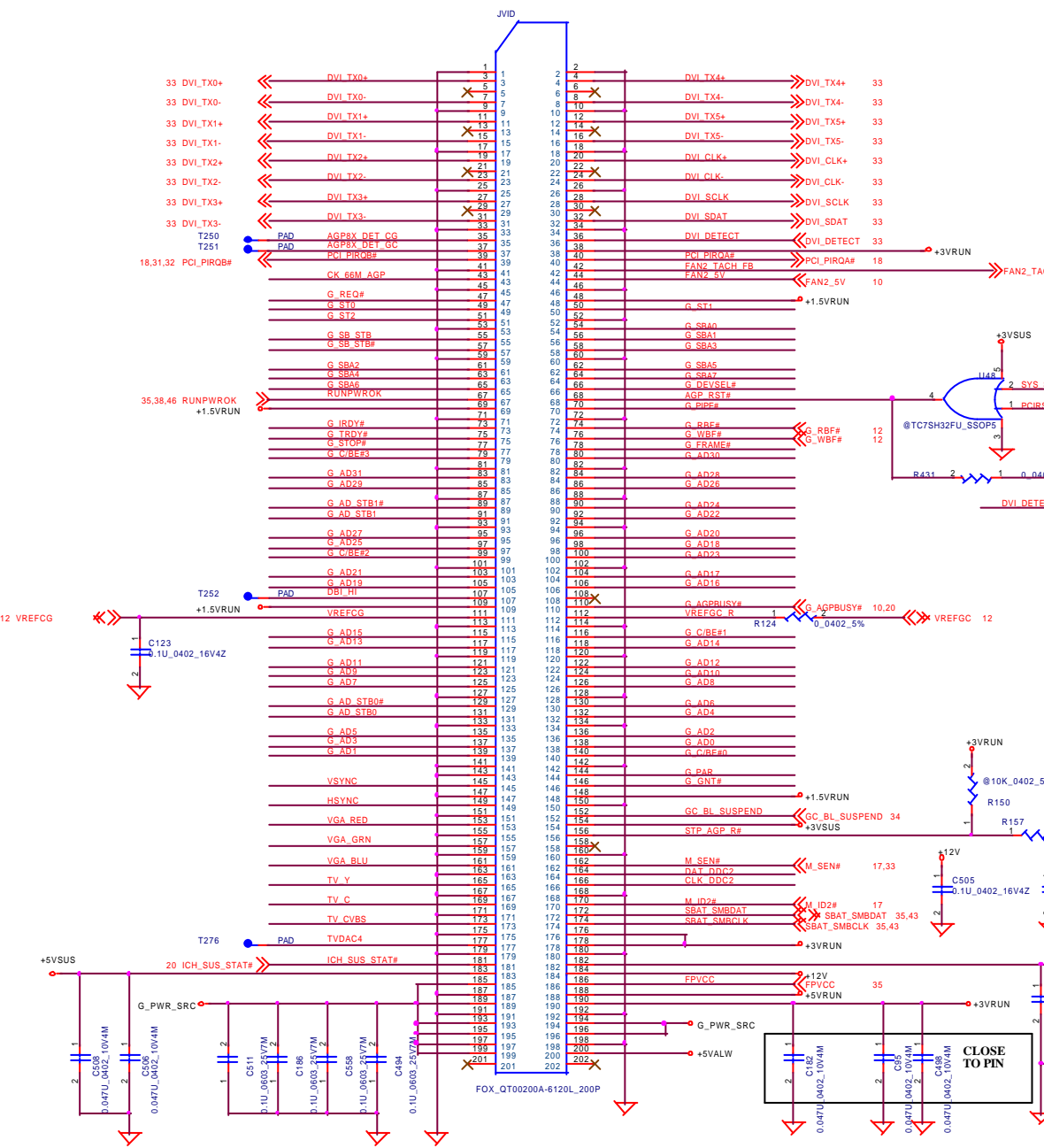
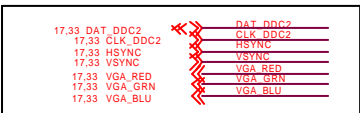
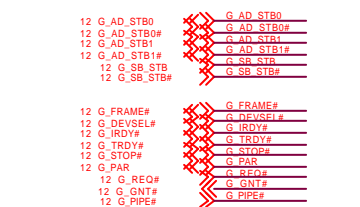
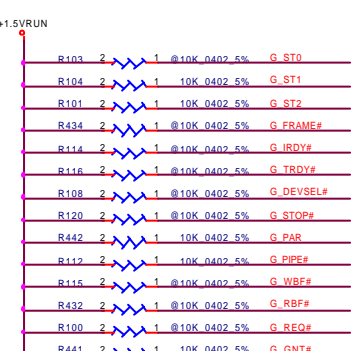
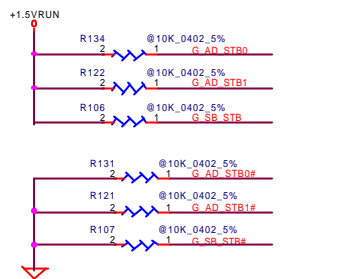
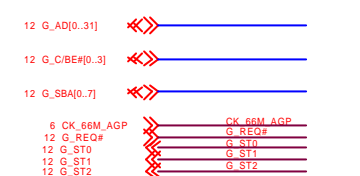
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DDR-SODIMM SLOT2

ADQ00/LA-1351

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**DIMM1
REVERSE**



Shielding Ground Pin

9,10

33,34

59,60

87,88

113,114

141,142

167,168

191,192

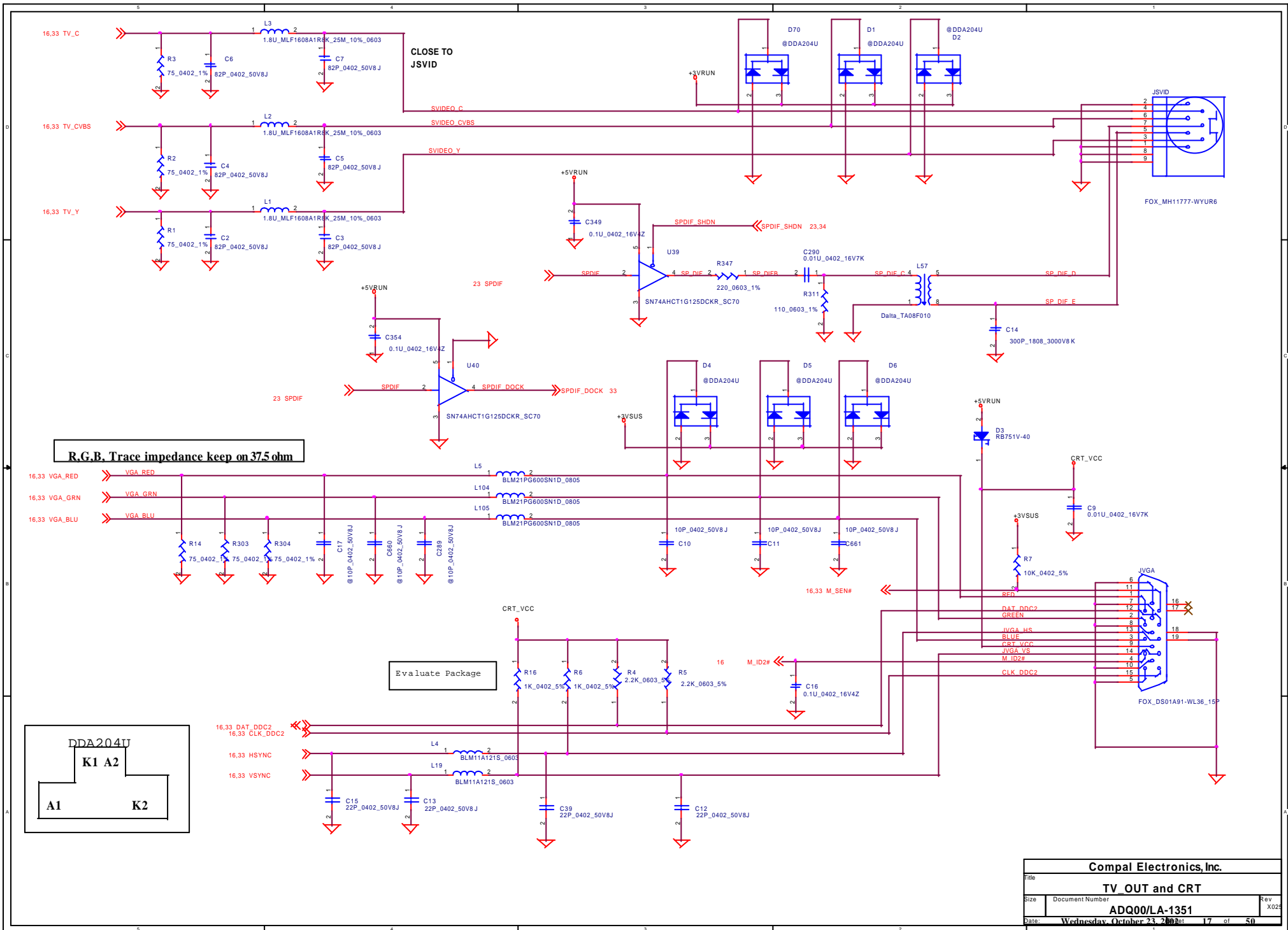
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VGA Daughter Board

ADQ00/LA-1351

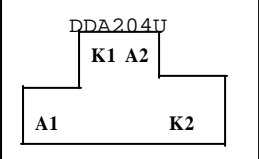
Wednesday, October 23, 2002

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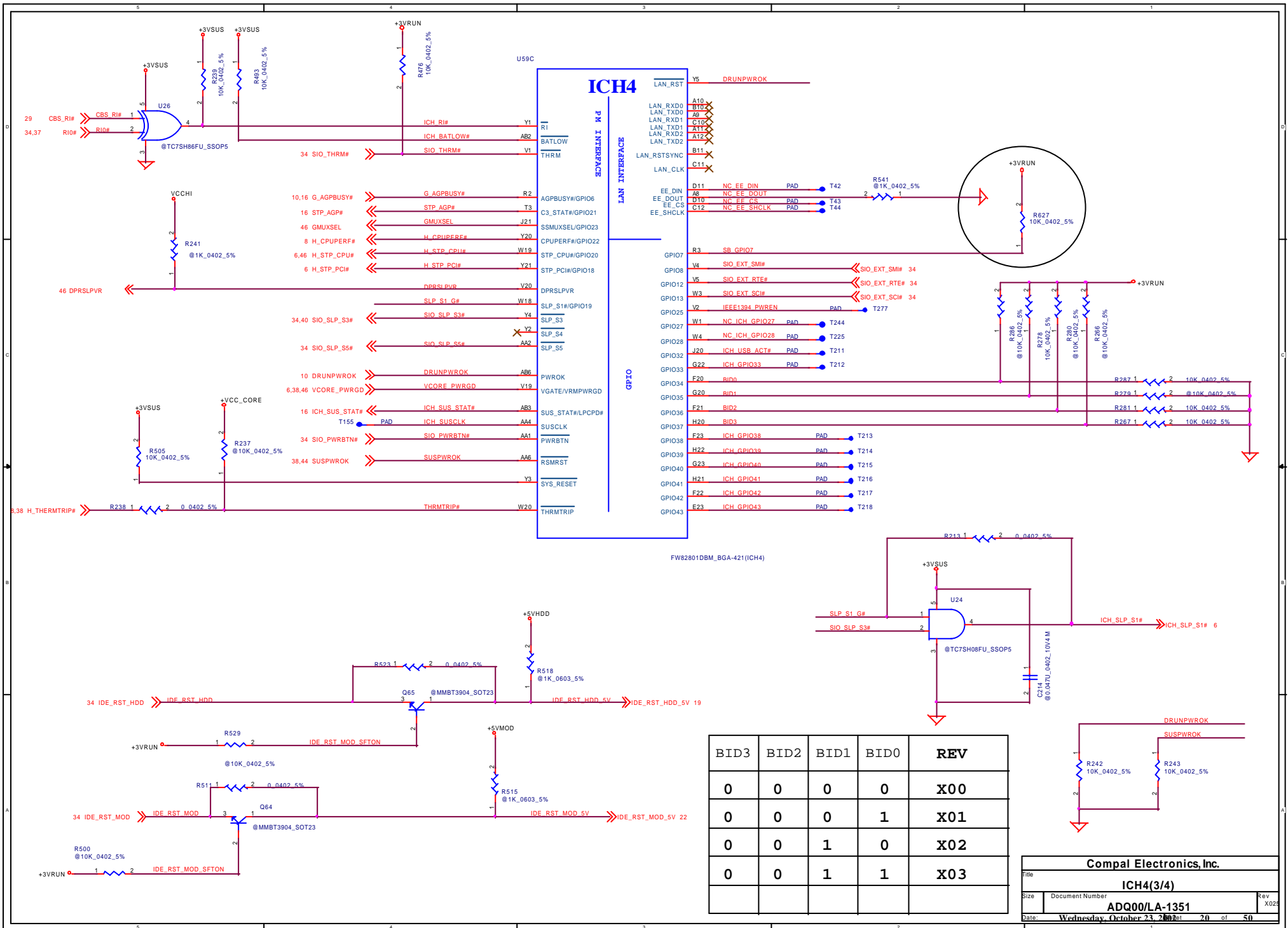


R.G.B. Trace impedance keep on 37.5 ohm

Evaluate Package



Compal Electronics, Inc.		
TV_OUT and CRT		
ADQ00/LA-1351		
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BID3	BID2	BID1	BID0	REV
0	0	0	0	X00
0	0	0	1	X01
0	0	1	0	X02
0	0	1	1	X03

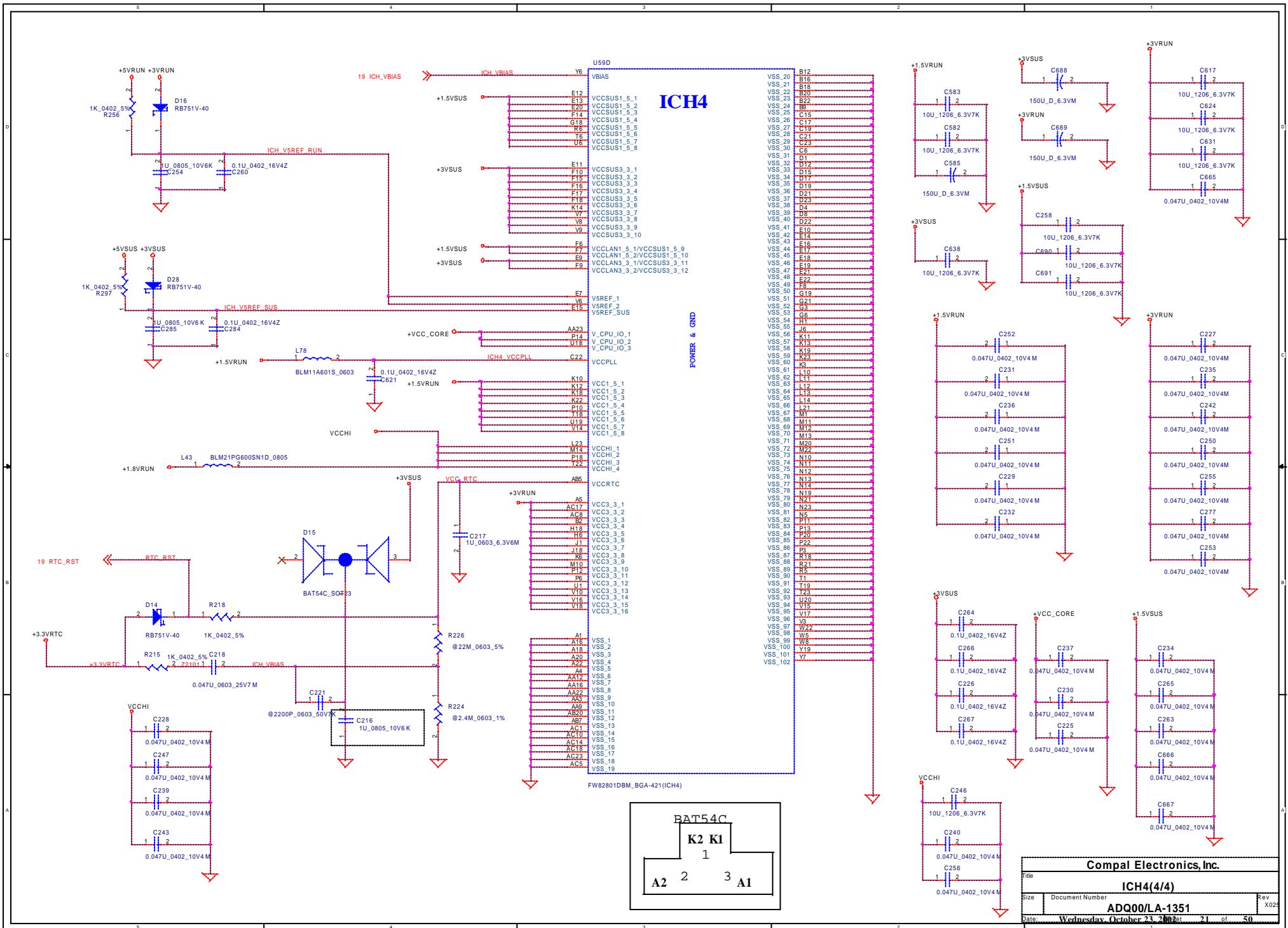
Compal Electronics, Inc.

ICH4(3/4)

File: _____

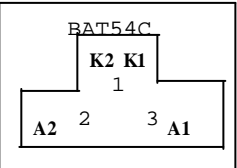
Size: _____ Document Number: **ADQ00/LA-1351** Rev: X023

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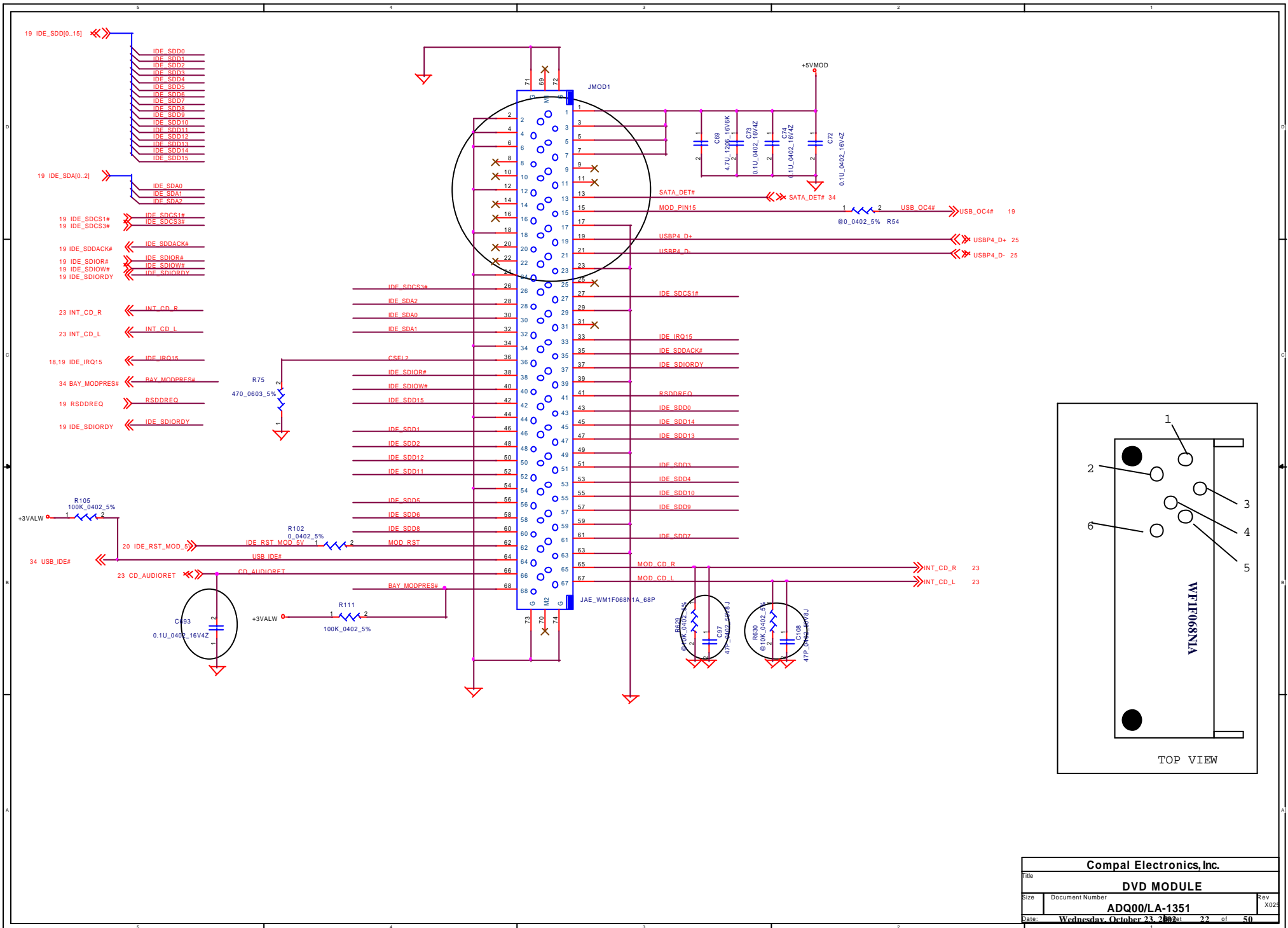


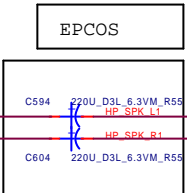
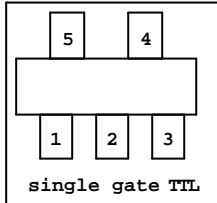
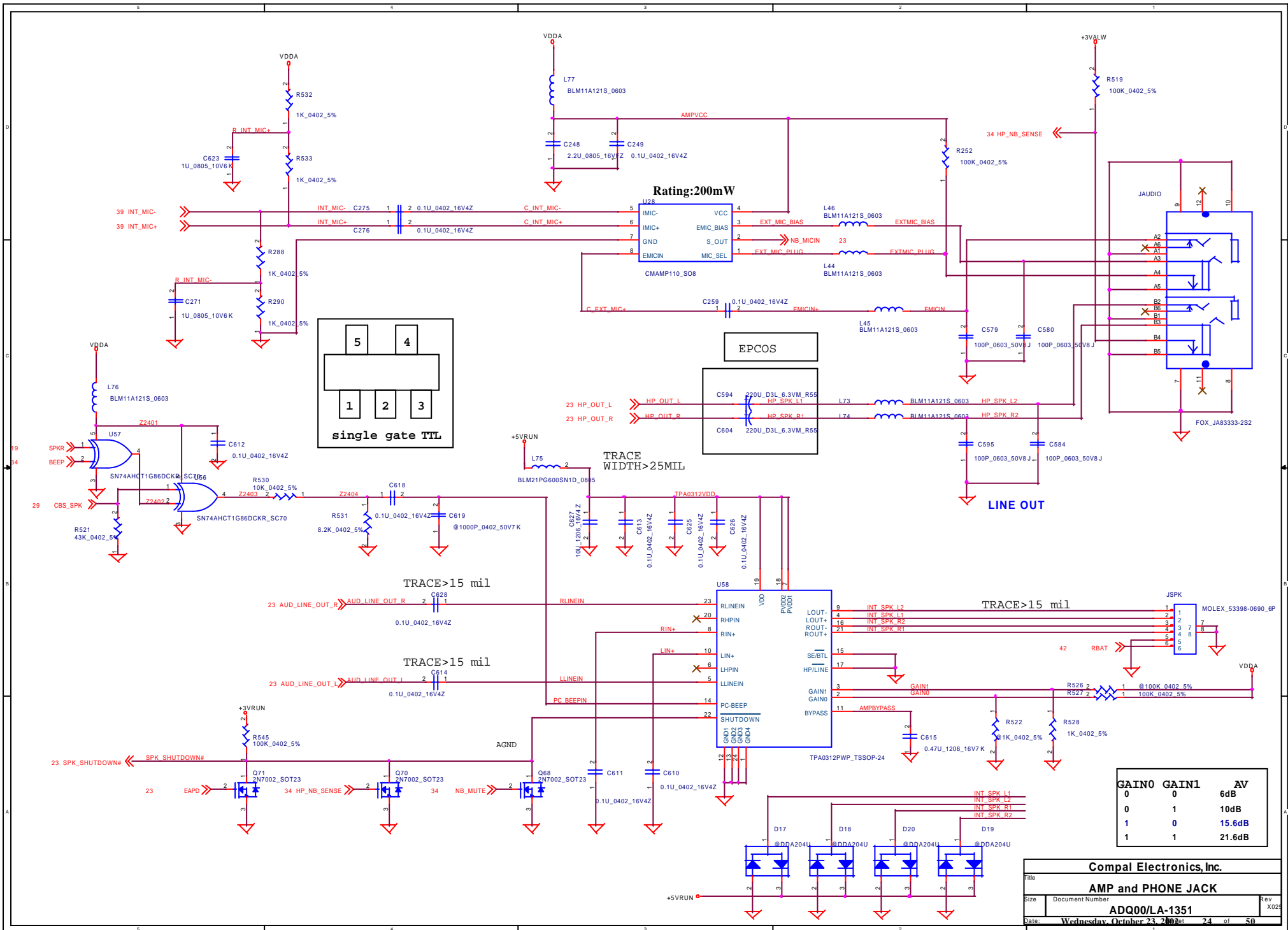
ICH4

Y6	VBIAS	B12	VSS_20
E12	VCCSUS1_5_1	B16	VSS_21
E20	VCCSUS1_5_2	B18	VSS_22
F14	VCCSUS1_5_3	B20	VSS_23
G18	VCCSUS1_5_4	B22	VSS_24
R6	VCCSUS1_5_5	B8	VSS_25
T8	VCCSUS1_5_6	C15	VSS_26
U6	VCCSUS1_5_7	C17	VSS_27
	VCCSUS1_5_8	C19	VSS_28
		C21	VSS_29
		C23	VSS_30
		D1	VSS_31
		D12	VSS_32
E11	VCCSUS3_3_1	D15	VSS_33
F15	VCCSUS3_3_2	D17	VSS_34
F16	VCCSUS3_3_3	D19	VSS_35
F18	VCCSUS3_3_4	D21	VSS_36
K14	VCCSUS3_3_5	D23	VSS_37
Y7	VCCSUS3_3_6	D4	VSS_38
V8	VCCSUS3_3_7	D8	VSS_39
V9	VCCSUS3_3_8	D22	VSS_40
	VCCSUS3_3_9	E10	VSS_41
	VCCSUS3_3_10	E16	VSS_42
		E17	VSS_43
F6	VCCLAN1_5_1/VCCSUS1_5_9	E18	VSS_44
F7	VCCLAN1_5_2/VCCSUS1_5_10	E21	VSS_45
E9	VCCLAN3_3_1/VCCSUS3_3_11	E22	VSS_46
F9	VCCLAN3_3_2/VCCSUS3_3_12	E23	VSS_47
		E24	VSS_48
		E25	VSS_49
		G19	VSS_50
E7	V5REF_1	G21	VSS_51
V6	V5REF_2	H3	VSS_52
E15	V5REF_SUS	H6	VSS_53
		H1	VSS_54
		H2	VSS_55
		J6	VSS_56
AA23	V_CPU_IO_1	K11	VSS_57
F11	V_CPU_IO_2	K13	VSS_58
U18	V_CPU_IO_3	K19	VSS_59
		K2	VSS_60
C22	VCCPLL	K9	VSS_61
		L10	VSS_62
		L11	VSS_63
K10	VCC1_5_1	L12	VSS_64
K18	VCC1_5_2	L15	VSS_65
K22	VCC1_5_3	L14	VSS_66
P10	VCC1_5_4	M1	VSS_67
F18	VCC1_5_5	M11	VSS_68
U19	VCC1_5_6	M12	VSS_69
V14	VCC1_5_7	M13	VSS_70
	VCC1_5_8	M20	VSS_71
L23	VCCHI_1	M22	VSS_72
P14	VCCHI_2	N10	VSS_73
L22	VCCHI_3	N11	VSS_74
VCCHI_4	VCCHI_4	N12	VSS_75
		N13	VSS_76
AB5	VCCRTC	N14	VSS_77
		N19	VSS_78
		N21	VSS_79
		N23	VSS_80
		N5	VSS_81
AC17	VCC3_3_1	P11	VSS_82
AC8	VCC3_3_2	P13	VSS_83
B2	VCC3_3_3	P20	VSS_84
H8	VCC3_3_4	P22	VSS_85
J1	VCC3_3_5	R9	VSS_86
K8	VCC3_3_6	R18	VSS_87
M10	VCC3_3_7	R21	VSS_88
P12	VCC3_3_8	R5	VSS_89
R6	VCC3_3_9	R1	VSS_90
U1	VCC3_3_10	T19	VSS_91
V10	VCC3_3_11	T23	VSS_92
V16	VCC3_3_12	U20	VSS_93
V18	VCC3_3_13	V15	VSS_94
V15	VCC3_3_14	W2	VSS_95
V18	VCC3_3_15	W8	VSS_96
VCC3_3_16	VCC3_3_16	W9	VSS_97
		Y19	VSS_98
		Y7	VSS_99
			VSS_100
			VSS_101
			VSS_102



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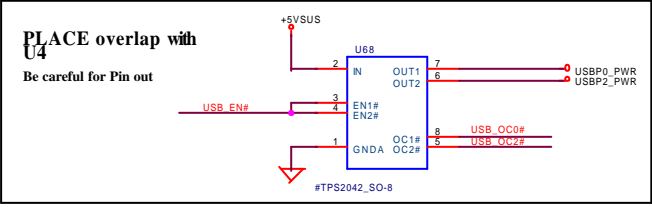
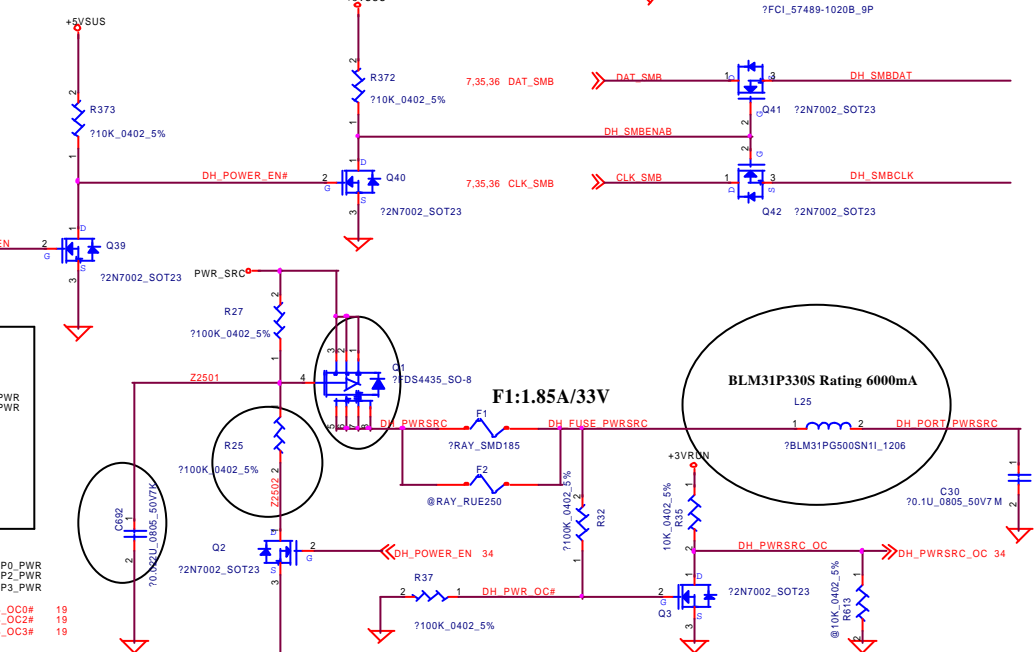
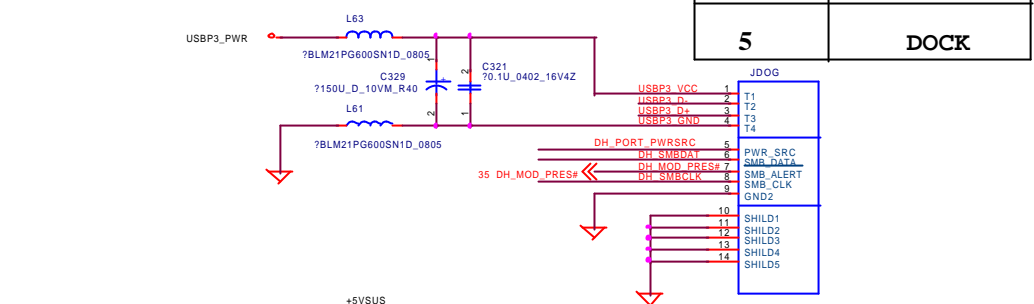
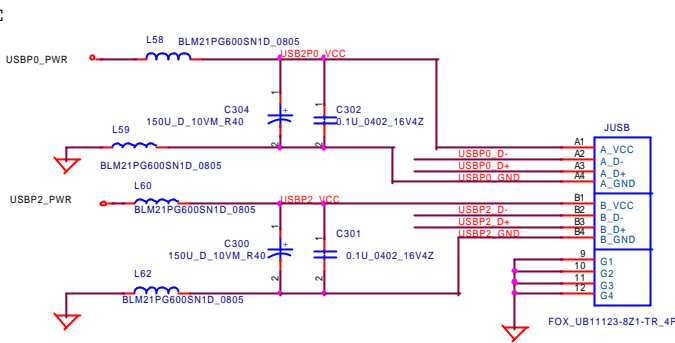
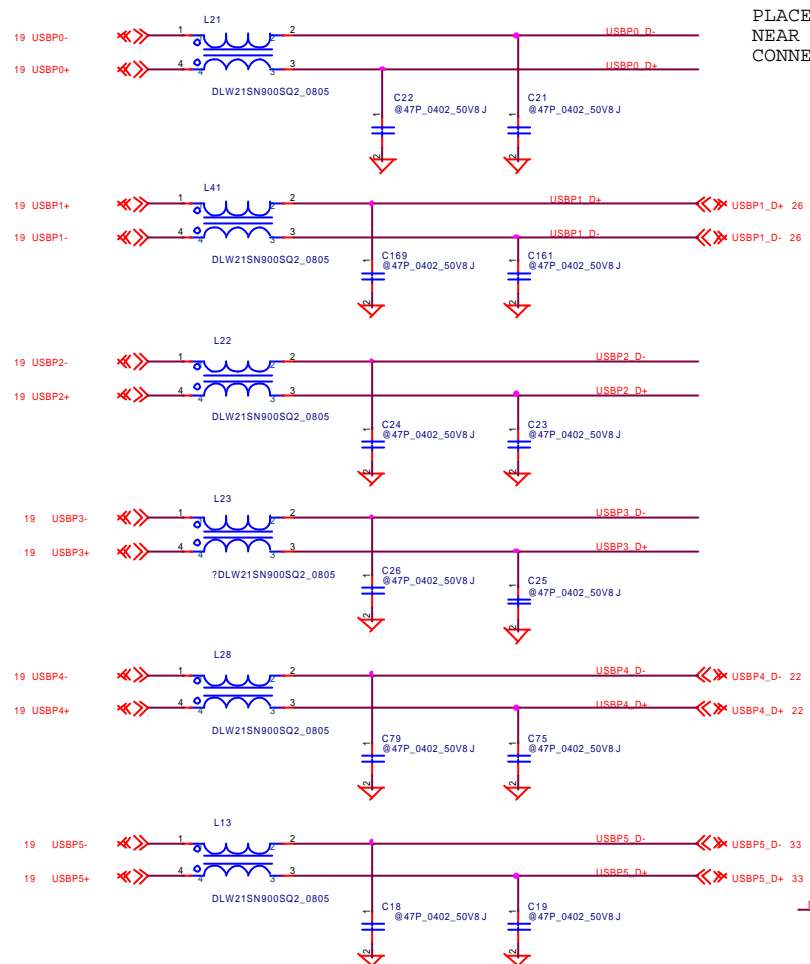


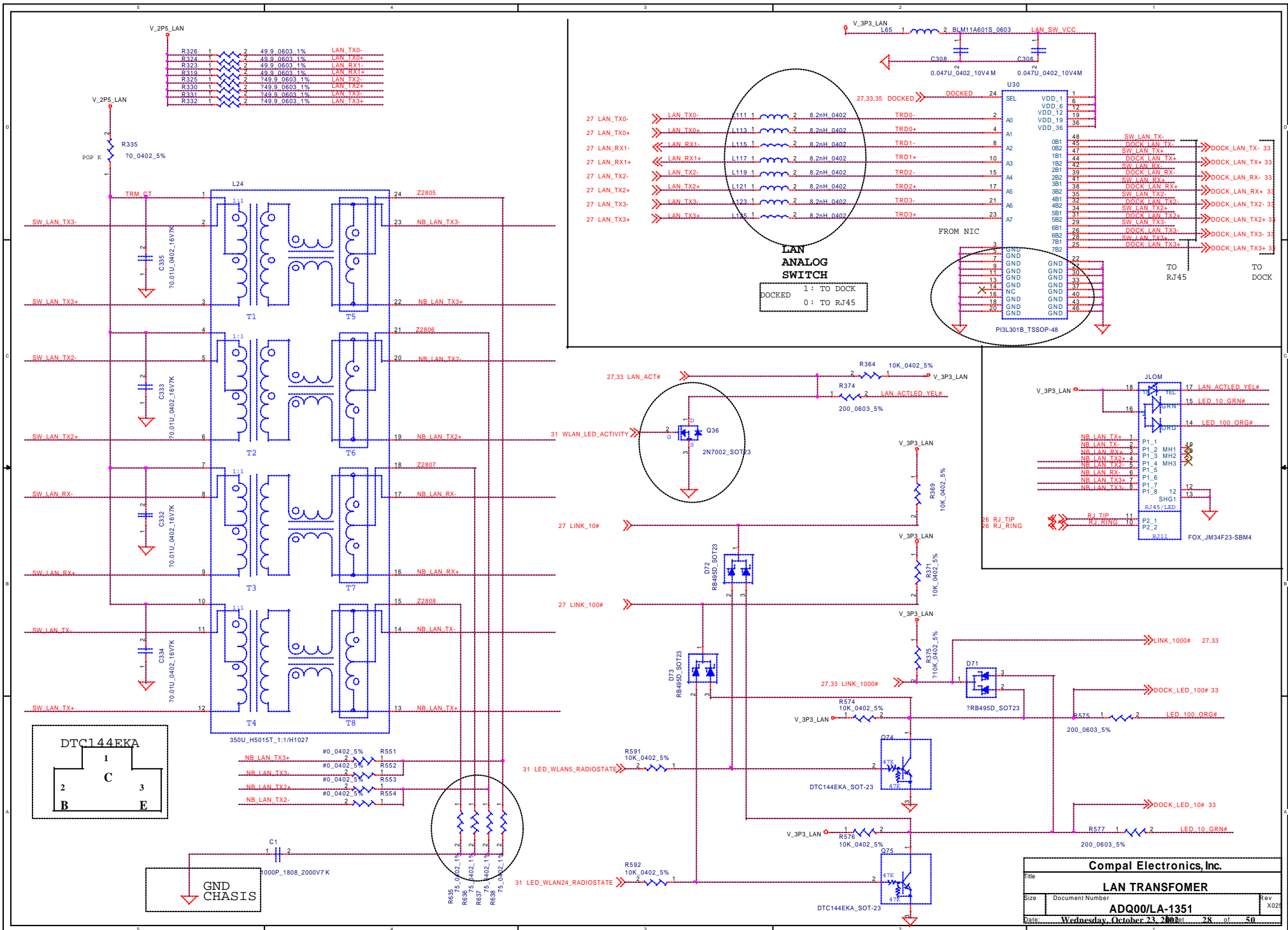


GAIN	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

USB PORT#	DESTINATION
0	BACK
1	BT
2	BACK
3	DOG
4	MOD
5	DOCK

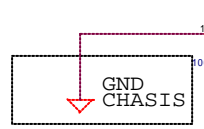
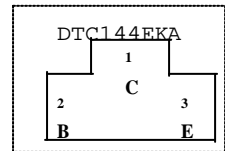
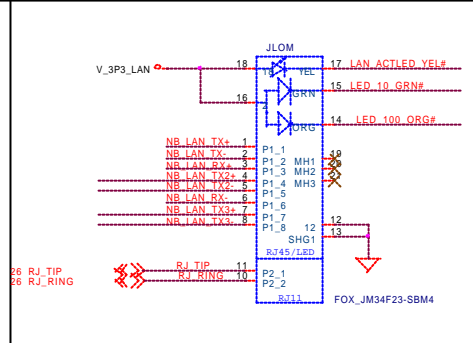
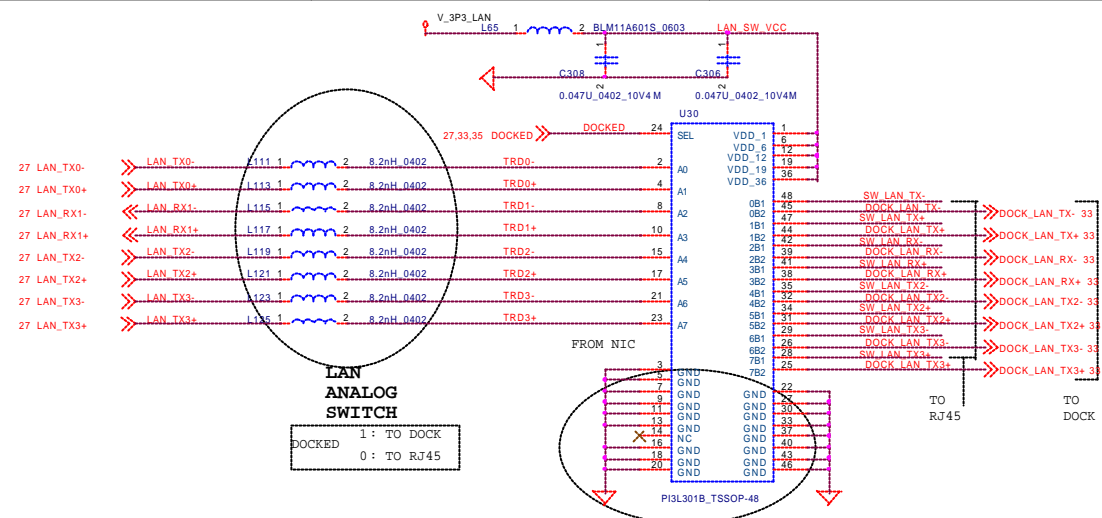
PLACE CHOKE
NEAR
CONNECTOR



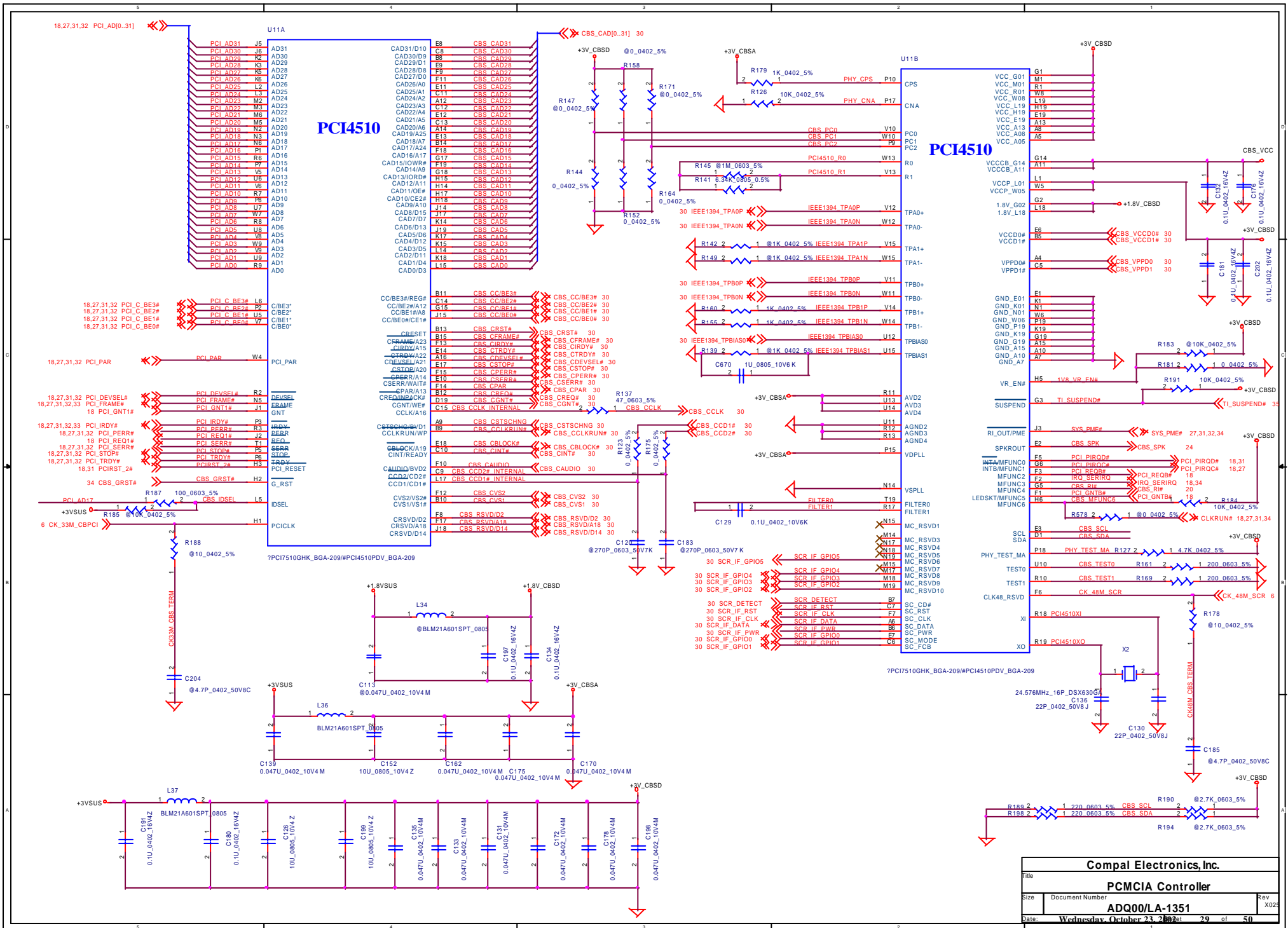


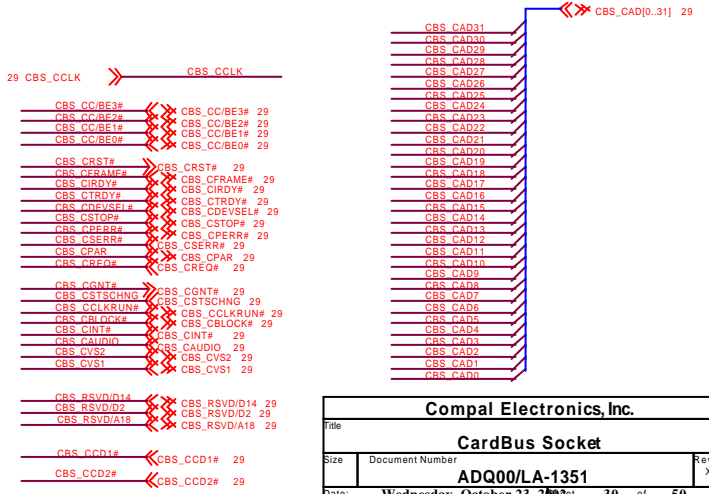
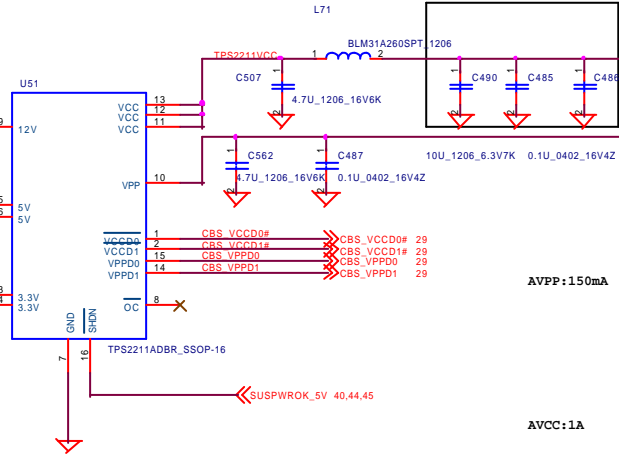
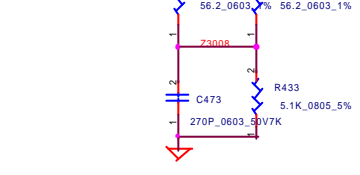
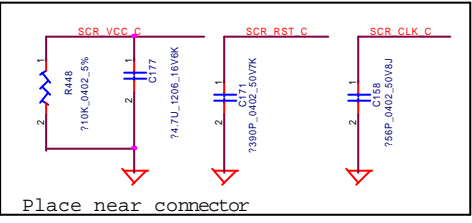
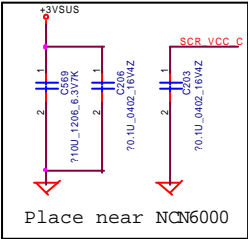
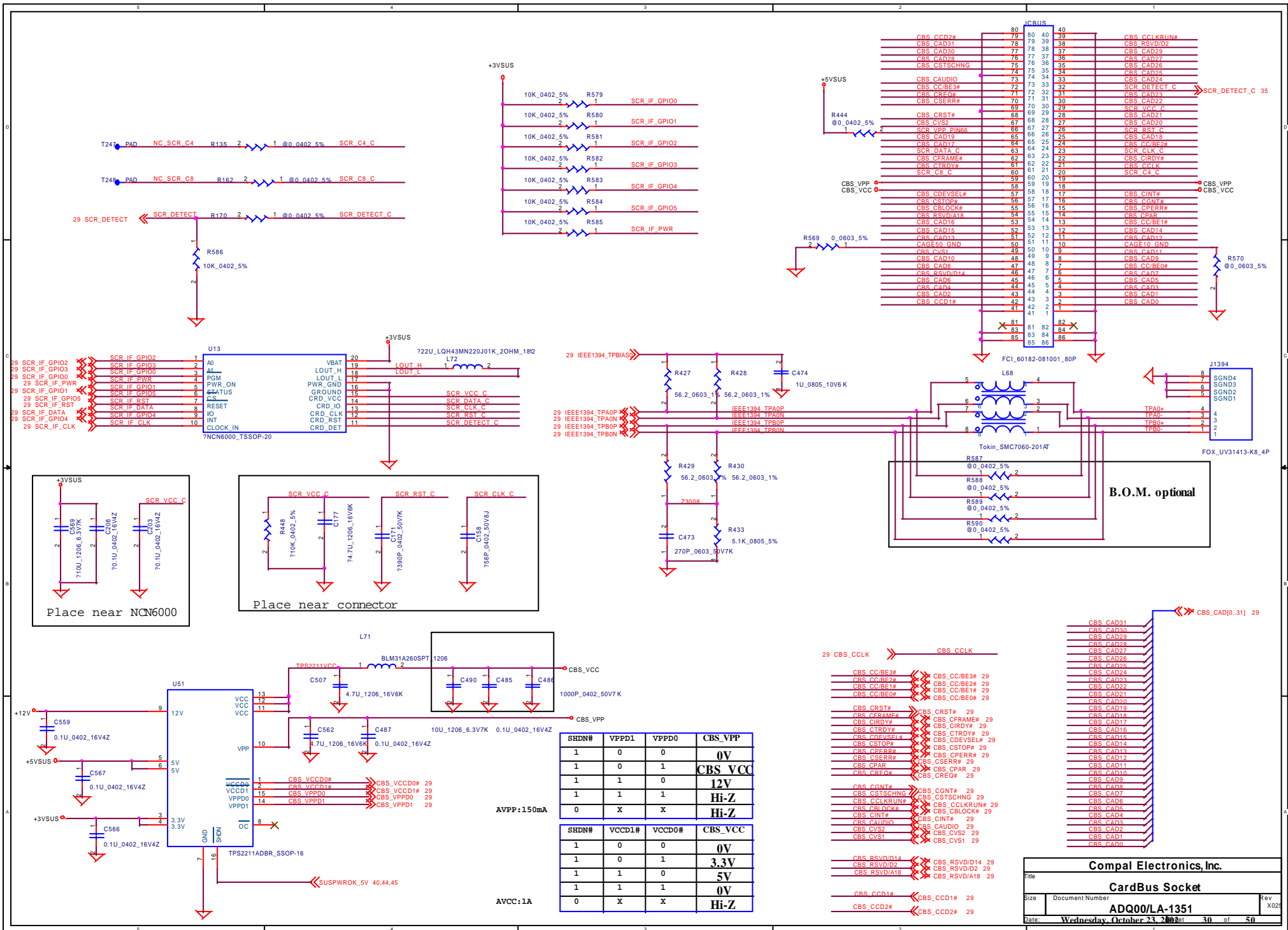
V_2P5_LAN

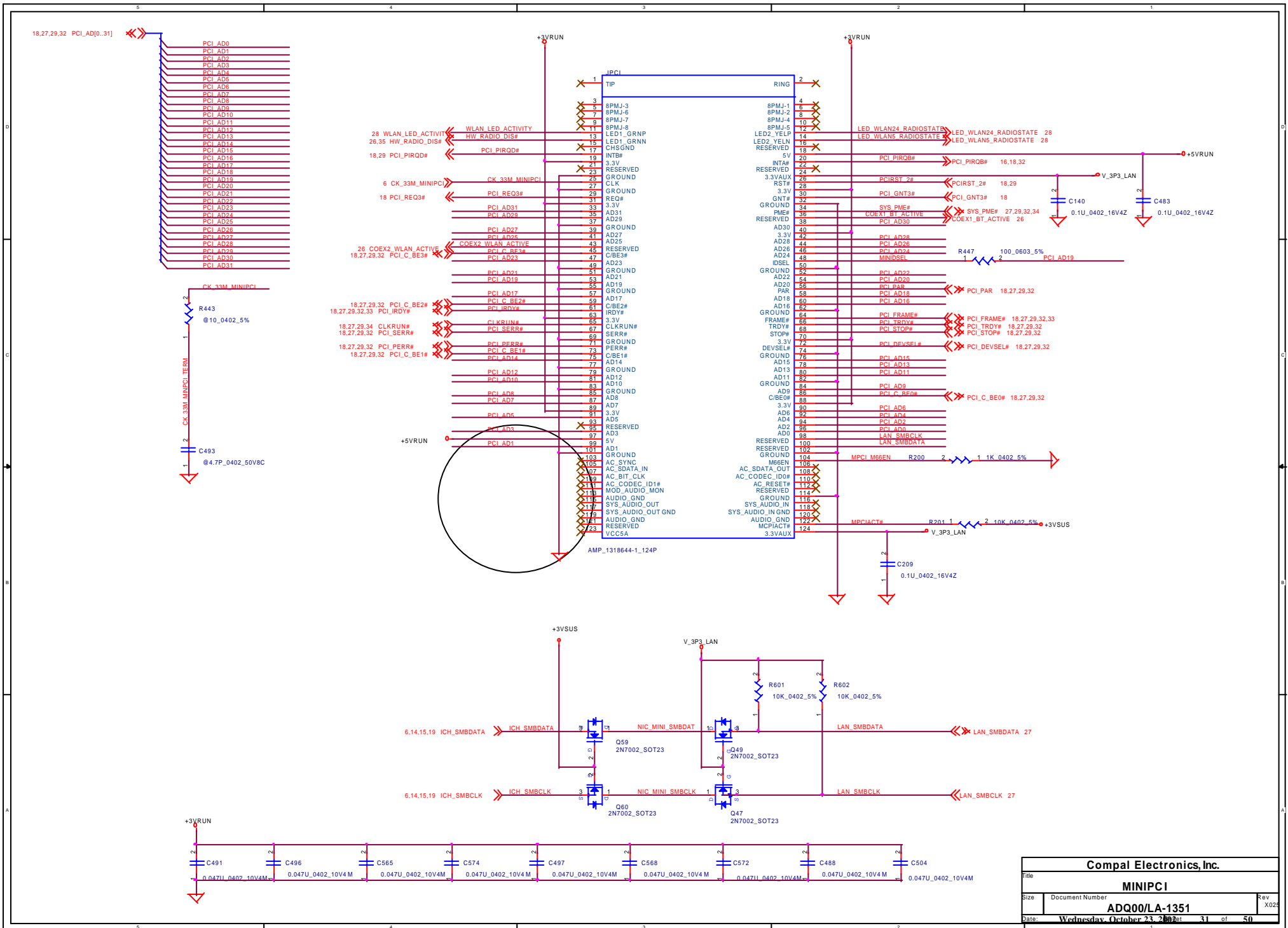
R326	1	2	49.9	0603	1%	LAN_TX0-
R324	1	2	49.9	0603	1%	LAN_TX0+
R323	1	2	49.9	0603	1%	LAN_RX1-
R319	1	2	49.9	0603	1%	LAN_RX1+
R325	1	2	749.9	0603	1%	LAN_TX2-
R330	1	2	749.9	0603	1%	LAN_TX2+
R331	1	2	749.9	0603	1%	LAN_TX3-
R332	1	2	749.9	0603	1%	LAN_TX3+



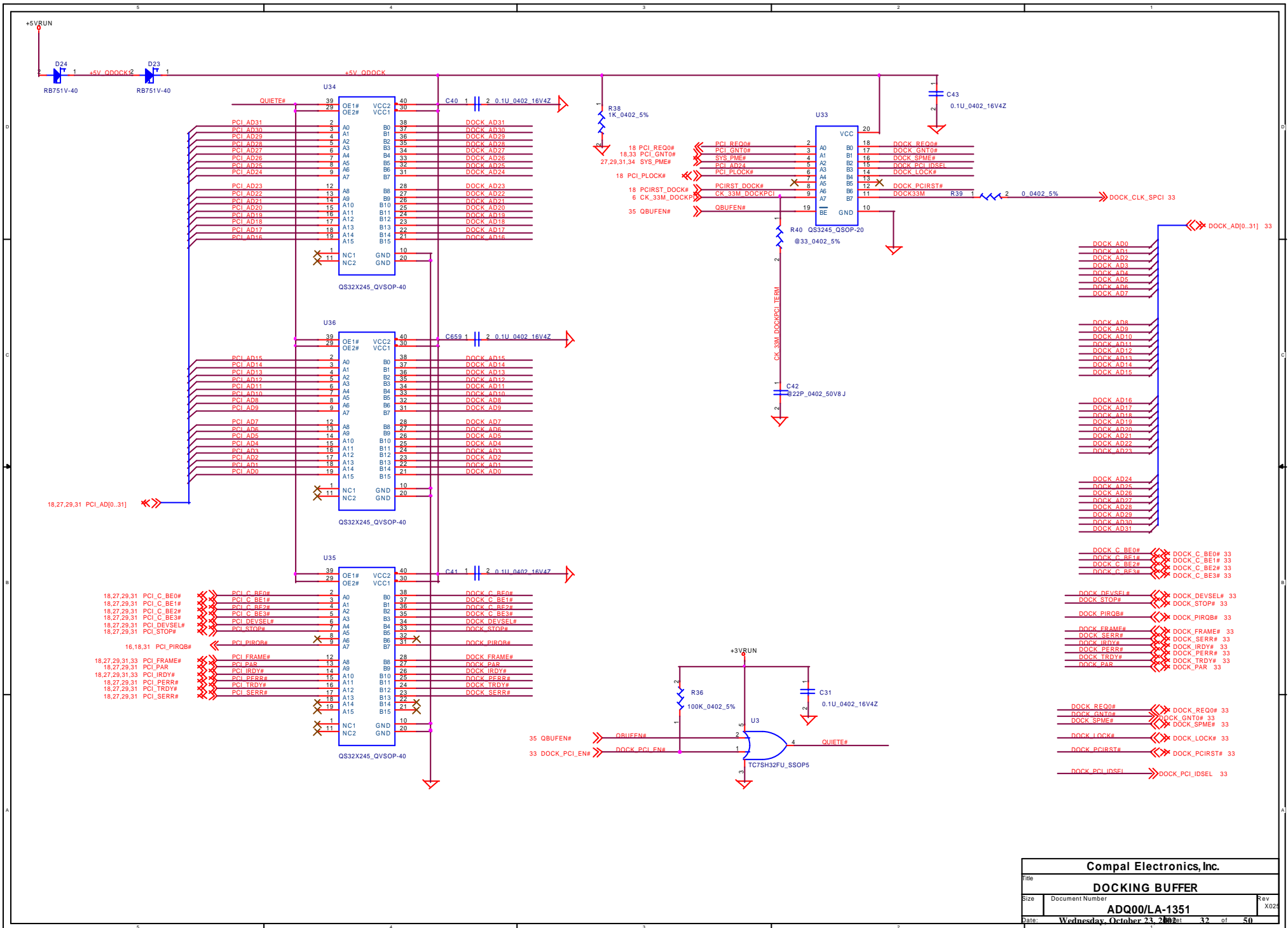
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LAN TRANSFORMER		
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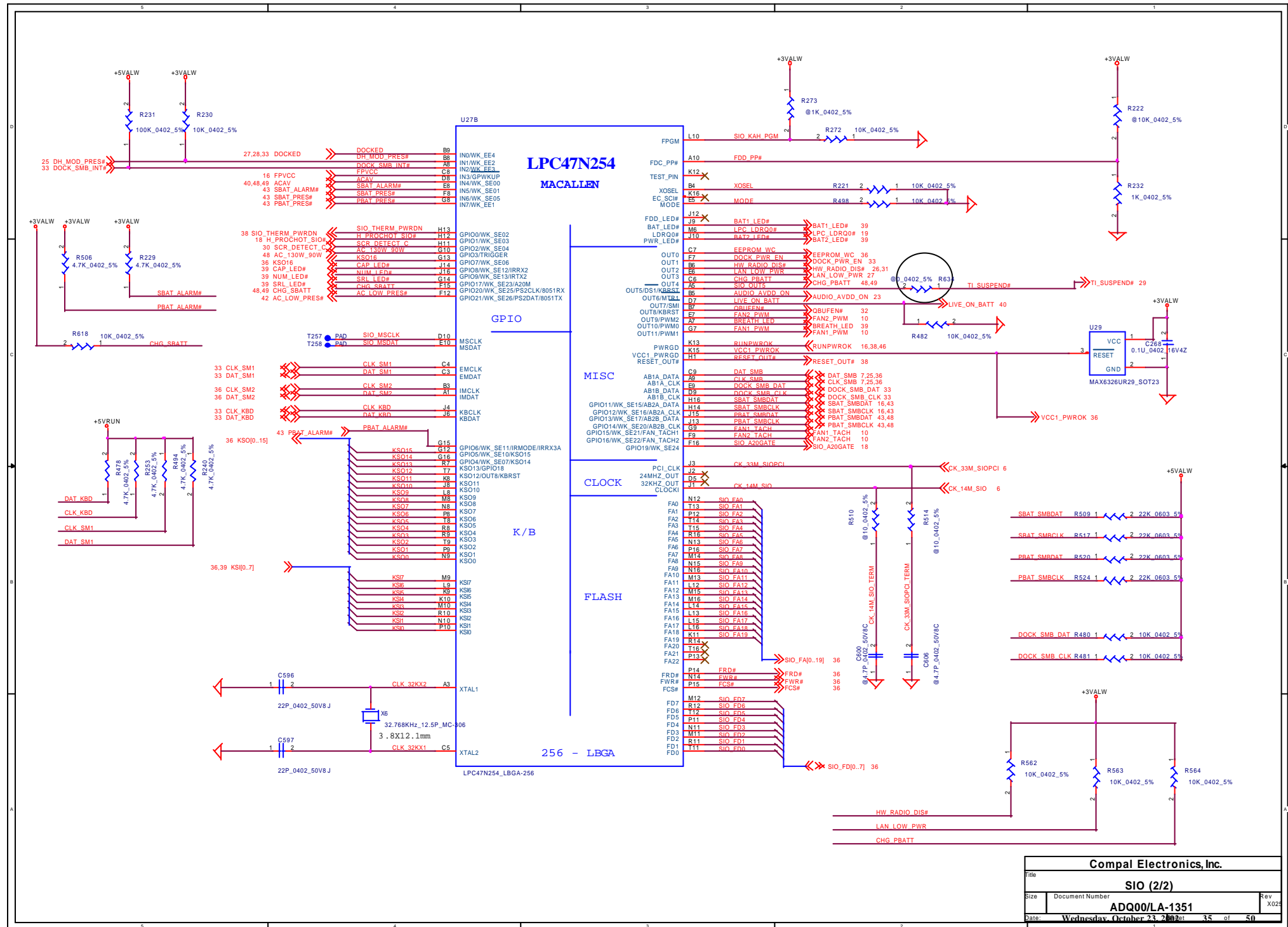


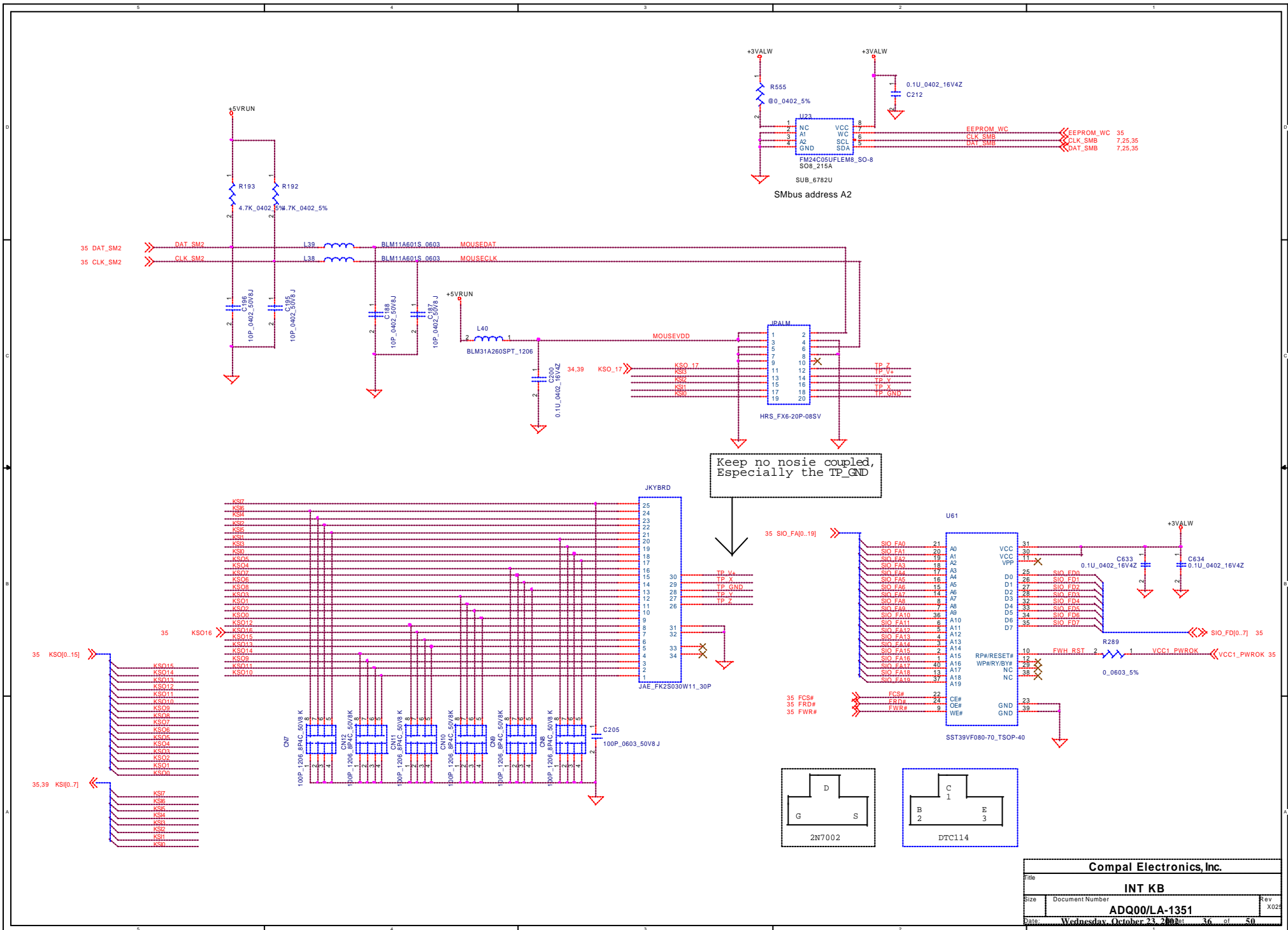




Compal Electronics, Inc.		
MINIPCI		
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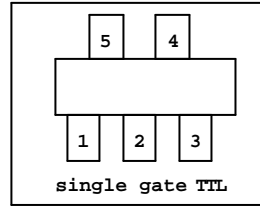
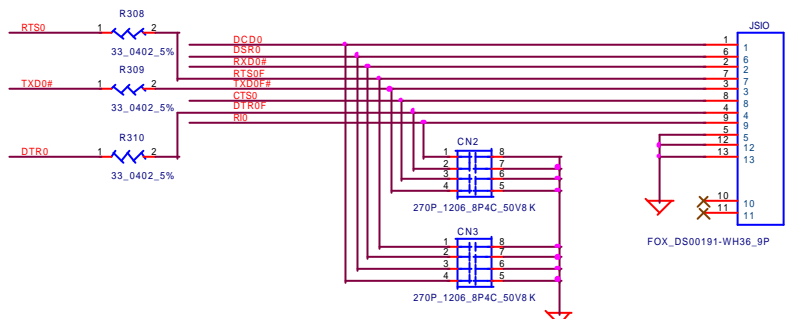
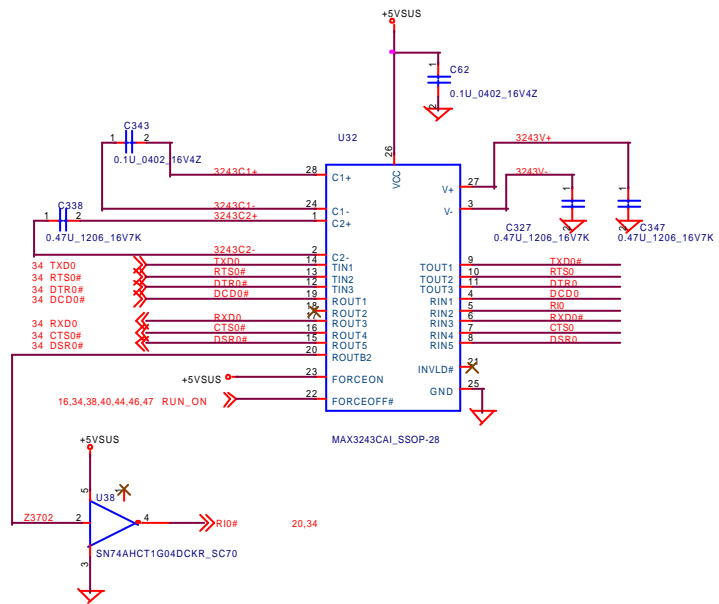
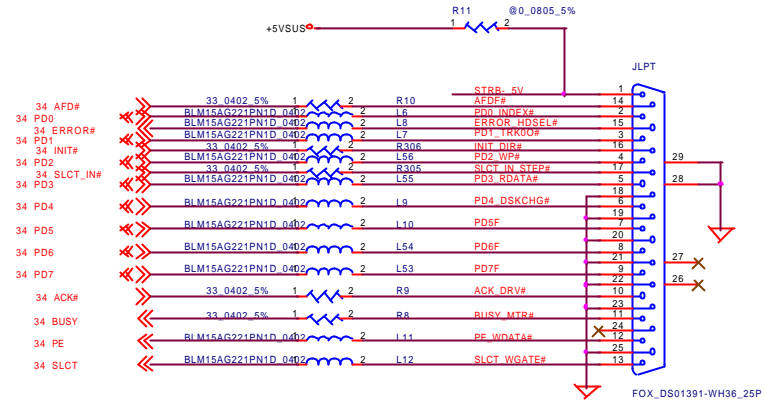
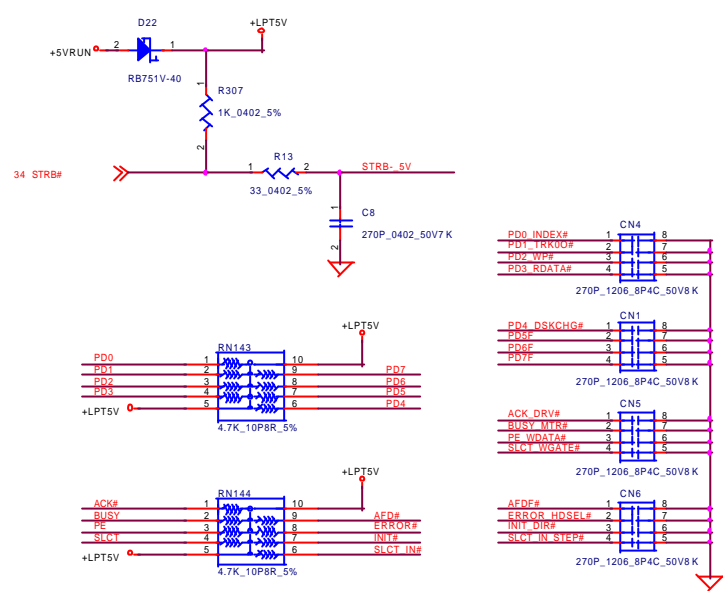


Keep no noise coupled,
Especially the TP_GND

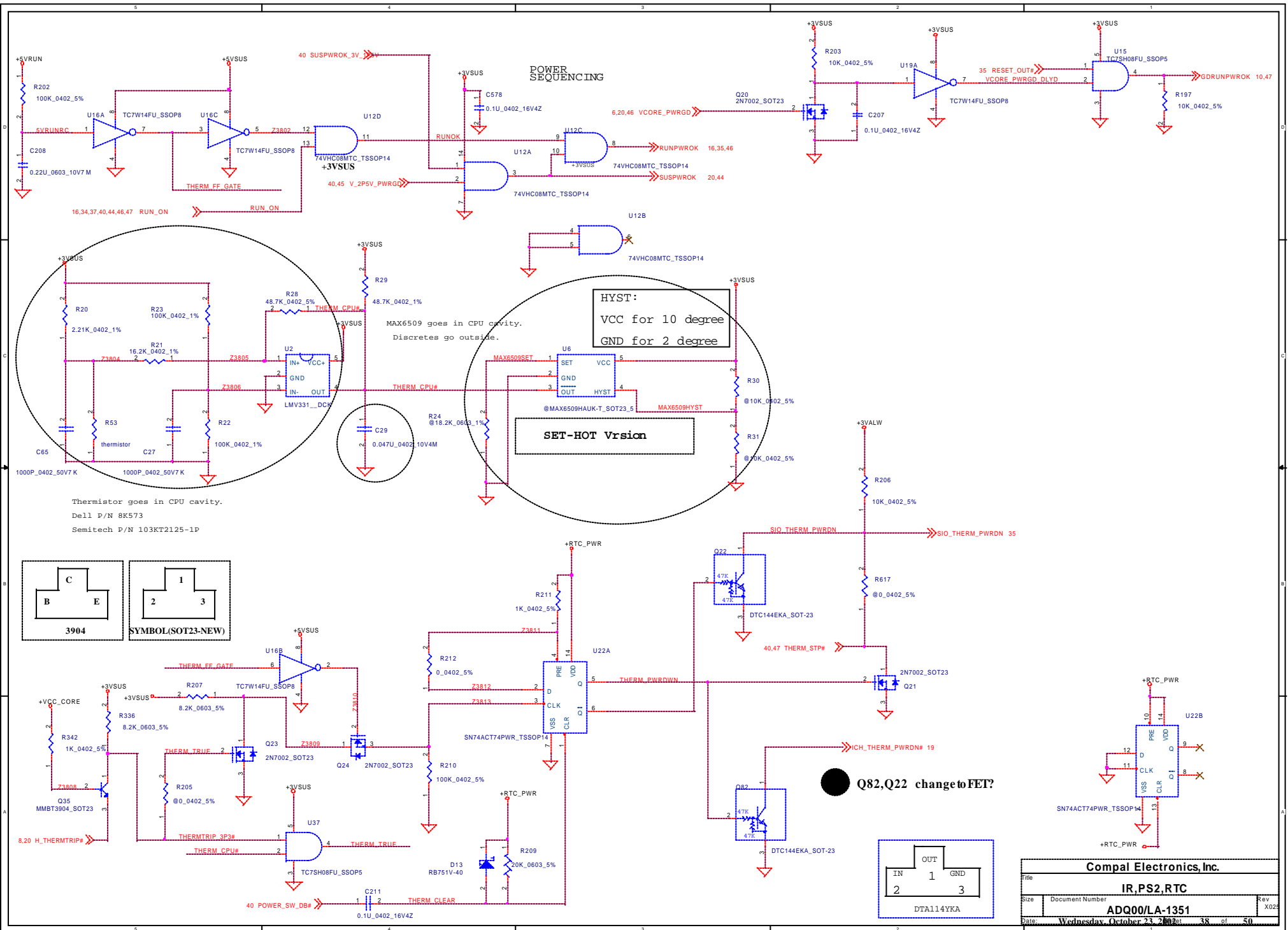
Compal Electronics, Inc.

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Parallel Port



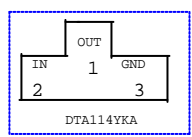
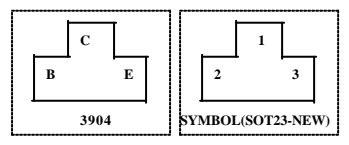
Compal Electronics, Inc.		
Title: LPT/SIO/RTC		
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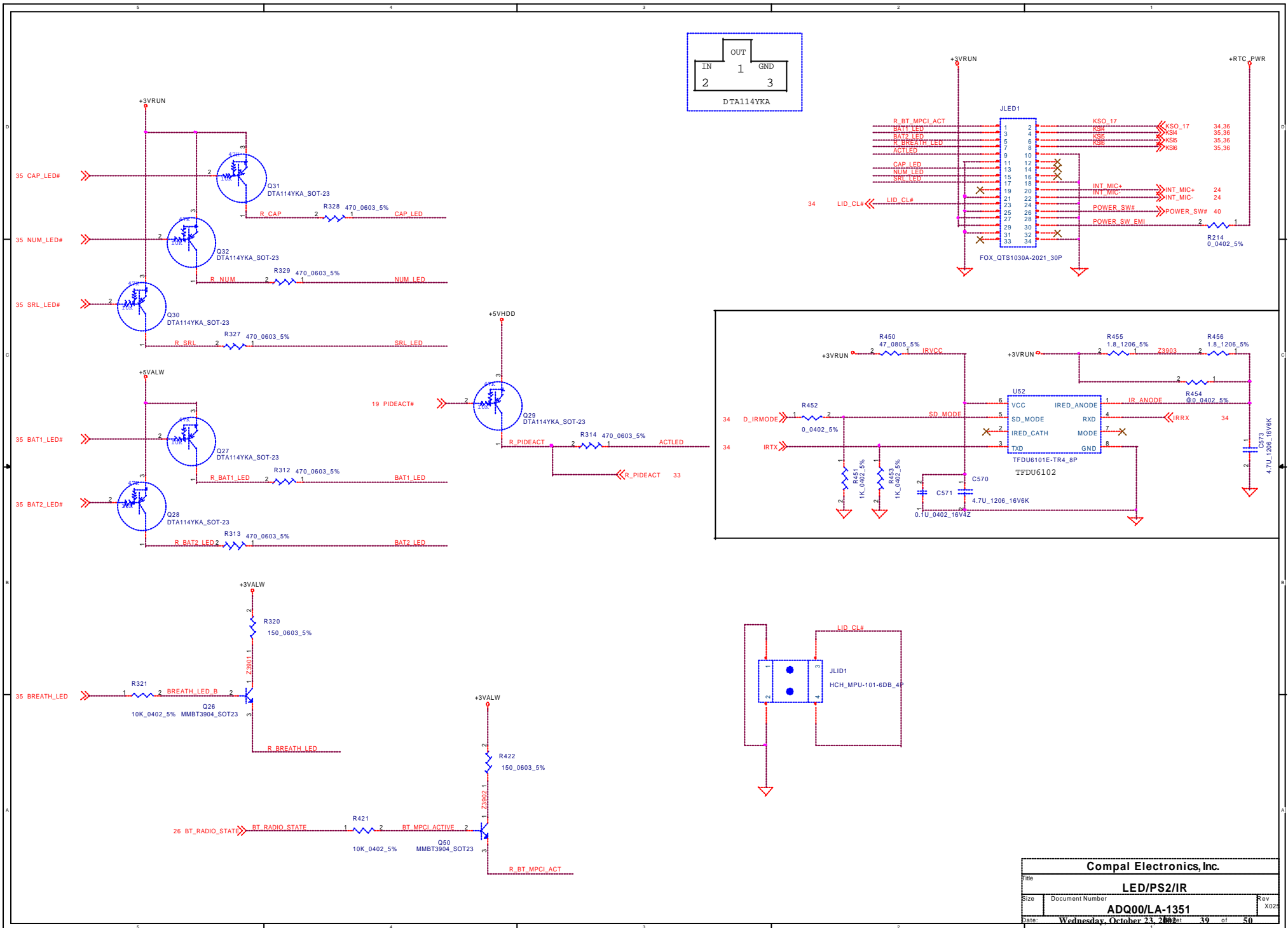
HYST:
VCC for 10 degree
GND for 2 degree

SET-HOT Vrsion

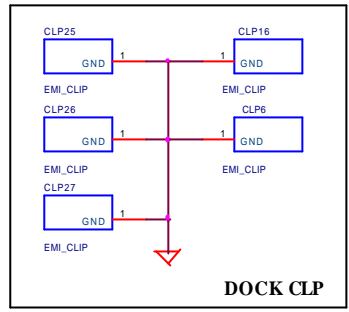
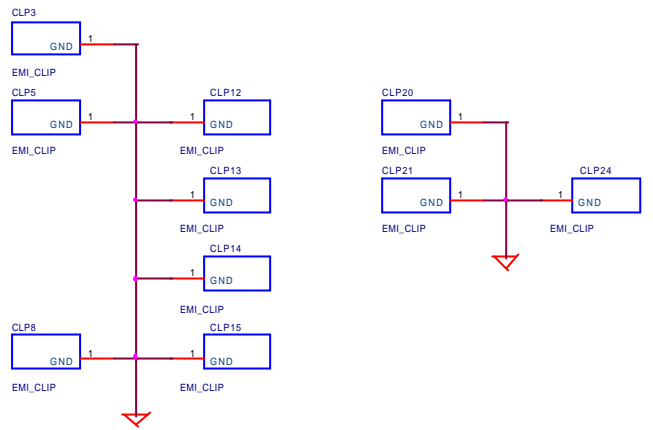
Thermistor goes in CPU cavity.
Dell P/N 8K573
Semitech P/N 103KT2125-1P



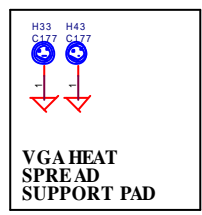
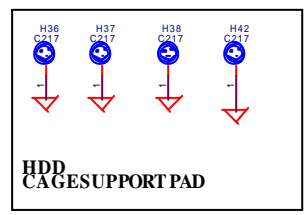
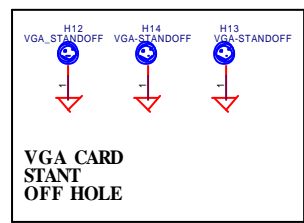
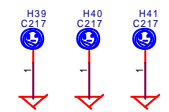
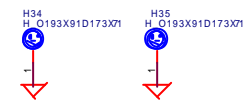
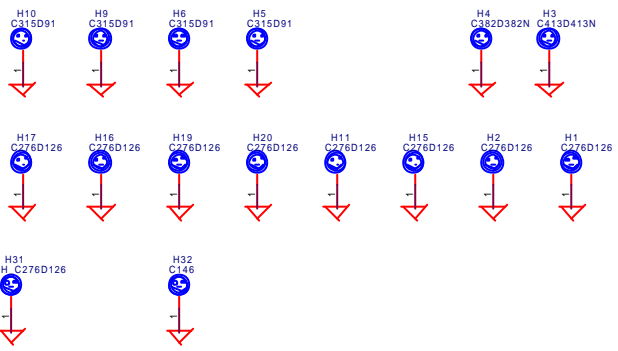
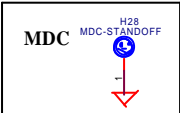
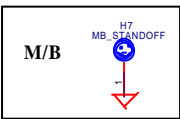
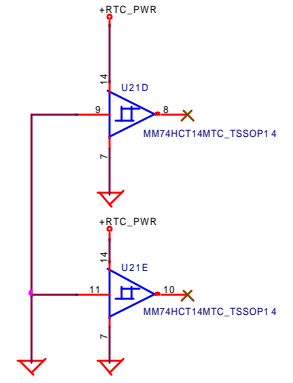
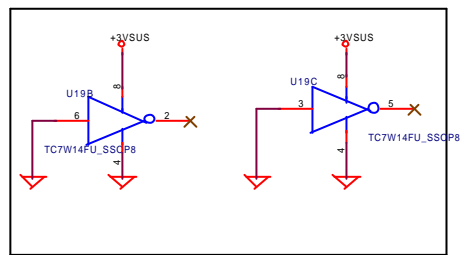
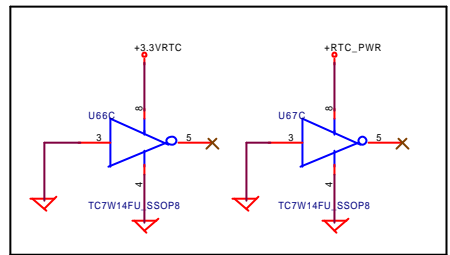
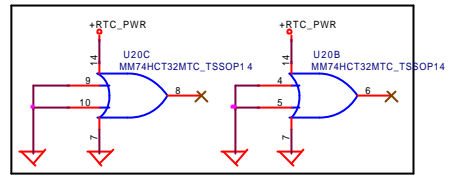
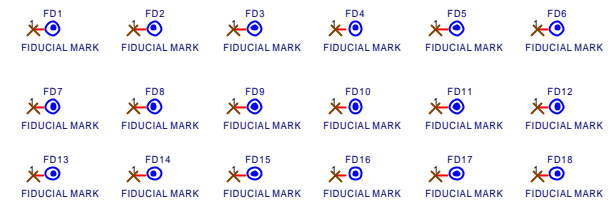
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IR,PS2,RTC		
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Compal Electronics, Inc.		
Title LED/PS2/IR		
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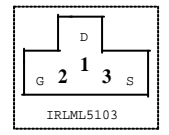
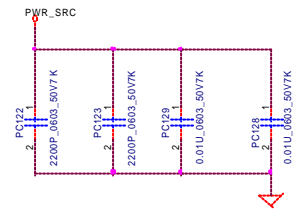
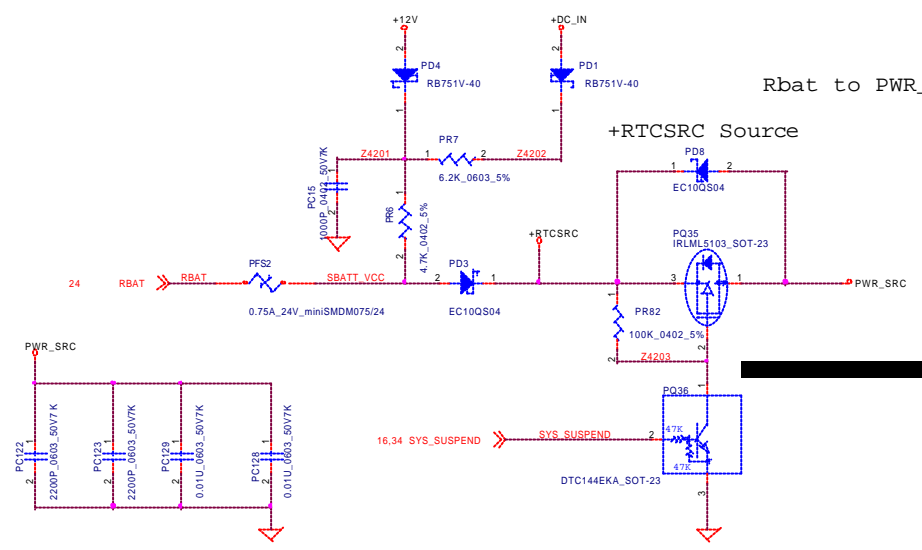


Fiducial Mark

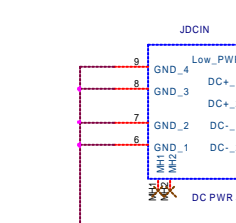


Rbat to PWR_SRC Enable

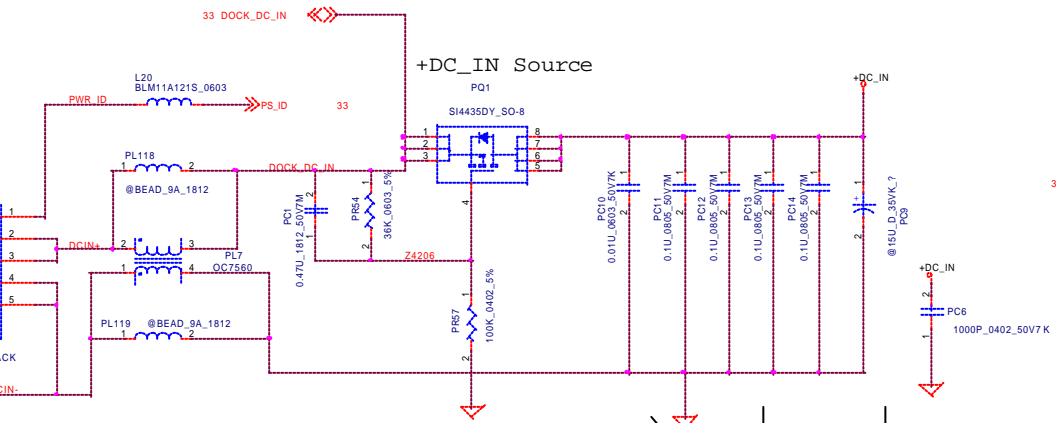
+RTCSRC Source



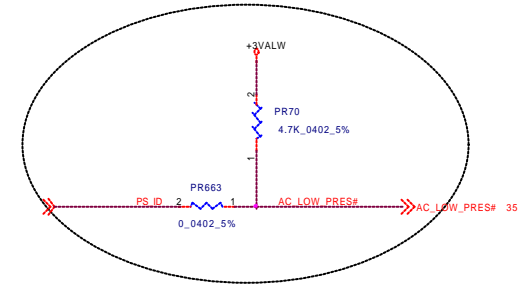
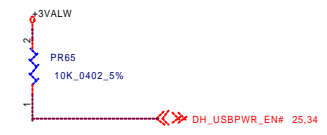
Z-series AC Adaptor Connector



+DC_IN Source



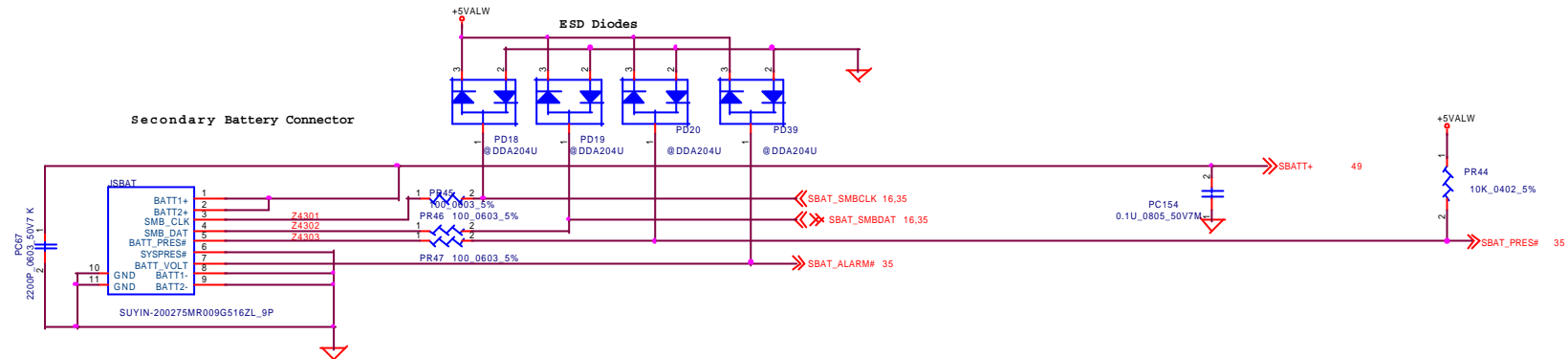
NOTE: *THE POINT LOCKED AT PS MODULE



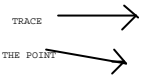
Old Low-Power Adapter Detection

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Title DC-IN		
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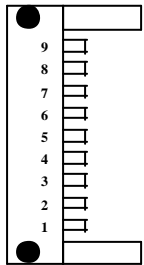
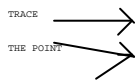
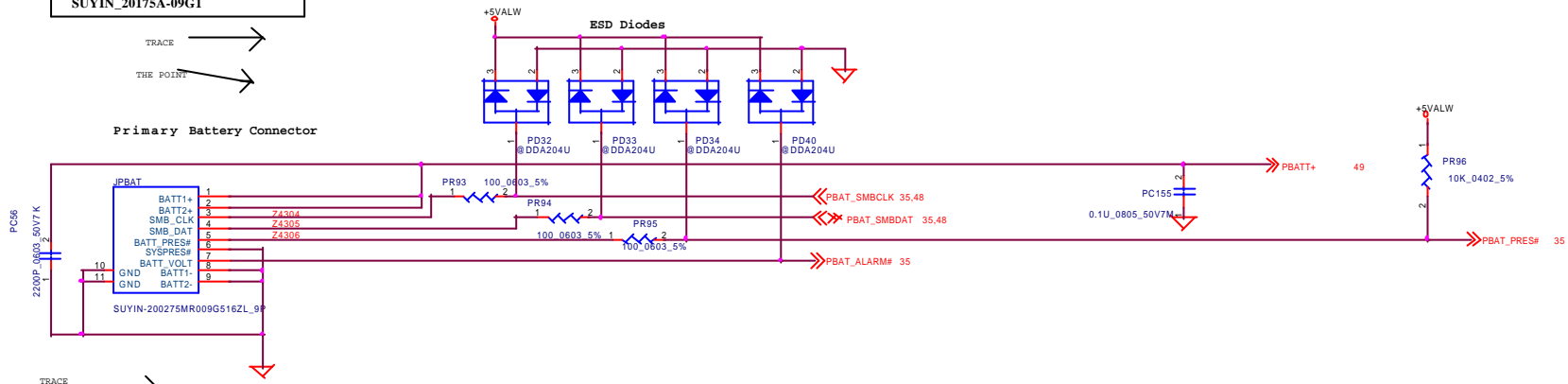
Secondary Battery Connector



SUYIN_20175A-09G1

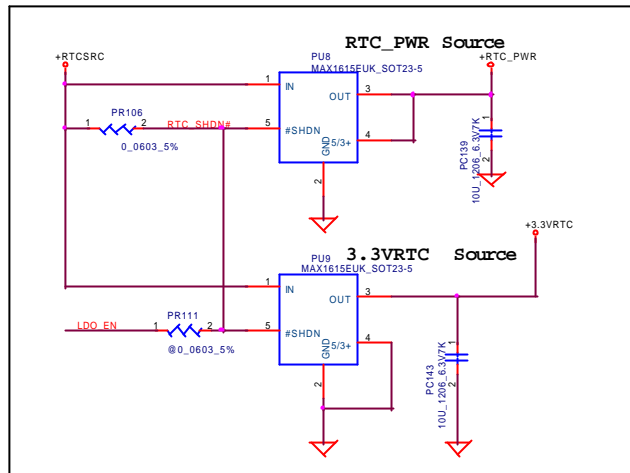
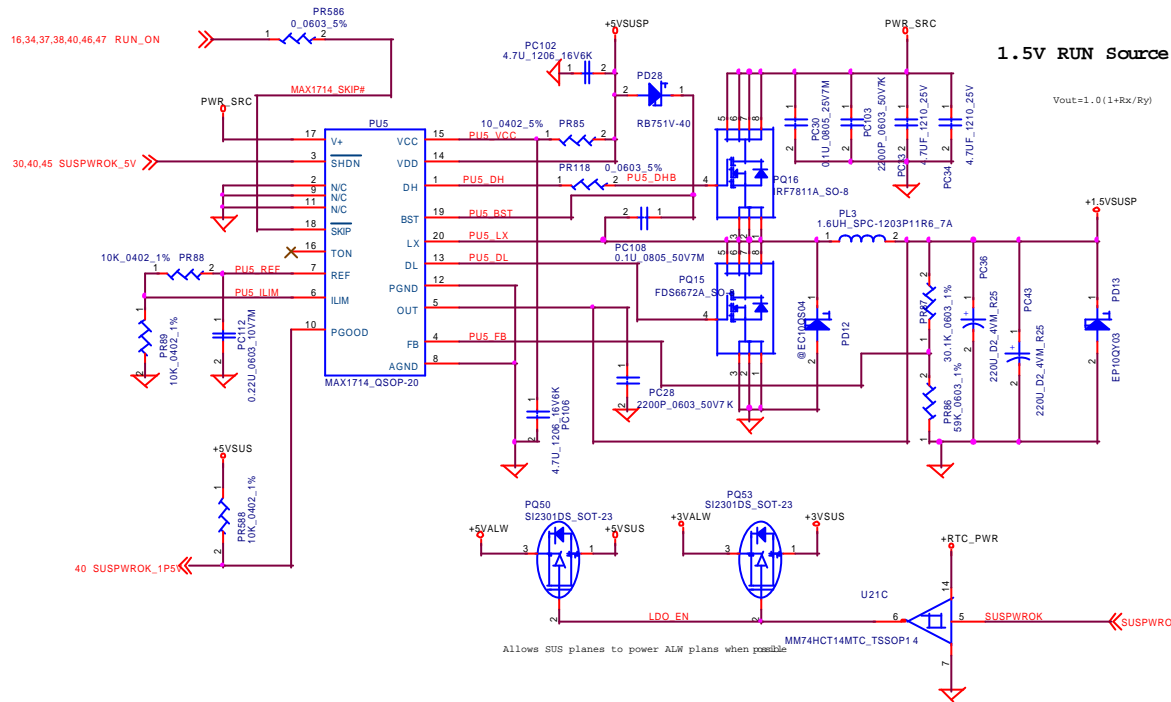


Primary Battery Connector

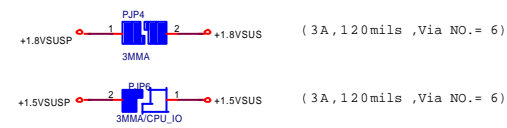
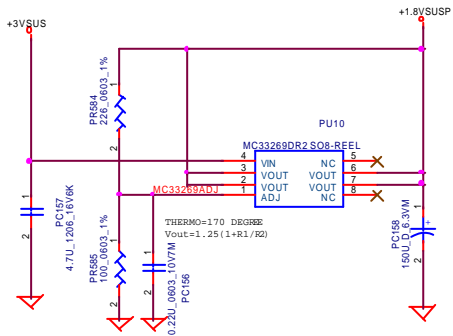


SUYIN_20175A-09G1
TOP view

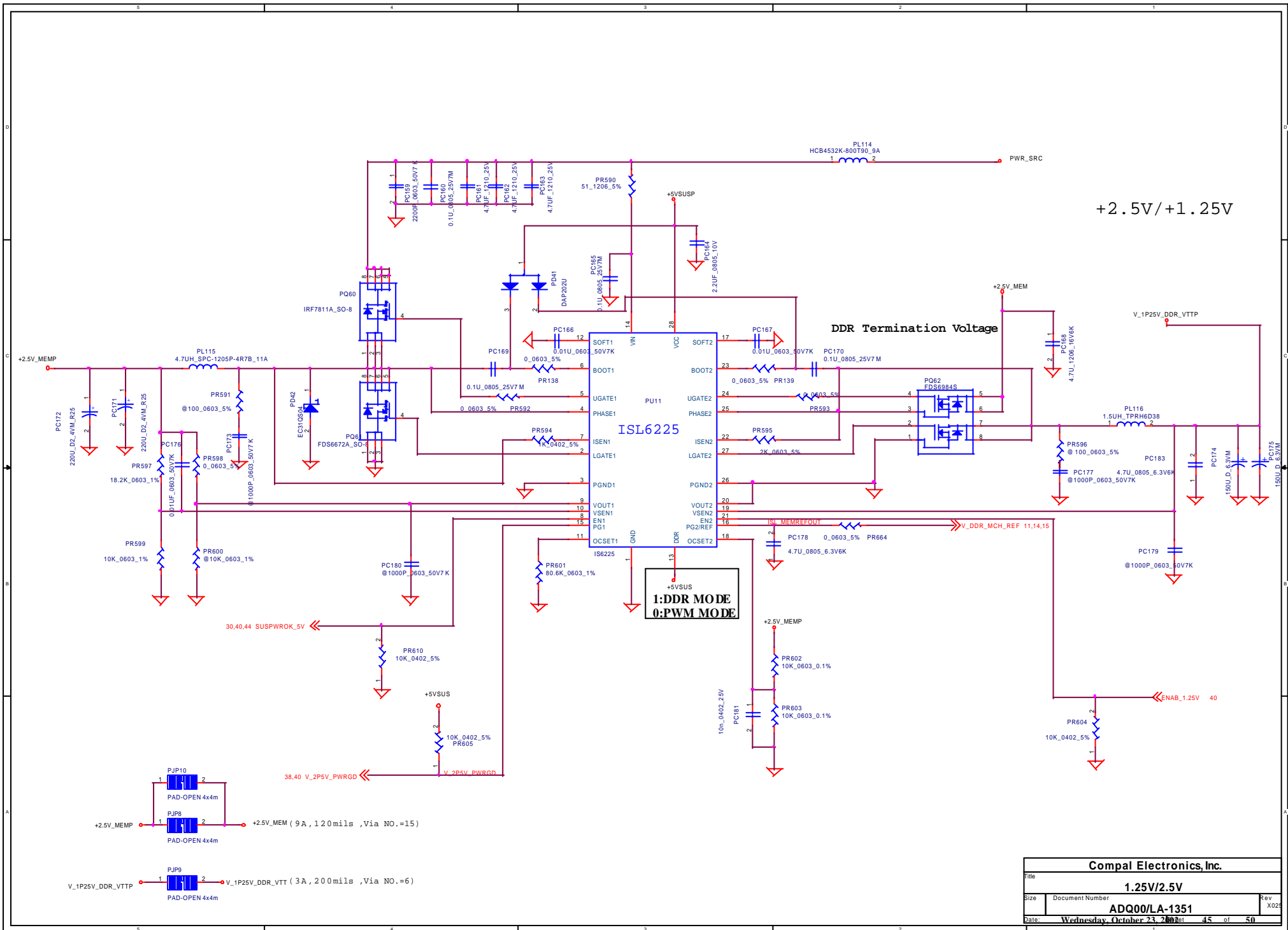
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Title		
Battery CONN.		
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+1.8V SUS Source



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Title 1.5V/1.8V		
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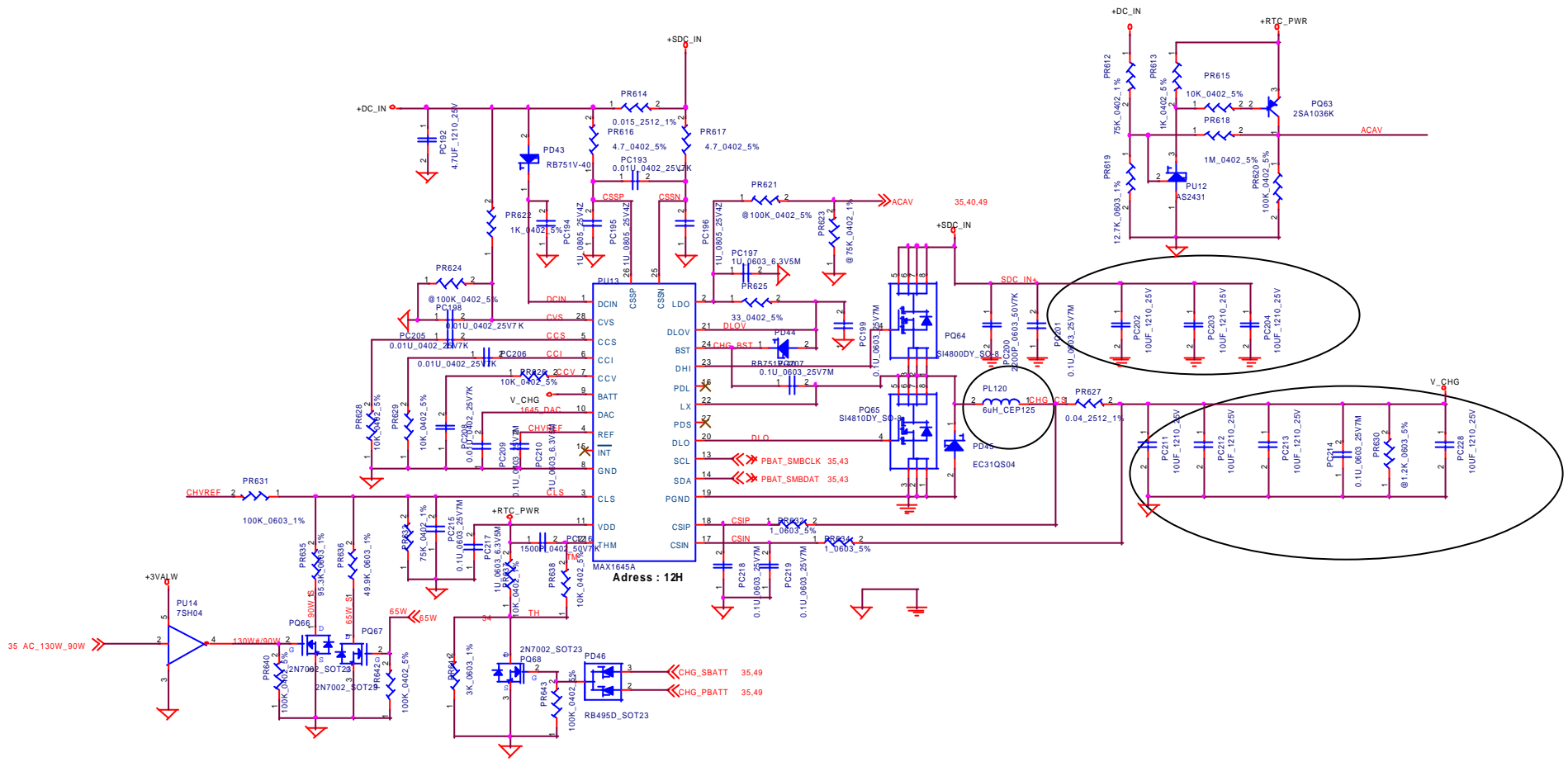


+2.5V/+1.25V

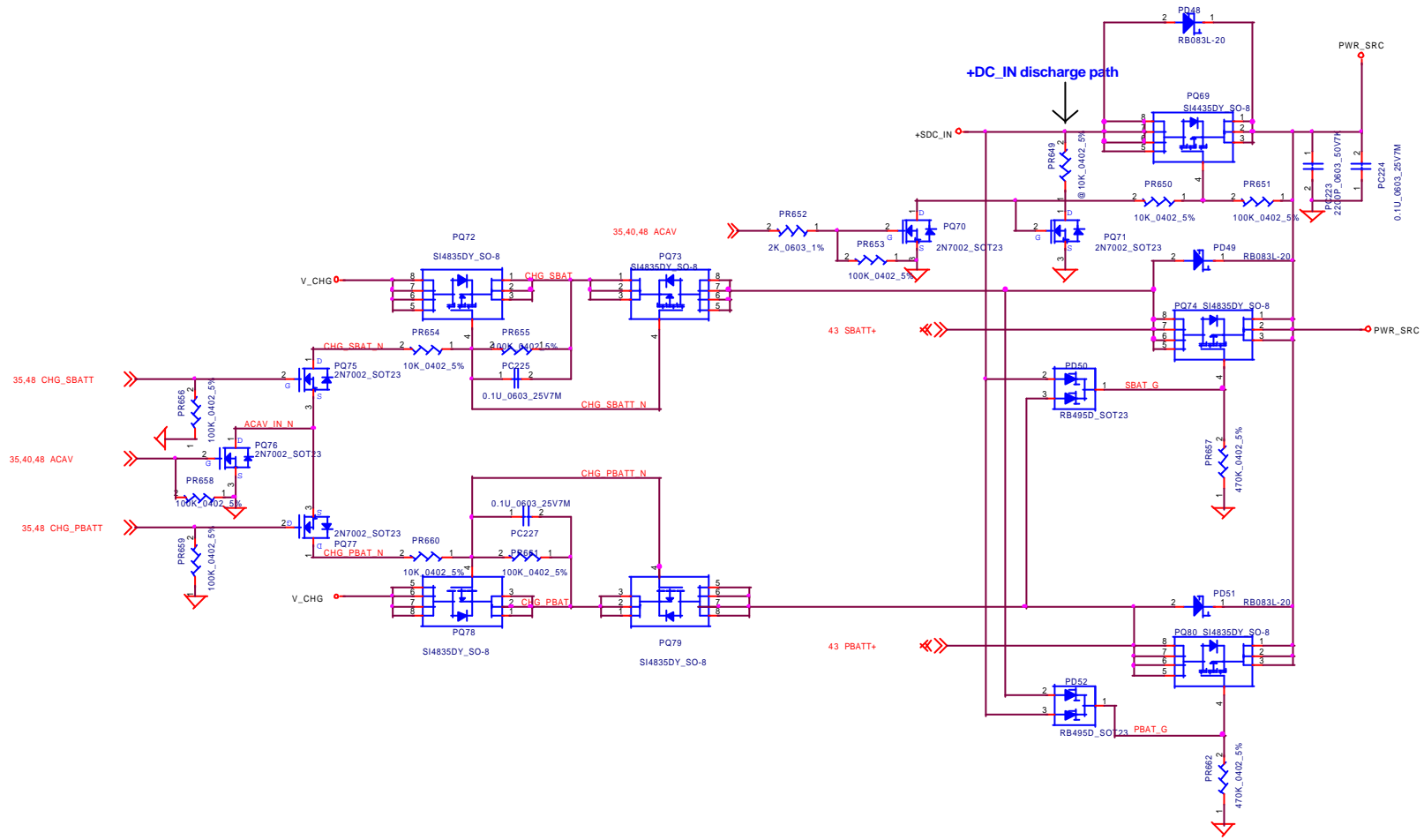
DDR Termination Voltage

1:DDR MODE
0:PWM MODE

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Title 1.25V/2.5V		
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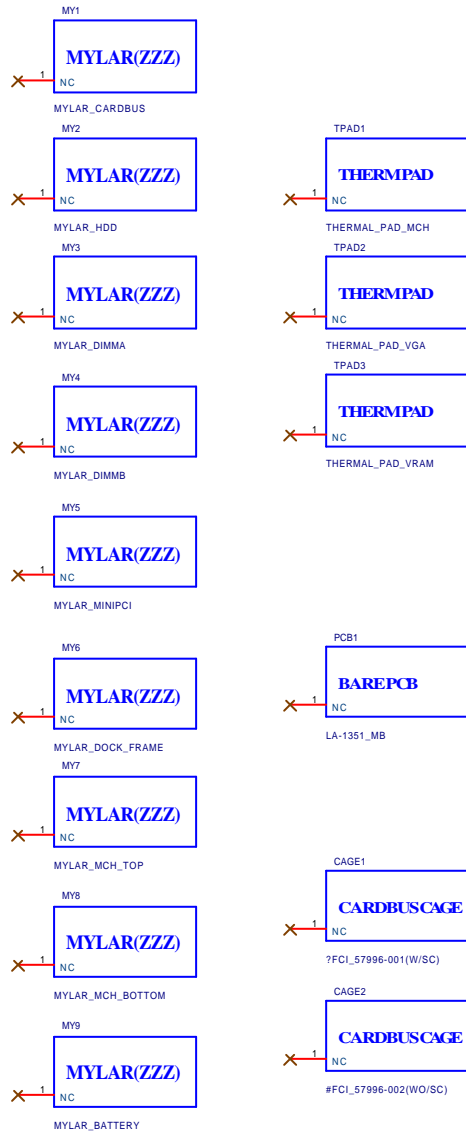
	65W (2.53A)	90W (4.03A)	130W (5.85A)
65W	H	L	L
130W#/90W	H	H	L



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PIR



ITEM	PAGE	REV.	NOTE		
1	9	X025	remove CPU VCCID jumper		
2	19	X025	Change R537 to 1K for PIDEACT# PU		
3	20	X025	remove SIO_LID_EC# signal ,PU 1CH4GPIO to +3VRUN		
4	21	X025	change JMOD1 pin8,10,14,16,9,11, to NC,conect SATA_DET# to pin13	reserve C693,R629,R630 for CD AUDIO termination	
5	25	X025	change Q1,F1,F2,L25 part to meet Doghouse power current requirement	add R639 for USB port 3 power enable,reserve R640	
6	27	X025	add L109, L110 for BCM4401 PCI power for WOL issue		
7	28	X025	add eight 8.2uH inductor to TX/RX line	seperate RN1 to 4 small resistors	Change Q36 to 2N7002
8	29	X025	remove D11 for TI_SUSPEND#		
9	31	X025	Change JPC11 pin109 and pin 123 to NC and remove R457,C576		
10	34	X025	add R628 PU to U27 pin D12		
11	35	X025	reserve R634 for TI_SUSPEND#		
12	38	X025	change OTP to discrete solution		
13	40	X025	change Q12 and Q77 to SI4810		
14	42	X025	remove AC LOW PRES circuit		
15	46	X025	change PQ37 to FCX789	remove PC147 change PR1,PR10 to 3.3ohm	add PC229,PC230,PC231,PC232
16	47	X025	change PR20 to 3.74K		
17	48	X025	addPC228,change C202,PC203, PC204,PC211,PC212,PC213,PC214 to 10uF/25V	Change PL120 to 6uH	

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