

# SULLIVAN

REV : X01

@ : Depop Component for All

Dothan Schematic with Capture CIS and Function field

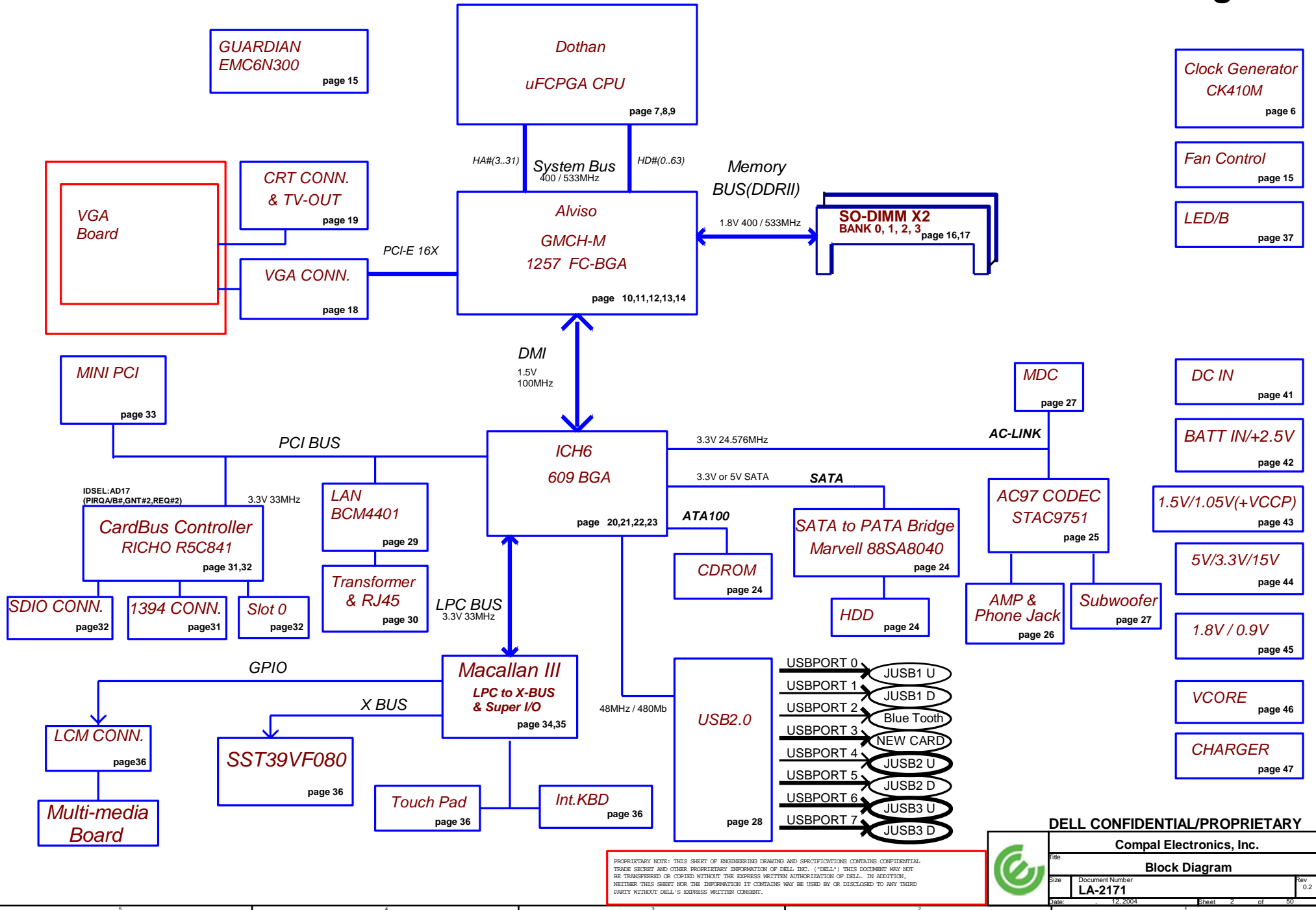
uFCPGA Dothan  
02-11-2004  
REV: 0.2

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Title Cover Sheet		
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Block Diagram		
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**PM TABLE**

State \ power plane	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS +1.5VSUS	+5VRUN +3VRUN +0.9V_DDR_VTT +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP +15V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

**PCI TABLE**

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
MINI PCI	AD19	3	D,B
LAN	AD16	4	C

**USB TABLE**

USB PORT#	DESTINATION
0	JUSB1 (Top)
1	JUSB1 (Bottom)
2	Blue Tooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	JUSB3 (Top)
7	JUSB3 (Bottom)

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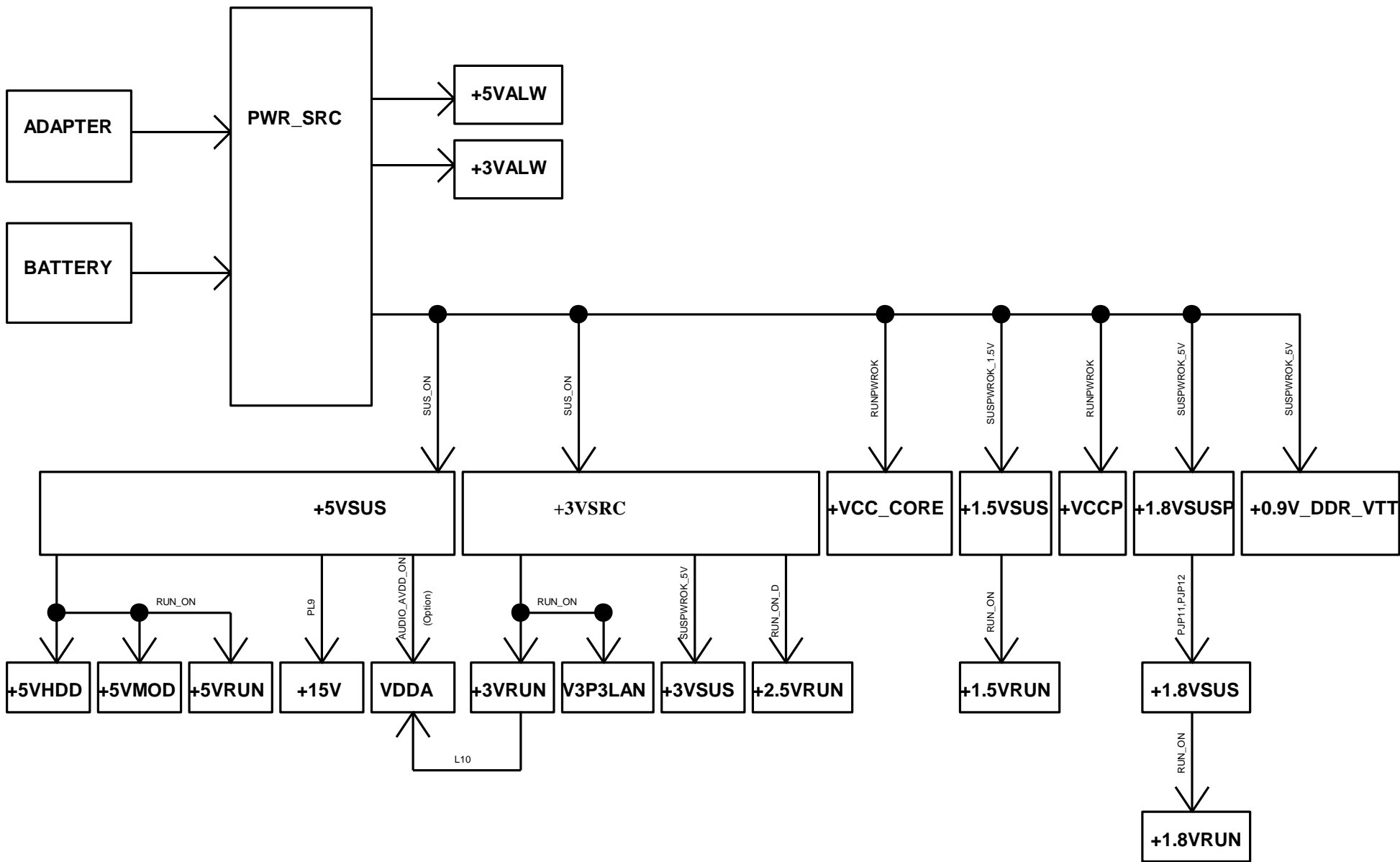
**Compal Electronics, Inc.**

**Index and Config.**



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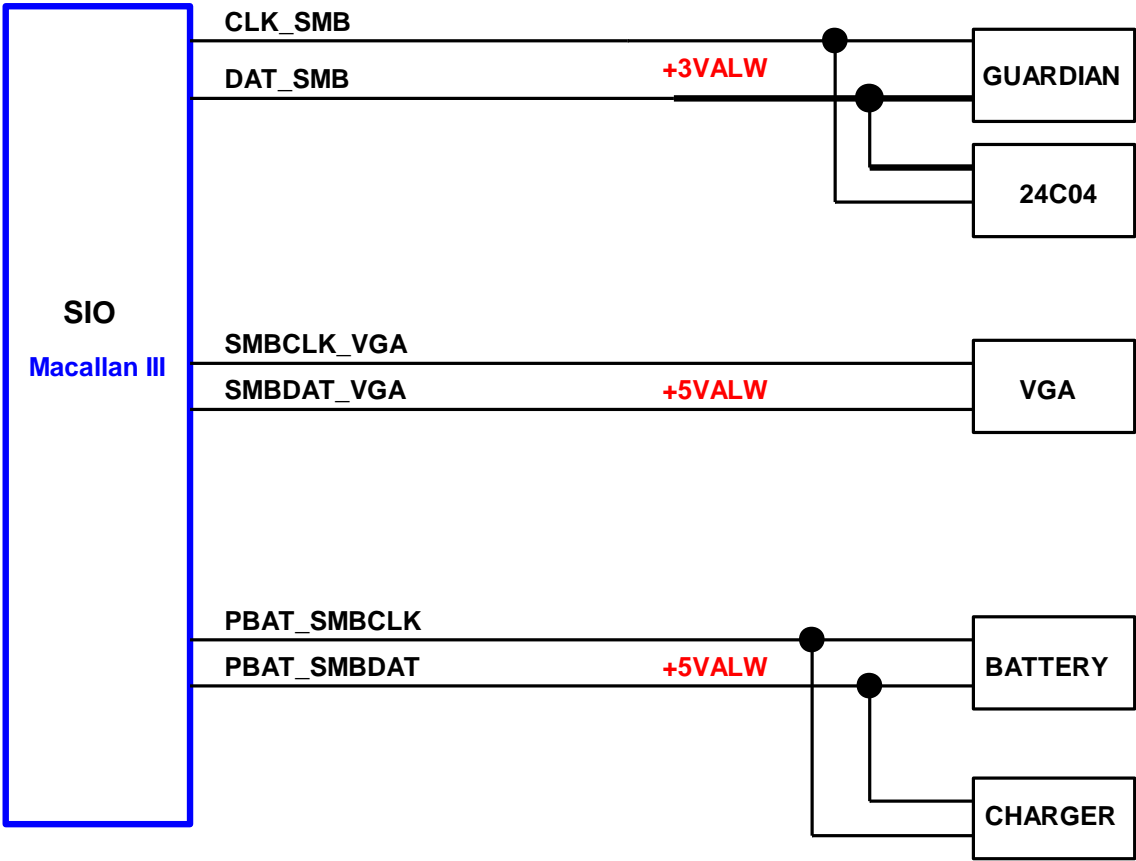
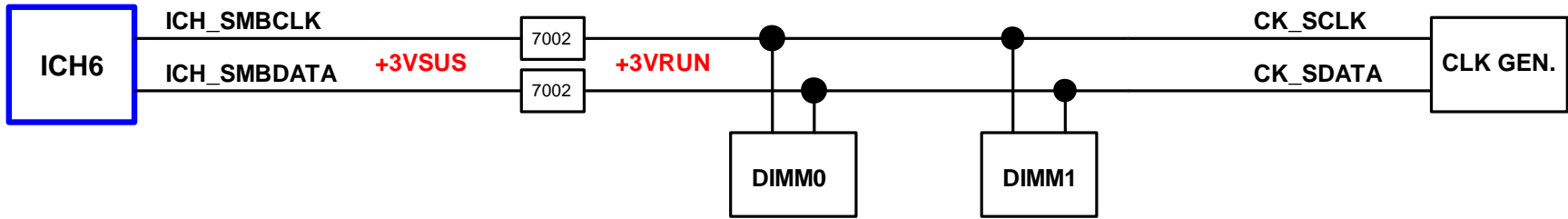
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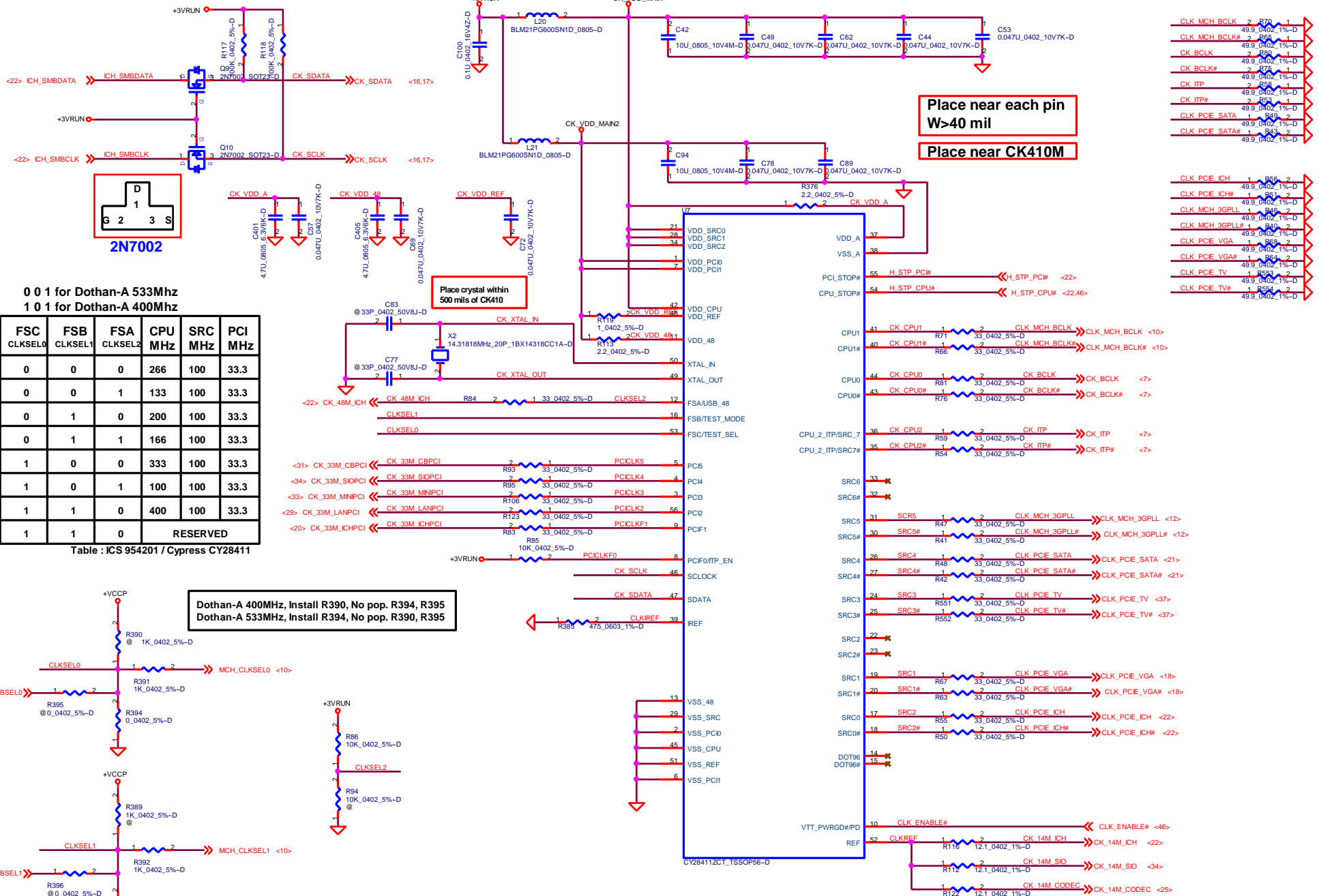
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Title <b>Power Rail</b>		
Size <b>LA-2171</b>	Document Number	Rev 0.2
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	Device	Address
ICH6-SMBus	DIM0	A0h
	DIM1	A2h
	CLK GEN.	D2h
EC-SMBus	GUARDIAN	5Eh
	24C04	A2h
	VGA	58h
	Battery	16h
	Charger	12h

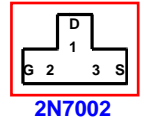
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**SMBUS TOPOLOGY**  
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Place near each pin  
W>40 mil

Place near CK410M



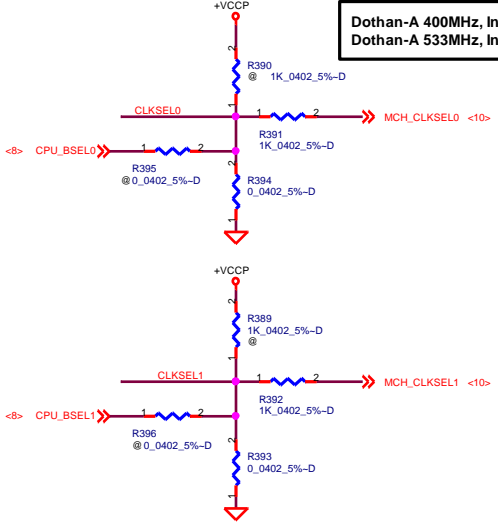
0 0 1 for Dothan-A 533Mhz  
1 0 1 for Dothan-A 400Mhz

FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	0	RESERVED		

Table : ICS 954201 / Cypress CY28411

Dothan-A 400MHz, Install R390, No pop. R394, R395  
Dothan-A 533MHz, Install R394, No pop. R390, R395

- CLK\_MCH\_BCLK# 2 R70 1 49.9\_0402\_1%-D
- CLK\_MCH\_BCLK# 2 R56 1 49.9\_0402\_1%-D
- CK\_BCLK 2 R58 1 49.9\_0402\_1%-D
- CK\_BCLK# 2 R57 1 49.9\_0402\_1%-D
- CK\_ITP# 2 R58 1 49.9\_0402\_1%-D
- CLK\_PCE\_SATA 1 R49 2 49.9\_0402\_1%-D
- CLK\_PCE\_SATA# 1 R53 2 49.9\_0402\_1%-D
- CLK\_PCE\_ICH 1 R50 2 49.9\_0402\_1%-D
- CLK\_PCE\_ICH# 1 R51 2 49.9\_0402\_1%-D
- CLK\_MCH\_3GPLL 1 R40 2 49.9\_0402\_1%-D
- CLK\_MCH\_3GPLL# 1 R40 2 49.9\_0402\_1%-D
- CLK\_PCE\_VGA 1 R53 2 49.9\_0402\_1%-D
- CLK\_PCE\_VGA# 1 R53 2 49.9\_0402\_1%-D
- CLK\_PCE\_TV 1 R54 2 49.9\_0402\_1%-D
- CLK\_PCE\_TV# 1 R54 2 49.9\_0402\_1%-D



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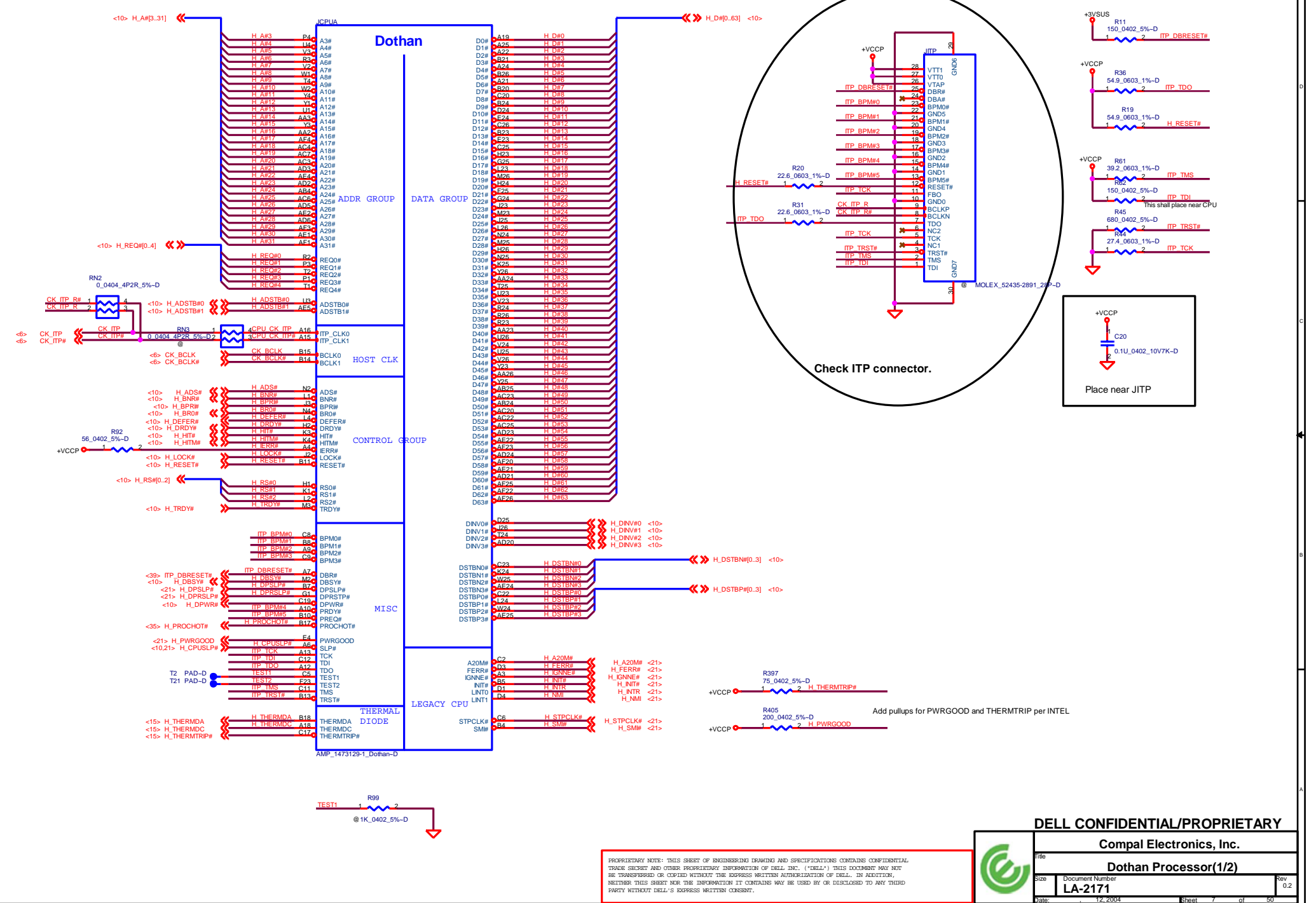


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**Clock Generator**

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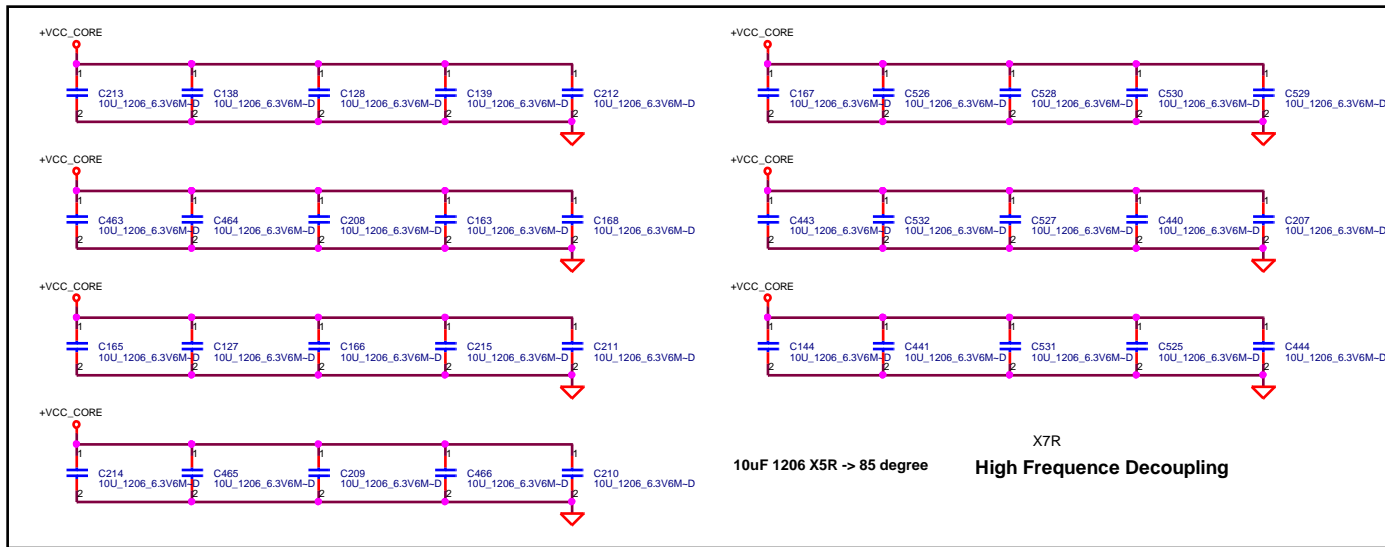
**Dothan Processor(1/2)**

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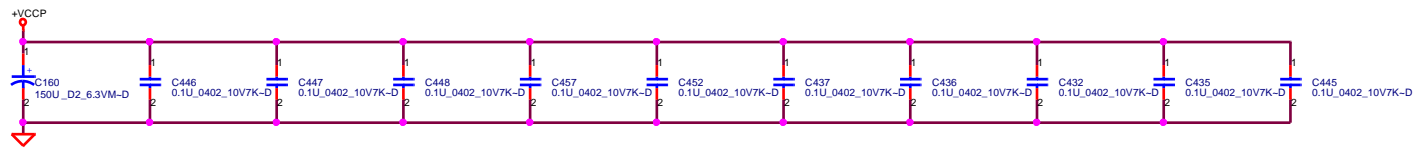
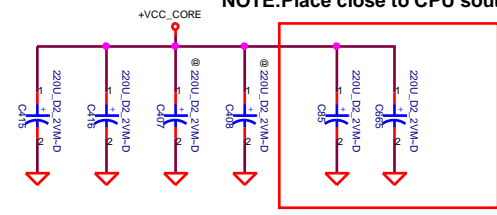






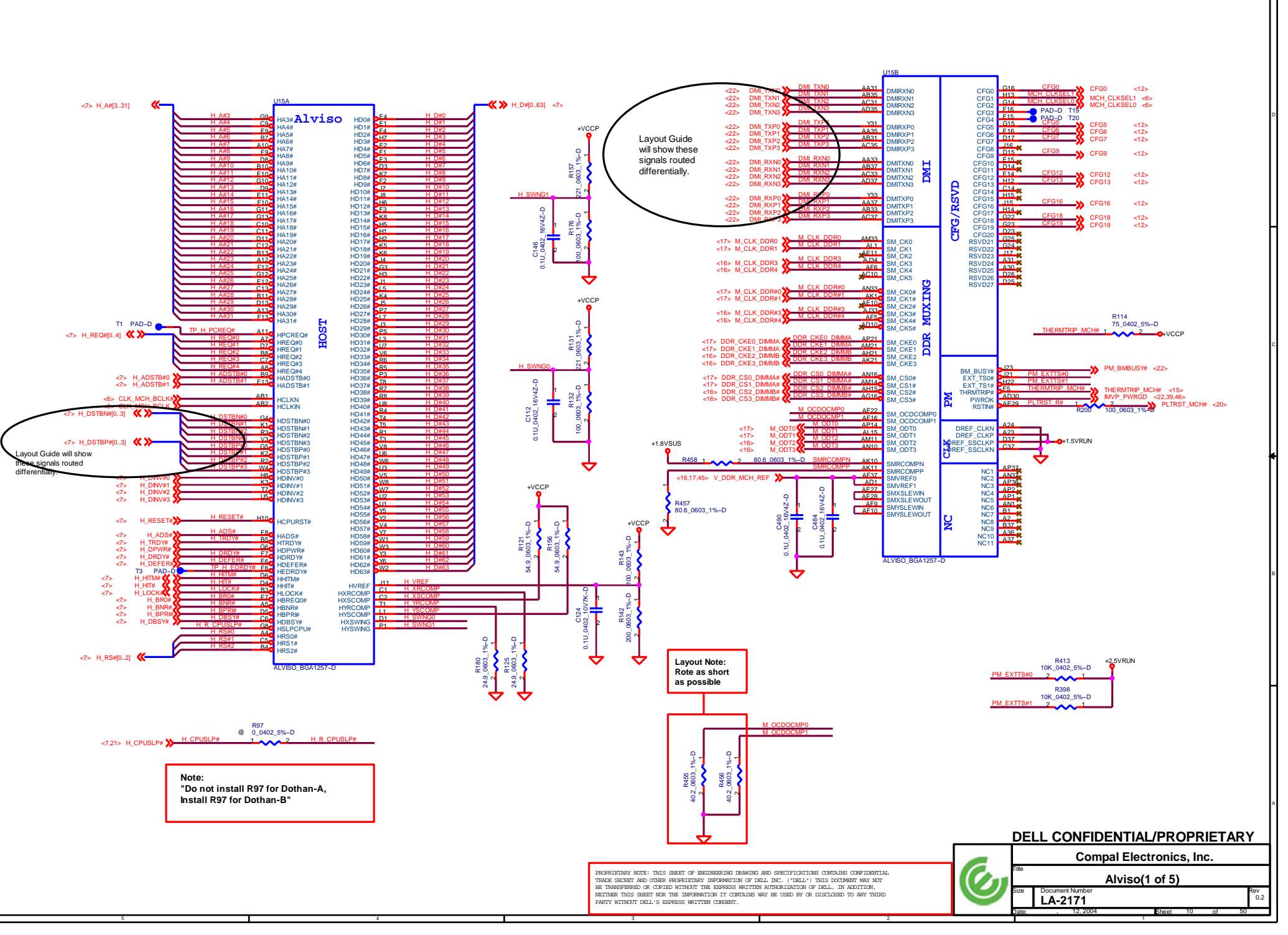
**Near VCORE regulator.**

**NOTE: Place close to CPU south side**



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 Title: **Dothan Bypass**  
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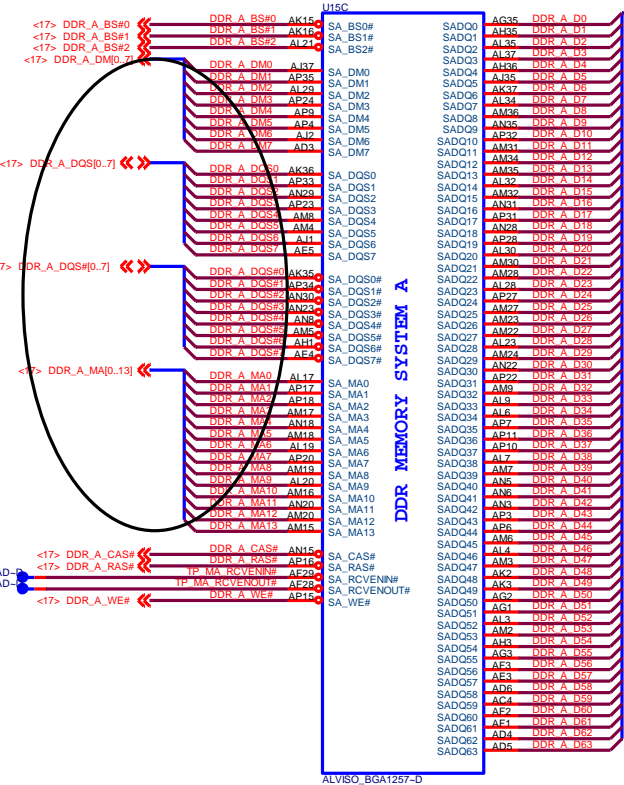
**Note:**  
 "Do not install R97 for Dothan-A,  
 Install R97 for Dothan-B"

**Layout Note:**  
 Rotate as short as possible

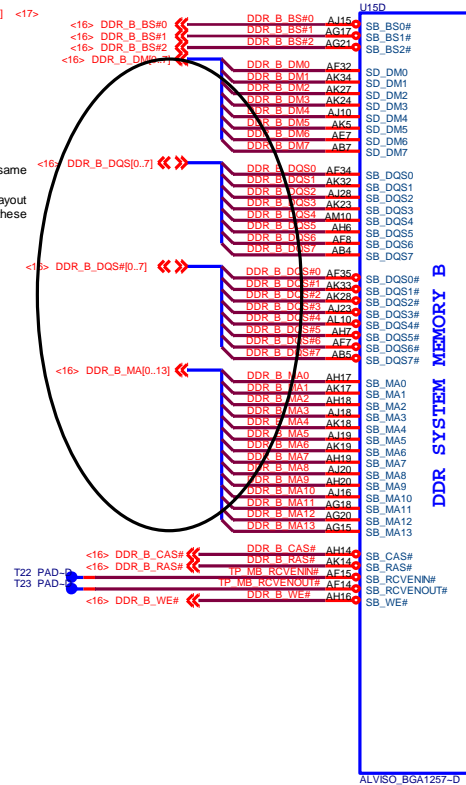
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 Alviso(1 of 5)  
 Document Number: LA-2171  
 Date: 12/2004

This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



ALVISO\_BGA1257-D

ALVISO\_BGA1257-D

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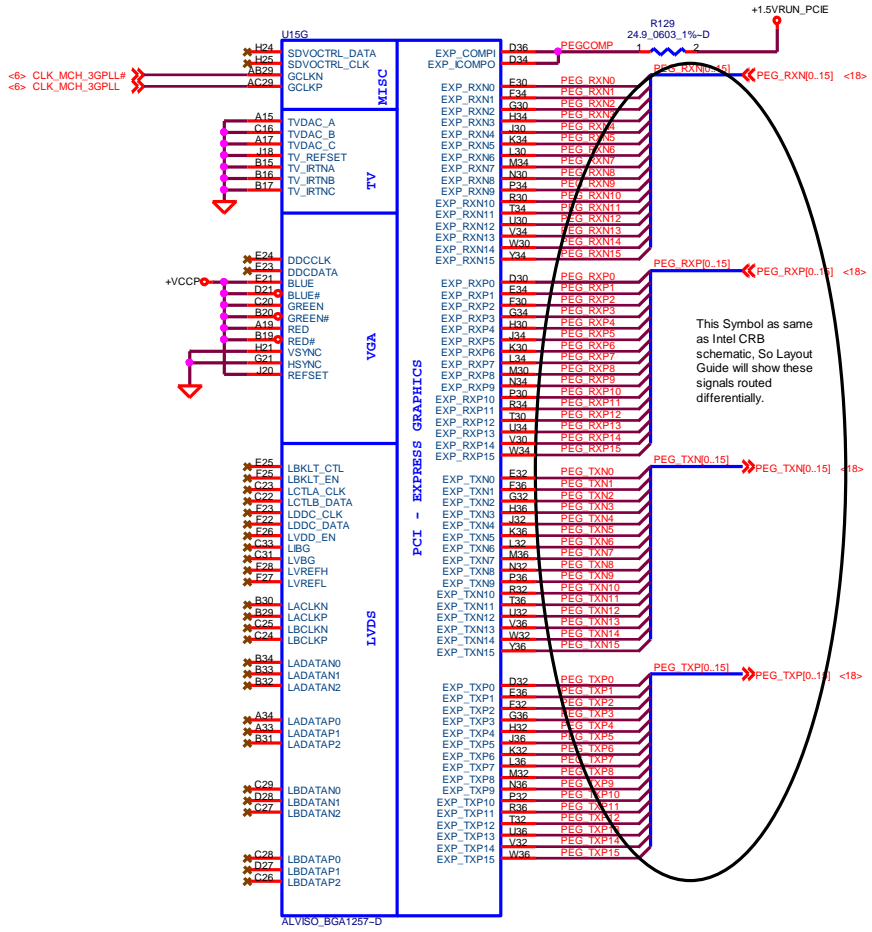
Alviso(2 of 5)



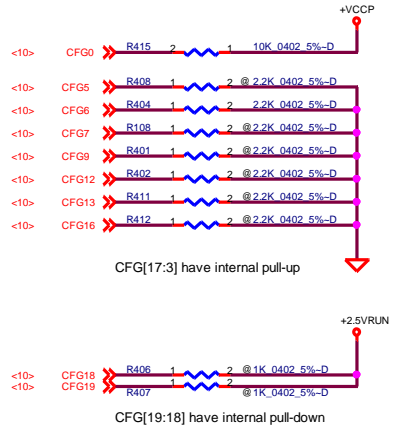
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CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XDR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



This Symbol is same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.

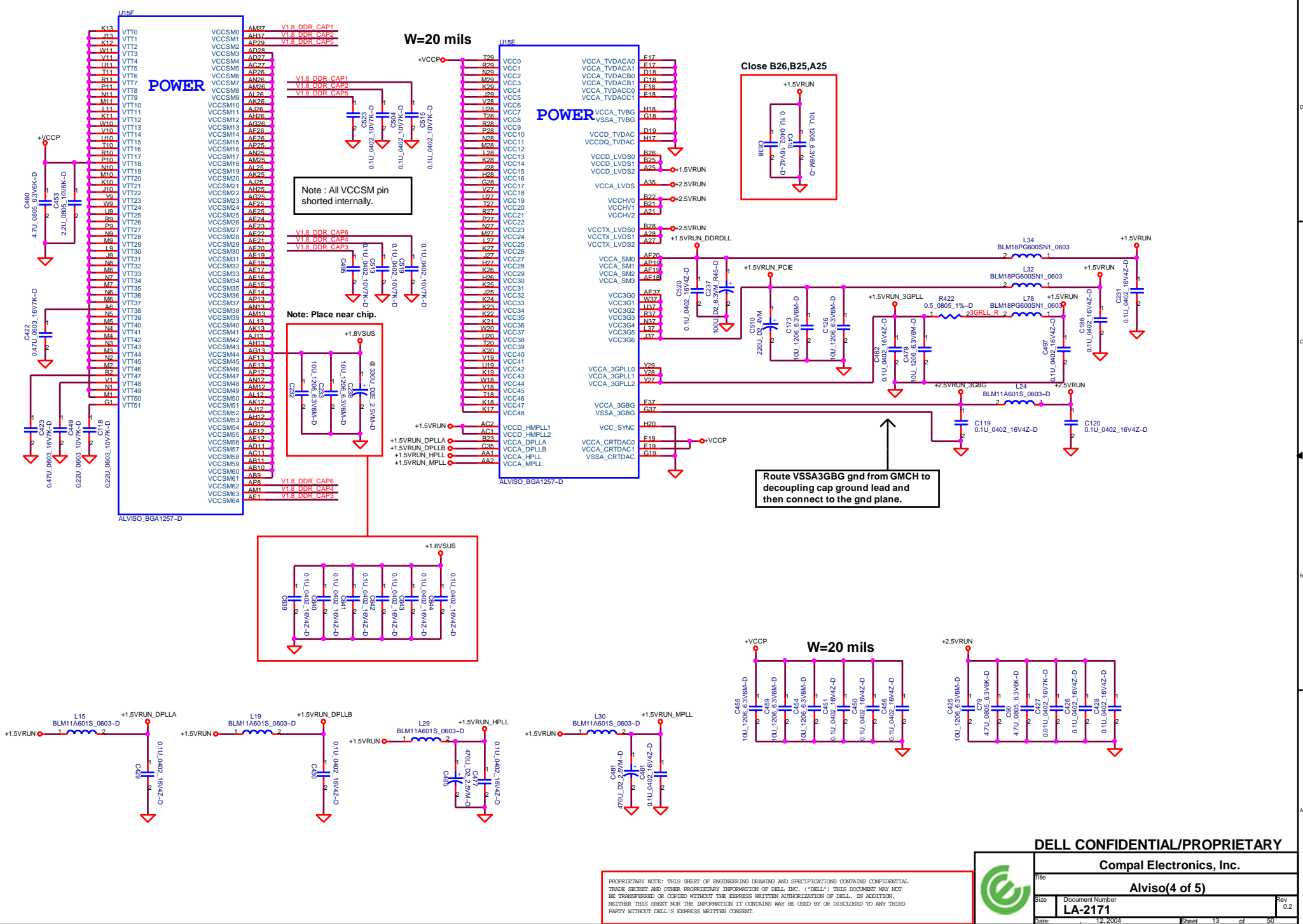
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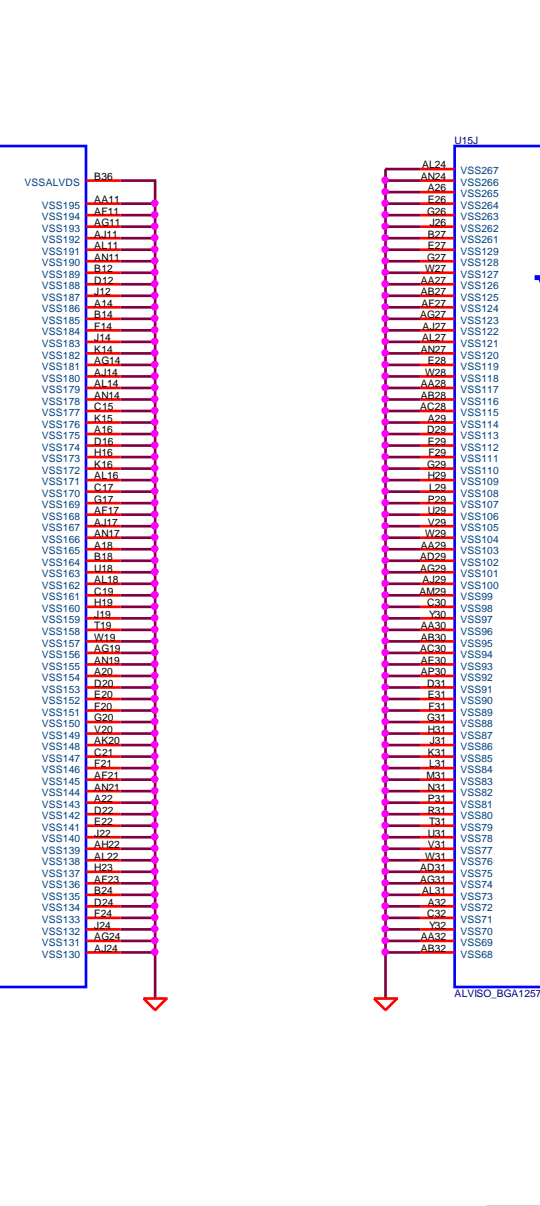
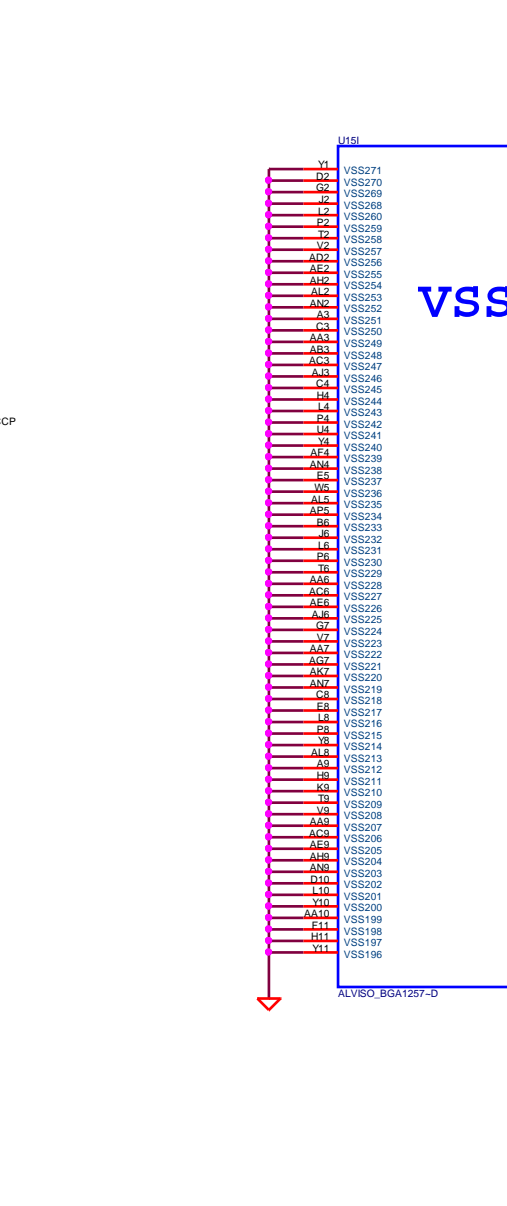
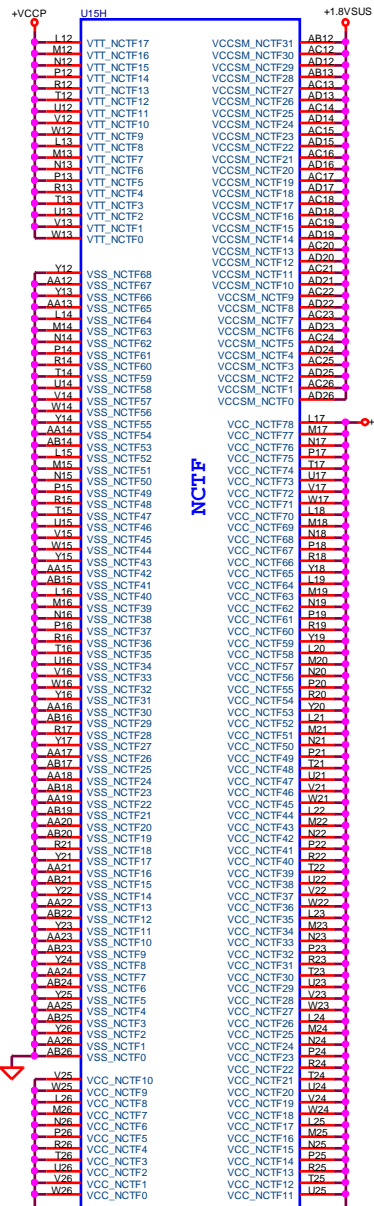
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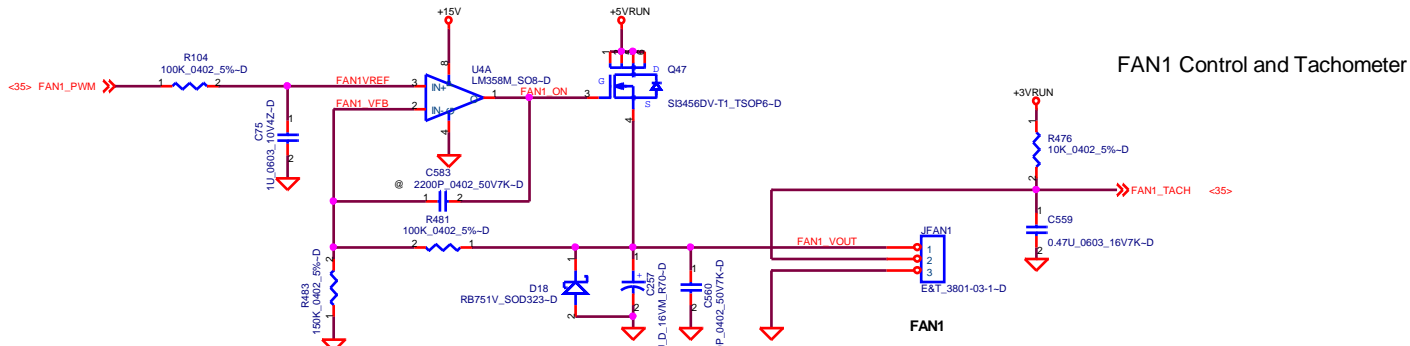
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Size: **LA-2171** Document Number

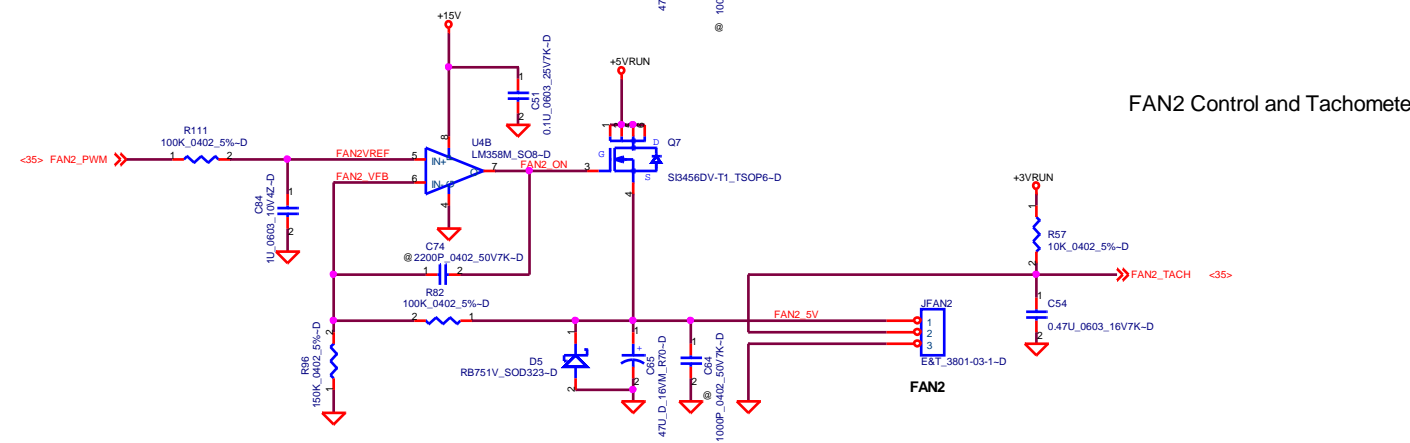
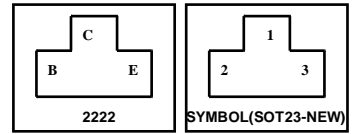
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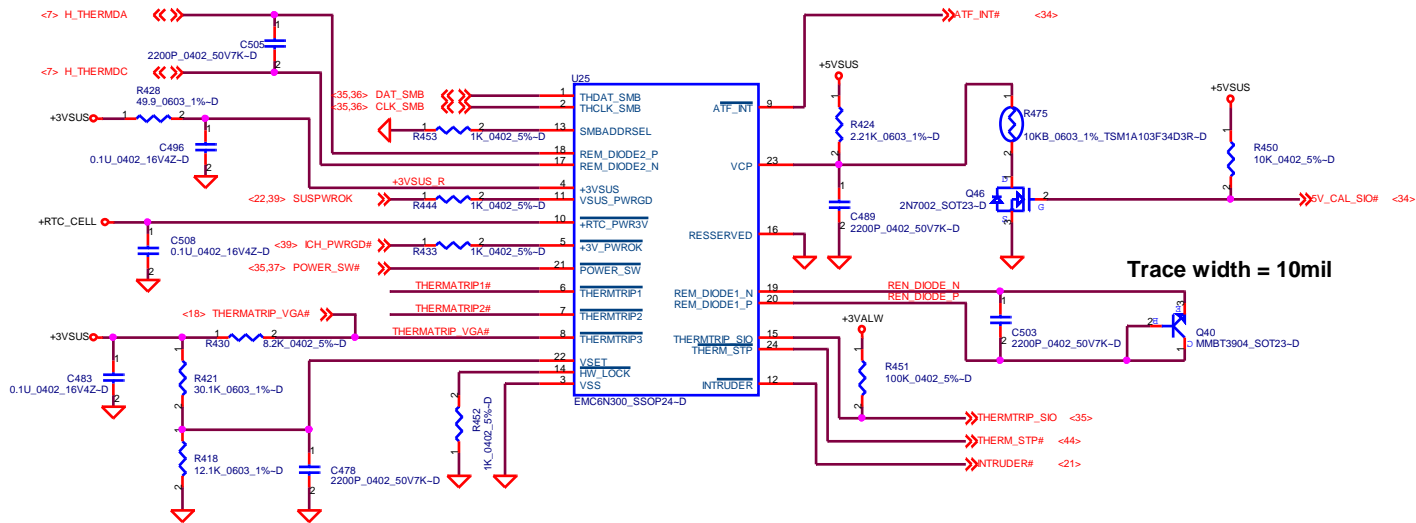
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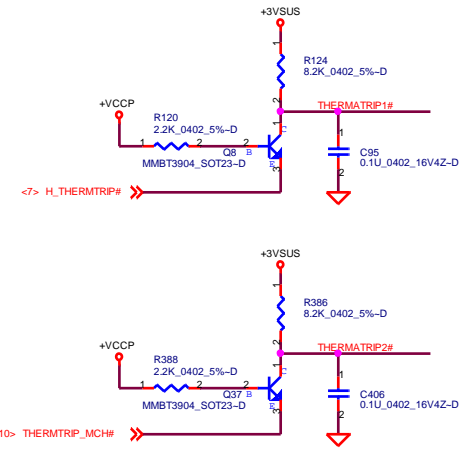
FAN1 Control and Tachometer




FAN2 Control and Tachometer



Trace width = 10mil



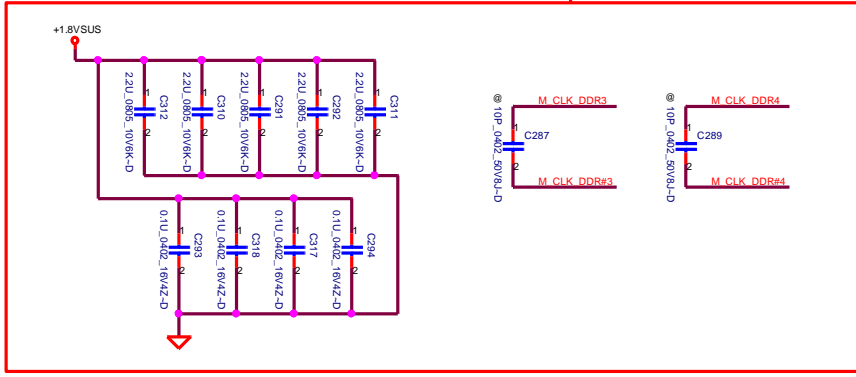
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		Compal Electronics, Inc.	
		Thermal sensor and Fan	
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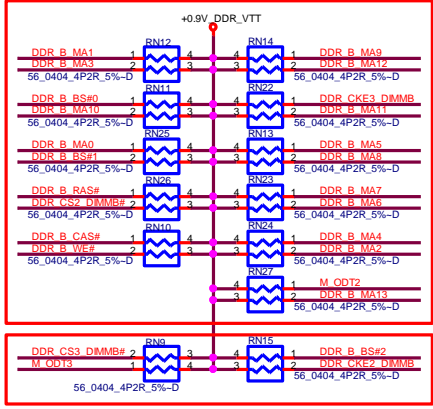
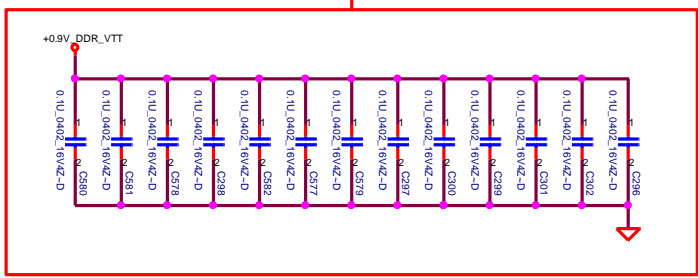
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<11> DDR\_B\_DQS[0..7] <<>>  
 <11> DDR\_B\_D[0..63] <<>>  
 <11> DDR\_B\_DM[0..7] <<>>  
 <11> DDR\_B\_DQS[0..7] <<>>  
 <11> DDR\_B\_MA[0..13] <<>>

**Layout Note:**  
Place near JDIM1

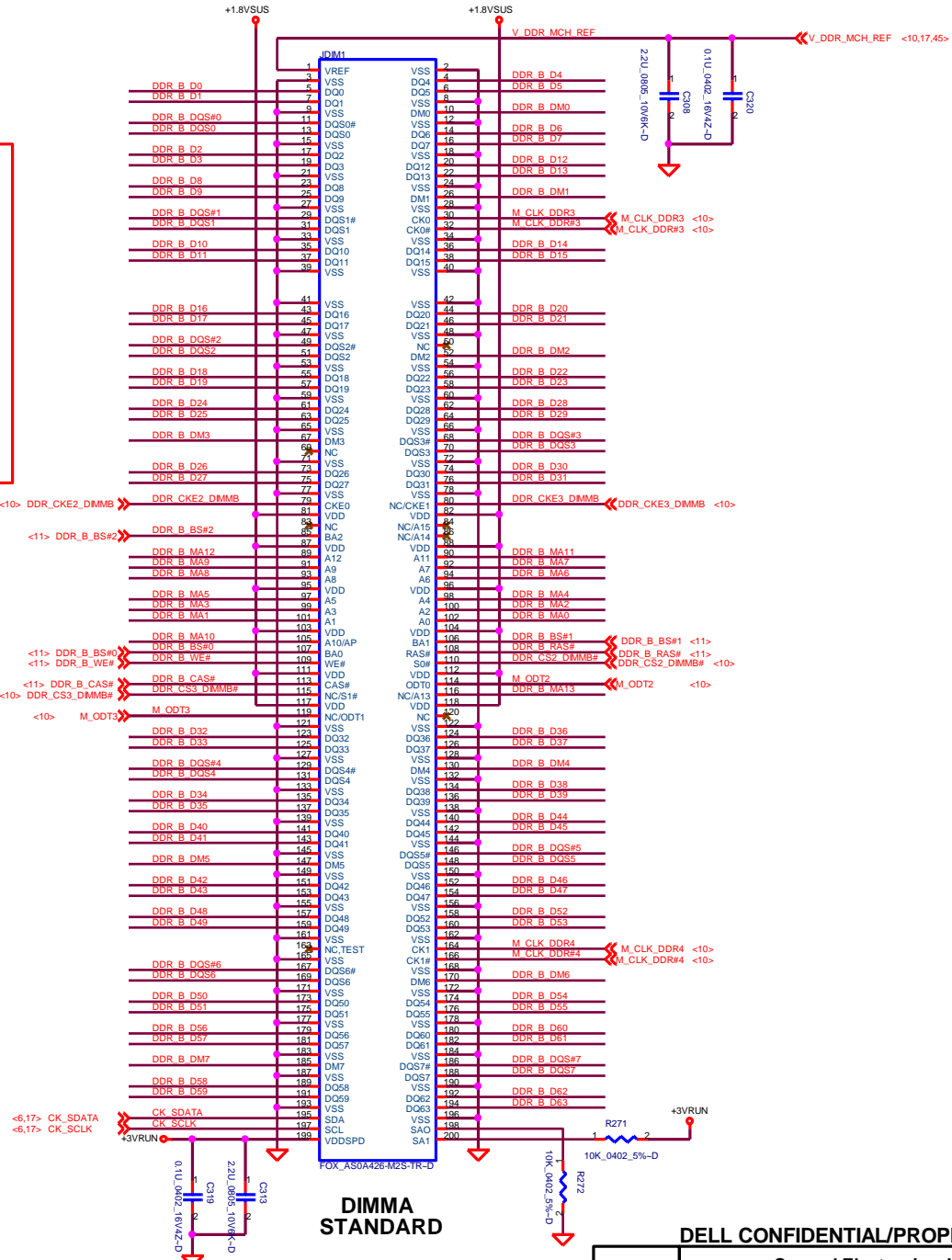


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



**Layout Note:**  
Place these resistor closely JDIM1, all trace length <750 mil

**Layout Note:**  
Place these resistor closely JDIM1, all trace length Max<1.3"



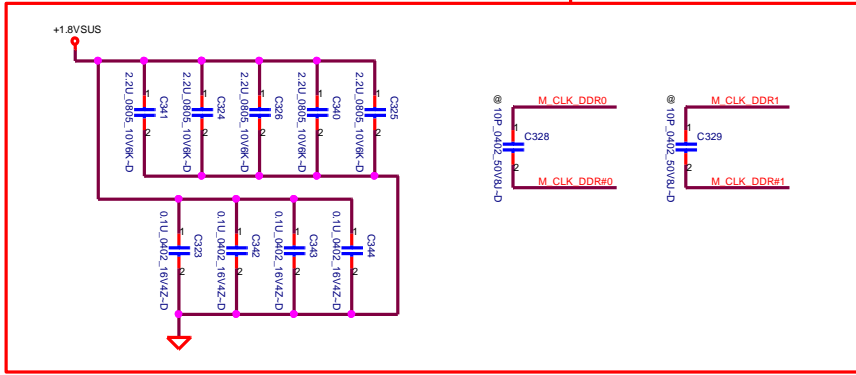
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 File  
**DDRII-SODIMM SLOT1**  
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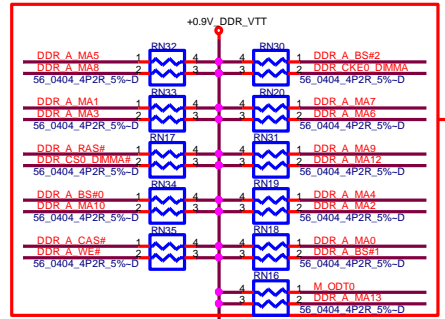
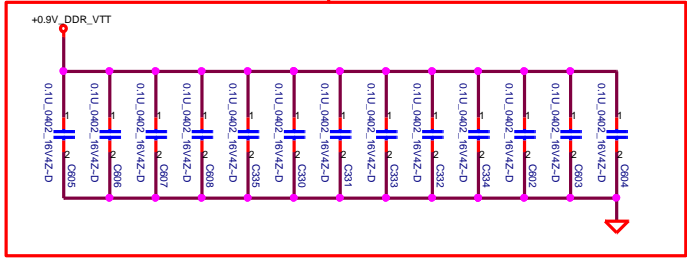


- <11> DDR\_A\_DQS#0[0..7]
- <11> DDR\_A\_D0[0..63]
- <11> DDR\_A\_DM0[0..7]
- <11> DDR\_A\_DQS[0..7]
- <11> DDR\_A\_MA[0..13]

**Layout Note:**  
Place near JDIM2

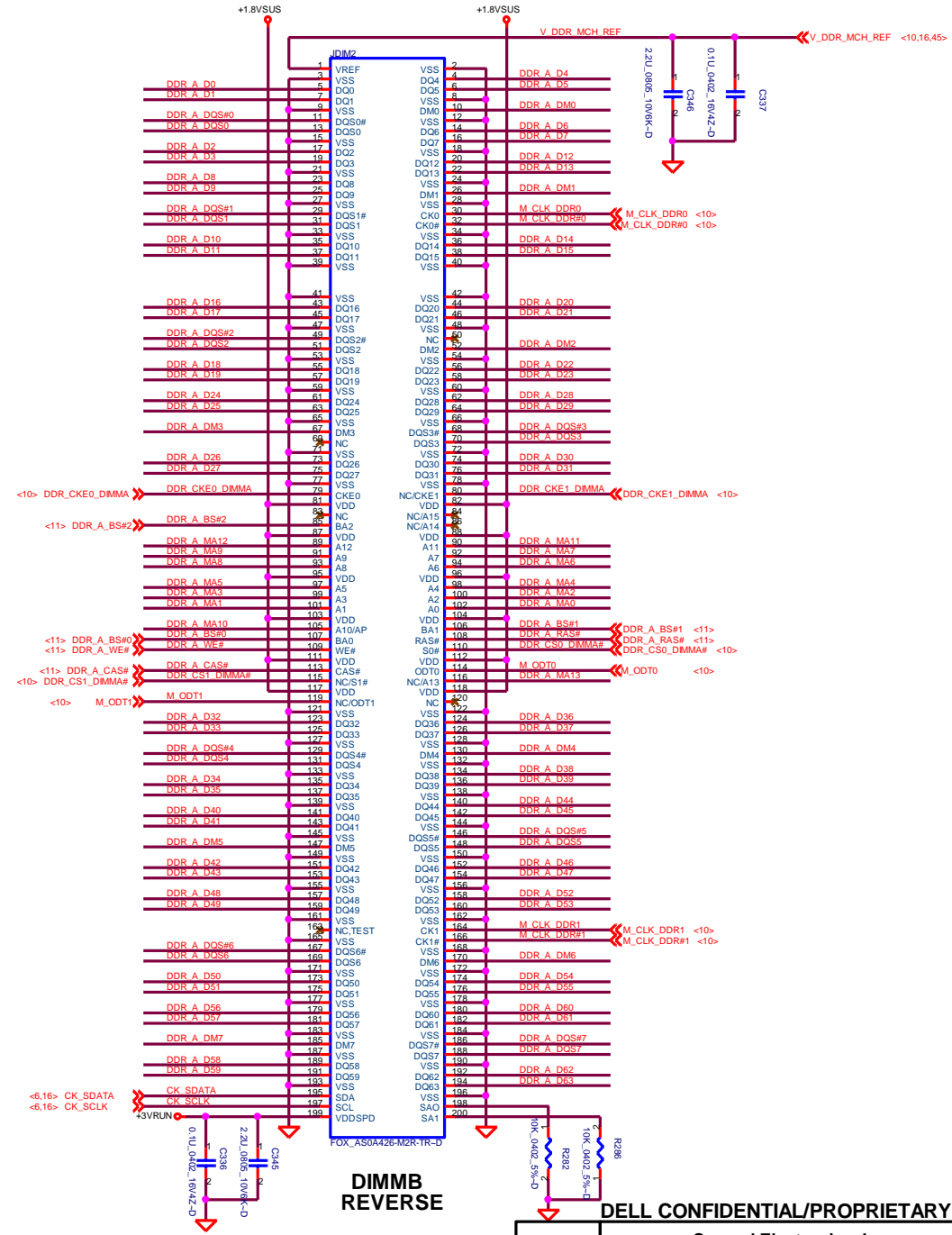


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



**Layout Note:**  
Place this resistor closely JDIM2, all trace length <750 mil

**Layout Note:**  
Place these resistor closely JDIM2, all trace length Max=1.3"



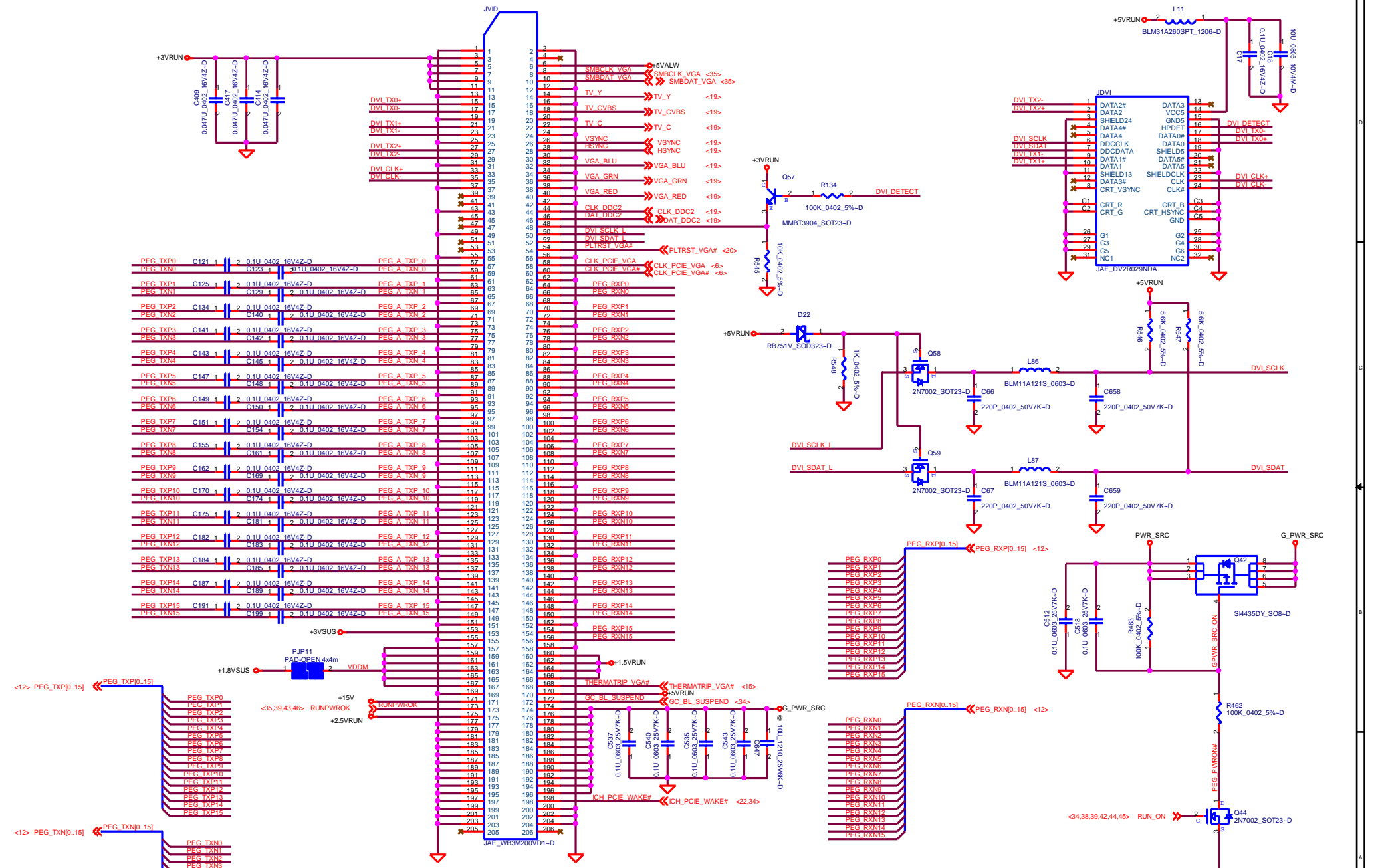
**DIMM REVERSE**

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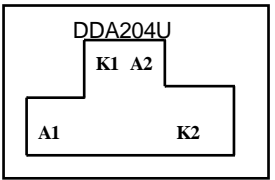
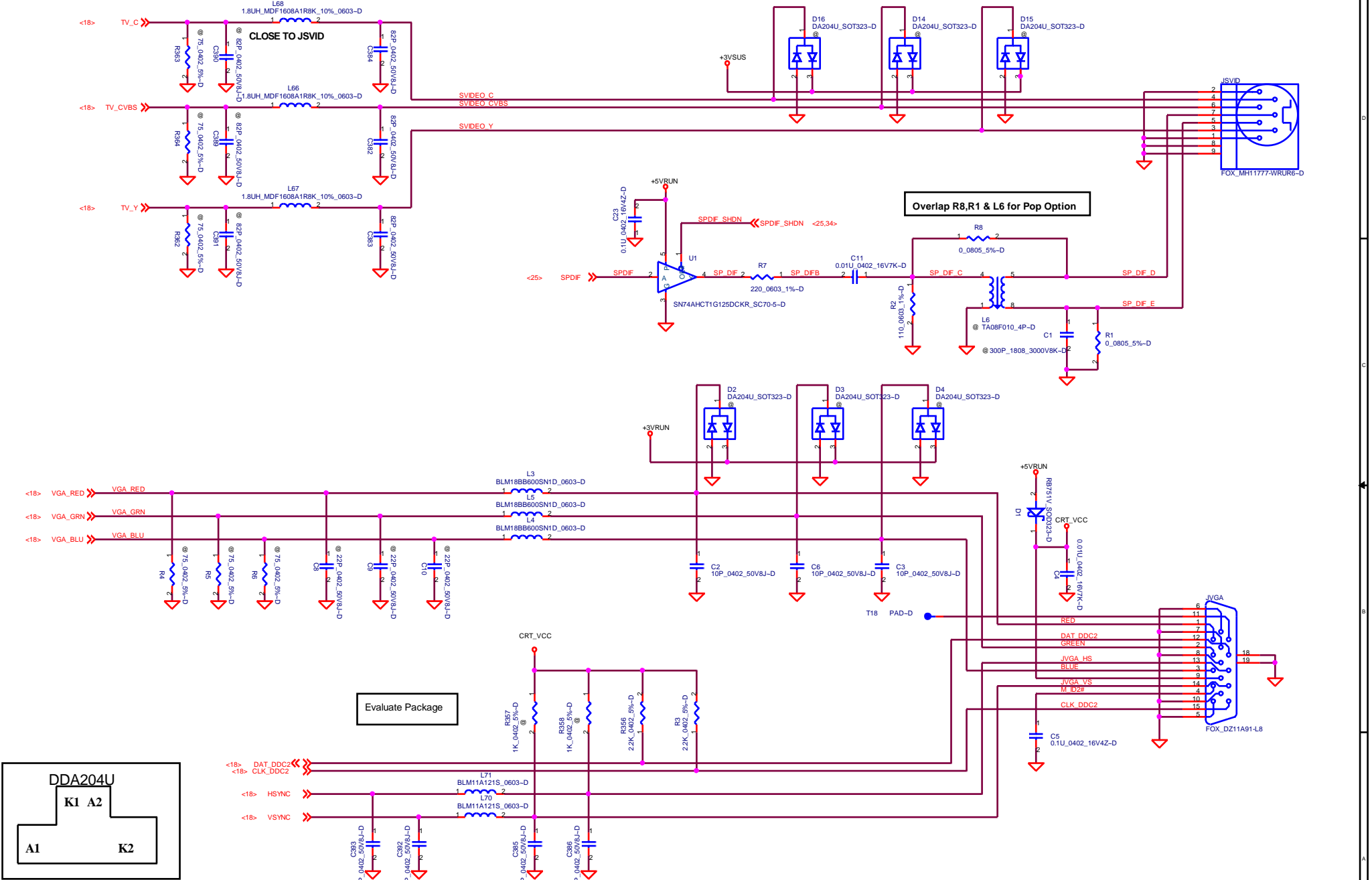
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		<b>VGA and DVI connector</b>	
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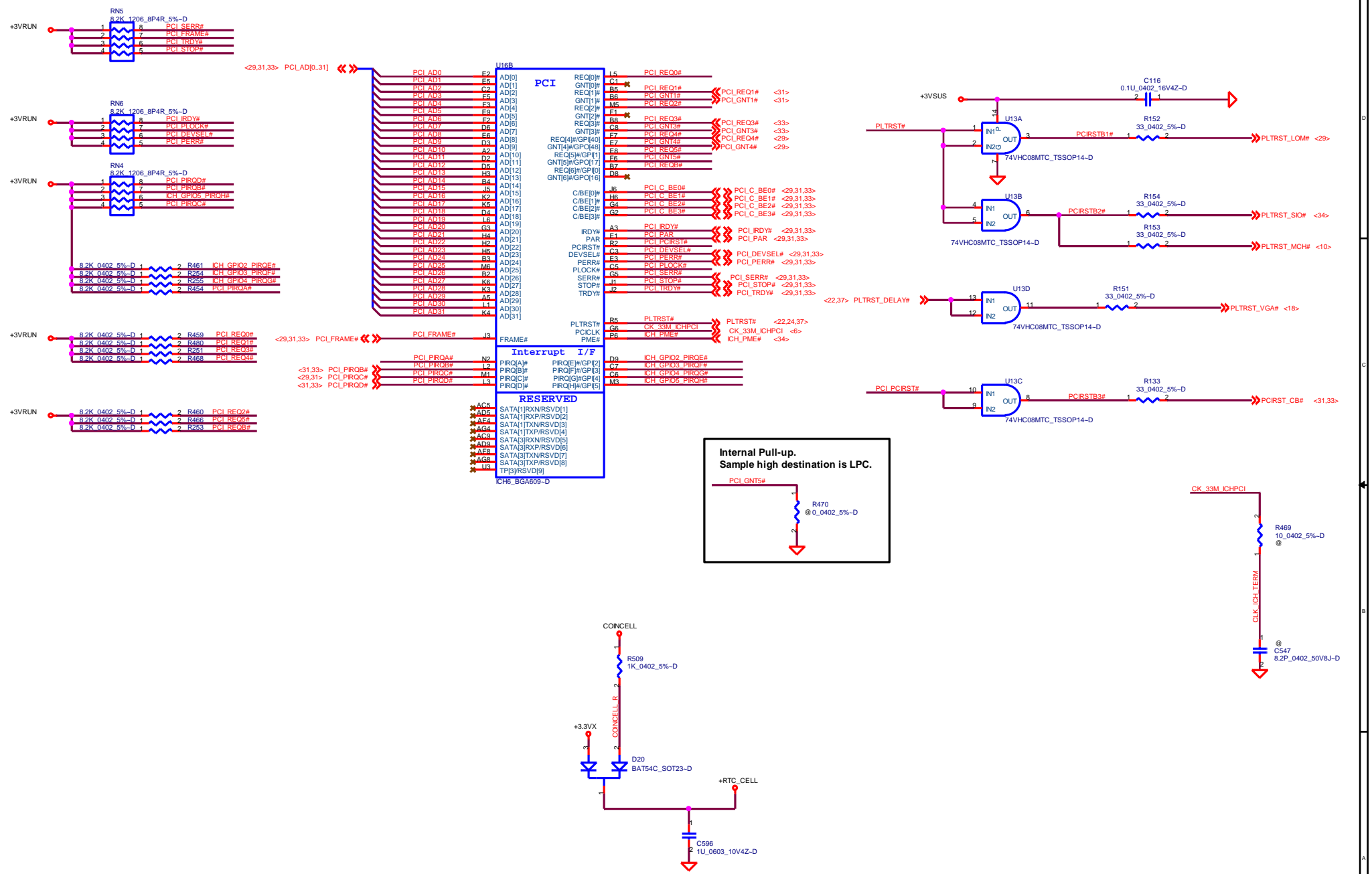


Evaluate Package

Overlap R8,R1 & L6 for Pop Option

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**TV\_OUT and CRT connector**  
 Size Document Number  
**LA-2171**  
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**Internal Pull-up.**  
Sample high destination is LPC.

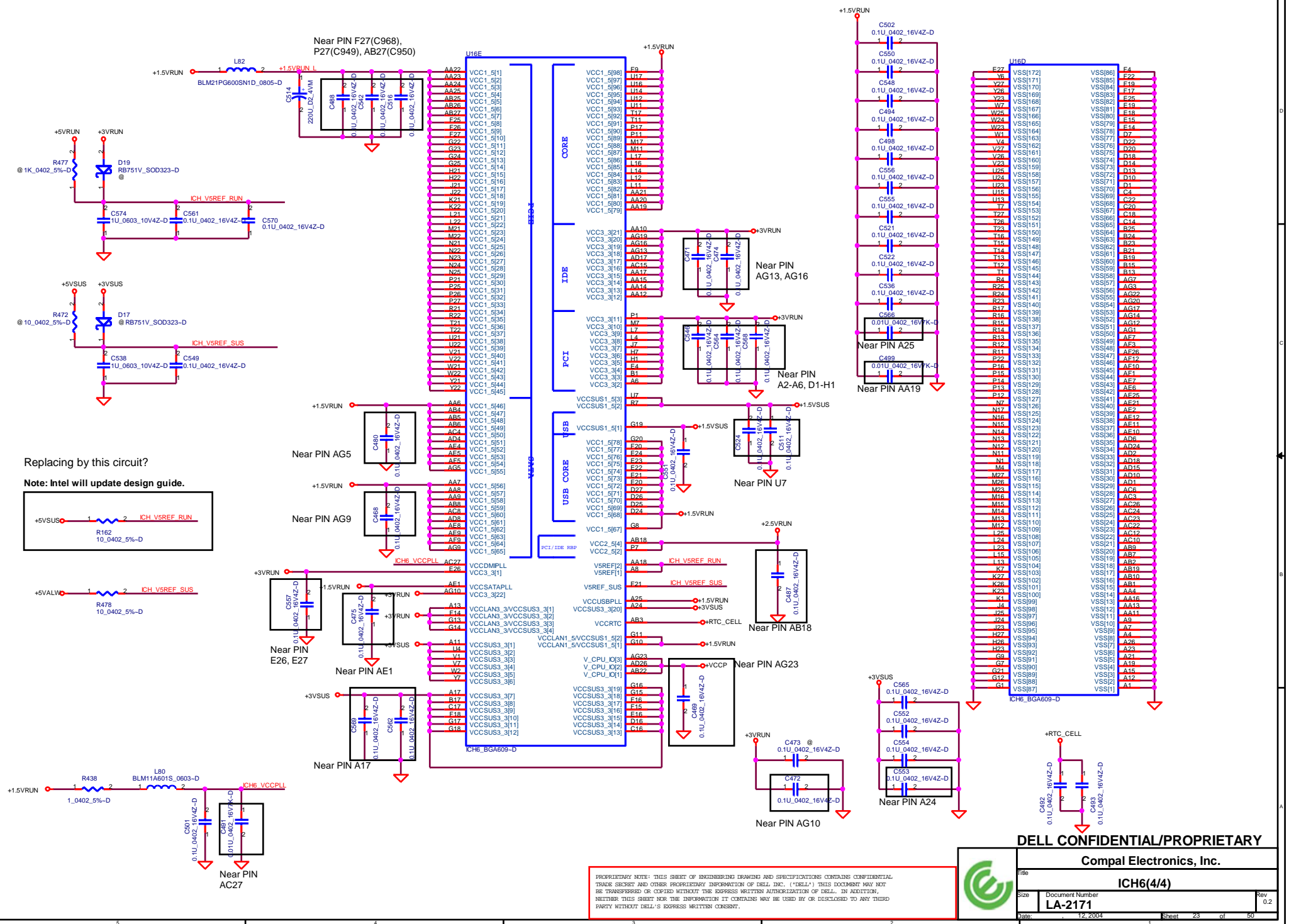
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Part: ICH6(1/4)  
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 Date: 12, 2004  
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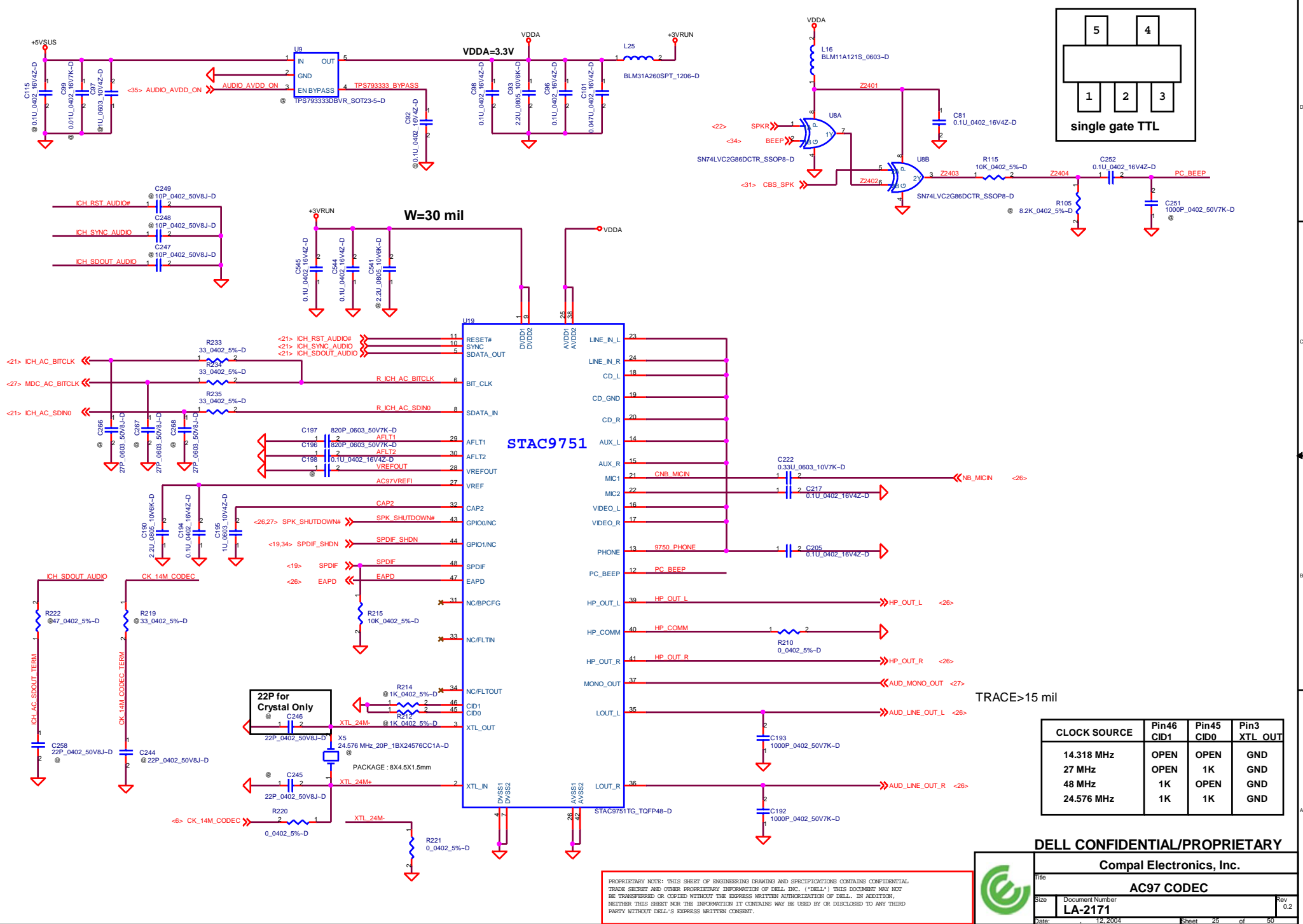












CLOCK SOURCE	Pin46 CID1	Pin45 CID0	Pin3 XTL_OUT
14.318 MHz	OPEN	OPEN	GND
27 MHz	OPEN	1K	GND
48 MHz	1K	OPEN	GND
24.576 MHz	1K	1K	GND

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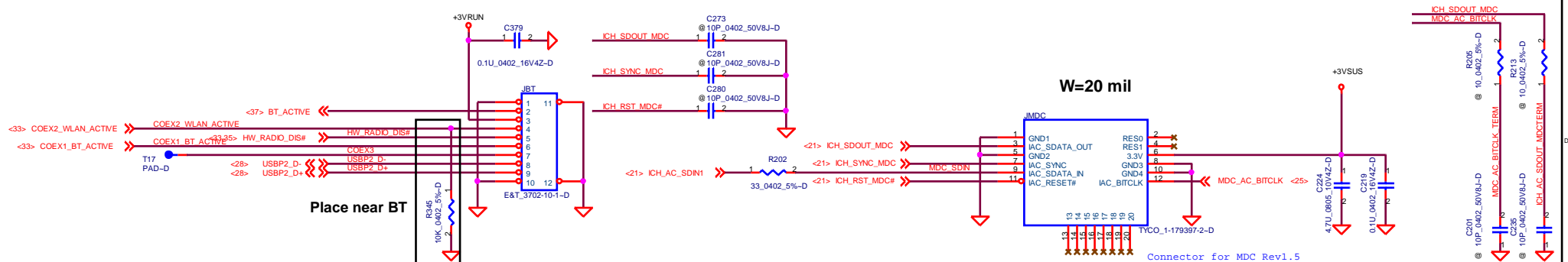
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Size: **LA-2171** Rev: 0.2

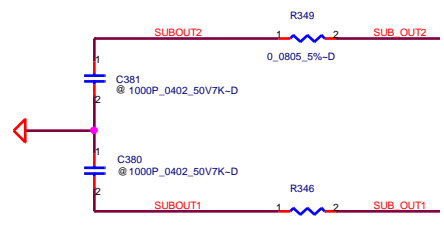
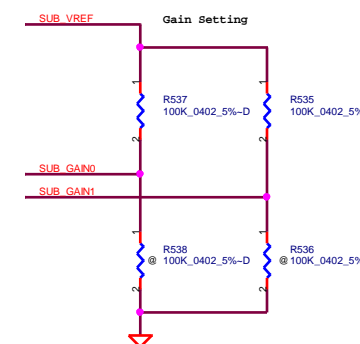
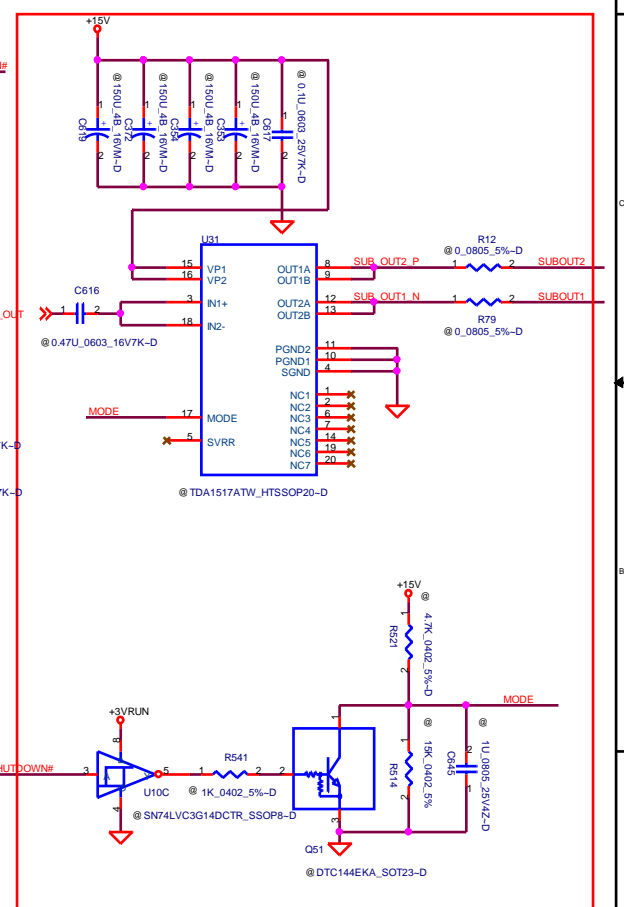
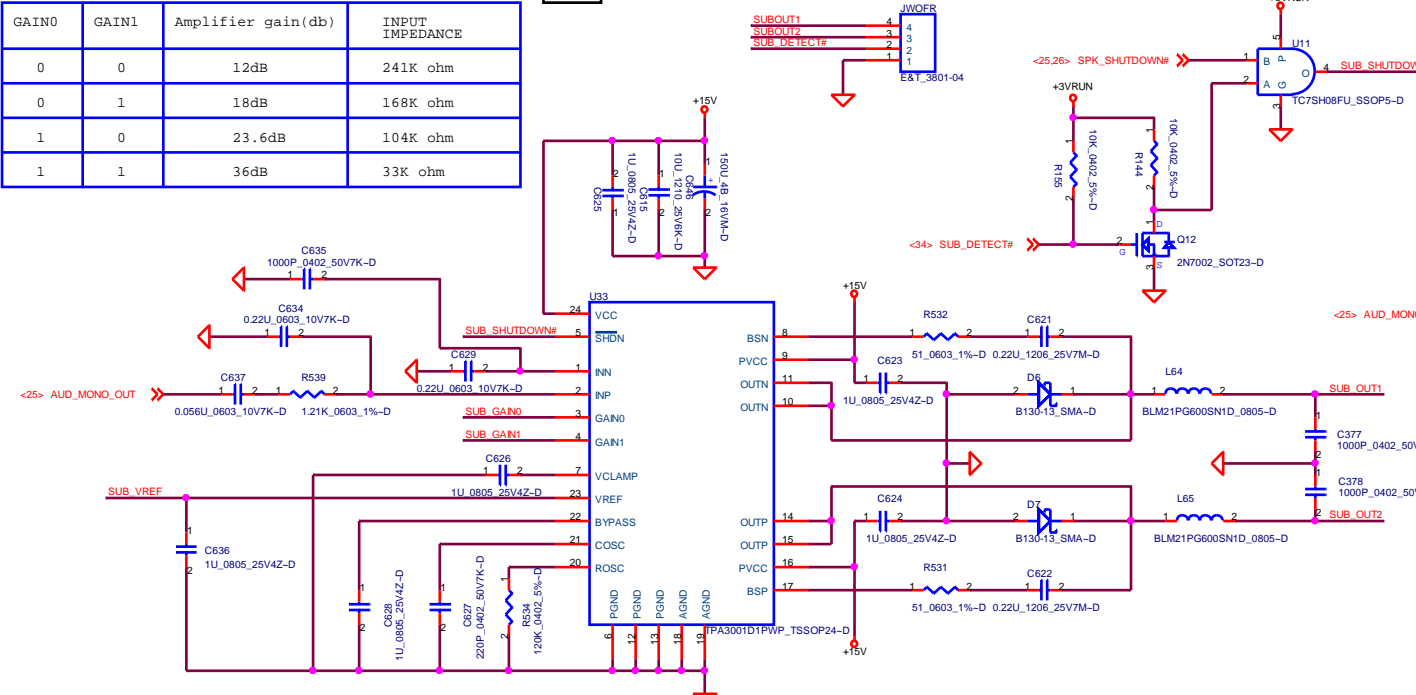
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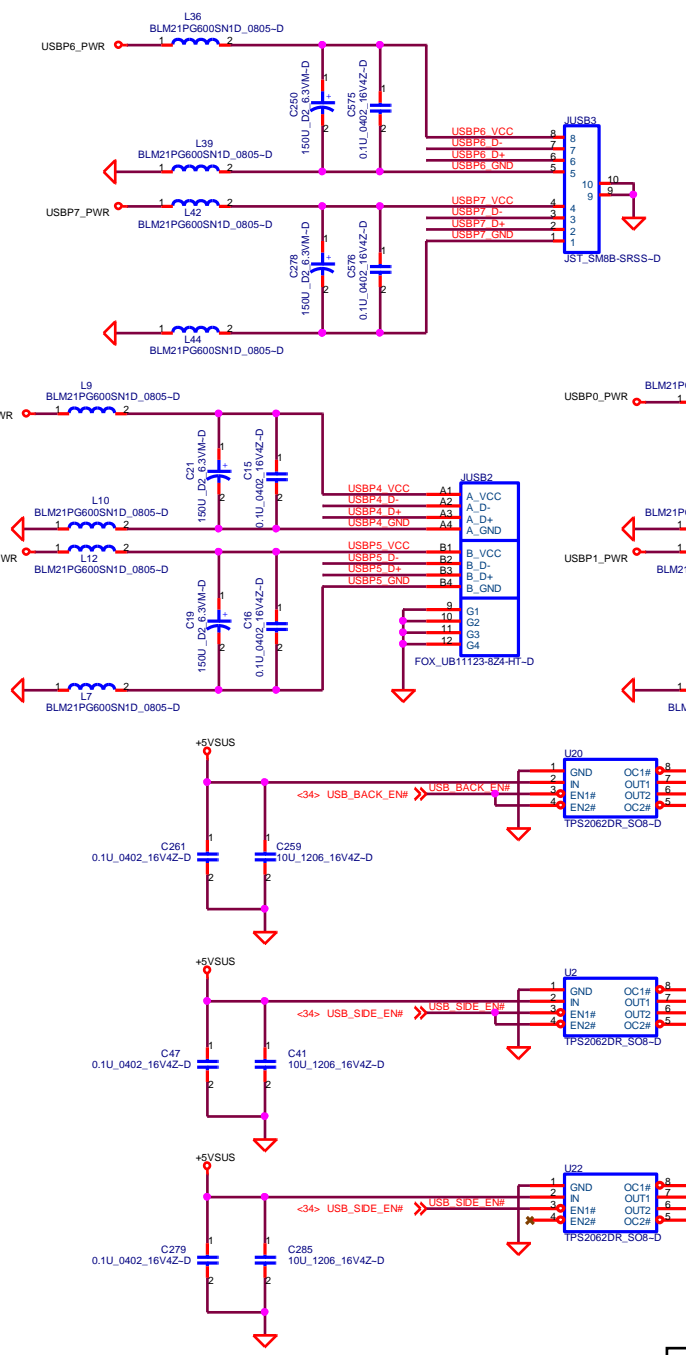
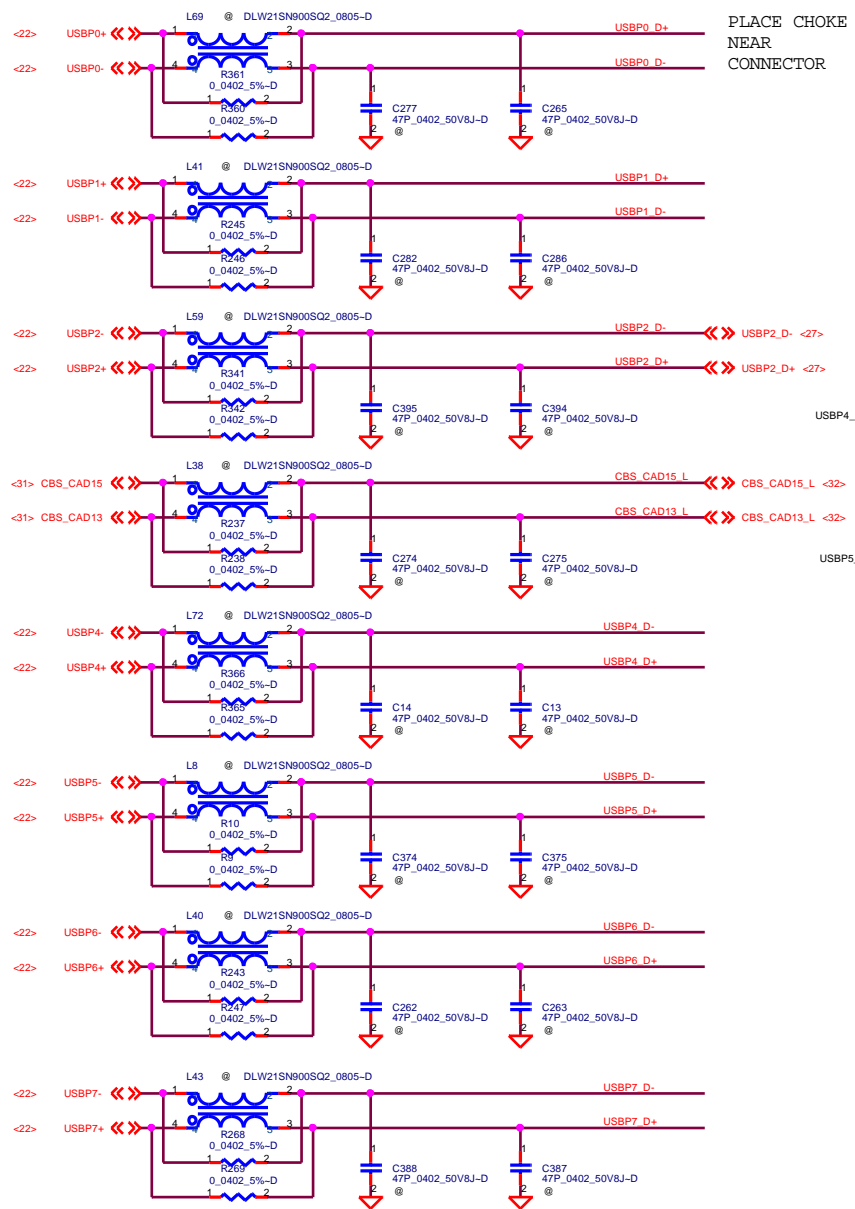


GAIN0	GAIN1	Amplifier gain(db)	INPUT IMPEDANCE
0	0	12dB	241K ohm
0	1	18dB	168K ohm
1	0	23.6dB	104K ohm
1	1	36dB	33K ohm

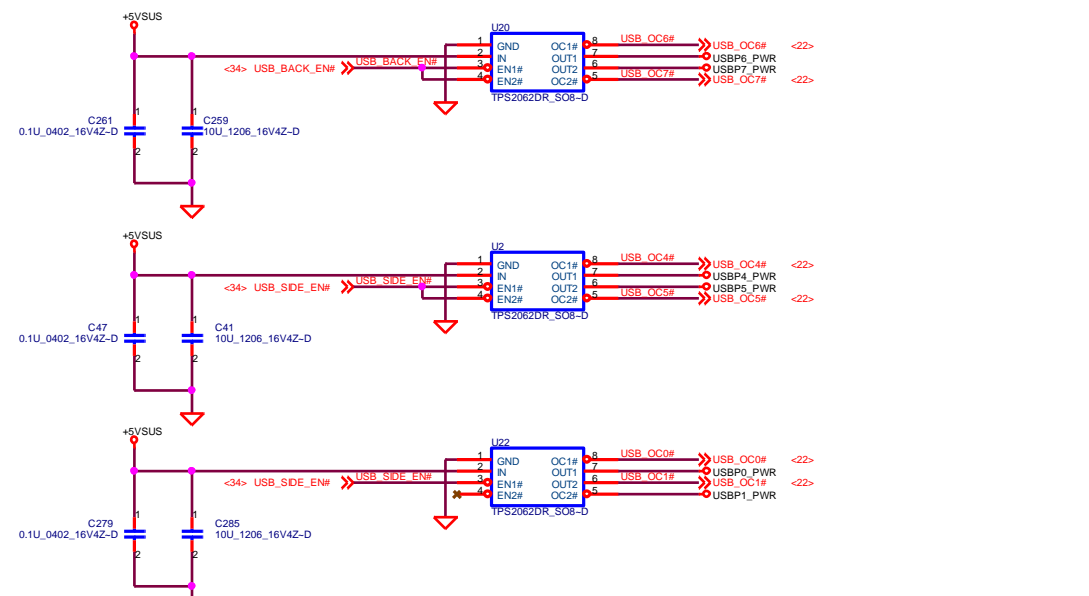
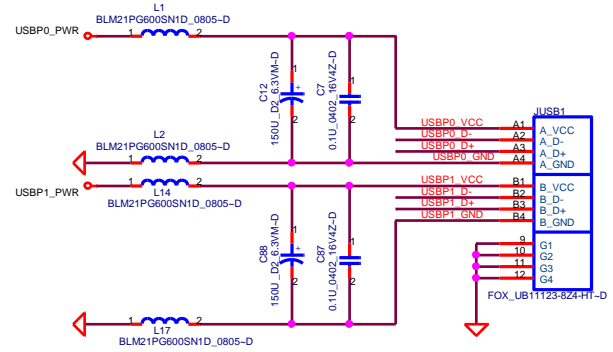


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**SUBWOOFER,BT PORT and MDC**  
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USB PORT#	DESTINATION
0	JUSB1 (Top)
1	JUSB1 (Bottom)
2	BlueTooth
3	NEW CARD
4	JUSB2 (Top)
5	JUSB2 (Bottom)
6	JUSB3 (Top)
7	JUSB3 (Bottom)

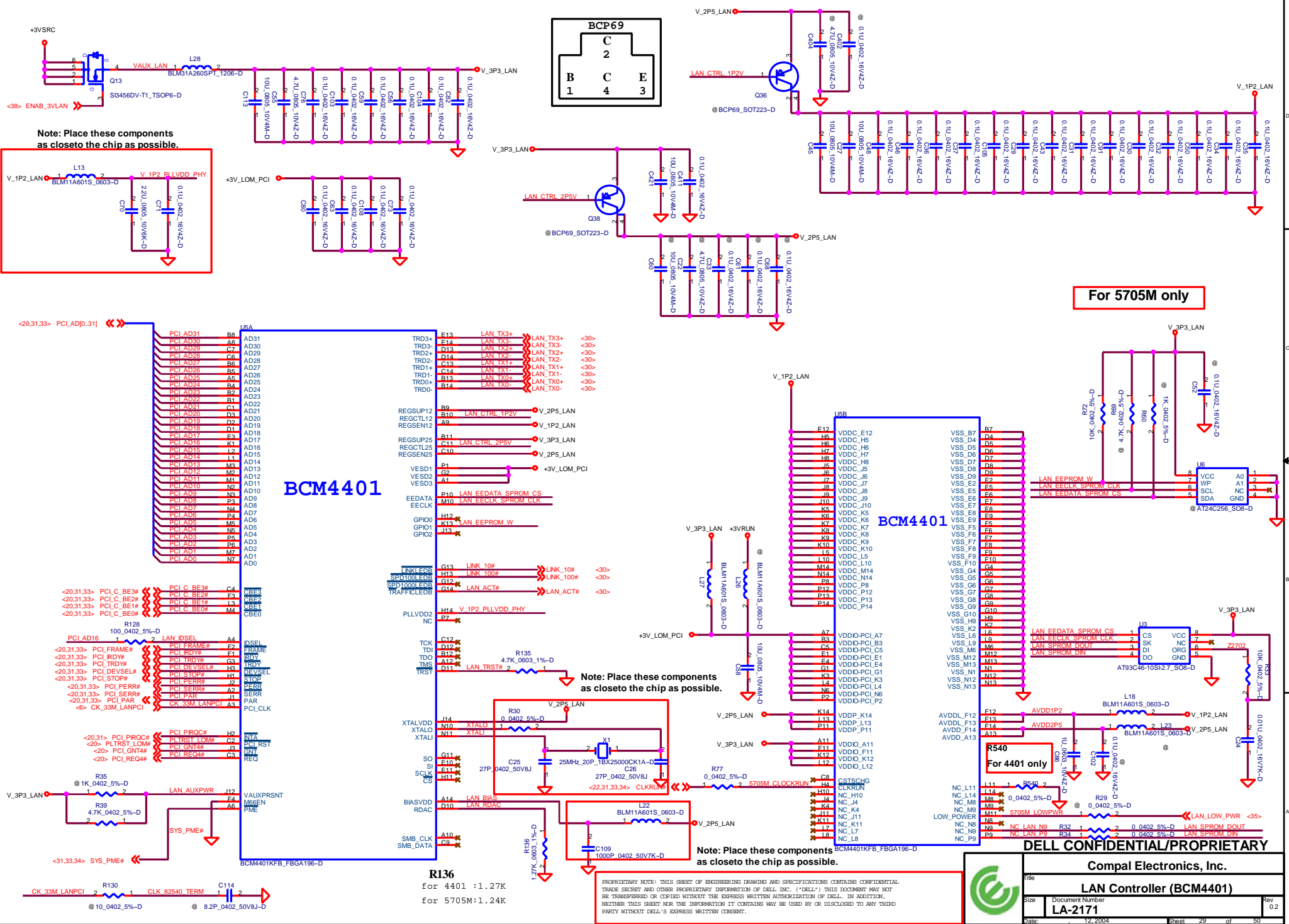


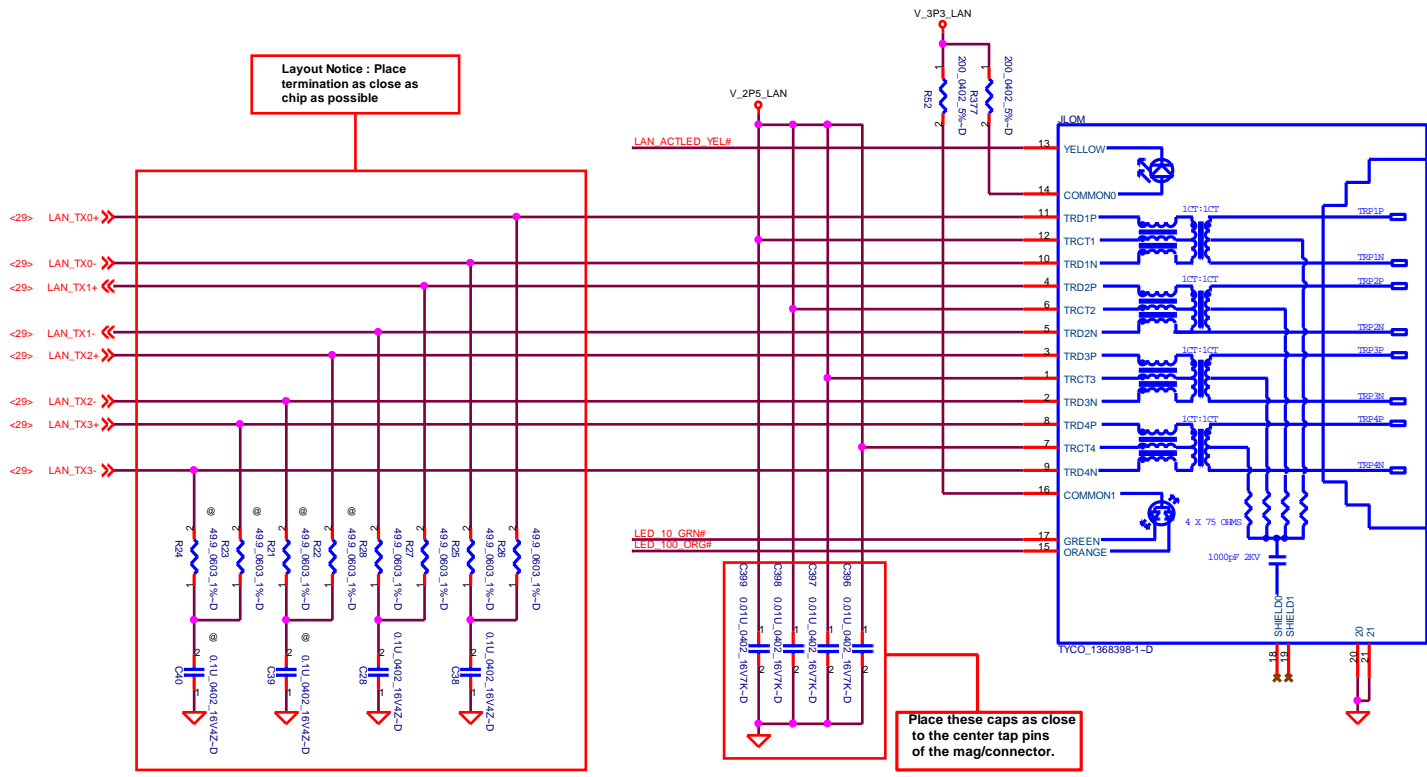
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Compal Electronics, Inc.	
<b>USB 2.0 PORT</b>	
Size	Document Number
	<b>LA-2171</b>
Date	Rev
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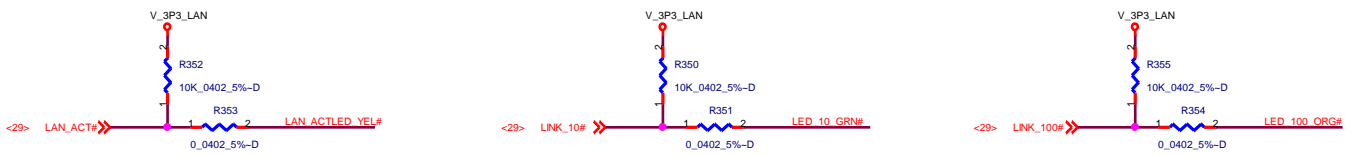
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Layout Notice : Place termination as close as chip as possible

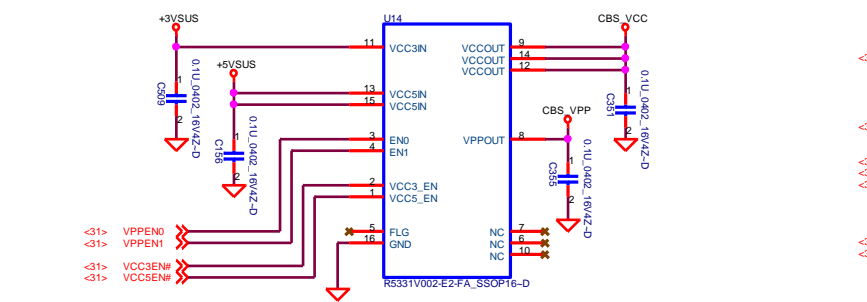
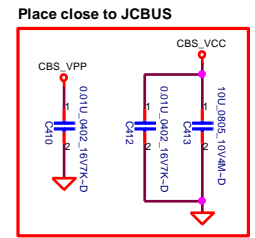
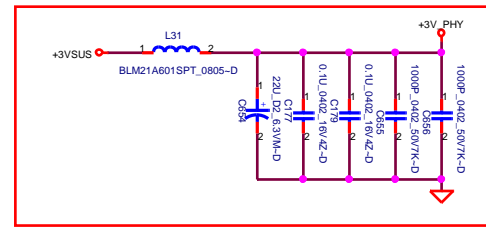
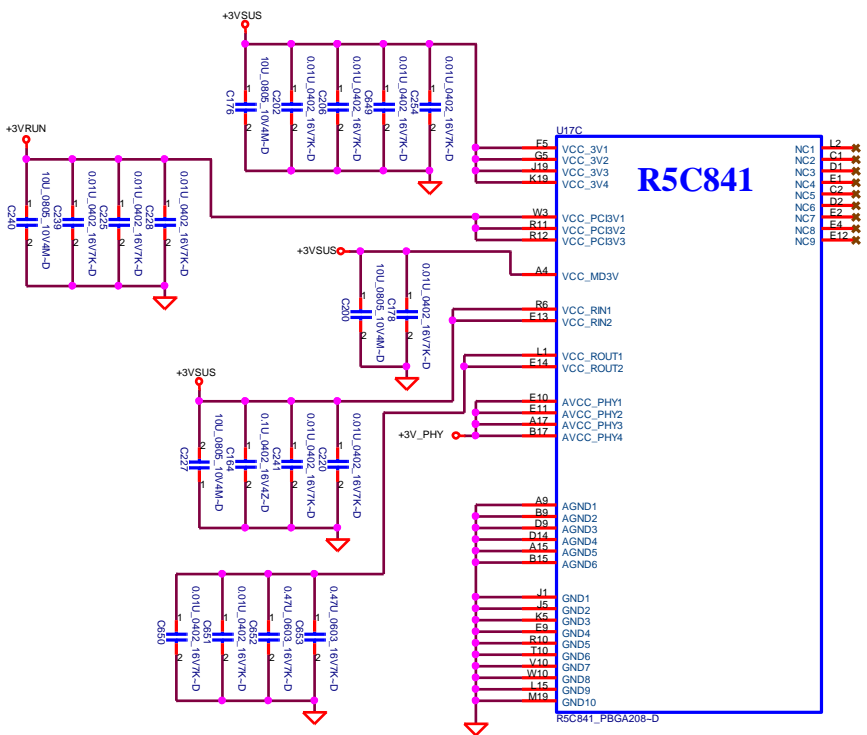
Place these caps as close to the center tap pins of the mag/connectors.



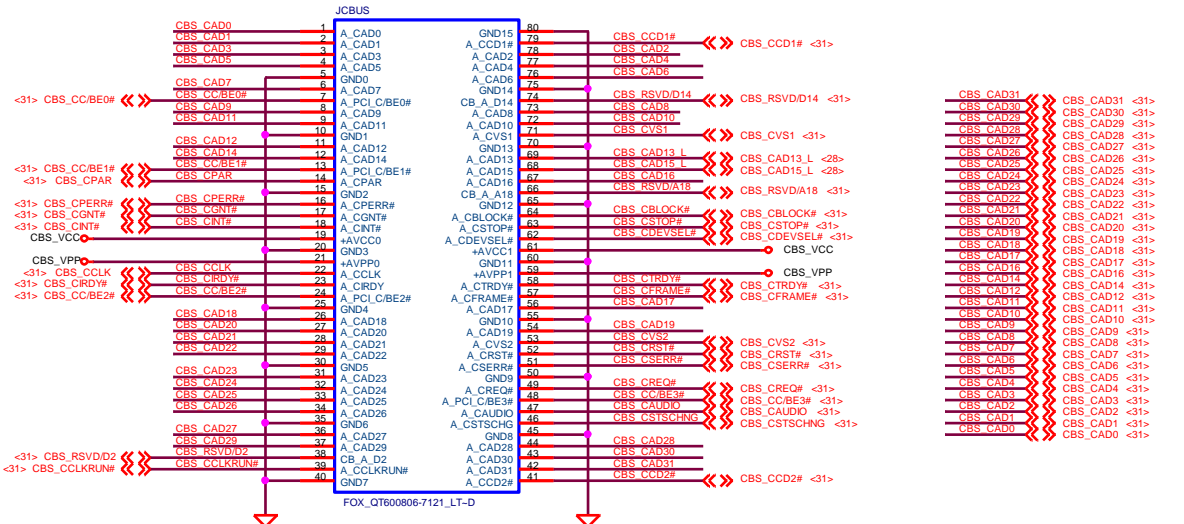
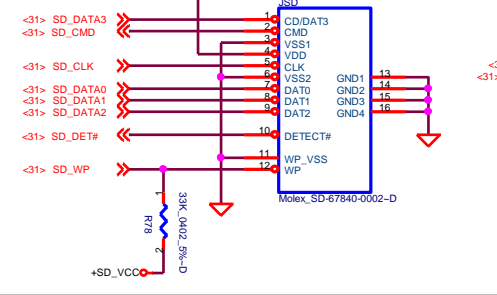
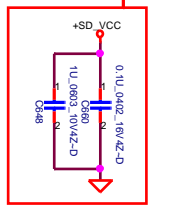
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**LAN Transfomer and RJ45**  
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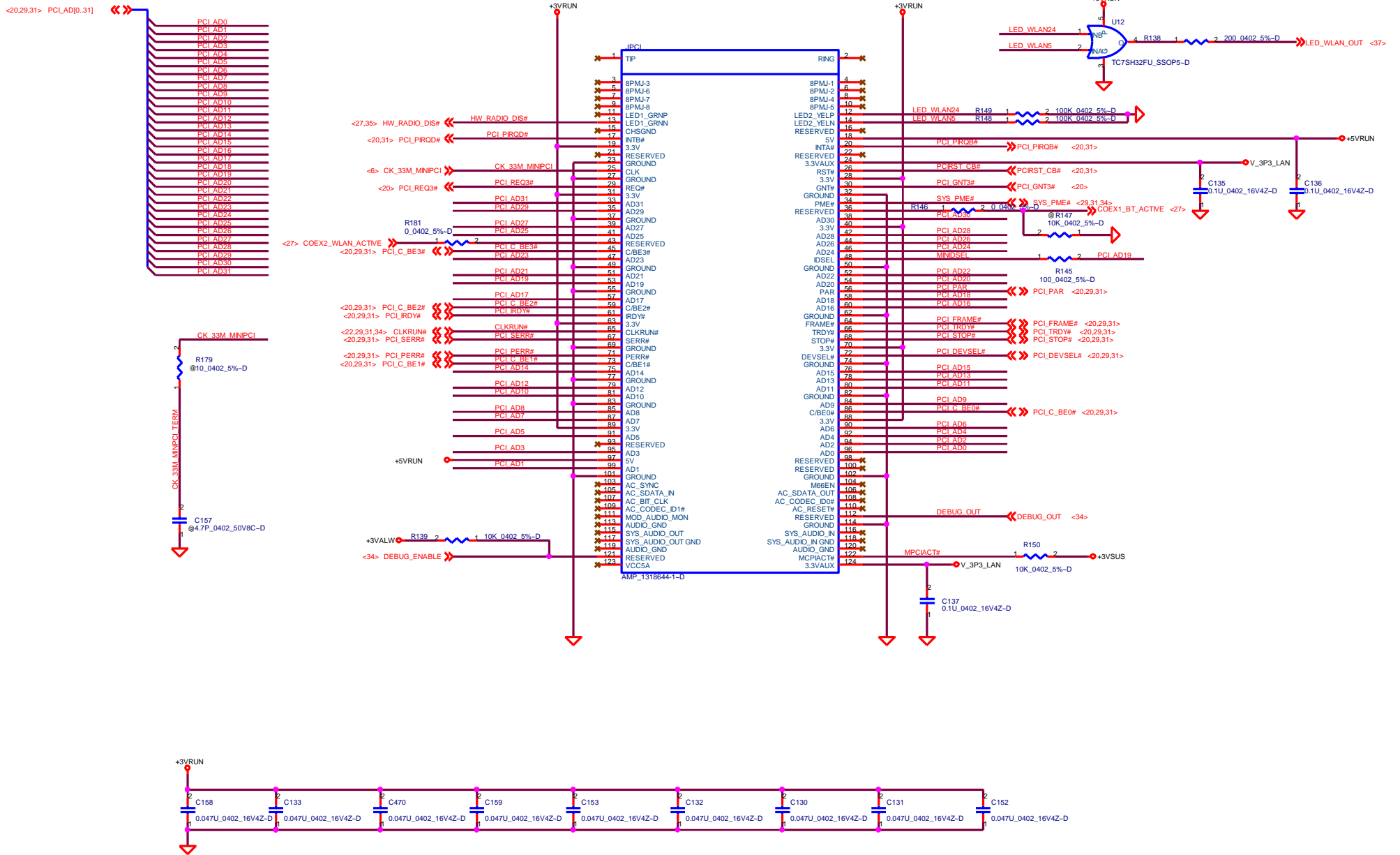
Layout Note: Place close to SD CONN.



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**CardBus/SD card Socket**  
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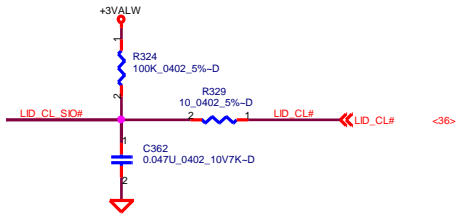
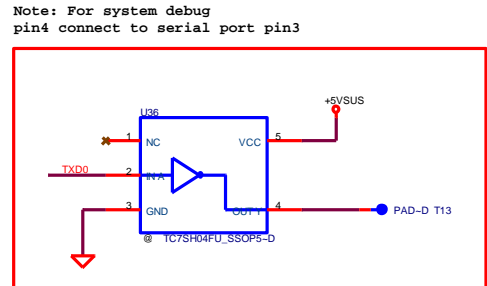
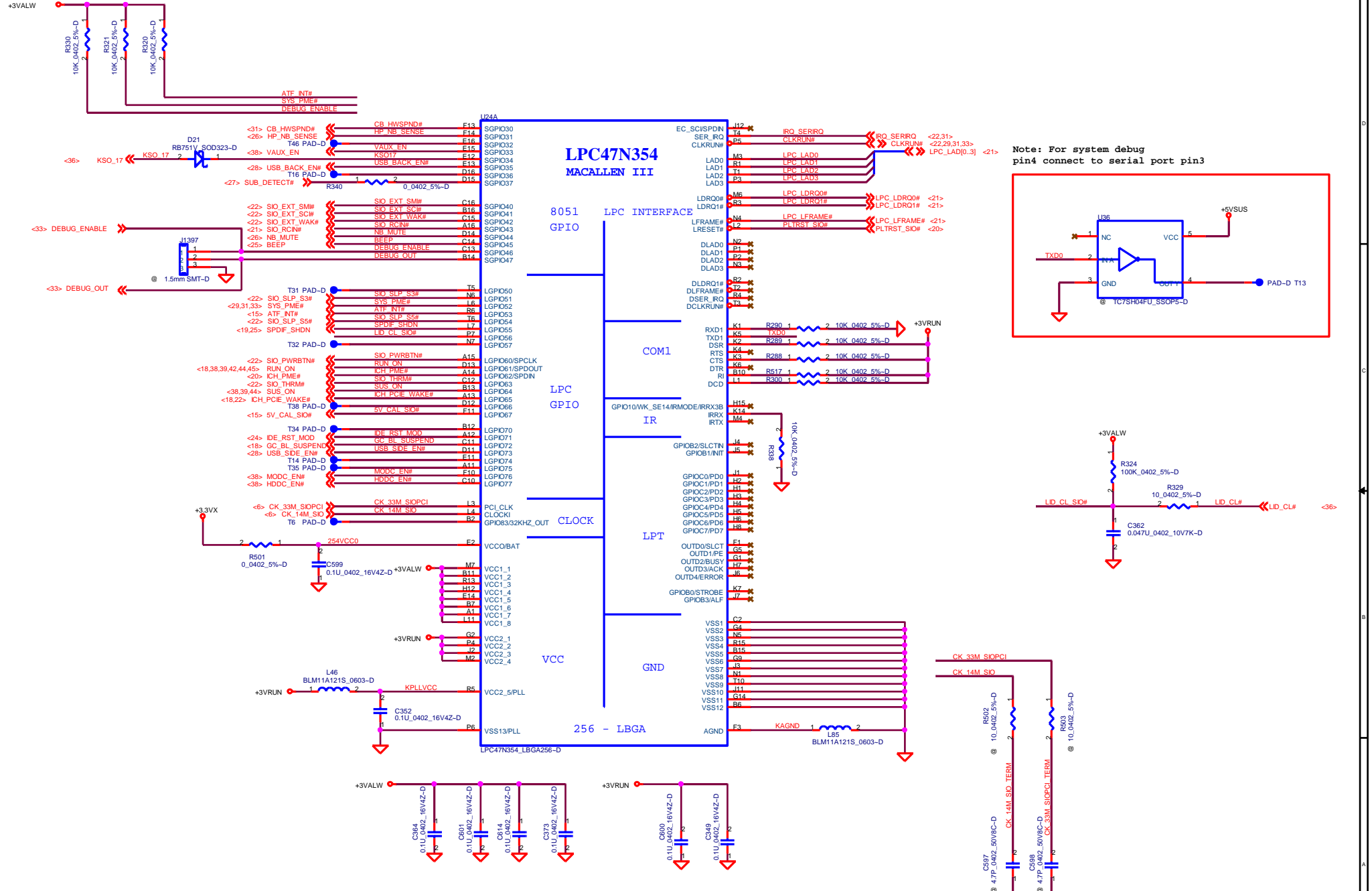
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Compal Electronics, Inc.

**SIO LPC47N354(1/2)**

Size: Document Number  
**LA-2171**

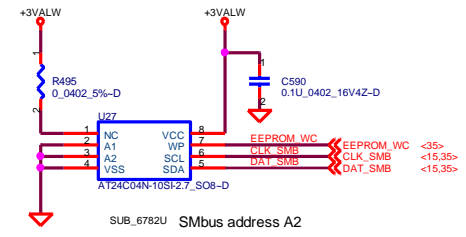
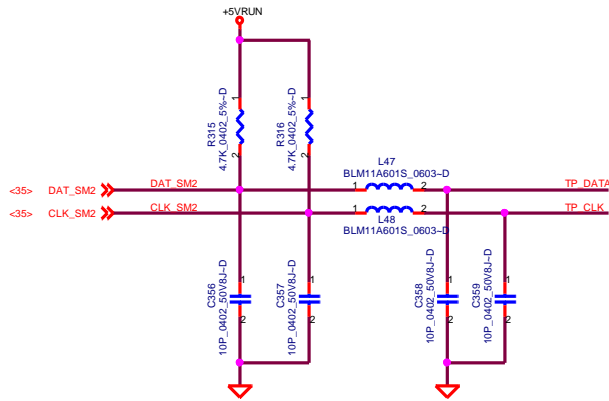
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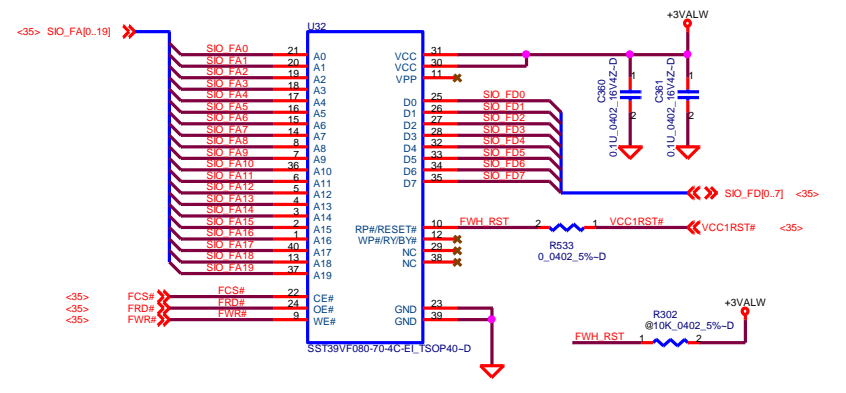
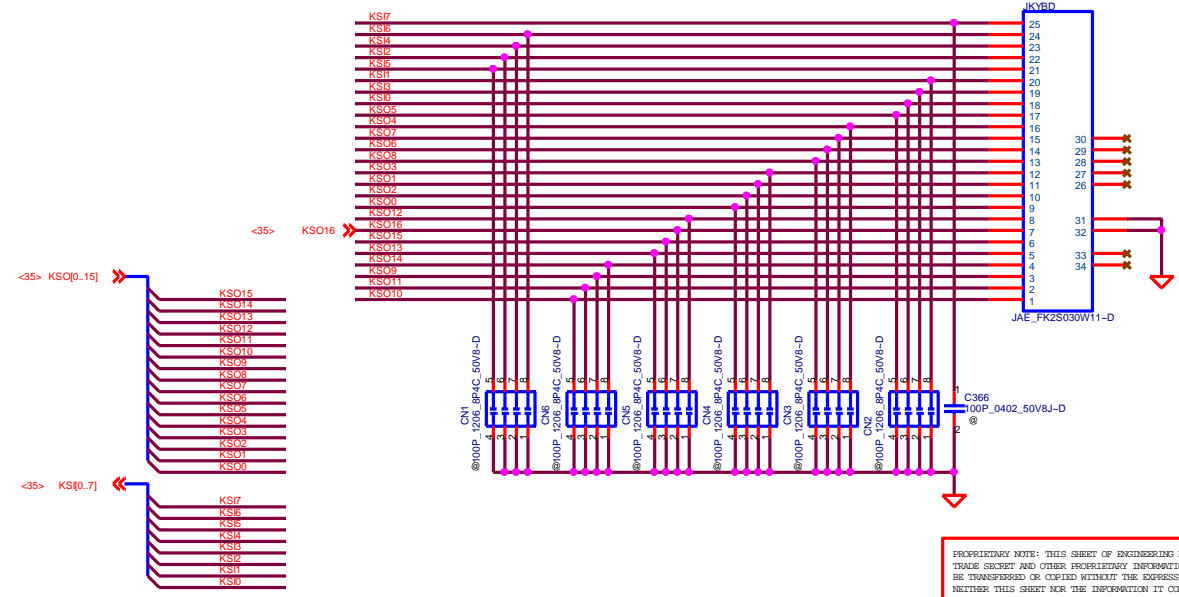
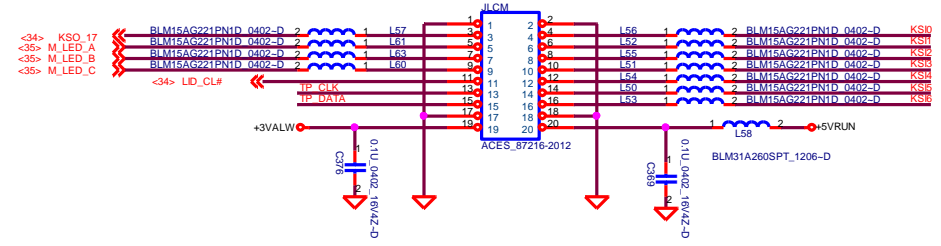
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**Note: SMSC errata**  
**LPC47N354 A Rev Anomaly - Touch Pad IMCLK and IMDAT signals are inverted**

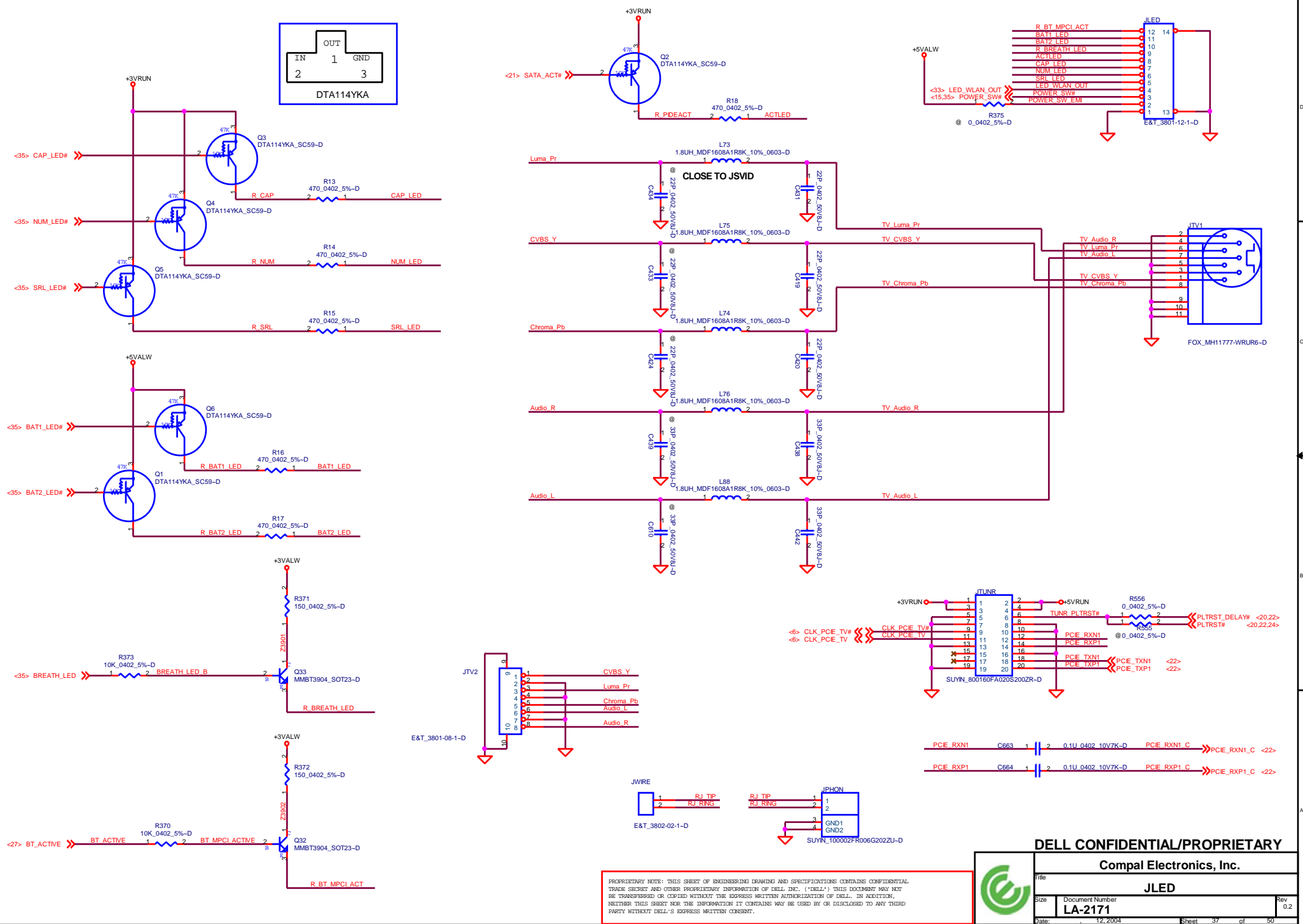


**LCM & Direct play SW & T PAD**



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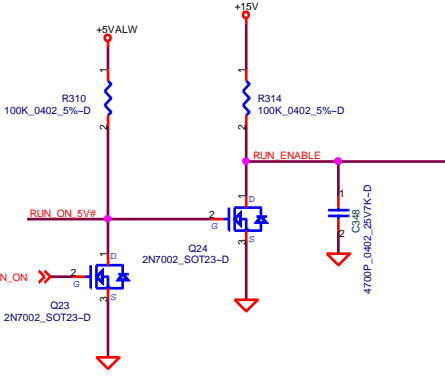


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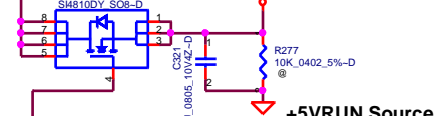


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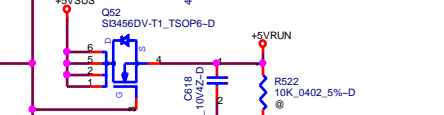
Run Planes Enable



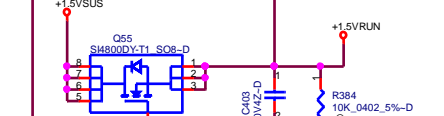
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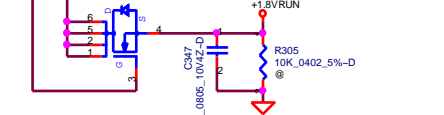
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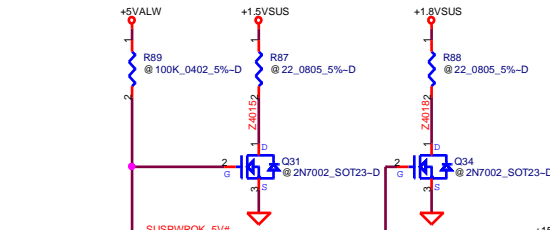
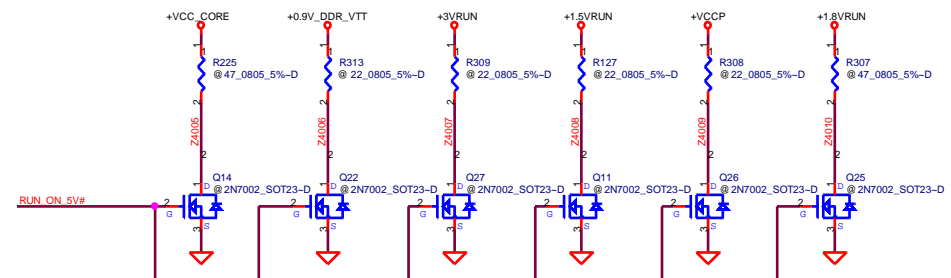
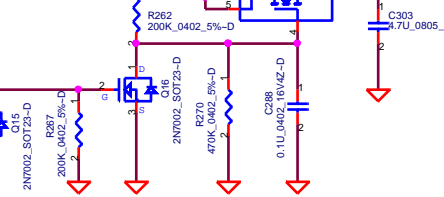
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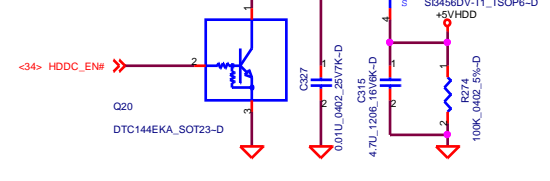
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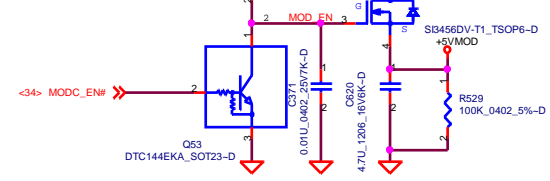
+3VSUS Source



+5VHDD Source



+5VMOD Source



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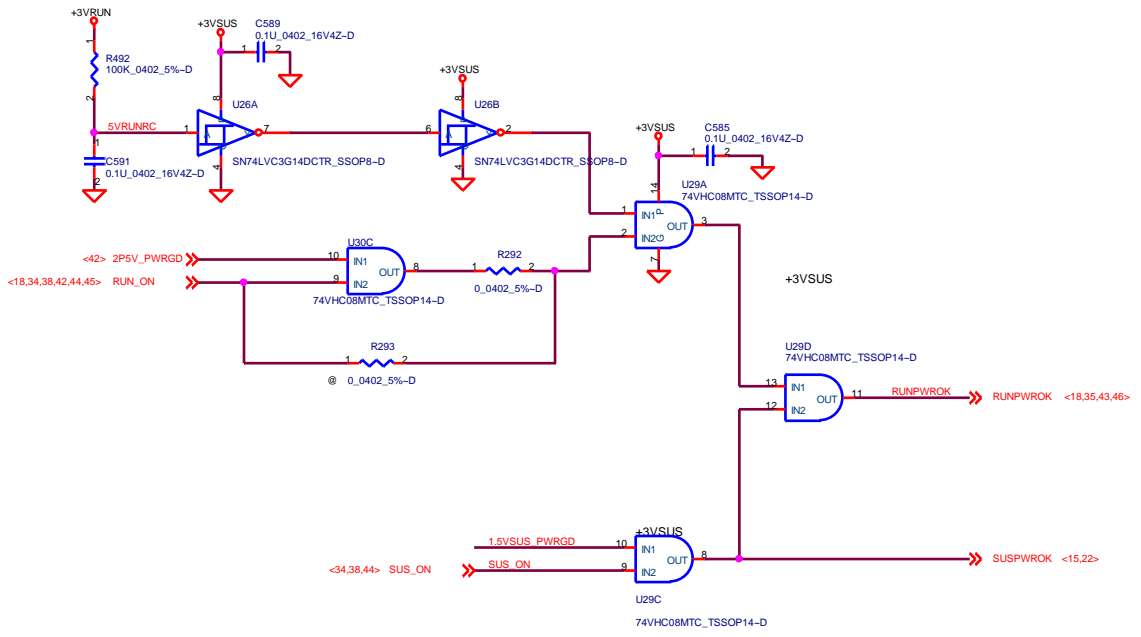
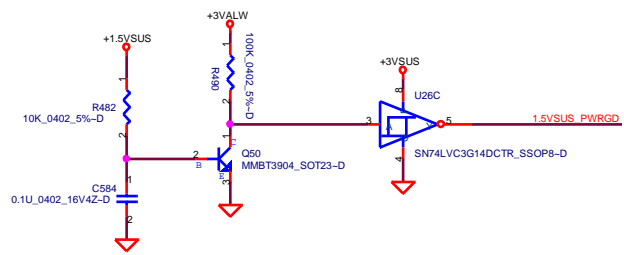
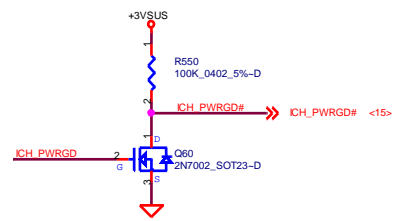
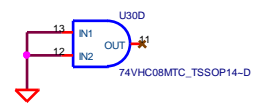
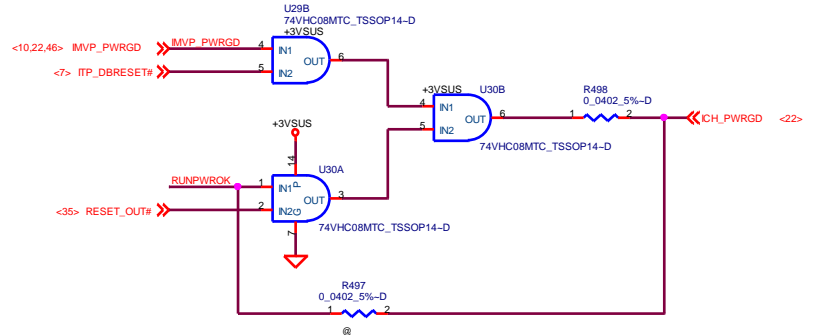
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POWER CONTROL

LA-2171

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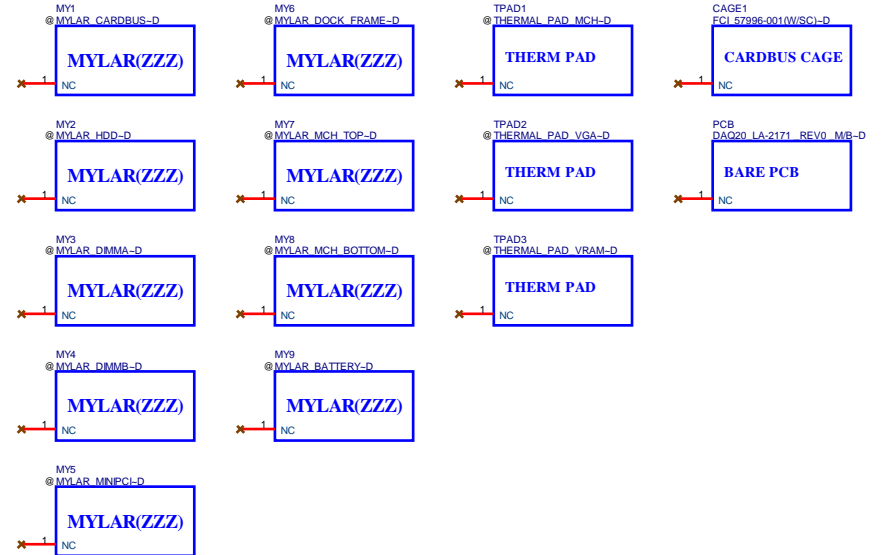
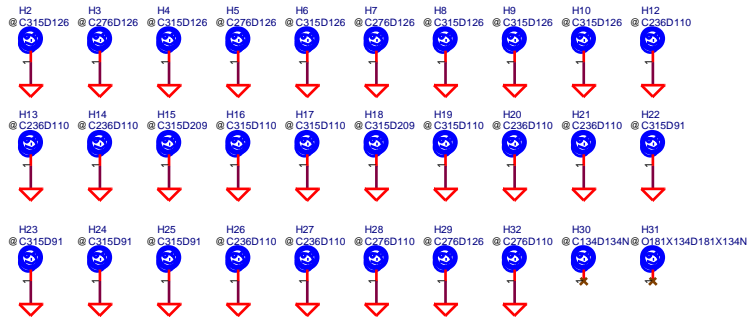
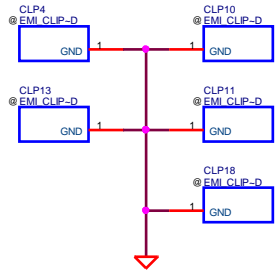
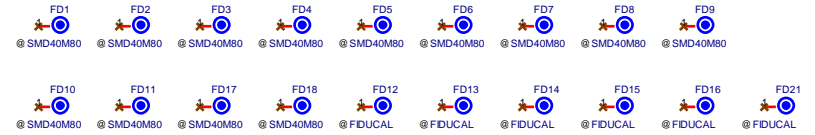


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Fiducial Mark



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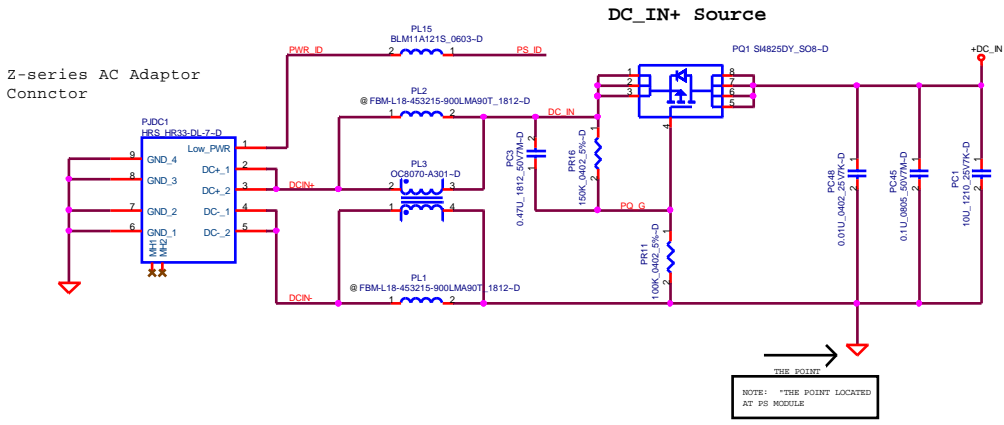
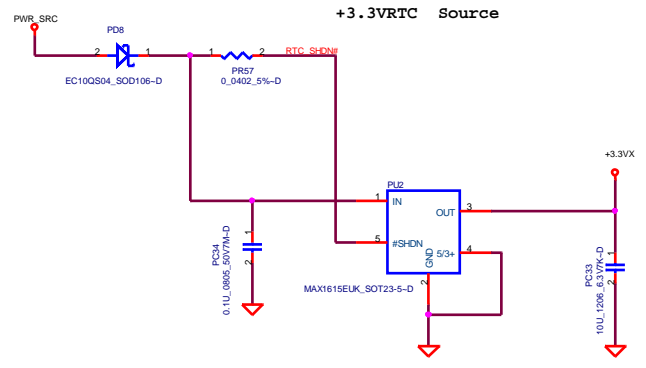
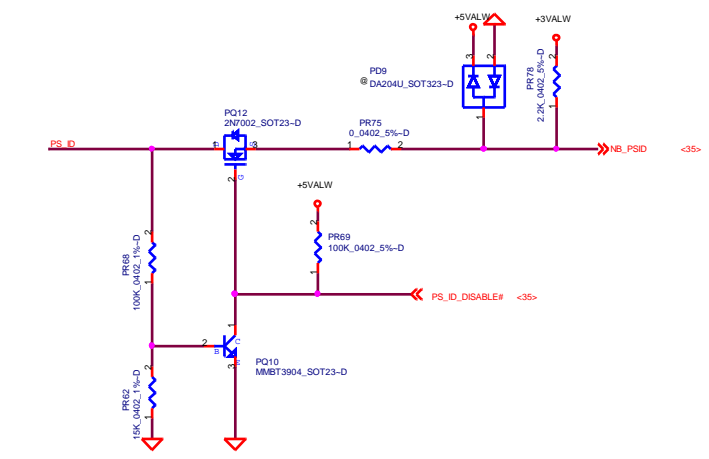
PAD and Standoff

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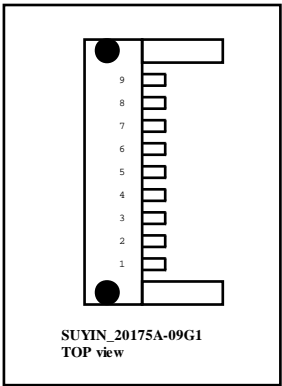
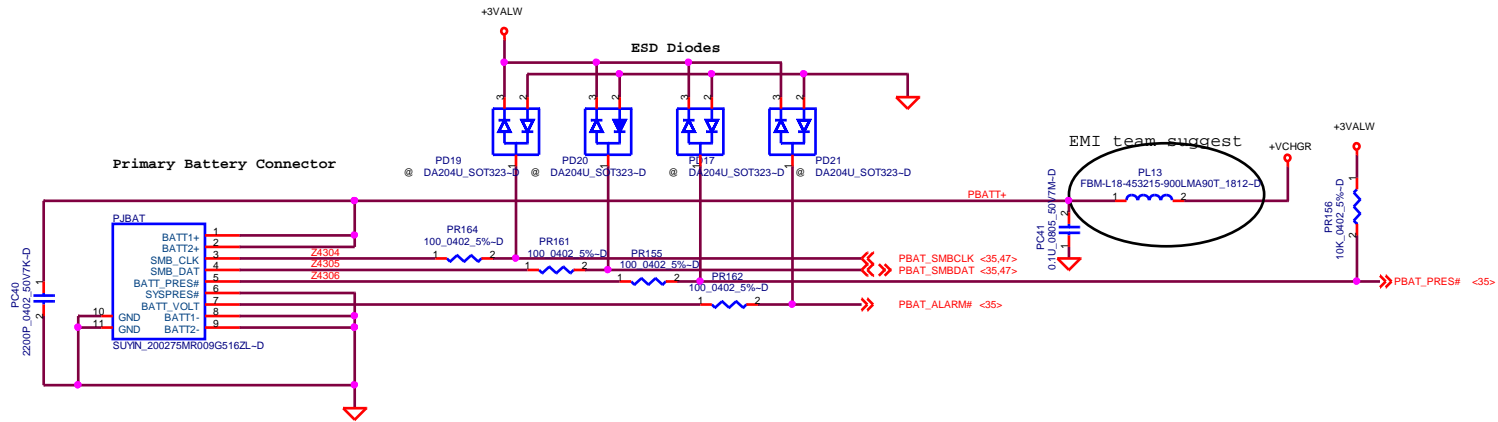
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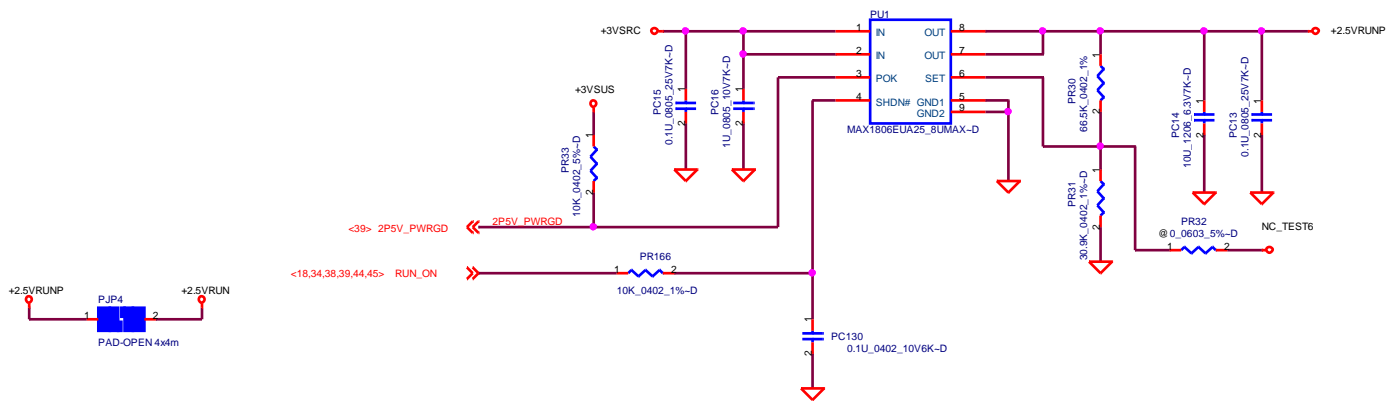
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**+DCIN**

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**+2.5V RUN**  $R1=R2 * (V_o / 0.8 - 1)$ , R2:25K~100K.



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**Battery Conn./+2.5V**

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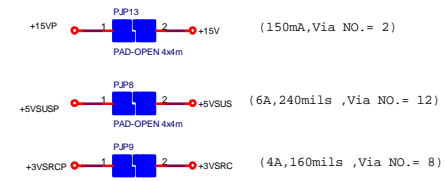
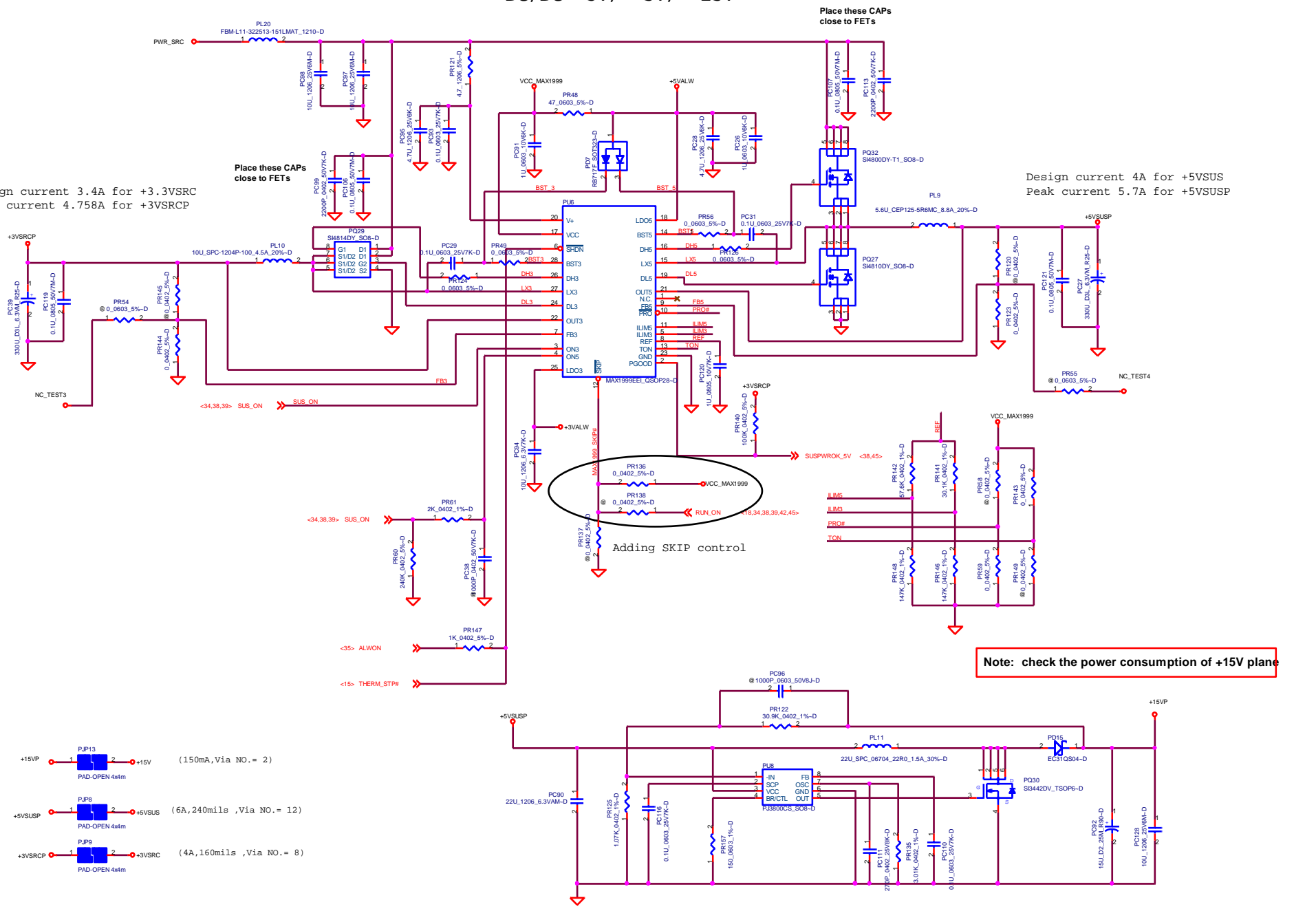
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# DC/DC +3V/ +5V/ +15V

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**Note: check the power consumption of +15V plane**

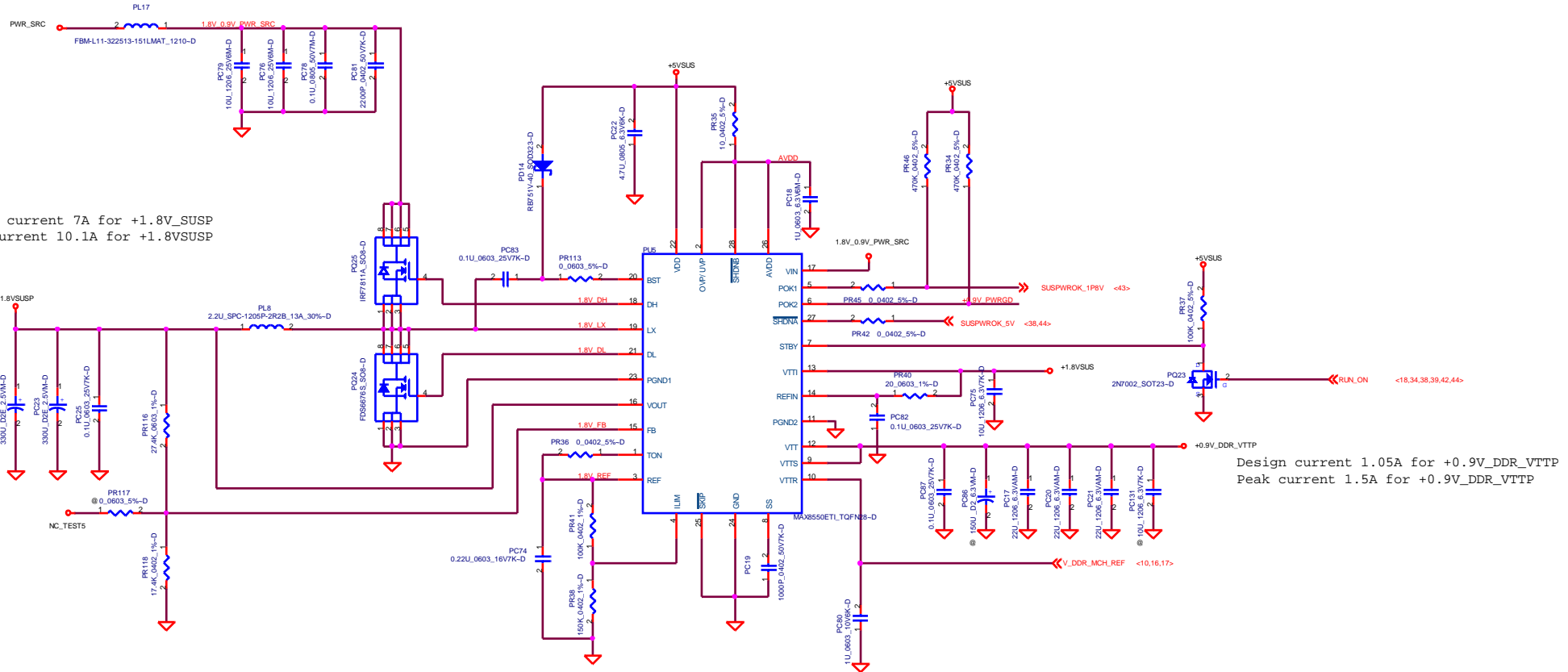
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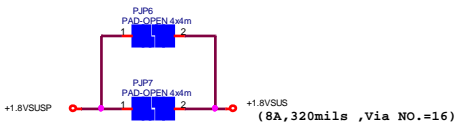
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### +1.8VSUSP/ +0.9V\_DDR\_VTT DDR2 Termination



Design current 7A for +1.8V\_SUSP  
Peak current 10.1A for +1.8VSUSP

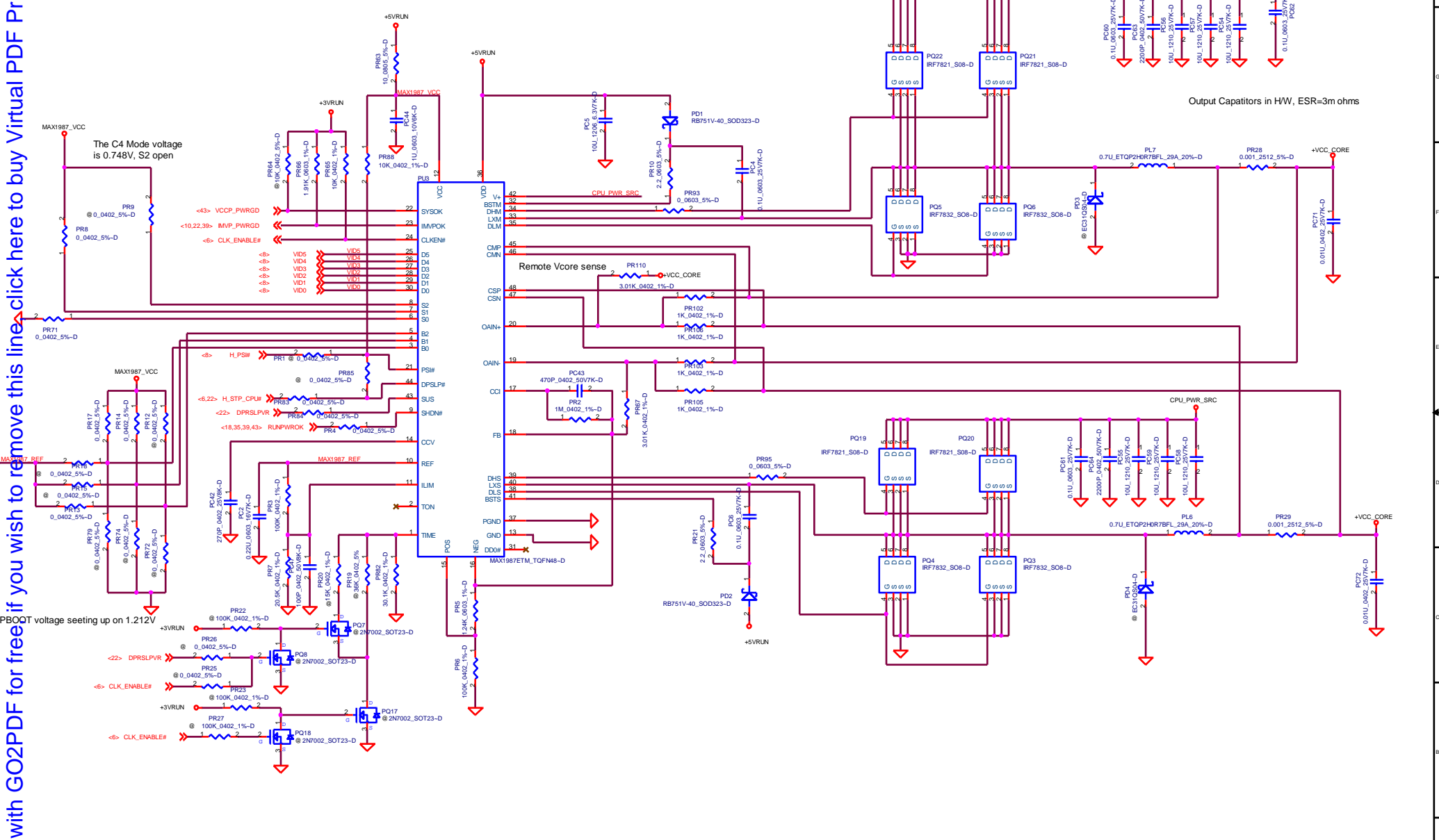
Design current 1.05A for +0.9V\_DDR\_VTTP  
Peak current 1.5A for +0.9V\_DDR\_VTTP



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<b>+1.8VSUSP/ +0.9V_DDR_VT</b>		
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V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	1	1	1	0	1.484
0	1	1	0	0	1	1.308
1	0	1	1	1	1	0.956
1	1	1	1	1	0	0.748



Change PR22 to 1k. Delete PR22/PQ8/PQ17/PQ1/PQ18/PR20/PR26/PR23/PQ19 for BANIAS and DOTHAN.  
 PR22/PQ8/PQ17/PQ1/PQ18/PR20/PR26/PR23 and PR19 are only for YONAH CPU.

- TRANSITION TIMING:
- (a) START-UP and SHUTDOWN (SUS=LOW, RUNPWROK=LOW) : 2mV/us
  - (b) ENTER SUSPEND (SUS=HIGH, RUNPWROK=HIGH) : 8.6mV/us
  - (c) EXIT SUSPEND (SUS=LOW, RUNPWROK=HIGH) : 24.7mV/us

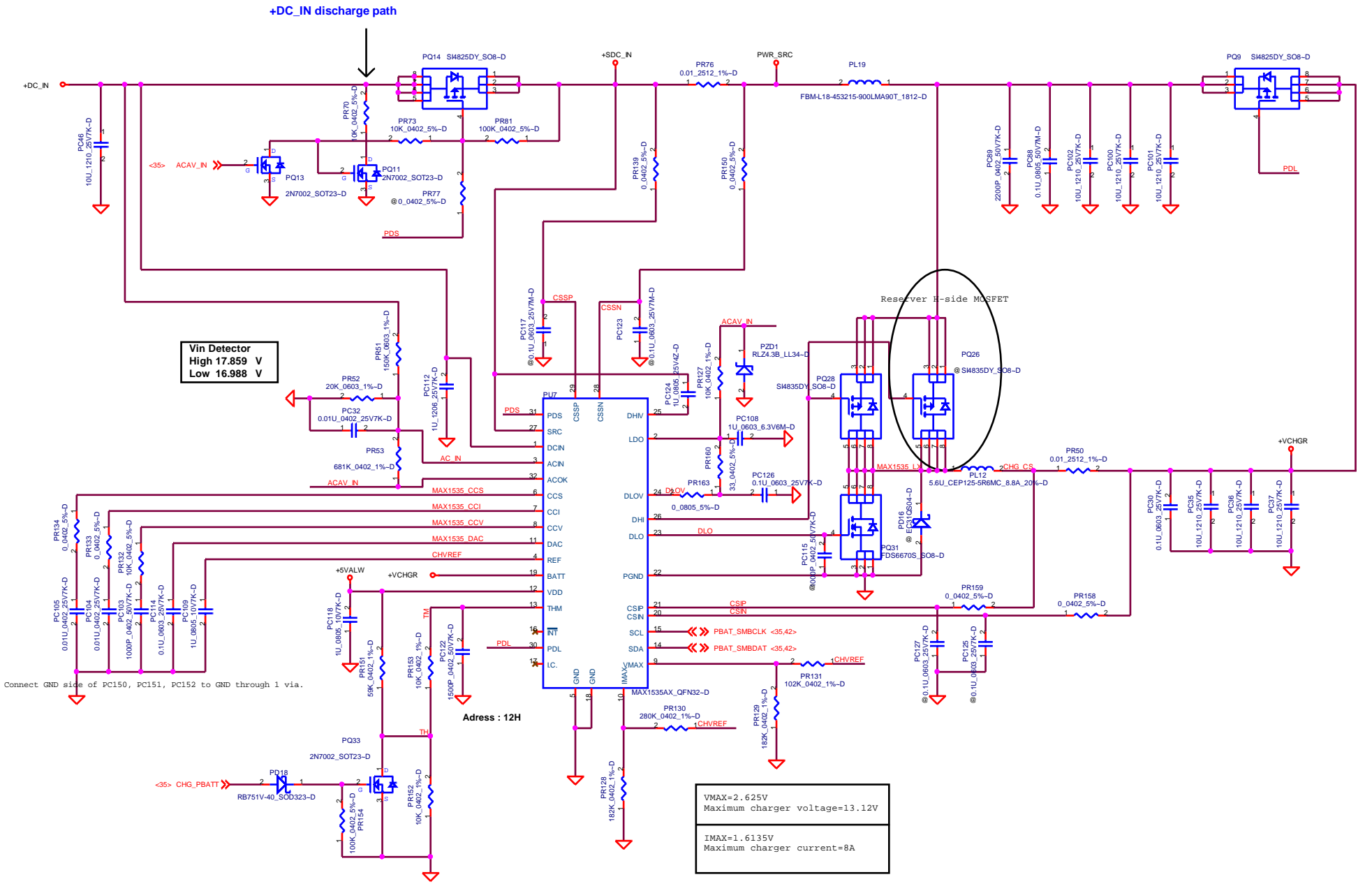
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**+VCORE**

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Charger

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31&32	Cardbus	10/15/03	Dell	Change cardbus controller to TI PCI4515.	Change U162	M00
2	18	VGA/B & DVI CONN.	10/16/03	Dell	Add DVI connector.	Add JDVI	M00
3	25	SATA Bridge	10/16/03	Dell	Add SATA to PATA circuit.	Add page 25	M00
4	28	Subwoofer	10/16/03	Dell	Add subwoofer circuit.	Add page 28	M00
5	40	LED/B	10/16/03	Dell	Removed IR circuit.	Delete U52	M00
6	27	Amplifier & Phone JACK	10/17/03	Dell	Removed internal MIC circuit.		X00
7	31&32	LOM	10/17/03	Dell	Change LAN controller (U164) from 5751M to 4401. Add pop option for the 5705 like Kapalua/Lindbergh board.		X00
8	33	Cardbus	10/17/03	Dell	Depop 1394 choke, L142 and pop bypass resistors, R1025, R1026, R1027, R1028		X00
9	1	Cover page	10/17/03	Dell	Change schematic revision from M00 to X00.		X00
10	40	PAD & ME & spare parts	01/07/04	Compal	For EMI requirement.	Pop CLP4,5,10,11,13 and depop CLP18	X01
11	22	ICH6(3/4)	01/08/04	Dell	Connected PCIE channel 1 to TV-Tuner connector.	Delete T4,T5,T29,T30 and add C661,C662	X01
12	37	LED/B & TV TUNER	01/08/04	Dell	Connected TV tuner signals.	Add C663,C664	X01
13	40	PAD & ME & spare parts	01/08/04	Compal	Added ME standoff.	Pop H12,H13,H14,H17,H20,H21,H26,H27	X01
14	32	CardBus(2/2)	01/28/04	Compal	Fixed SD card issue.	The pin11 of JSD need to be connected to GND and pin 12 need to be connected to U17 pin b3.	X01
15	10	Alviso(1/5)	01/28/04	Dell	From Intel Message.	Change C124 from 220pF to 0.1uF and move capacitor as close as possible to the HVREF pin (pin J11 of U15).	X01
16	6	Clock Generator	01/28/04	Dell	Per Intel and ICS recommendation.	Connect the SATA clock to SRC4 and connect the VGA clock to SRC1.	X01
17	7&10	Dothan(1/2) & Alviso(1/5)	01/28/04	Dell	Per the Intel Check list 1.301	Change R397 and R114 to 75 ohm.	X01
18	36	Internal K/B & LCM CONN.	01/29/04	Compal	The BIOS debug connector is for bring up only.	Delete JDEBUG.	X01
19	1	Cover page	01/29/04	Compal	Change schematic revision from X00 to X01.		X01
20	35	Macallen(2/2)	01/29/04	Compal	Board ID X01.	Pop R318 and depop R319.	X01
21	34	Macallen(1/2)	01/29/04	Compal	Reserved a inverter for serial port debug.	Add U36 and T13.	X01
22	40	PAD & ME & spare parts	01/30/04	Compal	This clip have interferenced with screw hole.	Delete CLP5 and add H32	X01
23	37	LED/B & TV TUNER	02/02/04	Compal	The indicative LED of HDD doesn't work well.	Remove R12 and connect the pin3 of Q2 to +3VRUN.	X01
24	37	LED/B & TV TUNER	02/04/04	Dell	Changed JTUNR pin definitions	Added PCIRST#, CLK_PCIE_TV/TV# signals	X01
25	6	Clock Generator	02/04/04	Dell	Added PCIE clock connection to JTUNR	Added R551, R552, R553, R554	X01

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Changed-List History

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# Version Change List ( P. I. R. List ) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	49	Charger selector	2003/10/14	Compal	Modify charger selector circuit.	Need to discuss.	0.0
2	42	PSID & +3VX	2003/10/15	Compal	Modify PSID circuit same as Nimitas. And add current limit resistor on RTC charger.	Add ESD solution on PSID, and limit RTC charge current.	0.0
3	44	+15VP	2003/11/4	Compal	+15VP current rating is not enough for subwoofer	Use MB3800 Boost IC to generate +15VP from +5VSUSP	X00
4	47	Charger	2003/11/5	Compal	That has leakage current from battery goes through PQ22 and PQ44 to DC IN.	Move Adaptor current sense PR144 after PQ24 and before PWR_SRC. That is same as Nimitaz.	X00
5	44	+15VP	2003/12/11	Compal	Test +15VP on Demon board. The output ripple voltage is large and improve efficiency.	Add PC128 10U_1206_25V, change PQ30 from SI2302DS to SI3442DV, change PR157 form 392_0603_1% to 150_0603_1%, no-pop PC96.	M00
6	45	+1.8VSUSP	2004/2/1	DELL	Change DDRII DC-DC solution for cost down.	Using MAXIM MAX8550 .	X01
7	43	+VCCP_1P05VP	2004/2/1	Compal	VCCP_1p05VP has two 330uF caps on it(PC10, PC11), Laguna only has one. Do we need two?	Can de-populate PC11, and test is OK.	X01
8	45	+1.8VSUSP	2004/2/5	Compal	Voltage divider setting is error, the FB regulate on 0.7V.	Change PR116 from 45.3K_0402_1% to 27.4K_0603_1%. Change PC22 from 1U_0603_6.3V to 4.7U_0805_6.3V	X01
9	46	+VCC_CORE	2004/2/5	Compal	Choke height is over mechanical height limitation	Change PL6 and PL7 from 0.6U_HK_AE26A0R6 to 0.7U_ETQP2H0R7BFL.	X01
10	46	+VCC_CORE	2004/2/6	Compal	EMI broad band test is over 1~2 db	Change PR10 and PR21 from 0_0603_5% to 2.2_0603_5%.	X01
11	41	PS_ID	2004/2/11	DELL	Open issue #60 Change PS_ID pullup resistor, PR78, from 1.5K to 2.2K	Change PR78 from 1.5K_0603_1% to 2.2K_0402_5%.	X01
12	45	+0.9V_DDR_VTTP	2004/2/11	DELL	Open issue #63 Please add a 10uf, 1206 package capacitor at the output of PU5 pin 12, +0.9V_DDR_VTTP.	Add and reserve PC131 10U_1206_6.3V7K.	X01
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**Power-Changed-List History**



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