

Compal Confidential

DCL55 Schematics Document

Banias ICP uFCBGA/uFCPGA Package with Montara-GM Core Logic

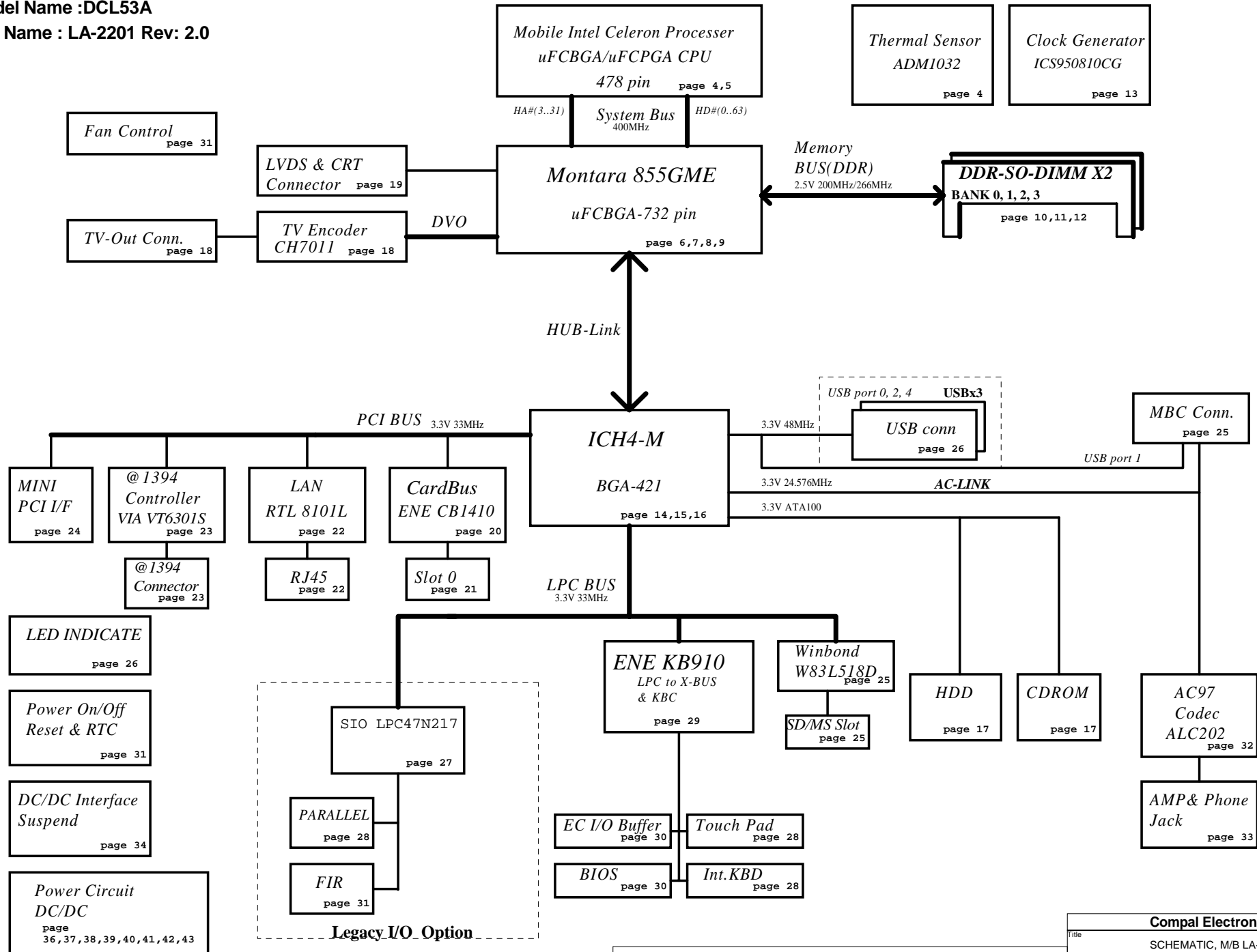
2005-05-23

REV: 3.0

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Title	SCHEMATIC, M/B LA-2201	
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	401282	C
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Model Name :DCL53A
File Name : LA-2201 Rev: 2.0



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
R368	100K +/- 5%			
Board ID	R361	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

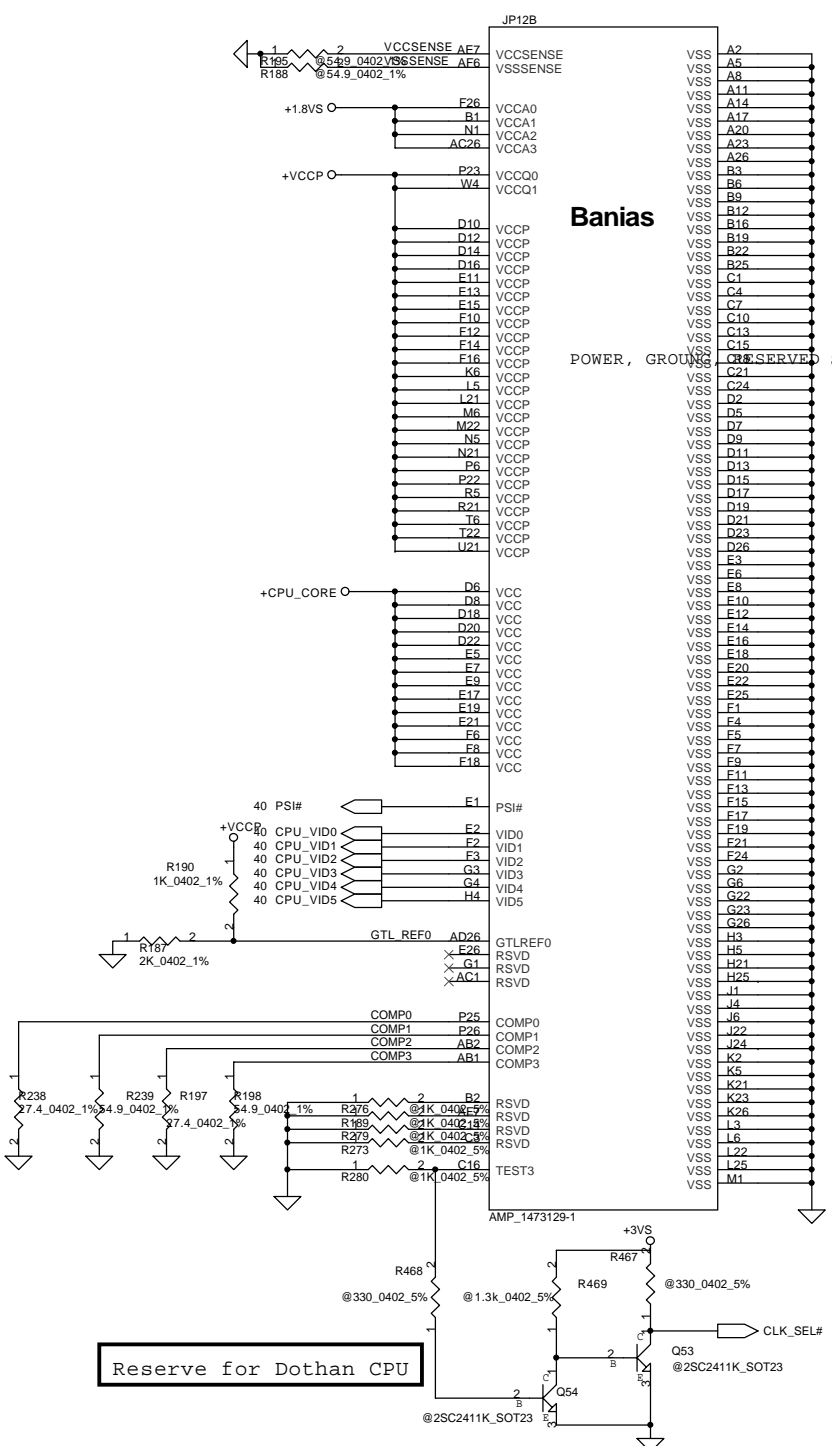
Board ID	PCB Revision
0	
1	0.1
2	0.2
3	1.0
4	
5	
6	
7	

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

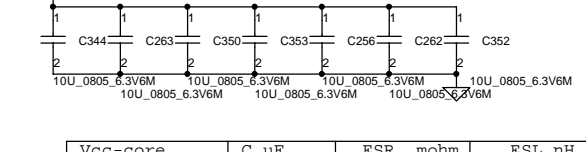
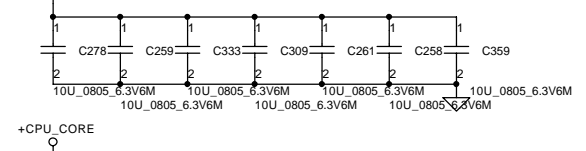
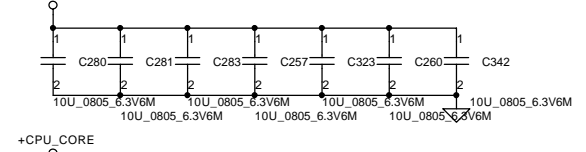
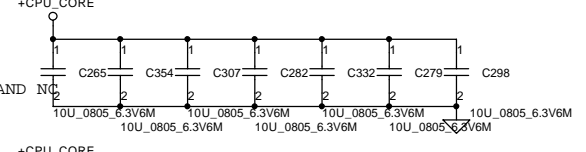
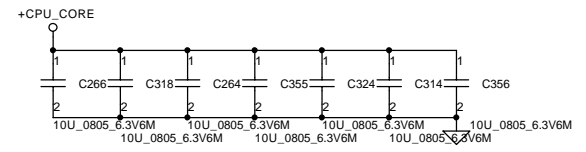
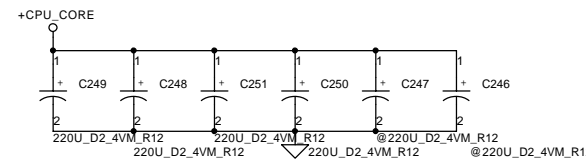
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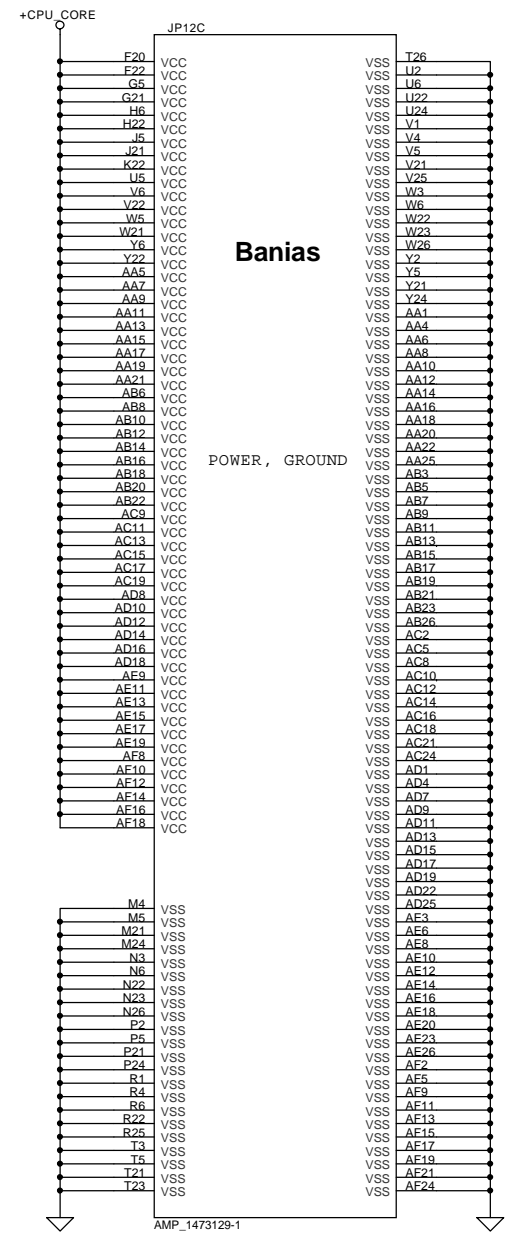
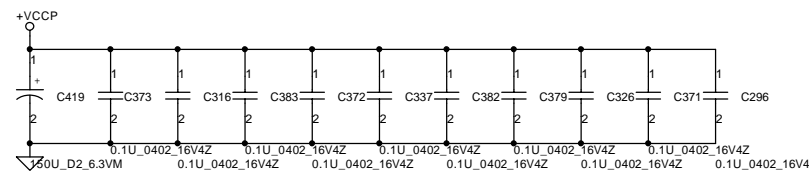
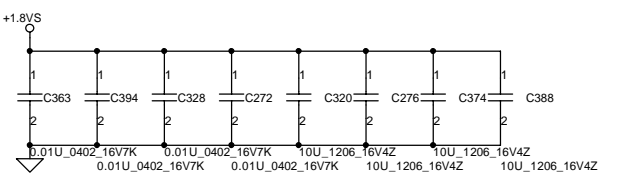


Banias

POWER, GROUND RESERVED SIGNALS AND NC



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



Banias

POWER, GROUND

Reserve for Dothan CPU

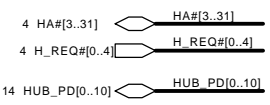
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Montara-GM(L)

HA#3	P23	HA#3	K22
HA#4	T25	HA#4	H27
HA#5	T28	HA#5	K25
HA#6	R27	HA#6	L24
HA#7	U23	HA#7	L27
HA#8	U24	HA#8	G28
HA#9	R24	HA#9	L27
HA#10	U28	HA#10	L23
HA#11	V28	HA#11	L25
HA#12	U27	HA#12	J24
HA#13	T27	HA#13	K23
HA#14	V27	HA#14	G27
HA#15	U25	HA#15	J23
HA#16	V26	HA#16	H26
HA#17	Y24	HA#17	E26
HA#18	V25	HA#18	B27
HA#19	V23	HA#19	H23
HA#20	W25	HA#20	E27
HA#21	Y25	HA#21	G25
HA#22	AA27	HA#22	E28
HA#23	W24	HA#23	G27
HA#24	W23	HA#24	G24
HA#25	W27	HA#25	C28
HA#26	Y27	HA#26	B26
HA#27	AA28	HA#27	C26
HA#28	W28	HA#28	E26
HA#29	AB27	HA#29	B26
HA#30	Y26	HA#30	G22
HA#31	AB26	HA#31	C26

H_REQ#0	R28	HREQ#0	R28
H_REQ#1	P25	HREQ#1	P25
H_REQ#2	R23	HREQ#2	R23
H_REQ#3	R25	HREQ#3	R25
H_REQ#4	T23	HREQ#4	T23
HADSTB#0	T26	HADSTB#0	T26
HADSTB#1	AA26	HADSTB#1	AA26

AD29	BCLK#	AD29	BCLK#
AE29	BCLK	AE29	BCLK
K28	HYSWING	K28	HYSWING
B18	HXSWING	B18	HXSWING
H28	HYRCOMP	H28	HYRCOMP
B20	HXRCOMP	B20	HXRCOMP

K21	HVREF0	K21	HVREF0
J21	HVREF1	J21	HVREF1
J17	HVREF2	J17	HVREF2
Y28	HCCVREF	Y28	HCCVREF
Y22	HAVREF	Y22	HAVREF

J28	H_DSTBN#0	J28	HDSTBN#0
C27	H_DSTBN#1	C27	HDSTBN#1
E22	H_DSTBN#2	E22	HDSTBN#2
D18	H_DSTBN#3	D18	HDSTBN#3
K27	H_DSTBP#0	K27	HDSTBP#0
D26	H_DSTBP#1	D26	HDSTBP#1
E21	H_DSTBP#2	E21	HDSTBP#2
E18	H_DSTBP#3	E18	HDSTBP#3
J25	H_DINV#0	J25	HDINV#0
E25	H_DINV#1	E25	HDINV#1
B25	H_DINV#2	B25	HDINV#2
G19	H_DINV#3	G19	HDINV#3

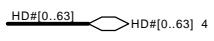
F15	CPURST#	F15	CPURST#
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U17	HUB_PD0	U17	HL_0
U4	HUB_PD1	U4	HL_1
U3	HUB_PD2	U3	HL_2
V3	HUB_PD3	V3	HL_3
W2	HUB_PD4	W2	HL_4
W6	HUB_PD5	W6	HL_5
V6	HUB_PD6	V6	HL_6
W7	HUB_PD7	W7	HL_7
T3	HUB_PD8	T3	HL_8
V5	HUB_PD9	V5	HL_9
V4	HUB_PD10	V4	HL_10
W3	HI_PSTRB	W3	HLSTB
V2	HI_PSTRB#	V2	HLSTB#
T2	HUB_VSWING	T2	HLRCOMP
U2	HUB_VREF	U2	PSWING
W1		W1	HLVREF

HOST

HUB I/F

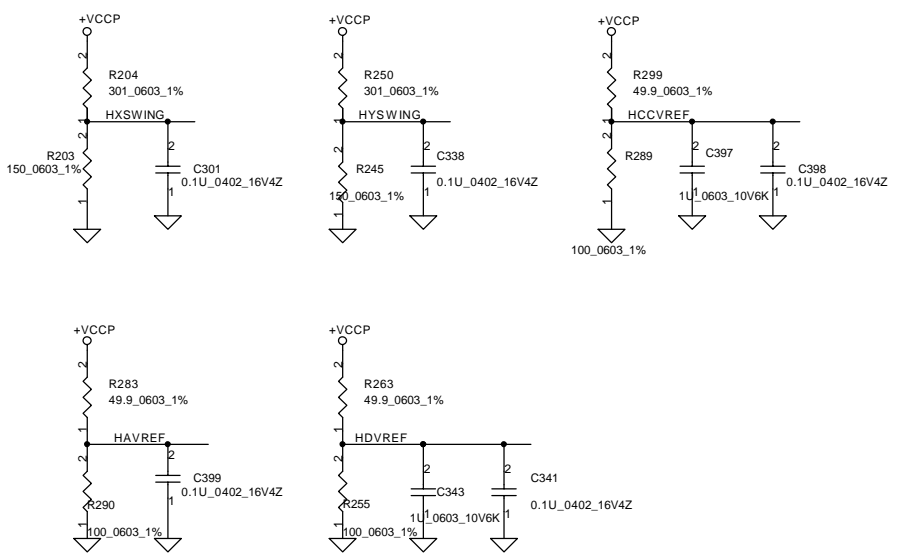
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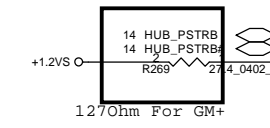
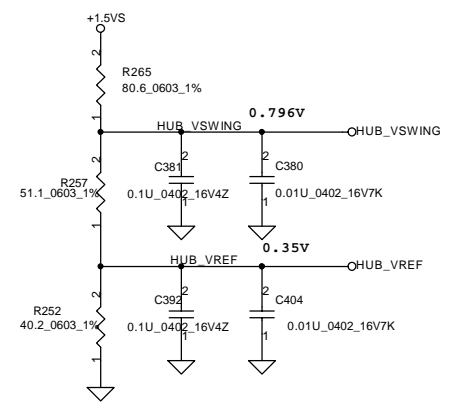
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HD#1	H27	HD#1	H27
HD#2	K25	HD#2	K25
HD#3	L24	HD#3	L24
HD#4	L27	HD#4	L27
HD#5	G28	HD#5	G28
HD#6	L27	HD#6	L27
HD#7	L23	HD#7	L23
HD#8	L25	HD#8	L25
HD#9	J24	HD#9	J24
HD#10	K23	HD#10	K23
HD#11	G27	HD#11	G27
HD#12	K26	HD#12	K26
HD#13	H23	HD#13	H23
HD#14	J23	HD#14	J23
HD#15	H26	HD#15	H26
HD#16	E26	HD#16	E26
HD#17	B27	HD#17	B27
HD#18	H23	HD#18	H23
HD#19	E27	HD#19	E27
HD#20	G25	HD#20	G25
HD#21	E28	HD#21	E28
HD#22	G27	HD#22	G27
HD#23	G24	HD#23	G24
HD#24	C28	HD#24	C28
HD#25	B26	HD#25	B26
HD#26	C26	HD#26	C26
HD#27	E26	HD#27	E26
HD#28	C26	HD#28	C26
HD#29	C23	HD#29	C23
HD#30	B28	HD#30	B28
HD#31	B21	HD#31	B21
HD#32	HREQ#3	HD#32	HREQ#3
HD#33	G21	HD#33	G21
HD#34	C24	HD#34	C24
HD#35	C23	HD#35	C23
HD#36	E22	HD#36	E22
HD#37	E24	HD#37	E24
HD#38	D24	HD#38	D24
HD#39	B22	HD#39	B22
HD#40	G20	HD#40	G20
HD#41	E23	HD#41	E23
HD#42	B23	HD#42	B23
HD#43	C23	HD#43	C23
HD#44	E21	HD#44	E21
HD#45	C20	HD#45	C20
HD#46	C21	HD#46	C21
HD#47	G18	HD#47	G18
HD#48	E19	HD#48	E19
HD#49	E20	HD#49	E20
HD#50	G17	HD#50	G17
HD#51	D20	HD#51	D20
HD#52	F19	HD#52	F19
HD#53	C19	HD#53	C19
HD#54	C17	HD#54	C17
HD#55	B19	HD#55	B19
HD#56	G16	HD#56	G16
HD#57	E16	HD#57	E16
HD#58	C16	HD#58	C16
HD#59	E17	HD#59	E17
HD#60	D16	HD#60	D16
HD#61	C18	HD#61	C18
HD#62		HD#62	
HD#63		HD#63	

L28	H_ADS#	L28	H_ADS# 4
M25	H_TRDY#	M25	H_TRDY# 4
M21	H_DRDY#	M21	H_DRDY# 4
M28	H_DEFER#	M28	H_DEFER# 4
N28	H_HIT#	N28	H_HIT# 4
N27	H_HIT#	N27	H_HIT# 4
N27	H_HIT#	N27	H_HIT# 4
M23	H_LOCK#	M23	H_LOCK# 4
M25	H_BR0#	M25	H_BR0# 4
P28	H_BNR#	P28	H_BNR# 4
M26	H_BPR#	M26	H_BPR# 4
N23	H_DBSY#	N23	H_DBSY# 4
P26	H_RS#0	P26	H_RS#0 4
P26	H_RS#1	P26	H_RS#1 4
M27	H_RS#2	M27	H_RS#2 4

HOST REF VOLTAGE



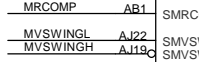
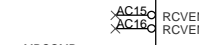
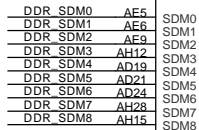
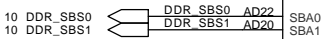
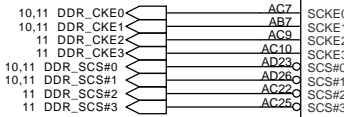
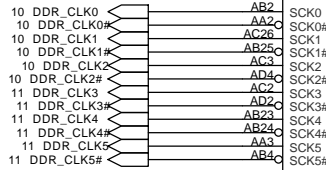
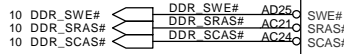
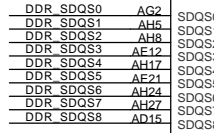
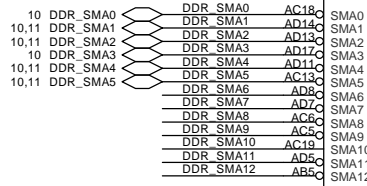
HUB I/F REF VOLTAGE



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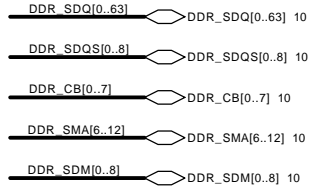
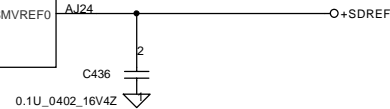
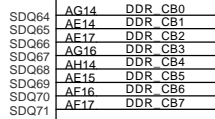
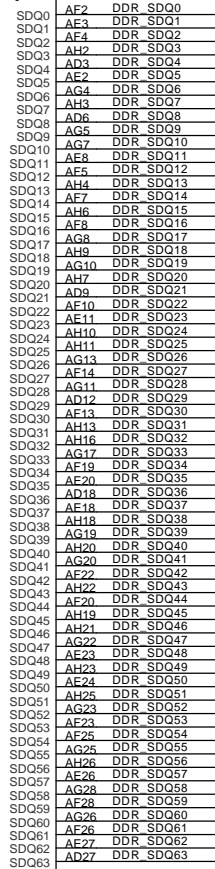
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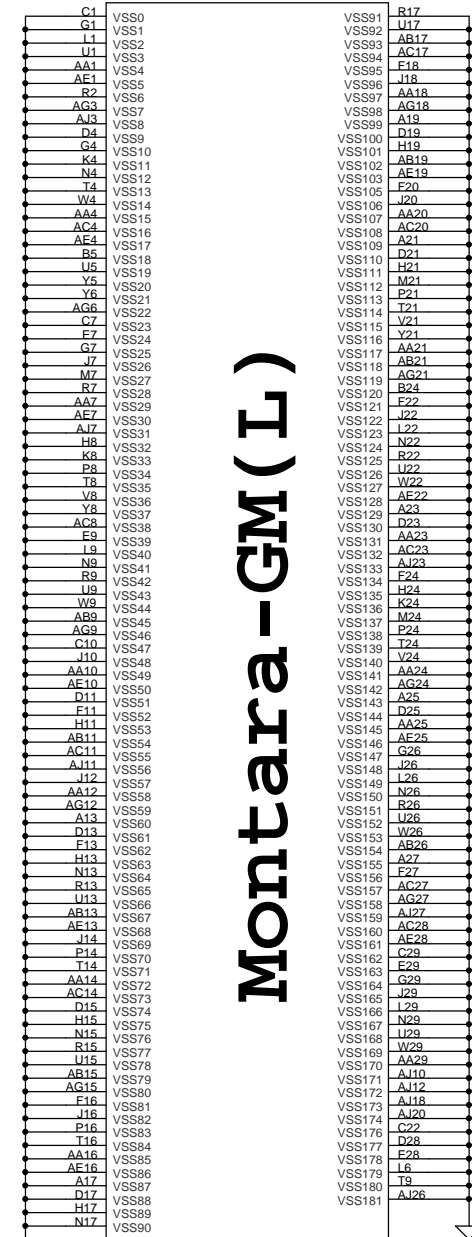
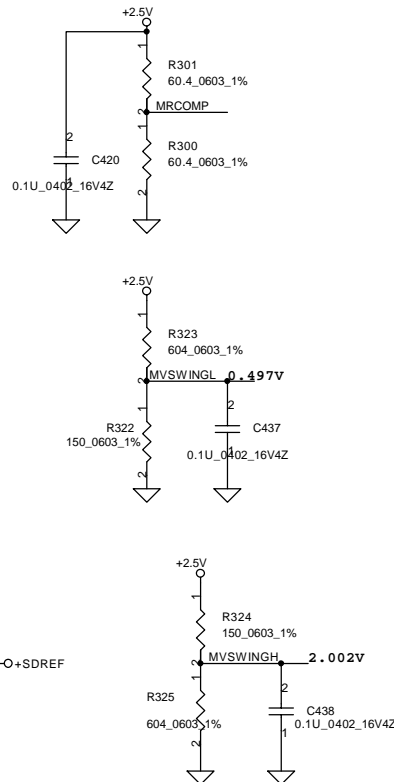


MEMORY

RG82G4350M_uFCBGA732



DDR REF & SWING VOLTAGE



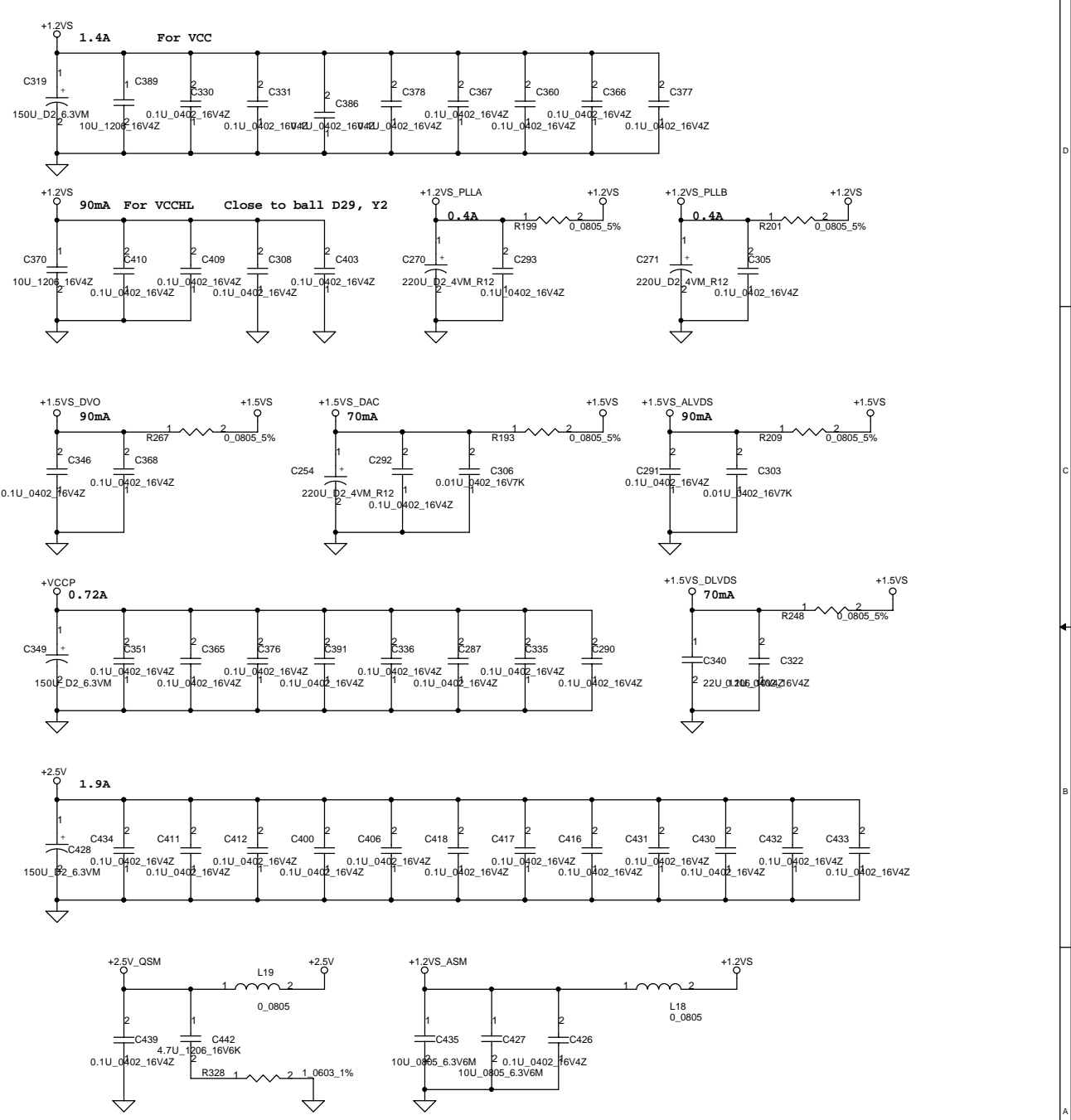
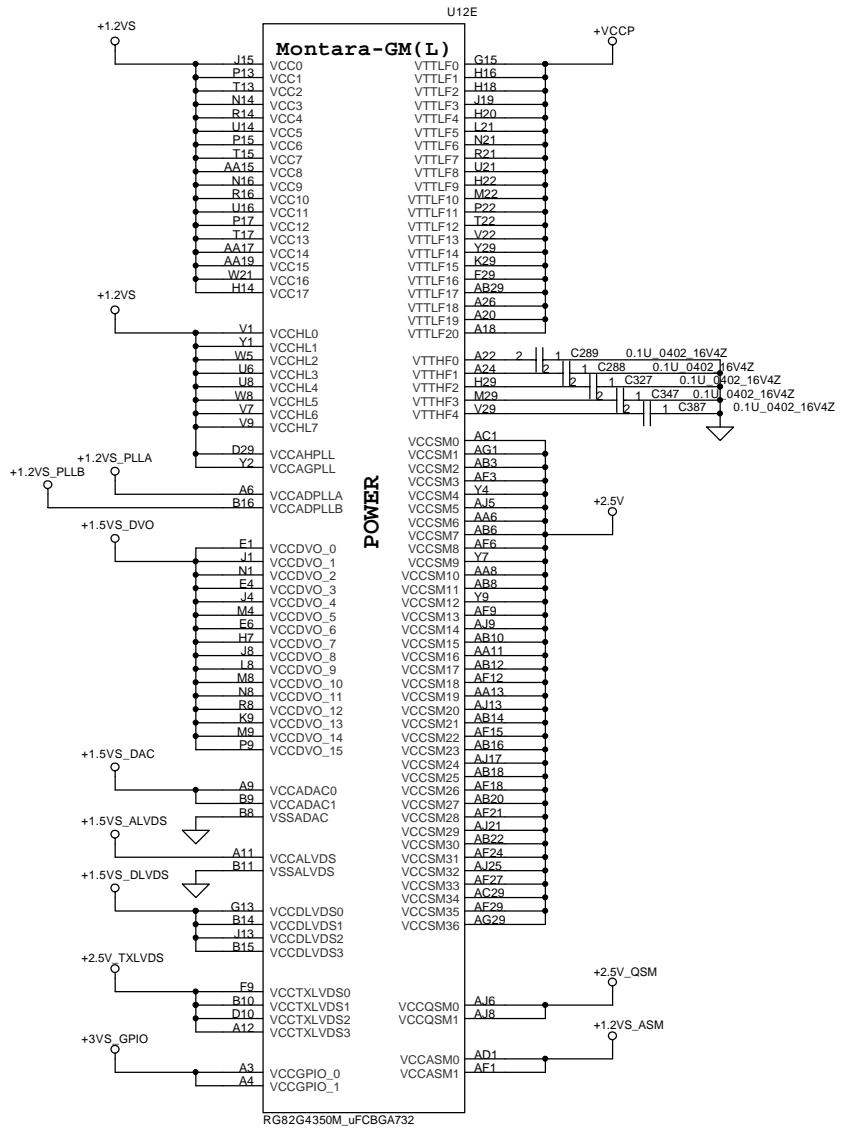
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Montara-GM(L)

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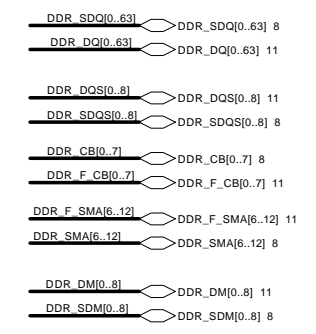
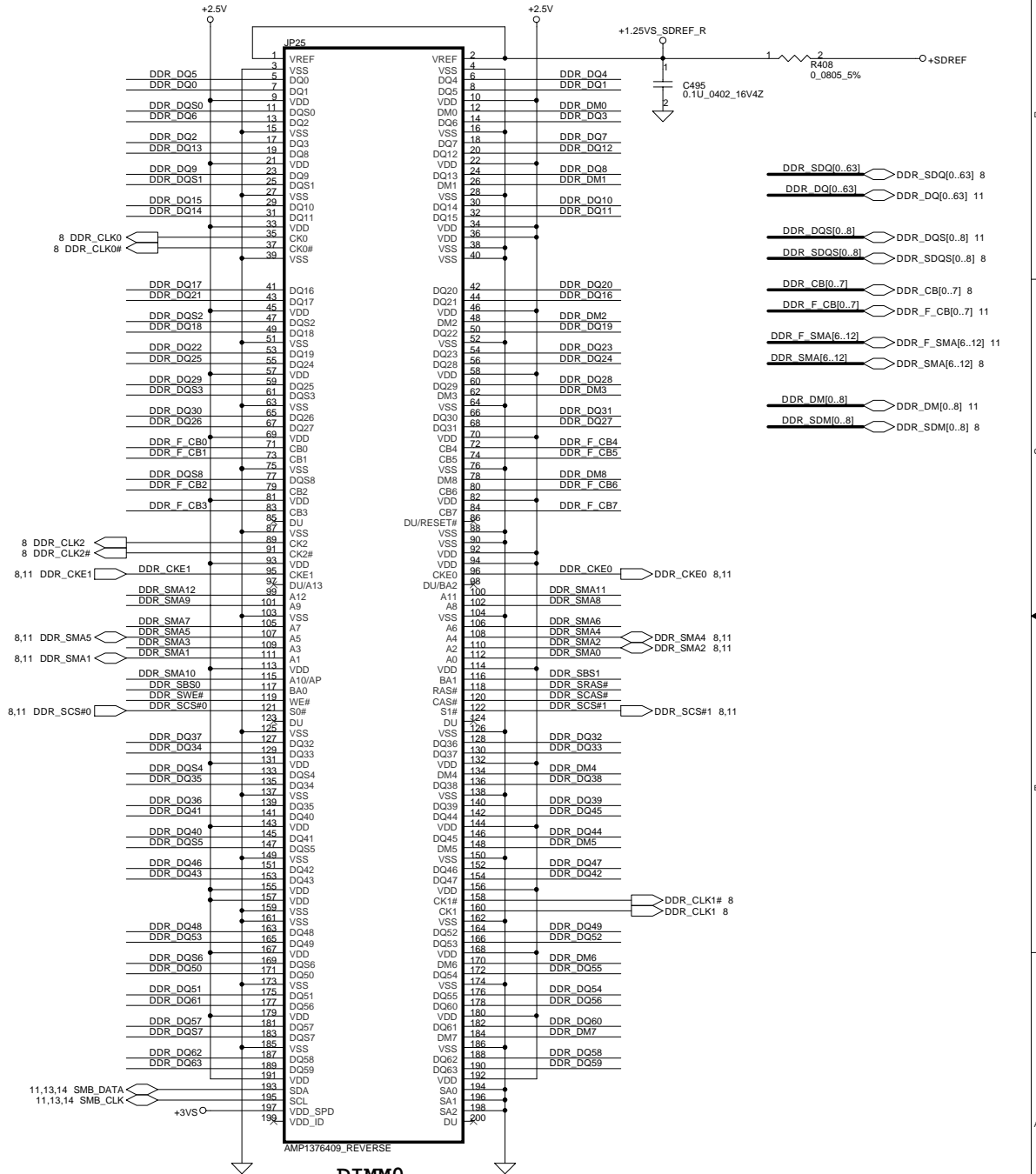
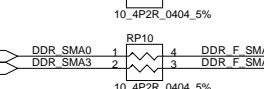
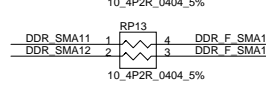
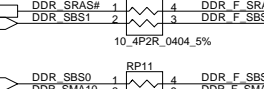
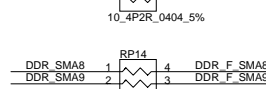
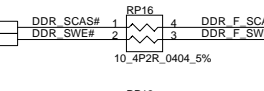
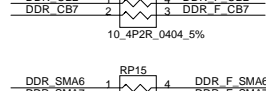
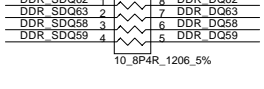
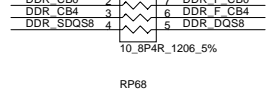
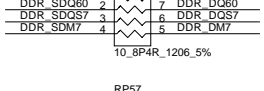
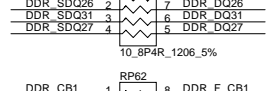
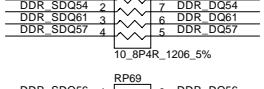
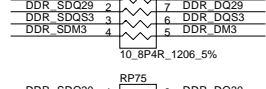
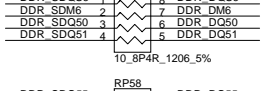
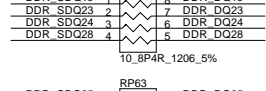
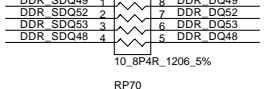
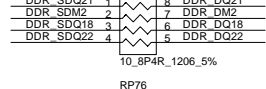
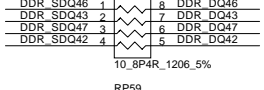
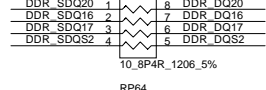
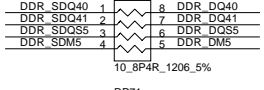
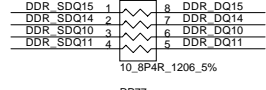
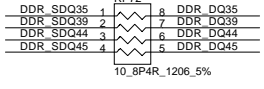
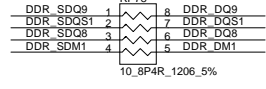
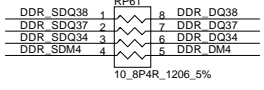
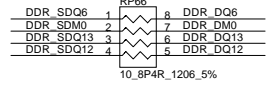
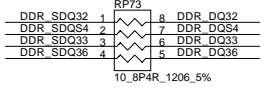
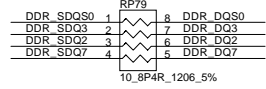
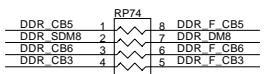
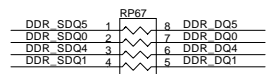
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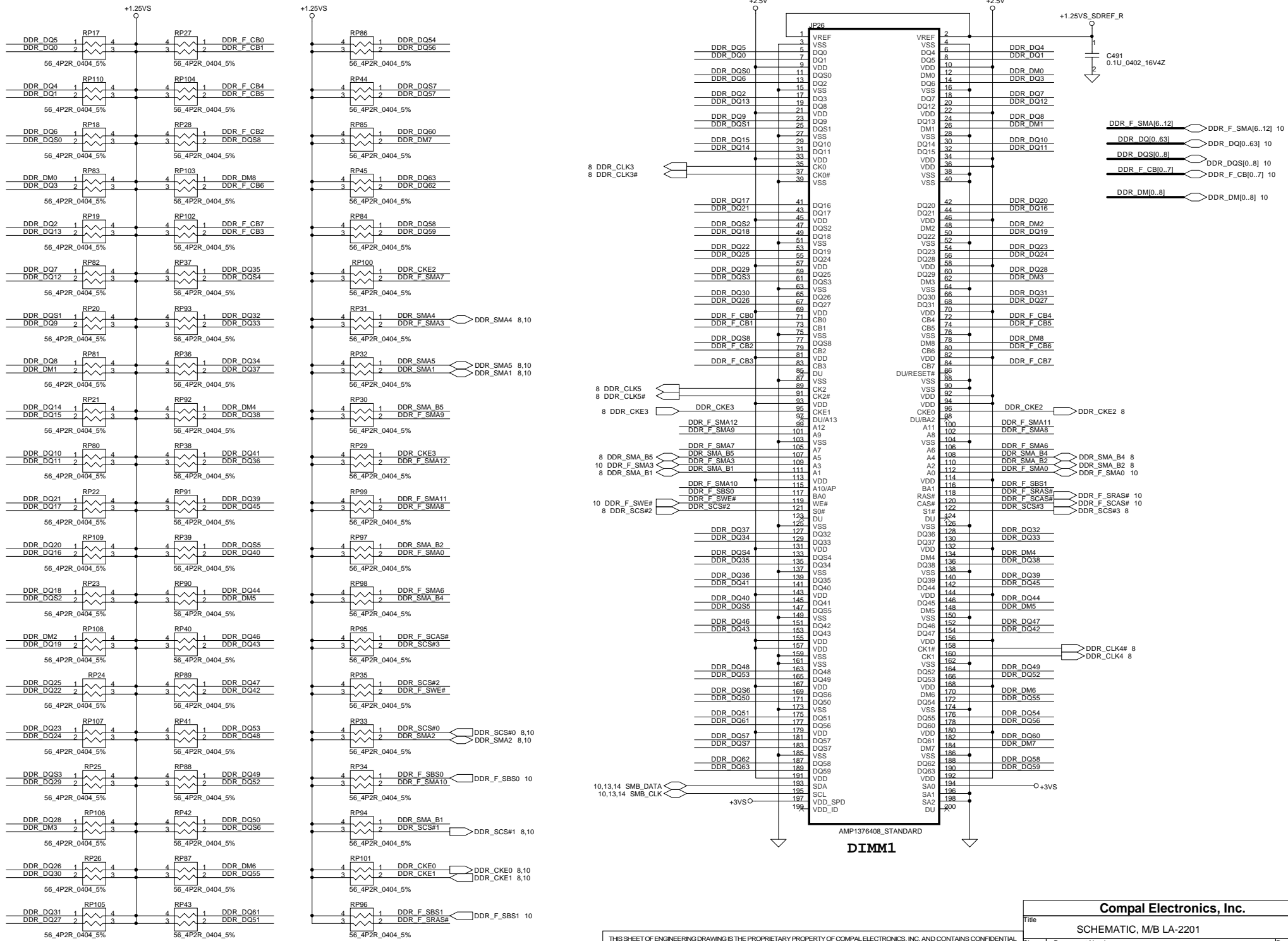


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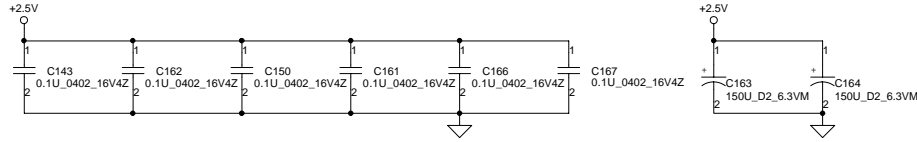
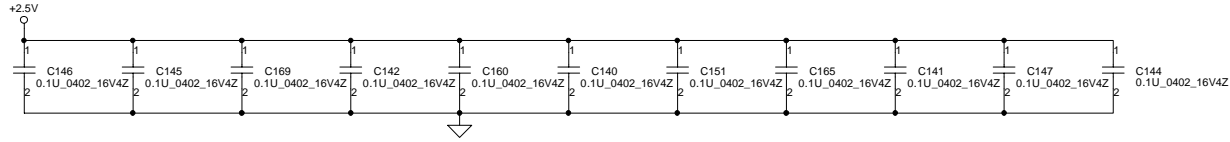
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- DDR DQ[0..63] ○ DDR_DQ[0..63] 10
- DDR DQS[0..8] ○ DDR_DQS[0..8] 10
- DDR F CB[0..7] ○ DDR_F_CB[0..7] 10
- DDR DM[0..8] ○ DDR_DM[0..8] 10

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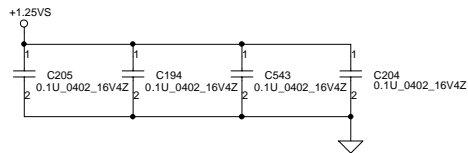
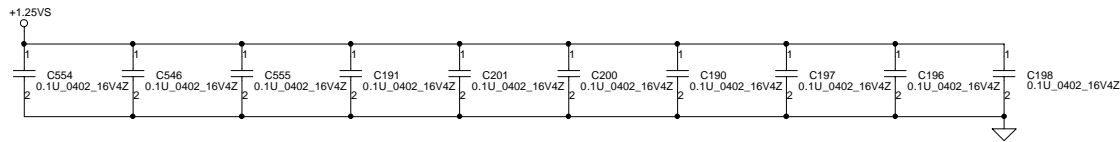
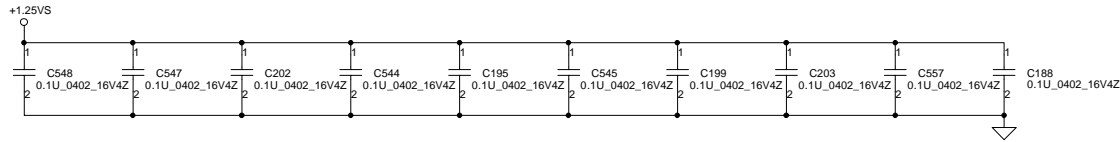
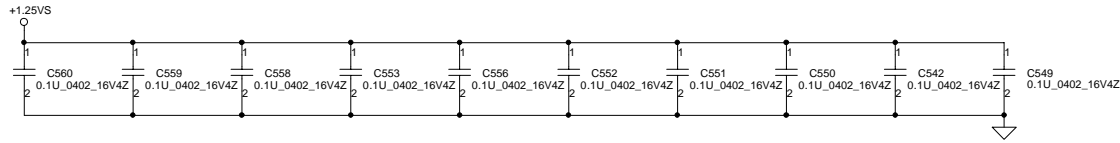
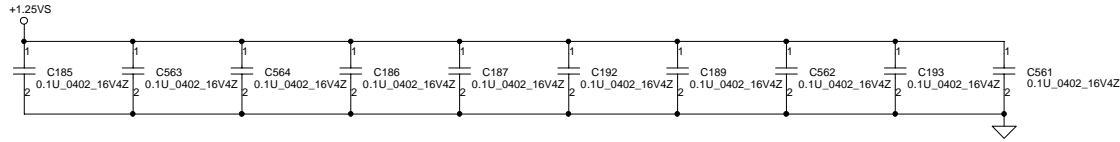
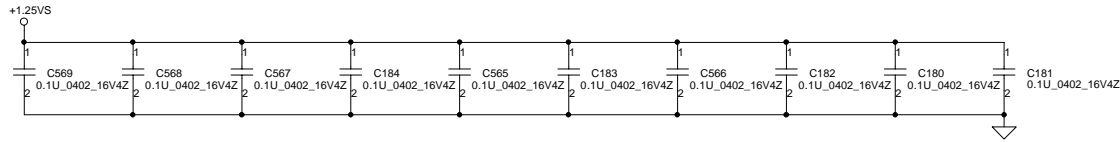
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



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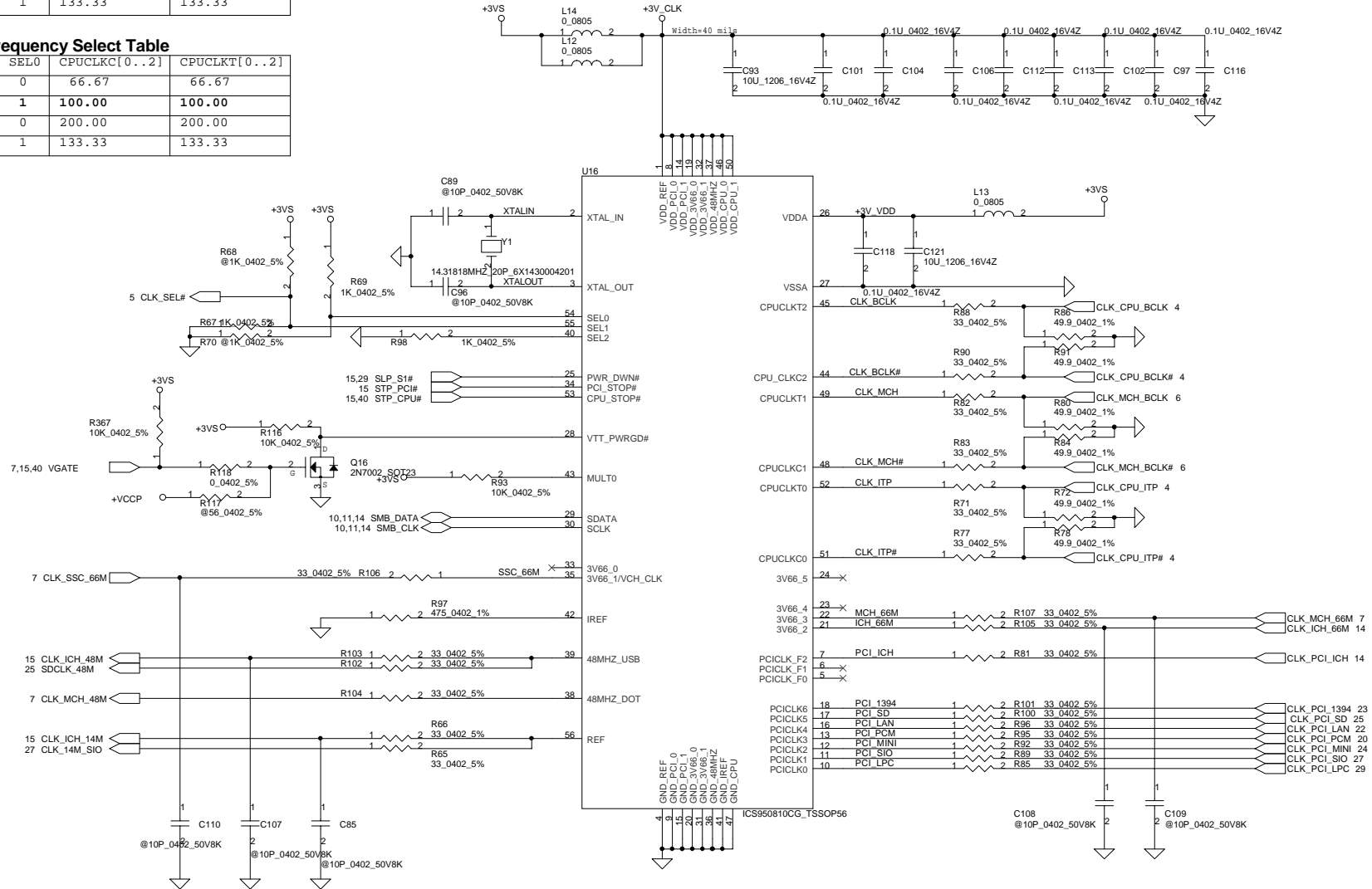
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ICS950810 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

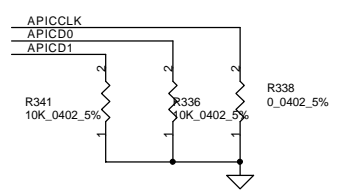
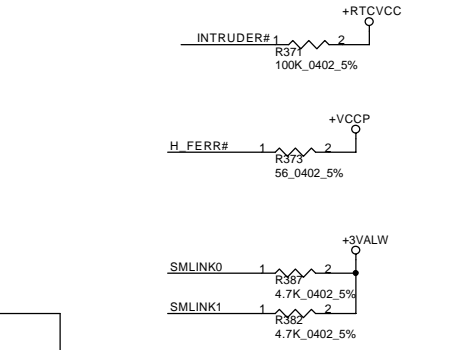
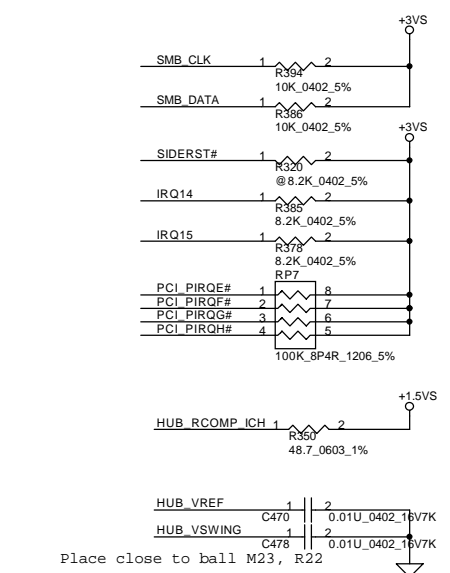
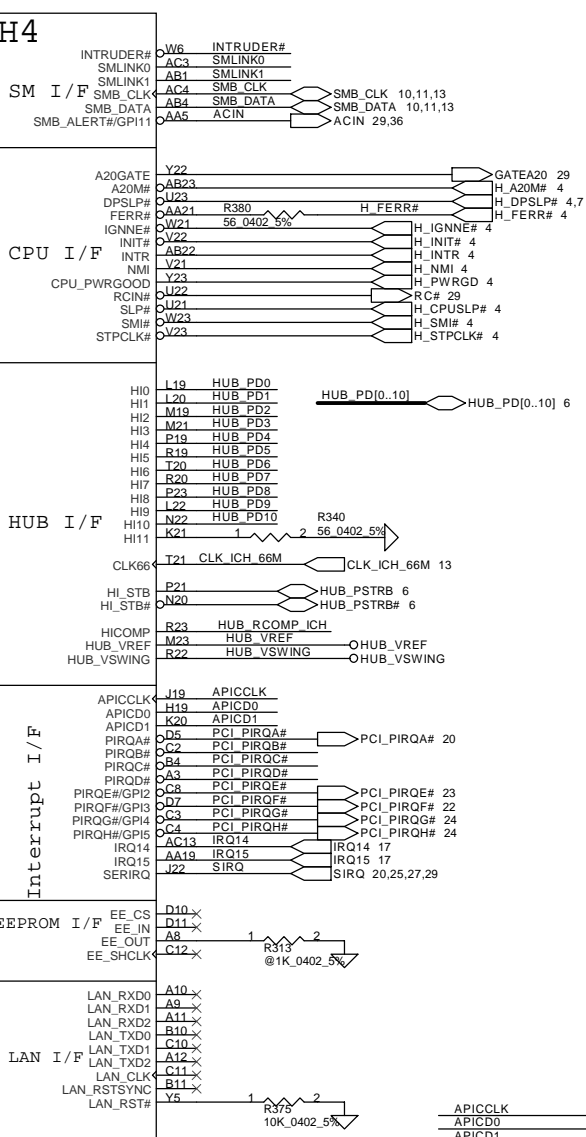
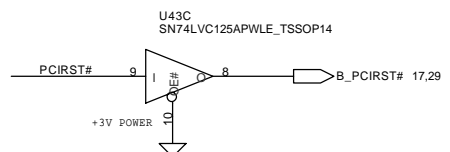
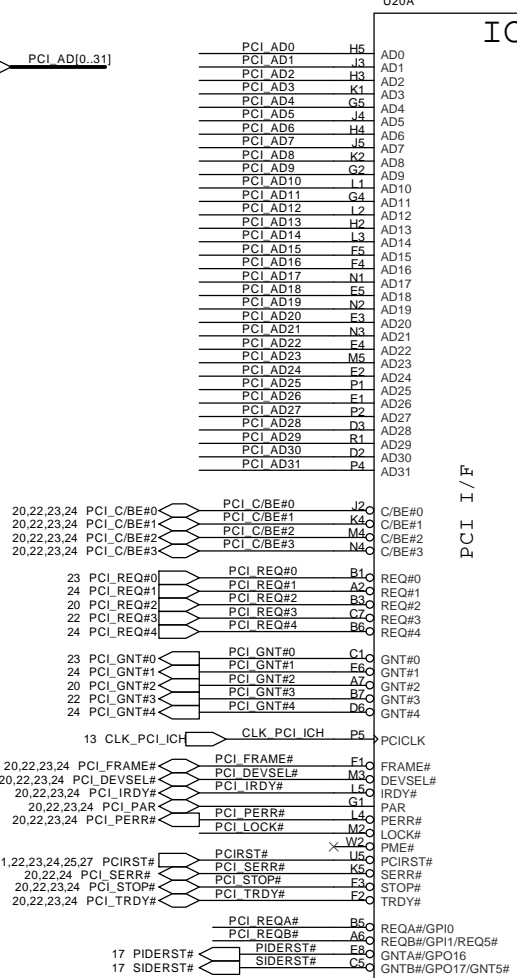
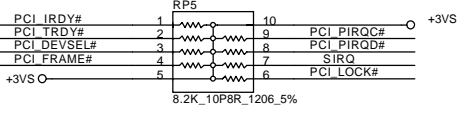
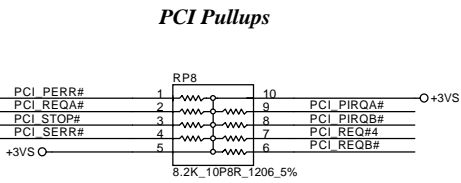
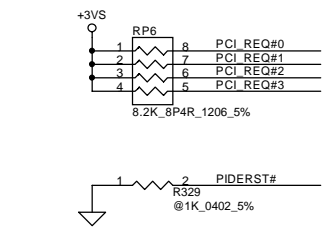
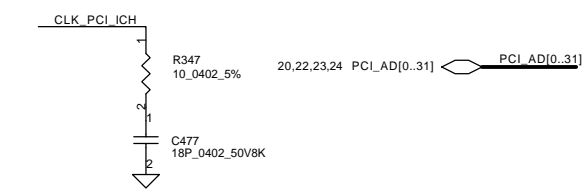
CY28346-2 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



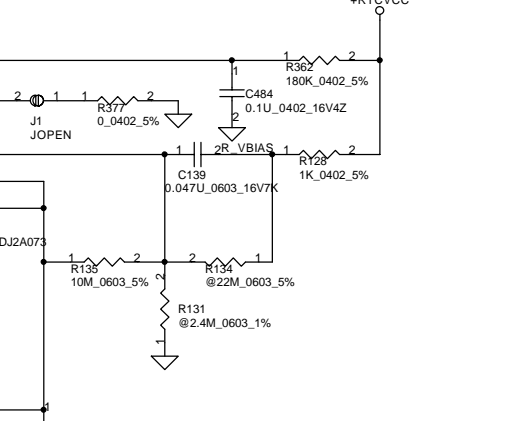
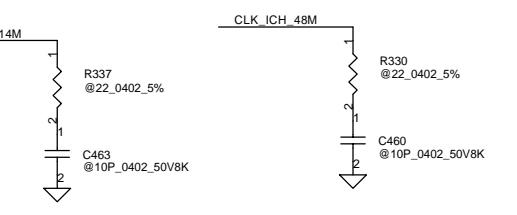
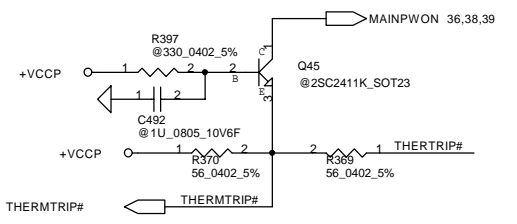
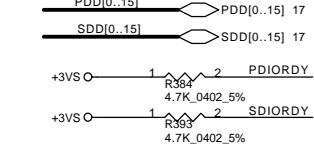
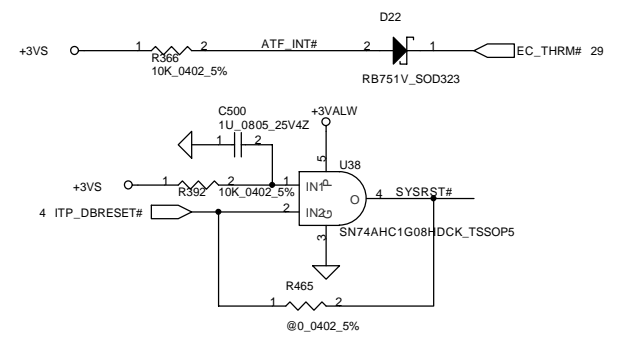
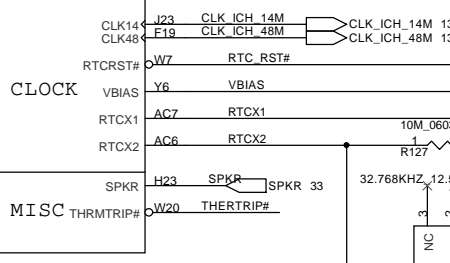
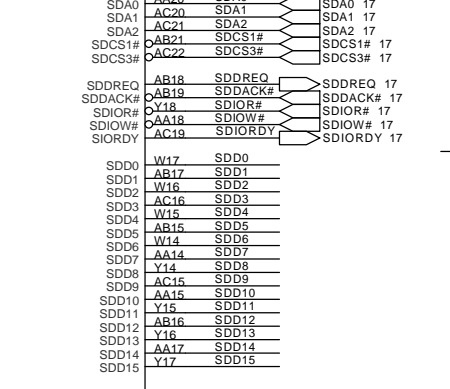
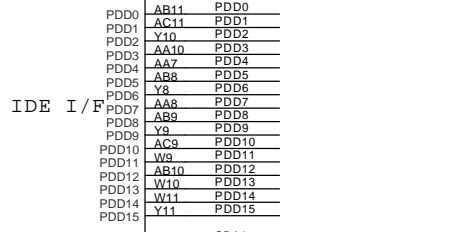
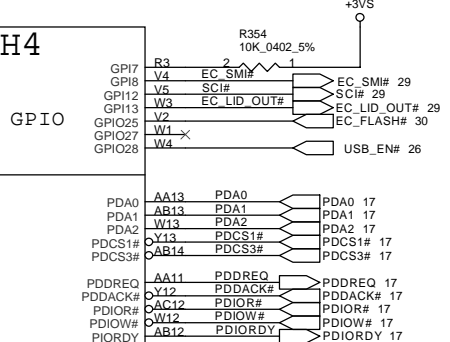
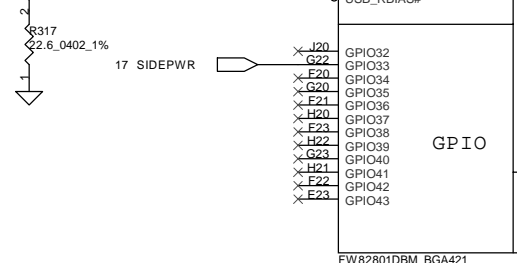
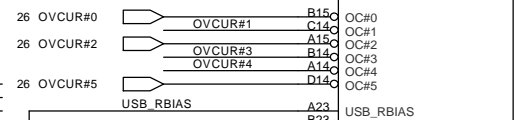
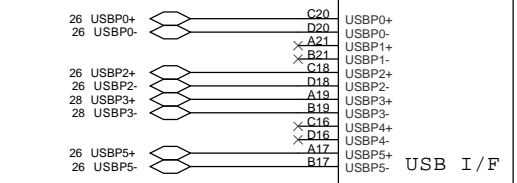
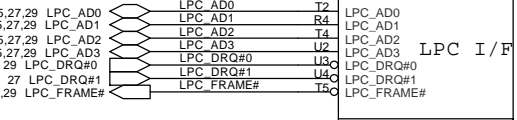
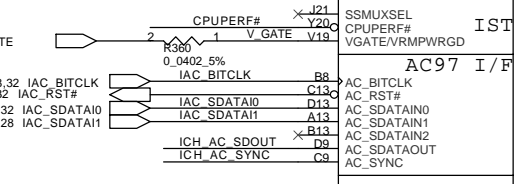
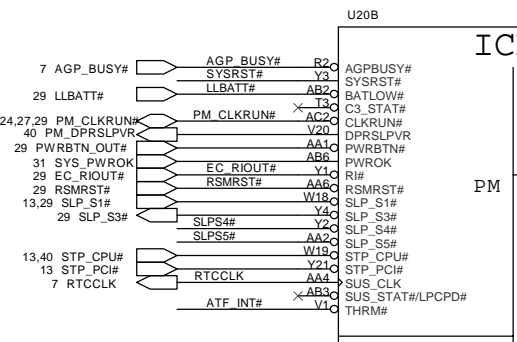
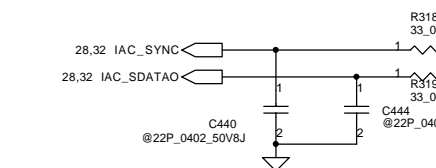
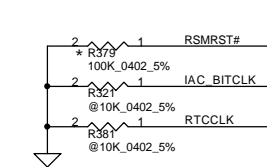
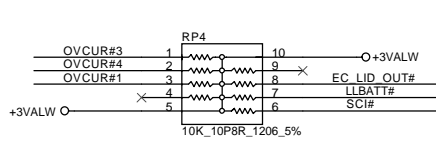
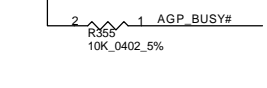
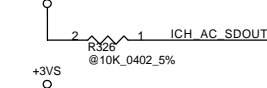
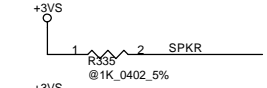
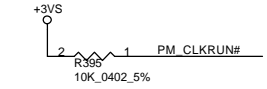
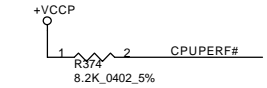
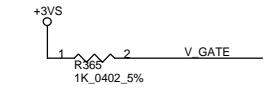
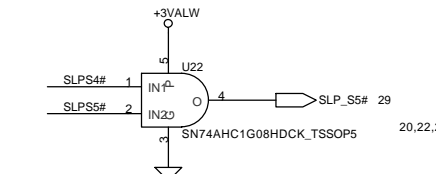
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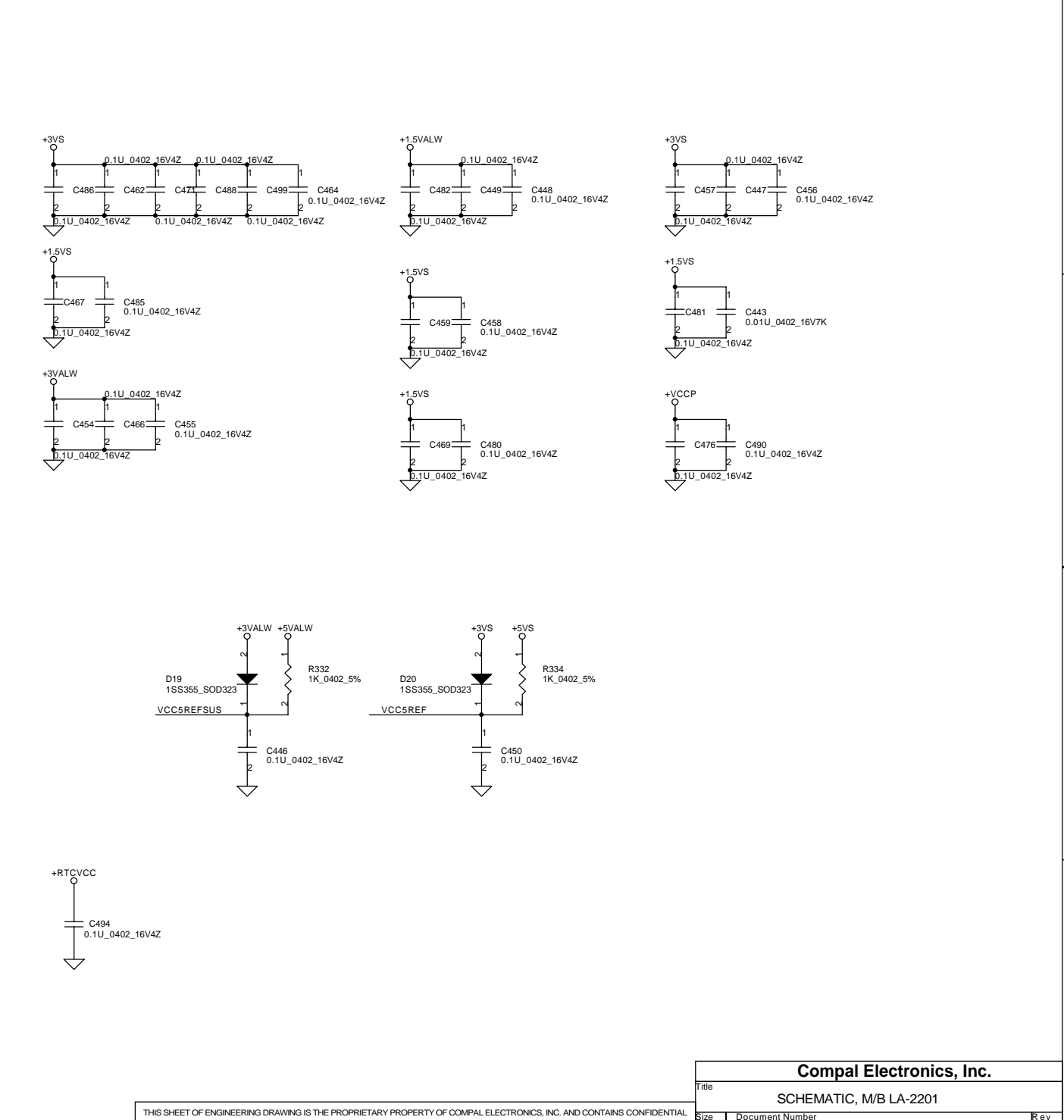
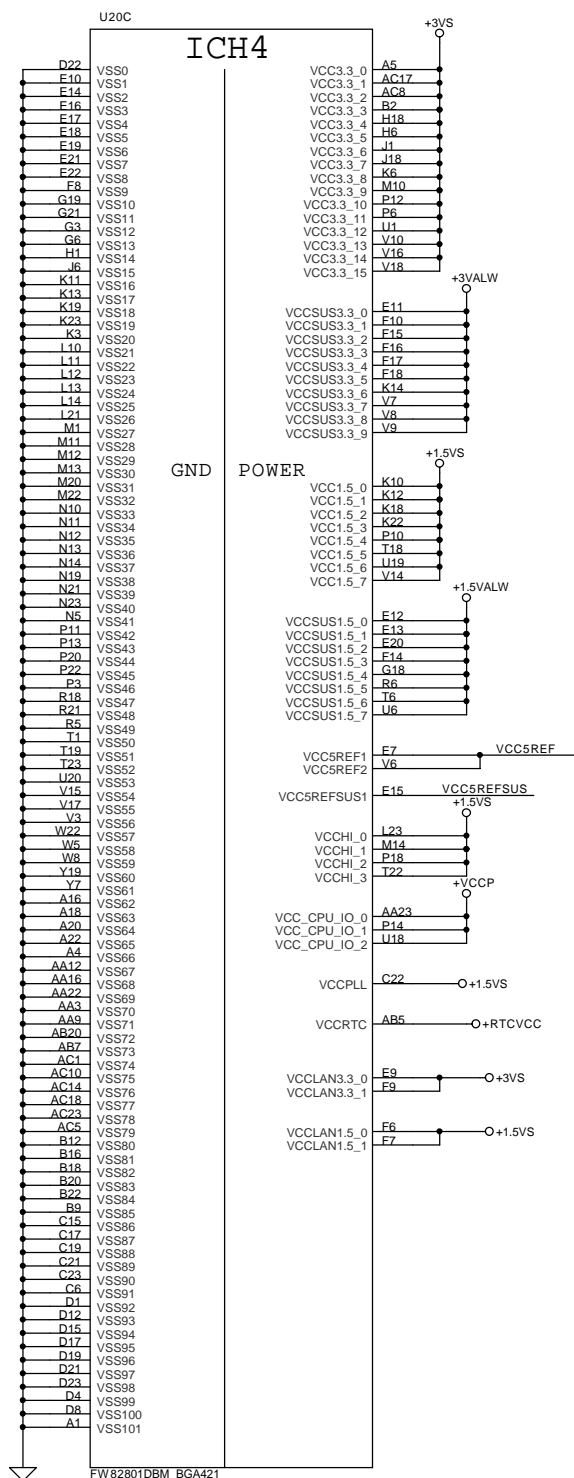
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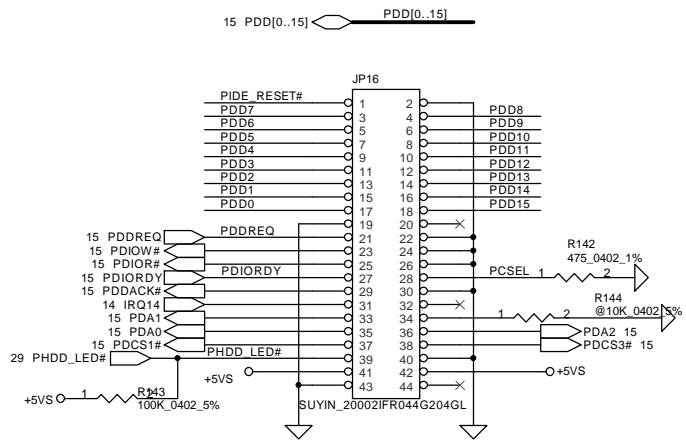
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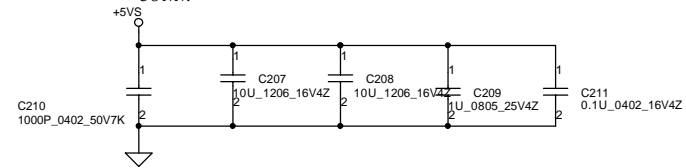
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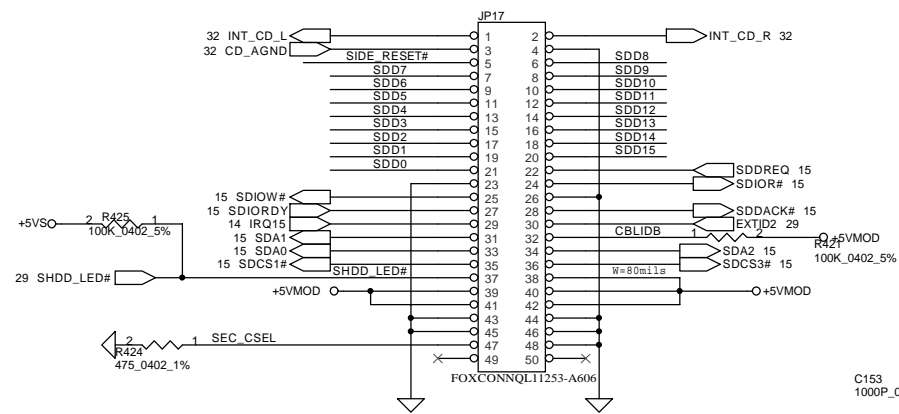
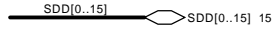
HDD Connector



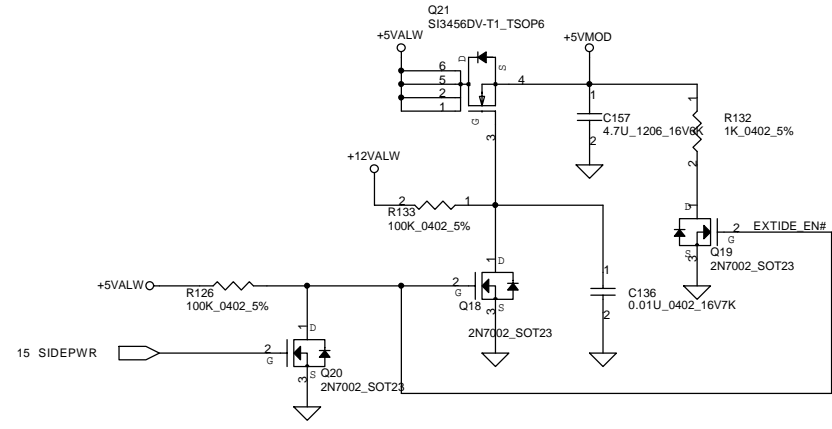
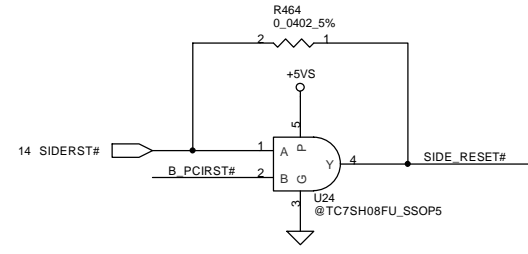
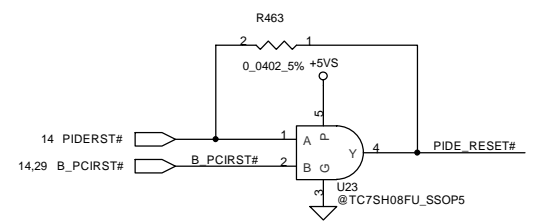
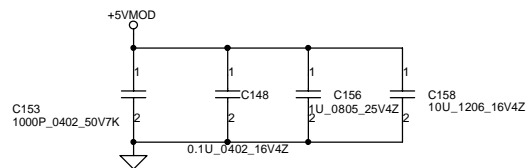
Placea caps. near HDD CONN.



CD-ROM Connector



Placea caps. near CDROM CONN.



SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

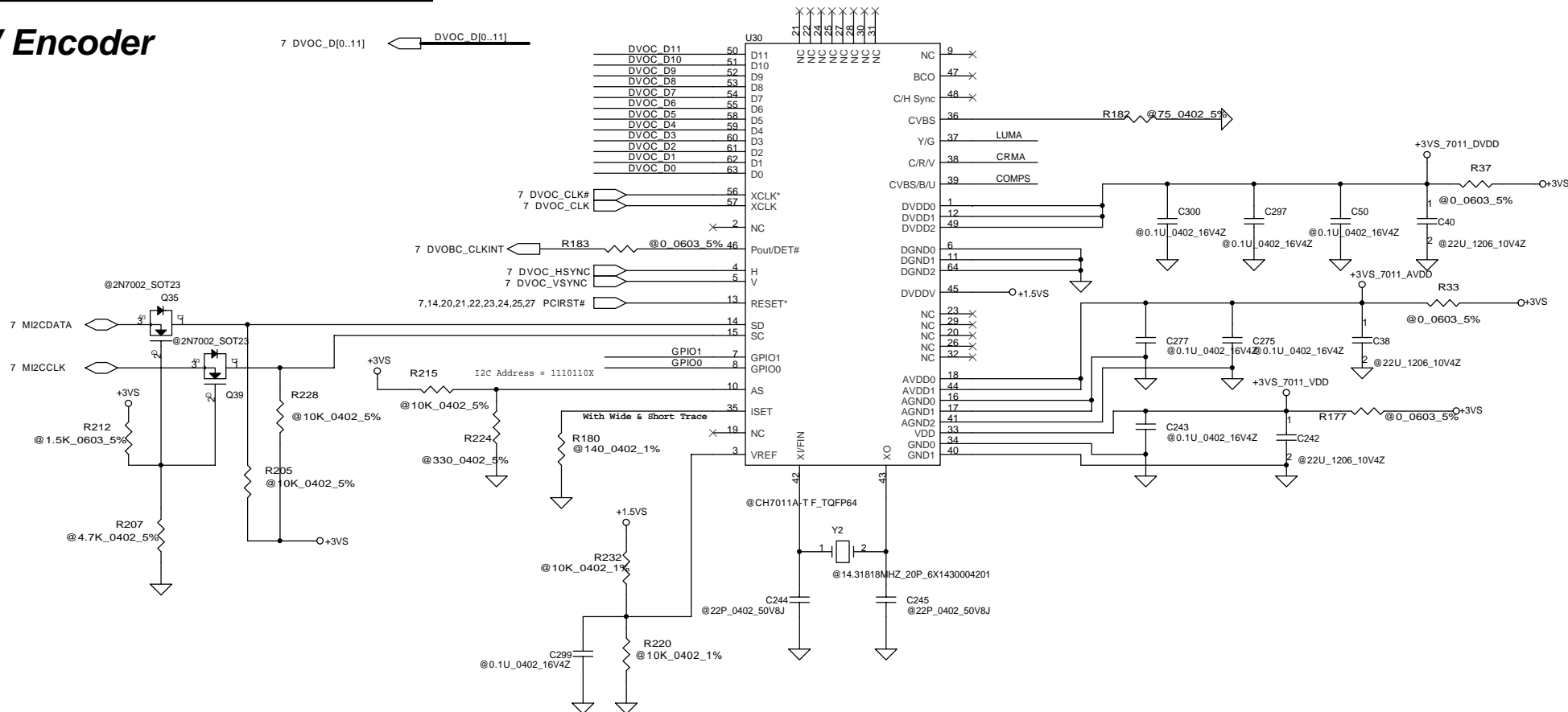
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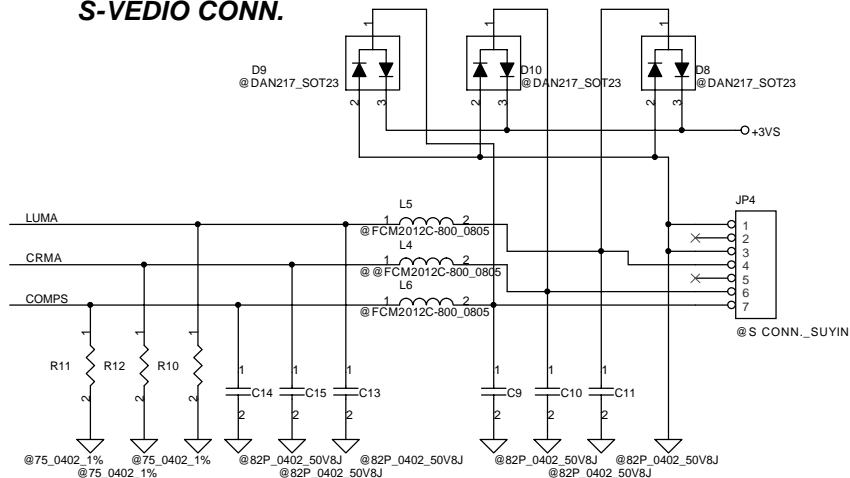
For ABO without TV_out:all this page component unmount

TV Encoder

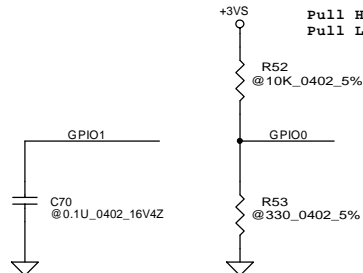
7 DVOC_D[0..11] ← DVOC_D[0..11]



S-VIDEO CONN.



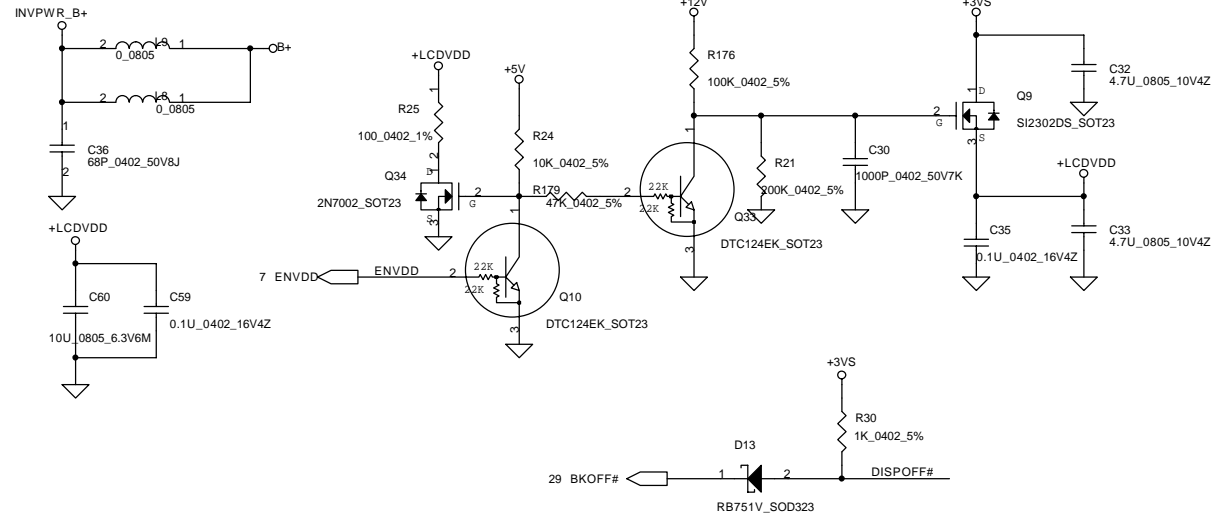
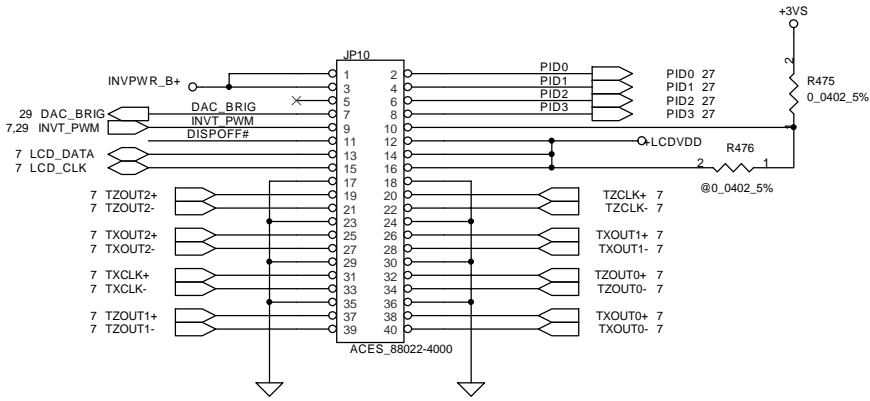
Pull High: Default PAL
Pull Low: Default NTSC



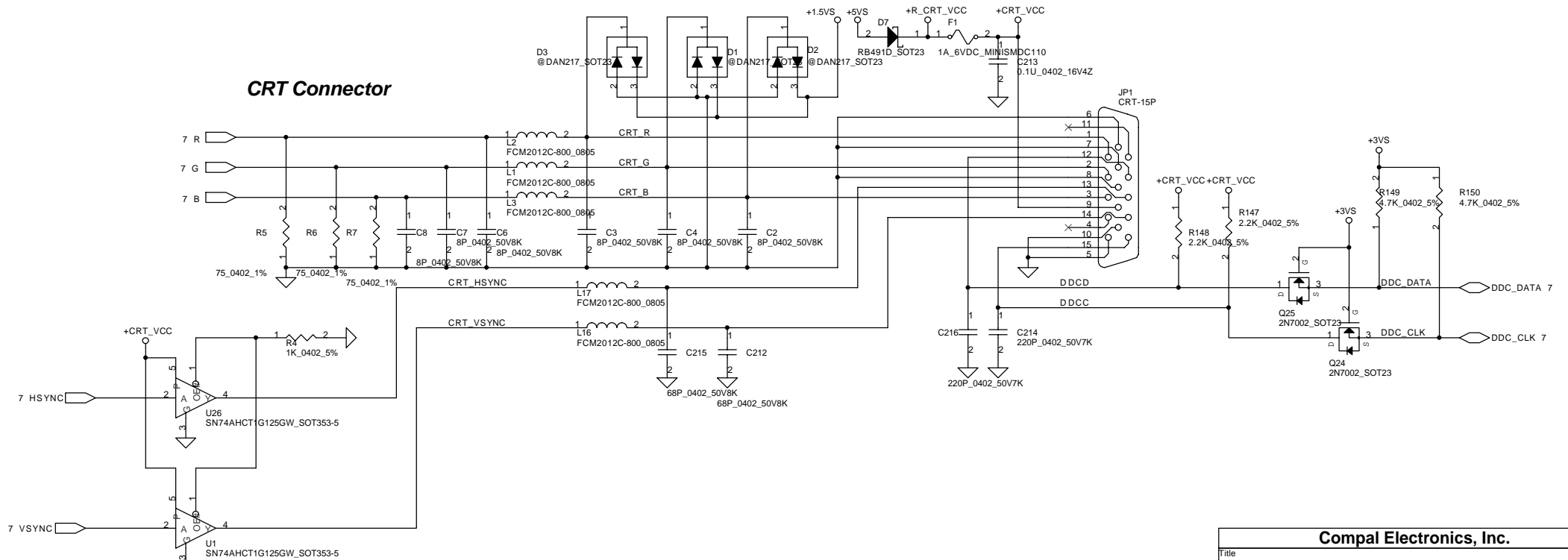
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LVDS Connector

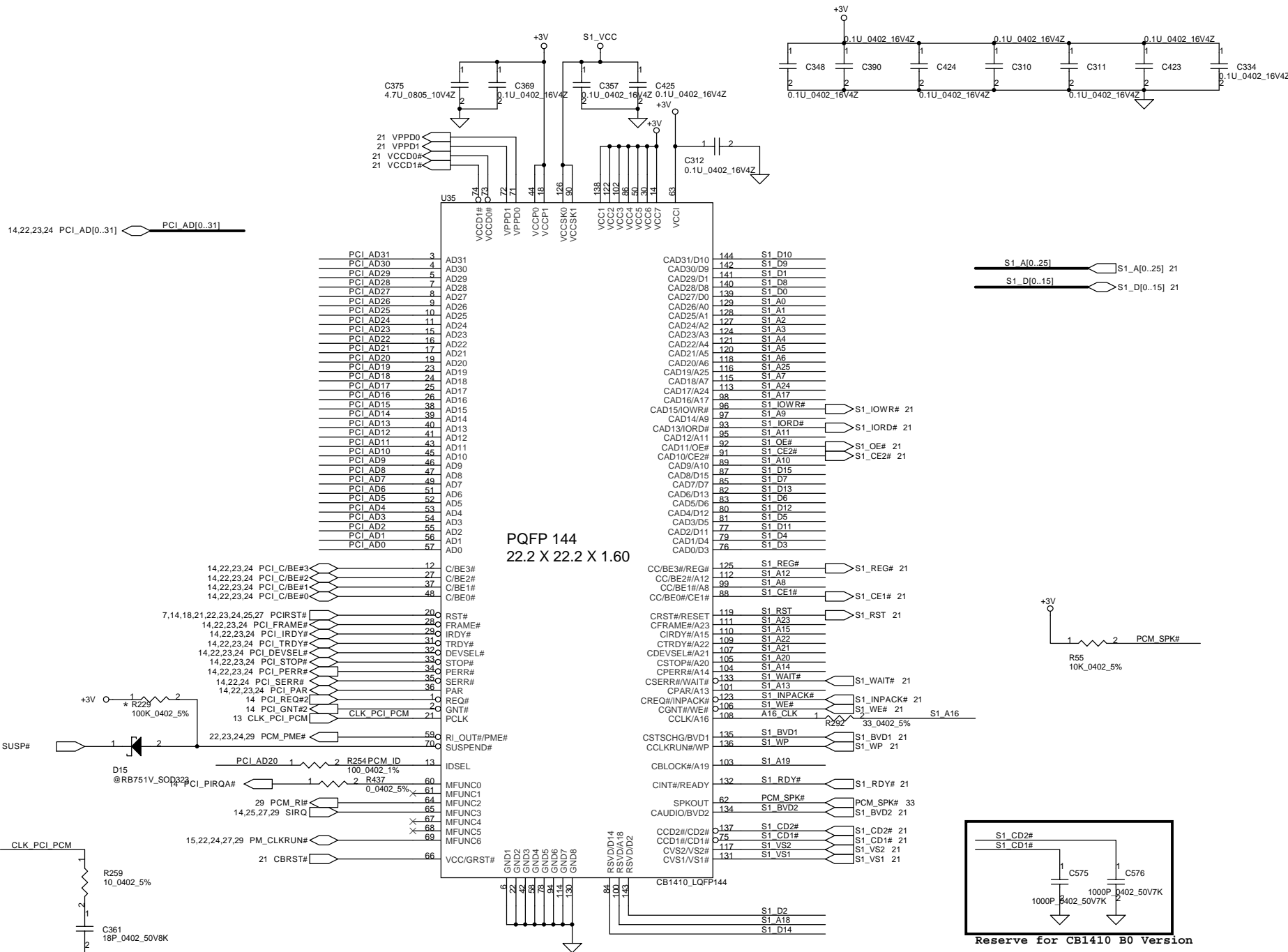


CRT Connector

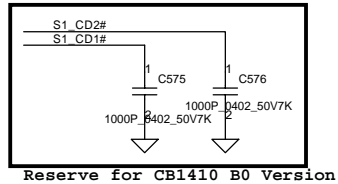


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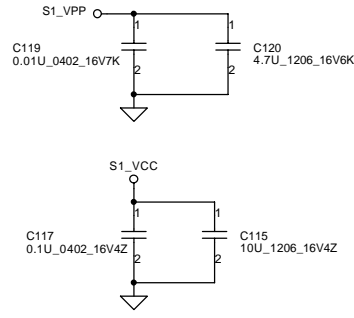
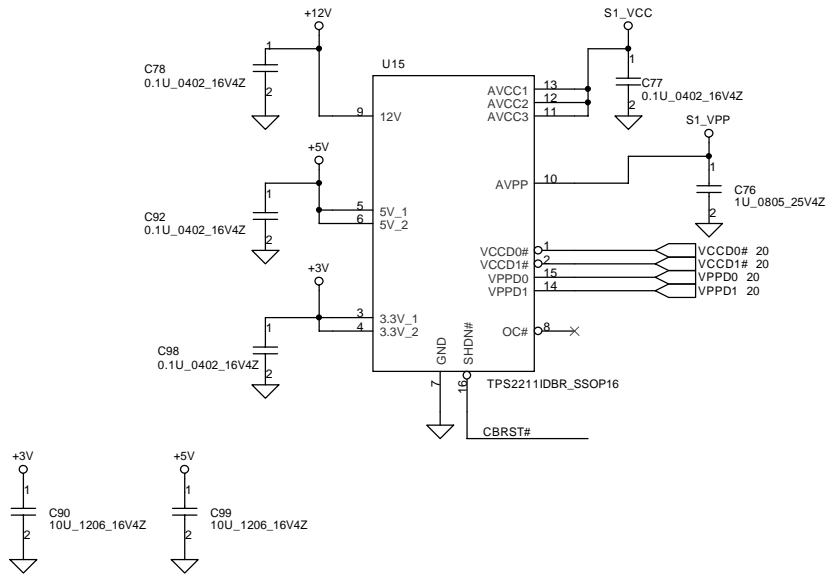
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22.2 X 22.2 X 1.60



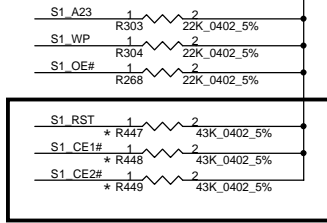
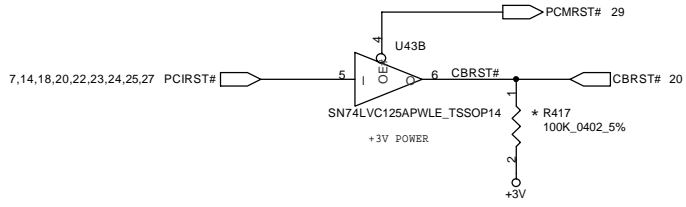
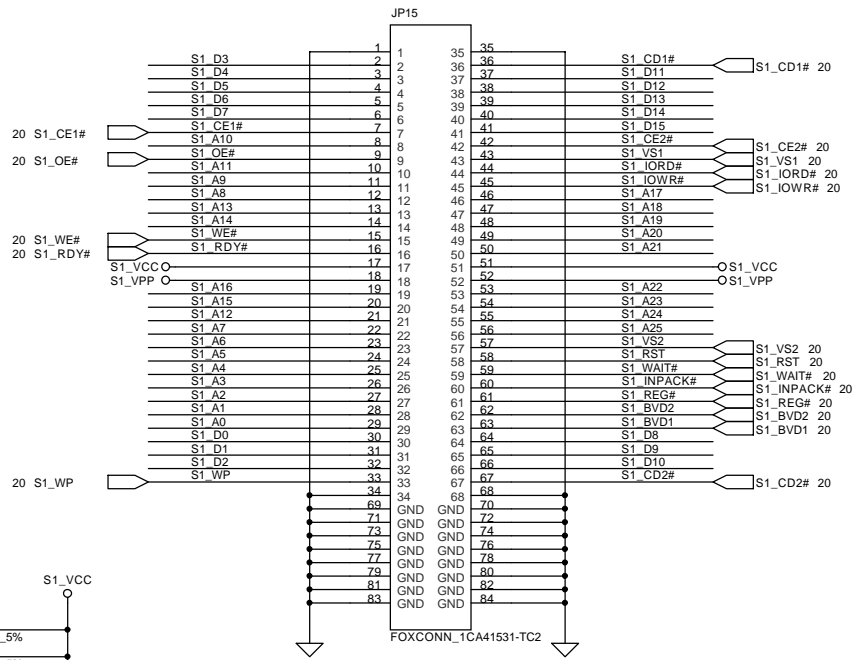
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PCMCIA Power Controller



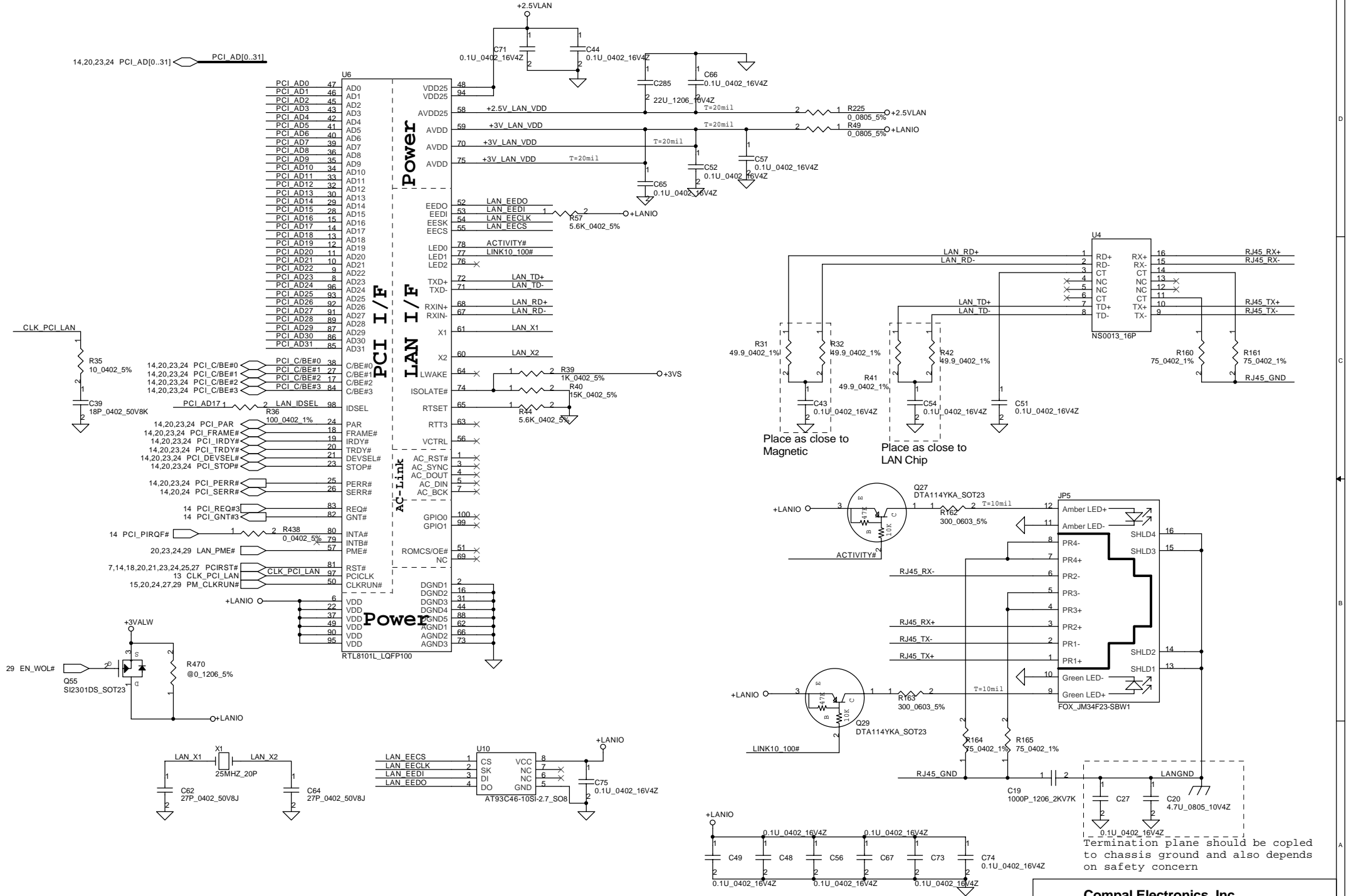
CardBus Socket



Reserve for CB1410 B0 Version

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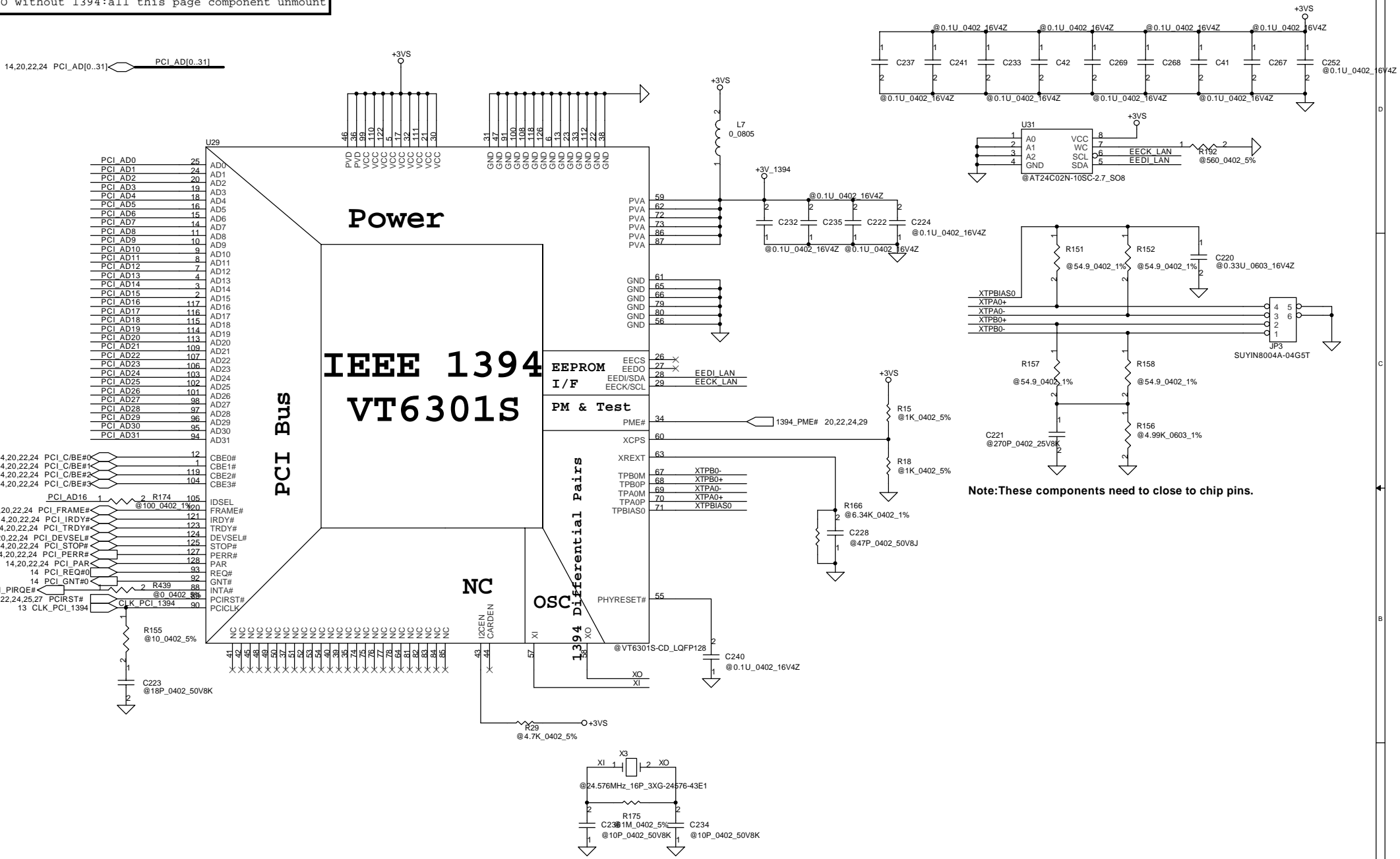
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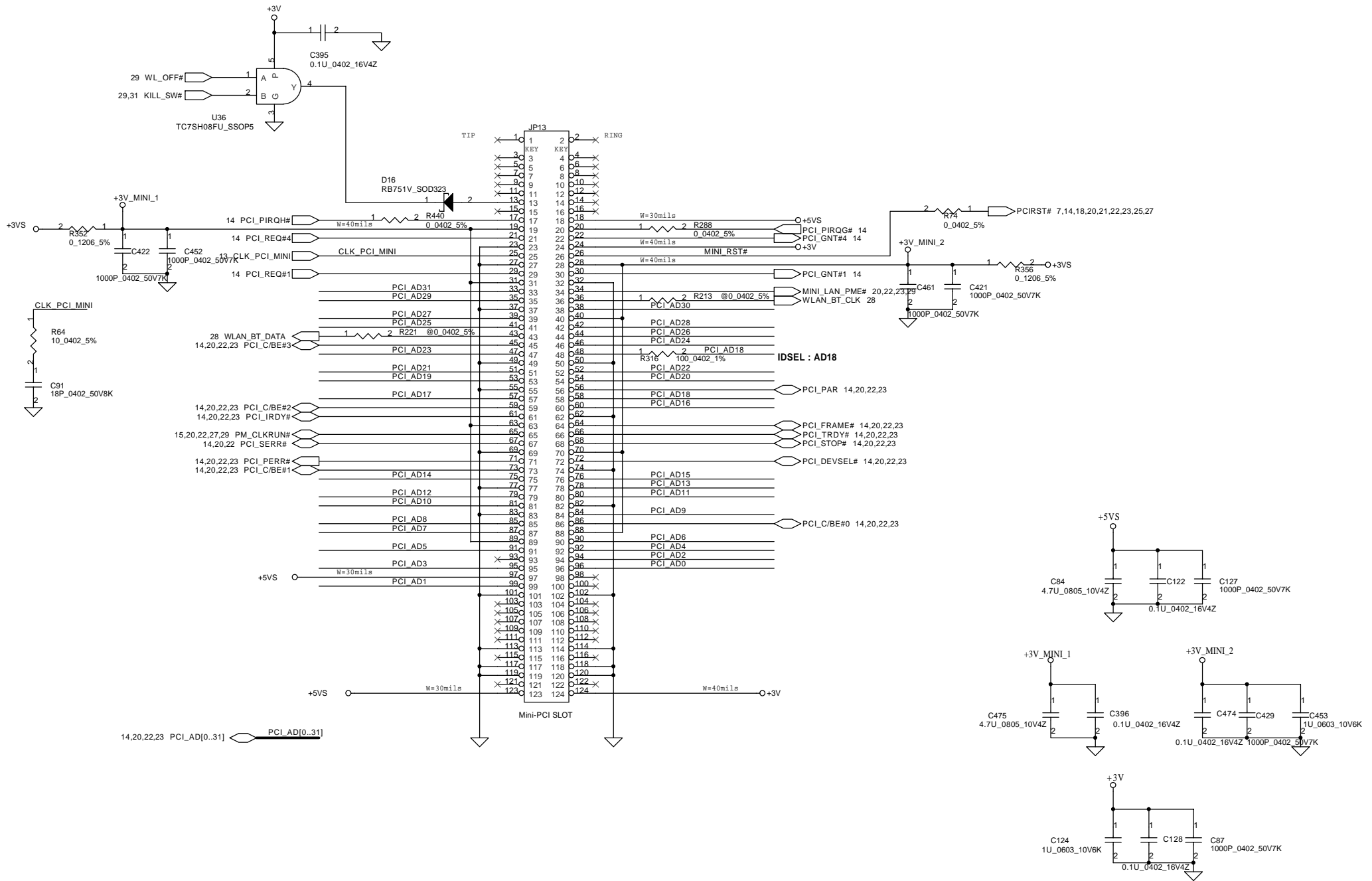
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For ABO without 1394:all this page component unmount



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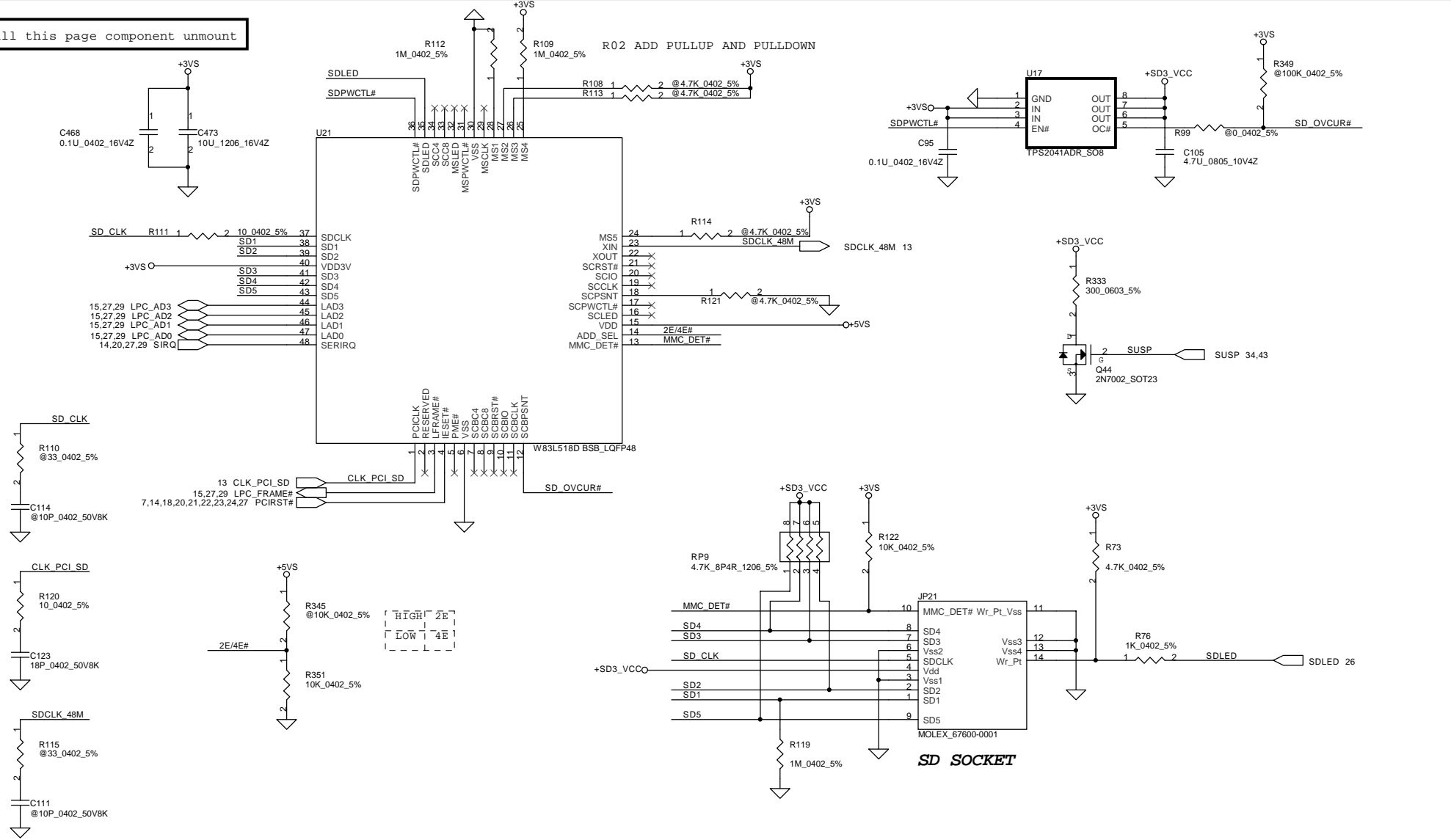
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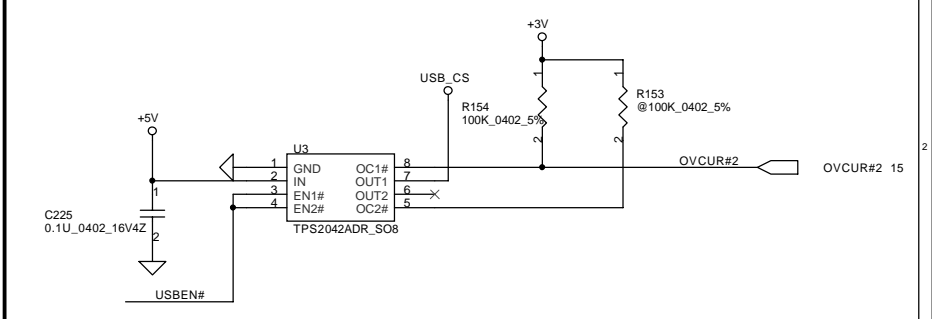
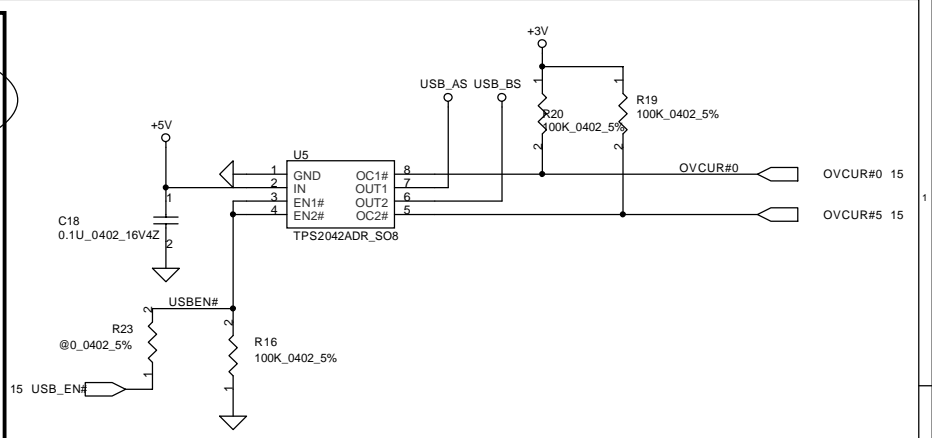
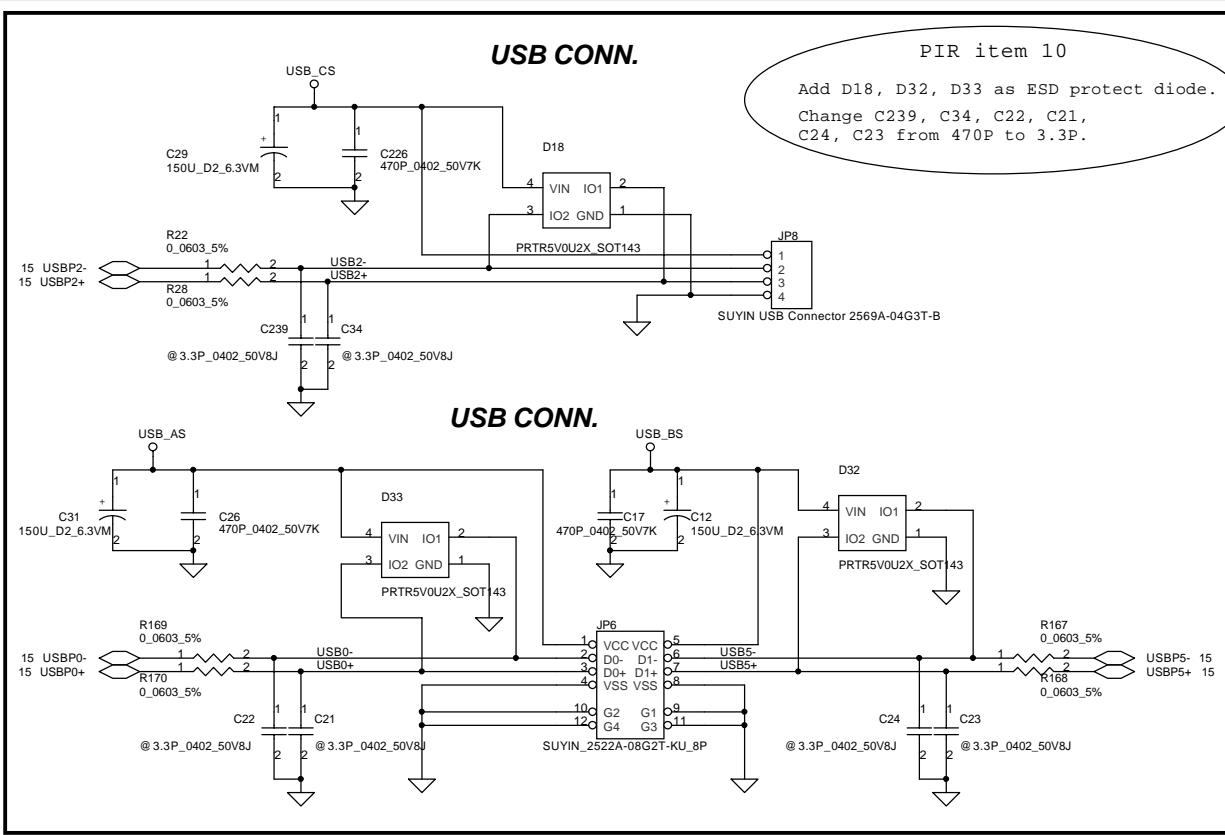
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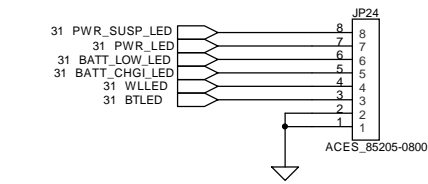
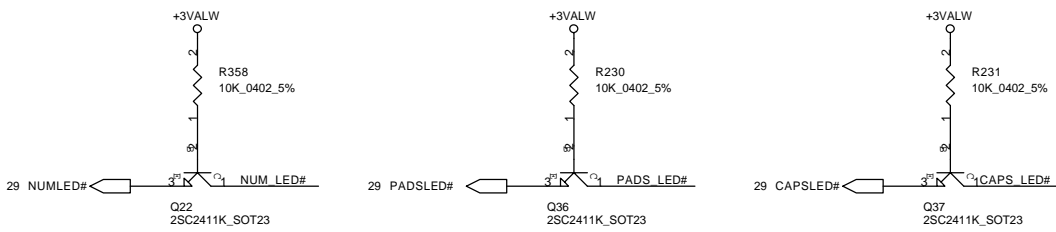


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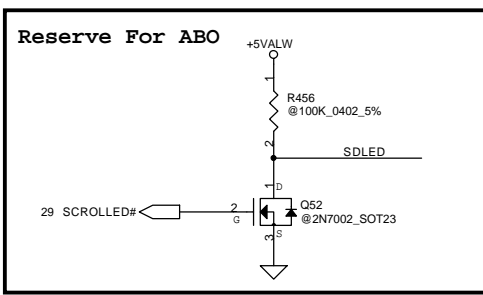
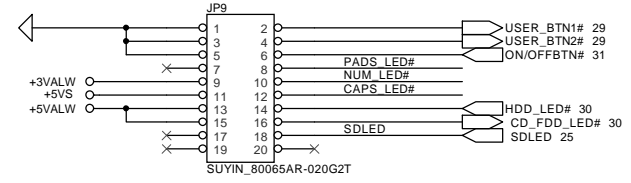
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LED/B CONN.



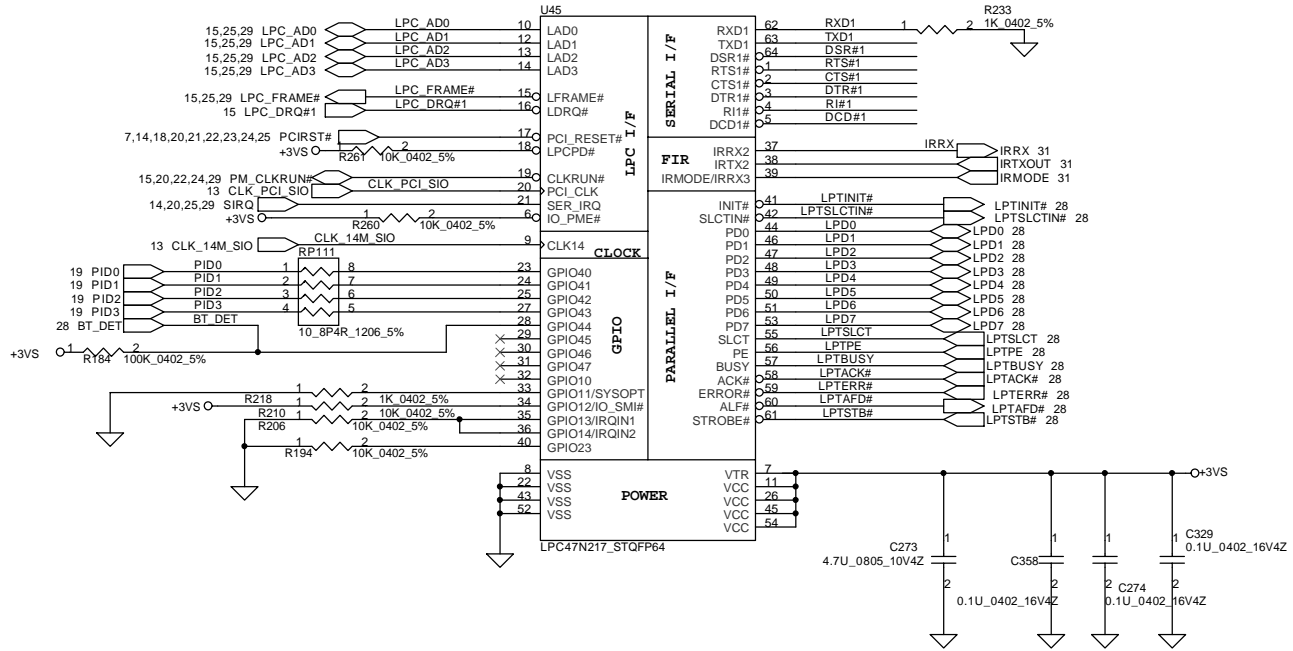
POWER/B CONN.



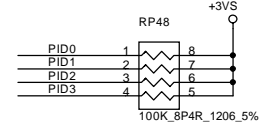
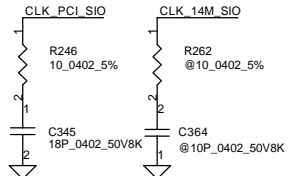
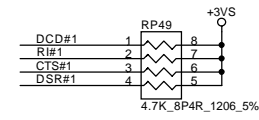
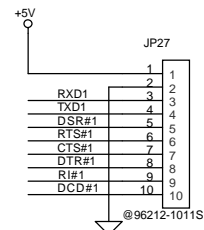
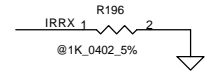
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SUPER I/O SMC FDC47N227



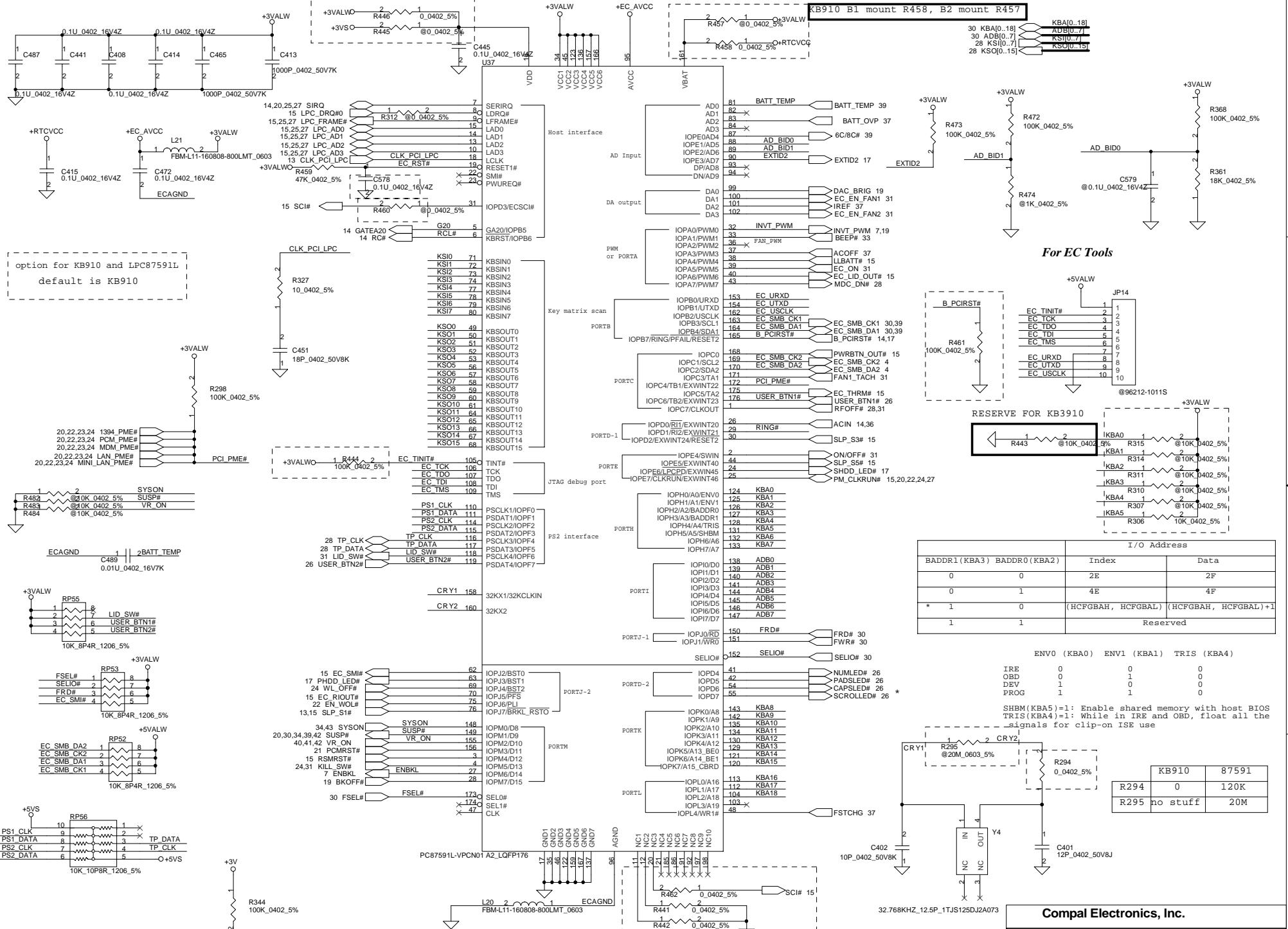
Base I/O Address
 * 0 = 02Eh
 1 = 04Eh



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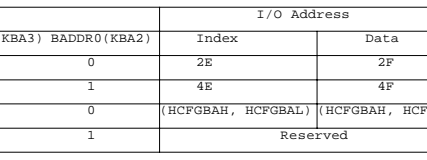
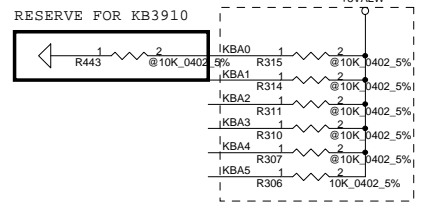
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option for KB910 and LPC87591L
default is KB910

For EC Tools



I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
1	1	Reserved	

ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE 0	NUMLED# 26	0
OBD 0	PADSLED# 26	1
DEV 1	CAPSLED# 26	0
PROG 1	SCROLLED# 26	1

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

	KB910	87591
R294	0	120K
R295	no stuff	20M

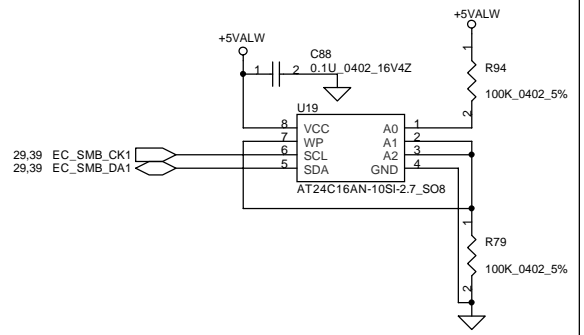
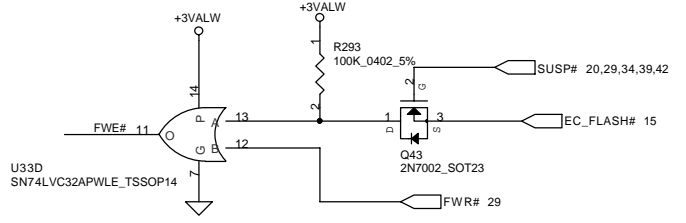
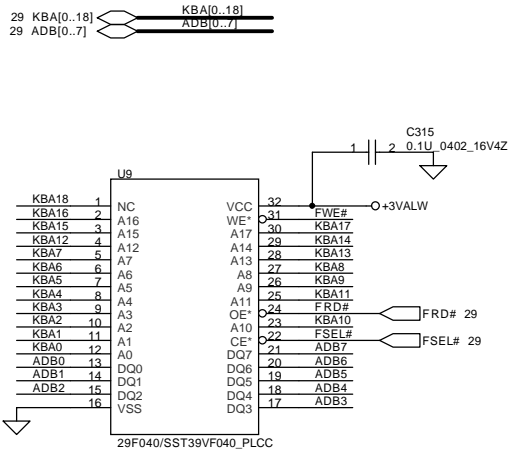
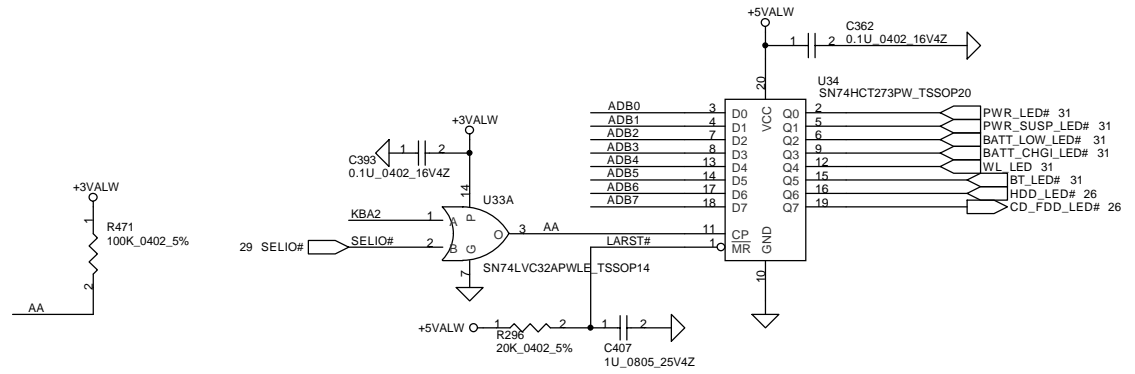
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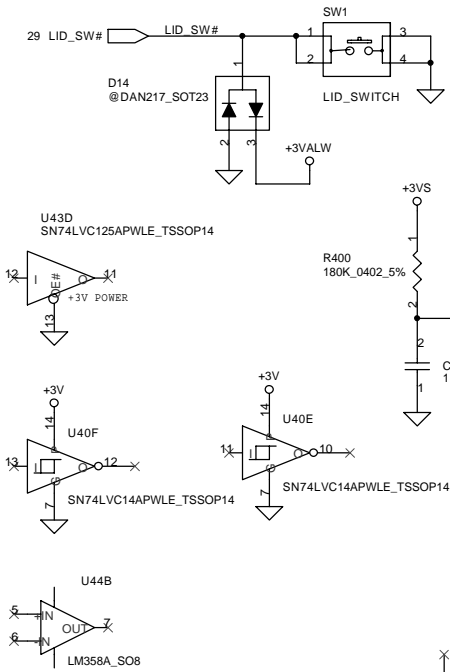
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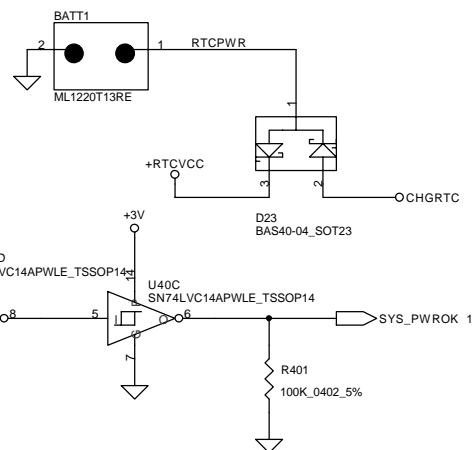
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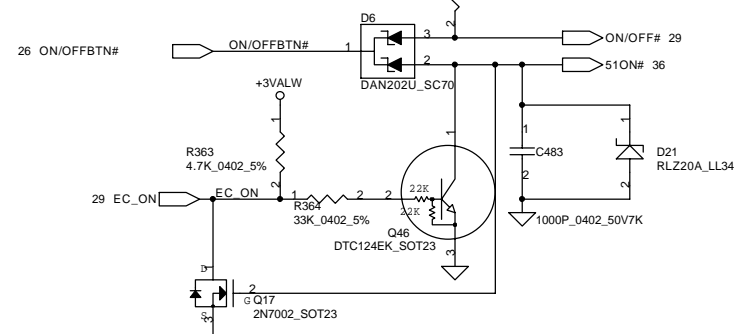
Power ON Circuit



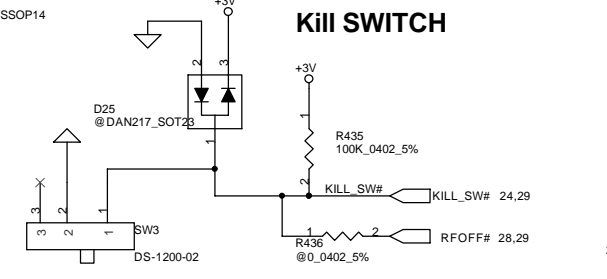
RTC Battery



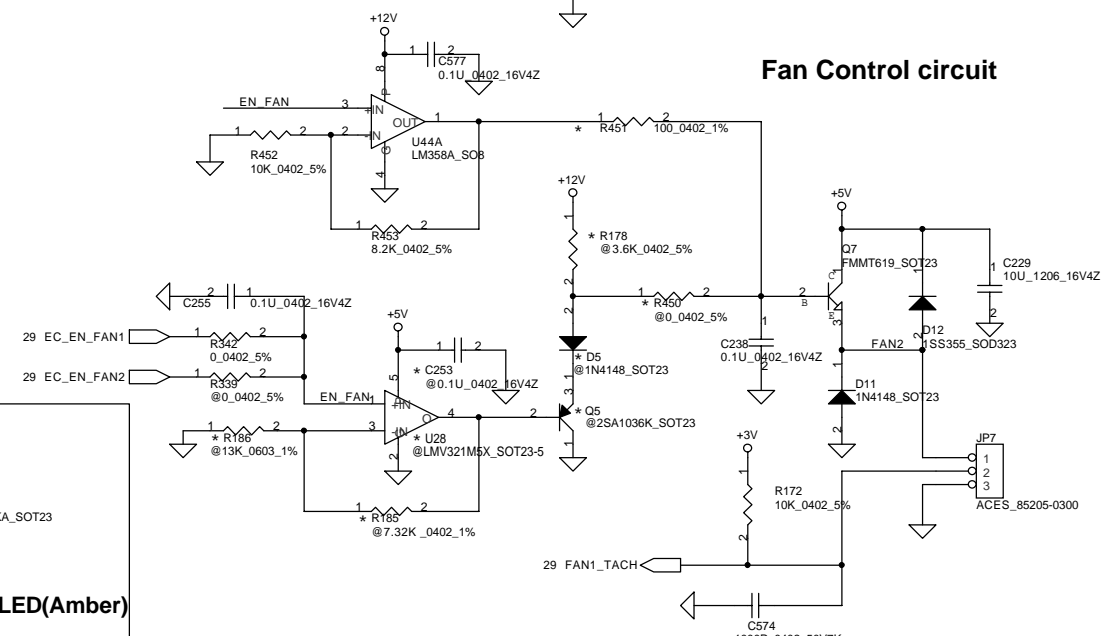
Power BTN



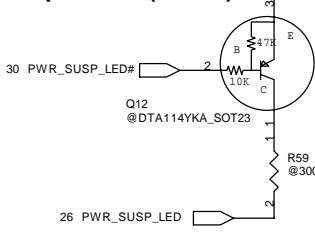
Kill SWITCH



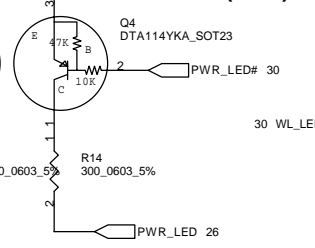
Fan Control circuit



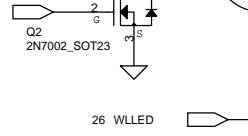
Suspend LED(Amber)



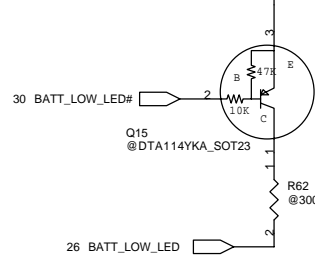
Power LED(Blue)



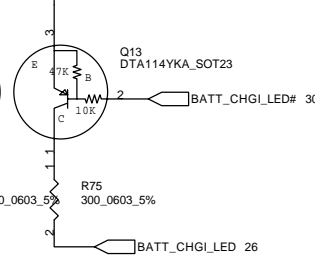
Wireless LED(Amber)



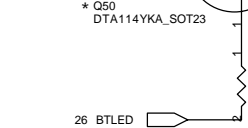
BATT Low LED(Amber)



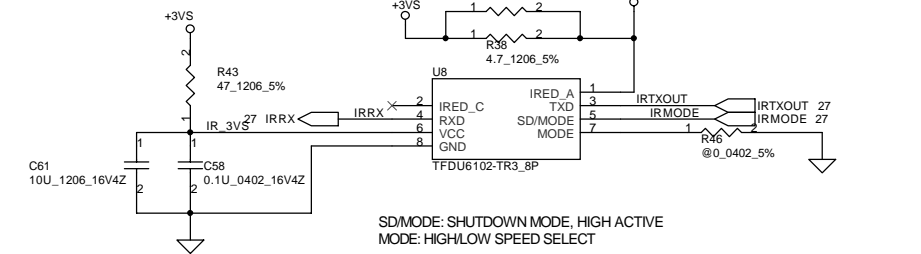
BATT Charge LED(Blue)



Bluetooth LED(Blue)



FIR Module

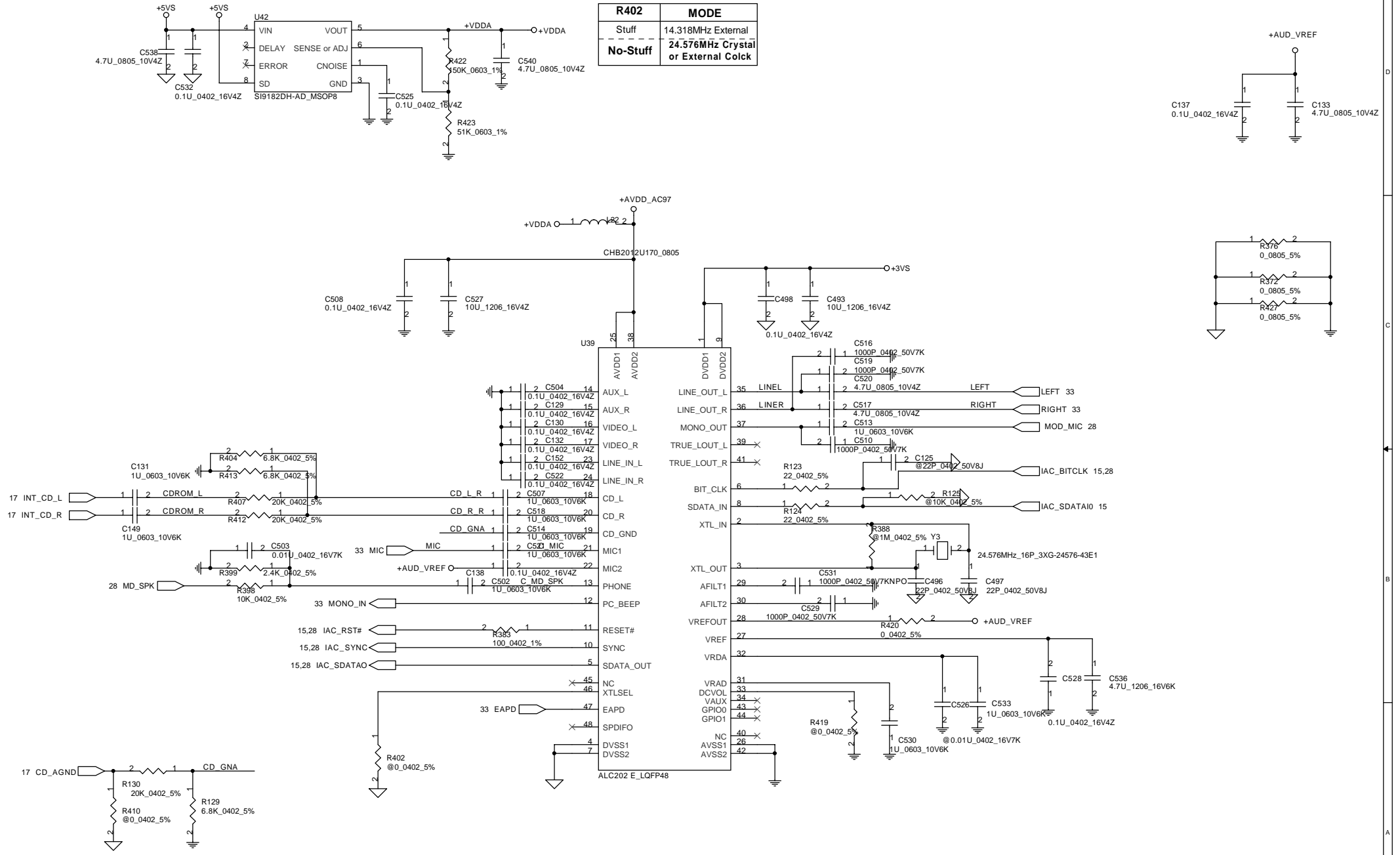


SD/MODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT

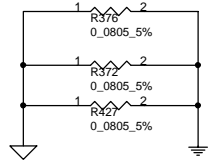
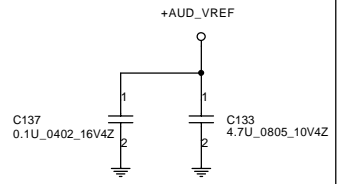
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AC97 Codec



R402	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck



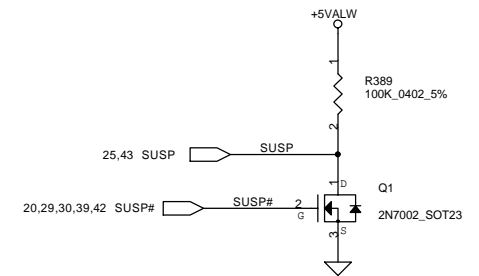
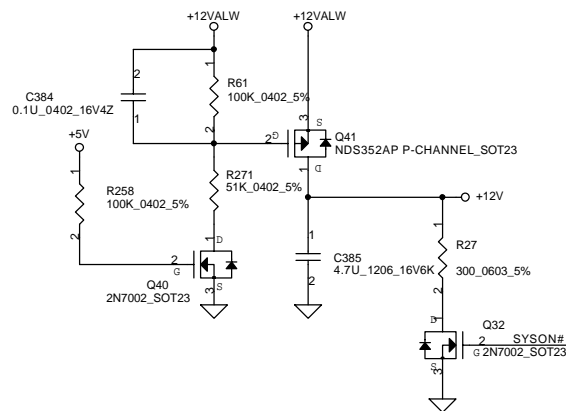
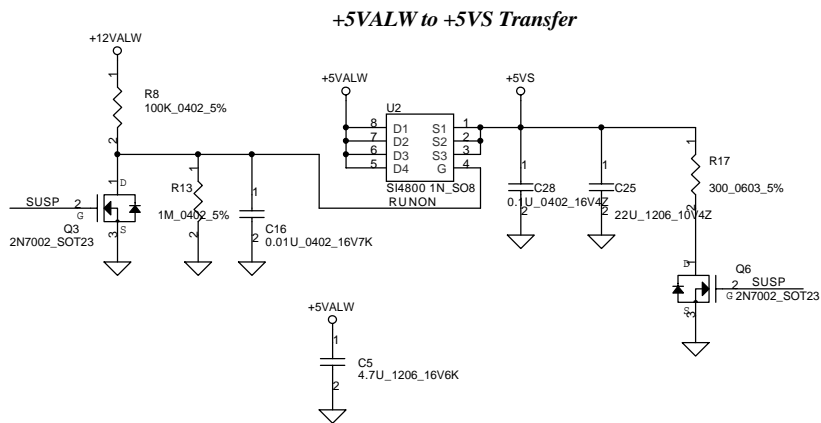
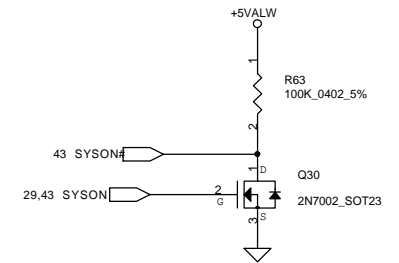
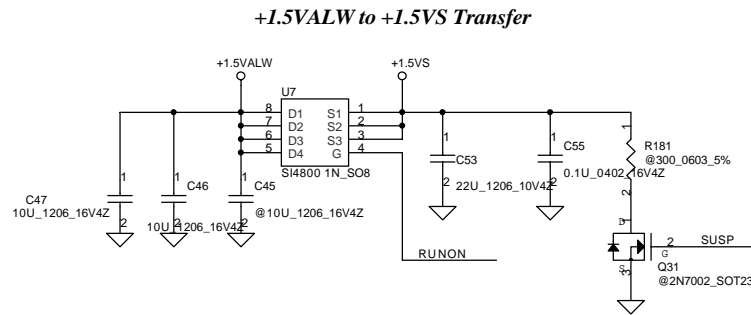
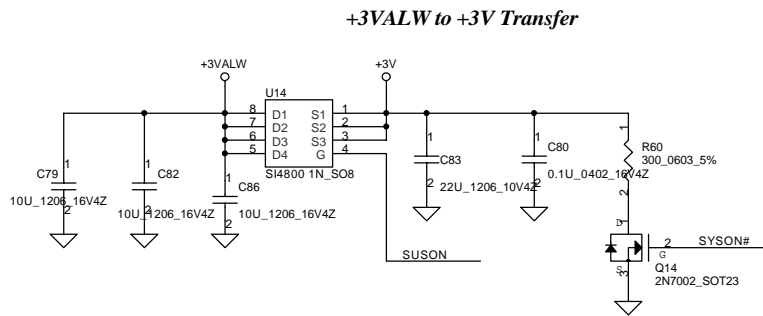
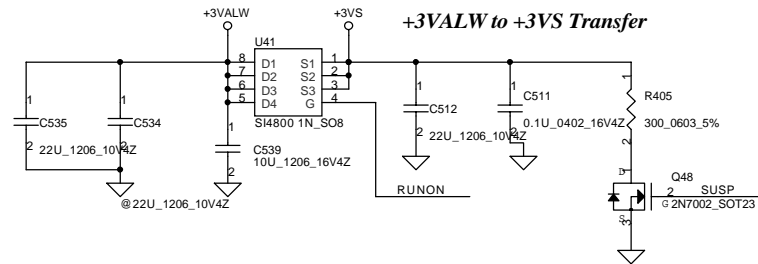
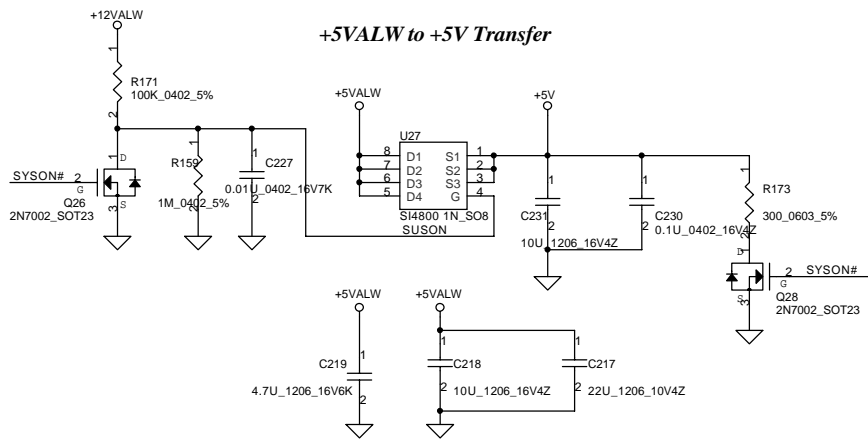
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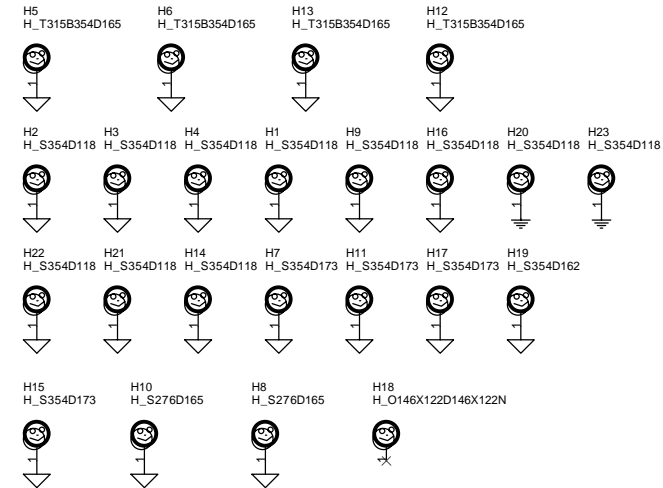
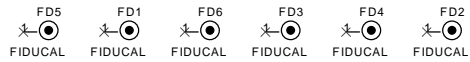
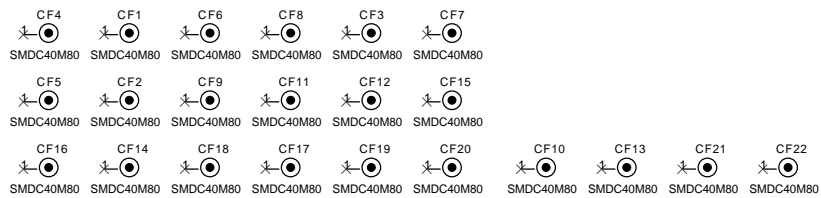
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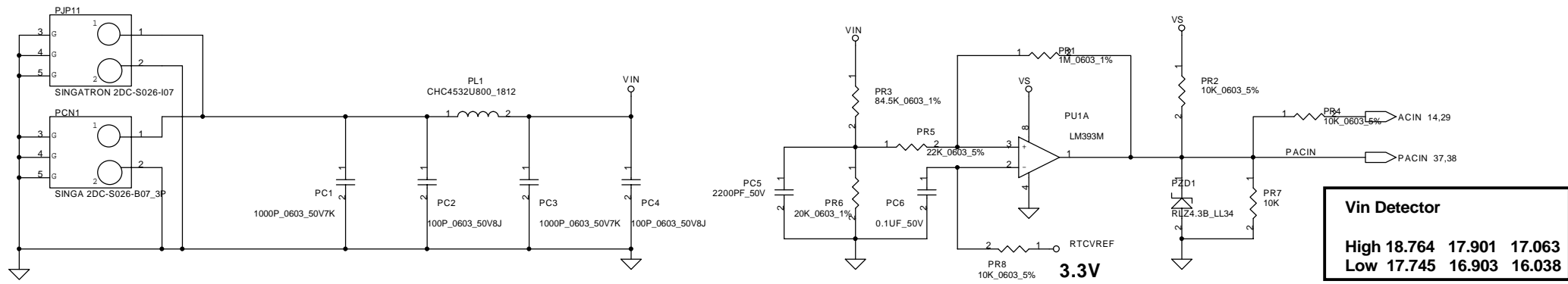
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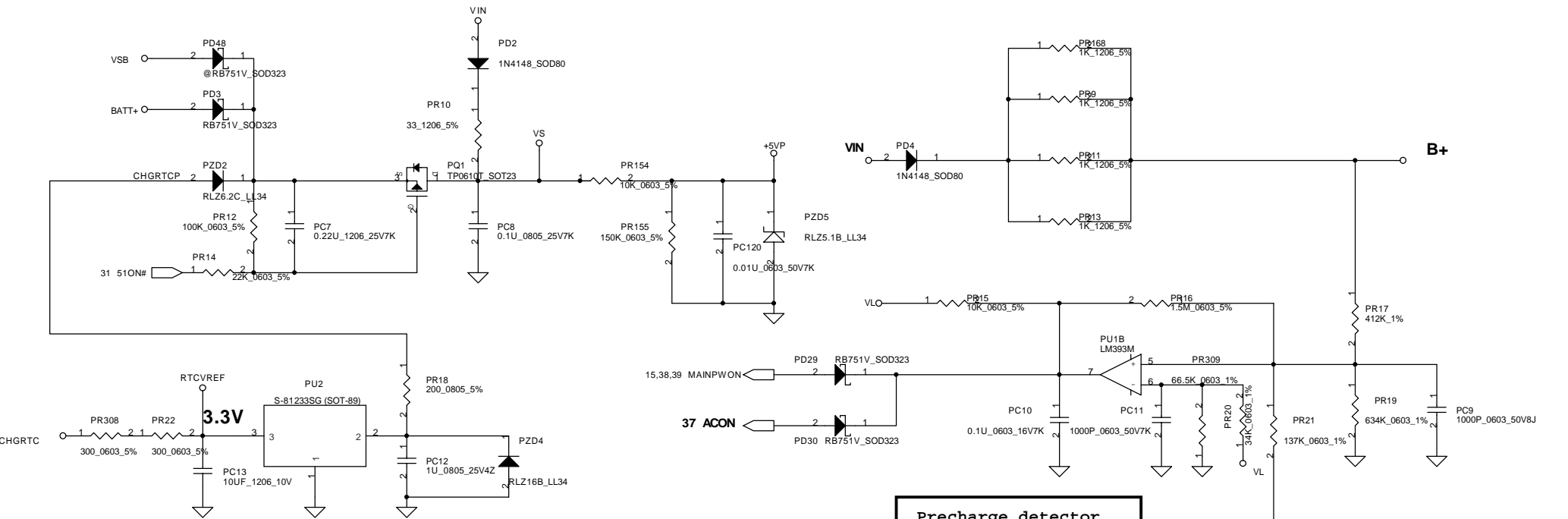


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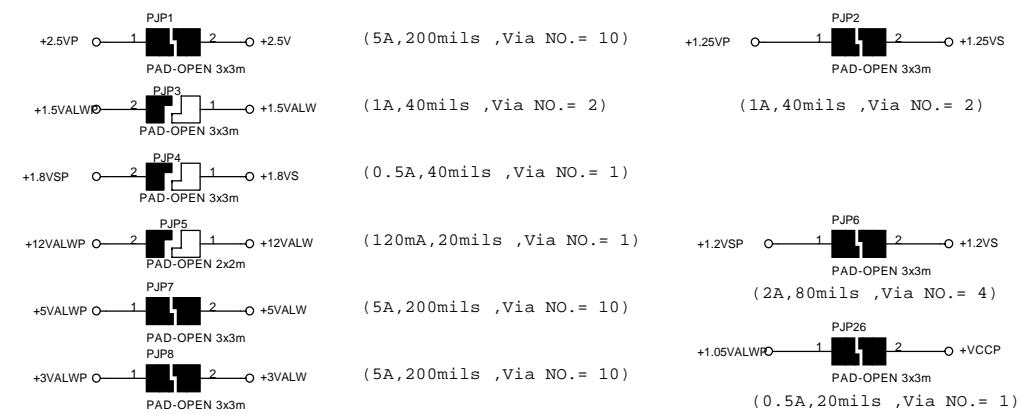


Vin Detector		
High	18.764	17.901
Low	17.745	16.903
	17.063	16.038

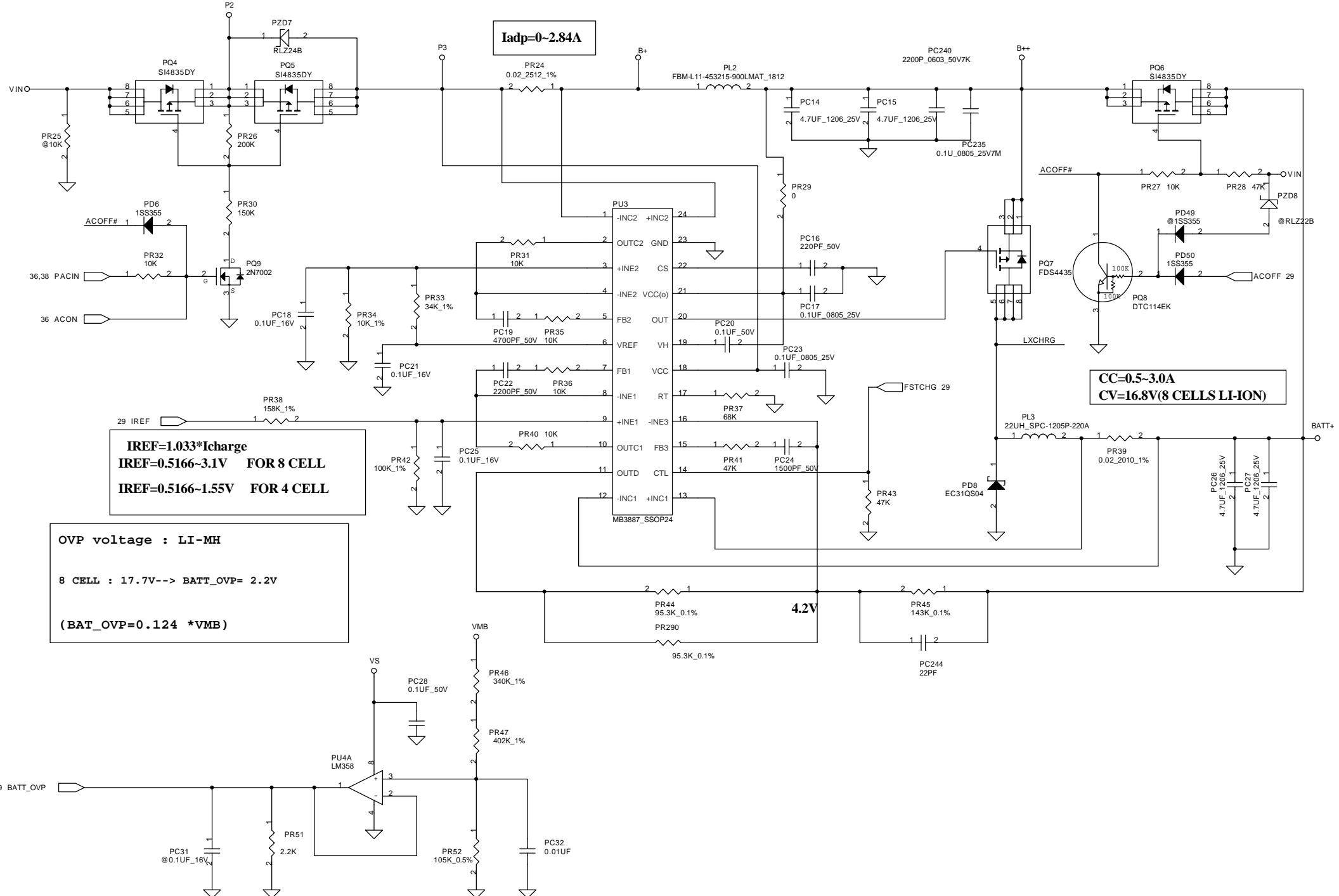


Precharge detector AC ADAPTOR		
	16.69	16.05
	15.6	15.02
	14.35	

Precharge detector AC ADAPTOR		
	6.33	6.12
	5.227	5.09
	4.85	



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IREF=1.033*Icharge
IREF=0.5166-3.1V FOR 8 CELL
IREF=0.5166-1.55V FOR 4 CELL

OVP voltage : LI-MH
8 CELL : 17.7V--> BATT_OVP= 2.2V
(BAT_OVP=0.124 *VMB)

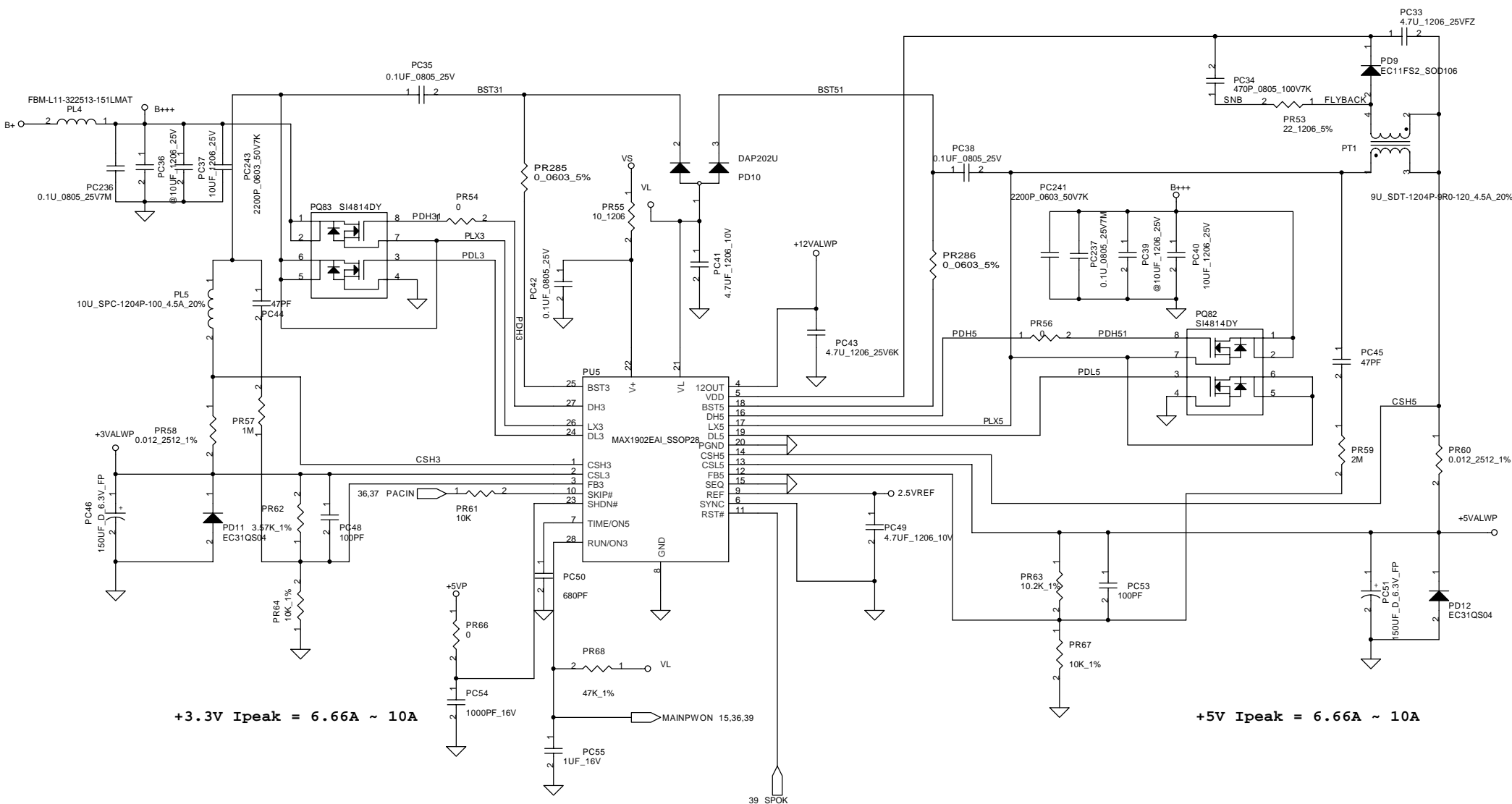
Iadp=0-2.84A

CC=0.5-3.0A
CV=16.8V(8 CELLS LI-ION)

4.2V

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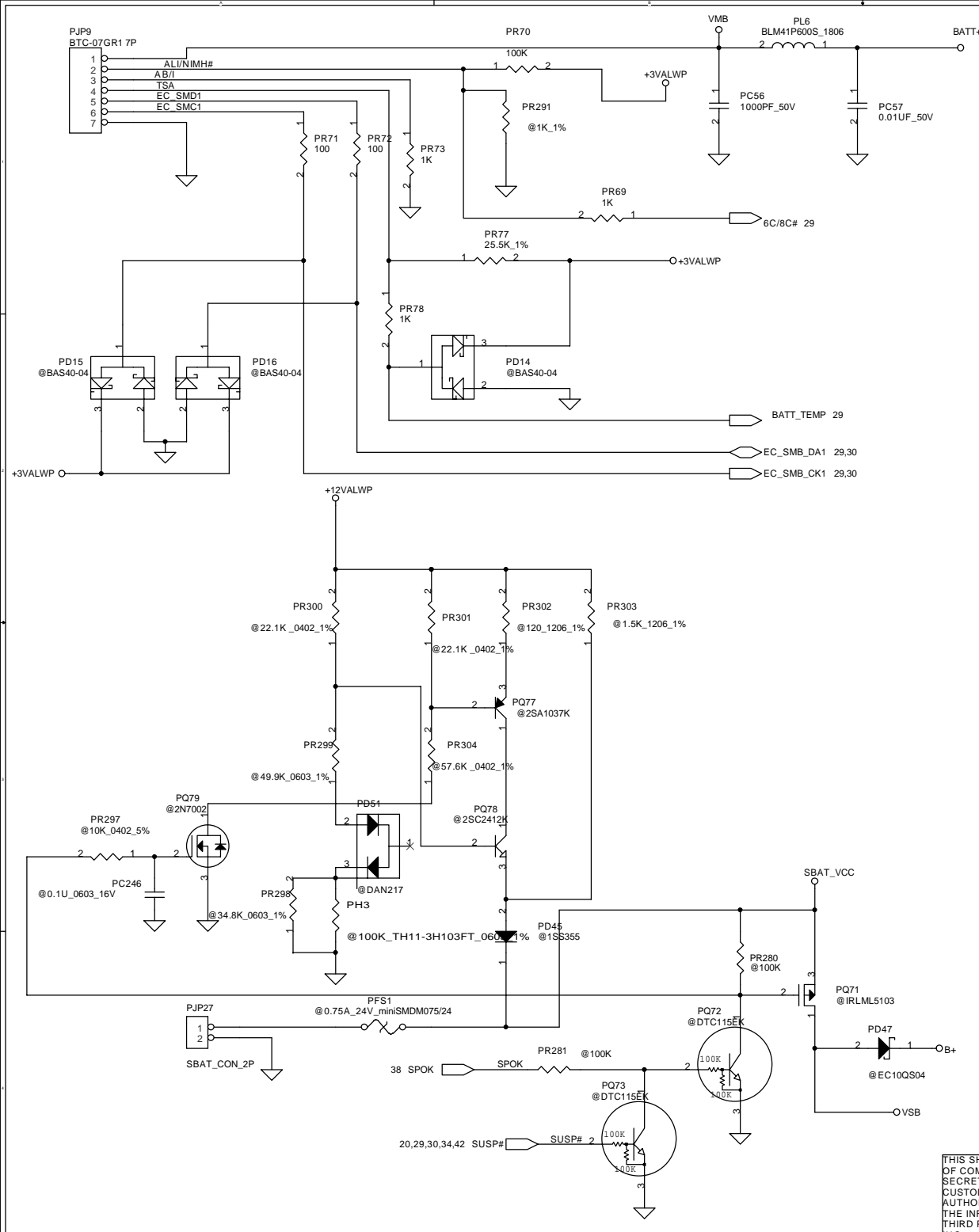


+3.3V Ipeak = 6.66A ~ 10A

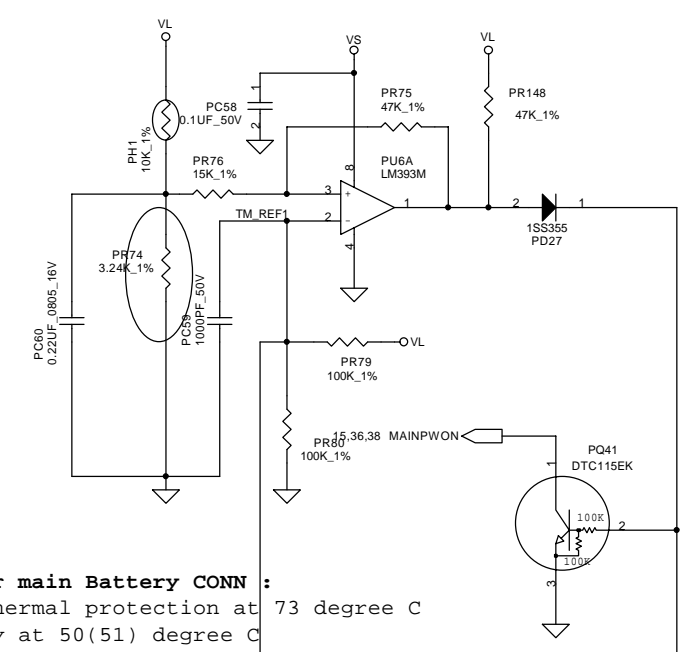
+5V Ipeak = 6.66A ~ 10A

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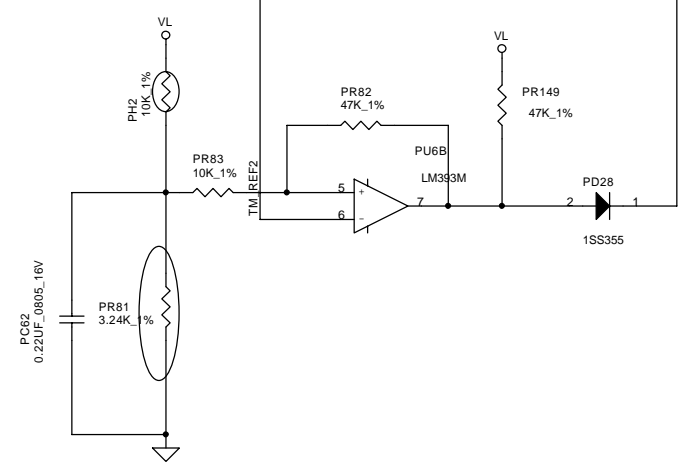
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PH1 under CPU bottom side :
 CPU thermal protection at 82 degree C
 Recovery at 48 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50(51) degree C

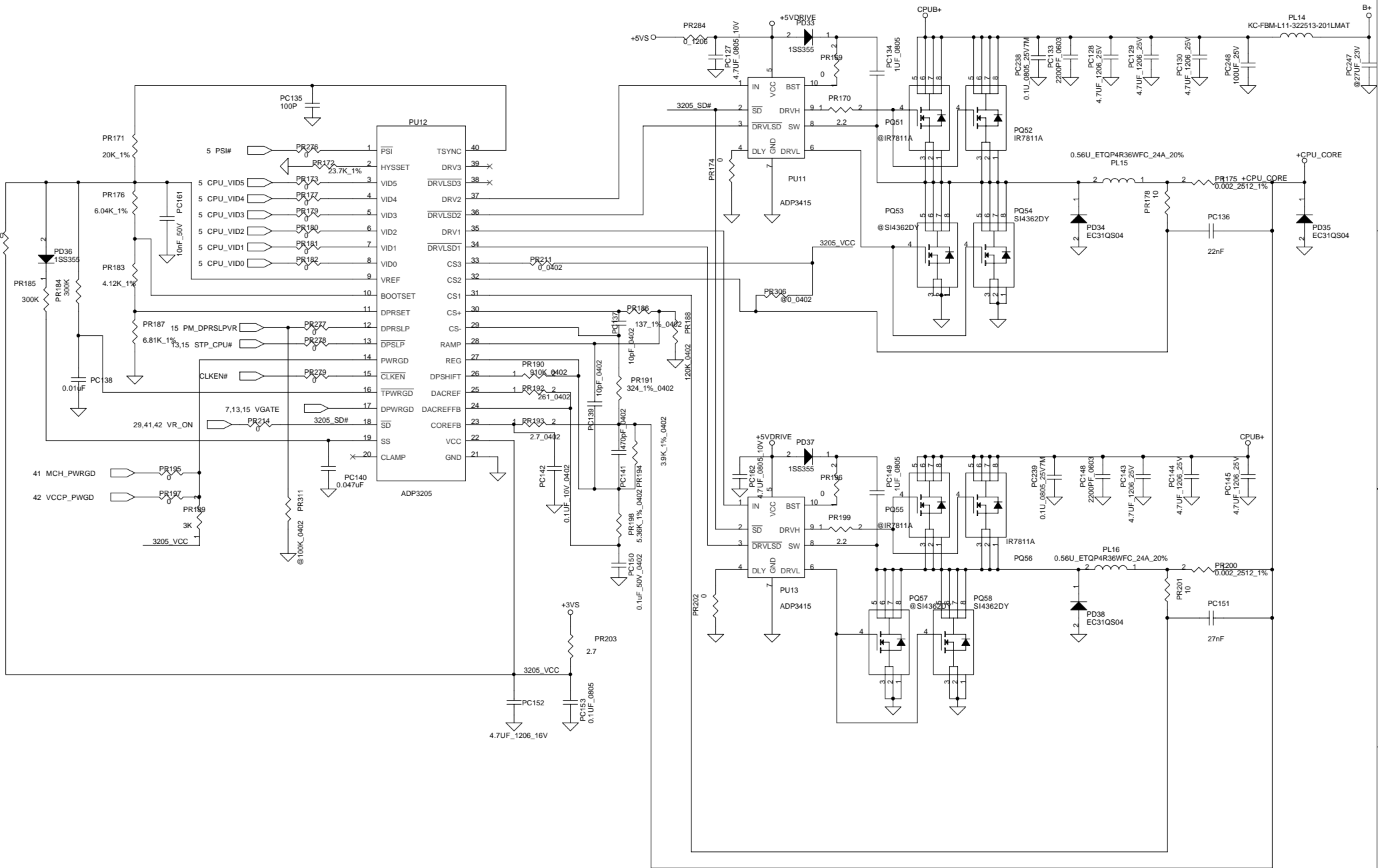


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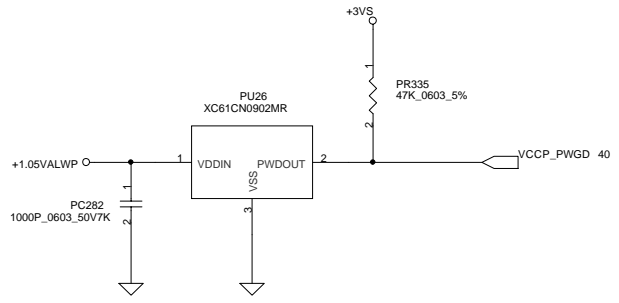
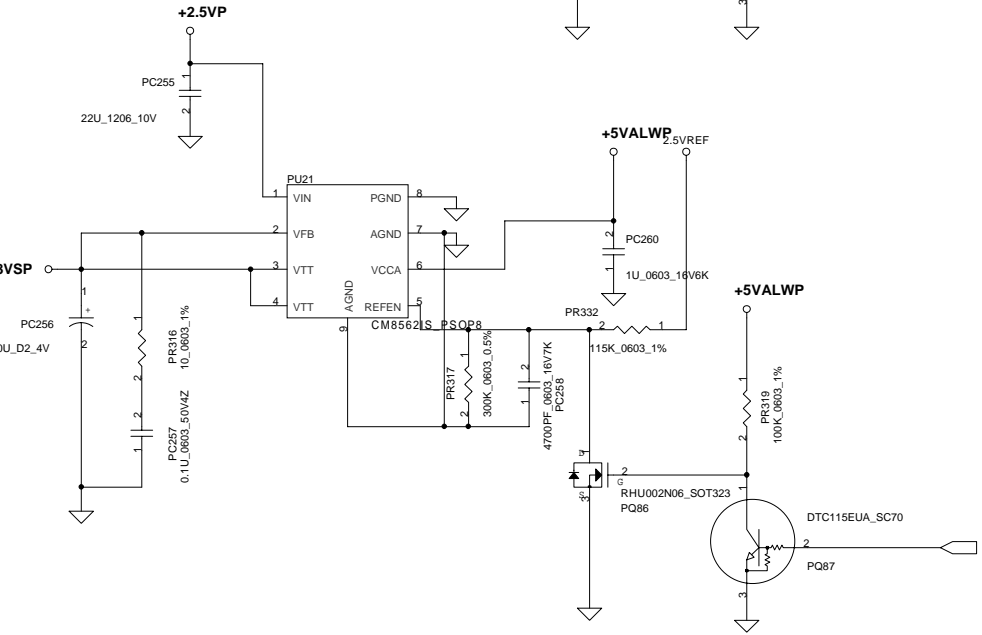
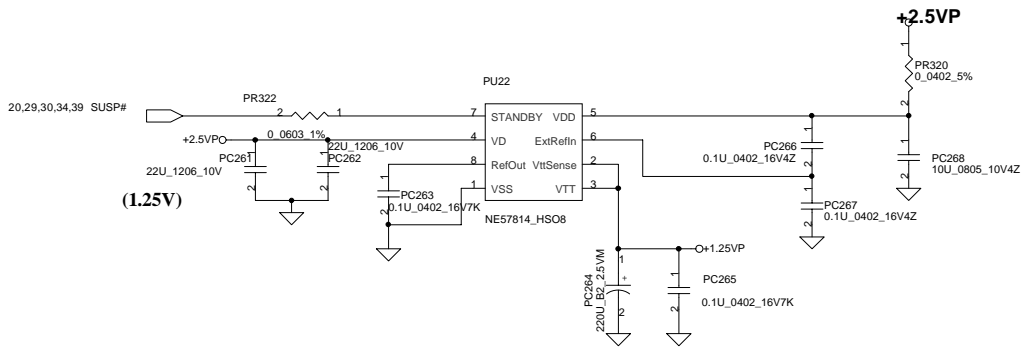
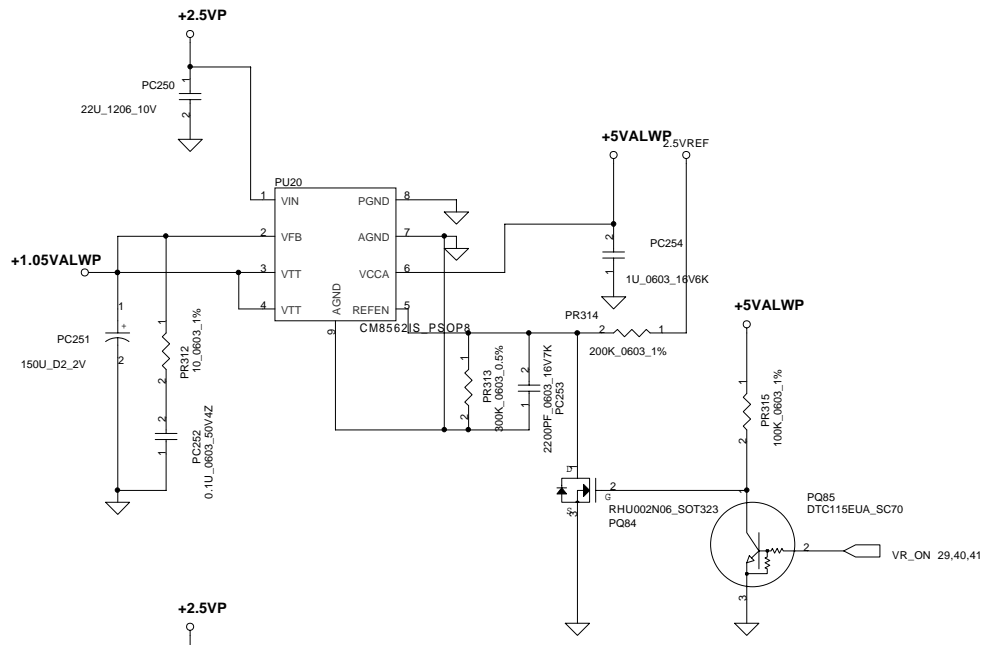
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CPU-CORE



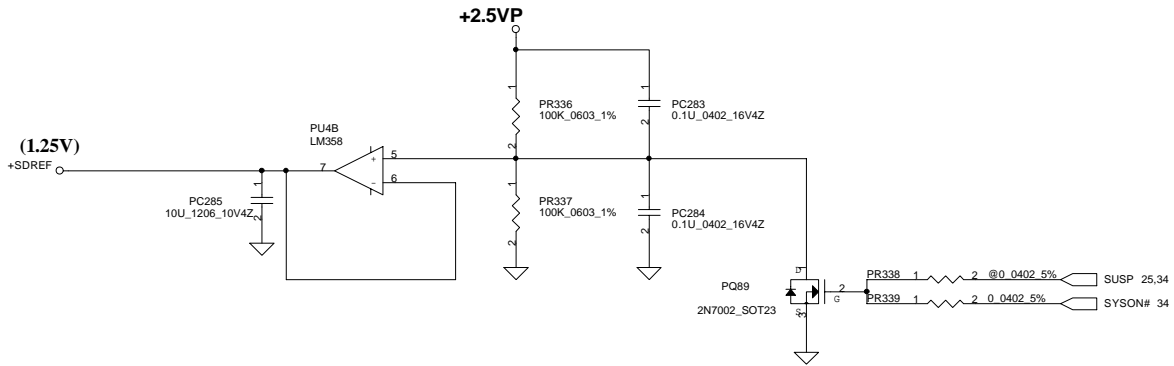
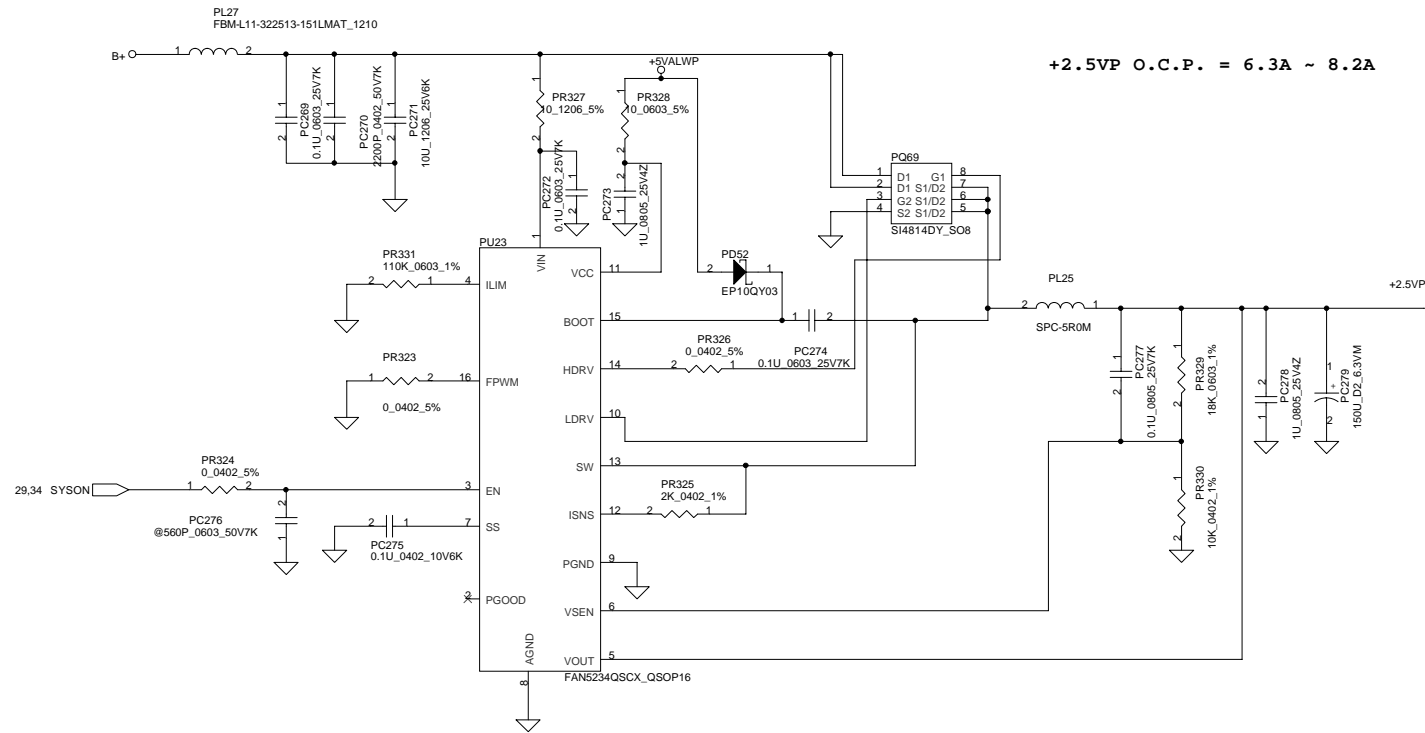
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		Set c4 mode controlled by bios based difference CPU		40	DELETE PR311:100K ; ADD PR277:0		DVT
2		Modify 1.05VP voltage level		42	1. change PR314 to 200k		DVT
3		modify 1.05VP,1.8VP soft start time		42	add PC253, PC258 to be 0.1U		DVT
4		add +SDREF signal circuit		43	add PR339:0; PQ89: 2N7002; PC283,PC284 :0.1U 16V;PR336,PR337:100K;PC285:10U 1206		PVT
5		Add one set power good:VCCP_PWGD		42,41	ADD LDO PU26 :XC61CN;PR335:47K;PC282:1000P 50V,PCHANGE R235 FROM 10K TO 47K		PVT
6		modify 1.05VP,1.8VP soft start time		42	CHANGE PC253 from 0.1u to 2200PF, PC258 from 0.1U to 4700PF		PVT
7		CHANGE PU5 from MAX1631 to MAX1902 (BECAUSE MAX1631 shortage)		38	CHANGE PT1 from 10u_1205P to 9u_sdt-1204p-9r0-120;delete PU19;CHANGE p15 FROM 10U_SPC-1205P-100 to 10u_1204p-100_4.5A;change PC39 from 180PF to 470PF;DELETE PZD6;change PU5 from max1631 to max1902		MP
8		FOR CL53A ; To change 1.2VSP to 1.35 VSP		37,41	CHANGE PR224 from 3.48K to 5.1K, delete PD49,DELETE PZD8		
9							

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		reserve +SDREF signal circuit		8	reserve R477,R479		PVT
2		reserve +SDREF signal circuit		10	reserve R480,R481		PVT
3		EMI performance		8	change C420_net from MRCOMP to +2.5V		PVT
4		reserve syson,susp#,vr_on pull low resister		29	reserve R482,R483,R484		PVT
5		cost down			change L18,L19,L14,L13,L12,L8,L9,L7 to 0 ohm del C534,C45		PVT
6		board version update		29	change R361 from 8.2k to 18k		PVT
7		for customer request			del TV_out , 1394 funtion		PVT
8		solove leakage			del D15		preMP
9		board version update		29	change R361 from 8.2k to 33k		preMP
10	USB port will be damaged by ESD, add ESD protect diode.	Per Lenovo request, add USB ESD protect diode	Rev3.0	26	Add D18, D32, D33. Change C239, C34, C22, C21, C24, C23 from 470P to 3.3P.		MP

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