

Compal Confidential

Fortworth20 EDW10 Schematic Document

Intel Protability Processor with ATi RC300ML + IXP150

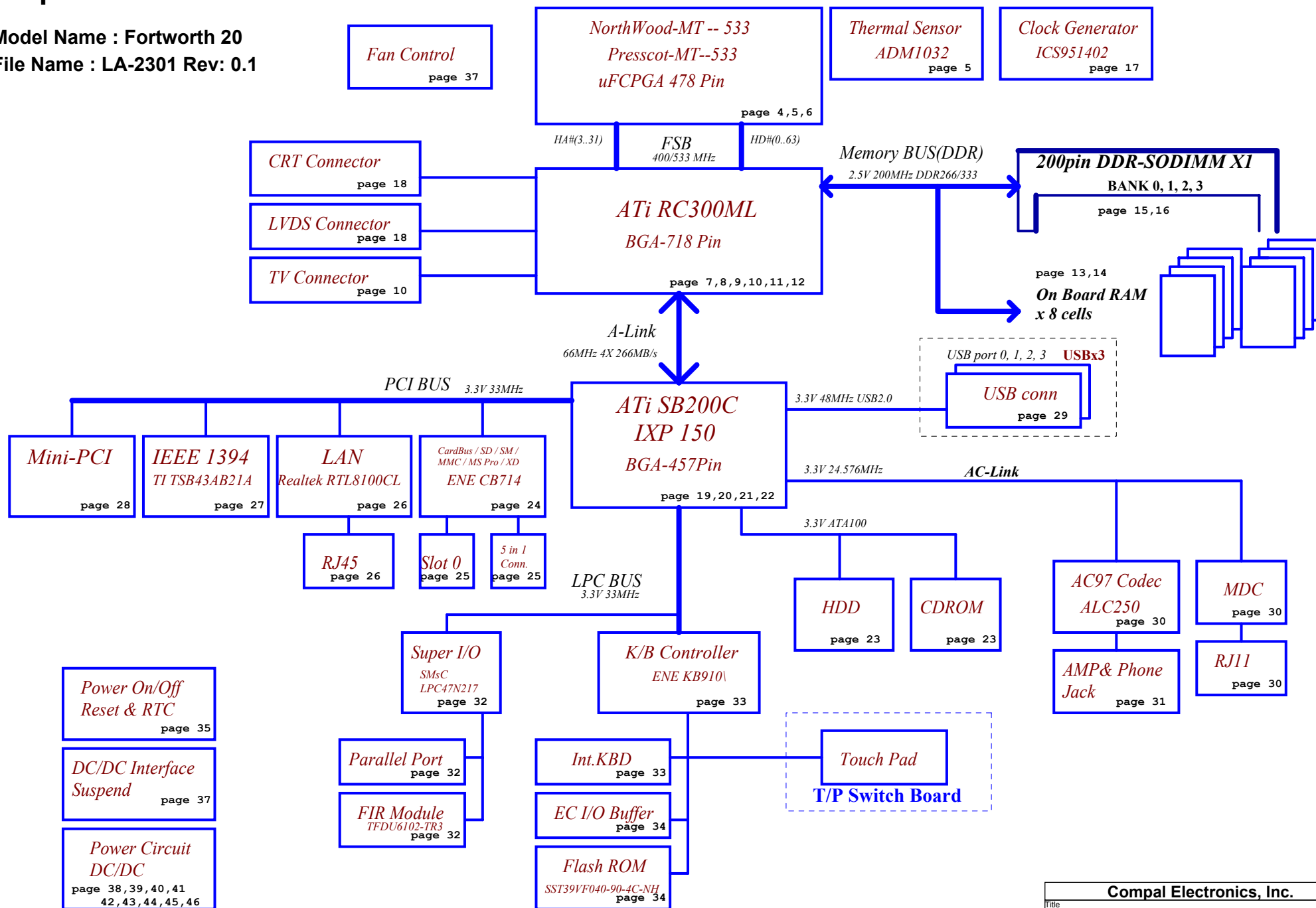
2004-03-16

REV: 0.2

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Title	Cover Sheet
Document Number	LA-2301
Date	Thursday, April 08, 2004
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Rev	0.2

Model Name : Fortworth 20
File Name : LA-2301 Rev: 0.1



Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V rail for Processor VID	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON*	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A
5 in 1	AD20	2	B
Mini-PCI	AD18	3	C/D

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16)	1010 000X b	ALC250	0000 000X b

EC SM Bus2 address

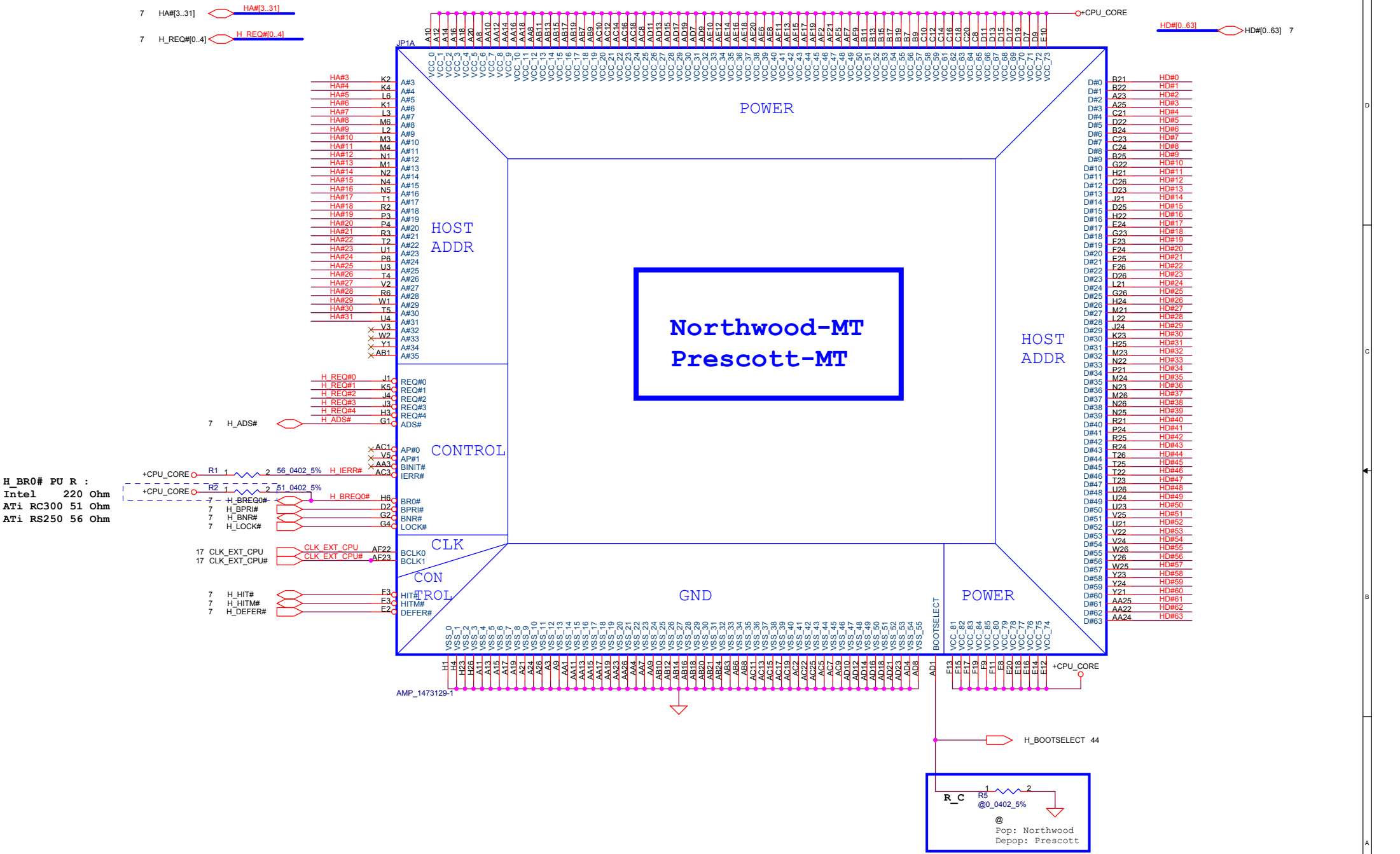
I2C / SMBUS ADDRESSING

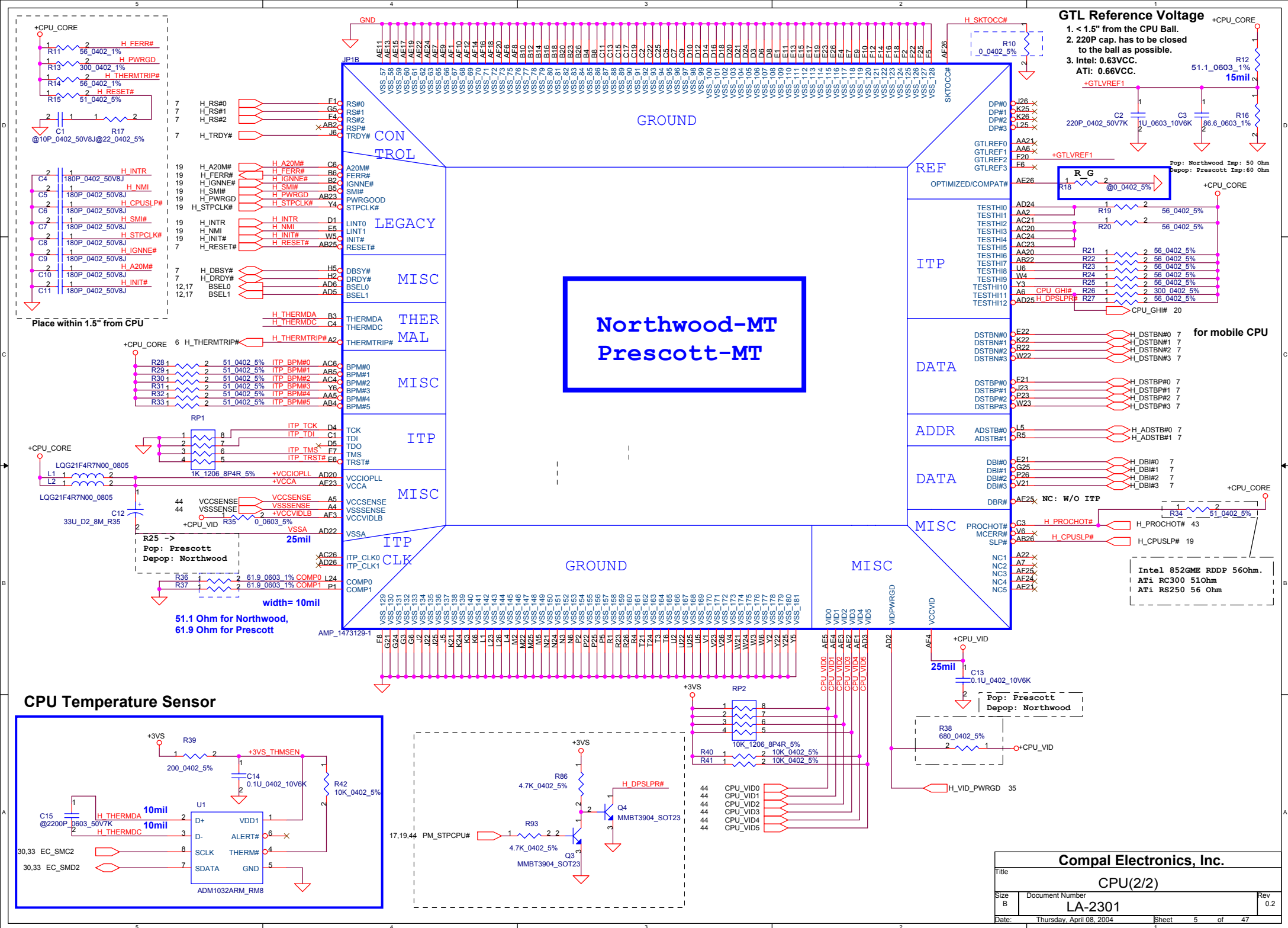
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

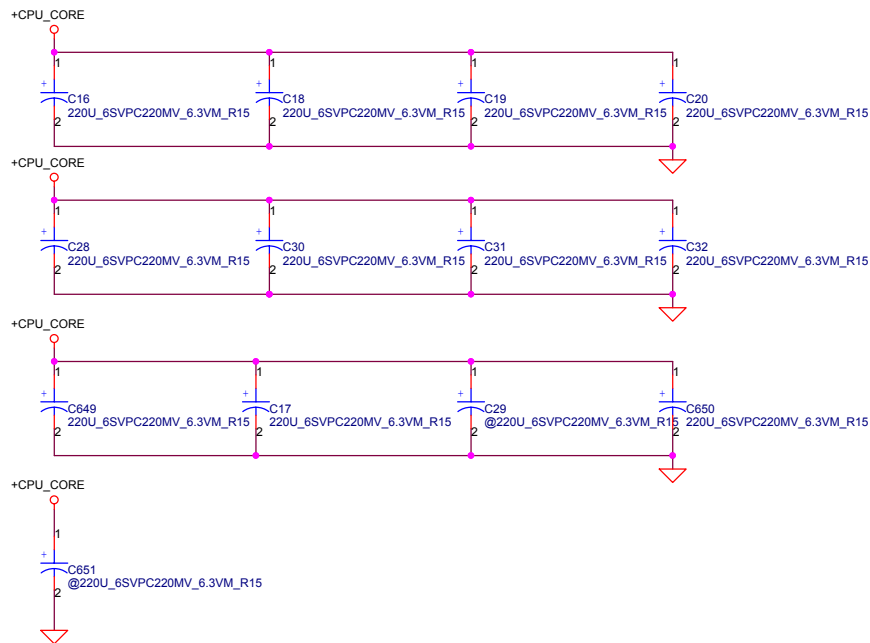
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	



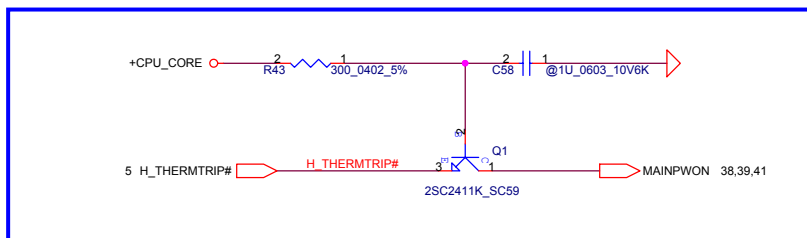




Layout note :

Place close to CPU power and ground pin as possible (<1inch)

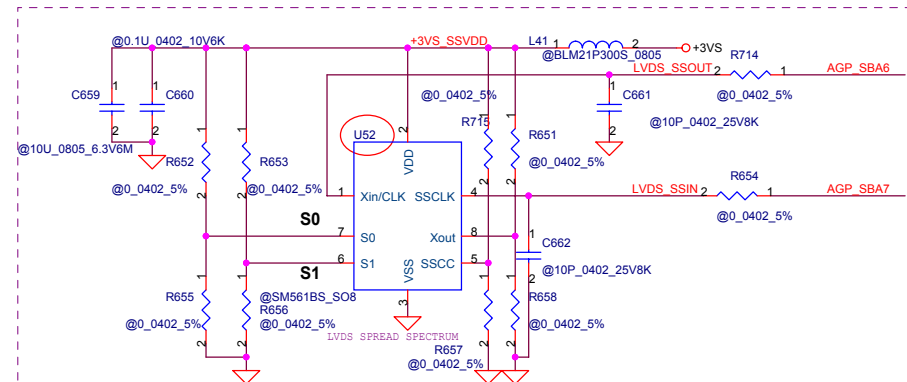
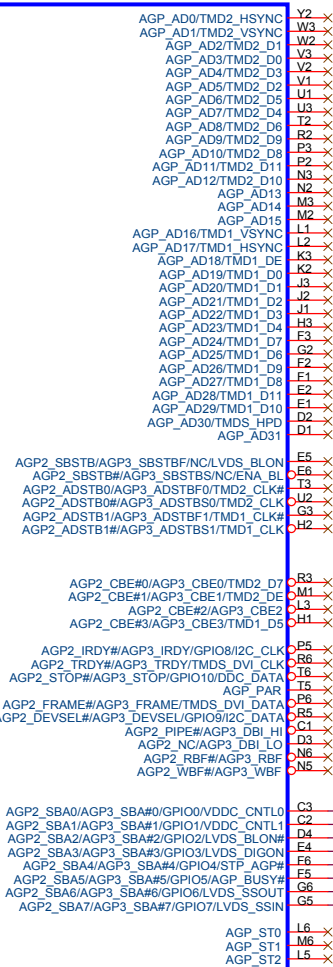
Sanyo : SGA27221300 (220uF, 13m Ohm)



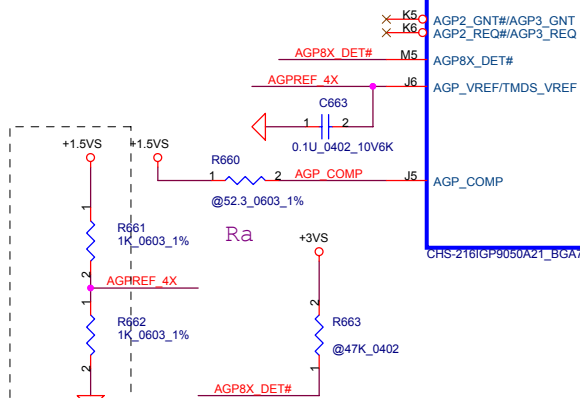
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CPU Decoupling

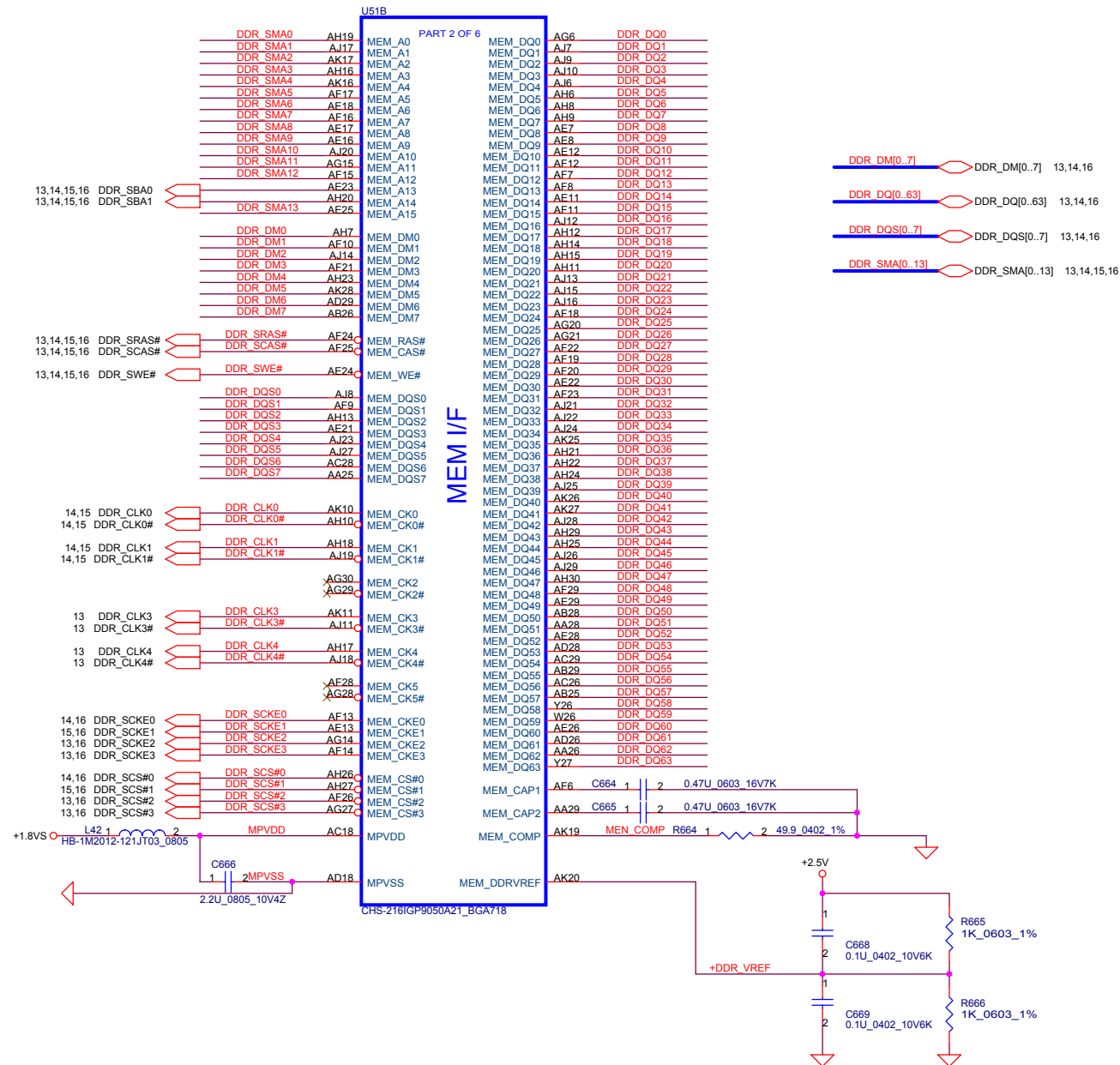
LA-2301

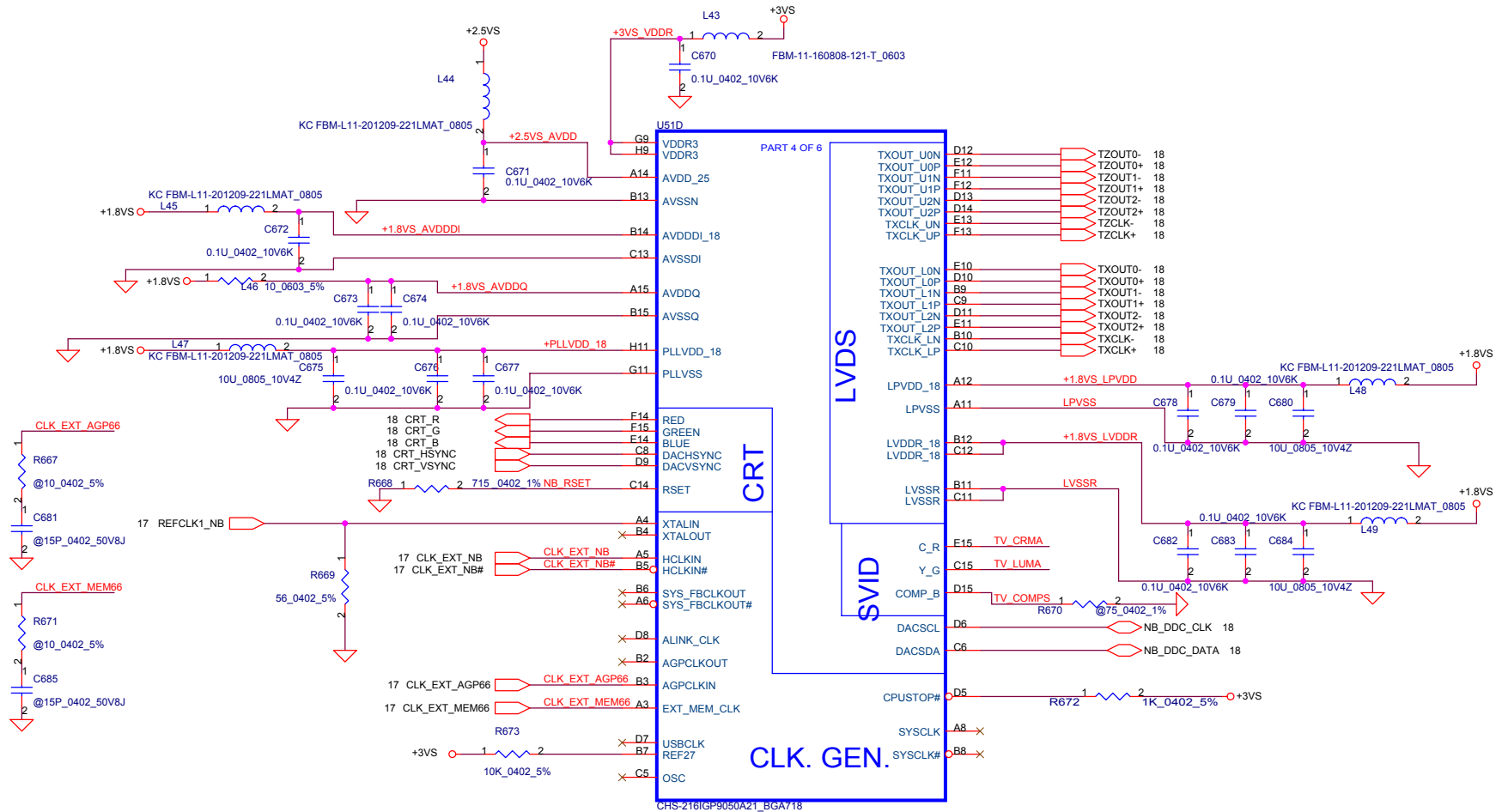


 Note: PLACE CLOSE TO U2 (NB RC300M)

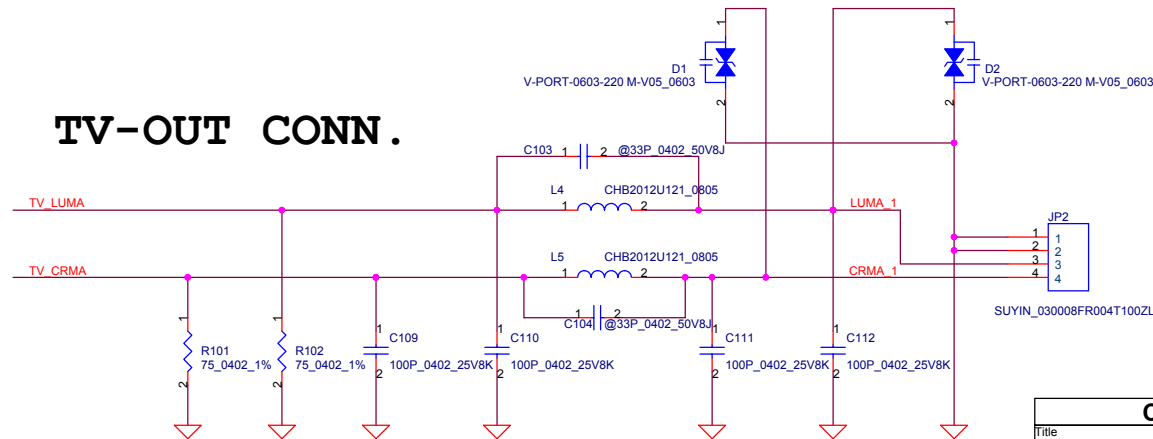


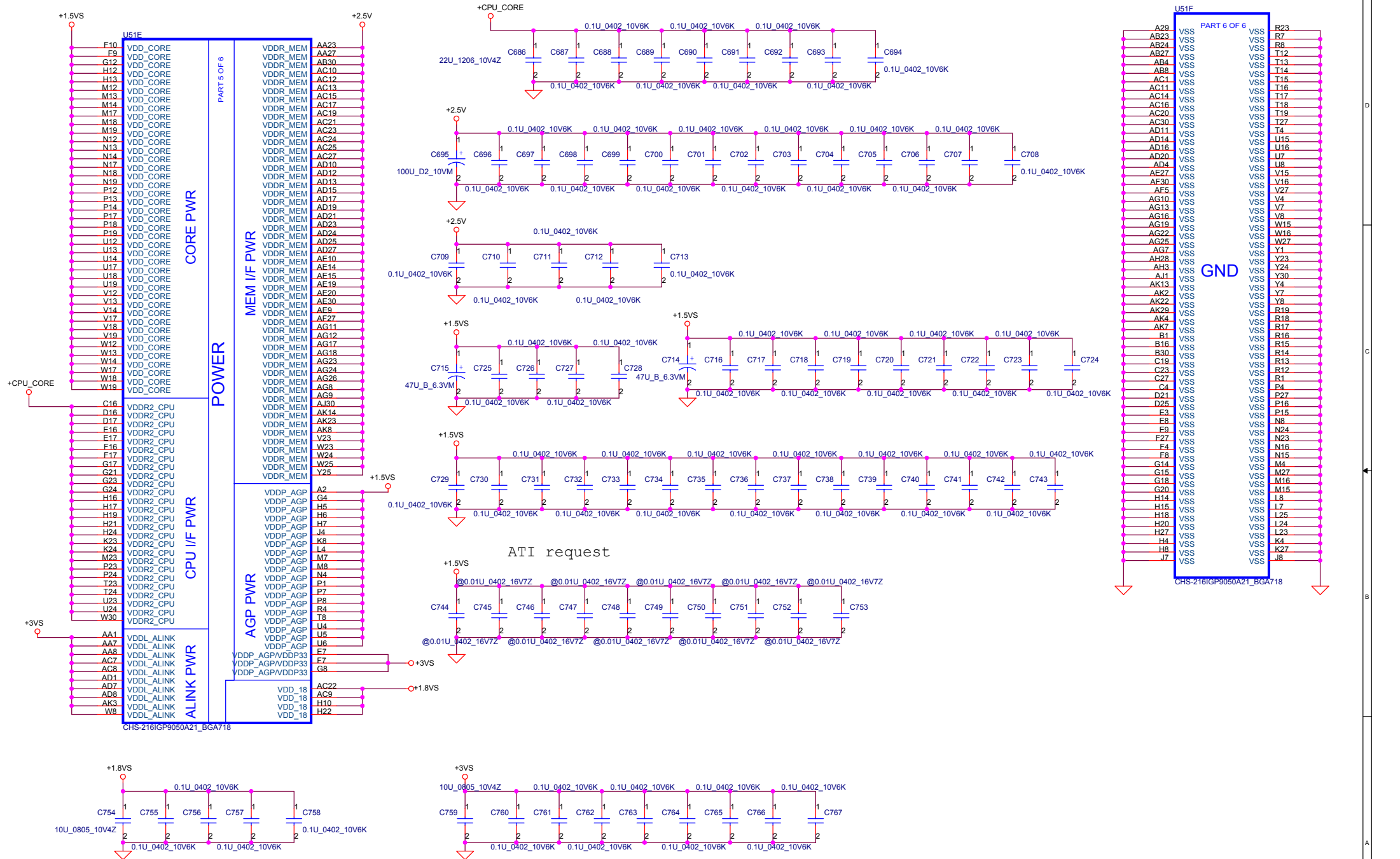
Close to Pin J6





TV-OUT CONN.

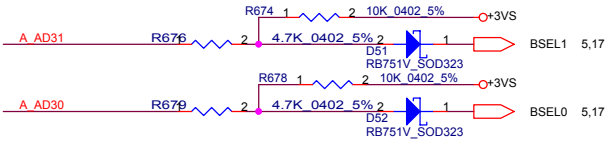




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A_CBE#[0..3] A_CBE#[0..3] 8,19

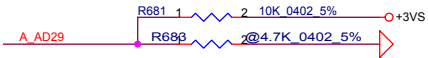
8,19 A_AD[0..31] A_AD[0..31]



A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

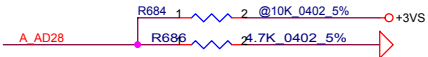
00: 100 MHZ
01: 133 MHZ
10: 200MHZ
11:166 MHZ



A_AD29: STRAP CONFIGURATION

DEFAULT: 1

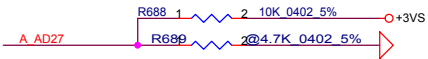
0: REDUCEDE SET
1: FULL SET(internal Pull high)



A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT: 0

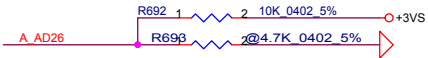
0: DISABLE
1: ENABLE



A_AD27: FrcShortReset#

DEFAULT: 1

0: TEST MODE
1: NORMAL
MODE



A_AD26 : ENABLE IOQ

DEFAULT: 1

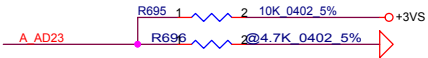
0: IOQ=1
1:
IOQ=12



A_AD24 : MOBILE CPU SELECT

DEFAULT: 1

0: BANIAS CPU
1: OTHER CPU



A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1

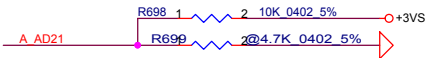
0: TEST MODE
1: NORMAL(internal Pull high)



A_AD22 : OSC PAD OUTPUT PCICLK

DEFAULT : 1

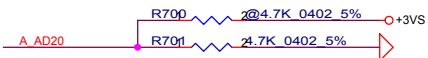
0:PCICLK OUT
1: OSC CLK OUT



A_AD21 : AUTO_CAL ENABLE

DEFAULT : 1

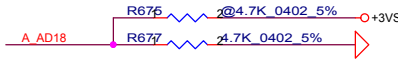
0: DISABLE
1: ENABLE



A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0

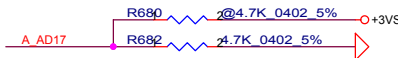
0: DISABLE
1: ENABLE



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0

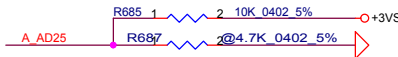
0: DISABLE
1:ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 0

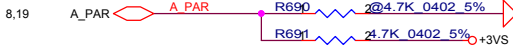
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 10

AD25=1 DESTOP CPU
AD25=0 MOBILE CPU
AD17--DON'T CARE
00: 1.05V
01: 1.35V
11: 1.75V
10: 1.45V



PAR: EXTENDED DEBUG MODE

DEFAULT : 1

0: DEBUG MODE
1: NORMAL

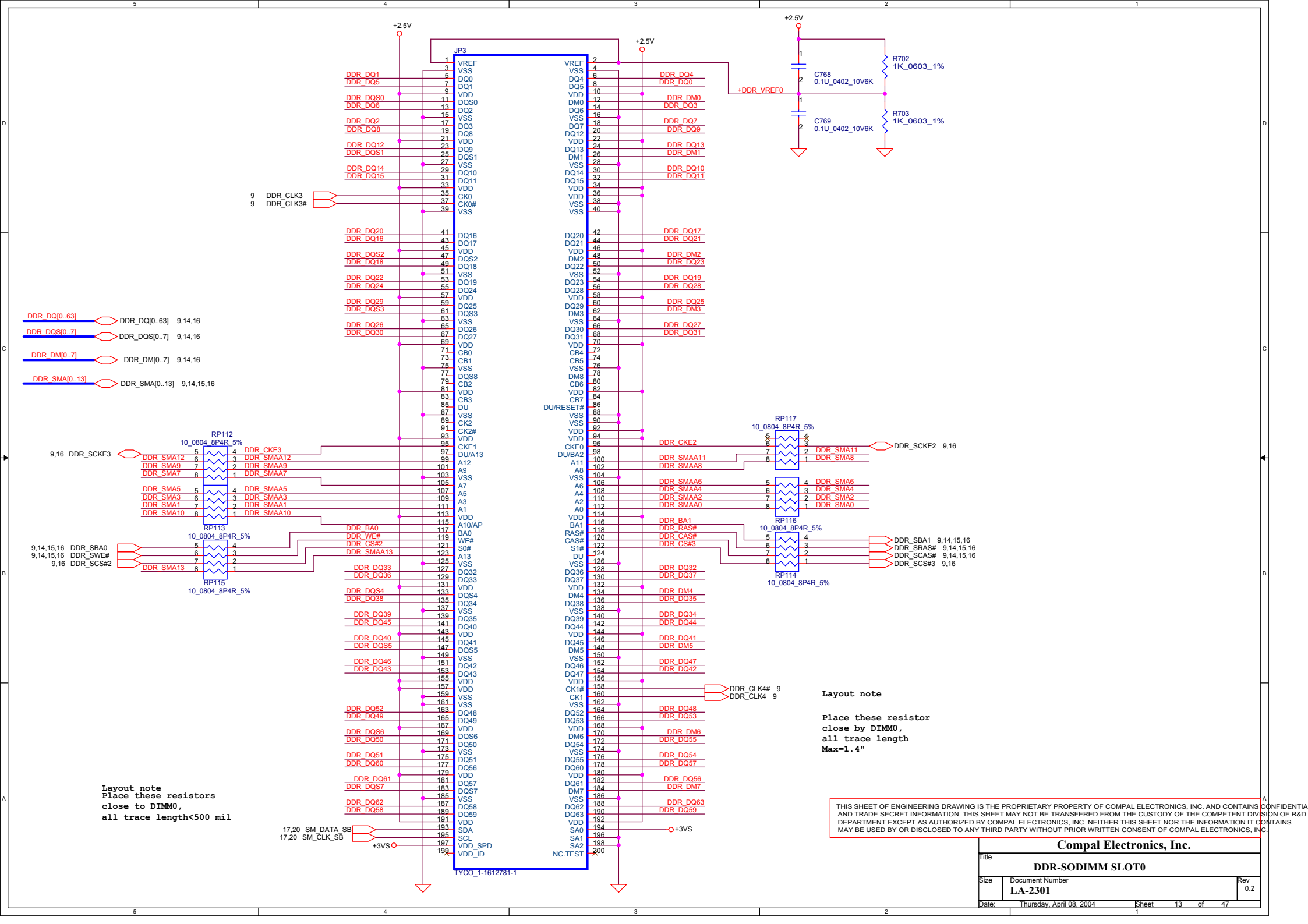
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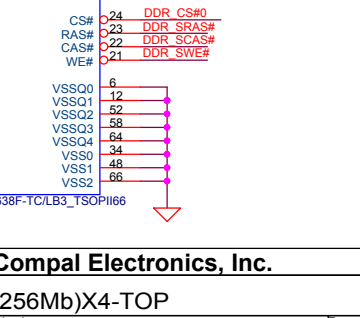
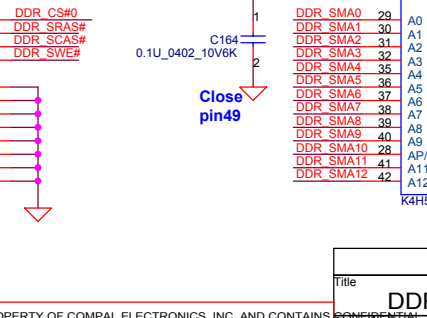
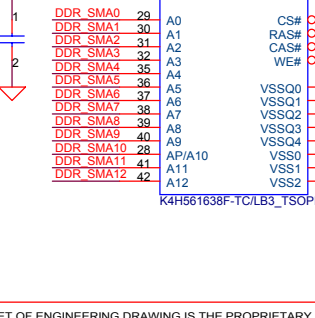
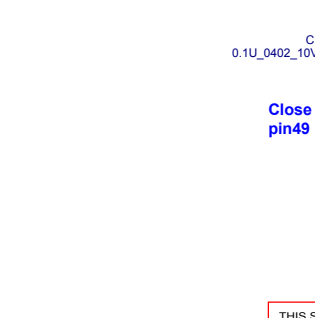
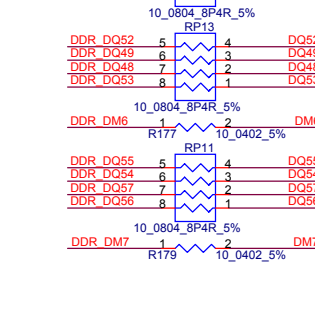
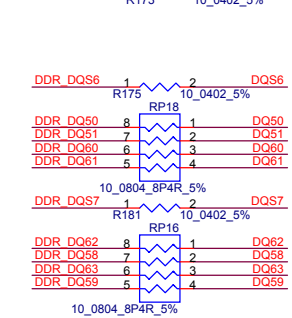
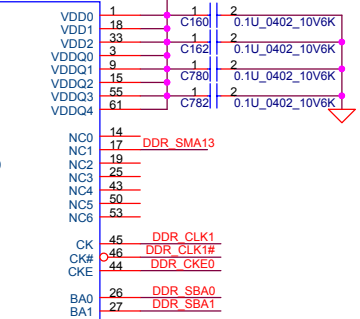
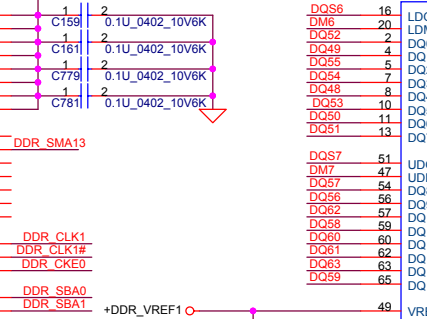
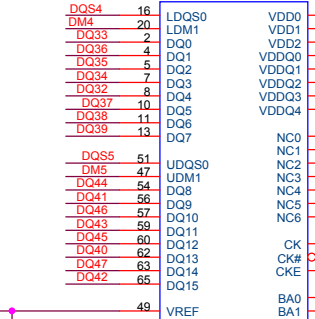
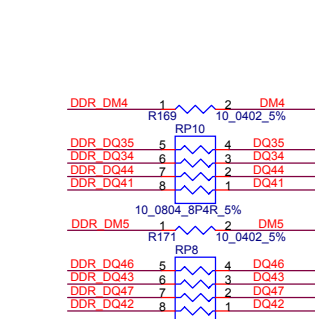
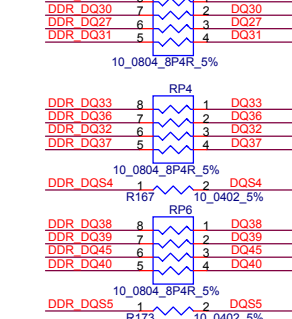
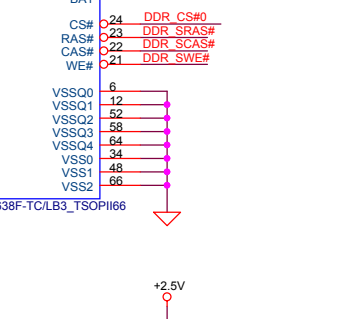
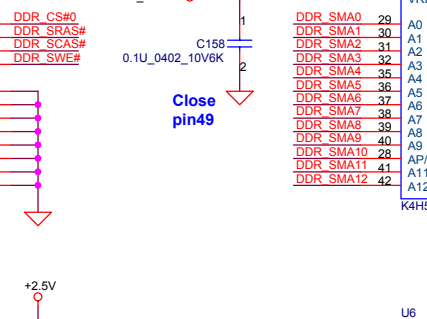
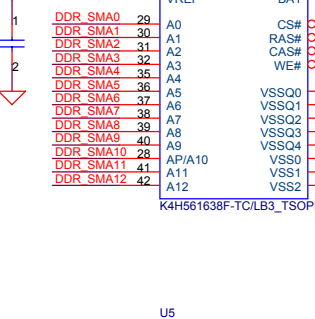
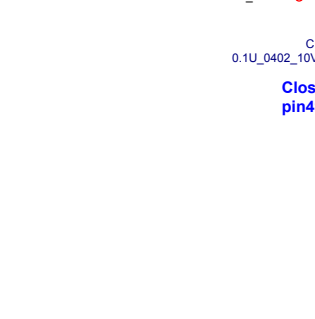
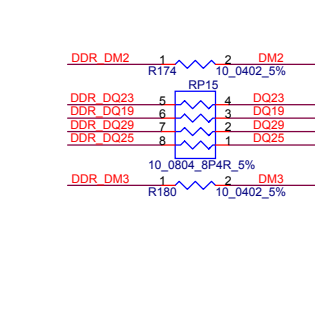
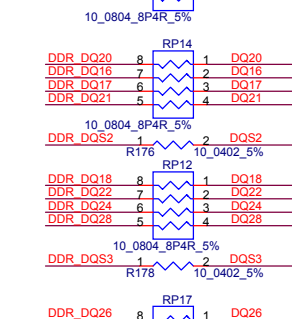
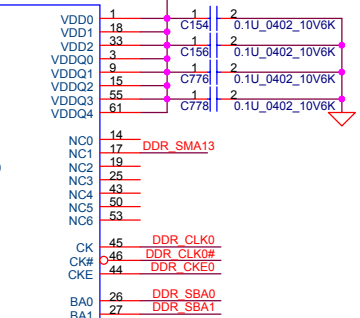
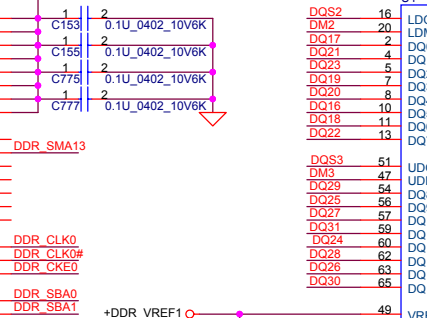
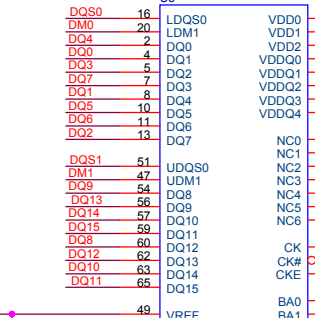
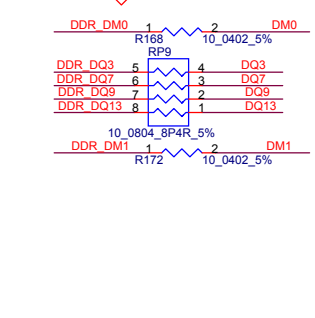
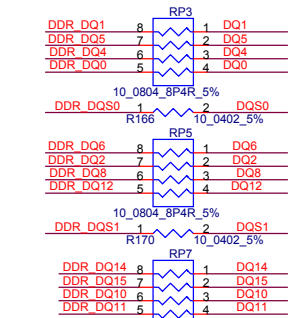
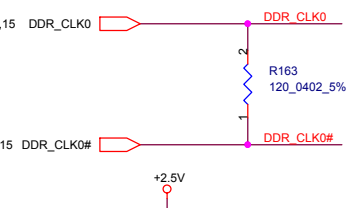
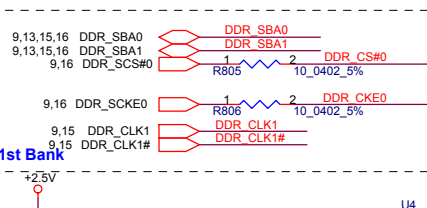
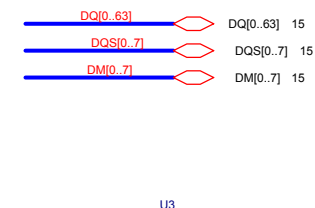
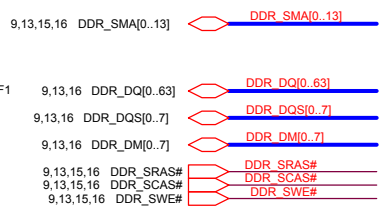
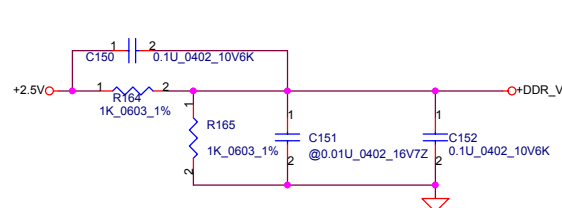
ATi RC300ML-SYS. CONFIG.

LA-2301

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9,13,14,16 DDR_SMA[0..13]

DDR_SMA[0..13]

14 DQ[0..63]

DQ[0..63]

14 DQS[0..7]

DQS[0..7]

14 DM[0..7]

DM[0..7]

9,13,14,16 DDR_SRAS#

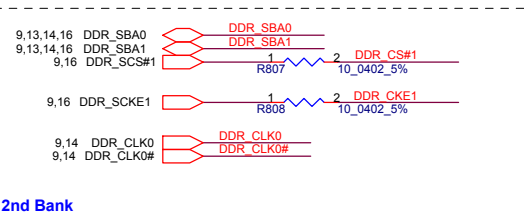
DDR_SRAS#

9,13,14,16 DDR_SCAS#

DDR_SCAS#

9,13,14,16 DDR_SWE#

DDR_SWE#

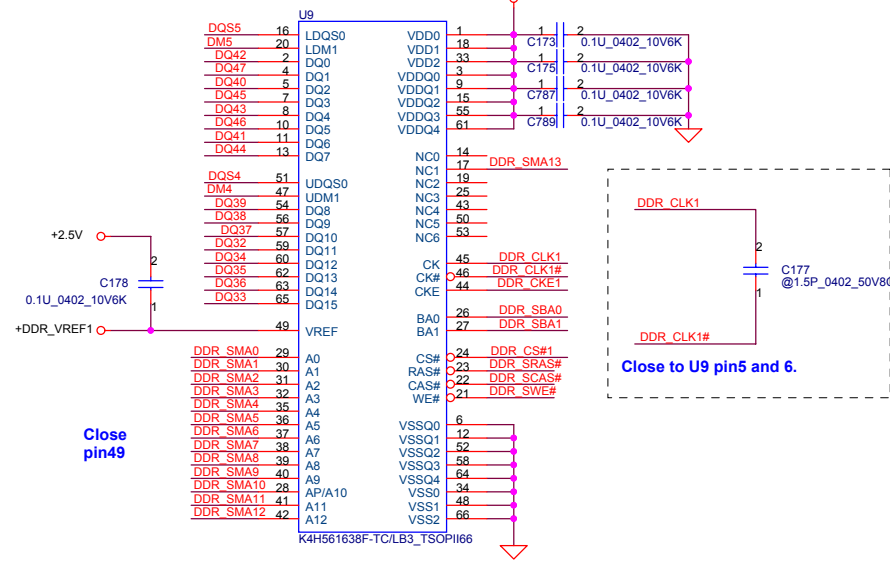
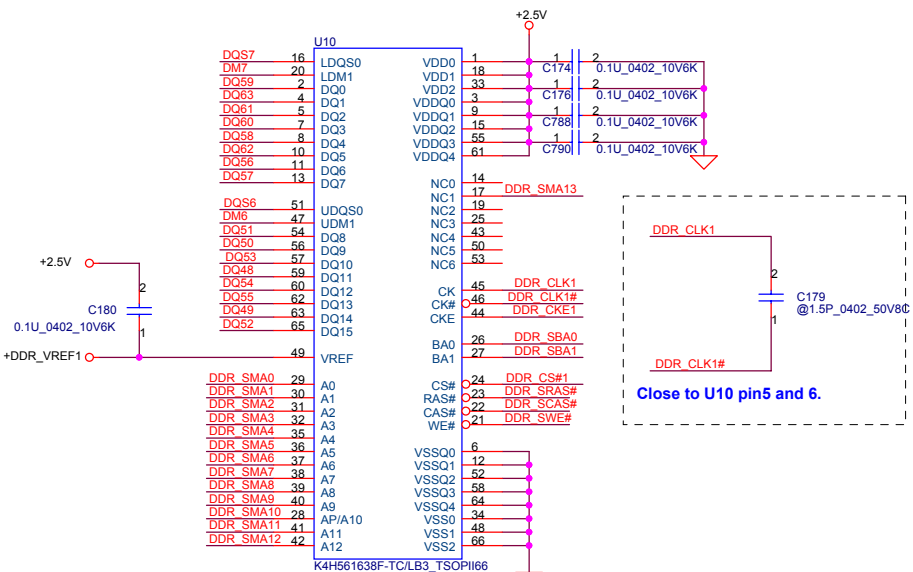
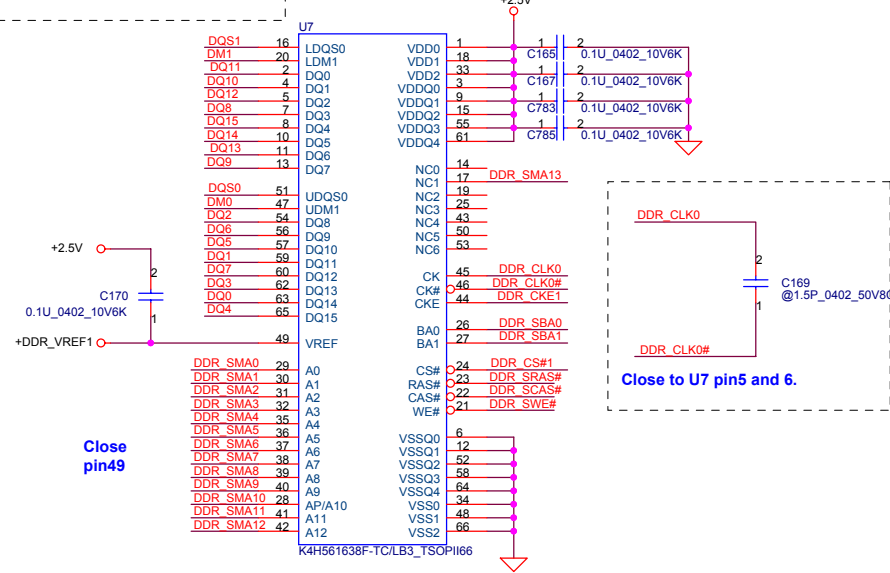
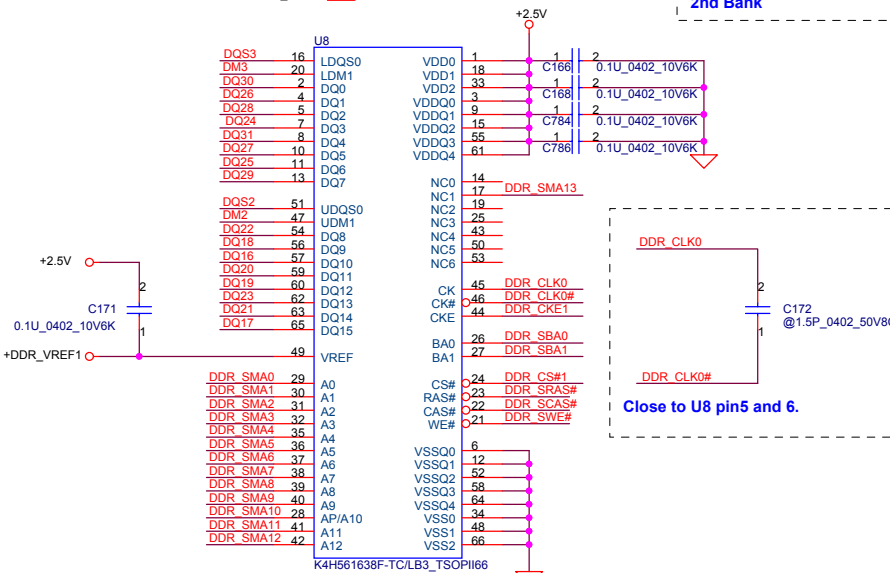


9,14 DDR_CLK1

DDR_CLK1

9,14 DDR_CLK1#

DDR_CLK1#



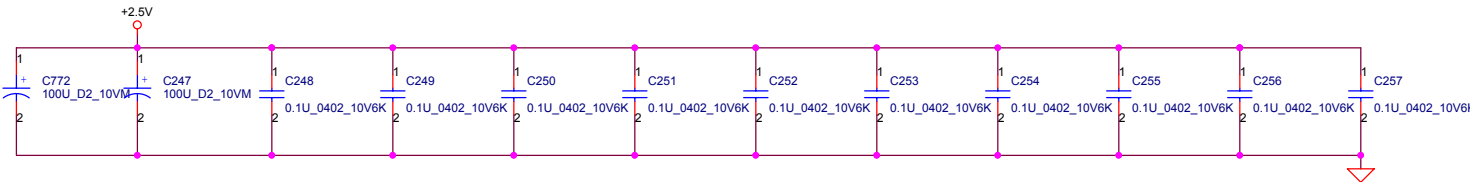
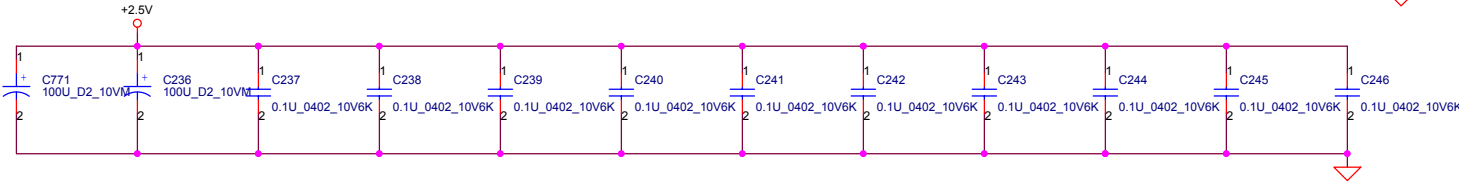
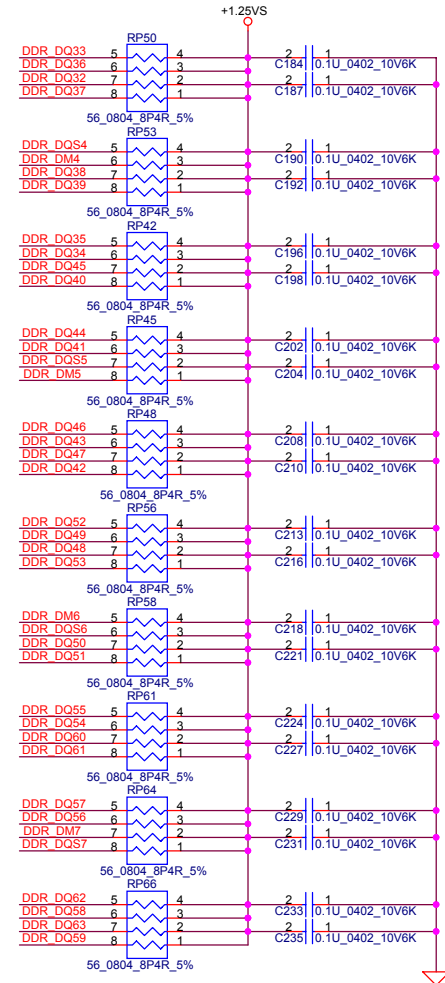
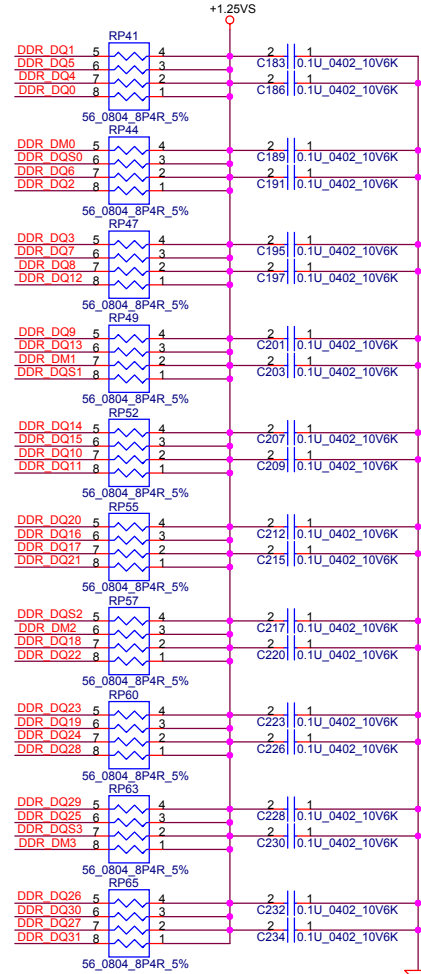
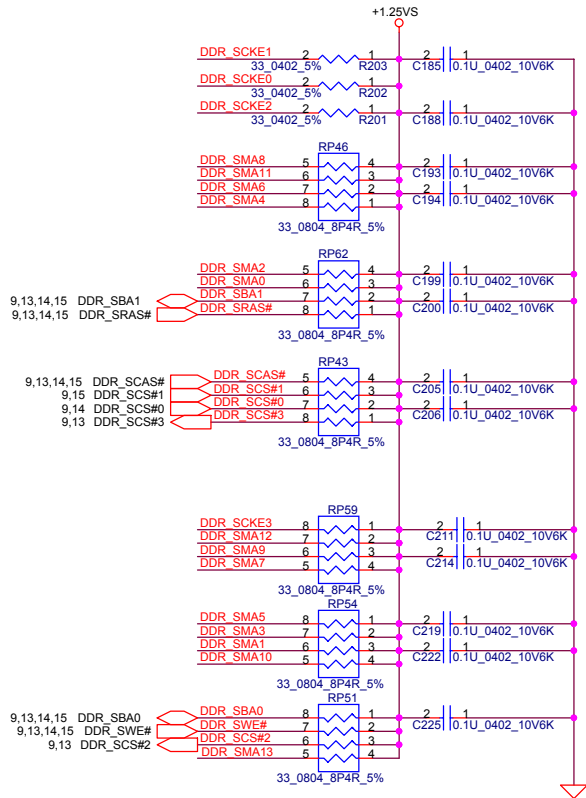
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DDR(256Mb)X4-BTN

9,13,14,15 DDR_SMA[0..13]  DDR_SMA[0..13]
9,13,14,15 DDR_SCKE[0..3]  DDR_SCKE[0..3]

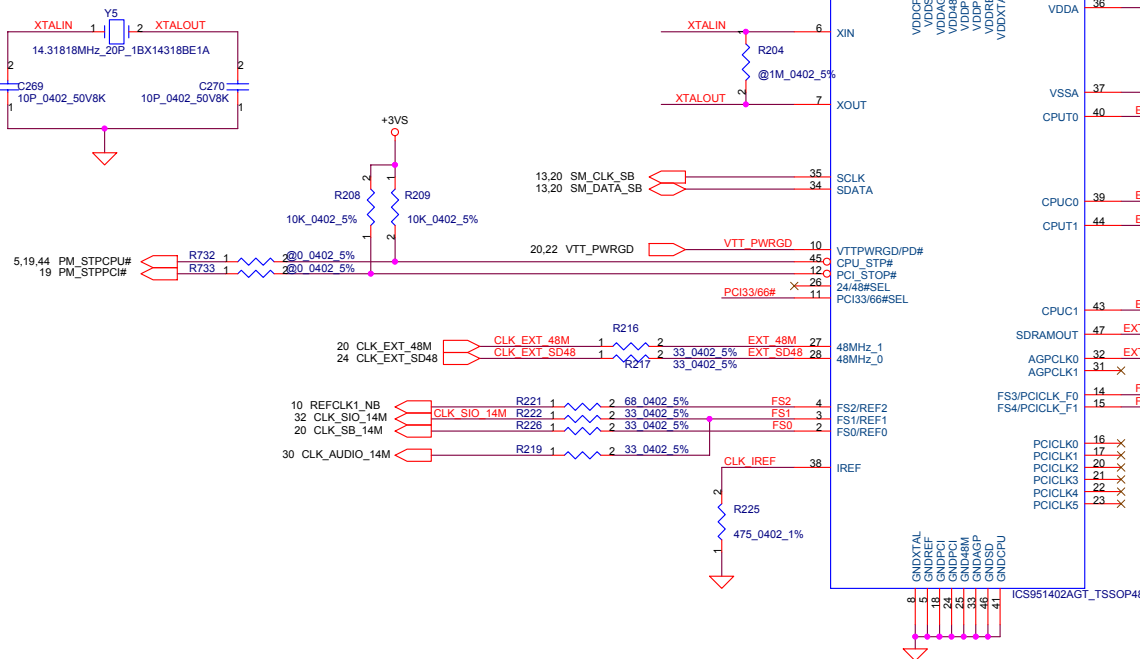
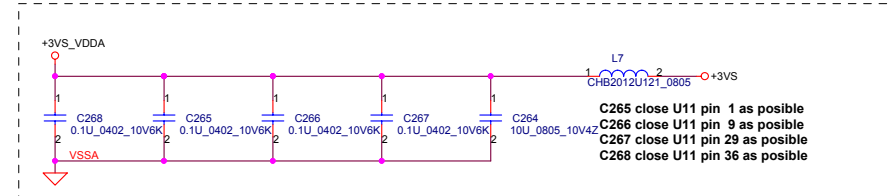
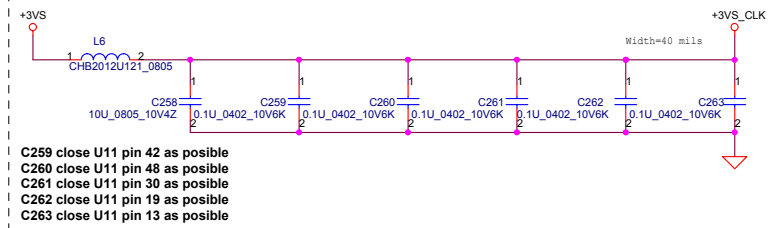
9,13,14 DDR_DQ[0..63]  DDR_DQ[0..63]
9,13,14 DDR_DQS[0..7]  DDR_DQS[0..7]

9,13,14 DDR_DM[0..7]  DDR_DM[0..7]



Title	
DDR-SODIMM Decoupling	
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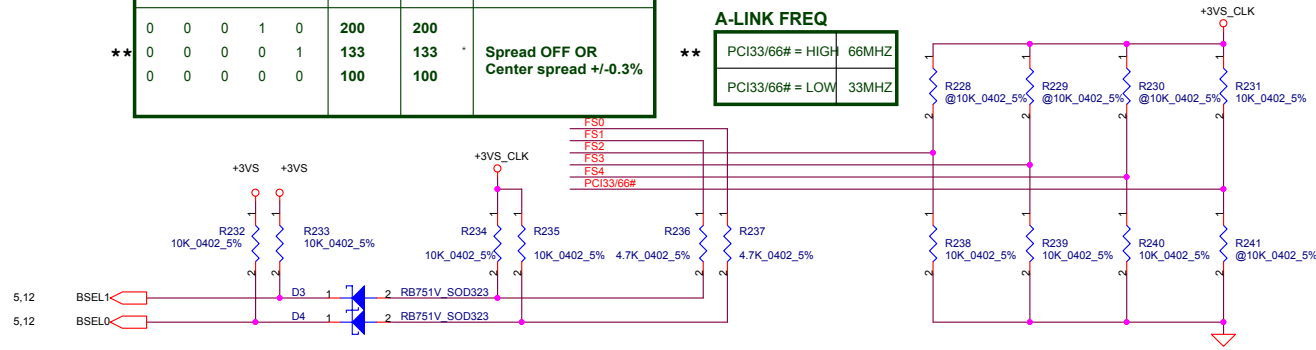
CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled
0	0	0	1	0	200	200	
0	0	0	0	1	133	133	Spread OFF OR Center spread +/-0.3%
0	0	0	0	0	100	100	

Note: 0 = PULL LOW
1 = PULL HIGH

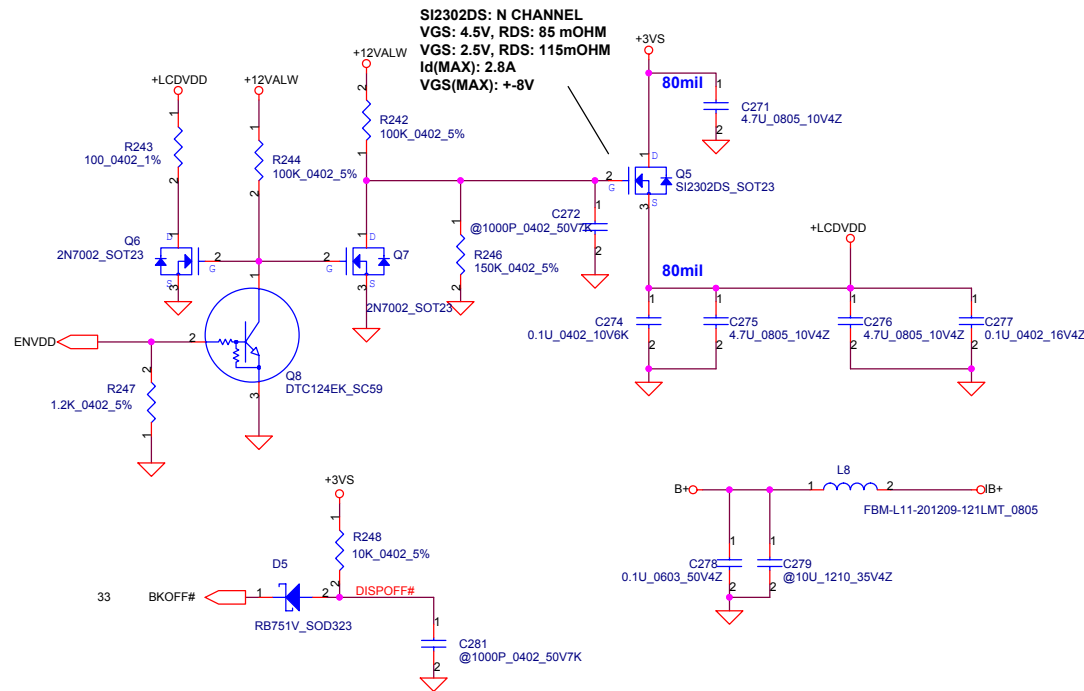
A-LINK FREQ

PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

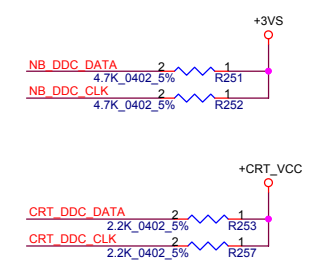
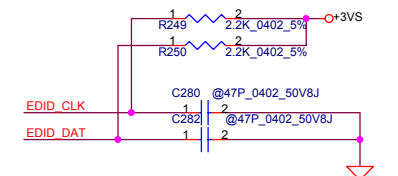
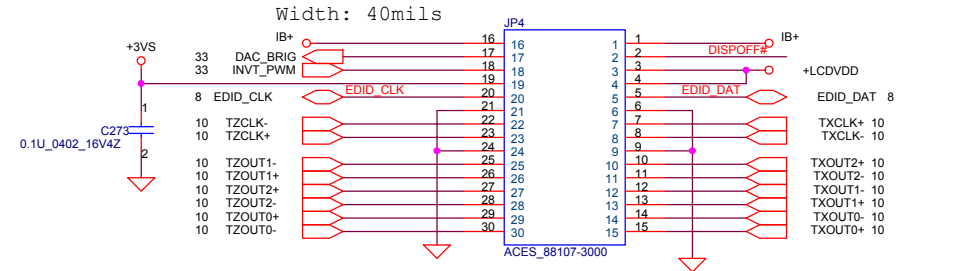
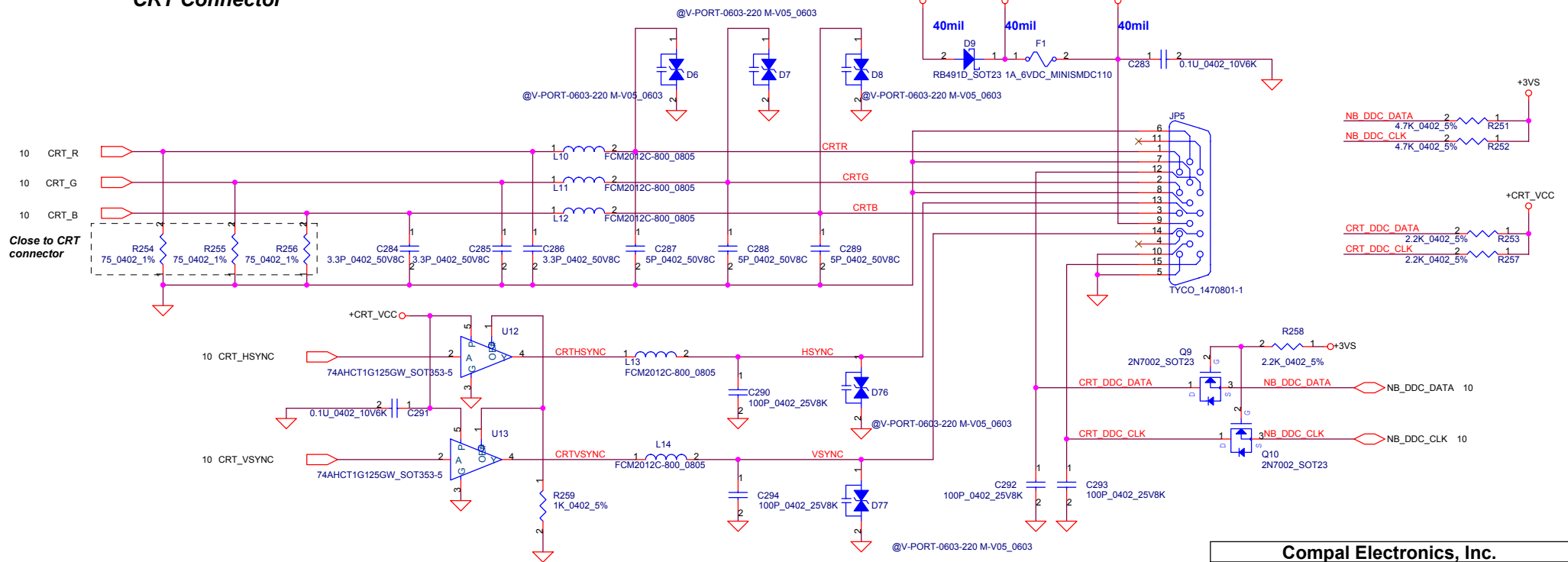


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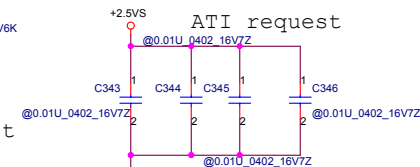
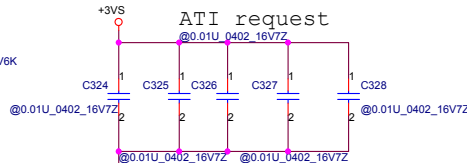
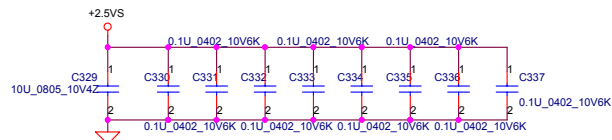
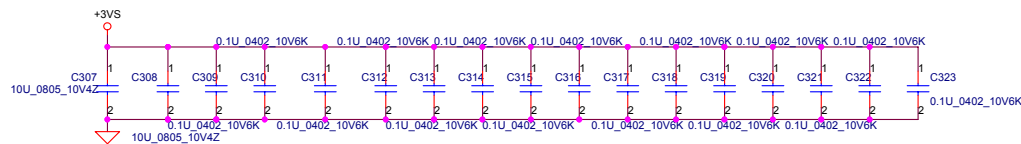
Clock Generator



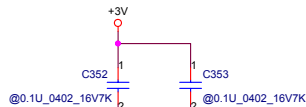
CRT Connector



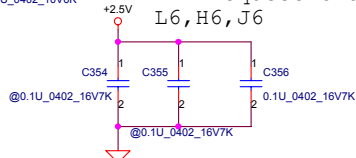
GPOC3#	GPOC2#	GPIO1			
RAM_SEL2	RAM_SEL1	RAM_SEL0	Size	Vendor	Cells
0	0	0	256M(16X16)	SAM	8
0	0	1	256M(16X16)	HYN	8
0	1	0	256M(16X16)	Elpida	8
0	1	1	256M(16X16)	Inficon	8
1	0	0	512M(32X16)	SAM	8
1	0	1	512M(32X16)	HYN	8
1	1	0	512M(32X16)	Elpida	8
1	1	1	512M(32X16)	Inficon	8



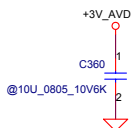
ATI request



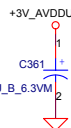
ATI request CLOSE TO L6,H6,J6



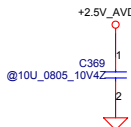
ATI request



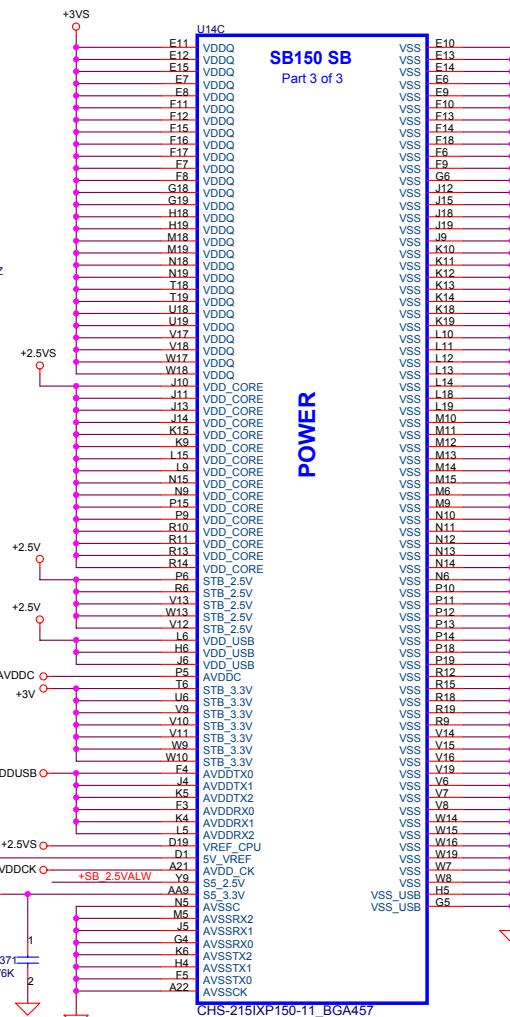
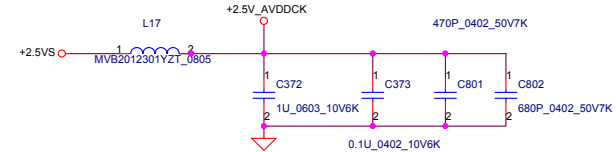
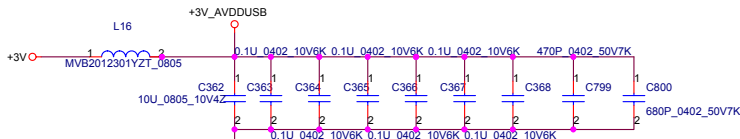
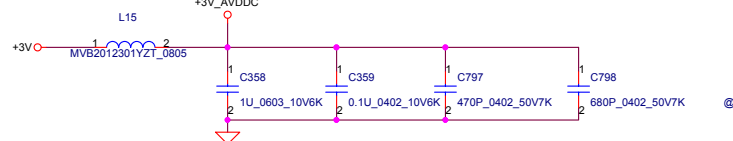
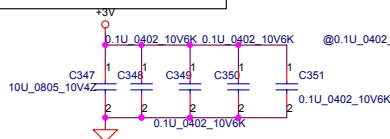
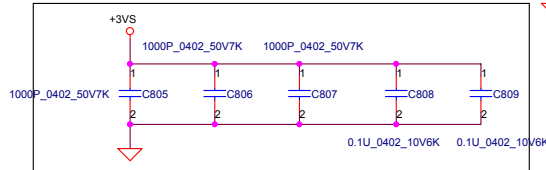
ATI request



ATI request



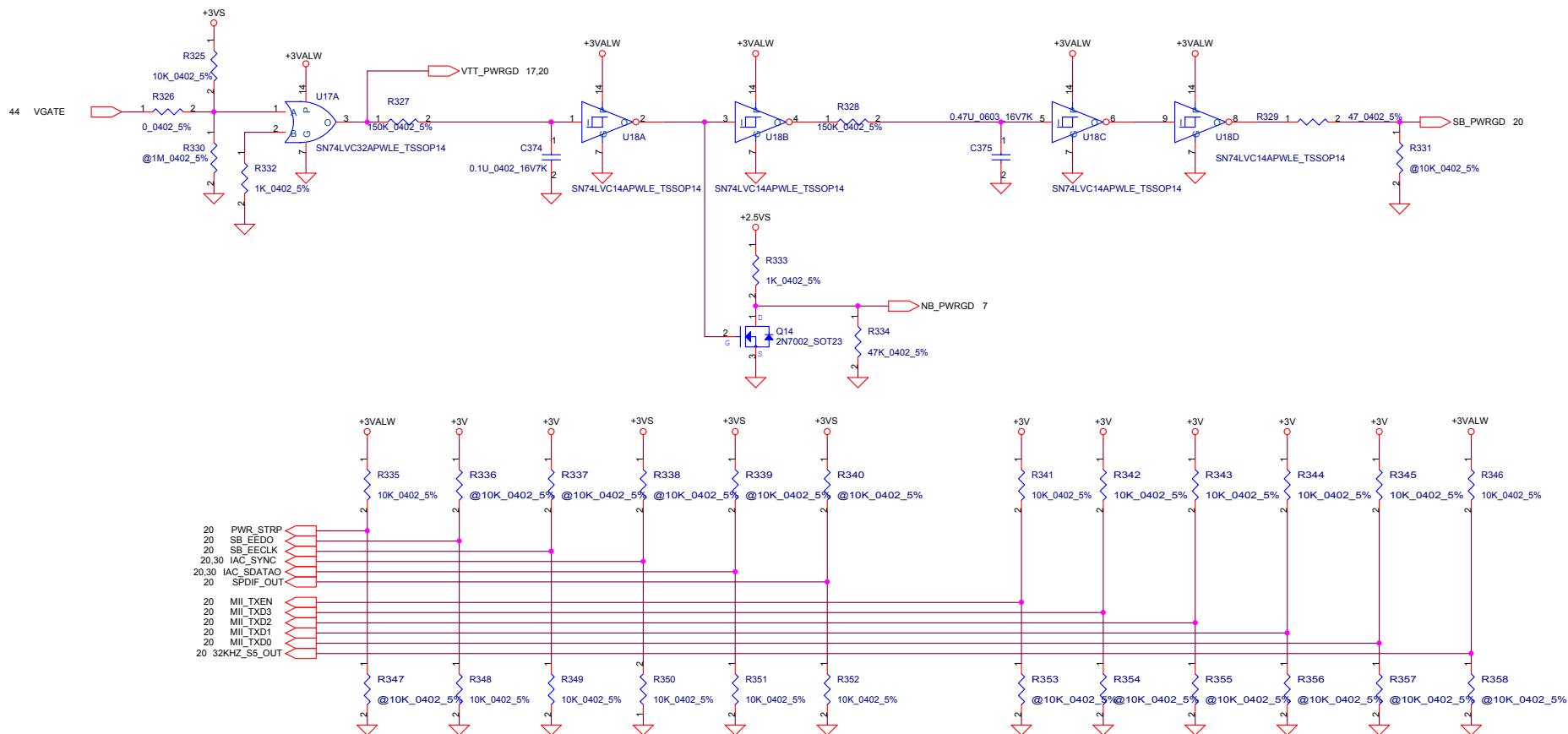
Add for EMI



POWER

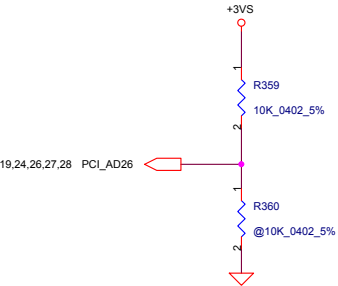
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Title	IXP150(3/4) - PWR
Document Number	IXP150-2301
Date	Thursday, April 08, 2004
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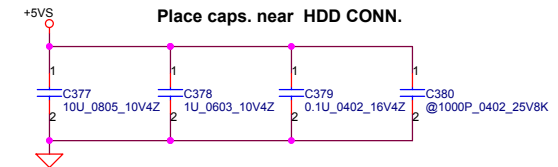
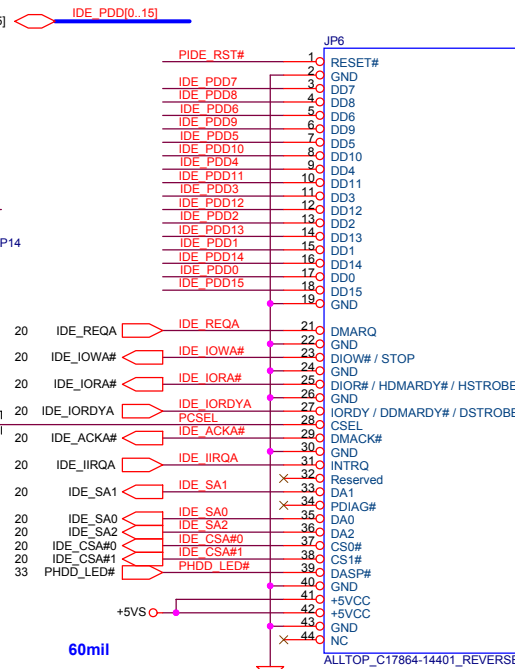
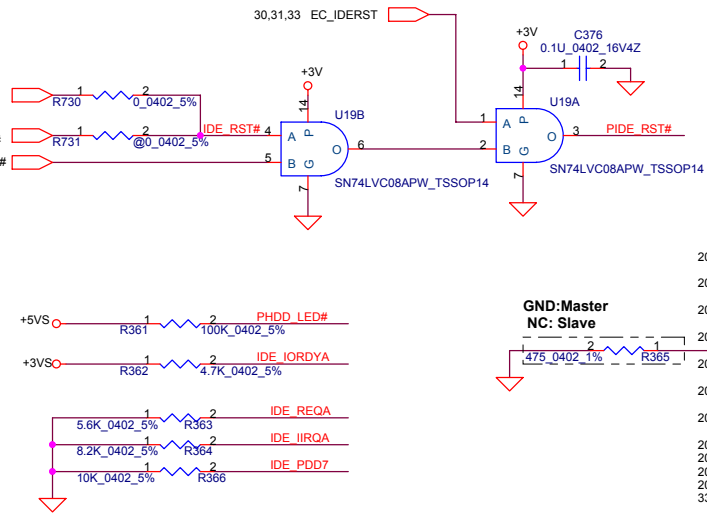
REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



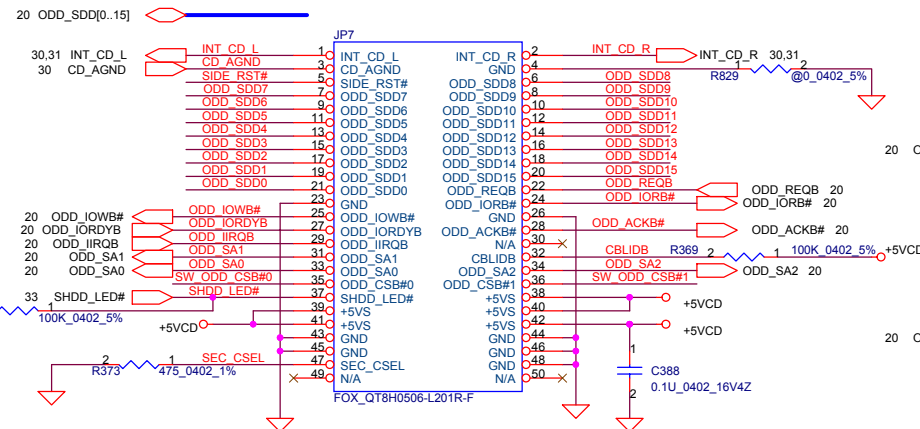
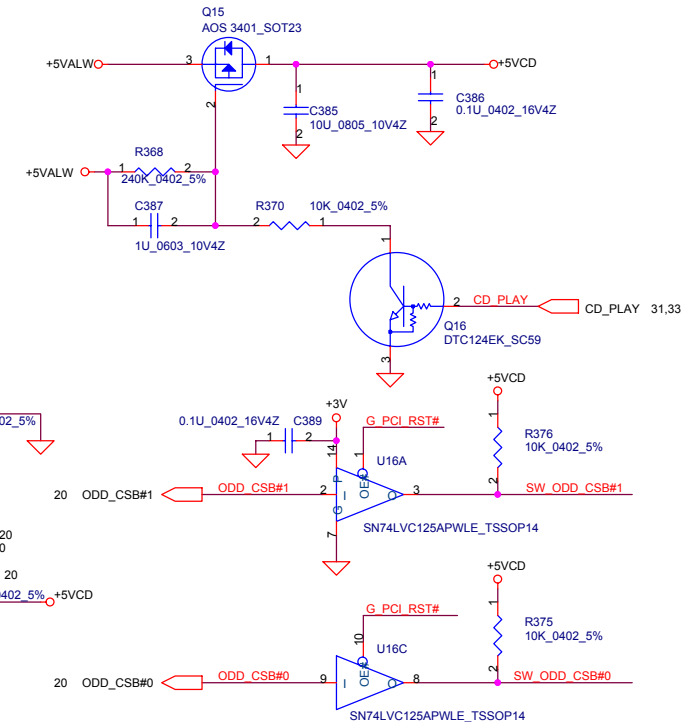
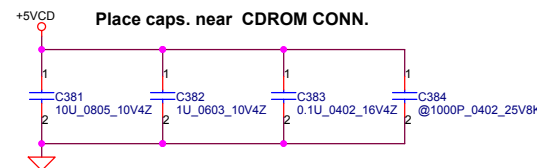
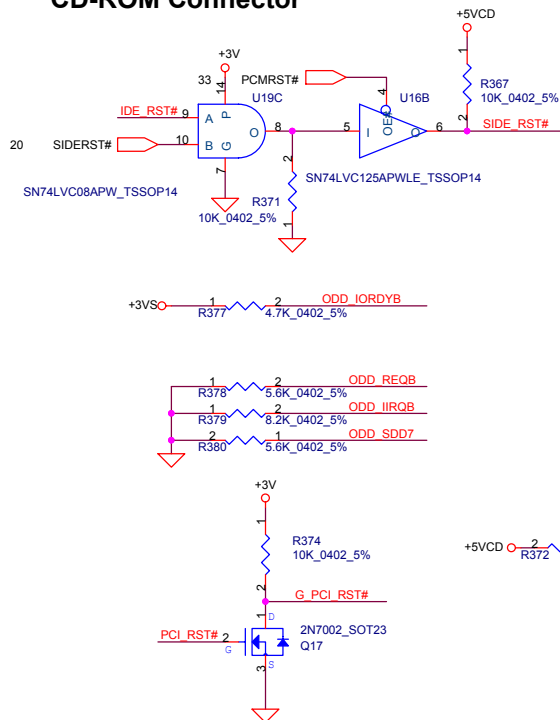
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HDD Connector



Net width should be 60mil wide

CD-ROM Connector



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IDE/CDROM CONN.

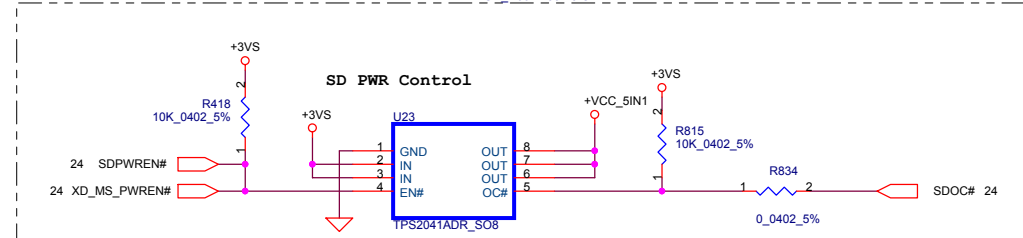
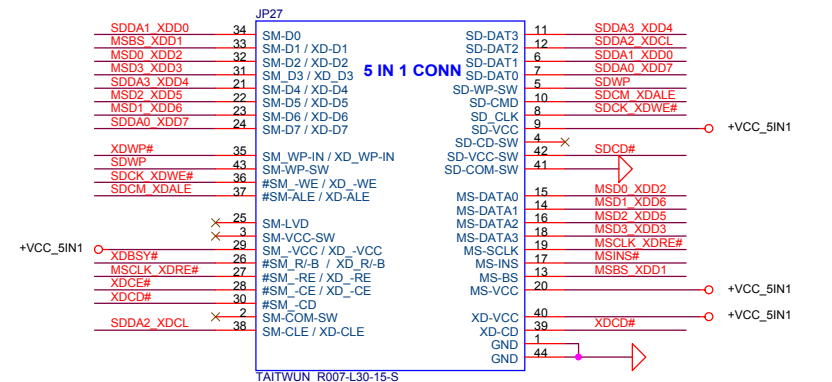
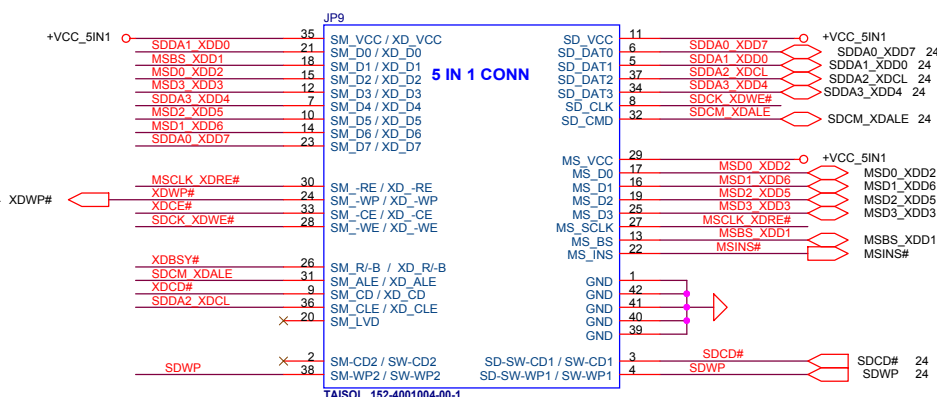
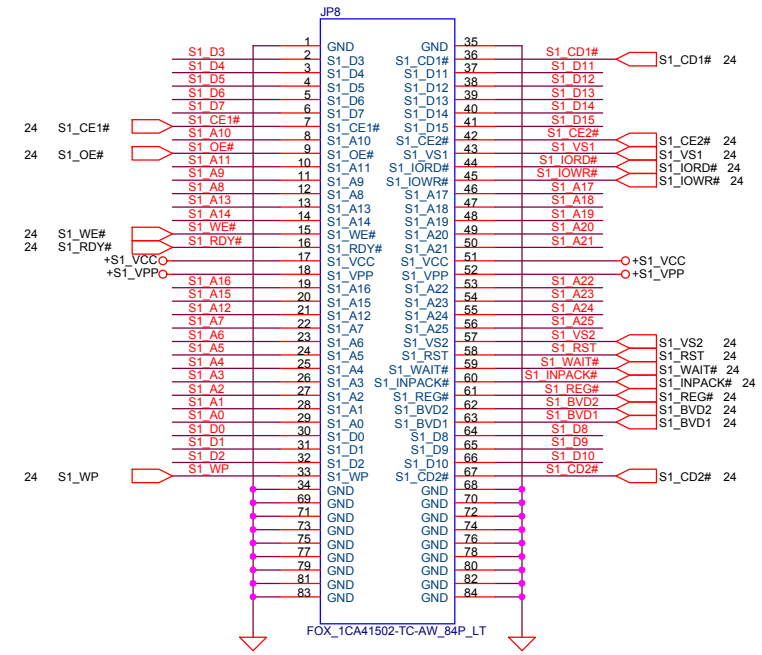
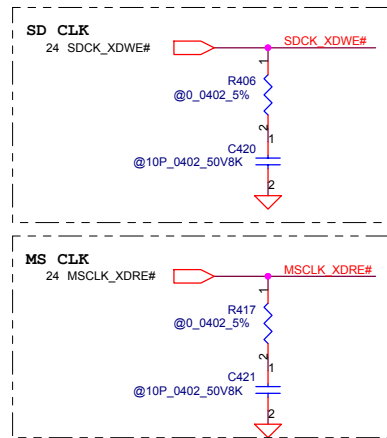
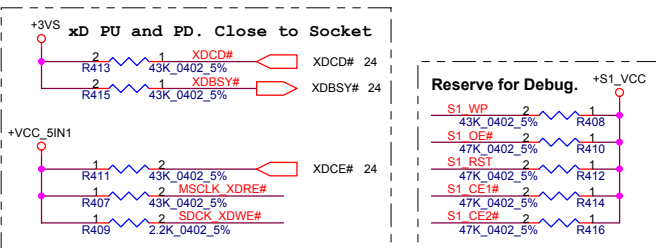
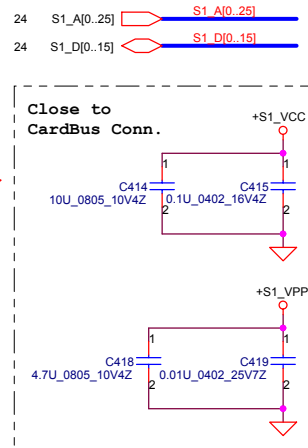
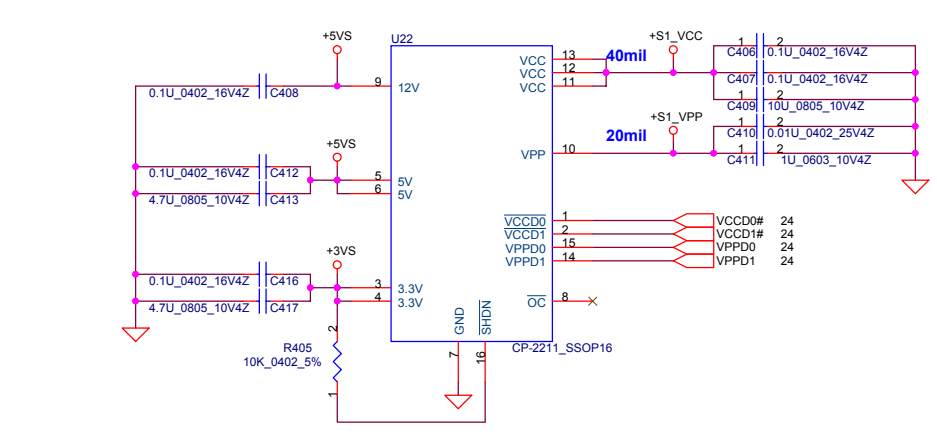
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CONFIDENTIAL
SIGNATURE OF R&D
Date: _____

PCMCIA Power Controller

CardBus Socket

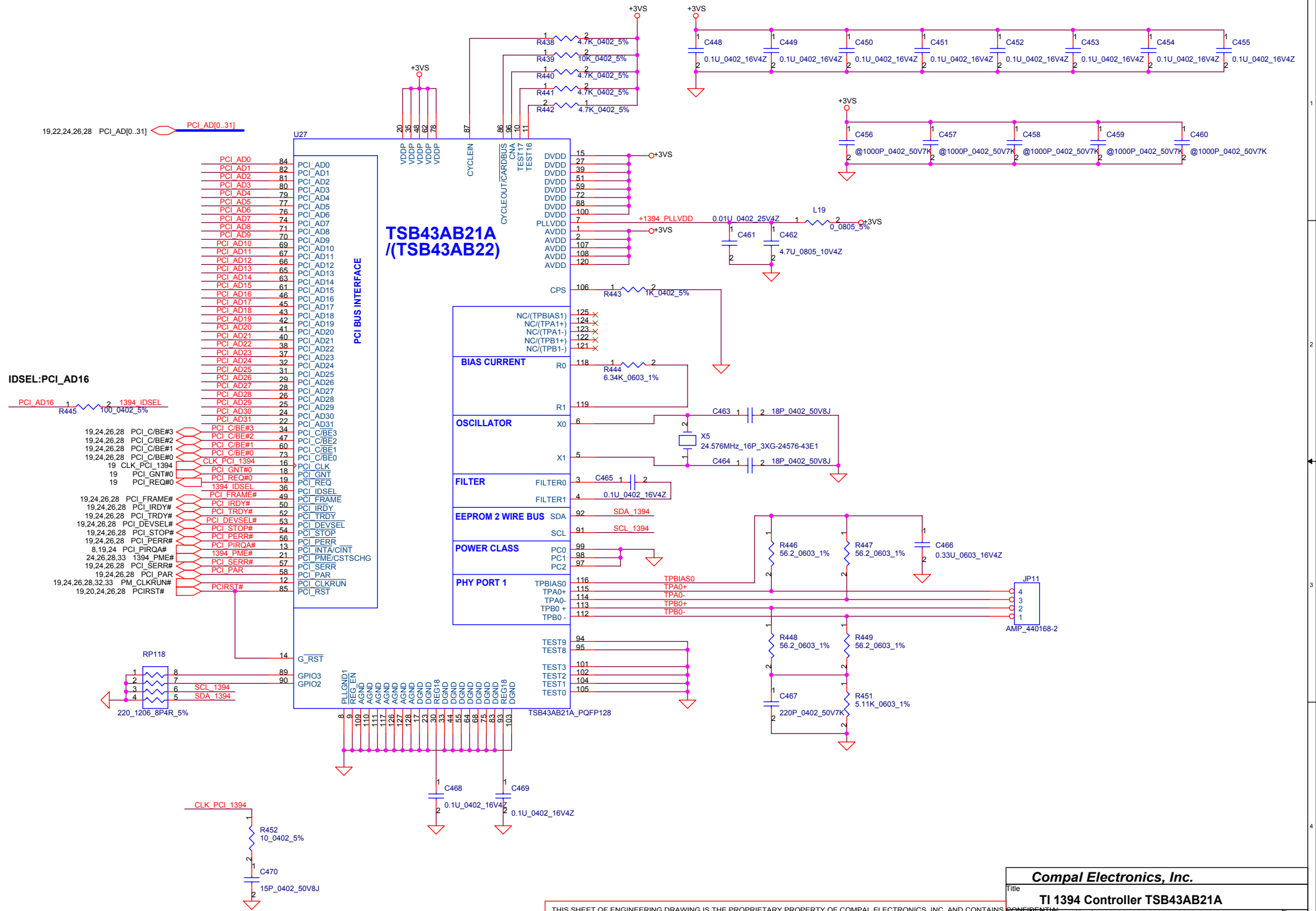
**TSB43AB21A
(/TSB43AB22)**

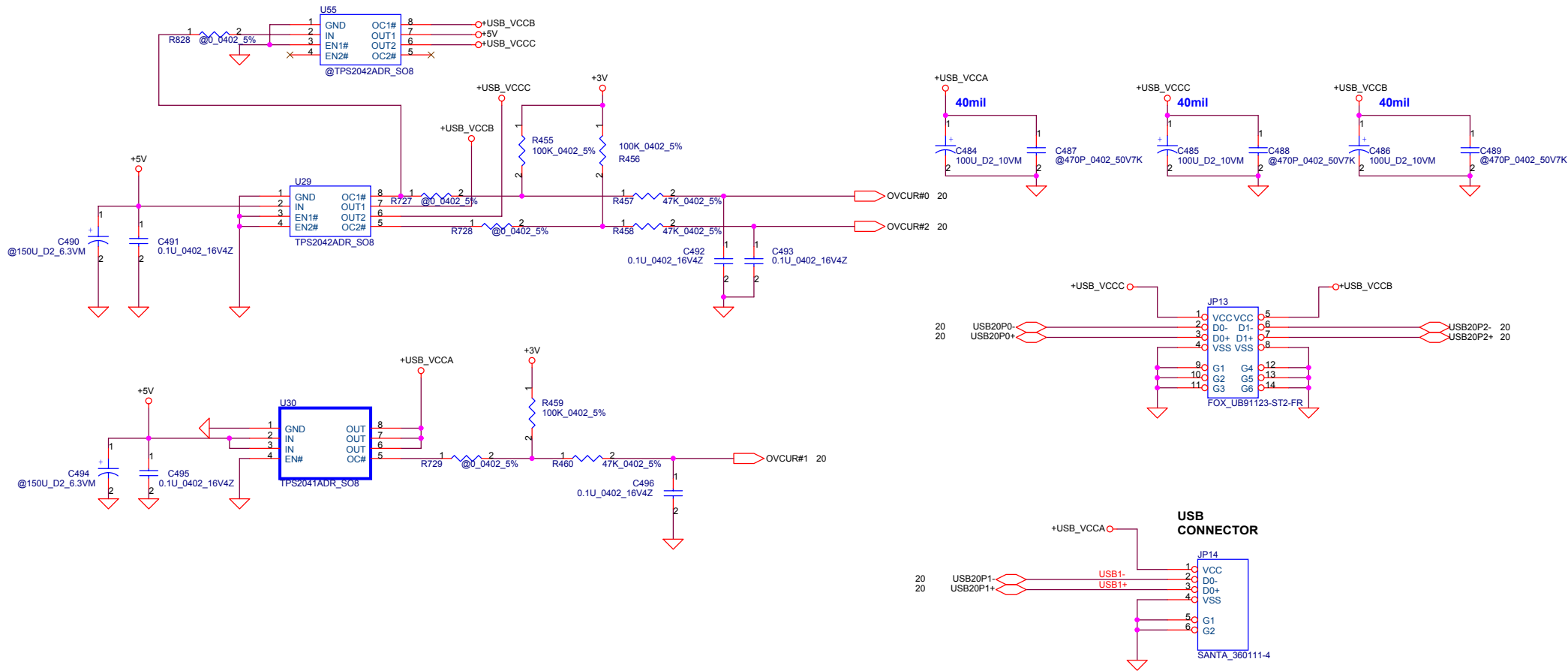
PCI BUS INTERFACE

NC/(TPBIAS1)	125	X
NC/(TPA1+)	124	X
NC/(TPA1-)	123	X
NC/(TPB1+)	122	X
NC/(TPB1-)	121	X

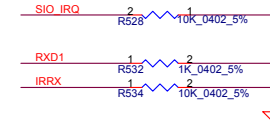
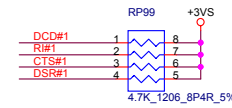
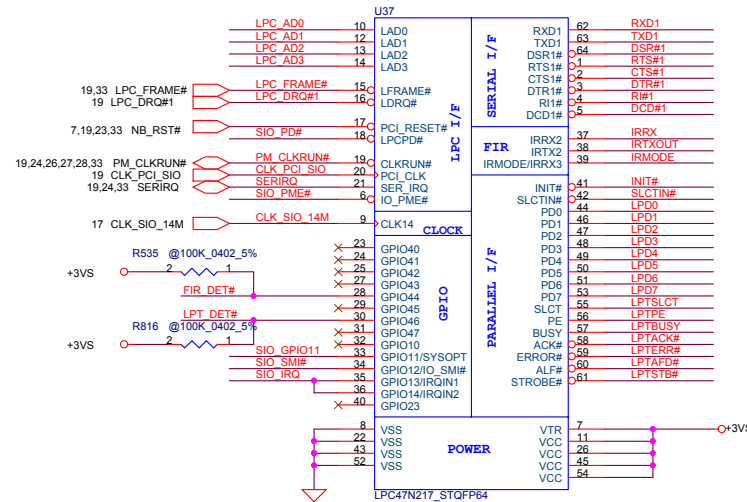
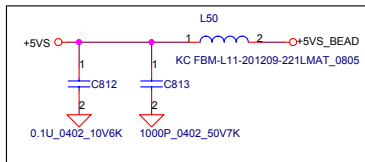
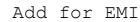
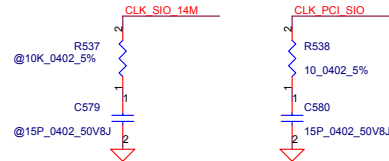
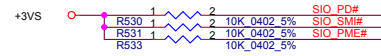
BIAS CURRENT	R0	R444	6.34K_0603_1%
OSCILLATOR	R1		
	X0		
	X1		
FILTER	FILTER0	C465	1 2 18P_0402_50V8J
	FILTER1	0.1U_0402_16V4Z	
EEPROM 2 WIRE BUS	SDA	SDA 1394	
	SCL	SCL 1394	
POWER CLASS	PC0		
	PC1		
	PC2		
PHY PORT 1	TPBIAS0	TPBIAS0	
	TPA0+	TPA0+	
	TPA0-	TPA0-	
	TPB0+	TPB0+	
	TPB0-	TPB0-	

TEST9	94	
TEST8	95	
TEST3	101	
TEST2	102	
TEST1	104	
TEST0	105	

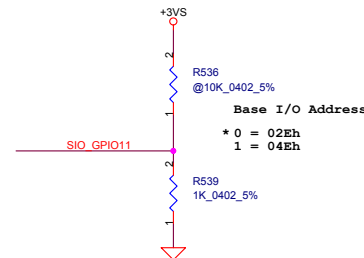
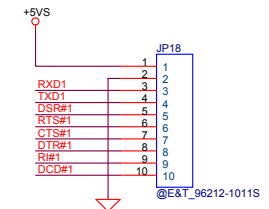




SUPER I/O SMsC LPC47N217



Serial Port for Debug

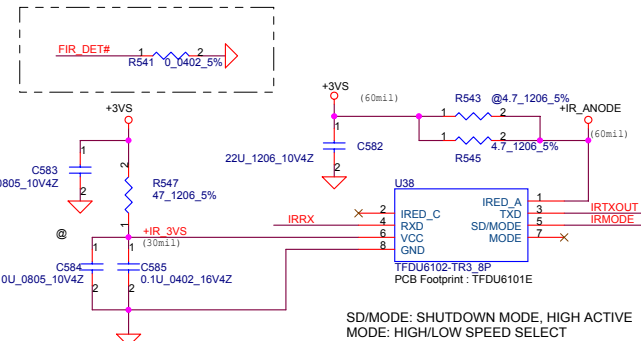


FIR Module

```

L: R POP; FIR Enable
H: R De-POP FIR Disable

```



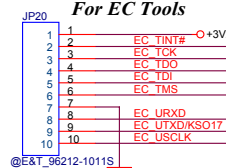
SD/MODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT

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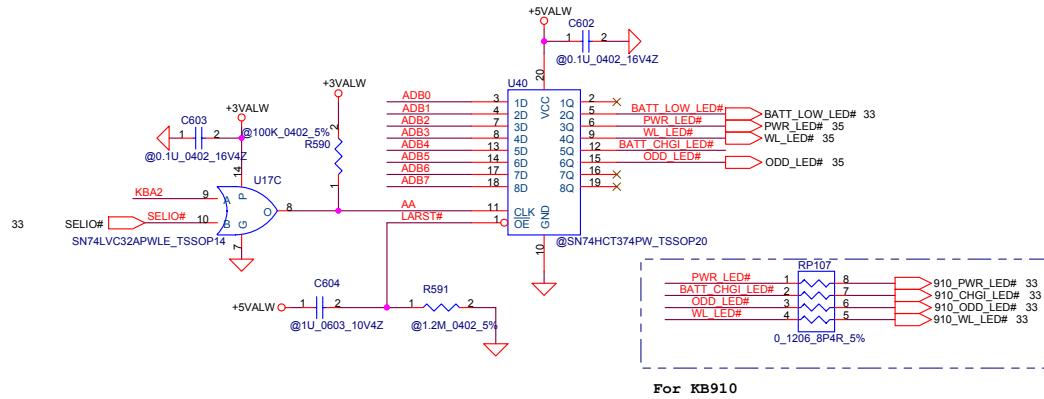
LPC-Super I/O

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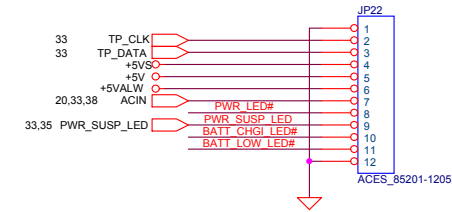
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Extension IO

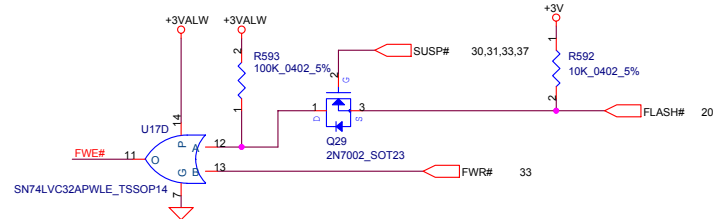


Touch Pad Connector

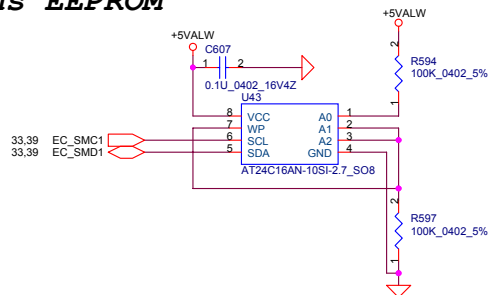


For MP3 / BUTTON LOCK / CD-PLAY

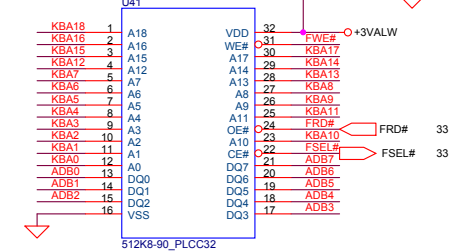
System BIOS



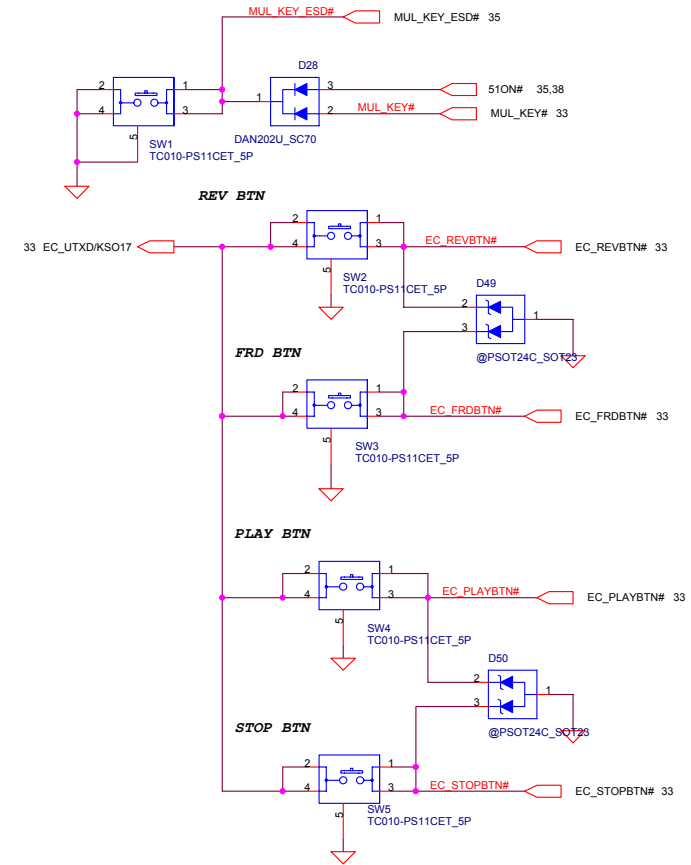
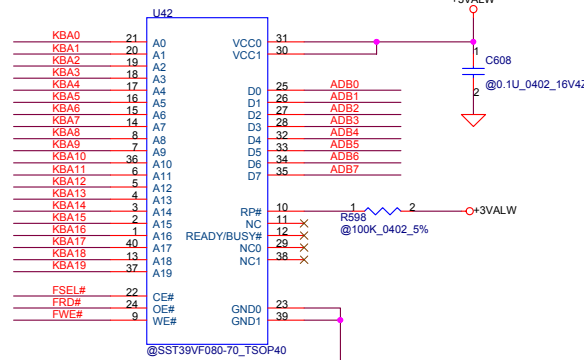
SMBus EEPROM



512KB Flash ROM



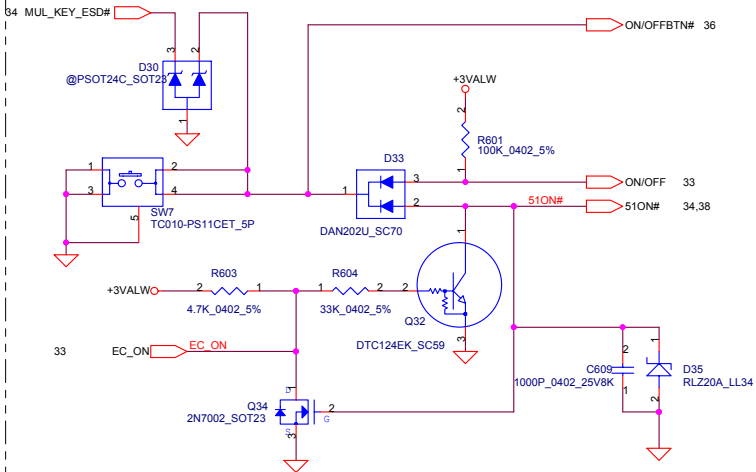
1MB Flash ROM



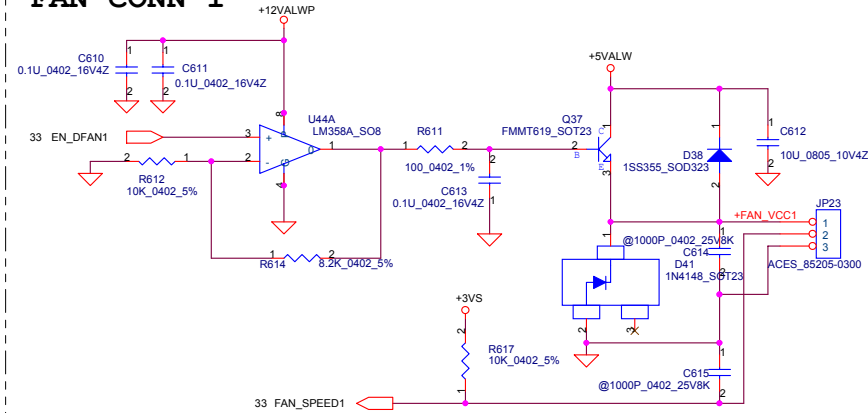
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BIOS & Ext.I/O

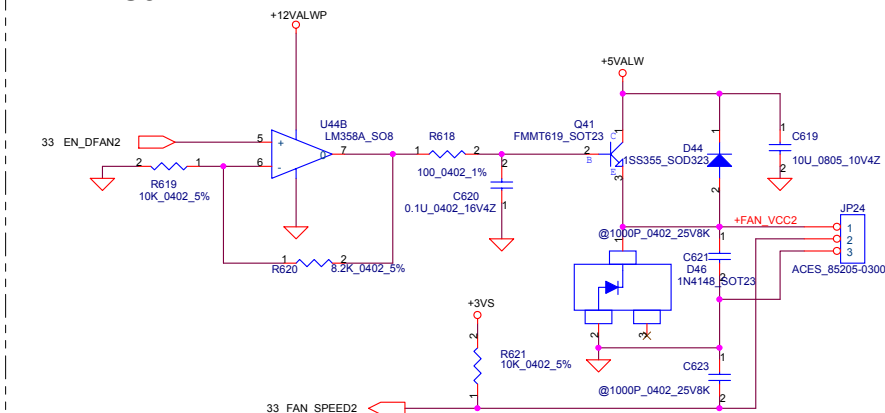
Power Button



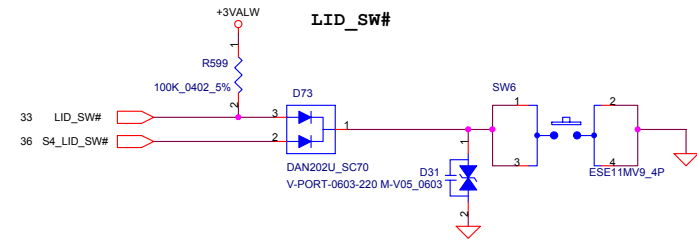
FAN CONN 1



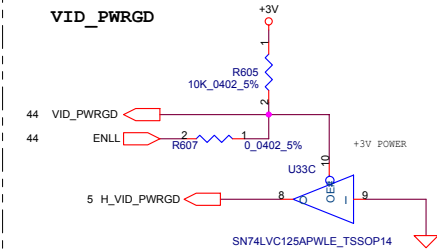
FAN CONN 2



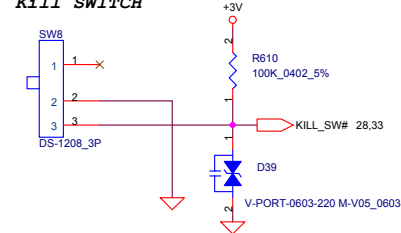
LID_SW#



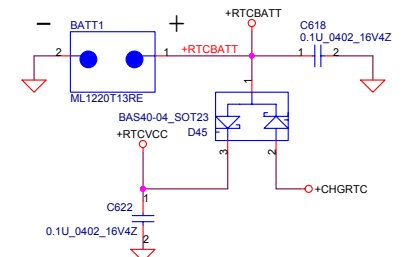
VID_PWRGD



Kill SWITCH



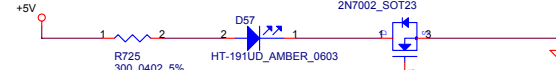
RTC BATT



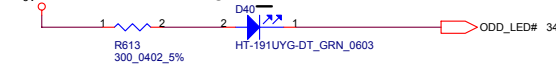
SYS. FUNT. LED--Flate PWR ON LED



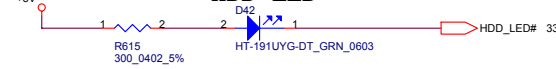
SUSP LED



ODD LED



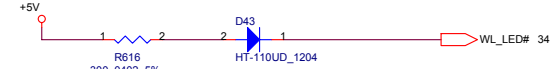
HDD LED



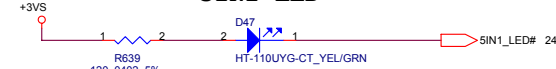
SYS. FUNT. LED--Right Angle



WL LED



5IN1 LED



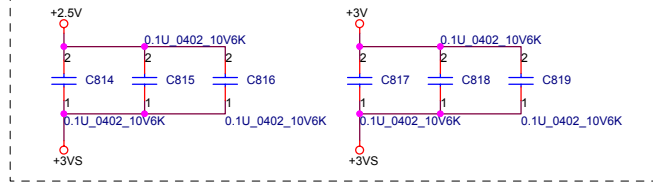
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PWRGD/Fan/PWRBTN/TP/LID.

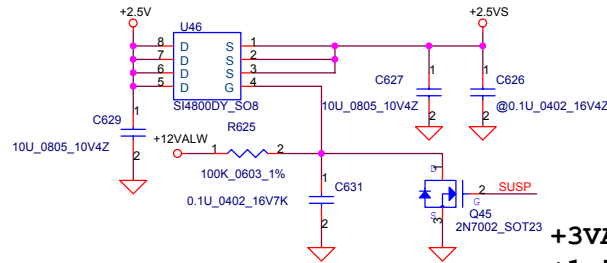
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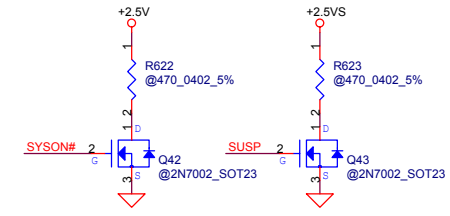
Add for EMI



+2.5V To +2.5VS Transfer

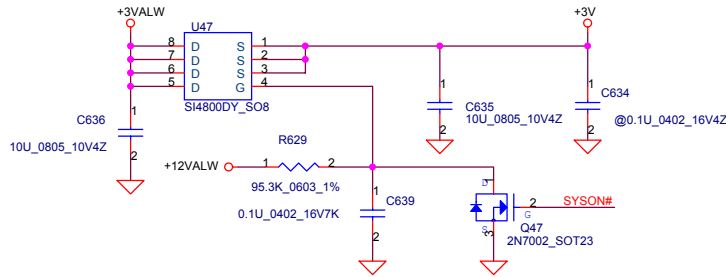


+2.5V & +2.5VS Discharge

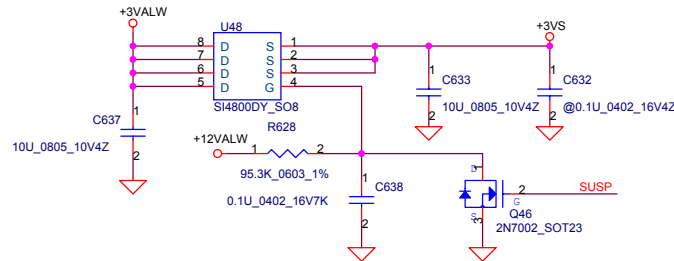


**+3VALW AND +2.5VALW MUST RISING SAME TIME
+1.5V MUST DELAY AFTER +2.5V**

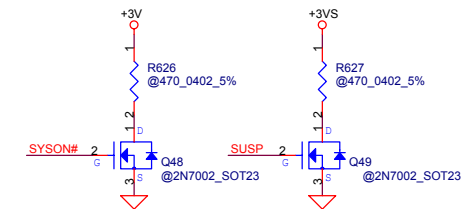
+3VALW To +3V Transfer



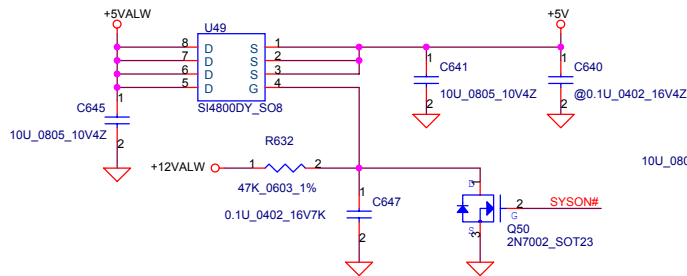
+3VALW To +3VS Transfer



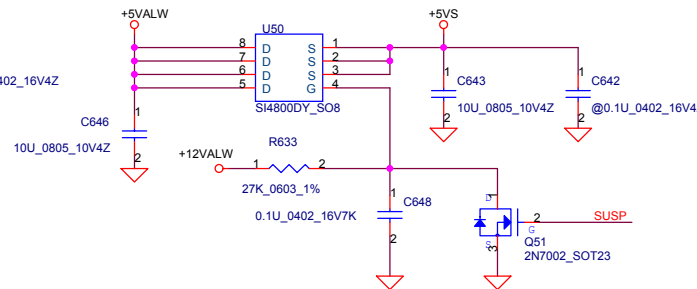
+3V & +3VS Discharge



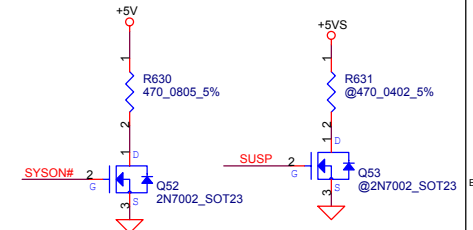
+5VALW To +5V Transfer



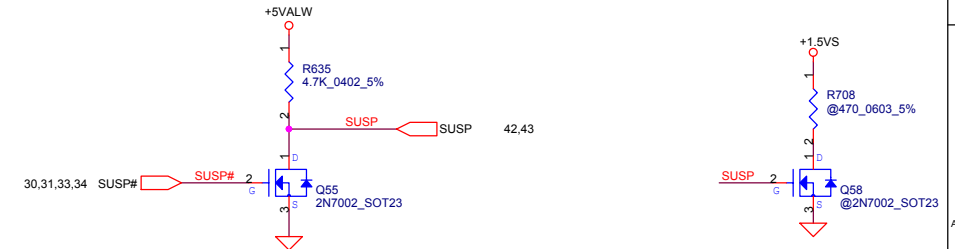
+5VALW To +5VS Transfer



+5V & +5VS Discharge



+1.5VS Discharge



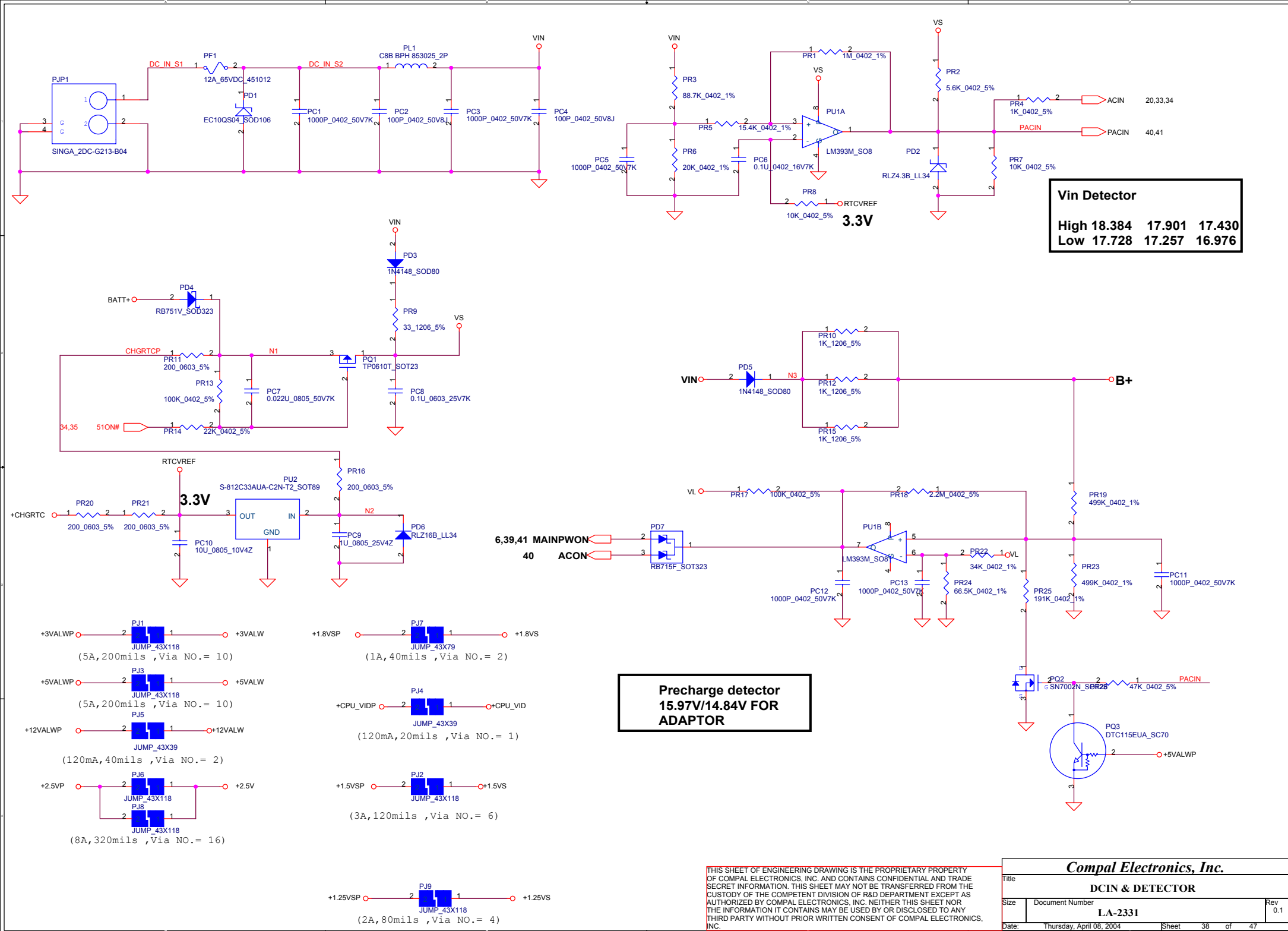
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DC-DC Circuit Interface

LA-2301

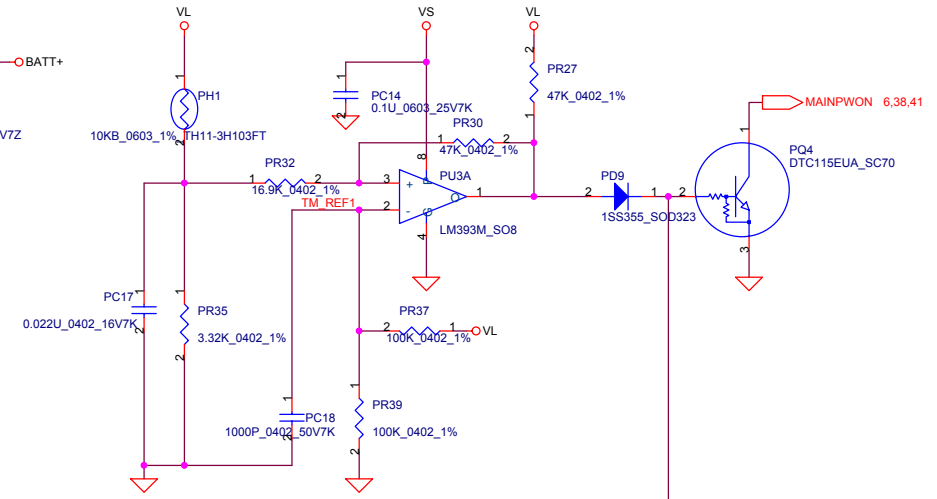
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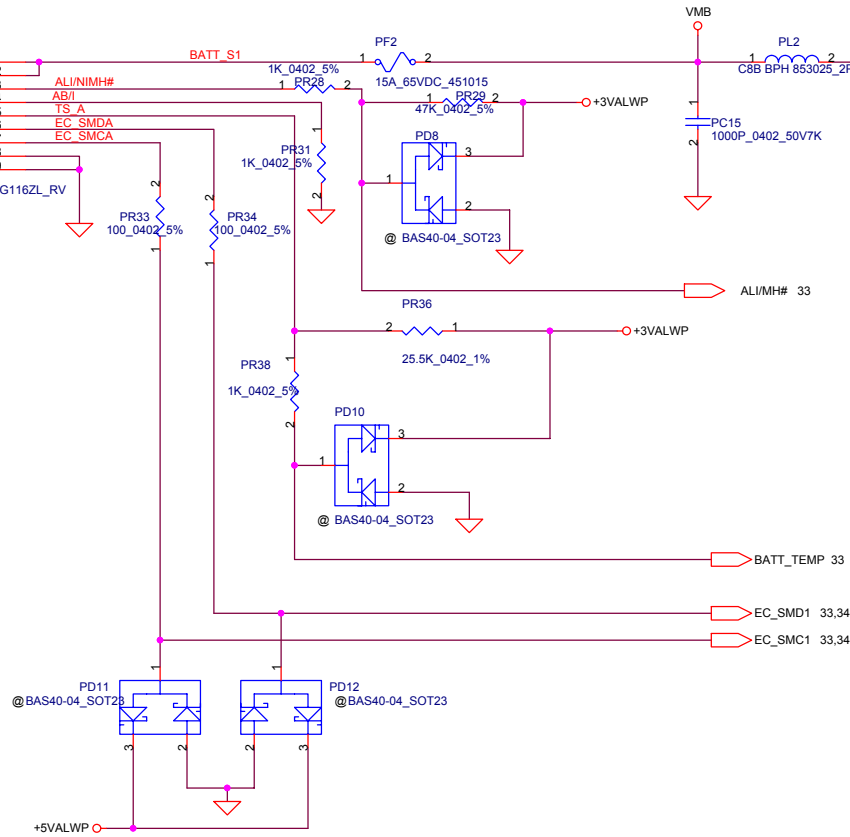
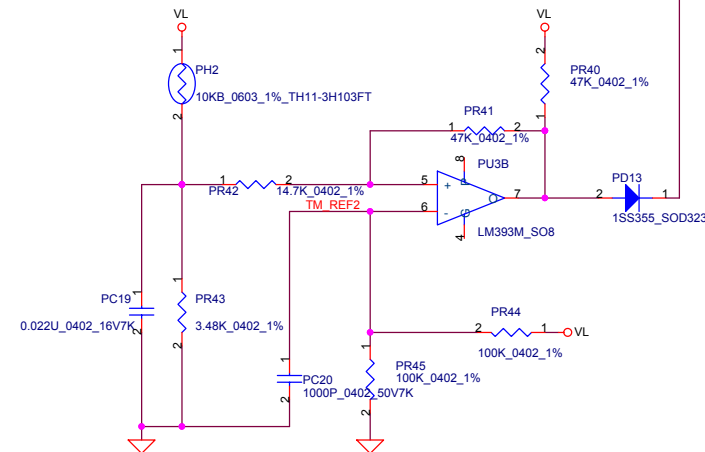
PH1 under CPU botten side :

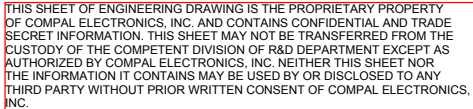
CPU thermal protection at 84 degree C
Recovery at 45 degree C

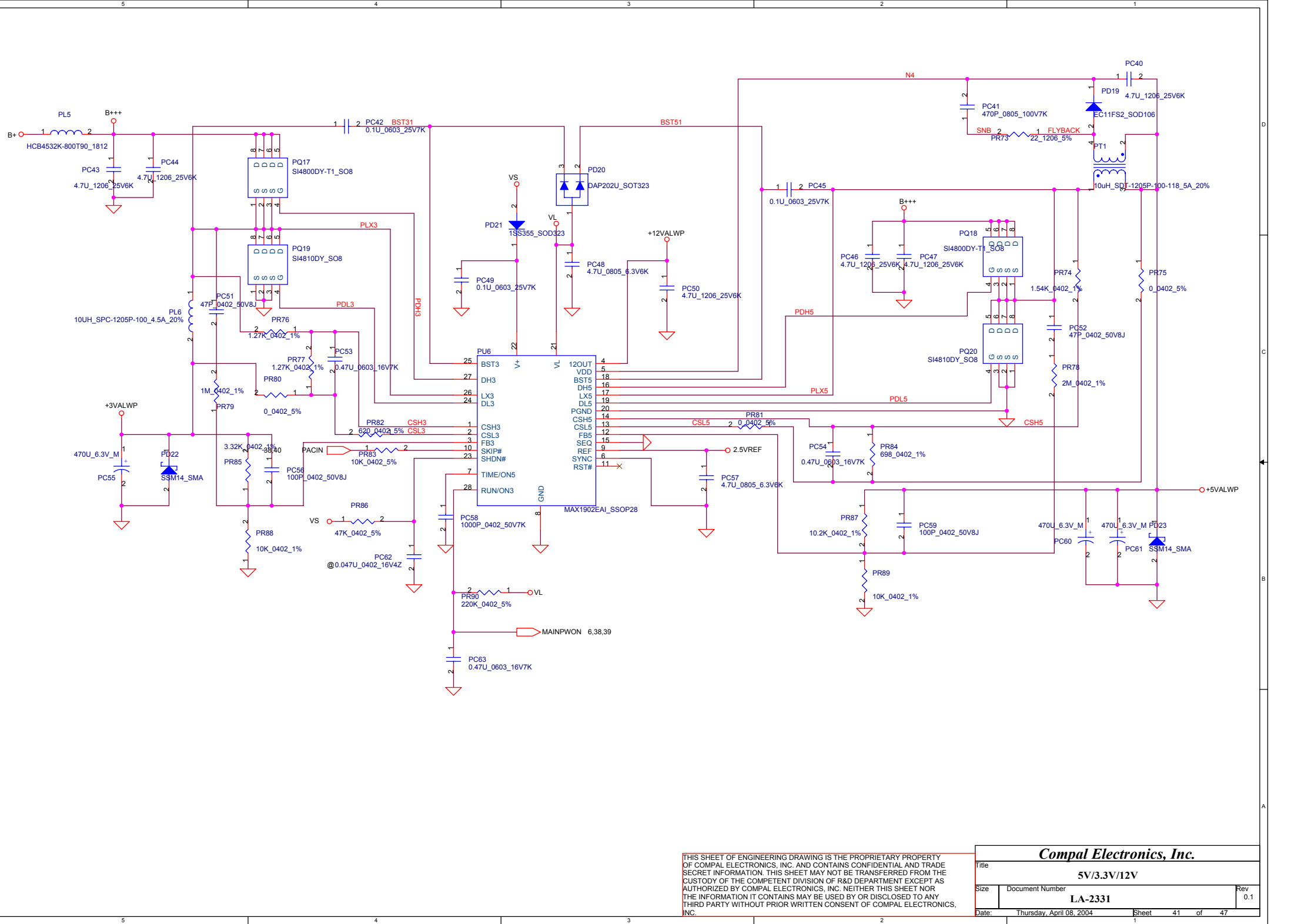


PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C
Recovery at 45 degree C

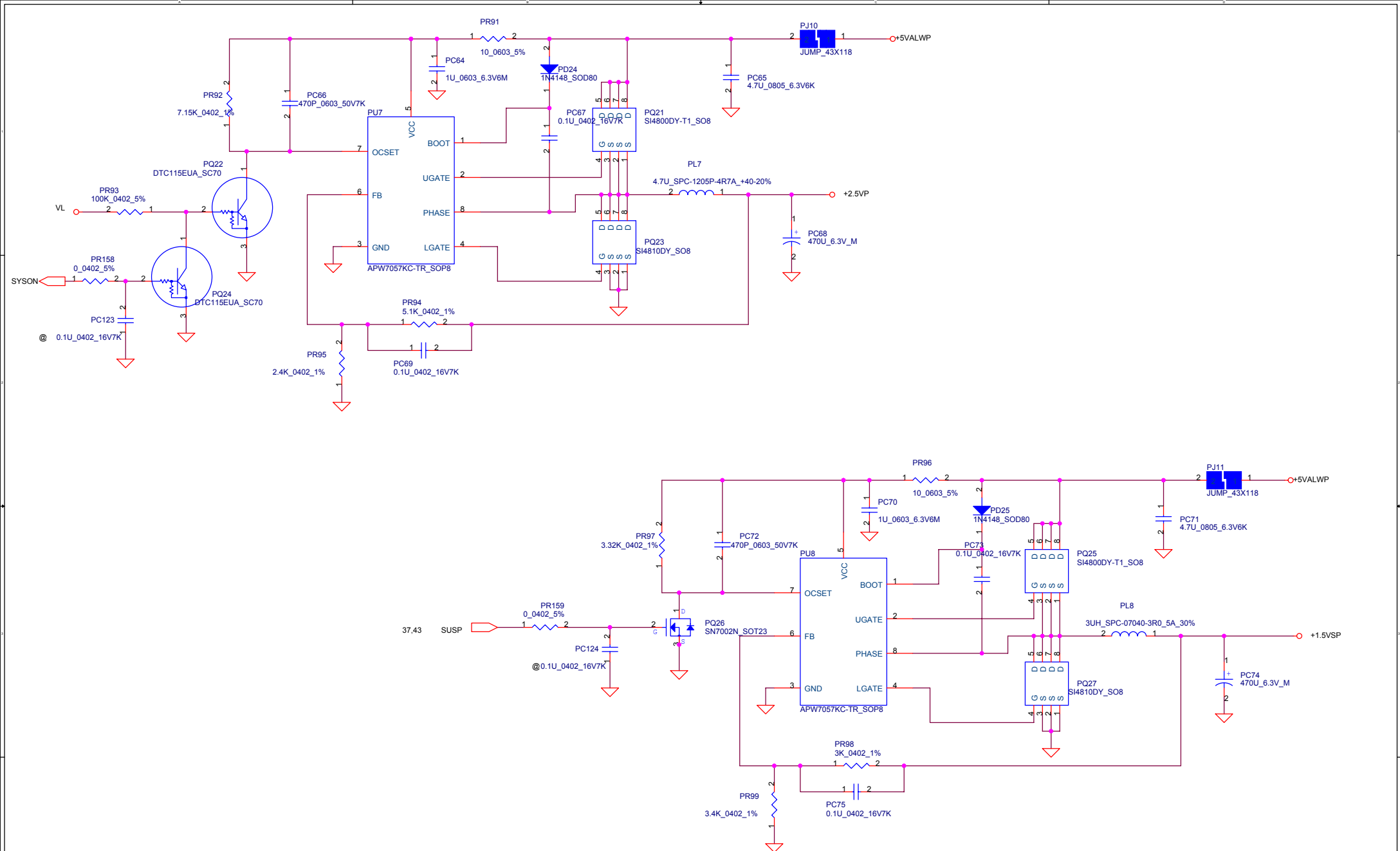






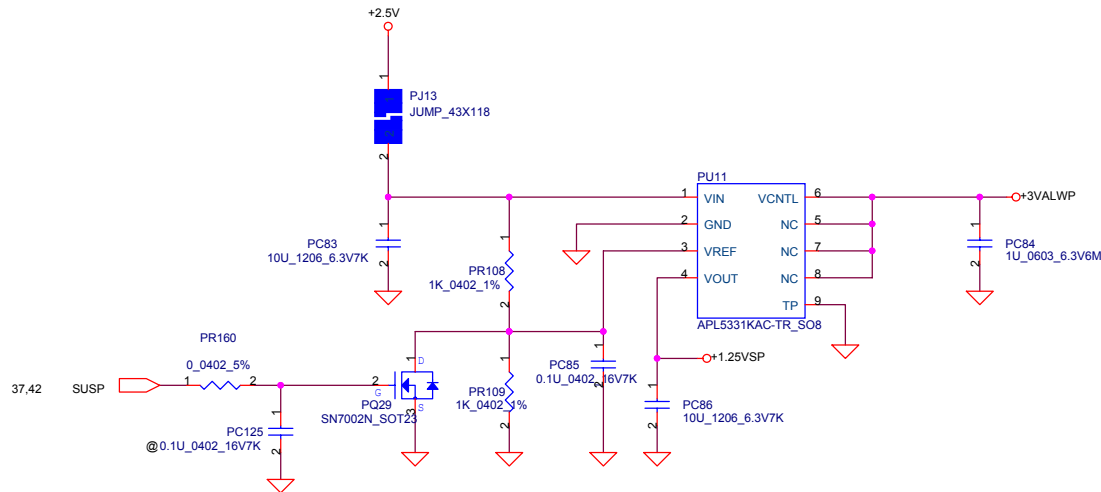
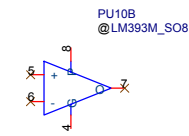
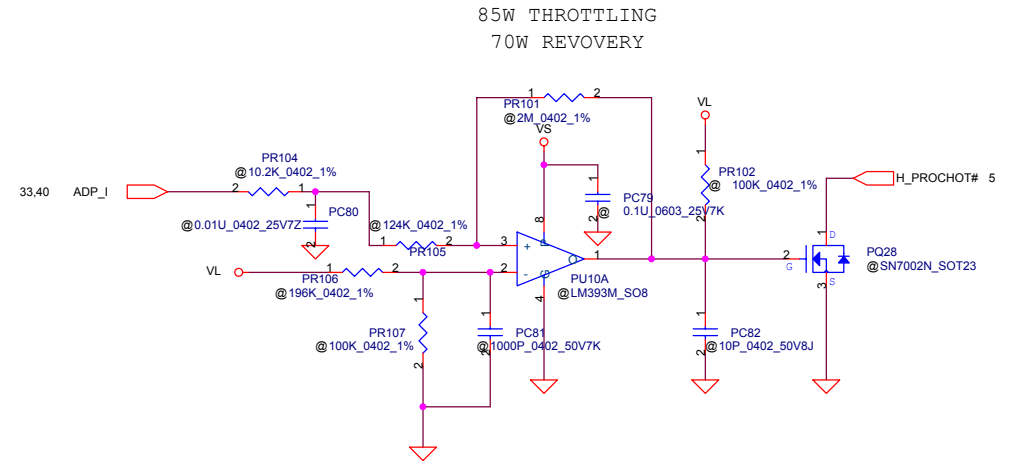
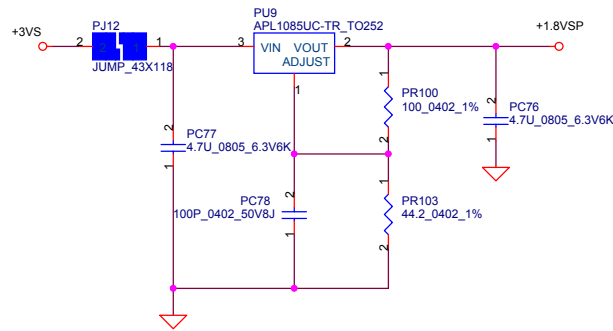
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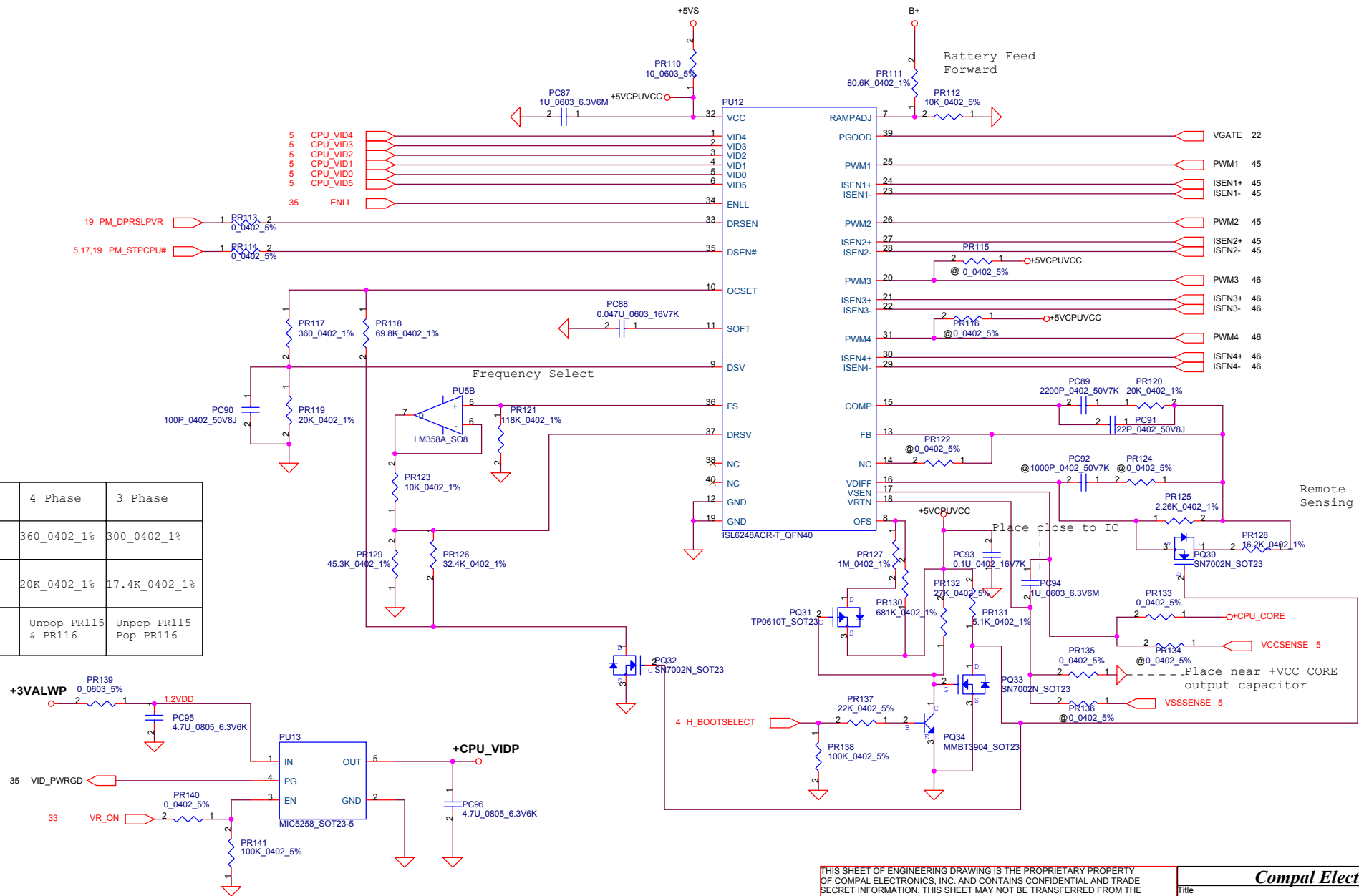
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Title		2.5V/1.5V	
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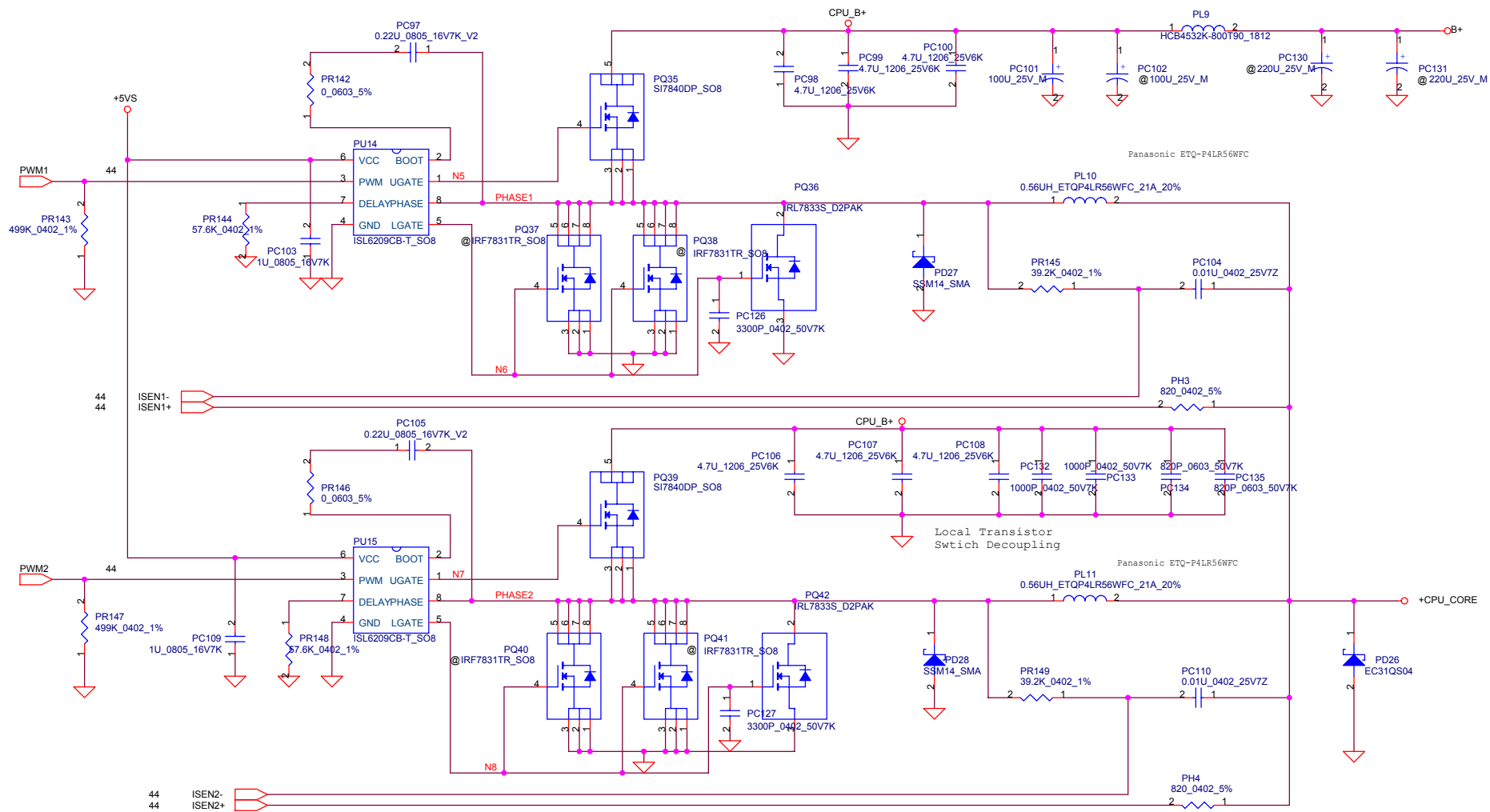
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Title		1.8V/1.25V/PROCHOT	
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	4 Phase	3 Phase
PR117	360_0402_1%	300_0402_1%
PR119	20K_0402_1%	17.4K_0402_1%
Others	Unpop PR115 & PR116	Unpop PR115 Pop PR116

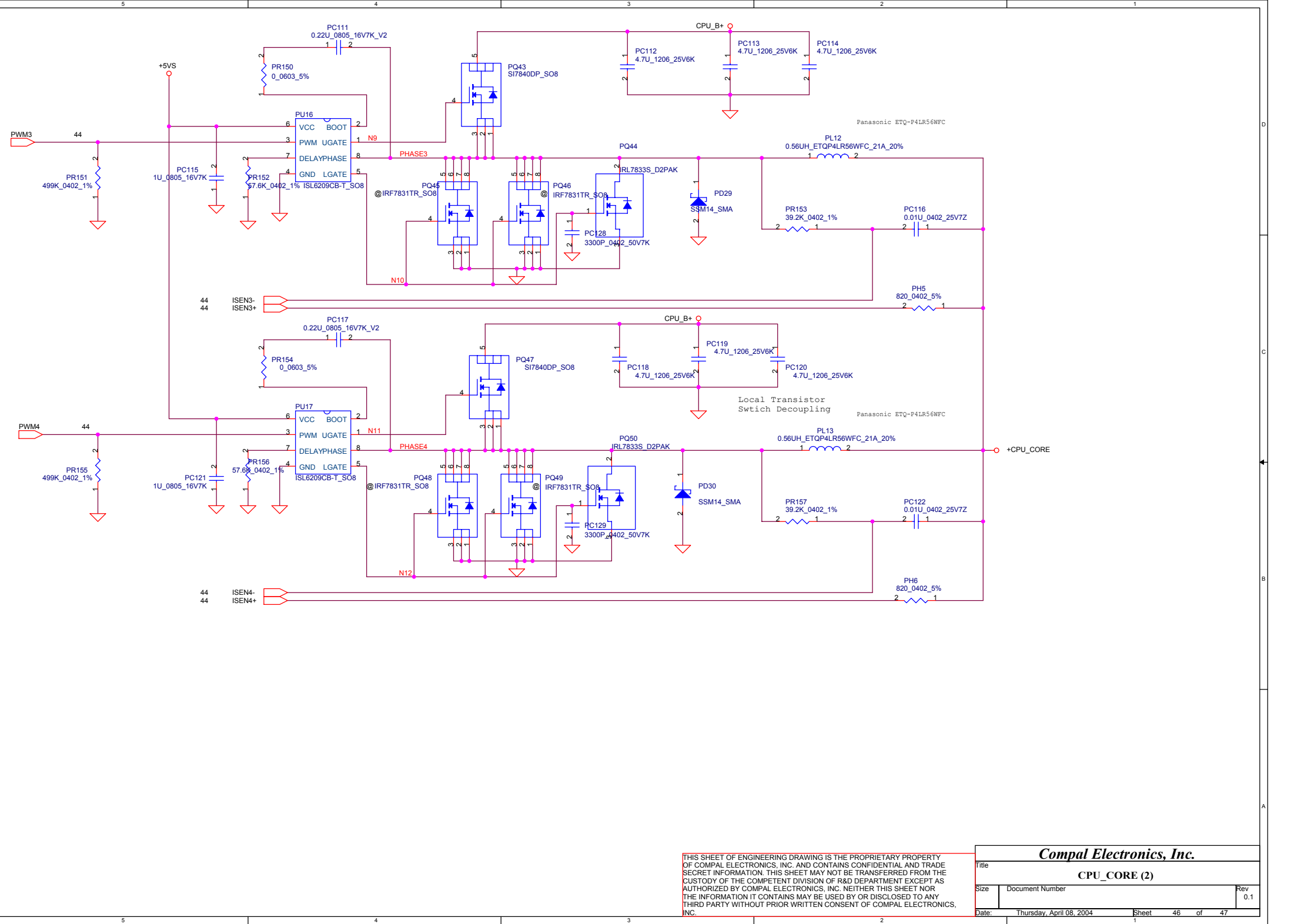


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CPU_CORE (2)		
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CPU_CORE (2)			
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Date	Page	Description	Location
03/10	P.14,15	Add 16 Cap in on board DDR chip VDD pin	ADD C775 ~ C790
03/10	P.18	Del L9 & change L8 to bead for EMI	DEL L9 Change L8 to Bead
03/15	P.19	Redefine On board DDR strap pin	DEL R643, R646
03/15	P.21	Change SB +2.5valw power design	DEL R641 ADD Q60,D72
03/15	P.25	Change 5 In 1 connector	Change JP9
03/15	P.32	Add Parallel Port detect strap pin	ADD R817
03/15	P.27	Change 1394 connector footprint	NONE
03/16	P.33	Change EC SMBus2 pull high plwer plan from +5VALW to +3V	NONE
03/16	P.36	Add Battery Hibernation circuit	ADD U54,Q61 ~ Q64,U53,D75,D74,R822,R823 ~ R827,C791, C794,C792, C793,R820,R821
04/5	P.23	Change ODD Conn. layout	
04/5	P.23	Change ODD Conn. layout	

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Title		
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