

# *HAZ00/HTW01*

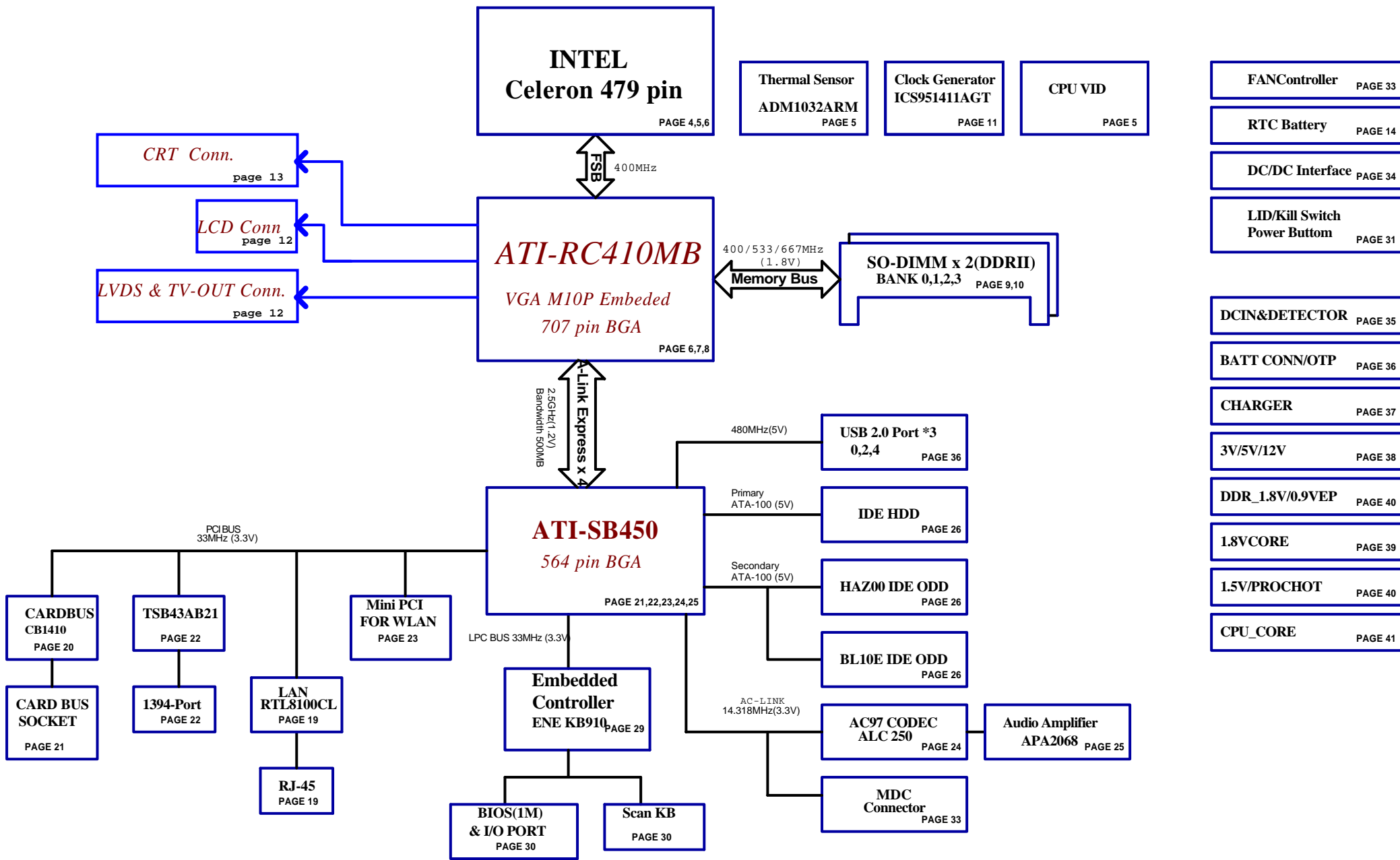
## LA-2861 REV 1.0 Schematic

UFC-PGA Dothan/ RC410MD(RC410MB) / SB450

2005-07-11 Rev.1.0

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# HAZ00 & HTW01 LA-2861 FUNCTION BLOCK DIAGRAM



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	DOTHAN B	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
TI 1410	AD20	2	PIRQA/PIRQB
LAN	AD22	1	PIRQG
Mini-PCI(WLAN)	AD18	3	PIRQF/PIRQG
1394	AD16	0	PIRQA

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b

## EC SM Bus2 address

## SB450 SM Bus address

Device	Address
Clock Generator (ICS951413BGLFT)	1101 001Xb
DDR DIMM0	1010 0100b A4
DDR DIMM1	1010 0110b A6

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

## Board ID Table for AD channel

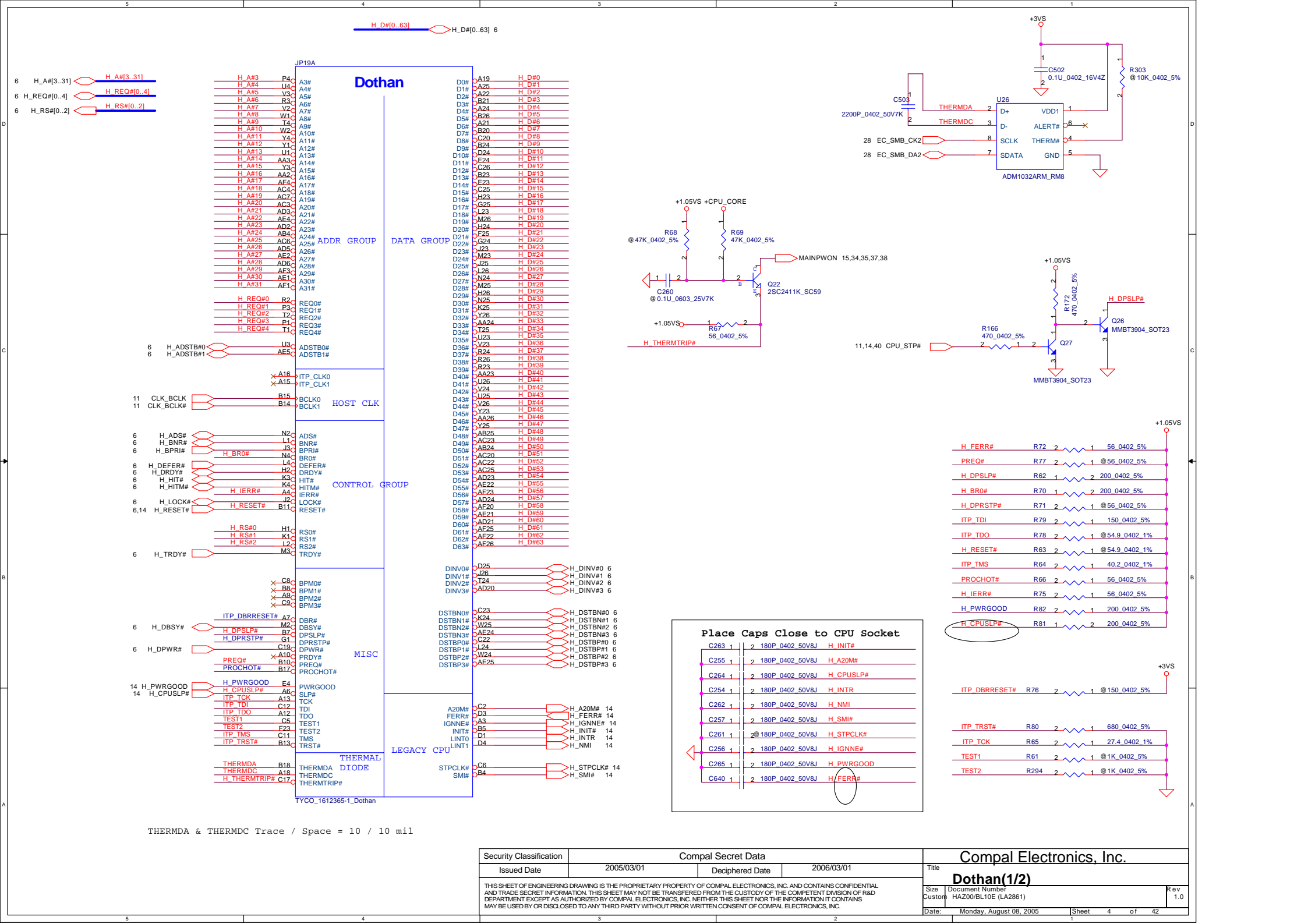
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1, 0.2
1	0.3
2	1.0
3	
4	
5	
6	
7	

SKU ID	SKU Status
0	
1	
2	
3	
4	
5	1 Buttons
6	
7	7 Buttons

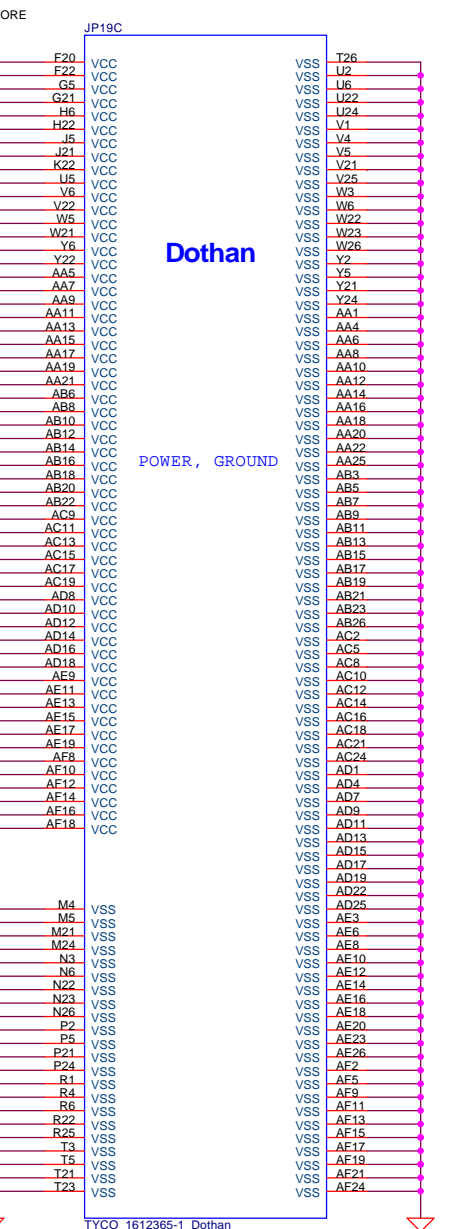
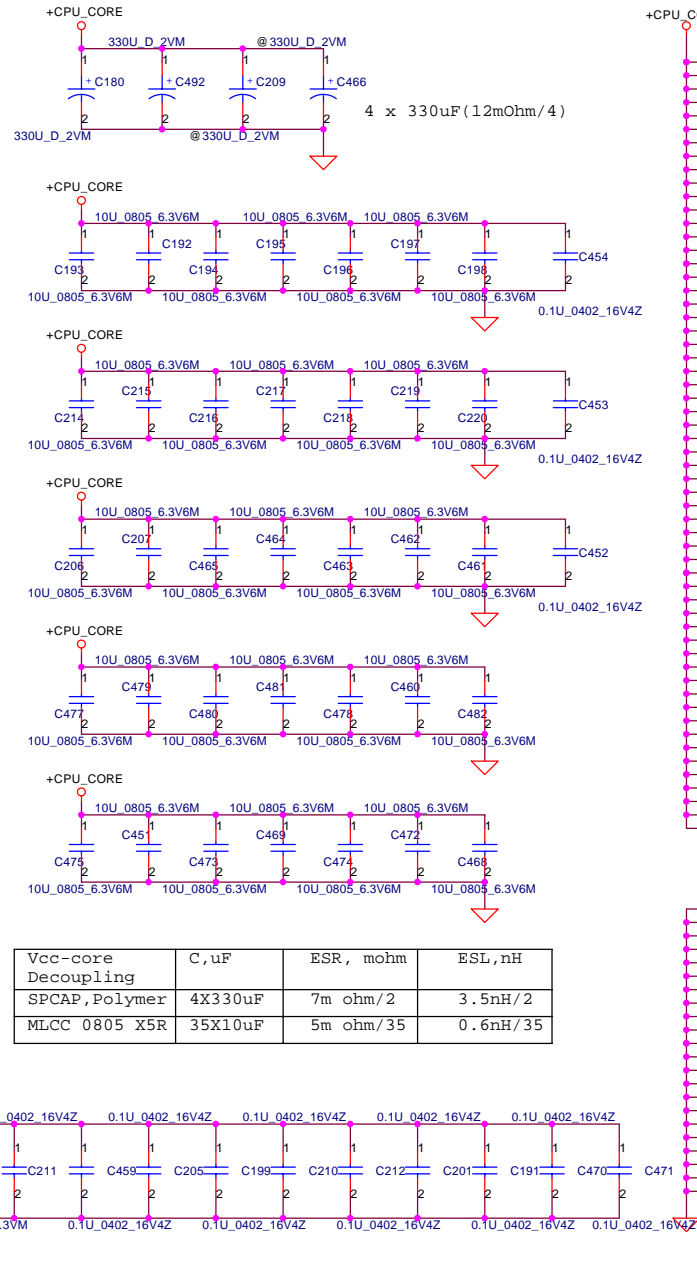
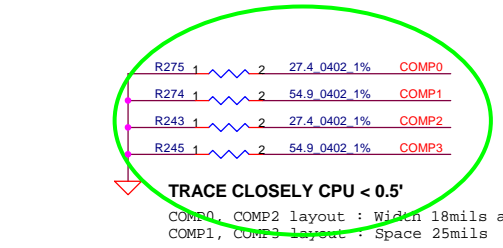
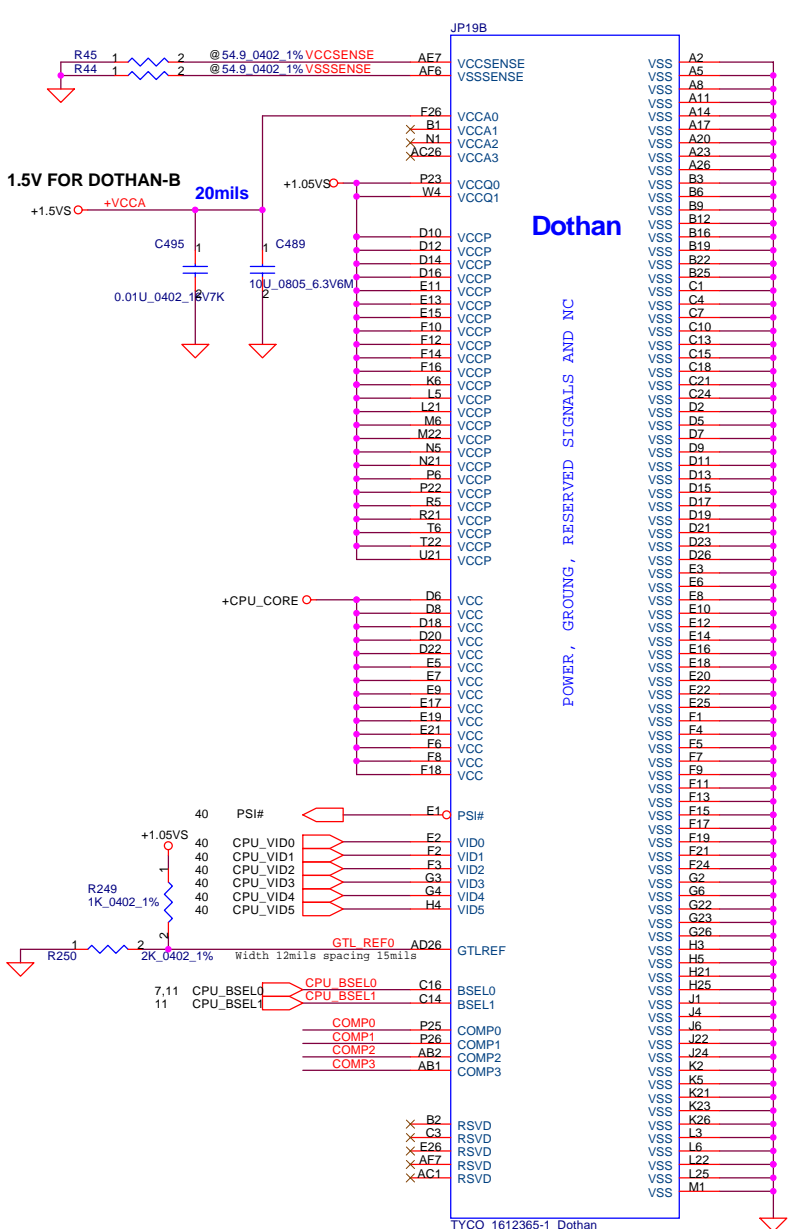
	HDD Password
0	NO
1	Yes

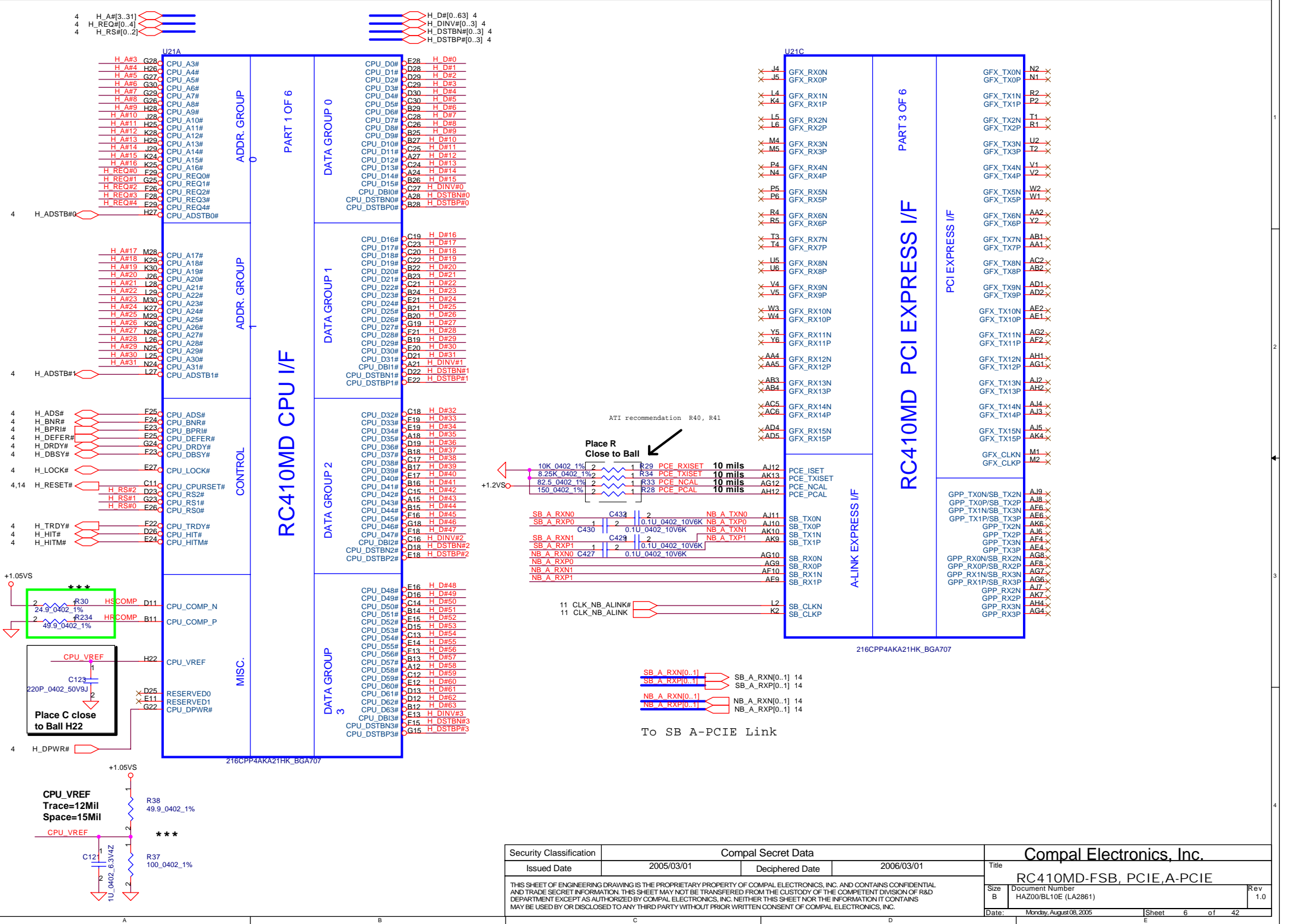
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THERMDA & THERMDC Trace / Space = 10 / 10 mil

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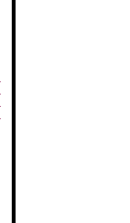
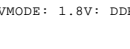
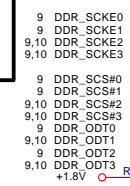
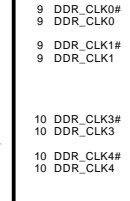
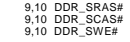
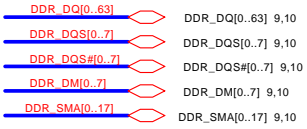




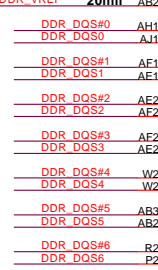
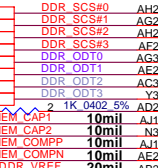
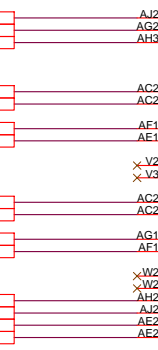
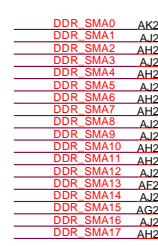
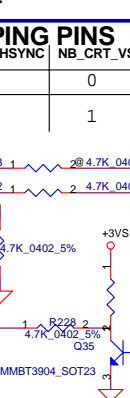
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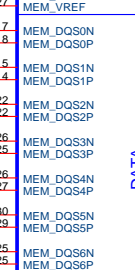
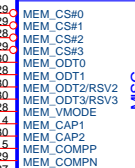
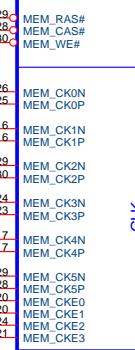
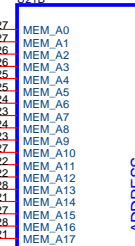




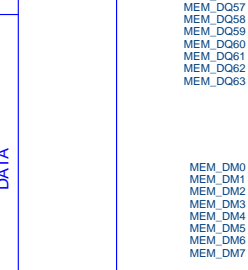
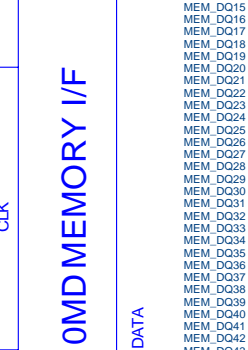
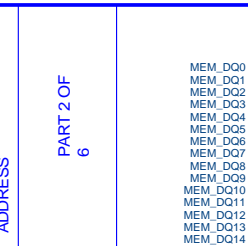
Place these R and C close to relative Ball.



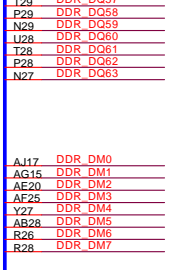
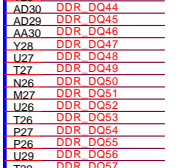
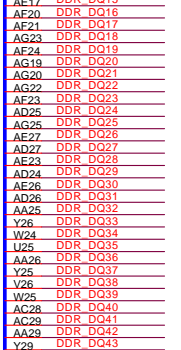
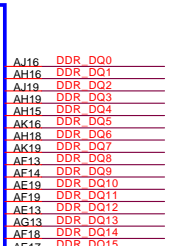
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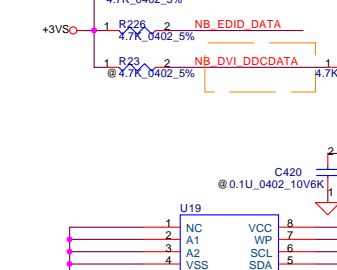
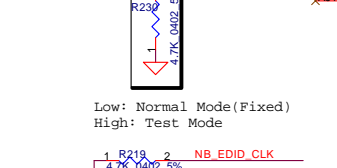
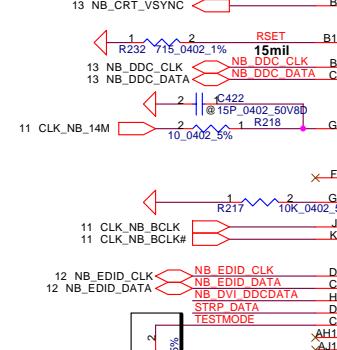
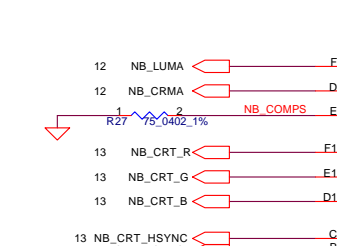
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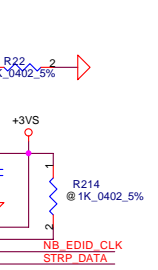
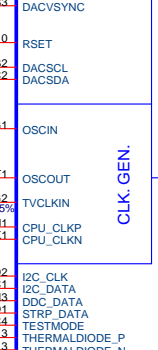
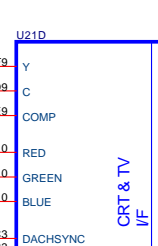
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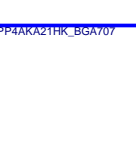
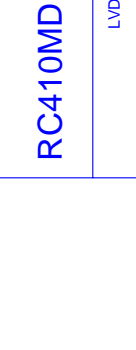
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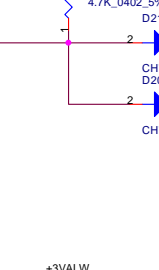
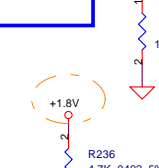
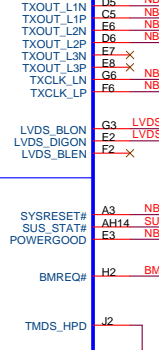
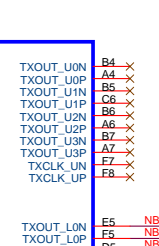
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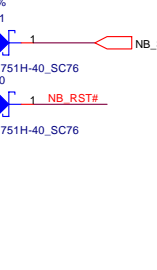
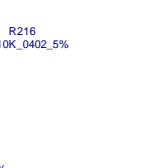
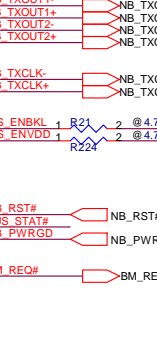
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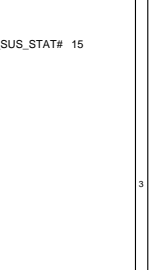
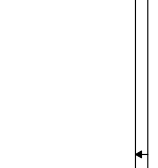
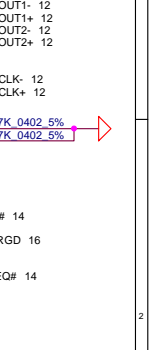
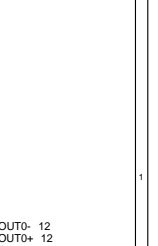
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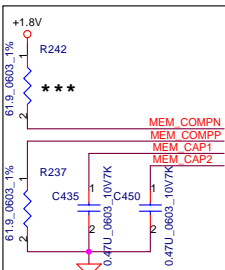
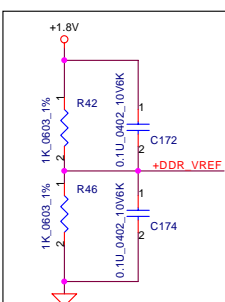
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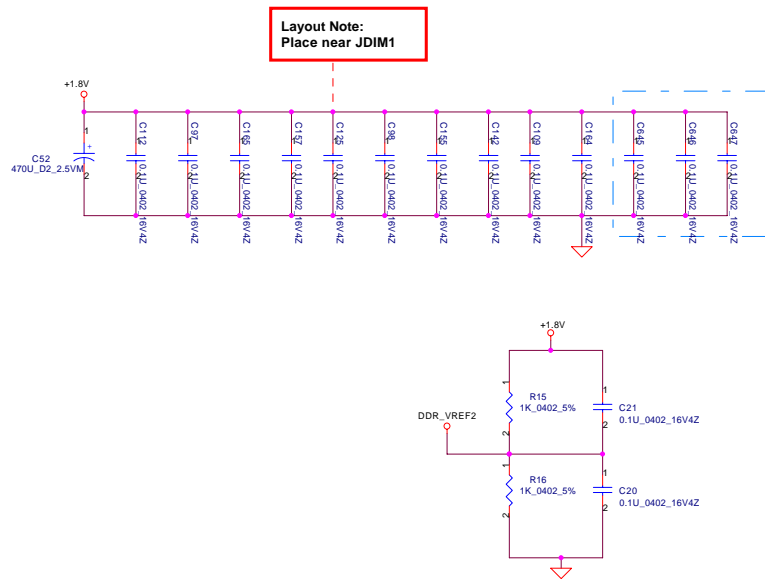
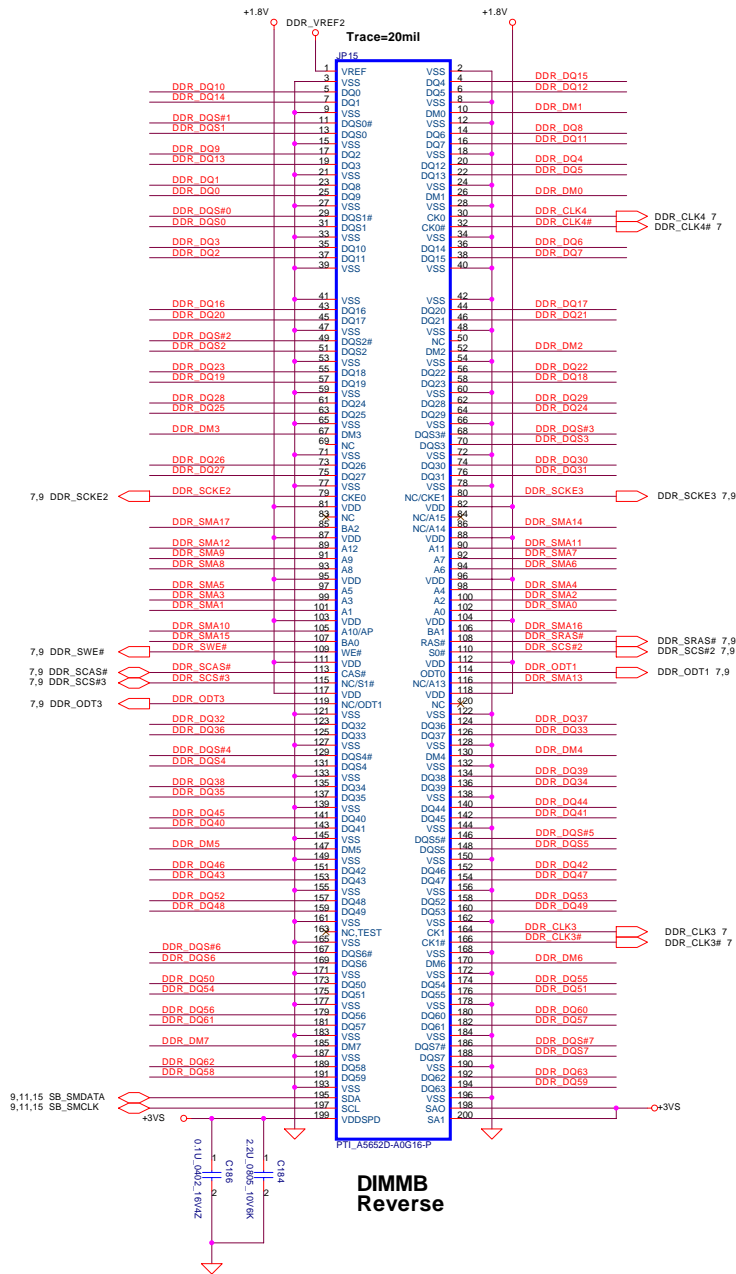








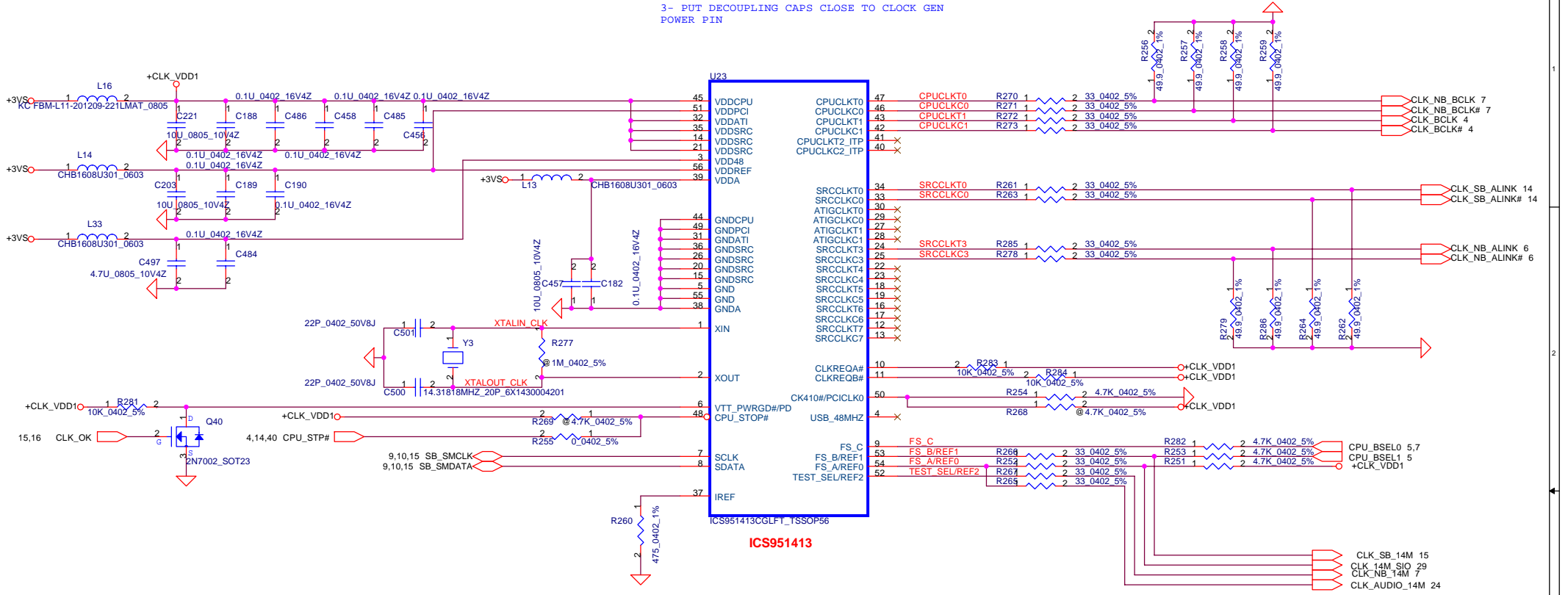
- 7.9 DDR\_DQ[0..63]  $\leftrightarrow$  DDR\_DQ[0..63]
- 7.9 DDR\_DQS[0..7]  $\leftrightarrow$  DDR\_DQS[0..7]
- 7.9 DDR\_DQS#[0..7]  $\leftrightarrow$  DDR\_DQS#0..7
- 7.9 DDR\_DM[0..7]  $\leftrightarrow$  DDR\_DM[0..7]
- 7.9 DDR\_SMA[0..17]  $\leftrightarrow$  DDR\_SMA[0..17]



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				Document Number HAZ00/BL10E (LA2861)
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# Clock Generator

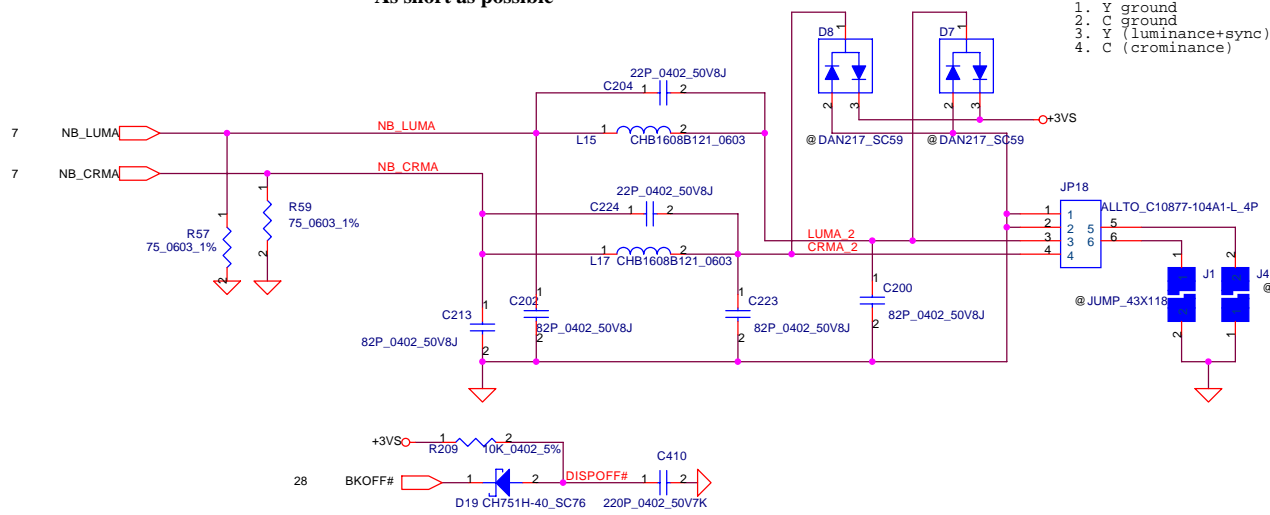
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



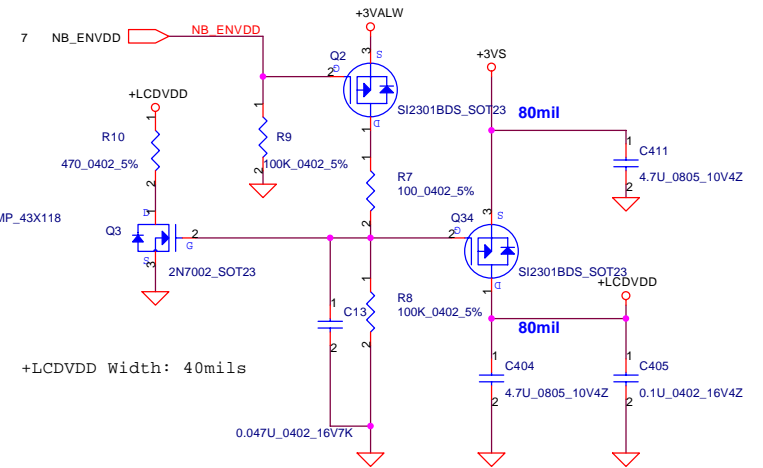
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
1	1	1	---	---	---	---	---

# TV-OUT CONNECTOR

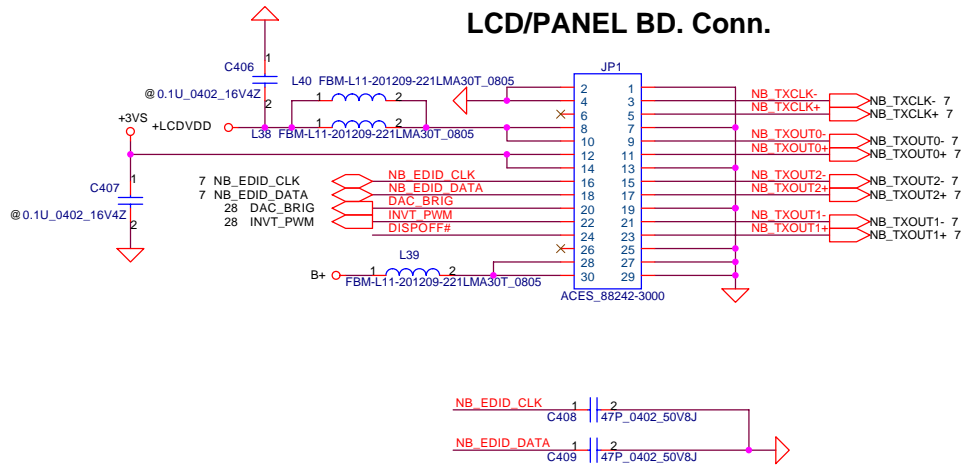
Reduce LUMA\_1 and CRMA\_1 length  
As short as possible



# PANEL +LCDVDD CTRL CKT

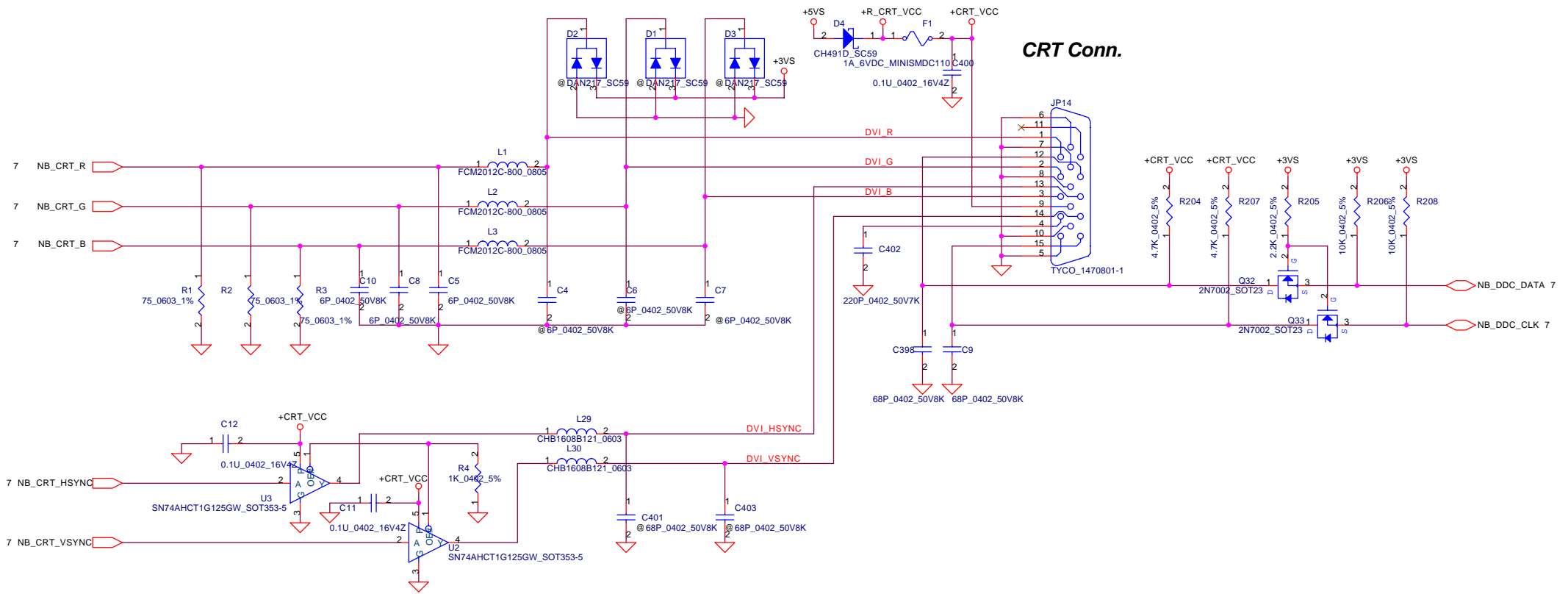


# LCD/PANEL BD. Conn.

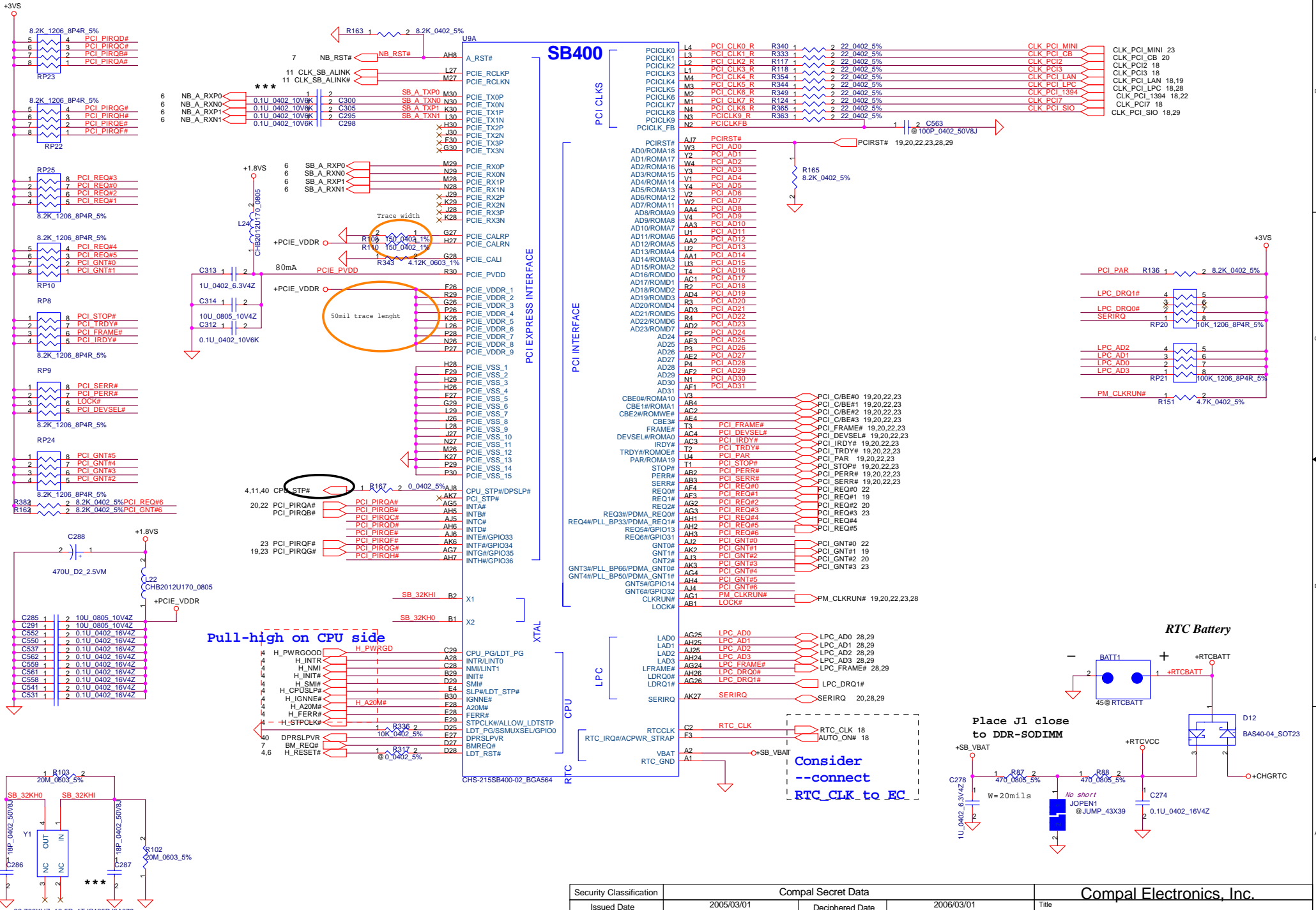


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Size	B	Document Number	HA200/BL10E (LA2861)	Rev	1.0
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# CRT CONNECTOR

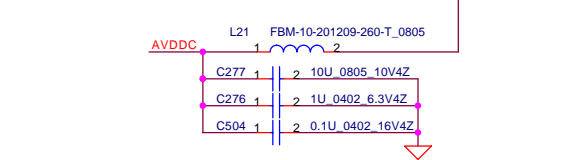
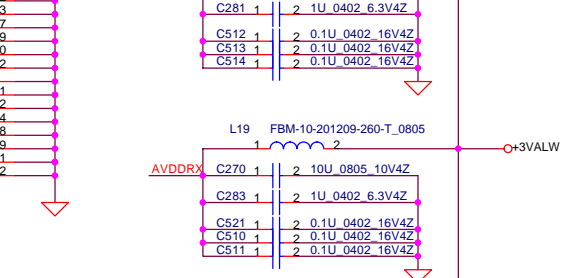
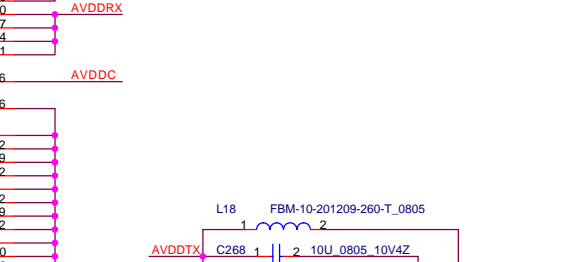
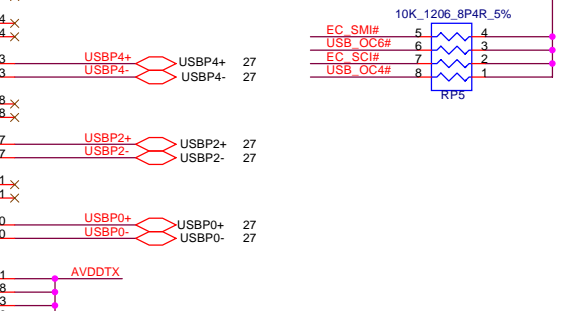
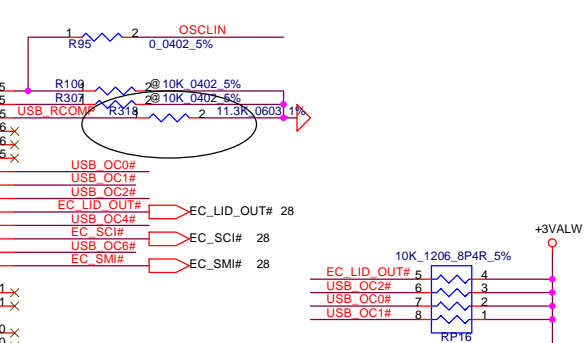
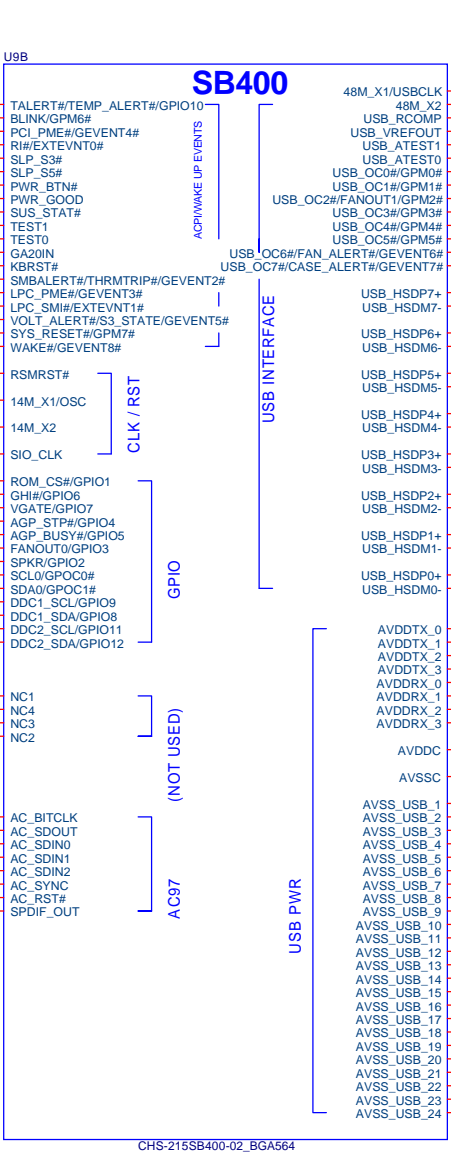
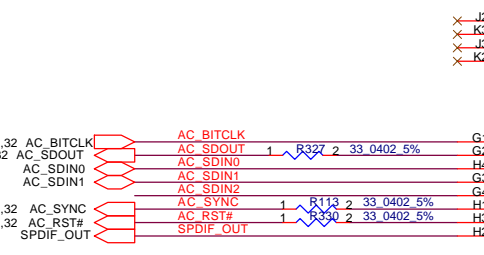
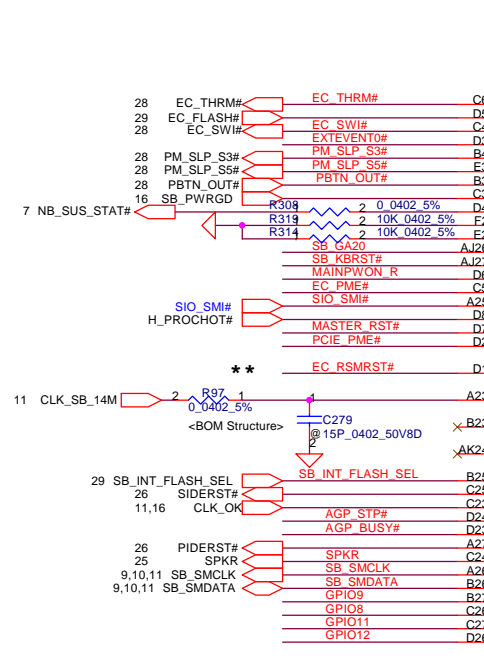
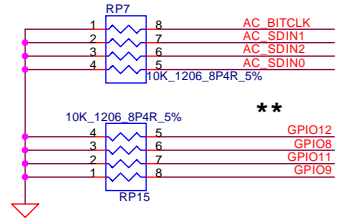
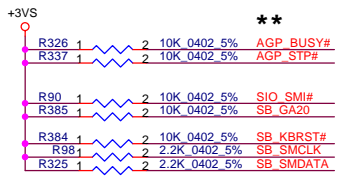
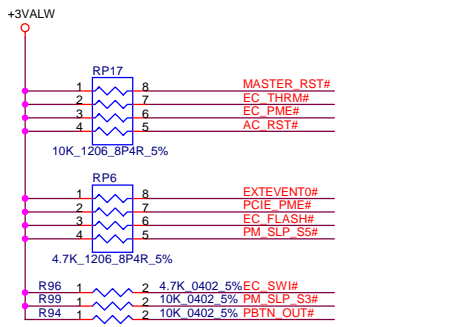


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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	
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Size	Document Number			Rev	
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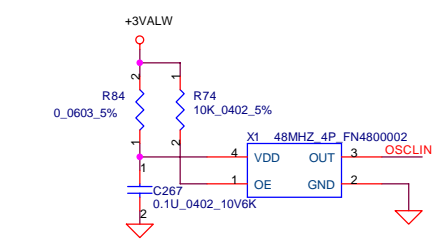
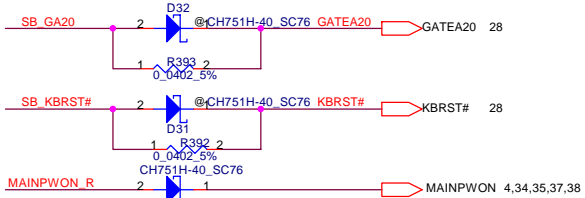


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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Compal Electronics, Inc.	
				PCI_EXP/LPC/RTC	
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		HAZ00/BL10E (LA2861)	1.0		
Date:	Mrcdy, Aug 08, 2005	Sheet	14	of	42



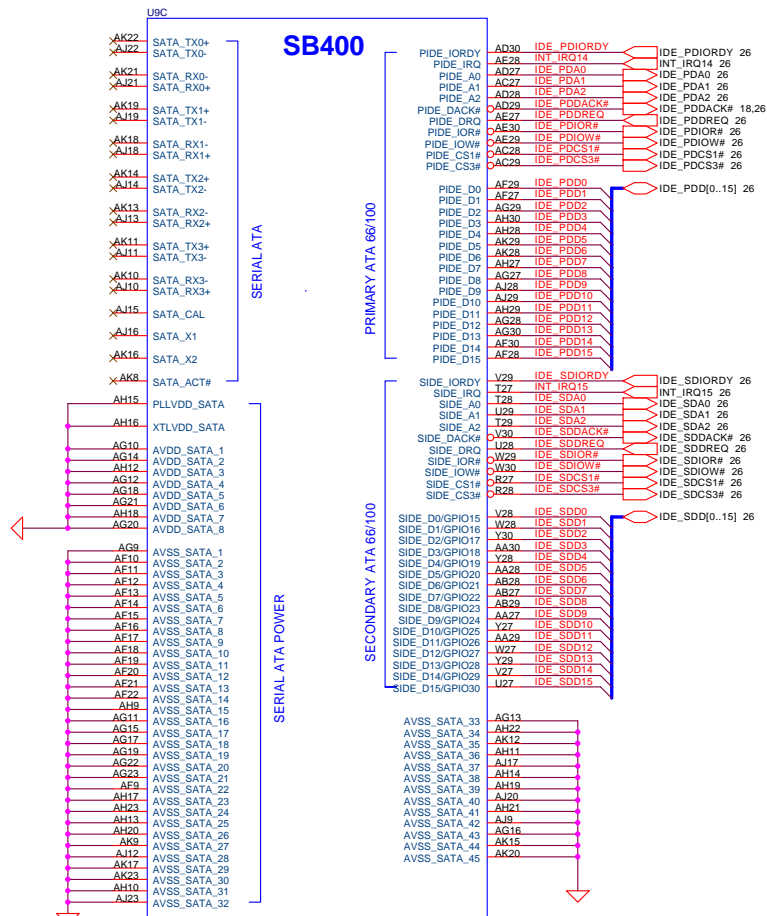


Control by EC  
Delay 50ms after +3VALW ready

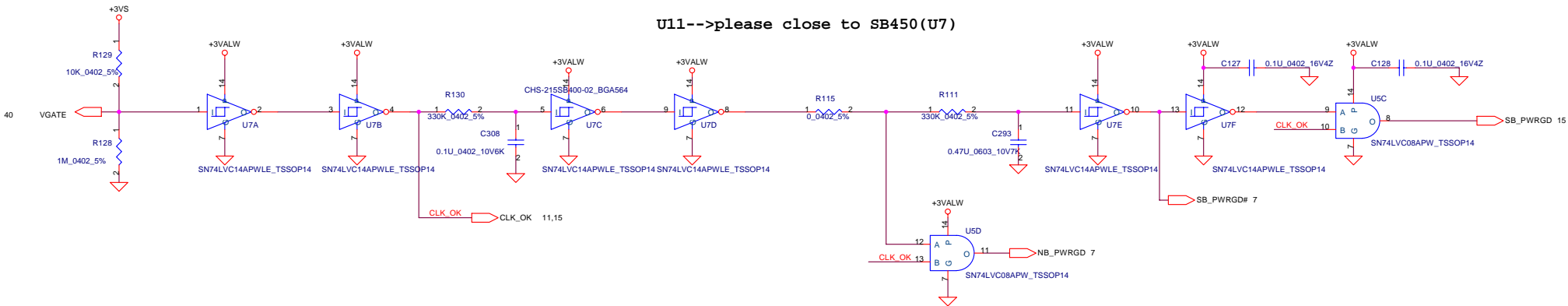


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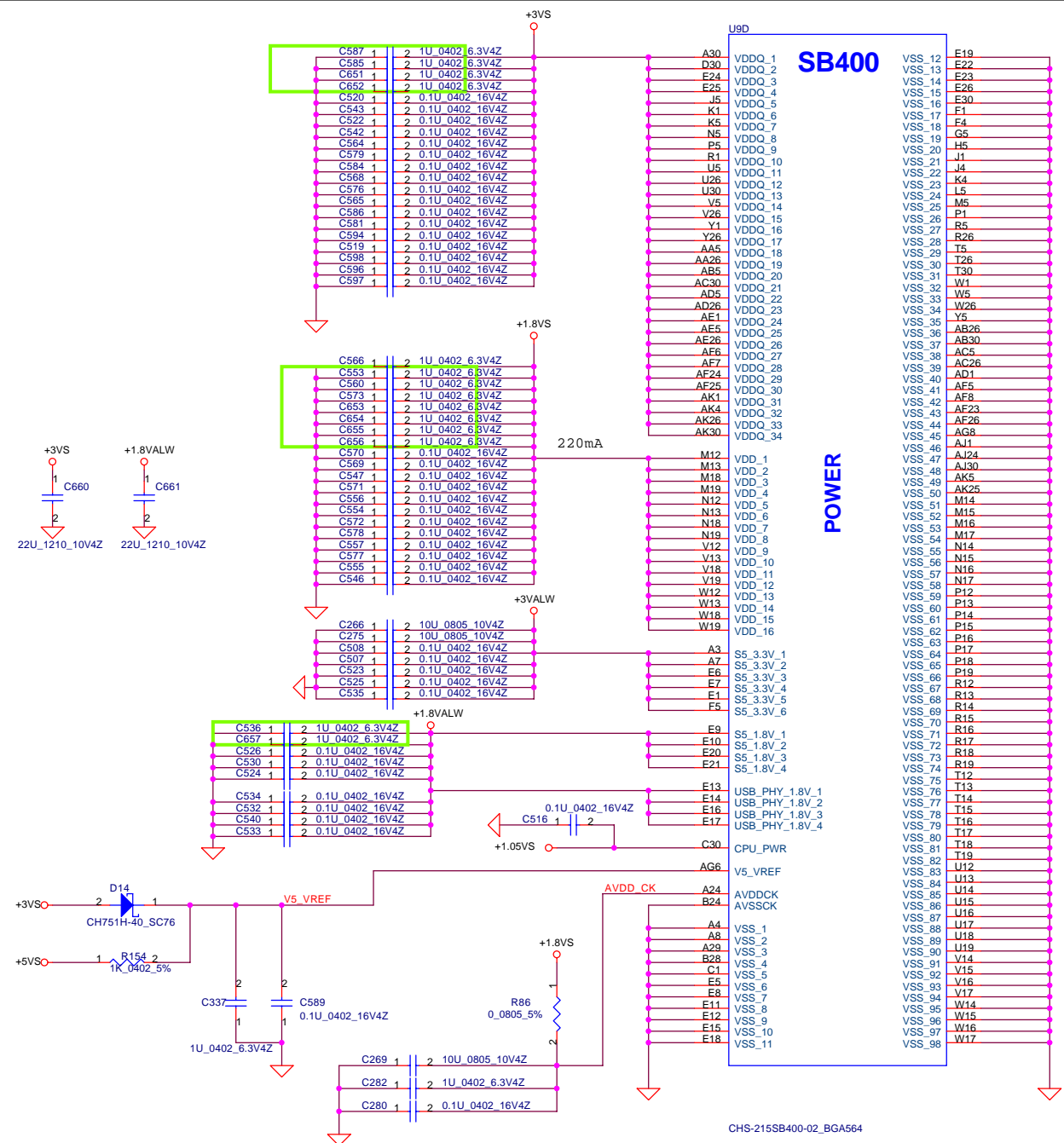
Compal Electronics, Inc.			
Title: SB450 USB/ACPI/AC97/GPIO			
Size	Document Number	Rev	
	Customer#HA200/BL10E (LA2861)	1.0	
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U11-->please close to SB450(U7)

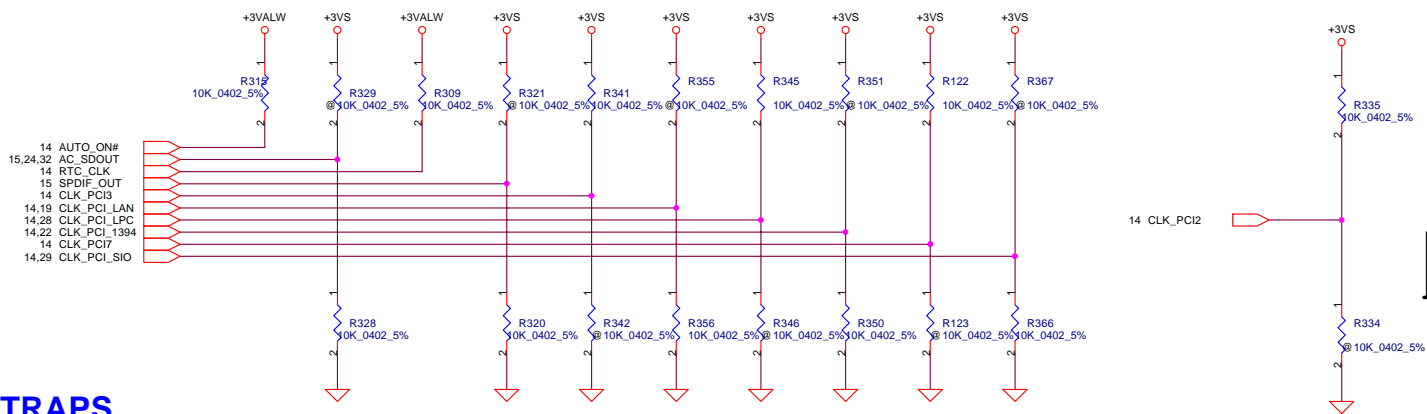


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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title
				SB450 IDE/SATA
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CHS-215SB400-02\_BGA564

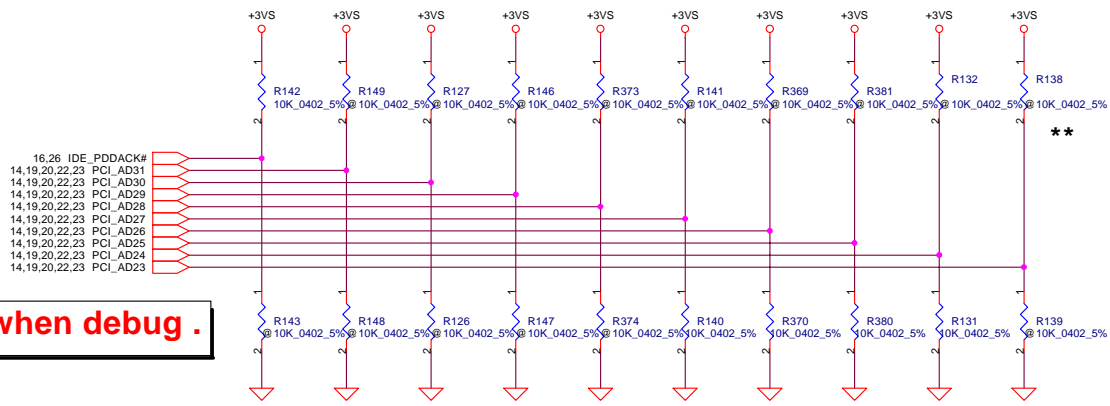
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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title
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Size	Document Number	Rev		
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## REQUIRED STRAPS



	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	CLK_PCI_MINI2
<b>PULL HIGH</b>	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS DEFAULT	INTERNAL RTC DEFAULT	PU for 48Mhz XTAL mode DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL DEFAULT	PCIE CM_SET low DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		Clock input buffer DEFAULT
<b>PULL LOW</b>	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	PCIE CM_SET HIGH	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		Crysal Pad



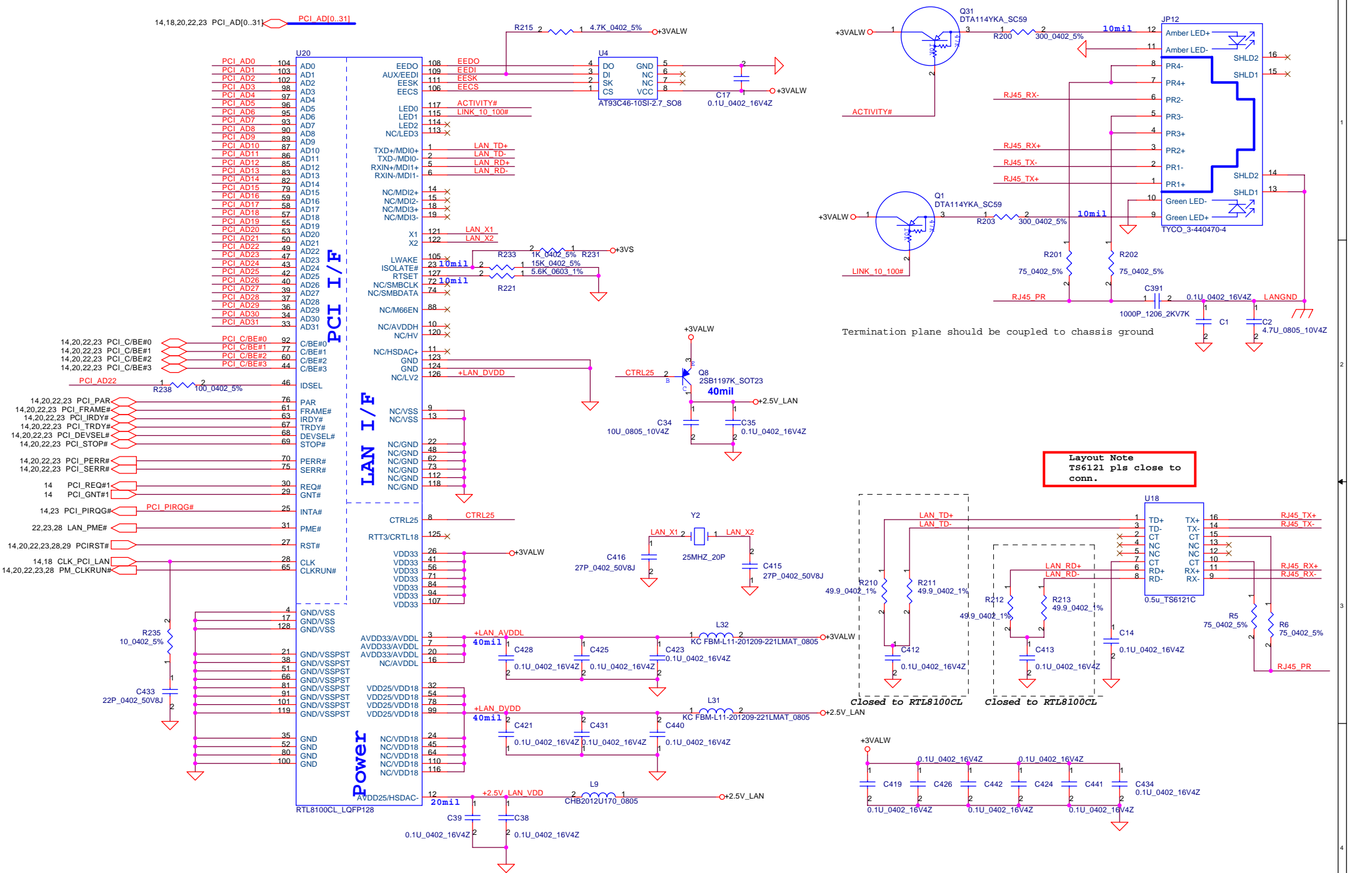
Pop R634 when debug .

## DEBUG STRAPS

	DE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
<b>PULL LOW</b>	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

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		2006/03/01
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Title		Compal Electronics, Inc.	
Size		HARDWARE TRAP	
Document Number	Customer#	Date	Rev
AZ000/BL10E (LA2861)		Monday, August 08, 2005	1.0
Date		Monday, August 08, 2005	Sheet 18 of 42



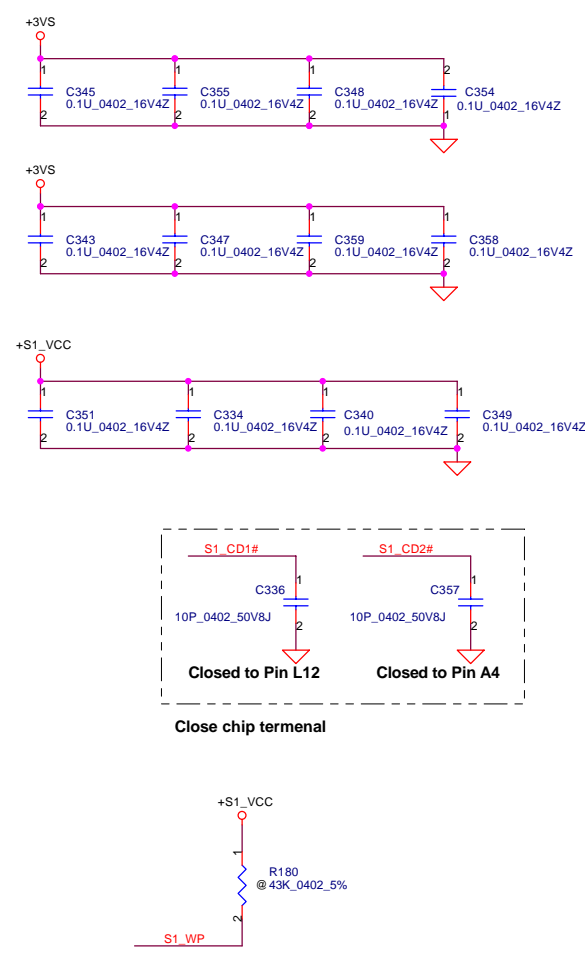
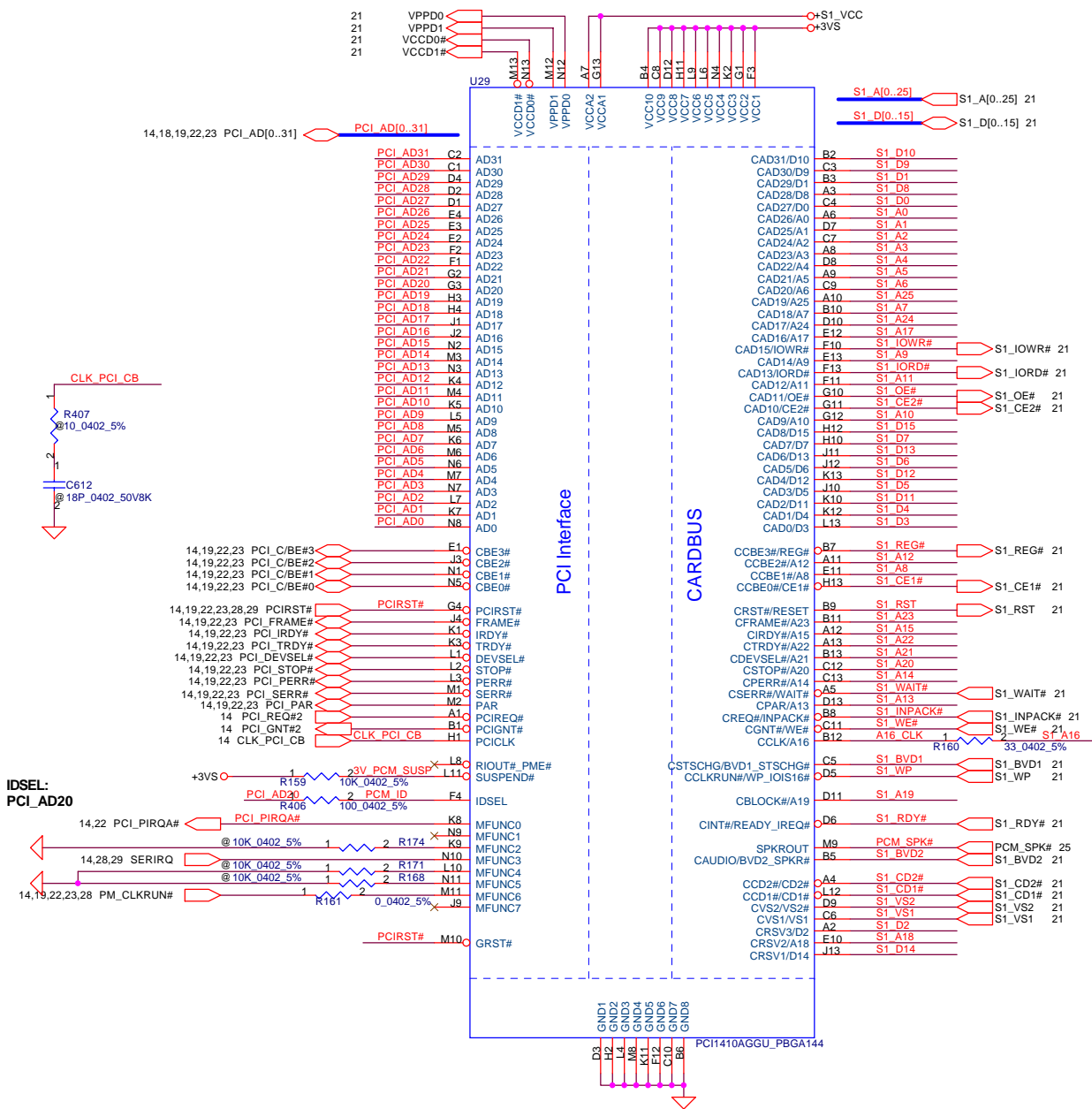
Termination plane should be coupled to chassis ground

**Layout Note**  
TS6121 pls close to conn.

Closed to RTL8100CL

Closed to RTL8100CL

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Issued Date		2005/03/01	Deciphered Date	2006/03/01	RTL8100CL
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Size	Document Number	Date		Monday, August 08, 2005	Rev 1.0
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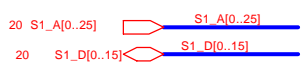
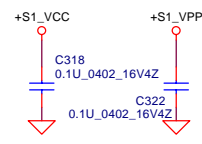
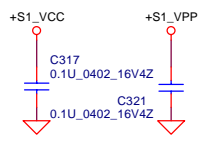
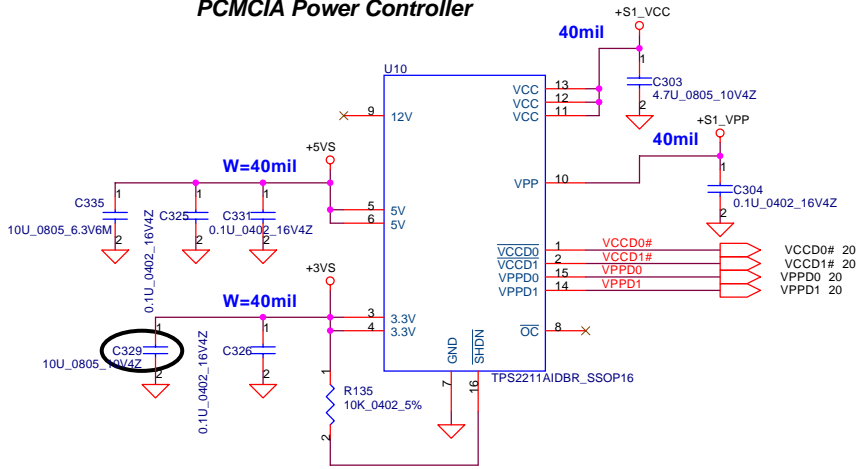


IDSEL:  
PCI\_AD20

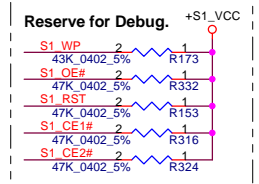
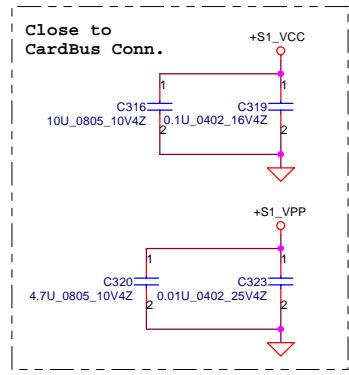
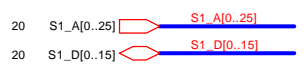
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Size	B	Document Number	HA200/BL10E (LA2861)	Rev	1.0
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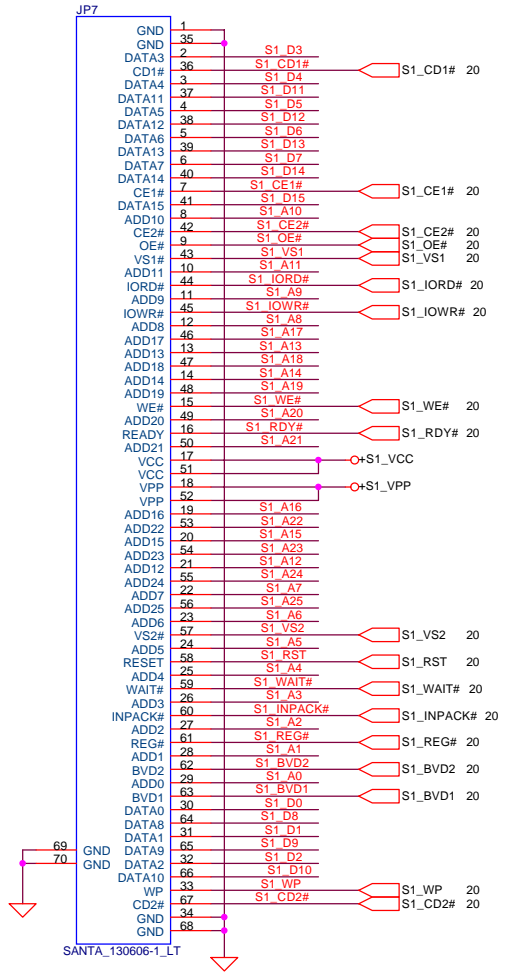
### PCMCIA Power Controller



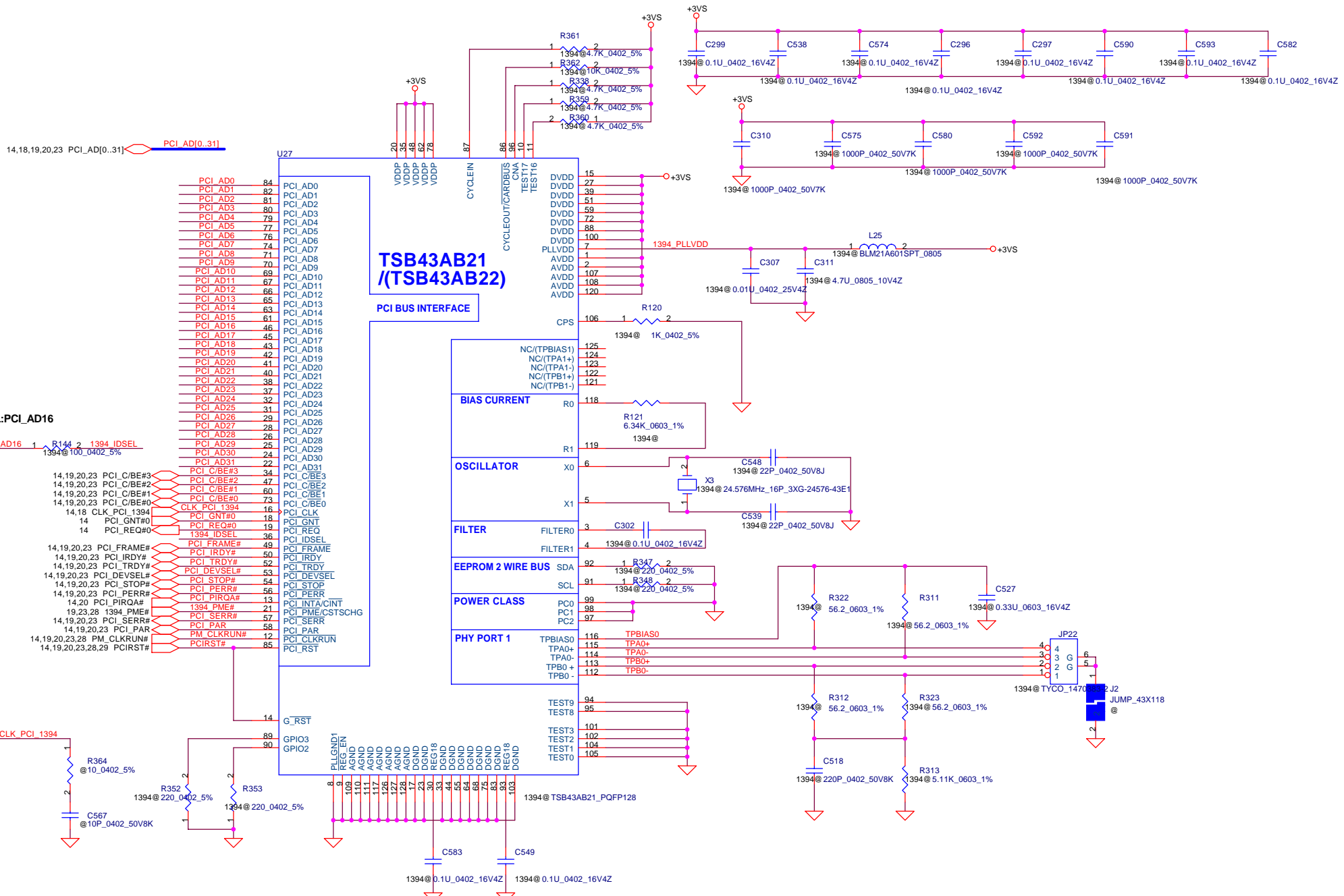
### CardBus Socket



### CardBus Socket



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**TSB43AB21  
(TSB43AB22)**

**PCI BUS INTERFACE**

**BIAS CURRENT**

**OSCILLATOR**

**FILTER**

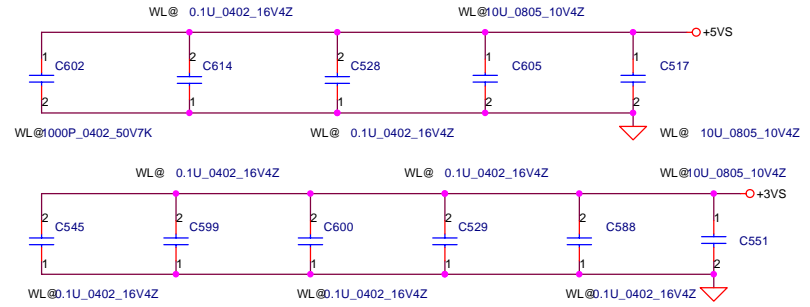
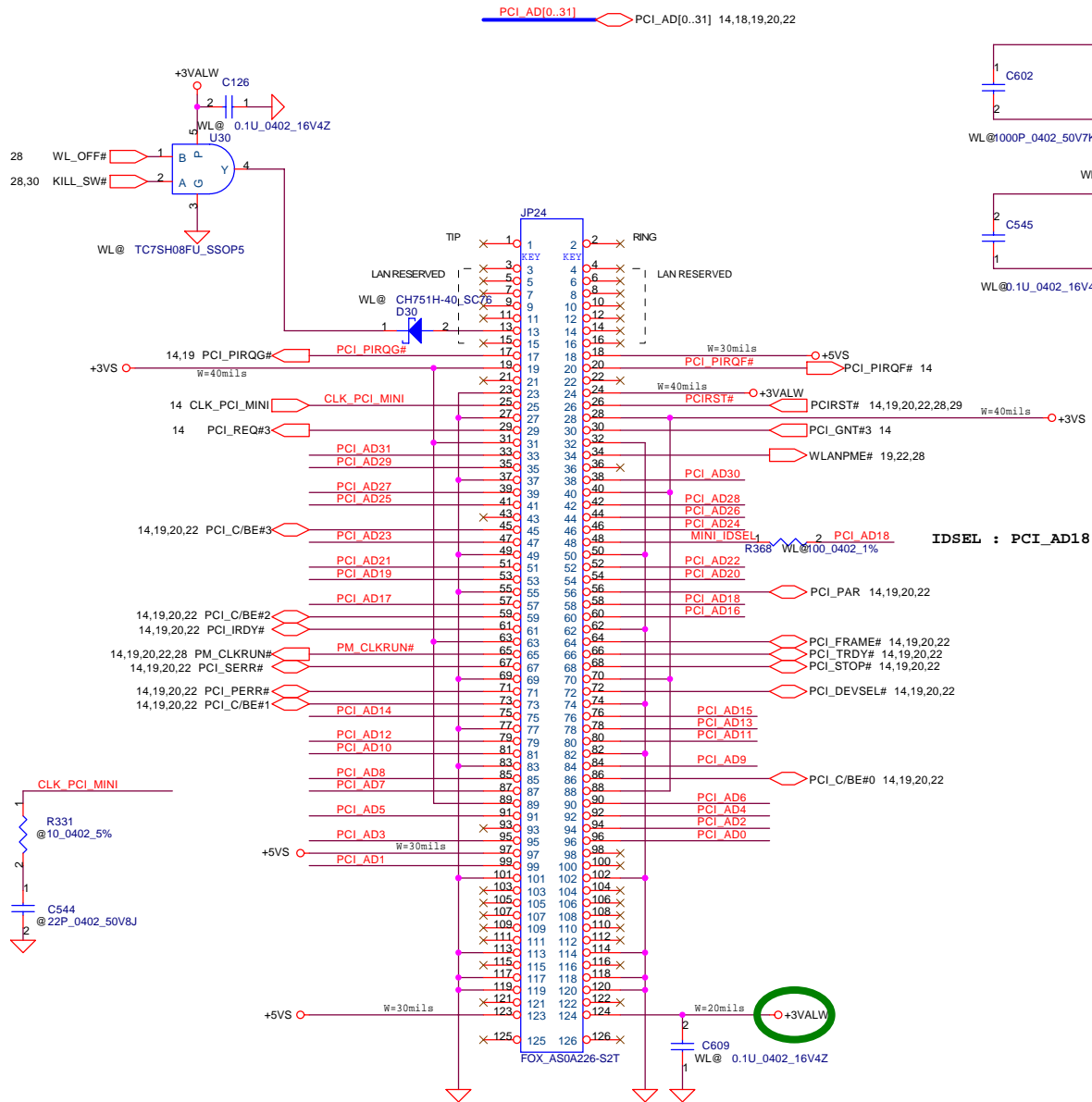
**EEPROM 2 WIRE BUS**

**POWER CLASS**

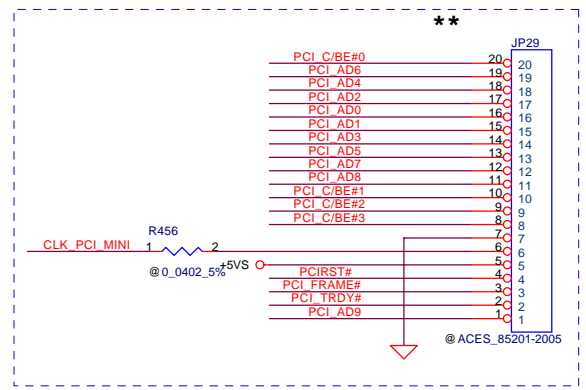
**PHY PORT 1**

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Size	B	Document Number	HAZ00/BL10E (LA2861)	Rev	1.0
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MINI\_PCI SOCKET FOR WLAN (BOTTOM)

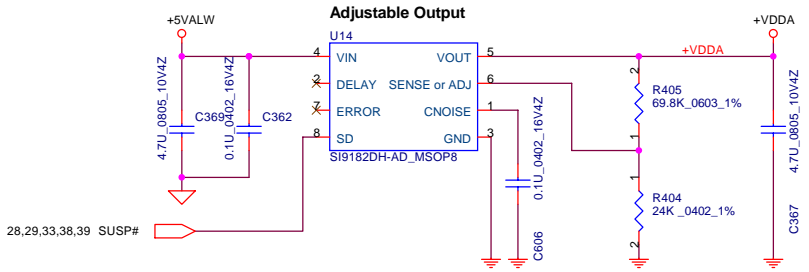


Port 80 Debug Card Connector

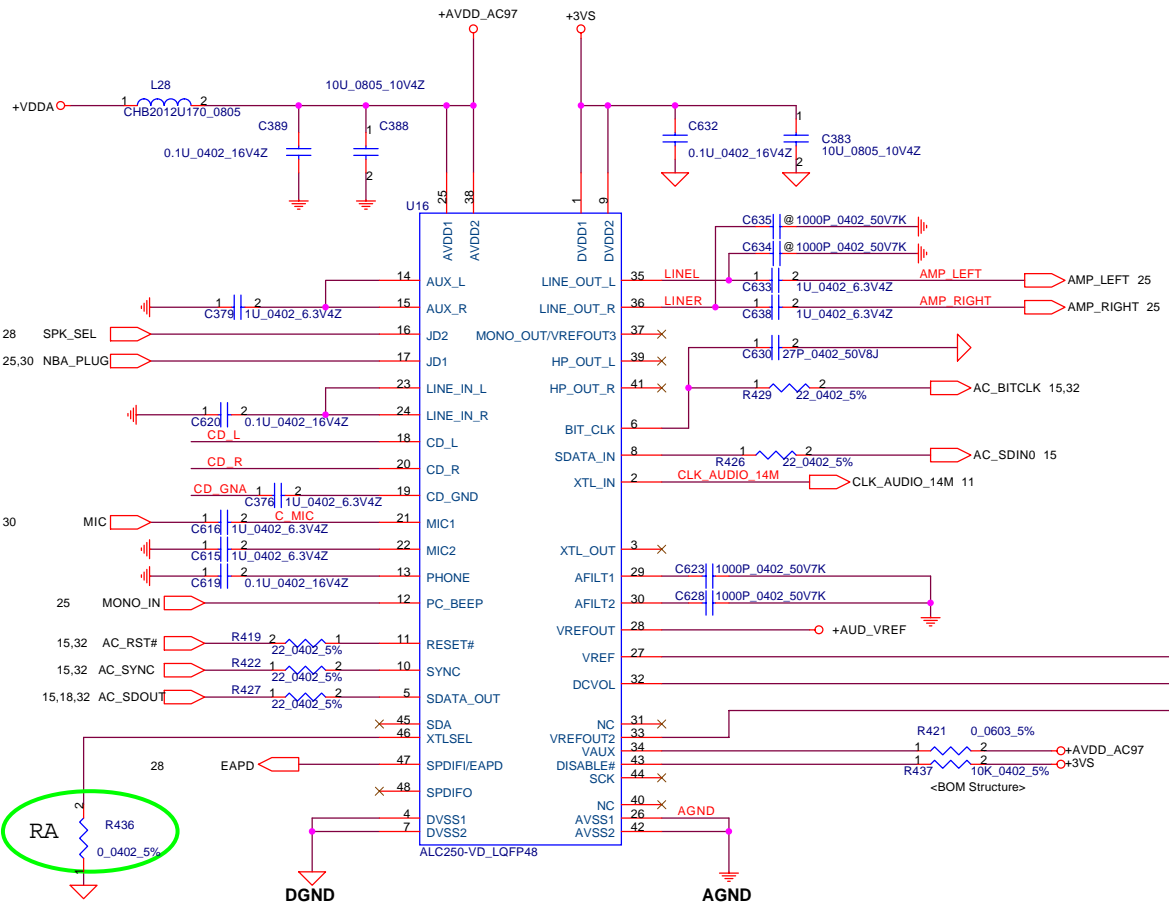


Place under MiniPCI Socket

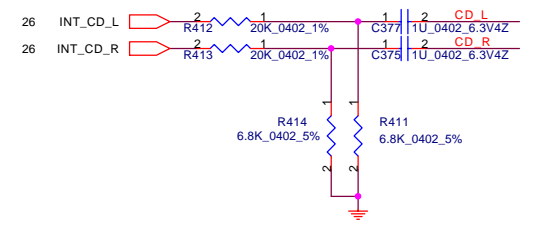
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Size	Document Number	Rev		
B	HAZ00/BL10E (LA2861)	1.0		
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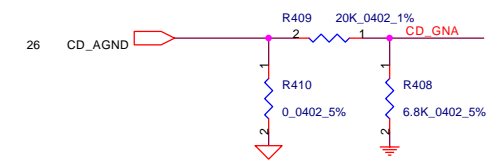
### AC97 Codec



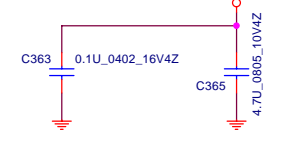
### Audio Signal Bias Circuit



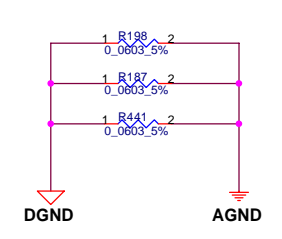
### CD\_AGND To CD\_GNA Bypass



### Analog Reference V

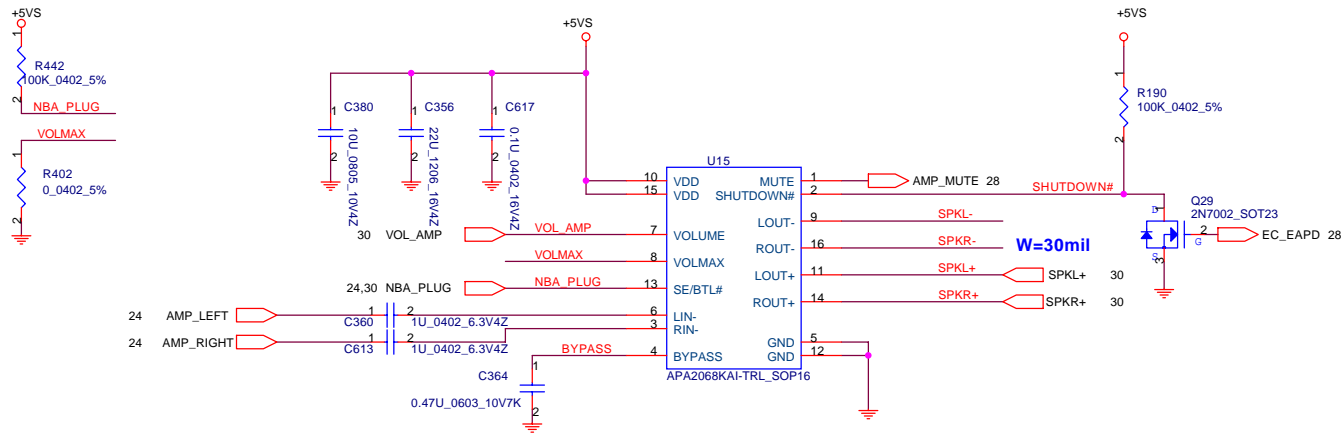


### DGND To AGND Bypass

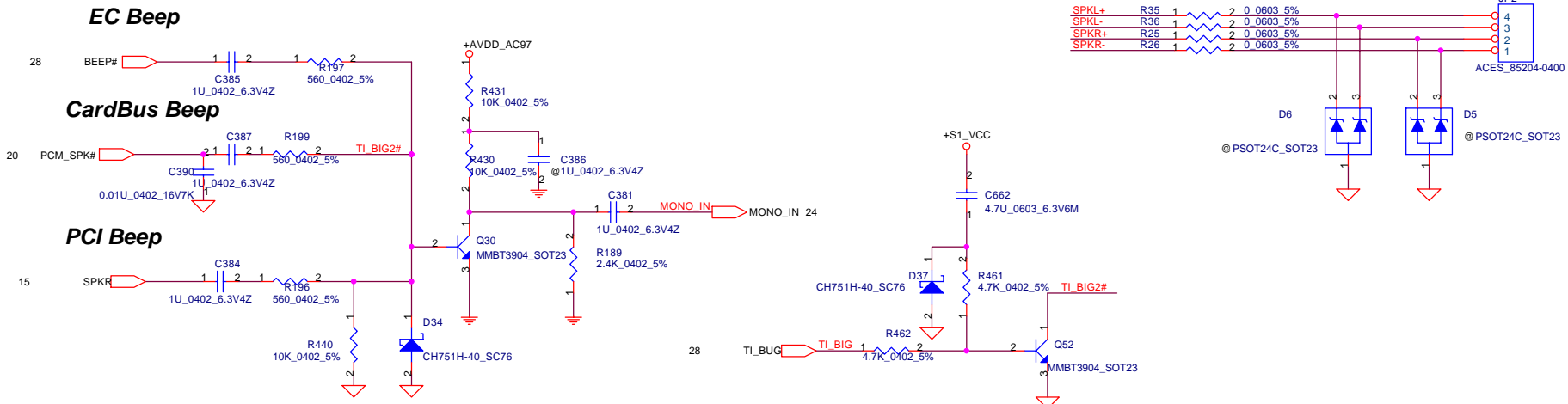


WITH 14.318MHz : RA POP  
WITH 24.576MHz : RA DEPOP

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Size B	Document Number	Date:		Rev	1.0
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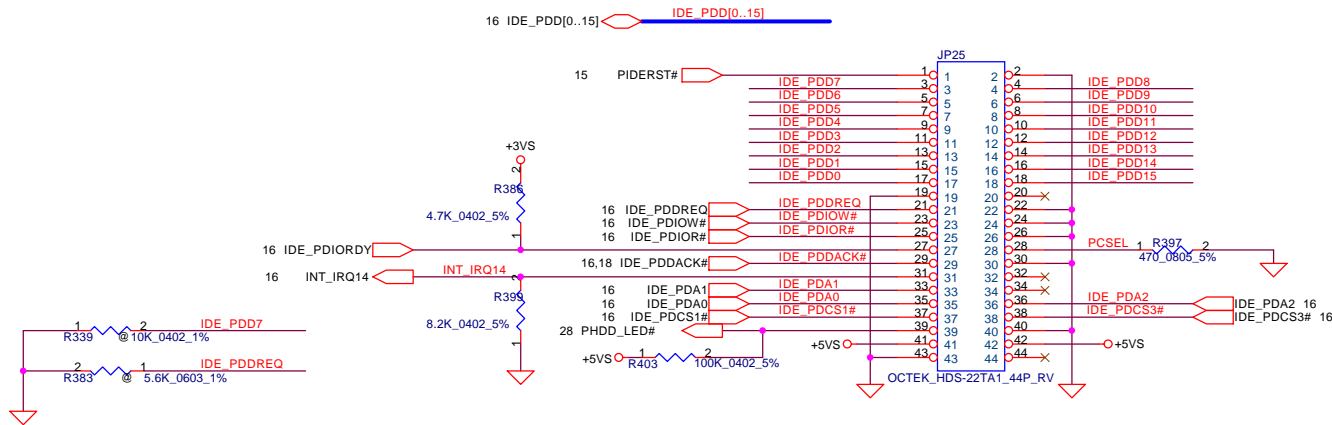


### Speaker Conn.

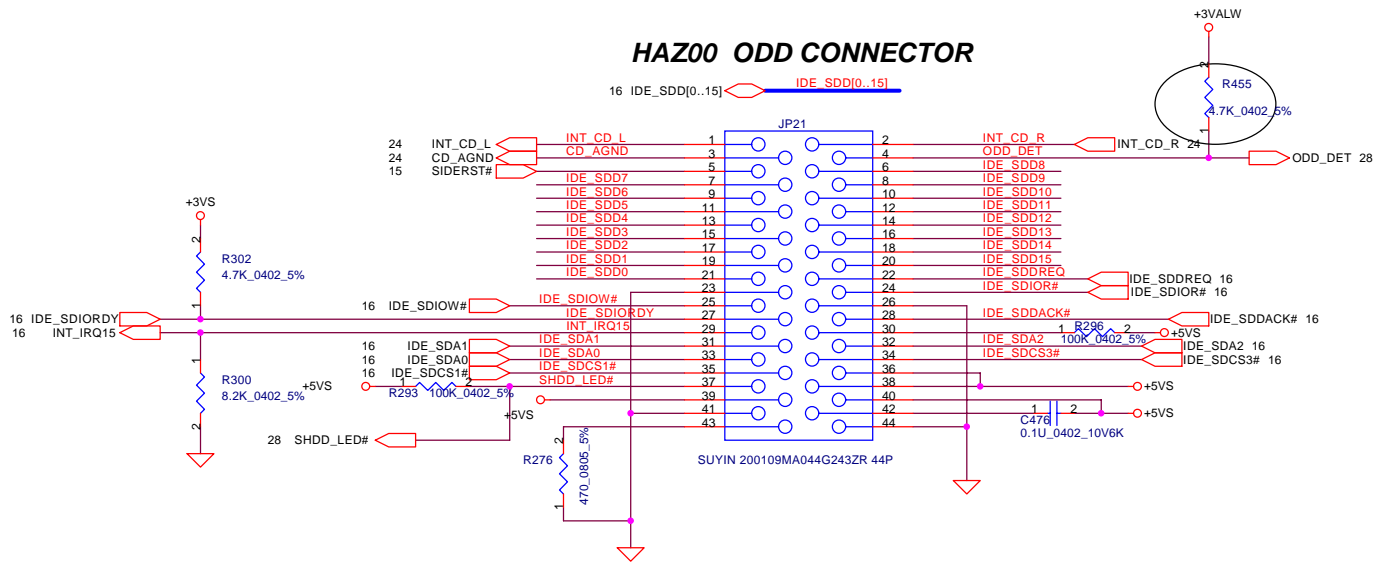


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				B	HA200/BL10E (LA2861)
				Date:	Rev
				Monday, August 08, 2005	1.0
				Sheet	25 of 42

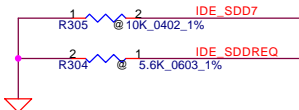
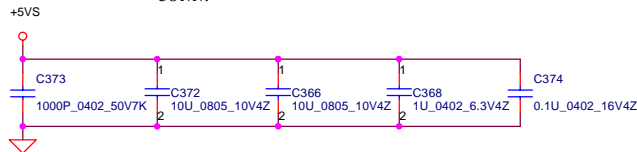
# HDD CONNECTOR



# HAZ00 ODD CONNECTOR



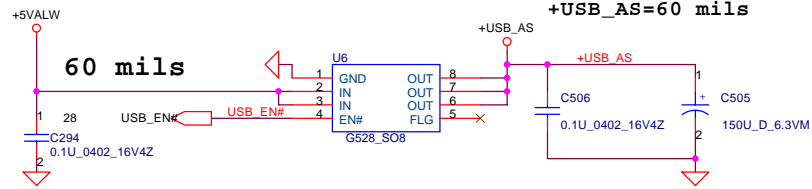
Place caps. near HDD  
CONN.



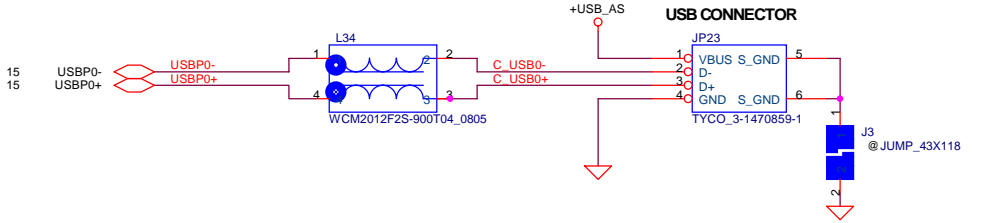
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title
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Size	Document Number	Rev		
B	HAZ00/BL10E (LA2861)	1.0		
Date:	Thursday, August 04, 2006	Sheet	26 of 42	



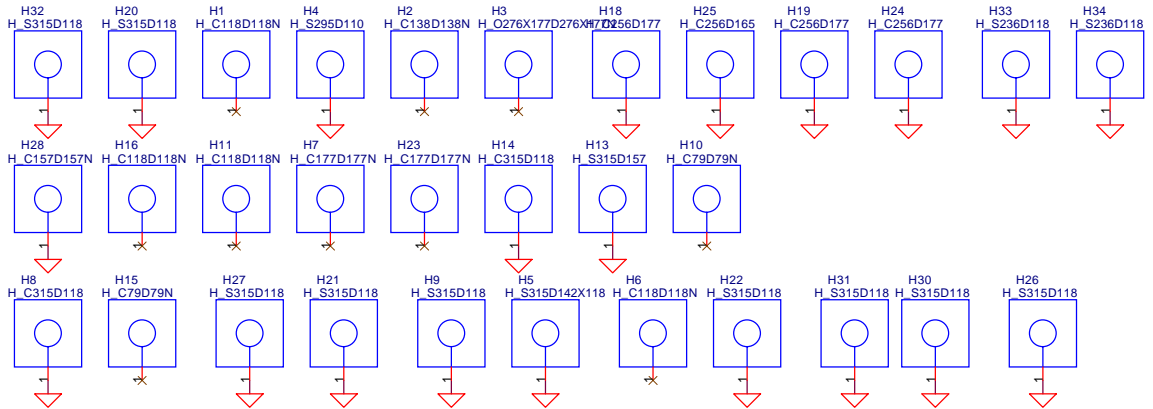
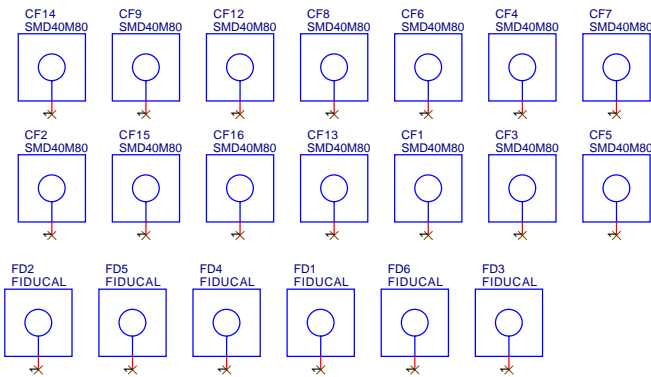
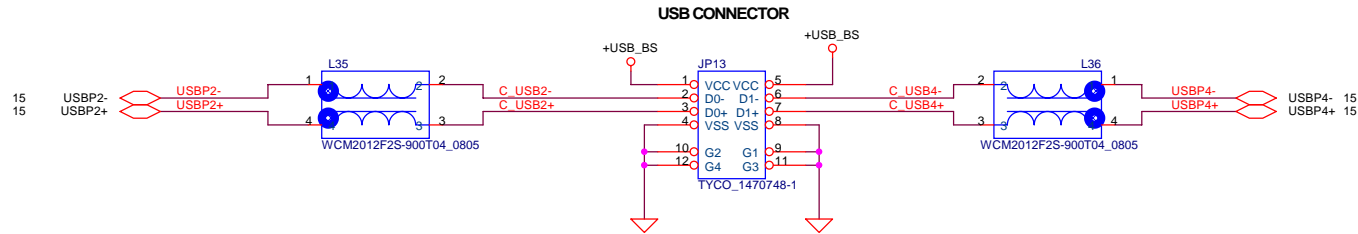
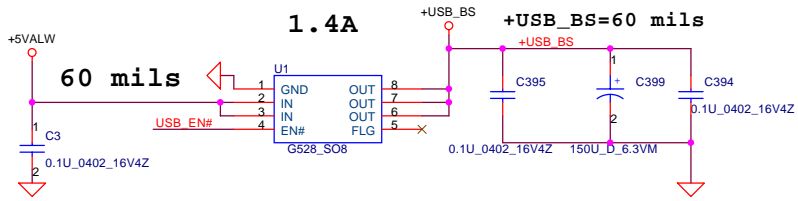
1.4A



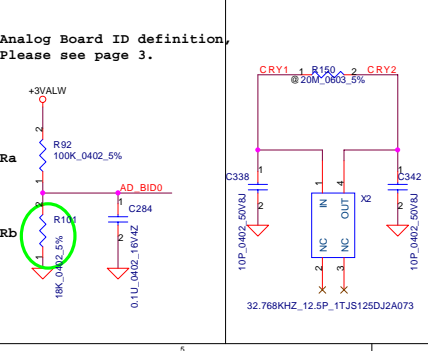
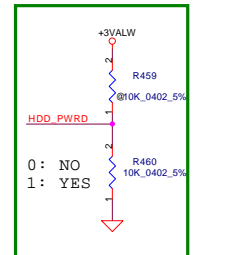
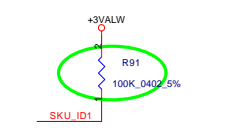
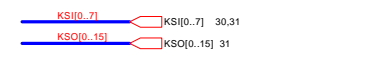
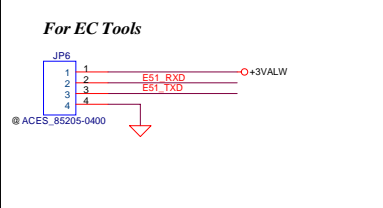
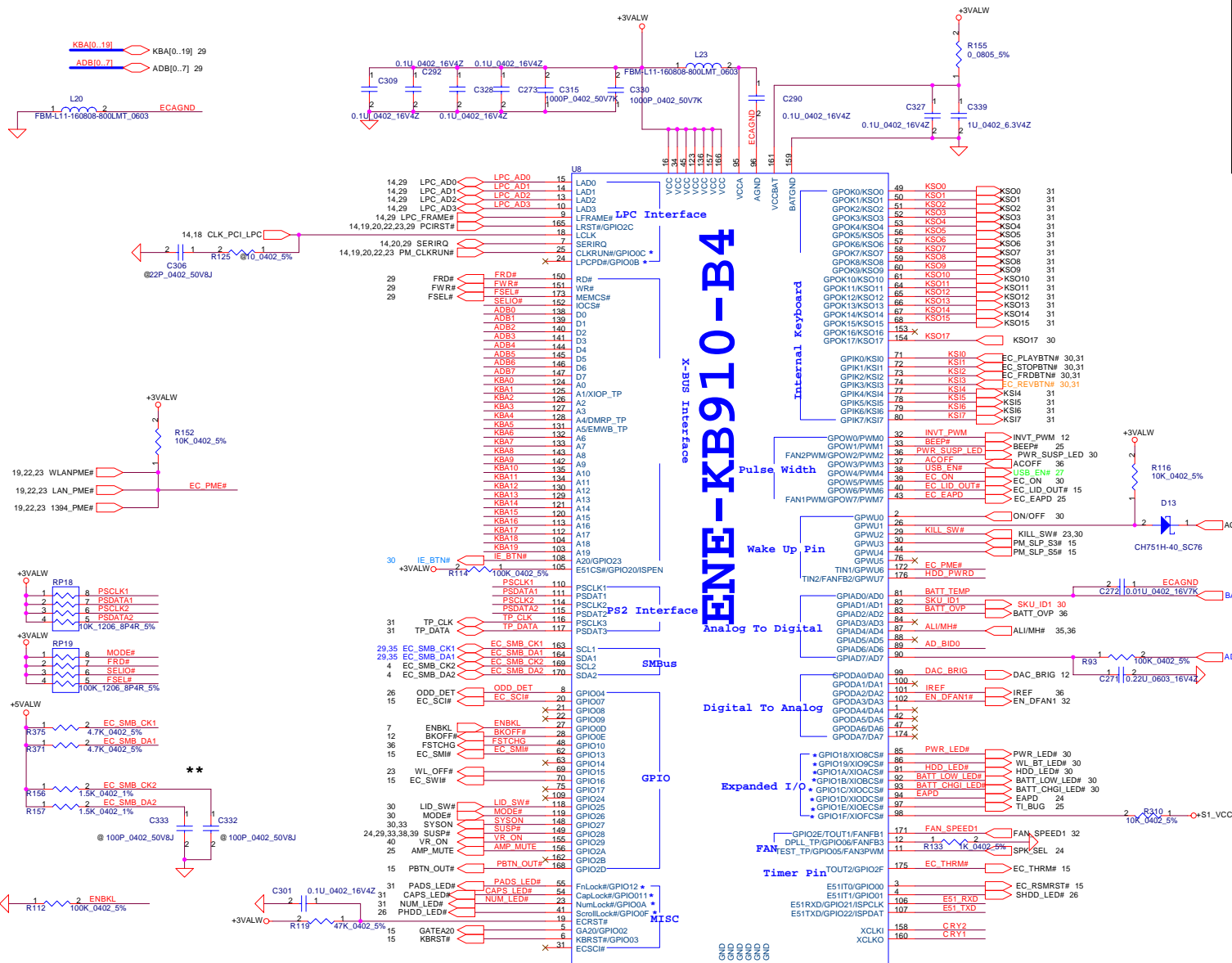
Keep 20 mils minimum spacing between USB signals and others signals



1.4A

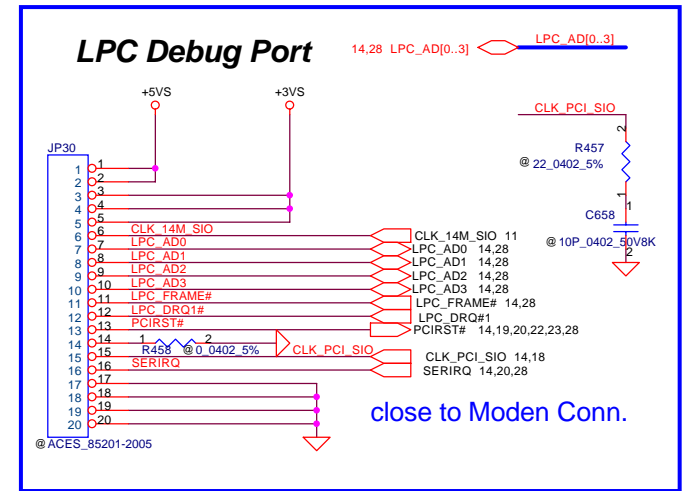
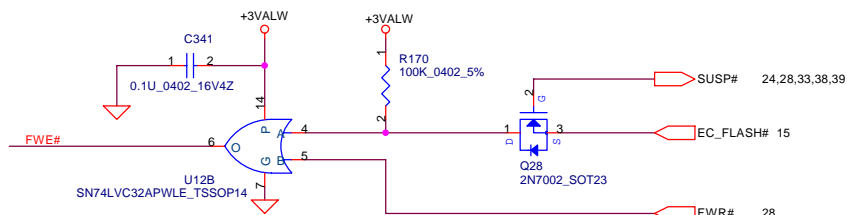
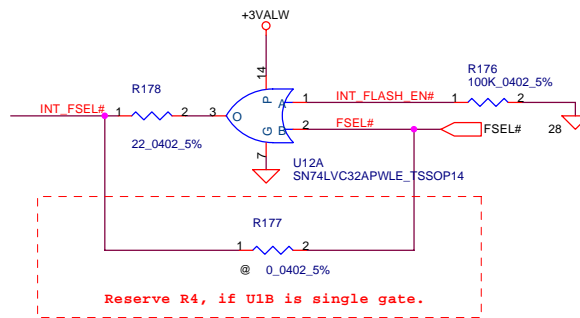
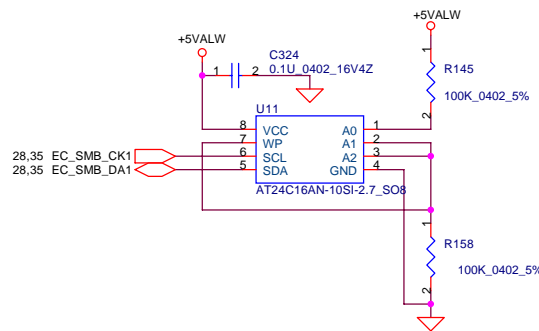


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Size	B	Document Number	HAZ00/BL10E (LA2861)	Rev
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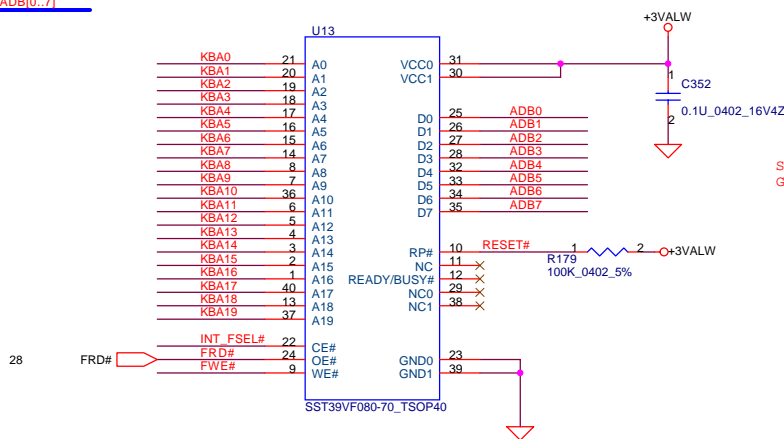
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Issued Date	2005/03/01	Deciphered Date
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Compal Electronics, Inc.	
Title	ENE-KB910
Size	Document Number
	Cust:zhn42009/BL10E (LA2861)
Date:	Monday, August 08, 2005
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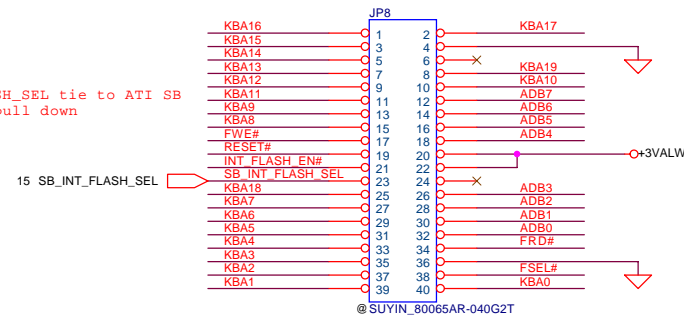


### 1MB Flash ROM

28 KBA[0..19] ↔ KBA[0..19]  
 28 ADB[0..7] ↔ ADB[0..7]

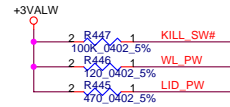
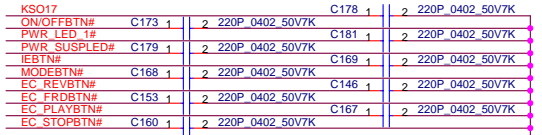
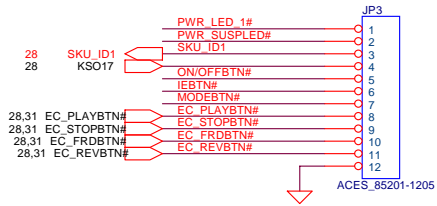


### 1MB ROM Socket

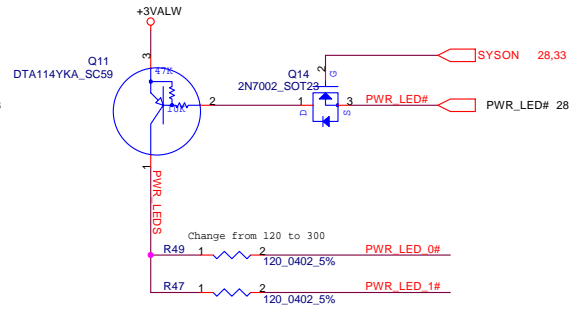
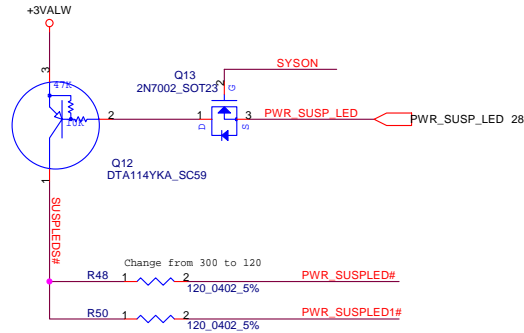
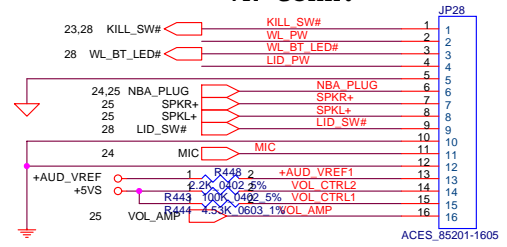


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Size	Document Number			Rev
B	HAZ00/BL10E (LA2861)			1.0
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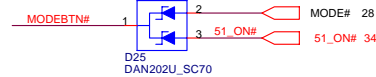
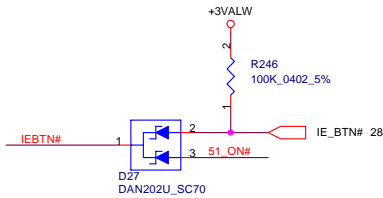
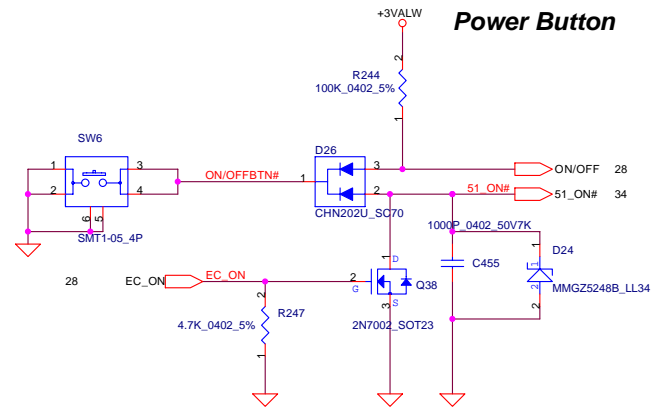
# Switch Board Conn.



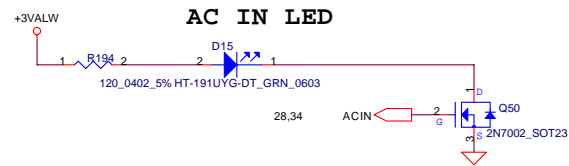
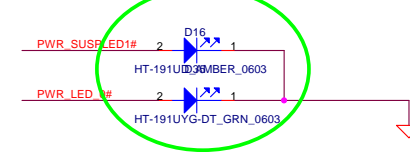
# VR Conn.



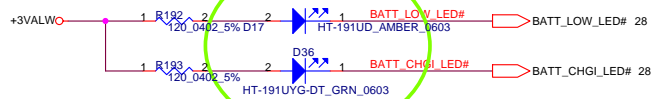
# Power Button



# POWER/ON LED

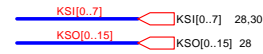


# BATTERY CHG

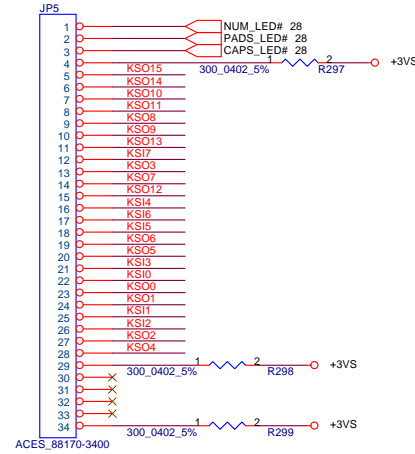
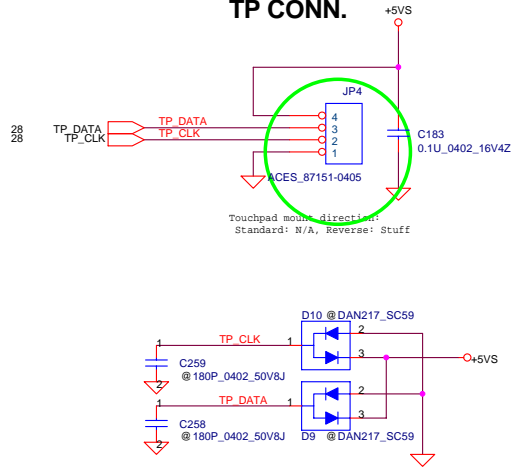


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	HA200/BL10E (LA2861)				1.0
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# INT\_KBD CONN.



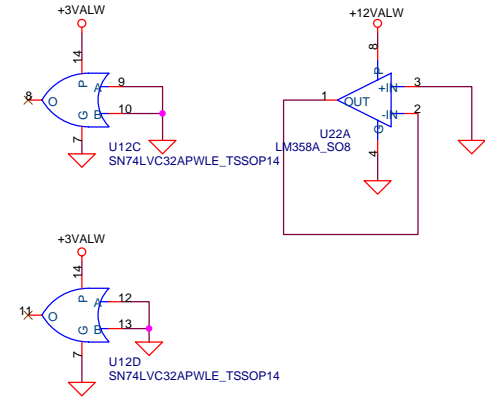
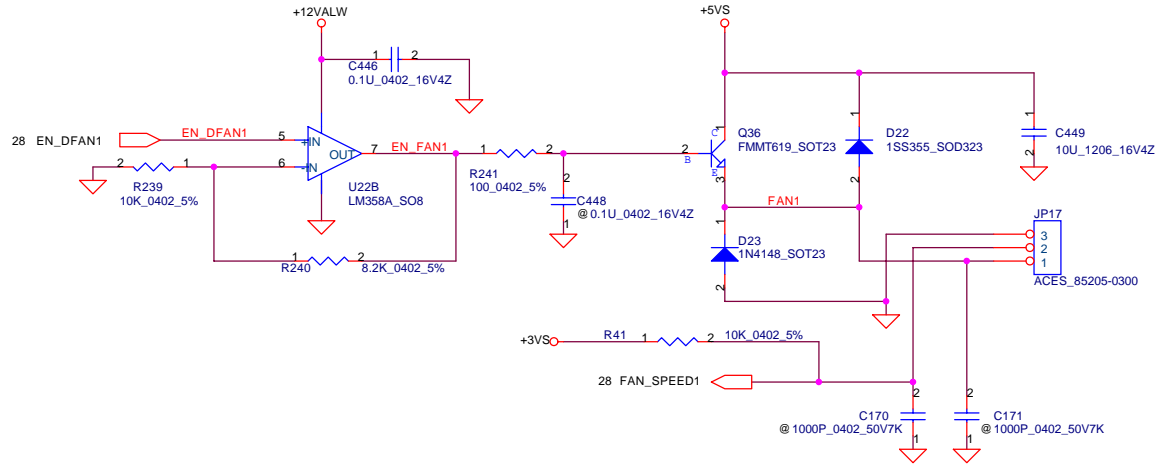
## TP CONN.



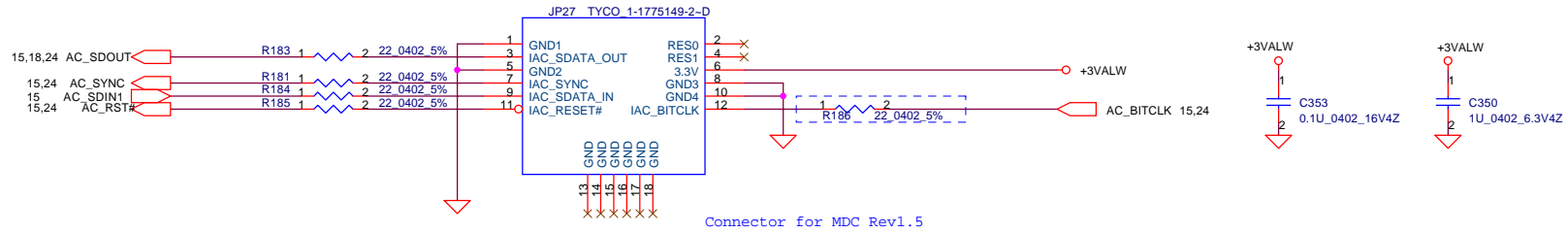
KSO7	C241	100P_0402_25V8K	KSO15	C250	100P_0402_25V8K
KSO6	C236	100P_0402_25V8K	KSO14	C249	100P_0402_25V8K
KSO5	C235	100P_0402_25V8K	KSO13	C244	100P_0402_25V8K
KSO4	C227	100P_0402_25V8K	KSO12	C240	100P_0402_25V8K
KSO3	C242	100P_0402_25V8K	KSI0	C233	100P_0402_25V8K
KSI4	C239	100P_0402_25V8K	KSO11	C247	100P_0402_25V8K
KSO2	C228	100P_0402_25V8K	KSO10	C248	100P_0402_25V8K
KSO1	C231	100P_0402_25V8K	KSI1	C230	100P_0402_25V8K
KSO0	C232	100P_0402_25V8K	KSI2	C229	100P_0402_25V8K
KSI5	C237	100P_0402_25V8K	KSO9	C245	100P_0402_25V8K
KSI6	C238	100P_0402_25V8K	KSI3	C234	100P_0402_25V8K
KSI7	C243	100P_0402_25V8K	PADS_LED#	C252	100P_0402_25V8K
KSO8	C246	100P_0402_25V8K	NUM_LED#	C253	100P_0402_25V8K
			CAPS_LED#	C251	100P_0402_25V8K

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Size		Document Number		Rev		
Customer: HAZ00/BL10E (LA2861)				1.0		
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# FAN Conn

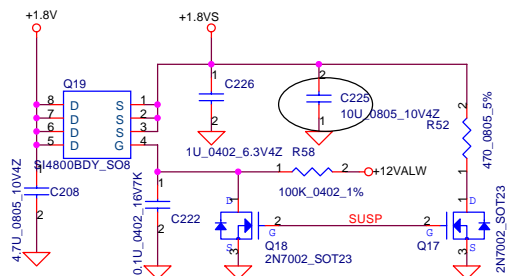


# MDC CONN.

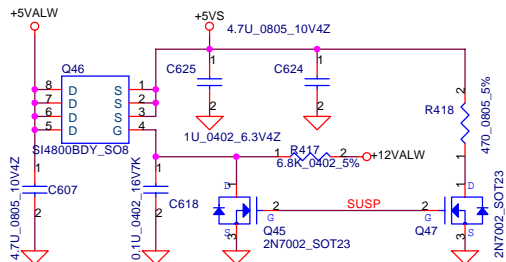


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				B	HA200/BL10E (LA2861)
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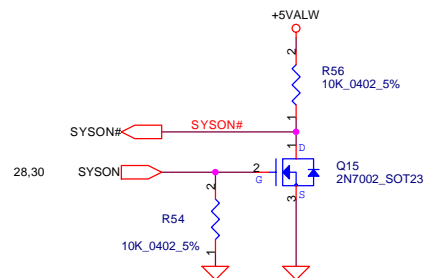
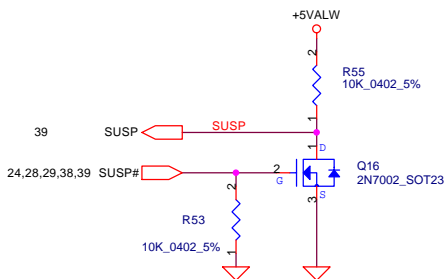
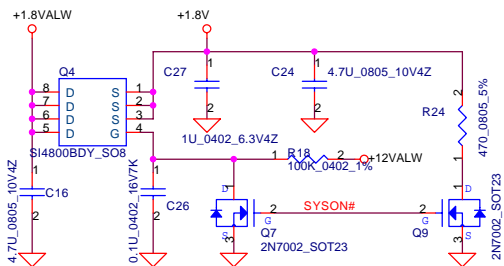
**+1.8VALW TO +1.8VS**



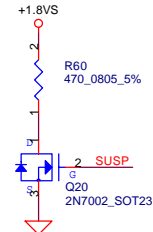
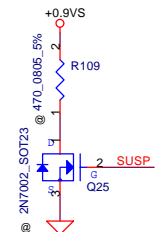
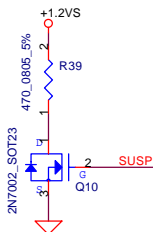
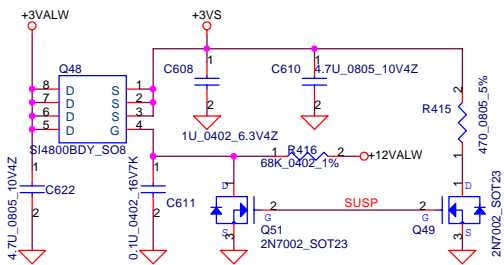
**+5VALW TO +5VS**



**+1.8VALW TO +1.8V**



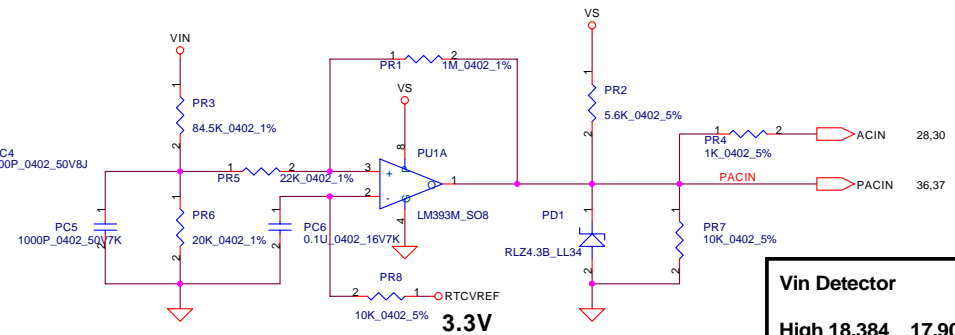
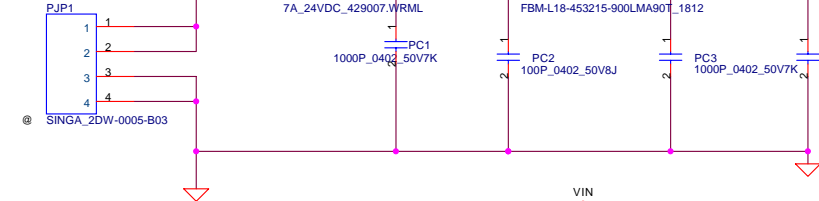
**+3VALW TO +3VS**



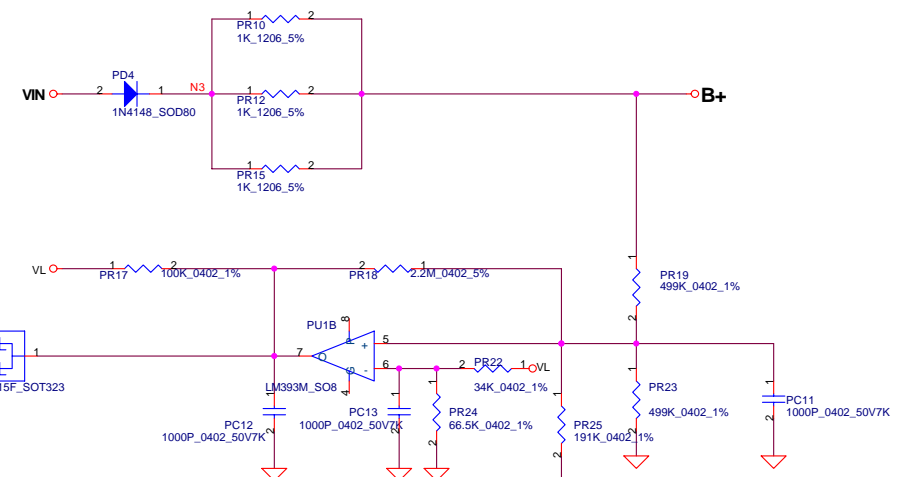
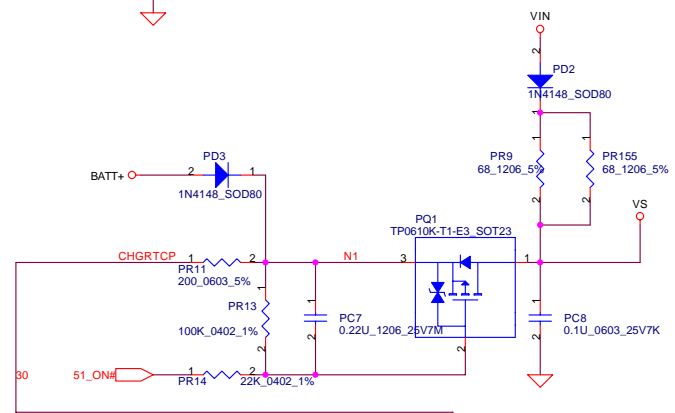
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Size	B	Document Number	HA200/BL10E (LA2861)	Rev	1.0
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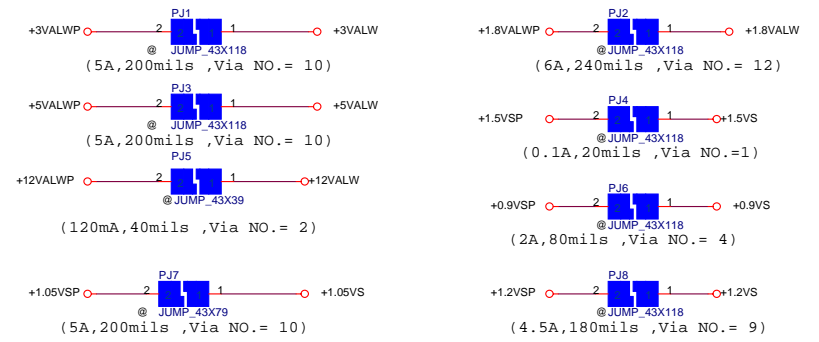
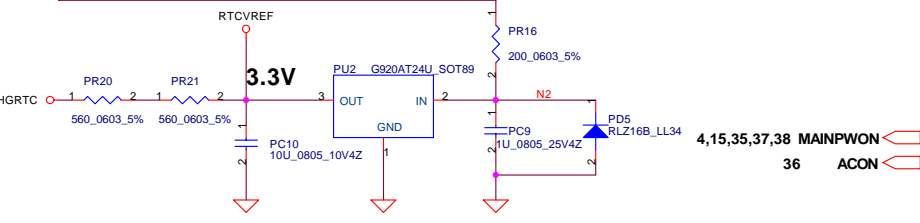
**DC301000F00**



**Vin Detector**  
 High 18.384 17.901 17.430  
 Low 17.728 17.257 16.976

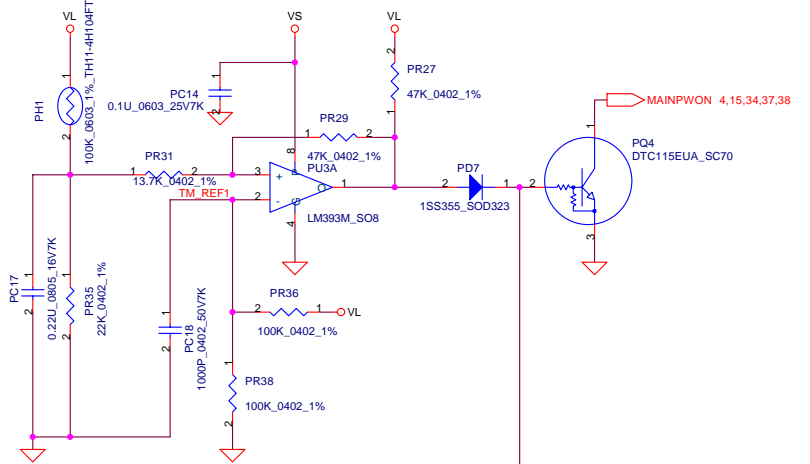
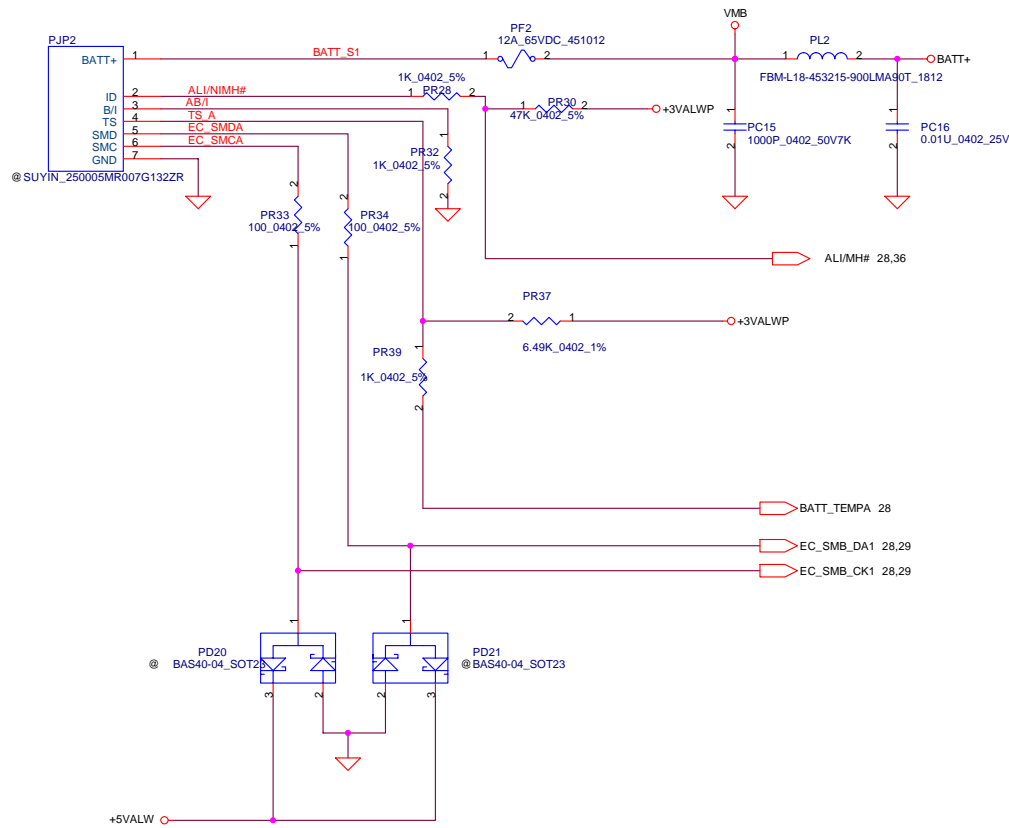


**Precharge detector**  
 15.97V/14.84V FOR  
 ADAPTOR

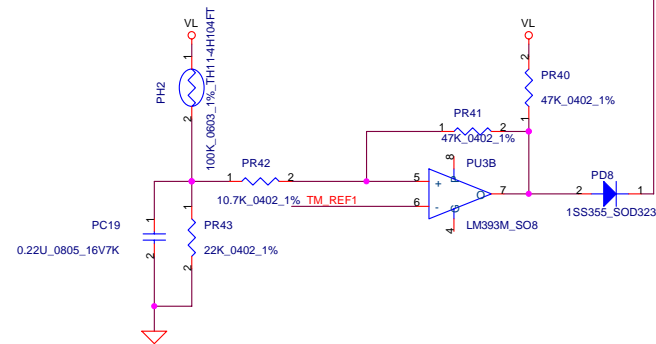


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**PH1 under CPU botten side :**  
 CPU thermal protection at 84 degree C  
 Recovery at 45 degree C



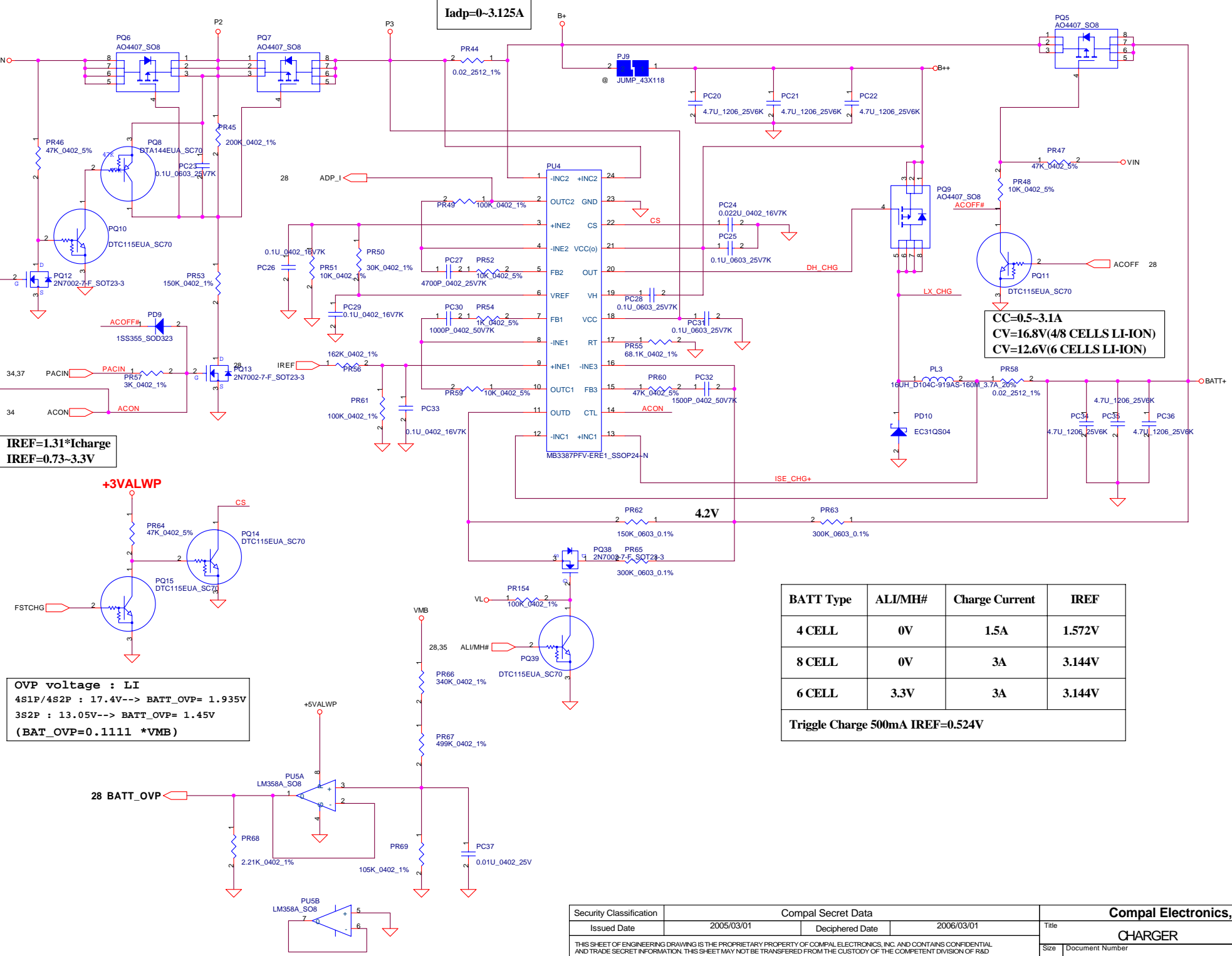
**PH2 near main Battery CONN :**  
 BAT. thermal protection at 79 degree C  
 Recovery at 45 degree C



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Iadp=0~3.125A

CC=0.5~3.1A  
CV=16.8V(4/8 CELLS LI-ION)  
CV=12.6V(6 CELLS LI-ION)



$I_{REF} = 1.31 * I_{charge}$   
 $I_{REF} = 0.73 \sim 3.3V$

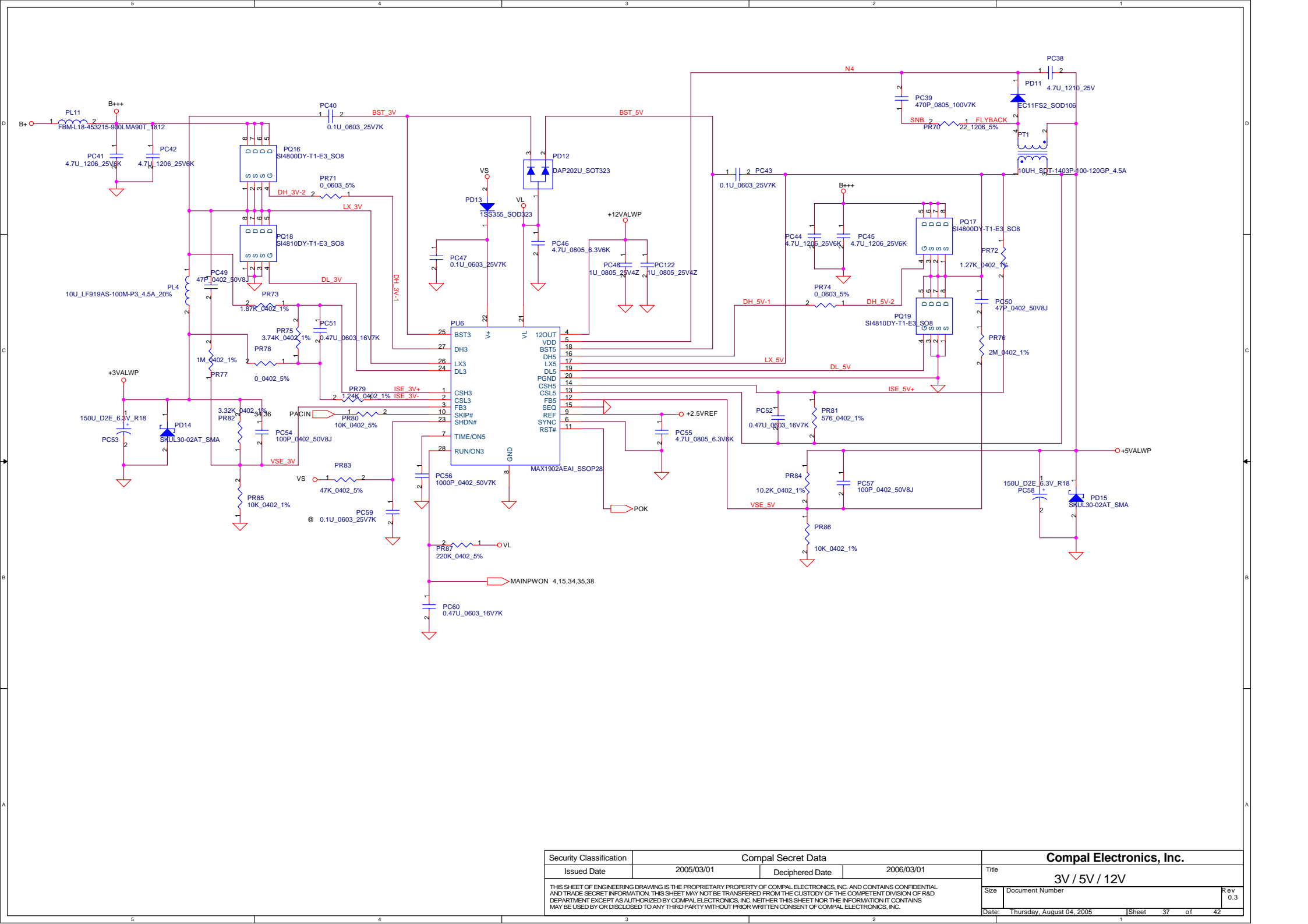
OVP voltage : LI  
4S1P/4S2P : 17.4V--> BATT\_OVP= 1.935V  
3S2P : 13.05V--> BATT\_OVP= 1.45V  
(BATT\_OVP=0.1111 \* VMB)

BATT Type	ALI/MH#	Charge Current	IREF
4 CELL	0V	1.5A	1.572V
8 CELL	0V	3A	3.144V
6 CELL	3.3V	3A	3.144V

Triggle Charge 500mA IREF=0.524V

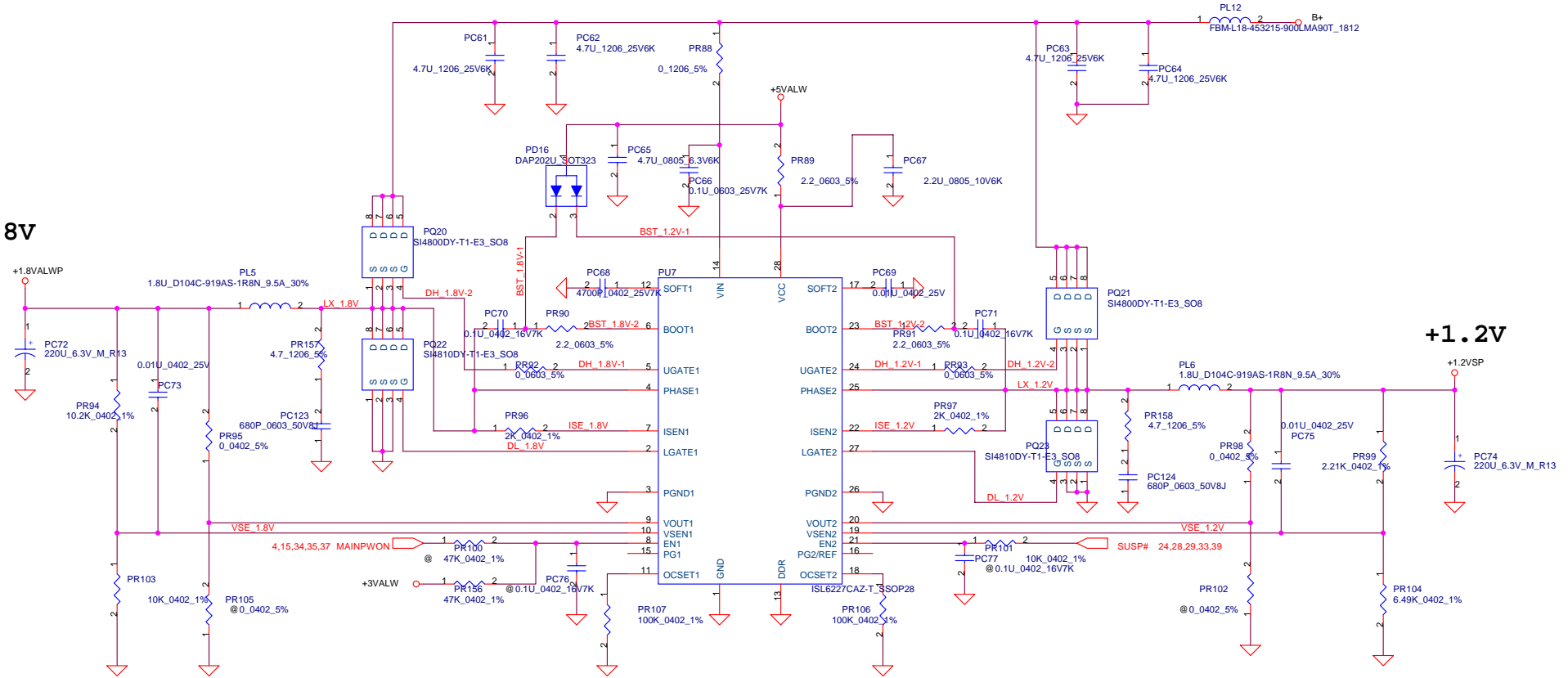
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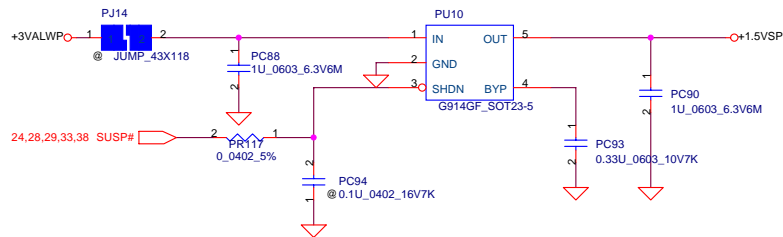
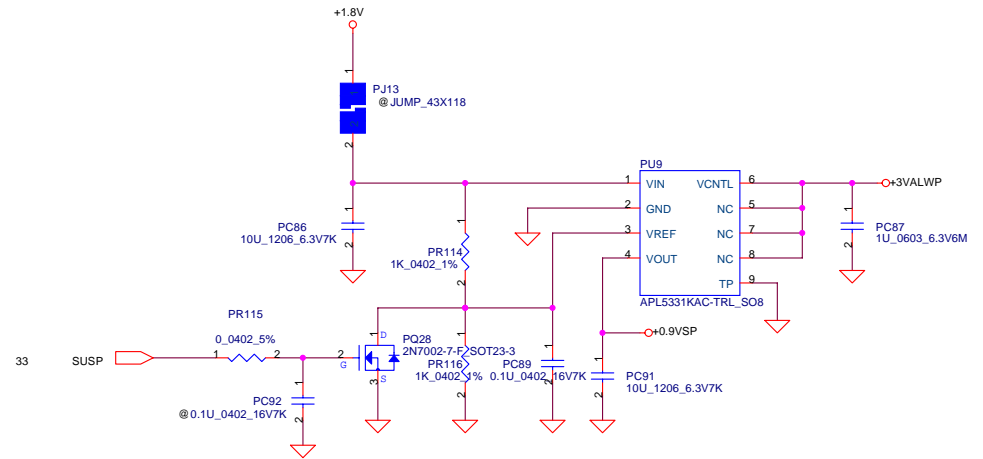
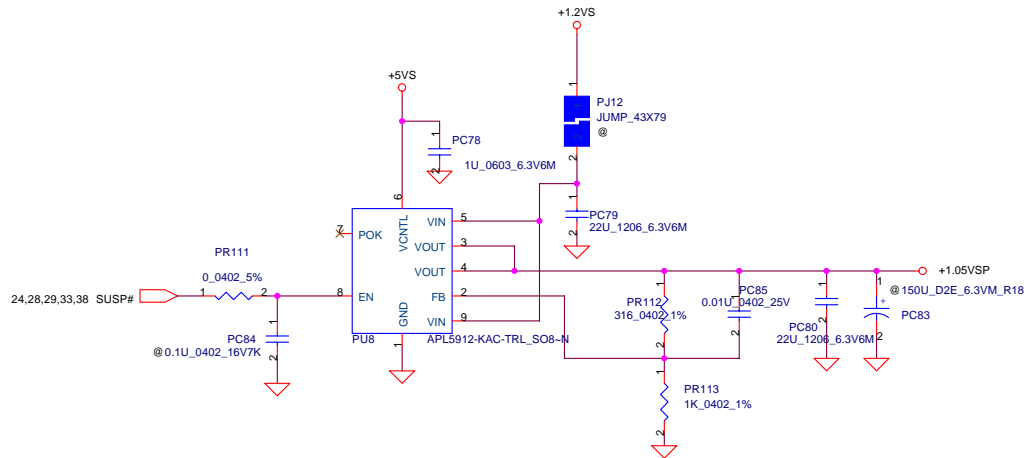
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**+1.8V**

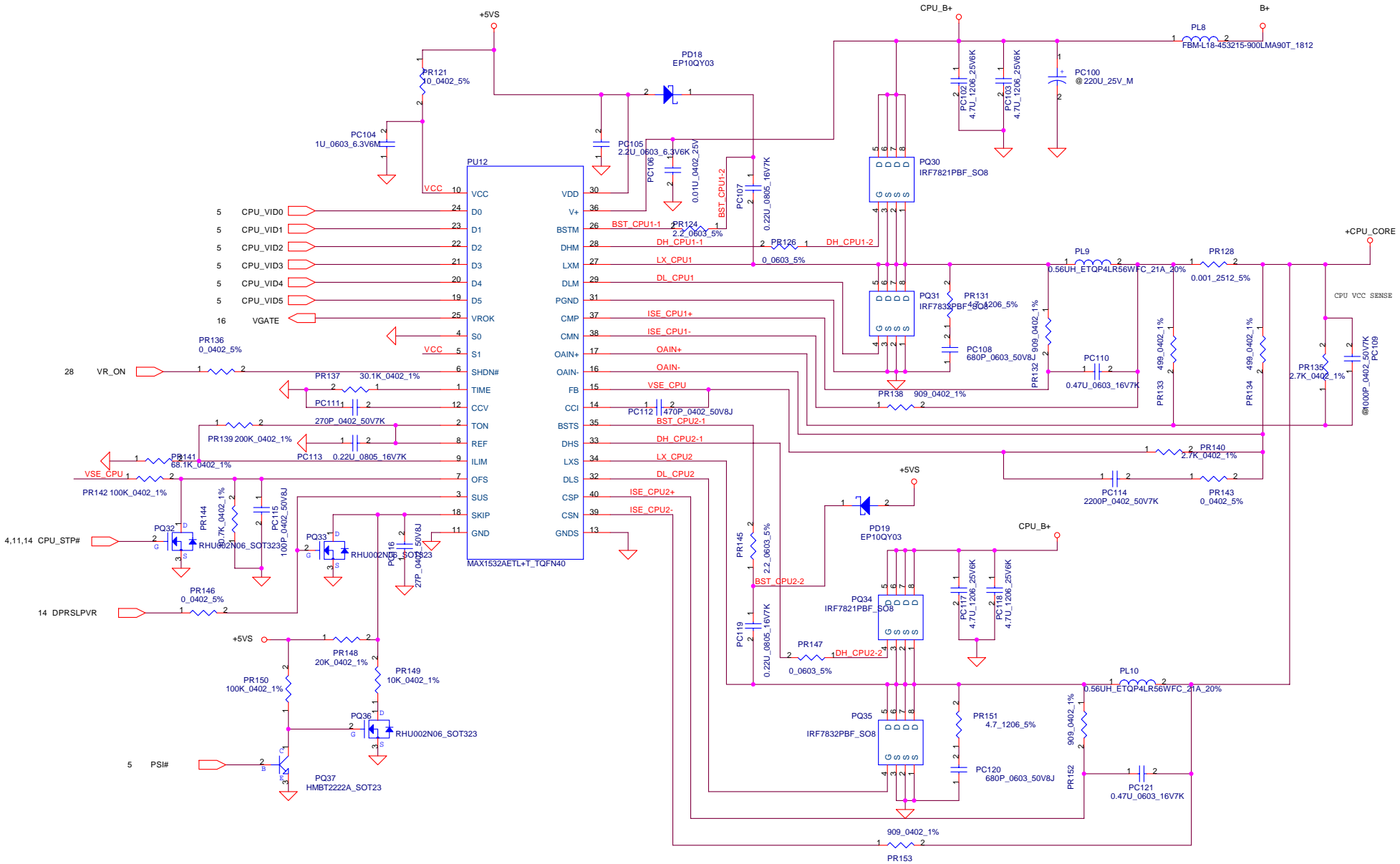


**+1.2V**

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				1.8V/VGA_CORE	
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Title		
CPU_CORE		
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0.1==>0.2		Written by Timo	
Date	Page	Action	Purpose
6/12	9	Add C642, C643 and C644	For Increase the DDR bypass capaciotrs
6/12	10	Add C645, C646 and C647	For Increase the DDR bypass capaciotrs
	12	Modify JP18 circuit	Making TV out function become correct
	15	Add @ on R317	Metting ATI reference circuit
	24	Del @ on R436	Solving MDC issue and sound slow issue
	26	Del R306 (move to sub board)	To differentiate between HAZ00 and HTW01 BIOS
	28	Add @ on Super I/O circuit	For DVT build
	29	Modify pin74 net-name of KB910	Solving reserve button no function
	31	Modify D16, D17	
		Add D35, D36	Change from double colors to signal color LED
6/22	27	Add H34, H33	For Me update new drawing

0.2==>0.3		Written by Timo	
7/8	8	Add C648, C649 and C650	Seperate the AVDD and DVDD for TVout and CRT
	17	Add C651~C657	
		Change C585, C587, C566, C533, C560, C573, C536 from 10 to 4.7U	For height limited of SB
	34	Change C225 from 4.7 to 10U	For height limited of SB
7/11	25	Del R456	
		Add Q52	For insert card bus device beep sound issue.
	27	Del R449~R454	For EMI request
7/13		Del Super I/O circuit	
	29	Add JP30, R457, C658	For LPC debug port
	23	ADD JP29, R456	For Port80 Debug card connector
	28	ADD R459, R460	For HDD password detect pin
	12	ADD J1, J4	
	22	ADD J2	
	27	ADD J3	For EMI request

0.3==>1.0		Written by Timo	
7/28	25	Add C662, R461, D37, R462, Q52	For Insert card bus device PoPo noise sound
	29	Change R101 from 8.2k to 18kohm	For Board ID change
	14	Change C587, C585, C651, C652, C566, C553, C560, C573, C653, C654, C655, C656, C536, C657	
	17	from 4.7U to 1U	For avoide the interfere area of HDD
		Change C288 from 150U fo 470UF	Making the capacitors of 1.8VS source blance of SB
		Add C660, C661	Making the capacitors of 1.8VALW and 3VS sources blance of SB
7/30	4	Add @ in C261	For throttle issue
	5	Add @ in C180	For cost down
	12	Add L38, L39, L40	For EMI issue

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EVT

page	Reason for change	Modify list
37	12V noise	Change PC38 from 4.7u_1206_25V to 4.7u_1210_25V
37	Lead free parts	Change PC53,PC58 to NEC lead free parts.
38	Modify 1.8V power sequence for HW requirement	Change PR100 from 0_0402_5% to 47K_0402_1% Add 0.1u_0402_16V at PC76
39	Modify 1.05V circuit	Delete PQ24,PQ26,PL7,PD17,PC82,PC81,PR109,PQ25,PQ27,PR110 Change PU8 to APL5912-KAC-TRL Change PC85 to 0.01u_0402_25V Change PR112 to 316_0402_1% Change PR13 to 1K_0402_1%
39	Delete reserved 1.5V circuit	Delete PU11,PC95,PR118,PR120,PQ29,PR119,PC99,PC97,PC98,PC96
39	Change 1.5V IC	Change PU10 from APL5151 to G914
40	Add snubber for CPU CORE	Add 4.7_1206_5% to PR131,PR151 Add 680P_0603_50V to PC108,PC120
37,38	Add bead at 3V/5V and 1.2V/1.8V input for EMI requirement	Add PL11,PL12 to replace PJ10,PJ11

DVT

34	Change VS resistor to 33 ohm	Change PR9 from 47_1206_5% to 33_1206_5%
34	Change 1N4148 to lead free P/N	Change PD2,PD3,PD4 P/N to SC11N414880
40	Change HMBT2222 to lead free P/N	Change PQ37 P/N to SB322220080
38	Raise 1.8V to 1.82V for HW requirement	Change PR94 from 10K_0402_1% to 10.2K_0402_1%

PVT

34	Change VS resistor to standard part	Change PR9 from 33_1206_5% to 68_1206_5% Add 68_1206_5% at PR155
38	Change 1.8VALWP power sequence for HW requirement	Change 47K_0402_1% from PR100 to PR156 Delete PC76 Change PC68 from 0.01u_0402_25V to 4700P_0402_25V

Pre-MP

38	Add BOOST 2.2 ohm and snubber at 1.8V / 1.2V for EMI	Add 4.7_1206_5% to PR157,PR158 Add 680P_0603_50V to PC123,PC124 Change PR90,PR91 from 0_0603_5% to 2.2_0603_5%
42	Change CPU CORE mosfet for EMI	Change PQ30,PQ34 from AO4408 to IRF7821 Change PQ31,PQ35 from AO4410 to IRF7832
42	Delete CPU VID 0 ohm debug resistor	Delete PR122,PR123,PR125,PR127,PR129,PR130

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