

HTW2E

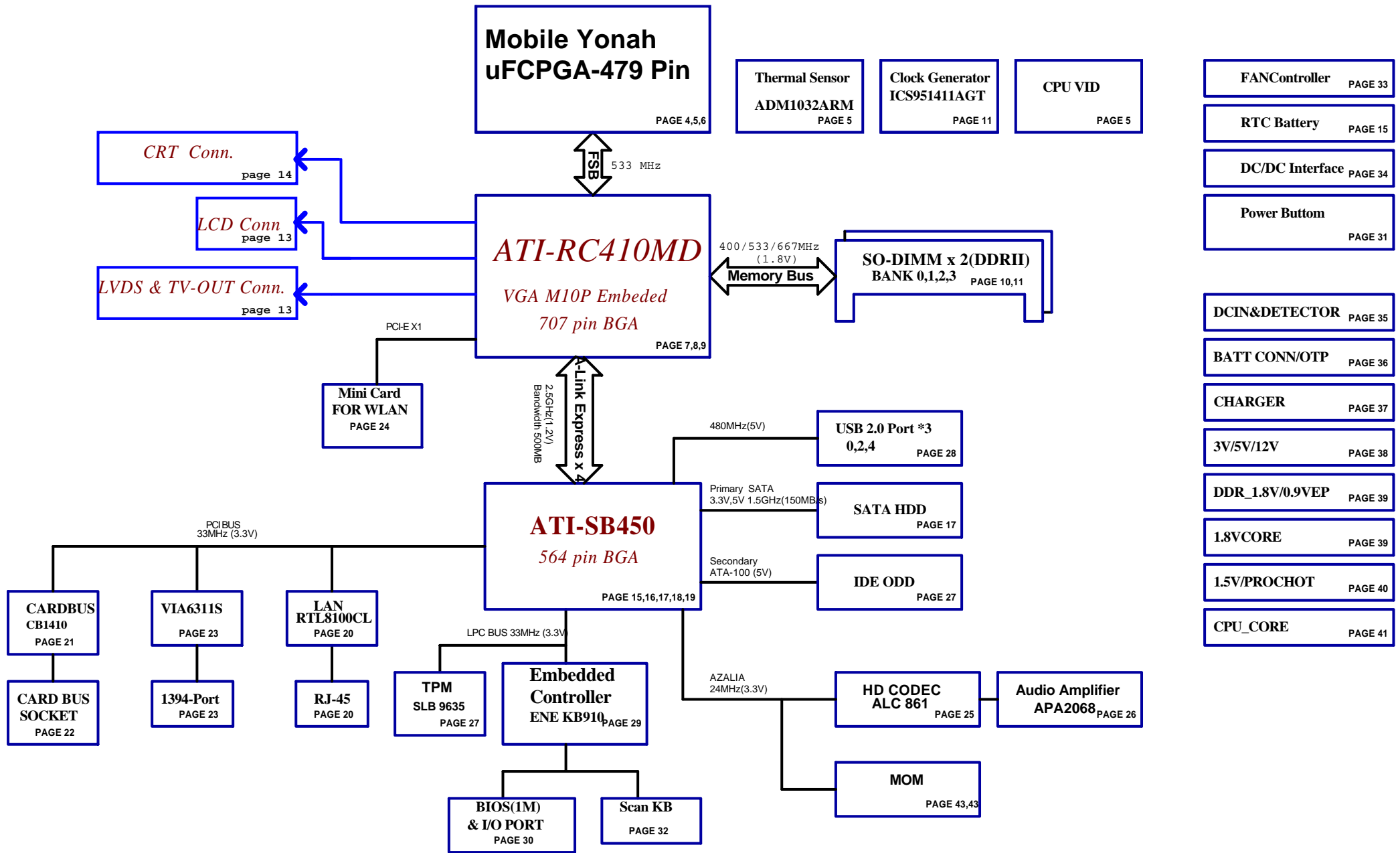
LA-3201P REV 1.0 Schematic

UFC-PGA Yonah/ RC410MD(ME)/ SB450

2006-04-18 Rev. 1.0

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HTW2E LA-3201P FUNCTION BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	DOTHAN B	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
TI 1410	AD20	2	PIRQB
LAN	AD22	1	PIRQG
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b

EC SM Bus2 address

SB450 SM Bus address

Device	Address
Clock Generator (ICS951413BGLFT)	1101 001Xb
DDR DIMM0	1010 0100b A4
DDR DIMM1	1010 0110b A6

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

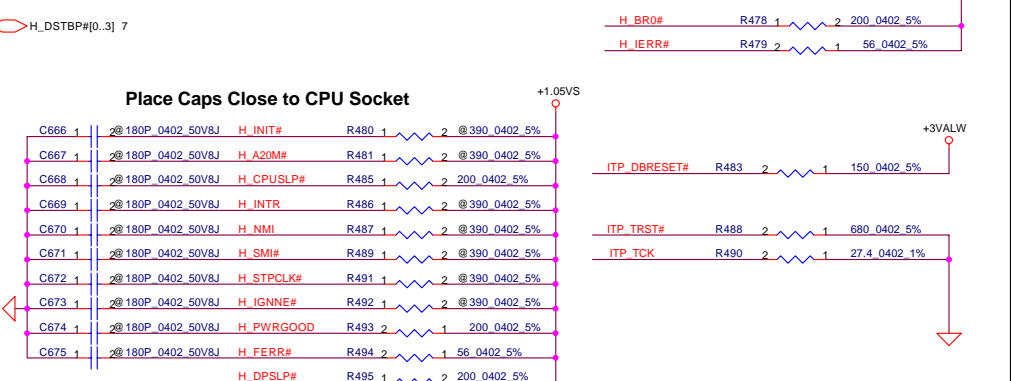
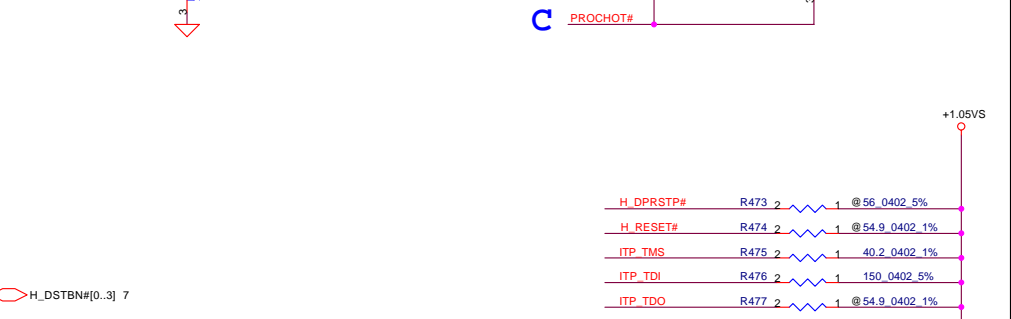
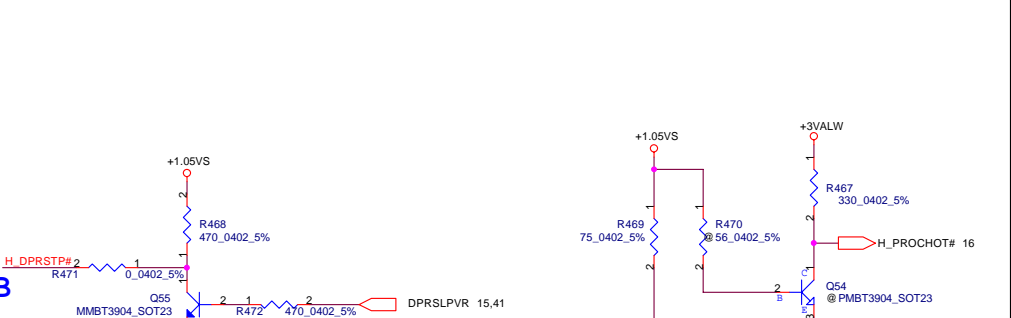
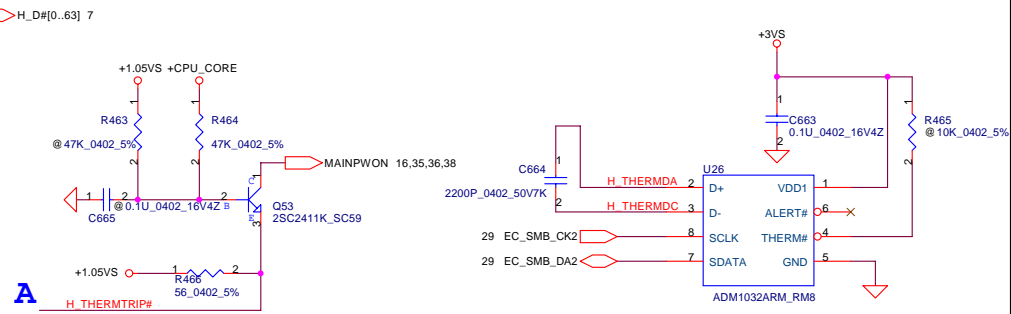
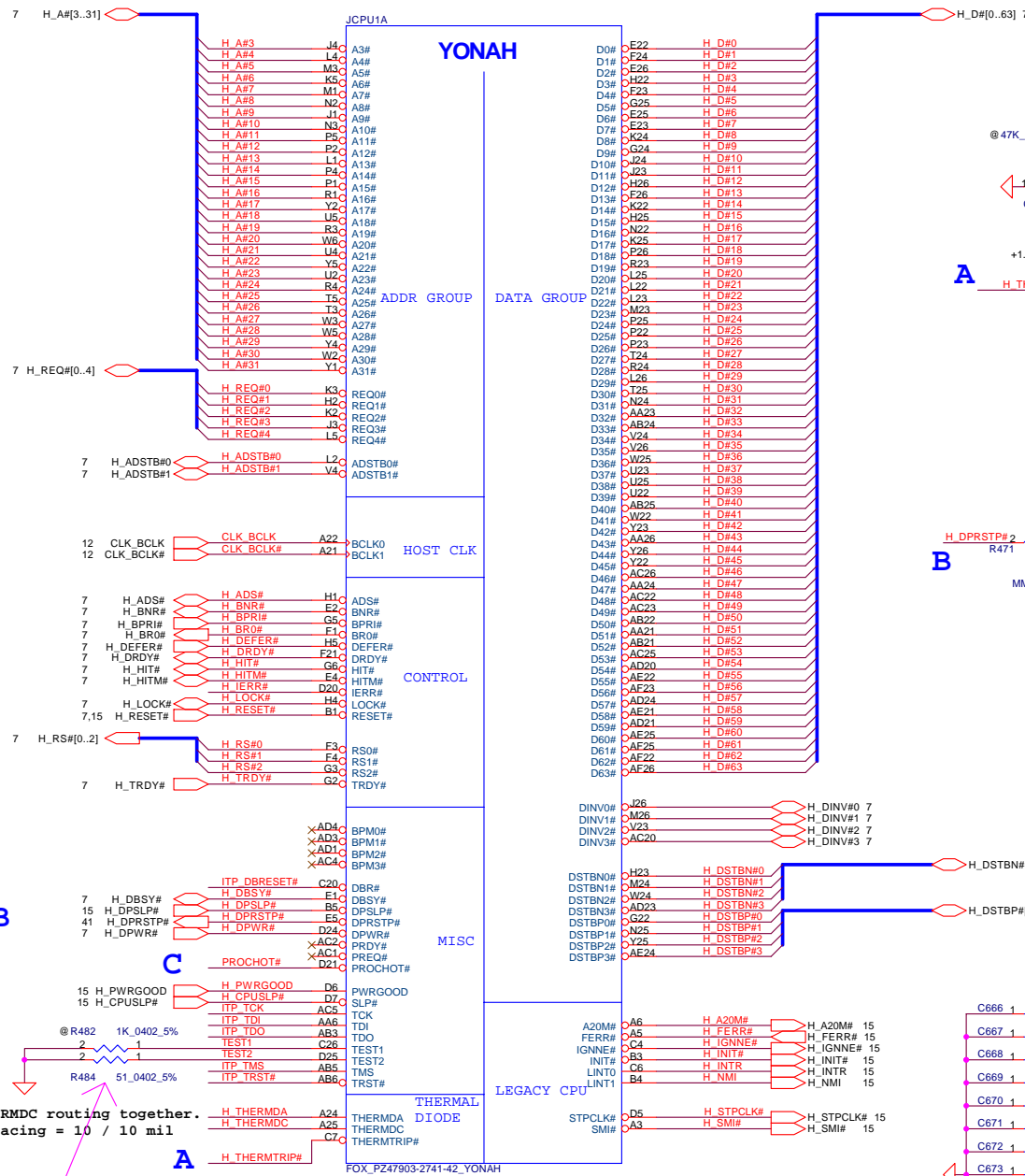
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO	BOM STURCTURE
WIRELESS	WLAN@
1394	1394@

SKU ID	BTN_ID
0	1 Buttons
1	7 Buttons
2	
3	
4	
5	
6	
7	

SKU_ID	SKU_ID
0	WW
1	JP
2	
3	
4	
5	
6	
7	

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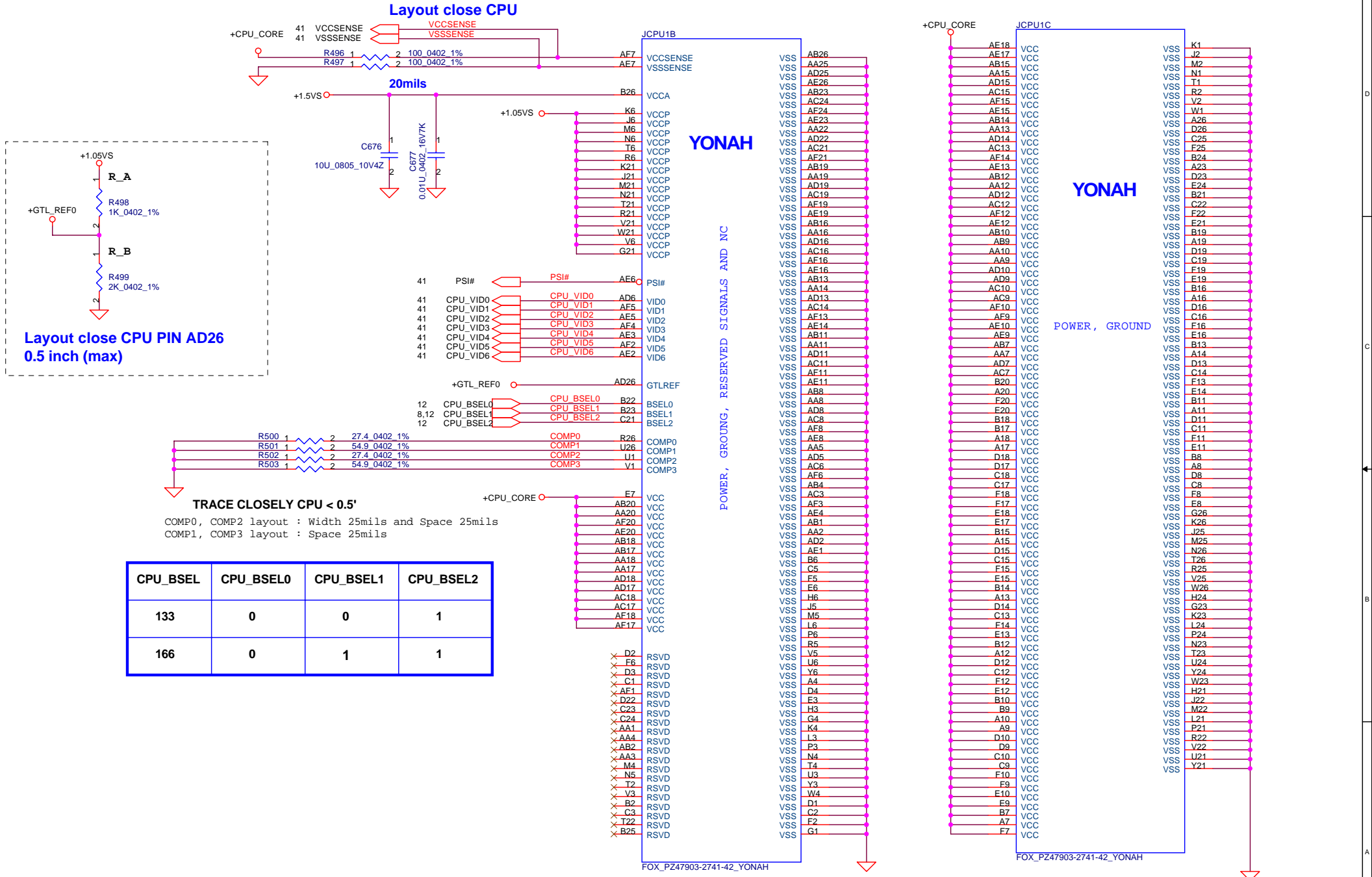


H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

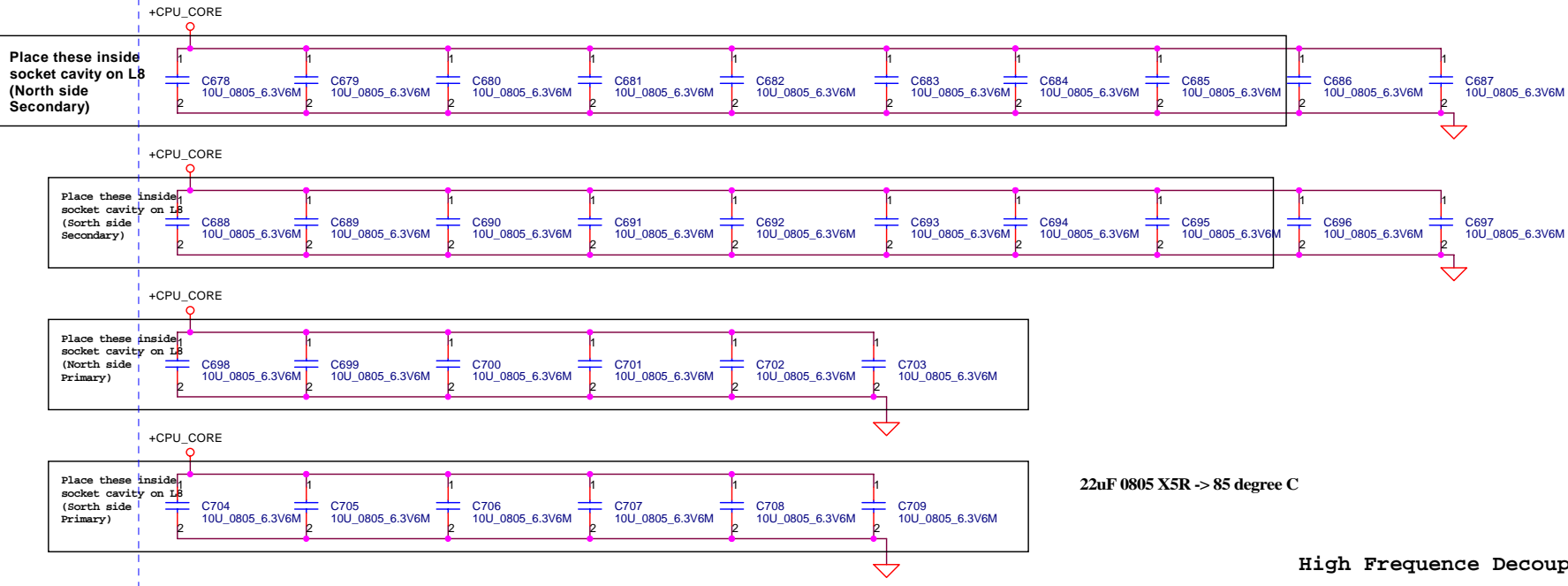
For B-0 stepping engineering samples (ES) of Celeron M processor need to pop this 51 ohm resistor.

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Length match within 25 mils



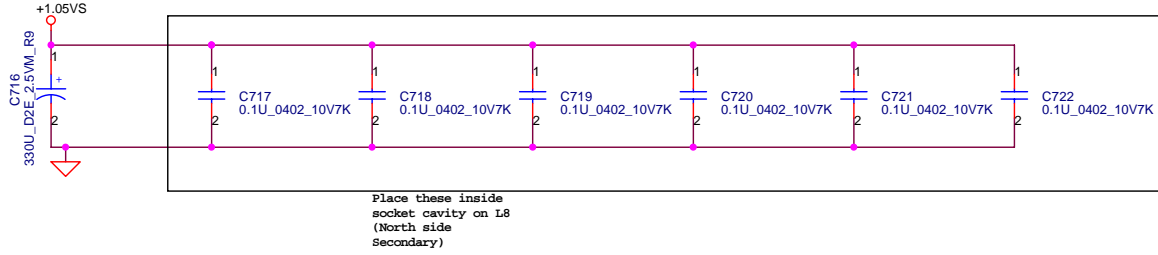
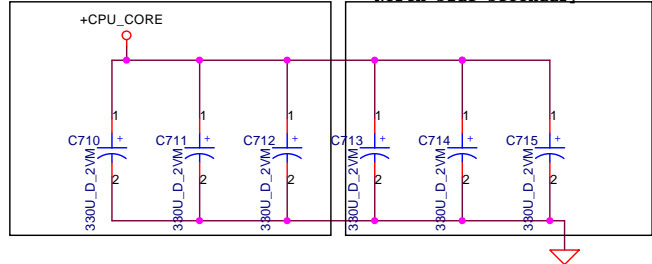
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Near VCORE regulator.

South Side Secondary

North Side Secondary



9mOhm 9mOhm 9mOhm 9mOhm 9mOhm 9mOhm
 7343 7343 7343 7343 7343 7343
 PS CAP PS CAP PS CAP PS CAP PS CAP PS CAP

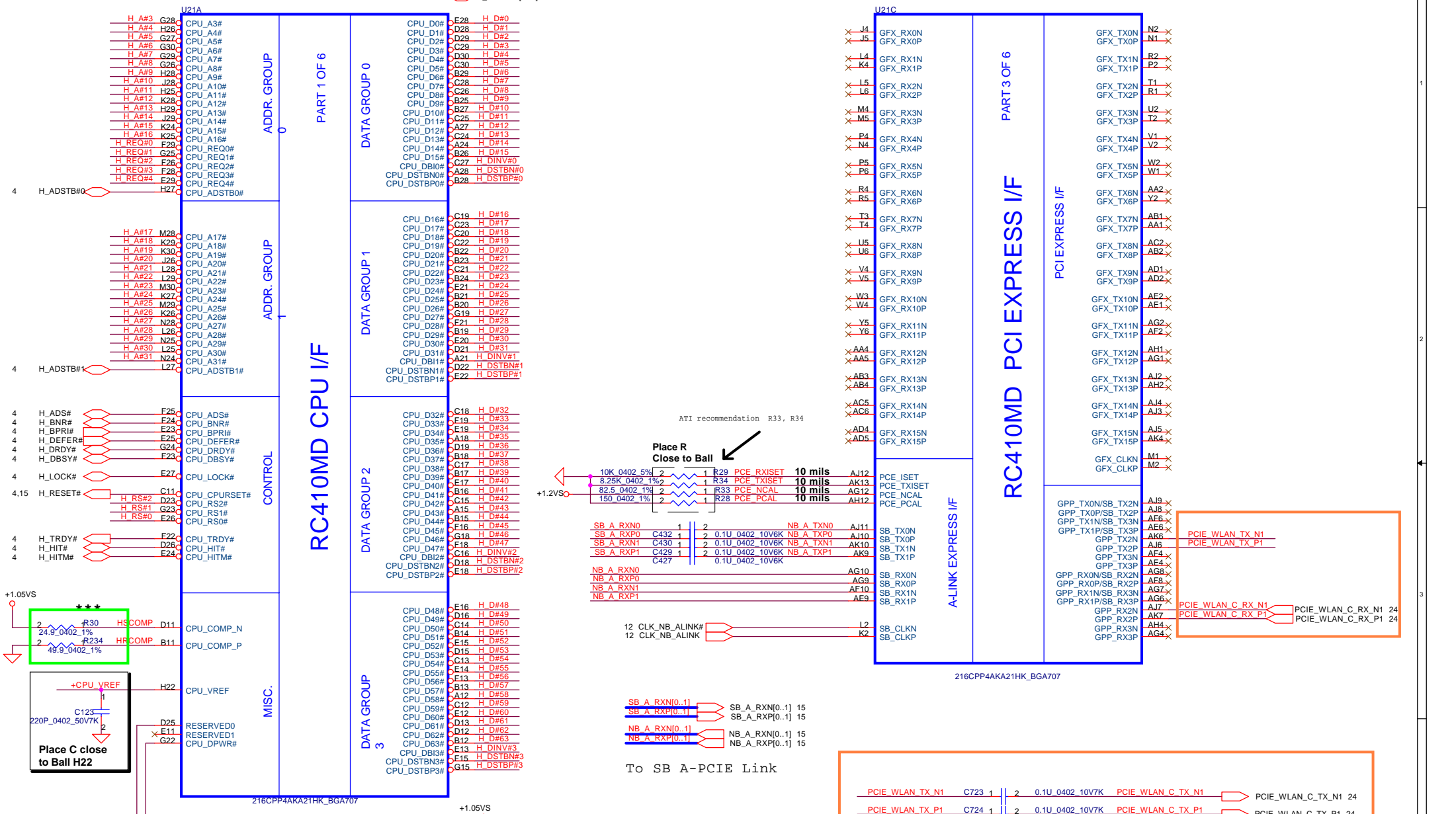
**ESR <= 1.5m ohm
 Capacitor > 1980uF**

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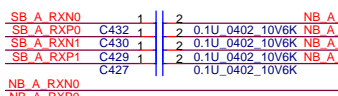
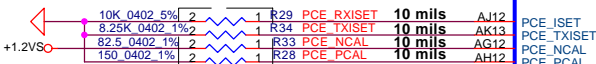
H_A#[3..31]
 H_REQ#[0..4]
 H_RS#[0..2]

H_D#[0..63] 4
 H_DINV#[0..3] 4
 H_DSTB#[0..3] 4
 H_DSTBP#[0..3] 4

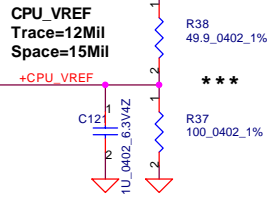
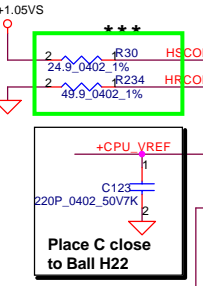
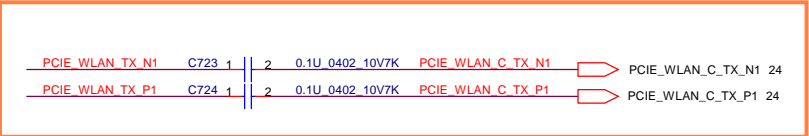


ATI recommendation R33, R34

Place R Close to Ball

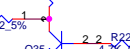
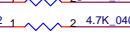
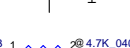
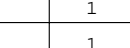
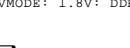
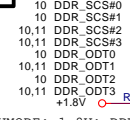
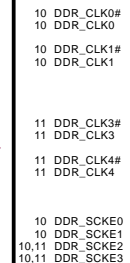
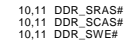
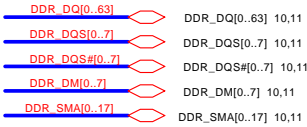


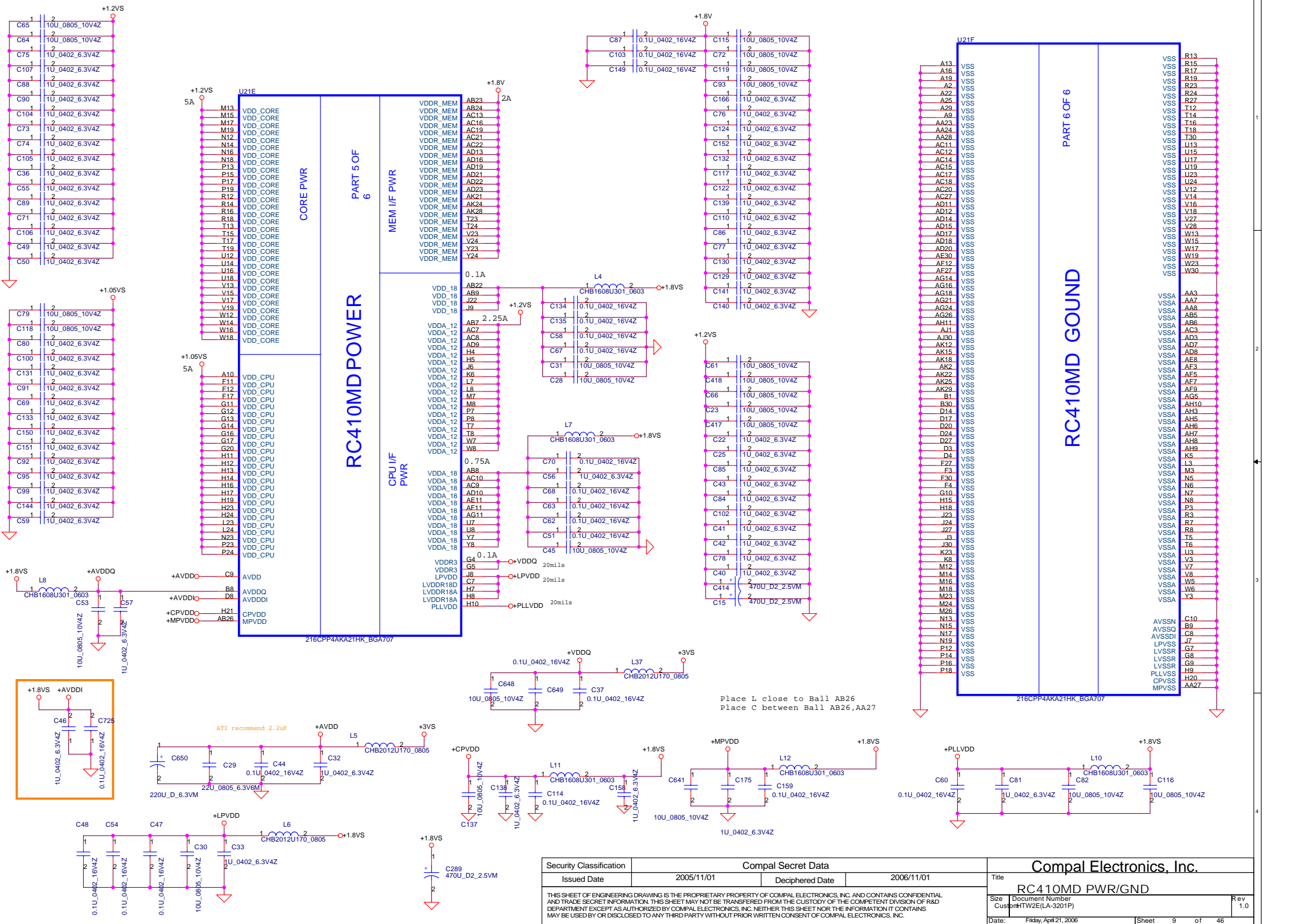
To SB A-PCIE Link



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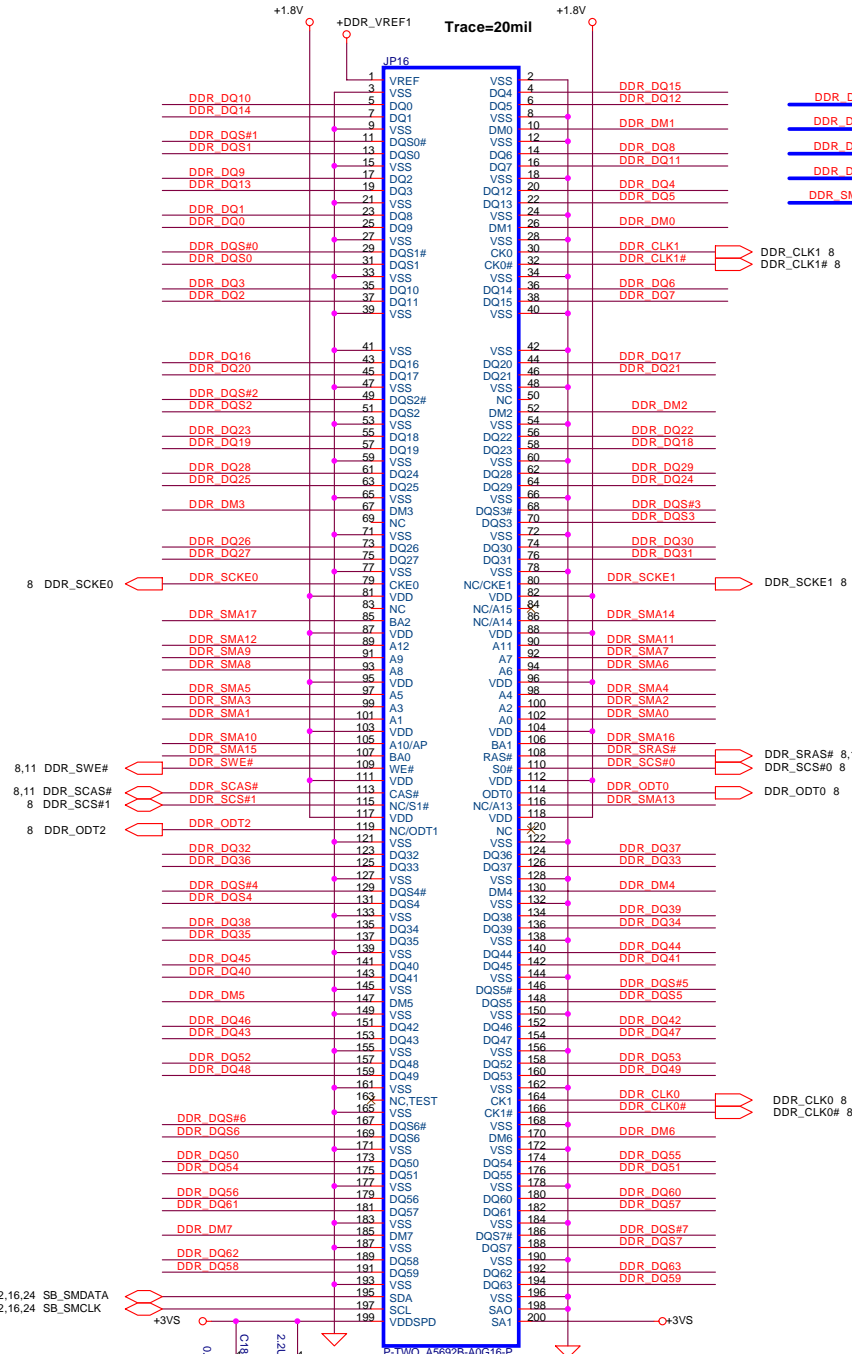


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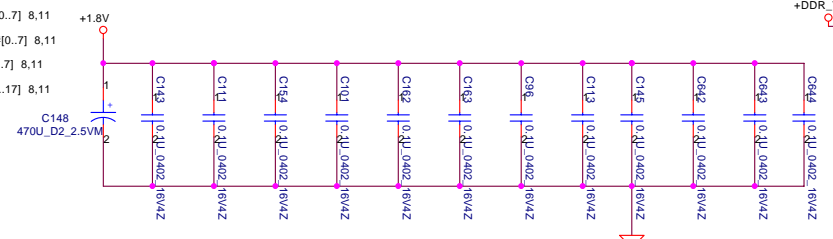
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Place L close to Ball AB26
Place C between Ball AB26, AA27

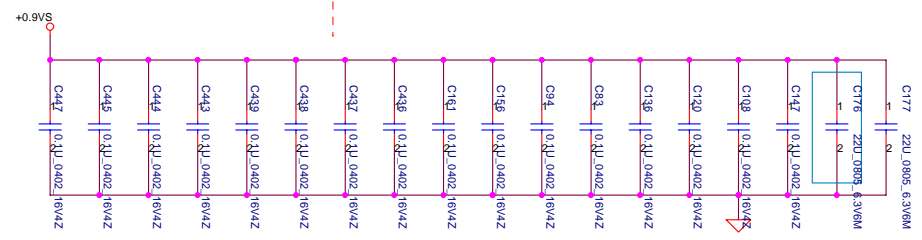


DIMMA Reverse

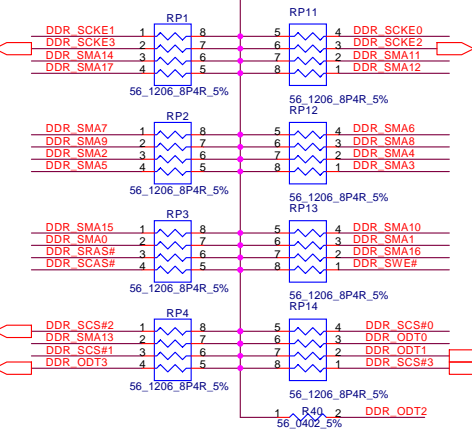
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to V_DDR_MCH_REF



Layout Note:
Place these resistor closely JDIM2, all trace length < 750 mil

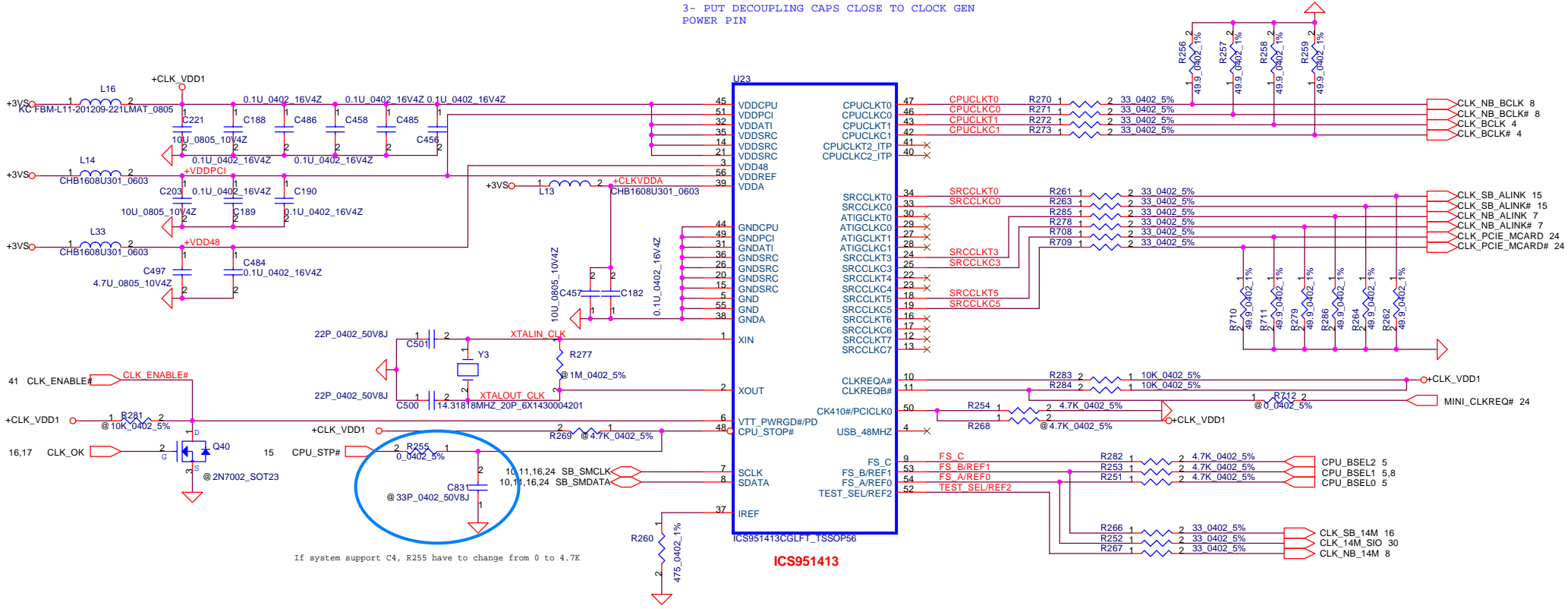


Layout Note:
Place these resistor closely JDIM2, all trace length Max=1.3"

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Clock Generator

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN

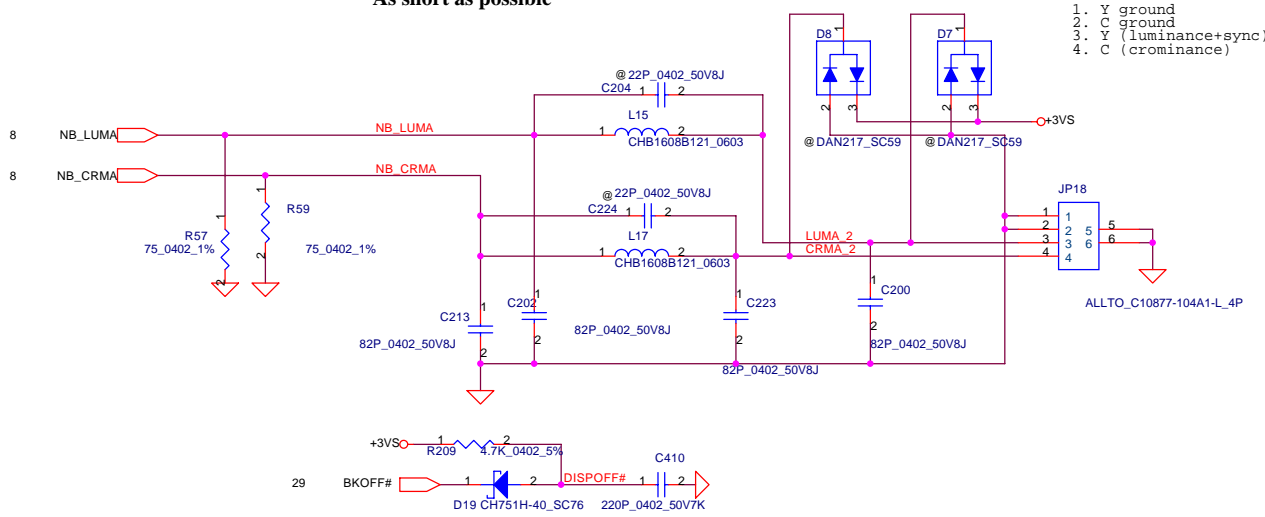


If system support C4, R255 have to change from 0 to 4.7K

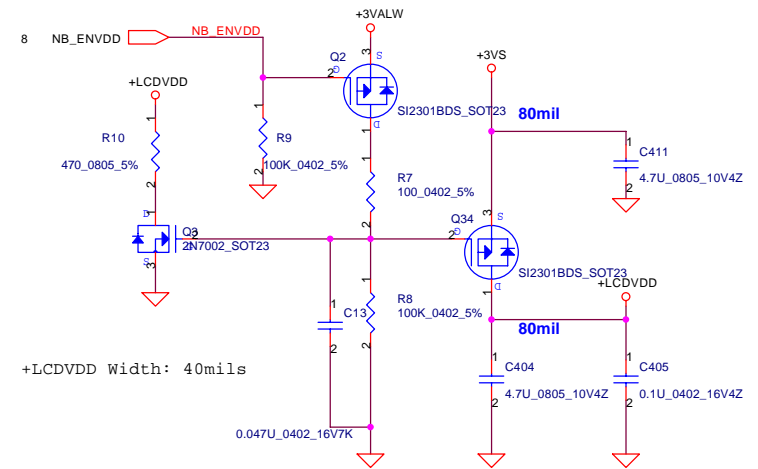
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

TV-OUT CONNECTOR

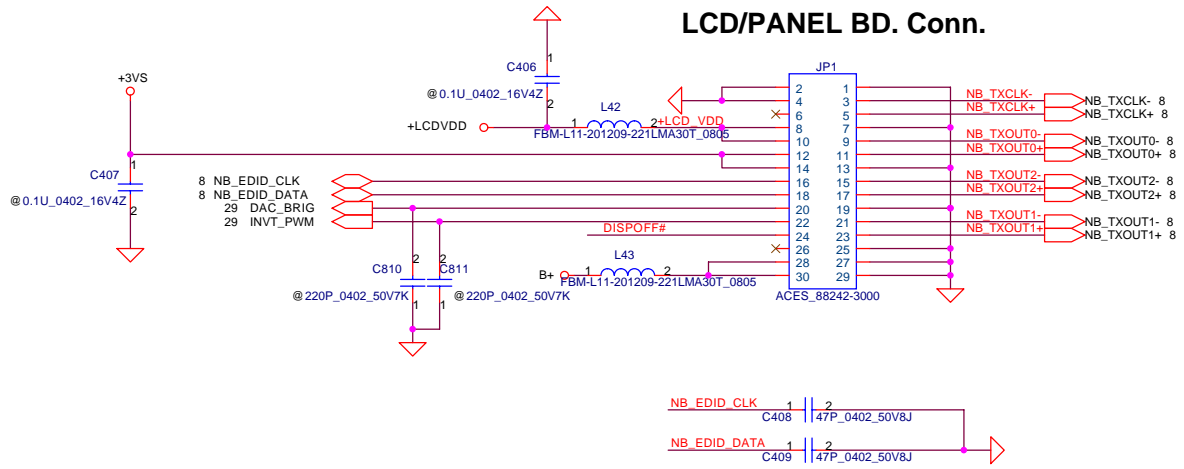
Reduce LUMA_1 and CRMA_1 length
As short as possible



PANEL +LCDVDD CTRL CKT

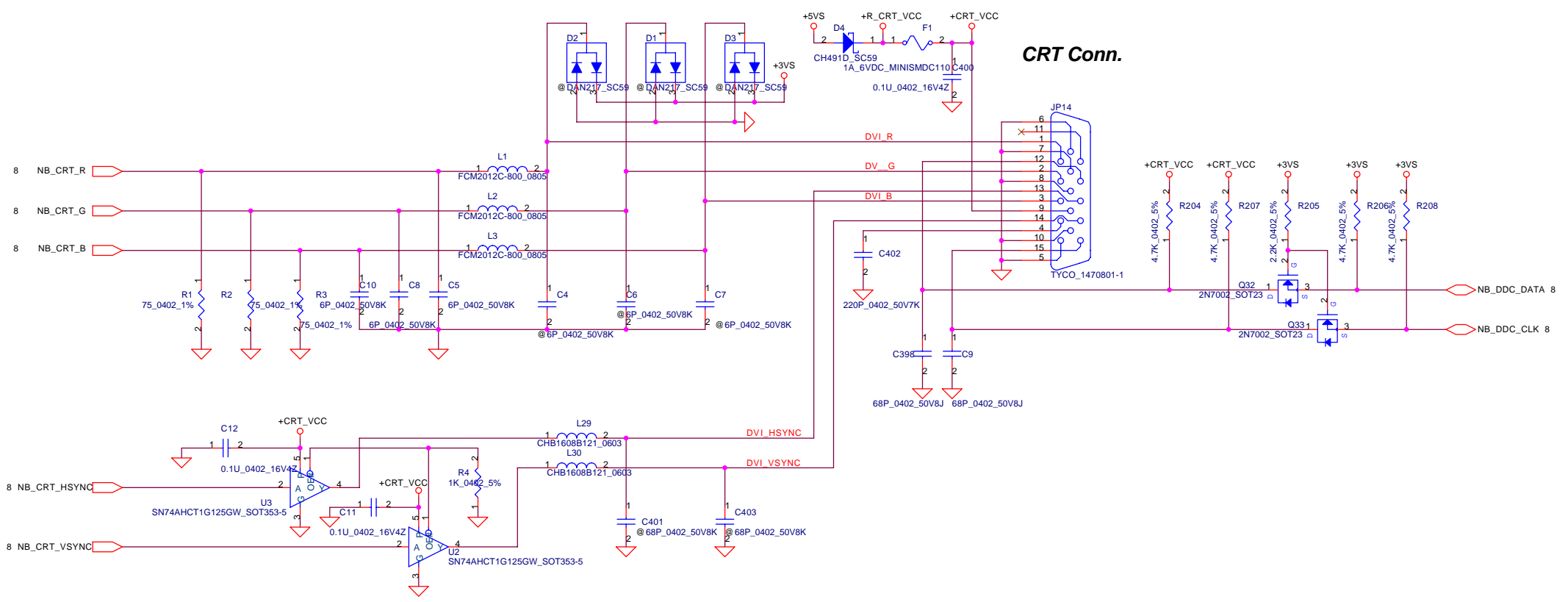


LCD/PANEL BD. Conn.

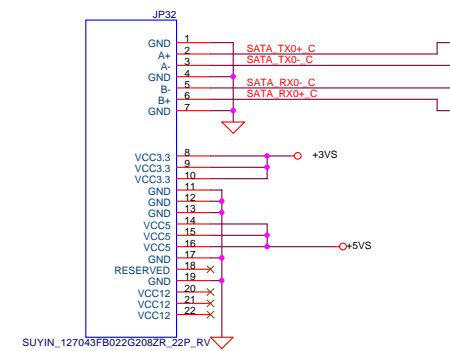
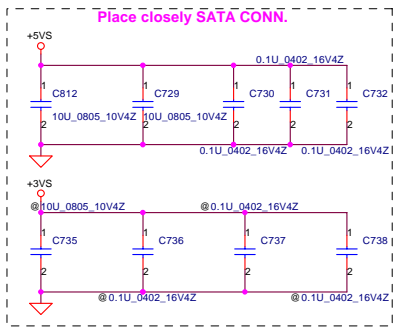


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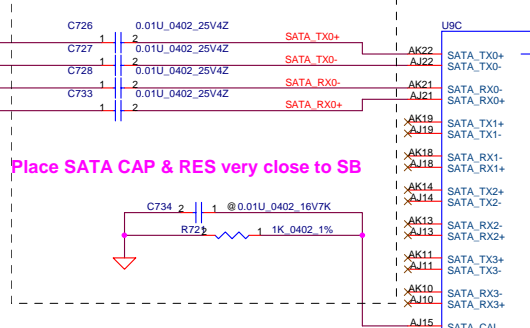
CRT CONNECTOR



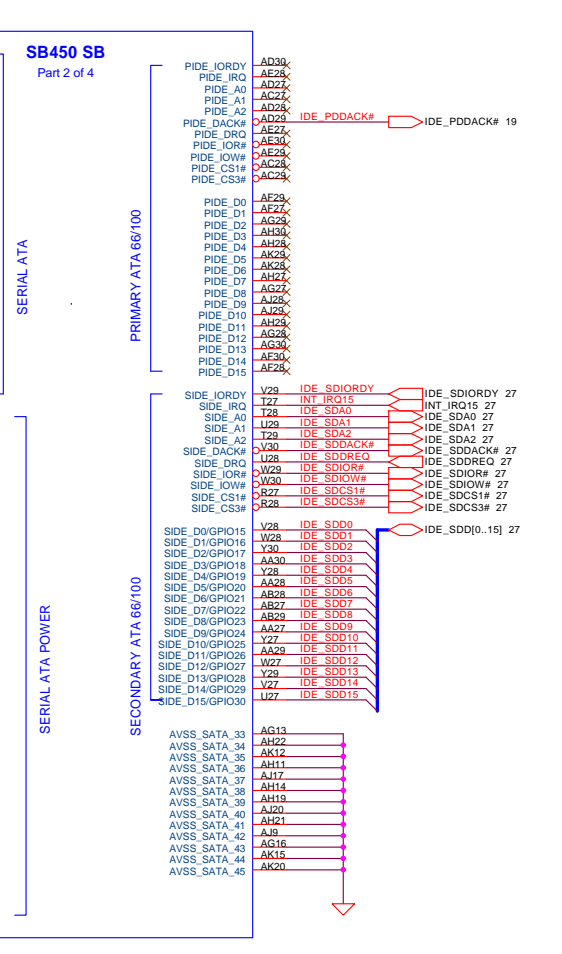
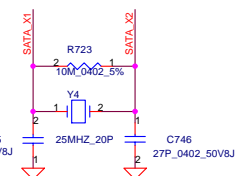
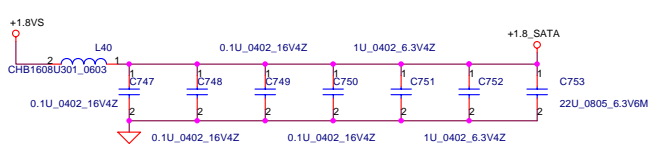
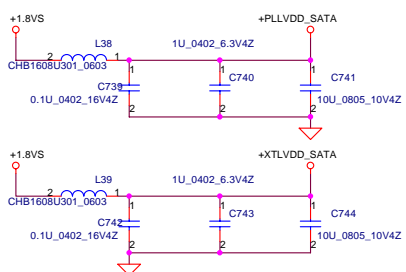
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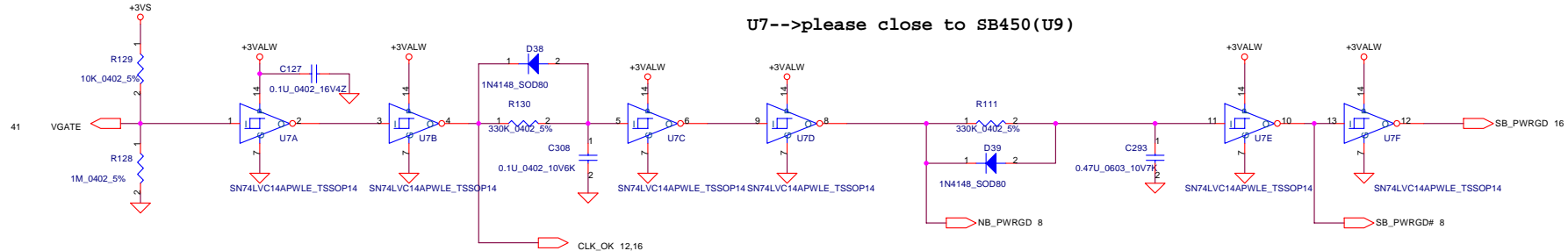
SATA HDD CONNECTOR



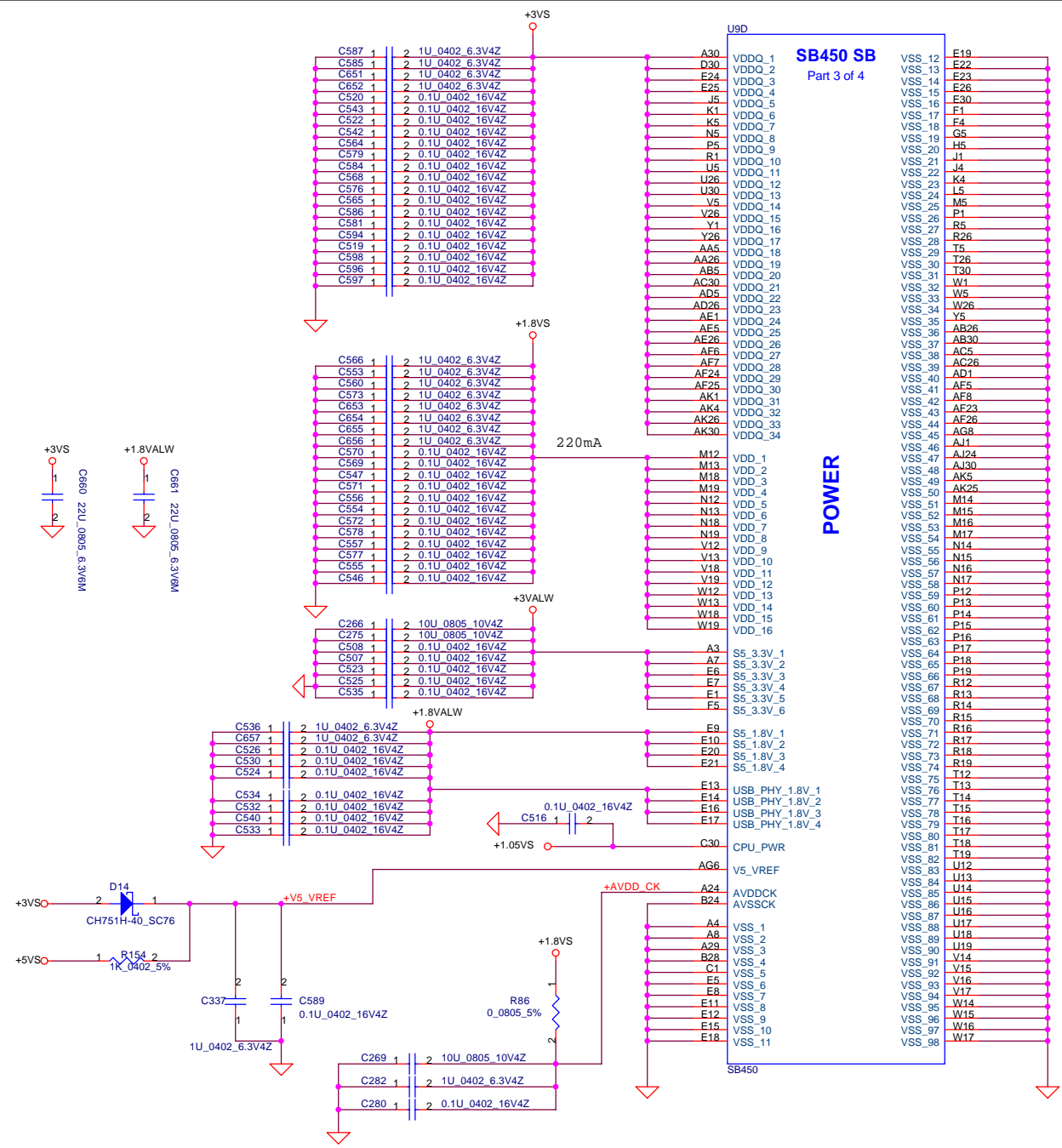
Place SATA CAP & RES very close to SB



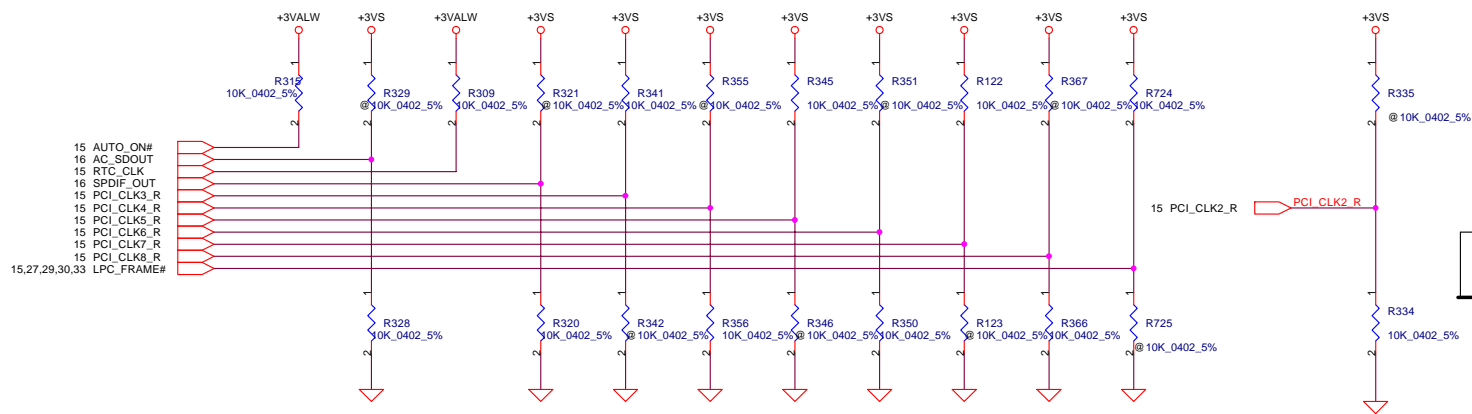
U7-->please close to SB450(U9)



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Size	Document Number	Rev	1.0	
Date:	Friday, April 21, 2006	Sheet	17	of 46



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Size	Document Number			Rev
B	HTW2E(LA-3201P)			1.0
Date:	Friday, April 21, 2006	Sheet	18 of 46	

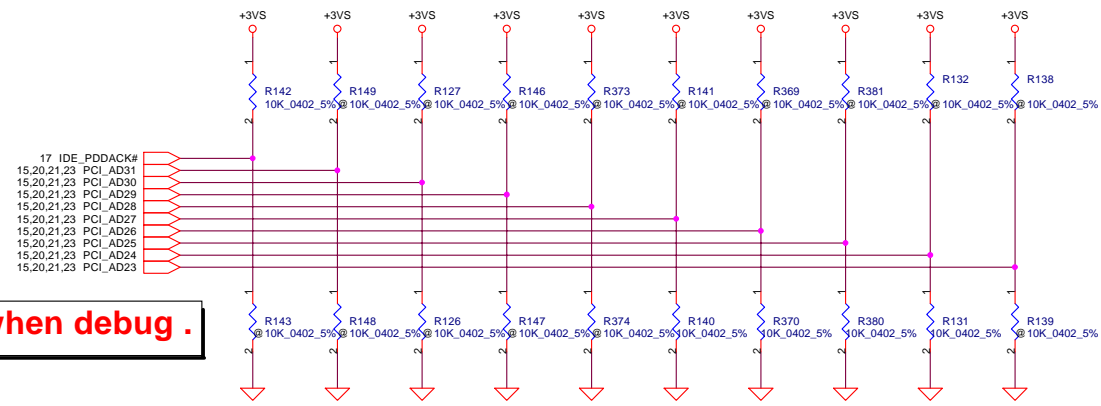


Selects type of 48MHz clock pad

ACPWRON

	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK2_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE	Internal PLL	PCIE CM_SET low DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		Crysal Pad	THERMTIP# ENABLE
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	PCIE CM_SET HIGH	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		Clock input buffer DEFAULT	THERMTIP# DISENABLE

REQUIRED STRAPS

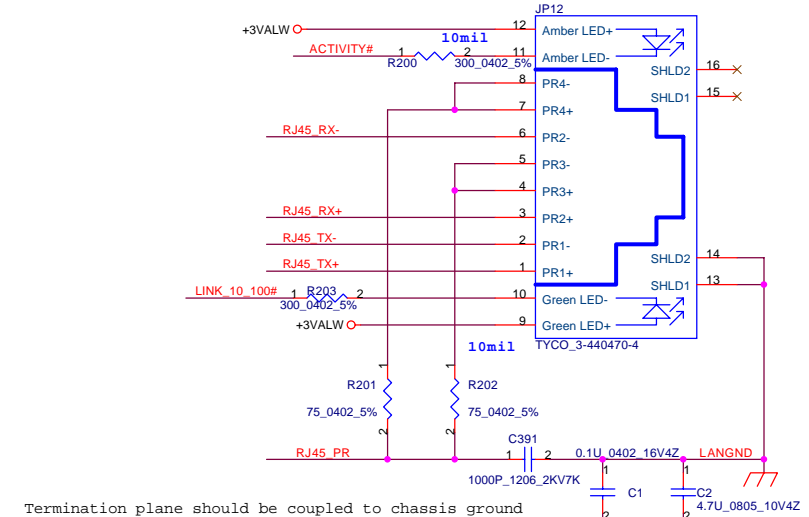
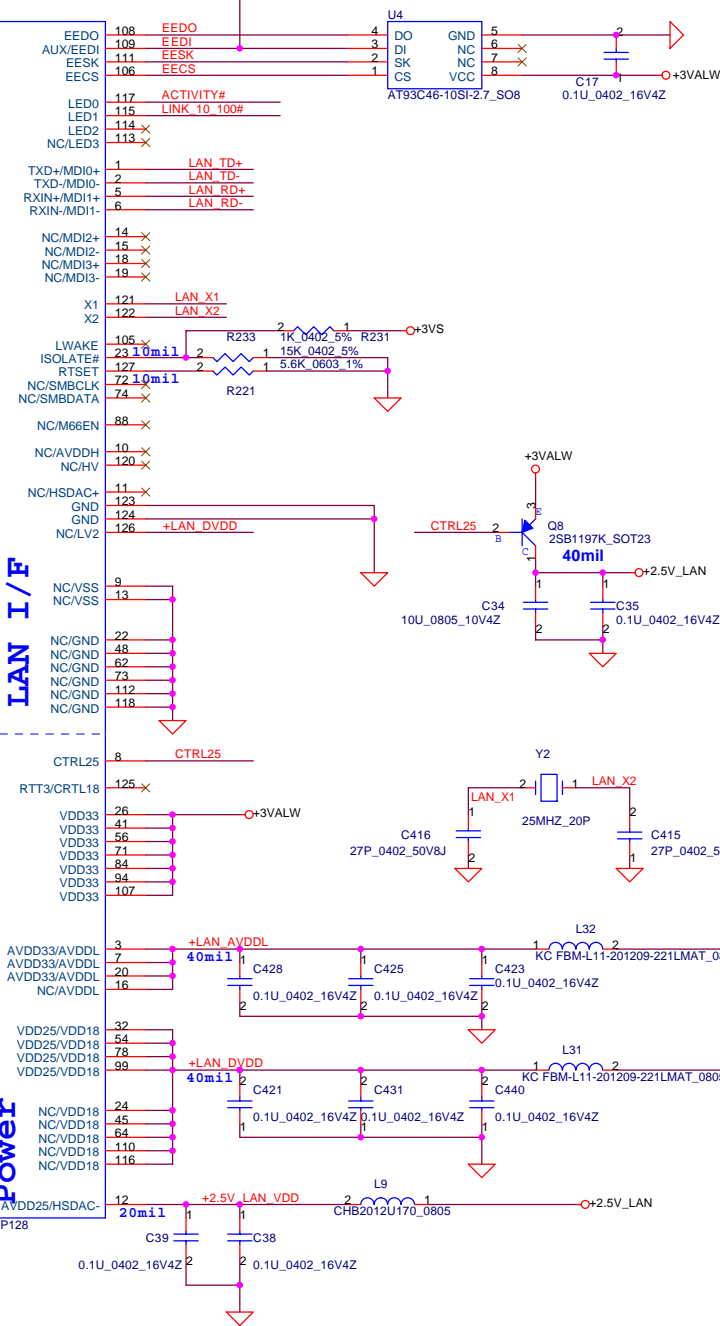
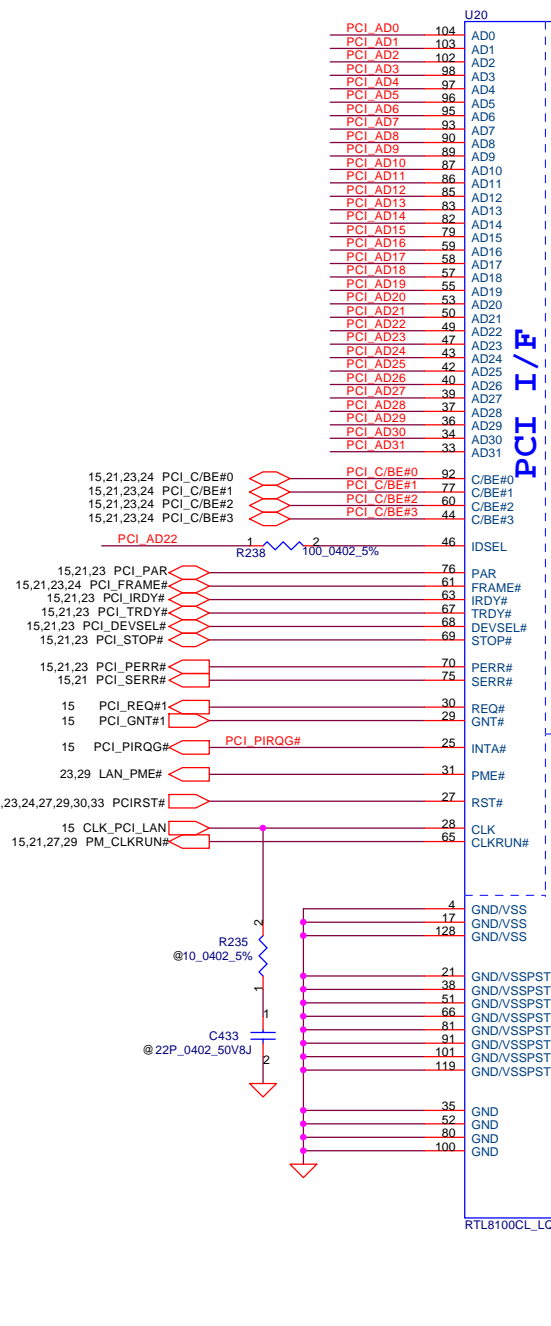


Pop R634 when debug

DEBUG STRAPS

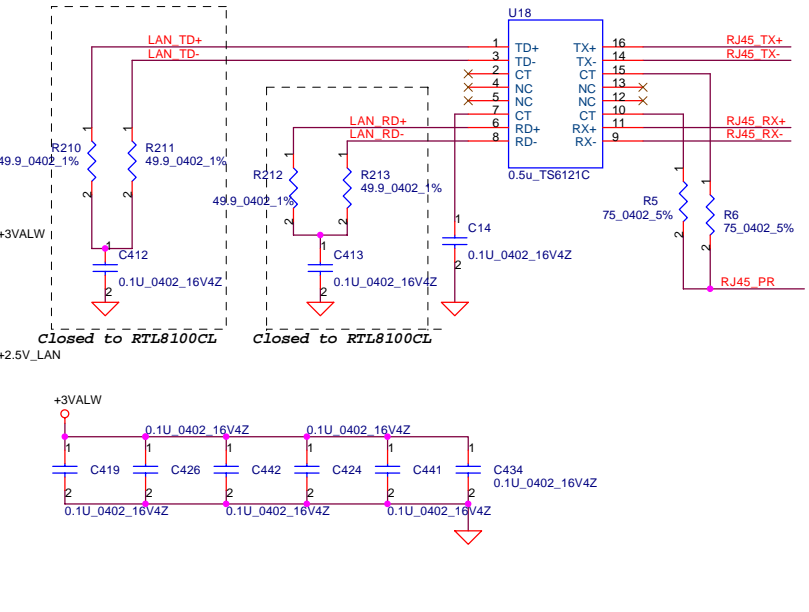
	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

15,19,21,23,24 PCI_AD[0..31] PCI_AD[0..31]

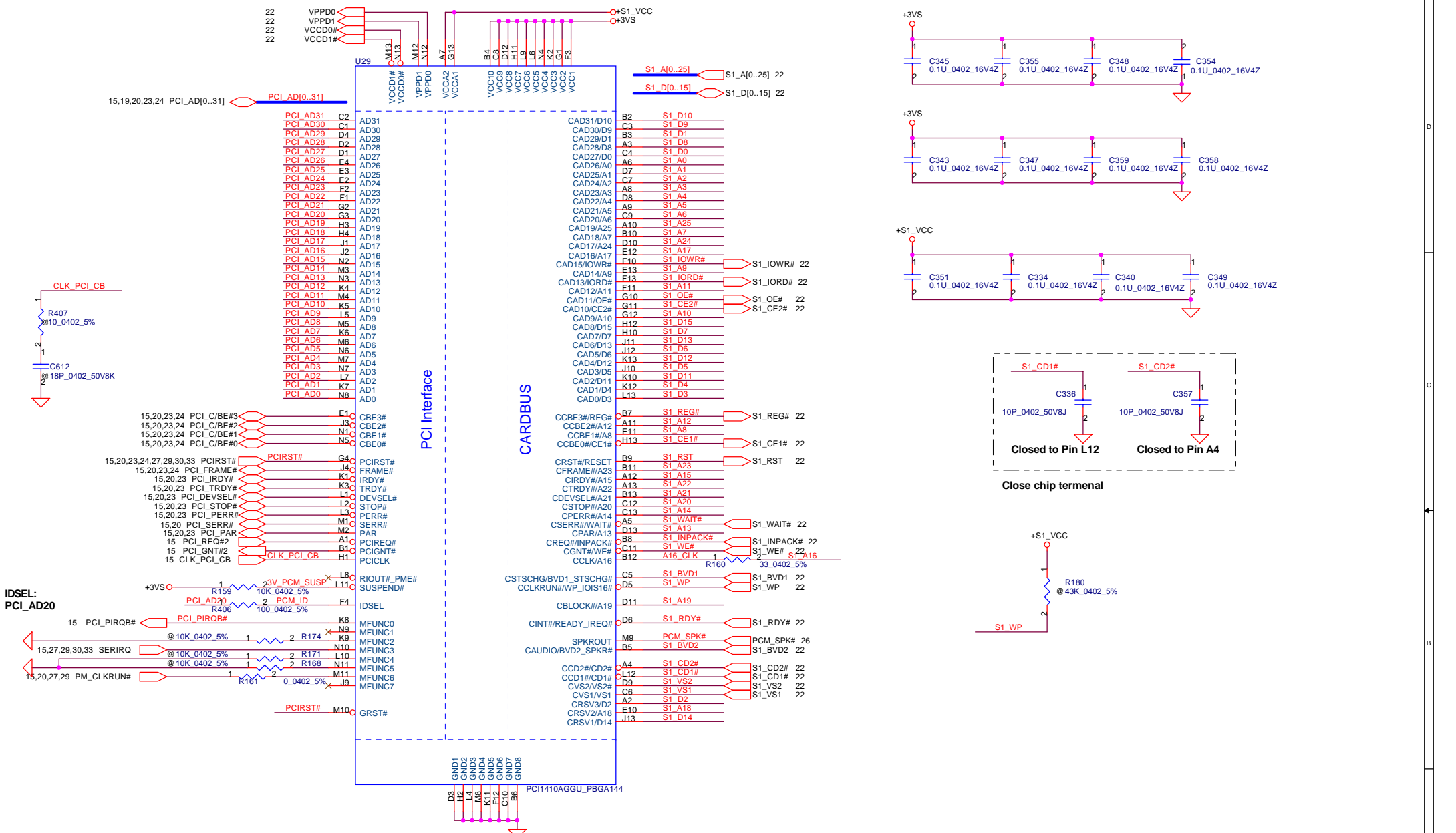


Termination plane should be coupled to chassis ground

Layout Note
TS6121 pls close to conn.

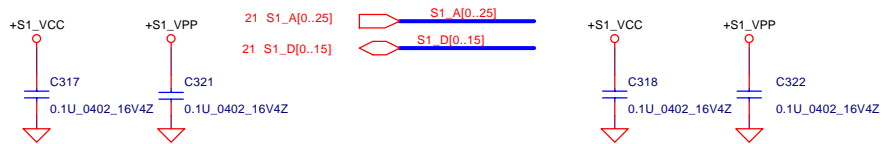
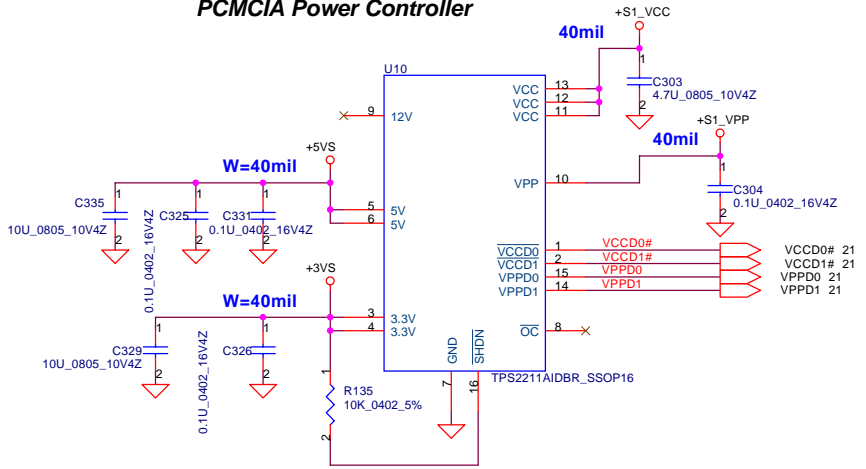


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Date:	Friday, April 21, 2006	Sheet	20	of	46

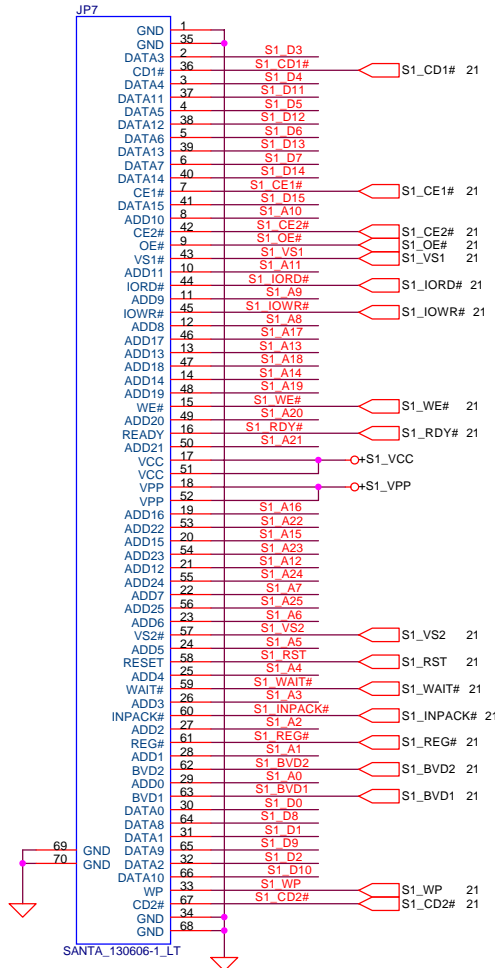


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Date:	Friday, April 21, 2006	Sheet	21	of	46

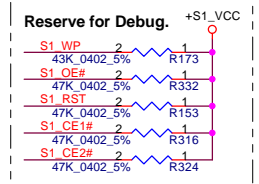
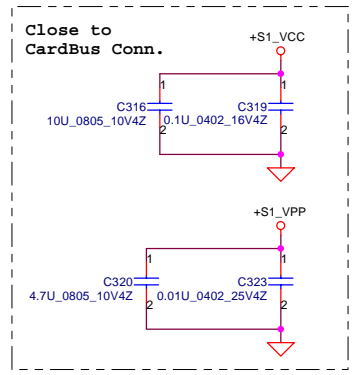
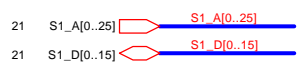
PCMCIA Power Controller



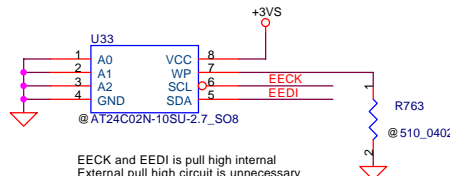
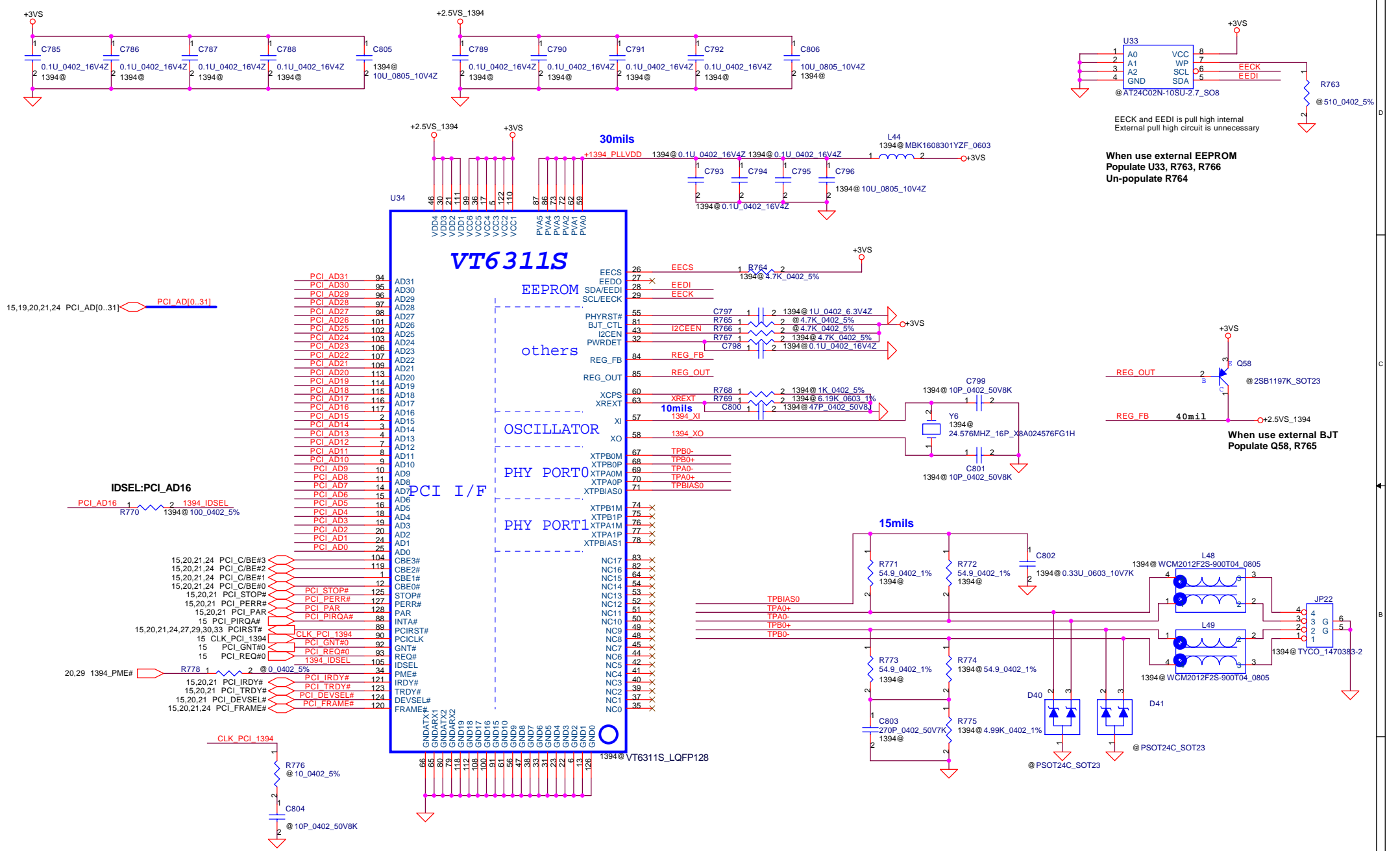
CardBus Socket



CardBus Socket

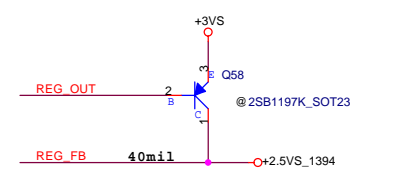


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Size	B	Document Number	HTW2E(LA-3201P)	Rev	1.0
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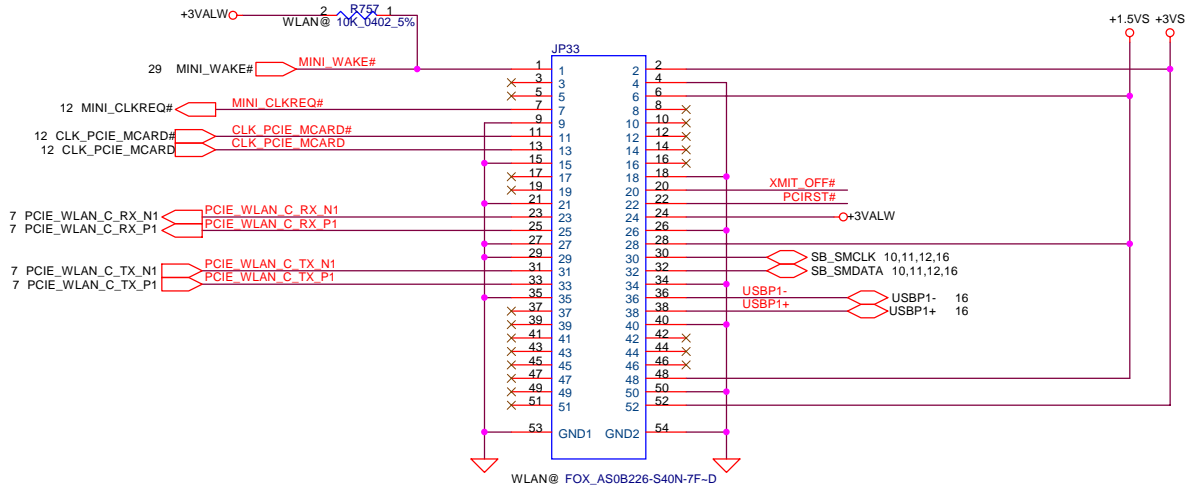
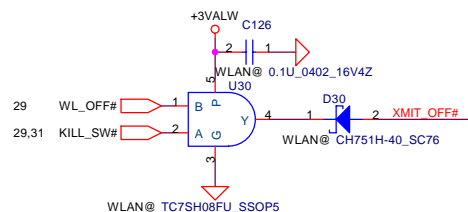
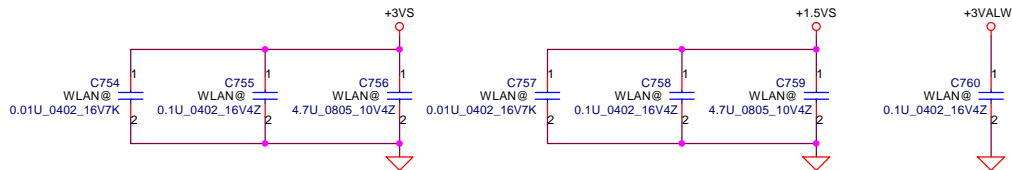
EECK and EEDI is pull high internal
External pull high circuit is unnecessary

When use external EEPROM
Populate U33, R763, R766
Un-populate R764



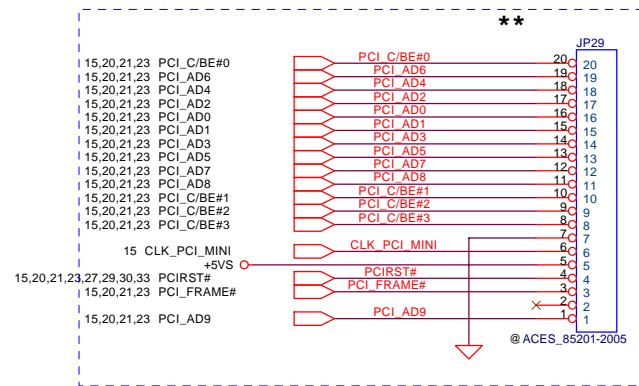
When use external BJT
Populate Q58, R765

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Size B	Document Number HTW2E(LA-3201P)	Date: Friday, April 21, 2006		Sheet 23	of 46



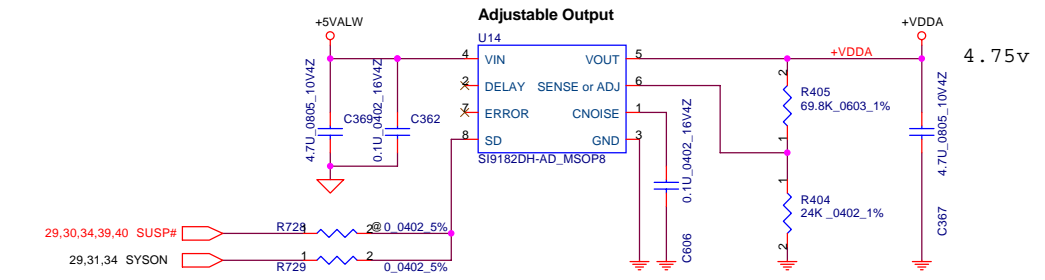
Mini-Express Card

Port 80 Debug Card Connector



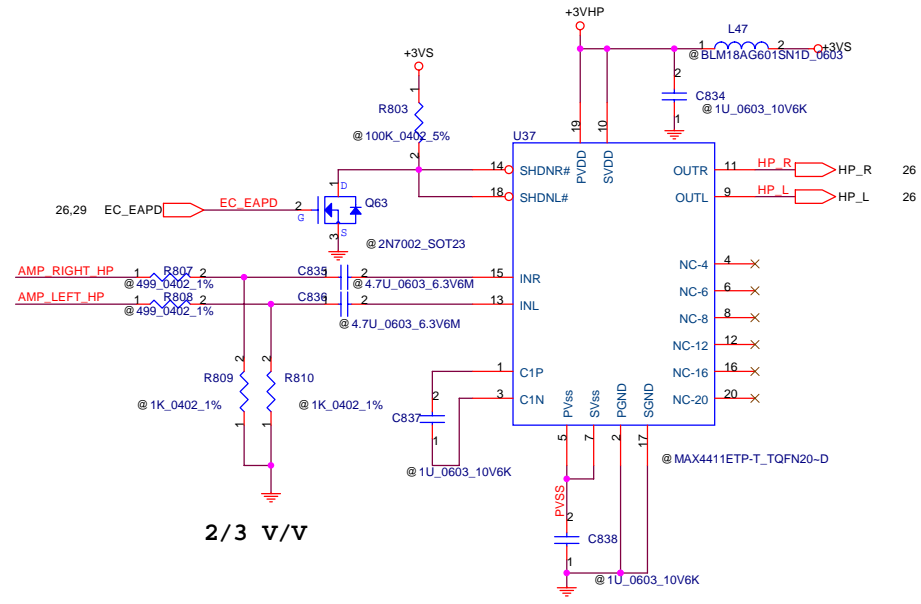
Place under MiniPCI Socket

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Size	B	Document Number	HTW2E(LA-3201P)	Rev
Date:	Friday, April 21, 2006	Sheet	24 of 46	1.0

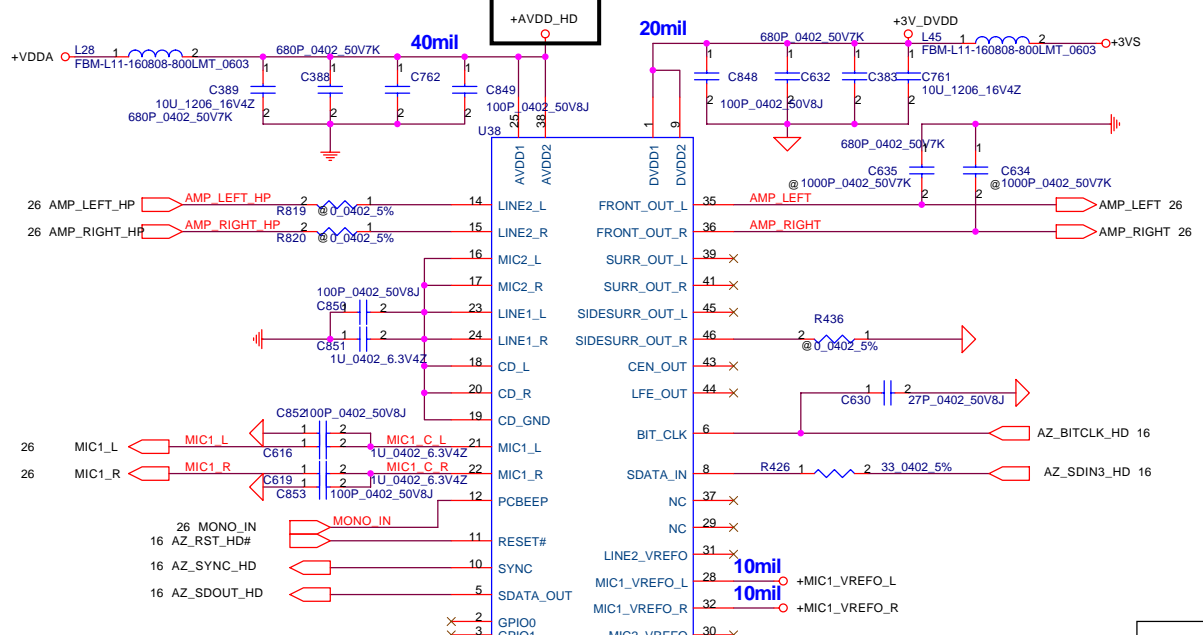


HD Audio Codec

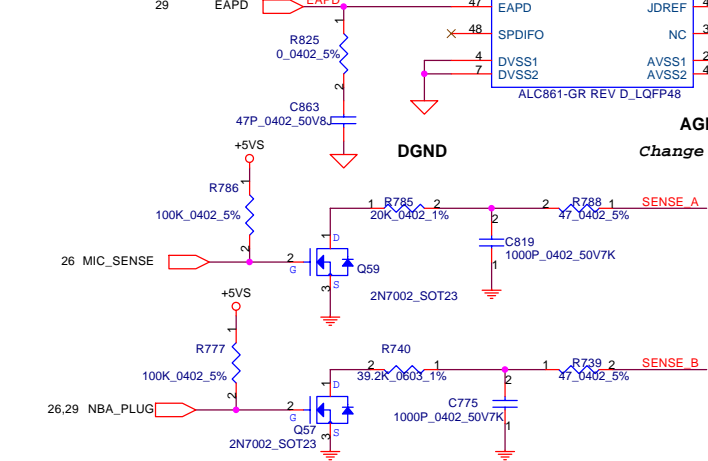
Headphone AMP



2/3 V/V



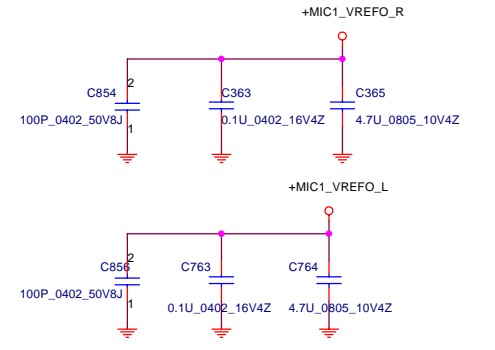
To EC, Reserve for ALC861D



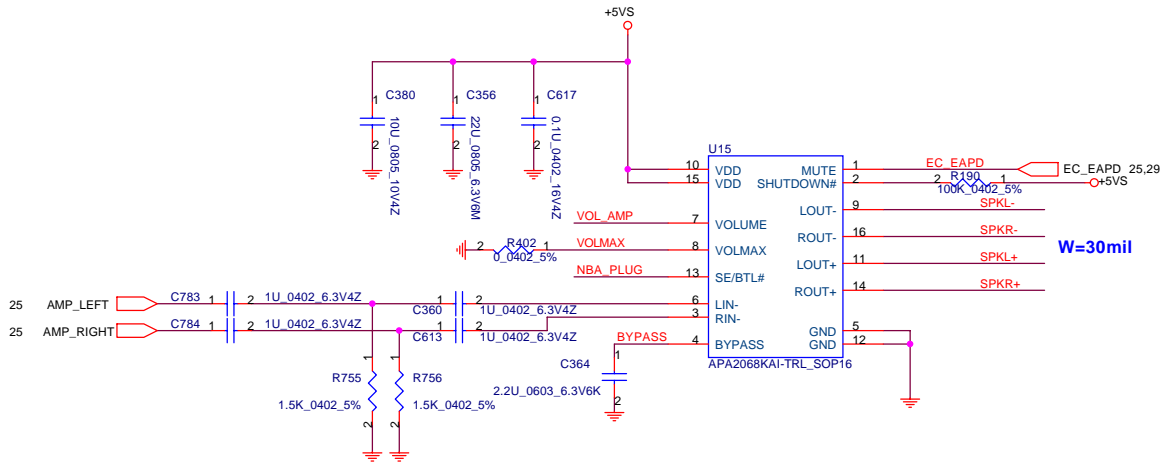
Change R788 to 0_0402_5%
Delete C819
for ALC861 ver. D

Change R739 to 0_0402_5%
Delete C775
for ALC861 ver. D

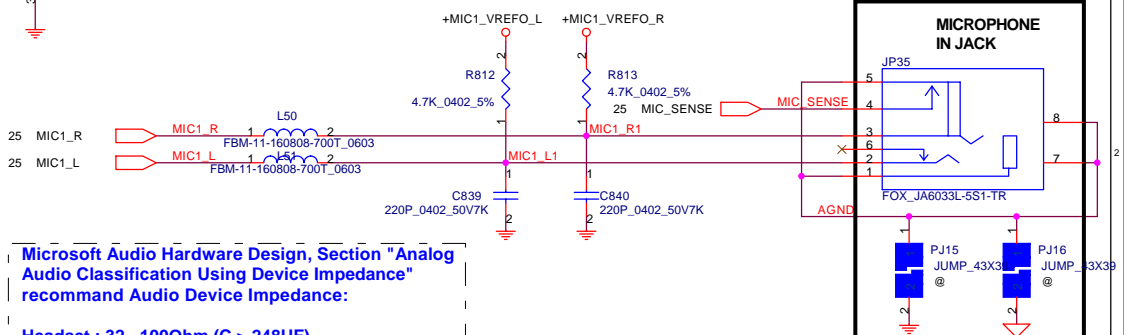
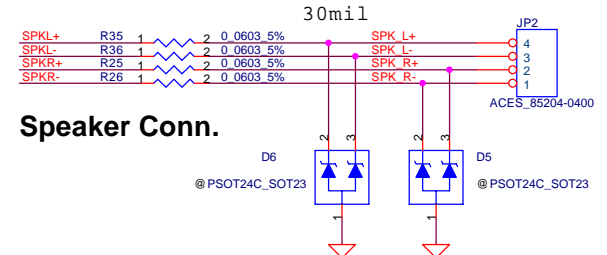
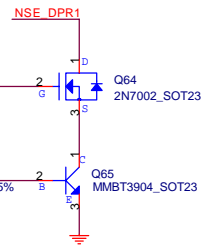
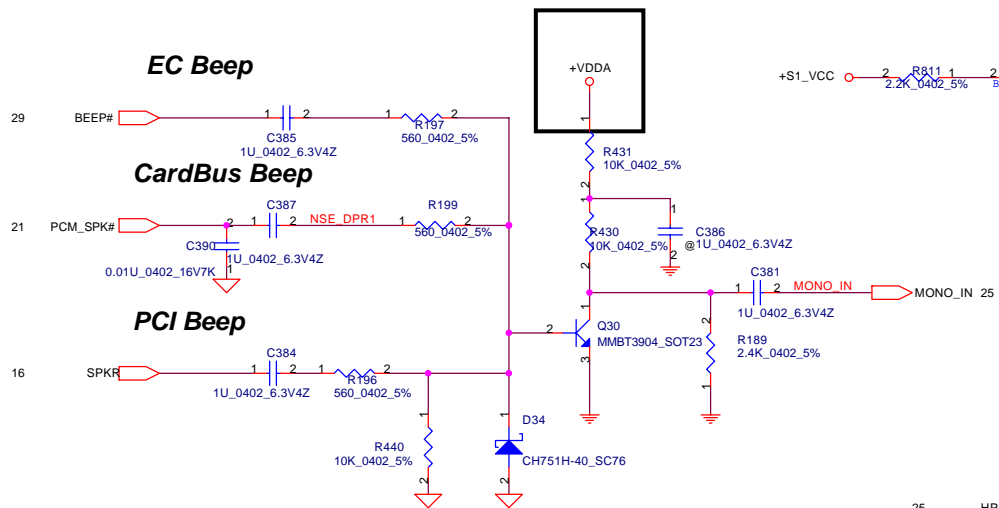
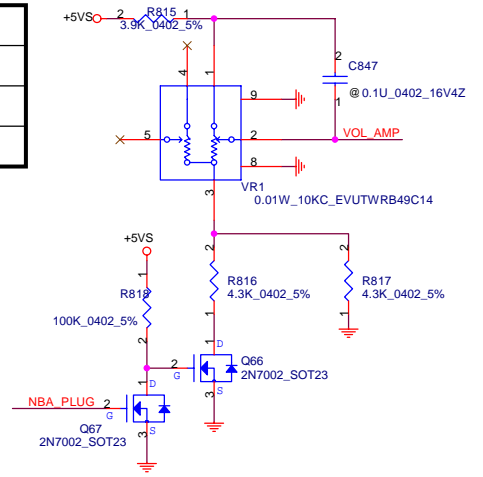
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



DGND To AGND Bypass

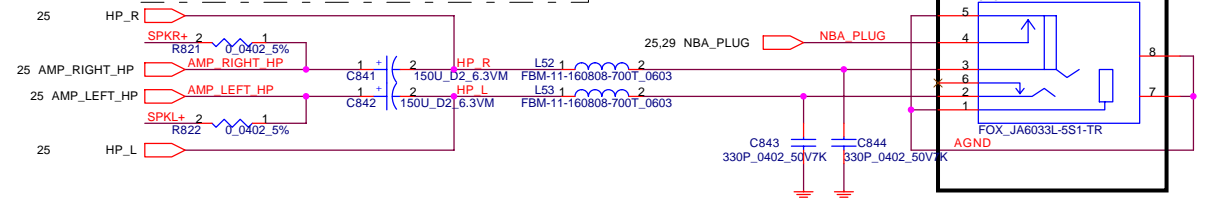


Gain Setting		
	DB	VOL AMP
SPK	10	0.66-3.7
HP	0	1.25-3.9



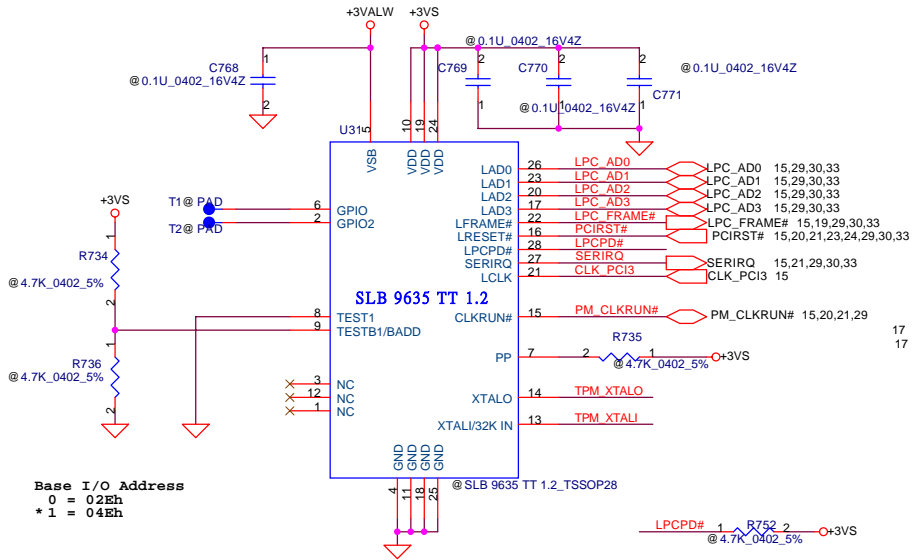
Microsoft Audio Hardware Design, Section "Analog Audio Classification Using Device Impedance" recommend Audio Device Impedance:

Headset : 32 ~100Ohm (C > 248UF)
 Paassive Speakers: 4 ~ 16Ohm (C >1989UF)
 Active Speakers: 3K ~ 15K Ohm (C >2.65UF)

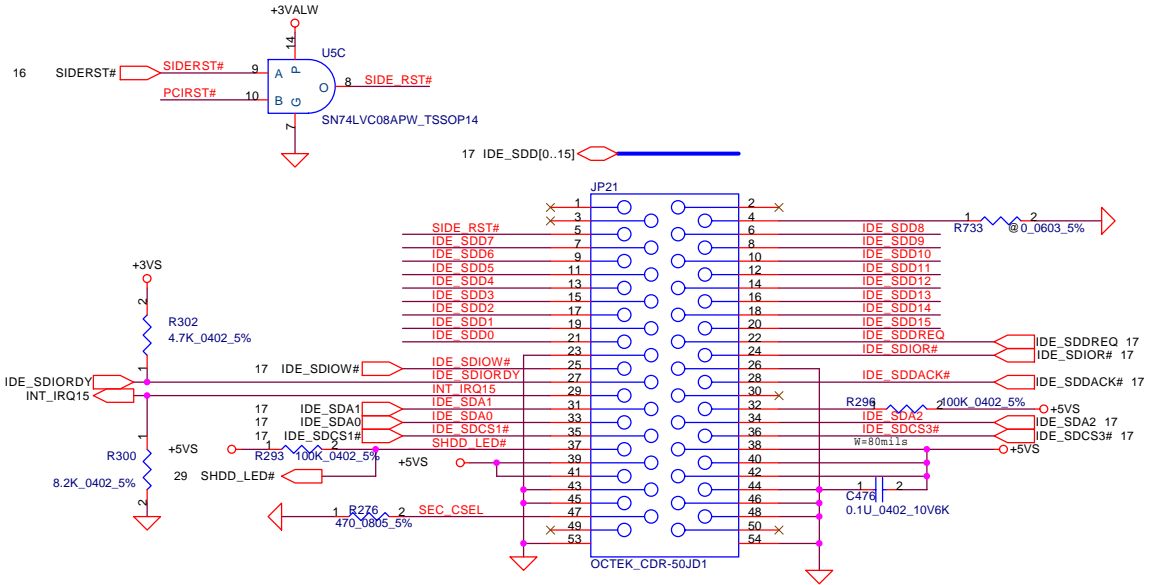
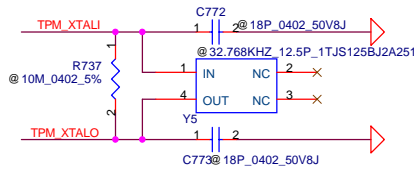


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TPM1.2 on board



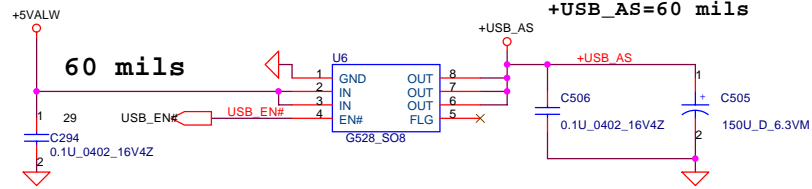
Base I/O Address
 0 = 02Eh
 * 1 = 04Eh



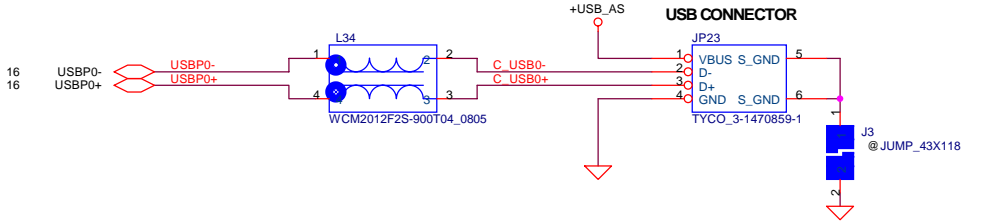
Placea caps. near ODD CONN.

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Size	B	Document Number	HTW2E(LA-3201P)	Rev
Date:	Friday, April 21, 2006	Sheet	27 of 46	1.0

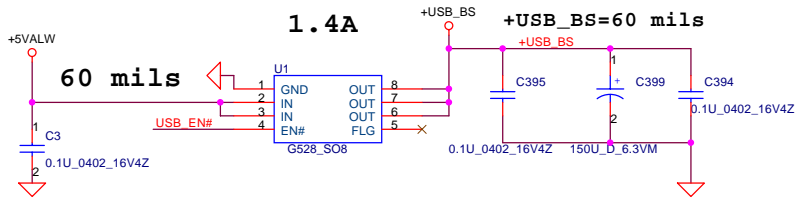
1.4A



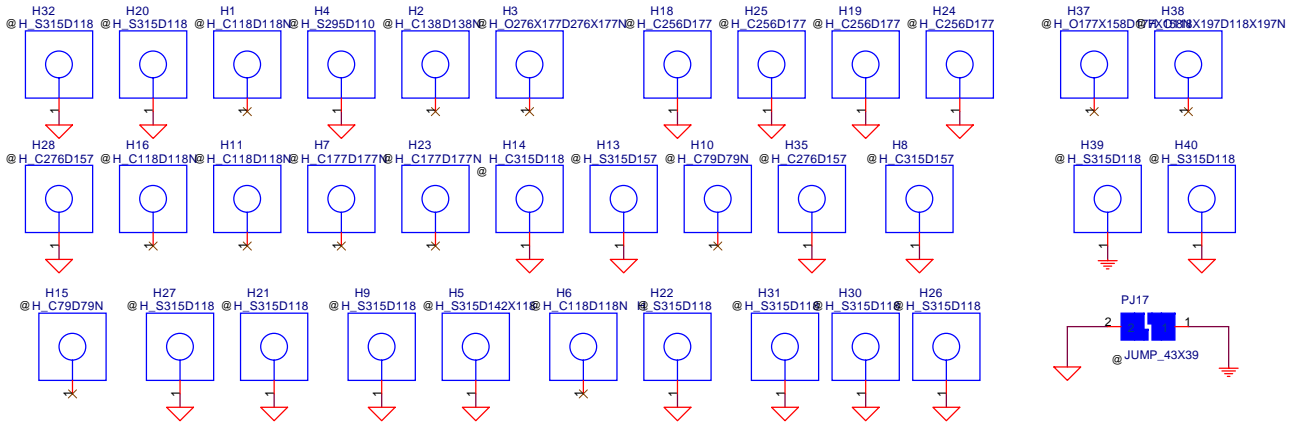
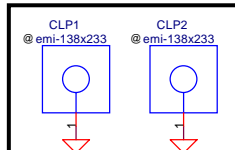
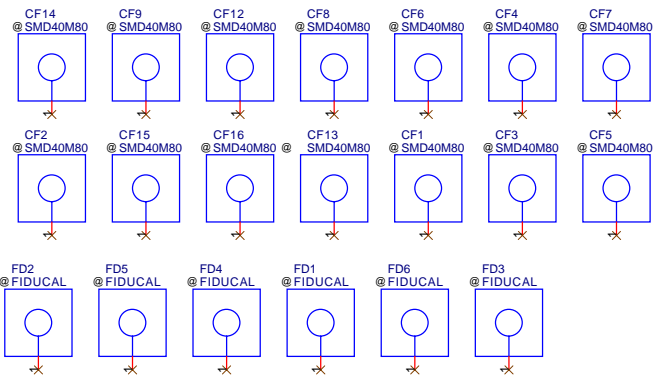
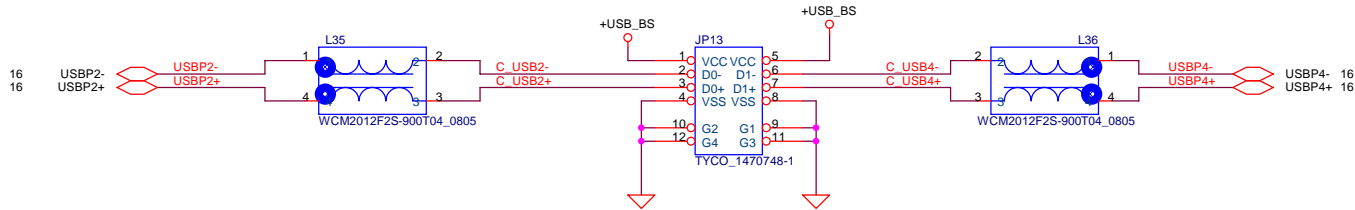
Keep 20 mils minimum spacing between USB signals and others signals



1.4A

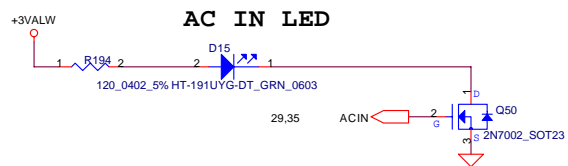
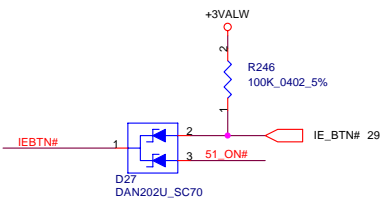
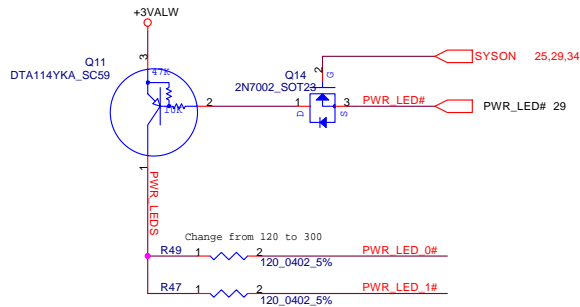
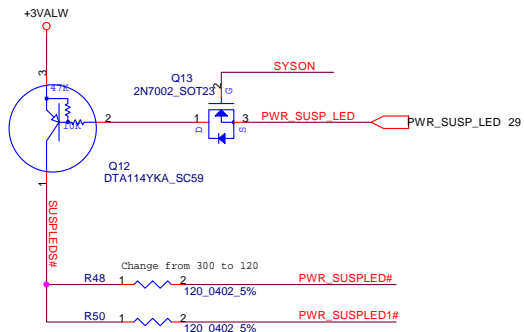
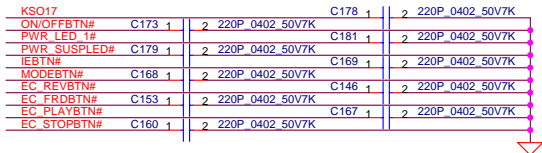
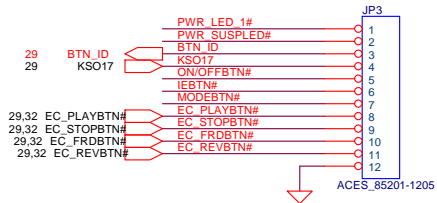


USB CONNECTOR

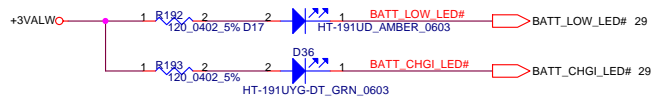


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Size	B	Document Number	HTW2E(LA-3201P)	Rev
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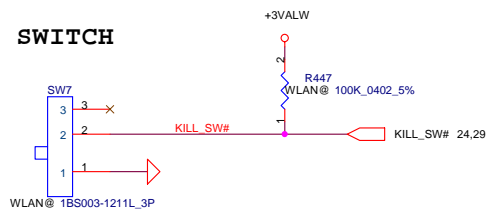
Switch Board Conn.



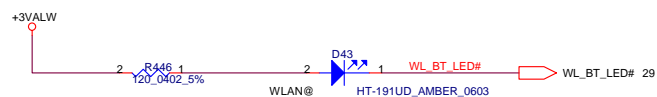
BATTERY CHG



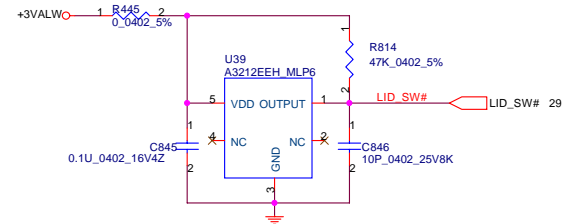
Kill SWITCH



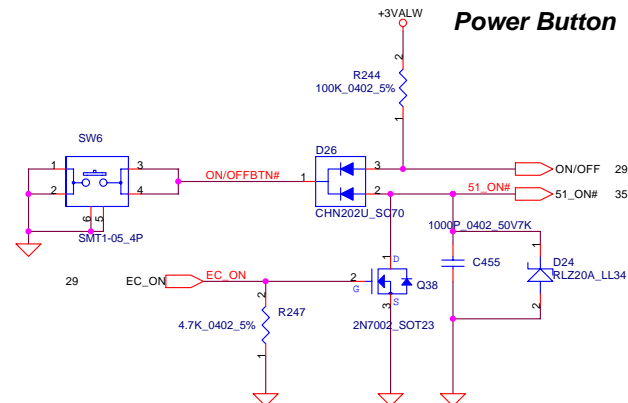
WL&BT LED



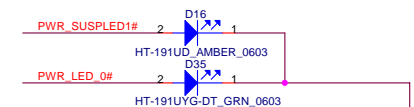
LID Switch



Power Button



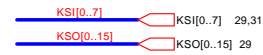
POWER/ON LED



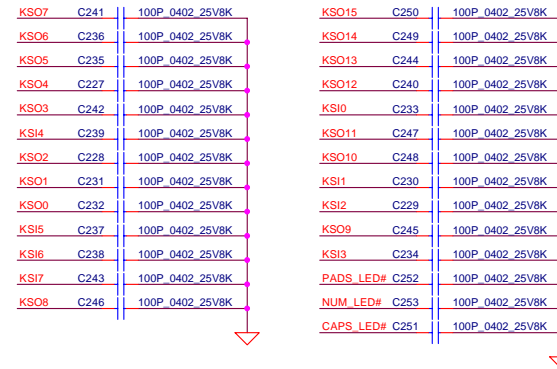
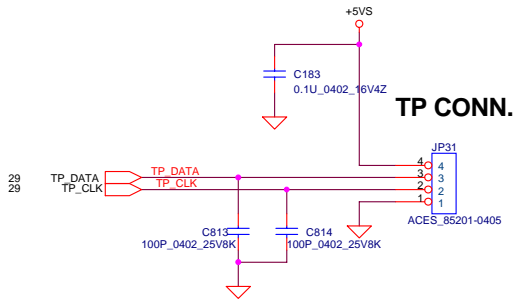
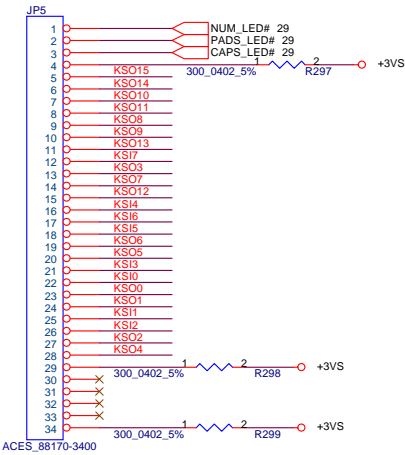
HDD LED



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Date:	Friday, April 21, 2006	Sheet	31	of 46

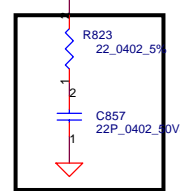
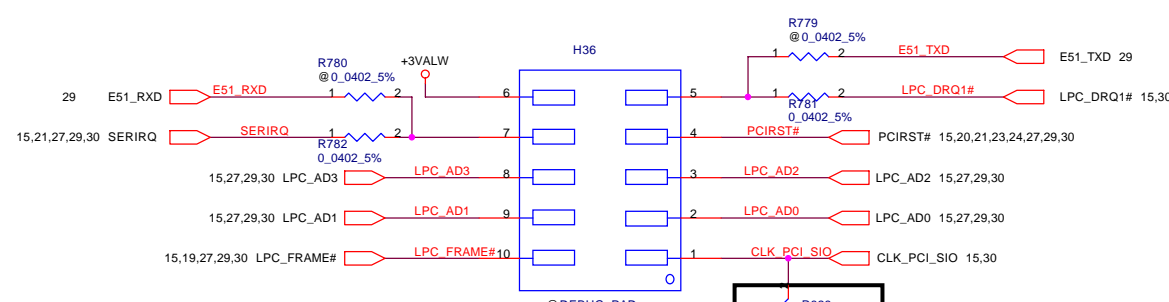
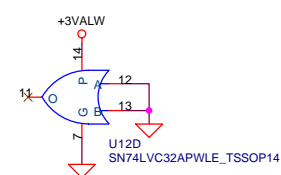
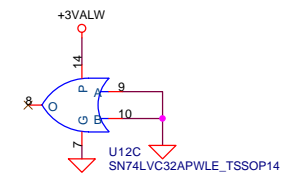
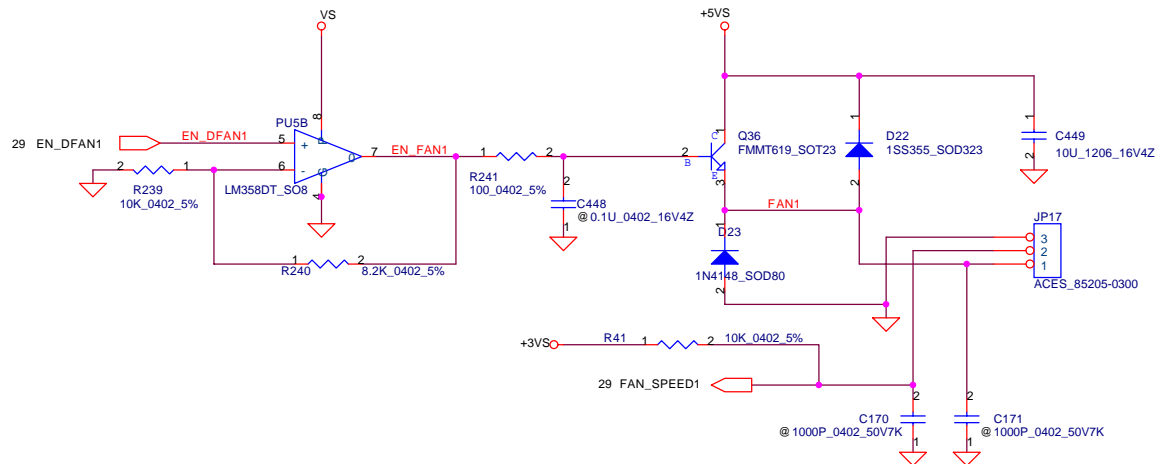


INT_KBD CONN.



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Size	Document Number	Date	Sheet	of	Rev
	Custom#HTWZE(LA-3201P)	Friday, April 21, 2006	1	32	1.0
				46	

FAN Conn



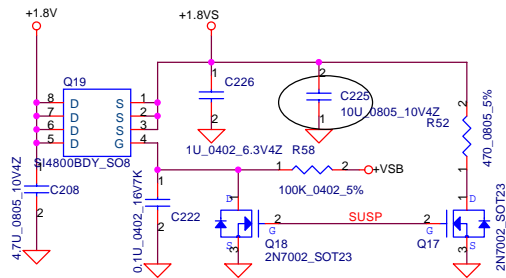
LPC Debug card

BOM

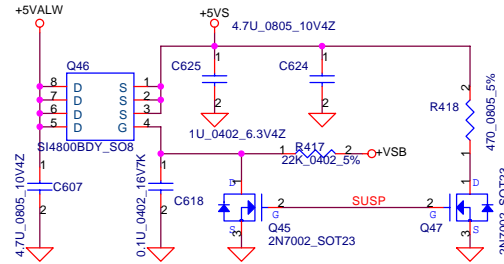


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Size	Document Number			Rev	
B	HTW2E(LA-3201P)			1.0	
Date:	Thursday, April 27, 2006			Sheet	33 of 46

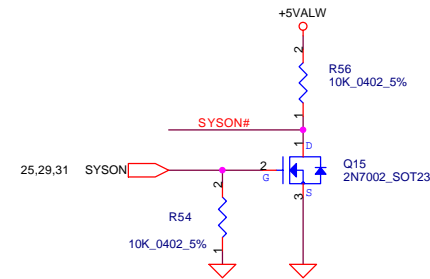
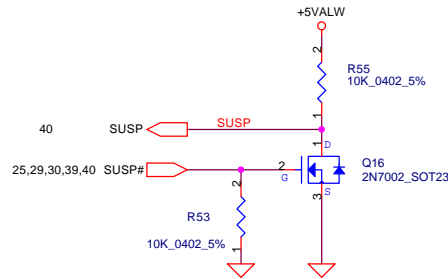
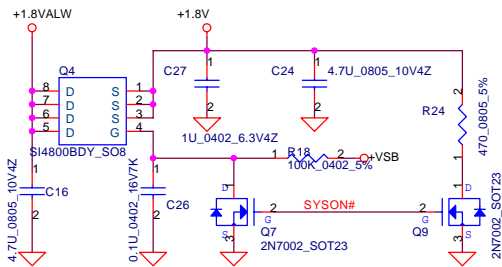
+1.8V TO +1.8VS



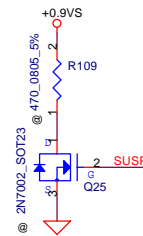
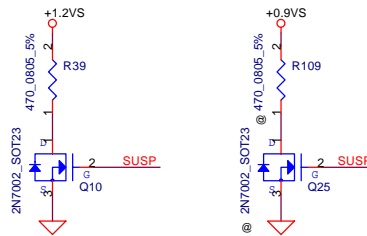
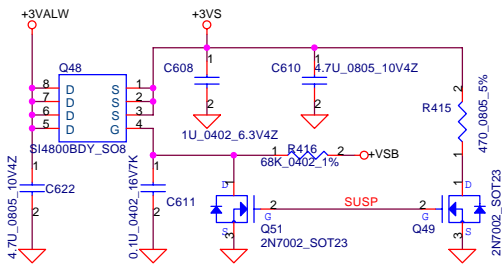
+5VALW TO +5VS



+1.8VALW TO +1.8V

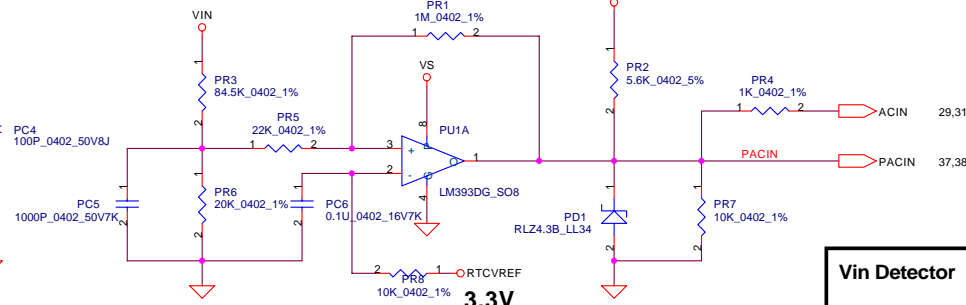
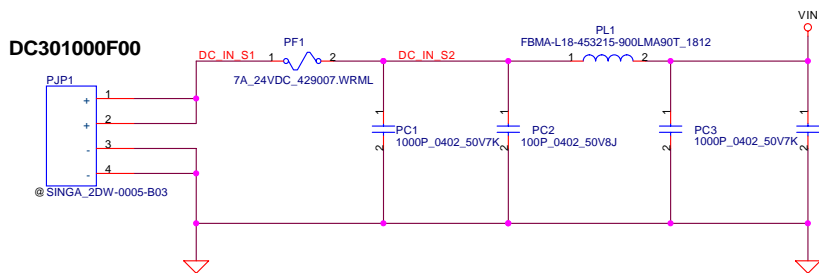


+3VALW TO +3VS

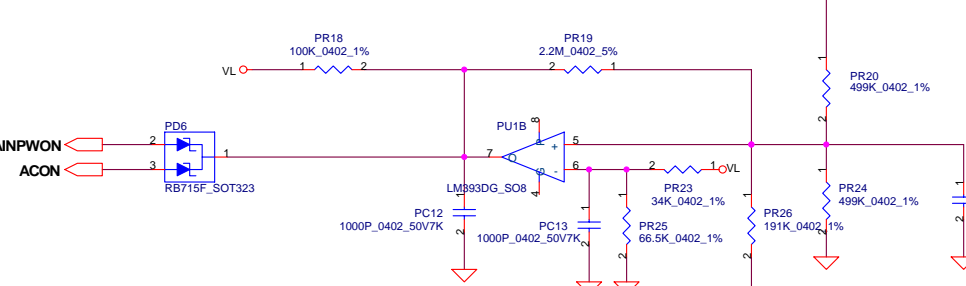
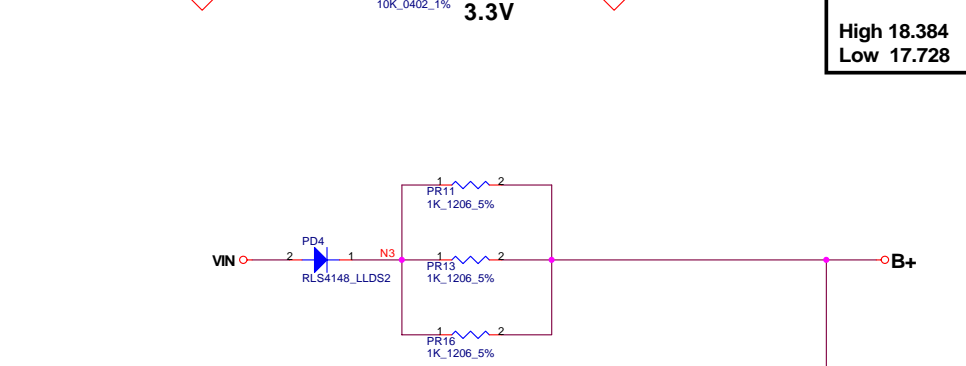
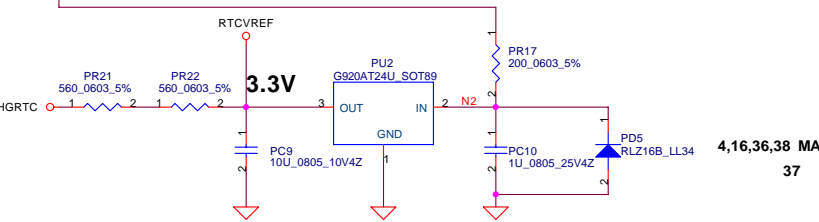
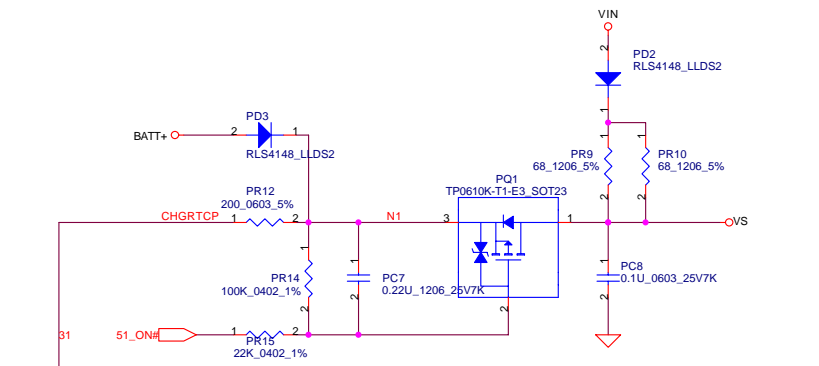


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Size	B	Document Number	HTW2E(LA-3201P)	Rev	1.0
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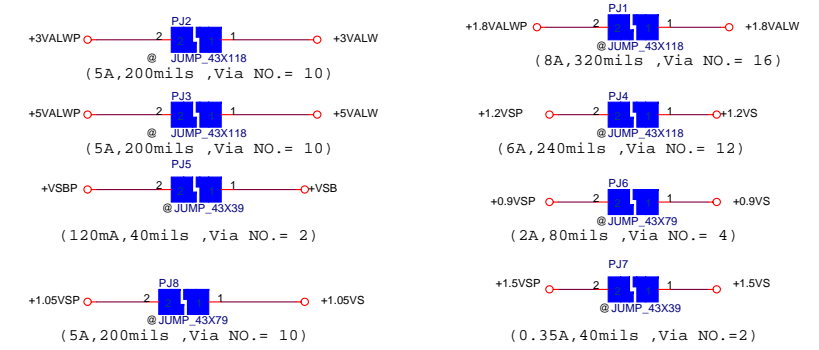
DC301000F00



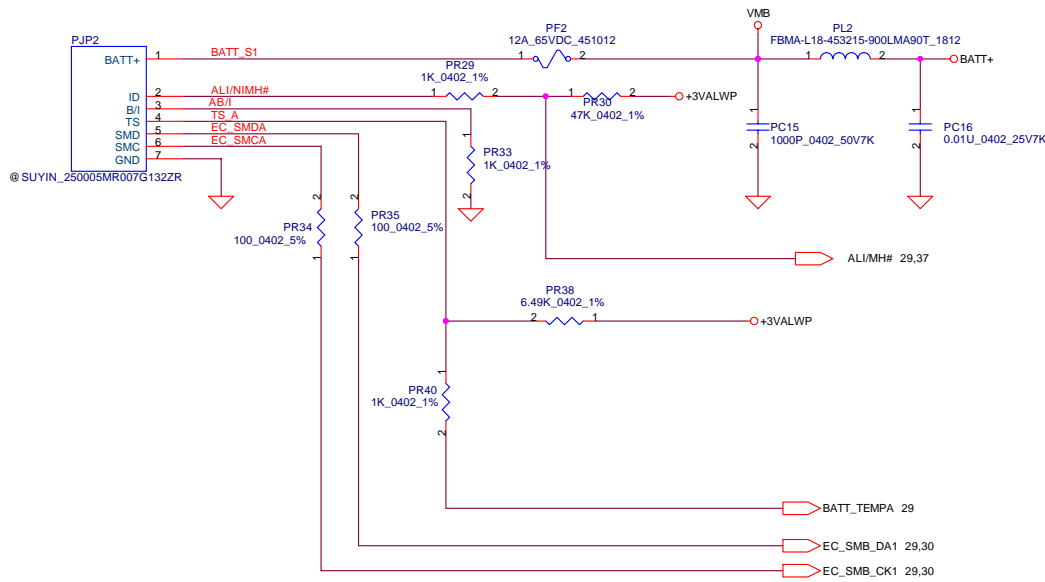
Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



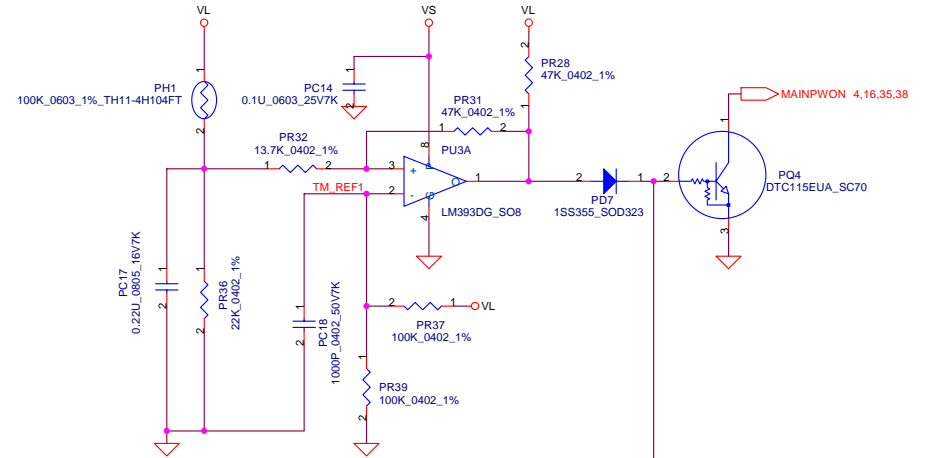
Precharge detector
 15.97V/14.84V FOR
 ADAPTOR



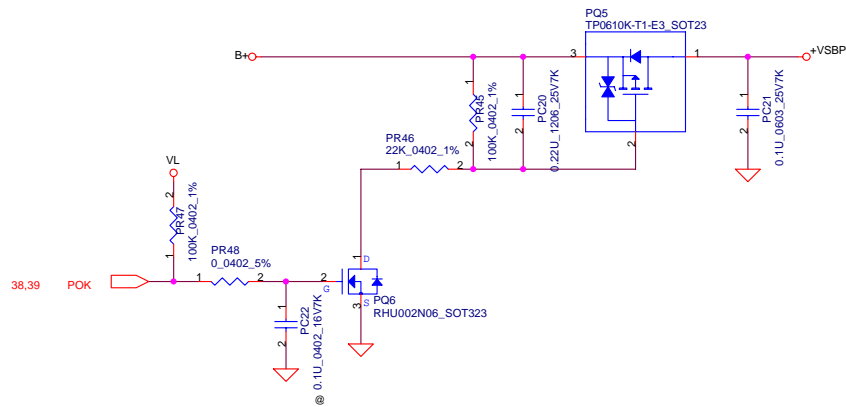
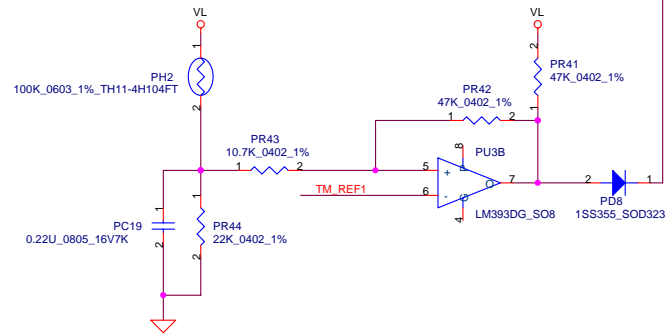
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title
				DCIN & DETECTOR
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Size	Document Number			Rev
				1.0
Date:	Friday, April 21, 2006	Sheet	35	of 46



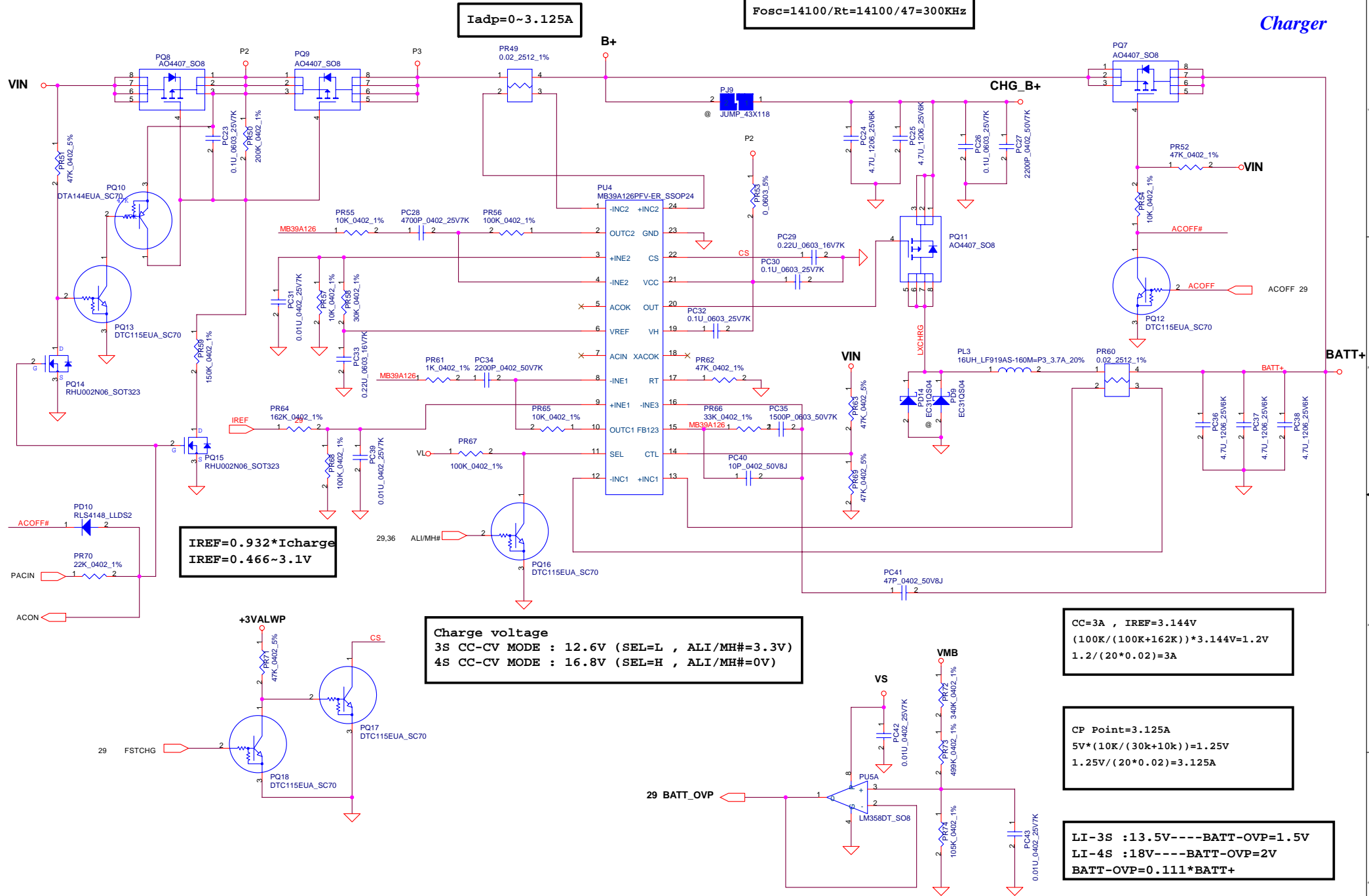
PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



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					1.0



$I_{adp} = 0 \sim 3.125A$

$F_{osc} = 14100 / R_t = 14100 / 47 = 300KHz$

Charger

$I_{REF} = 0.932 * I_{charge}$
 $I_{REF} = 0.466 \sim 3.1V$

Charge voltage
 3S CC-CV MODE : 12.6V (SEL=L , ALI/MH#=3.3V)
 4S CC-CV MODE : 16.8V (SEL=H , ALI/MH#=0V)

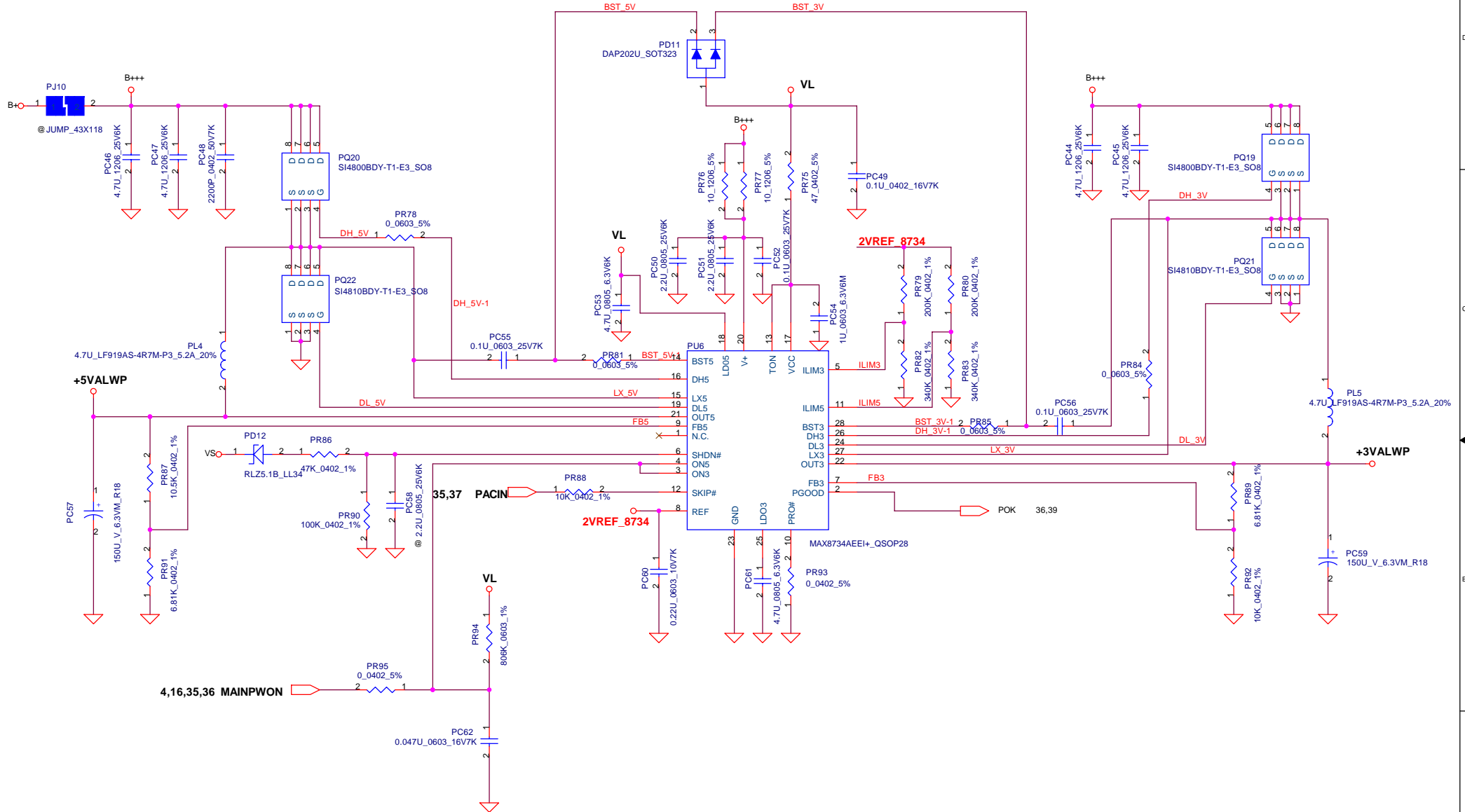
CC=3A , IREF=3.144V
 $(100K / (100K + 162K)) * 3.144V = 1.2V$
 $1.2V / (20 * 0.02) = 3A$

CP Point=3.125A
 $5V * (10K / (30K + 10K)) = 1.25V$
 $1.25V / (20 * 0.02) = 3.125A$

LI-3S : 13.5V --- BATT-OVP=1.5V
 LI-4S : 18V --- BATT-OVP=2V
 $BATT-OVP = 0.111 * BATT+$

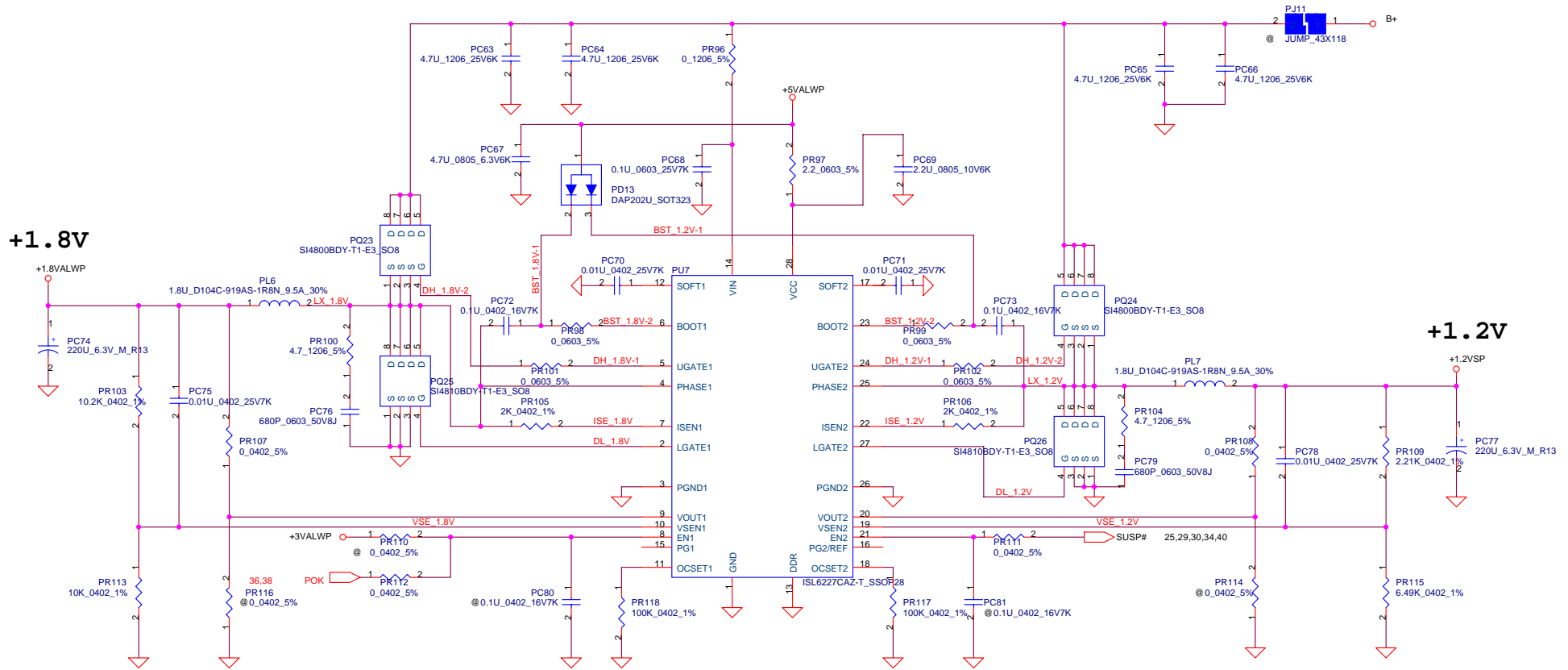
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	CHARGER
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Size	Document Number				Rev
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+3.3VALWP/+5VALWP

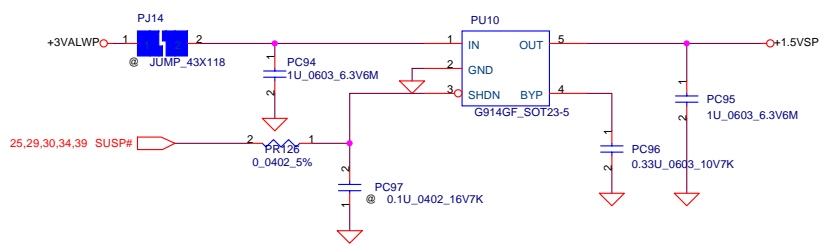
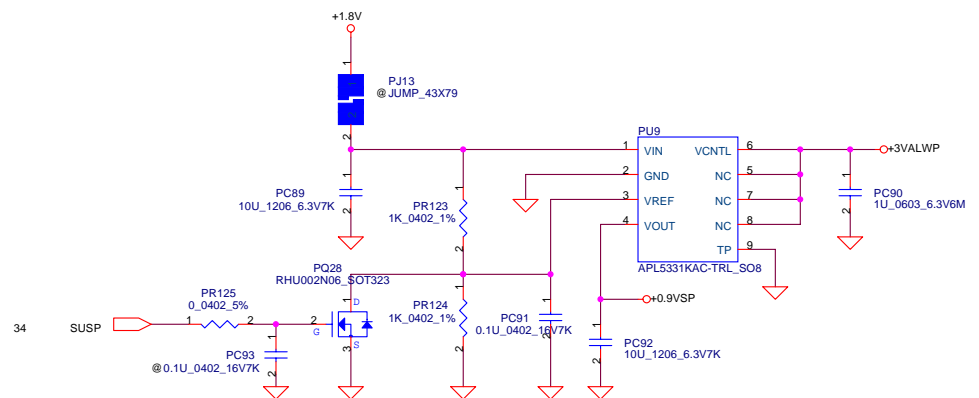
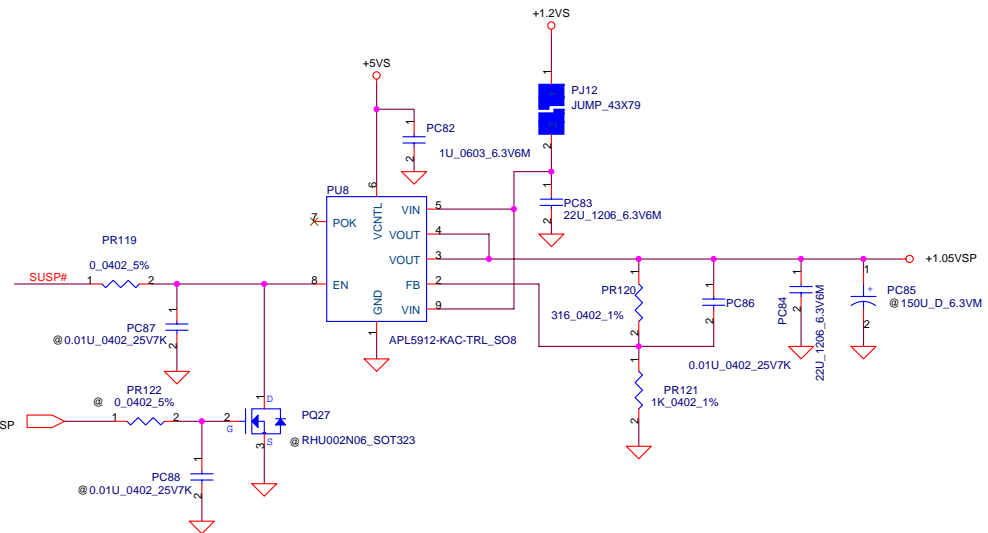


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Date:	Friday, April 21, 2006	Sheet	38	of	46

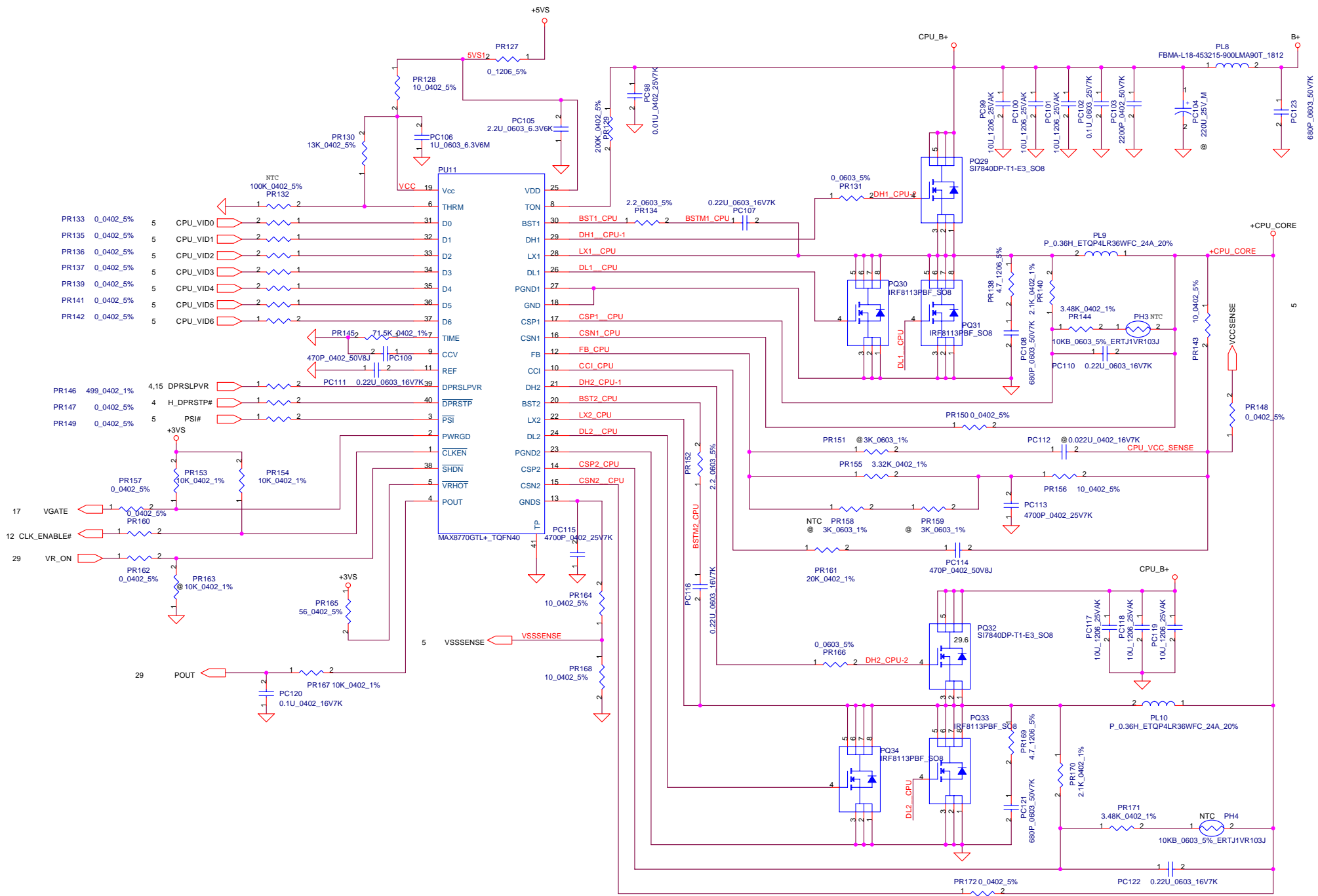
+1.8V



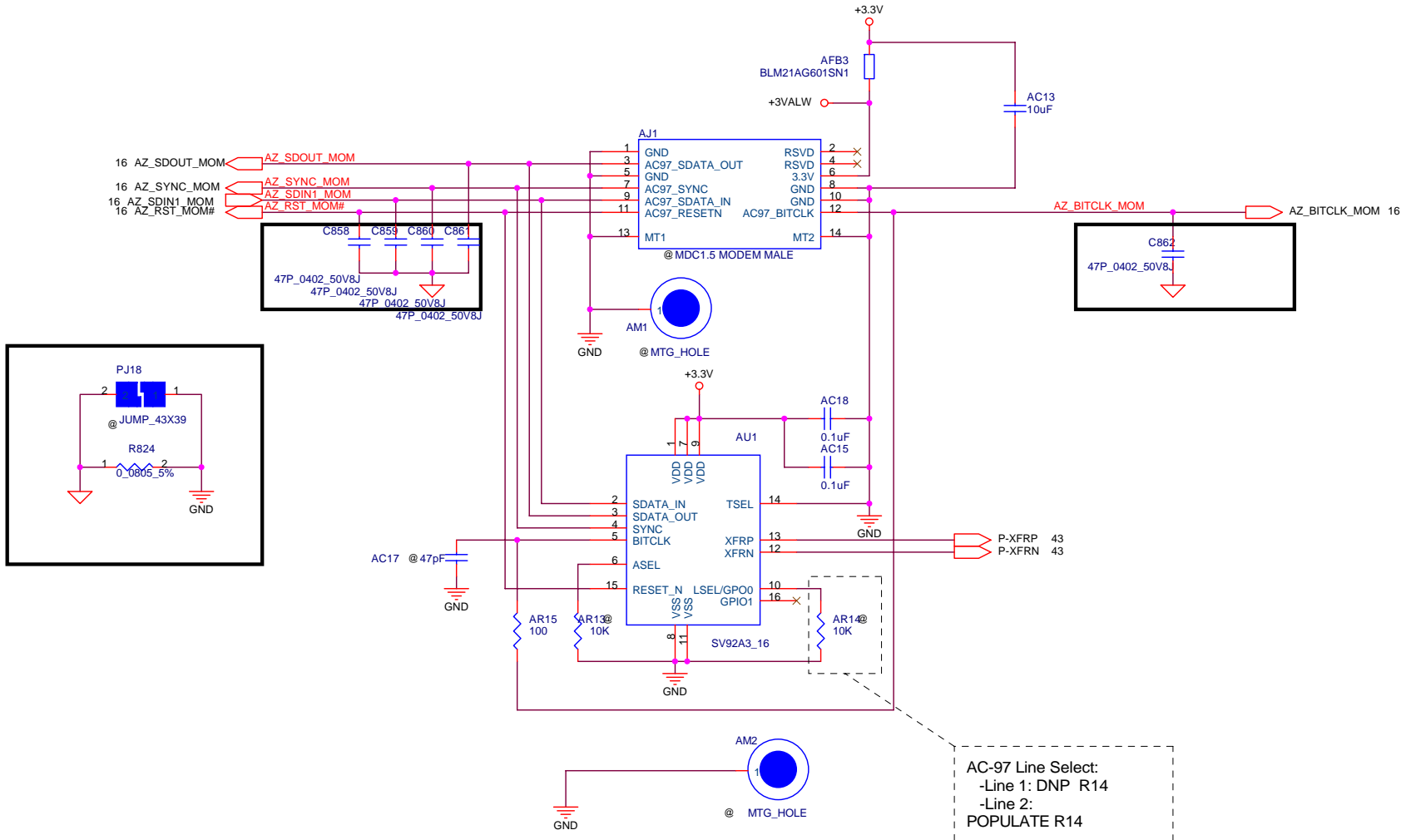
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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	
				1.8V / 1.2V	
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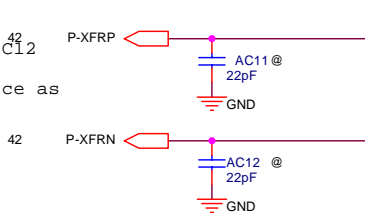


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Date:	Friday, April 21, 2006	Sheet	41	of 46



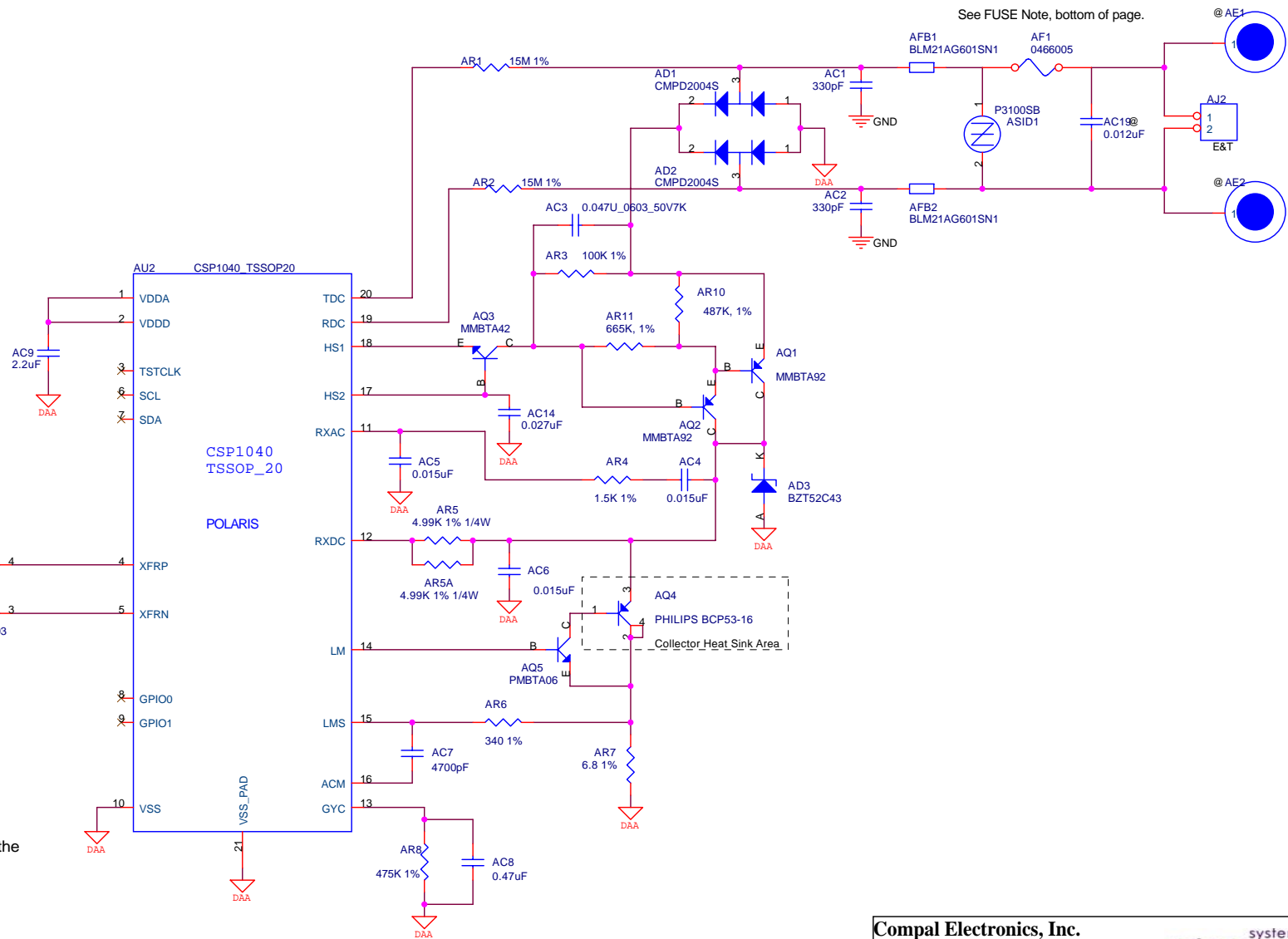
AC-97 Line Select:
 -Line 1: DNP R14
 -Line 2:
 POPULATE R14

Locate C11, C12 as close to digital device as possible.



FUSE Note:
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.



See FUSE Note, bottom of page.

Compal Electronics, Inc.		agere systems
123		
Design Engineer: R. Trevino		
Title		
DELPHI SV92A3 MDC 1.5 Reference Design		
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B	HTW2E(LA-3201P)	1.0
Date:	Friday, April 28, 2006	Sheet 43 of 46

HW4 Product Improvement Record (P.I.R.)

Phase: A to B Date: 2006/01/04 Writer: Timo Teng

Page #	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
12	Modify	R266 R252			For avoid 14M CLK reflection	0.2	
13	Add	C808..C811		220P_0402	For EMI request	0.2	
13	Change	R57 R59	75_0603_1%	75_0402_1%	BOM item reducing	0.2	
14	Change	R1 R2 R3	75_0603_1%	75_0402_1%	BOM item reducing	0.2	
15	Modify	PCICLK Circuit		Mount U32 and relation circuits	For EMI request	0.2	
17	Add	C812		10U_0805	For BOM reducing	0.2	
24	Delete	R754	0_0402_5%		Mount Diode	0.2	
26	Add	R777		100K_0402_5%	Add pull high resistor on NBA_PLUG	0.2	
29	Change		0_0402_5%	8.2K_0402_5%	Change Board ID from 0 to 1	0.2	
30	Delete	R177	0_0402_5%		No using	0.2	
9	Change	C29	22U_1206	22U_0805	BOM Reducing	0.2	
10	Change	C176 C177	22U_1206	22U_0805	BOM Reducing	0.2	
26	Change	C356	22U_1206	22U_0805	BOM Reducing	0.2	
30	Add	C813 C814		220P_0402	For EMI request	0.2	
25	Change	C632 C383	0.1u_0402	680P_0402	For EMI request	0.2	
33	Add	Debug Card Circuit			For Debug	0.2	
16	Modify	GPIO8, 40, 46 pull down		10K_0402	For ATI suggestion.	0.2	
25	Add	R788 R785 Q59 R786 C819			For microphone sense of HD codec	0.2	
26	Add	Gain setting circuit			For adjusting the gain of amplifier by EC	0.2	
31	Add	C820~C830		100P_0402	For EMI debug	0.2	
26	Add	R797 to R801 Q60 Q61			For Gain adjusting	0.2	

Phase: B to C Date: 2006/02/28 Writer: Timo Teng

12	Add	C813		@33P_0402	For ATI PA recommendation	0.3	
12	Add	Q62 U36 R802 C832 C833 D42		2N7002, 7400, 200K 0.1U, 330P, CH751	For ATI PA recommendation	0.3	
26	Change	R800	3.3K_0603	3.3K_0402	Change the size of resistor	0.3	
29	Change	R101	8.2K_0402	18K_0402_5%	Change Board ID for 02 to 03	0.3	
20	Delete	Q31 Q1	DTA114YKA		Meet the retek reference circuit	0.3	
24	Add	R446 R447 D443 SW7			Add Kill switch circuit and W/L LED circuit from sub board.	0.3	
25	Add	U37 relation circuit		MAX4411 and relation circuits	Meet the VISTA standard design	0.3	
26	Add	U15 JP34 JP35 SW8 relation circuits	TPA0232	APA2068 HP and Mic Jack VR relation circuits	Move the audio board circuit to M/B	0.3	

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				Date:	Friday, April 21, 2006
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HW4 Product Improvement Record (P.I.R.)

Phase: C to PreMP Date: 2006/04/18 Writer: Timo Teng

Page #	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
26	ADD	PJ15 PJ16		JUMP	FOR EMI REQUEST	1.0	
33	ADD	R823 C857		0 ohm and 22p	FOR EMI REQUEST	1.0	
28	ADD	CLP1 CLP2		CLIP	FOR EMI REQUEST	1.0	
42	ADD	R824, C858~C862		0 ohm and 47P	FOR EMI REQUEST	1.0	
28	ADD	PJ17		JUMP	FOR EMI REQUEST	1.0	
42	ADD	PJ18		JUMP	FOR EMI REQUEST	1.0	
25	ADD	R825, C863		0 ohm and 22p	FOR EMI REQUEST	1.0	
6	Modify	C713, C715	@330U	330U	FOR ESD Solution	1.0	
16	Modify	R714, R717	33_0402	47_0402	FOR EMI REQUEST		

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POWER PIR LIST

page	Reason for change	Modify list
39	Increase 1.8VALWP to 1.82V for HW requirement	Change PR103 from 10K_0402_1% to 10.2K_0402_1%
41	Add 680P at B+ near CPU core for EMI requirement	Add PC123(680P_0603_50V) at B+ near CPU CORE
38	Adjust 3V/5V OCP to 8A	Change PR79,PR80 to 200K_0402_1%, PR82,PR83 to 340K_0402_1%, PL4,PL5 to 4.7uH
41	Adjust CPU CORE loadline	Change PR155 to 3.32K_0402_1%, PR156,PR164=10_0402_5%, PC115=4700P_0402_25V,PR148=0_0402_5%, Unpop PR151,PC112

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