Compal Confidential

Schematic Document

Crestline + ICH8

2007 / 11 / 14 Rev:0.2

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

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Title: ***Cover Sheet***

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Custom	***LA-4231P***	0.1

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Compal confidential

File Name : LA-4231P

SMB 13.3

ZZZ1

PCB

Thermal Sensor ADM1032ARMZ P.4

Fan conn P.4

Mobile Merom uFCPGA-478 CPU P.4,5,6

H_A#(3..35)
H_D#(0..63)

FSB 667/800MHz 1.05V

CK505 TSSOP-64
Clock Generator ICS 9LPRS365 P.16

CRT P.15

LVDS Panel Interface P.15

nVidia NB8M-GS P.34,35,36,37

VRAM x 2 P.38

Intel Crestline MCH FCBGA 1299 P.7,8,9,10,11,12

DDR2 667MHz 1.8V

Dual Channel

DDR2-SO-DIMM X2 BANK 0, 1, 2, 3 P.13,14

CardBus Controller O2MICRO OZ129 P.40

PCI

DMI X4

C-Link

1394

Media Card

Intel ICH8 mBGA-676 P.17,18,19,20

USB2.0

Azalia

SATA Master

SATA Slave

PCI-E BUS

USB conn x 4 P.32

FingerPrinter P.32

Felica Conn P.32

BT Conn P.32

Camera P.32

Mic

Express Card P.28

Mini-Card-2 P.24

10/100/1000 LAN REALTEK RTL8111C-GR P.22

RJ45/11 CONN

Mini-Card-1 (WLAN) P.24

Mini-Card-2 P.24

Express Card P.28

LPC BUS

ENE KB926 P.29

Touch Pad CONN. P.31

Int.KBD P.31

BIOS(System/EC) P.29

Audio CKT ALC268 P.25

AMP & Audio Jack P.26

SATA HDD Connector P.21

CDROM Conn. P.21

TPM CONN P.29

Power On/Off CKT.

DC/DC Interface CKT.

RTC CKT. P.18

Power Circuit DC/DC

Power OK CKT.

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Title: Block diagram

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Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	+B	+5VALW +3VALW	+3V +1.8V	+5VS +3VS +1.8VS +1.5VS +1.25VS +CPU_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	O
S5 S4/AC	O	O	X	X	O
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b?
EEPROM(24C16/02)	1010 000X b?
(24C04)	1011 000Xb?

EC SM Bus2 address

Device	Address
ADM1032	4D

ICH7 SM Bus address

Device	Address
Clock Generator (ICS ICS9LPR310)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

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Title: Notes

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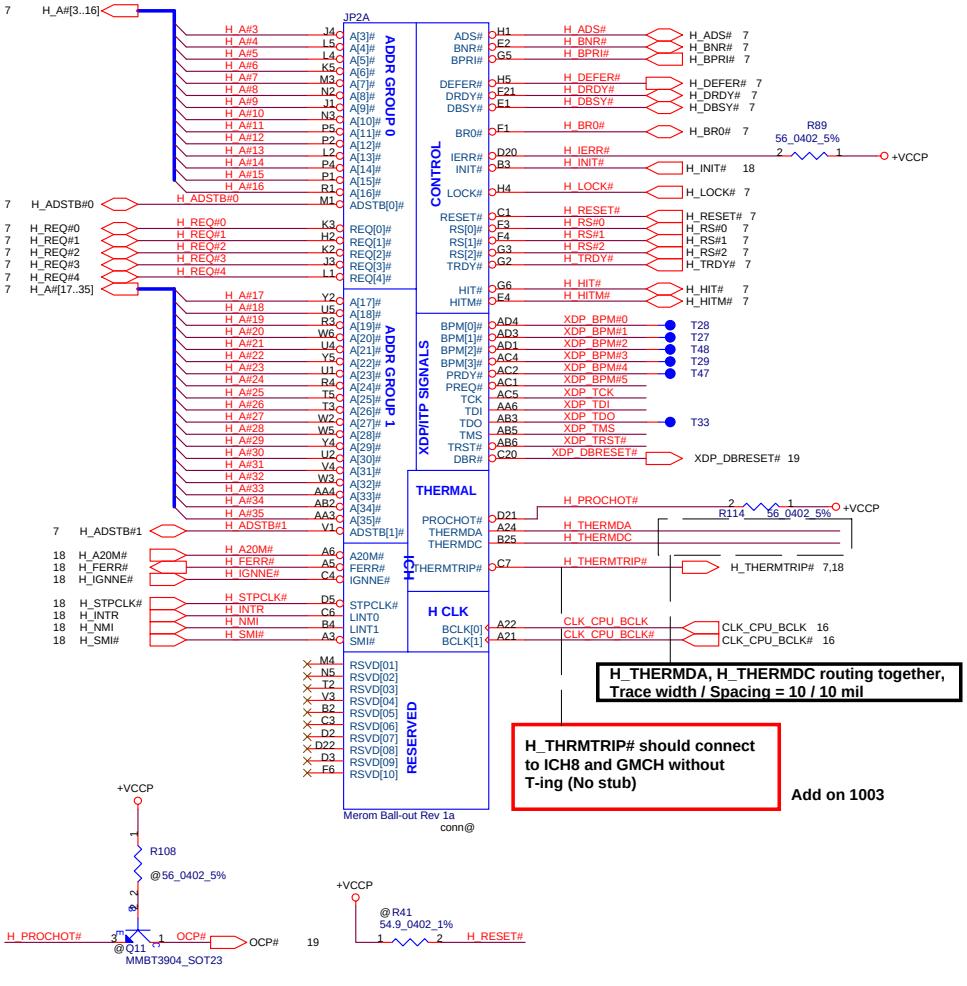
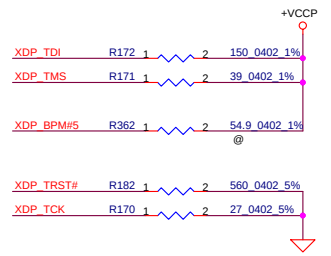


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

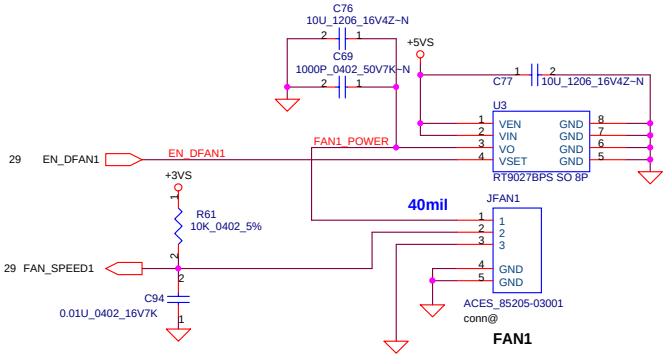
H_THRMTRIP# should connect to ICH8 and GMCH without T-ing (No stub)

Add on 1003

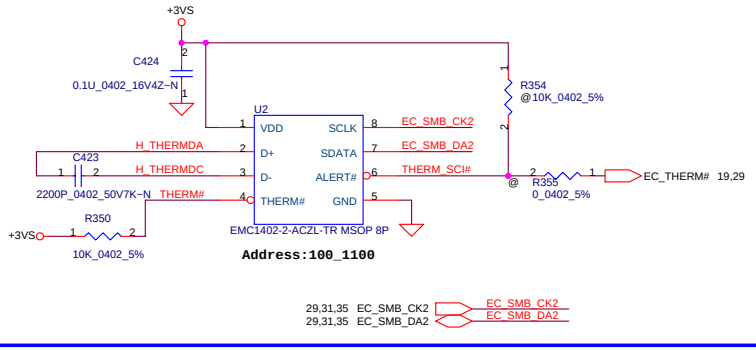
XDP Reserve



FAN1 Control and Tachometer



Thermal Sensor EMC1402-1-ACZL-TR



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Title: **Merom(1/3)-AGTL+/XDP**

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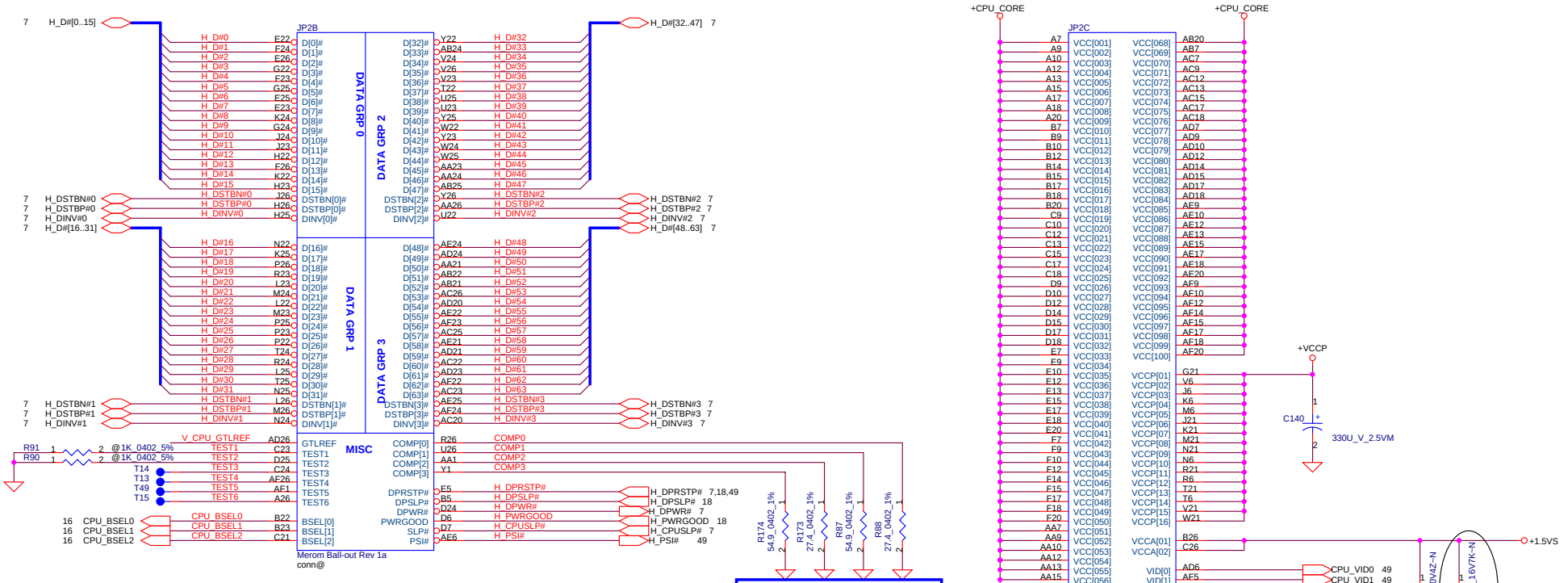
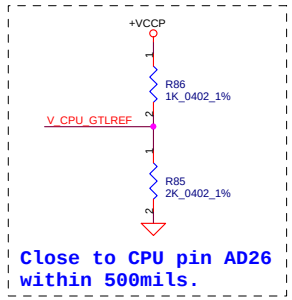


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

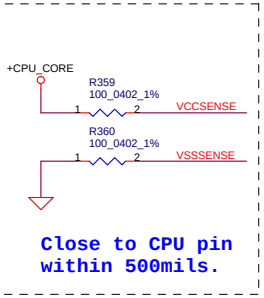
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: Merom(2/3)-AGTL+/PWR

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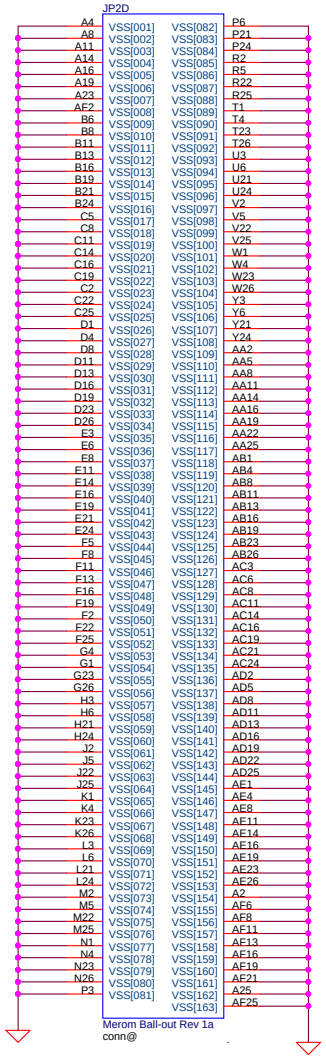
High Frequence Decoupling

10uF 0805 X5R -> 85 degree.



Place these caps inside the CPU socket cavity.
(Left side on Top).

+CPU_CORE

C1150 10U_0805_6.3V6M
C1151 10U_0805_6.3V6M
C1152 10U_0805_6.3V6M
C1153 10U_0805_6.3V6M
C1154 10U_0805_6.3V6M
C1155 10U_0805_6.3V6M
C1156 10U_0805_6.3V6M

Place these caps inside the CPU socket.
(Left side on Top).

C1157 10U_0805_6.3V6M
C1158 10U_0805_6.3V6M
C1159 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Right side on Top side).

+CPU_CORE

C1160 10U_0805_6.3V6M
C1161 10U_0805_6.3V6M
C1162 10U_0805_6.3V6M
C1163 10U_0805_6.3V6M
C1164 10U_0805_6.3V6M
C1165 10U_0805_6.3V6M
C1166 10U_0805_6.3V6M

Place these caps inside the CPU socket.
(Right side on Top).

C1167 10U_0805_6.3V6M
C1168 10U_0805_6.3V6M
C1169 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Left side on Bottom).

+CPU_CORE

C1170 10U_0805_6.3V6M
C1171 10U_0805_6.3V6M
C1172 10U_0805_6.3V6M
C1173 10U_0805_6.3V6M
C1174 10U_0805_6.3V6M
C1175 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Right side on Bottom).

+CPU_CORE

C1176 10U_0805_6.3V6M
C1177 10U_0805_6.3V6M
C1178 10U_0805_6.3V6M
C1179 10U_0805_6.3V6M
C1180 10U_0805_6.3V6M
C1181 10U_0805_6.3V6M

Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

+CPU_CORE

C190 330U_V_2.5VM
C429 330U_V_2.5VM
@
C207 330U_V_2.5VM
C426 330U_V_2.5VM

Place these inside socket cavity on L8 (North side Secondary)

+VCCP

C212 220U_D2_4VY_R15M
C210 0.1U_0402_10V6K
C209 0.1U_0402_10V6K
C208 0.1U_0402_10V6K
C185 0.1U_0402_10V6K
C183 0.1U_0402_10V6K
C184 0.1U_0402_10V6K

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Title: **Merom(3/3)-GND&Bypass**

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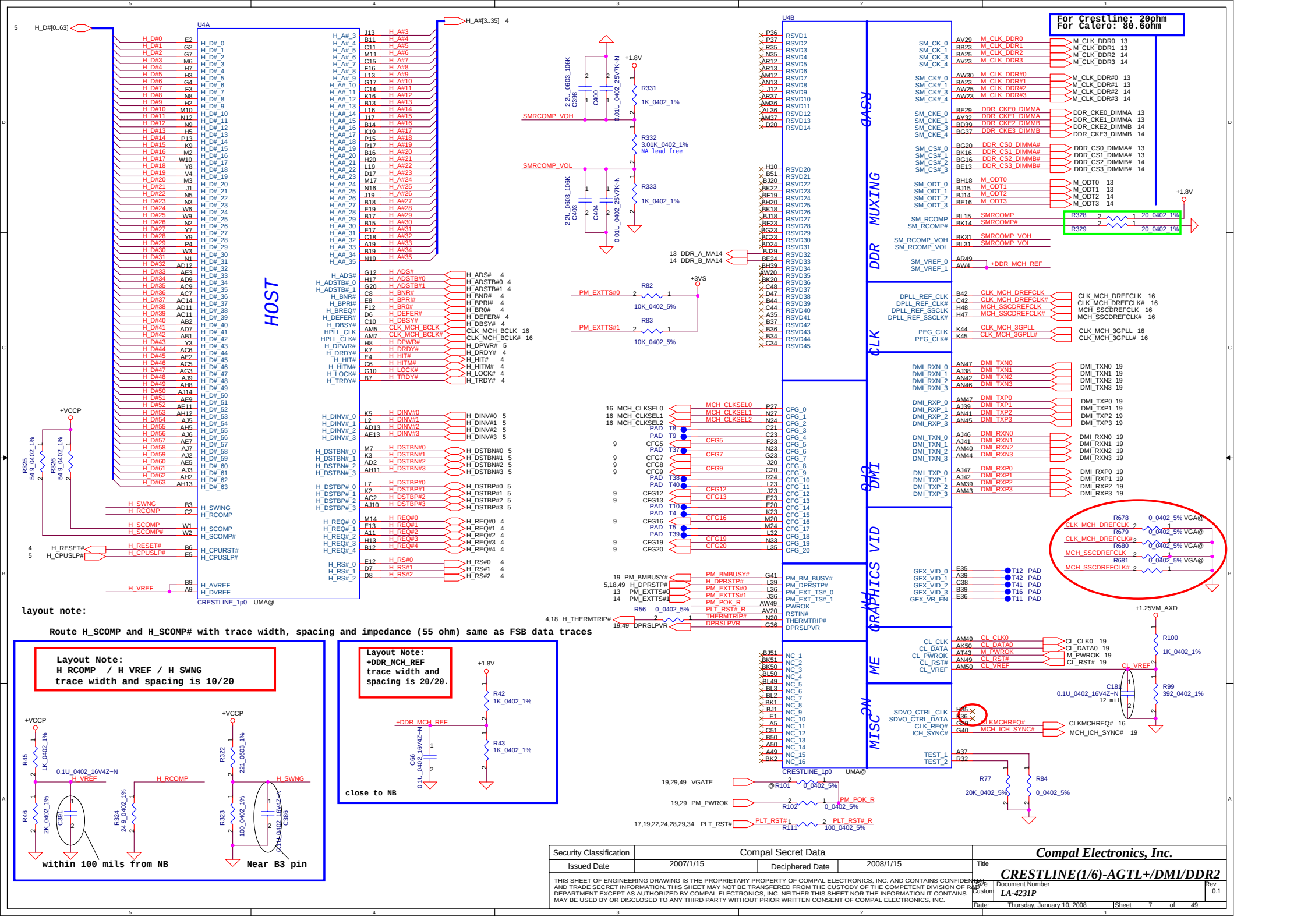
For Crestline: 20ohm
For Calero: 80.6ohm
HOST
U4A
U4B
CRESTLINE_1p0 UMA@
layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.
close to NB
within 100 mils from NB
Near B3 pin
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2008/1/15
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Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
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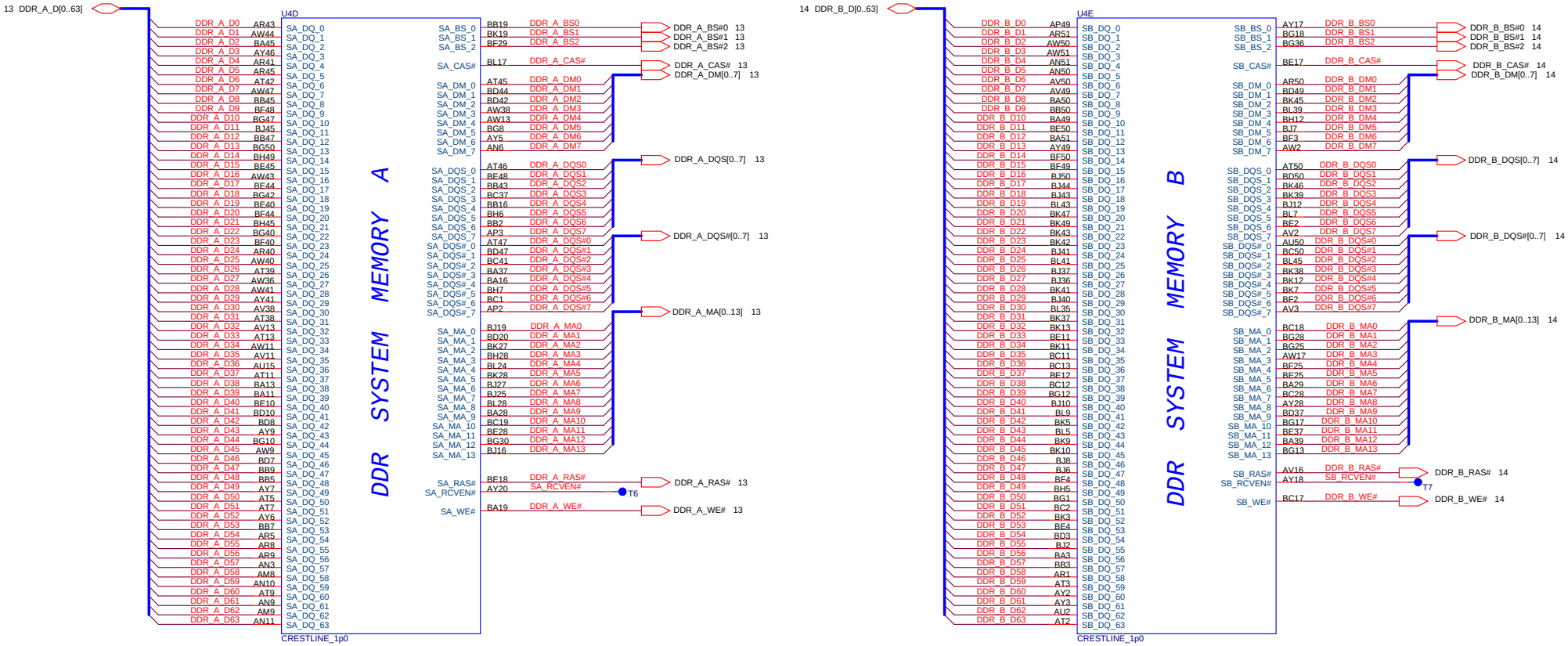

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Title: **CRESTLINE((2/6)-DDR2 A/B CH**

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For Crestline:2.4kohm
For Calero: 1.5Kohm

PEGCOMP trace width
and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

For Crestline:1.3kohm
For Calero: 255ohm

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

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Title: CRESTLINE((3/6)-VGA/LVDS/TV

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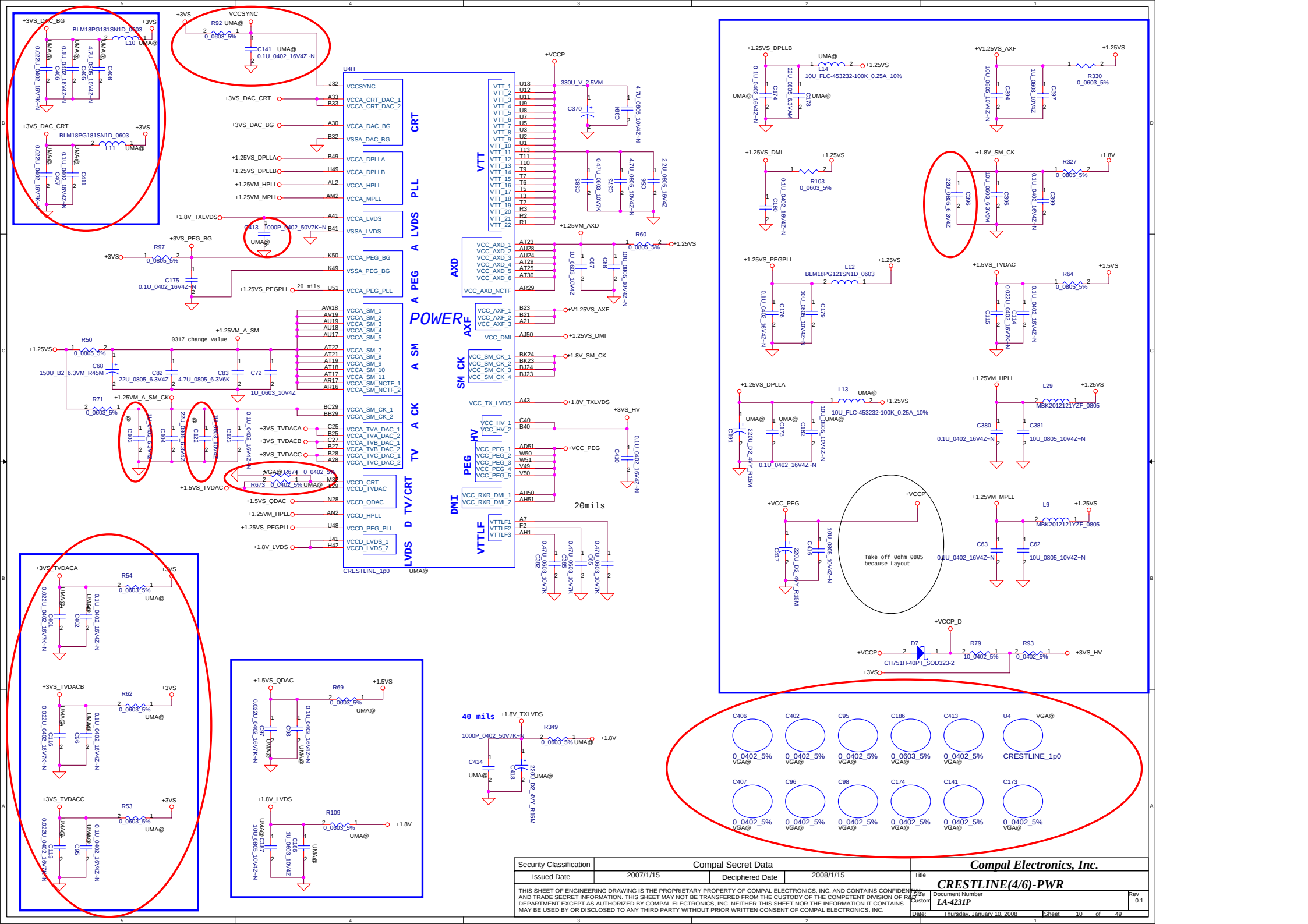

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Title: **CRESTLINE(4/6)-PWR**

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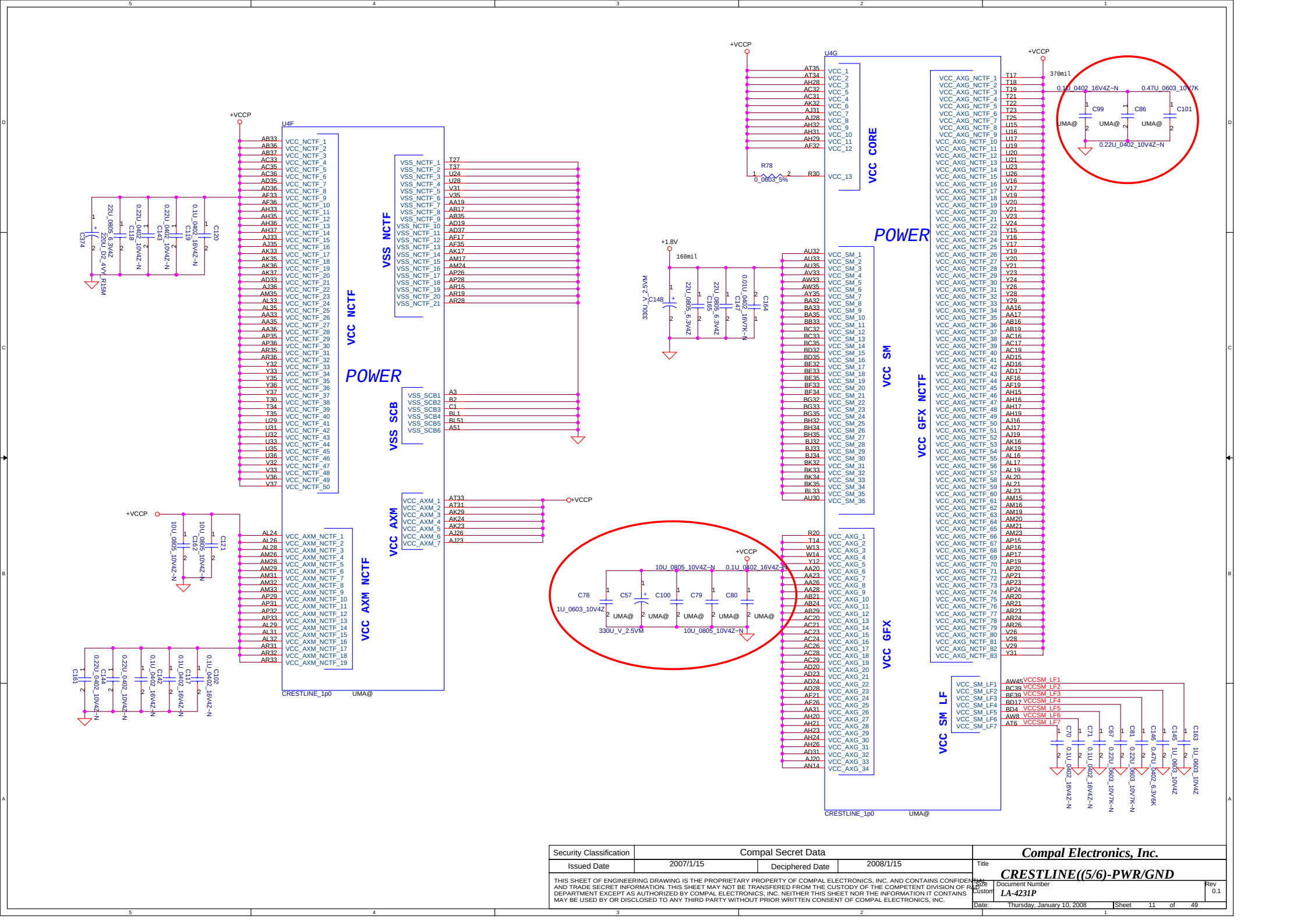

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Title	CRESTLINE((5/6)-PWR/GND
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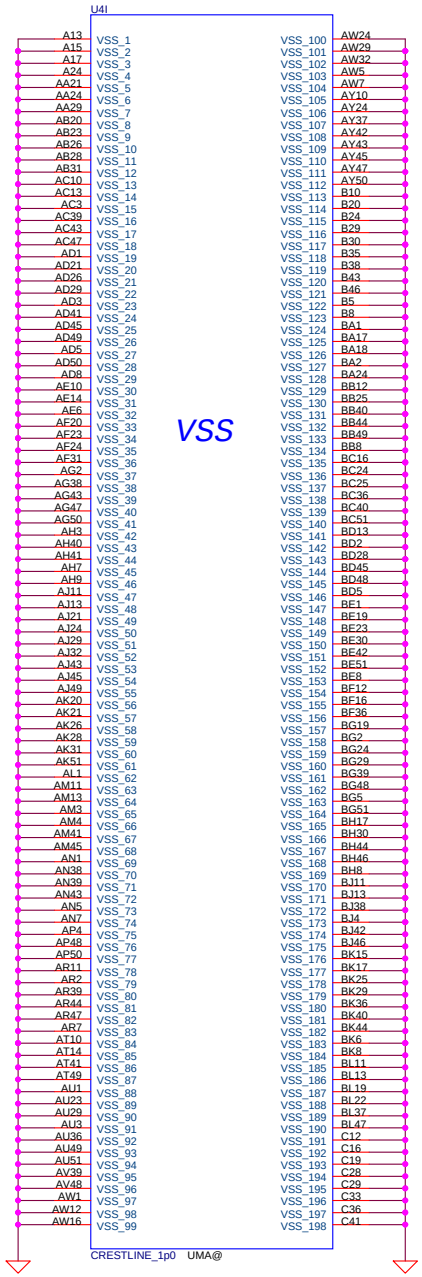

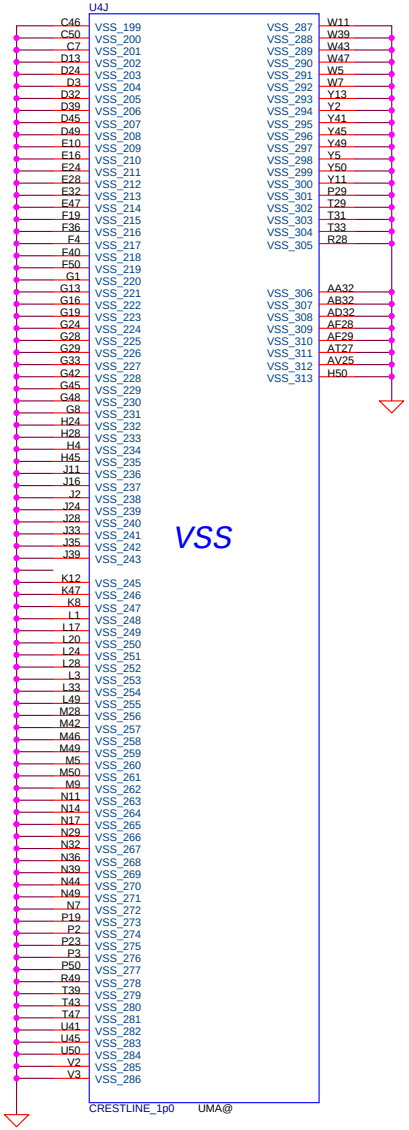

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Title: **CRESTLINE((6/6)-PWR/GND**

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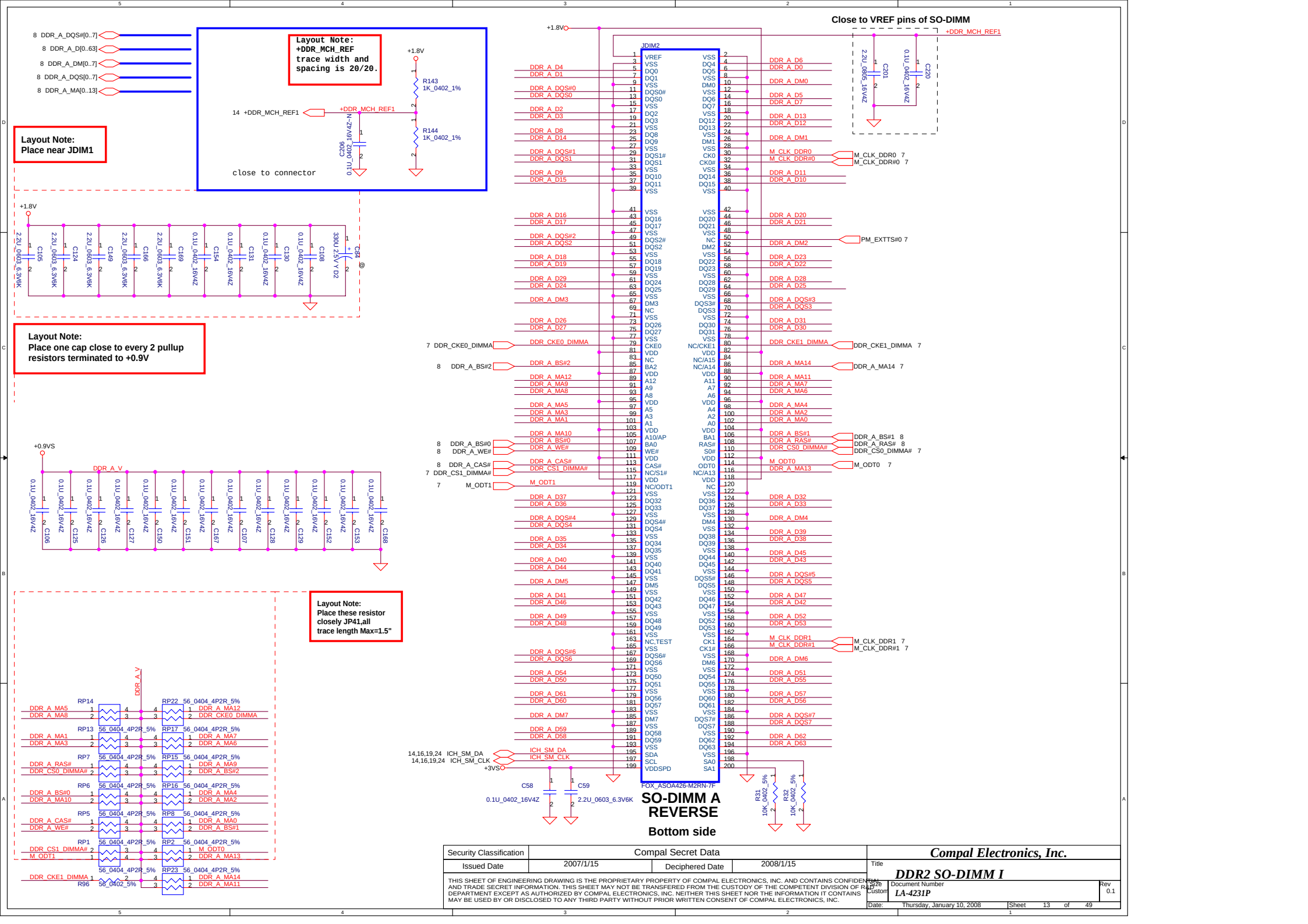

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Title: **DDR2 SO-DIMM I**

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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V

C112 2.2U_0603_6.3V6K
C139 2.2U_0603_6.3V6K
C160 2.2U_0603_6.3V6K
C138 2.2U_0603_6.3V6K
C177 2.2U_0603_6.3V6K
C109 0.1U_0402_16V4Z
C132 0.1U_0402_16V4Z
C133 0.1U_0402_16V4Z
C155 0.1U_0402_16V4Z
C189@ 330U 2.5V Y D2

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS

DDR_B_V

C110 0.1U_0402_16V4Z
C134 0.1U_0402_16V4Z
C135 0.1U_0402_16V4Z
C156 0.1U_0402_16V4Z
C157 0.1U_0402_16V4Z
C170 0.1U_0402_16V4Z
C171 0.1U_0402_16V4Z
C111 0.1U_0402_16V4Z
C136 0.1U_0402_16V4Z
C158 0.1U_0402_16V4Z
C137 0.1U_0402_16V4Z
C172 0.1U_0402_16V4Z
C159 0.1U_0402_16V4Z

Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"

DDR_B_V

RP18 56_0404_4P2R_5%: DDR_B_MA3, DDR_B_MA1 / DDR_B_MA12, DDR_B_MA9
RP10 56_0404_4P2R_5%: DDR_B_BS#0, DDR_B_MA10 / DDR_B_MA14, DDR_B_MA11
RP12 56_0404_4P2R_5%: DDR_B_MA0, DDR_B_BS#1 / DDR_B_MA5, DDR_B_MA8
RP11 56_0404_4P2R_5%: DDR_B_RAS#, DDR_CS2_DIMMB# / DDR_B_MA7, DDR_B_MA6
RP9 56_0404_4P2R_5%: DDR_B_CAS#, DDR_B_WE# / DDR_B_MA4, DDR_B_MA2
RP3 56_0404_4P2R_5%: DDR_CS3_DIMMB#, M_ODT3 / DDR_B_MA13, M_ODT2
RP25 56_0404_4P2R_5%: DDR_CKE3_DIMMB, R335 56_0402_5% / DDR_B_BS#2, DDR_CKE2_DIMMB
RP24_56_0404_4P2R_5%
RP26_56_0404_4P2R_5%
RP19_56_0404_4P2R_5%
RP21_56_0404_4P2R_5%
RP20_56_0404_4P2R_5%
RP4_56_0404_4P2R_5%

Close to VREF pins of SO-DIMM

+1.8V
+DDR_MCH_REF1 → +DDR_MCH_REF1 13
C221 2.2U_0805_16V4Z
C222 0.1U_0402_16V4Z

JDIM1
FOX_AS0A426-NARN-7F-N

1	VREF	VSS	2		
3	VSS	DQ4	4	DDR_B_D0	DDR_B_D5
5	DQ0	DQ5	6	DDR_B_D1	DDR_B_D4
7	DQ1	VSS	8		
9	VSS	DM0	10	DDR_B_DQS#0	DDR_B_DM0
11	DQS0#	VSS	12	DDR_B_DQS0	
13	DQS0	DQ6	14		DDR_B_D6
15	VSS	DQ7	16	DDR_B_D2	DDR_B_D7
17	DQ2	VSS	18		
19	DQ3	DQ12	20	DDR_B_D3	DDR_B_D12
21	VSS	DQ13	22		DDR_B_D13
23	DQ8	VSS	24	DDR_B_D8	
25	DQ9	DM1	26	DDR_B_D9	DDR_B_DM1
27	VSS	VSS	28		
29	DQS1#	CK0	30	DDR_B_DQS#1	M_CLK_DDR2 → M_CLK_DDR2 7
31	DQS1	CK0#	32	DDR_B_DQS1	M_CLK_DDR#2 → M_CLK_DDR#2 7
33	VSS	VSS	34		
35	DQ10	DQ14	36	DDR_B_D10	DDR_B_D14
37	DQ11	DQ15	38	DDR_B_D11	DDR_B_D15
39	VSS	VSS	40		
41	VSS	VSS	42		
43	DQ16	DQ20	44	DDR_B_D17	DDR_B_D21
45	DQ17	DQ21	46	DDR_B_D20	DDR_B_D16
47	VSS	VSS	48		
49	DQS2#	NC	50	DDR_B_DQS#2	PM_EXTTS#1 7
51	DQS2	DM2	52	DDR_B_DQS2	DDR_B_DM2
53	VSS	VSS	54		
55	DQ18	DQ22	56	DDR_B_D18	DDR_B_D22
57	DQ19	DQ23	58	DDR_B_D19	DDR_B_D23
59	VSS	VSS	60		
61	DQ24	DQ28	62	DDR_B_D28	DDR_B_D26
63	DQ25	DQ29	64	DDR_B_D25	DDR_B_D24
65	VSS	VSS	66		
67	DM3	DQS3#	68	DDR_B_DM3	DDR_B_DQS#3
69	NC	DQS3	70		DDR_B_DQS3
71	VSS	VSS	72		
73	DQ26	DQ30	74	DDR_B_D30	DDR_B_D29
75	DQ27	DQ31	76	DDR_B_D31	DDR_B_D27
77	VSS	VSS	78		
79	CKE0	NC/CKE1	80	7 DDR_CKE2_DIMMB → DDR_CKE2_DIMMB	DDR_CKE3_DIMMB → DDR_CKE3_DIMMB 7
81	VDD	VDD	82		
83	NC	NC/A15	84		
85	BA2	NC/A14	86	8 DDR_B_BS#2 → DDR_B_BS#2	DDR_B_MA14 → DDR_B_MA14 7
87	VDD	VDD	88		
89	A12	A11	90	DDR_B_MA12	DDR_B_MA11
91	A9	A7	92	DDR_B_MA9	DDR_B_MA7
93	A8	A6	94	DDR_B_MA8	DDR_B_MA6
95	VDD	VDD	96		
97	A5	A4	98	DDR_B_MA5	DDR_B_MA4
99	A3	A2	100	DDR_B_MA3	DDR_B_MA2
101	A1	A0	102	DDR_B_MA1	DDR_B_MA0
103	VDD	VDD	104		
105	A10/AP	BA1	106	DDR_B_MA10	DDR_B_BS#1 → DDR_B_BS#1 8
107	BA0	RAS#	108	8 DDR_B_BS#0 → DDR_B_BS#0	DDR_B_RAS# → DDR_B_RAS# 8
109	WE#	S0#	110	8 DDR_B_WE# → DDR_B_WE#	DDR_CS2_DIMMB# → DDR_CS2_DIMMB# 7
111	VDD	VDD	112		
113	CAS#	ODT0	114	8 DDR_B_CAS# → DDR_B_CAS#	M_ODT2 → M_ODT2 7
115	NC/S1#	NC/A13	116	7 DDR_CS3_DIMMB# → DDR_CS3_DIMMB#	DDR_B_MA13 → DDR_B_MA13
117	VDD	VDD	118		
119	NC/ODT1	NC	120	7 M_ODT3 → M_ODT3	
121	VSS	VSS	122		
123	DQ32	DQ36	124	DDR_B_D32	DDR_B_D36
125	DQ33	DQ37	126	DDR_B_D33	DDR_B_D37
127	VSS	VSS	128		
129	DQS4#	DM4	130	DDR_B_DQS#4	DDR_B_DM4
131	DQS4	VSS	132	DDR_B_DQS4	
133	VSS	DQ38	134		DDR_B_D39
135	DQ34	DQ39	136	DDR_B_D34	DDR_B_D38
137	DQ35	VSS	138	DDR_B_D35	
139	VSS	DQ44	140		DDR_B_D44
141	DQ40	DQ45	142	DDR_B_D40	DDR_B_D45
143	DQ41	VSS	144	DDR_B_D41	
145	VSS	DQS5#	146		DDR_B_DQS#5
147	DM5	DQS5	148	DDR_B_DM5	DDR_B_DQS5
149	VSS	VSS	150		
151	DQ42	DQ46	152	DDR_B_D42	DDR_B_D46
153	DQ43	DQ47	154	DDR_B_D43	DDR_B_D47
155	VSS	VSS	156		
157	DQ48	DQ52	158	DDR_B_D48	DDR_B_D52
159	DQ49	DQ53	160	DDR_B_D49	DDR_B_D53
161	VSS	VSS	162		
163	NC,TEST	CK1	164		M_CLK_DDR3 → M_CLK_DDR3 7
165	VSS	CK1#	166		M_CLK_DDR#3 → M_CLK_DDR#3 7
167	DQS6#	VSS	168	DDR_B_DQS#6	
169	DQS6	DM6	170	DDR_B_DQS6	DDR_B_DM6
171	VSS	VSS	172		
173	DQ50	DQ54	174	DDR_B_D51	DDR_B_D54
175	DQ51	DQ55	176	DDR_B_D50	DDR_B_D55
177	VSS	VSS	178		
179	DQ56	DQ60	180	DDR_B_D56	DDR_B_D60
181	DQ57	DQ61	182	DDR_B_D61	DDR_B_D57
183	VSS	VSS	184		
185	DM7	DQS7#	186	DDR_B_DM7	DDR_B_DQS#7
187	VSS	DQS7	188		DDR_B_DQS7
189	DQ58	DQ62	190	DDR_B_D59	DDR_B_D62
191	DQ59	DQ63	192	DDR_B_D58	DDR_B_D63
193	VSS	VSS	194		
195	SDA	SA1	196	13,16,19,24 ICH_SM_DA → ICH_SM_DA	
197	SCL	SAO	198	13,16,19,24 ICH_SM_CLK → ICH_SM_CLK	
199	VDDSPD	VSS	200		

+3VS
C61 0.1U_0402_16V4Z
C60 2.2U_0603_6.3V6K
R33 10K_0402_5% → +3VS
R34 10K_0402_5%

SO-DIMM B
REVERSE
Bottom side

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

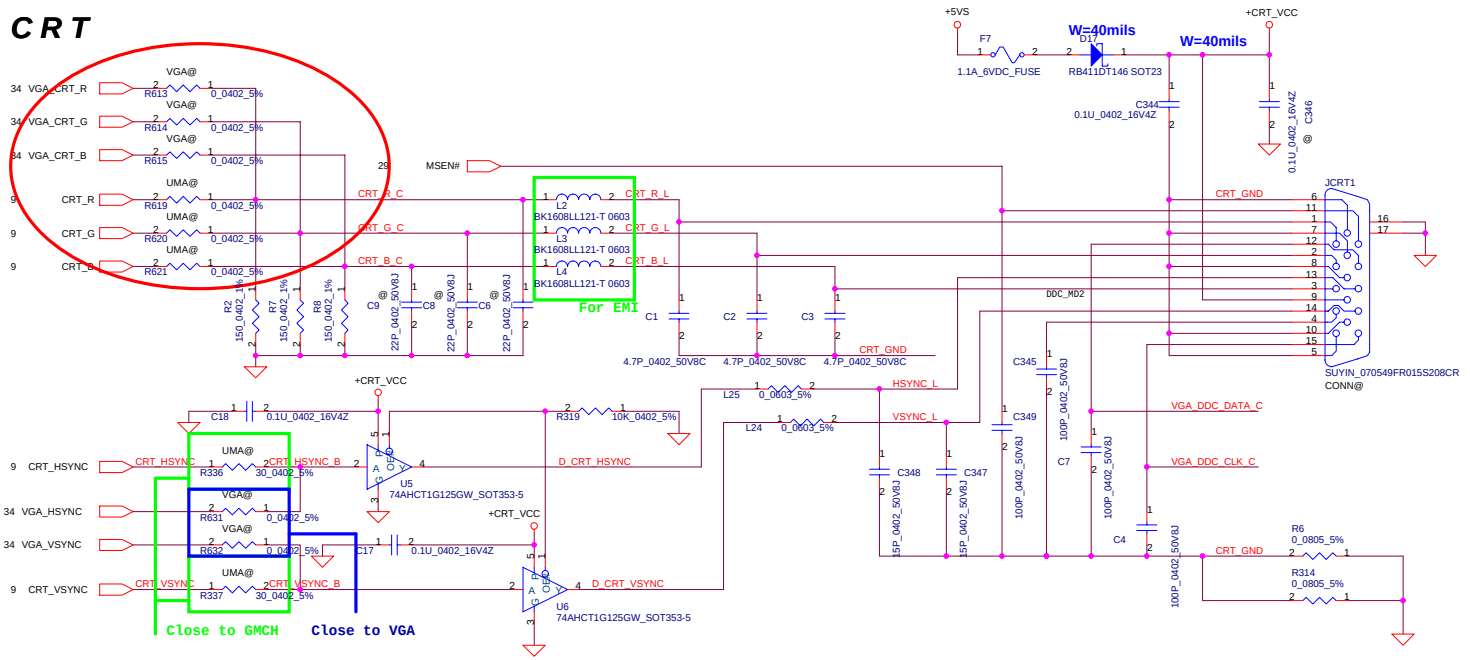
Compal Electronics, Inc.

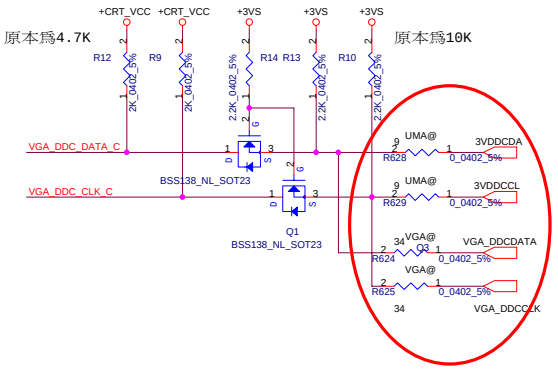
Title: **DDR2 SO-DIMM II**

Size: Custom | Document Number: **LA-4231P** | Rev: 0.1

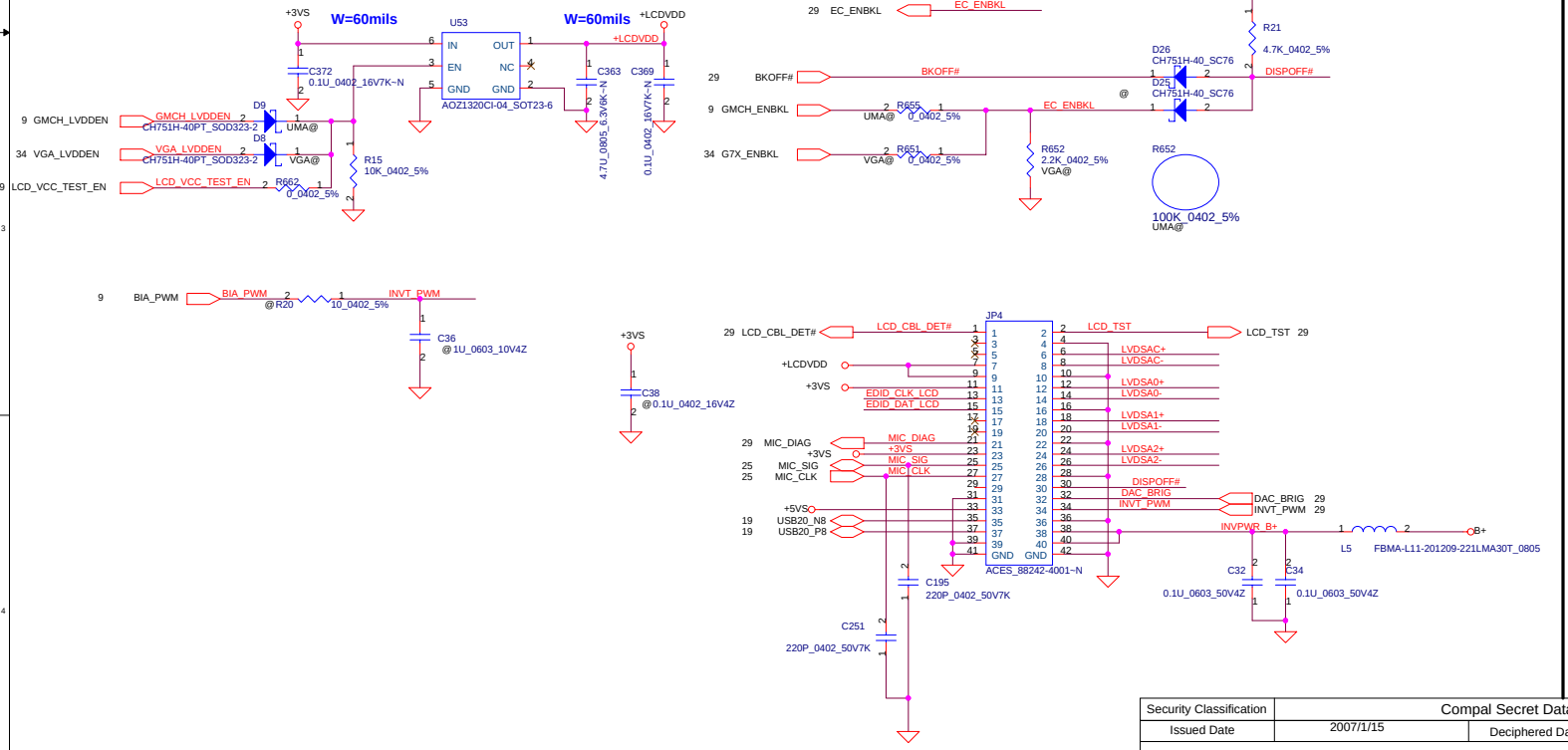
Date: Thursday, January 10, 2008 | Sheet 14 of 49

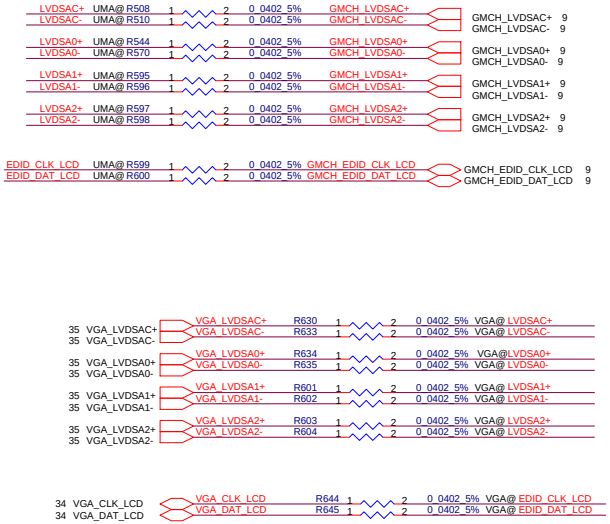
CRT





LCD





Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: CRT CONN/LCD CONN

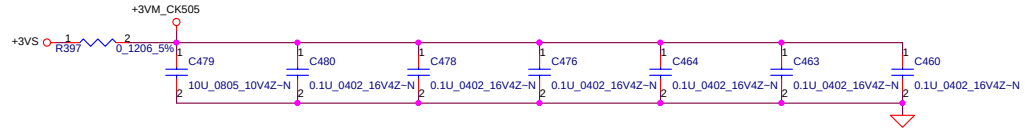
Size: Custom | Document Number: LA-4231P | Rev: 0.1

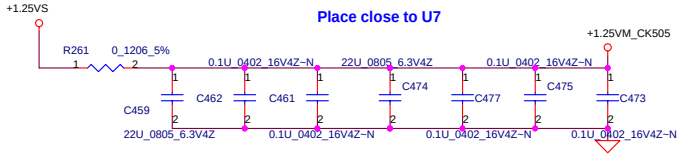
Date: Thursday, January 10, 2008 | Sheet 15 of 49

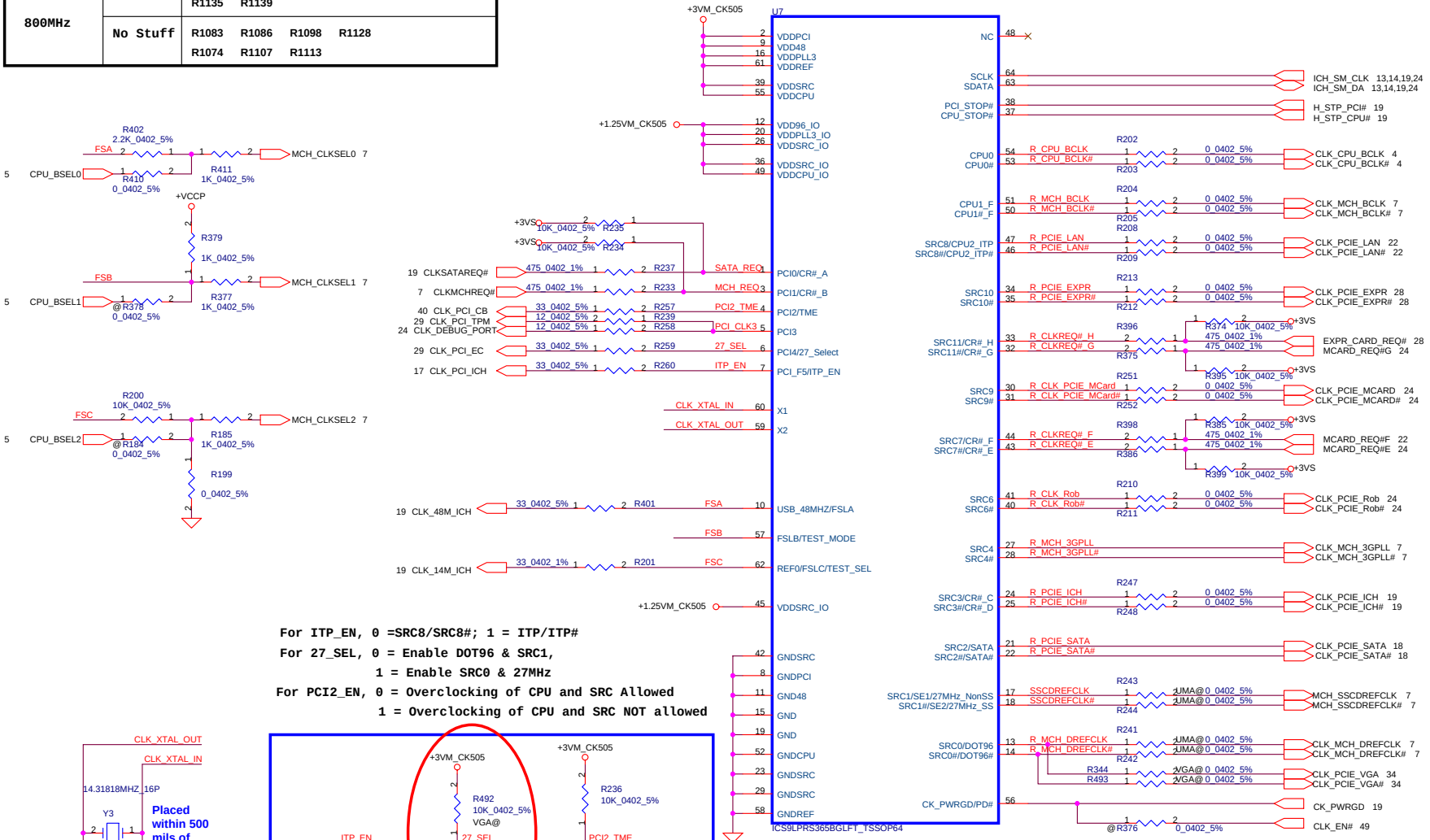
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			







For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

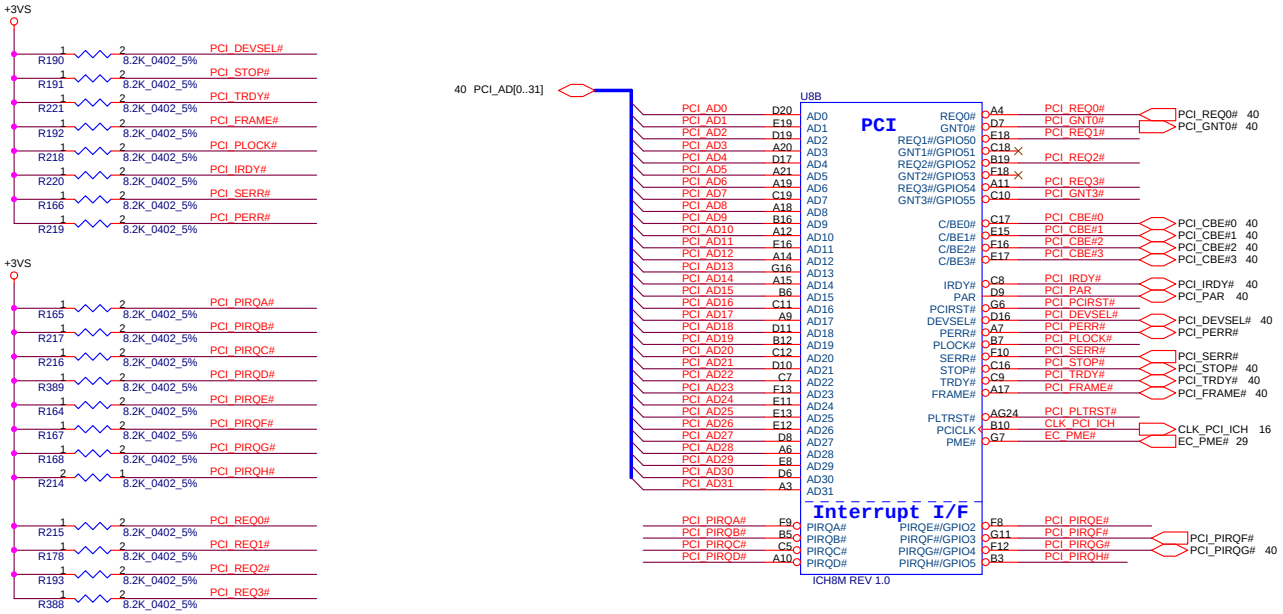
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

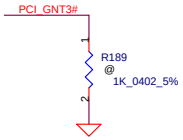
Compal Electronics, Inc.

Title: **Clock generator**

Size	Document Number	Rev
Custom	LA-4231P	0.1

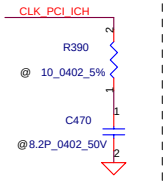
Date: Thursday, January 10, 2008 | Sheet 16 of 49





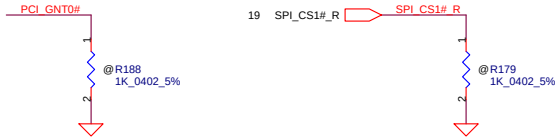
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

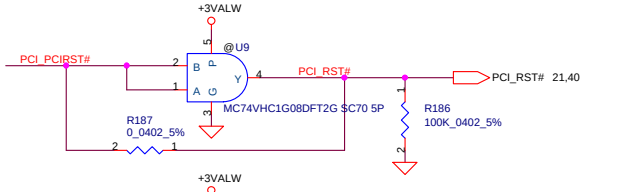
Place closely pin B10

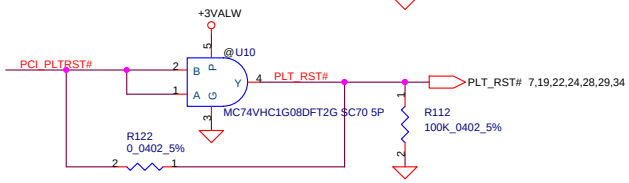


Check if use LPC?

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *







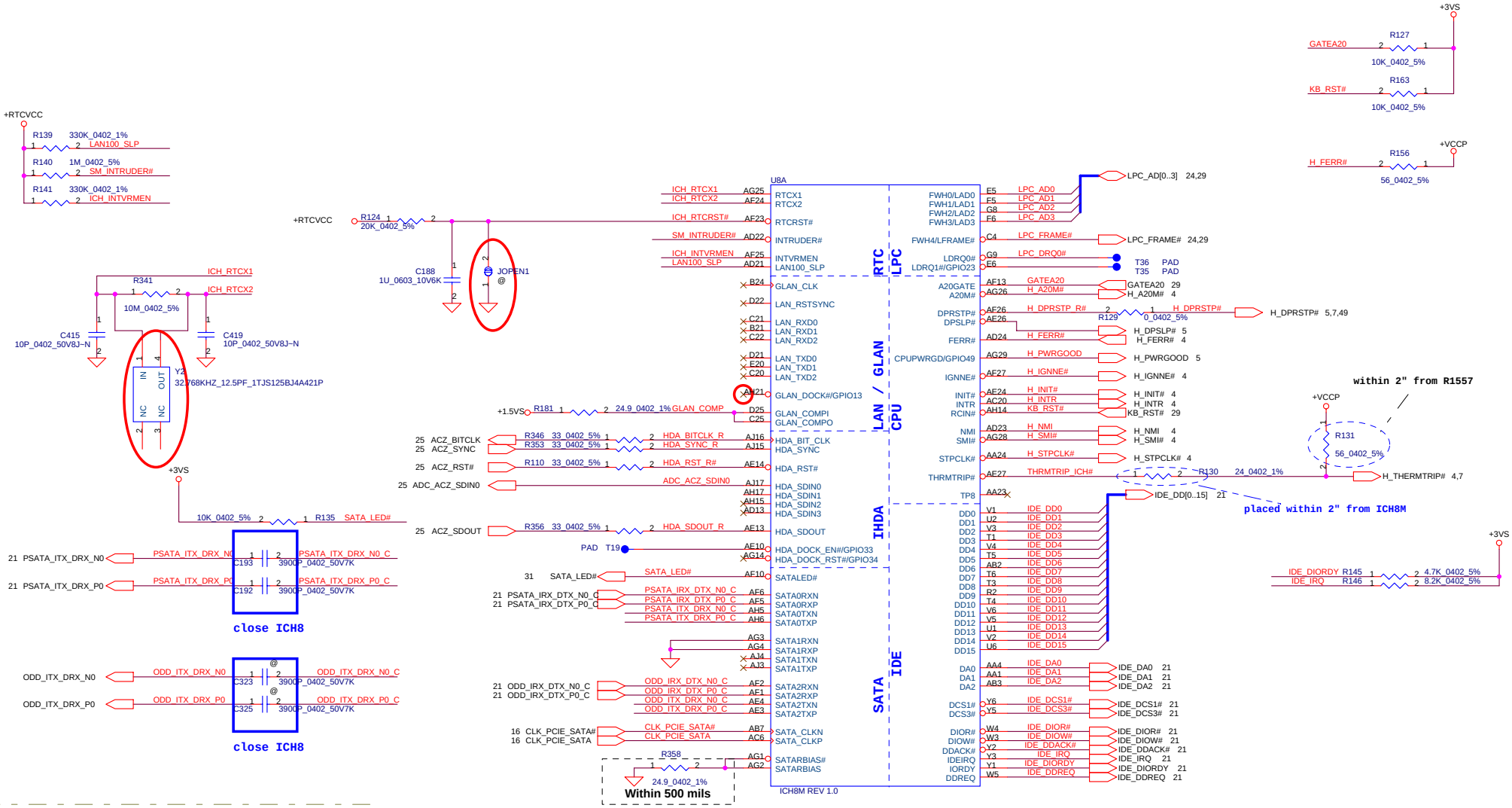
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ICH8(1/4)-PCI/INT

Size	Document Number	Rev
Custom	LA-4231P	0.1

Date: Thursday, January 10, 2008 Sheet 17 of 49



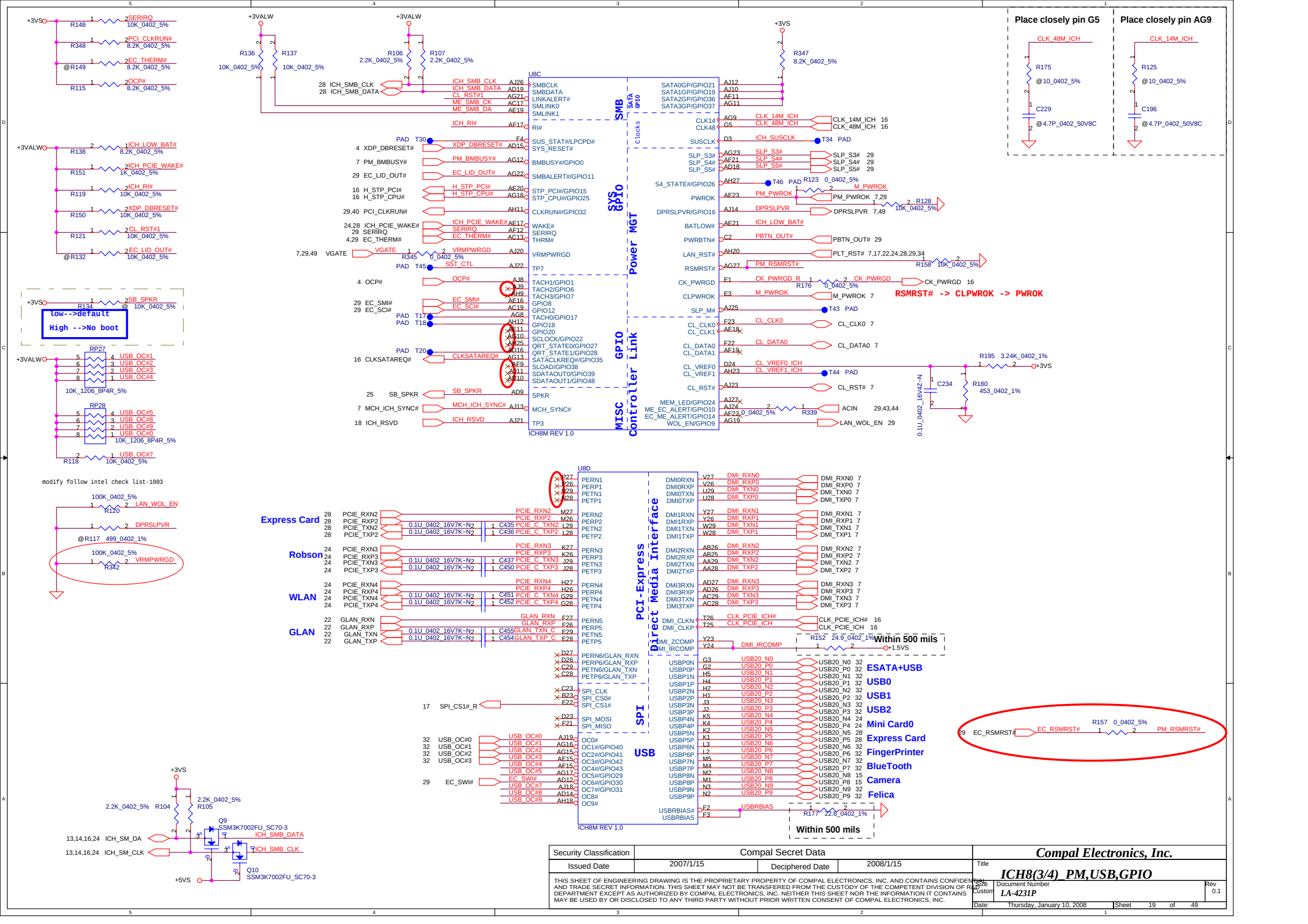
XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Compal Electronics, Inc.

Title: ICH8(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: LA-4231P | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 18 of 49



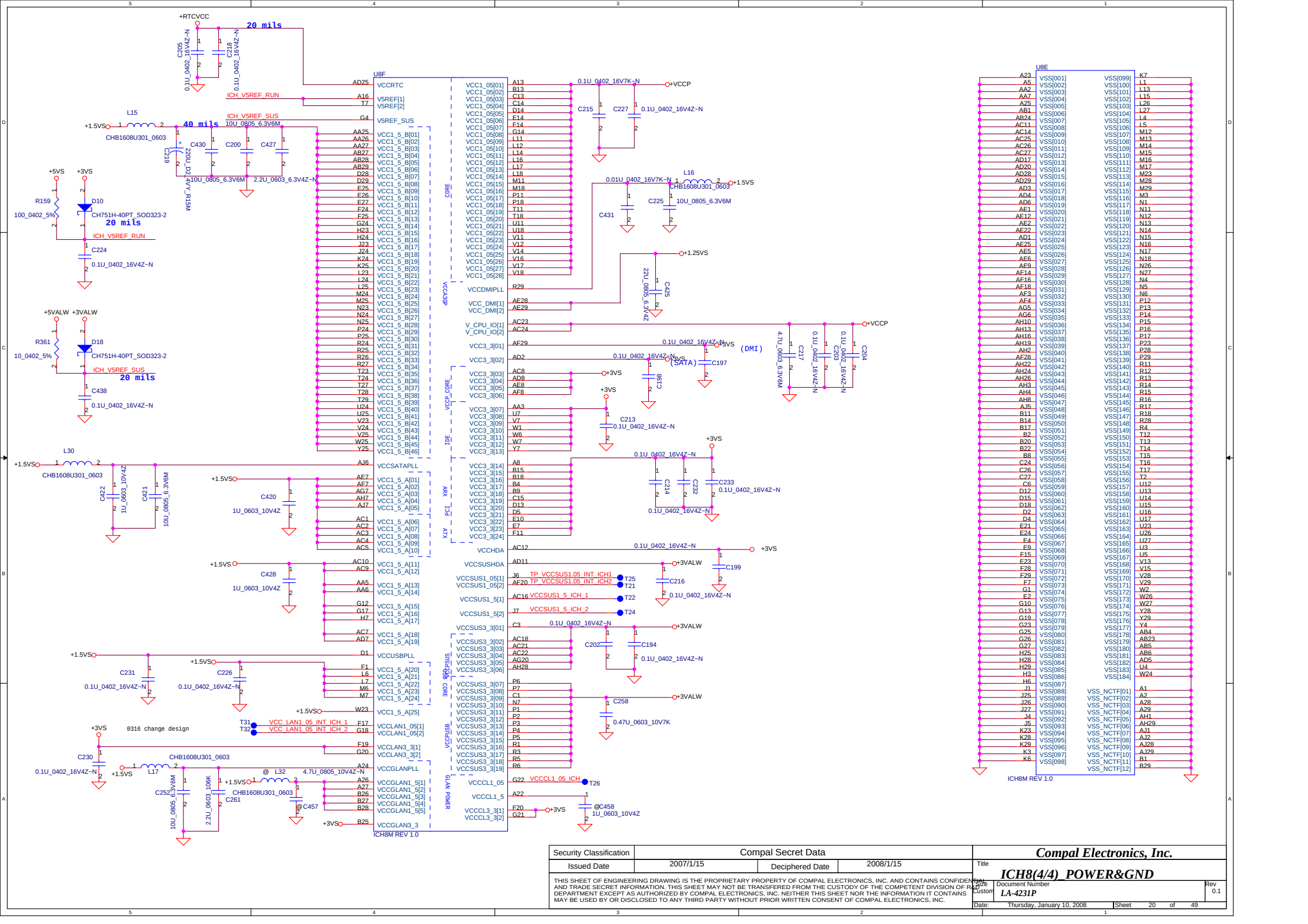
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **ICH8(3/4)_PM,USB,GPIO**

Size	Document Number	Rev
Custom	LA-4231P	0.1

Date: Thursday, January 10, 2008 | Sheet 19 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

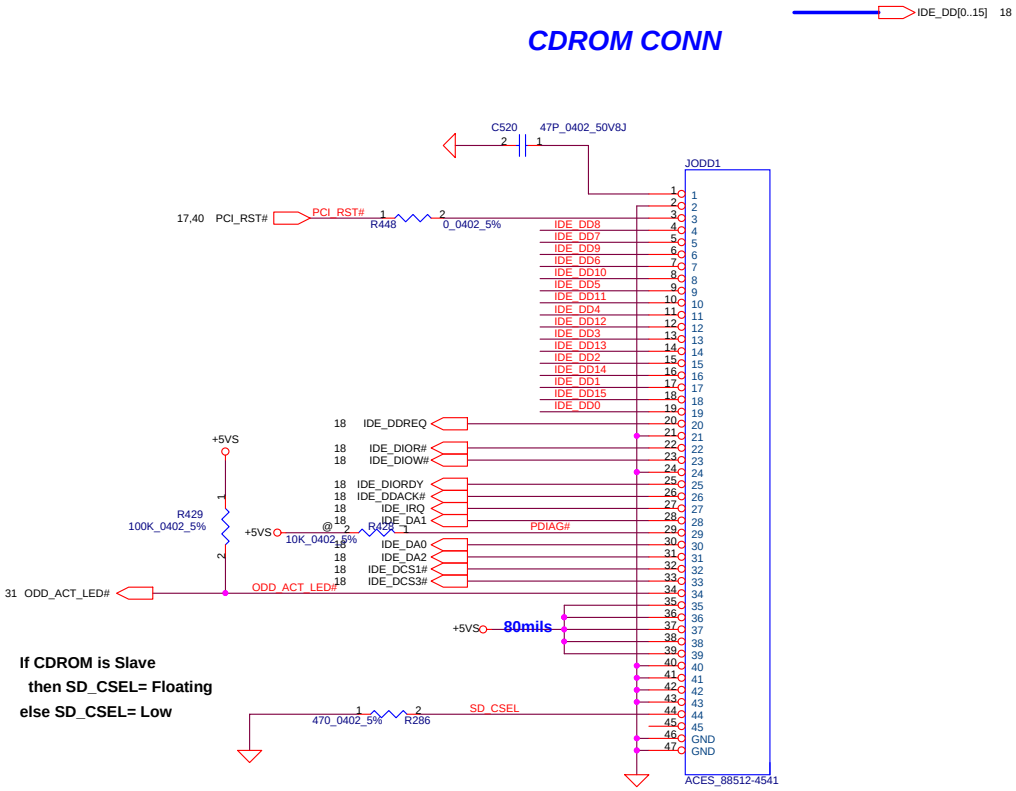
Compal Electronics, Inc.

Title: ICH8(4/4)_POWER&GND

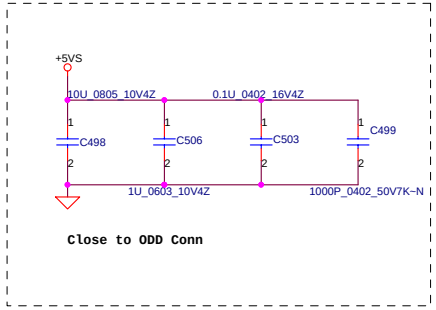
Size	Document Number	Rev
Custom	LA-4231P	0.1

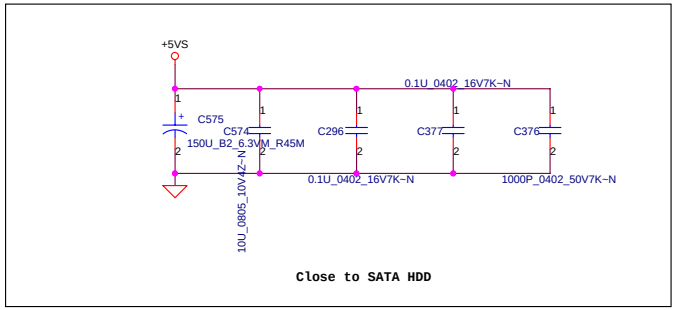
Date: Thursday, January 10, 2008 Sheet 20 of 49

CDROM CONN

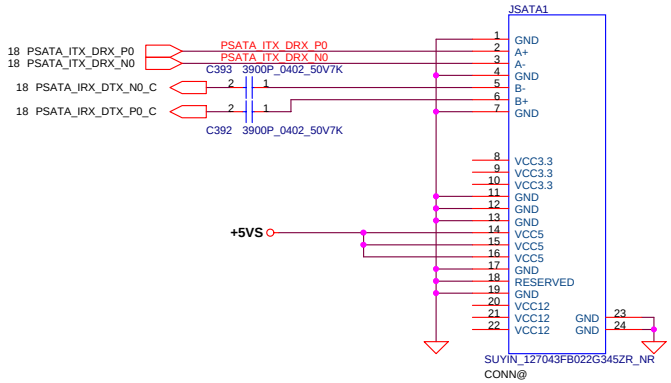


If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low

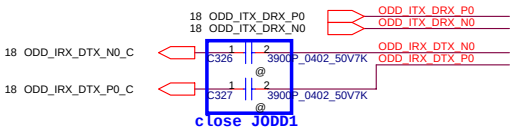




SATA HDD CONN



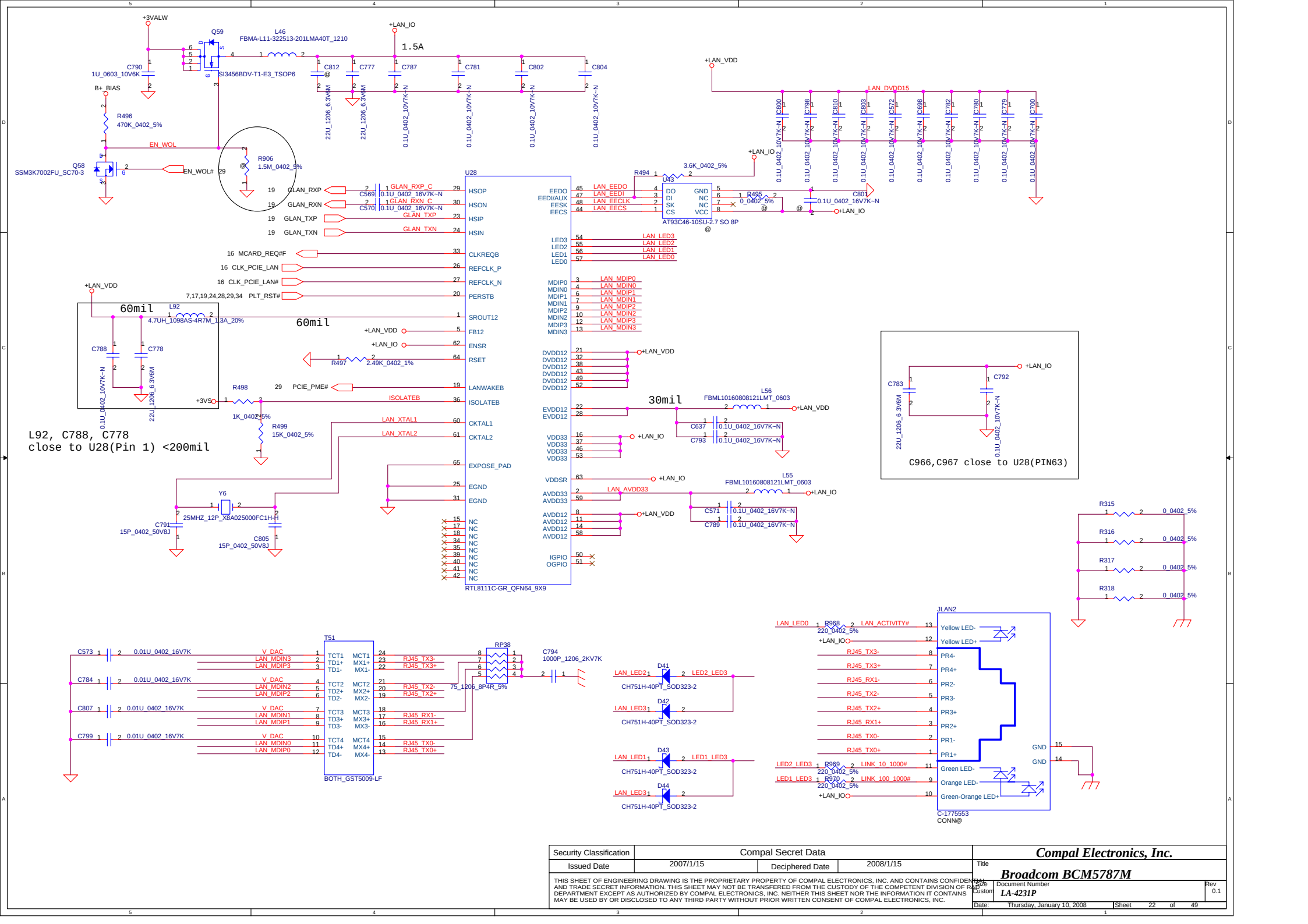
RESERVE(SATA ODD NET)



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title: **HDD/CDROM**

Size: Custom	Document Number: LA-4231P	Rev: 0.1
Date: Thursday, January 10, 2008	Sheet 21 of 49	



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Broadcom BCM5787M**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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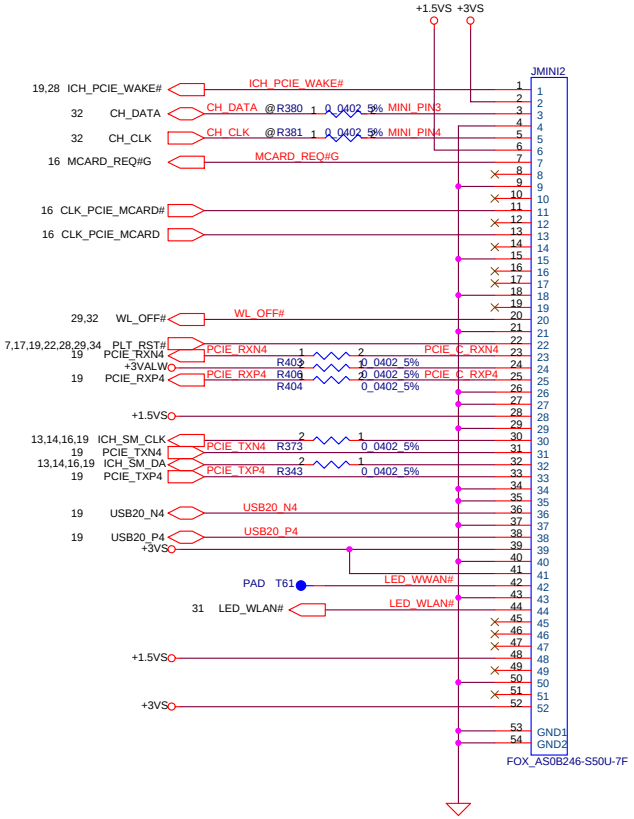
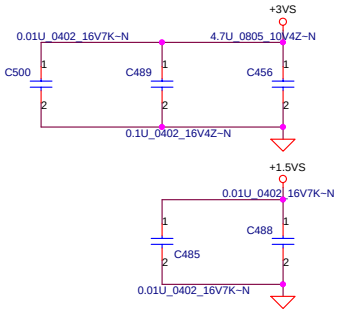
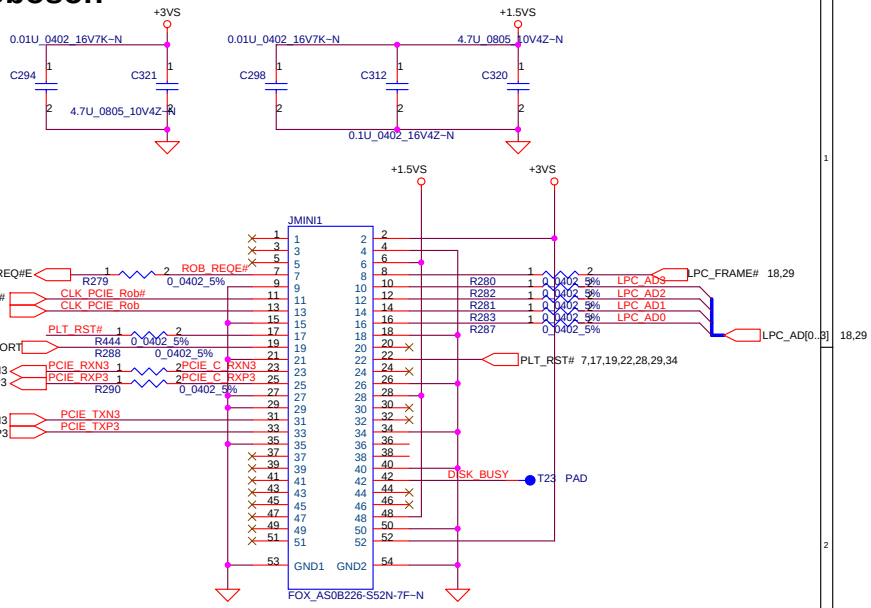
Mini-Express Card---WLAN

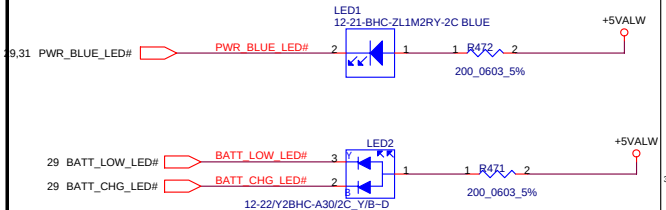




Roboson



Power status(Left)



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

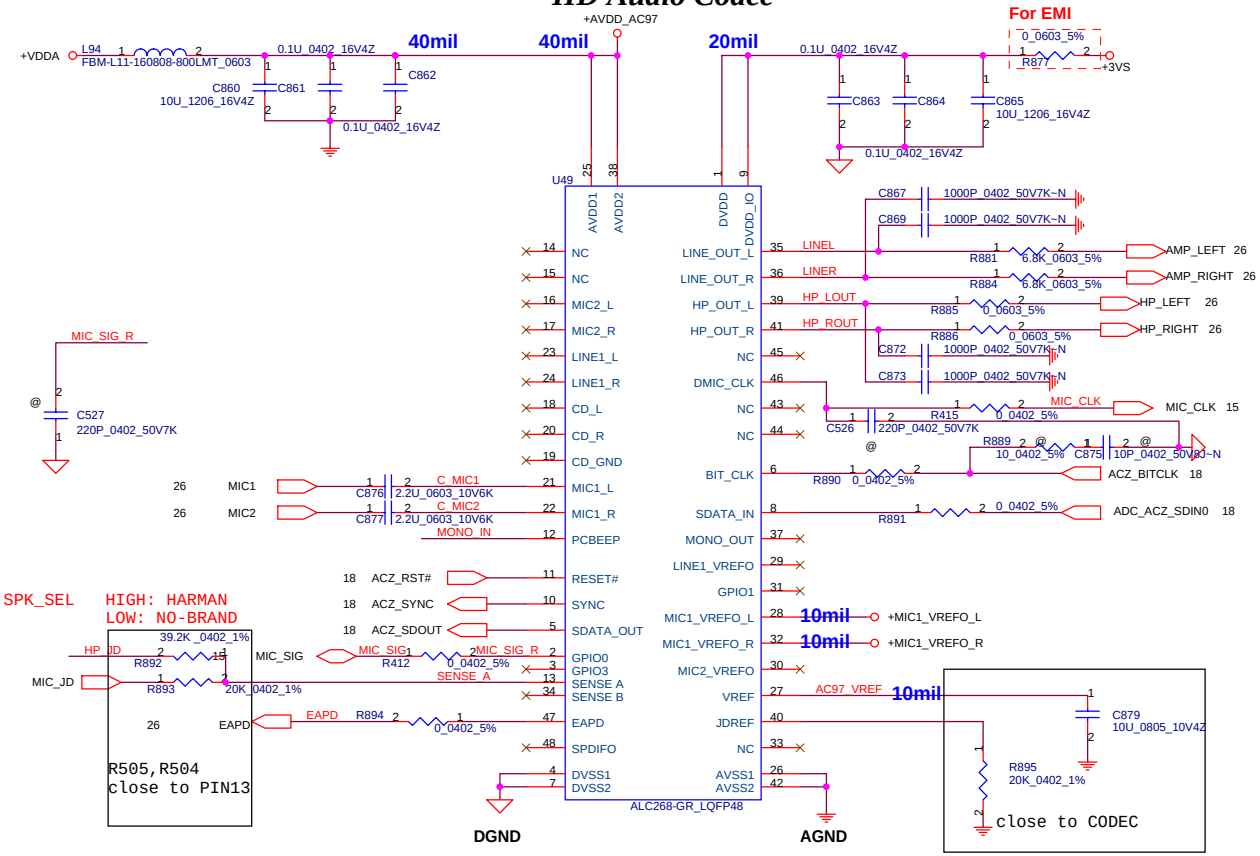
Compal Electronics, Inc.

Title: **Mini-Card/LED**

Size	Document Number	Rev
Custom	LA-4231P	0.1

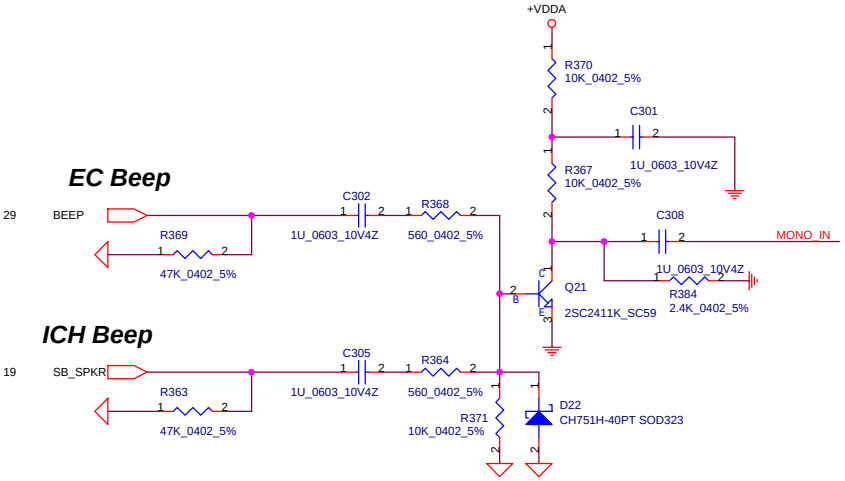
Date: Thursday, January 10, 2008 Sheet 24 of 49

HD Audio Codec



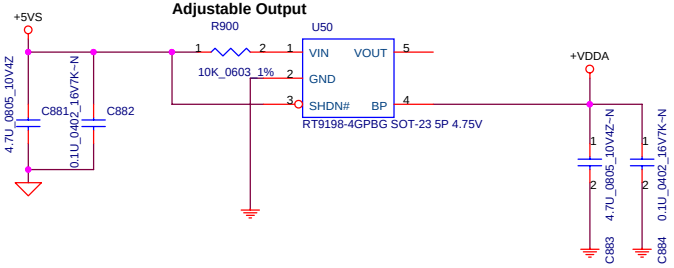
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

EC Beep

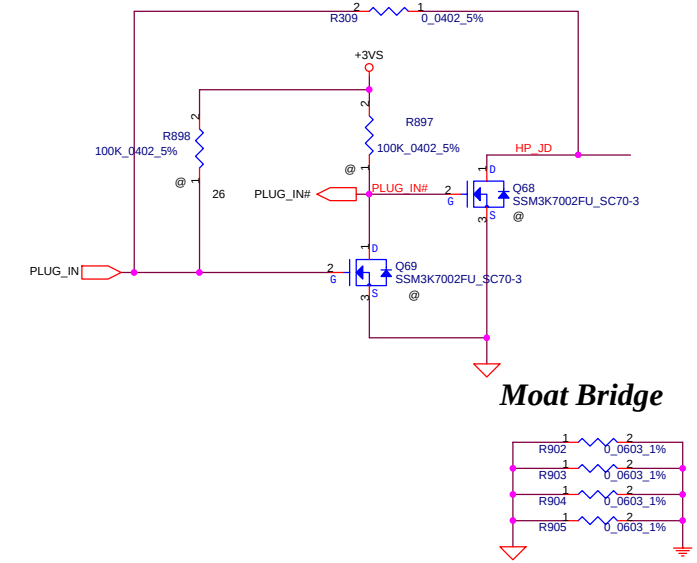


ICH Beep

Regulator for CODEC



Moat Bridge



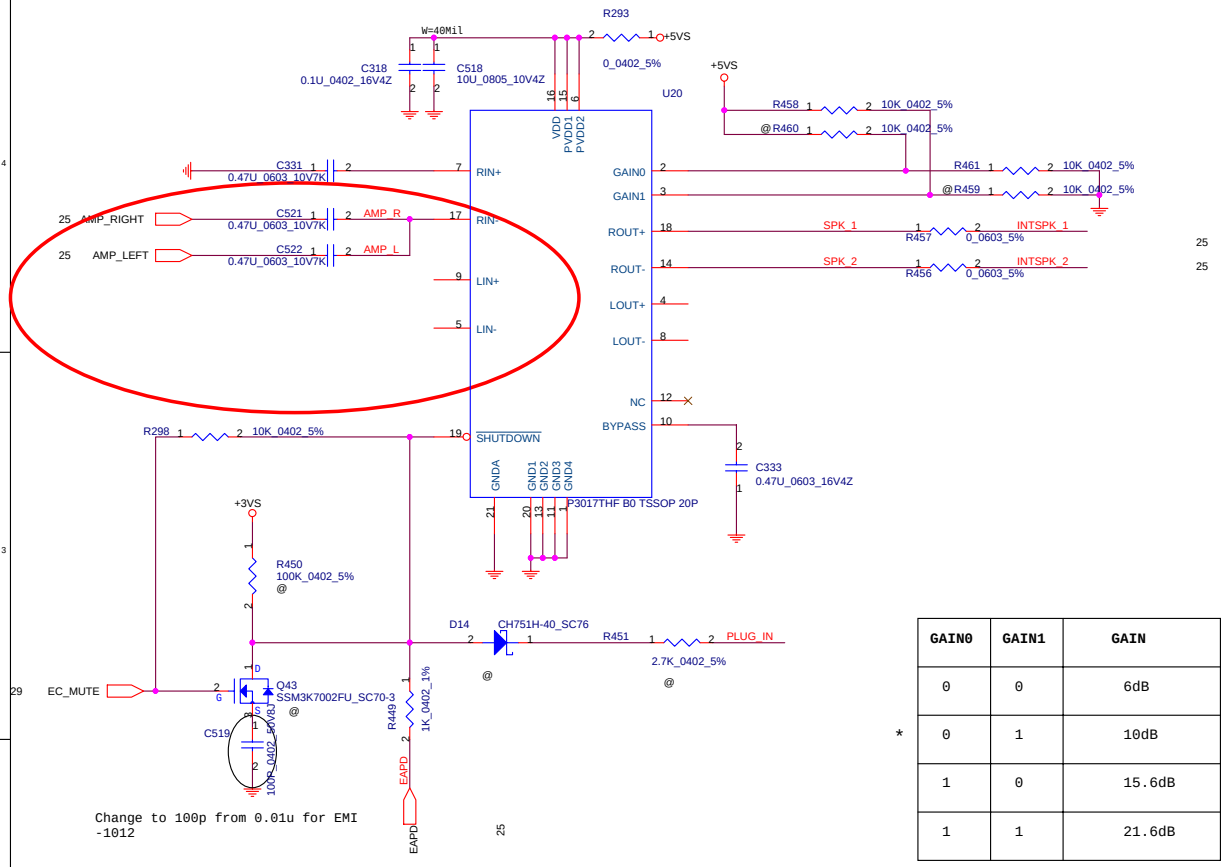
Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

Compal Electronics, Inc.

Title: **HD Audio Codec_ALC268**

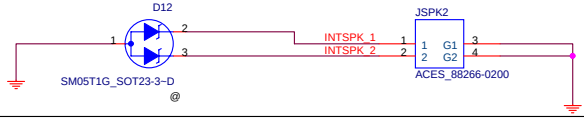
Size	Document Number	Rev
	LA-4231P	1.0

Date: Thursday, January 10, 2008 | Sheet 25 of 49

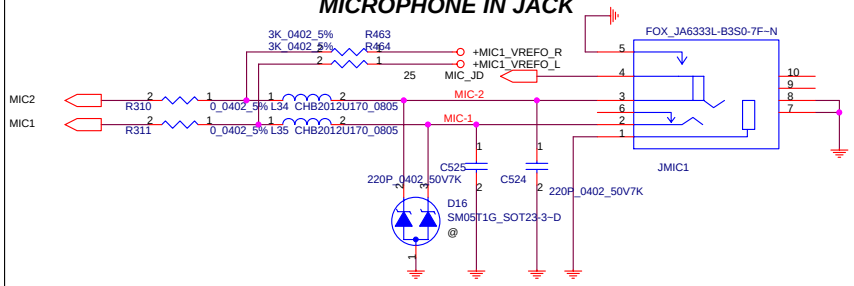


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

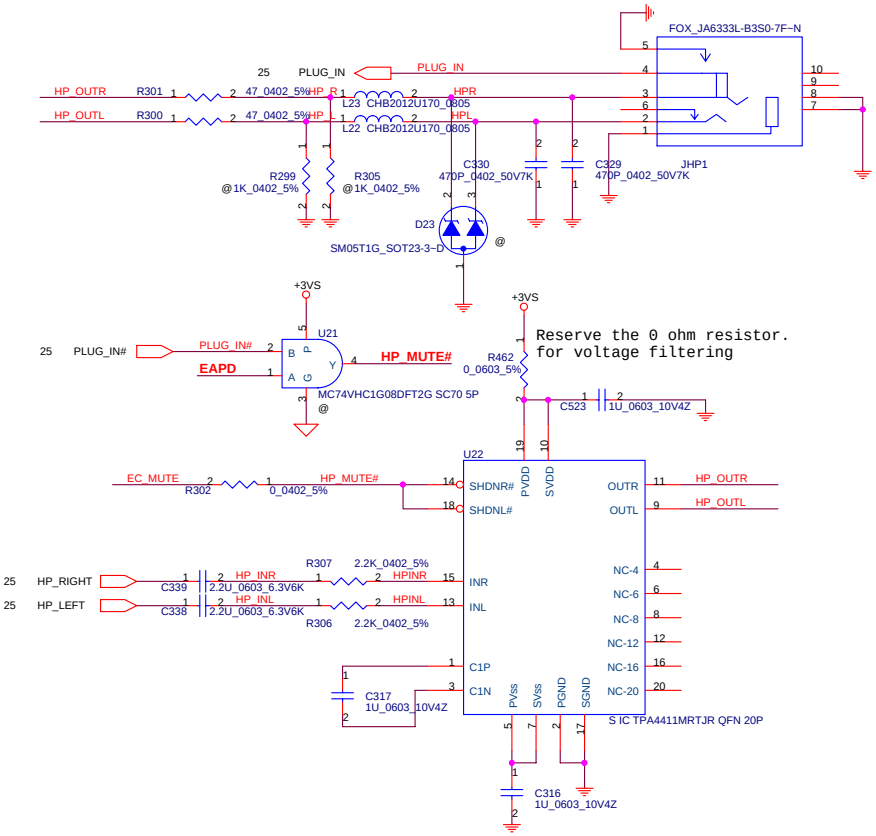
Speaker Connector



MICROPHONE IN JACK



HEADPHONE OUT JACK



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **AMP/Audio Jack**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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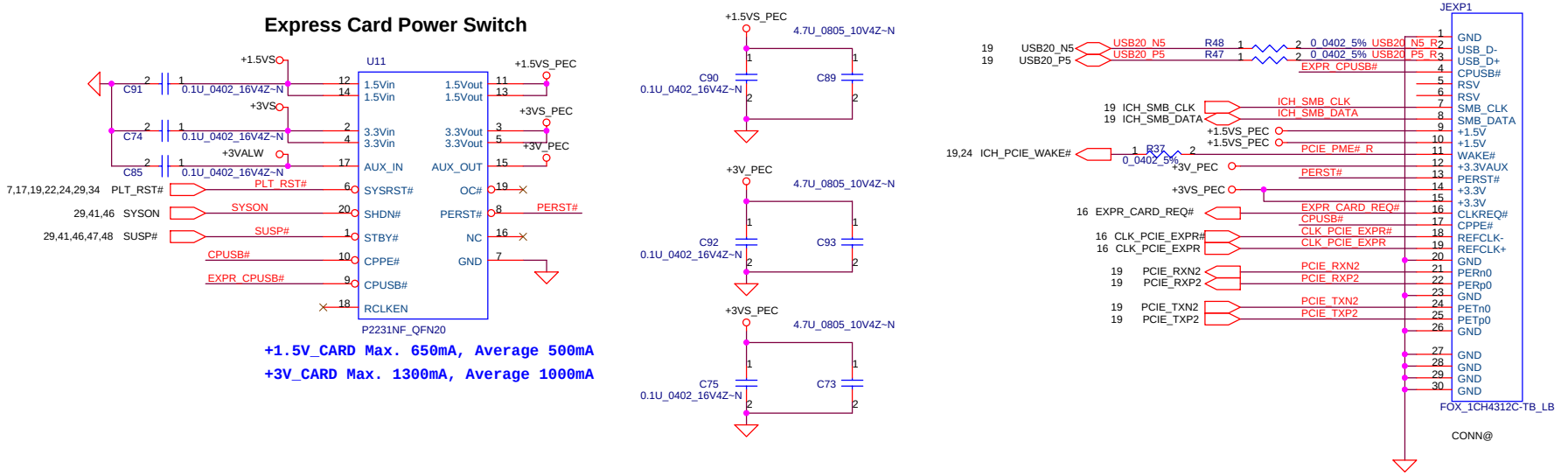
Express card



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **EXPRESS CARD**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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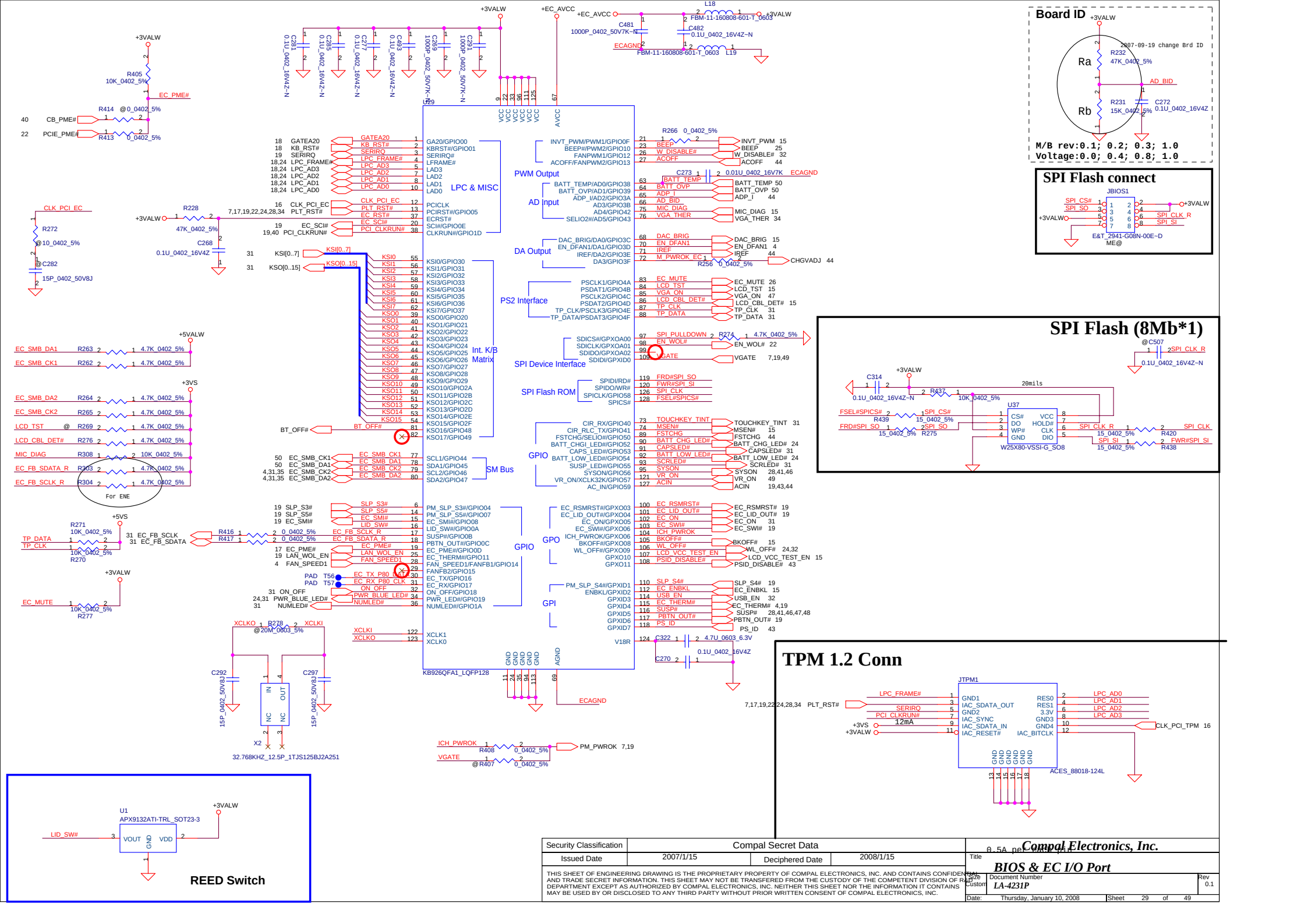
Board ID
+3VALW
2007-09-19 change Brd ID
Ra
R232
47K_0402_5%
AD_BID
Rb
R231
15K_0402_5%
C272
0.1U_0402_16V4Z
M/B rev:0.1; 0.2; 0.3; 1.0
Voltage:0.0; 0.4; 0.8; 1.0
SPI Flash connect
JBIOS1
SPI_CS#
SPI_SO
SPI_CLK_R
SPI_SI
+3VALW
E&T_2941-G08N-00E-D
ME@
SPI Flash (8Mb*1)
@C507
SPI_CLK_R
0.1U_0402_16V4Z-N
C314
R437
10K_0402_5%
20mils
U37
FSEL#SPICS#
FRD#SPI_SO
SPI_CS#
SPI_SO
CS#
DO
WP#
GND
VCC
HOLD#
CLK
DIO
W25X80-VSSI-G_SO8
R439
R275
R420
R438
SPI_CLK
SPI_SI
FWR#SPI_SI
TPM 1.2 Conn
JTPM1
LPC_FRAME#
SERIRQ
PCI_CLKRUN#
12mA
+3VS
+3VALW
GND1
IAC_SDATA_OUT
GND2
IAC_SYNC
IAC_SDATA_IN
IAC_RESET#
RES0
RES1
3.3V
GND3
GND4
IAC_BITCLK
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
CLK_PCI_TPM
ACES_88018-124L
U29
KB926QFA1_LQFP128
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
R405
10K_0402_5%
EC_PME#
R414
R413
CB_PME#
PCIE_PME#
R228
47K_0402_5%
C268
0.1U_0402_16V4Z
CLK_PCI_EC
R272
@10_0402_5%
@C282
15P_0402_50V8J
R266
C273
0.01U_0402_16V7K
ECAGND
C481
1000P_0402_50V7K-N
C482
0.1U_0402_16V4Z-N
L18
FBM-11-160808-601-T_0603
L19
C322
4.7U_0603_6.3V
C270
0.1U_0402_16V4Z
R263
R262
R264
R265
R269
R276
R308
R303
R304
4.7K_0402_5%
10K_0402_5%
For ENE
R271
R270
R277
10K_0402_5%
R416
R417
0_0402_5%
R278
@20M_0603_5%
X2
32.768KHZ_12.5P_1TJS125BJ2A251
C292
C297
15P_0402_50V8J
R408
R407
ICH_PWROK
VGATE
PM_PWROK 7,19
U1
APX9132ATI-TRL_SOT23-3
LID_SW#
VOUT
GND
VDD
REED Switch
Security Classification
Compal Secret Data
Issued Date
2007/1/15
Deciphered Date
2008/1/15
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
BIOS & EC I/O Port
Size
Custom
Document Number
LA-4231P
Rev
0.1
Date:
Thursday, January 10, 2008
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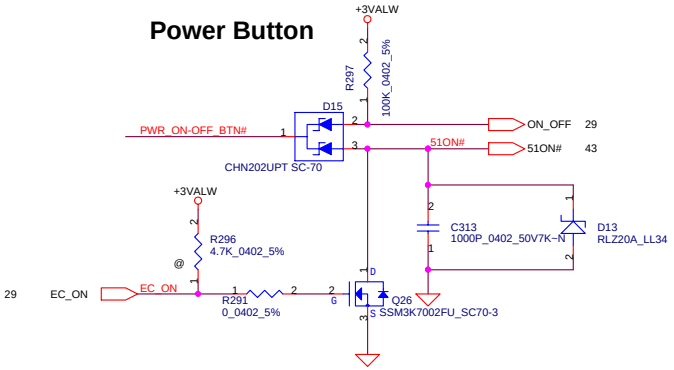
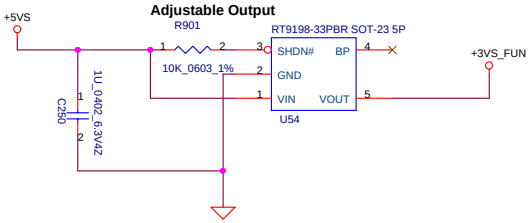
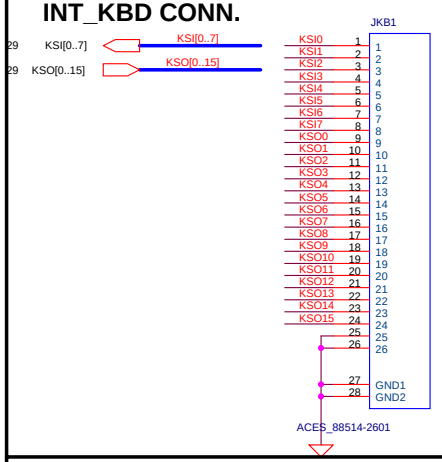
Power Button

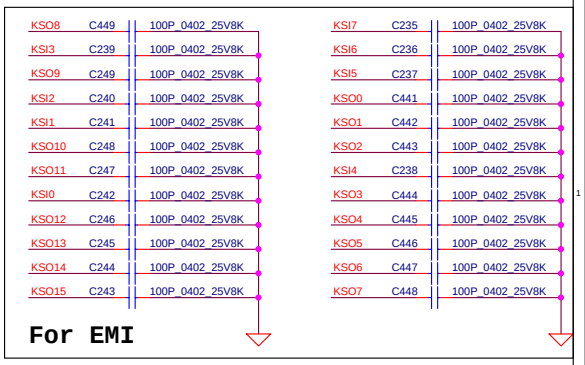


Regulator for ENE sensor

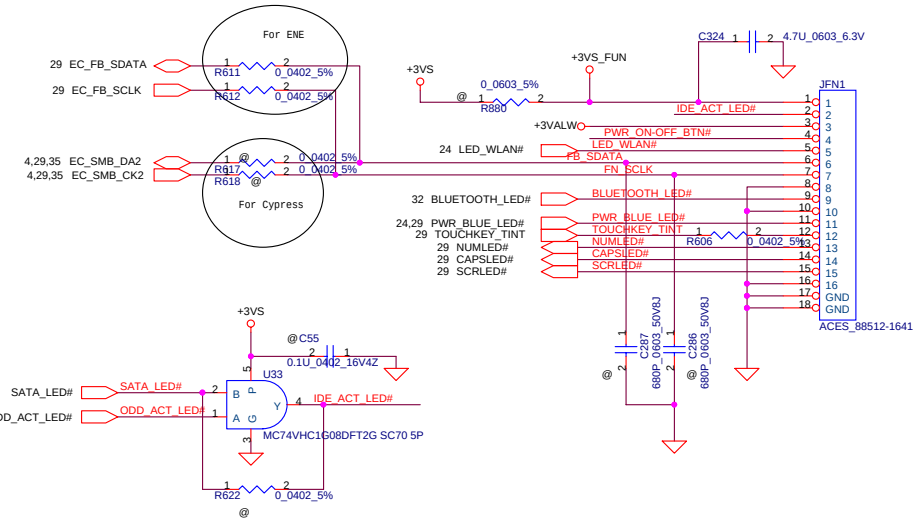


INT_KBD CONN.

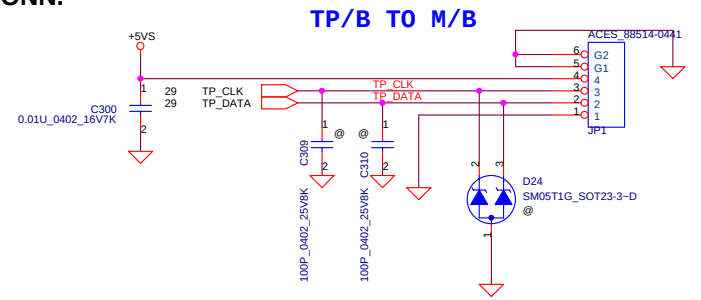




Function/B CONN.



Touch PAD/B CONN.



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **PWR_OK/BTN/TP**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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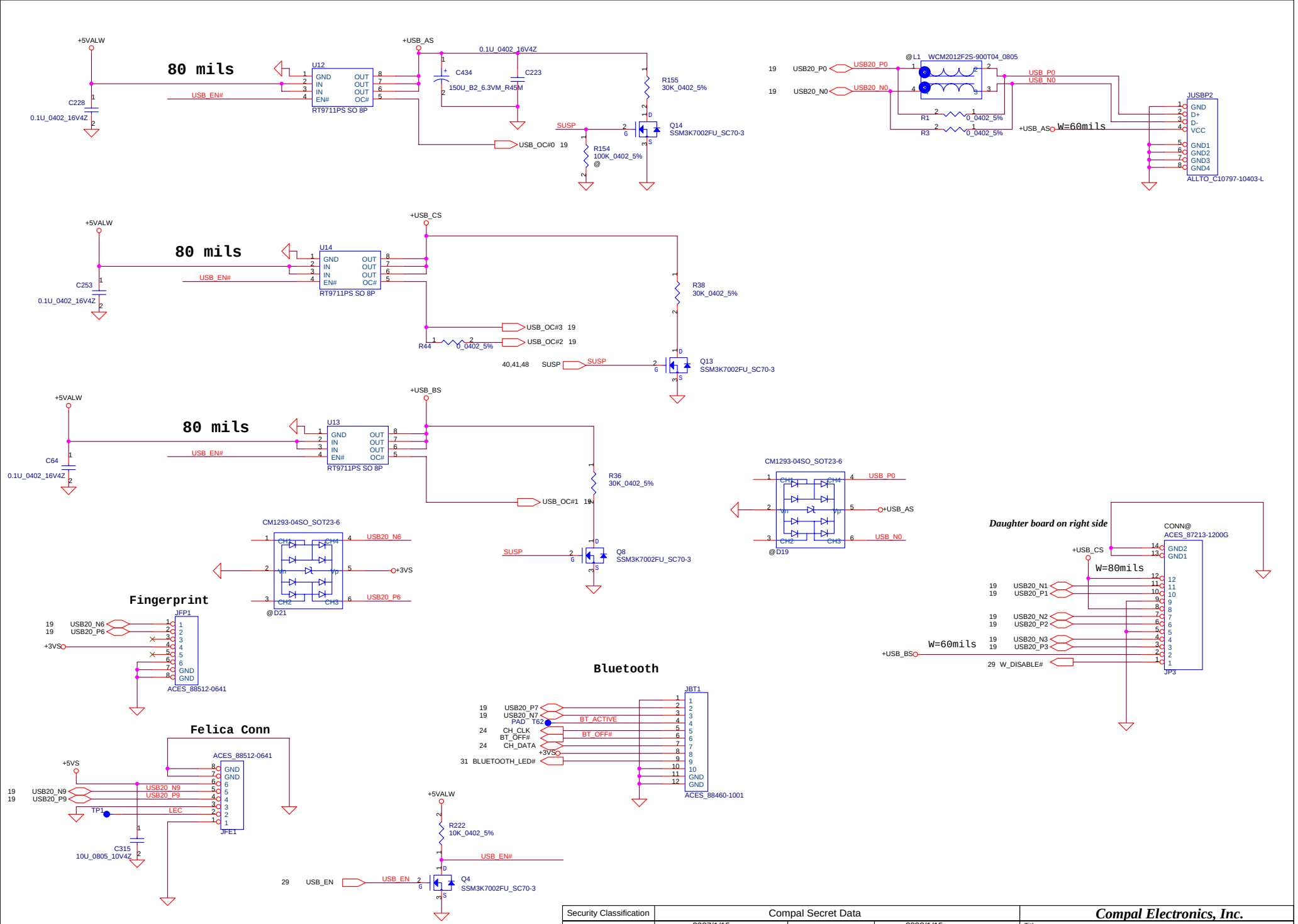


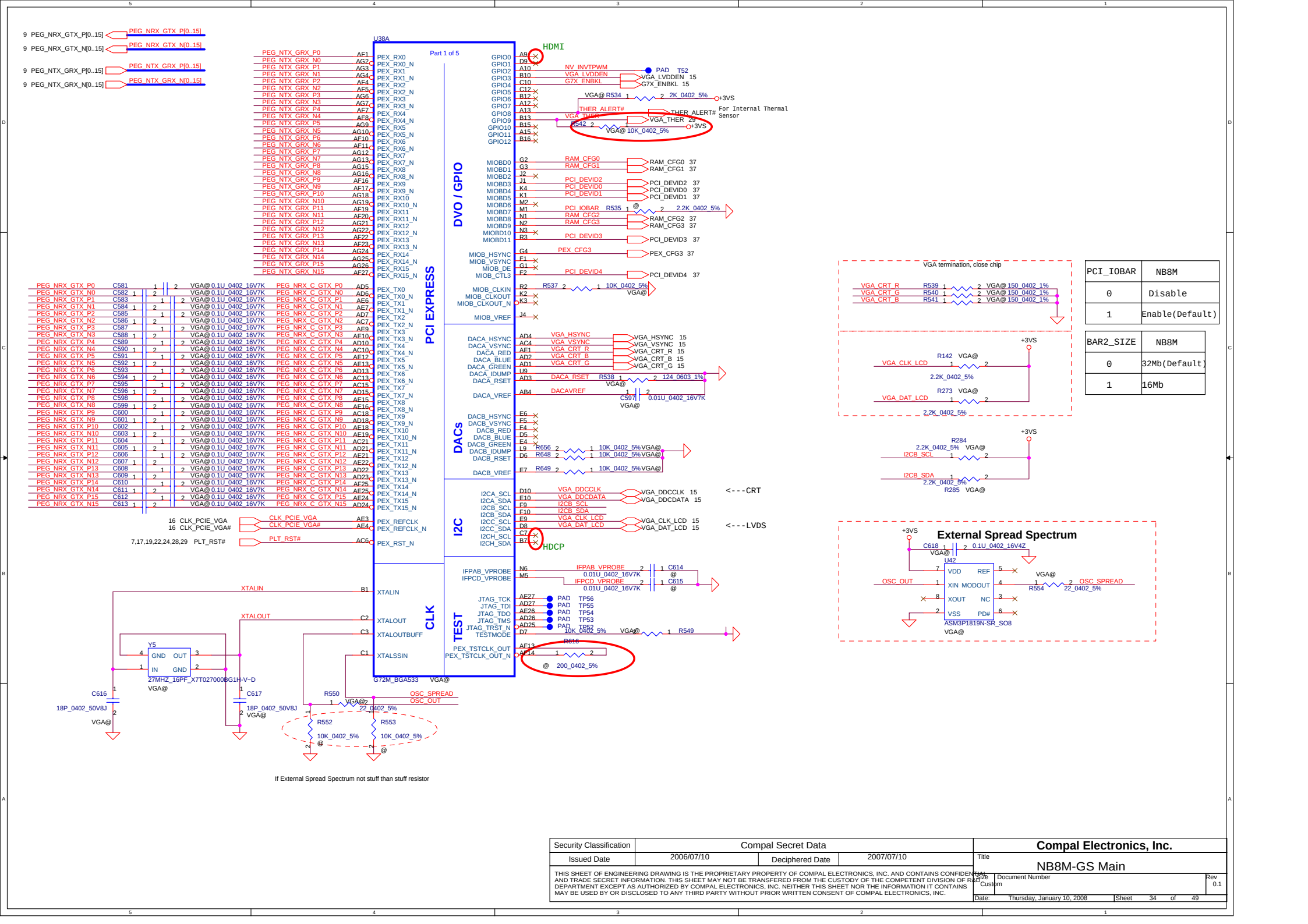
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **USB/BlueTooth/FP/Felcia**

Size	Document Number	Rev
Custom	LA-4231P	0.1

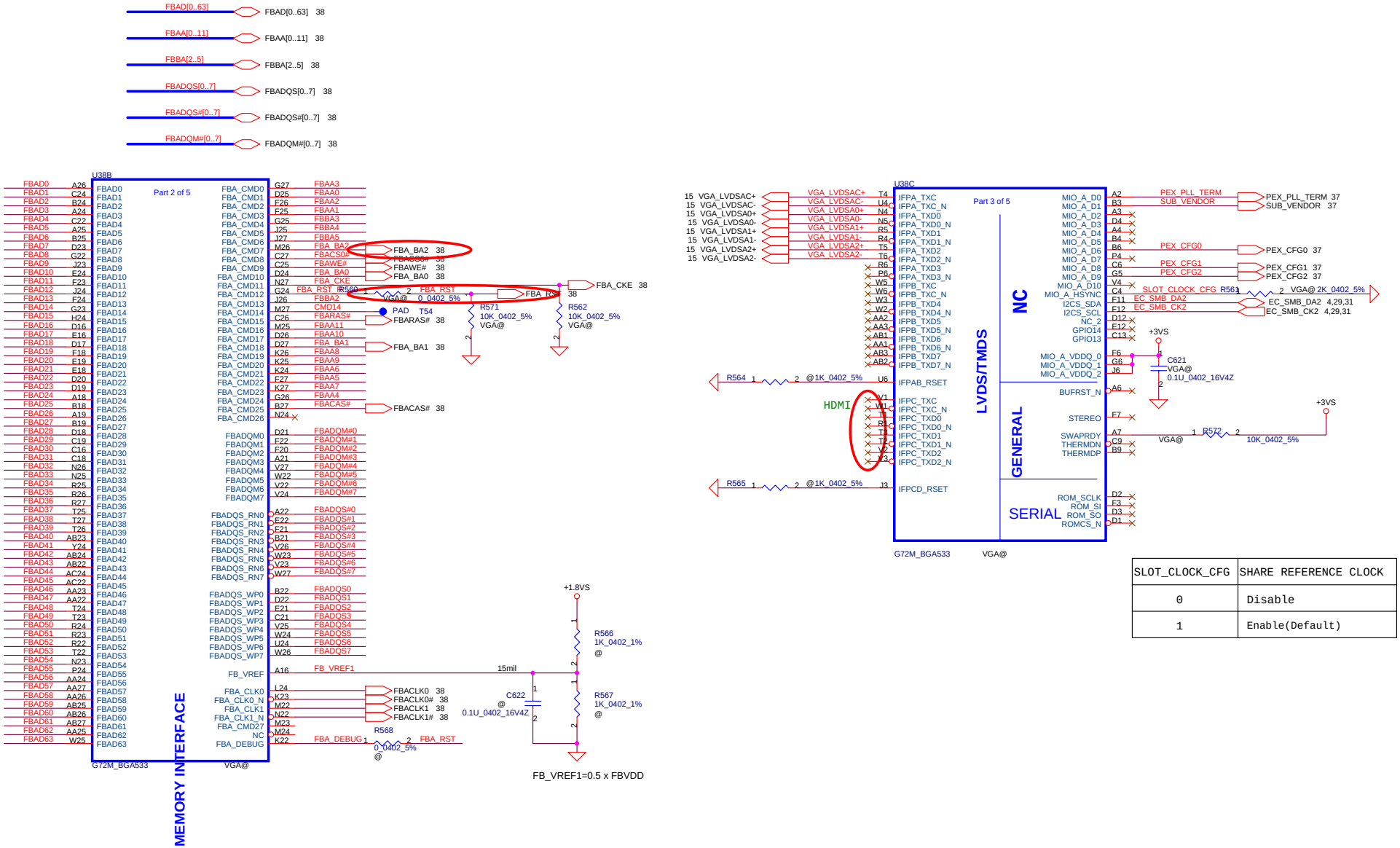
Date: Thursday, January 10, 2008 | Sheet 32 of 49



PCI_IOBAR	NB8M
0	Disable
1	Enable(Default)

BAR2_SIZE	NB8M
0	32Mb(Default)
1	16Mb

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/07/10	Deciphered Date	2007/07/10
Title	NB8M-GS Main		
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, January 10, 2008	Sheet 34 of 49		



SLOT_CLOCK_CFG	SHARE REFERENCE CLOCK
0	Disable
1	Enable(Default)

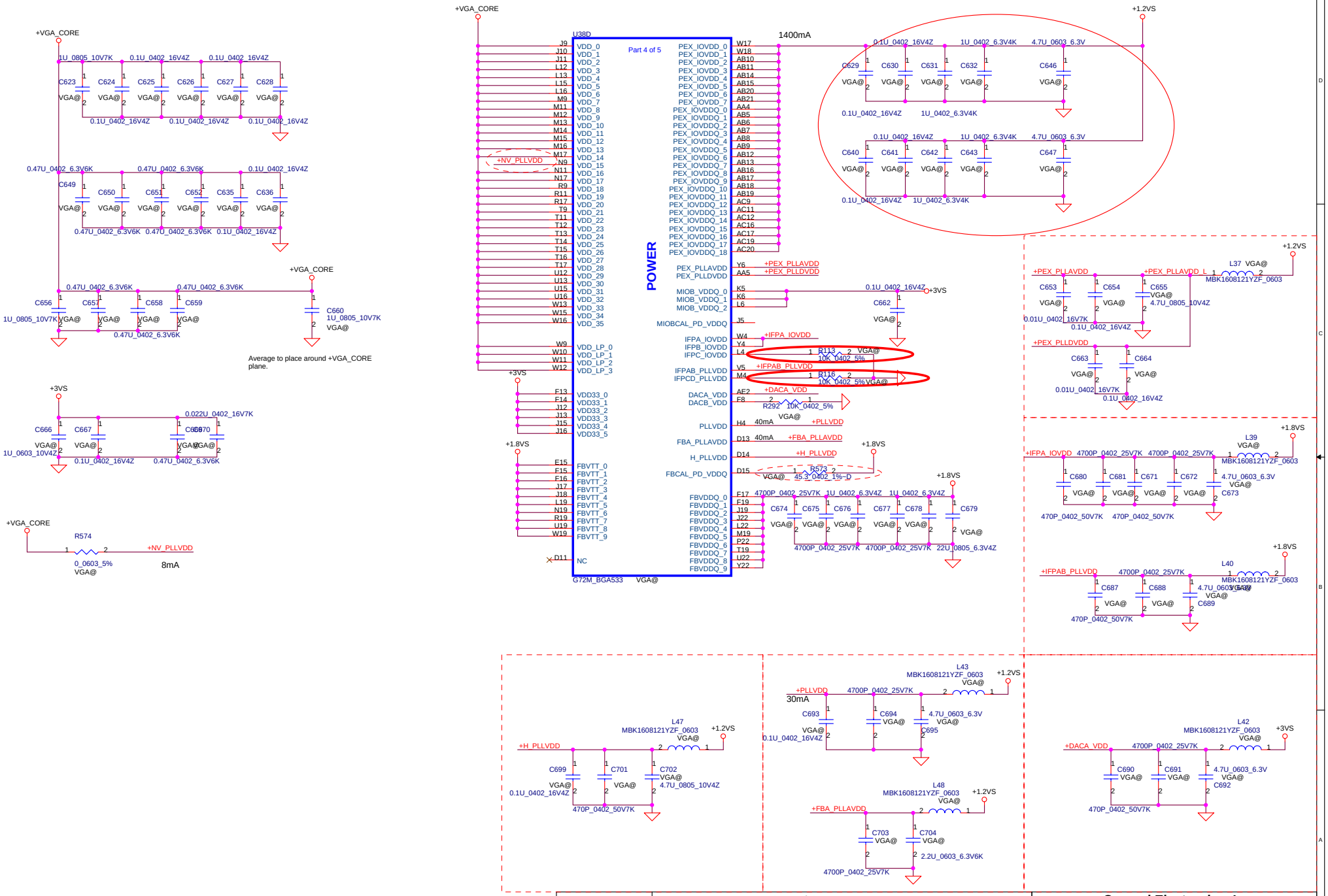
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS Memory

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 35 of 49



Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS Power

Size	Document Number	Rev
Custom		0.1

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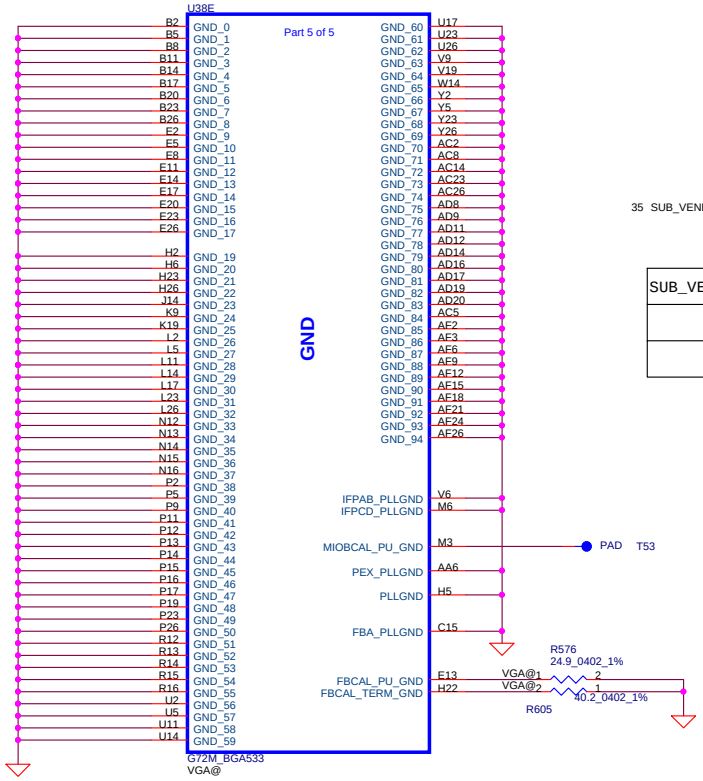
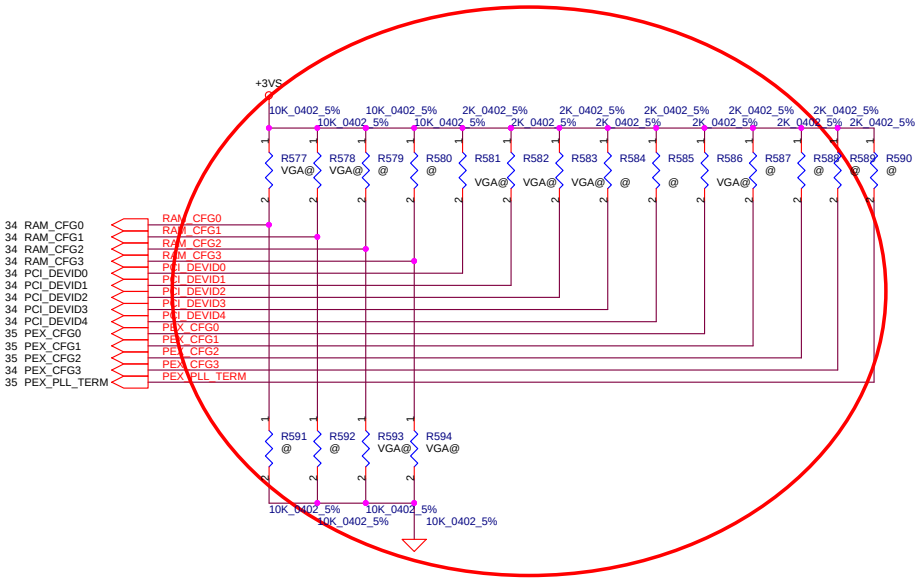


SUB_VENDOR	
0	N0 VIDEO BIOS ROM
1	BIOS ROM is present(Default)

STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIO_A_D1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIO_A_D0	PCI-E PLL termination 0---->Enable (Default) 1---->Disable	0	
PEX_CFG[3:0]	MIOAD [9,8,6] MIOBD_HSYNC	Recommended for G8x	0001	
RAM_CFG[3:0]	MIOAD0 MIOAD1 MIOAD8 MIOAD9	0001 ---> Qimonda 16Mx32 0010 ---> Hynix 16Mx32 0011 ---> Samsung 16Mx32	0011	
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8 NB8M-GS : 0X0427 NB8M-SE : 0X0428	0111 1000	
		G72MV-0x01D7 TBD/TBD	0111	



Bandwidth	RAM Type	Vendor	
FULL R17	32M R11	Samsung	R20, R19
HALF R12	16M R16	Hynix	R18, R19
		Infineon	R18, R21

Package		
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS GND & STRAP

Size	Document Number	Rev
Custom		0.1

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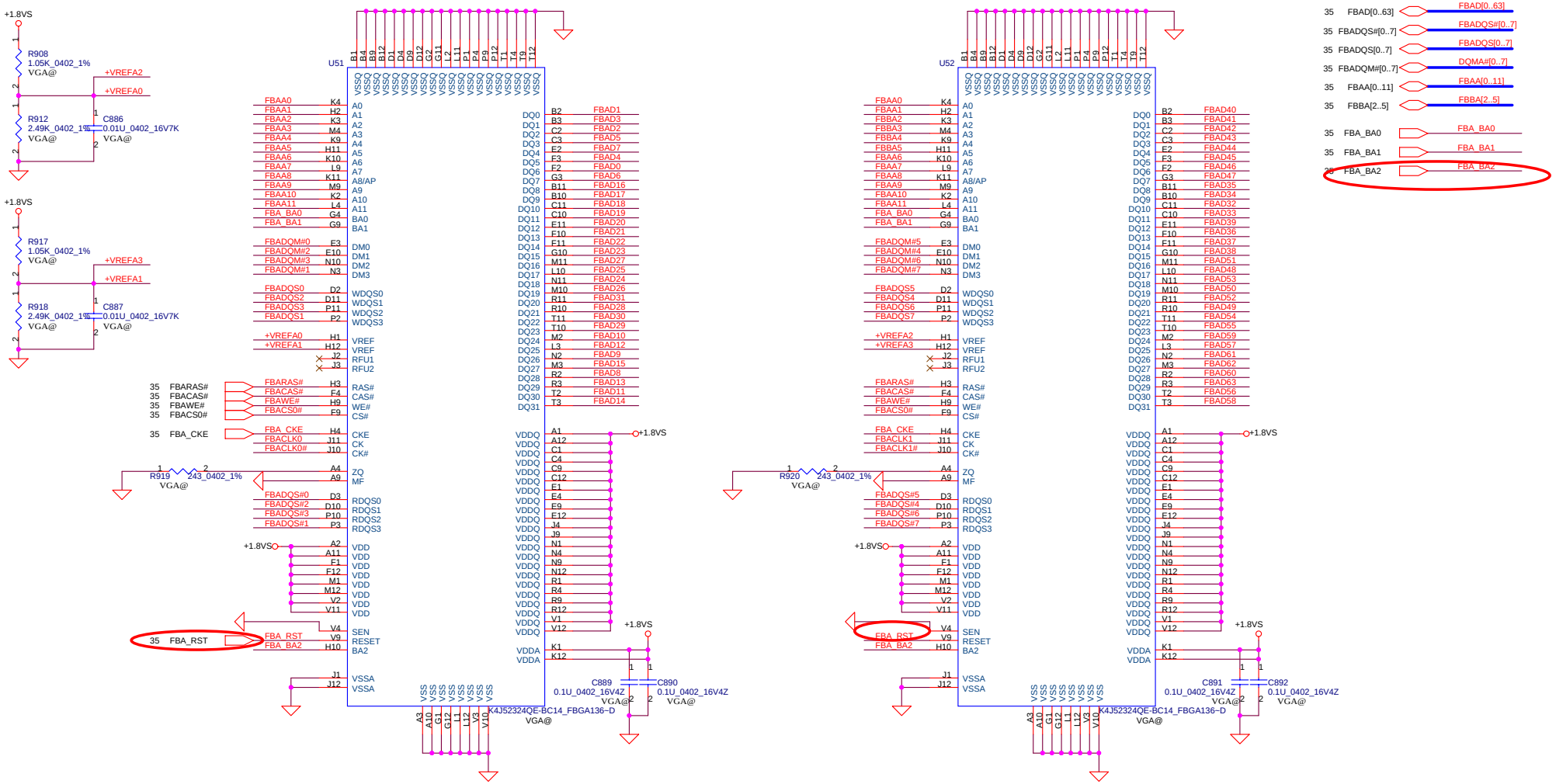
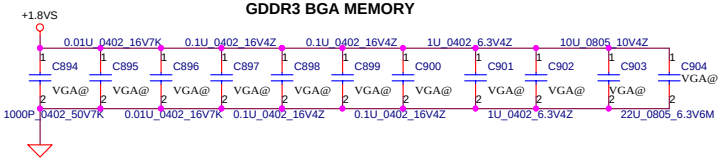
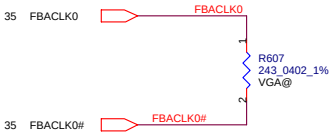
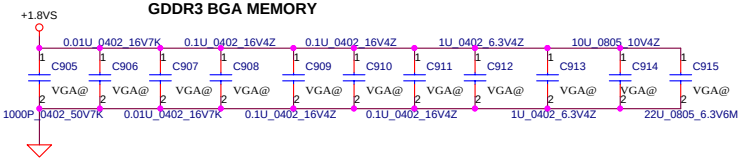


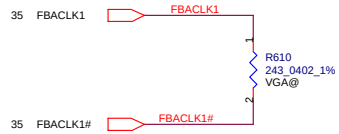
GDDR3 BGA MEMORY





GDDR3 BGA MEMORY





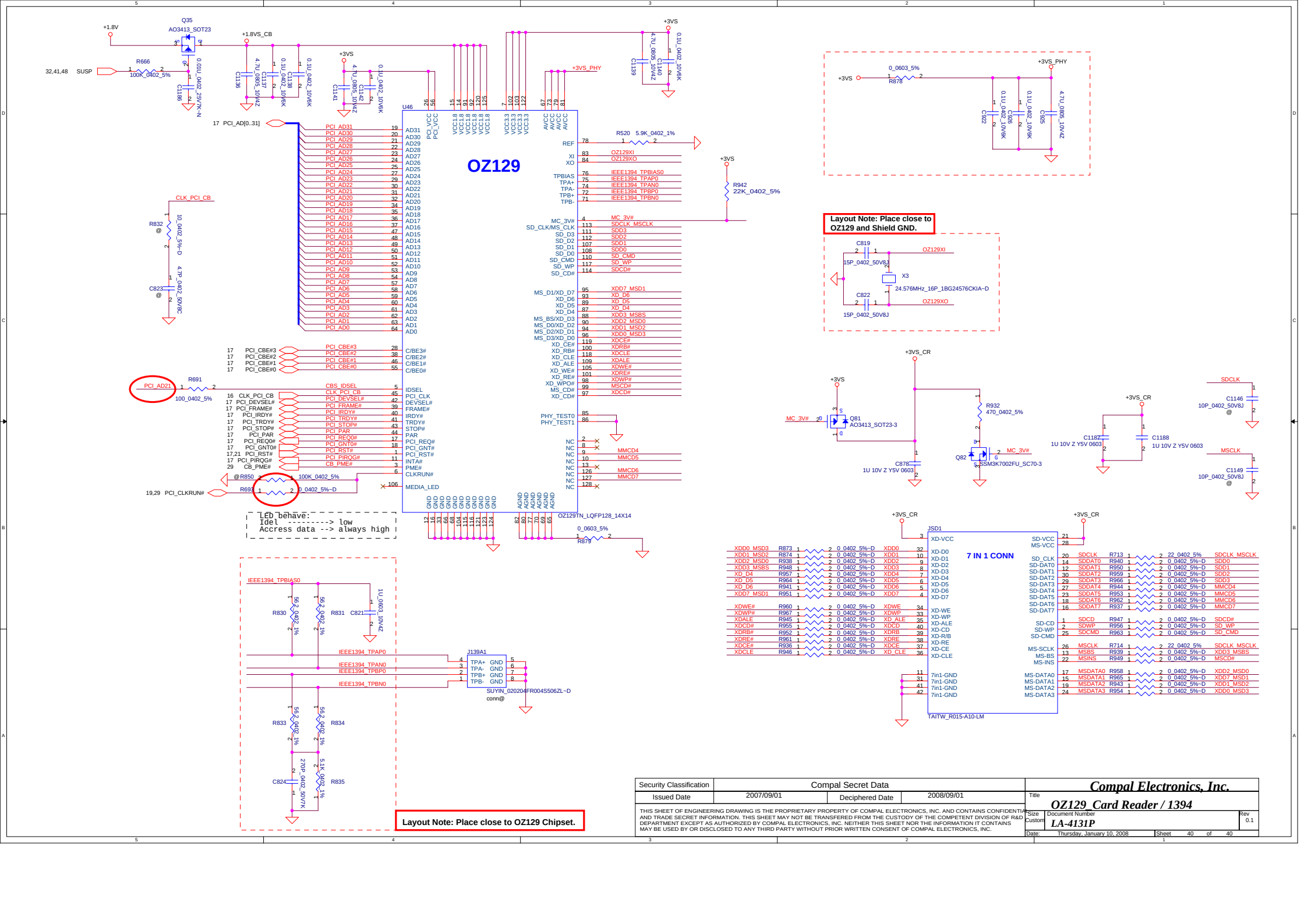
Security Classification	Compal Secret Data		
Issued Date	2007/02/12	Deciphered Date	2008/02/12

Compal Electronics, Inc.

Title: **VRAM GDDR3 A**

Size | Document Number: *LA-4231P* | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 38 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/09/01	Deciphered Date	2008/09/01

Compal Electronics, Inc.

Title: *OZ129_Card Reader / 1394*

Size	Document Number	Rev
Custom	LA-4131P	0.1

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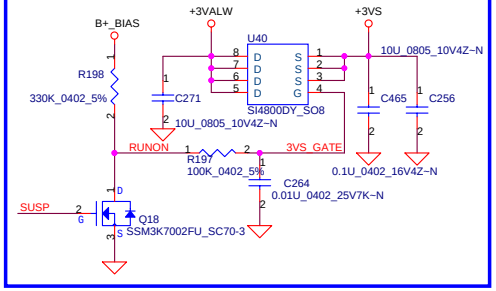
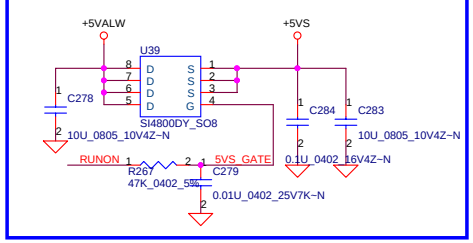
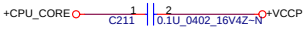
+3VALW to +3VS Transfer

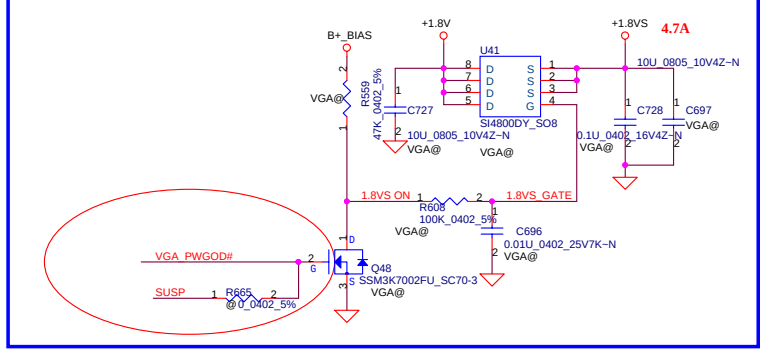


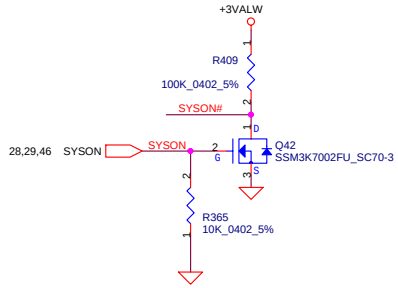
+5VALW to +5VS Transfer

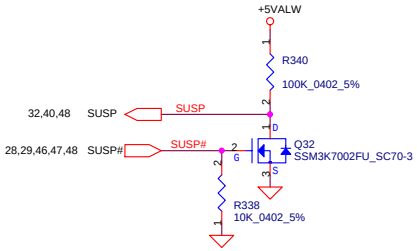


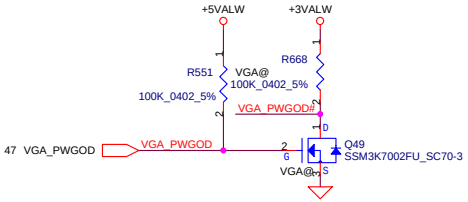


+1.8V to +1.8VS Transfer



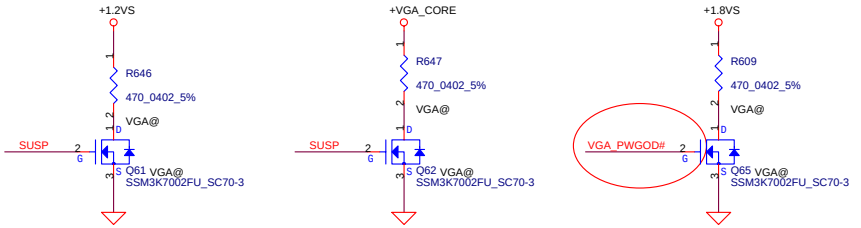




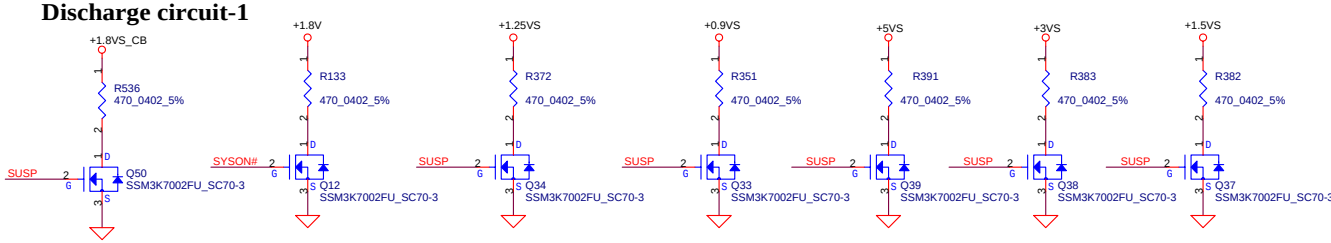


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

VGA Discharge circuit



Discharge circuit-1



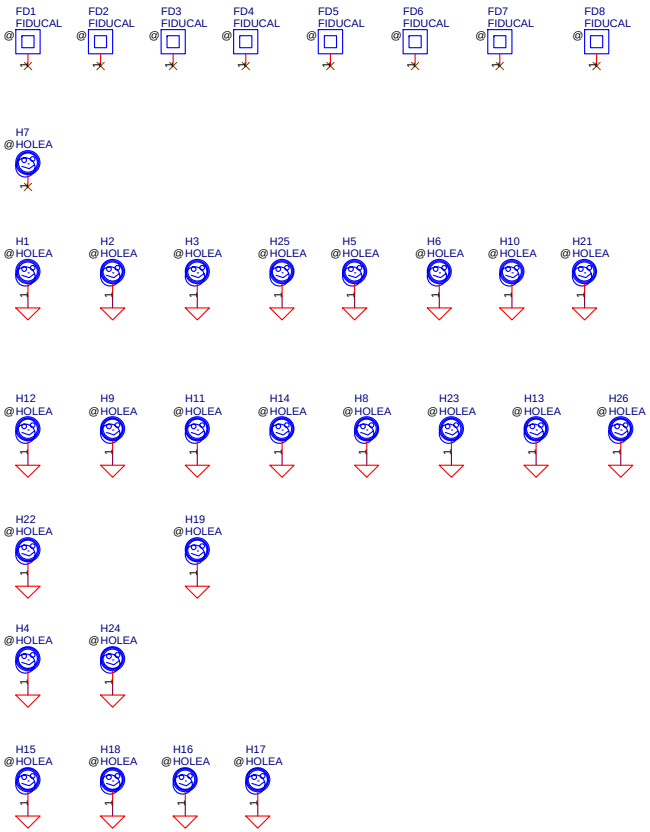
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size: Custom | Document Number: **LA-4231P** | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 41 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Screws**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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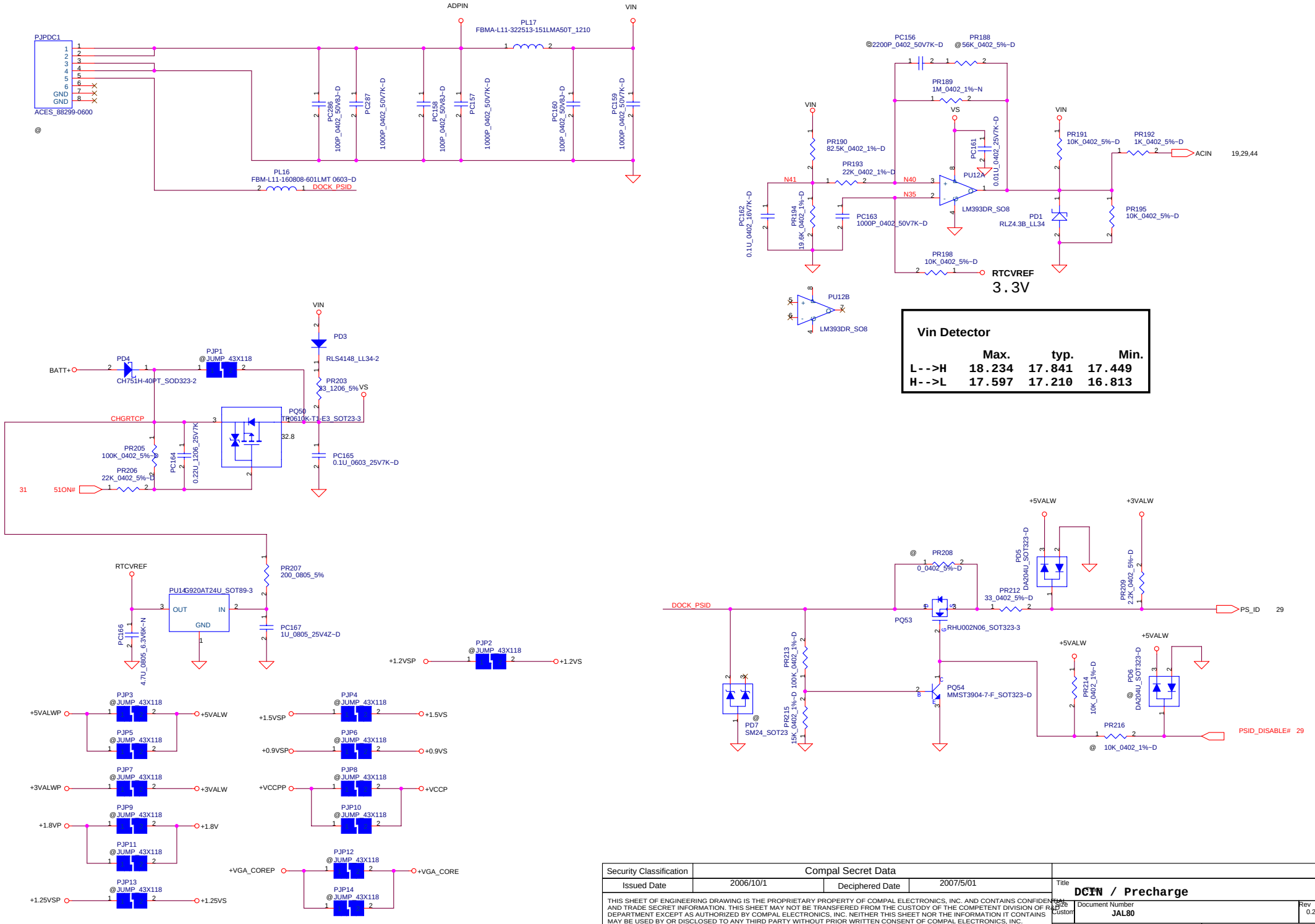


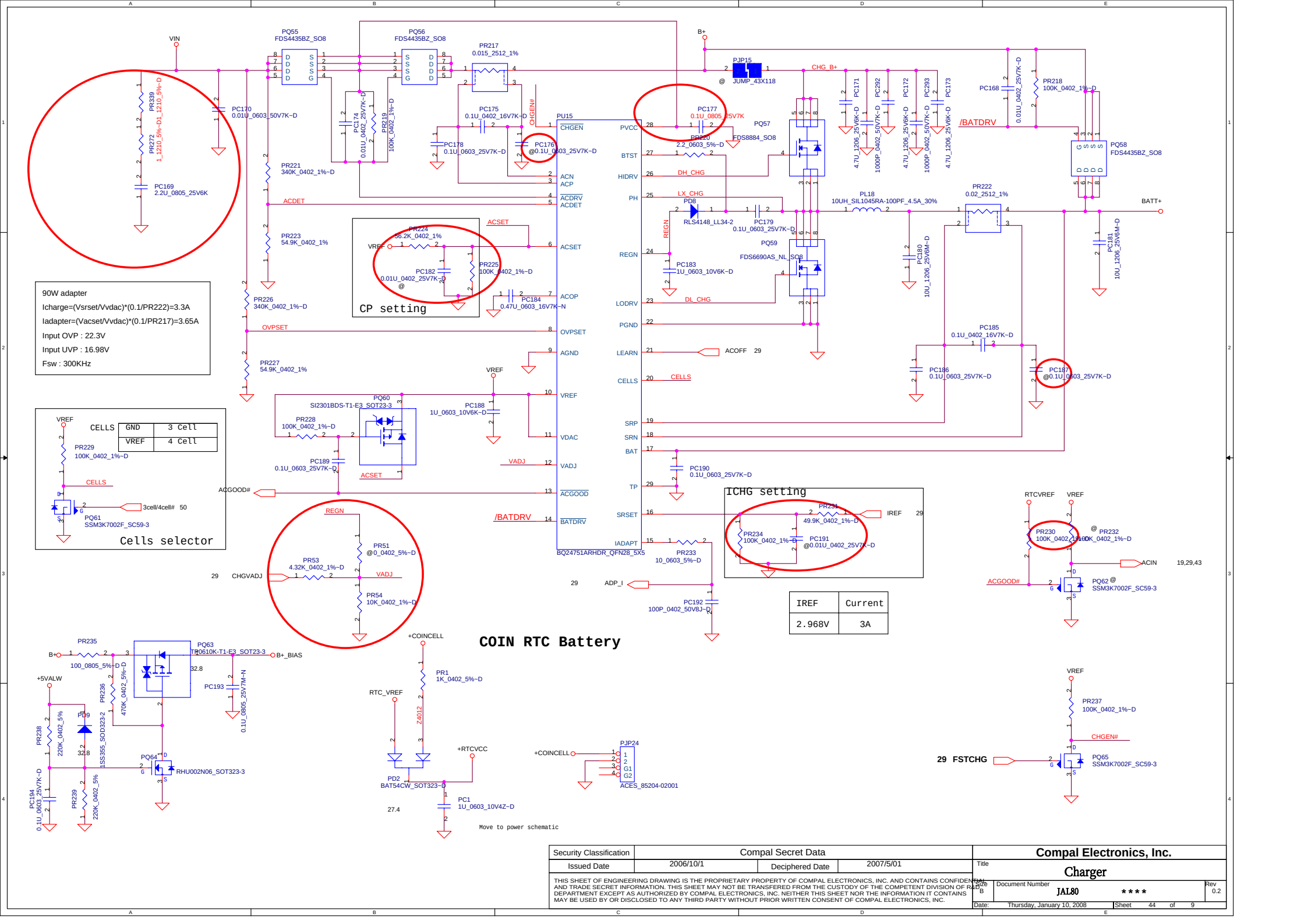
Vin Detector

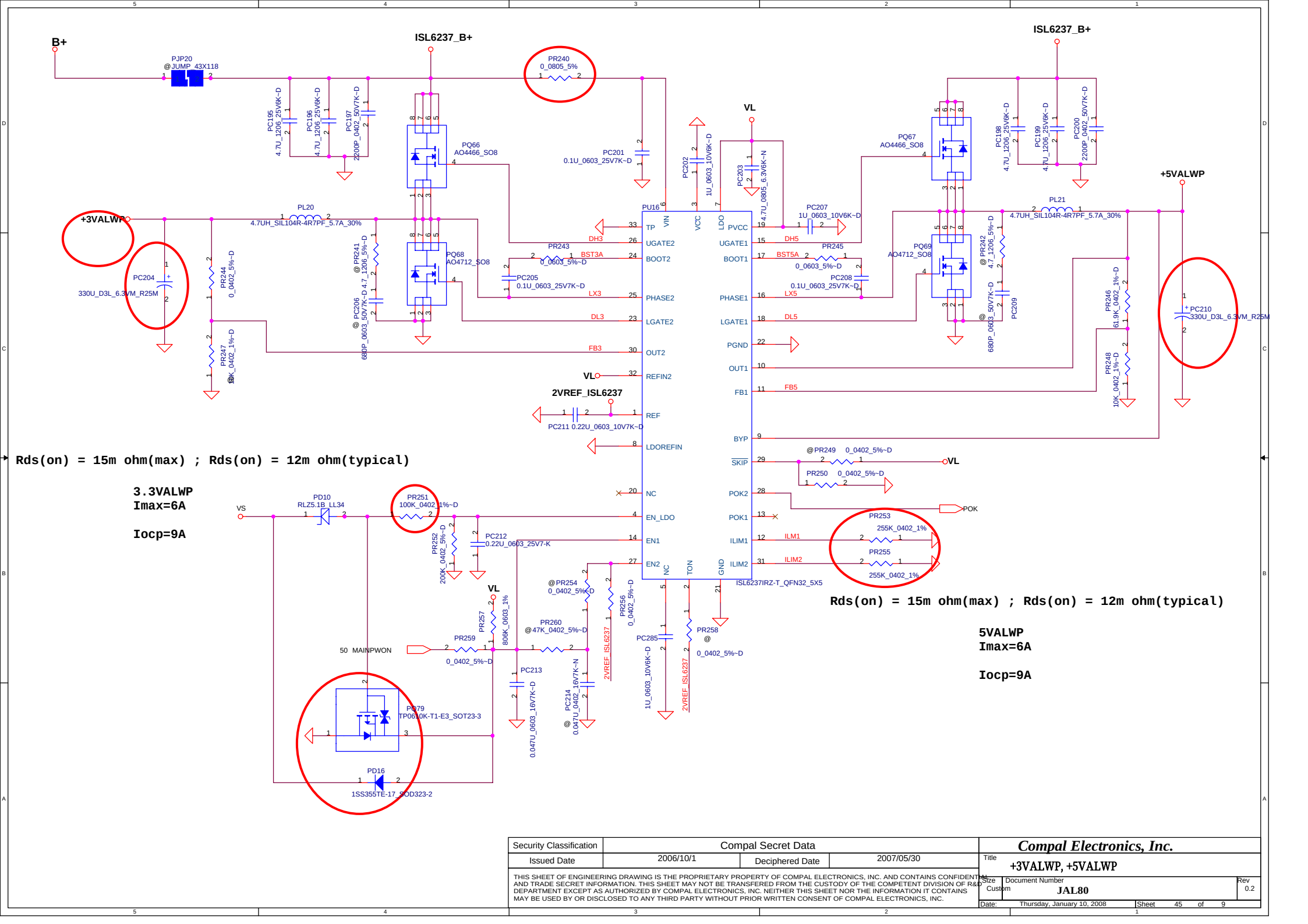
	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title: **DCIN / Precharge**

Size: Custom	Document Number: JAL80	Rev: 0.2
Date: Thursday, January 10, 2008	Sheet 43 of 9	

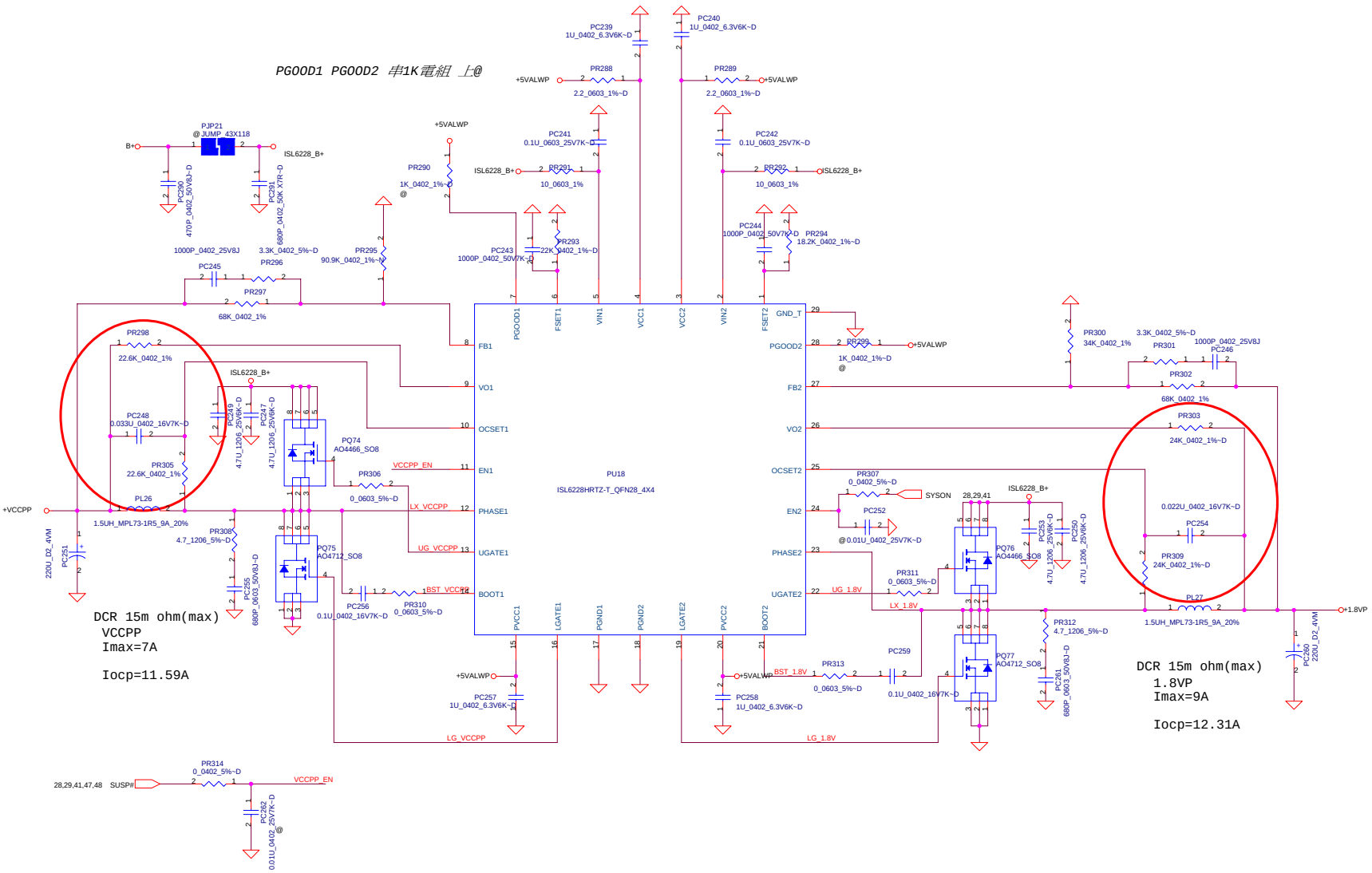

90W adapter
Icharge=(Vsrset/Vvdac)*(0.1/PR222)=3.3A
Iadapter=(Vacset/Vvdac)*(0.1/PR217)=3.65A
Input OVP : 22.3V
Input UVP : 16.98V
Fsw : 300KHz
CP setting
Cells selector
CELLS GND 3 Cell
VREF 4 Cell
ICHG setting
IREF Current
2.968V 3A
COIN RTC Battery
Move to power schematic
BQ24751ARHDR_QFN28_5X5
/BATDRV
CHG_B+
BATT+
ACIN 19,29,43
29 FSTCHG
Security Classification Compal Secret Data
Issued Date 2006/10/1 Deciphered Date 2007/5/01
Compal Electronics, Inc.
Title Charger
Size B
Document Number JAL80 ****
Rev 0.2
Date: Thursday, January 10, 2008
Sheet 44 of 9



Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

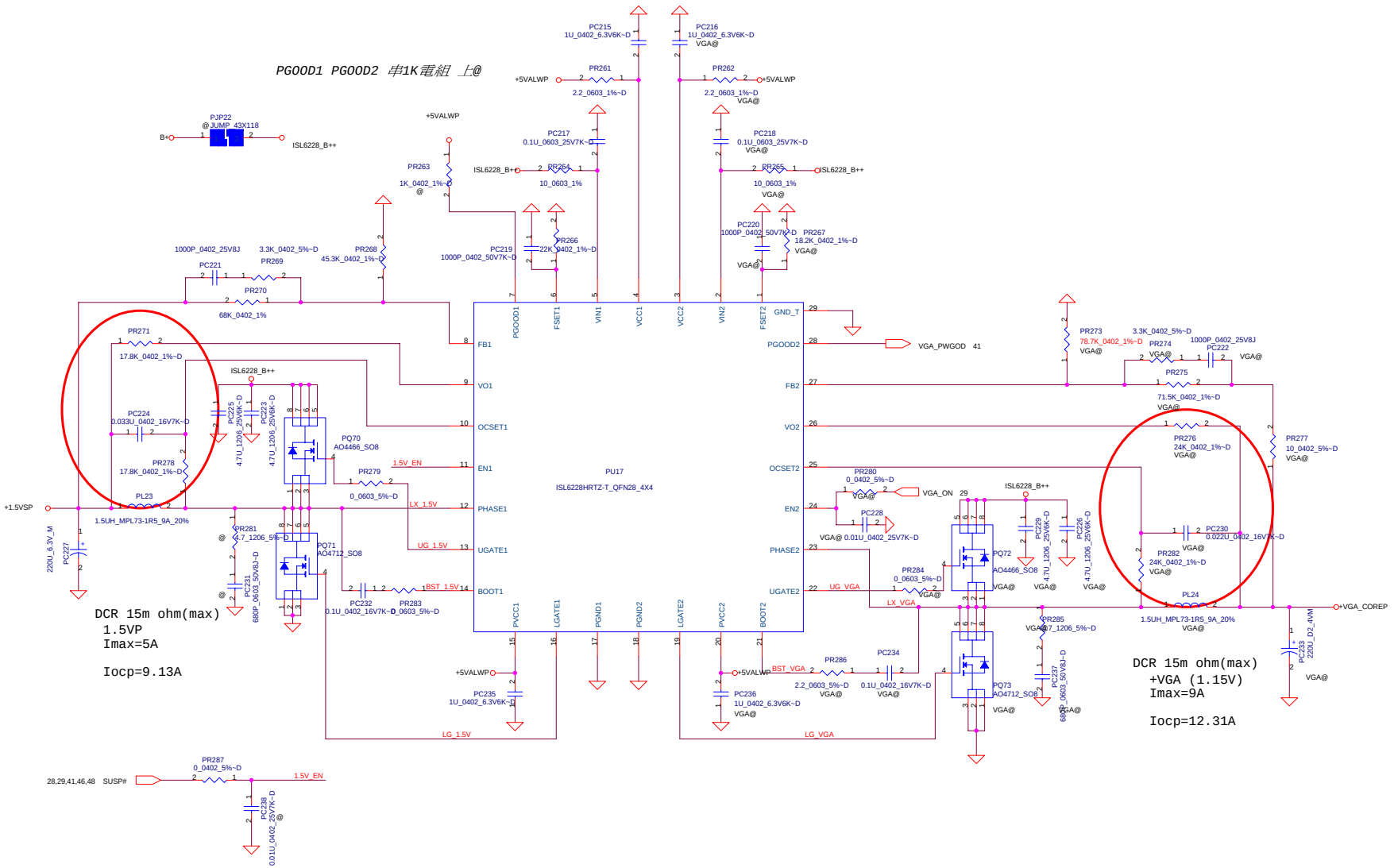
Compal Electronics, Inc.

Title	+3VALWP, +5VALWP		
Size	Custom	Document Number	JAL80
Rev	0.2		
Date:	Thursday, January 10, 2008	Sheet	45 of 9



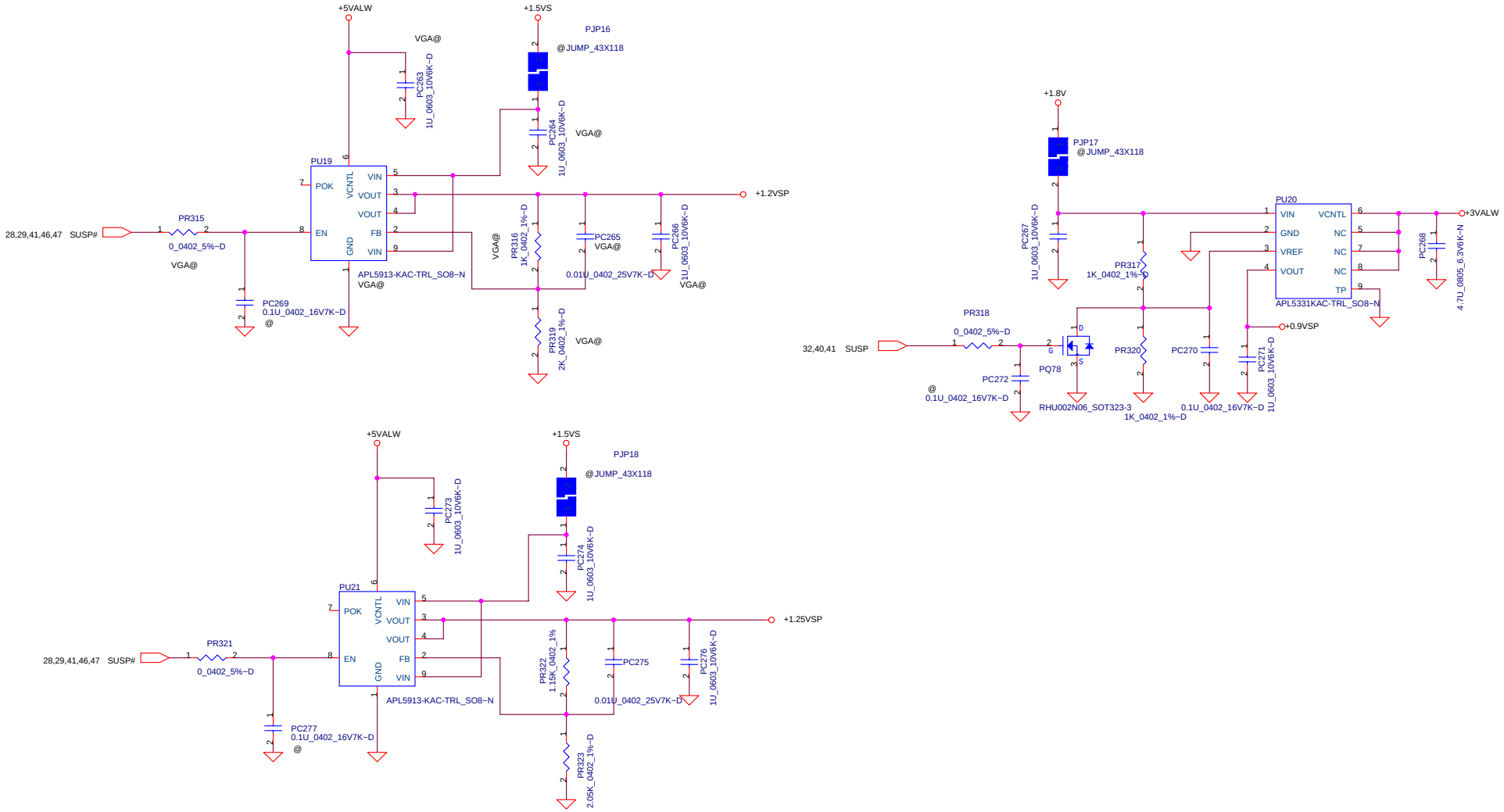
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	+1.8VP/+VCCPP		
Size	Document Number JAL80		Rev 0.2
Date: Thursday, January 10, 2008		Sheet 46 of 9	



Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	+1.5VP/+VGA		
Size	Document Number	JAL80	Rev 0.2
Date: Thursday, January 10, 2008	Sheet 47 of 9		



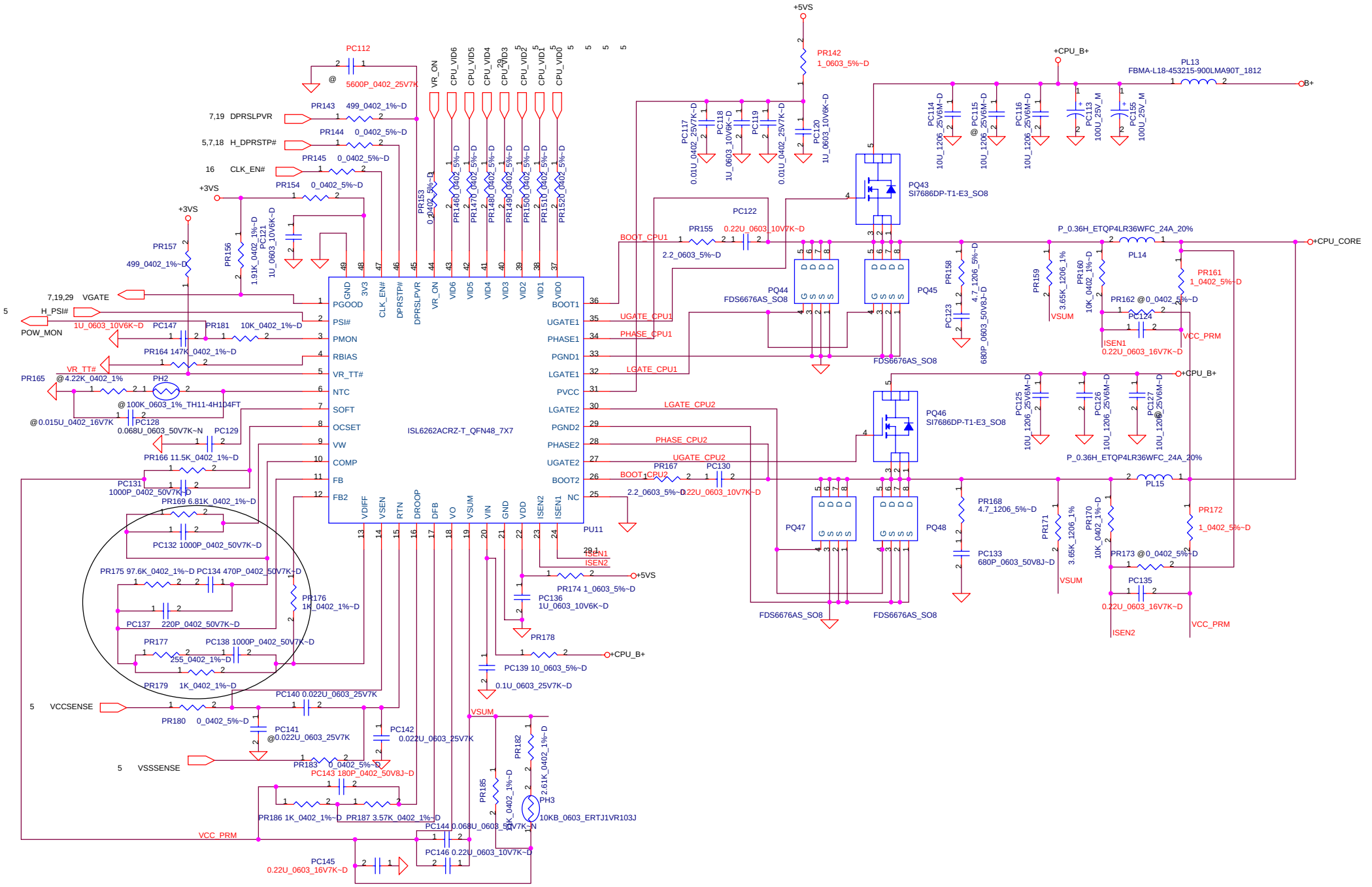
Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: **+1.25VSP / +0.9VSP/ +1.2VSP**

Size	Document Number	Rev
Custom	JAL80	0.2

Date: Thursday, January 10, 2008 Sheet 48 of 9



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

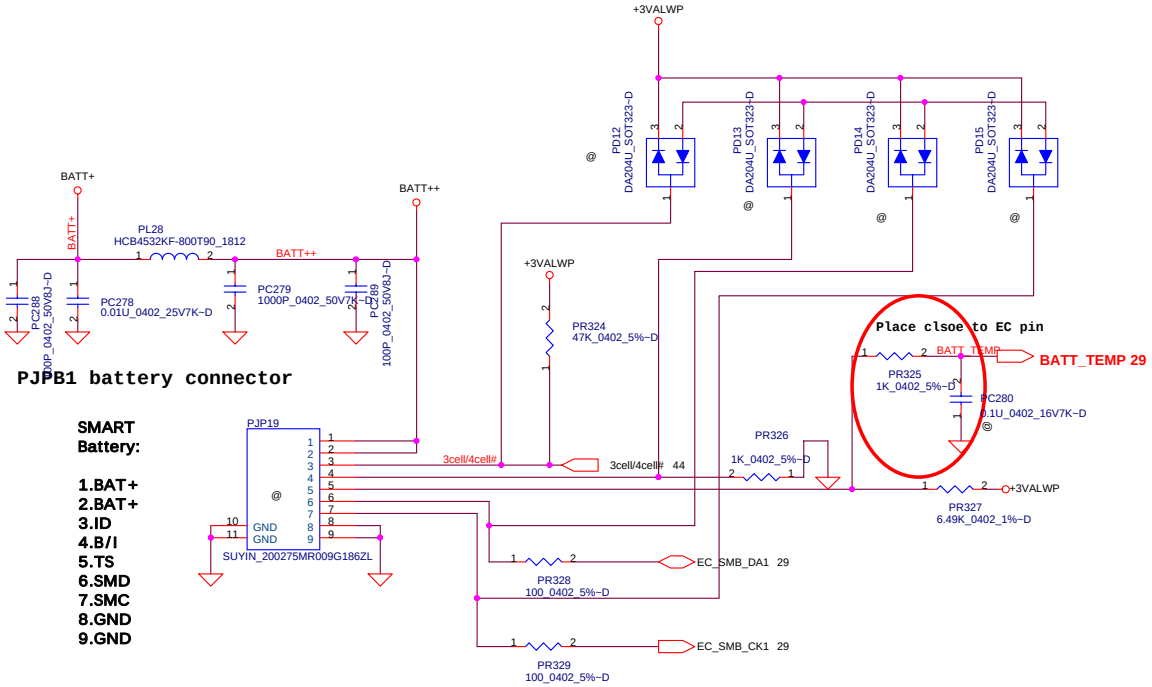
Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom	LA-4121P	0.1

Date: Thursday, January 10, 2008 | Sheet 49 of 9

Battery Connect/OTP



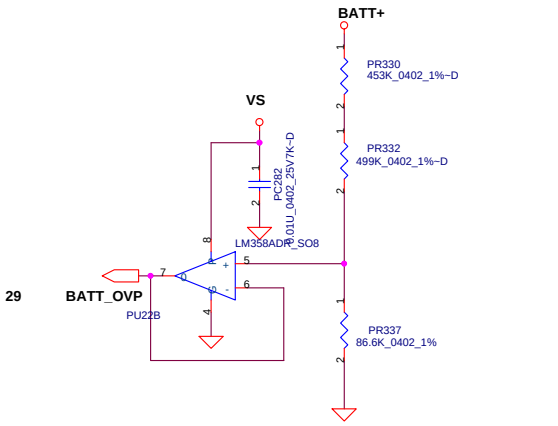
PJPB1 battery connector

SMART Battery:

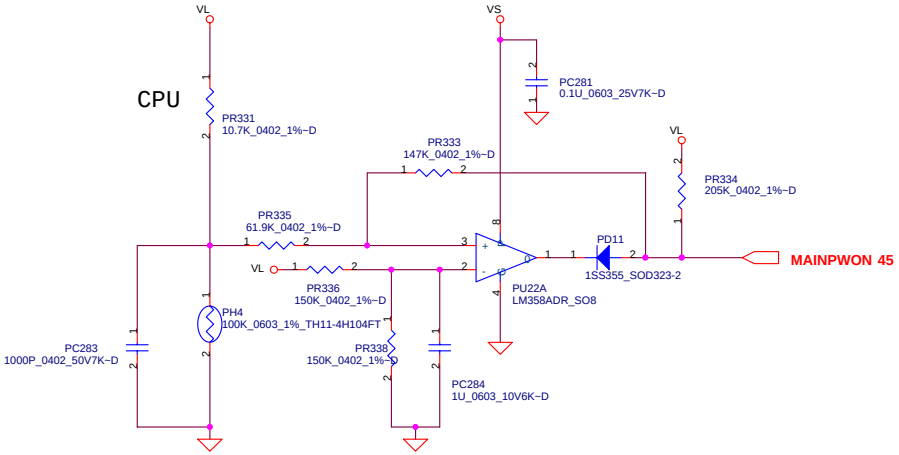
1. BAT+
2. BAT+
3. ID
4. B/I
5. TS
6. SMD
7. SMC
8. GND
9. GND

CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title	BATTERY CONN		
Size	Custom	Document Number	JAL80
Rev	0.2		
Date:	Thursday, January 10, 2008	Sheet	50 of 9

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-OZ129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to OZ129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ BlueTooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Frequence Decoupling Capacitance	C195 change to C1150~C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
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Compal Electronics, Inc.

Title: EE PIR-1

Size: Custom | Document Number: LA-4231P | Rev: 0.1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PQ79 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	44	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
3	49	CPU_CORE	07/12/26	COMPAL	Increase Resistor 0ohm on CPU_CORE high side gate for EMI request	ADD PR163 PR184	
4	45	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location is wrong	DEL PL19	
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Compal Electronics, Inc.

Title: PW PIR-1

Size: Custom | Document Number: LA-3682P | Rev: 0.1

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