

# Compal Confidential

## KBYF0 Schematics Document

AMD Griffin Processor with RS780M+SB700

(With ATI MXM/B)

2009-01-22

REV: 0.3

ZZZ1



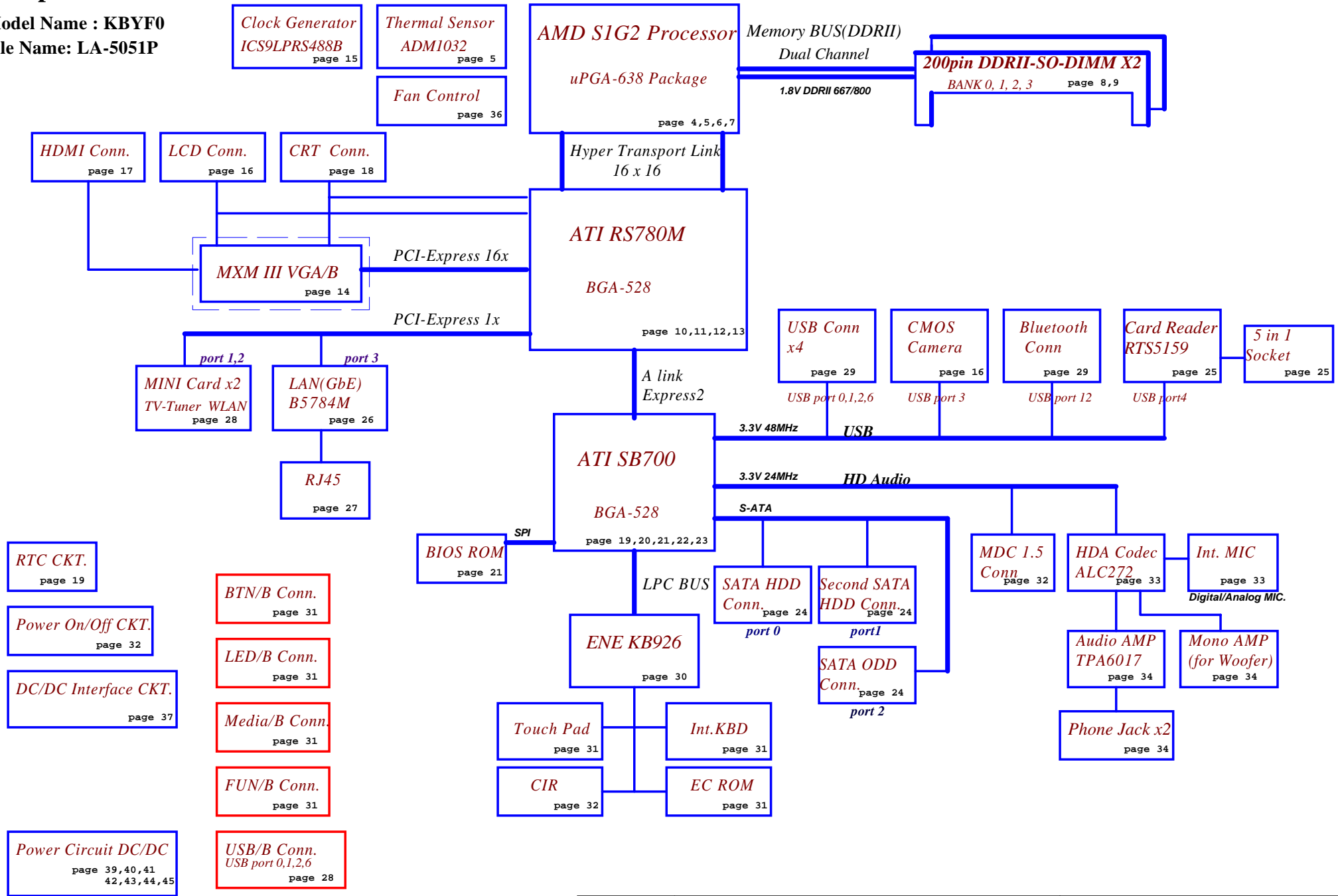
PCB

DA60000B600-\*

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				Cover Page		
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Model Name : KBYF0  
File Name: LA-5051P



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE_0	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.05V switched power rail	ON	OFF	OFF
+1.2V_HT	1.25V switched power rail	ON	OFF	OFF
+NB_CORE	1.0V~1.1V switched power rail for NB VDDC	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA and MXM/B	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

No PCI device

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	CPUSB	1001 101X b
MXM.GMT G781-1	1001 101X b		

## EC SM Bus2 address

## SB700 SM Bus 0 address

Device	Address	Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb	Lan	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Minicard			
Minicard			

## SB700 SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
* 2	0.3 0.4 1.0
3	
4	
5	
6	
7	

## BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@

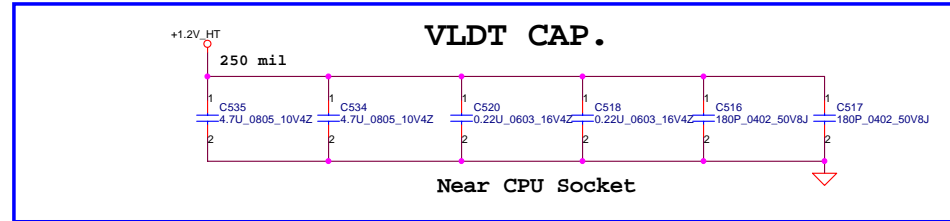
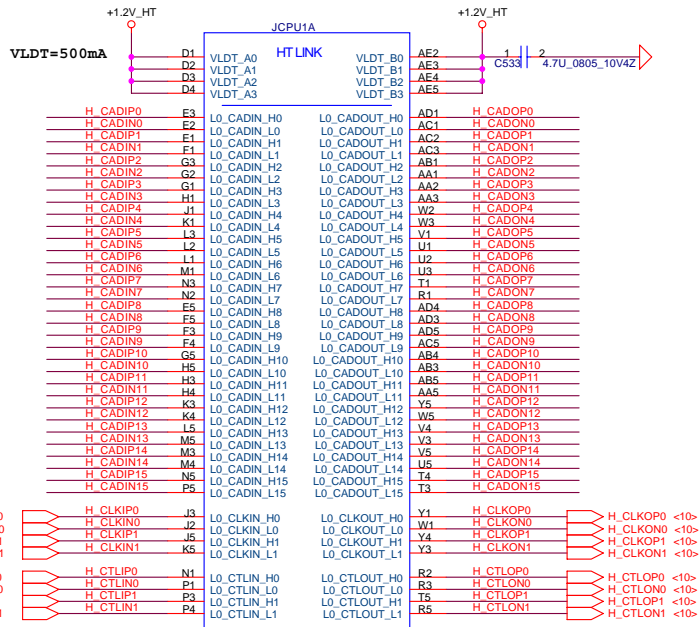
## PROJECT ID Table

Board ID	PROJECT
0	KBK0 (SJM70)
1	KBYF0 (SJV70)
2	
3	
4	
5	
6	
7	

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				Notes List		
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 <10> H\_CADIN[0..15] H\_CADIN[0..15]

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 H\_CADON[0..15] H\_CADON[0..15] <10>



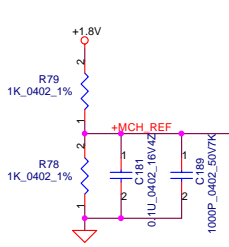
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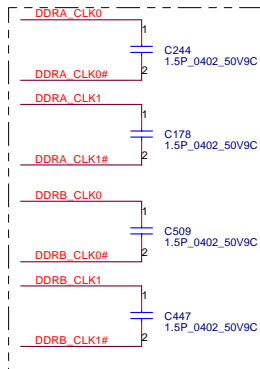
6090022100G\_B  
 Athlon 64 S1  
 Processor Socket  
 CONNN@

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				AMD CPU SIG2 HT I/F		
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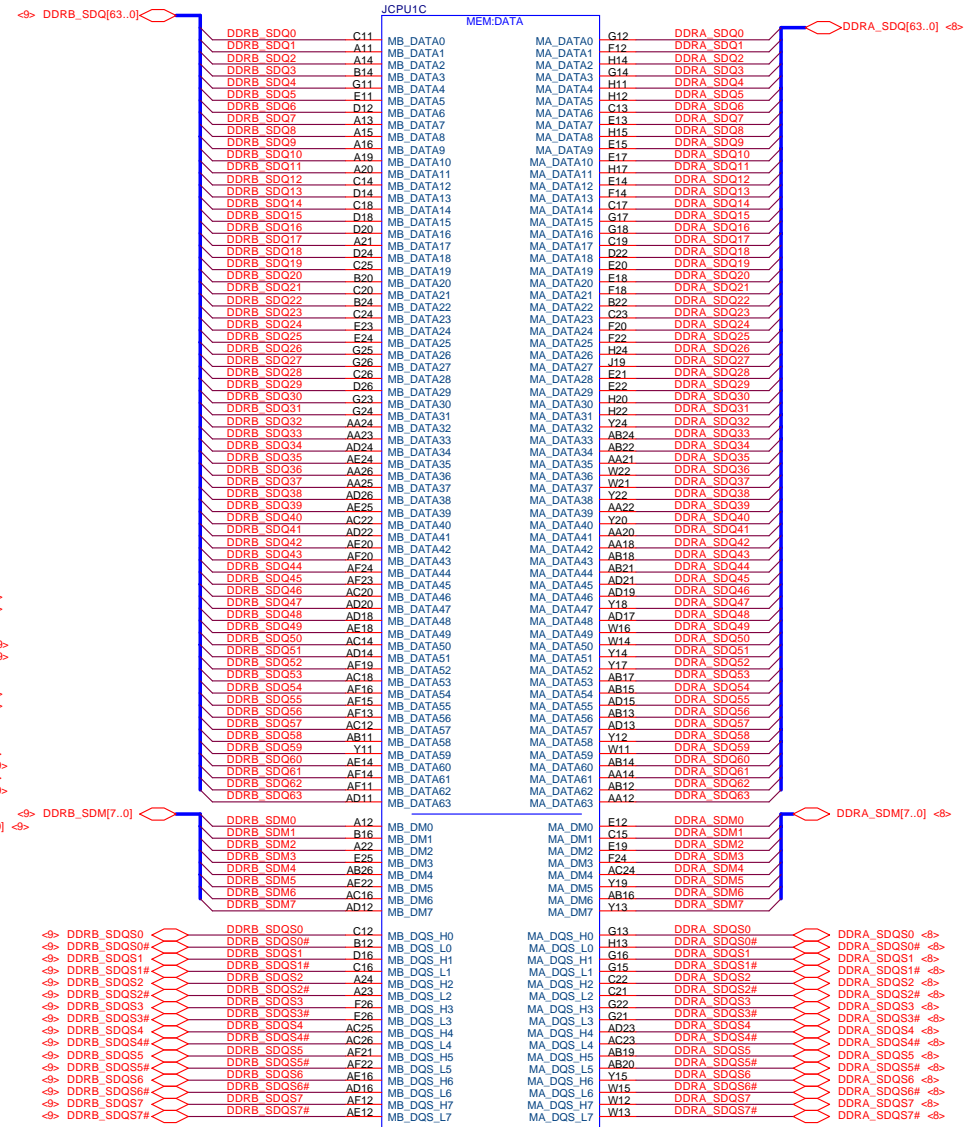
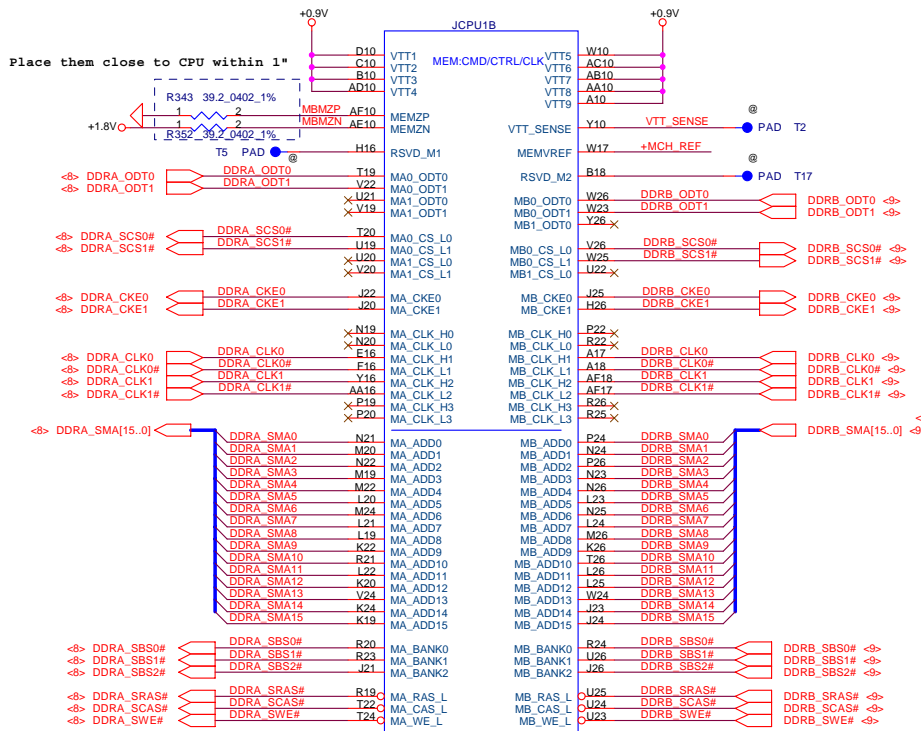
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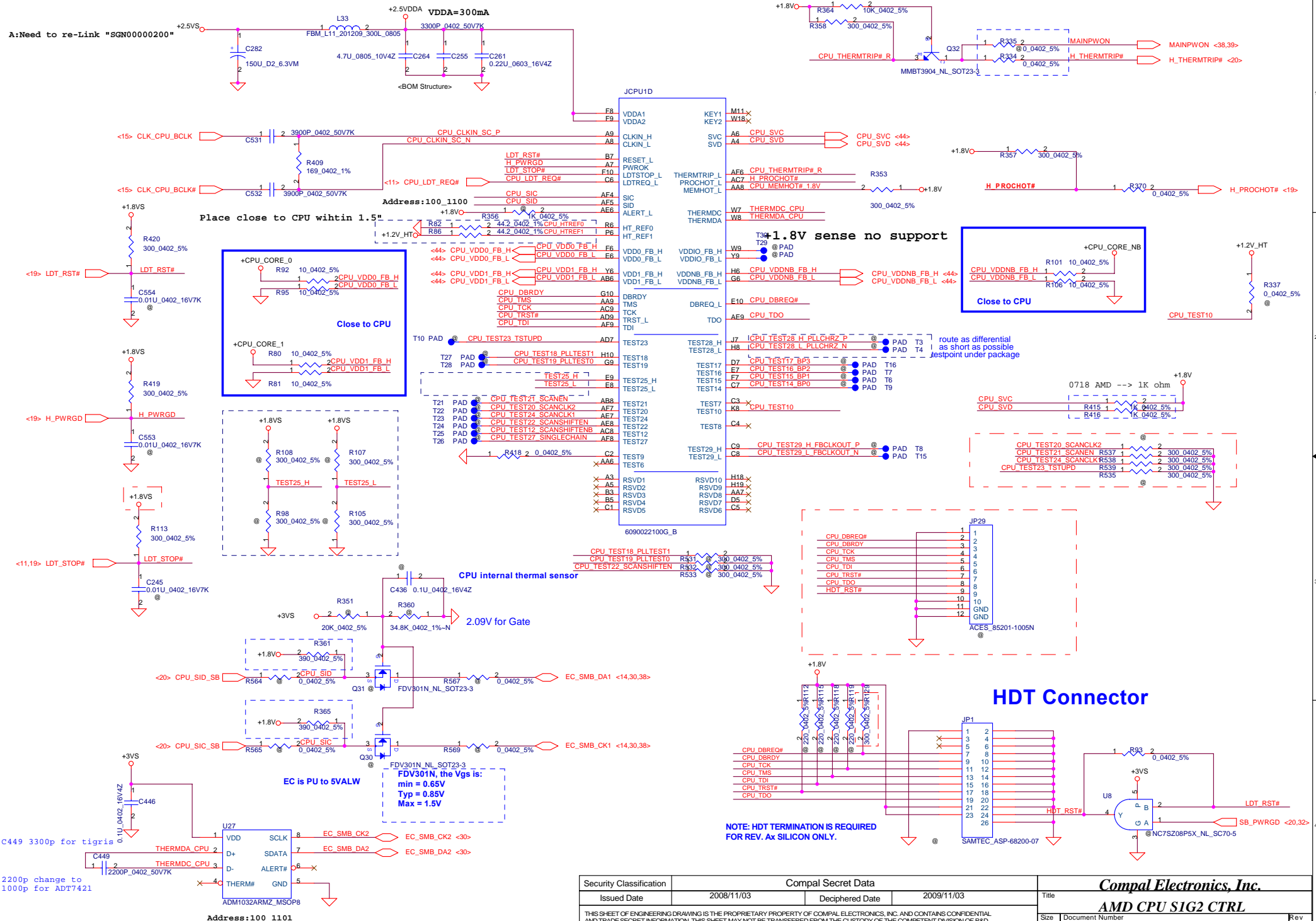


PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



Place them close to CPU within 1"

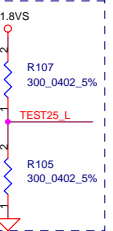
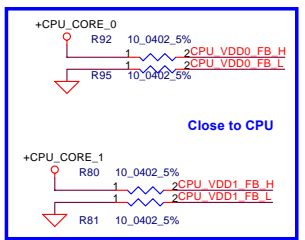




A:Need to re-Link "SGN0000200"

Place close to CPU within 1.5"

Address:100\_1100



CPU internal thermal sensor

2.09V for Gate

EC is PU to SVALW  
FDV301N, the Vgs is:  
min = 0.65V  
Typ = 0.85V  
Max = 1.5V

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

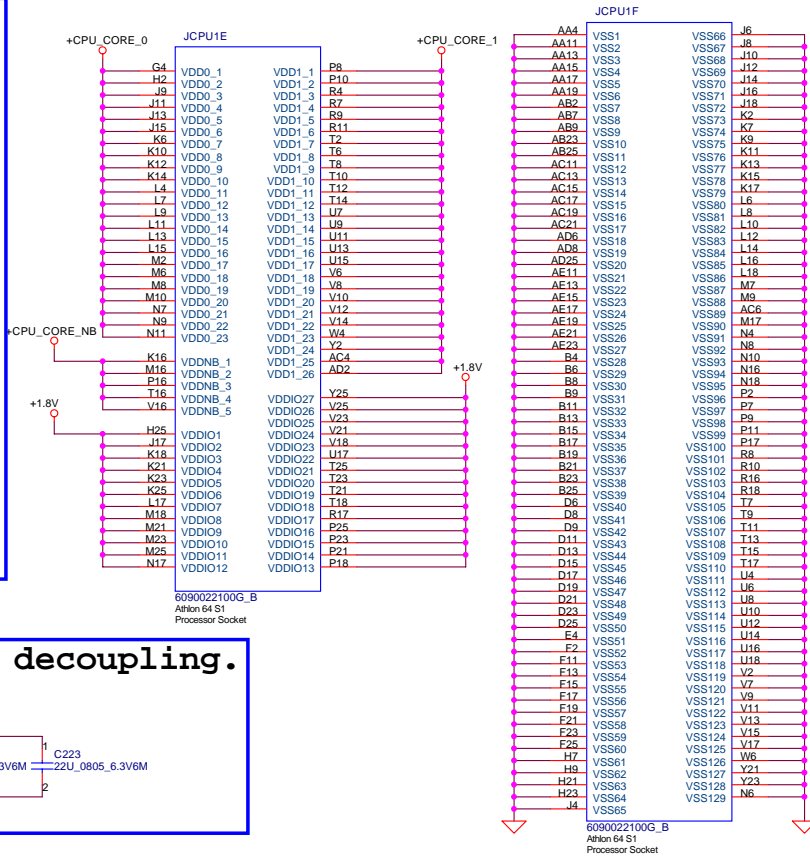
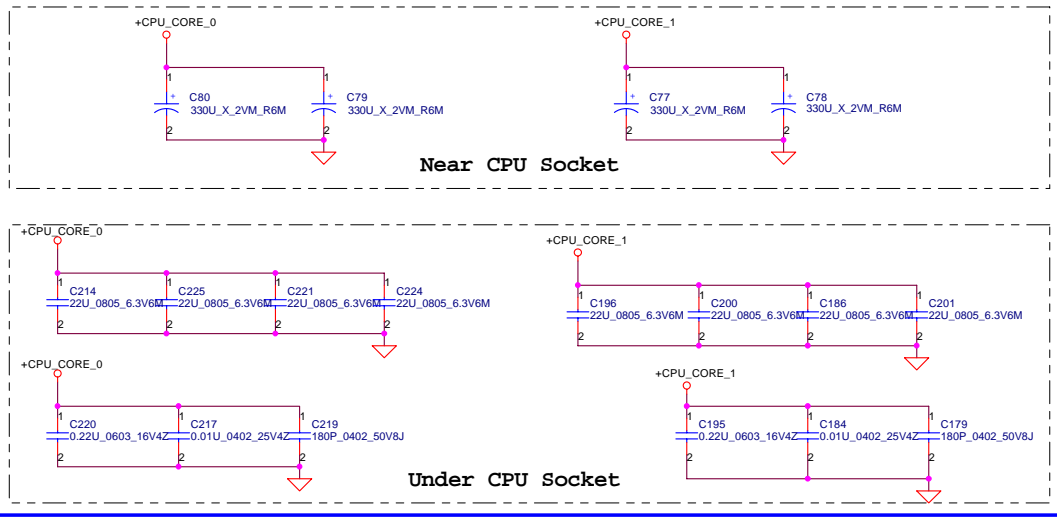
### HDT Connector

2200p change to 1000p for ADT7421

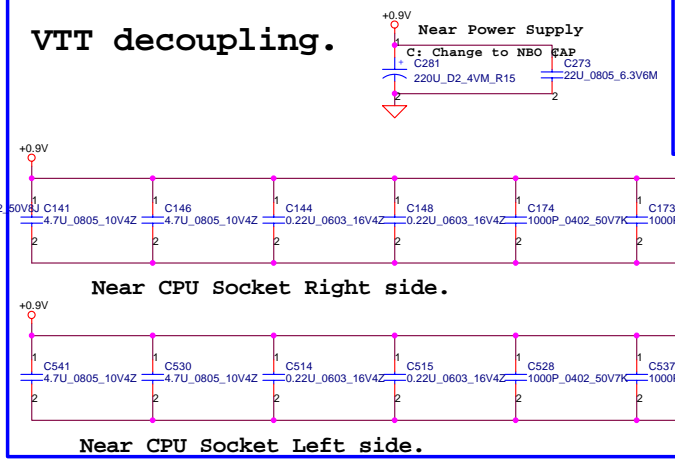
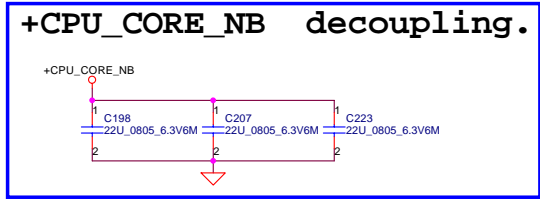
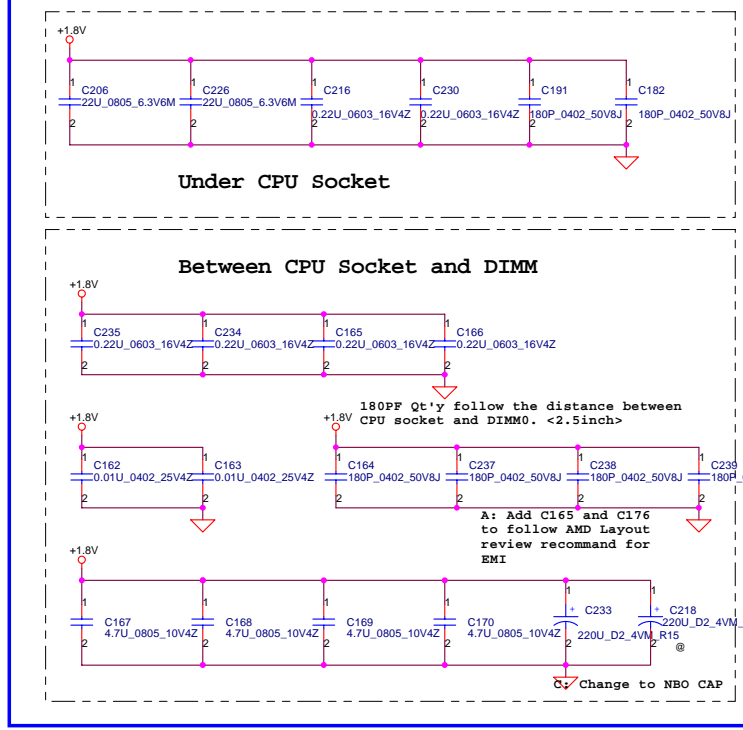
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# VDD(+CPU\_CORE) decoupling.

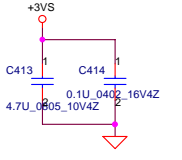
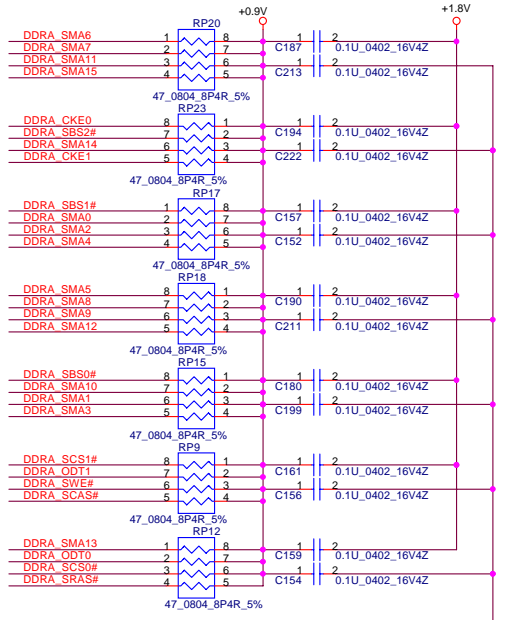
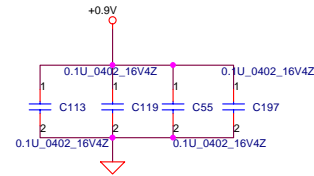
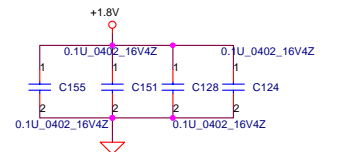
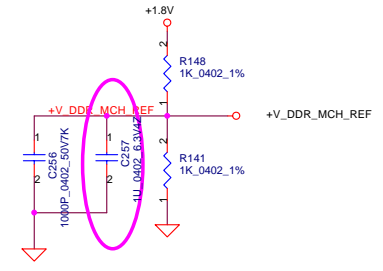
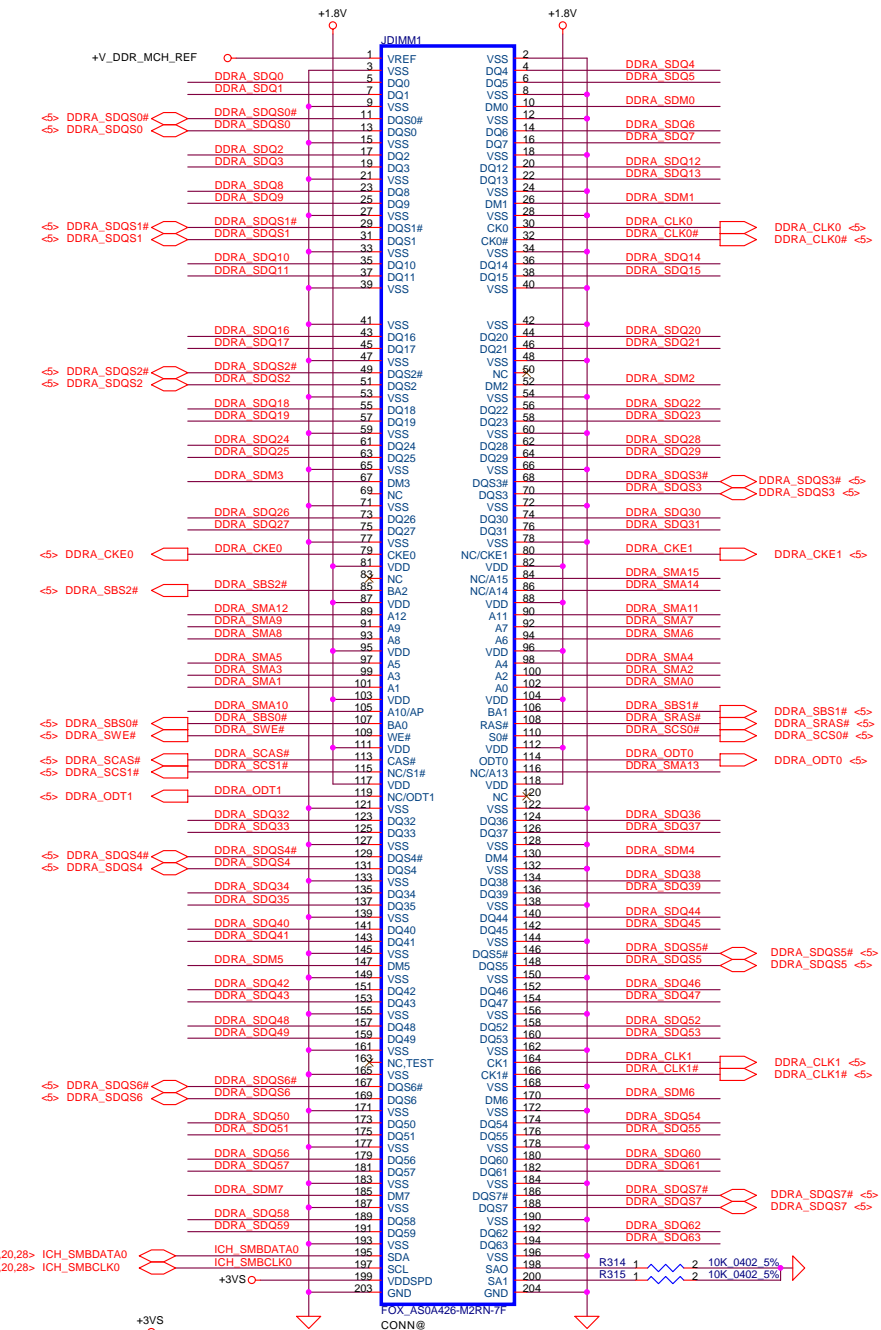


# VDDIO decoupling.



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**RESERVE**  
+V\_DDR\_MCH\_REF BUFFER CIRCUIT



**DIMM1 REV H:5.2mm (BOT)**

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U258B

PCIE GTX_C_MRX_P0	C680	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX_MRX_P0_D4	GFX_RX0P
PCIE GTX_C_MRX_N0	C681	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX_MRX_N0_C4	GFX_RX0N
PCIE GTX_C_MRX_P1	C682	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX_MRX_P1_A3	GFX_RX1P
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PCIE GTX_C_MRX_P9	C698	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX_MRX_P9_M8	GFX_RX9P
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PCIE GTX_C_MRX_P15	C710	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX_MRX_P15_T4	GFX_RX15P
PCIE GTX_C_MRX_N15	C711	1	2VGA@ 0.1U 0402 16V7K	PCIE GTX_MRX_N15_T3	GFX_RX15N

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GFX_TX0P	A5	PCIE_MTX_GRX_P0	C451	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P0
GFX_TX0N	B5	PCIE_MTX_GRX_N0	C450	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N0
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GFX_TX6N	H4	PCIE_MTX_GRX_N6	C473	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N6
GFX_TX7P	H3	PCIE_MTX_GRX_P7	C472	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P7
GFX_TX7N	J1	PCIE_MTX_GRX_N7	C459	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N7
GFX_TX8P	H2	PCIE_MTX_GRX_P8	C458	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P8
GFX_TX8N	J2	PCIE_MTX_GRX_N8	C475	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N8
GFX_TX9P	J1	PCIE_MTX_GRX_P9	C474	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P9
GFX_TX9N	K4	PCIE_MTX_GRX_N9	C461	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N9
GFX_TX10P	K1	PCIE_MTX_GRX_P10	C460	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P10
GFX_TX10N	K3	PCIE_MTX_GRX_N10	C477	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N10
GFX_TX11P	K2	PCIE_MTX_GRX_P11	C476	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P11
GFX_TX11N	M4	PCIE_MTX_GRX_N12	C462	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N12
GFX_TX12P	M1	PCIE_MTX_GRX_P12	C479	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P12
GFX_TX12N	M2	PCIE_MTX_GRX_N13	C478	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N13
GFX_TX13P	N2	PCIE_MTX_GRX_P14	C465	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P14
GFX_TX13N	N1	PCIE_MTX_GRX_N14	C464	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N14
GFX_TX14P	P1	PCIE_MTX_GRX_P15	C481	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_P15
GFX_TX14N	P2	PCIE_MTX_GRX_N15	C480	1	2VGA@0.1U 0402 16V7K	PCIE_MTX_C_GRX_N15

PCIE I/F GFX

PCIE I/F GPP

<28> PCIE_PTX_C_IRX_P1	PCIE_PTX_C_IRX_P1	AE3	GPP_RX0P
<28> PCIE_PTX_C_IRX_N1	PCIE_PTX_C_IRX_N1	AD4	GPP_RX0N
<28> PCIE_PTX_C_IRX_P2	PCIE_PTX_C_IRX_P2	AD1	GPP_RX1P
<28> PCIE_PTX_C_IRX_N2	PCIE_PTX_C_IRX_N2	AD2	GPP_RX1N
<28> PCIE_PTX_C_IRX_P3	PCIE_PTX_C_IRX_P3	V5	GPP_RX2P
<28> PCIE_PTX_C_IRX_N3	PCIE_PTX_C_IRX_N3	W6	GPP_RX2N
<28> PCIE_PTX_C_IRX_P4	PCIE_PTX_C_IRX_P4	U7	GPP_RX3P
<28> PCIE_PTX_C_IRX_N4	PCIE_PTX_C_IRX_N4	U8	GPP_RX3N
<28> PCIE_PTX_C_IRX_P5	PCIE_PTX_C_IRX_P5	U9	GPP_RX4P
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<28> PCIE_PTX_C_IRX_P6	PCIE_PTX_C_IRX_P6	U7	GPP_RX5P
<28> PCIE_PTX_C_IRX_N6	PCIE_PTX_C_IRX_N6	U7	GPP_RX5N

PCIE I/F SB

<19> SB_RX0P	SB_RX0P	AAR	SB_RX0P
<19> SB_RX0N	SB_RX0N	Y8	SB_RX0N
<19> SB_RX1P	SB_RX1P	AA7	SB_RX1P
<19> SB_RX1N	SB_RX1N	Y7	SB_RX1N
<19> SB_RX2P	SB_RX2P	AA6	SB_RX2P
<19> SB_RX2N	SB_RX2N	AA5	SB_RX2N
<19> SB_RX3P	SB_RX3P	AA8	SB_RX3P
<19> SB_RX3N	SB_RX3N	Y5	SB_RX3N

PCIE I/F GPP

GPP_TX0P	AC1	GPP_TX0P
GPP_TX0N	AB4	GPP_TX0N
GPP_TX1P	AB3	GPP_TX1P
GPP_TX1N	AB2	GPP_TX1N
GPP_TX2P	AA2	GPP_TX2P
GPP_TX2N	Y1	GPP_TX2N
GPP_TX3P	Y2	GPP_TX3P
GPP_TX3N	Y2	GPP_TX3N
GPP_TX4P	Y4	GPP_TX4P
GPP_TX4N	Y1	GPP_TX4N
GPP_TX5P	Y2	GPP_TX5P
GPP_TX5N	Y2	GPP_TX5N

TV Tuner

PCIE_ITX_C_PRX_P1	<28>	PCIE_ITX_C_PRX_P1
PCIE_ITX_C_PRX_N1	<28>	PCIE_ITX_C_PRX_N1
PCIE_ITX_C_PRX_P2	<28>	PCIE_ITX_C_PRX_P2
PCIE_ITX_C_PRX_N2	<28>	PCIE_ITX_C_PRX_N2
PCIE_ITX_C_PRX_P3	<28>	PCIE_ITX_C_PRX_P3
PCIE_ITX_C_PRX_N3	<28>	PCIE_ITX_C_PRX_N3

WLAN

GLAN

H\_CADOP[0..15]

H\_CADON[0..15]

PCIE CALR(P/CE\_BCALR/P)

AC8	R33	1	2	1.27K 0402 1%
AB8	R31	1	2	2K 0402 1%

+1.1V5

RS780M\_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PCIE_MTX_GRX_P0	C897	1	2	UMA@0.1U 0402 10V7K HDMI_TX2+ UMA	HDMI_TX2+ UMA <17>
PCIE_MTX_GRX_N0	C898	1	2	UMA@0.1U 0402 10V7K HDMI_TX2- UMA	HDMI_TX2- UMA <17>
PCIE_MTX_GRX_P1	C899	1	2	UMA@0.1U 0402 10V7K HDMI_TX1+ UMA	HDMI_TX1+ UMA <17>
PCIE_MTX_GRX_N1	C900	1	2	UMA@0.1U 0402 10V7K HDMI_TX1- UMA	HDMI_TX1- UMA <17>
PCIE_MTX_GRX_P2	C901	1	2	UMA@0.1U 0402 10V7K HDMI_TX0+ UMA	HDMI_TX0+ UMA <17>
PCIE_MTX_GRX_N2	C902	1	2	UMA@0.1U 0402 10V7K HDMI_TX0- UMA	HDMI_TX0- UMA <17>
PCIE_MTX_GRX_P3	C903	1	2	UMA@0.1U 0402 10V7K HDMI_CLK+ UMA	HDMI_CLK+ UMA <17>
PCIE_MTX_GRX_N3	C904	1	2	UMA@0.1U 0402 10V7K HDMI_CLK- UMA	HDMI_CLK- UMA <17>

PART 1 OF 6

U258A

H_CADOP0	Y25	HT_RXCAD0P	D24	H_CADIP0
H_CADON0	Y24	HT_RXCAD0N	D25	H_CADIN0
H_CADOP1	Y22	HT_RXCAD1P	E24	H_CADIP1
H_CADON1	Y23	HT_RXCAD1N	E25	H_CADIN1
H_CADOP2	V25	HT_RXCAD2P	F24	H_CADIP2
H_CADON2	V24	HT_RXCAD2N	F25	H_CADIN2
H_CADOP3	U24	HT_RXCAD3P	F23	H_CADIP3
H_CADON3	U25	HT_RXCAD3N	F22	H_CADIN3
H_CADOP4	T25	HT_RXCAD4P	H23	H_CADIP4
H_CADON4	T24	HT_RXCAD4N	H22	H_CADIN4
H_CADOP5	V22	HT_RXCAD5P	J25	H_CADIP5
H_CADON5	P23	HT_RXCAD5N	J24	H_CADIN5
H_CADOP6	P25	HT_RXCAD6P	K24	H_CADIP6
H_CADON6	P24	HT_RXCAD6N	K25	H_CADIN6
H_CADOP7	N24	HT_RXCAD7P	K23	H_CADIP7
H_CADON7	N25	HT_RXCAD7N	K22	H_CADIN7
H_CADOP8	AC24	HT_RXCAD8P	F21	H_CADIP8
H_CADON8	AC25	HT_RXCAD8N	G24	H_CADIN8
H_CADOP9	AB25	HT_RXCAD9P	G21	H_CADIP9
H_CADON9	AB24	HT_RXCAD9N	H21	H_CADIN9
H_CADOP10	AA24	HT_RXCAD10P	J20	H_CADIP10
H_CADON10	AA25	HT_RXCAD10N	J21	H_CADIN10
H_CADOP11	Y22	HT_RXCAD11P	J18	H_CADIP11
H_CADON11	Y23	HT_RXCAD11N	K17	H_CADIN11
H_CADOP12	W21	HT_RXCAD12P	L19	H_CADIP12
H_CADON12	W20	HT_RXCAD12N	L18	H_CADIN12
H_CADOP13	V21	HT_RXCAD13P	J19	H_CADIP13
H_CADON13	V20	HT_RXCAD13N	M19	H_CADIN13
H_CADOP14	U20	HT_RXCAD14P	M21	H_CADIP14
H_CADON14	U21	HT_RXCAD14N	P21	H_CADIN14
H_CADOP15	U19	HT_RXCAD15P	P18	H_CADIP15
H_CADON15	U18	HT_RXCAD15N	M18	H_CADIN15
H_CLKOP0	T22	HT_RXCLK0P	H24	H_CLKIP0 <4>
H_CLKON0	T23	HT_RXCLK0N	H25	H_CLKIN0 <4>
H_CLKOP1	AB23	HT_RXCLK1P	L21	H_CLKIP1 <4>
H_CLKON1	AA22	HT_RXCLK1N	L20	H_CLKIN1 <4>
H_CTLOP0	M22	HT_RXCTL0P	M24	H_CTLIP0 <4>
H_CTLOP1	M23	HT_RXCTL0N	M25	H_CTLIN0 <4>
H_CTLOP2	R21	HT_RXCTL1P	P19	H_CTLIP1 <4>
H_CTLOP3	R20	HT_RXCTL1N	P18	H_CTLIN1 <4>
H_RXCALP	C23	HT_RXCALP	B24	
H_RXCALN	A24	HT_RXCALN	B25	

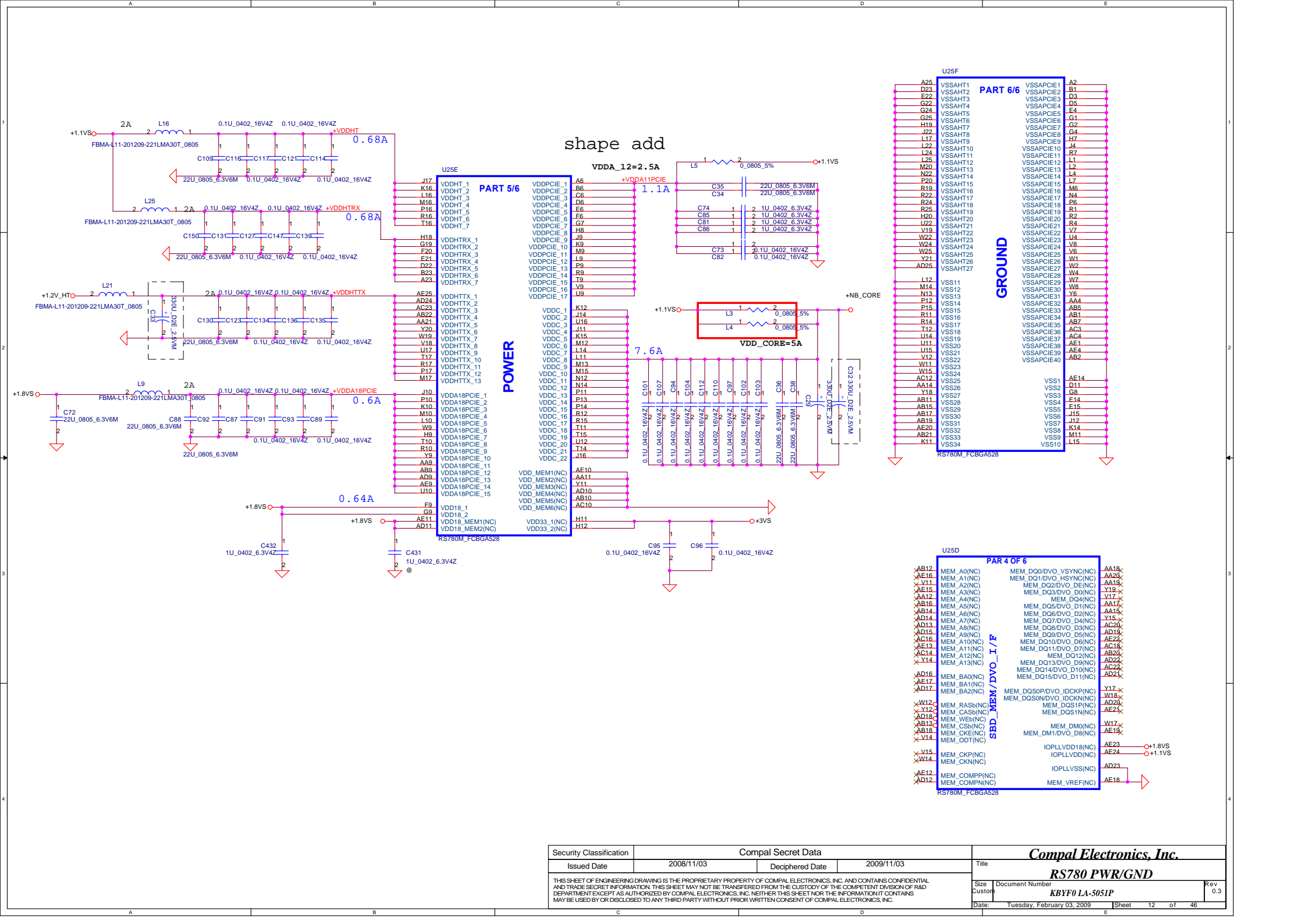
HYPER TRANSPORT CPU I/F

0718 Place within 1" layout 1:2

RS780M\_FCBGA528

0718 Place within 1" layout 1:2





shape add

VDDA\_12=2.5A

VDDA11PCIE 1.1A

VDD\_CORE=5A

7.6A

VDD33\_1(NC) VDD33\_2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

VDD18\_1 VDD18\_2 VDD18\_MEM1(NC) VDD18\_MEM2(NC)

U25F

PART 6/6

GROUND

U25D

PAR 4 OF 6

SBD\_MEM/DVO\_I/F

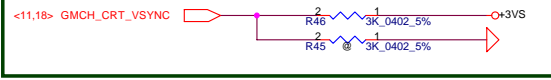
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Issued Date	2008/11/03	Deciphered Date	2009/11/03
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Size	Document Number	Rev	
Custom	KB70 LA-501P	0.3	
Date:	Tuesday, February 03, 2009	Sheet	12 of 46

Compal Electronics, Inc.

RS780 PWR/GND

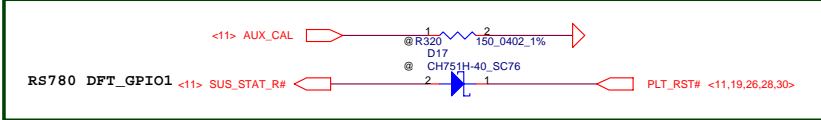
KB70 LA-501P

Tuesday, February 03, 2009 Sheet 12 of 46



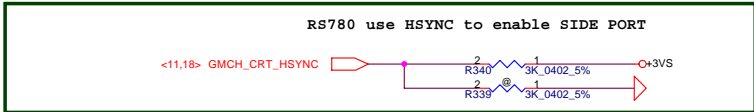
**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO. (VSYNC)  
 1 : Disable (RS780)  
 0 : Enable (RS780)



**DFT\_GPIO1:LOAD\_EEPROM\_STRAPS**

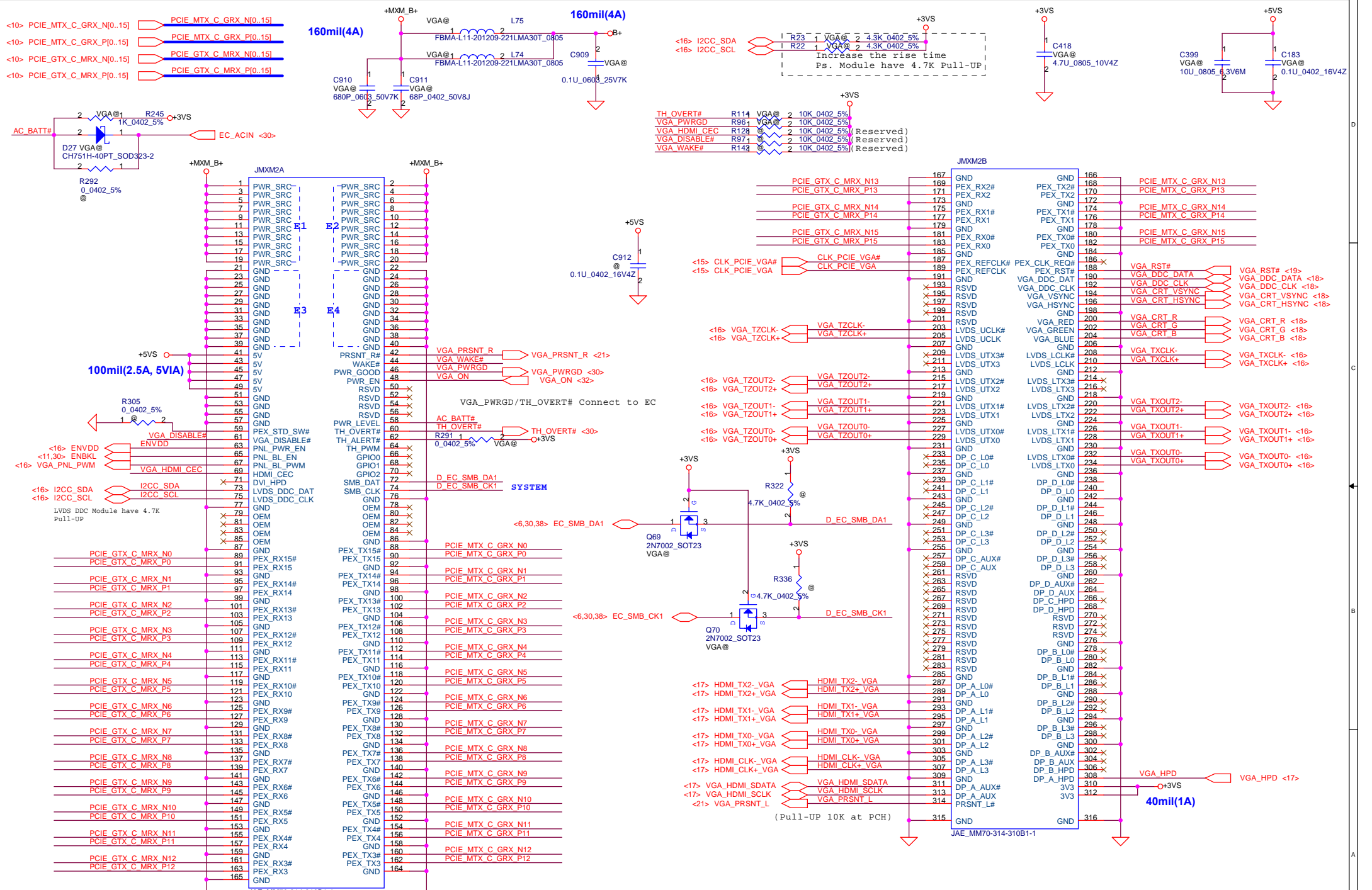
Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



**RS780 use HSYNC to enable SIDE PORT**

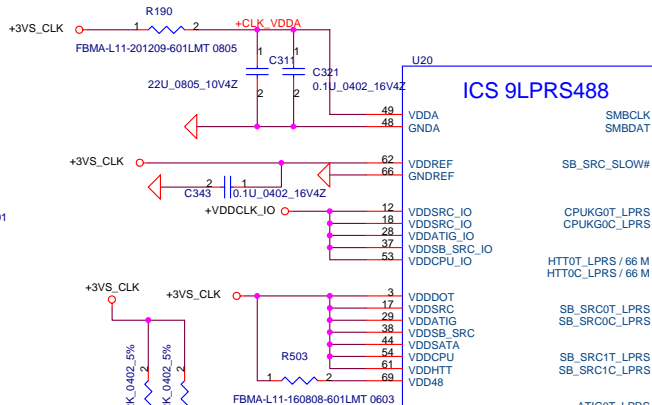
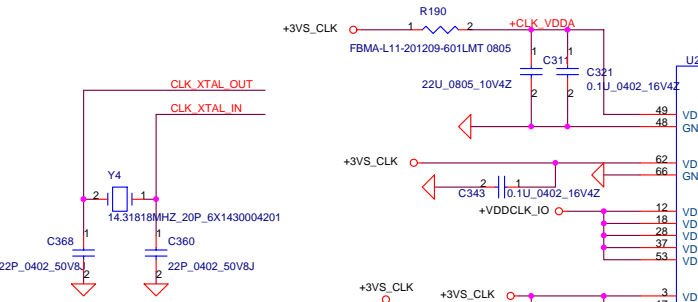
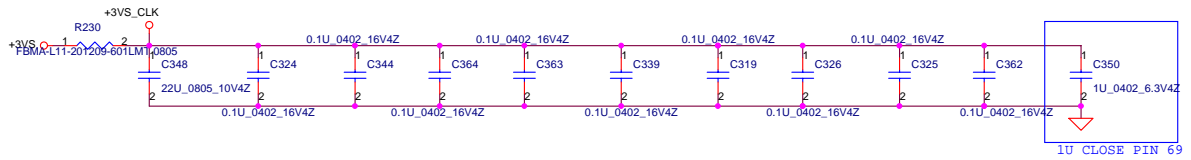
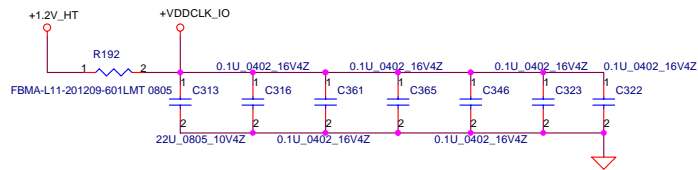
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)  
 0 : Enable (RS780)  
 1 : Disable(RS780)

Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	RS780 STRAPS	
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				Date:	Tuesday, February 03, 2009
				Sheet	13 of 46
				Rev	0.3



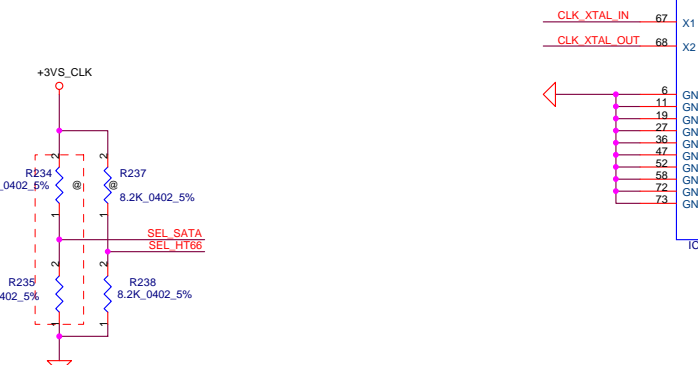
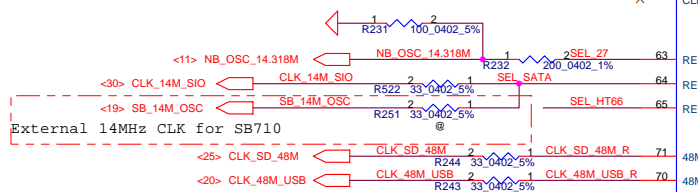
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Issued Date	2008/11/03	Deciphered Date	2009/11/03
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Compal Electronics, Inc.		
Title <b>MXM Connector</b>		
Size B	Document Number <b>KBYFO LA-5051P</b>	Rev 0.3
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REQ0# FOR SRC1  
 REQ2# FOR SRC2  
 REQ3# FOR SRC3

<28> MINI1\_CLKREQ#  
 <28> MINI2\_CLKREQ#



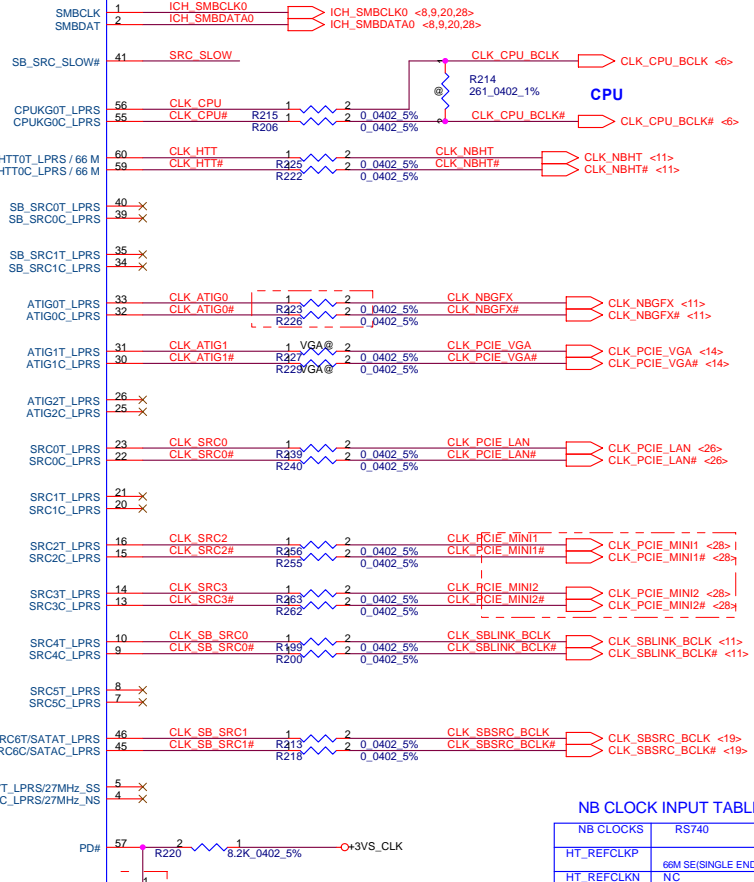
SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

\* default

NB_OSC_14.318M	1	configure as 27M and 27M_SS output
	0*	configure as SRC_7 output

SRC 0	LAN
SRC 1	NEWCARD
SRC 2	MINI2
SRC 3	MINI1

**ICS 9LPRS488**



NB GFX

VGA chip(Dis)

GLAN

MiniCard\_1

MiniCard\_2

NB A LINK

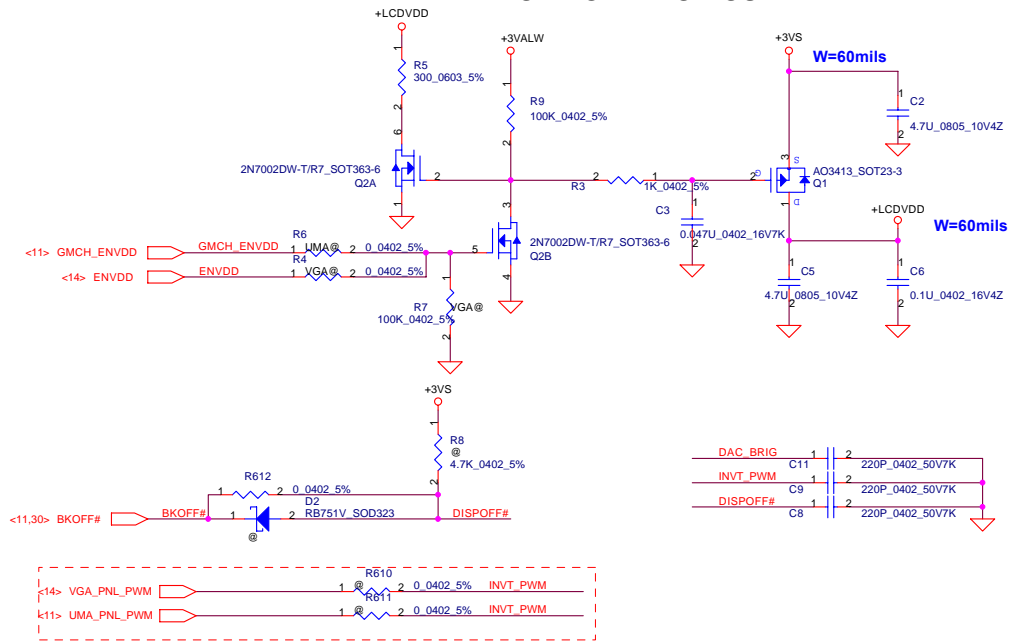
SB RCLK

**NB CLOCK INPUT TABLE**

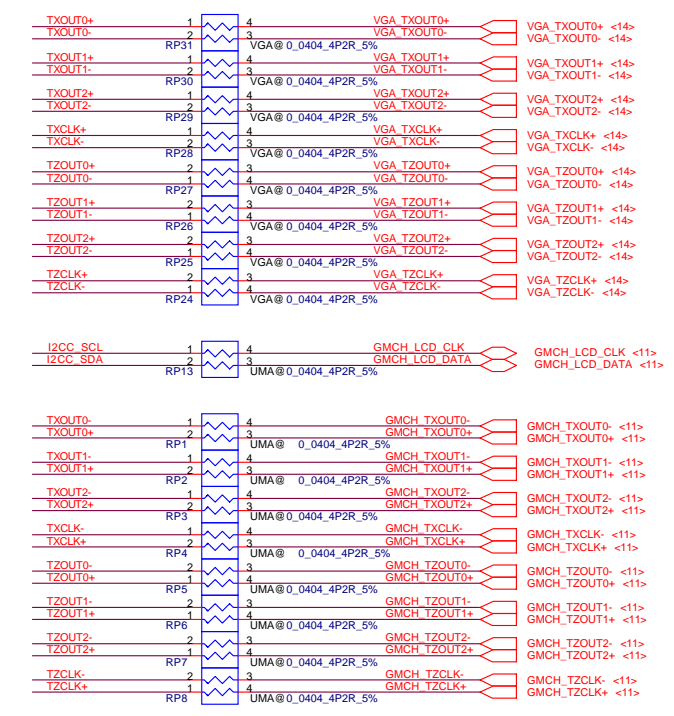
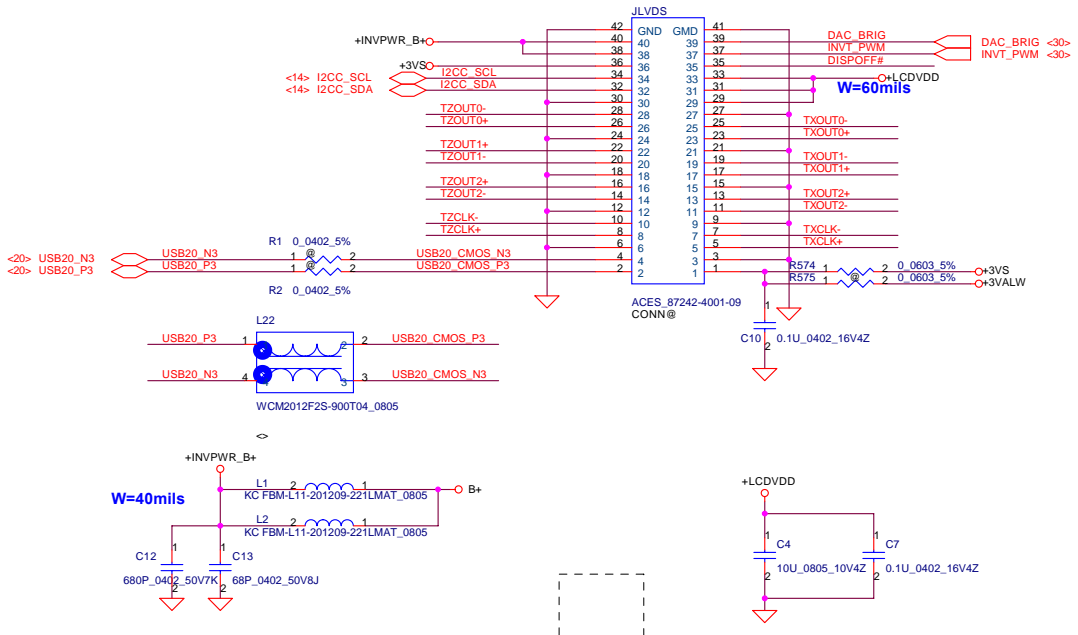
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(N/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPS_REFCLK	100M DIFF	100M DIFF	100M DIFF

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Issued Date	2008/11/03	Deciphered Date	2009/11/03	Compal Electronics, Inc.
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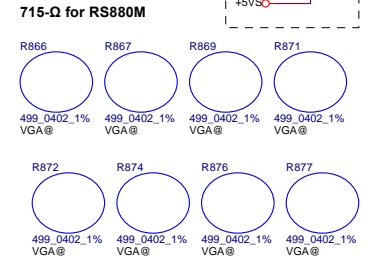
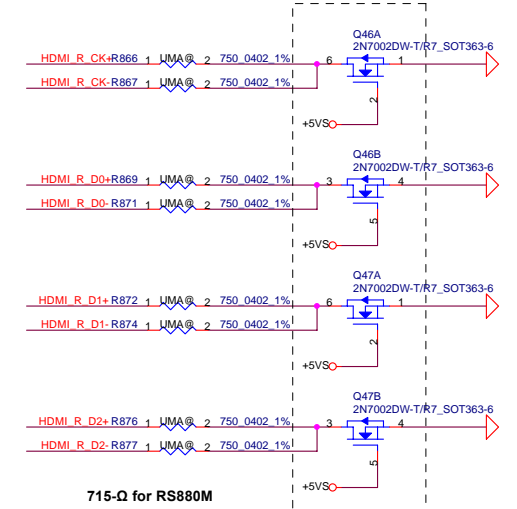
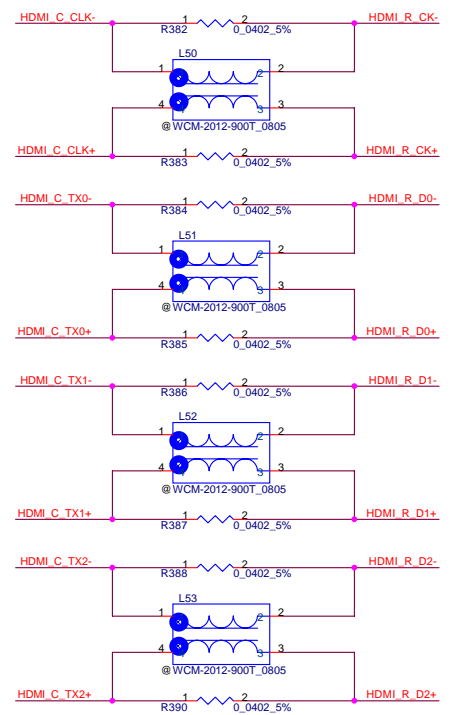
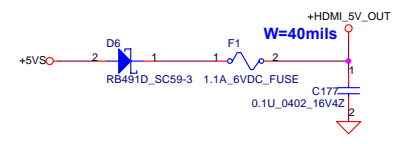
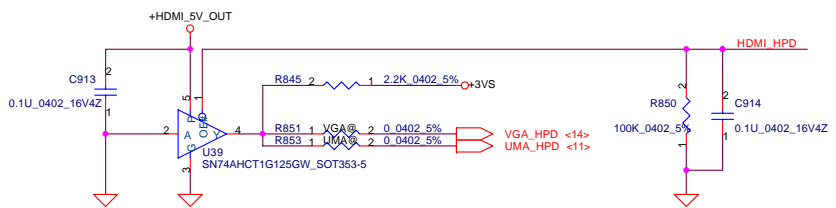
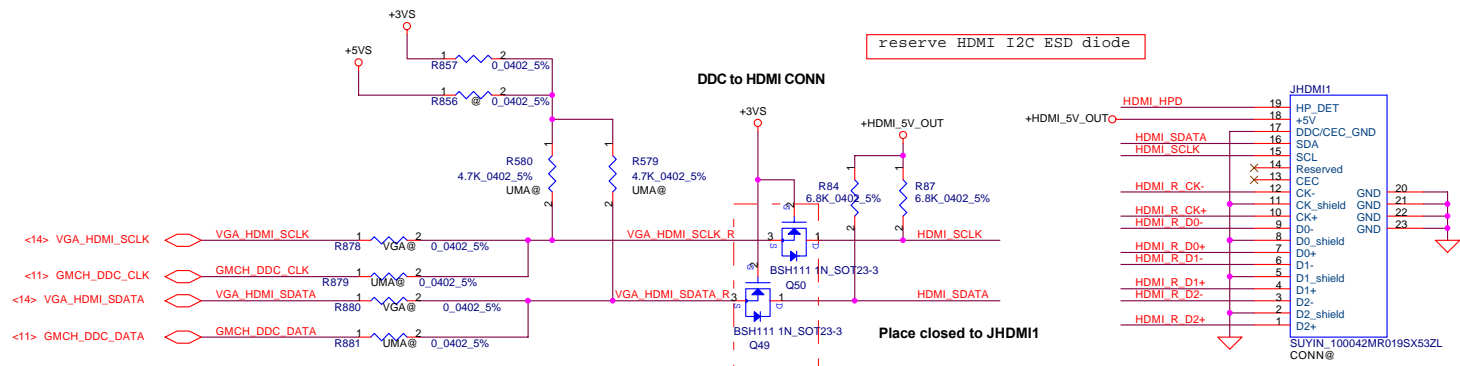
# LCD POWER CIRCUIT



# LCD/PANEL BD. Conn.



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Size	Document Number	Date		Sheet	
B	KBYF0 LA-5051P	Tuesday, February 03, 2009		16 of 46	
				Rev	
				0.3	

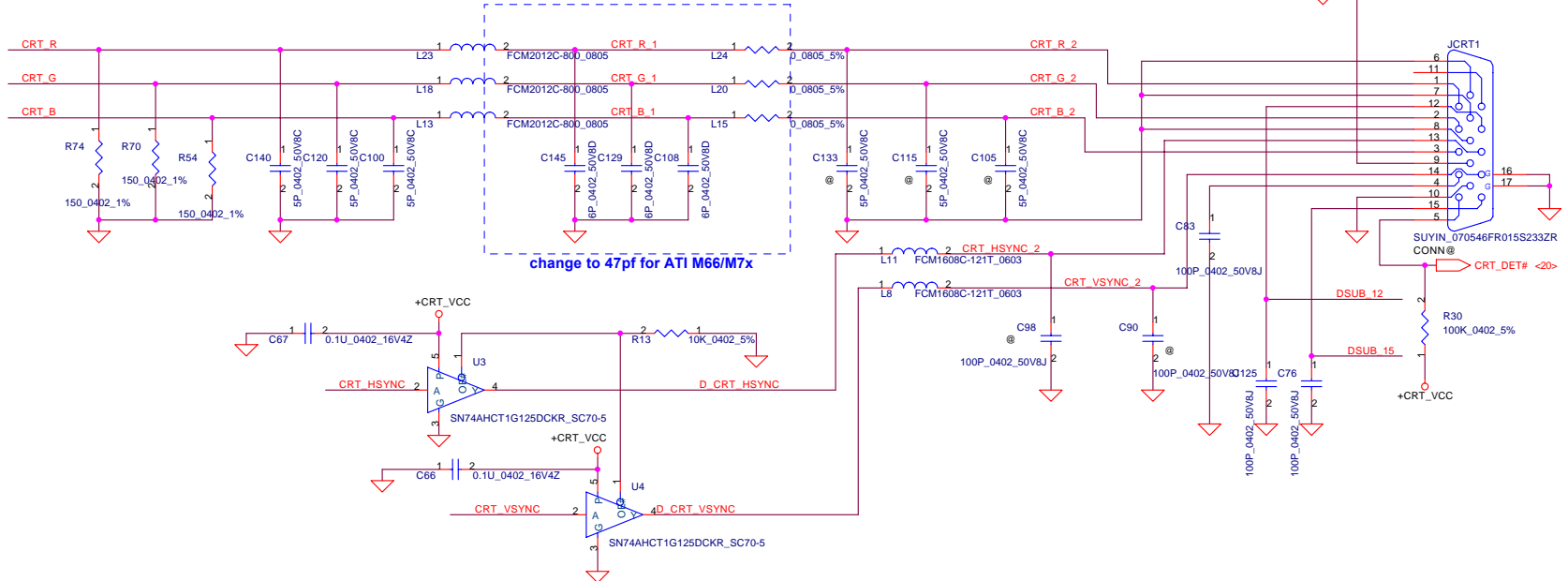


<14> HDMI_CLK+_VGA	C712	VGA@1	2	0.1U_0402_16V7K	HDMI_C_CLK+
<14> HDMI_CLK-_VGA	C713	VGA@1	2	0.1U_0402_16V7K	HDMI_C_CLK-
<14> HDMI_TX0+_VGA	C714	VGA@1	2	0.1U_0402_16V7K	HDMI_C_TX0+
<14> HDMI_TX0-_VGA	C715	VGA@1	2	0.1U_0402_16V7K	HDMI_C_TX0-
<14> HDMI_TX1+_VGA	C716	VGA@1	2	0.1U_0402_16V7K	HDMI_C_TX1+
<14> HDMI_TX1-_VGA	C717	VGA@1	2	0.1U_0402_16V7K	HDMI_C_TX1-
<14> HDMI_TX2+_VGA	C718	VGA@1	2	0.1U_0402_16V7K	HDMI_C_TX2+
<14> HDMI_TX2-_VGA	C719	VGA@1	2	0.1U_0402_16V7K	HDMI_C_TX2-

<10> HDMI_CLK+_UMA	R858	UMA@	2	0.0402_5%	HDMI_C_CLK+
<10> HDMI_CLK-_UMA	R859	UMA@	2	0.0402_5%	HDMI_C_CLK-
<10> HDMI_TX0+_UMA	R860	UMA@	2	0.0402_5%	HDMI_C_TX0+
<10> HDMI_TX0-_UMA	R861	UMA@	2	0.0402_5%	HDMI_C_TX0-
<10> HDMI_TX1+_UMA	R862	UMA@	2	0.0402_5%	HDMI_C_TX1+
<10> HDMI_TX1-_UMA	R863	UMA@	2	0.0402_5%	HDMI_C_TX1-
<10> HDMI_TX2+_UMA	R864	UMA@	2	0.0402_5%	HDMI_C_TX2+
<10> HDMI_TX2-_UMA	R865	UMA@	2	0.0402_5%	HDMI_C_TX2-

Security Classification	Compal Secret Data		Title	DVI/HDMI Connector	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Size	Document Number
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				Date:	Tuesday, February 03, 2009
				Sheet	17 of 46
				Rev	0.3

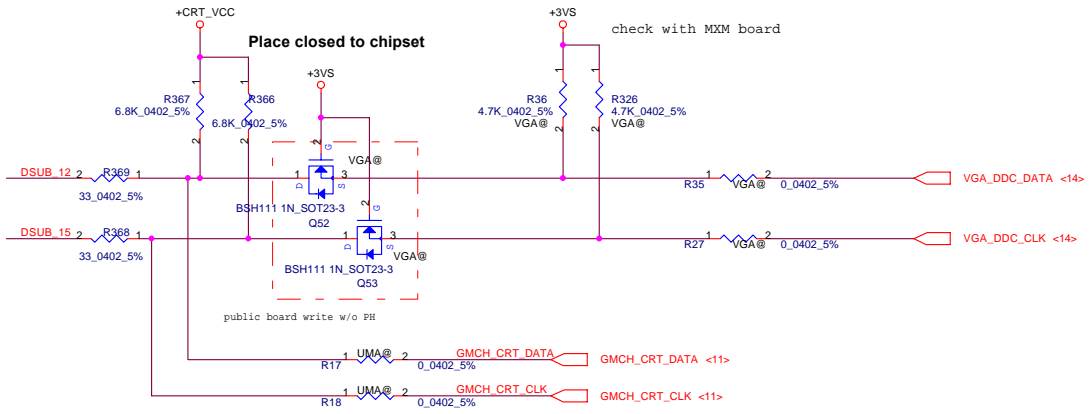
# CRT Connector



change to 47pf for ATI M66/M7x



Place closed to chipset

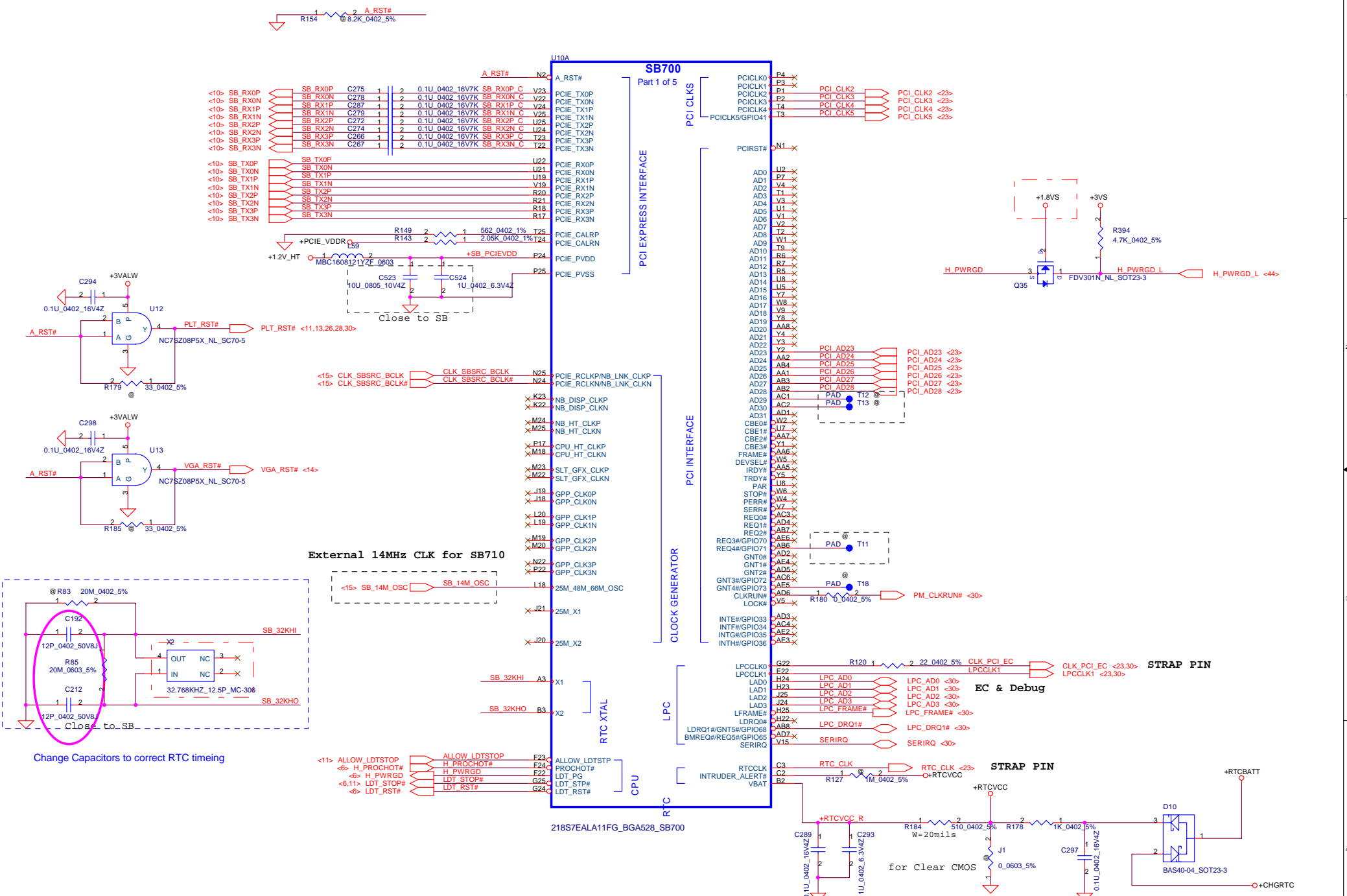


Place closed to chipset

check with MXM board

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Compal Electronics, Inc.			
Title CRT Connector			
Size B	Document Number KBYF0 LA-5015P	Rev 0.3	
Date:	Tuesday, February 03, 2009	Sheet	18 of 46

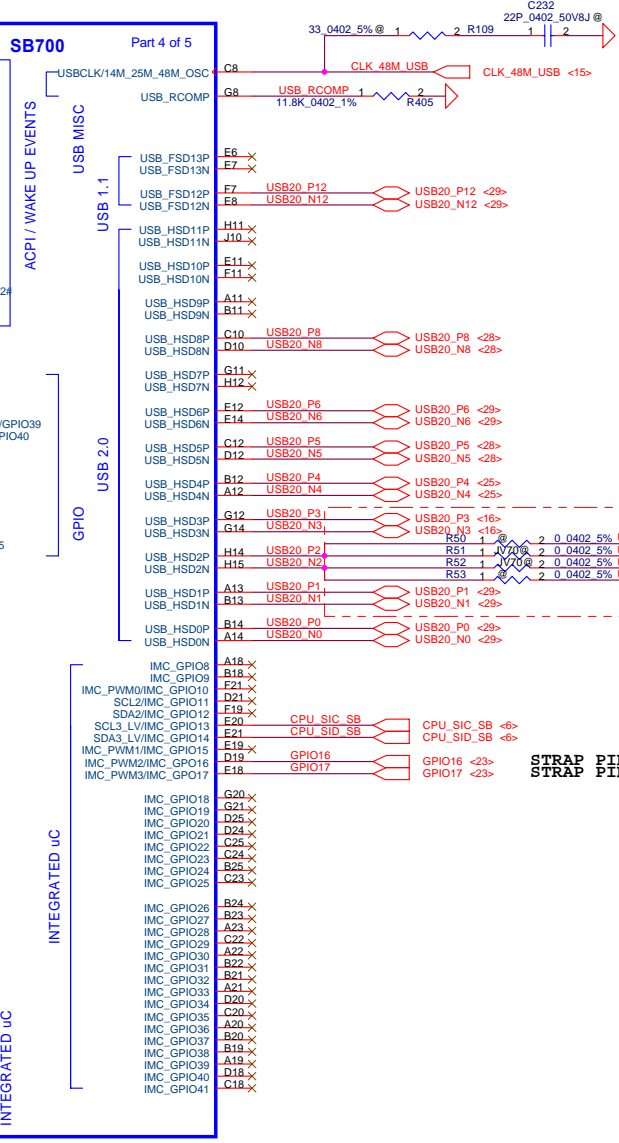
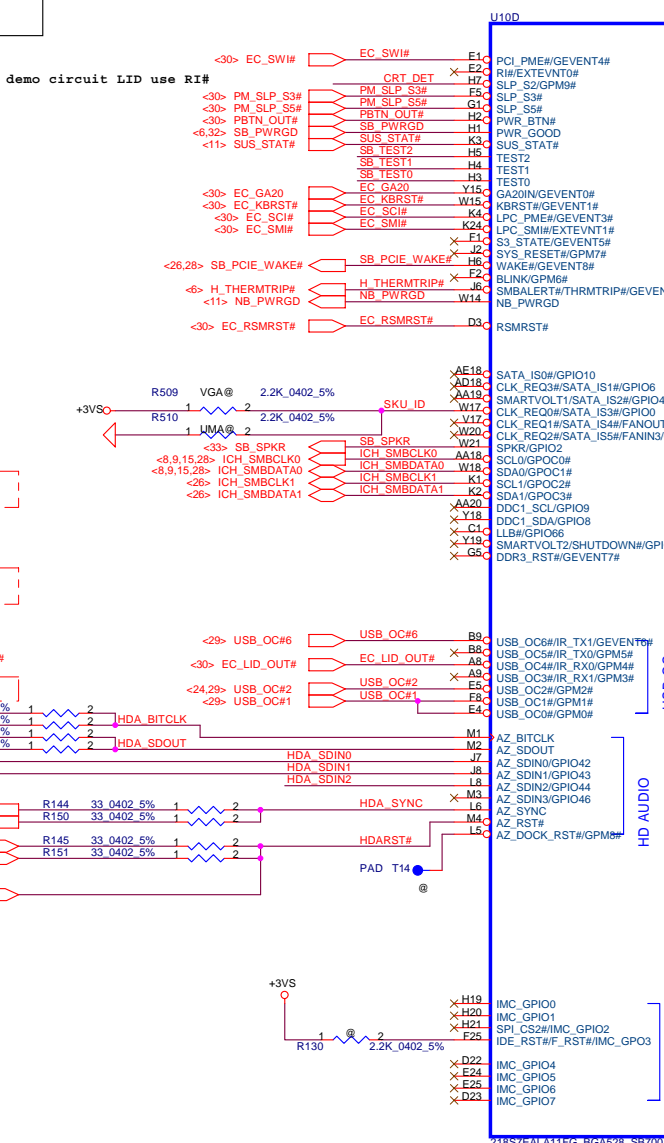
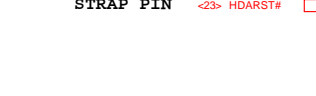
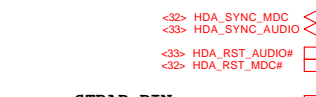
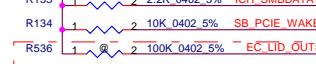
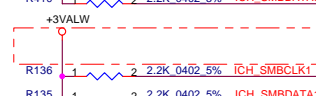
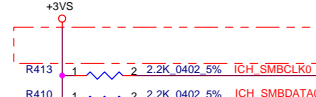
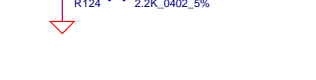
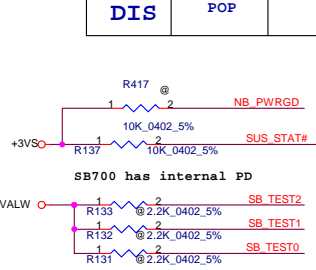


Security Classification	Compal Secret Data	
Issued Date	2008/11/03	Deciphered Date
		2009/11/03

<b>Compal Electronics, Inc.</b>		
<b>SB700-PCIe/PCI/ACPI/LPC/RTC</b>		
Size	Document Number	Rev
Custom	<b>KBYF0 LA-5051P</b>	0.3
Date:	Tuesday, February 03, 2009	Sheet 19 of 46

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SKU-ID	R509	R510
UMA		POP
DIS	POP	



- USB-12 Bluetooth
- USB-8 MiniCard(WLAN)
- USB-6 HS-USB
- USB-5 MiniCard(TV)
- USB-4 Card Reader
- USB-3 USB Camera
- USB-2 USB (eSATA) for SJW70  
Ext.USB/B for SJV70
- USB-1 Ext.USB/B
- USB-0 Ext.USB/B

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Title			
<b>Compal Electronics, Inc.</b>			
<b>SB700 USB/HD audio</b>			
Size	Document Number	Rev	
Custom	<b>KBYF0 LA-5051P</b>	0.3	
Date:	Tuesday, February 03, 2009	Sheet	20 of 46

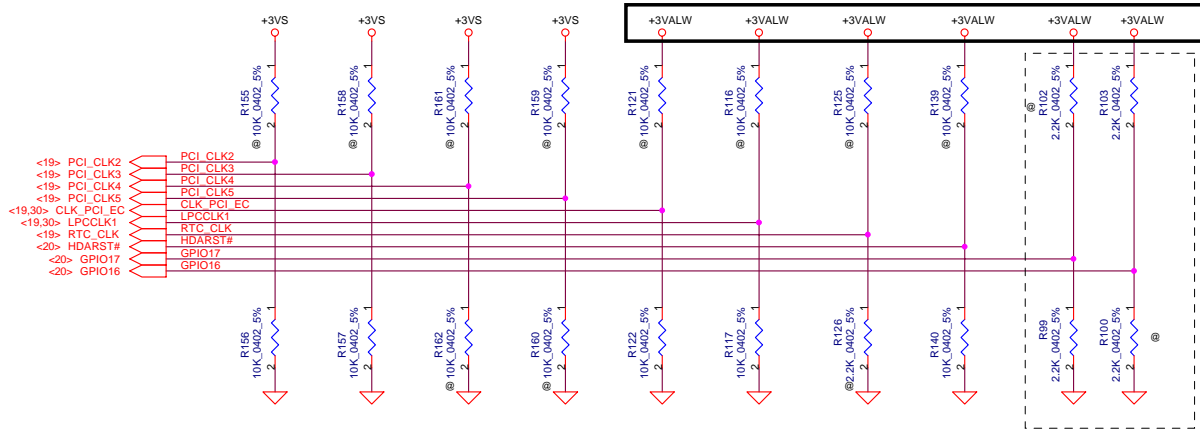




# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

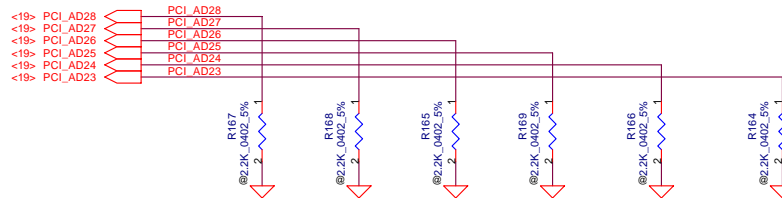
	PCI_CLK2 CLK_FCI_PCM	PCI_CLK3 CLK_FCI_DBG	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_FCI_BC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	<b>INTERNAL RTC</b>  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved HL = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) LL = FWH ROM



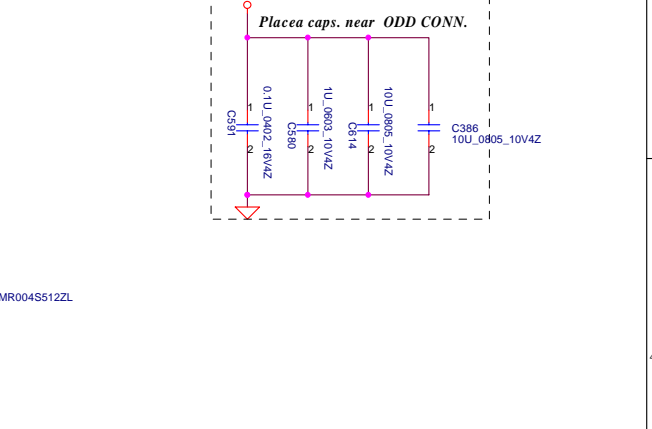
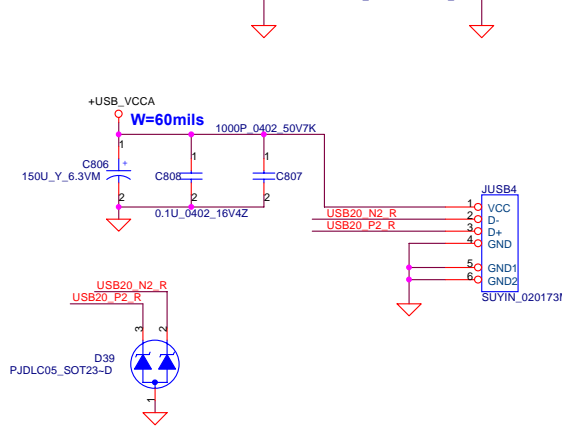
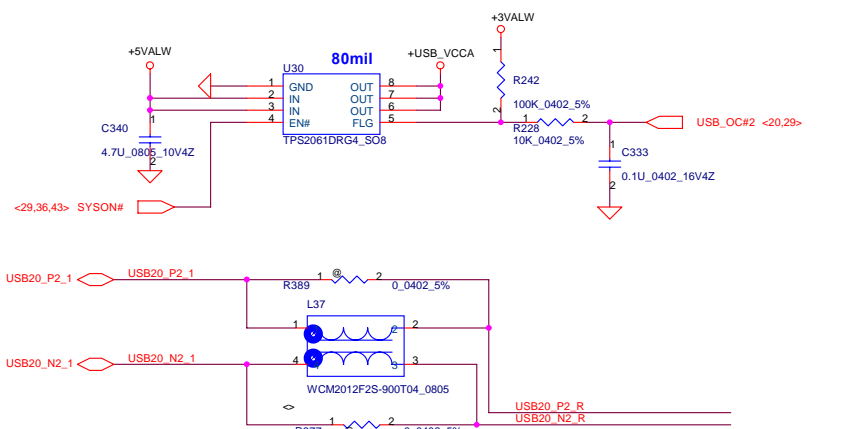
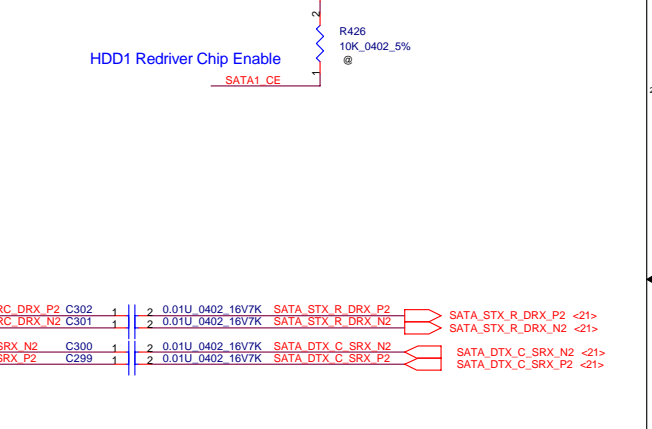
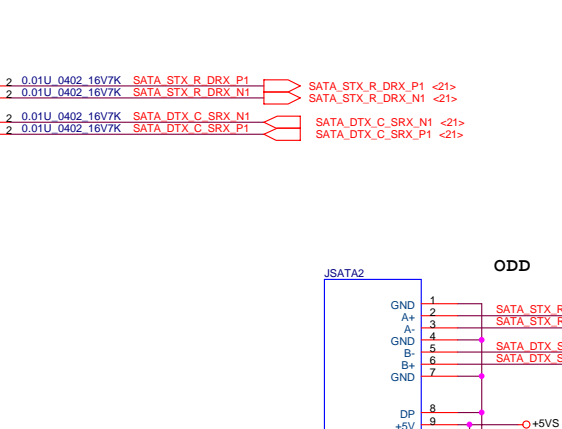
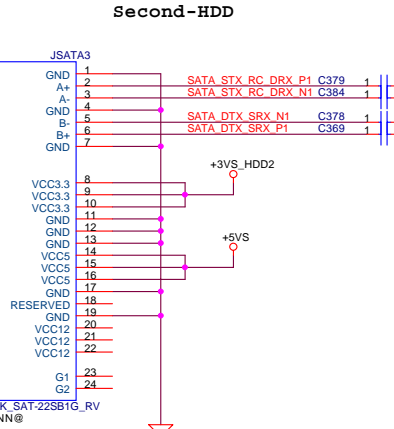
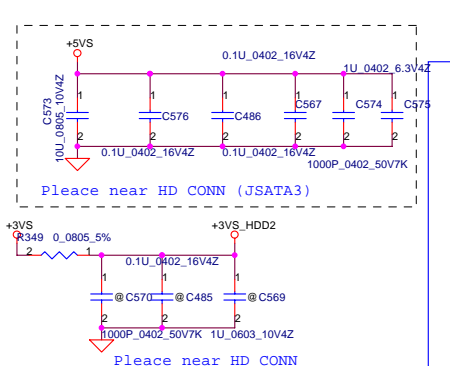
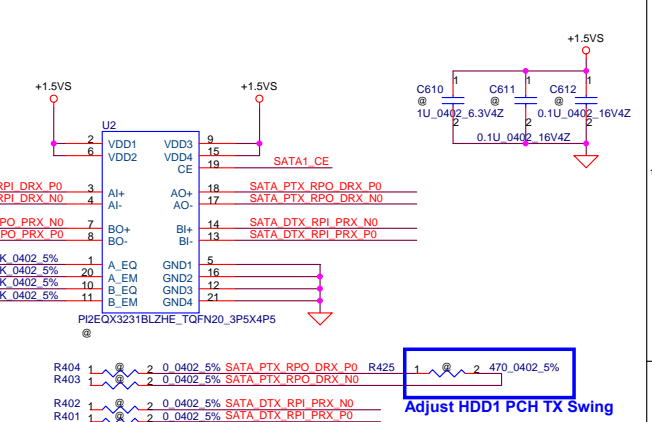
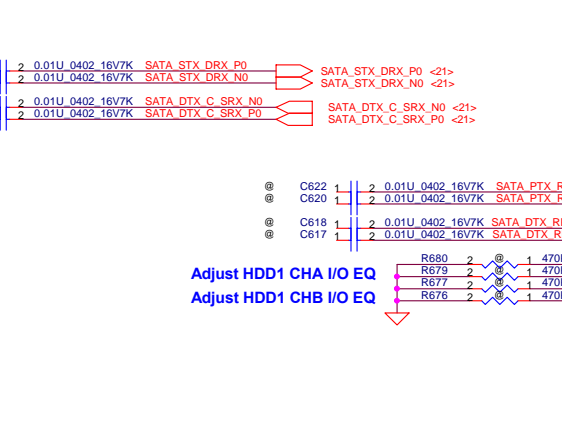
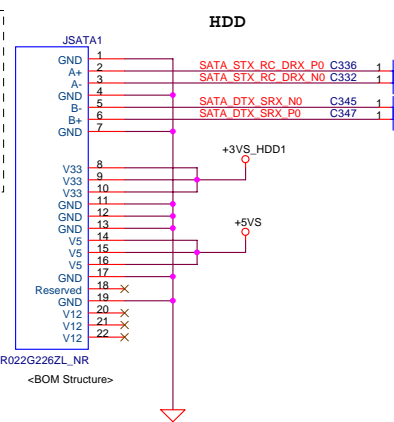
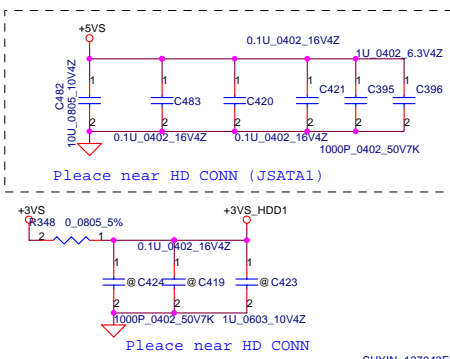
# DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>SB700 STRAPS</b>			
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				Date:	Tuesday, February 03, 2009	Sheet	23 of 46

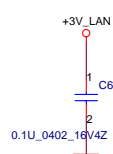
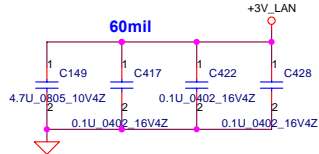


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				Date: Tuesday, February 03, 2009	Sheet 24 of 46



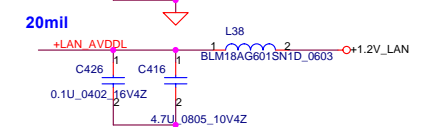
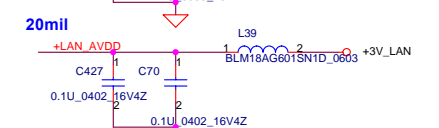
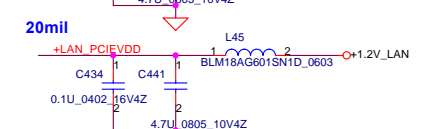
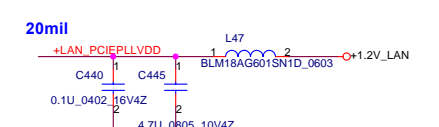
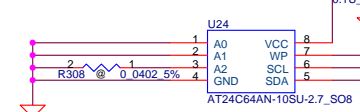
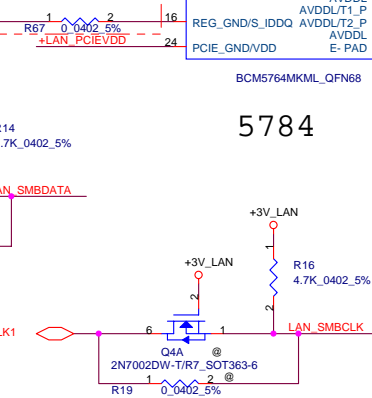
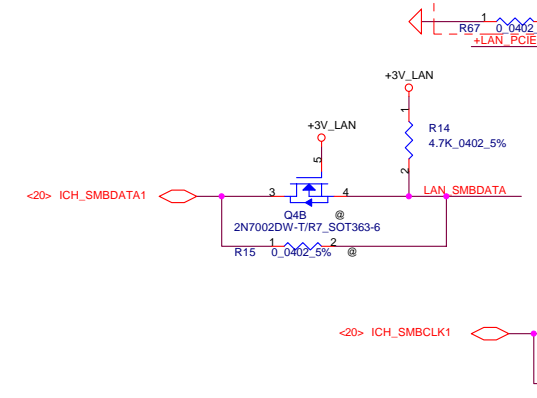
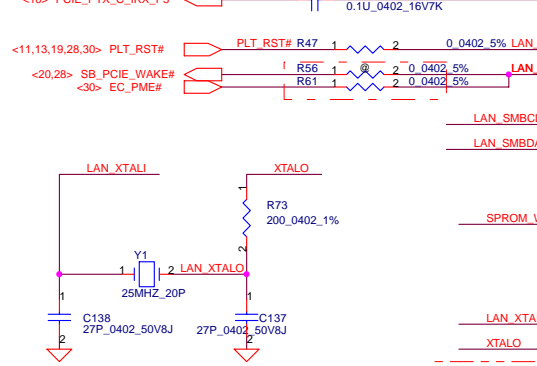
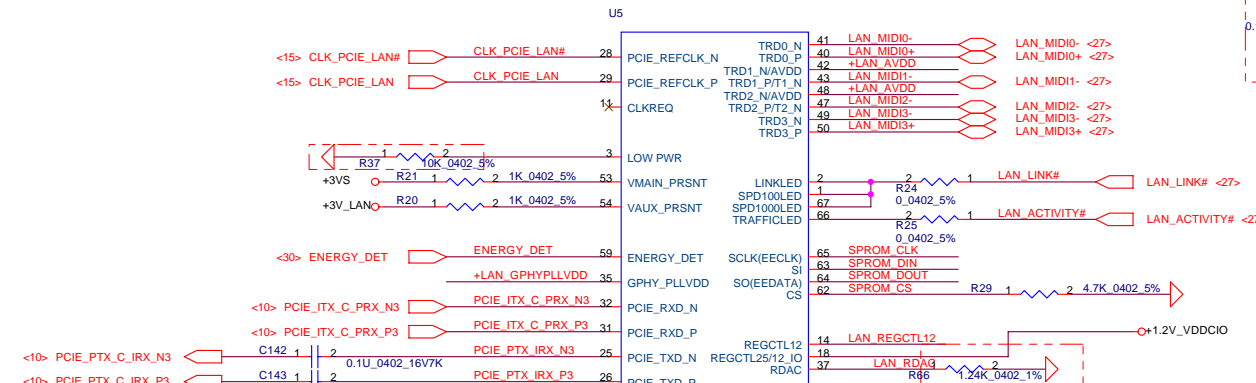
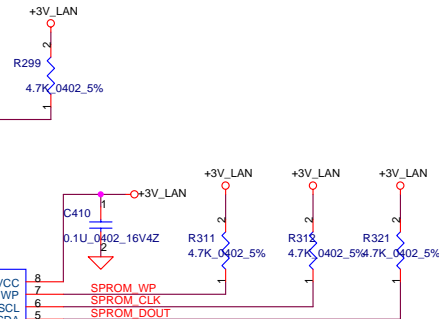
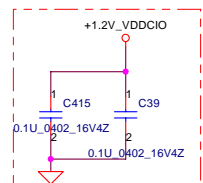
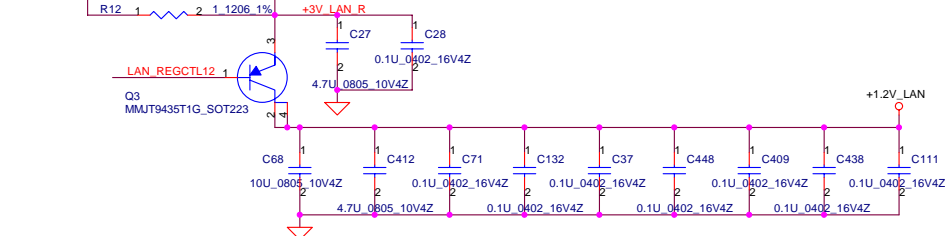
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+3V\_LAN R60 4.7K\_0402\_5% LAN\_PME#



+3V\_LAN R309 1.206\_1% R12 1.206\_1%

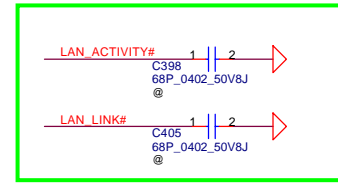
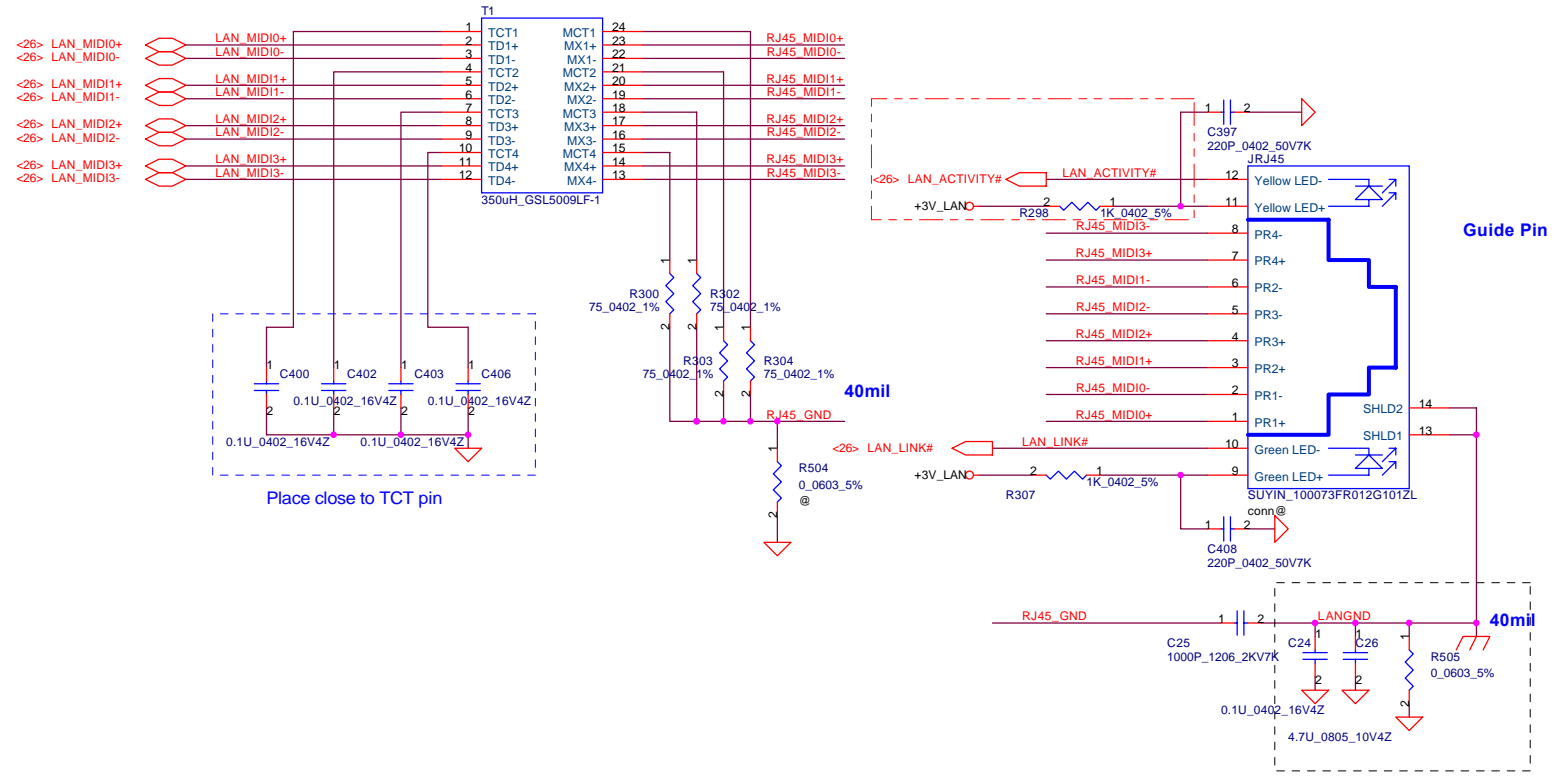
LAN\_REGCTL12 Q3 MMJT9435T1G\_SOT223



5784

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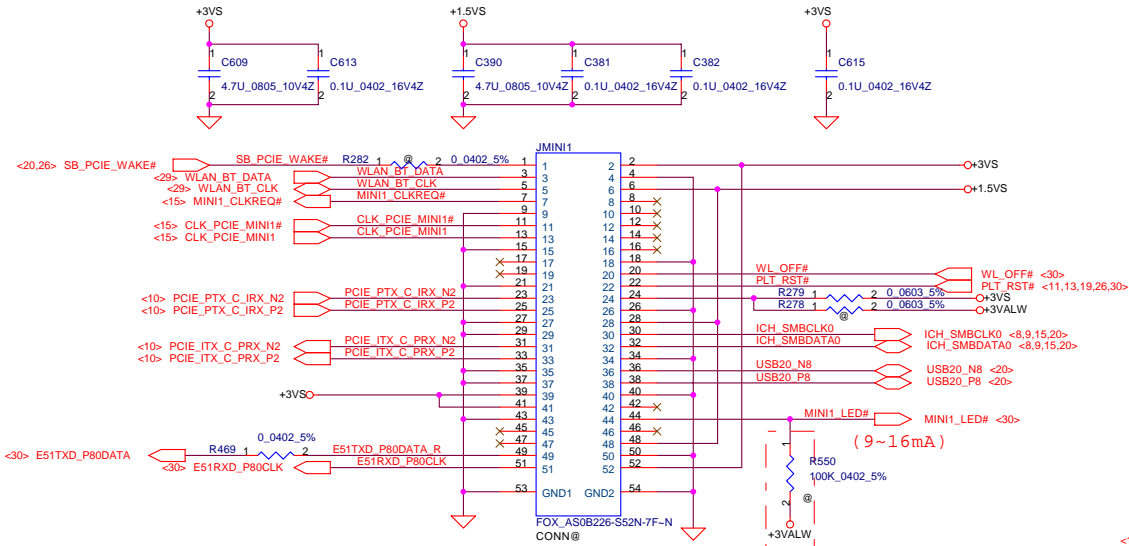
Compal Electronics, Inc.		
Title		
BCM5764M_5787M		
Size	Document Number	Rev
Custom	KBYF0 LA-5051P	0.3
Date:	Tuesday, February 03, 2009	Sheet 26 of 46



For EMI

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Size	Document Number			Rev	
B	KBYF0 LA-5051P			0.3	
Date:	Tuesday, February 03, 2009	Sheet	27	of	46

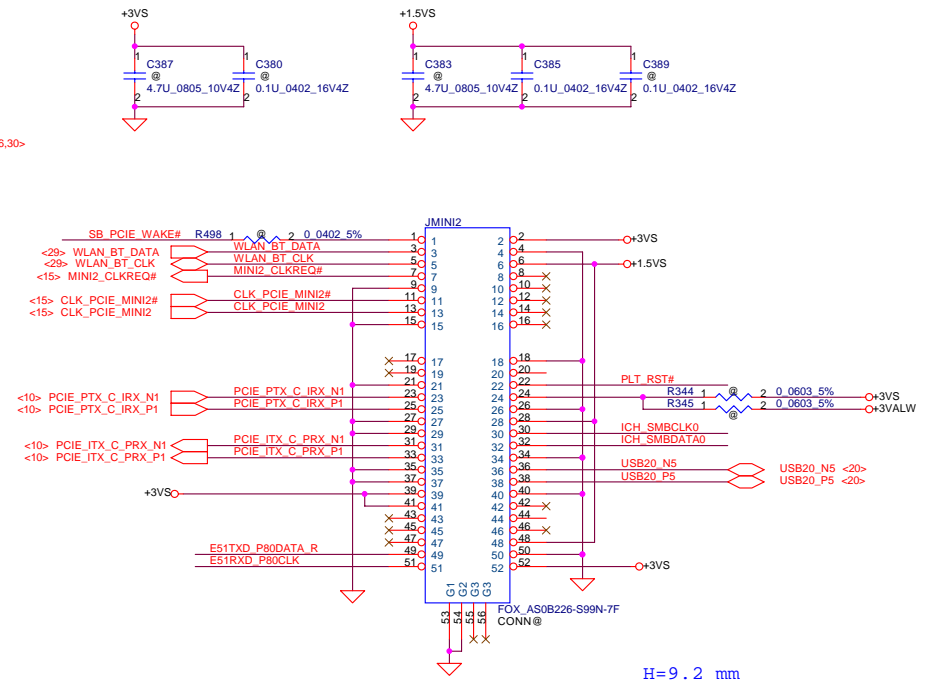
### For Wireless LAN



H=5.2 mm

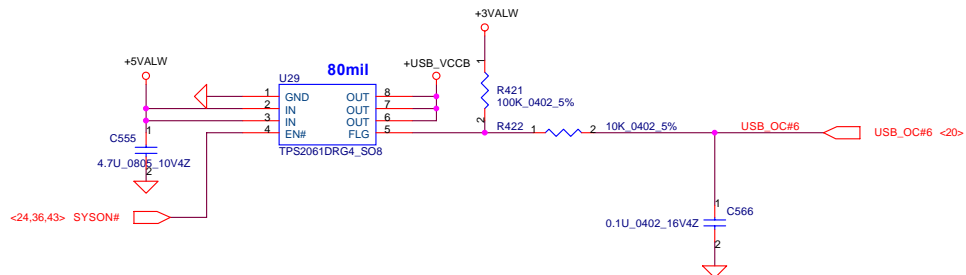
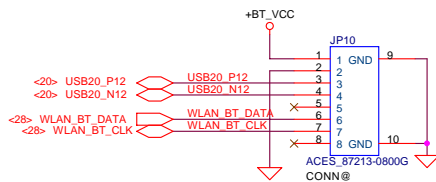
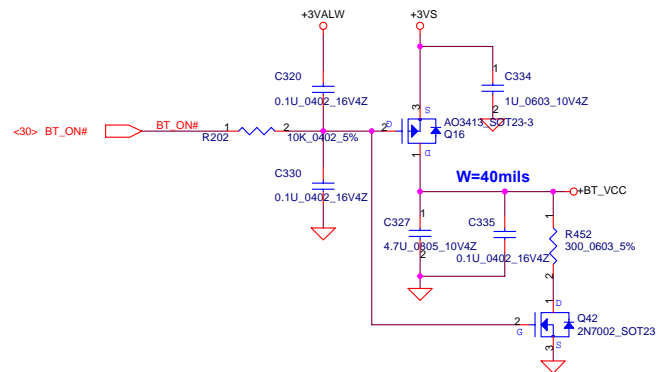
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

### For TV-Tuner/HW MPEG

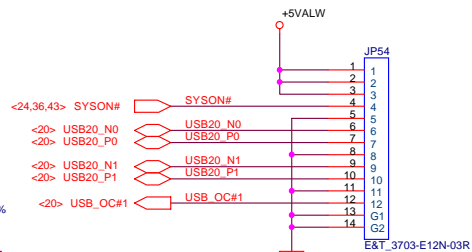


H=9.2 mm

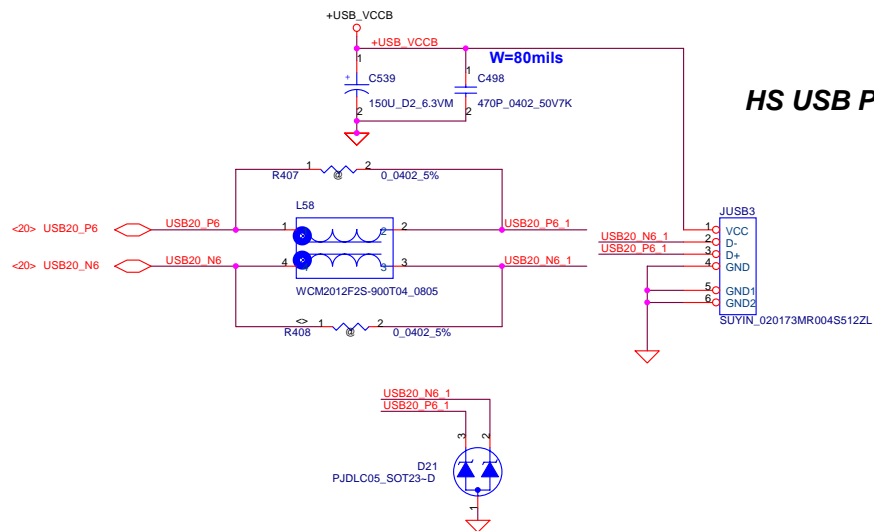
# Bluetooth Conn.



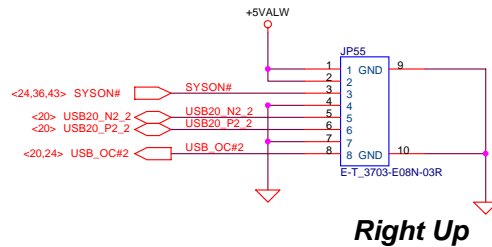
## 2 PORT



## HS USB PORT

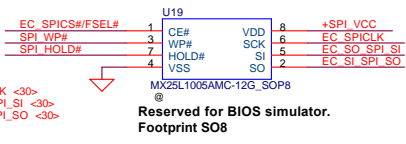
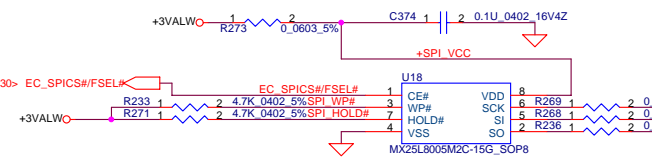


## 1 PORT FOR JV70



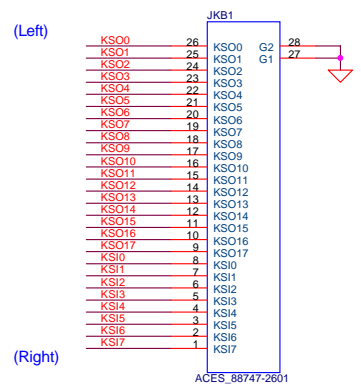
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	NEW CARD & USB Connector	
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				Date: Tuesday, February 03, 2009	Sheet 29 of 46



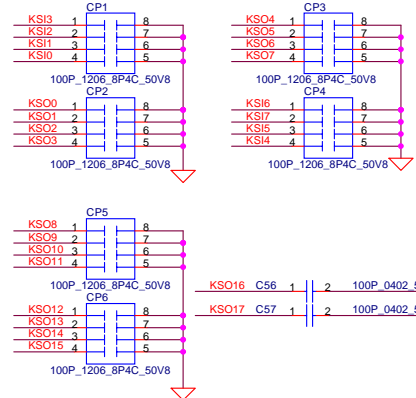


Reserved for BIOS simulator.  
Footprint S08

**INT\_KBD Conn.**

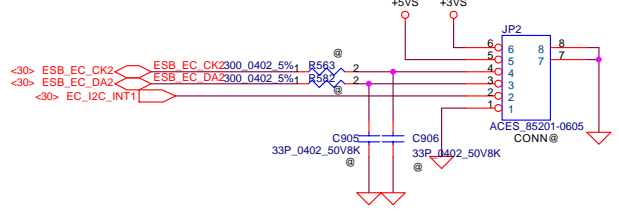


**For EMI**

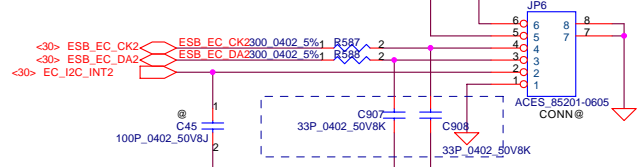


**To Media/B Conn.**

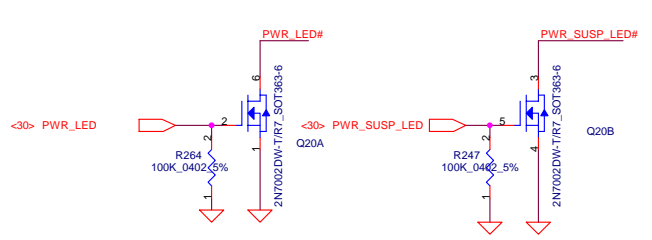
**CAP Sensor right JM70**



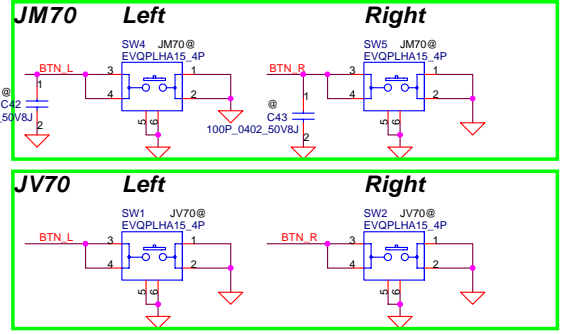
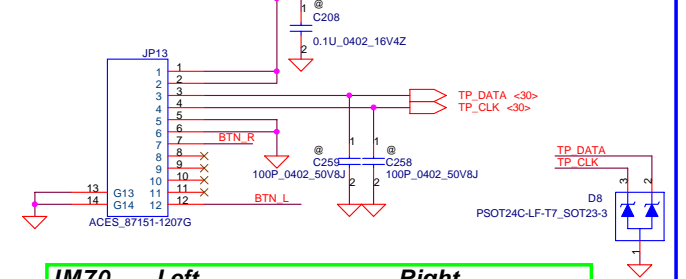
**CAP Sensor left for JM70**



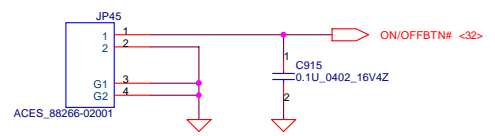
**CAP Sensor up for JV70**



**To TP/B Conn.**

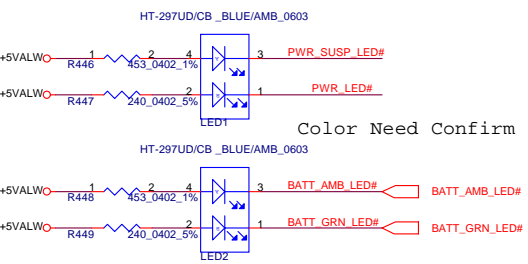
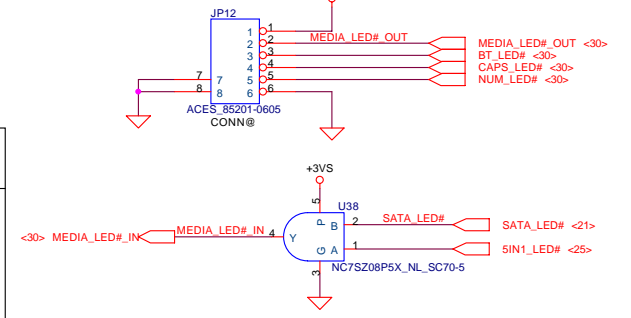


**TO POWER BTN/B for JV70**



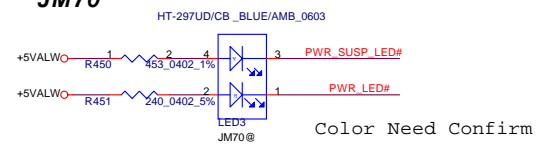
Need Check

**To LED/B Conn.**



Color Need Confirm

**JM70**

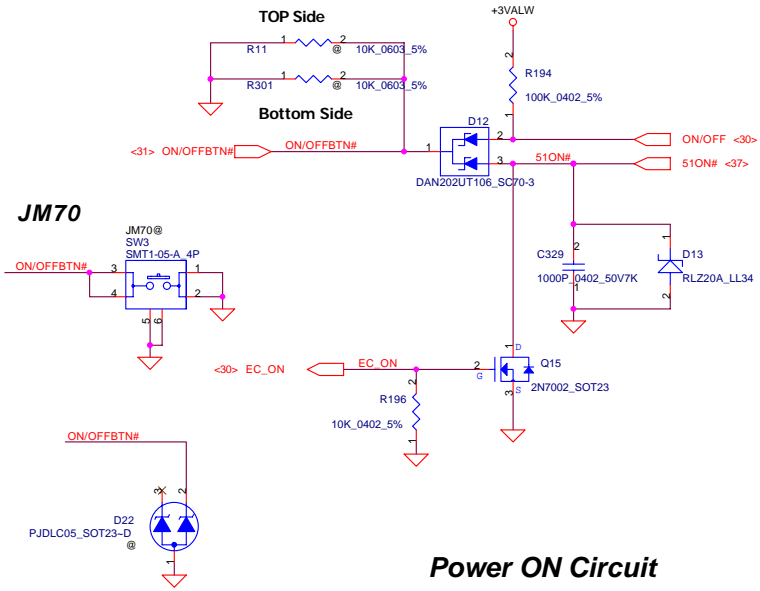


Color Need Confirm

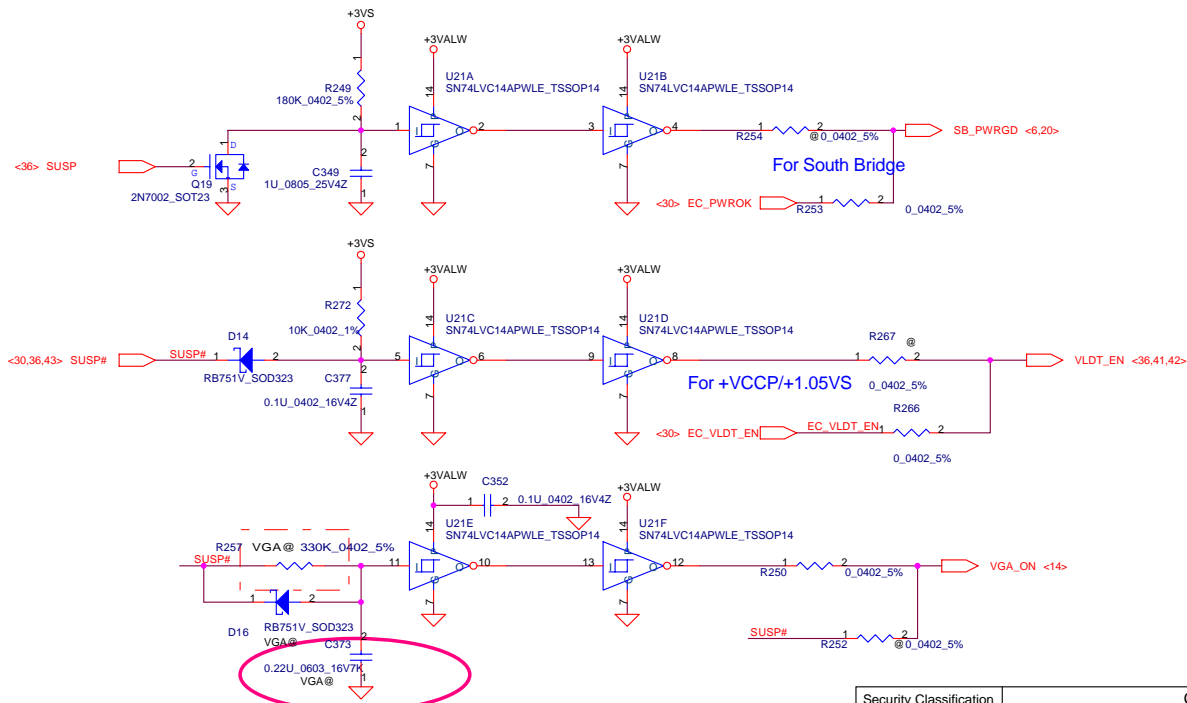
	JM70	JV70
1.	HDD	HDD
2.	BT_LED	BT_LED
3.	CAP_LED	NUM_LED
4.	NUM_LED	CAP_LED

# Power Button

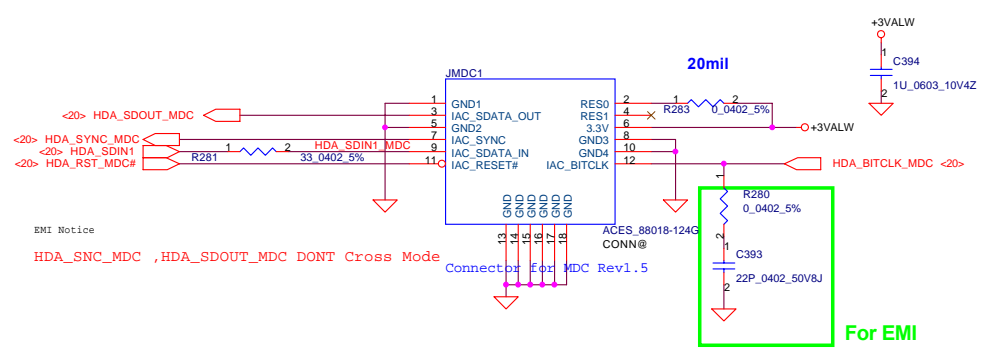
ON/OFF switch



# Power ON Circuit

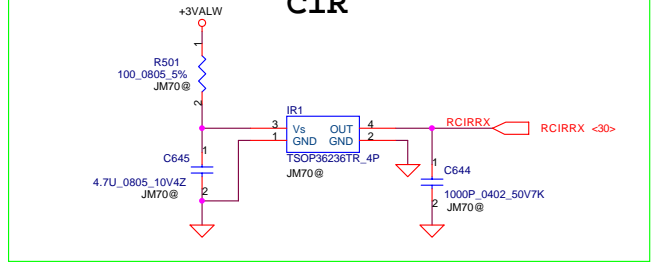


# HDA MDC Conn.



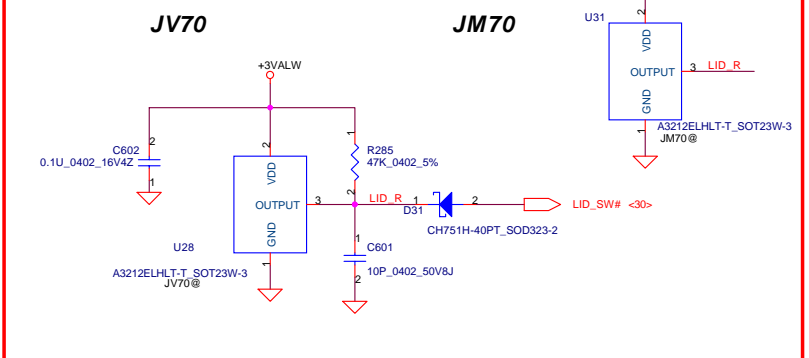
# JM70

# CIR

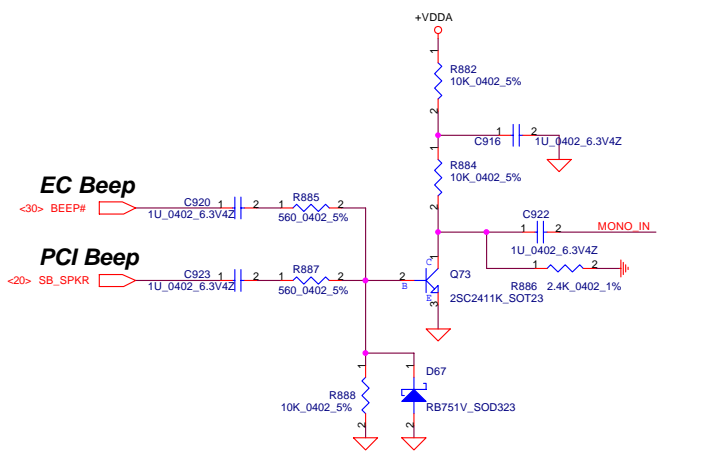


# Lid Switch

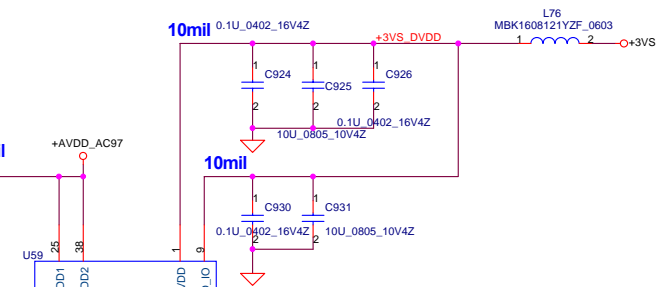
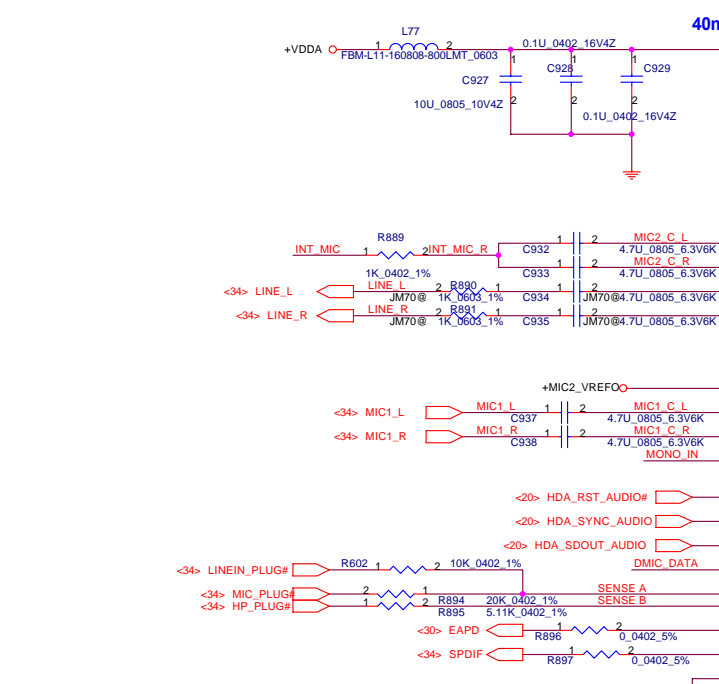
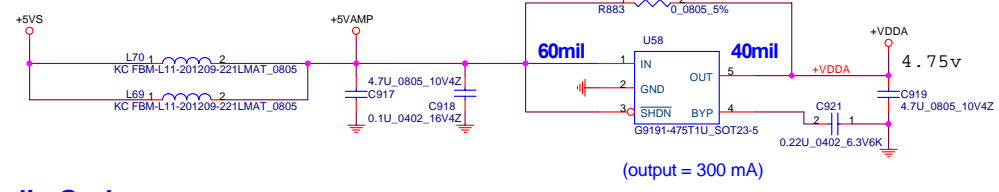
(Hall Effect Switch)



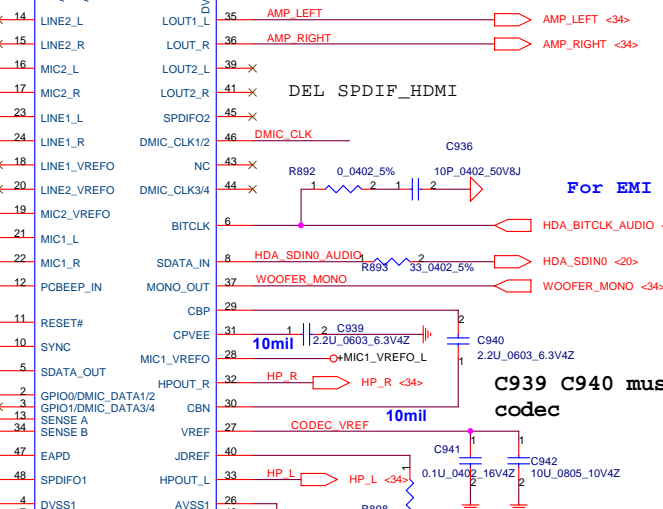
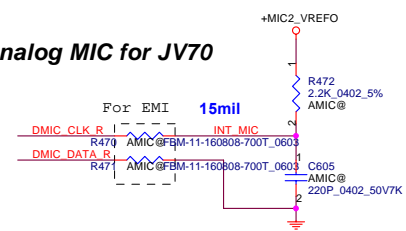
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Power OK, Reset and RTC Circuit, TP	
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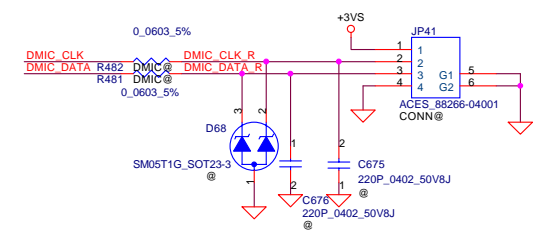
### HD Audio Codec



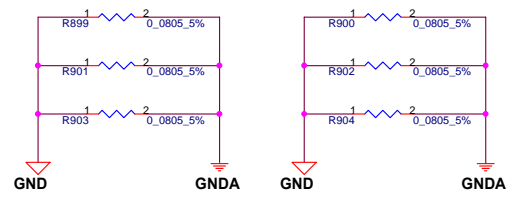
### Analog MIC for JV70



### Digital MIC for JM70 DMIC Conn.

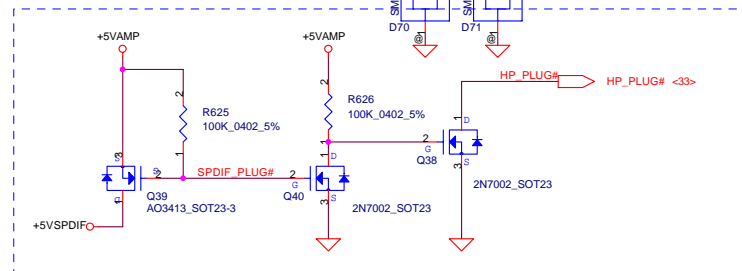
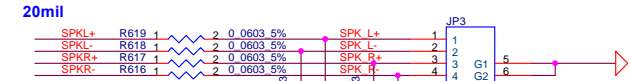
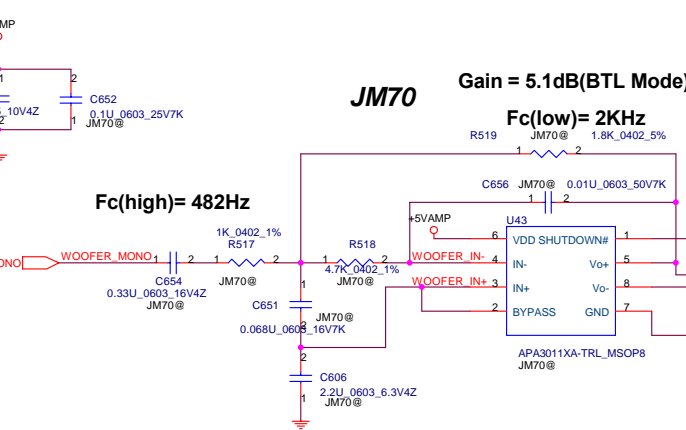
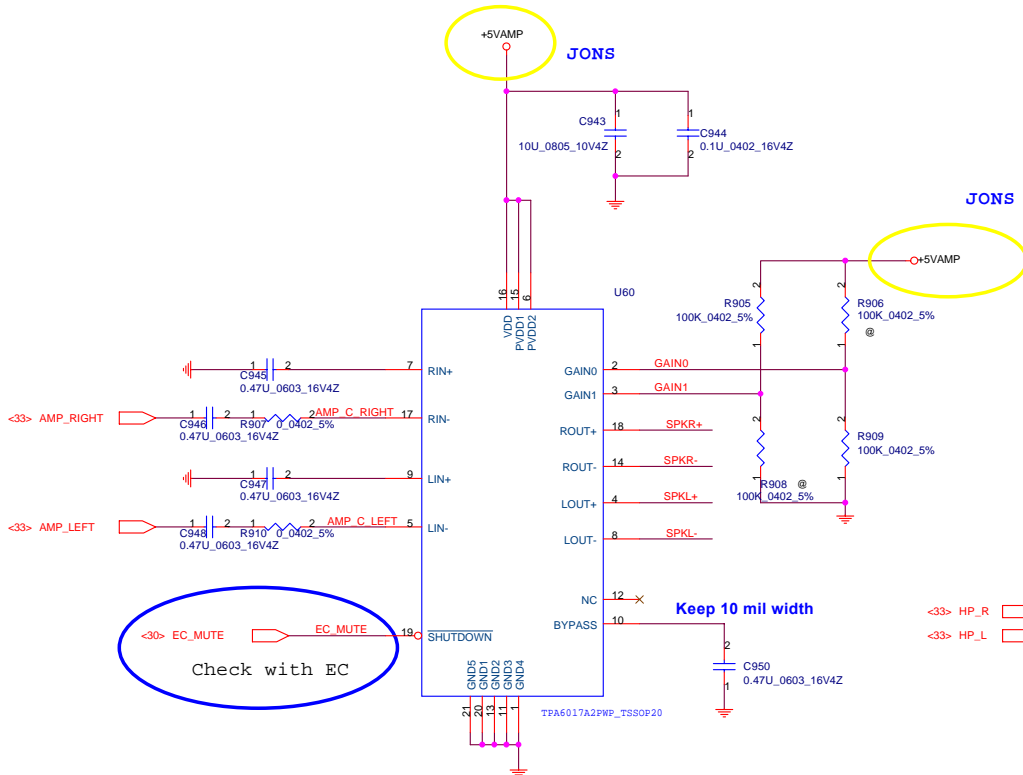


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



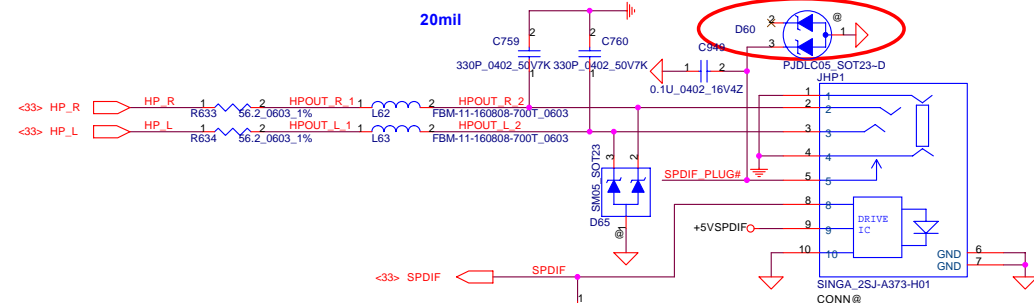
Security Classification	Compal Secret Data		Title	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	HD Audio Codec ALC268
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size B Document Number <b>KBYFO LA-5051P</b> Date: Tuesday, February 03, 2009
			Sheet 33 of 46	Rev 0.3

# Int. Speaker Conn.

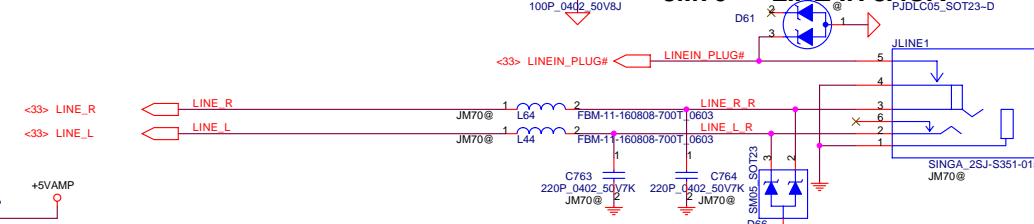


## LINE Out/Headphone Out

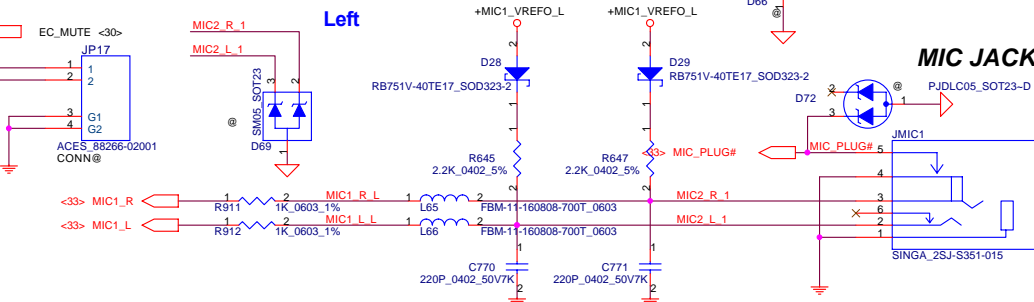
2007/12/07 S/PDIF Out JACK



## JM70 LINE-IN JACK

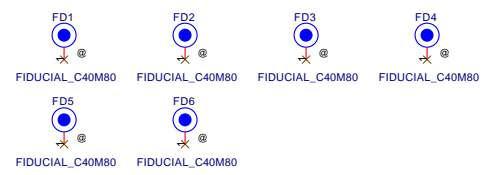
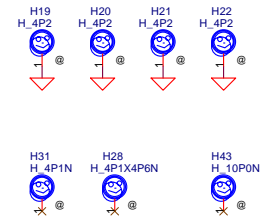
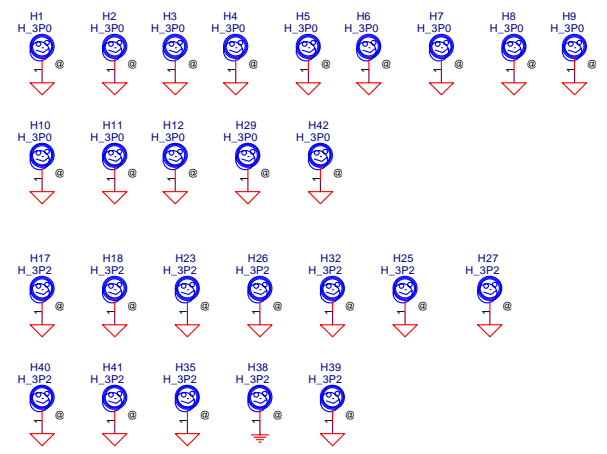
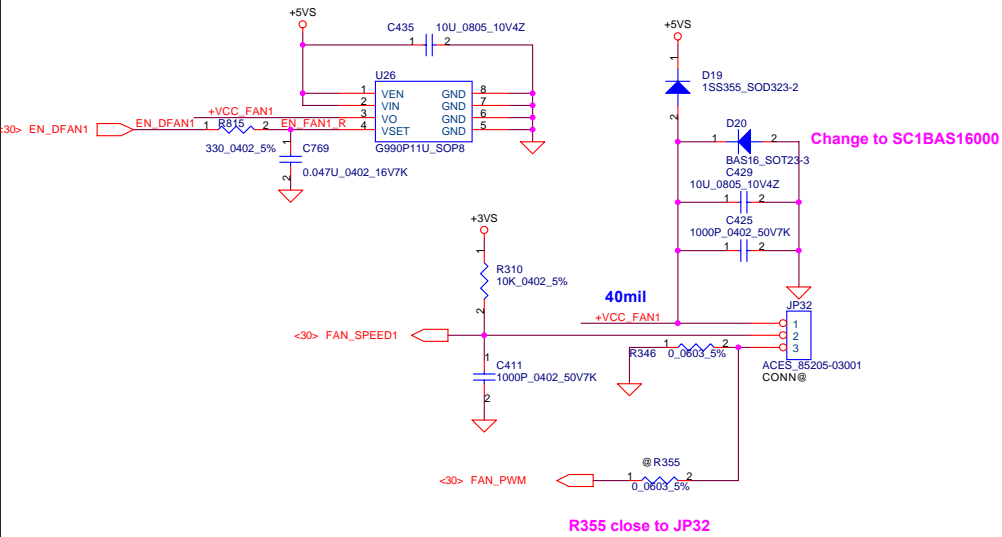


## MIC JACK



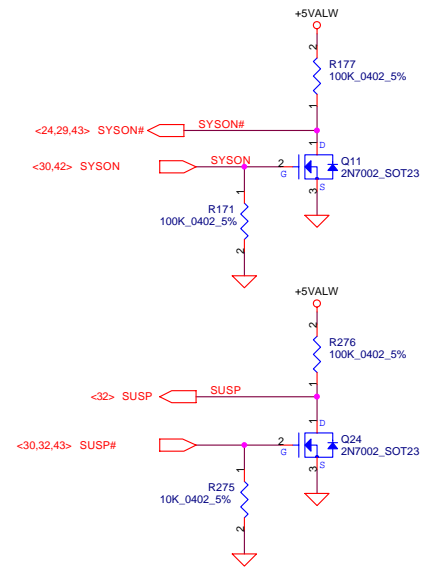
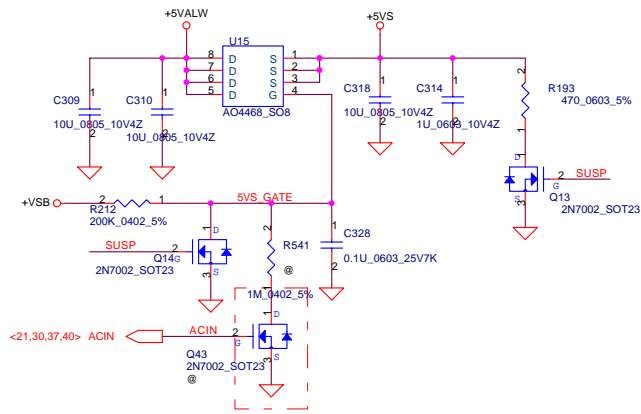
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Amplifier & Audio Jack	
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### FAN1 Conn

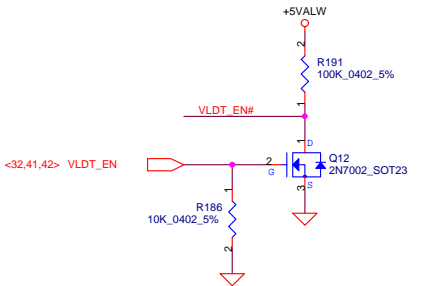
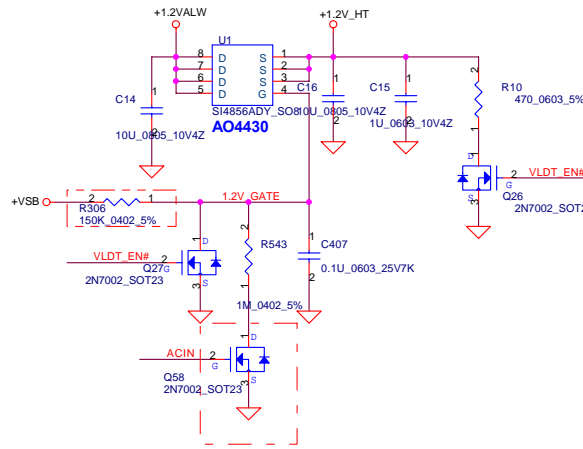
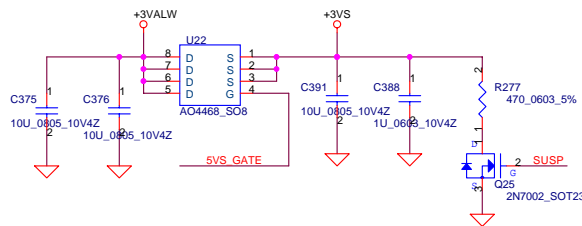


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	Title
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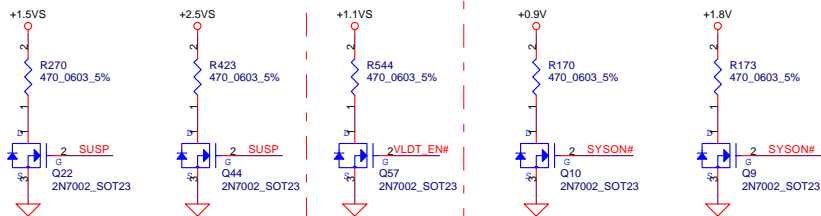
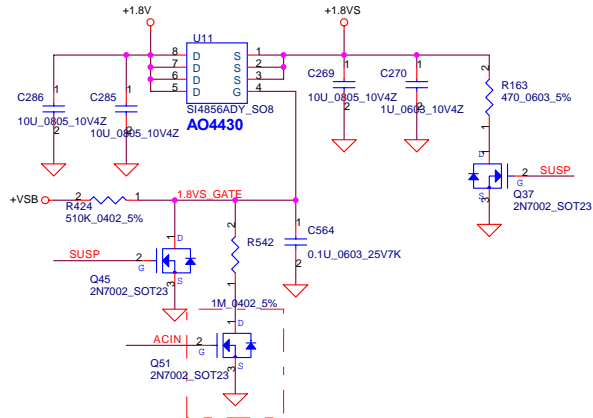
**+5VALW TO +5VS**



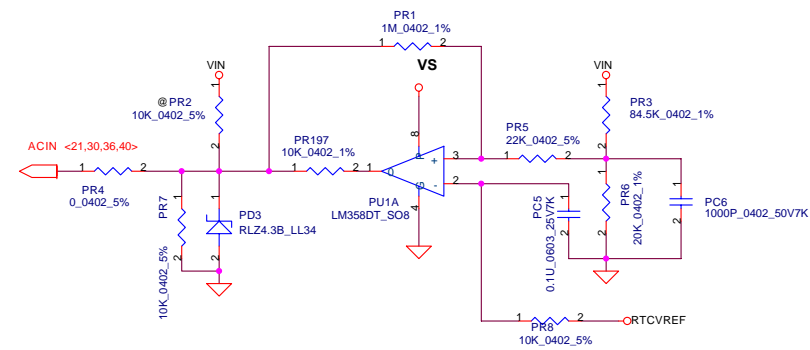
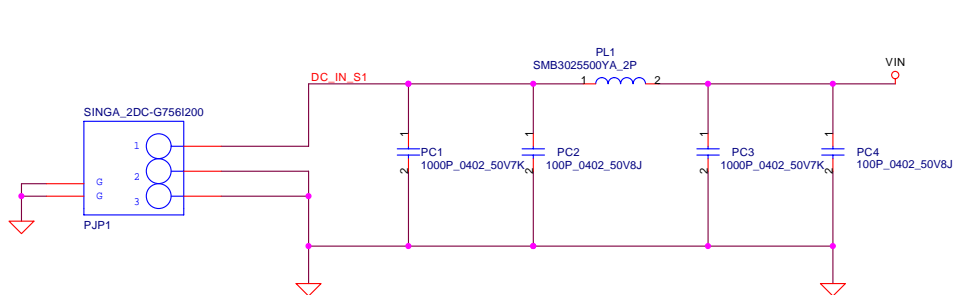
**+3VALW TO +3VS**



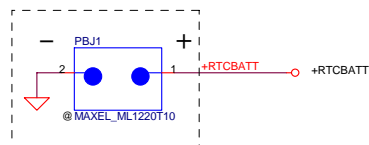
**+1.8V to +1.8VS**



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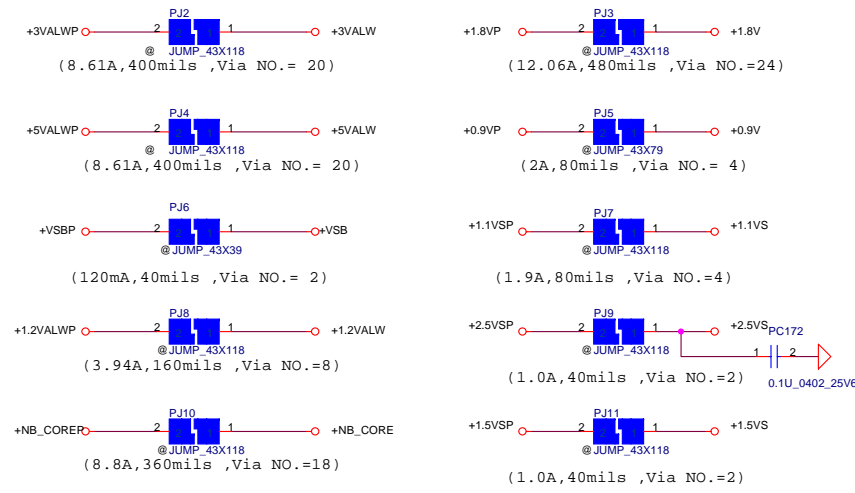
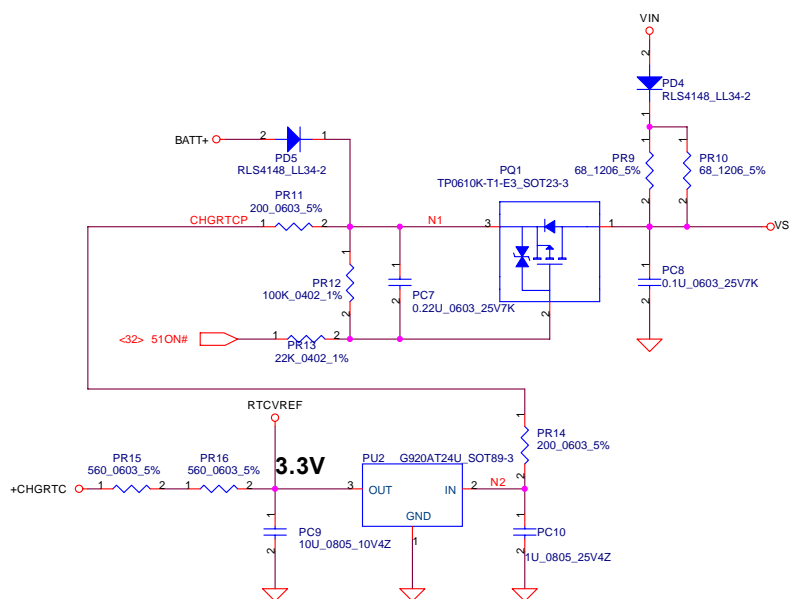


**RTC Battery**



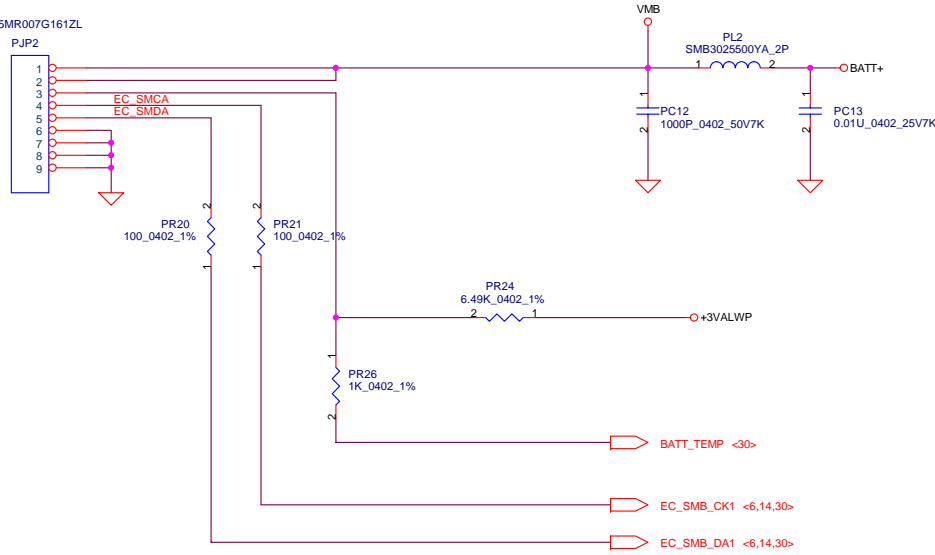
SP093MX0000

Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

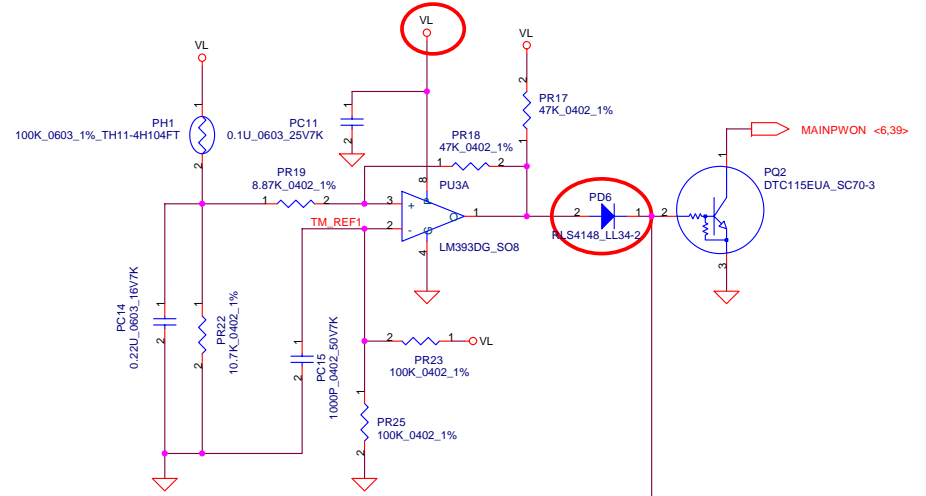


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				DCIN & DETECTOR		
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Size	Document Number		KBKC0_KBYF0		Rev	0.3
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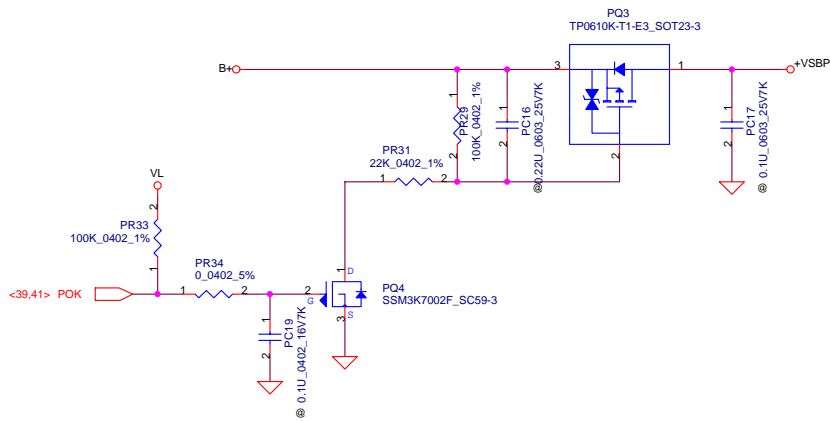
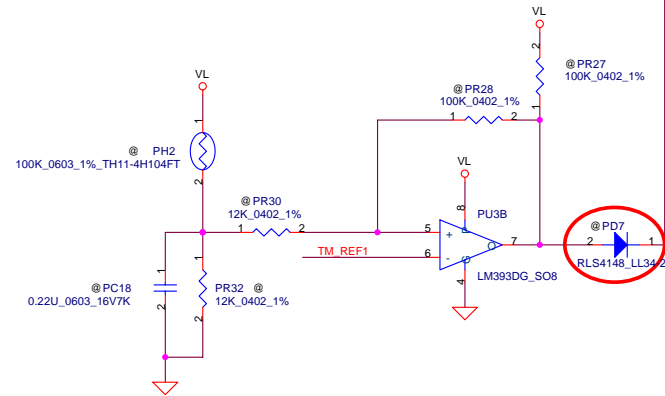
SUYIN\_200275MR007G161ZL



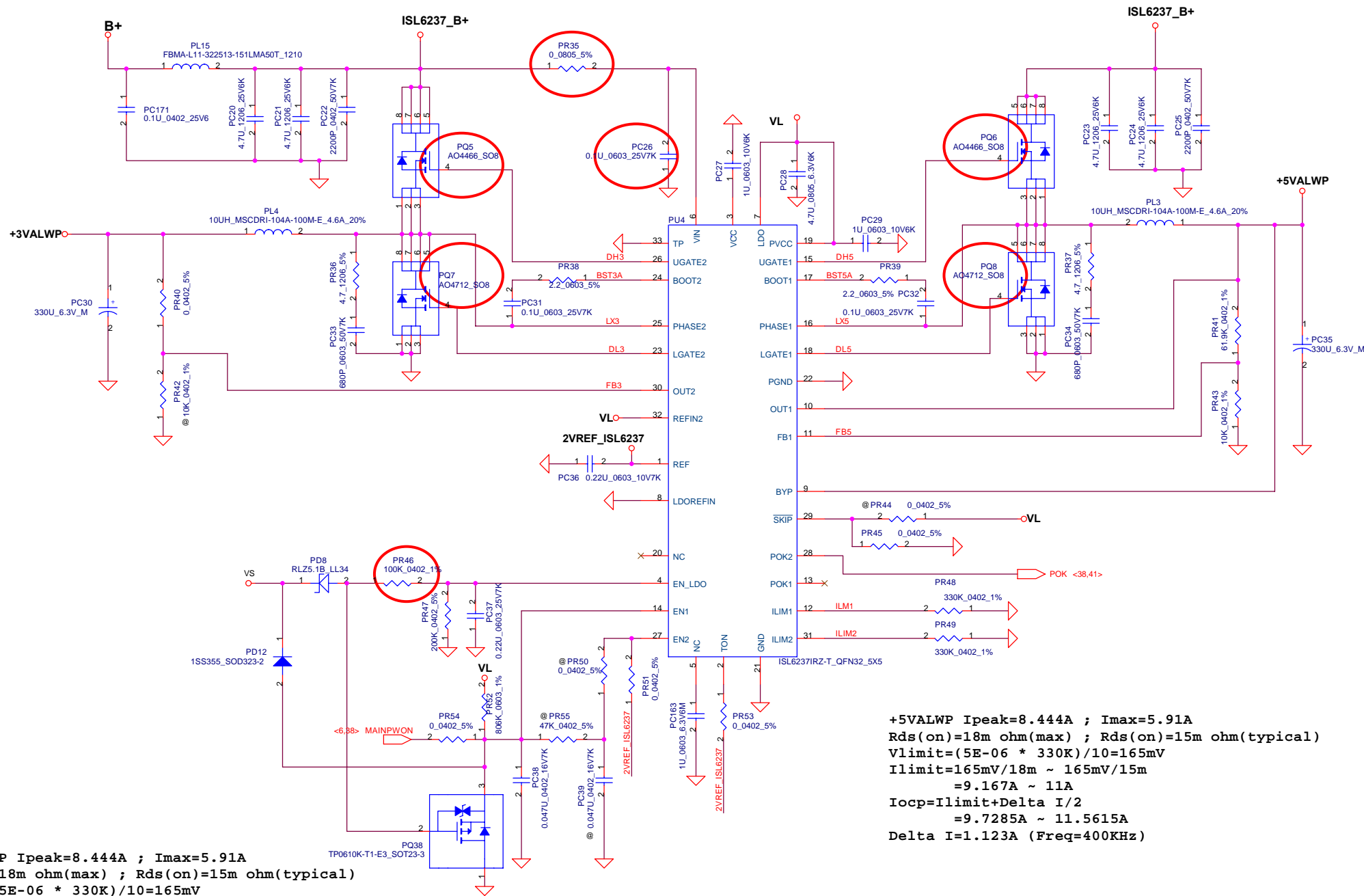
PH1 under CPU botten side :  
CPU thermal protection at 92 degree C  
Recovery at 56 degree C



PH2 near main Battery CONN :  
BAT. thermal protection at 92 degree C  
Recovery at 56 degree C



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Size	Document Number			Rev	0.3
	KBK0_KBYF0			Date:	Tuesday, February 03, 2009
				Sheet	38 of 46

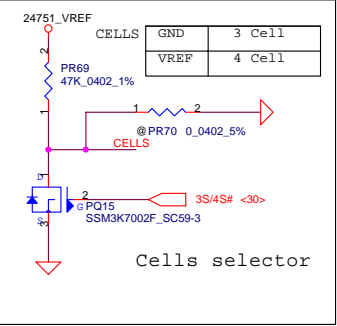


**+5VALWP Ipeak=8.444A ; Imax=5.91A**  
**Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)**  
**Vlimit=(5E-06 \* 330K)/10=165mV**  
**Ilimit=165mV/18m ~ 165mV/15m**  
**=9.167A ~ 11A**  
**Iocp=Ilimit+Delta I/2**  
**=9.7285A ~ 11.5615A**  
**Delta I=1.123A (Freq=400KHz)**

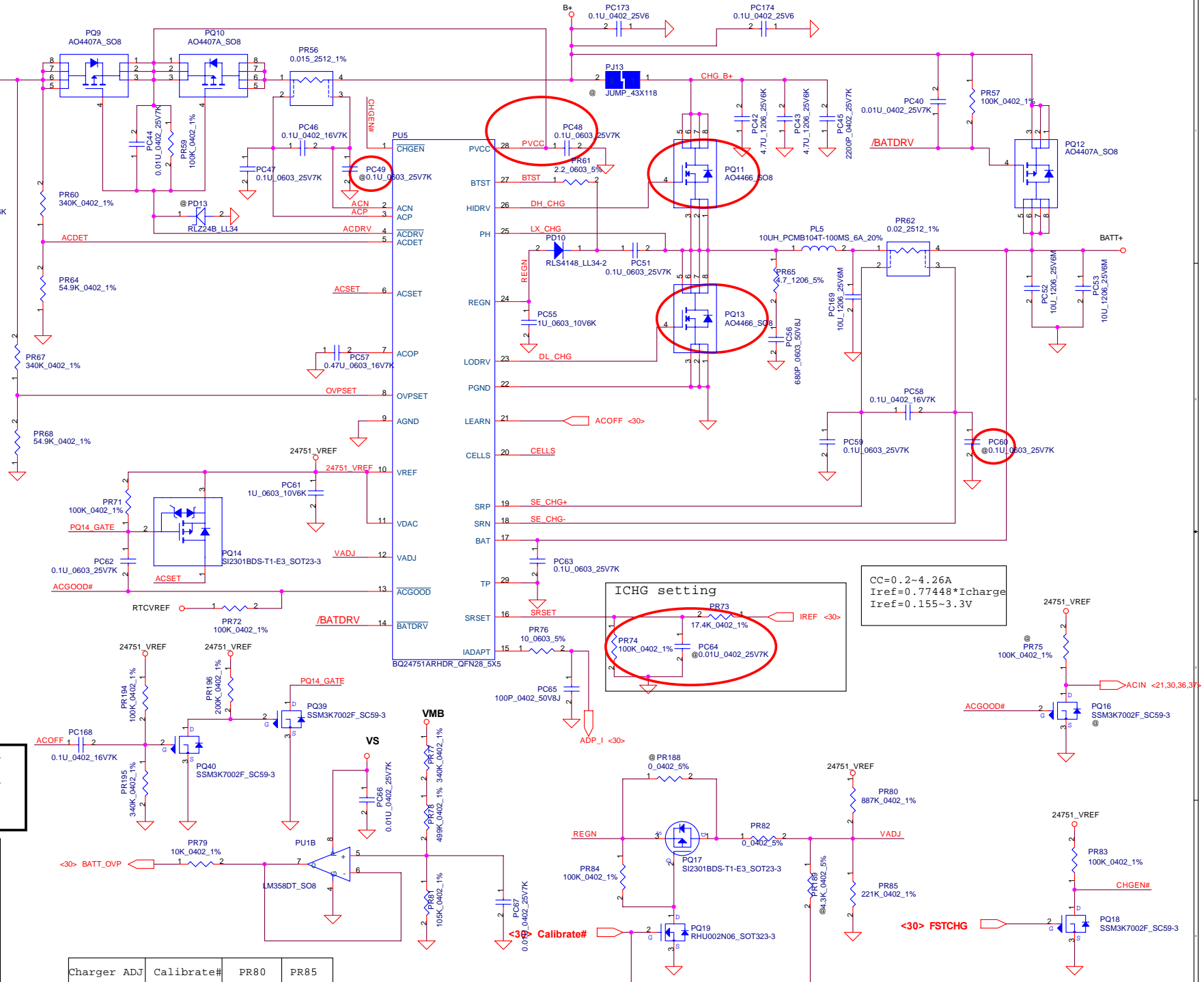
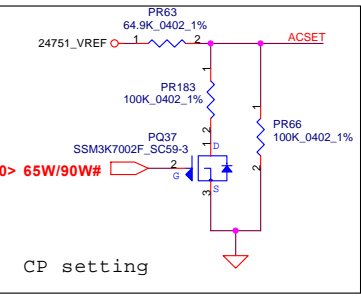
**+3.3VALWP Ipeak=8.444A ; Imax=5.91A**  
**Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)**  
**Vlimit=(5E-06 \* 330K)/10=165mV**  
**Ilimit=165mV/18m ~ 165mV/15m**  
**=9.167A ~ 11A**  
**Iocp=Ilimit+Delta I/2**  
**=9.721A ~ 11.554A**  
**Delta I=1.108A (Freq=300KHz)**

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				of	46

$I_{charge} = (V_{rsset}/V_{vdac}) * (0.1/PR36)$   
 90W adapter  
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR48) = 4.04A$   
 65W adapter  
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR48) = 2.90A$   
 Input OVP : 22.3V  
 Input UVP : 17.26V  
 Fsw : 300KHz



**LI-3S : 13.5V --- BATT-OVP = 1.5V**  
**LI-4S : 18V --- BATT-OVP = 1.998V**  
**BATT-OVP = 0.111 \* BATT+**



**IChg setting**  
 $PR74 = 100K_0402_1\%$   
 $PC64 @ 0.01U_0402_25V7K$   
 $PR73 = 17.4K_0402_1\%$   
 $IREF <30>$

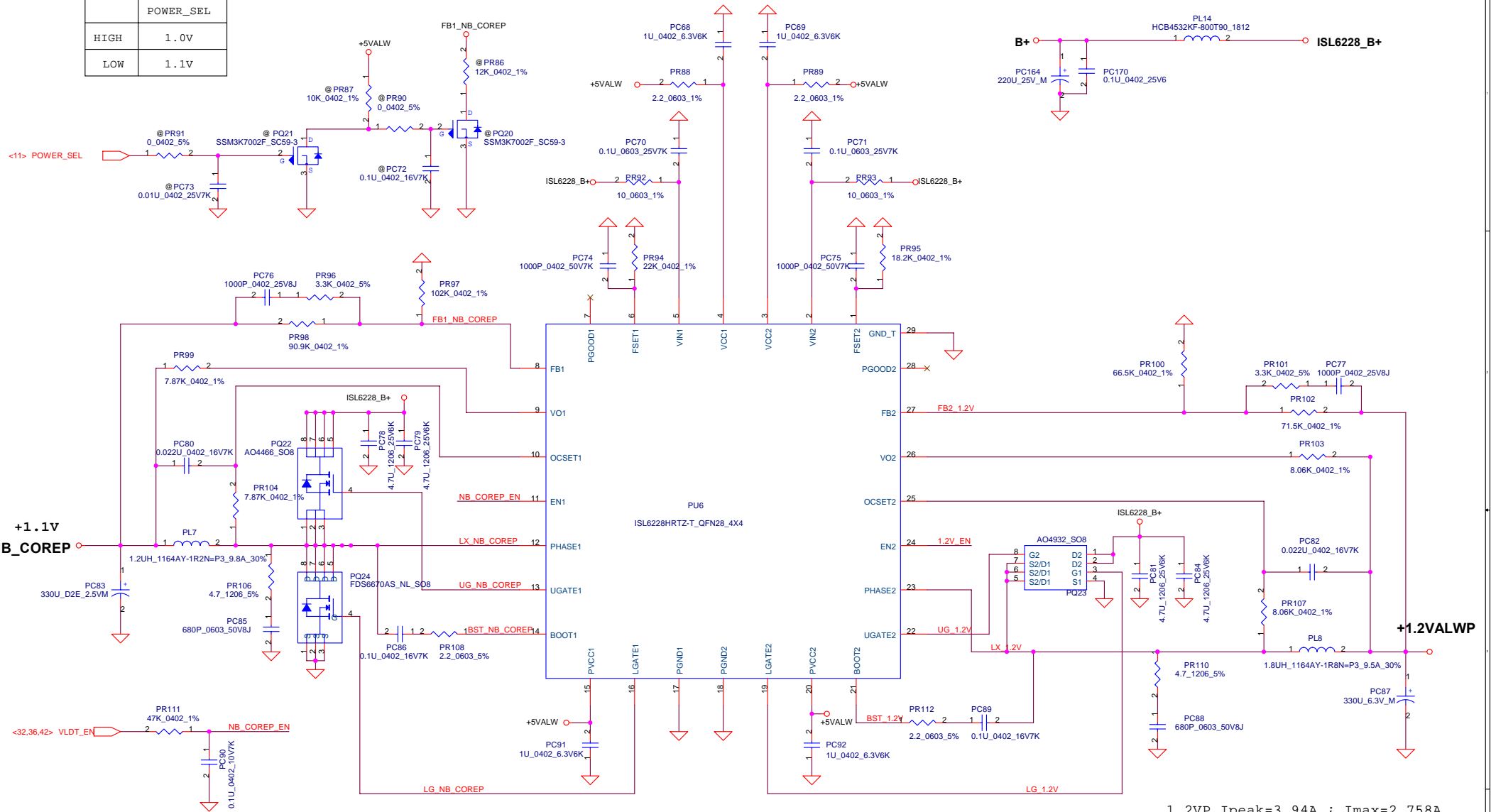
$CC = 0.2 - 4.26A$   
 $I_{ref} = 0.77448 * I_{charge}$   
 $I_{ref} = 0.155 - 3.3V$

Charger ADJ	Calibrate#	PR80	PR85
4.0V	L	@	0
4.1V	L	887K	221K
4.2V	H	887K	221K

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<b>CHARGER</b>			
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	POWER_SEL
HIGH	1.0V
LOW	1.1V



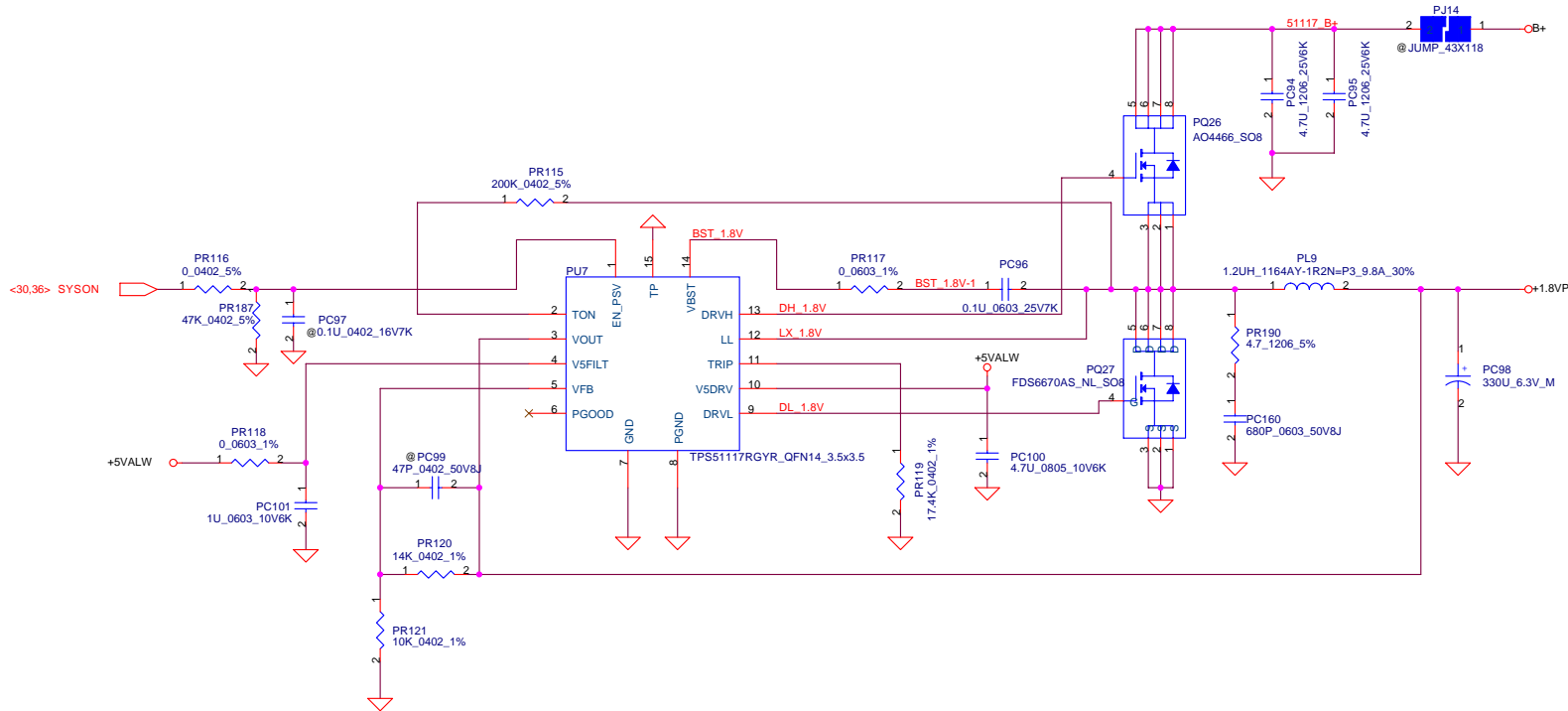
1.1VP Ipeak=8.9A ; Imax=6.23A  
 DCR=6m ohm (max)  
 $Rocset=(Iocp*DCR)/10E-06=7.68K\ ohm$   
 $Iocp=9.846A(1.3*DCR)$   
 $Csen=L/(Rocset*DCR)=0.022uF$

Freq=303KHz  
 $Rfset=1/(1.5E-10 * Freq)=22K$

1.2VP Ipeak=3.94A ; Imax=2.758A  
 DCR=10m ohm (max)  
 $Rocset=(Iocp*DCR)/10E-06=6.65K\ ohm$   
 $Iocp=5.542A(1.2*DCR)$   
 $Csen=L/(Rocset*DCR)=0.027uF$

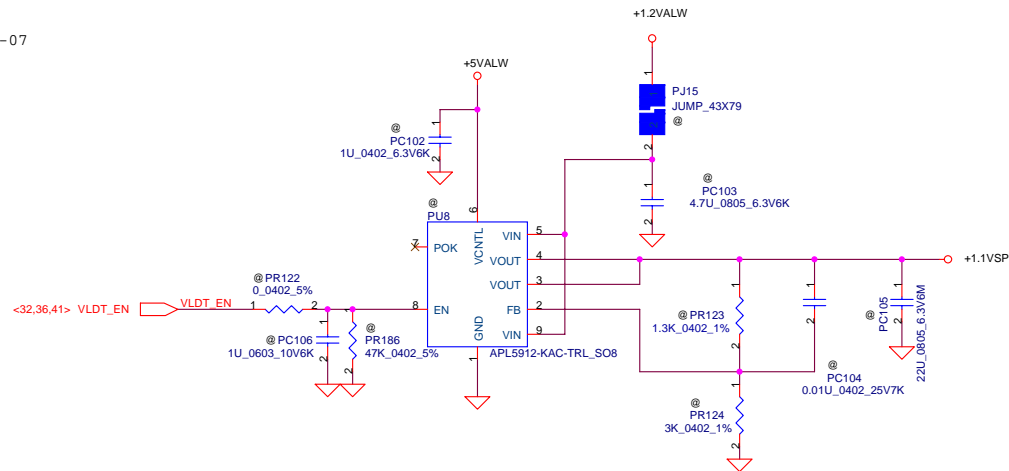
Freq=366KHz  
 $Rfset=1/(1.5E-10 * Freq)=18.2K$

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Title	NB_COREP / 1.2VSB			Rev
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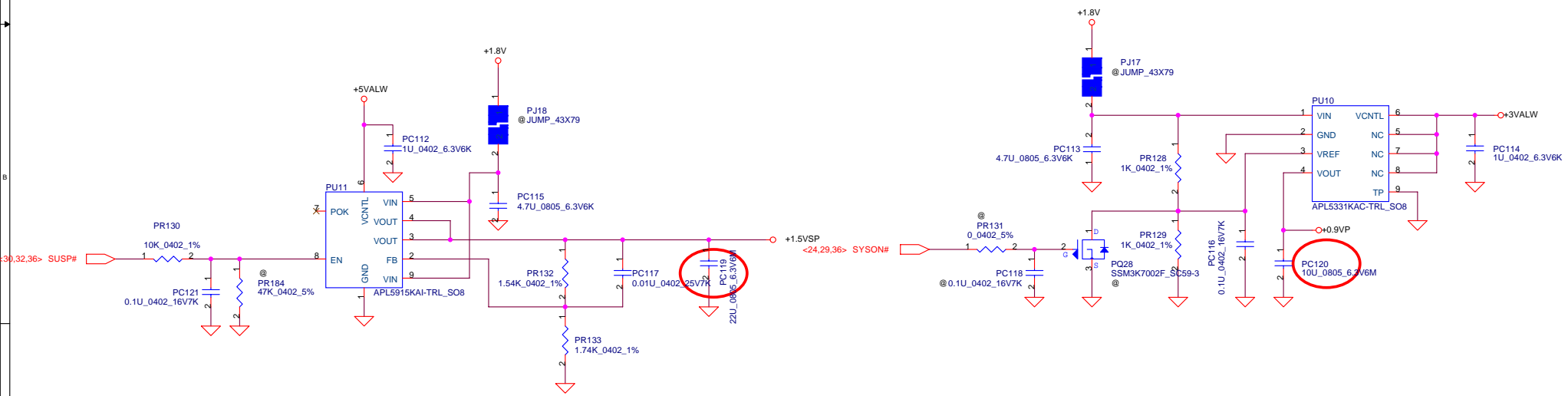
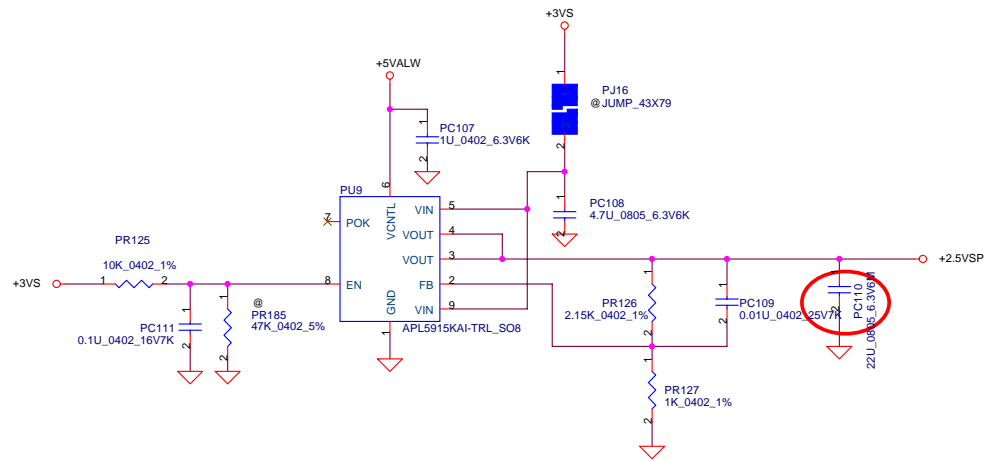


$VFB=0.75V$   
 $V_o=VFB*(1+PR120/PR121)=1.8V$   
 $Ton=19E-12*Ron*((2/3)*Vo+100mV)/(Vin)+50ns=3.1E-07$   
 $Freq=305KHz$

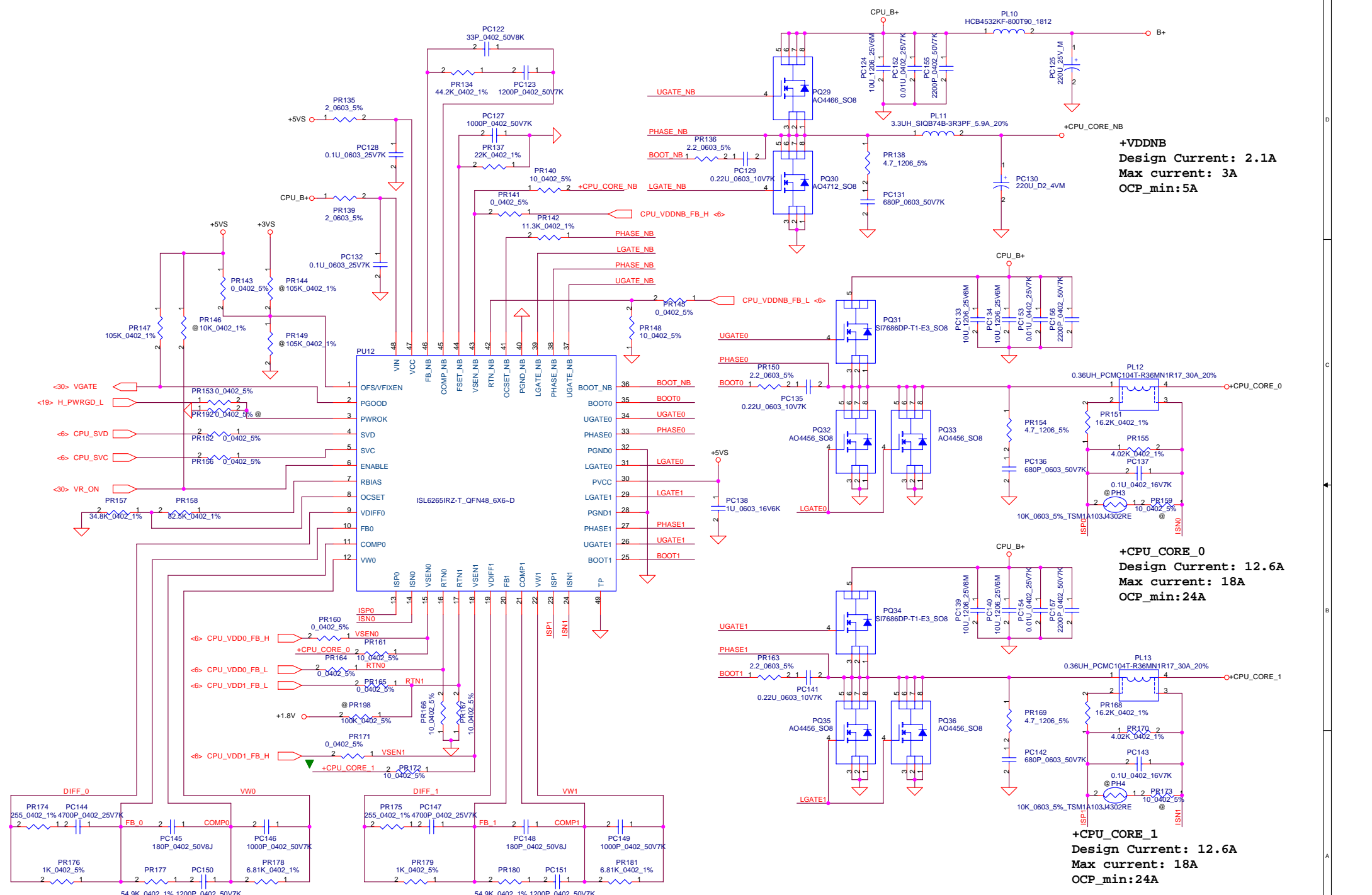
$Cesr=15m\ ohm$   
 $I_{peak}=12.6A\ I_{max}=8.82A$   
 $\Delta i=((19-1.8)*(1.8/19))/(L*Freq)=5.332A$   
 $V_{trip}=R_{trip}*10\mu A=0.24V$   
 $I_{ocp-min}=V_{trip}/R_{ds(on)max}*1.4+2.666=17.573A$   
 $I_{ocp-max}=V_{trip}/R_{ds(on)typ}*1.2+2.666=26.908A$   
 $I_{ocp}=17.573-26.908A$



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**+VDDNB**  
**Design Current: 2.1A**  
**Max current: 3A**  
**OCp\_min:5A**

**+CPU\_CORE\_0**  
**Design Current: 12.6A**  
**Max current: 18A**  
**OCp\_min:24A**

**+CPU\_CORE\_1**  
**Design Current: 12.6A**  
**Max current: 18A**  
**OCp\_min:24A**

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EMI request.	EMI request.	0.1	40	Change PR38, PR39, PR108, PR112, PR136, PR150, PR163 from SD013000080 to SD013220B80.	08, 12/24	to DVT
2	EMI request.	EMI request.	0.1	40	Add PC170, PC171, PC172, PC173, PC174 SE000000G880 S CER CAP 0.1U 25V K X5R 0402	08, 12/24	to DVT
3	EMI request.	EMI request.	0.1	39	Add PL15 SM010016410 S SUPPRE_ KC FBMA-L11-322513-151LMA50T	08, 12/24	to DVT
4	EMI request.	EMI request.	0.1	41	Add PL14 SM010018210 S SUPPRE_ TAI-TECH HCB4532KF -800T90 1812	08, 12/24	to DVT
5	Link CIS error.	Link CIS error.	0.1	40	Change PQ9, PQ10, PQ12 from SB944070000 S TR AO4407 1P SO8 W/D to SB000000DL00 S TR AO4407A 1P SO8	08, 12/24	to DVT
6	cost down	cost down	0.1	40	Change PC30 from SGA19331360 S POLY C 330U 6.3V M D3L ESR25M TPE H2.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
7	cost down	cost down	0.1	40	Change PC35 from SGA20151320 S POLY C 150U 6.3V M D2E TPE ESR18 H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
8	cost down	cost down	0.1	41, 42	Change PC87, PC98 from SGA19331D00 S POLY C 330U 2.5V D2 TPE LESR15M H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
9	schematic update.	schematic update.	0.1	44	Delete PR198 SD028100380 S RES 1/16W 100K +-5% 0402	08, 12/24	to DVT
10	layout space too small.	layout space too small.	0.1	41	Change PQ23 from SB00000CG00 S TR AO4466 1N SO8 to SB00000BG00 S TR AO4932 2N SO8 Delete PQ25 SB00000AJ00 S TR AO4712 1N SO8	08, 12/24	to DVT
11							
12							
13							
14							
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16							
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18							

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				PIR List	
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
12/17		p.12	L3,L4 change from bead to 0 Ohm	
12/17		P.17	Add R858~R865 for VGA HDMI	
12/17		P.18	R374,R375,R376 change from 0 ohm to 10 ohm	
12/17		P.20	R50 ,R53 change from JV70@ to @	
12/17		P.20	R51 ,R52 change from JM70@ to JV70@	
12/17		P.24	JP18 change from ESATA to USB port	
12/17		P.25	R396 change from 10K to 0 Ohm	
12/17		P.31	C905~C907 change from 0.1u to 33P	
12/17		P.31	U19 change from mount to @ ; U18 change from @ to mount	
12/17		P.32	D22 change from mount to @	
12/18		P.24	SATA re-driver IC reserved	
12/22		P.8	Add c124,c128,c151,c155,c55,c119,c113,c197 0.1uF	EMI request
12/22		P.30	Add c40 c41 100P	EMI request
12/22		P.30	Add c42,c43,c45	EMI request
12/22		P.37~p.45	upgrade PWR schematic	
12/22		P.30	Add C65 22uF for CRT flicker	
12/23		P.21	Delete R174,R175	
01/16		P.16	Add r611,r612 connect to INVT_PWM	Vari-Bright reserved
01/16		P.11	Add r347 connect to BKOFF#	Vari-Bright reserved
01/16		P.30	add r288 BKOFF# 4.7k pull low	

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