Compal Confidential

NAT02 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2009-11-26

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

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Title: **Cover Page**

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Block Diagram
Compal confidential
Model : NAT01

FFS
+3VS
P.14

FAN
+5VS
+3VS
P.14

Intel Arrandale (UMA) Processor rPGA988A
+CPU_CORE
+1.1VS_VTT
page 5,6,7,8,9,10

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
48MHZ to CardReader page 13

CPU XDP
133MHz
page 06

Memory BUS(DDRIII)
Dual Channel
1.5V DDRIII 800/1066/1333
6.4G/8.5G/10.6G
100M/133M/166M(CFD)

DDRIII-DIMM X2
BANK 0, 1, 2, 3, 4 ,5 ,6 ,7 ,8
+1.5V
P.11,12
+0.75VS

CRT CONN
+5VS
P.35
VGA

LVDS CONN
+LCDVDD
+3.3V_ALW
P.35
LVDS

DP CONN
+5VS
P.37
DPD

HDMI CONN
+5VS
P.36
DPB

HDMI Level Shift
P.36

FDI x8 (UMA)
100MHz
2.7GT/s

DMI x4
100MHz
1GB/s x4

Intel Ibex Peak-M PCH
+1.05VS
page 15,16,17 18,19, 20,21,22,23

100MHz

PCI-Express x 8 (ABD PCIE1 2.5GT/S CKD PCIE1/2 2.5/5GT/S)

USBx14 3.3V 48MHz
SATA x 6 100MHz
(GEN1 1.5GT/S ,GEN2 3GT/S)
HD Audio 3.3V 24MHz

Right Front Side.
USB Port X1
+5V_ALW
P.30
To Card-reader subboard

Right behind side.
USB Port1 X1
+5V_ALW
P.30
To Single USB subboard

Bluetooth
P.30

Touch Screen
P.32

Camera
P.30

Charge USB/E-SATA Ports X1
+5VALW
P.30
port 5

SPI

SPI ROM x1
32Mbit
page 15

LPC BUS
+3VS
33MHz

To Card-reader subboard
P.30

8 IN 1 CONN
+3VS

IEEE1394

CardBus OZ888GS0
+3VS
+1.8VS

Express Card
P.28
PCI Express BUS

RJ45

RTL8111DL
+3VALW
P.24

ENE KBC KB926QFD3
+RTC_CELL
+3VALW
P.31

SB3526
+3VS
page 32
To Cap Sensor subboard

SPI

Int.KBD & BL
P.32

Touch Pad
P.32

Flash ROM
P.31
16Mx1sector

port 4
E-ODD
+3VS
+5VS
P.29

port 0
S-HDD-2
+5VS
P.29

port 1
S-HDD-1
+5VS
P.29

Azalia Codec 92HD73C
+3VS
+VDDA
P.25

AMP MAX9736A
B+
P.26

Speaker

AMP MAX9736A
B+
P.26

Subwoofer

AMP MAX4411x2
P.25

Dig. MIC
P.30

HeadPhone & MIC Jack
+3VS
P.25

PCIE3
Mini Card 3 TV Tuner
+3VS
+1.5VS
P.28
USB[x]

PCIE2
Mini Card 2 WLAN
+3VS
+1.5VS
P.27
USB[x]

PCIE1
Mini Card 1 WWAN
+3VS
+1.5VS
P.27
USB[x]

DC/DC Interface
P.33

BATT IN
P.47

VCORE
P.46

1.5V/0.75V
P.44

Power Sequence

1.1VS_VTT
P.45

CHARGER
P.41

3V/5V
P.42

DC IN
P.40

GFX_Core/1.05V
P.48

1.05V/1.8V
P.43

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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Graphic	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.1VS	1.1V power rail for PCIE of GUP	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
B+_BIAS	B+ always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%	
Ra	100K +/- 1%	

Board ID	VGA	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
X00	M96	0	0 V	0 V	0.100 V
X01	M96	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
X02	M96	18K +/- 1%	0.436 V	0.503 V	0.538 V
MP	M96	33K +/- 1%	0.712 V	0.819 V	0.875 V
X00	Madison	56K +/- 1%	1.036 V	1.185 V	1.264 V
X01	Madison	100K +/- 1%	1.453 V	1.650 V	1.759 V
X02	Madison	200K +/- 1%	1.935 V	2.200 V	2.341 V
MP	Madison	NC	2.500 V	3.300 V	3.300 V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
WWAN	
WLAN	
Express Card	

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3191AKLFT, SLG8SP585)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
Free Fall Sensor	
CPU XDP	
PCH XDP	remove
XDCP_ISL90727	0101 110Xb
XDCP_ISL90728	0111 110Xb

USB Port Table

USB Port	Device
0	USB&ESATA
1	Reader/BD
2	USB board
3	WPAN
4	WLAN
5	WWAN
6	NC
7	NC
8	Express
9	Touch screen
10	Bluetooth
11	Camera

BTO Option Table

BTO Item	BOM Structure

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Title: Notes List

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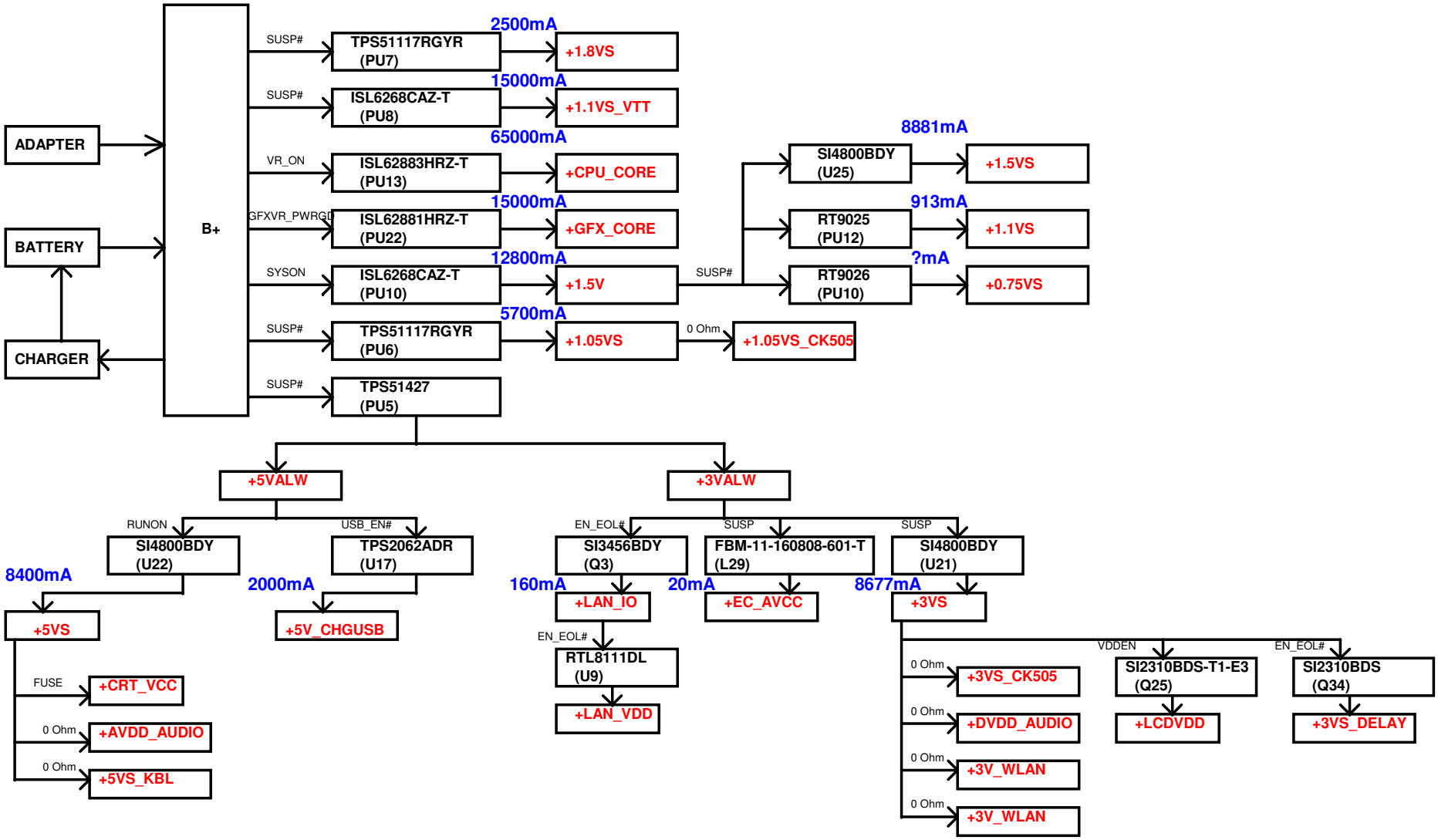

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Title: **Power Rail**

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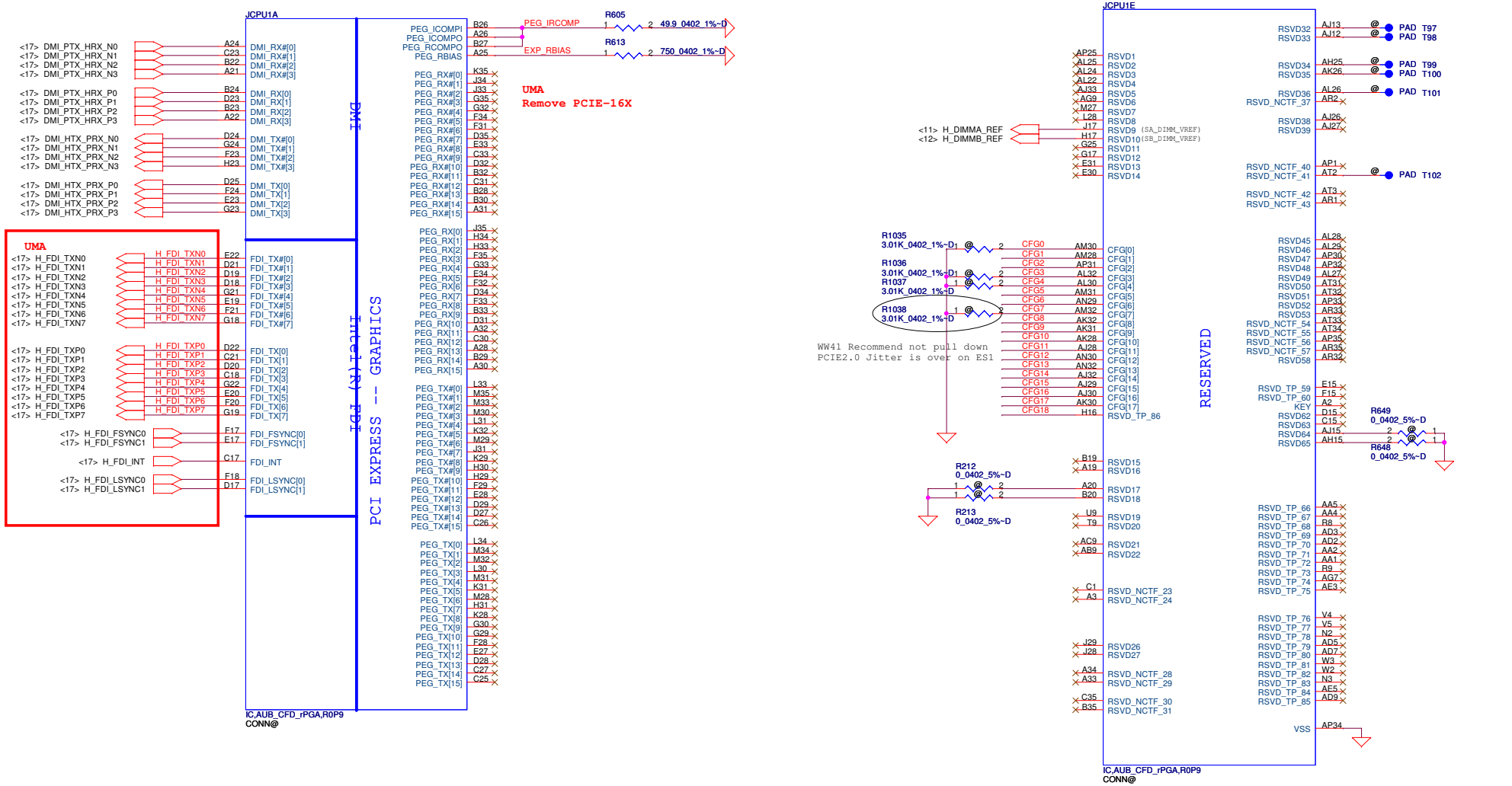

CFG0 – PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG4 – Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

CFG3 – PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

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Title: **PROCESSOR (1/6) DMI,FDI,PEG**

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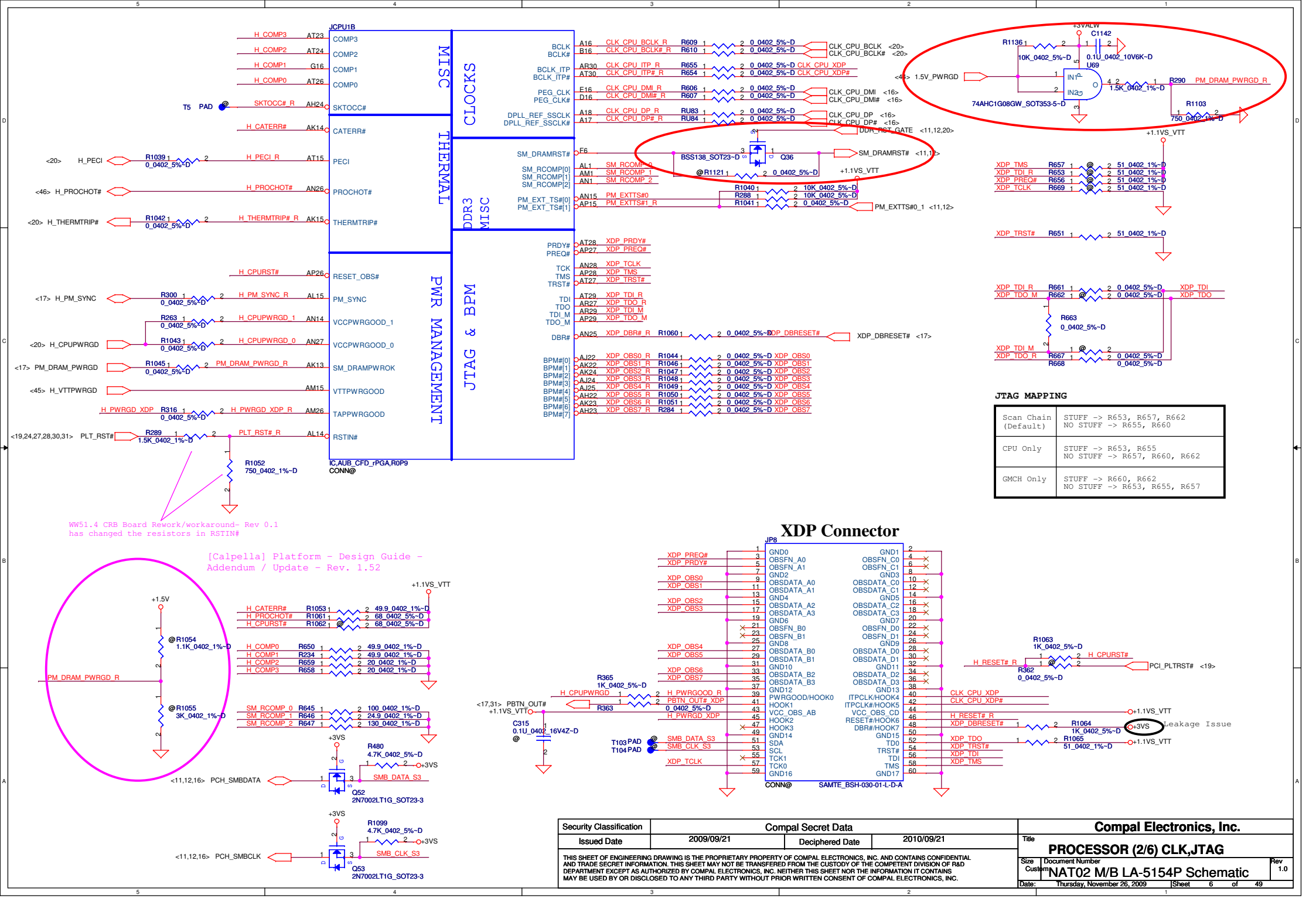

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Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

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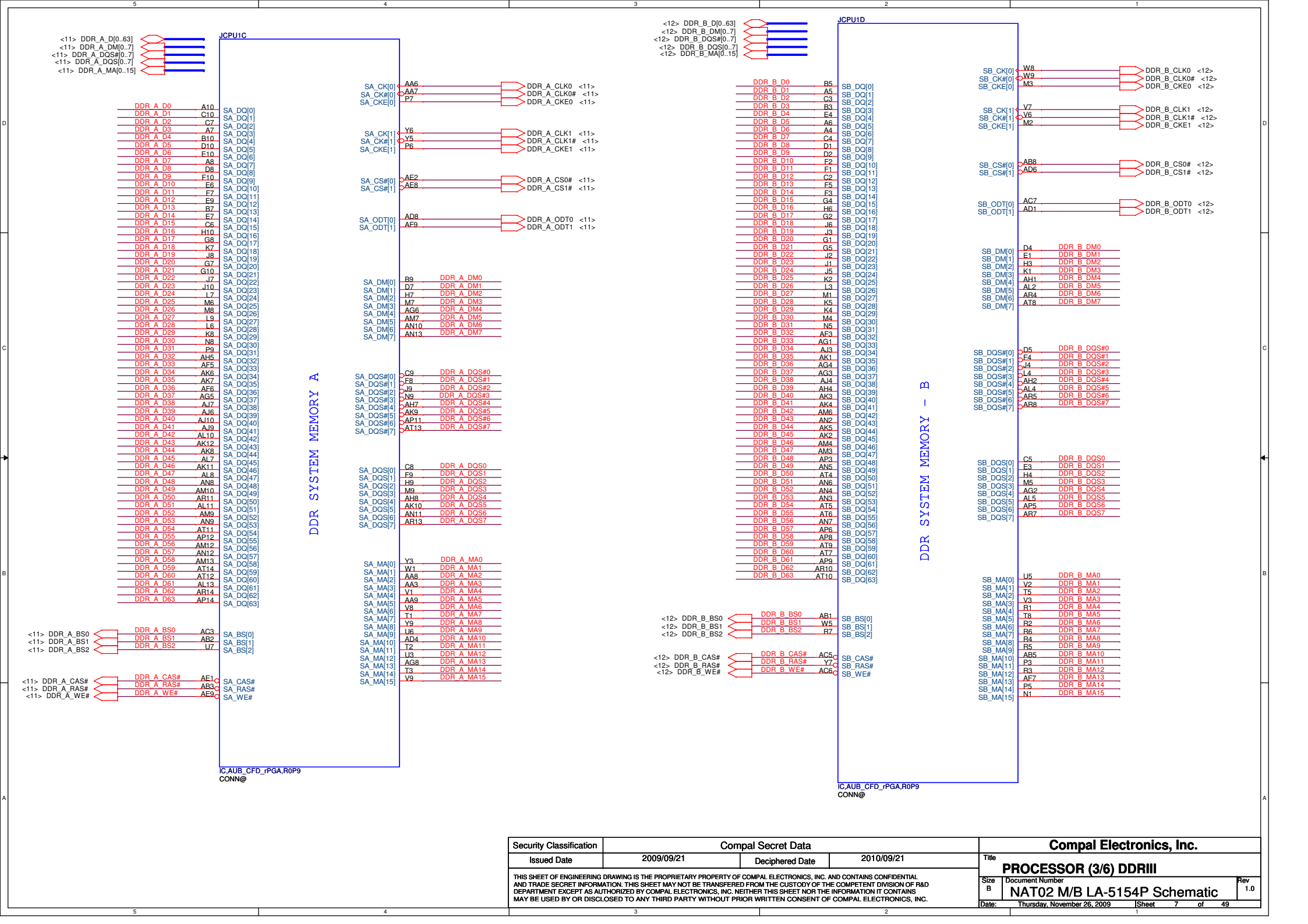

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Title: **PROCESSOR (3/6) DDRIII**

Size	Document Number	Rev
B	NAT02 M/B LA-5154P Schematic	1.0

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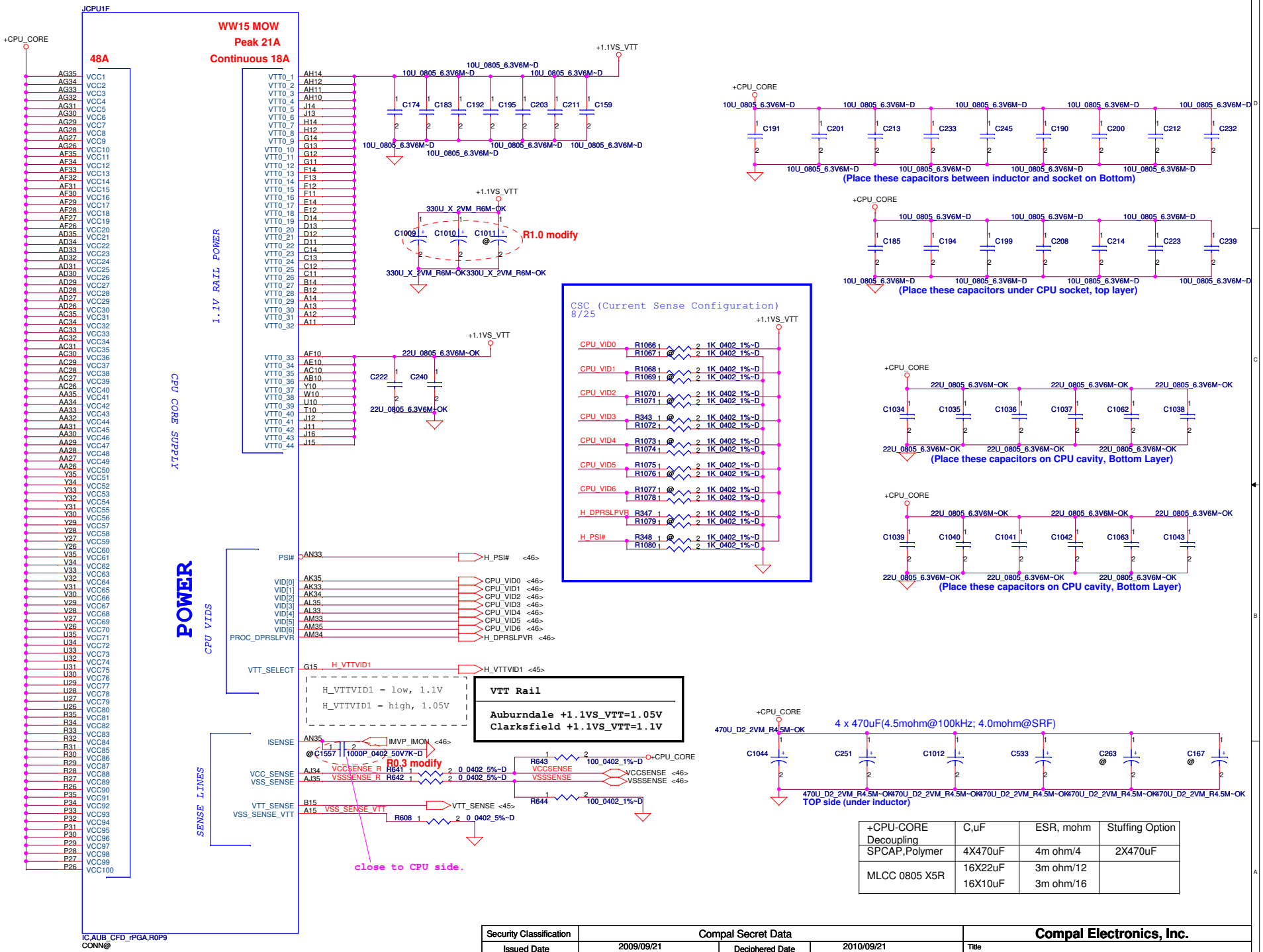

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Title: PROCESSOR (4/6) PWR,Bypass

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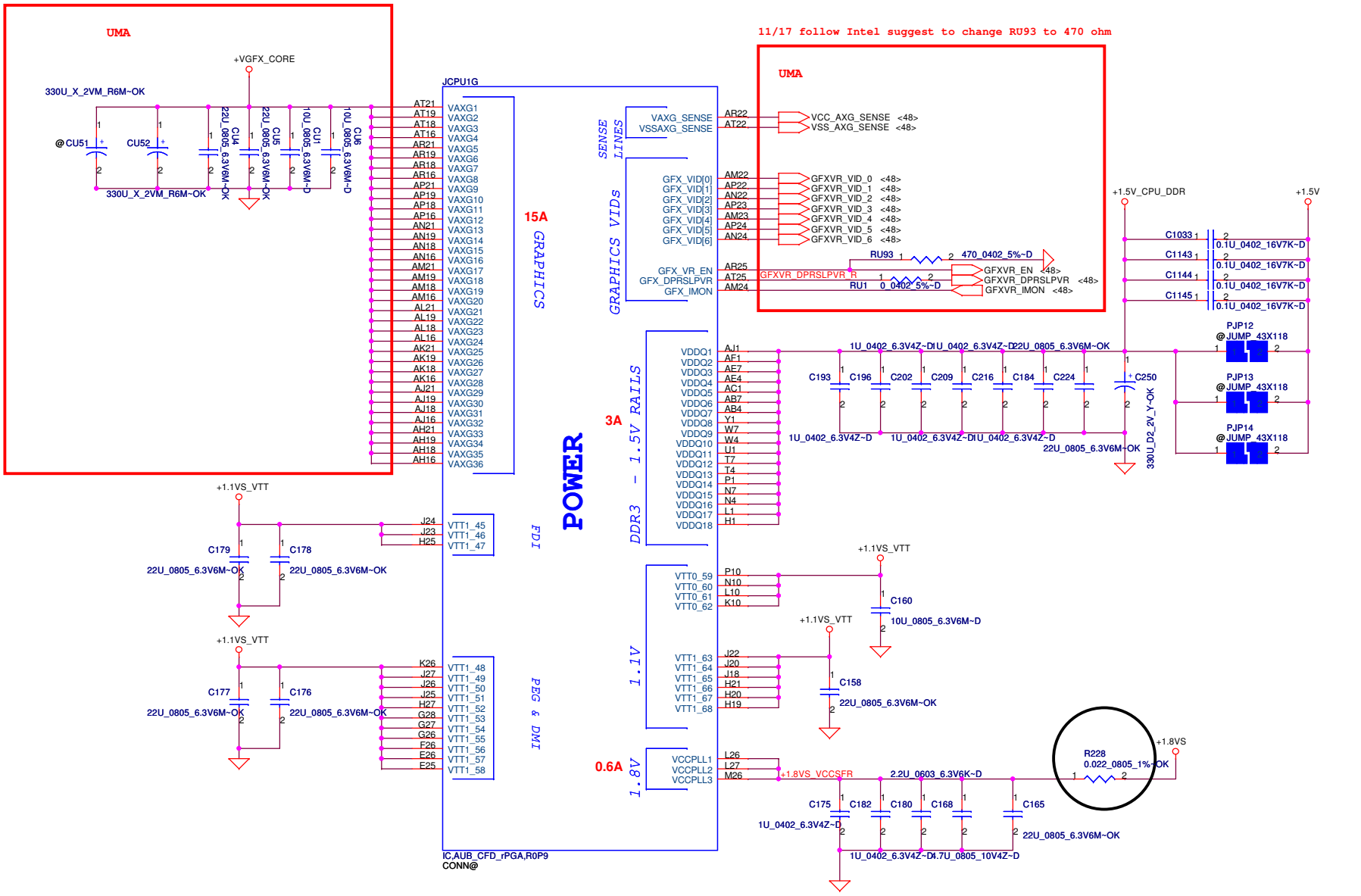

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Title: **PROCESSOR (5/6) PWR**

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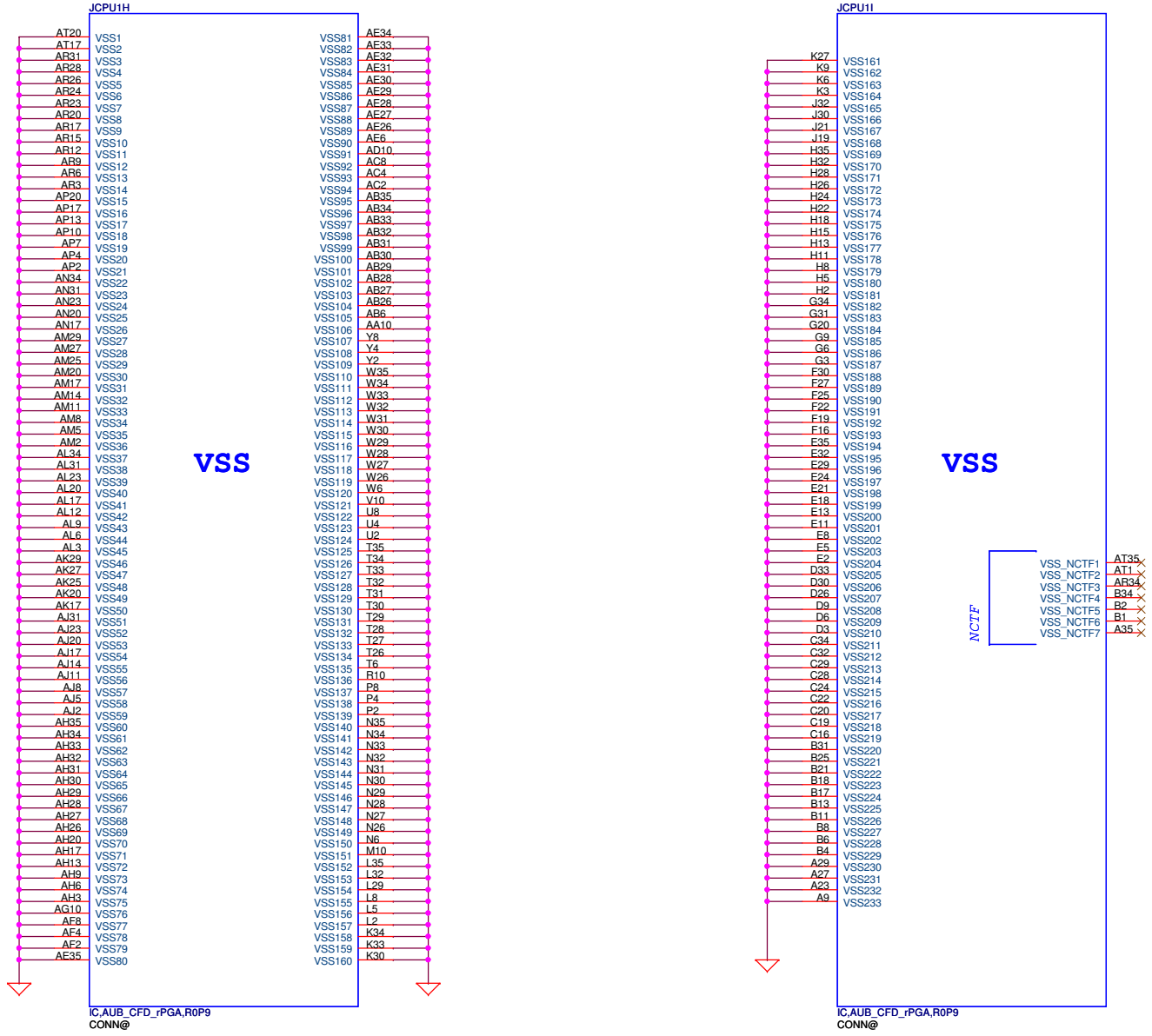

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Title: **PROCESSOR (6/6) VSS**

Size	Document Number	Rev
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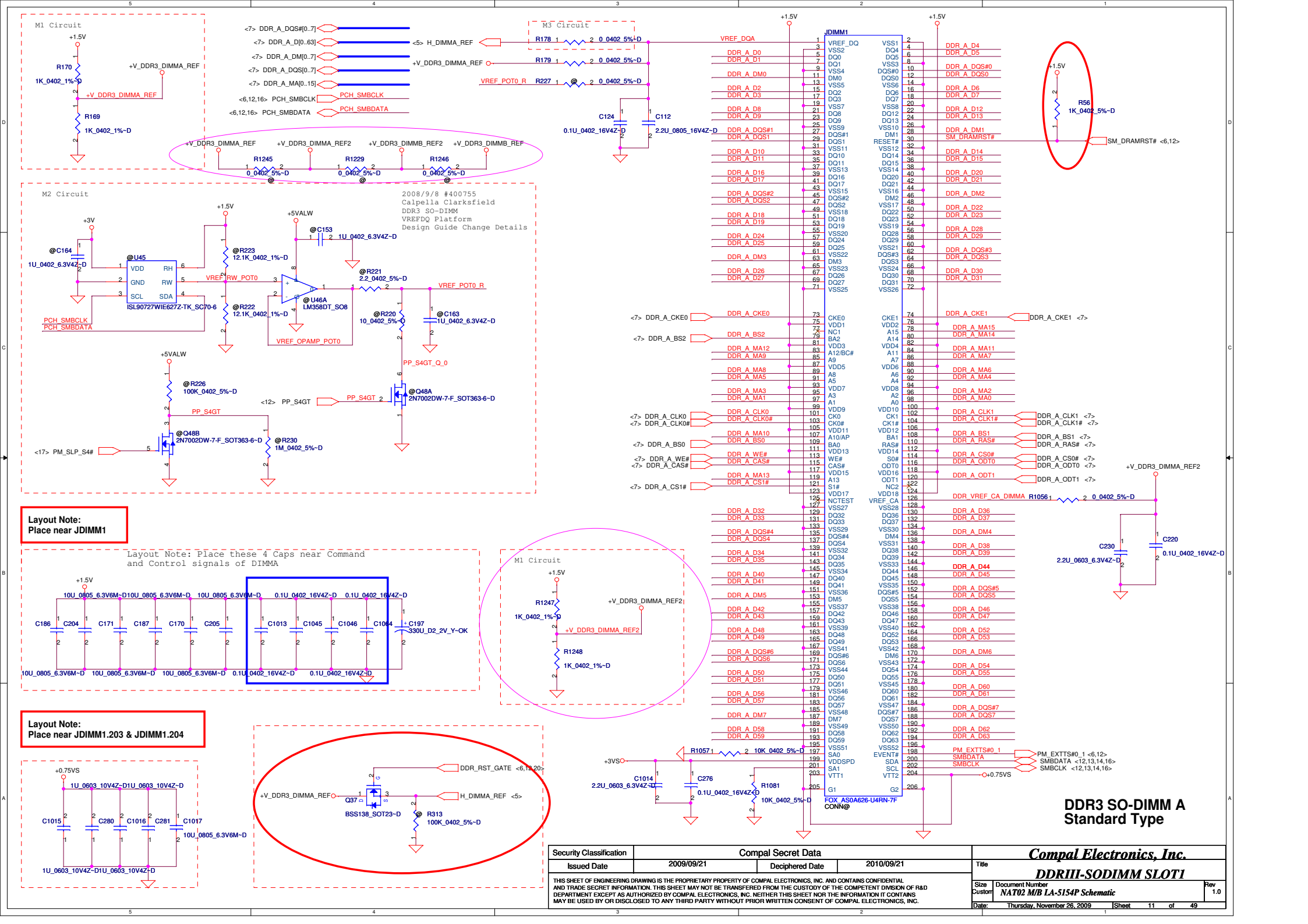
M1 Circuit
+1.5V
R170
1K_0402_1%~D
+V_DDR3_DIMMA_REF
R169
1K_0402_1%~D
<7> DDR_A_DQS#[0..7]
<7> DDR_A_D[0..63]
<7> DDR_A_DM[0..7]
<7> DDR_A_DQS[0..7]
<7> DDR_A_MA[0..15]
<6,12,16> PCH_SMBCLK
<6,12,16> PCH_SMBDATA
PCH_SMBCLK
PCH_SMBDATA
<5> H_DIMMA_REF
+V_DDR3_DIMMA_REF
+V_DDR3_DIMMA_REF2
+V_DDR3_DIMMB_REF2
+V_DDR3_DIMMB_REF
R1245
R1229
R1246
0_0402_5%~D
M3 Circuit
R178
R179
R227
0_0402_5%~D
VREF_POT0_R
C124
0.1U_0402_16V4Z~D
C112
2.2U_0805_16V4Z~D
M2 Circuit
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details
+3V
+1.5V
+5VALW
@C164
1U_0402_6.3V4Z~D
@U45
VDD
GND
SCL
RH
RW
SDA
ISL90727WIE627Z-TK_SC70-6
@R223
12.1K_0402_1%~D
@R222
12.1K_0402_1%~D
VREF_RW_POT0
@C153
1U_0402_6.3V4Z~D
@R221
2.2_0402_5%~D
@U46A
LM358DT_SO8
VREF_OPAMP_POT0
VREF_POT0_R
@R220
10_0402_5%~D
@C163
1U_0402_6.3V4Z~D
PP_S4GT_Q_0
@R226
100K_0402_5%~D
PP_S4GT
@Q48A
2N7002DW-7-F_SOT363-6~D
<12> PP_S4GT
@Q48B
2N7002DW-7-F_SOT363-6~D
@R230
1M_0402_5%~D
<17> PM_SLP_S4#
JDIMM1
VREF_DQ
VREF_CA
DDR_A_D0
DDR_A_D1
DDR_A_DM0
DDR_A_D2
DDR_A_D3
DDR_A_D8
DDR_A_D9
DDR_A_DQS#1
DDR_A_DQS1
DDR_A_D10
DDR_A_D11
DDR_A_D16
DDR_A_D17
DDR_A_DQS#2
DDR_A_DQS2
DDR_A_D18
DDR_A_D19
DDR_A_D24
DDR_A_D25
DDR_A_DM3
DDR_A_D26
DDR_A_D27
DDR_A_CKE0
DDR_A_BS2
DDR_A_MA12
DDR_A_MA9
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_CLK0
DDR_A_CLK0#
DDR_A_MA10
DDR_A_BS0
DDR_A_WE#
DDR_A_CAS#
DDR_A_MA13
DDR_A_CS1#
DDR_A_D32
DDR_A_D33
DDR_A_DQS#4
DDR_A_DQS4
DDR_A_D34
DDR_A_D35
DDR_A_D40
DDR_A_D41
DDR_A_DM5
DDR_A_D42
DDR_A_D43
DDR_A_D48
DDR_A_D49
DDR_A_DQS#6
DDR_A_DQS6
DDR_A_D50
DDR_A_D51
DDR_A_D56
DDR_A_D57
DDR_A_DM7
DDR_A_D58
DDR_A_D59
DDR_A_D4
DDR_A_D5
DDR_A_DQS#0
DDR_A_DQS0
DDR_A_D6
DDR_A_D7
DDR_A_D12
DDR_A_D13
DDR_A_DM1
SM_DRAMRST#
DDR_A_D14
DDR_A_D15
DDR_A_D20
DDR_A_D21
DDR_A_DM2
DDR_A_D22
DDR_A_D23
DDR_A_D28
DDR_A_D29
DDR_A_DQS#3
DDR_A_DQS3
DDR_A_D30
DDR_A_D31
DDR_A_CKE1
DDR_A_MA15
DDR_A_MA14
DDR_A_MA11
DDR_A_MA7
DDR_A_MA6
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
DDR_A_CLK1
DDR_A_CLK1#
DDR_A_BS1
DDR_A_RAS#
DDR_A_CS0#
DDR_A_ODT0
DDR_A_ODT1
DDR_VREF_CA_DIMMA
R1056
0_0402_5%~D
DDR_A_D36
DDR_A_D37
DDR_A_DM4
DDR_A_D38
DDR_A_D39
DDR_A_D44
DDR_A_D45
DDR_A_DQS#5
DDR_A_DQS5
DDR_A_D46
DDR_A_D47
DDR_A_D52
DDR_A_D53
DDR_A_DM6
DDR_A_D54
DDR_A_D55
DDR_A_D60
DDR_A_D61
DDR_A_DQS#7
DDR_A_DQS7
DDR_A_D62
DDR_A_D63
PM_EXTTS#0_1
SMBDATA
SMBCLK
+0.75VS
R1057
10K_0402_5%~D
C1014
2.2U_0603_6.3V4Z~D
C276
0.1U_0402_16V4Z~D
R1081
10K_0402_5%~D
FOX_AS0A626-U4RN-7F
CONN@
R56
1K_0402_5%~D
C230
2.2U_0603_6.3V4Z~D
C220
0.1U_0402_16V4Z~D
Layout Note:
Place near JDIMM1
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA
10U_0805_6.3V6M~D
0.1U_0402_16V4Z~D
C186
C204
C171
C187
C170
C205
C1013
C1045
C1046
C1064
C197
330U_D2_2V_Y~OK
M1 Circuit
R1247
1K_0402_1%~D
R1248
1K_0402_1%~D
Layout Note:
Place near JDIMM1.203 & JDIMM1.204
1U_0603_10V4Z~D
C1015
C280
C1016
C281
C1017
DDR_RST_GATE
Q37
BSS138_SOT23~D
R313
100K_0402_5%~D
DDR3 SO-DIMM A
Standard Type
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DDRIII-SODIMM SLOT1
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NAT02 M/B LA-5154P Schematic
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2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

M1 Circuit

+1.5V
R1230 1K_0402_1%~D
+V_DDR3_DIMMB_REF
R1231 1K_0402_1%~D
DDR_RST_GATE <6,11,20>
Q44 BSS138_SOT23~D
H_DIMMB_REF <5>
R321 100K_0402_5%~D

M2 Circuit

+3V
@C156 1U_0402_6.3V4Z~D
@U8 ISL90728WIE627Z-TK_SC70-6
VDD RH GND RW SCL SDA
PCH_SMBCLK
PCH_SMBDATA
+1.5V
@R196 12.1K_0402_1%~D
VREF_RW_POT1
@R197 12.1K_0402_1%~D
+5VALW
@U46B LM358DT_SO8
VREF_OPAMP_POT1
@R193 2.2_0402_5%~D
@R194 10_0402_5%~D
VREF_POT1_R
@C128 1U_0402_6.3V4Z~D
PP_S4GT_Q_1
<11> PP_S4GT
PP_S4GT
@Q49 2N7002LT1G_SOT23-3

Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C172 10U_0805_6.3V6M~D
C188 10U_0805_6.3V6M~D
C206 10U_0805_6.3V6M~D
C173 10U_0805_6.3V6M~D
C189 10U_0805_6.3V6M~D
C207 10U_0805_6.3V6M~D
C1047 0.1U_0402_16V4Z~D
C1048 0.1U_0402_16V4Z~D
C1049 0.1U_0402_16V4Z~D
C1050 0.1U_0402_16V4Z~D
C198 330U_D2_2V_Y~OK

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

+0.75VS
1U_0603_10V4Z~D
C1018 C282 C283 C1019 C298
10U_0805_6.3V6M~D
1U_0603_10V4Z~D 1U_0603_10V4Z~D

M1 Circuit
+V_DDR3_DIMMB_REF R166 0_0402_5%~D VREF_DQB
M3 Circuit
<5> H_DIMMB_REF R165 0_0402_5%~D
VREF_POT1_R R186 @ 0_0402_5%~D
C110 2.2U_0805_16V4Z~D
C122 0.1U_0402_16V4Z~D

<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DM[0..7]
<7> DDR_B_DQS[0..7]
<7> DDR_B_MA[0..15]
<6,11,16> PCH_SMBCLK
<6,11,16> PCH_SMBDATA

JDIMM2
+1.5V
VREF_DQ VSS1 DQ0 DQ4 DQ1 DQ5 VSS2 DQS#0 DM0 DQS0 VSS4 DQ6 DQ2 DQ7 VSS5 DQ12 DQ3 DQ13 VSS7 VSS8 DQ8 DQ14 DQ9 DQ15 VSS9 DM1 DQS#1 RESET# DQS1 VSS10 VSS11 DQ20 DQ10 DQ21 DQ11 VSS12 VSS13 DQ22 DQ16 DQ23 DQ17 VSS14 VSS15 DQ28 DQS#2 DQ29 DQS2 VSS16 DM2 VSS17 VSS18 DQ30 DQ18 DQ31 DQ19 VSS19 VSS20 DQS#3 DQ24 DQS3 DQ25 VSS21 VSS22 DQ26 DM3 VSS24 VSS23 DQ27 DQ26 VSS25 DQ31 VSS26
+1.5V
DDR_B_D0 DDR_B_D1 DDR_B_DM0 DDR_B_D2 DDR_B_D3 DDR_B_D8 DDR_B_D9 DDR_B_DQS#1 DDR_B_DQS1 DDR_B_D10 DDR_B_D11 DDR_B_D16 DDR_B_D17 DDR_B_DQS#2 DDR_B_DQS2 DDR_B_D18 DDR_B_D19 DDR_B_D24 DDR_B_D25 DDR_B_DM3 DDR_B_D26 DDR_B_D27
DDR_B_D4 DDR_B_D5 DDR_B_DQS#0 DDR_B_DQS0 DDR_B_D6 DDR_B_D7 DDR_B_D12 DDR_B_D13 DDR_B_DM1 SM_DRAMRST# DDR_B_D14 DDR_B_D15 DDR_B_D20 DDR_B_D21 DDR_B_DM2 DDR_B_D22 DDR_B_D23 DDR_B_D28 DDR_B_D29 DDR_B_DQS#3 DDR_B_DQS3 DDR_B_D30 DDR_B_D31
SM_DRAMRST# <6,11>

<7> DDR_B_CKE0 DDR_B_CKE0 CKE0 VDD1 NC1 BA2 VDD3 A12/BC# A9 VDD5 A8 A5 VDD7 A3 A1 VDD9 CK0 CK0# VDD11 A10/AP BA0 VDD13 WE# CAS# VDD15 A13 S1# VDD17 NCTEST
<7> DDR_B_BS2 DDR_B_BS2
DDR_B_MA12 DDR_B_MA9 DDR_B_MA8 DDR_B_MA5 DDR_B_MA3 DDR_B_MA1
<7> DDR_B_CLK0 <7> DDR_B_CLK0# DDR_B_CLK0 DDR_B_CLK0#
DDR_B_MA10 DDR_B_BS0
<7> DDR_B_BS0
<7> DDR_B_WE# <7> DDR_B_CAS# DDR_B_WE# DDR_B_CAS#
DDR_B_MA13 DDR_B_CS1#
<7> DDR_B_CS1#
CKE1 VDD2 A15 A14 VDD4 A11 A7 VDD6 A6 A4 VDD8 A2 A0 VDD10 CK1 CK1# VDD12 BA1 RAS# VDD14 S0# ODT0 VDD16 ODT1 NC2 VDD18 VREF_CA VSS28 DQ36 DQ37 VSS30 DM4 VSS31 DQ38 DQ39 VSS33 DQ44 DQ45 VSS35 DQS#5 DQS5 VSS38 DQ46 DQ47 VSS40 DQ52 DQ53 VSS42 DM6 VSS43 DQ54 DQ55 VSS45 DQ60 DQ61 VSS47 DQS#7 DQS7 VSS50 DQ62 DQ63 VSS52 EVENT# SDA SCL VTT2
DDR_B_CKE1 <7>
DDR_B_MA15 DDR_B_MA14 DDR_B_MA11 DDR_B_MA7 DDR_B_MA6 DDR_B_MA4 DDR_B_MA2 DDR_B_MA0 DDR_B_CLK1 DDR_B_CLK1# DDR_B_BS1 DDR_B_RAS# DDR_B_CS0# DDR_B_ODT0 DDR_B_ODT1
DDR_B_CLK1 <7>
DDR_B_CLK1# <7>
DDR_B_BS1 <7>
DDR_B_RAS# <7>
DDR_B_CS0# <7>
DDR_B_ODT0 <7>
DDR_B_ODT1 <7>
+V_DDR3_DIMMB_REF2
DDR_VREF_CA_DIMMB R1058 0_0402_5%~D
DDR_B_D32 DDR_B_D33 DDR_B_DQS#4 DDR_B_DQS4 DDR_B_D34 DDR_B_D35 DDR_B_D40 DDR_B_D41 DDR_B_DM5 DDR_B_D42 DDR_B_D43 DDR_B_D48 DDR_B_D49 DDR_B_DQS#6 DDR_B_DQS6 DDR_B_D50 DDR_B_D51 DDR_B_D56 DDR_B_D57 DDR_B_DM7 DDR_B_D58 DDR_B_D59
DDR_B_D36 DDR_B_D37 DDR_B_DM4 DDR_B_D38 DDR_B_D39 DDR_B_D44 DDR_B_D45 DDR_B_DQS#5 DDR_B_DQS5 DDR_B_D46 DDR_B_D47 DDR_B_D52 DDR_B_D53 DDR_B_DM6 DDR_B_D54 DDR_B_D55 DDR_B_D60 DDR_B_D61 DDR_B_DQS#7 DDR_B_DQS7 DDR_B_D62 DDR_B_D63
C231 2.2U_0603_6.3V4Z~D
C221 0.1U_0402_16V4Z~D
M1 Circuit
+1.5V
R1249 1K_0402_1%~D
+V_DDR3_DIMMB_REF2
R1250 1K_0402_1%~D
+3VS
R1059 10K_0402_5%~D
R1082 10K_0402_5%~D
C1020 2.2U_0603_6.3V4Z~D
C277 0.1U_0402_16V4Z~D
SDA SCL VDDSPD SA1 VTT1 SA0 G1 G2
PM_EXTTS#0_1 PM_EXTTS#0_1 <6,11>
SMBDATA SMBDATA <11,13,14,16>
SMBCLK SMBCLK <11,13,14,16>
+0.75VS
FOX_AS0A626-U8RN-7F
CONN@

DDR3 SO-DIMM B
Standard Type

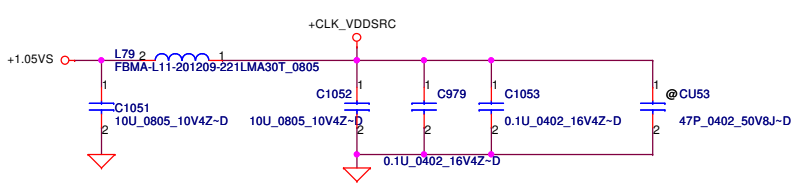
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

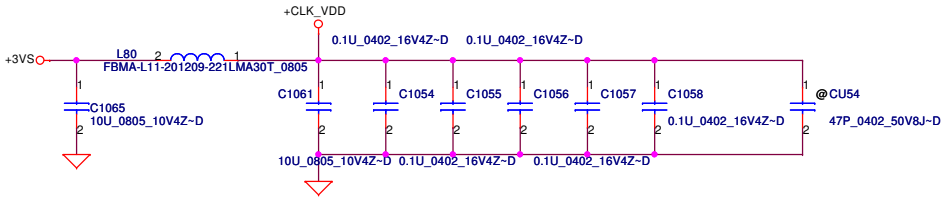
Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

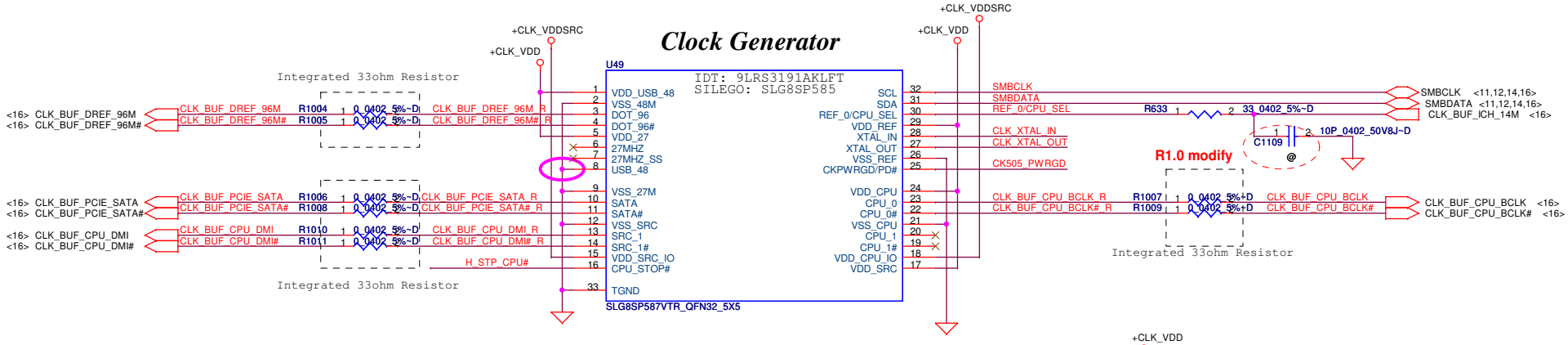
Size | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

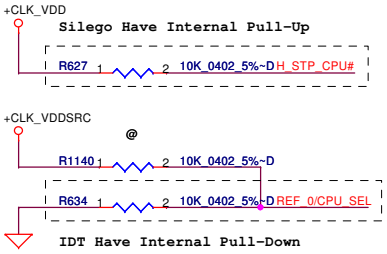
Date: Thursday, November 26, 2009 | Sheet 12 of 49



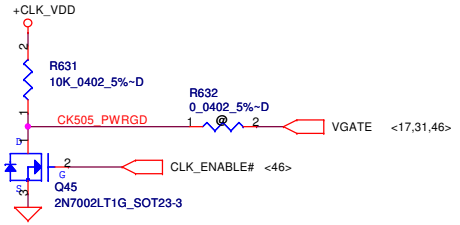


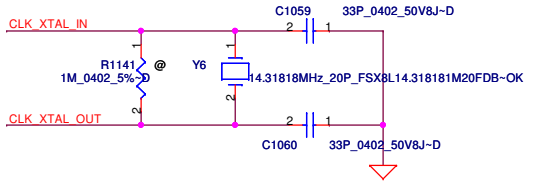
Clock Generator





PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz





Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

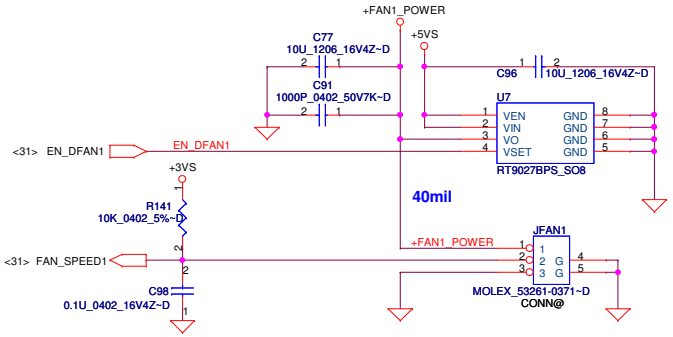
Compal Electronics, Inc.

Title: **Clock Generator (CK505)**

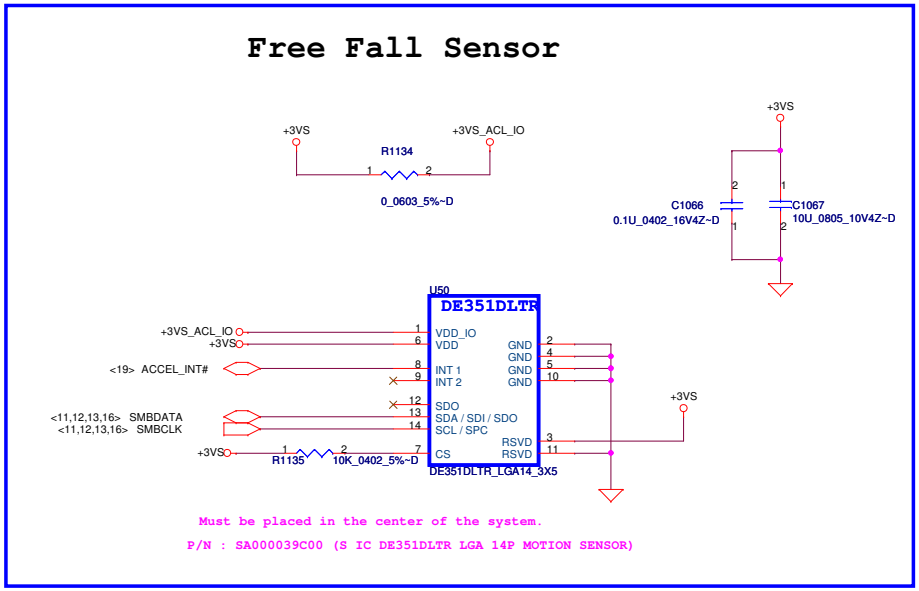
Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

Date: Thursday, November 26, 2009 Sheet 13 of 49

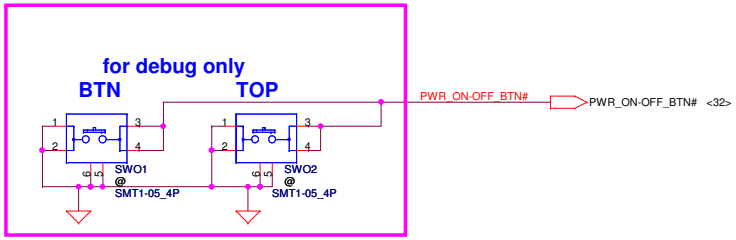
FAN Control circuit



Free Fall Sensor



Power Button



Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **FAN & Screw Hole**

Size	Document Number	Rev
B	NAT02 M/B LA-5154P Schematic	1.0

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+RTCVCC
R46 20K_0402_1%~D
PCH_RTCRST#
RC Delay 18~25mS
close to RAM door
CMOS1
C15 1U_0603_10V6K~D
+RTCVCC
R36 20K_0402_1%~D
PCH_SRTCRST#
RC Delay 18~25mS
close to RAM door
ME1
C13 1U_0603_10V6K~D
C398 18P_0402_50V8J~D
X2
NC OSC
NC OSC
32.768KHZ_12.5PF_Q13MC14610002
C402 18P_0402_50V8J~D
PCH_RTCX1
R1100 10M_0402_5%~D
PCH_RTCX2
U47A
REV1.0
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
LDRQ1# / GPIO23
SERIRQ
LPC_AD0 <27,31>
LPC_AD1 <27,31>
LPC_AD2 <27,31>
LPC_AD3 <27,31>
LPC_FRAME# <27,31>
SERIRQ <31>
+RTCVCC
R64 1M_0402_5%~D SM_INTRUDER#
R51 330K_0402_5%~D PCH_INTVRMEN
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
HDA for AUDIO
<25> HDA_BITCLK_AUDIO R1083 33_0402_5%~D HDA_BITCLK_PCH
<25> HDA_SYNC_AUDIO R1084 33_0402_5%~D HDA_SYNC_PCH
<25> HDA_RST_AUDIO# R1085 33_0402_5%~D HDA_RST_PCH#
<25> HDA_SDOUT_AUDIO R1086 33_0402_5%~D HDA_SDOUT_PCH
HDA_BITCLK_PCH
HDA_SYNC_PCH
<25> PCH_SPKR
PCH_SPKR
HDA_RST_PCH#
<25> HDA_SDIN0
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
IHDA
HDA_BITCLK_AUDIO C1110 10P_0402_50V8J~D
<31,32> TOUCHKEY_TINT
R1024 0_0402_5%~D
R1232 1K_0402_5%~D
GPIO033 pull down only for ME disable
HDA_SDOUT_PCH
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13
SATA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_ITX_DRX_N0 0.01U_0402_16V7K~D C961
SATA_ITX_DRX_P0 0.01U_0402_16V7K~D C962
SATA_IRX_DTX_N0 <29>
SATA_IRX_DTX_P0 <29>
SATA_ITX_C_DRX_N0 <29>
SATA_ITX_C_DRX_P0 <29>
SATA for HDD1
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA_ITX_DRX_N1 C963 0.01U_0402_16V7K~D
SATA_ITX_DRX_P1 C964 0.01U_0402_16V7K~D
SATA_IRX_DTX_N1 <29>
SATA_IRX_DTX_P1 <29>
SATA_ITX_C_DRX_N1 <29>
SATA_ITX_C_DRX_P1 <29>
SATA for HDD2
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
From PCH EDS 5.16, SATA port2 & 3 are not available in all sku.
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA_ITX_DRX_N4 0.01U_0402_16V7K~D C965
SATA_ITX_DRX_P4 0.01U_0402_16V7K~D C966
SATA_IRX_DTX_N4 <29>
SATA_IRX_DTX_P4 <29>
SATA_ITX_C_DRX_N4 <29>
SATA_ITX_C_DRX_P4 <29>
SATA for ODD
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_ITX_DRX_N5 0.01U_0402_16V7K~D C967
SATA_ITX_DRX_P5 0.01U_0402_16V7K~D C968
SATA_IRX_DTX_N5 <30>
SATA_IRX_DTX_P5 <30>
SATA_ITX_C_DRX_N5 <30>
SATA_ITX_C_DRX_P5 <30>
SATA for eSATA
+1.05VS
SATAICOMPO
SATAICOMPI
SATA_COMP R139 37.4_0402_1%~OK
JTAG
PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#
SPI
PCH_SPI_CLK_1 R584 0_0402_5%~D PCH_SPI_CLK
PCH_SPI_CLK_2 RU86 0_0402_5%~D
PCH_SPI_CS0# R571 15_0402_5%~D PCH_SPI_CS0#_R
PCH_SPI_CS1# RU87 15_0402_5%~D PCH_SPI_CS1#_R
PCH_SPI_MOSI_1 R575 15_0402_5%~D PCH_SPI_MOSI
PCH_SPI_MOSI_2 RU88 15_0402_5%~D
PCH_SPI_MISO_1 R565 33_0402_5%~D PCH_SPI_MISO
PCH_SPI_MISO_2 RU89 33_0402_5%~D
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
IBEXPEAK-M_FCBGA1071~D
SATALED#
SATA0GP / GPIO21
SATA1GP / GPIO19
PCH_SATALED# R129 10K_0402_5%~D
+3VS
R1120 1K_0402_5%~D
PCH_SPKR
SERIRQ
R115 10K_0402_5%~D
R77 10K_0402_5%~D
R116 10K_0402_5%~D
PAD T110
PAD T111
R111 10K_0402_5%~D
R82 10K_0402_5%~D
+3V
+1.05VS
R1130 51_0402_1%~D
R1101 200_0402_5%~D
R1102 100_0402_1%~D
R1131 51_0402_1%~D
R1104 200_0402_5%~D
R1105 100_0402_1%~D
R1132 51_0402_1%~D
R1106 200_0402_5%~D
R1107 100_0402_1%~D
R1133 51_0402_1%~D
R1108 20K_0402_1%~D
R1109 10K_0402_5%~D
2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R1104, R1105 on ES2 Sample
MP mount R1130, R1131, R1132, R1133 and remove others
U68
RU91 3.3K_0402_5%~D
PCH_SPI_CS1#
PCH_SPI_MISO_2
SPI_WP2#
CS#
SO
WP#
GND
VCC
HOLD#
SCLK
SI
SPI_HOLD2# 3.3K_0402_5%~D RU90
PCH_SPI_CLK_2
PCH_SPI_MOSI_2
@MX25L1605AM2C-12G_SO8
U29
R1110 3.3K_0402_5%~D
PCH_SPI_CS0#
PCH_SPI_MISO_1
SPI_WP1#
/CS
DO
/WP
GND
VCC
/HOLD
CLK
DIO
SPI_HOLD1# 3.3K_0402_5%~D R1122
PCH_SPI_CLK_1
PCH_SPI_MOSI_1
MX25L3205DM2I-12G_SO8~D
SPI Flash (32Mbit/4Mbyte)
Change to SA000021A0L
PCH_SPI_MOSI R173 1K_0402_5%~D
enable iTPM: SPI_MOSI High
PCH_JTAG_TCK R1111 4.7K_0402_5%~D
CRB 1.0 Change to 4.7K

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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U47B

REV1.0

IBEXPEAK-M_FCBGA1071~D

1. Connect Directly XDCP of DDR3
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2, FFS
3. Level Shift2, Pull-Up to +3VS CPU & PCH XDP

Remove

Buffer Mode check is need or not

R0.3 Modify

XTAL25_IN should be pulled to GND using a 0Ω resistor. (Calpella_Schematic_Checklist_Rev1.6)

Note: ADD 25MHz crystal for Display Clock Integration

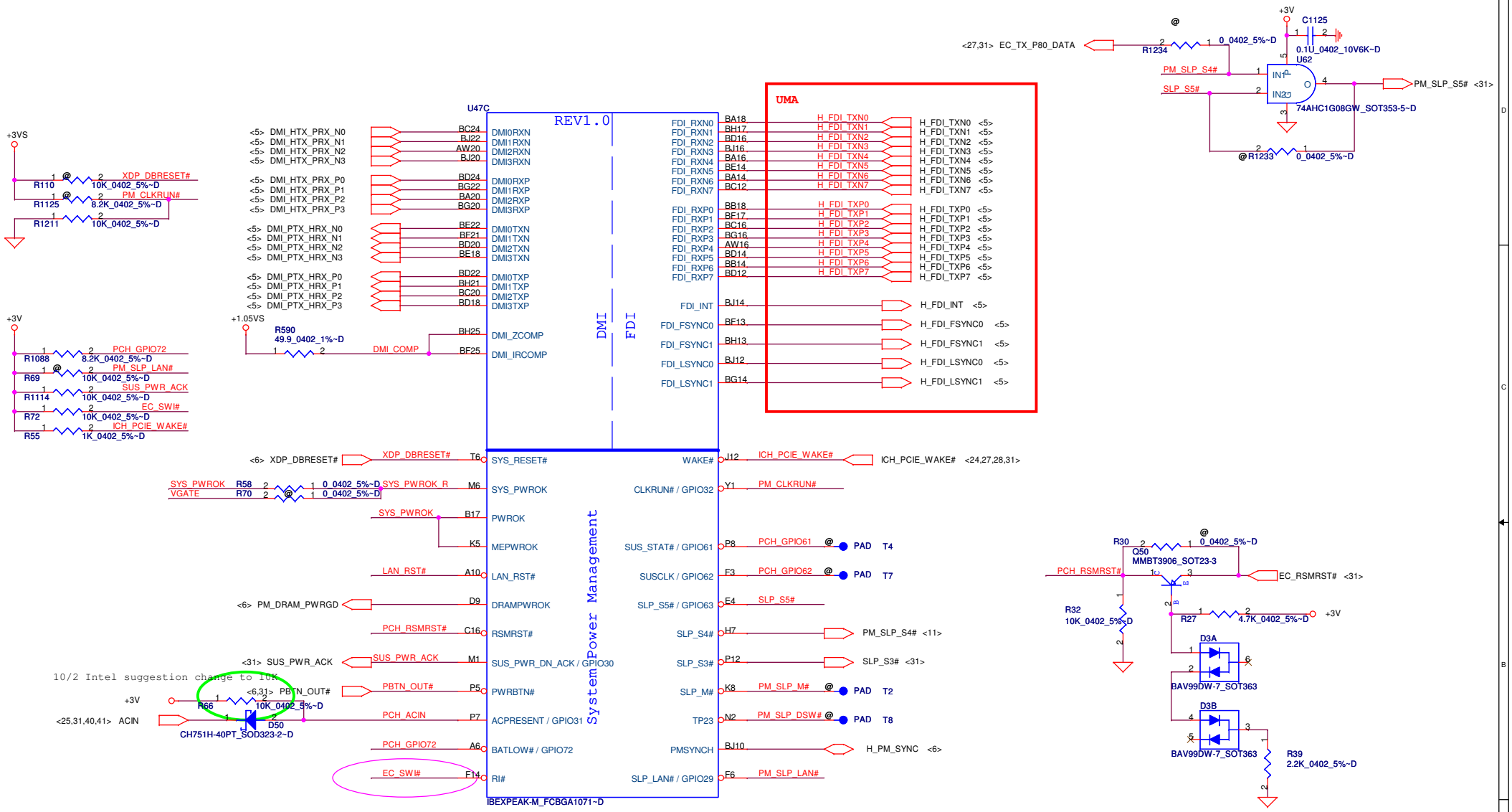
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

Date: Thursday, November 26, 2009 | Sheet 16 of 49



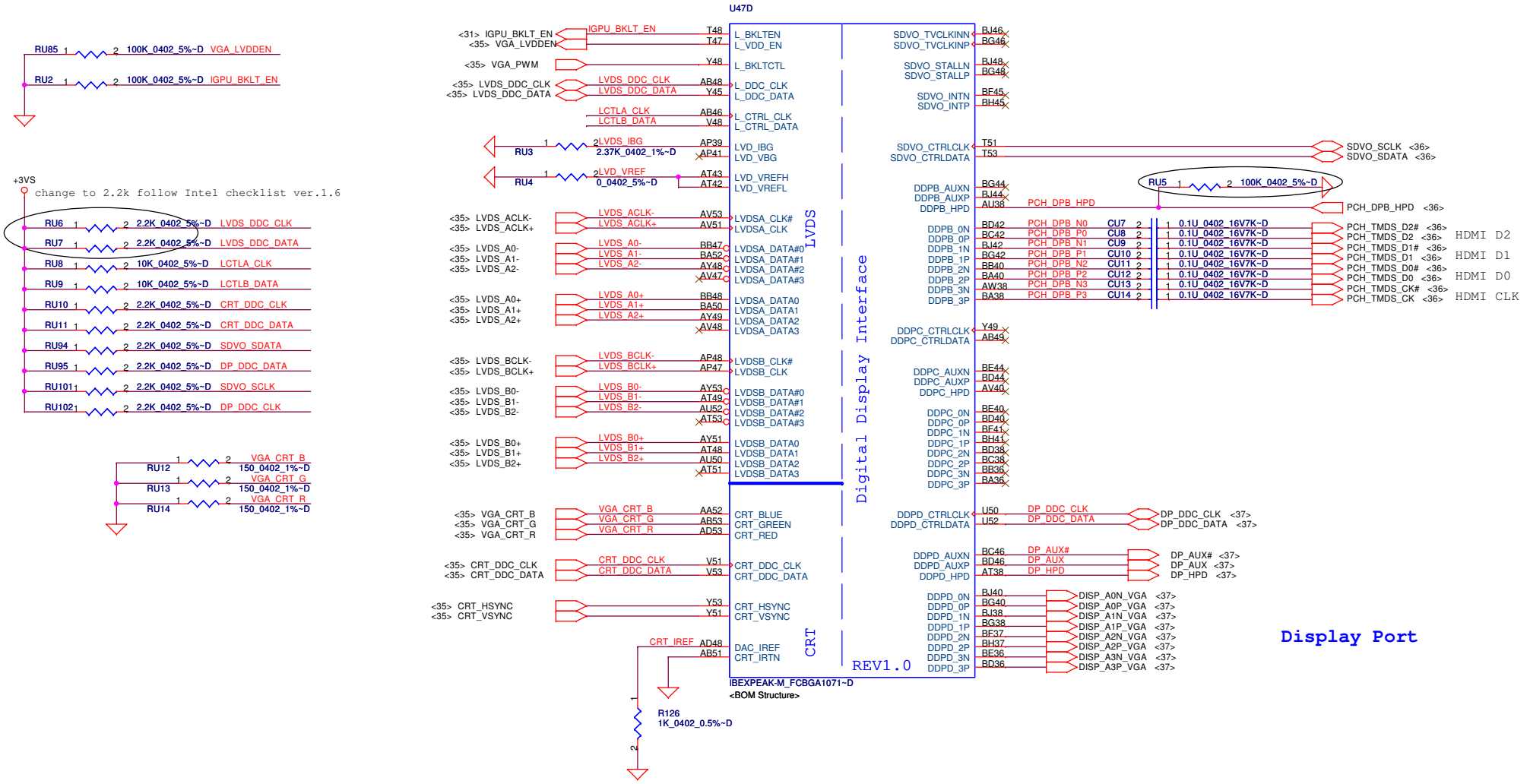
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **PCH (3/9) DMI, FDI, PM**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

Date: Thursday, November 26, 2009 Sheet 17 of 49



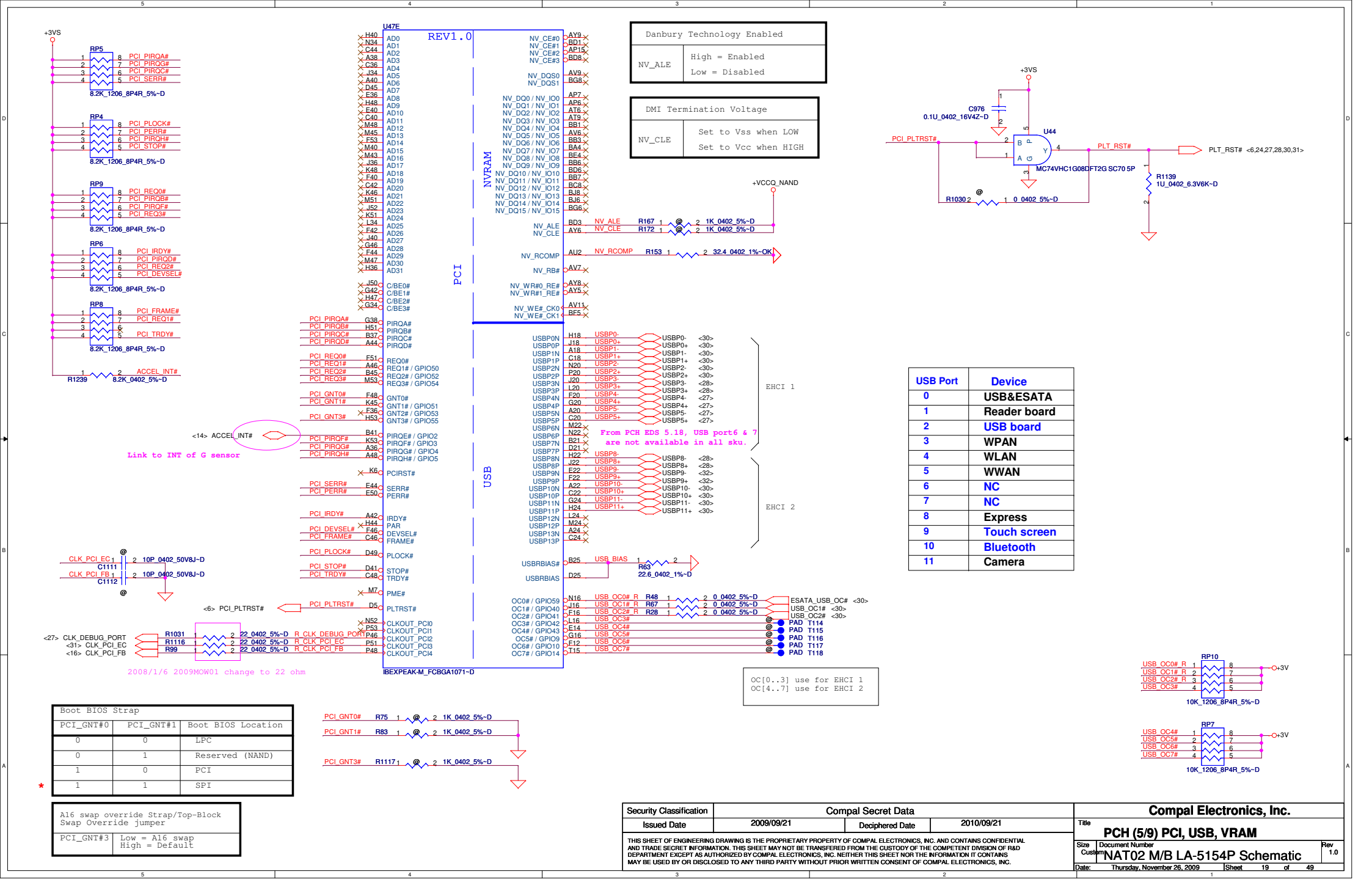
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **PCH (4/9) LVDS, CRT, DPI**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

Date: Thursday, November 26, 2009 Sheet 18 of 49



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

USB Port	Device
0	USB&ESATA
1	Reader board
2	USB board
3	WPAN
4	WLAN
5	WWAN
6	NC
7	NC
8	Express
9	Touch screen
10	Bluetooth
11	Camera

Boot BIOS Strap

PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap High = Default

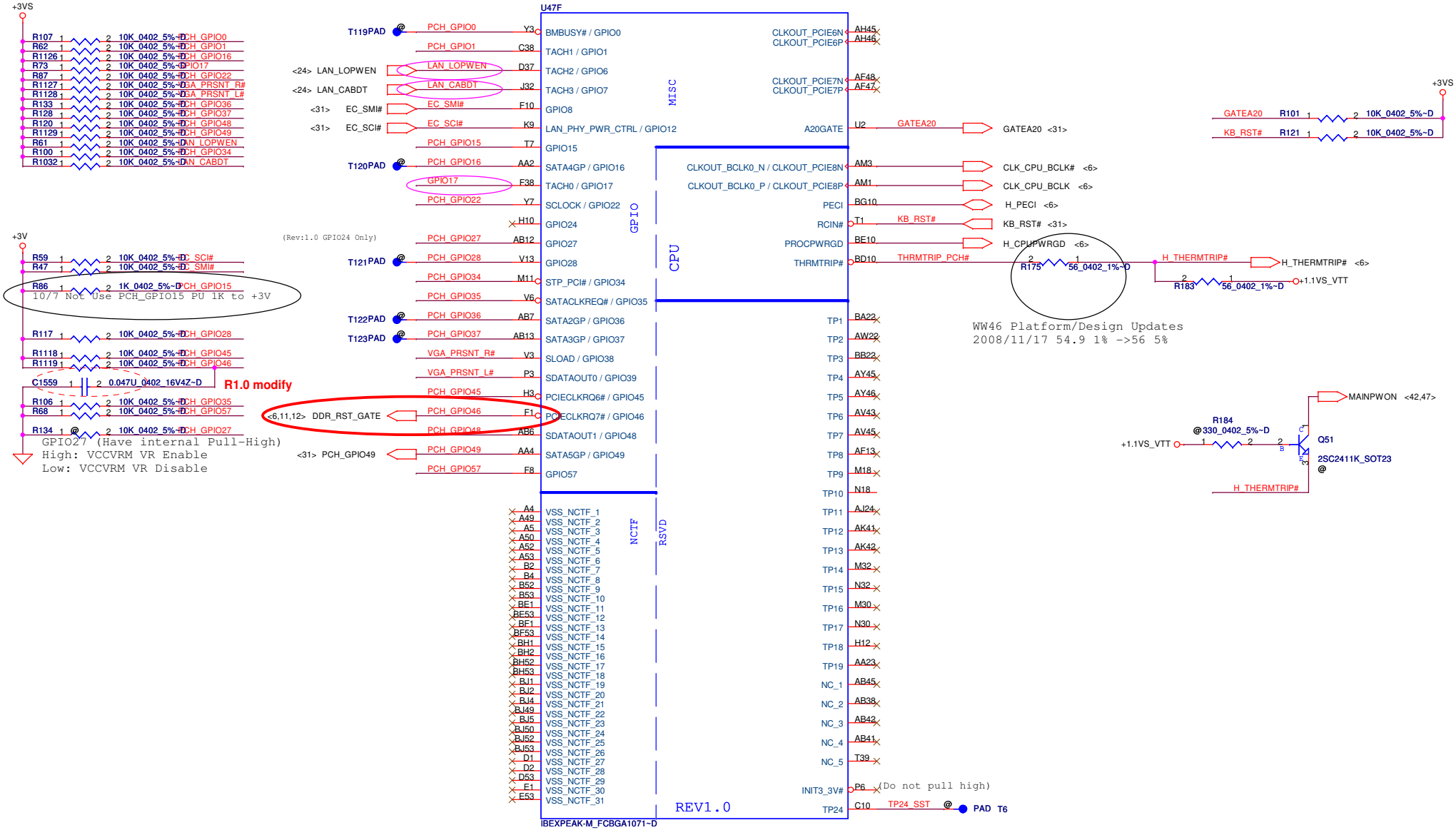
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **PCH (5/9) PCI, USB, VRAM**

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

Date: Thursday, November 26, 2009 | Sheet 19 of 49



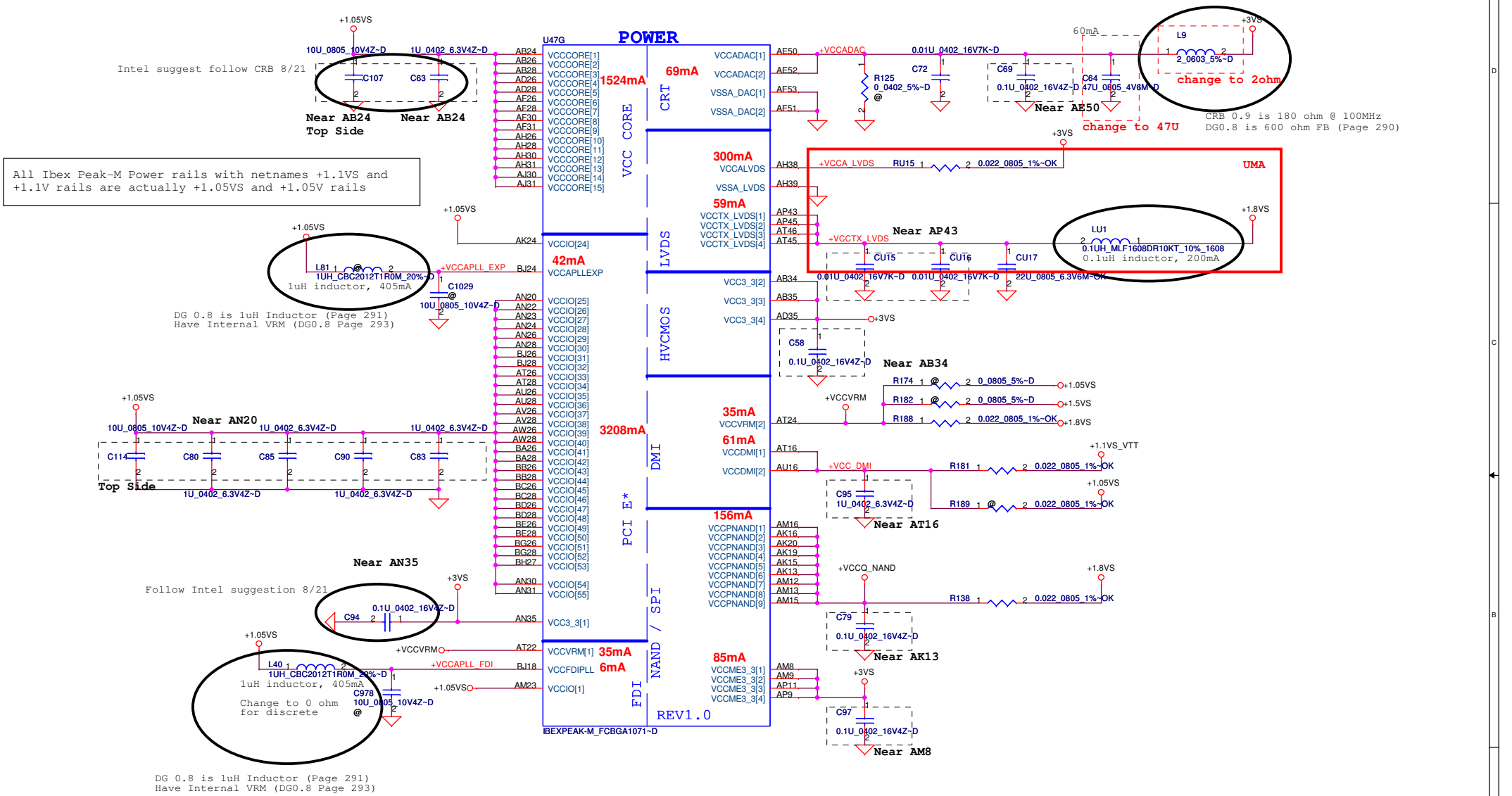
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **PCH (6/9) GPIO, CPU, MISC**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

Date: Thursday, November 26, 2009 Sheet 20 of 49



Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **PCH (7/9) PWR**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

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POWER

REV1.0

DG 0.8 is 10uH Inductor (Page 290)
Have Internal VRM (DG0.8 Page 293)

All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

Follow Intel design

Follow Intel suggestion

Follow Intel Suggestion 8/21

Change to 1U for power sequence issue on ICH9

DG 0.8 is 10uH Inductor (Page 291)
Have Internal VRM (DG0.8 Page 293)

IBEXPEAK-M_FCBGA1071~D

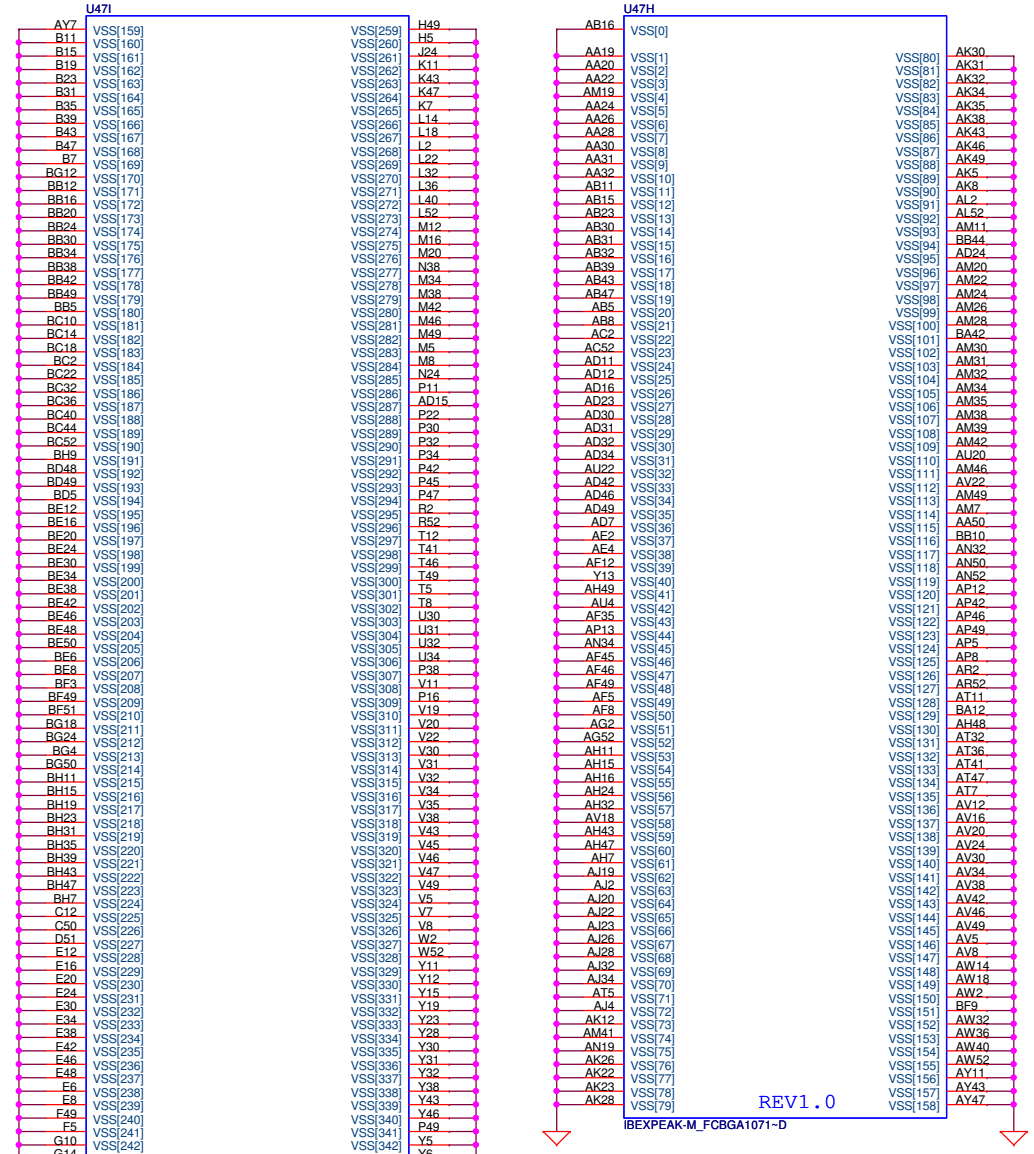
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **PCH (8/9) PWR**

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

Date: Thursday, November 26, 2009 | Sheet 22 of 49

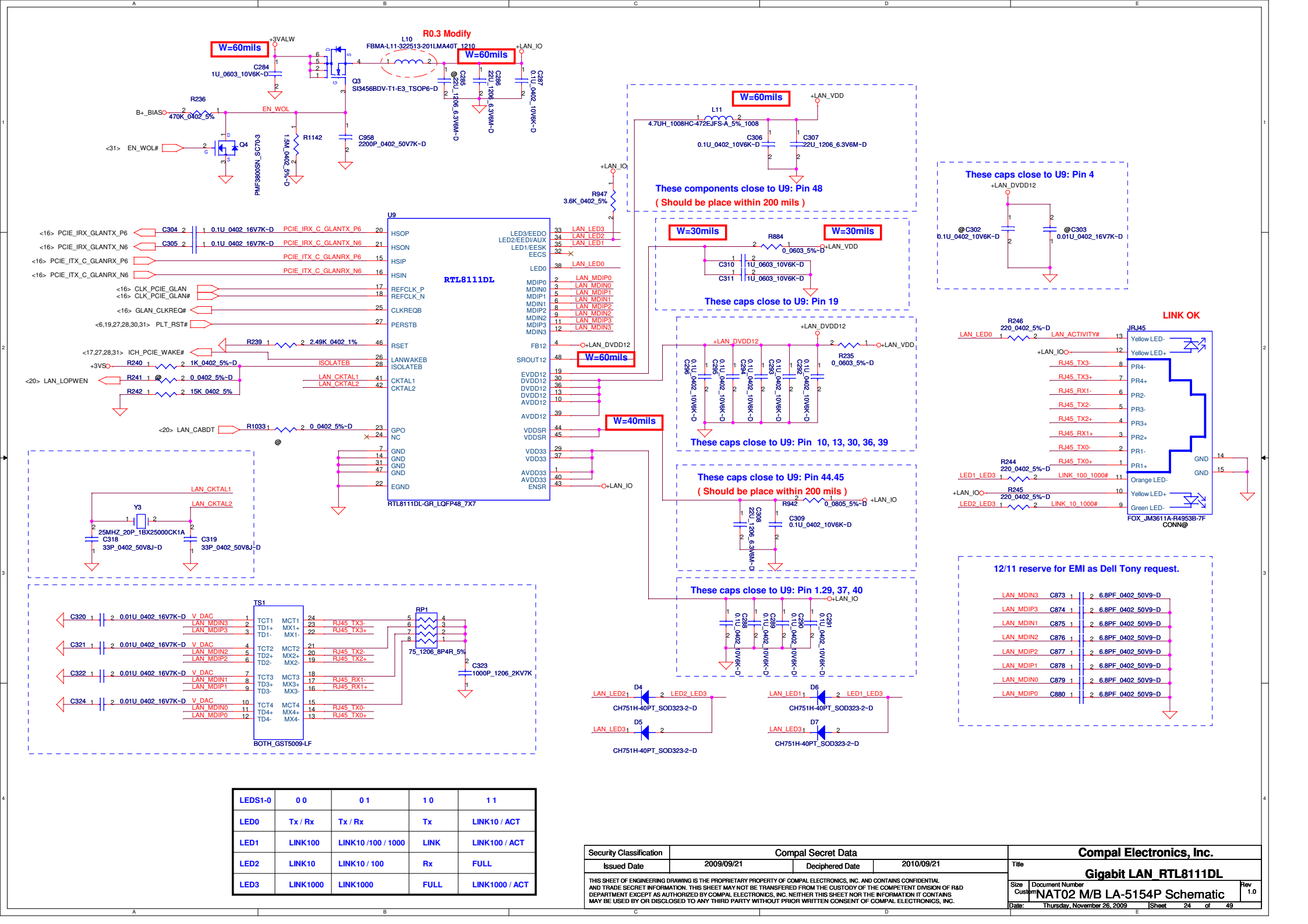


Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

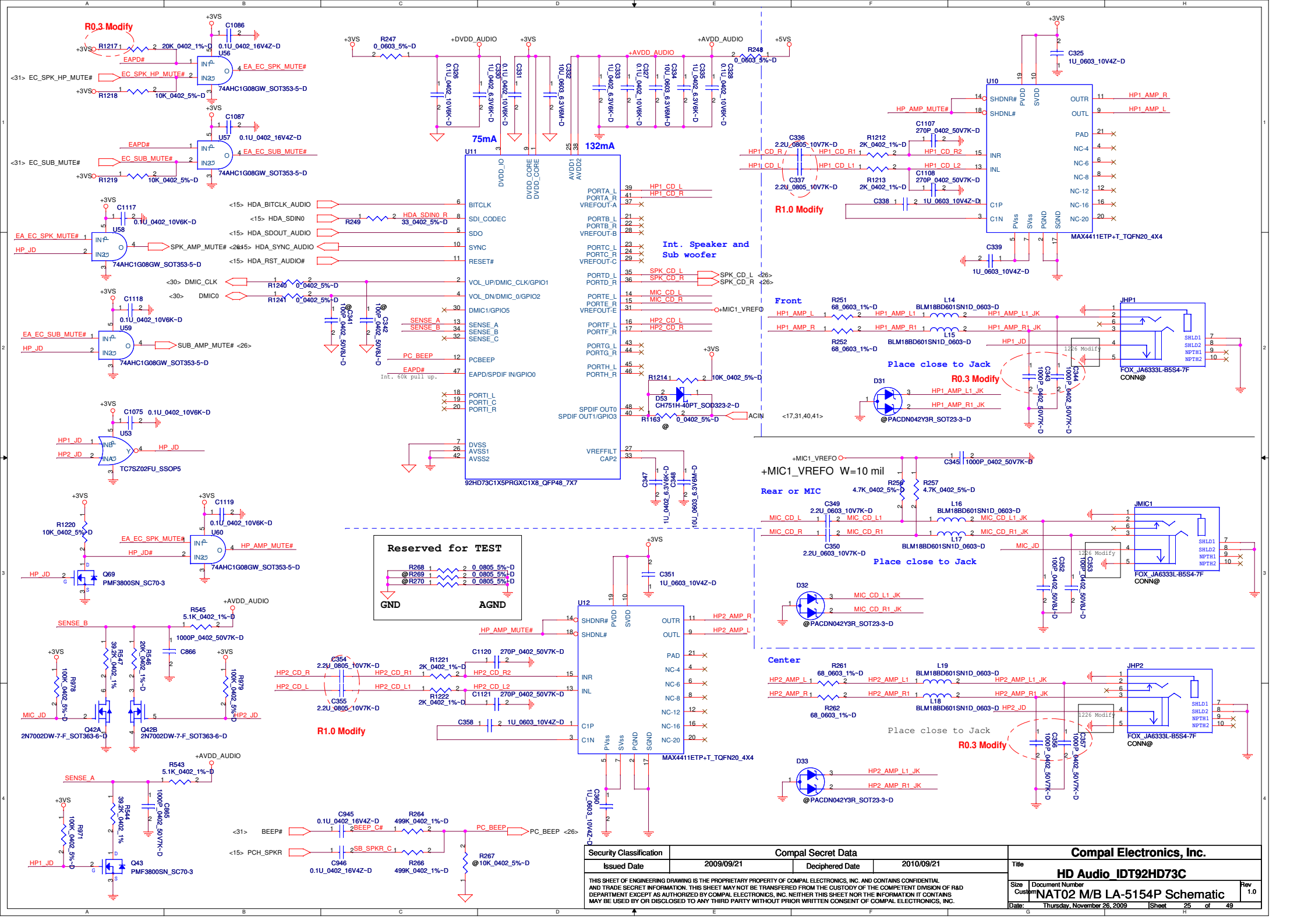
Date: Thursday, November 26, 2009 | Sheet 23 of 49



LEDS1-0	0 0	0 1	1 0	1 1
LED0	Tx / Rx	Tx / Rx	Tx	LINK10 / ACT
LED1	LINK100	LINK10 /100 / 1000	LINK	LINK100 / ACT
LED2	LINK10	LINK10 / 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 / ACT

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.	
Title	Gigabit LAN_RTL8111DL
Size: Custom	Document Number: NAT02 M/B LA-5154P Schematic
Rev	1.0
Date: Thursday, November 26, 2009	Sheet 24 of 49



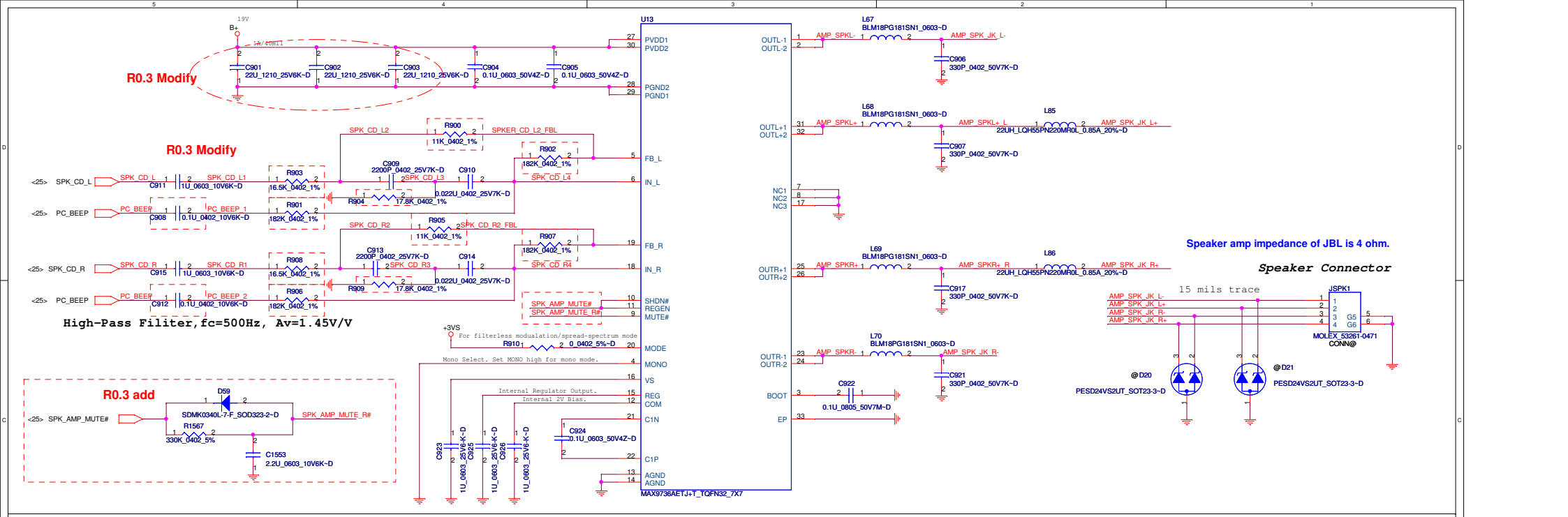
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

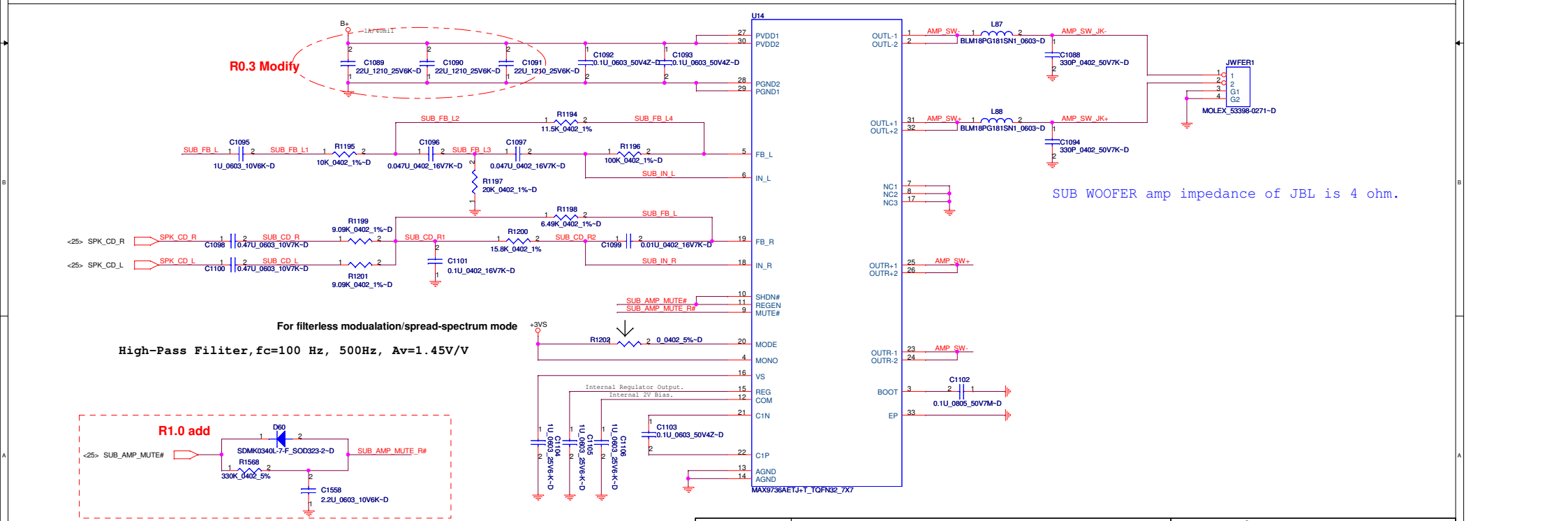
Compal Electronics, Inc.

Title: **HD Audio_IDT92HD73C**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

Date: Thursday, November 26, 2009 | Sheet 25 of 49





Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **Sub woofer / Speaker AMP**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

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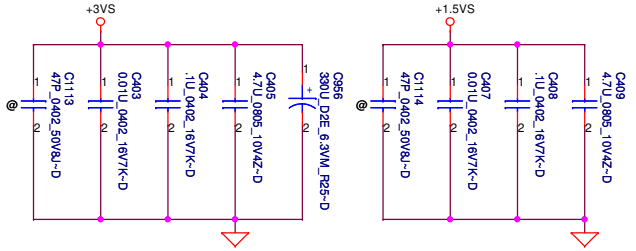
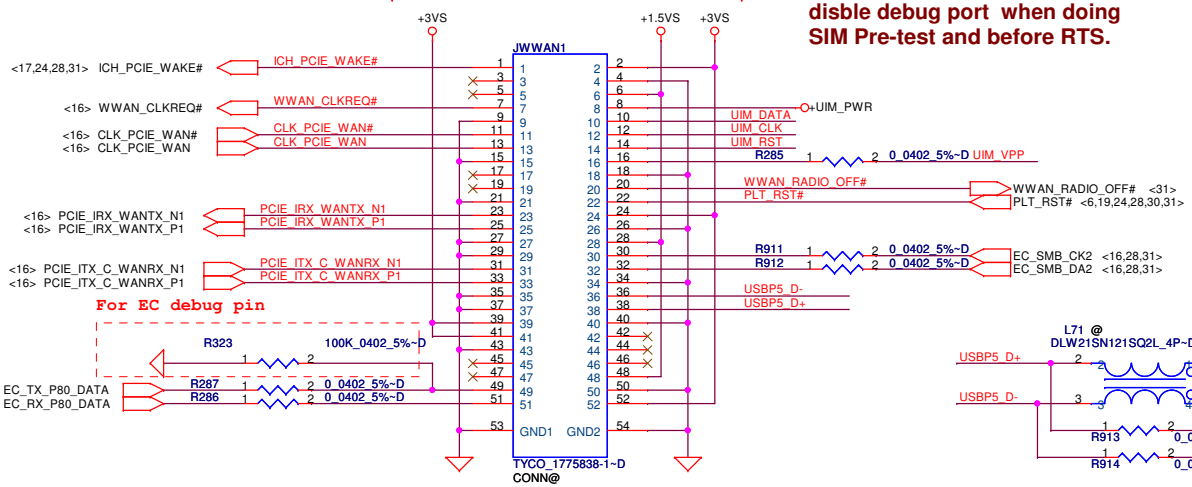
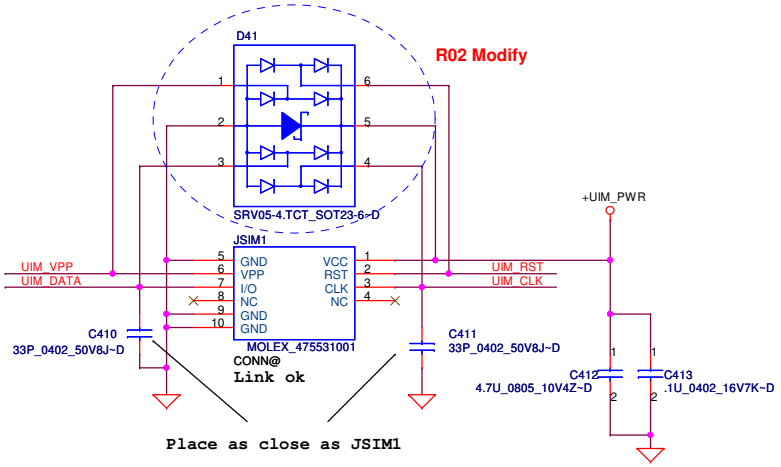
WWAN

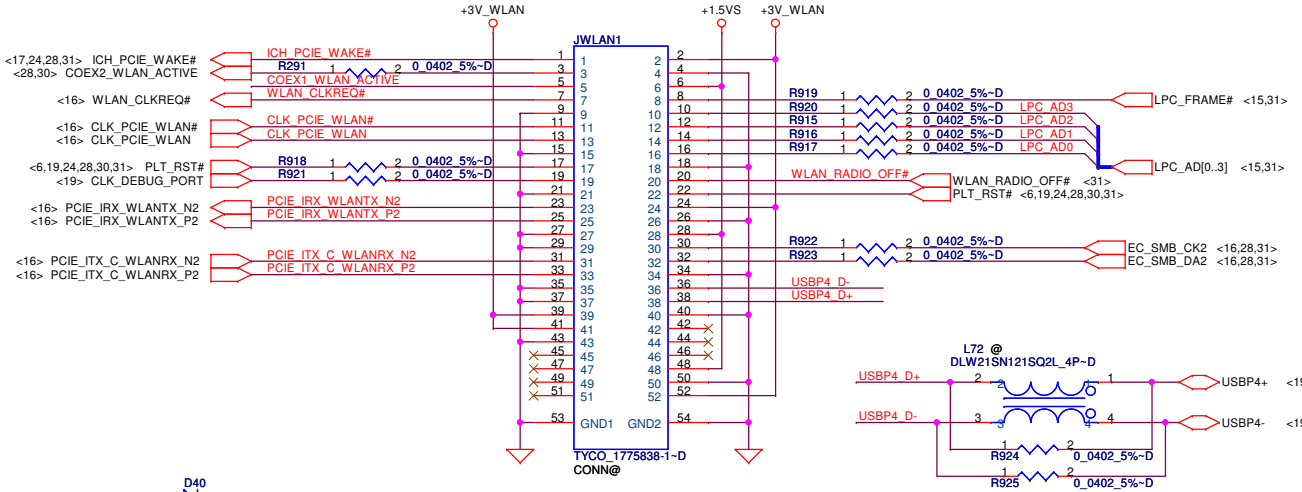


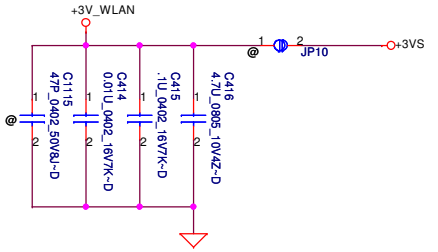
Don't forget to remove R287 or disble debug port when doing SIM Pre-test and before RTS.

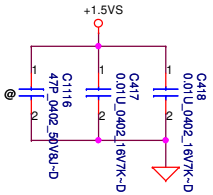


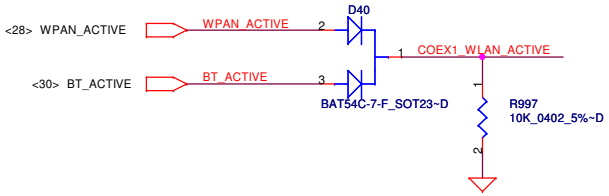


WLAN









Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: Mini Card_WLAN/WWAN

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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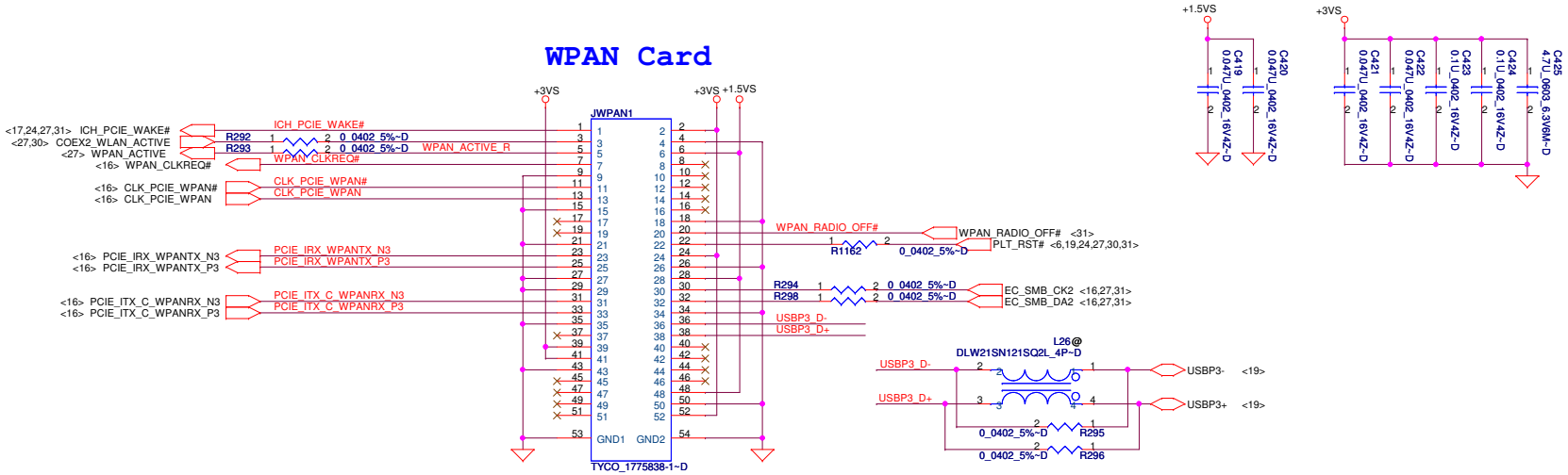
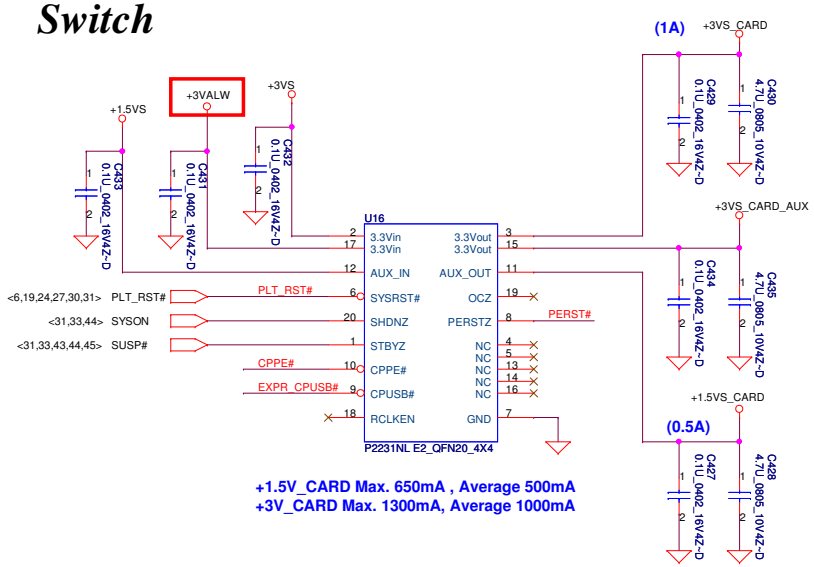
WPAN Card

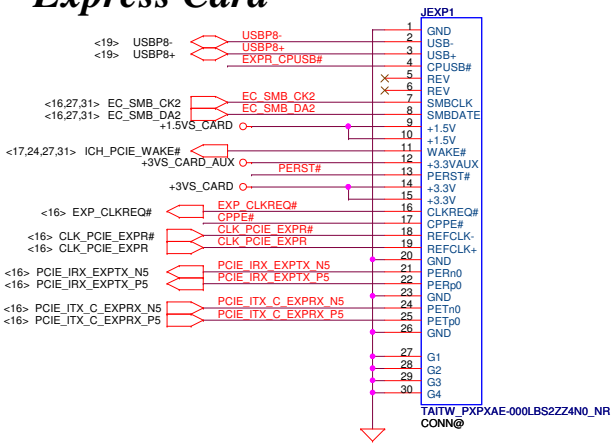


Express Card Power Switch



+1.5V_CARD Max. 650mA , Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

Express Card



Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **Mini Card_WPAN / Express**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

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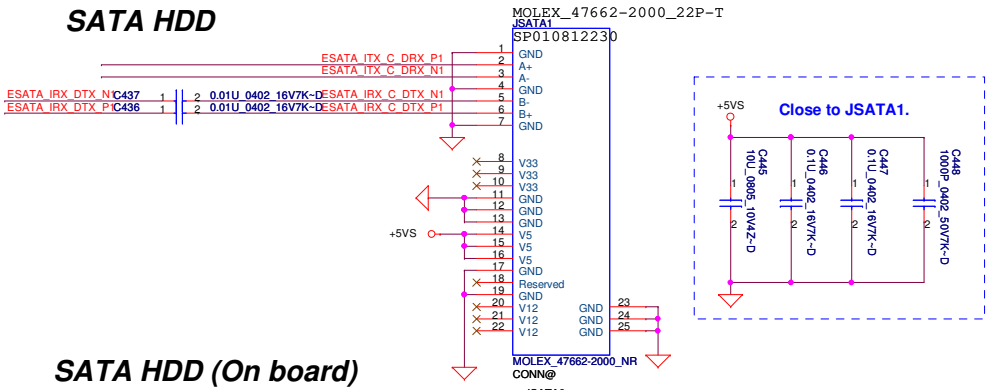
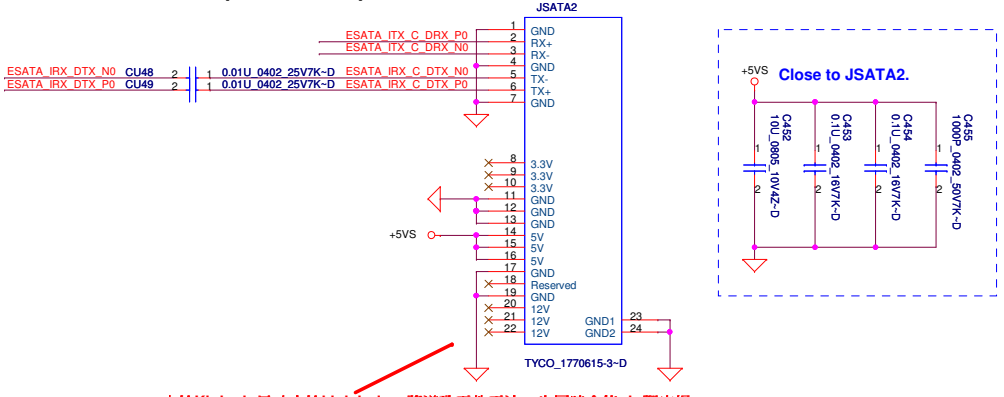
SATA HDD

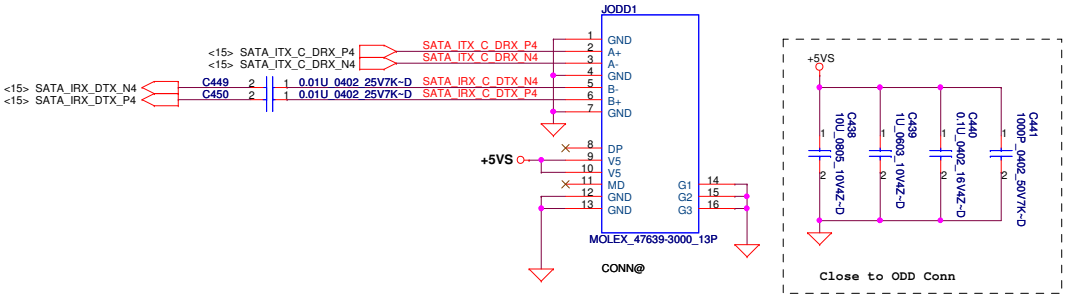


SATA HDD (On board)



由於Kink pin尺寸大於kink hole，將導致零件干涉，也同時會使pin腳空焊，
因此將 原HDD Conn.(REV.) –FOXCONN–SP01000LC0L layout 改成Tyco–SP01000E70L layout
即可解決造成pin腳空焊的問題

SATA ODD CONN



Place close U67 pin 2 & pin3

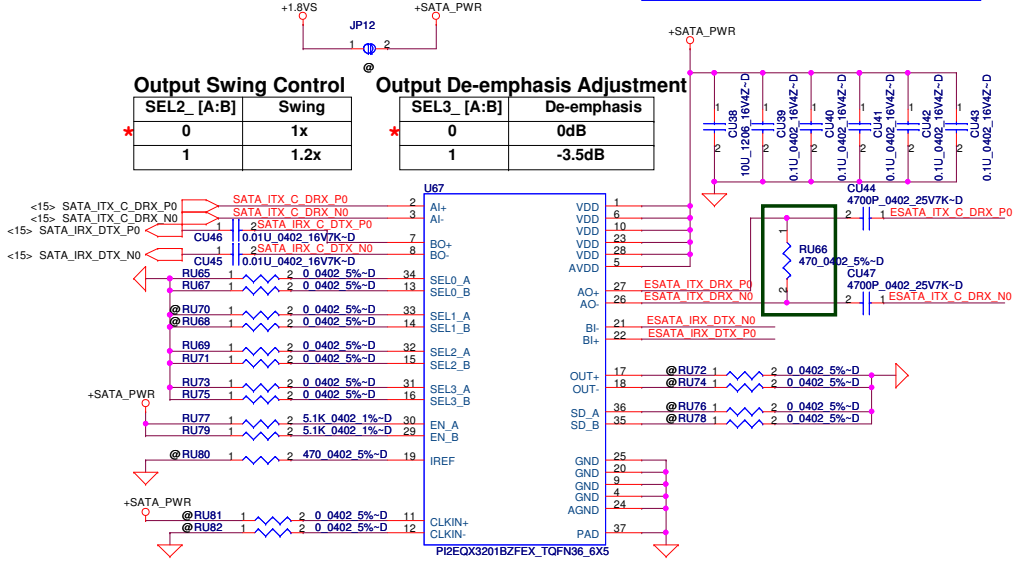
Place close U67 pin 21 & pin22

Output Swing Control

SEL2_ [A:B]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

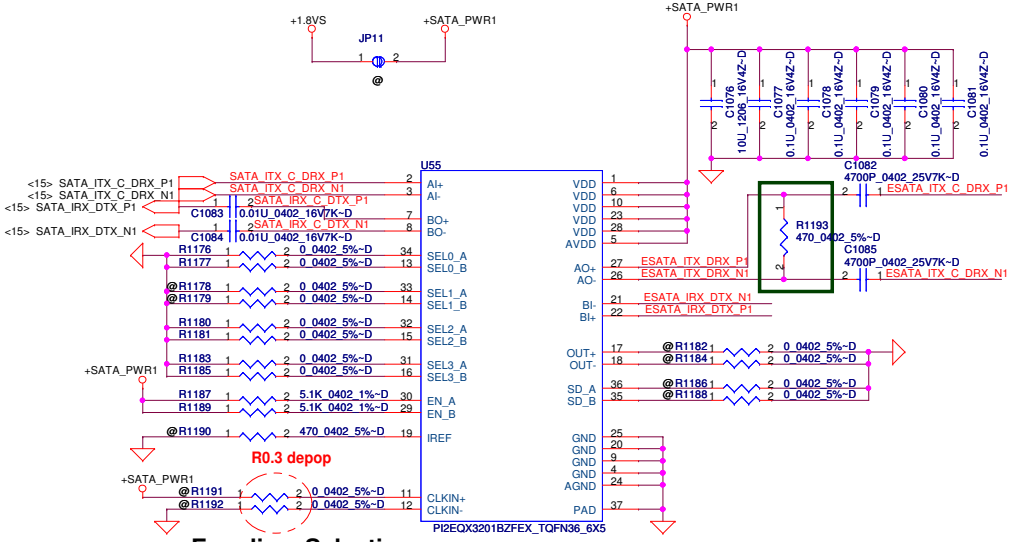
SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB



R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

Place close U55 pin 2 & pin3

Place close U55 pin 21 & pin22



R0.3 depop

Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: ODD/SATA HDD

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Place close U40 pin 2 & pin3

Place close U40 pin 21 & pin22

Output Swing Control

SEL2_ [A:B]	Swing
0	1x
* 1	1.2x

Output De-emphasis Adjustment

SEL3_ [A:B]	De-emphasis
* 0	0dB
1	-3.5dB

U40 PI2EQX3201BZFEX_TQFN36_6X5

R0.3 depop

R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
* 0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

U17 TPS2062ADR_SO8~D

U18 TS3USB221RSER_QFN10_2x1P5~D

S Logic"1" Work from BKT

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

R1.0 modify

Place close JESA1

JESA1 FOX_3Q3813C-RB1C3B-7F CONN@

Place close JCAM1

JCAM1 MOLEX_48227-0701 CONN@

Layout note: Pin5 thru individual via to GND layer

Bluetooth

JBT1 HRS_DF12(3.0)-14DP-0.5V(86)~D

Cardreader Connector

JCARD1 CONN@

to Single USB board

JSUSB1 FCI_10089709-010010-LF CONN@

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: USB/BlueTooth/Camera/ESATA

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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	VCC	3.3V+/-5%	0.6V~1.6V
	Ra	100K	
Board ID	VGA	Rb	
X00	UMA	0 +/- 5%	0 V
X01	UMA	8.2K+/- 5%	0.250V
X02	UMA	18K +/- 5%	0.503V
* MP	UMA	33K +/- 5%	0.819V

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **EC_KB926/BIOS/Reed SW**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

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To power board

R896 200_0402_5%~D

+5VALW

<31> PWR_BTN_LED#

PWR_LED+

PWR_BTN_LED#

PWR_ON-OFF_BTN#

JPBTN1

MOLEX_53261-0471

CONN@

D30

PWR_ON-OFF_BTN#

PESD24VS2UT_SOT23-3~D

Place close JPBTN1

Power Button Circuit

+3VALW

R335 100K_0402_5%~D

R0.3 Modify

D11

<14> PWR_ON-OFF_BTN#

ON_OFF <31>

51ON# <40>

BAT54C-7-F_SOT23~D

<31> EC_ON

EC_ON

R336 0_0402_5%~D

R337 10K_0402_5%~D

Q6

PMF3800SN_SC70-3

INT_KB_Conn.1

<31> KSI[0..7]

<31> KSO[0..18]

KSI[0..7]

KSO[0..18]

JAE_FL4S030HB3R3000

JKB1

CONN@

KSI0 @C485 100P_0402_50V8J~D

KSI1 @C487 100P_0402_50V8J~D

KSI2 @C489 100P_0402_50V8J~D

KSI3 @C491 100P_0402_50V8J~D

KSI4 @C493 100P_0402_50V8J~D

KSI5 @C495 100P_0402_50V8J~D

KSI6 @C497 100P_0402_50V8J~D

KSI7 @C499 100P_0402_50V8J~D

KSO0 @C501 100P_0402_50V8J~D

KSO1 @C503 100P_0402_50V8J~D

KSO2 @C505 100P_0402_50V8J~D

KSO3 @C507 100P_0402_50V8J~D

KSO4 @C509 100P_0402_50V8J~D

KSO5 @C511 100P_0402_50V8J~D

KSO6 @C486 100P_0402_50V8J~D

KSO7 @C488 100P_0402_50V8J~D

KSO8 @C490 100P_0402_50V8J~D

KSO9 @C492 100P_0402_50V8J~D

KSO10 @C494 100P_0402_50V8J~D

KSO11 @C496 100P_0402_50V8J~D

KSO12 @C498 100P_0402_50V8J~D

KSO13 @C500 100P_0402_50V8J~D

KSO14 @C502 100P_0402_50V8J~D

KSO15 @C504 100P_0402_50V8J~D

KSO16 @C506 100P_0402_50V8J~D

KSO17 @C508 100P_0402_50V8J~D

KSO18 @C510 100P_0402_50V8J~D

For EMI

RTCVREF

R1143 10K_0402_1%~D

R1144 220K_0402_5%

D51 SDMK0340L-7-F

C1068 0.1U_0402_16V4Z~D

CLOSE TO U48

<30> USB_DETECT#

USB_DETECT#

C1069 2.2U_0603_10V7K~D

U51 TC7SZ14FU_SSOP5~D

51ON# <40>

Q56 2N7002LT1G_SOT23-3

R1145 100K_0402_5%~D

R1238 0_0402_5%~D

R0.3 Modify

USB_DET#_DELAY <31>

D52 SDMK0340L-7-F

@ D58 SDMK0340L-7-F

Power share

Touch Screen Connector

D36

@CM1293-04SO_SOT23-6

USBP9-

USBP9+

+3VS

Place close JTCH1

R0.3 Modify

JTCH1

JST_SM08B-SURS-TF(LF)(SN)~D

CONN@

C927 0.1U_0402_16V4Z~D

Touch PAD/B Conn.

<31> TP_CLK

<31> LID_SW#

<31> TP_DATA

+HALL_VCC

C512 0.1U_0402_16V4Z~D

D55 PESD5V2S2UT_SOT23-3~D

C513 100P_0402_50V8J~D

C514 100P_0402_50V8J~D

JTP1

TYCO_2041084-6~D

CONN@

+3VALW

R933 0_0402_5%~D

R934 10K_0402_5%~D

C521 0.1U_0402_16V4Z~D

R0.3 Modify

Keyboard back light

+5VS

Q38 SI3456BDV-T1-E3 1N TSOP6 W/D

F1 0.75A_24V_1812L075-24DR-OK

20mil

B+_BIAS

R928 300K_0402_5%

C928 1U_0603_10V6K~D

EN_KBL

<31> EN_KBL#

Q40 PMF3800SN_SC70-3

R931 2M_0402_5%~D

+5VS_KBL

R927 10K_0402_5%~D

BKLT_KB_DET#

BKLT_KB_DET# <31>

BKLT_KB_DET

R929 0_0805_5%~D

R930 100K_0402_5%~D

Q39 MMBF170LT1G 1N SOT23-3

JKBL1

KB_BL_PWM

TYCO_2041084-4

CONN@

<31> KB_BL_PWM#

Q41 MMBF170LT1G 1N SOT23-3

Cap Sensor

<31> EC_FB_SDATA

<31> EC_FB_SCLK

<15,31> TOUCHKEY_TINT

L77 BLM18BD601SN1D_0603~D

L78 BLM18BD601SN1D_0603~D

TOUCHKEY_TINT

FB_SDATA

FB_SCLK

R1003 @ 0_0402_5%~D

C959 33P_0402_50V8J~D

C960 33P_0402_50V8J~D

D56 PESD5V2S2UT_SOT23-3~D

R0.3 Modify

JCAP1

TYCO_2041084-6

CONN@

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **PWROK/BTN/KB/Touch Pad**

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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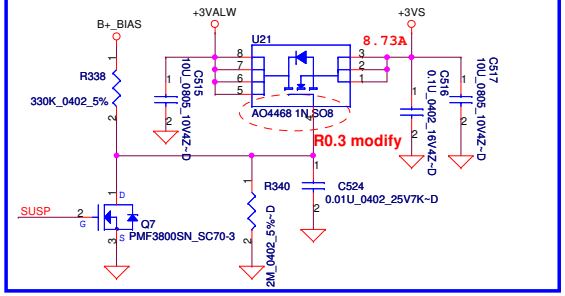
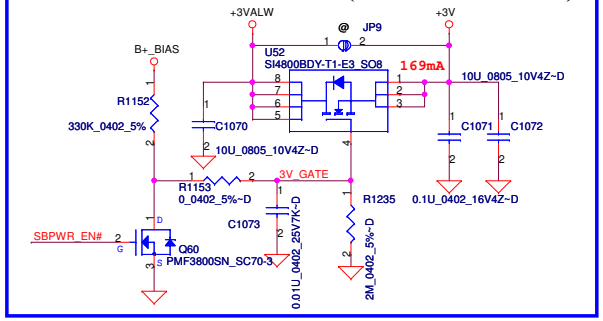
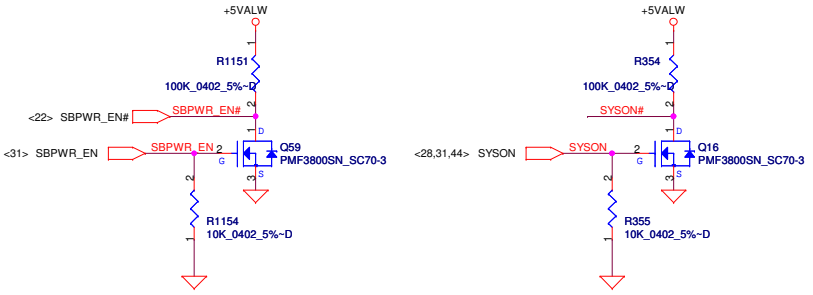
+3VALW to +3VS Transfer

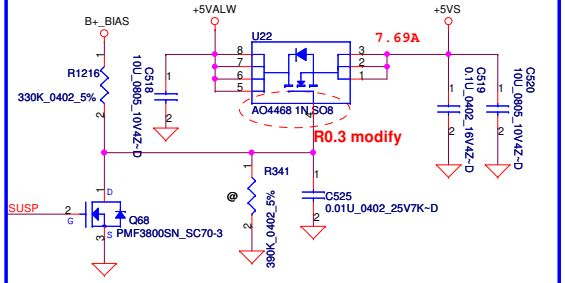


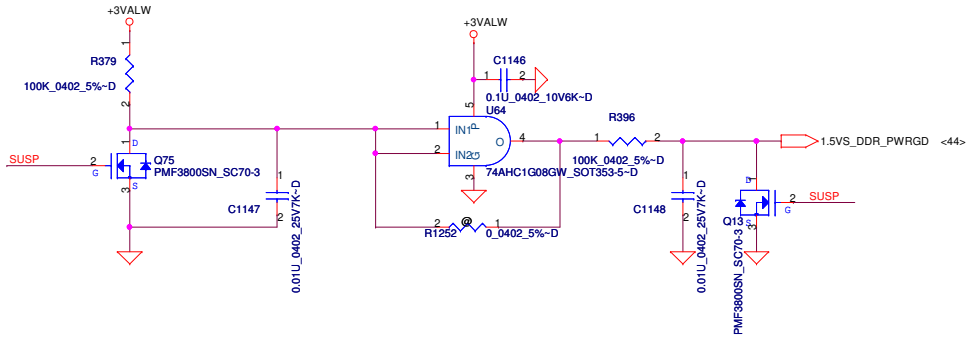
+3VALW to +3V Transfer (PCH AUX Power)

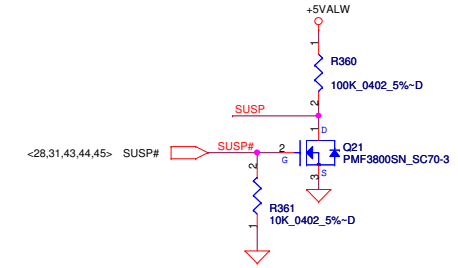




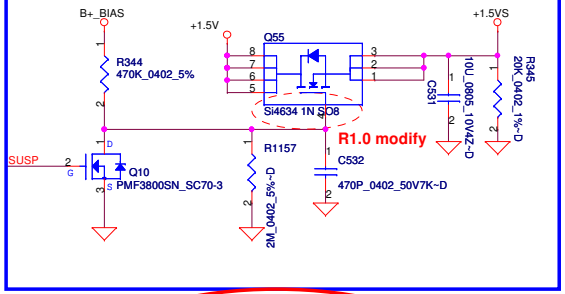
+5VALW to +5VS Transfer



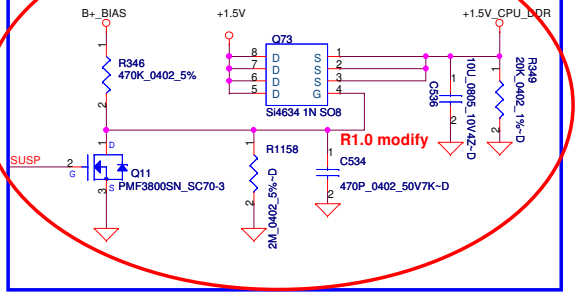




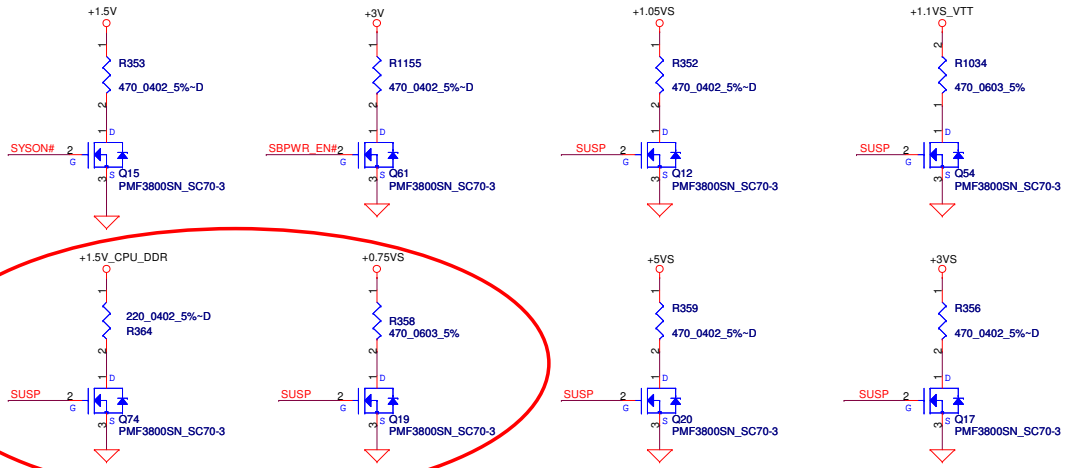
+1.5V to +1.5VS Transfer



+1.5V to +1.5VS_DDR Transfer



Discharge Circuit



Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: DC/DC Interface

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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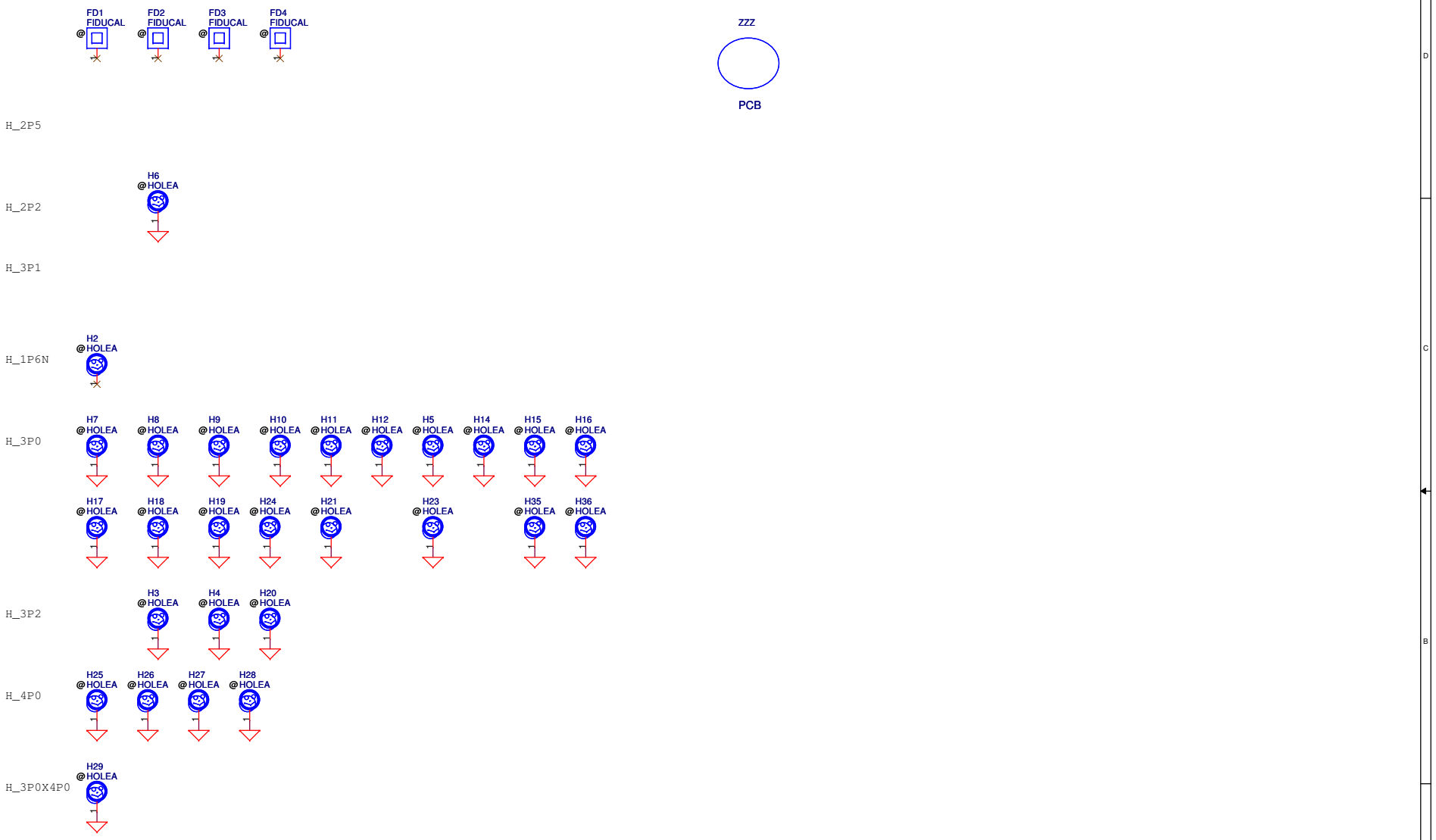

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **Screws**

Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

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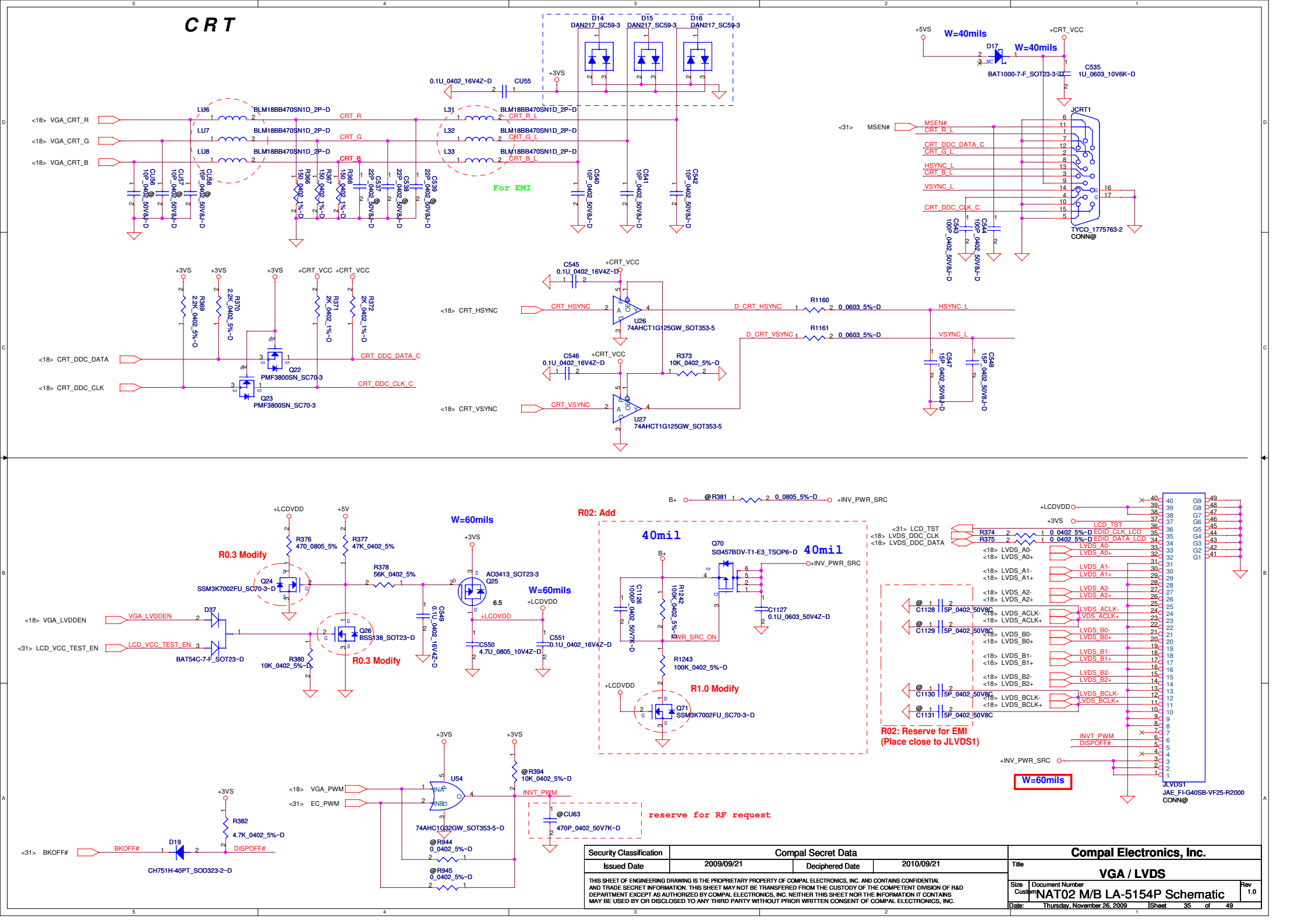


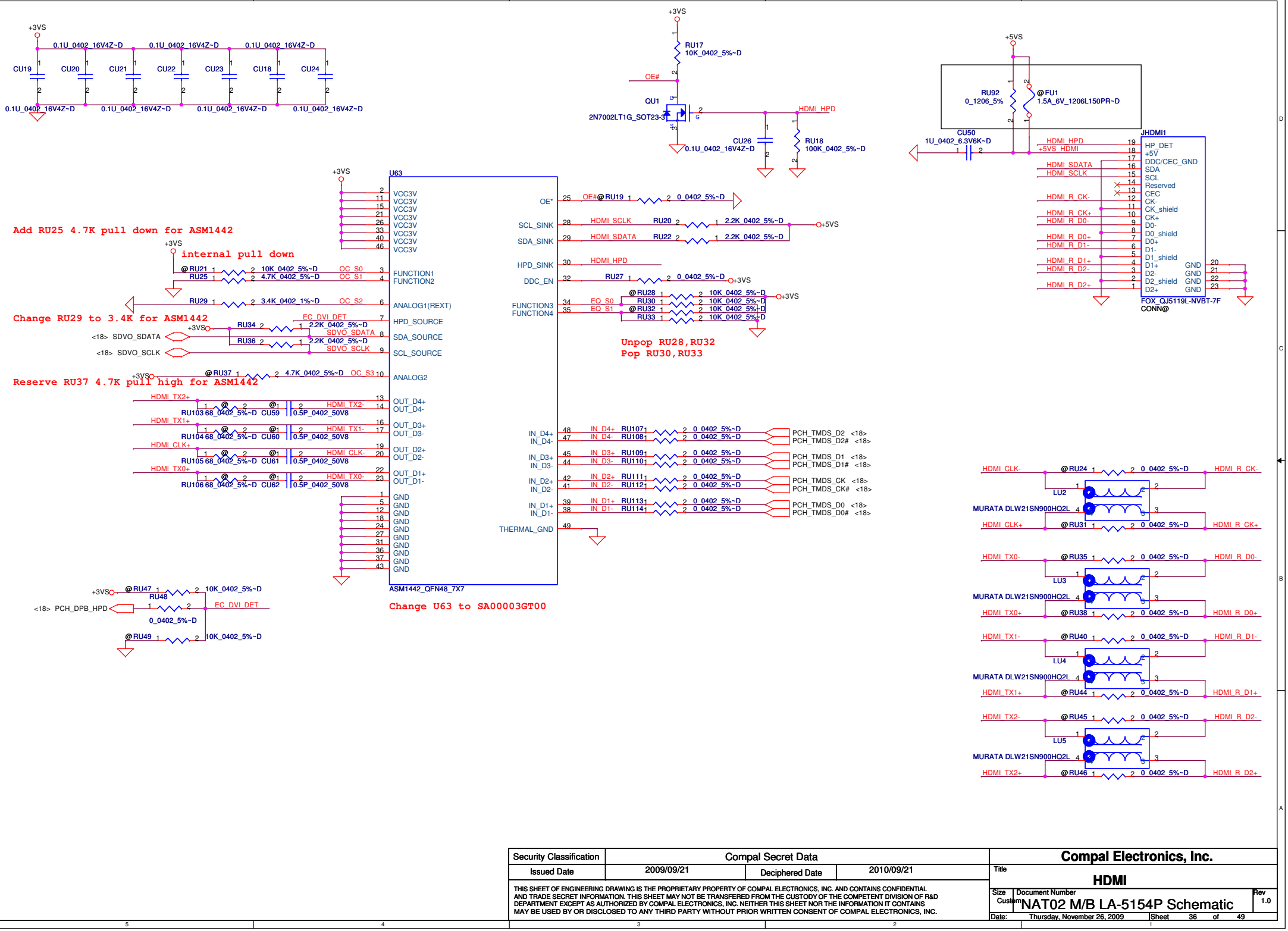
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **VGA / LVDS**

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

Date: Thursday, November 26, 2009 | Sheet 35 of 49



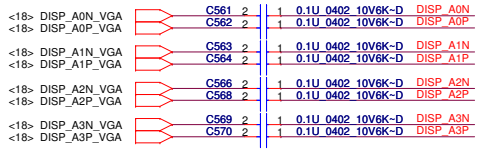
Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

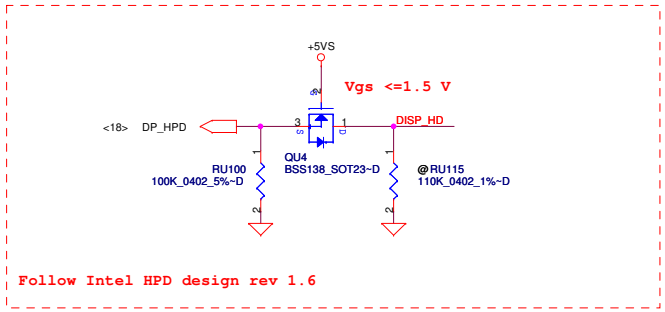
Compal Electronics, Inc.

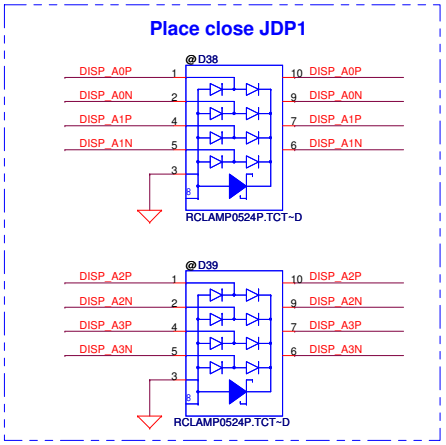
Title: **HDMI**

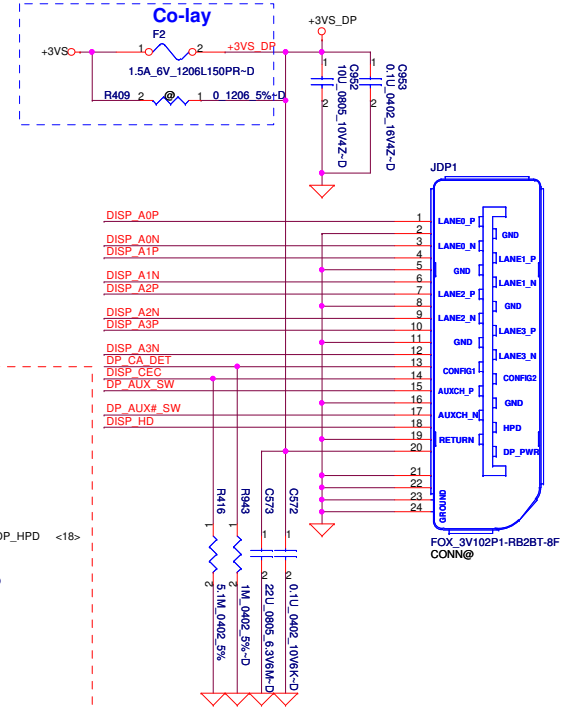
Size	Document Number	Rev
Custom	NAT02 M/B LA-5154P Schematic	1.0

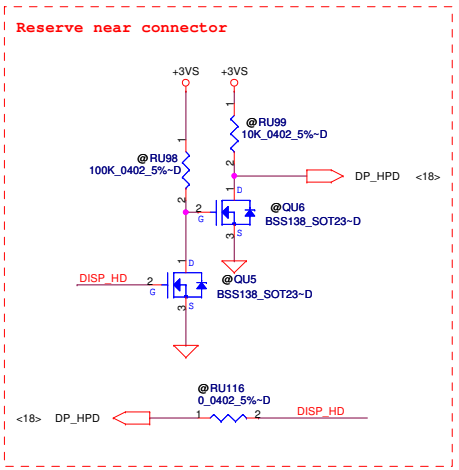
Date: Thursday, November 26, 2009 Sheet 36 of 49

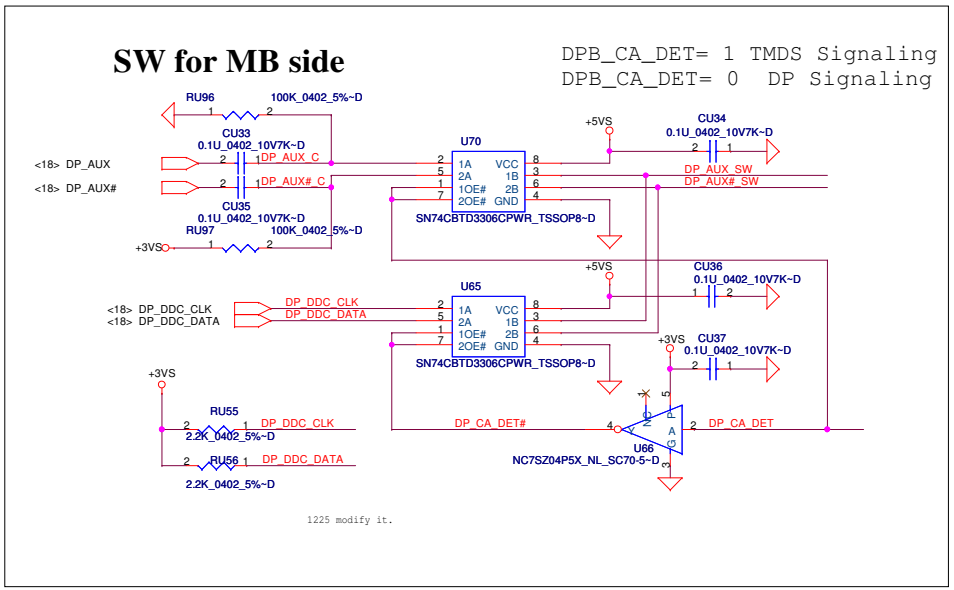












Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **Display Port**

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	08	PROCESSOR (4/6) PWR,Bypass	2009/07/22	Compal	Design change for IMVP6.5 current gain	R343 un-pop,R1072 pop,R1074 pop,R1073 unpop,R1075 pop,R1076 un-pop	Rev02 (X01)
02	16	PCH (2/9) PCIE, SMBUS, CLK	2009/08/10	Compal	XTAL25_IN should be pulled to GND using a 0Ω resistor.	Pop C1027 with a 0 ohm resister	Rev02 (X01)
03	06	+1.5V and resert	2009/08/10	Compal	Reduce S3 state Power	Add U63,Q36,R290,R310,R1103,R1136,C1142	Rev02 (X01)
04	09	Separate +1.5V power	2009/08/10	Compal	Reduce S3 state Power	Add PJP12,PJP13,PJP14,C1033,C1143,C1144,C1145	Rev02 (X01)
05	11	VrefDQ	2009/08/10	Compal	VrefDQ should be Maintained within SPEC during S3	Add Q37,R313	Rev02 (X01)
06	12	VrefDQ	2009/08/10	Compal	VrefDQ should be Maintained within SPEC during S3	Add Q44,R321	Rev02 (X01)
07	20	DDR_RST_GATE	2009/08/10	Compal	DDR_RST_GATE from GPIO46	Add GPIO46	Rev02 (X01)
08	33	VDDQ	2009/08/10	Compal	Processor VDDQ should be turned off in S3	Add Q73,Q11,R346,R349,R1158,C534,C536	Rev02 (X01)
09	15	GPIO1D	2009/08/18	Compal	ADD EC GPIO1D to PCH GPIO33	Add GPIO33	Rev02 (X01)
10	26	Sub woofer / Speaker AMP	2009/08/25	Compal	Reserve Subwoofer delay circuit for mute	Reserve D60, R1568, C1558	Rev02 (X01)
11	24,31		2009/08/25	Compal	Follow crystal vendor's recommend	C318,C319,C479,C481 BOM change to SE071330J8L (S CER CAP 33P 50V +-5% NPO 0402)	Rev02 (X01)
12	6	PROCESSOR (2/6) CLK,JTAG	2009/08/25	Compal	Intel S3 solution disable	POP R1054,R1055,R1121; Depop Q36,R290,R1103	Rev02 (X01)
13	11,12		2009/08/25	Compal	Intel S3 solution disable	Depop Q37,Q44,R56	Rev02 (X01)
14	33	DC/DC Interface	2009/08/25	Compal	Intel S3 solution disable	Depop Q73 Q73 BOM change to SB000001Y8L R358 BOM change to SD013470080 (S RES 1/10W 470 +-5% 0603)	Rev02 (X01)
15	35	VGA / LVDS	2009/08/25	Compal	to improve +LCDVDD voltage quality.	Pop C550	Rev02 (X01)
16	31	EC_KB926/BIOS/Reed SW	2009/08/25	Compal	Board ID change	R312 BOM change to 8.2K	Rev02 (X01)
17	31	EC_KB926/BIOS/Reed SW	2009/08/25	Compal	Reserve a 0ohm resister on SUS_PWR_ACK from PCH to EC	Reserve R1569 on SUS_PWR_ACK	Rev02 (X01)
18	35		2009/09/01	Compal	In common with MV	Q71 BOM change to SB00000960L	Rev02 (X01)
19	20		2009/09/21	Compal	S3 POWER Reduction update from Intel	Reserve C1559 on DDR_RST_GATE	Rev03 (X02)
20	30		2009/09/21	Compal	Reserve common choke on USB0	Reserve L89,R1571,R1572	Rev03 (X02)

Compal Electronics, Inc.

Title: HW PIR

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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	30	ESATA	2009/09/21	Compal	Add ESATA re-driver	Unpop R1164,R1165,R1166,R1167,R949,R950,R951,R952 pop JP13,C941,C944,C942,C943	Rev03 (X02)
02	33		2009/09/21	Compal		Q55,Q73 BOM change to SB00000DA0L	Rev03 (X02)
03	8		2009/09/21	Compal	BOM reason	C1009,C1010 BOM change to SGA00002U1L	Rev03 (X02)
04	25	HD Audio_IDT92HD73C	2009/09/21	Compal		BOM change for C336,C337,C354,C355	Rev03 (X02)
05	26	Sub woofer/Speaker AMP	2009/09/21	Compal	implement Subwoofer delay circuit for mute	Pop D60,C1558 R1568 change to 330K	Rev03 (X02)
06	37	Display Port	2009/09/21	Compal	Follow Intel HPD design	remove RU98,RU99;add RU115; change QU4 to SB50138008L	Rev03 (X02)
07	22	PCH (8/9) PWR	2009/09/21	Compal	Follow Intel design	Add LU9,CU64,CU65,CU66	Rev03 (X02)
08	11,12	DDRIII SO-DIMM	2009/10/08	Compal	Add M3 solution	Pop R166,R178	Rev03 (X02)
09	31	EC	2009/10/12	Compal	For ENE issue	Add R322 47K ohm pull high	Rev03 (X02)
10	17	PCH	2009/10/15	Compal	Bom reason	Change U2 SA007080B90 to SA007080100	Rev03 (X02)
11	19	PCH	2009/10/16	Compal	Design follow NAT01	Change R1139 SD02810038L to SE000000K8L	Rev03 (X02)
12	31	EC	2009/10/22	Compal	Change Board ID	Change R312 SD02882018L to SD02818028L	Rev03 (X02)
13	32	Touch Screen	2009/11/02	Compal	Add for Touch Screen issue	Add R1236	Rev03 (X02)
14	36	HDMI	2009/11/24	Compal	For HDMI Deep color mode	Unpop RU28,RU32 , Pop RU30,RU33	Rev10 (A00)
15	30	Camera	2009/11/02	Compal	improve 888MHZ noise	Add C458,C459	Rev10 (A00)
16	27	WLAN	2009/11/05	Compal	for EC debug pin	Add R323 100K pull down	Rev10 (A00)
17	9	PWR	2009/11/05	Compal	Intel suggest to reduce GFX voltage overshoot	Change RU93 to 470ohm	Rev10 (A00)
18	26	Sub woofer/Speaker Amp	2009/11/16	Compal	Follow NAT01 design	Change C922 & C1102 to 0.1uF	Rev10 (A00)
19	31	EC	2009/11/19	Compal	Change Board ID	Change R312 SD02818028L to SD02833028L	Rev10 (A00)
20	36	HDMI	2009/11/24	Compal	Change HDMI level shift	Change U63 to SA00003GT00	Rev10 (A00)
21	36	HDMI	2009/11/24	Compal	For HDMI Deep color mode	Add RU25 4.7K pull down for ASM1442	Rev10 (A00)
22	36	HDMI	2009/11/24	Compal	For HDMI Deep color mode	Reserve RU37 4.7K pull high for ASM1442	Rev10 (A00)
23	36	HDMI	2009/11/24	Compal	For HDMI Level shift ASM1442	Change RU29 to 3.4K for ASM1442	Rev10 (A00)
24							
25							

Compal Electronics, Inc.

Title: HW PIR

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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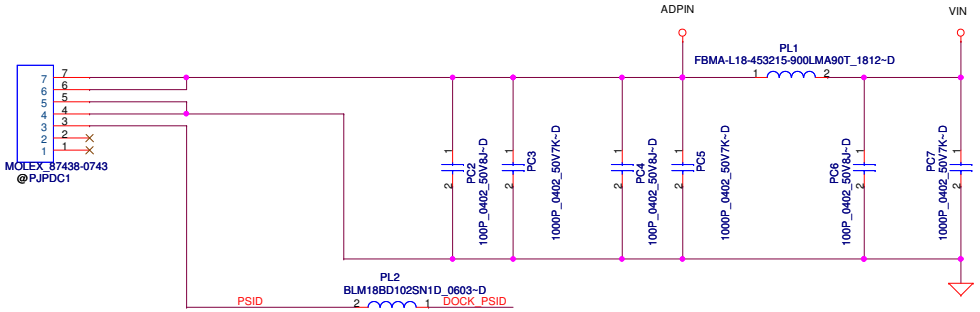

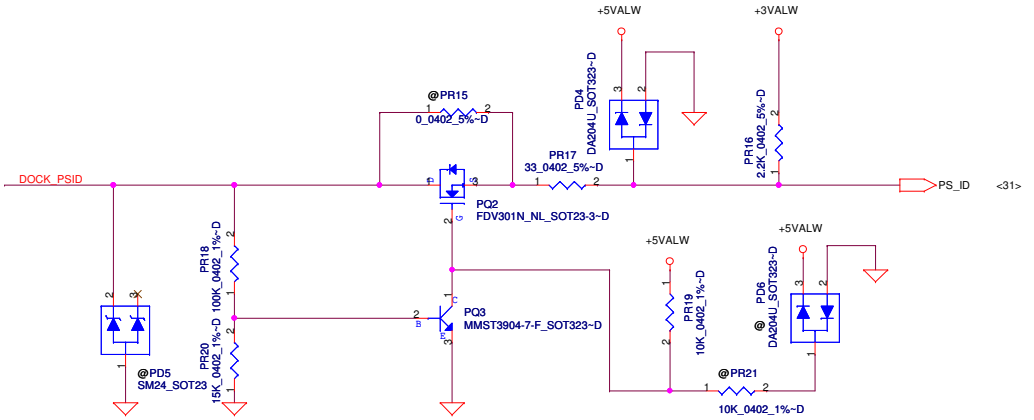

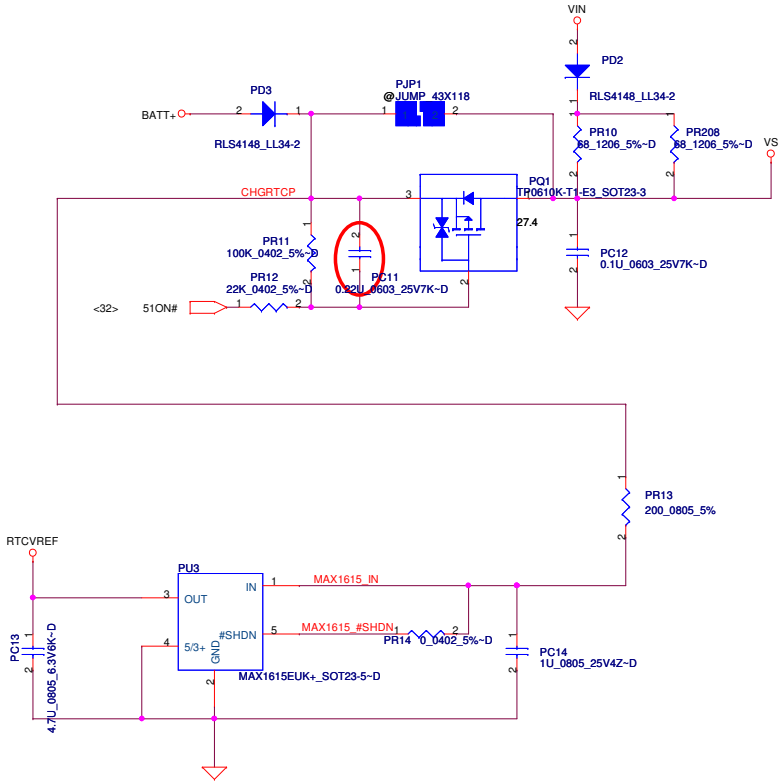

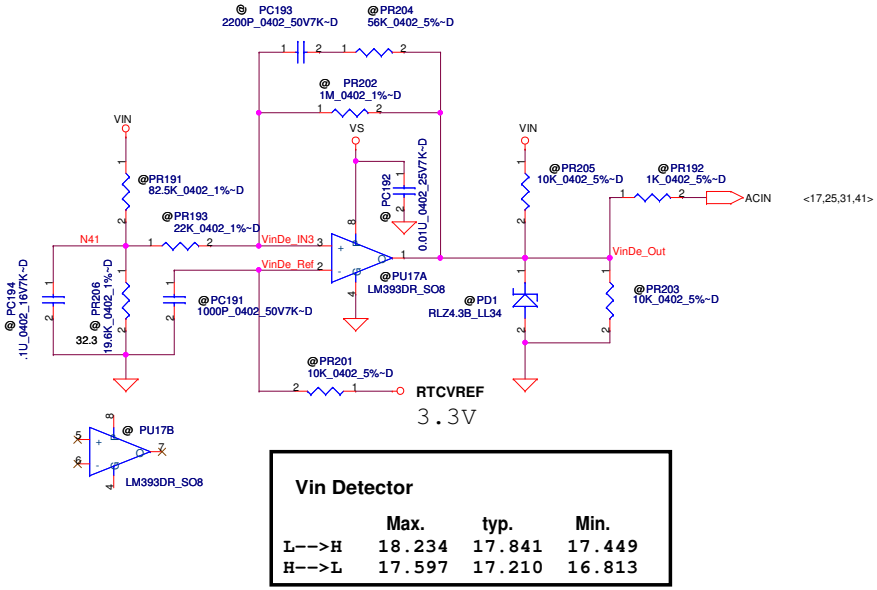

Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: **DCIN/Precharger**

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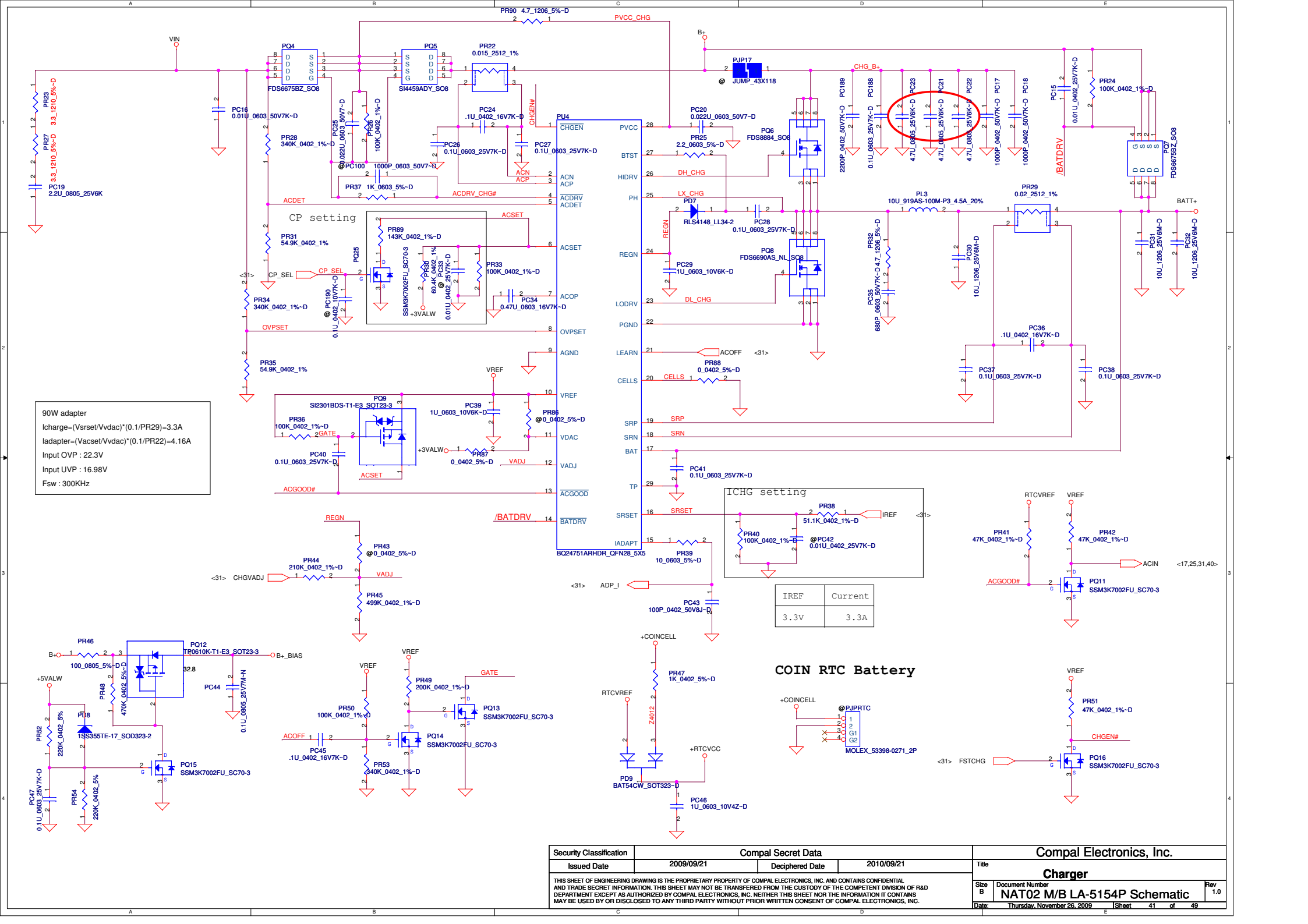
90W adapter
Icharge=(Vsrset/Vvdac)*(0.1/PR29)=3.3A
Iadapter=(Vacset/Vvdac)*(0.1/PR22)=4.16A
Input OVP : 22.3V
Input UVP : 16.98V
Fsw : 300KHz
CP setting
ICHG setting
IREF | Current
3.3V | 3.3A
COIN RTC Battery
PU4
BQ24751ARHDR_QFN28_5X5
PQ4 FDS6675BZ_SO8
PQ5 SI4459ADY_SO8
PQ6 FDS8884_SO8
PQ7 FDS6675BZ_SO8
PQ8 FDS6690AS_NL_SO8
PQ9 SI2301BDS-T1-E3_SOT23-3
PQ11 SSM3K7002FU_SC70-3
PQ12 TP0610K-T1-E3_SOT23-3
PQ13 SSM3K7002FU_SC70-3
PQ14 SSM3K7002FU_SC70-3
PQ15 SSM3K7002FU_SC70-3
PQ16 SSM3K7002FU_SC70-3
PD7 RLS4148_LL34-2
PD8 1SS355TE-17_SOD323-2
PD9 BAT54CW_SOT323-D
PJP17 JUMP_43X118
PL3 10U_919AS-100M-P3_4.5A_20%
@PJPRTC MOLEX_53398-0271_2P
VIN
B+
BATT+
+5VALW
+3VALW
+COINCELL
+RTCVCC
RTCVREF
VREF
PVCC_CHG
CHG_B+
/BATDRV
B+_BIAS
CHGEN
CHGEN#
ACDET
ACDRV_CHG#
ACSET
CP_SEL
OVPSET
VADJ
GATE
REGN
ACGOOD#
ACOFF
ADP_I
CHGVADJ
IREF
SRP
SRN
BAT
CELLS
LEARN
FSTCHG
ACIN
PR90 4.7_1206_5%~D
PR22 0.015_2512_1%
PR23 3.3_1210_5%~D
PR27 3.3_1210_5%~D
PC19 2.2U_0805_25V6K
PC16 0.01U_0603_50V7K~D
PR28 340K_0402_1%~D
PC25 0.022U_0603_50V7~D
PR26 100K_0402_1%~D
@PC100 1000P_0603_50V7~D
PR37 1K_0603_5%~D
PC24 .1U_0402_16V7K~D
PC26 0.1U_0603_25V7K~D
PC27 0.1U_0603_25V7K~D
PC20 0.022U_0603_50V7~D
PR25 2.2_0603_5%~D
PR31 54.9K_0402_1%
PR89 143K_0402_1%~D
PR30 60.4K_0402_1%
@PC33 0.01U_0402_25V7K~D
PR33 100K_0402_1%~D
PC34 0.47U_0603_16V7K~D
PR34 340K_0402_1%~D
@PC190 0.1U_0402_10V7K~D
PR35 54.9K_0402_1%
PR36 100K_0402_1%~D
PC40 0.1U_0603_25V7K~D
PC39 1U_0603_10V6K~D
PR86 @0_0402_5%~D
PR87 0_0402_5%~D
PR88 0_0402_5%~D
PC41 0.1U_0603_25V7K~D
PR38 51.1K_0402_1%~D
PR40 100K_0402_1%~D
@PC42 0.01U_0402_25V7K~D
PR39 10_0603_5%~D
PC43 100P_0402_50V8J~D
PR43 @0_0402_5%~D
PR44 210K_0402_1%~D
PR45 499K_0402_1%~D
PR46 100_0805_5%~D
32.8
PC44 0.1U_0805_25V7M~N
PR48 470K_0402_5%
PR52 220K_0402_5%
PR54 220K_0402_5%
PC47 0.1U_0603_25V7K~D
PR49 200K_0402_1%~D
PR50 100K_0402_1%~D
PC45 .1U_0402_16V7K~D
PR53 340K_0402_1%~D
PR47 1K_0402_5%~D
Z4012
PC46 1U_0603_10V4Z~D
PC189 2200P_0402_50V7K~D
PC188 0.1U_0603_25V7K~D
PC23 4.7U_0805_25V6K~D
PC21 4.7U_0805_25V6K~D
PC22 4.7U_0805_25V6K~D
PC17 1000P_0402_50V7K~D
PC18 1000P_0402_50V7K~D
PC15 0.01U_0402_25V7K~D
PR24 100K_0402_1%~D
PR29 0.02_2512_1%
PC28 0.1U_0603_25V7K~D
PC29 1U_0603_10V6K~D
PR32 4.7_1206_5%~D
PC35 680P_0603_50V7K~D
PC30 10U_1206_25V6M~D
PC31 10U_1206_25V6M~D
PC32 10U_1206_25V6M~D
PC36 .1U_0402_16V7K~D
PC37 0.1U_0603_25V7K~D
PC38 0.1U_0603_25V7K~D
PR41 47K_0402_1%~D
PR42 47K_0402_1%~D
PR51 47K_0402_1%~D
<31>
<17,25,31,40>
Security Classification: Compal Secret Data
Issued Date: 2009/09/21
Deciphered Date: 2010/09/21
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title: Charger
Size: B
Document Number: NAT02 M/B LA-5154P Schematic
Rev: 1.0
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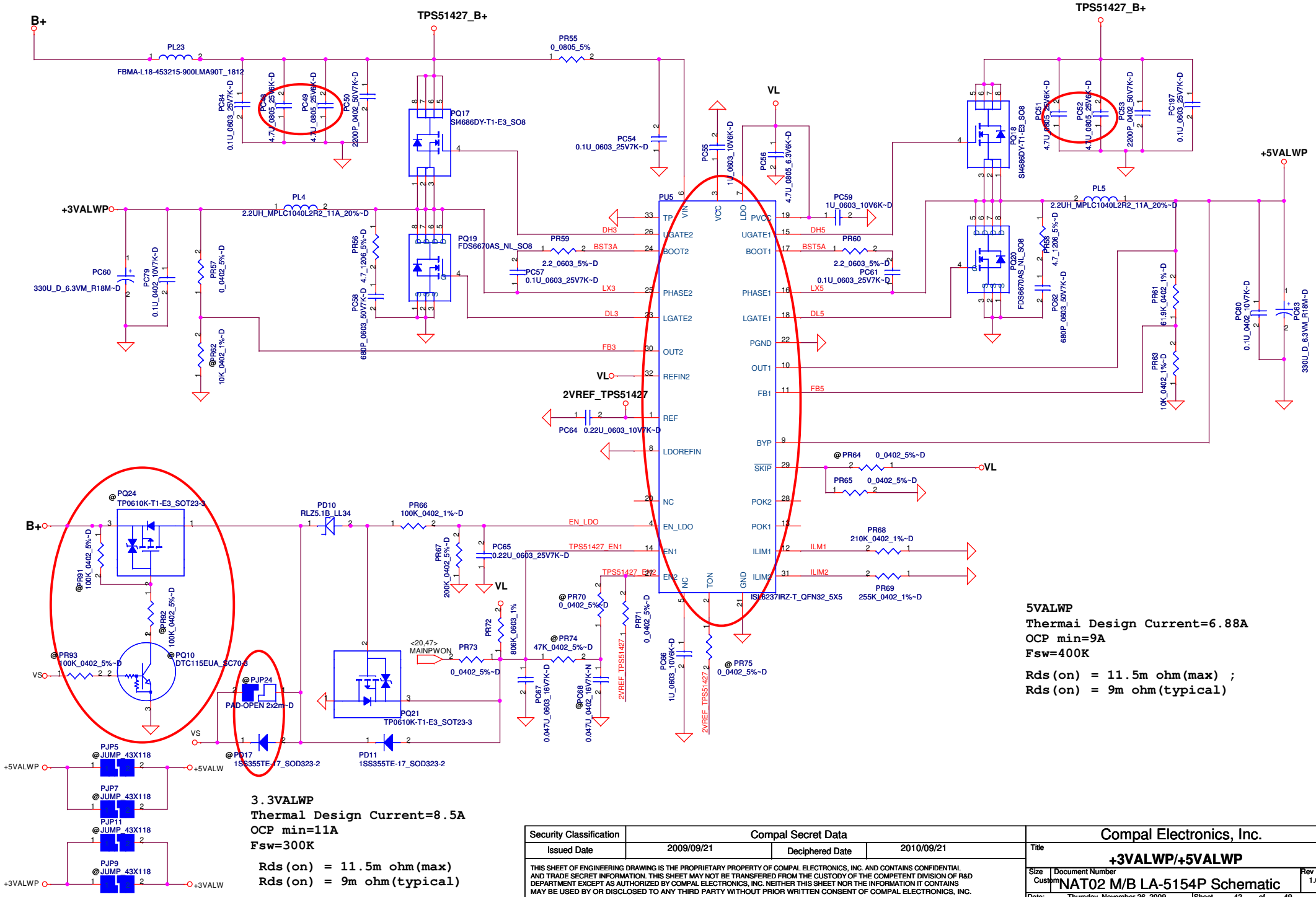

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: +3VALWP/+5VALWP

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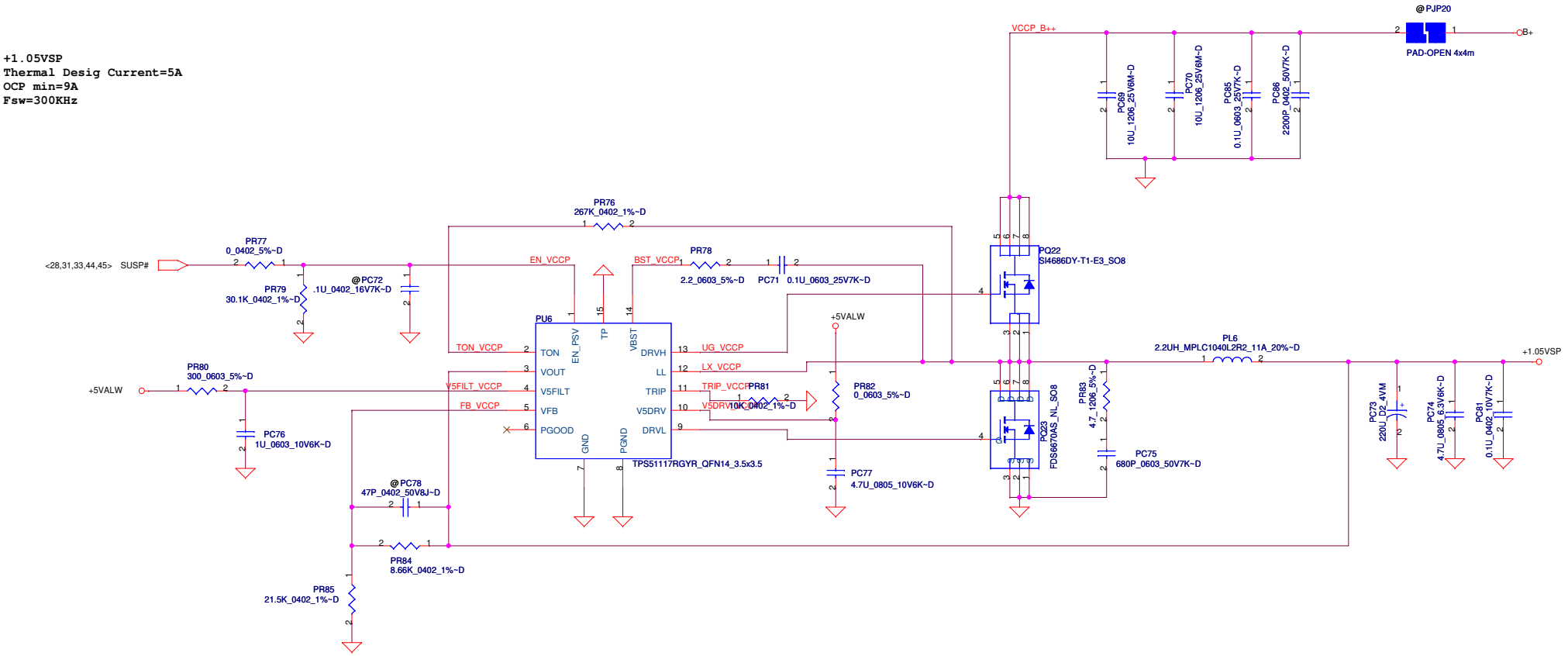
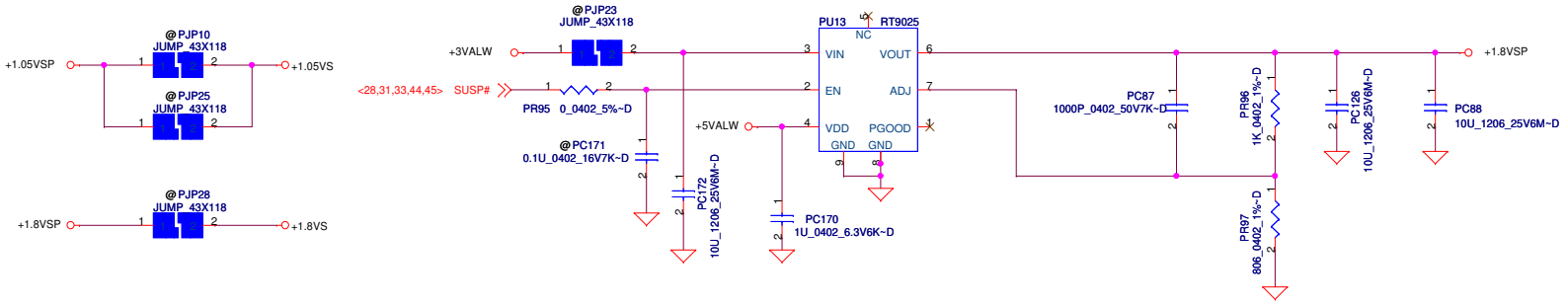
+1.05VSP
Thermal Desig Current=5A
OCP min=9A
Fsw=300KHz





+1.8VSP
Thermal Desig Current=0.69A

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: +1.05VSP/+1.8VSP

Size	Document Number	Rev
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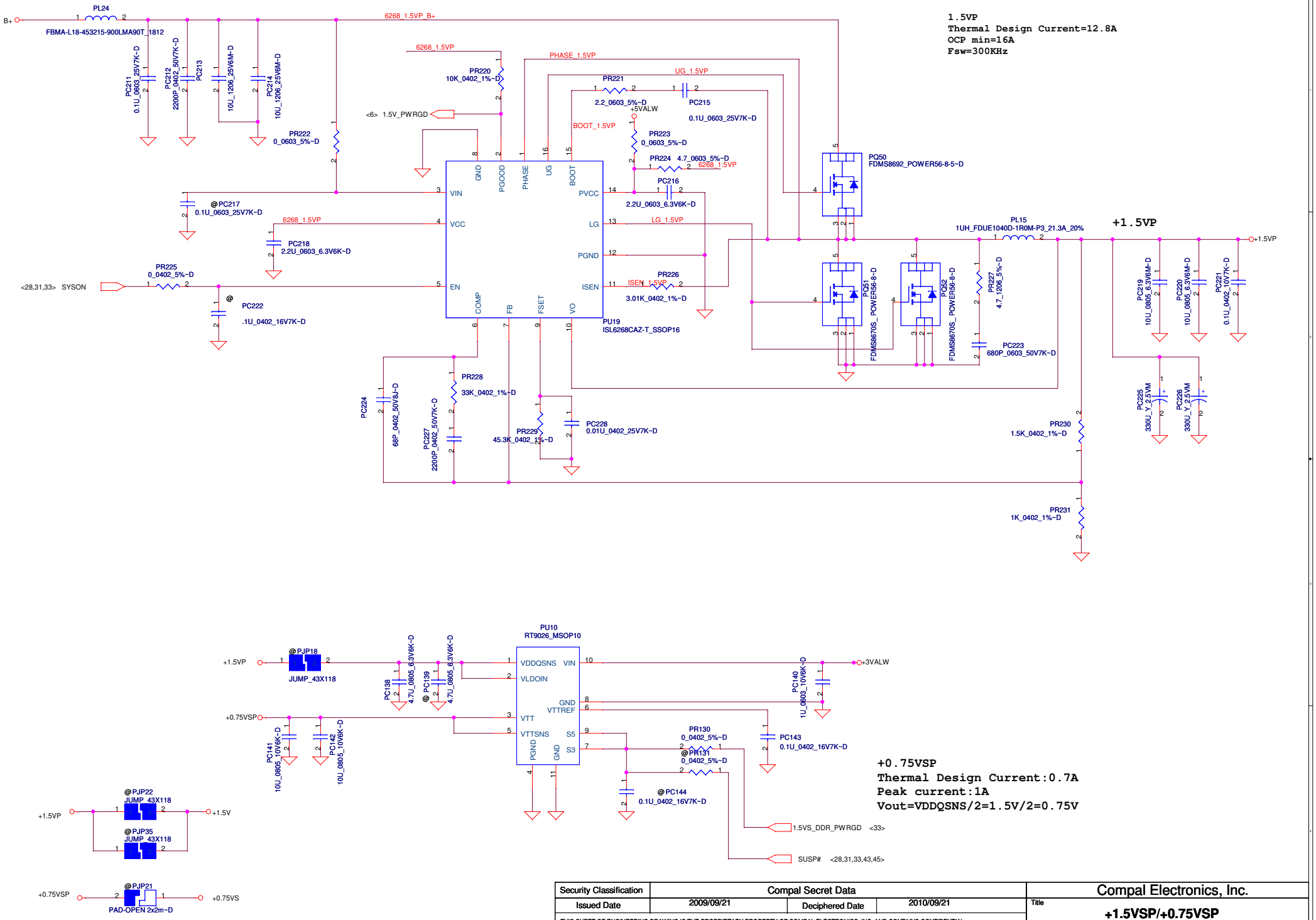

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

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Title: +1.5VSP/+0.75VSP

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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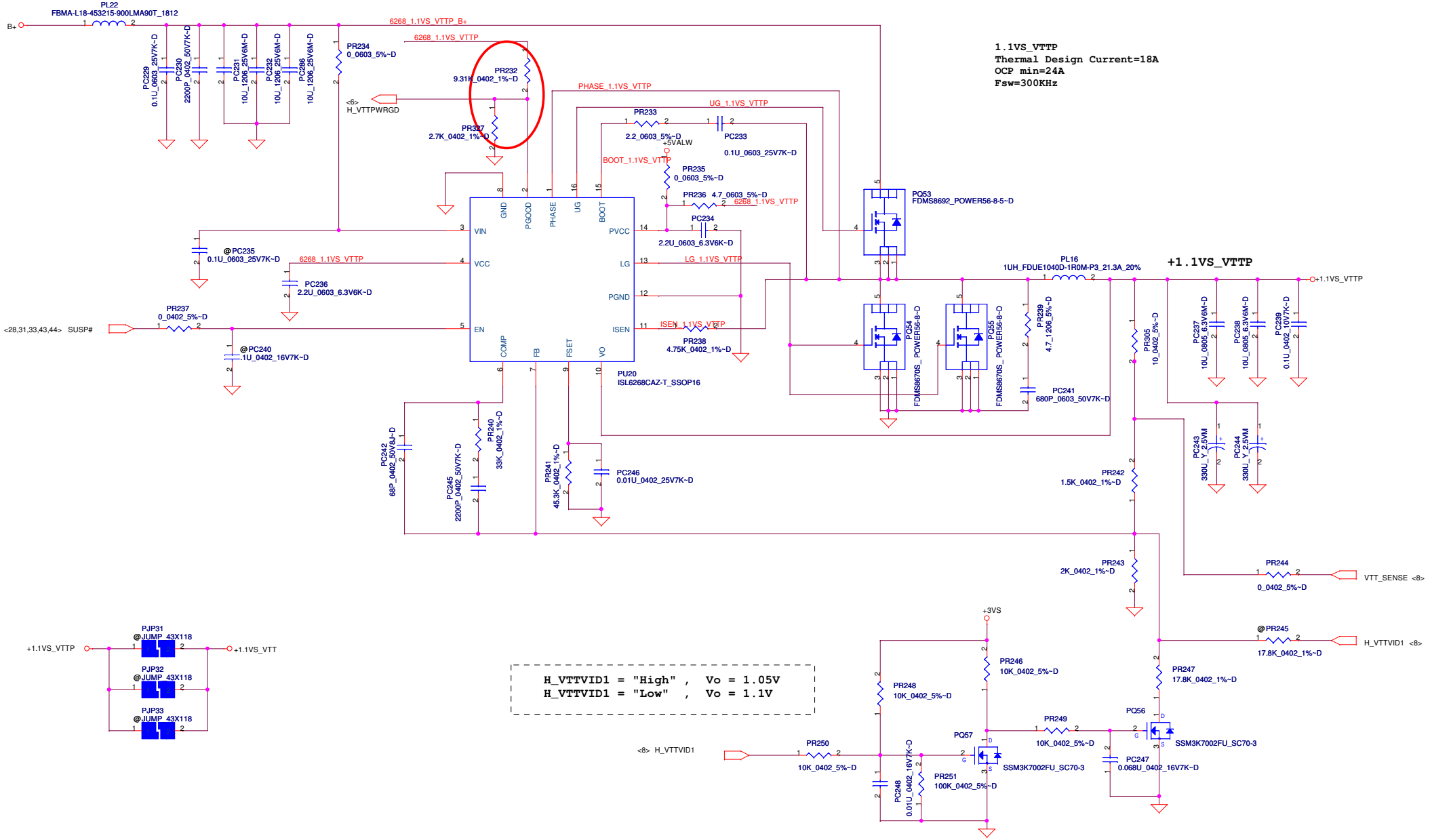

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: +1.1VS_VTTP

Size: Custom | Document Number: NAT02 M/B LA-5154P Schematic | Rev: 1.0

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OCP calculation: Assume DCR=0.88mOhm
G1=Rn/(Rn+Rsum/3),
where Rn=PR224//(PR171+PH5); Rsum=PR143,PR215
DROOP=2*(DCR/2)*G1*Rdroop/Ri=1.896mOhm
where Rdroop=PR161;Ri=PR212
Iocp=42.7u*Rdroop/DROOP=~68A.

Iccmax= TBD
I_TDC=TDB
OCP=68A, Intel spec=TDB

Layout Note:
PH3 place near Phase1 L-MOS

Layout Note:
Place near Phase1 Choke

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
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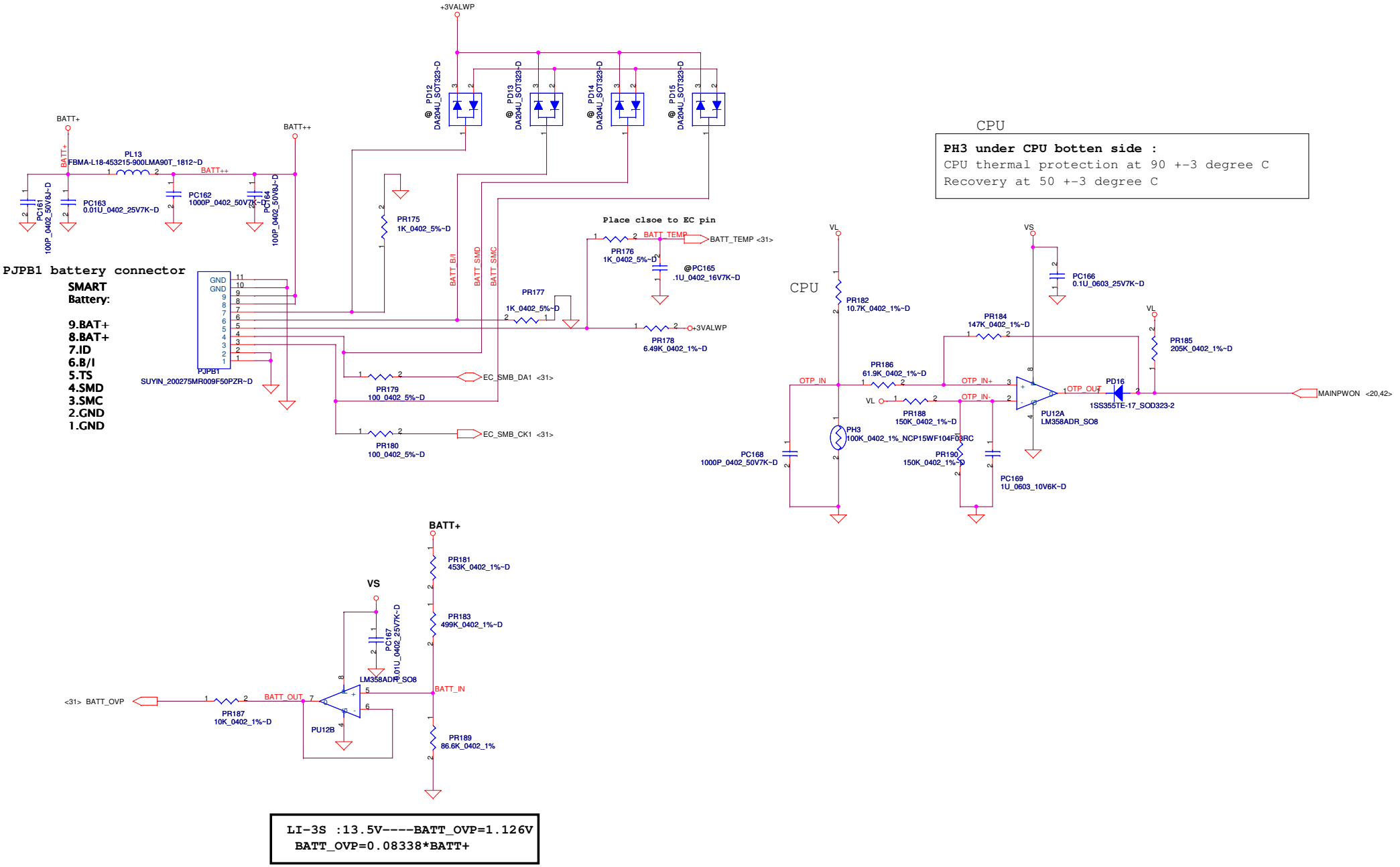
Battery Connect/OTP



LI-3S :13.5V----BATT_OVP=1.126V
BATT_OVP=0.08338*BATT+

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: BATTERY CONN

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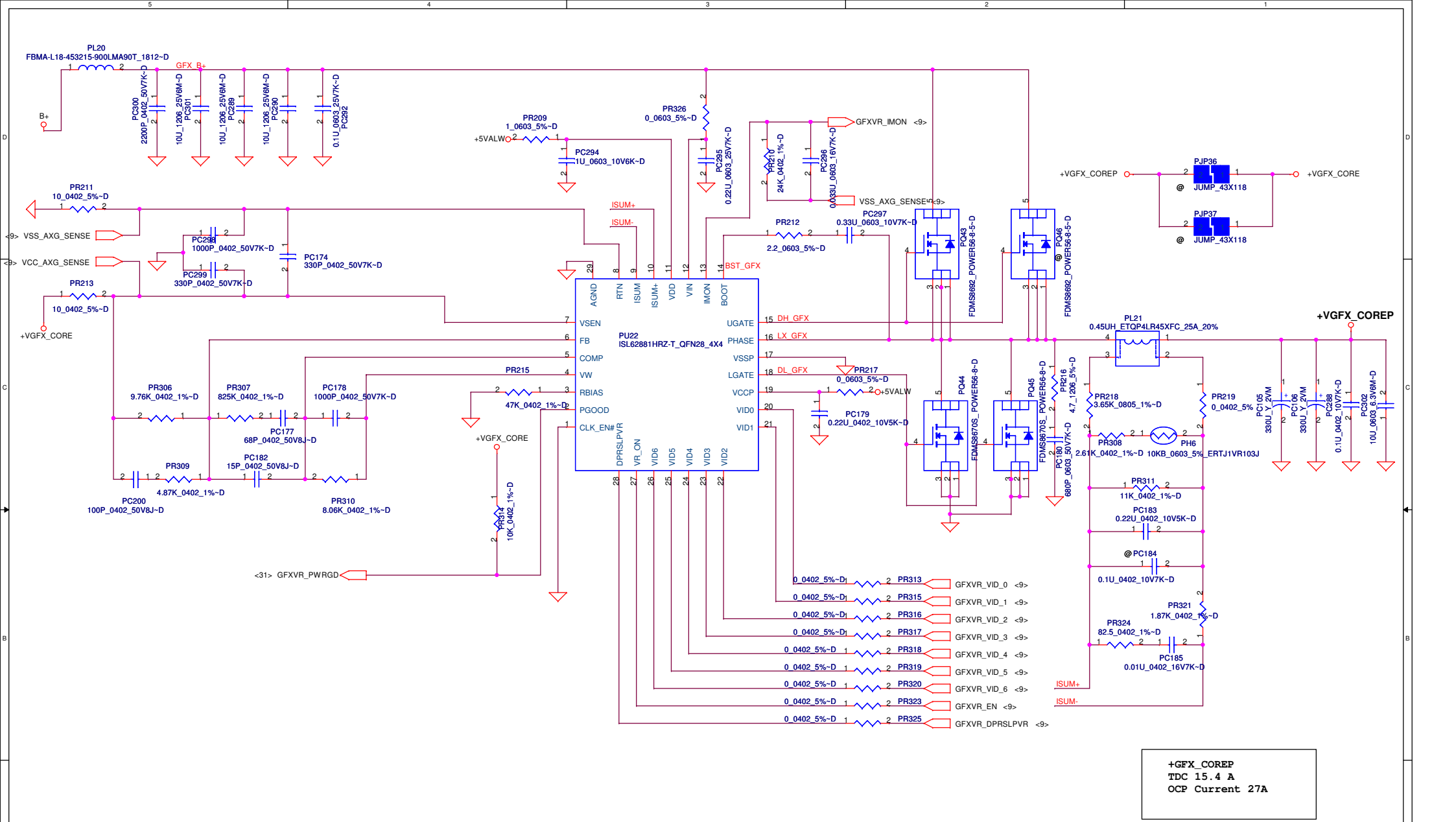

Security Classification	Compal Secret Data		
Issued Date	2009/09/21	Deciphered Date	2010/09/21

Compal Electronics, Inc.

Title: +GFX_COREP

Size	Document Number	Rev
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	P51	+1.1VS_VTTP	08/31	Lin Will	Slove EMI	Add PL22 and Change PR233 form 0 ohm to 2.2 ohm.	X01
02	P53	+CPU_Core	08/31	Lin Will	Slove EMI	Change PR259 and PR291 from 0 ohm to 2.2 ohm.	X01
03	P55	+GFX_COREP	08/31	Lin Will	Adjust load-line and Imon	Change PR306 form 9.54K to 9.76K, PR210 from 22.3K to 24K and PC296 from 0.22uF to 0.033uF.	X01
04	P55	+GFX_COREP	08/31	Lin Will	Adjust output voltage ripple and thermal dispation	Add PQ46 and change PC289, PC290, PC301 from 4.7uF to 10uF, and PC105, PC106 from 330uF 9mohm to 330uF 6mohm.	X01
05	P43	+1.05VSP/+0.75VSP	10/14	Lin Will	Slove the IC input power sequence.	Change TPS51117 V5FILT and V5DRV from 5VS to 5VALW.	X02
06	P42	+3VALWP/+5VALWP	10/14	Lin Will	Slove EMI.	Change PJP19 to PL23, and PR59, PR60 from 0 ohm to 2.2 ohm.	X02
07	P44	+1.5VSP/+0.75VSP	10/14	Lin Will	Slove EMI.	Change PJP29 to PL24.	X02
08	P45	+1.1VS_VTTP	11/20	Lin Will	Low down the power consumption.	Change PR232 from 43.2K to 9.31K, and add PR327 2.7K.	X03
09	P41/P42	Charger +3VALWP/+5VALWP	11/20	Lin Will	1206 size shortage issue.	Change SE142475K8L(1206) to SE000006R8L(0805), and SE041224K8L(1206) to SE000005Z8L(0603).	X03
10	P42	+3VALWP/+5VALWP	11/20	Lin Will	When adapter inserts and pulls out quickly two twice, it will make TPS51427 out of electricity.	Add PR91,PR92,PR93 100K, PQ24 TP0610K, PQ10 DTC115EUA, and PD17 1SS355TE-17. But all unpop. Change PU5 to ISL6237, and add PJP24.	X03

Compal Electronics, Inc.

Title: PWR PIR-1

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