

NDU00/NDU10

Streamline-S 11.6"

Streamline-M 13.3"

LA-6031P REV 1.0 Schematic

Intel Arrandale SFF/IBEX PEAK

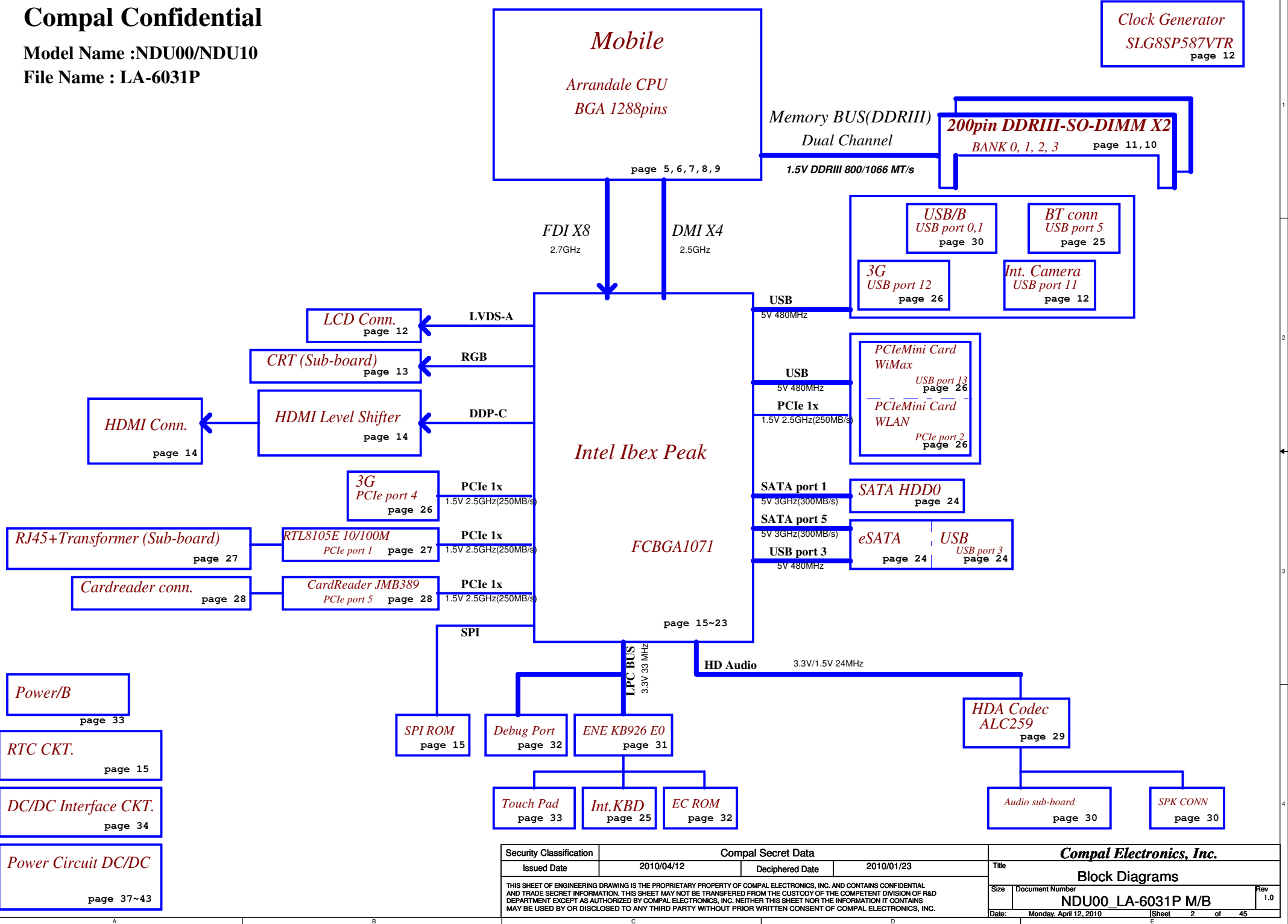
2010-04-12 Rev 1.0

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				Cover Page	
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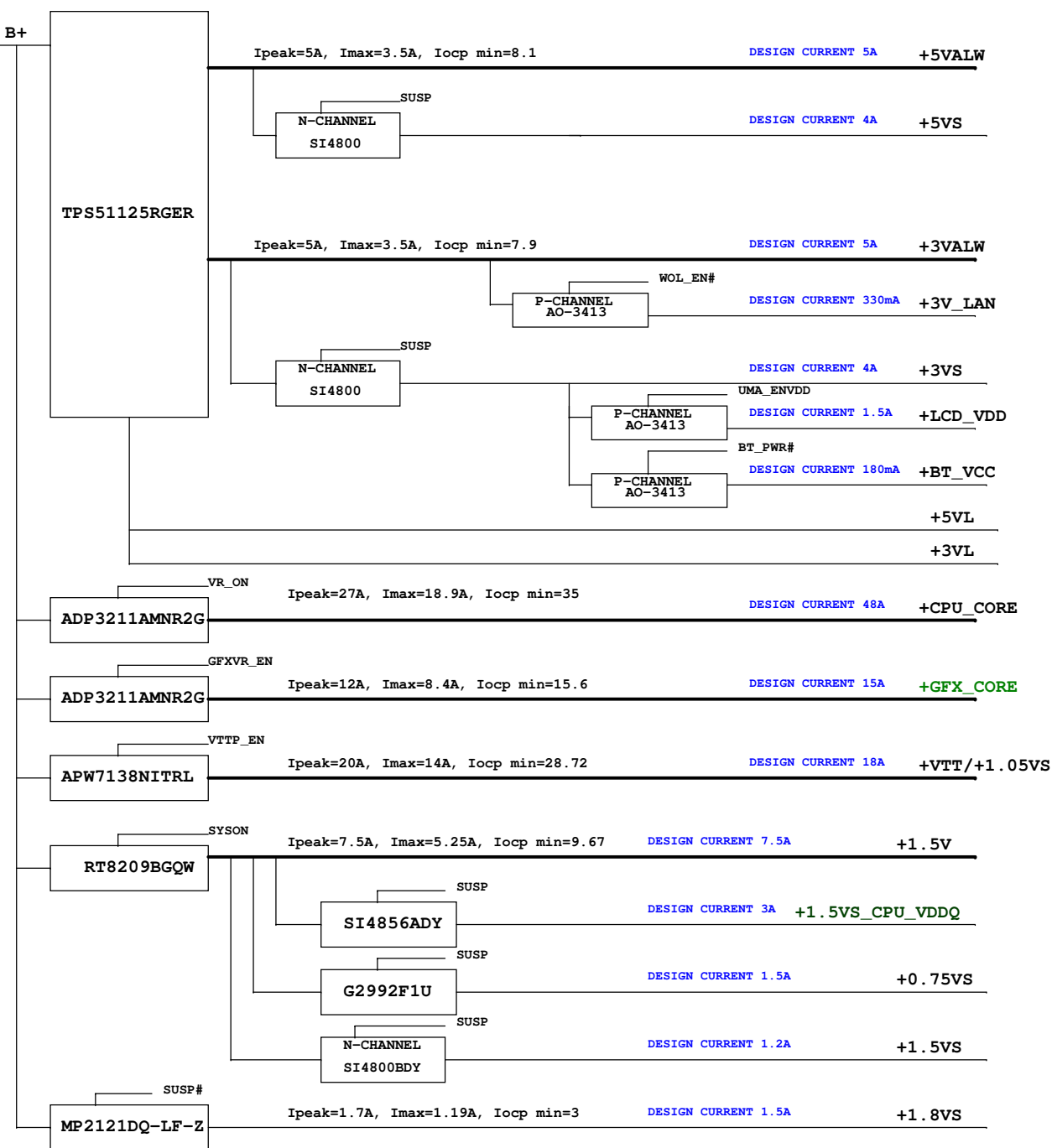
Model Name :NDU00/NDU10

File Name : LA-6031P



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NSWAA Liverpool Intel Arrandale
NTWAA Sunderland Intel Arrandale



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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +GFX_CORE +CPU_CORE +VTT +0.75VS +1.8VS +1.5VS_CPU_VDDQ
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	HDMI	3G	Mini Card	Mini Card	Gensor	
explain	Bluetooth	HDMI	3G	WIRELESS	WIMAX	main	2nd
						R5F211B4D31SP	R5F211B4D34SP
BTO	BT@	IHDMI@	3G@	WLAN@	WIMAX@	GSENSOR@ 1STGSENSOR@ 1ST@	GSENSOR@ 2NDGSENSOR@ 2ND@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

EC SM Bus1 address

EC SM Bus2 address

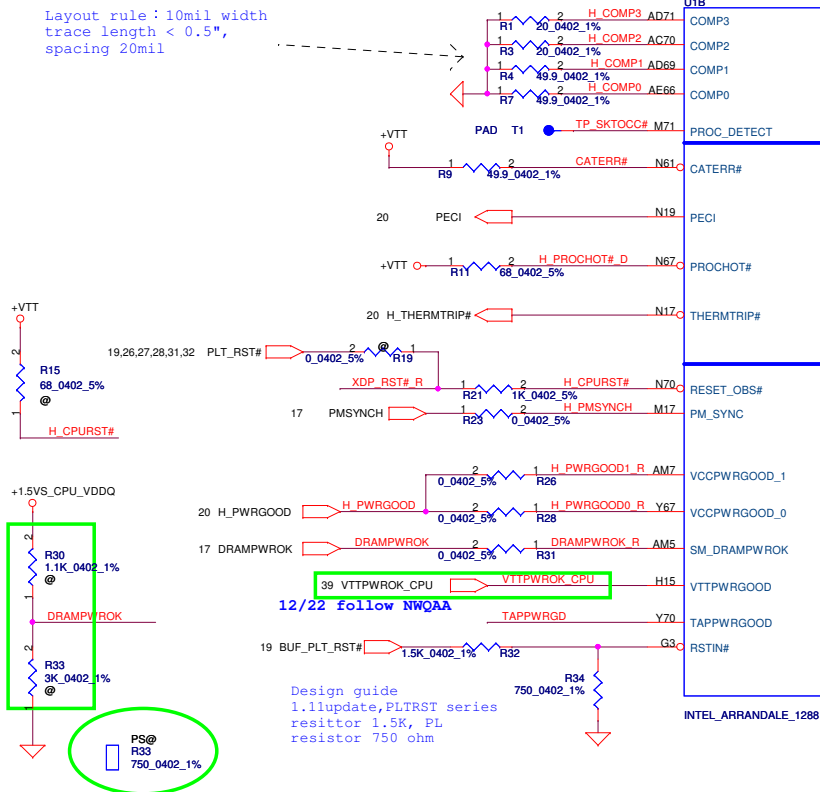
Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 011x b	+3VS	Gensor	
			+3VS	PCH	0100 110x b

PCH SM Bus address

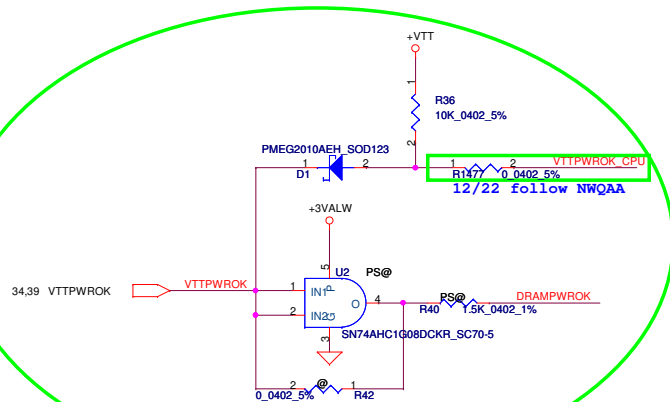
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	WLAN/Wimax/3G	

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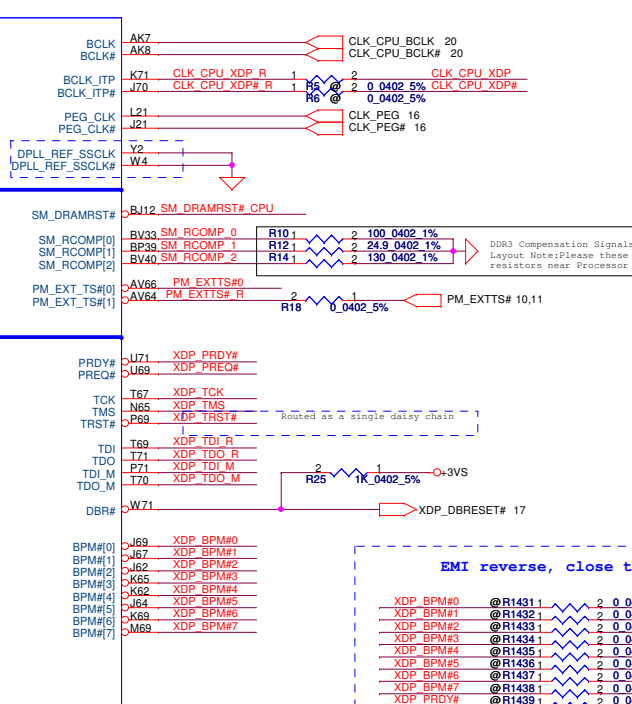
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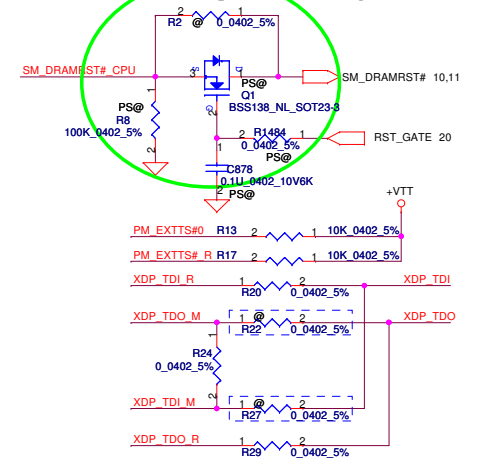
For S3 CPU power saving



Clocks
Thermal
Power Management
JTAG & MBP



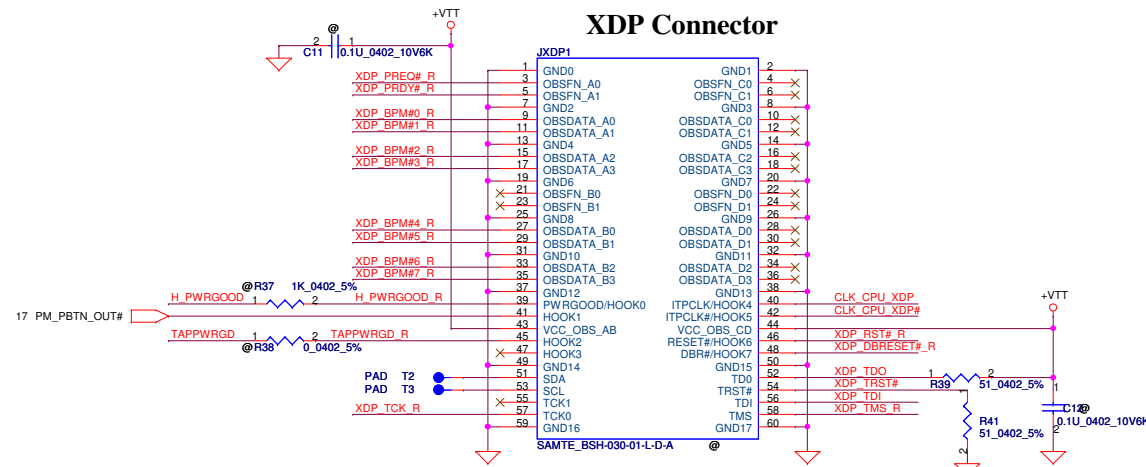
For S3 CPU power saving



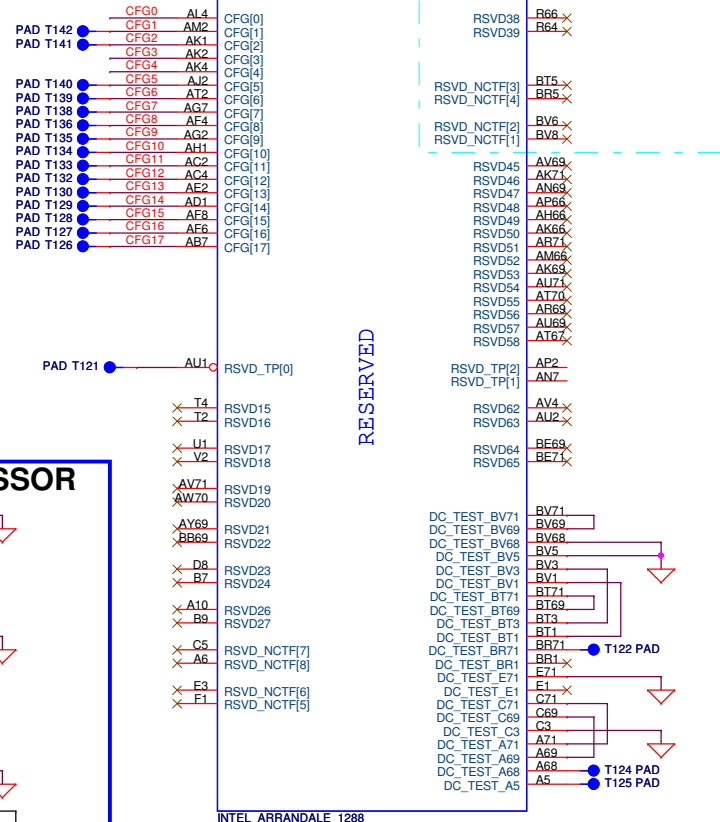
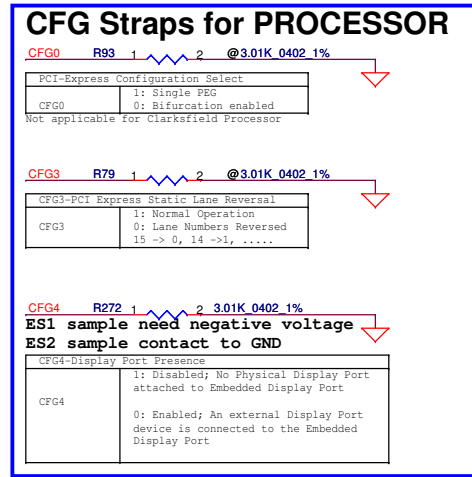
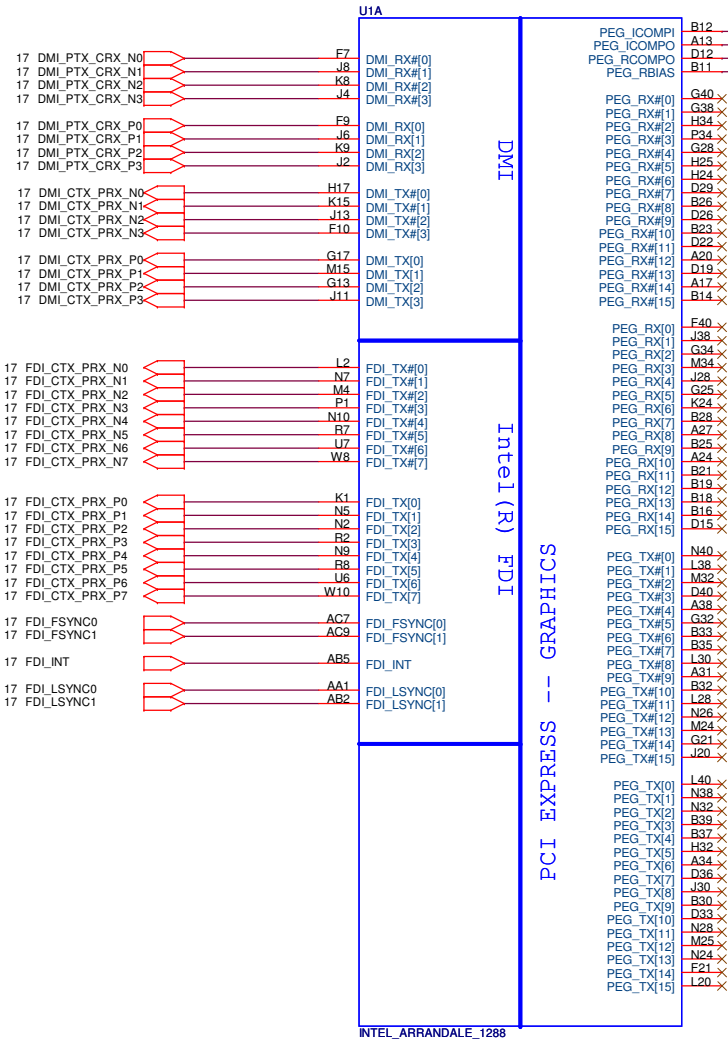
JTAG MAPPING

Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

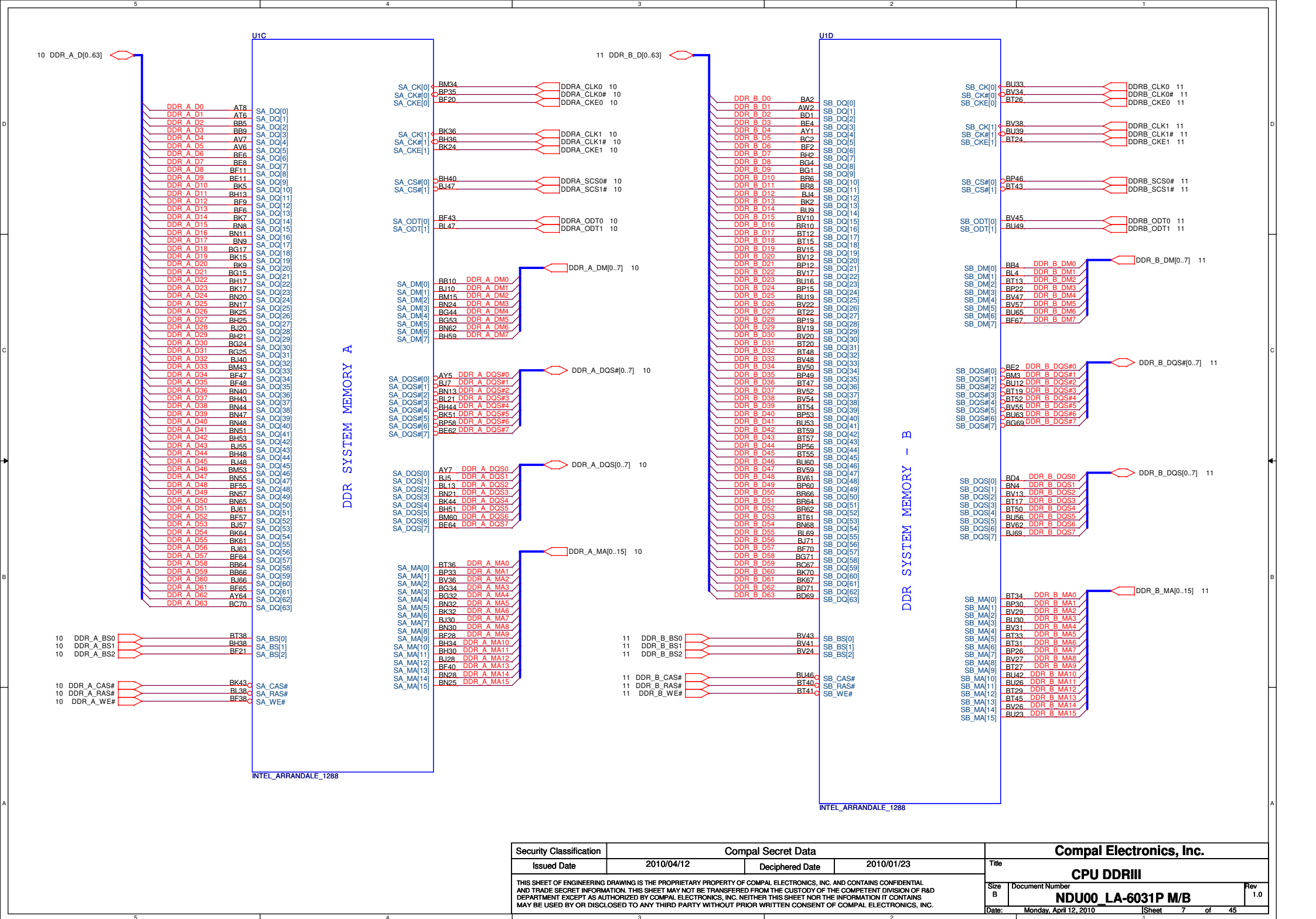
XDP Connector

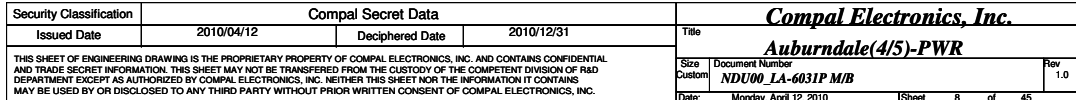


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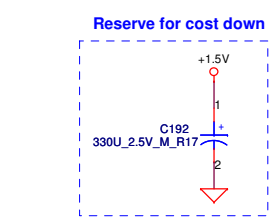
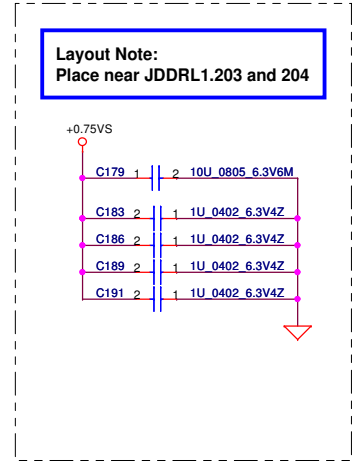
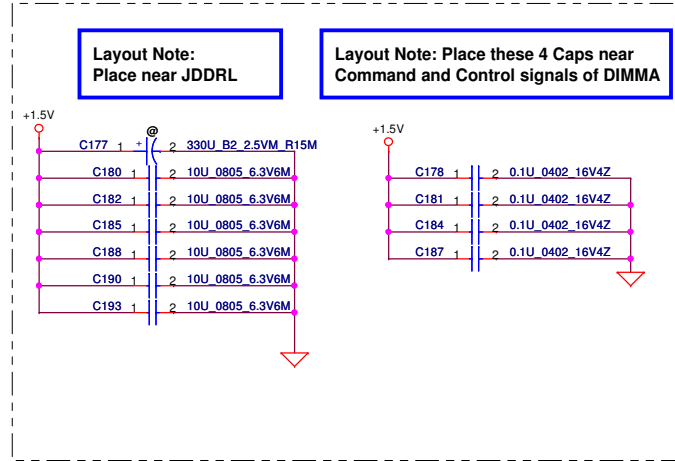
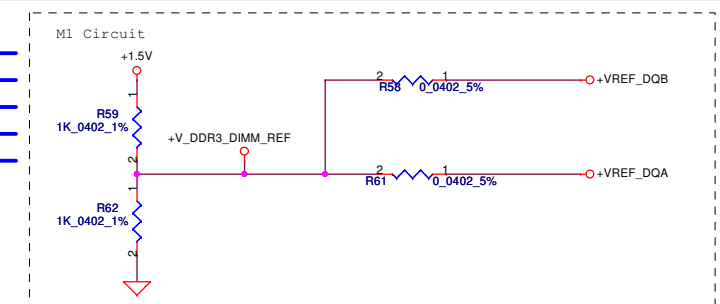
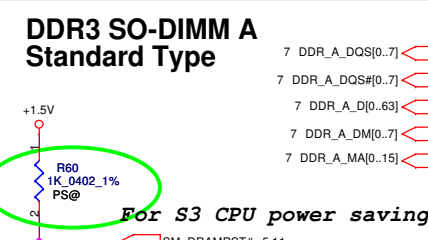
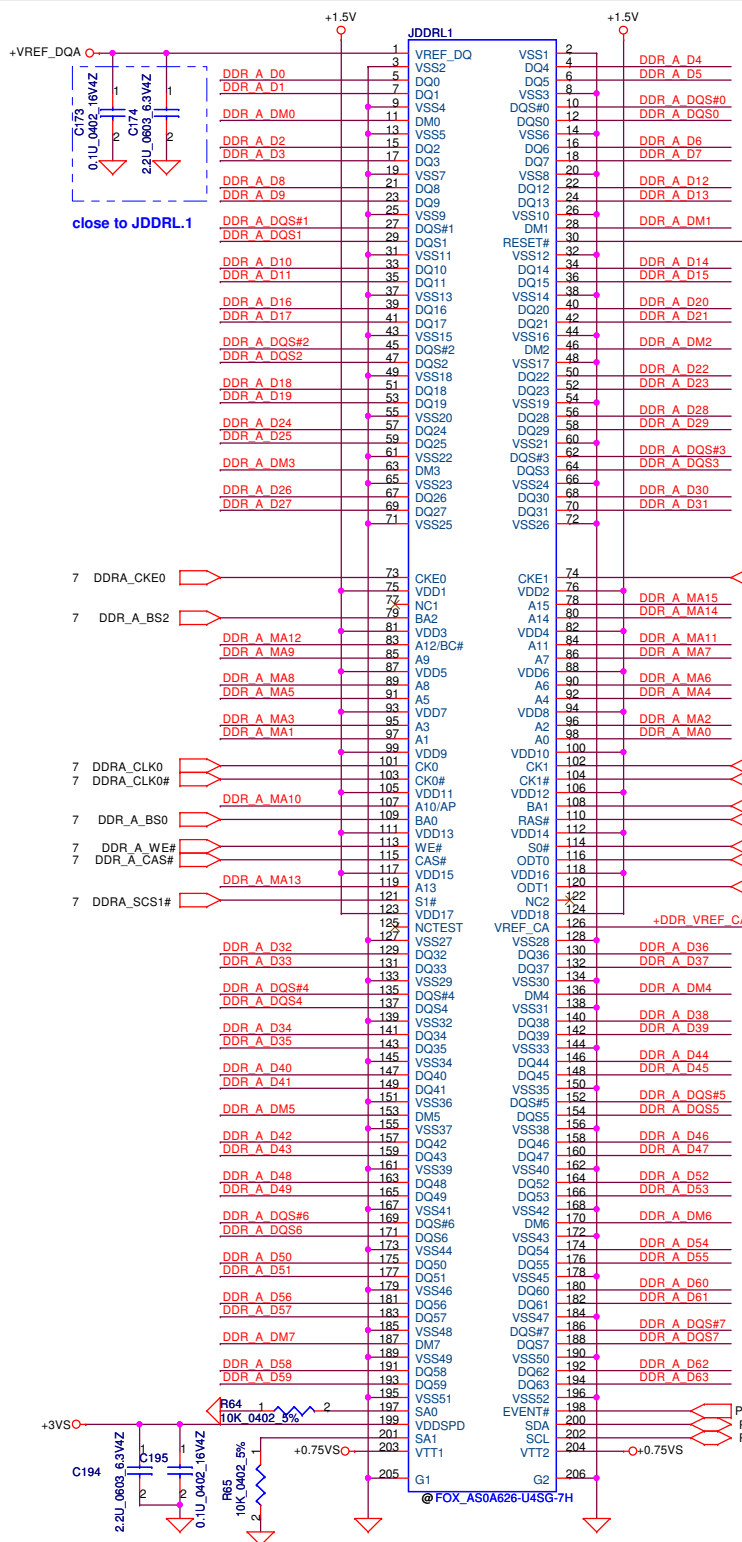


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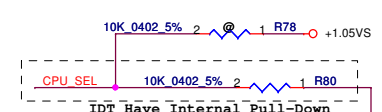
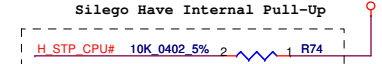
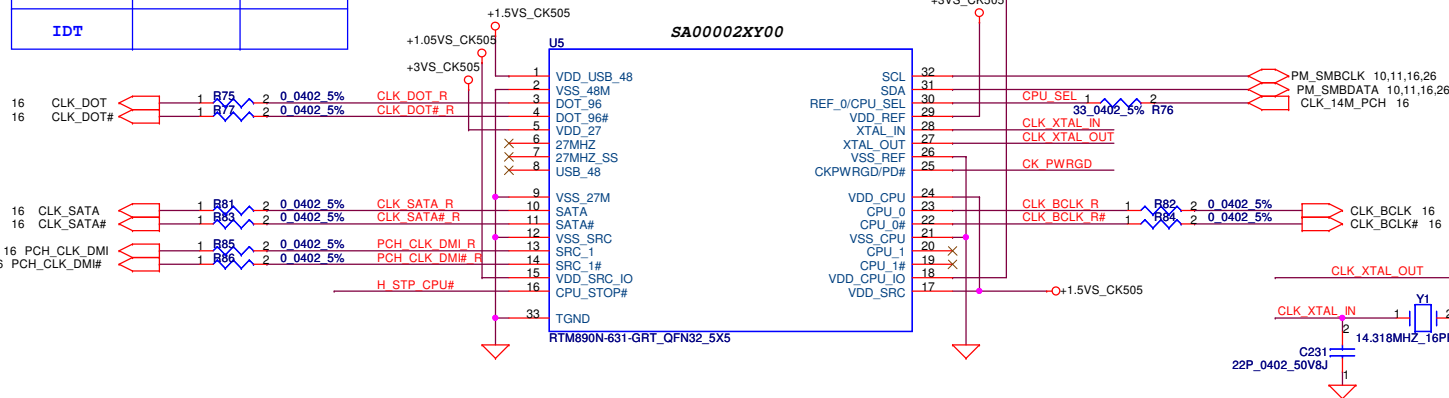
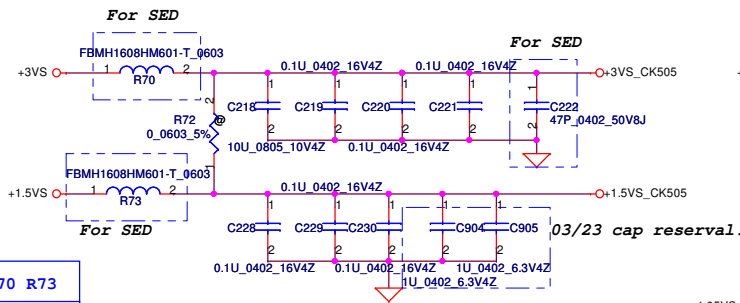
U11		AY24		U1J		
BU62	VSS1	VSS90		AH33	VSS202	VSS404
BU68	VSS2	VSS91	AY23	AH31	VSS203	VSS405
BU69	VSS3	VSS92	AY21	AH32	VSS204	VSS406
BU70	VSS4	VSS93		AH33	VSS205	VSS407
BU71	VSS5	VSS94		AH34	VSS206	VSS408
BU72	VSS6	VSS95		AH35	VSS207	VSS409
BU73	VSS7	VSS96		AH36	VSS208	VSS410
BU74	VSS8	VSS97		AH37	VSS209	VSS411
BU75	VSS9	VSS98		AH38	VSS210	VSS412
BU76	VSS10	VSS99		AH39	VSS211	VSS413
BU77	VSS11	VSS100	AW57	AH40	VSS212	VSS414
BU78	VSS12	VSS101	AW58	AH41	VSS213	VSS415
BU79	VSS13	VSS102	AW59	AH42	VSS214	VSS416
BU80	VSS14	VSS103	AW60	AH43	VSS215	VSS417
BU81	VSS15	VSS104	AW61	AH44	VSS216	VSS418
BU82	VSS16	VSS105	AW62	AH45	VSS217	VSS419
BU83	VSS17	VSS106	AW63	AH46	VSS218	VSS420
BU84	VSS18	VSS107	AW64	AH47	VSS219	VSS421
BU85	VSS19	VSS108	AW65	AH48	VSS220	VSS422
BU86	VSS20	VSS109	AW66	AH49	VSS221	VSS423
BU87	VSS21	VSS110	AW67	AH50	VSS222	VSS424
BU88	VSS22	VSS111	AW68	AH51	VSS223	VSS425
BU89	VSS23	VSS112	AW69	AH52	VSS224	VSS426
BU90	VSS24	VSS113	AW70	AH53	VSS225	VSS427
BU91	VSS25	VSS114	AW71	AH54	VSS226	VSS428
BU92	VSS26	VSS115	AW72	AH55	VSS227	VSS429
BU93	VSS27	VSS116	AW73	AH56	VSS228	VSS430
BU94	VSS28	VSS117	AW74	AH57	VSS229	VSS431
BU95	VSS29	VSS118	AW75	AH58	VSS230	VSS432
BU96	VSS30	VSS119	AW76	AH59	VSS231	VSS433
BU97	VSS31	VSS120	AW77	AH60	VSS232	VSS434
BU98	VSS32	VSS121	AW78	AH61	VSS233	VSS435
BU99	VSS33	VSS122	AW79	AH62	VSS234	VSS436
BU00	VSS34	VSS123	AW80	AH63	VSS235	VSS437
BU01	VSS35	VSS124	AW81	AH64	VSS236	VSS438
BU02	VSS36	VSS125	AW82	AH65	VSS237	VSS439
BU03	VSS37	VSS126	AW83	AH66	VSS238	VSS440
BU04	VSS38	VSS127	AW84	AH67	VSS239	VSS441
BU05	VSS39	VSS128	AW85	AH68	VSS240	VSS442
BU06	VSS40	VSS129	AW86	AH69	VSS241	VSS443
BU07	VSS41	VSS130	AW87	AH70	VSS242	VSS444
BU08	VSS42	VSS131	AW88	AH71	VSS243	VSS445
BU09	VSS43	VSS132	AW89	AH72	VSS244	VSS446
BU10	VSS44	VSS133	AW90	AH73	VSS245	VSS447
BU11	VSS45	VSS134	AW91	AH74	VSS246	VSS448
BU12	VSS46	VSS135	AW92	AH75	VSS247	VSS449
BU13	VSS47	VSS136	AW93	AH76	VSS248	VSS450
BU14	VSS48	VSS137	AW94	AH77	VSS249	VSS451
BU15	VSS49	VSS138	AW95	AH78	VSS250	VSS452
BU16	VSS50	VSS139	AW96	AH79	VSS251	VSS453
BU17	VSS51	VSS140	AW97	AH80	VSS252	VSS454
BU18	VSS52	VSS141	AW98	AH81	VSS253	VSS455
BU19	VSS53	VSS142	AW99	AH82	VSS254	VSS456
BU20	VSS54	VSS143	AW00	AH83	VSS255	VSS457
BU21	VSS55	VSS144		AH84	VSS256	VSS458
BU22	VSS56	VSS145		AH85	VSS257	VSS459
BU23	VSS57	VSS146		AH86	VSS258	VSS460
BU24	VSS58	VSS147		AH87	VSS259	VSS461
BU25	VSS59	VSS148		AH88	VSS260	VSS462
BU26	VSS60	VSS149		AH89	VSS261	VSS463
BU27	VSS61	VSS150		AH90	VSS262	VSS464
BU28	VSS62	VSS151		AH91	VSS263	VSS465
BU29	VSS63	VSS152		AH92	VSS264	VSS466
BU30	VSS64	VSS153		AH93	VSS265	VSS467
BU31	VSS65	VSS154		AH94	VSS266	VSS468
BU32	VSS66	VSS155		AH95	VSS267	VSS469
BU33	VSS67	VSS156		AH96	VSS268	VSS470
BU34	VSS68	VSS157		AH97	VSS269	VSS471
BU35	VSS69	VSS158		AH98	VSS270	VSS472
BU36	VSS70	VSS159		AH99	VSS271	VSS473
BU37	VSS71	VSS160		AH00	VSS272	VSS474
BU38	VSS72	VSS161			VSS273	VSS475
BU39	VSS73	VSS162			VSS274	VSS476
BU40	VSS74	VSS163			VSS275	VSS477
BU41	VSS75	VSS164			VSS276	VSS478
BU42	VSS76	VSS165			VSS277	VSS479
BU43	VSS77	VSS166			VSS278	VSS480
BU44	VSS78	VSS167			VSS279	VSS481
BU45	VSS79	VSS168			VSS280	VSS482
BU46	VSS80	VSS169			VSS281	VSS483
BU47	VSS81	VSS170			VSS282	VSS484
BU48	VSS82	VSS171			VSS283	VSS485
BU49	VSS83	VSS172			VSS284	VSS486
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BU51	VSS85	VSS174			VSS286	VSS488
BU52	VSS86	VSS175			VSS287	VSS489
BU53	VSS87	VSS176			VSS288	VSS490
BU54	VSS88	VSS177			VSS289	VSS491
BU55	VSS89	VSS178			VSS290	VSS492
BU56	VSS90	VSS179			VSS291	VSS493
BU57	VSS91	VSS180			VSS292	VSS494
BU58	VSS92	VSS181			VSS293	VSS495
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BU60	VSS94	VSS183			VSS295	VSS497
BU61	VSS95	VSS184			VSS296	VSS498
BU62	VSS96	VSS185			VSS297	VSS499
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BU66	VSS100	VSS189			VSS301	VSS503
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BU74	VSS108	VSS197			VSS309	VSS511
BU75	VSS109	VSS198			VSS310	VSS512
BU76	VSS110	VSS199			VSS311	VSS513
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BU79	VSS113	VSS202			VSS314	VSS516
BU80	VSS114	VSS203			VSS315	VSS517
BU81	VSS115	VSS204			VSS316	VSS518
BU82	VSS116	VSS205			VSS317	VSS519
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BU84	VSS118	VSS207			VSS319	VSS521
BU85	VSS119	VSS208			VSS320	VSS522
BU86	VSS120	VSS209			VSS321	VSS523
BU87	VSS121	VSS210			VSS322	VSS524
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BU89	VSS123	VSS212			VSS324	VSS526
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BU92	VSS126	VSS215			VSS327	VSS529
BU93	VSS127	VSS216			VSS328	VSS530
BU94	VSS128	VSS217			VSS329	VSS531
BU95	VSS129	VSS218			VSS330	VSS532
BU96	VSS130	VSS219			VSS331	VSS533
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BU98	VSS132	VSS221			VSS333	VSS535
BU99	VSS133	VSS222			VSS334	VSS536
BU00	VSS134	VSS223			VSS335	VSS537
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BU02	VSS136	VSS225			VSS337	VSS539
BU03	VSS137	VSS226			VSS338	VSS540
BU04	VSS138	VSS227			VSS339	VSS541
BU05	VSS139	VSS228			VSS340	VSS542
BU06	VSS140	VSS229			VSS341	VSS543
BU07	VSS141	VSS230			VSS342	VSS544
BU08	VSS142	VSS231			VSS343	VSS545
BU09	VSS143	VSS232			VSS344	VSS546
BU10	VSS144	VSS233			VSS345	VSS547
BU11	VSS145	VSS234			VSS346	VSS548
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BU13	VSS147	VSS236			VSS348	VSS550
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BU15	VSS149	VSS238			VSS350	VSS552
BU16	VSS150	VSS239			VSS351	VSS553
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BU39	VSS173	VSS262			VSS374	VSS576
BU40	VSS174	VSS263			VSS375	VSS577
BU41	VSS175	VSS264			VSS376	VSS578
BU42	VSS176	VSS265			VSS377	VSS579
BU43	VSS177	VSS266			VSS378	VSS580
BU44	VSS178	VSS267			VSS379	VSS581
BU45	VSS179	VSS268			VSS380	VSS582
BU46	VSS180	VSS269			VSS381	VSS583
BU47	VSS181	VSS270			VSS382	VSS584
BU48	VSS182	VSS271			VSS383	VSS585
BU49	VSS183	VSS272			VSS384	VSS586
BU50	VSS184	VSS273			VSS385	VSS587
BU51	VSS185	VSS274			VSS386	VSS588
BU52	VSS186	VSS275			VSS387	VSS589
BU53	VSS187	VSS276			VSS388	VSS590
BU54	VSS188	VSS277			VSS389	VSS591
BU55	VSS189	VSS278			VSS390	VSS592
BU56	VSS190	VSS279			VSS391	VSS593
BU57	VSS191	VSS280			VSS392	VSS594
BU58	VSS192	VSS281			VSS393	VSS595
BU59	VSS193	VSS282			VSS394	VSS596
BU60	VSS194	VSS283			VSS395	VSS597
BU61	VSS195	VSS284			VSS396	VSS598
BU62	VSS196	VSS285			VSS397	VSS599
BU63	VSS197	VSS286			VSS398	VSS600
BU64	VSS198	VSS287			VSS399	VSS601
BU65	VSS199	VSS288			VSS400	VSS602
BU66	VSS200	VSS289				
BU67	VSS201	VSS290				
BU68	VSS202	VSS291				
BU69	VSS203	VSS292				
BU70	VSS204	VSS293				
BU71	VSS205	VSS294				
BU72	VSS206	VSS295				
BU73	VSS207	VSS296				
BU74	VSS208	VSS297				
BU75	VSS209	VSS298				
BU76	VSS210	VSS299				
BU77	VSS211	VSS300				
BU78	VSS212	VSS301				
BU7						



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				Custom				NDU00_LA-6031P M/B			
				Date				Monday, April 12, 2010			
				Sheet				10 of 45			

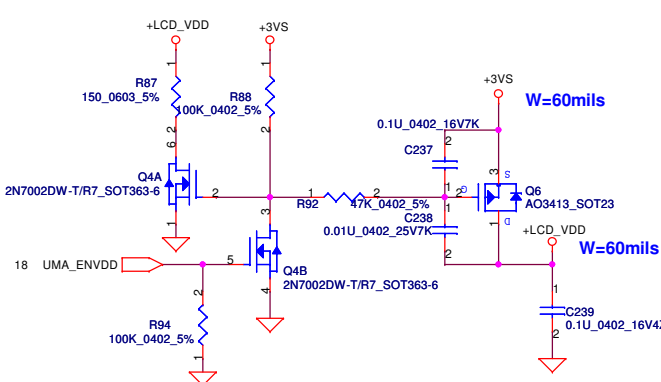
Clock Generator

Clock gen	R72	R70 R73
RTM	no-mount	mount
IDT		

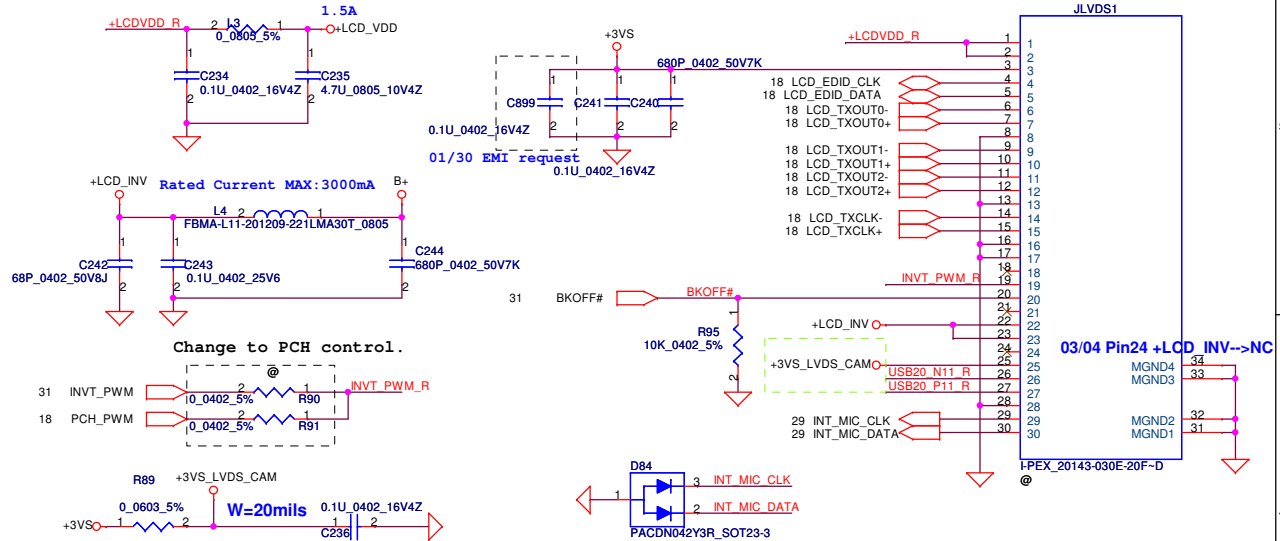
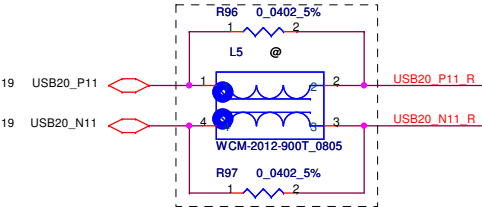


CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

LCD/PANEL BD. Conn.



Reserve for EMI request



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Size	Document Number	Rev		Date	
Custom	NDU00_LA-6031P M/B	Monday, April 12, 2010		Sheet 12 of 45	

CRT CONNECTOR

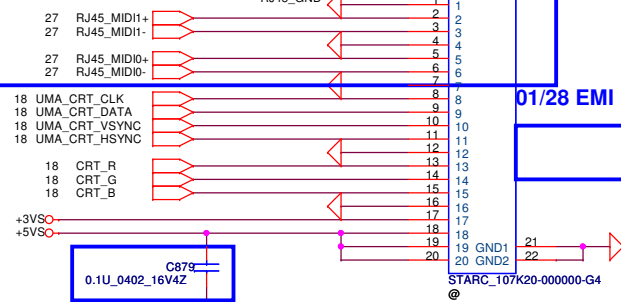
12/14 Fine tune pin define JP1 Pin1 Pin2 Pin8-->GND

12/21 pin 2,3 to RJ45_GND

12/22 Fine tune JP4 pin define

02/08 update connector footprint.

12/21 transformer on board.

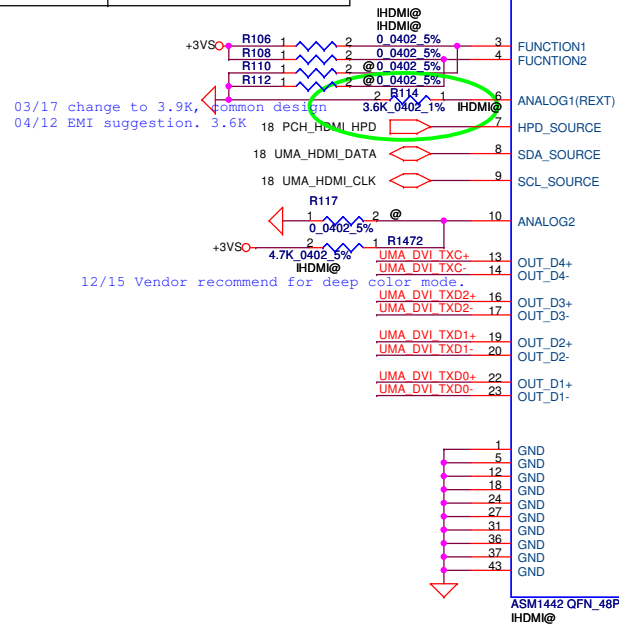
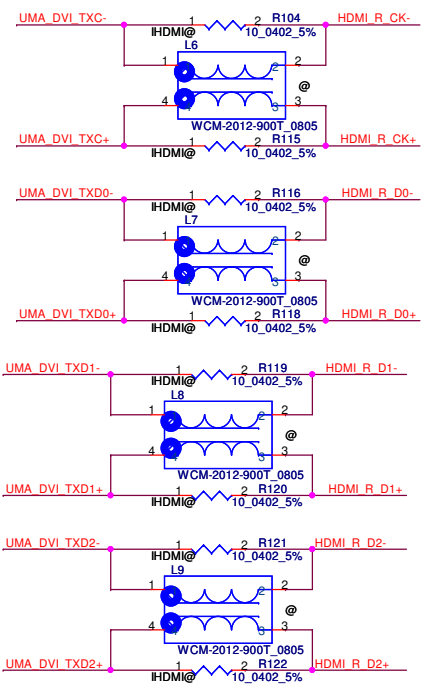
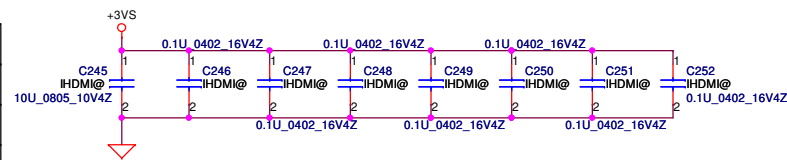


01/28 EMI request. Change pin definition.

12/17 EMI request.

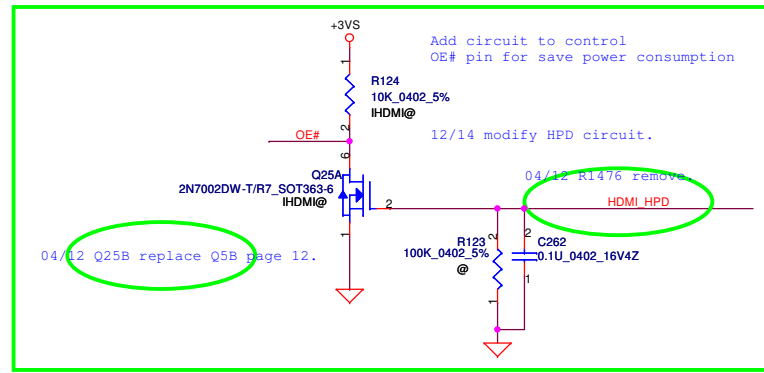
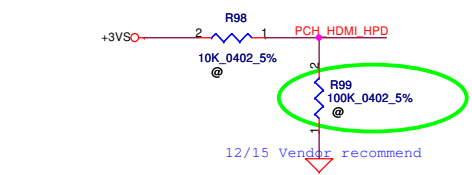
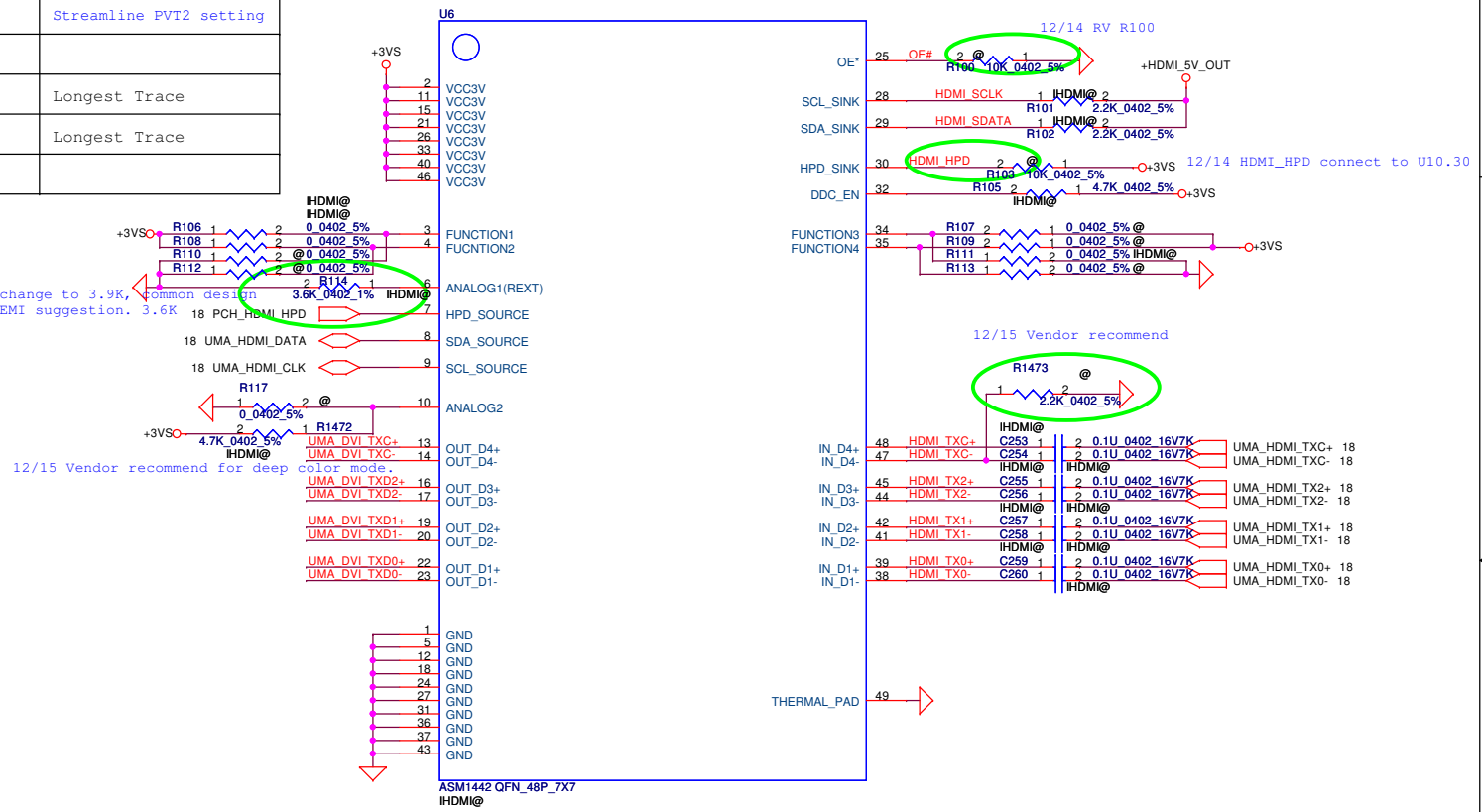
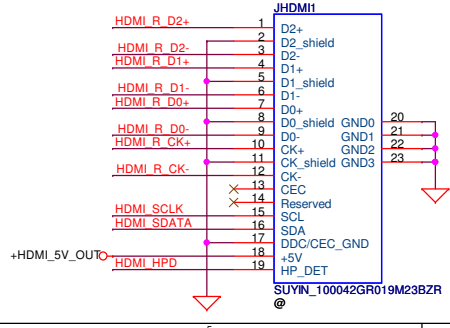
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Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title	
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Size		Document Number			Rev
Date:		Monday, April 12, 2010			1.0
Sheet		13		of 45	

ANALOG2	Function2	Function1	Swing	Pre-Amp	Slew-rate	Note
Low	Low	Low	450	0	0	
Low	Low	High	420	0	-3dB	Shortest trace
Low	High	Low	450	0	-3dB	Shortest trace
Low	High	High	460	0	-4dB	Streamline PVT2 setting
High	Low	Low	340	0	0	Longest Trace
High	High	Low	400	2dB	0	Longest Trace
High	High	High	420	0	0	

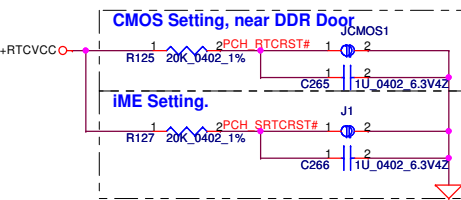


HDMI Connector

<01/27 update HDMI Connector >



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								Size		Document Number				Rev	
										NDU00 LA-6031P M/B				1.0	
						Date: Monday, April 12, 2010		Sheet 14 of 45							



Integrated SUS 1.05V VRM Enable

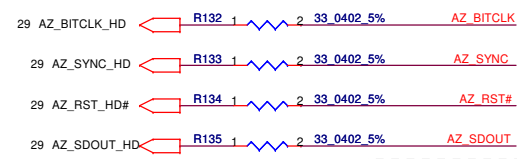
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

HDA_SYNC
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V

HDA_SDO
This signal has a weak internal pull down.
This signal can't PU

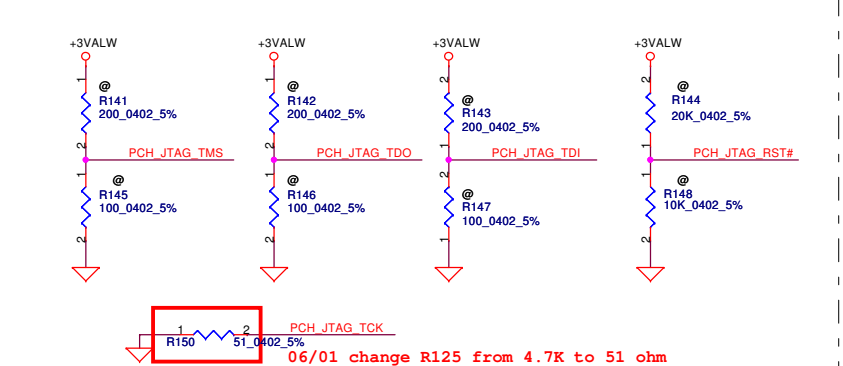
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------

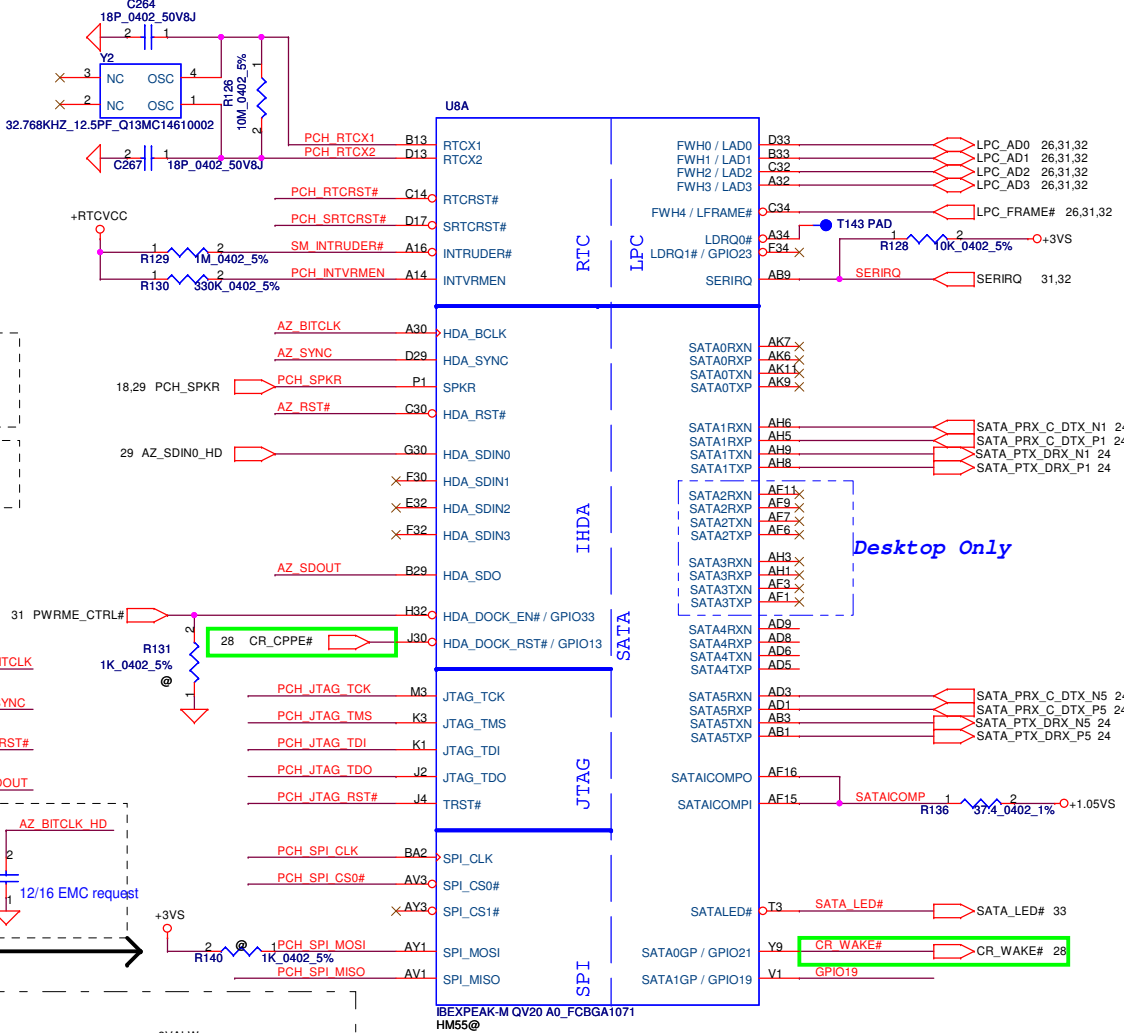


ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--

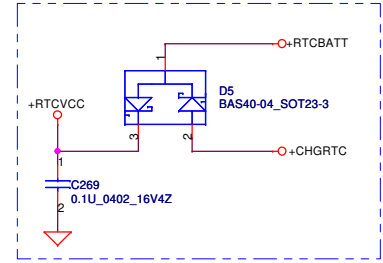


PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TCK	R356	200ohm	200ohm	20kohm	No Install
PCH_JTAG_RST#	R517	100ohm	100ohm	10kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
PCH_JTAG_RST#	R353	10kohm	10kohm	No Install	No Install

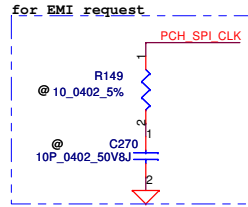
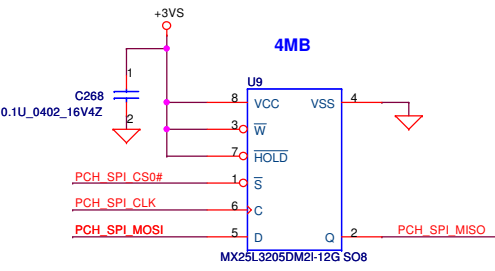


1ST HDD

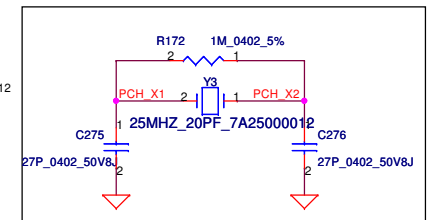
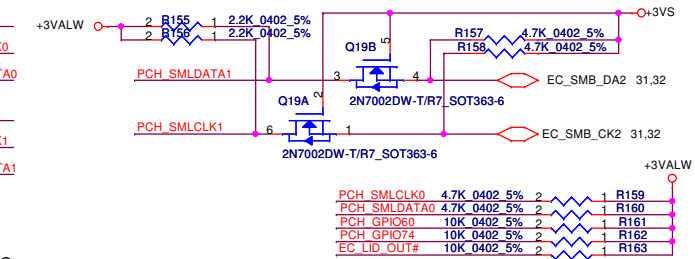
eSATA



2/8 change back to original.(Lion Wang)
del D86 and R1494.
2/1 Add R1494 D86 (EMI)

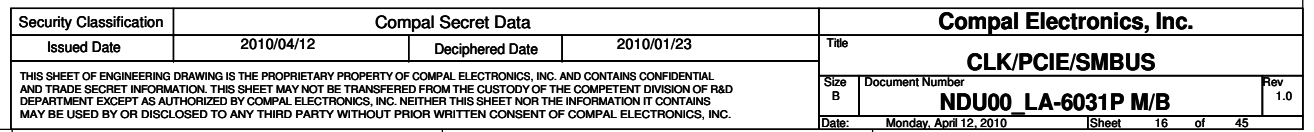


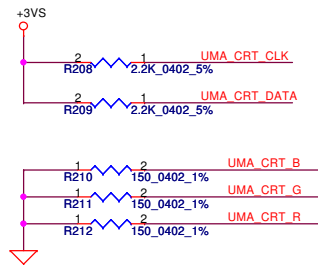
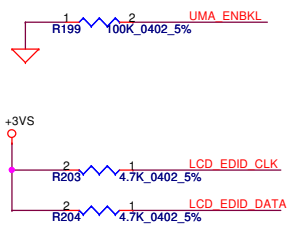
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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								PCH-SPI/SATA/LPC/RTC/HDA			
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								B	NDU00_LA-6031P M/B	1.0	
								Date:	Monday, April 12, 2010	Sheet	15 of 45



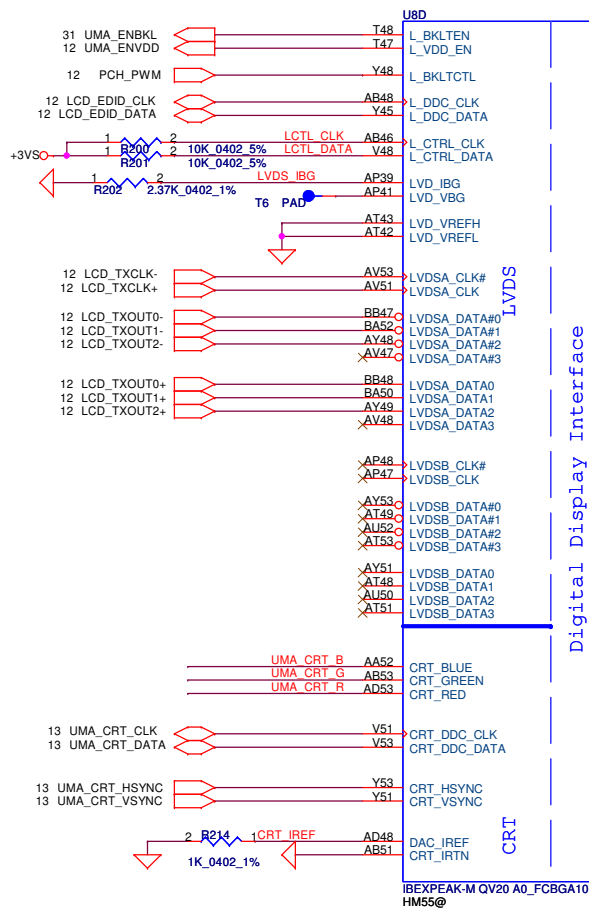
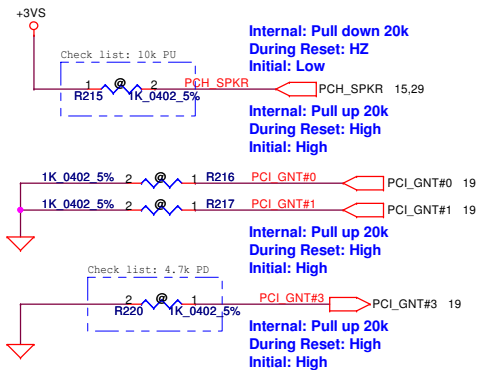
 C277 @
0_0402_5%

Note: Stuff 0 ohm if
25MHz crystal un-stuff

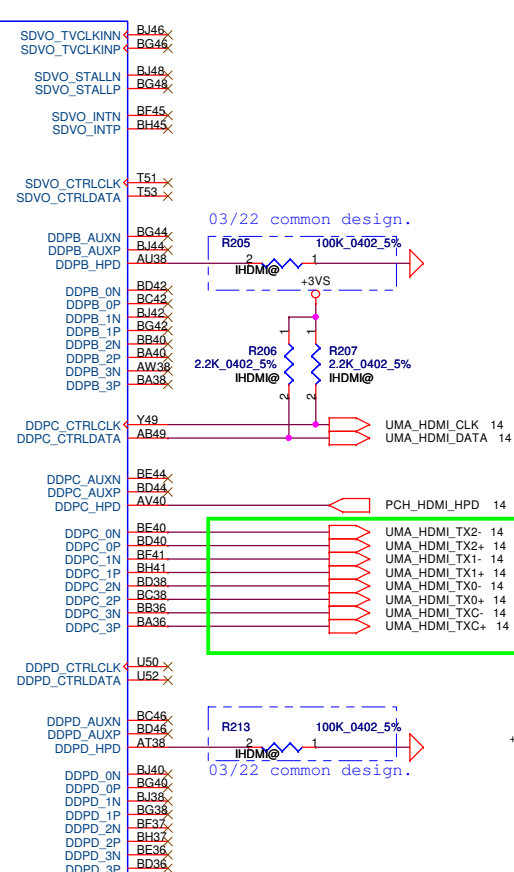




PCH Strap Pin



Digital Display Interface

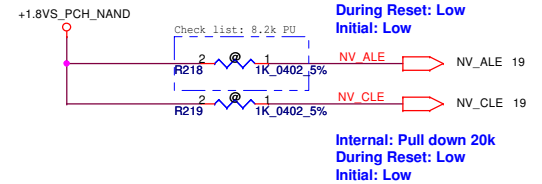


HDMI

Danbury Technology Enabled

NV_ALE	High = Enabled Low = Disabled (Default)
--------	--

Internal: Pull down 20k
During Reset: Low
Initial: Low



DMI Termination Voltage

NV_CLE	Low= Set to Vss (Default) High= Set to Vcc
--------	---

NO REBOOT Strap

PCH_SPKR	Low= Disable High= Enable
----------	------------------------------

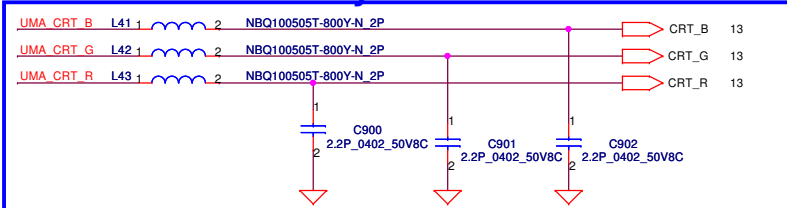
Boot BIOS Strap

PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

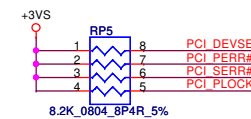
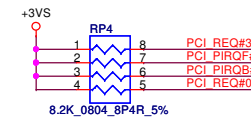
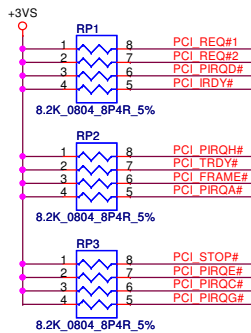
A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable
-----------	--

modify....



2/2 Add L41 L42 L43 C900 C901 C902 for EMI request



GNT2#: Not
pull low,
internal pull
up 20K

32 CLK_PCL_DDR
31 CLK_PCL_EC
16 CLK_PCL_LOOP

18 PCL_GNT#0
18 PCL_GNT#1
18 PCL_GNT#3

T37 PAD

5,26,27,28,31,32 PLT_RST#

PCI_PIRQA#
PCI_PIRQB#
PCI_PIRQC#
PCI_PIRQD#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3

PCI_PIRQE#
PCI_PIRQF#
PCI_PIRQG#
PCI_PIRQH#

PCI_IRDY#
PCI_DEVSEL#
PCI_FRAME#
PCI_PLOCK#

PCI_SERR#
PCI_PERR#
PCI_TRDY#

CLKOUT_PCL0
CLKOUT_PCL1
CLKOUT_PCL2
CLKOUT_PCL3
CLKOUT_PCL4

U8E
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
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AD15
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AD30
AD31

C/BE0#
C/BE1#
C/BE2#
C/BE3#

PIRQA#
PIRQB#
PIROC#
PIRQD#

REQ0# / GPIO50
REQ1# / GPIO52
REQ2# / GPIO53
REQ3# / GPIO54

GNT0# / GPIO51
GNT1# / GPIO52
GNT2# / GPIO53
GNT3# / GPIO55

PIRQE# / GPIO2
PIRQF# / GPIO3
PIRQG# / GPIO4
PIRQH# / GPIO5

PCIRST#
SERR#
PERR#

IRDY#
PAIR#
DEVSEL#
FRAME#

PLOCK#
STOP#
TRDY#

PME#
PLTRST#

CLKOUT_PCL0
CLKOUT_PCL1
CLKOUT_PCL2
CLKOUT_PCL3
CLKOUT_PCL4

IBEXPEAK-M QV20 A0_FCBGA1071
HM55@

PCI

NVRAM

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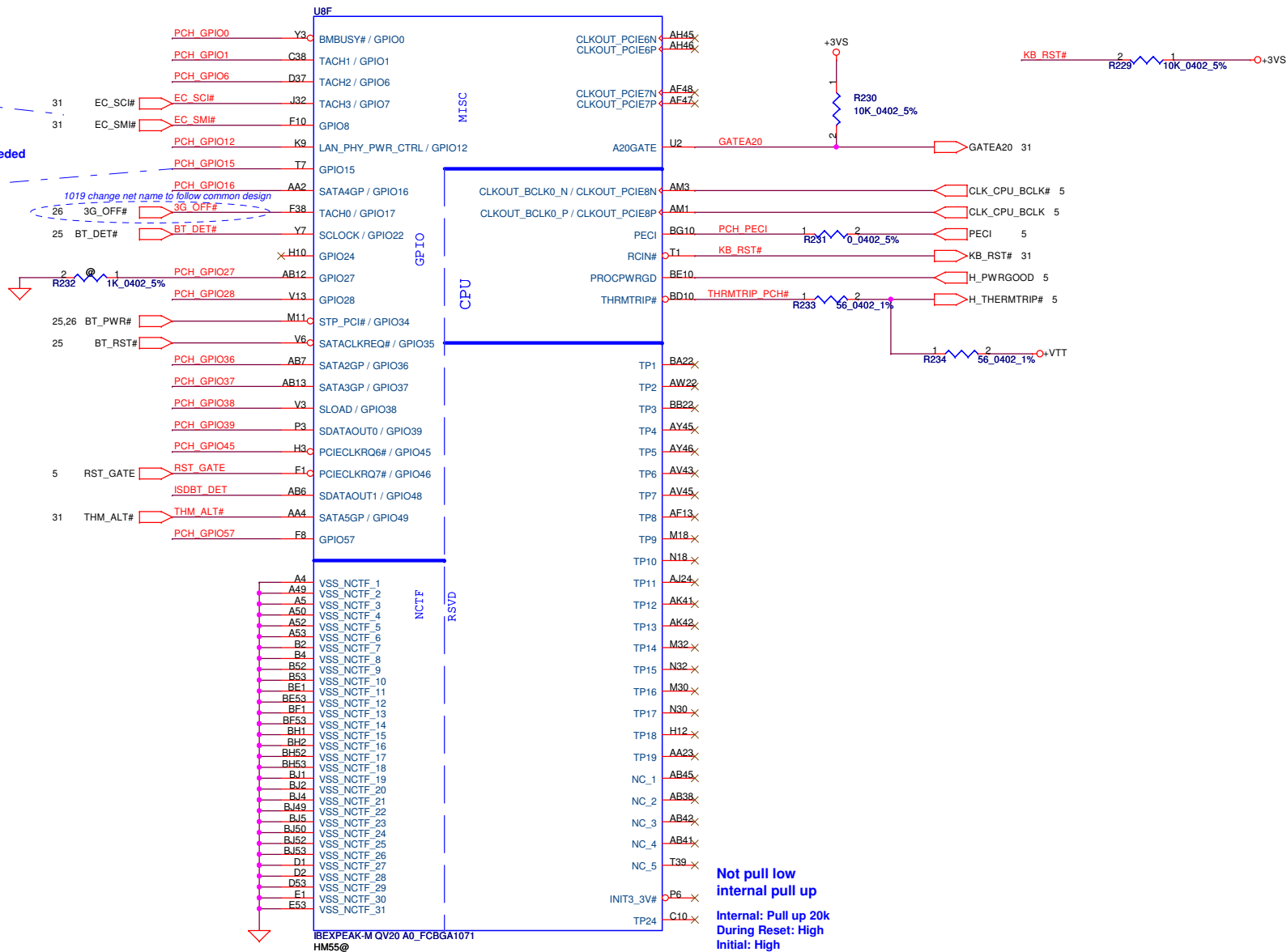
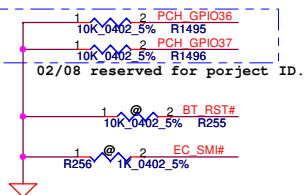
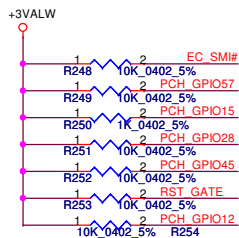
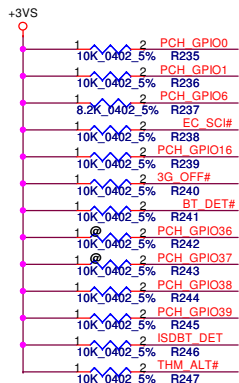
USB

GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

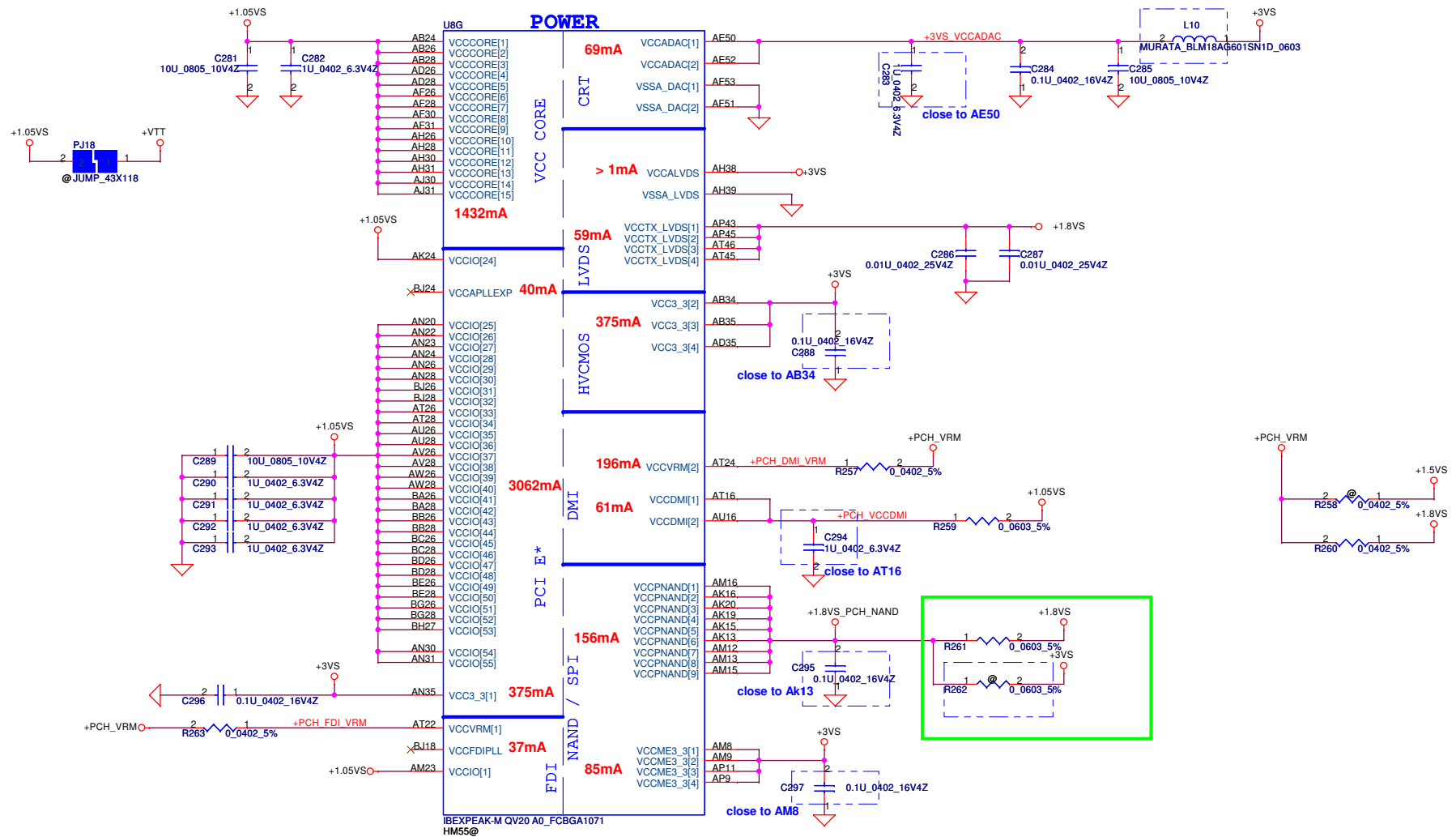
On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled

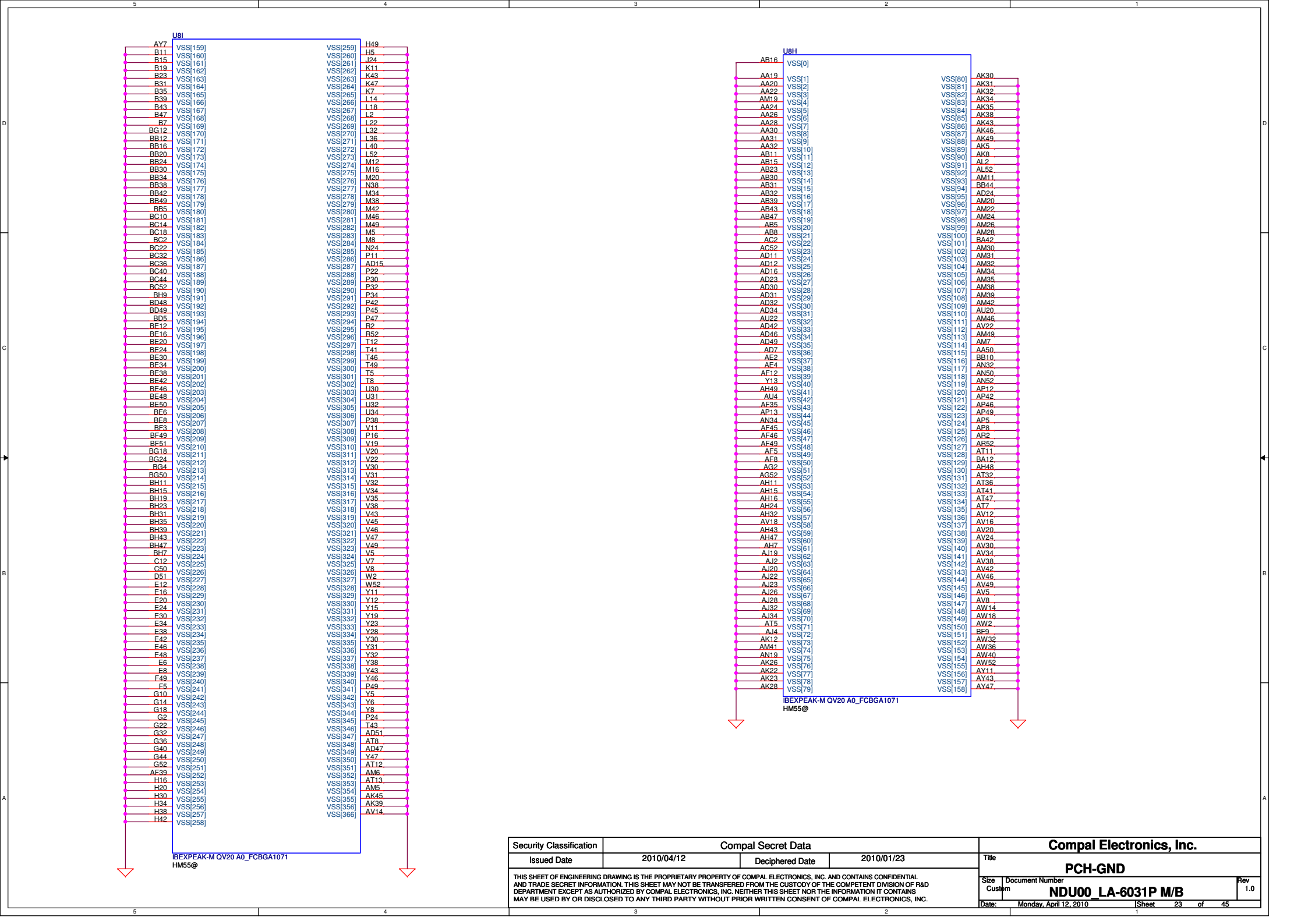


Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

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								Size	Document Number						Rev
									NDU00_LA-6031P M/B						1.0
								Date	Monday, April 12, 2010				Sheet	20 of 45	

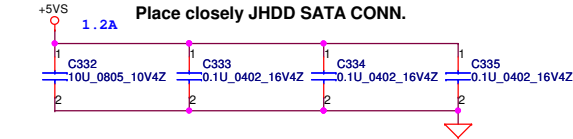


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				NDU00_LA-6031P M/B	
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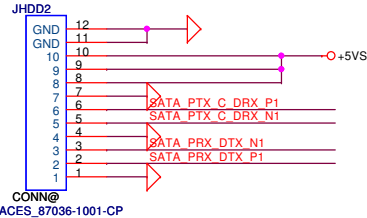
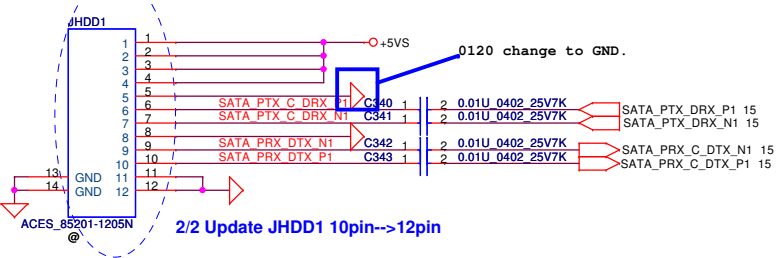
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Size	Document Number	Rev		1.0	
Custom	NDU00_LA-6031P M/B				
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SATA HDD Conn.



1/28 Add JHDD2

JHDD2 Layout symbol reverse JHDD1, reverse the pin define

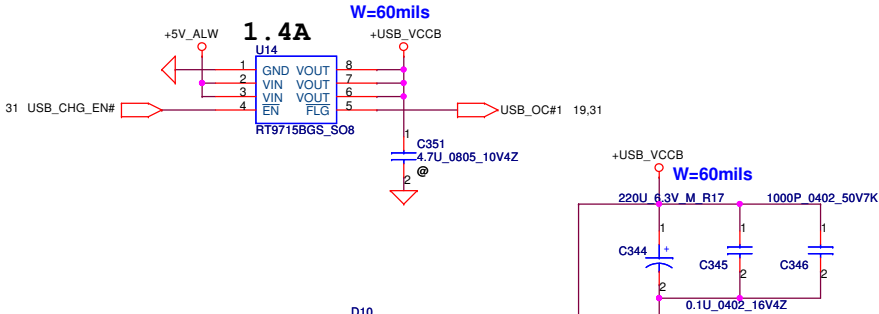
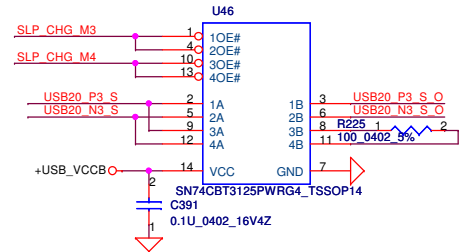
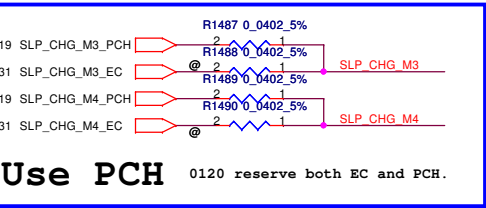
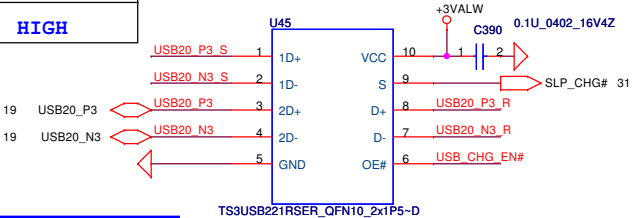


Add wire connector for H/W SATA verify

eSATA/USB Combo

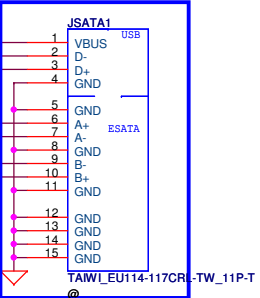
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



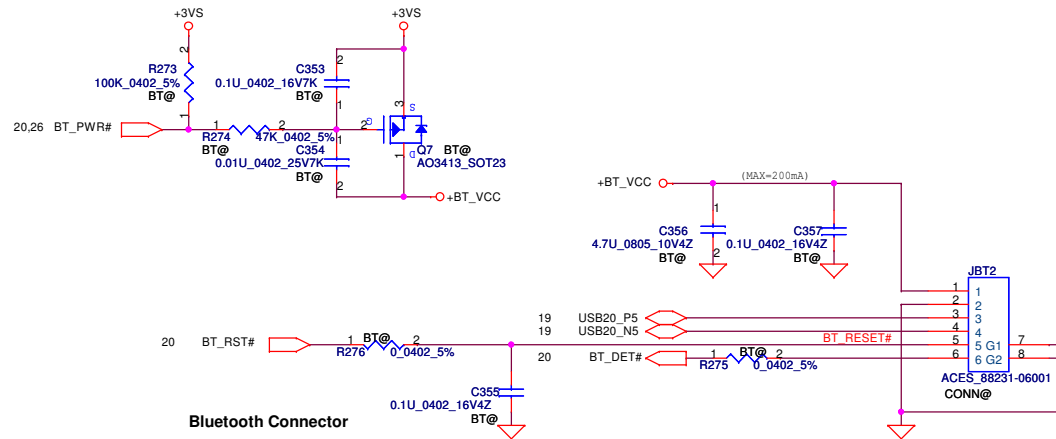
eSATA/USB Conn

1/26 update JSATA1 footprint

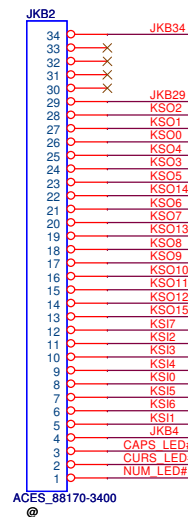


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				2010/01/23				Title			
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								Size			
								Document Number			
								NDU00_LA-6031P M/B			
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								24 of 45			

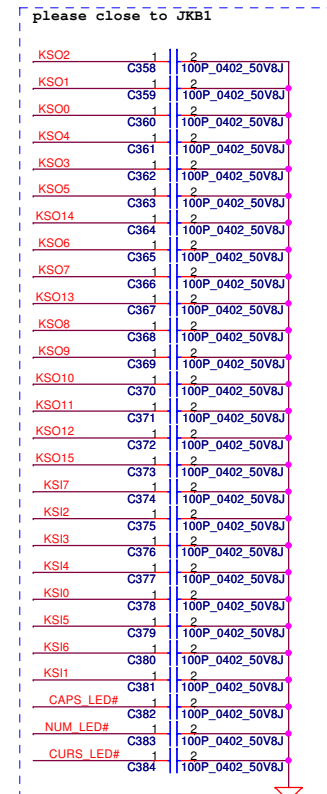
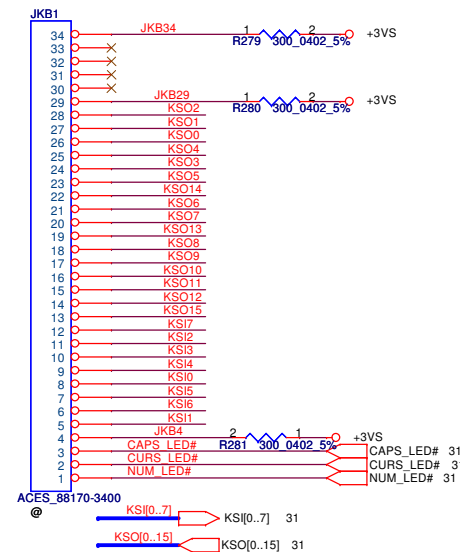
BlueTooth Interface



KEYBOARD CONN. for 11.6"

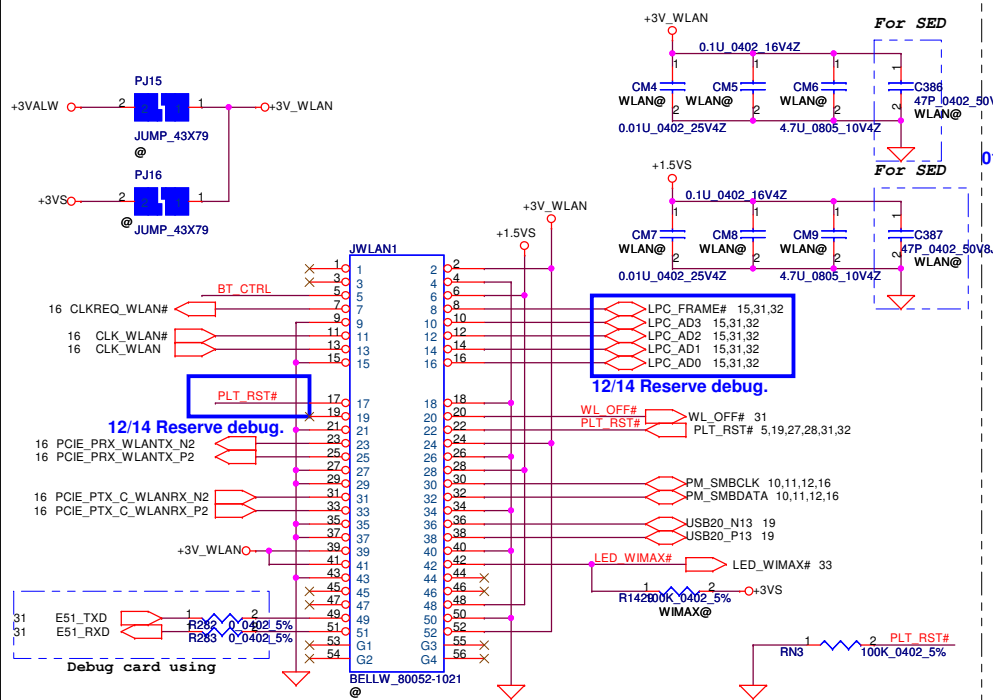


KEYBOARD CONN. for 13.3"

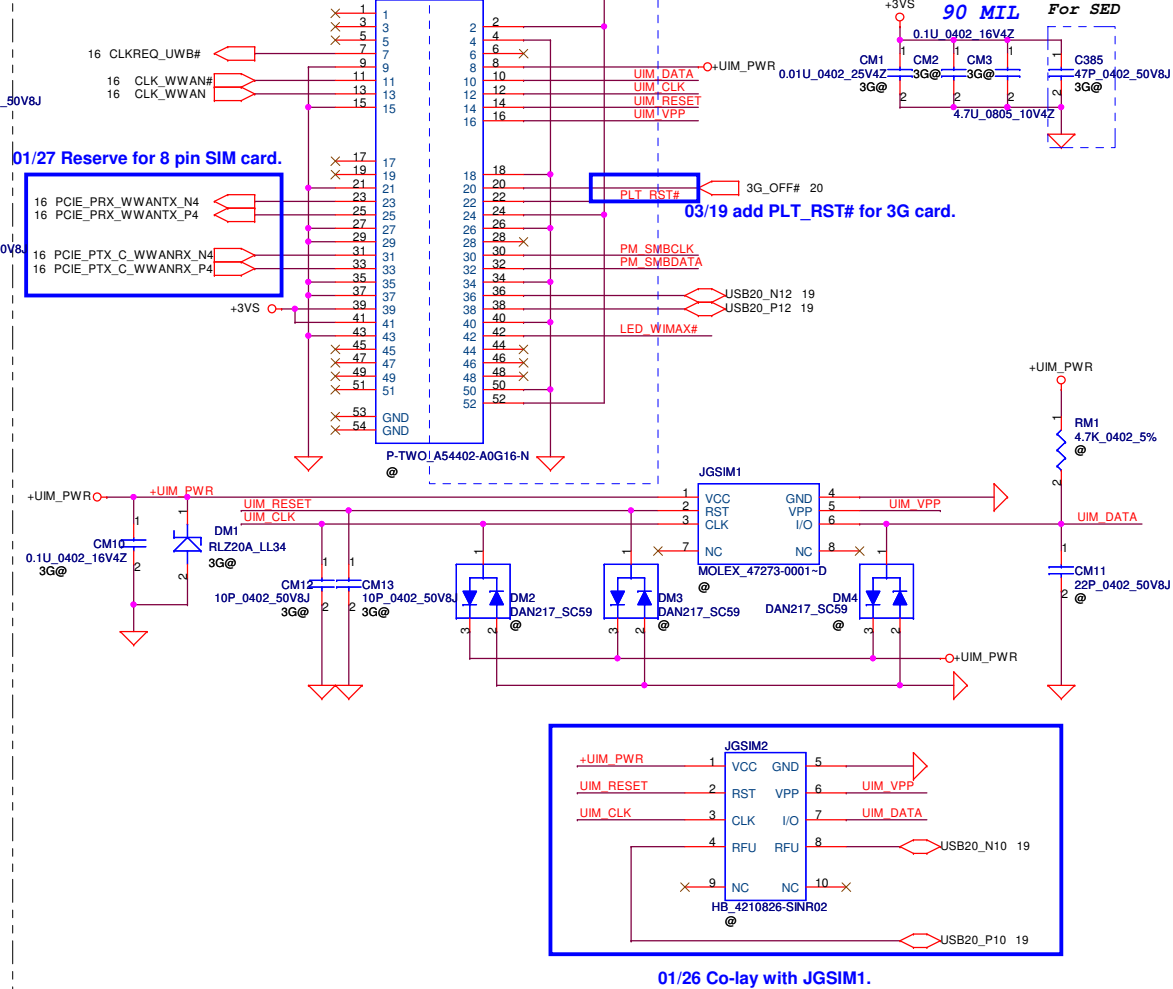


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Size		Document Number		Rev	
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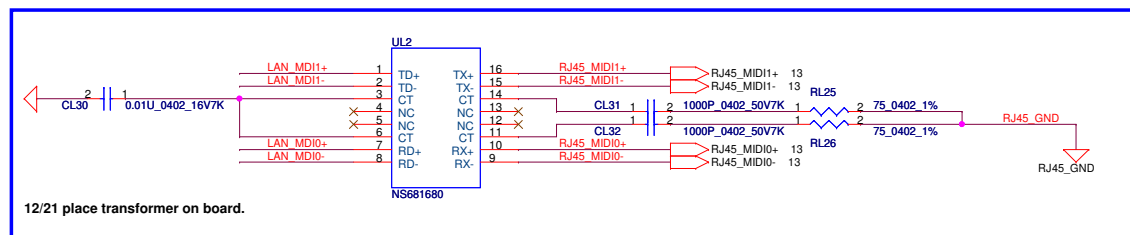
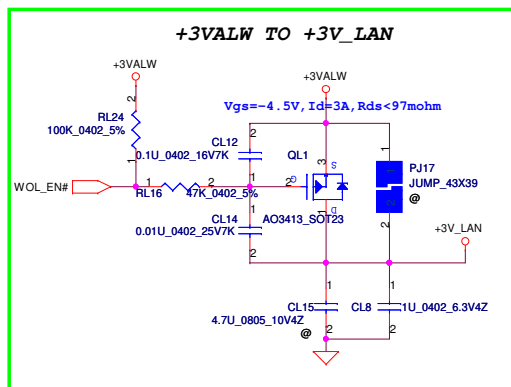
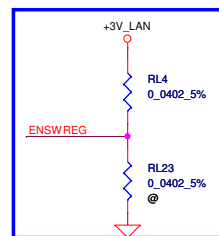
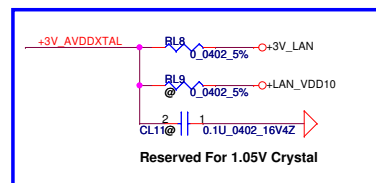
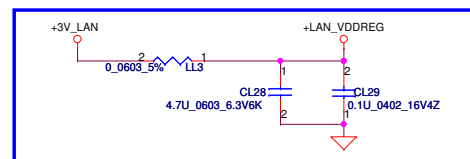
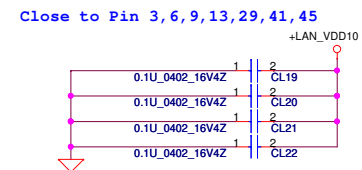
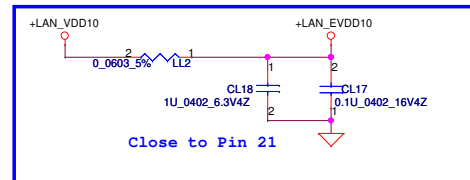
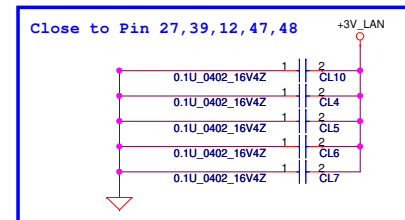
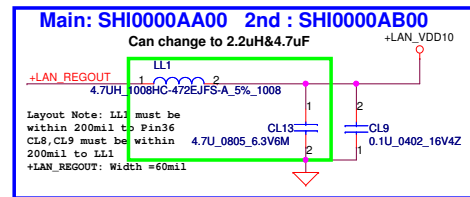
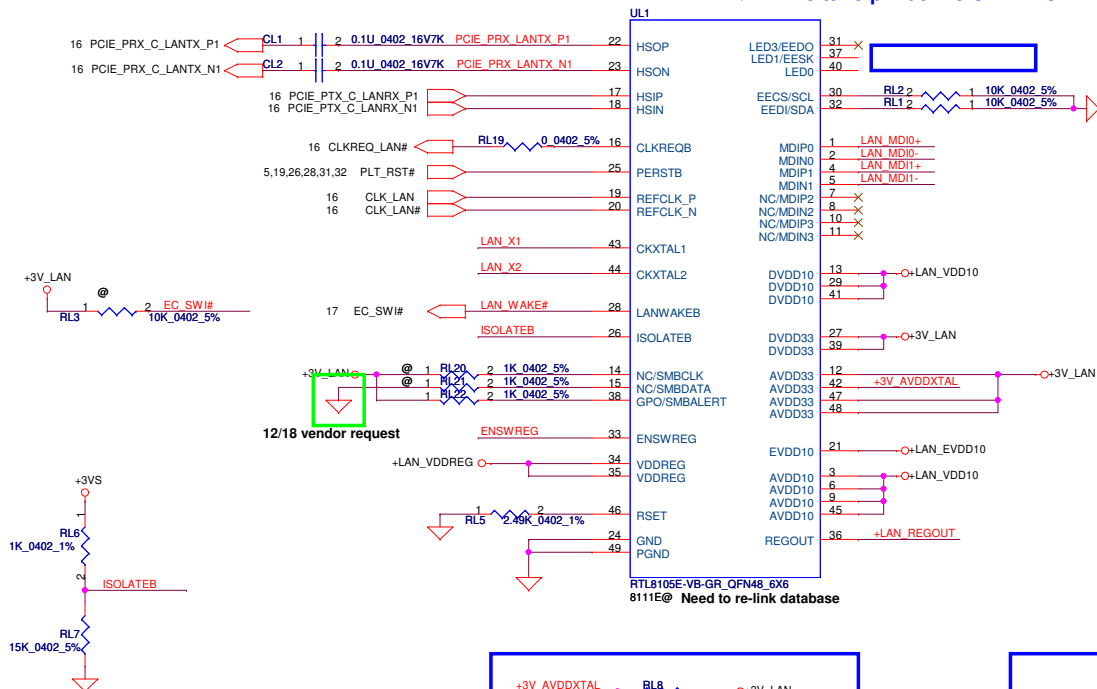
PCIe Mini Card-WLAN/WiMax



PCIe Mini Card-3G



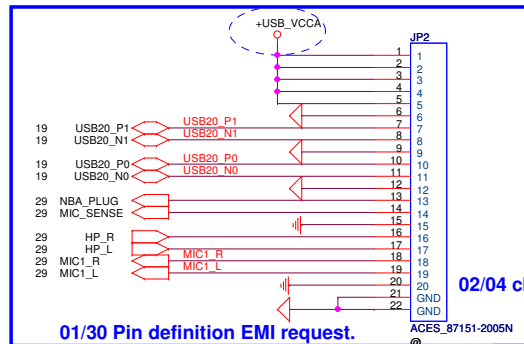
12/14 Fine tune pin define UL1 Pin37 Pin40 -->Dummy



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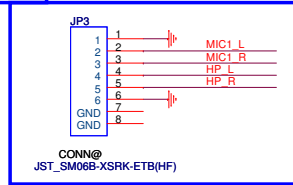
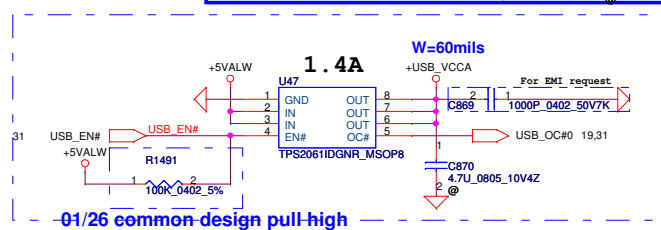
USB+Audio FFC conn Pin=20pin, pitch=0.5

01/30 New JP2 Layout symbol reverse old conn, reserse the pin define



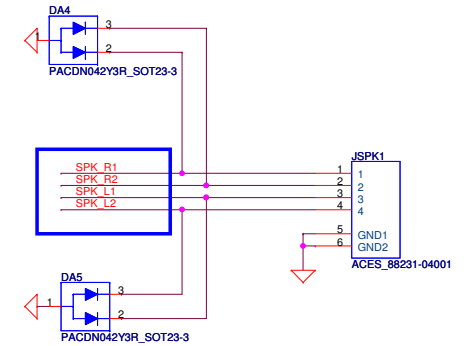
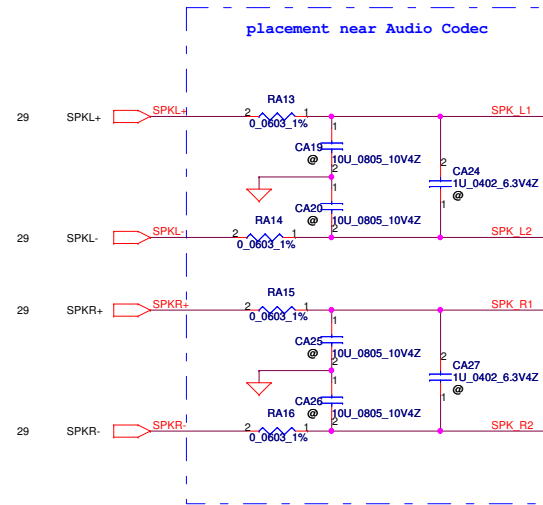
02/04 change back to 20 pins.

01/30 Pin definition EMI request.



12/19 Reserved JP6 for audio test

Speaker Connector

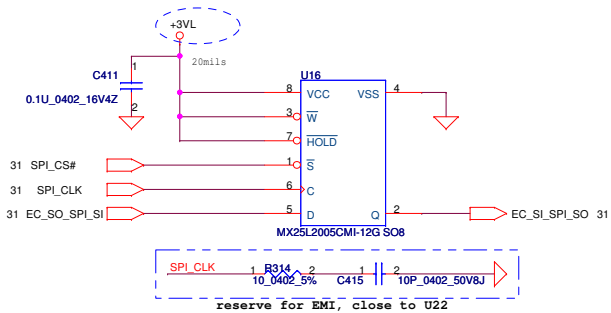


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								AMP/Audio Jack/HP/SPEAKER/VR			
								Size			
								Document Number			
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								1.0			



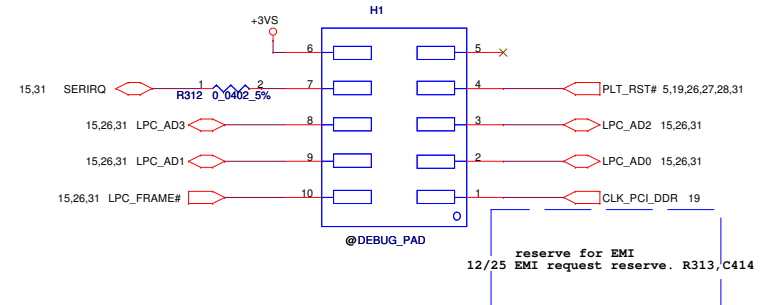
SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

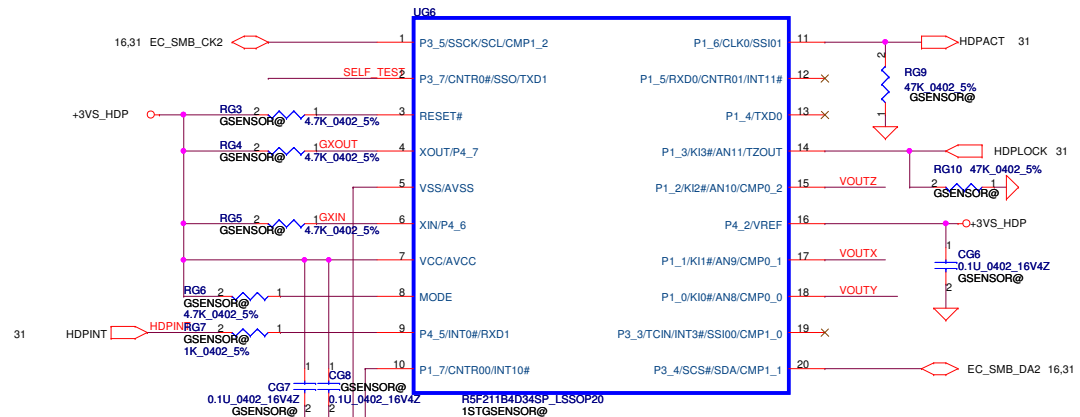
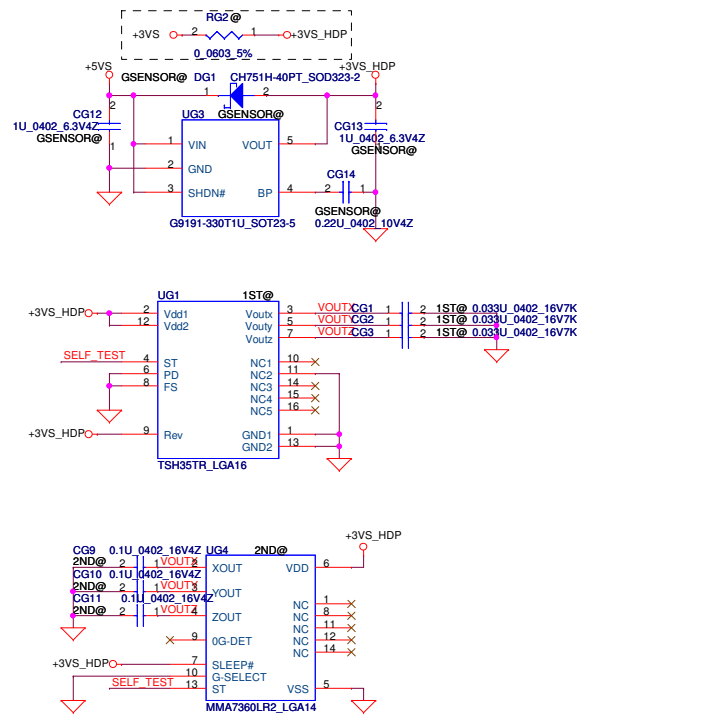


LPC Debug Port

Please place the PAD under DDR DIMM.

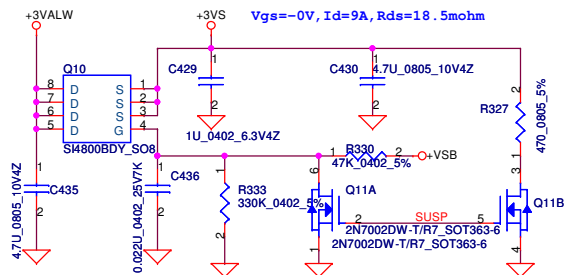


G-Sensor

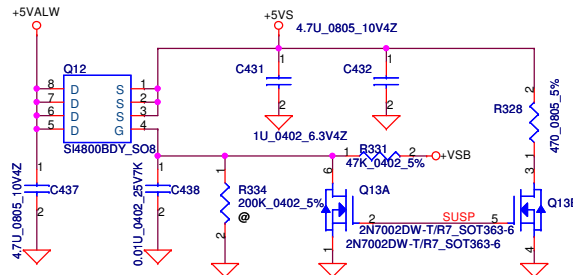


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1.0				Sheet				32 of 45			

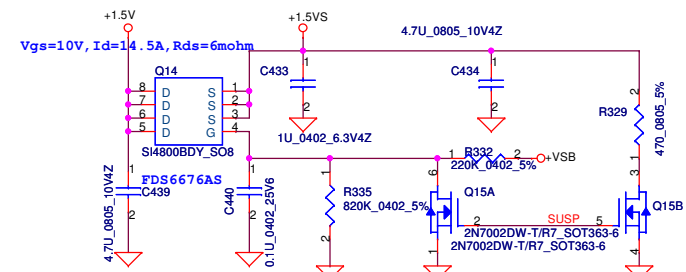
+3VALW TO +3VS



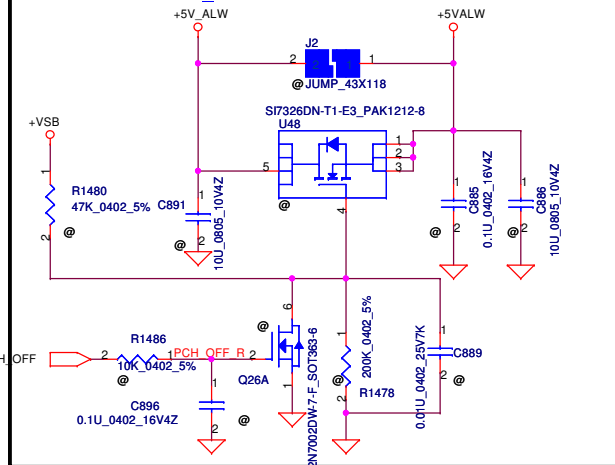
+5VALW TO +5VS



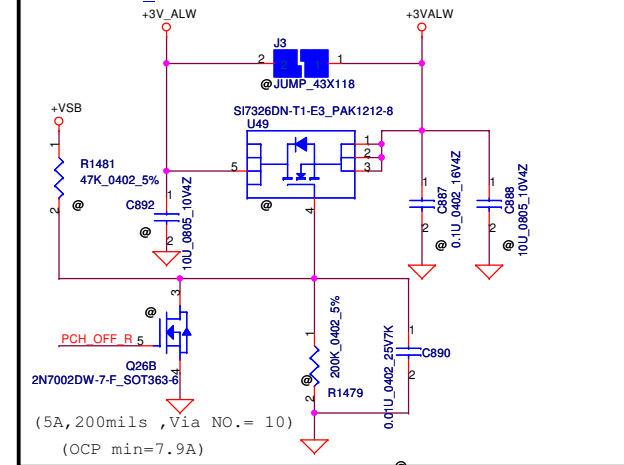
+1.5V to +1.5VS



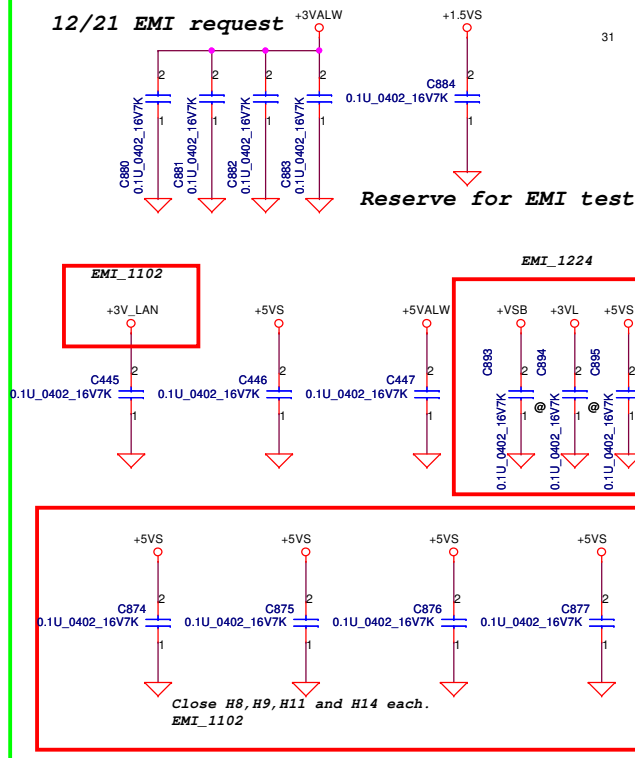
+5V_ALW to +5VALW Transfer



+3V_ALW to +3VALW Transfer

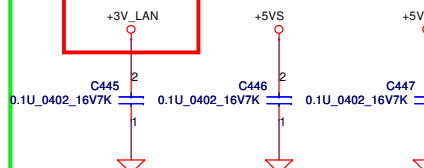


12/21 EMI request

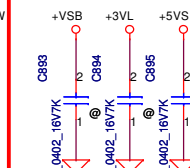


Reserve for EMI test

EMI_1102

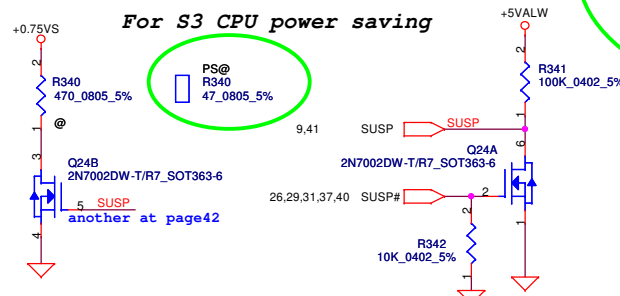


EMI_1224

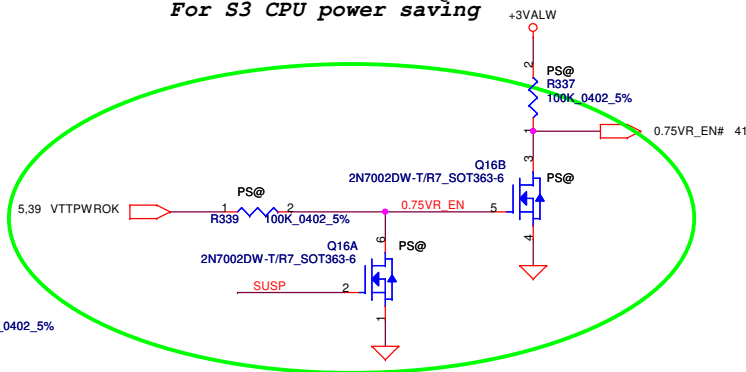


Close H8, H9, H11 and H14 each.
EMI_1102

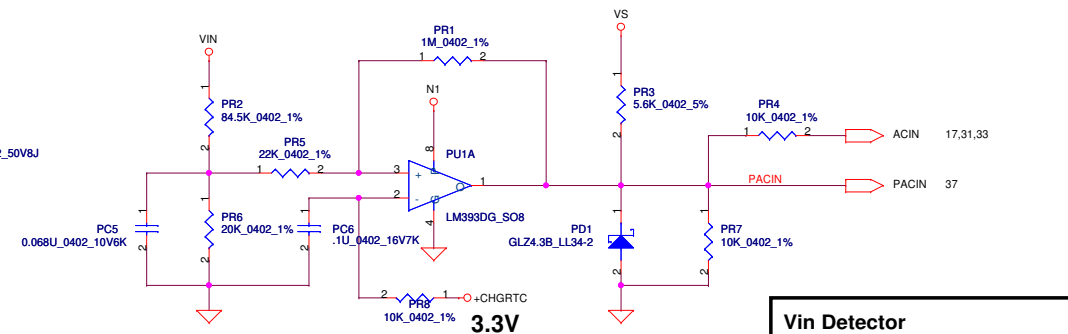
For S3 CPU power saving



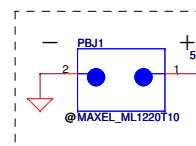
For S3 CPU power saving



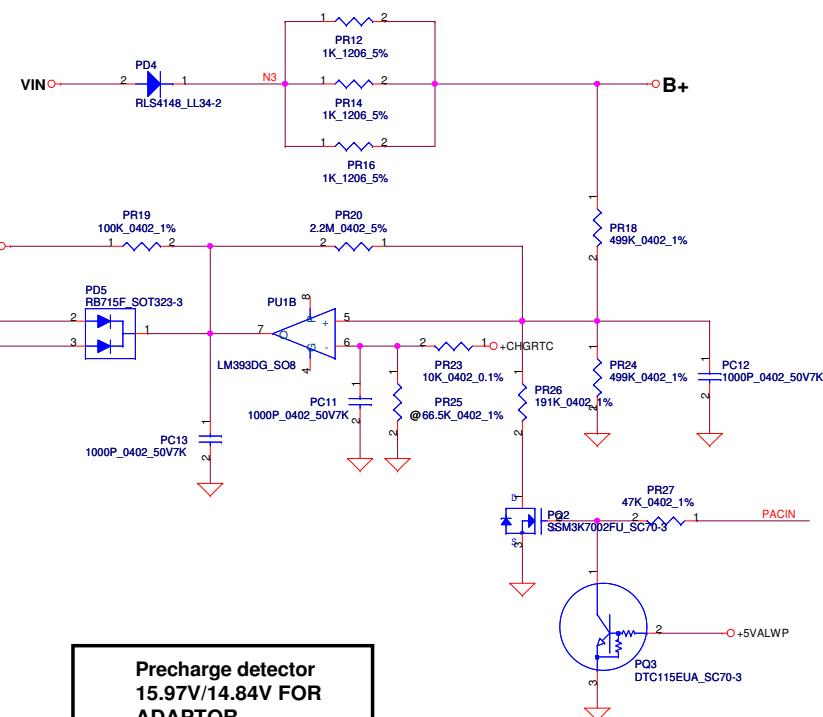
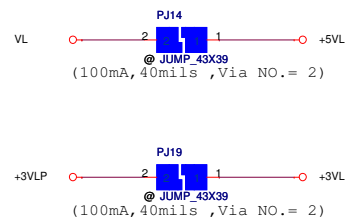
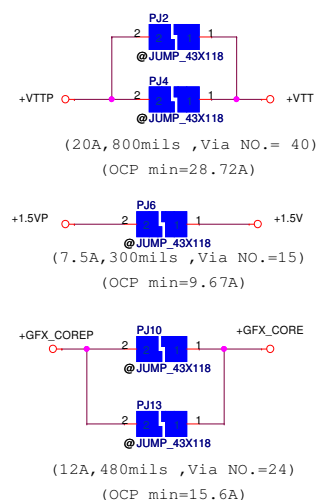
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High	18.384	17.901	17.430
Low	17.728	17.257	16.976



SP093MX0000

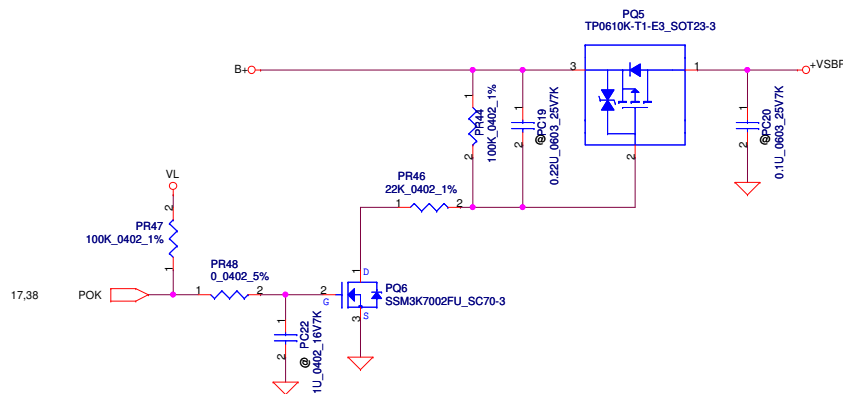
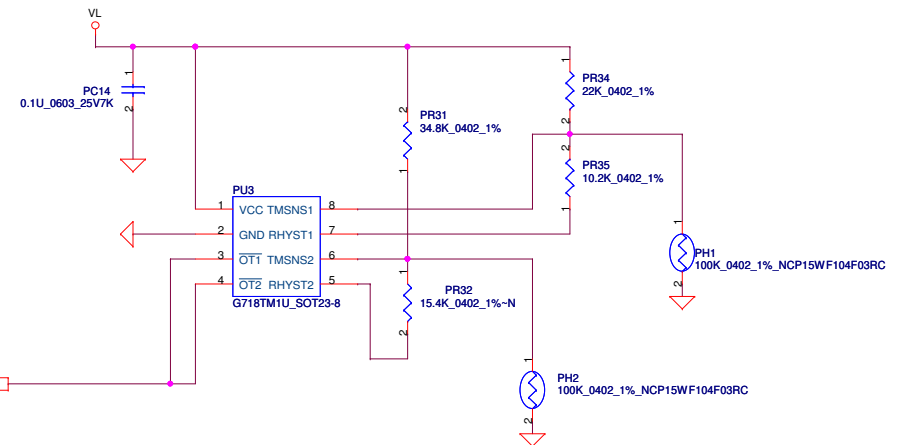
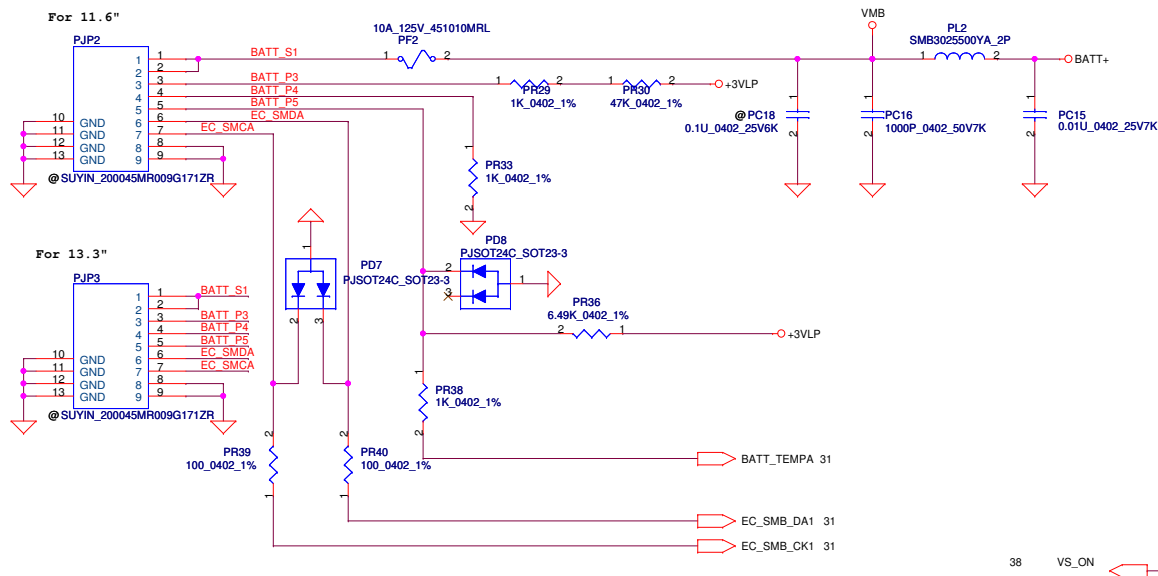


**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

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		Size	Document Number						Rev
			LA-6031P						1.0
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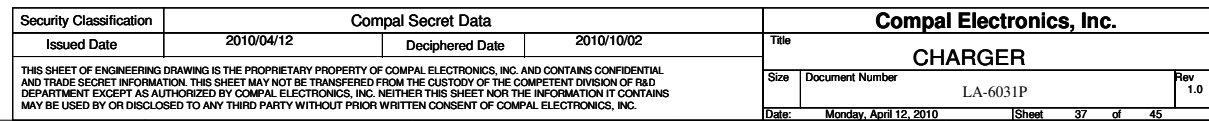
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C

PH2 near main battery CONN:
 BAT.thermal protection at 78 degree C
 Recovery at 42 degree C



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				Deciphered Date				BATTERY CONN / OTP			
				2010/10/02				Size			
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								LA-6031P			
								Rev			
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								Date			
								Monday, April 12, 2010			
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								36			
								of			
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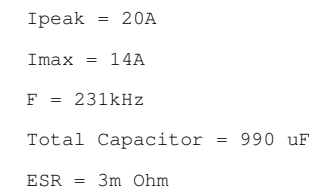
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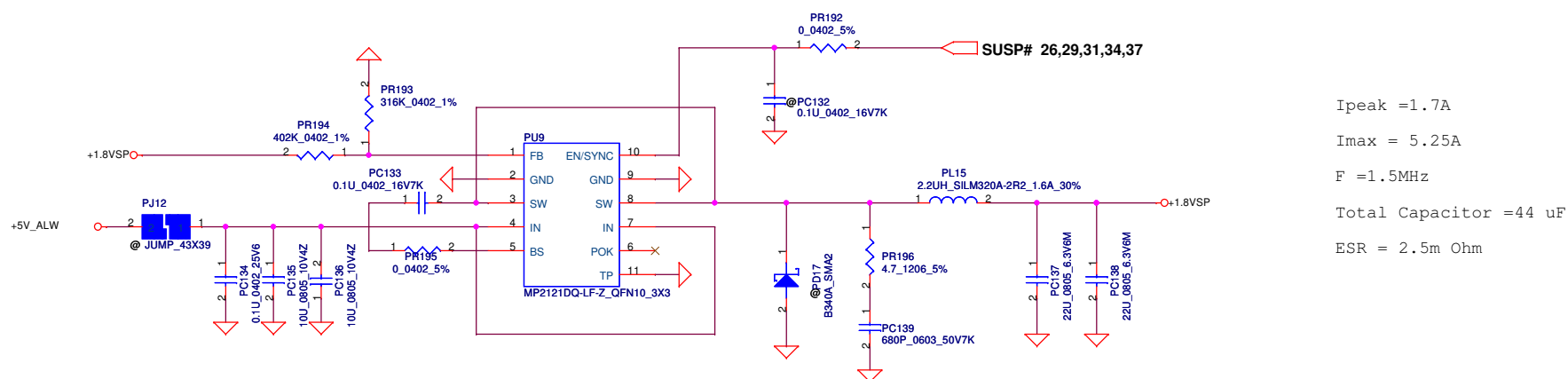
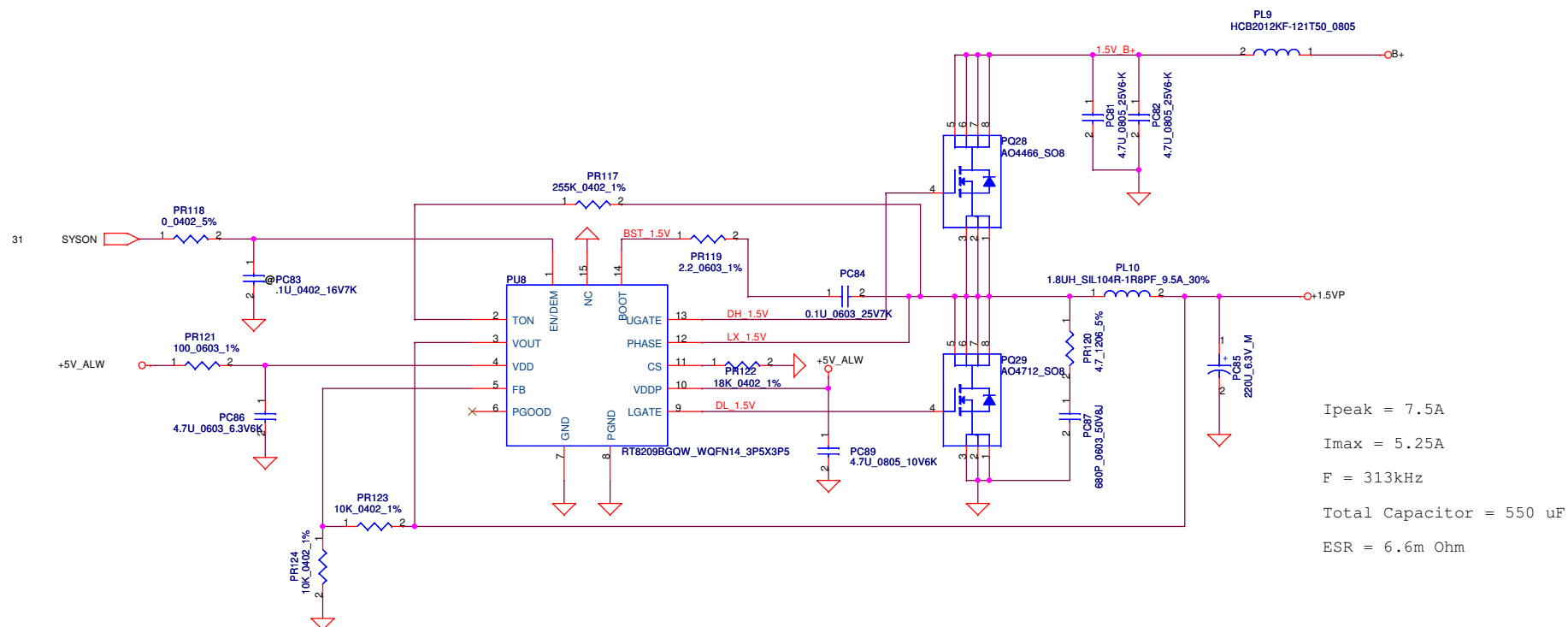
Ipeak = 5A
Imax = 3.5A
F = 305kHz
Total Capacitor = 150 uF
ESR = 18m Ohm

Ipeak = 5A
Imax = 3.5A
F = 245kHz
Total Capacitor = 150 uF
ESR = 18m Ohm

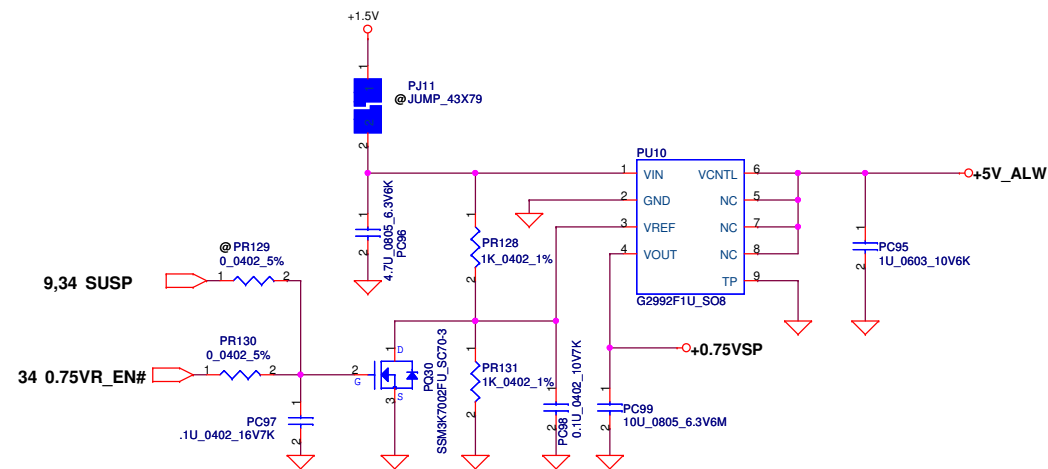
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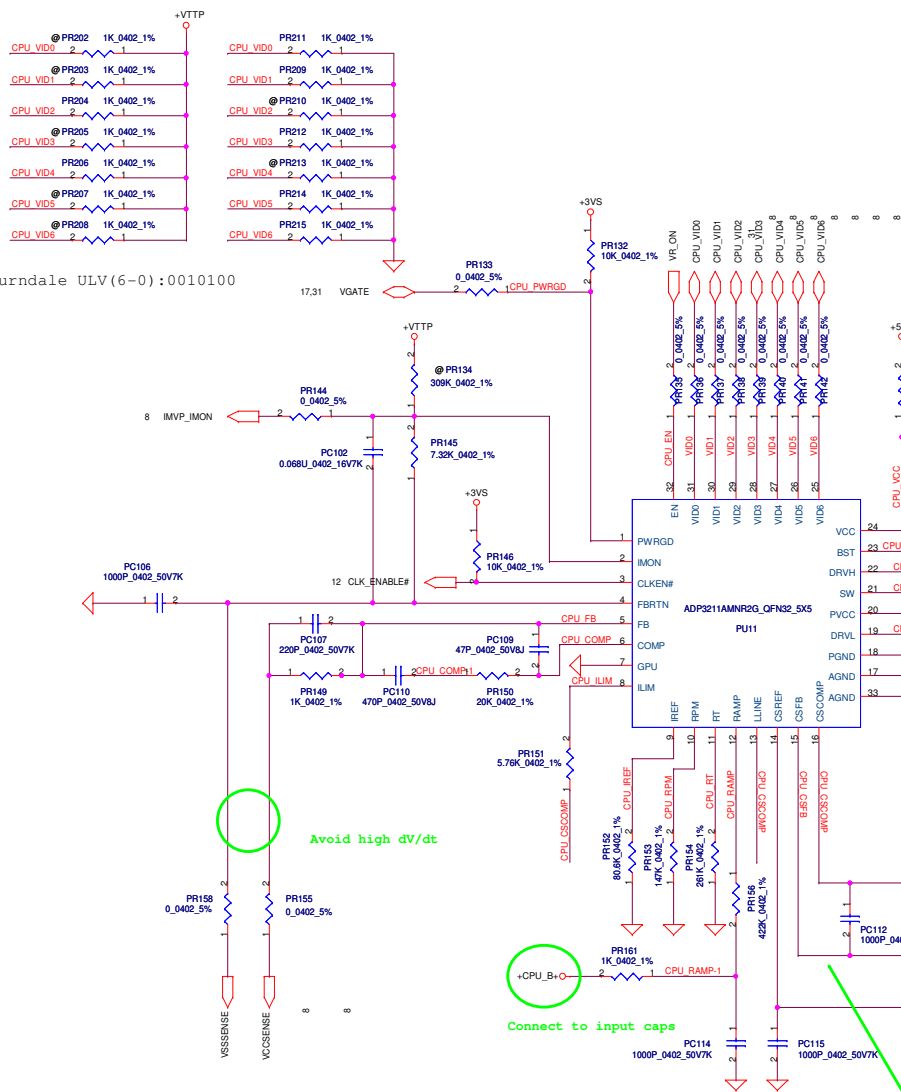


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				+1.5VP/+1.8VSP					
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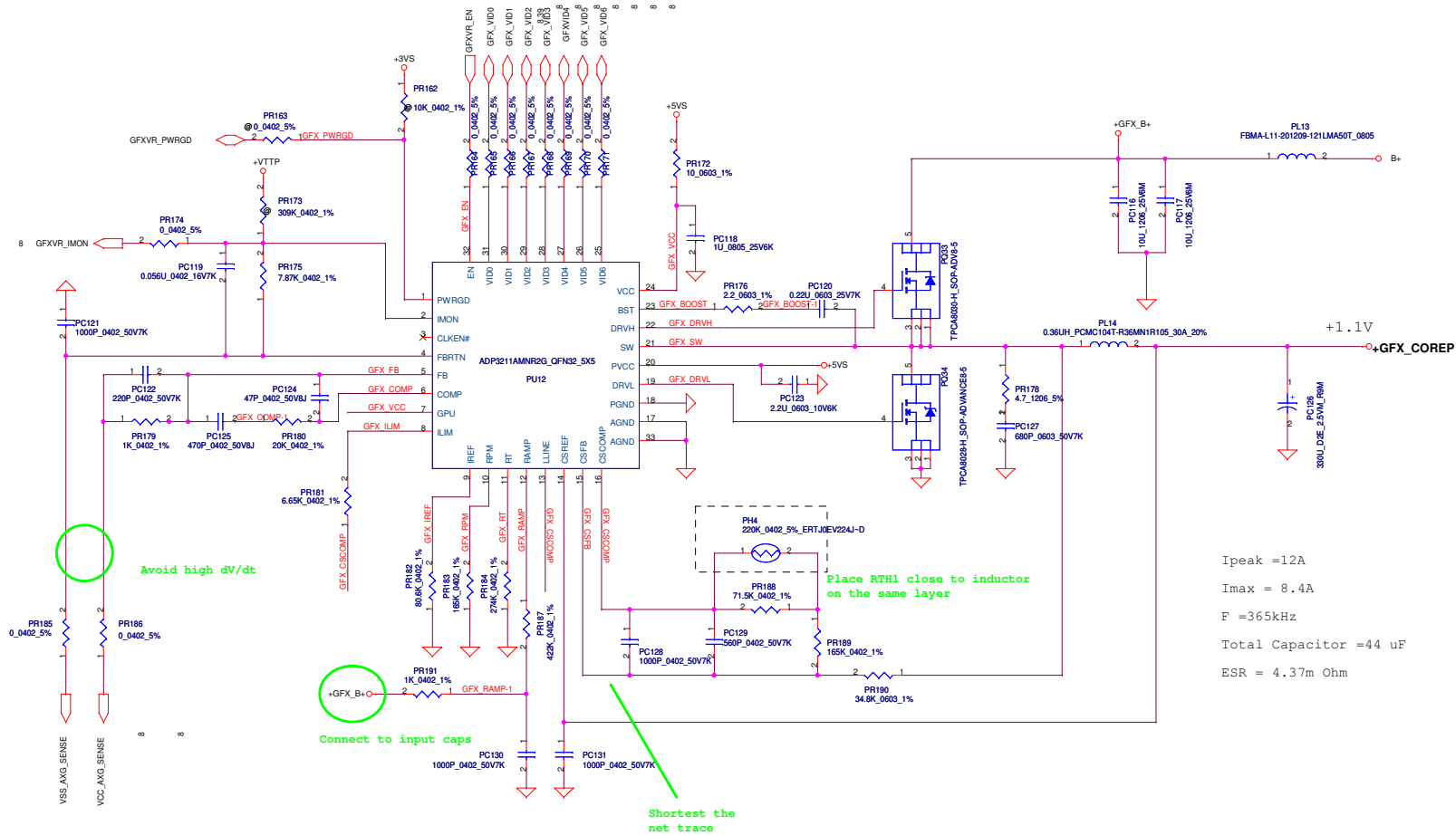
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Anburndale ULV(6-0):0010100



Ipeak = 27A
Imax = 18.9A
F = 350kHz
Total Capacitor = 1320 uF
ESR = 2.25m Ohm

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PC54,PC55,PC65,PC66 change SE076104KM8 to SE076104K80	change to A51 material
2009/11/9 (EVT)	P39	+VTTP	Resever PD15	Design change
2009/11/9 (EVT)	P41	+0.75VSP	Change PQ30 to SB000009610	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PU11 change to ADP3211	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PH3 &PH4	change to A51 material
2009/11/9 (EVT)	P37	CHARGE	Change PR49 change to 33m	Design change
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PR90 & PR91 change to 121K	Design change
2009/12/1 (DVT)	P39	+CPU-CORE	Add PR202~PR215 pull-up & pull-down	Design change
2009/12/17 (DVT)	P36	Battery	Change PR31,PR32,PR34,PR35	Design change
2009/12/17 (DVT)	P37	CHARGE	Change PC23,PC24,PC25,PC81,PC82 1206 to 0805	Design change
2009/12/22 (DVT)	P42	CPU_CORE	Change PR147 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P43	GFX	Change PR176 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P39	+VTTP	ADD material PR125 & PR104 & PR102 and add net VTTPWORK_CPU	Design change
2010/01/25 (PVT)	P36	Battery	Add PD7,PD8	EMI require
2010/01/27 (PVT)	P37	CHARGE	Add 10u x3 PC46,PC47,PC88	EMC require
2010/02/04 (PVT)	P41	+0.75VSP	Resever PR129 Add PR130 and PC97	Design change
2009/02/04 (PVT)	P38	+5VALWP/+3VALWP	Change PQ38	Design change
2010/02/04 (PVT)	P42	CPU_CORE	Change PR160 to 95.3K and PR145 to 7.32K	Design change
2010/02/08 (PVT-2)	P36	Battery	Change PR21&PR22 and +CHGRIC	Design change

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Intel S3 power saving	05	Install Q1, R1484, C878, R8, R40 and Remove R2, R42	12/25	DVT
2	HDMI Detection function	14	modify HDMI_HPD circuit (Remove U7)	12/25	DVT
3	Sleep charge control method change	19 & 31	SLP_CHG_M3_R & SLP_CHG_M4_R change from PCH to Pin103 & 74 of EC	12/25	DVT
4	Implement Low power HDA	22	Reserve R1468 & R1469 for 1.5VALW (Low Power HDA)	12/25	DVT
5	Debug usage	26	Reserve LPC bus at WLAN soft	12/14	DVT
6	LAN circuit change for Vendore request	27	RL21 contact to GND	12/18	DVT
7	Avoid power leakage & reduce double pull up	27	Remove RL3	12/25	DVT
8	Transformer change	27	Move Transformer from Sub-board to M/B	12/21	DVT
9	Prevent Card Reader IC damage when insert dummy card	28	Add F2	12/24	DVT
10	Audio PD# issue (Could not work)	29	Add RA29 pull up	12/19	DVT
11	Avoid Audio noise	29	reserve and unistall CA70, CA68, CA69, UA2, RA30, CA67	12/22	DVT
12	Enhance Right side USB ability	30	modify JP2 pin assignment and reserve JP3 pad for test	12/19	DVT
13	Sleep charge control method change	31	add pin 21 of EC for control ALW power MOS	12/21	DVT
14	Sleep charge control method change	34	add two ALW power transfer circuits (3V_ALW to 3VALW & 5V_ALW to 5VALW)	12/21	DVT
15	system idle hang up issue	8	CPU_PSI# Pull down 1k ohm & H_DPRS LPVR pull up 1k ohm to VIT	12/19	DVT
16	Sleep charge control method change	24	change U14 power from 5VALW to 5V_ALW	12/21	DVT
17					
18	EC_SW# pull up twice. R190	27	RL3 reserved.	01/20	PVT
19	Audio LDO reserved for AVDD.	29	UA2 pin 5 for +AVDD	01/20	PVT
20	For S3 power saving.	05	Reserve R2 and change R1484 to 0 ohm.	01/20	PVT
21	For 3G LED flash when resume from S3.	33	Reserve Q21 and Q22 circuit. Add R338 and R336.	01/20	PVT
22	Don't need discharge circuit.	34	Modify Q26 and Q27 circuit.	01/20	PVT
23	Reserve for PCH and EC both.	19,24,31	Add R1487,R1488,R1489 and R1490.	01/20	PVT
24	Change JHDD1 pin 4 to GND.	24		01/20	PVT
25	Add BT power control circuit.	26	Add D85 and Q27.	01/20	PVT
26	change cardreader connector.	28	ME request	01/26	PVT
27	change LED always power	33	3G LED flash issue.	01/26	PVT
28	change TP connector.	33	ME request	01/26	PVT
29	JGSIM2 connector.	26		01/26	PVT
30	add R1491 in USB_EN#	30		01/26	PVT
31	Lid switch change to +3V_ALW	31,33	Toshiba request.	01/26	PVT
32	add USB port 9 and PCIe port 4 for 8 pin SIM card.	16,19,26		01/27	PVT
33	add R1494 and D84 near D5, and add L1C near U8	15,18	EMI request	02/03	PVT
34	change MIC1_R and MIC1_L pull high	29	MIC issue.	02/03	PVT
35	JLVDS1 pin24 change to NC	12	Common design.	03/04	PVT2
36	CRT trace modify.	18	wrong trace.	03/04	PVT2
37	D5 layout close to PCH(U8)		layout change	03/04	PVT2
38	Change O2 to JMicon card reader.	28		03/22	PVT2
39	USB OC# change	19	Common design.	03/22	PVT2
40	Add R1505.	17	EMI request	03/22	PVT2

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