Compal confidential

Thin & Light

NDU01/NDU11 LA-6032P REV 1.0 Schematics Document

Mobile AMD ASB2/RS880M/SB820M

2010-03-22 Rev. 1.0

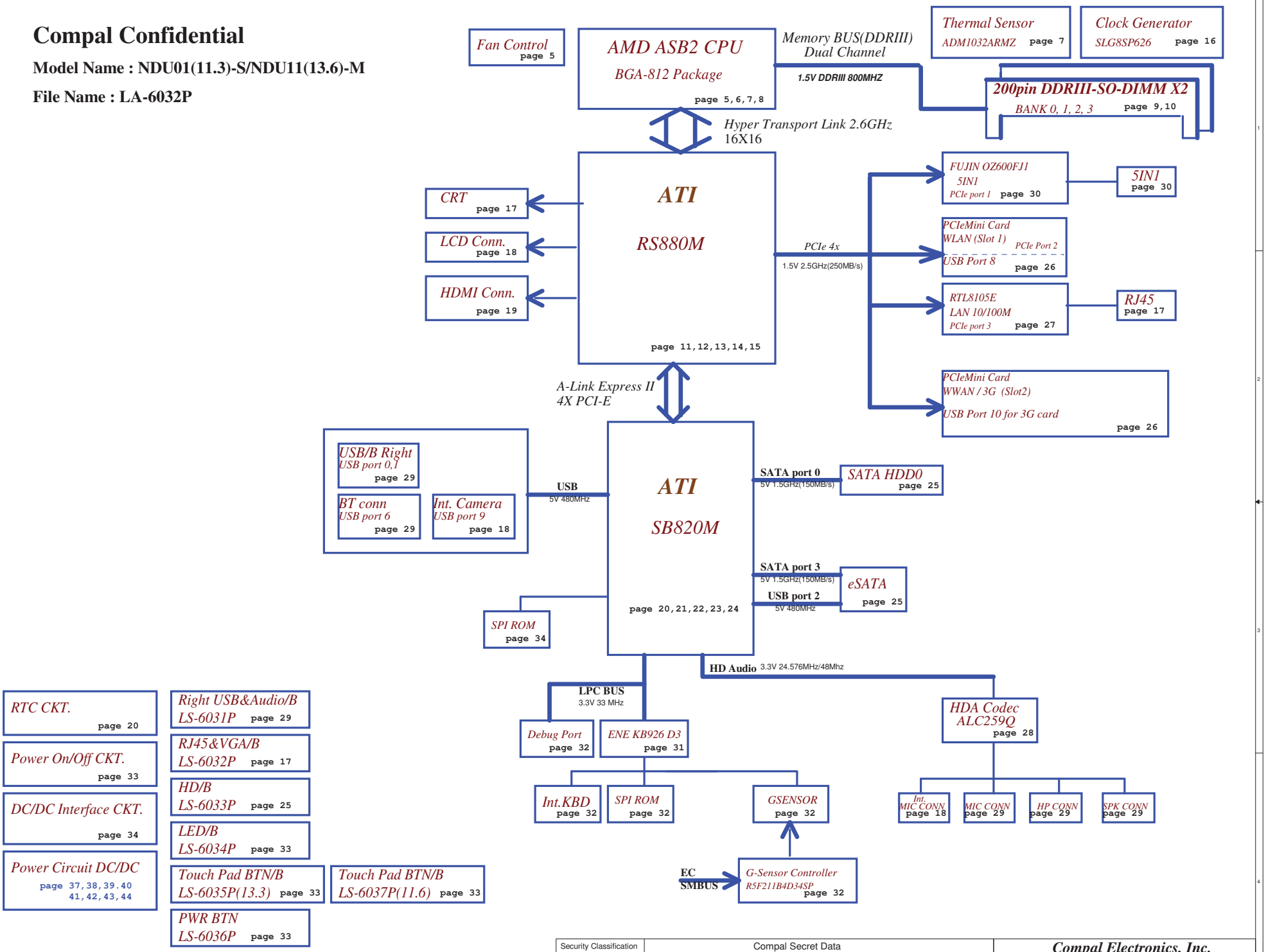
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: LA-6032P	Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 1 of 45	

Compal Confidential

Model Name : NDU01(11.3)-S/NDU11(13.6)-M

File Name : LA-6032P



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Block Diagram			
Size: Custom	Document Number: LA-6032P		Rev: 1.0
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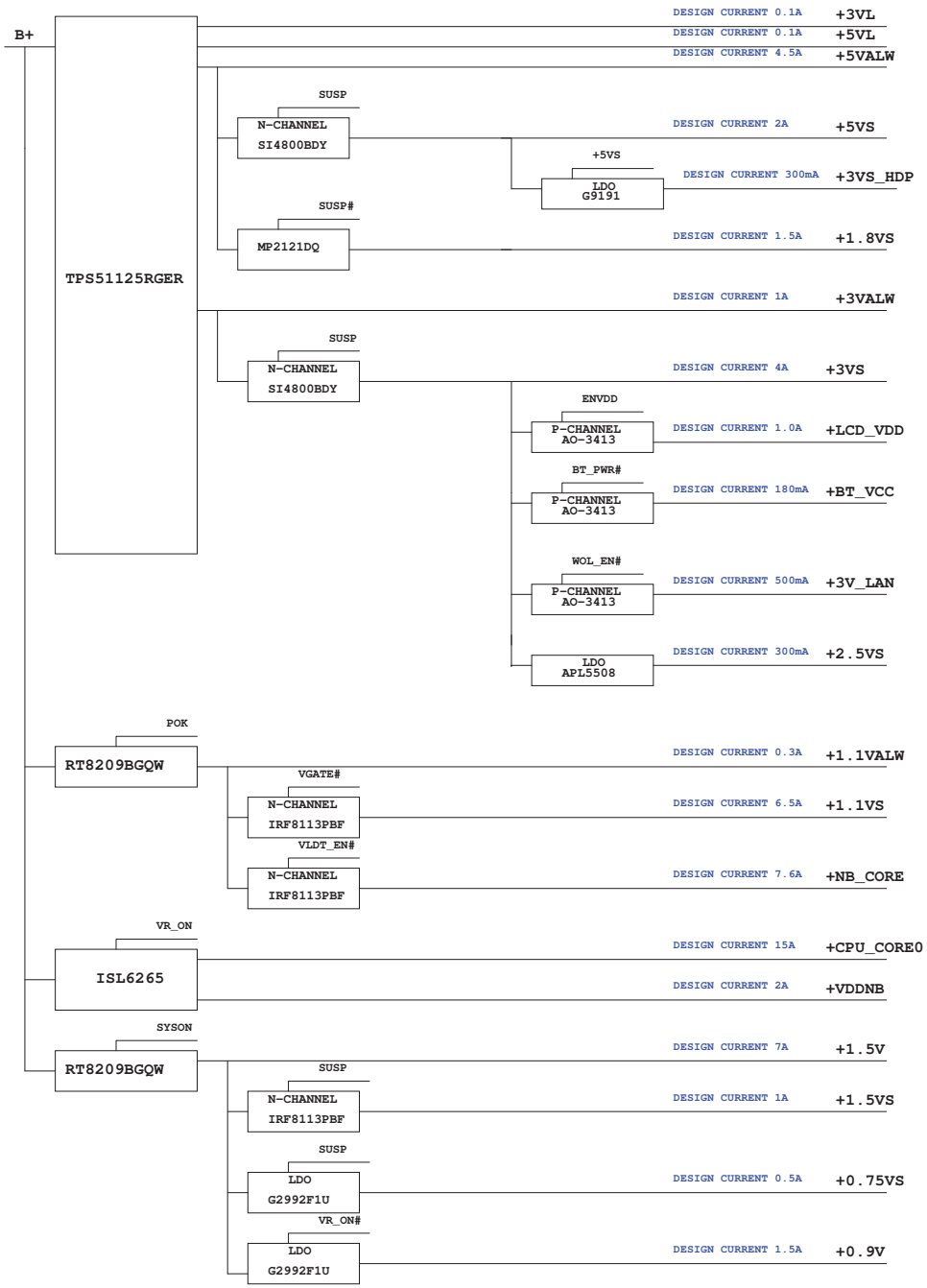

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **Power Map**

Size	Document Number	Rev
Custom	LA-5381P	1.0

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Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +0.9VS +0.75VS +NB_CORE +VDDNB +CPU_CORE_0
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground : means Analog Ground

@ : means just reserve , no build
K625R3@ : means just for 1.5G CPU
K125R3@ : means just for 1.7G CPU
K325R3@ : means just for 1.3G CPU
K625R1@ : means just for 1.5G CPU
K125R1@ : means just for 1.7G CPU
K325R1@ : means just for 1.3G CPU
M@ : means just reserve for 13.3 control
S@ : means just reserve for 11.6 control
GSENSOR@ : means just reserve for G sensor part
1ST@ : means just reserve 1st G sensor IC
1STGSENSOR@ : means just reserve 1st G sensor IC
2ND@ : means just reserve 2nd G sensor IC
~~2NDGSENSOR@ : means just reserve 2nd G sensor IC~~
NOSIDE@ : means just reserve NOSIDE
SIDE@ : means just reserve SIDE port
RS880MR1@ : means just for RS880MR1
RS880MR3@ : means just for RS880MR3
SB820MR1@ : means just for SB820MR1
SB820MR3@ : means just for SB820MR3

For 11.6 and 13.3 DAZ

ZZZ
PCB-MB

K625 mean 1.7G CPU
U1 K625R3@ K125 CPU

K125 mean 1.7G CPU
U1 K125R1@ K125 CPU

K325 mean 1.3G CPU
U1 K325R1@ K325 CPU

K125 mean 1.7G CPU
U1 K125R3@ K125 CPU

K325 mean 1.3G CPU
U1 K325R3@ K325 CPU

RS880M
U5 RS880MR3@ RS880M

SB820M
U7 SB820MR3@ SB820M

SB SM Bus1 Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b

SB SM Bus2 Address

Power	Device	HEX	Address
+3VALW	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	CPU_ADM1032-1	98 H	1001 100X b
+3VS	G-Sensor		

SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	G-sensor
EC_SMB_CK1 EC_SMB_DA1	KB926	V							
EC_SMB_CK2 EC_SMB_DA2	KB926		V						V
I2C_CLK I2C_DATA	RS880M						V		
DDC_CLK0 DDC_DATA0	RS880M							V	
SCL0 SDA0	SB820			V	V				
SCL1 SDA1	SB820					V			

Compal Electronics, Inc.

Title: Notes List

Size: B (Custom) | Document Number: LA-6032P | Rev: 1.0

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11 H_CADIP[0..15] H_CADIP[0..15]

11 H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] 11

H_CADON[0..15] H_CADON[0..15] 11

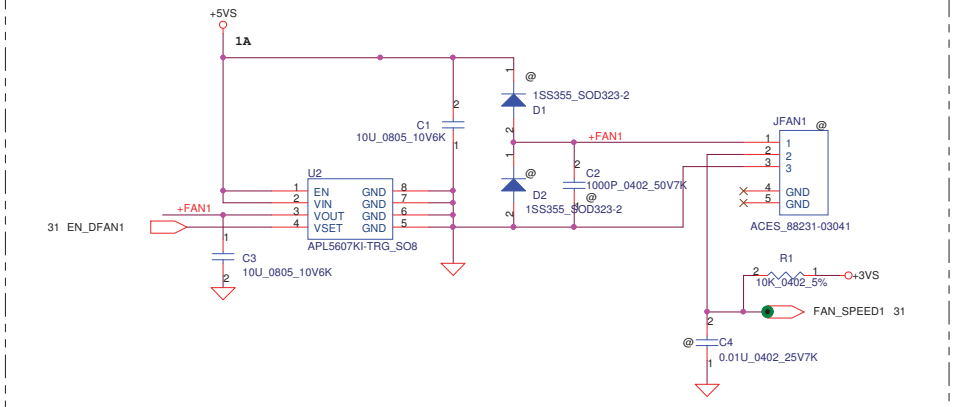
U1A

	H_CADIP15	W7	L0_CADIN_H15	L0_CADOUT_H15	AB6	H_CADOP15
	H_CADIN15	W6	L0_CADIN_L15	L0_CADOUT_L15	AB5	H_CADON15
	H_CADIP14	U6	L0_CADIN_H14	L0_CADOUT_H14	AB9	H_CADOP14
	H_CADIN14	U5	L0_CADIN_L14	L0_CADOUT_L14	AB8	H_CADON14
	H_CADIP13	R7	L0_CADIN_H13	L0_CADOUT_H13	AC7	H_CADOP13
	H_CADIN13	R6	L0_CADIN_L13	L0_CADOUT_L13	AC6	H_CADON13
	H_CADIP12	P6	L0_CADIN_H12	L0_CADOUT_H12	AE6	H_CADOP12
	H_CADIN12	P5	L0_CADIN_L12	L0_CADOUT_L12	AE5	H_CADON12
	H_CADIP11	L6	L0_CADIN_H11	L0_CADOUT_H11	AE9	H_CADOP11
	H_CADIN11	L5	L0_CADIN_L11	L0_CADOUT_L11	AE8	H_CADON11
	H_CADIP10	J6	L0_CADIN_H10	L0_CADOUT_H10	AH3	H_CADOP10
	H_CADIN10	J5	L0_CADIN_L10	L0_CADOUT_L10	AH4	H_CADON10
	H_CADIP9	H4	L0_CADIN_H9	L0_CADOUT_H9	AK3	H_CADOP9
	H_CADIN9	H3	L0_CADIN_L9	L0_CADOUT_L9	AK4	H_CADON9
	H_CADIP8	G6	L0_CADIN_H8	L0_CADOUT_H8	AH1	H_CADOP8
	H_CADIN8	G5	L0_CADIN_L8	L0_CADOUT_L8	AH2	H_CADON8
	H_CADIP7	T3	L0_CADIN_H7	L0_CADOUT_H7	Y1	H_CADOP7
	H_CADIN7	T4	L0_CADIN_L7	L0_CADOUT_L7	Y2	H_CADON7
	H_CADIP6	T2	L0_CADIN_H6	L0_CADOUT_H6	Y4	H_CADOP6
	H_CADIN6	T1	L0_CADIN_L6	L0_CADOUT_L6	Y3	H_CADON6
	H_CADIP5	P3	L0_CADIN_H5	L0_CADOUT_H5	AB1	H_CADOP5
	H_CADIN5	P4	L0_CADIN_L5	L0_CADOUT_L5	AB2	H_CADON5
	H_CADIP4	P2	L0_CADIN_H4	L0_CADOUT_H4	AB4	H_CADOP4
	H_CADIN4	P1	L0_CADIN_L4	L0_CADOUT_L4	AB3	H_CADON4
	H_CADIP3	M2	L0_CADIN_H3	L0_CADOUT_H3	AD4	H_CADOP3
	H_CADIN3	M1	L0_CADIN_L3	L0_CADOUT_L3	AD3	H_CADON3
	H_CADIP2	K3	L0_CADIN_H2	L0_CADOUT_H2	AF1	H_CADOP2
	H_CADIN2	K4	L0_CADIN_L2	L0_CADOUT_L2	AF2	H_CADON2
	H_CADIP1	K2	L0_CADIN_H1	L0_CADOUT_H1	AF4	H_CADOP1
	H_CADIN1	K1	L0_CADIN_L1	L0_CADOUT_L1	AF3	H_CADON1
	H_CADIP0	H2	L0_CADIN_H0	L0_CADOUT_H0	AK1	H_CADOP0
	H_CADIN0	H1	L0_CADIN_L0	L0_CADOUT_L0	AK2	H_CADON0
11 H_CLKIP1	H_CLKIP1	M8	L0_CLKIN_H1	L0_CLKOUT_H1	AF6	H_CLKOP1 11 H_CLKOP1
11 H_CLKIN1	H_CLKIN1	M7	L0_CLKIN_L1	L0_CLKOUT_L1	AF5	H_CLKON1 11 H_CLKON1
11 H_CLKIP0	H_CLKIP0	M3	L0_CLKIN_H0	L0_CLKOUT_H0	AD1	H_CLKOP0 11 H_CLKOP0
11 H_CLKIN0	H_CLKIN0	M4	L0_CLKIN_L0	L0_CLKOUT_L0	AD2	H_CLKON0 11 H_CLKON0
11 H_CTLIP1	H_CTLIP1	Y6	L0_CTLIN_H1	L0_CTLOUT_H1	Y8	H_CTLOP1 11 H_CTLOP1
11 H_CTLIN1	H_CTLIN1	Y5	L0_CTLIN_L1	L0_CTLOUT_L1	Y9	H_CTLON1 11 H_CTLON1
11 H_CTLIP0	H_CTLIP0	V2	L0_CTLIN_H0	L0_CTLOUT_H0	V4	H_CTLOP0 11 H_CTLOP0
11 H_CTLIN0	H_CTLIN0	V1	L0_CTLIN_L0	L0_CTLOUT_L0	V3	H_CTLON0 11 H_CTLON0

HT LINK

TMK625DBV23GM_FCBGA812
K625@

FAN Control Circuit



Security Classification	Compal Secret Data		
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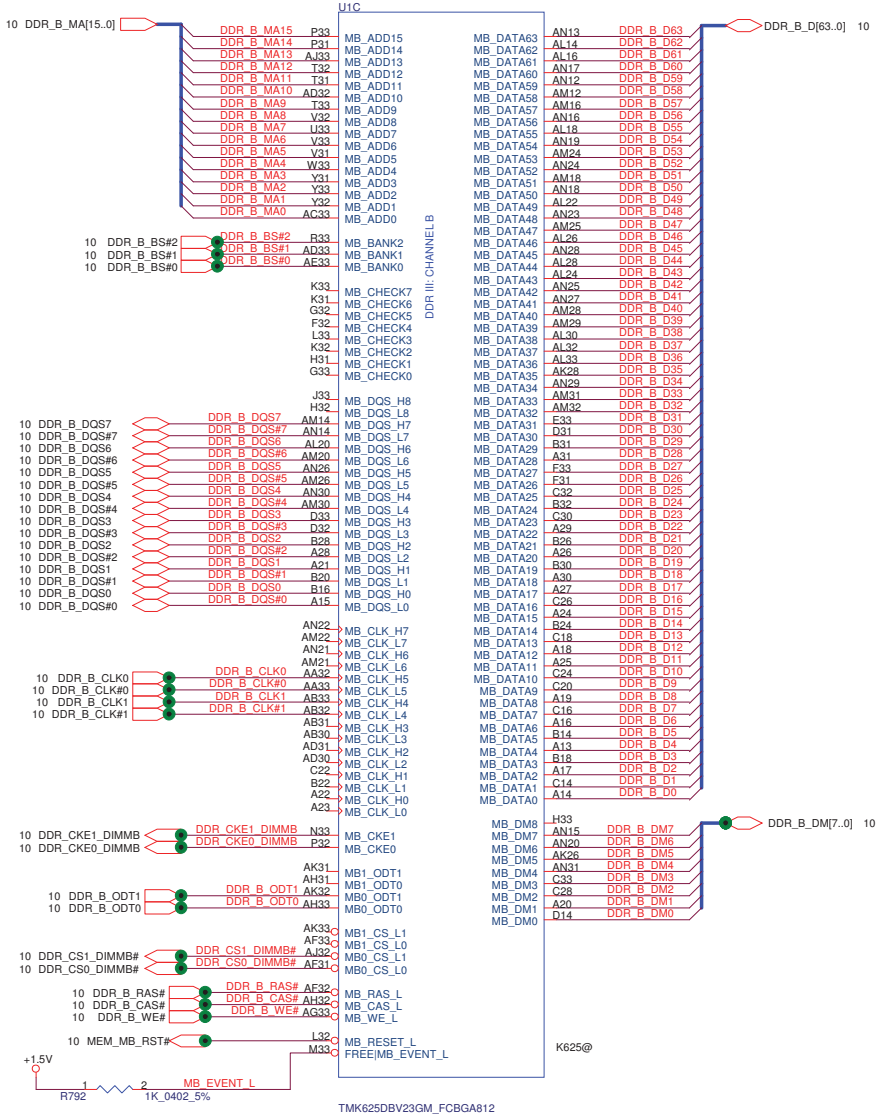
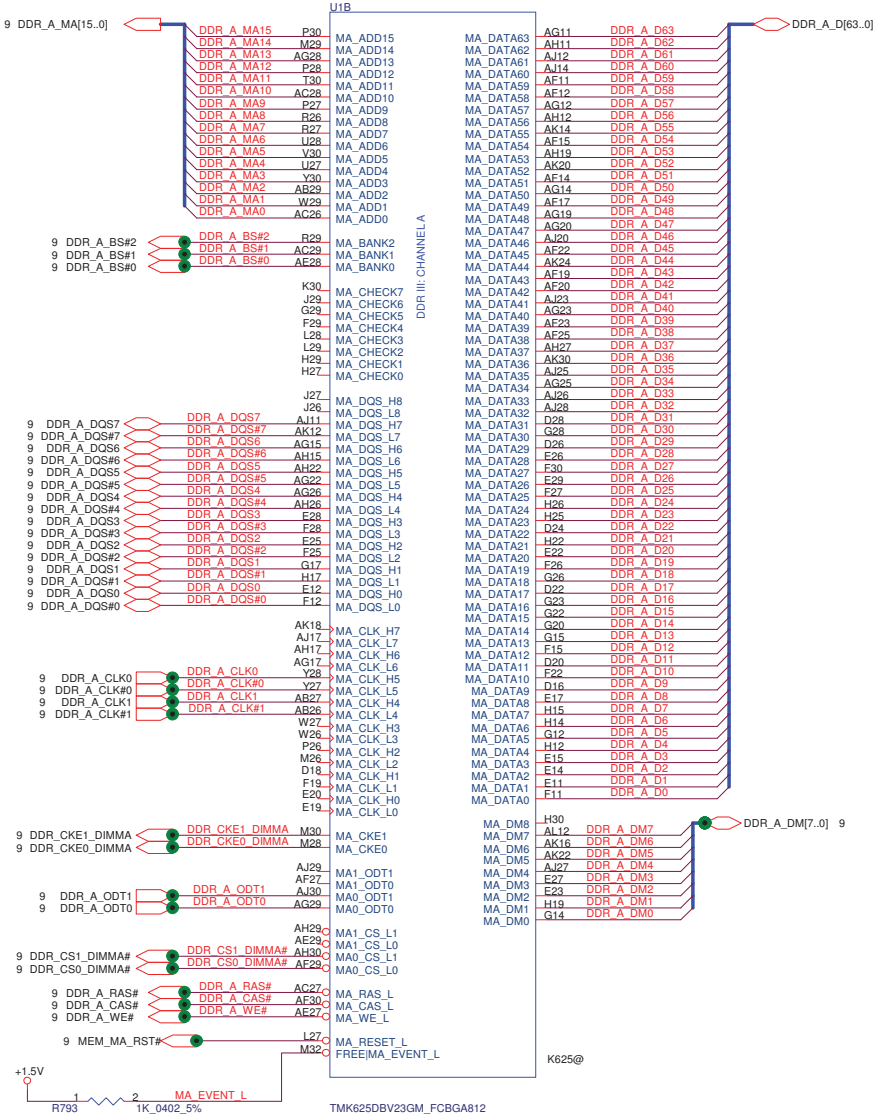
Compal Electronics, Inc.

Title: AMD CPU S1G2 HT I/F

Size: B(28 Custom) | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 5 of 45





Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: AMD CPU S1G2 DDRII I/F

Size: B(28 Custom) | Document Number: LA-6032P | Rev: 1.0

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+2.5VDDA@250mA

R8 Close to CPU within 0.6"
C9 C10 Close to CPU within 1.2"

Close to CPU within 1"

R14 R15 Close to CPU within 1.5"

Close to CPU

TMK625DBV23GM_FCBGA812 K625@

CONN@ SAMTEC_ASP-68200-07

ADM1032ARM-1 ZREEL_MSOP8

Thermal Sensor

Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

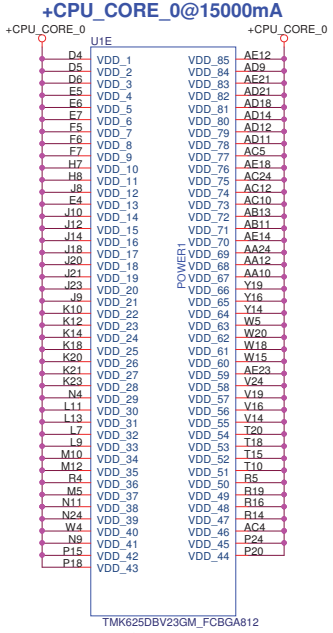
Compal Electronics, Inc.

Title: AMD CPU S1G2 CTRL

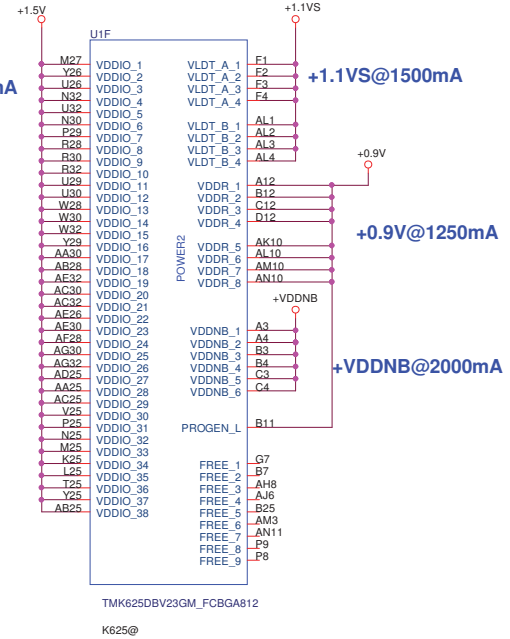
Size: B2B Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 7 of 45

+CPU_CORE_0@15000mA



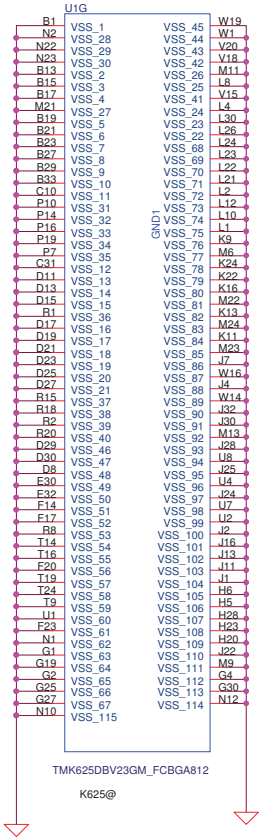
3000mA

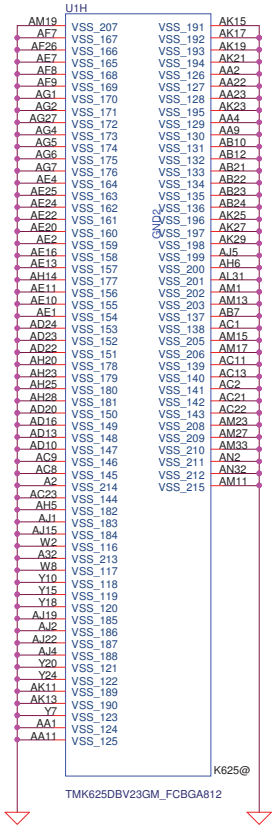


+1.1VS@1500mA

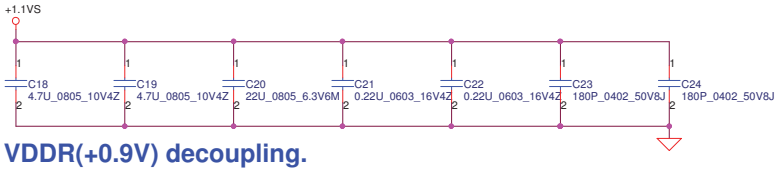
+0.9V@1250mA

+VDDNB@2000mA

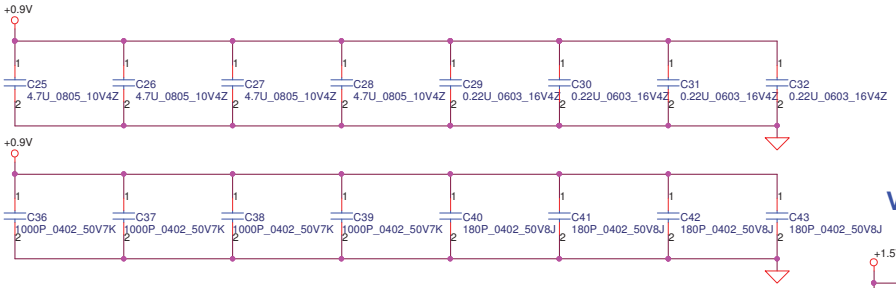




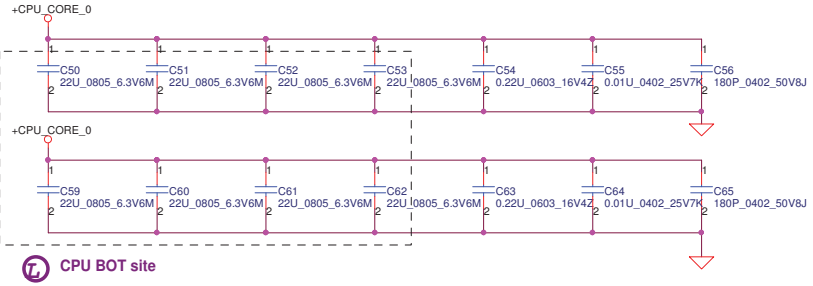
VLDT_A&VLDT_B(+1.1VS) decoupling.



VDDR(+0.9V) decoupling.

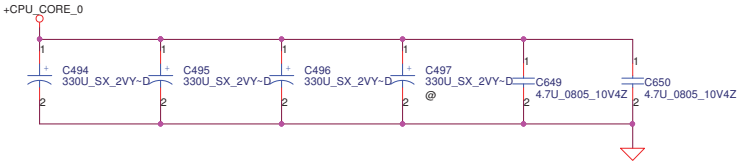


VDD(+CPU_CORE_0) decoupling.

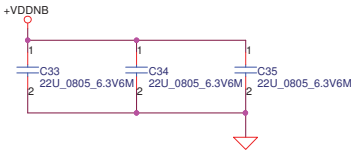


CPU BOT site

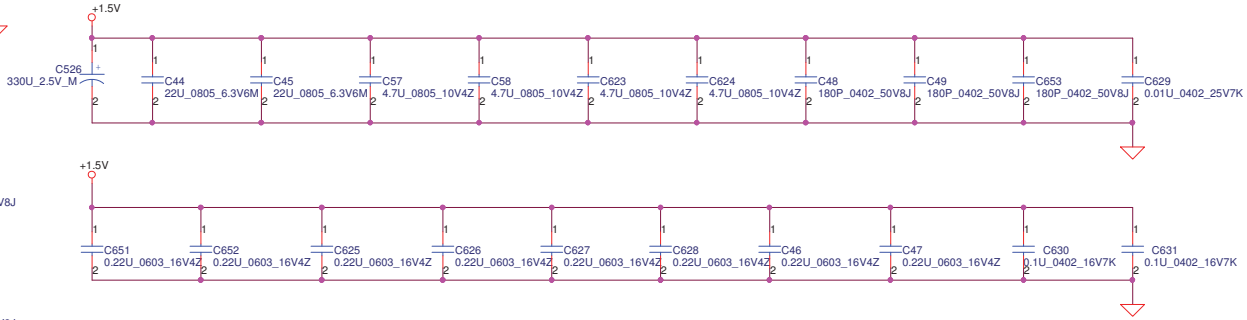
VDD(+CPU_CORE_0) decoupling.



VDDNB(+VDDNB) decoupling.



VDDIO(+1.5V) decoupling.



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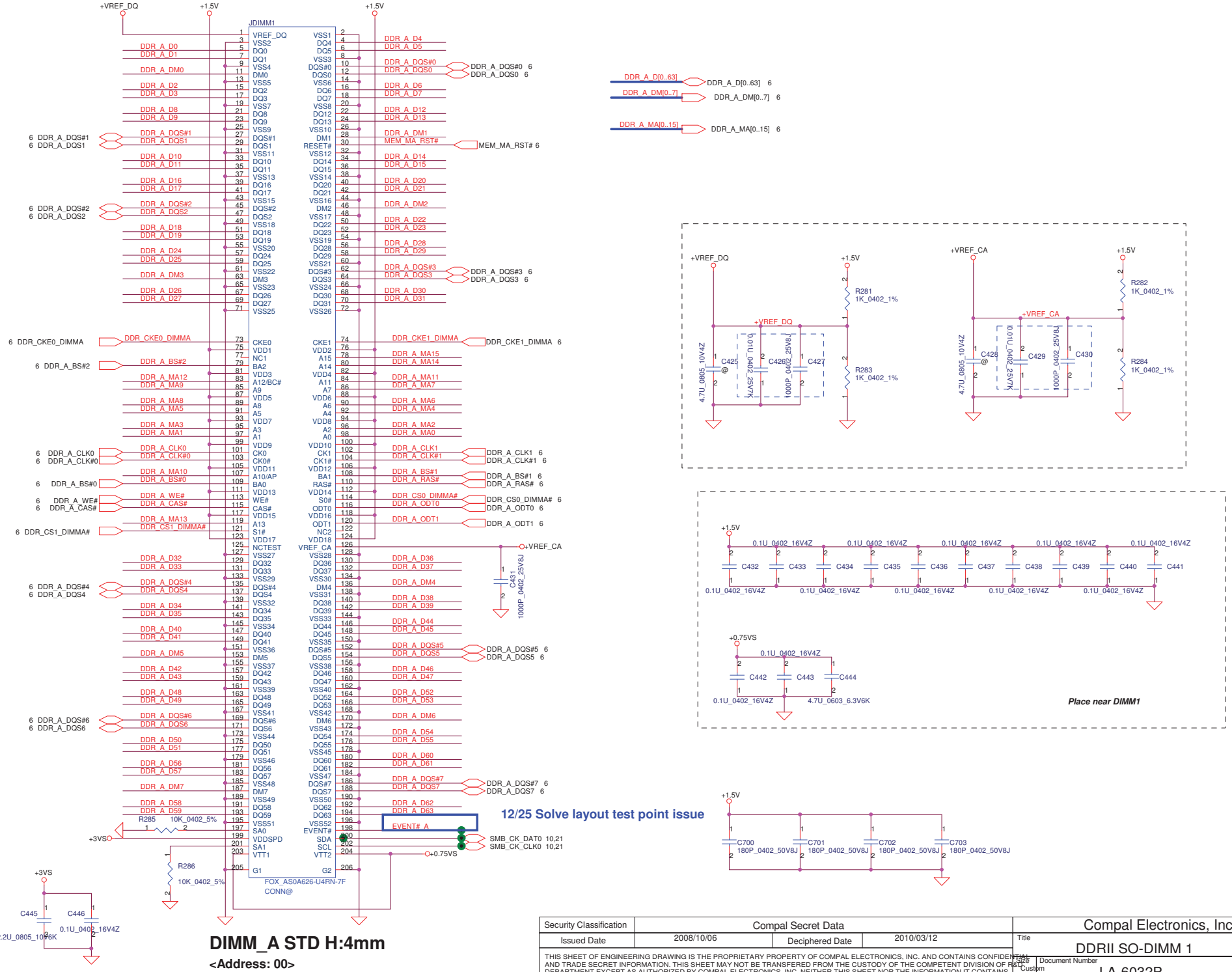
Compal Electronics, Inc.			
Title: AMD CPU S1G2 PWR & GND			
Size: C (Custom)	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 8 of 45		



DIMM_A STD H:4mm

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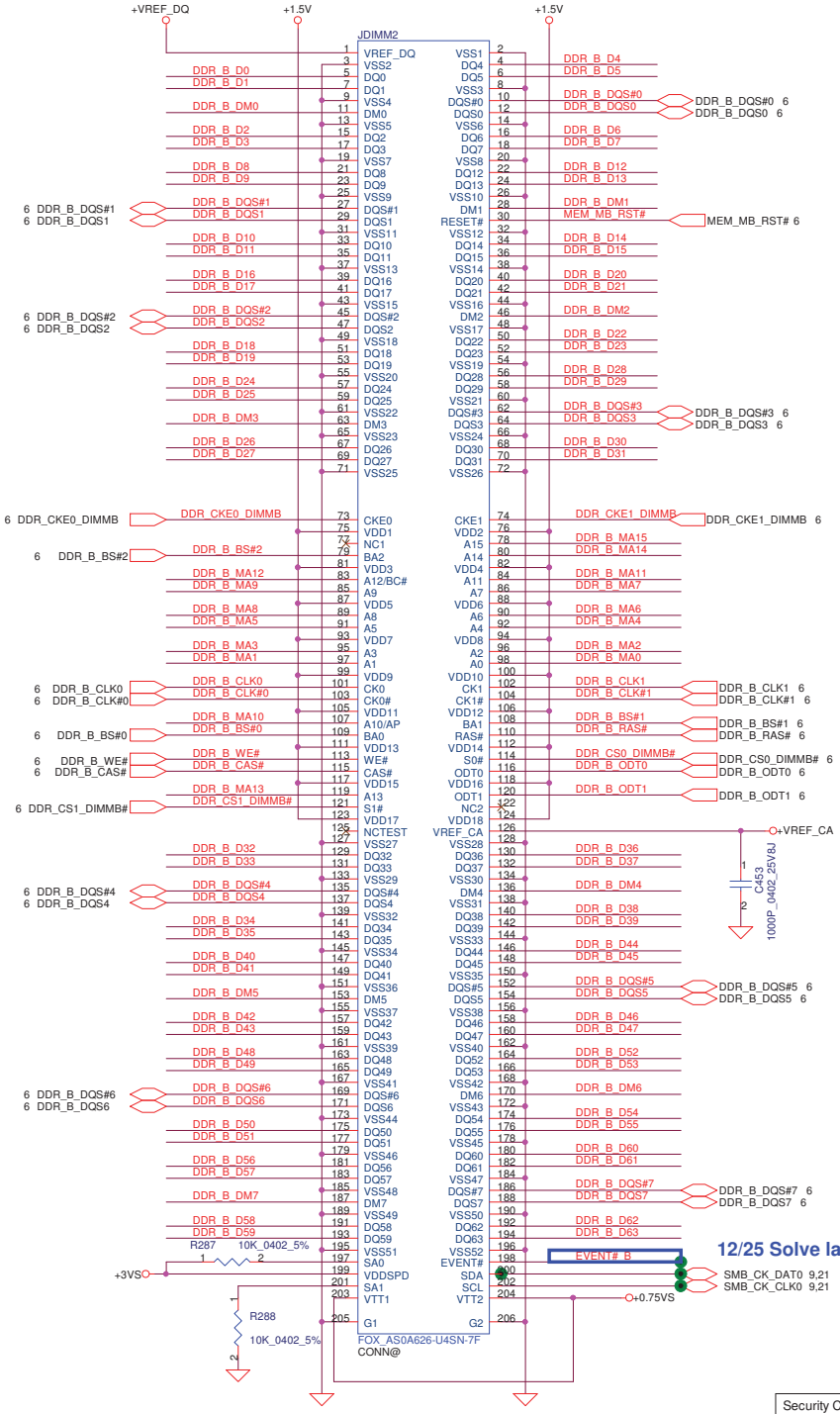
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

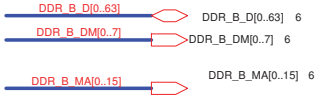
Compal Electronics, Inc.

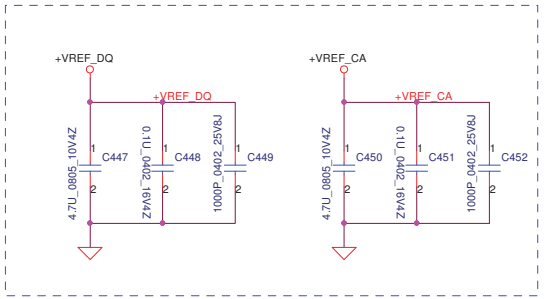
Title: DDRII SO-DIMM 1

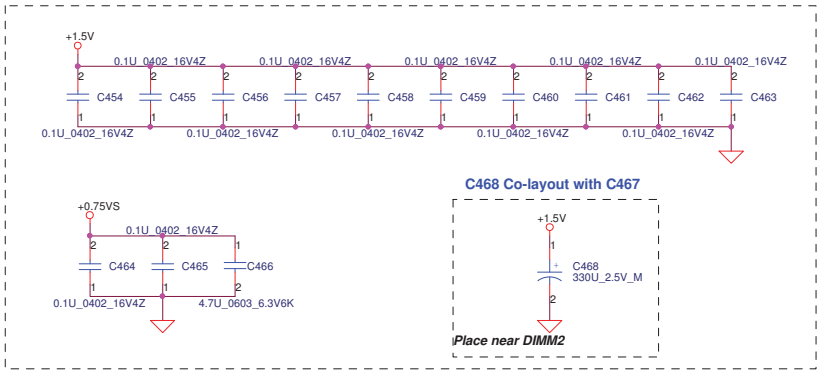
Size: B2B Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 9 of 45









DIMM_B STD H:4mm

<Address: 01>

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: DDRII SO-DIMM 2

Size: B28 Custom | Document Number: LA-6032P | Rev: 1.0

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U5B

PART 2 OF 6

PCIE I/F GFX

GFX_RX0P D4
GFX_RX0N C4
GFX_RX1P A3
GFX_RX1N B3
GFX_RX2P C2
GFX_RX2N C1
GFX_RX3P E5
GFX_RX3N F5
GFX_RX4P G5
GFX_RX4N G6
GFX_RX5P H5
GFX_RX5N H6
GFX_RX6P J6
GFX_RX6N J5
GFX_RX7P J7
GFX_RX7N J8
GFX_RX8P L5
GFX_RX8N L6
GFX_RX9P M8
GFX_RX9N L8
GFX_RX10P P7
GFX_RX10N M7
GFX_RX11P P5
GFX_RX11N M5
GFX_RX12P R8
GFX_RX12N P8
GFX_RX13P R6
GFX_RX13N R5
GFX_RX14P P4
GFX_RX14N P3
GFX_RX15P T4
GFX_RX15N T3

GFX_TX0P A5 HDMI_TXD2+
GFX_TX0N B5 HDMI_TXD2-
GFX_TX1P A4 HDMI_TXD1+
GFX_TX1N B4 HDMI_TXD1-
GFX_TX2P C3 HDMI_TXD0+
GFX_TX2N B2 HDMI_TXD0-
GFX_TX3P D1 HDMI_CLK0+
GFX_TX3N D2 HDMI_CLK0-
GFX_TX4P E2
GFX_TX4N E1
GFX_TX5P F4
GFX_TX5N F3
GFX_TX6P F1
GFX_TX6N F2
GFX_TX7P H4
GFX_TX7N H3
GFX_TX8P H1
GFX_TX8N H2
GFX_TX9P J2
GFX_TX9N J1
GFX_TX10P K4
GFX_TX10N K3
GFX_TX11P K1
GFX_TX11N K2
GFX_TX12P M4
GFX_TX12N M3
GFX_TX13P M1
GFX_TX13N M2
GFX_TX14P N2
GFX_TX14N N1
GFX_TX15P P1
GFX_TX15N P2

HDMI_TXD2+ 19
HDMI_TXD2- 19
HDMI_TXD1+ 19
HDMI_TXD1- 19
HDMI_TXD0+ 19
HDMI_TXD0- 19
HDMI_CLK0+ 19
HDMI_CLK0- 19

HDMI

< If integrated GFX is used, some PCIE pairs are used as HDMI signal pairs >

RS880M Display Port Support (muxed on GFX)

	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PCIE I/F GPP

GPP_RX0P AE3
GPP_RX0N AD4
GPP_RX1P AE2
GPP_RX1N AD3
GPP_RX2P AD1
GPP_RX2N AD2
GPP_RX3P V5
GPP_RX3N W6
GPP_RX4P U5
GPP_RX4N U6
GPP_RX5P U8
GPP_RX5N U7

GPP_TX0P AC1
GPP_TX0N AC2
GPP_TX1P AB4
GPP_TX1N AB3
GPP_TX2P AA2
GPP_TX2N AA1
GPP_TX3P Y1
GPP_TX3N Y2
GPP_TX4P Y4
GPP_TX4N Y3
GPP_TX5P V1
GPP_TX5N V2

30 PCIE_PTX_C_IRX_P1
30 PCIE_PTX_C_IRX_N1
26 PCIE_PTX_C_IRX_P2
26 PCIE_PTX_C_IRX_N2
27 PCIE_PTX_C_IRX_P3
27 PCIE_PTX_C_IRX_N3

PCIE_ITX_PRX_P1 C122 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_P1 30
PCIE_ITX_PRX_N1 C123 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_N1 30
PCIE_ITX_PRX_P2 C124 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_P2 26
PCIE_ITX_PRX_N2 C125 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_N2 26
PCIE_ITX_PRX_P3 C126 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_P3 27
PCIE_ITX_PRX_N3 C127 1 2 0.1U_0402_16V7K PCIE_ITX_C_PRX_N3 27

< To Card crader >
< To WLAN >
< To LAN >

< To Card crader >
< To WLAN >
< To LAN >

< To WWAN >

PCIE I/F SB

SB_RX0P AA8
SB_RX0N Y8
SB_RX1P AA7
SB_RX1N Y7
SB_RX2P AA5
SB_RX2N AA6
SB_RX3P W5
SB_RX3N Y5

SB_TX0P AD7
SB_TX0N AE7
SB_TX1P AE6
SB_TX1N AD6
SB_TX2P AB6
SB_TX2N AC6
SB_TX3P AD5
SB_TX3N AE5

20 SB_RX0P
20 SB_RX0N
20 SB_RX1P
20 SB_RX1N
20 SB_RX2P
20 SB_RX2N
20 SB_RX3P
20 SB_RX3N

SB_TX0P_C C130 1 2 0.1U_0402_16V7K SB_TX0P 20
SB_TX0N_C C131 1 2 0.1U_0402_16V7K SB_TX0N 20
SB_TX1P_C C132 1 2 0.1U_0402_16V7K SB_TX1P 20
SB_TX1N_C C133 1 2 0.1U_0402_16V7K SB_TX1N 20
SB_TX2P_C C134 1 2 0.1U_0402_16V7K SB_TX2P 20
SB_TX2N_C C135 1 2 0.1U_0402_16V7K SB_TX2N 20
SB_TX3P_C C136 1 2 0.1U_0402_16V7K SB_TX3P 20
SB_TX3N_C C137 1 2 0.1U_0402_16V7K SB_TX3N 20

< From SB820 : x4 PCIE A-link >

< To SB820 : x4 PCEI A-link>

< TX Impedance Calibration. Connect to GND >
< RX Impedance Calibration. Connect to VDDPCIE >

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

AC8 R51 1 2 1.27K_0402_1%
AB8 R54 1 2 2K_0402_1%
+1.1VS

RS880M_FCBGA528 RS880MR1@

R51 within U5 1"
R54 within U5 1"

U5A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

H_CADIP[0..15] H_CADIP[0..15] 5
H_CADIN[0..15] H_CADIN[0..15] 5

H_CADOP[0..15] H_CADOP[0..15] 5
H_CADON[0..15] H_CADON[0..15] 5

H_CADOP0 Y25
H_CADON0 Y24
H_CADOP1 V22
H_CADON1 V23
H_CADOP2 V25
H_CADON2 V24
H_CADOP3 U24
H_CADON3 U25
H_CADOP4 T25
H_CADON4 T24
H_CADOP5 P22
H_CADON5 P23
H_CADOP6 P25
H_CADON6 P24
H_CADOP7 N24
H_CADON7 N25
H_CADOP8 AC24
H_CADON8 AC25
H_CADOP9 AB25
H_CADON9 AB24
H_CADOP10 AA24
H_CADON10 AA25
H_CADOP11 Y22
H_CADON11 Y23
H_CADOP12 W21
H_CADON12 W20
H_CADOP13 V21
H_CADON13 V20
H_CADOP14 U20
H_CADON14 U21
H_CADOP15 U19
H_CADON15 U18

HT_RXCAD0P
HT_RXCAD0N
HT_RXCAD1P
HT_RXCAD1N
HT_RXCAD2P
HT_RXCAD2N
HT_RXCAD3P
HT_RXCAD3N
HT_RXCAD4P
HT_RXCAD4N
HT_RXCAD5P
HT_RXCAD5N
HT_RXCAD6P
HT_RXCAD6N
HT_RXCAD7P
HT_RXCAD7N
HT_RXCAD8P
HT_RXCAD8N
HT_RXCAD9P
HT_RXCAD9N
HT_RXCAD10P
HT_RXCAD10N
HT_RXCAD11P
HT_RXCAD11N
HT_RXCAD12P
HT_RXCAD12N
HT_RXCAD13P
HT_RXCAD13N
HT_RXCAD14P
HT_RXCAD14N
HT_RXCAD15P
HT_RXCAD15N

HT_TXCAD0P D24 H_CADIP0
HT_TXCAD0N D25 H_CADIN0
HT_TXCAD1P E24 H_CADIP1
HT_TXCAD1N E25 H_CADIN1
HT_TXCAD2P F24 H_CADIP2
HT_TXCAD2N F25 H_CADIN2
HT_TXCAD3P F23 H_CADIP3
HT_TXCAD3N F22 H_CADIN3
HT_TXCAD4P H23 H_CADIP4
HT_TXCAD4N H22 H_CADIN4
HT_TXCAD5P J25 H_CADIP5
HT_TXCAD5N J24 H_CADIN5
HT_TXCAD6P K24 H_CADIP6
HT_TXCAD6N K25 H_CADIN6
HT_TXCAD7P K23 H_CADIP7
HT_TXCAD7N K22 H_CADIN7
HT_TXCAD8P F21 H_CADIP8
HT_TXCAD8N G21 H_CADIN8
HT_TXCAD9P G20 H_CADIP9
HT_TXCAD9N H21 H_CADIN9
HT_TXCAD10P J20 H_CADIP10
HT_TXCAD10N J21 H_CADIN10
HT_TXCAD11P J18 H_CADIP11
HT_TXCAD11N K17 H_CADIN11
HT_TXCAD12P L19 H_CADIP12
HT_TXCAD12N J19 H_CADIN12
HT_TXCAD13P M19 H_CADIP13
HT_TXCAD13N L18 H_CADIN13
HT_TXCAD14P M21 H_CADIP14
HT_TXCAD14N P21 H_CADIN14
HT_TXCAD15P P18 H_CADIP15
HT_TXCAD15N M18 H_CADIN15

< From S1G4 CPU : x16 HT>

< To S1G4 CPU : x16 HT>

5 H_CLKOP0 H_CLKOP0 T22
5 H_CLKON0 H_CLKON0 T23
5 H_CLKOP1 H_CLKOP1 AB23
5 H_CLKON1 H_CLKON1 AA22

HT_RXCLK0P
HT_RXCLK0N
HT_RXCLK1P
HT_RXCLK1N

HT_TXCLK0P H24 H_CLKIP0
HT_TXCLK0N H25 H_CLKIN0
HT_TXCLK1P L21 H_CLKIP1
HT_TXCLK1N L20 H_CLKIN1

H_CLKIP0 5
H_CLKIN0 5
H_CLKIP1 5
H_CLKIN1 5

5 H_CTLOP0 H_CTLOP0 M22
5 H_CTLON0 H_CTLON0 M23
5 H_CTLOP1 H_CTLOP1 R21
5 H_CTLON1 H_CTLON1 R20

HT_RXCTL0P
HT_RXCTL0N
HT_RXCTL1P
HT_RXCTL1N

HT_TXCTL0P M24 H_CTLIP0
HT_TXCTL0N M25 H_CTLIN0
HT_TXCTL1P P19 H_CTLIP1
HT_TXCTL1N R18 H_CTLIN1

H_CTLIP0 5
H_CTLIN0 5
H_CTLIP1 5
H_CTLIN1 5

R52 1 2 301_0402_1% C23
A24

HT_RXCALP
HT_RXCALN

HT_TXCALP B24
HT_TXCALN B25

R53 1 2 301_0402_1%

RS880M_FCBGA528 RS880MR1@

Place within 1" layout 1:2

Place within 1" layout 1:2

Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: RS880M HT/PCIE

Size: Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 11 of 45

+AVDD1@125mA

Total +1.1VS_PLL@230mA

Total +1.8VS PLL@100mA

2/2 Fine tune pin define

12/07 Internal clock gen

+VDDLT18@220mA

If support VB, R780 R777->SMT, R776->@
If no support VB, R776-->SMT, R780 R777->@

PS:Need to fine tune R783 and R784 on Page17

Strap pin

CPU_LDT_REQ# Pull +1.8VS on page 20

Contact with NB signal

Contact to CRT conn signal

2/2 Add L41 L42 L43 C911 C912 C913 for EMI request

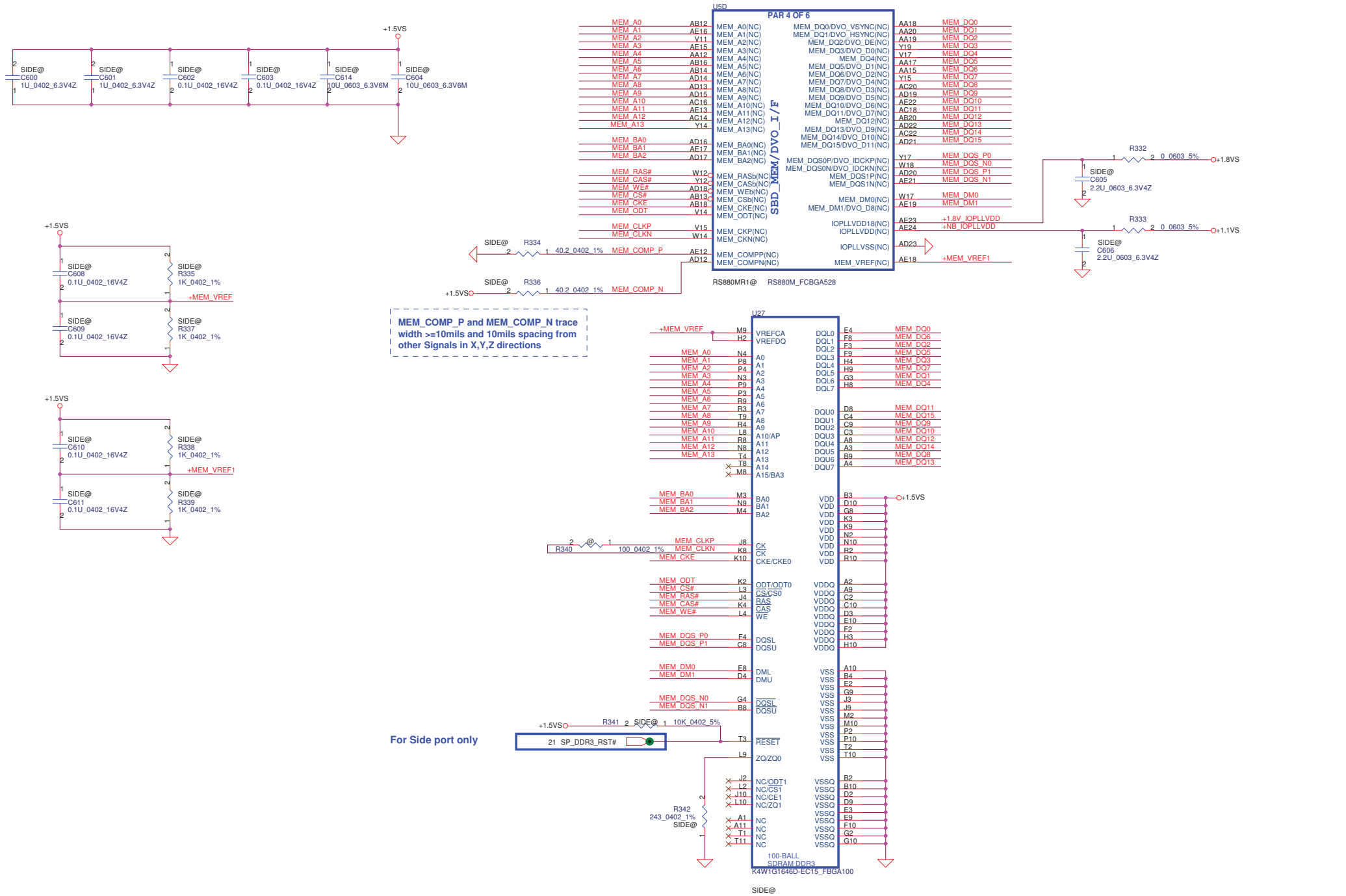
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: RS880M VEDIO/CLK GEN

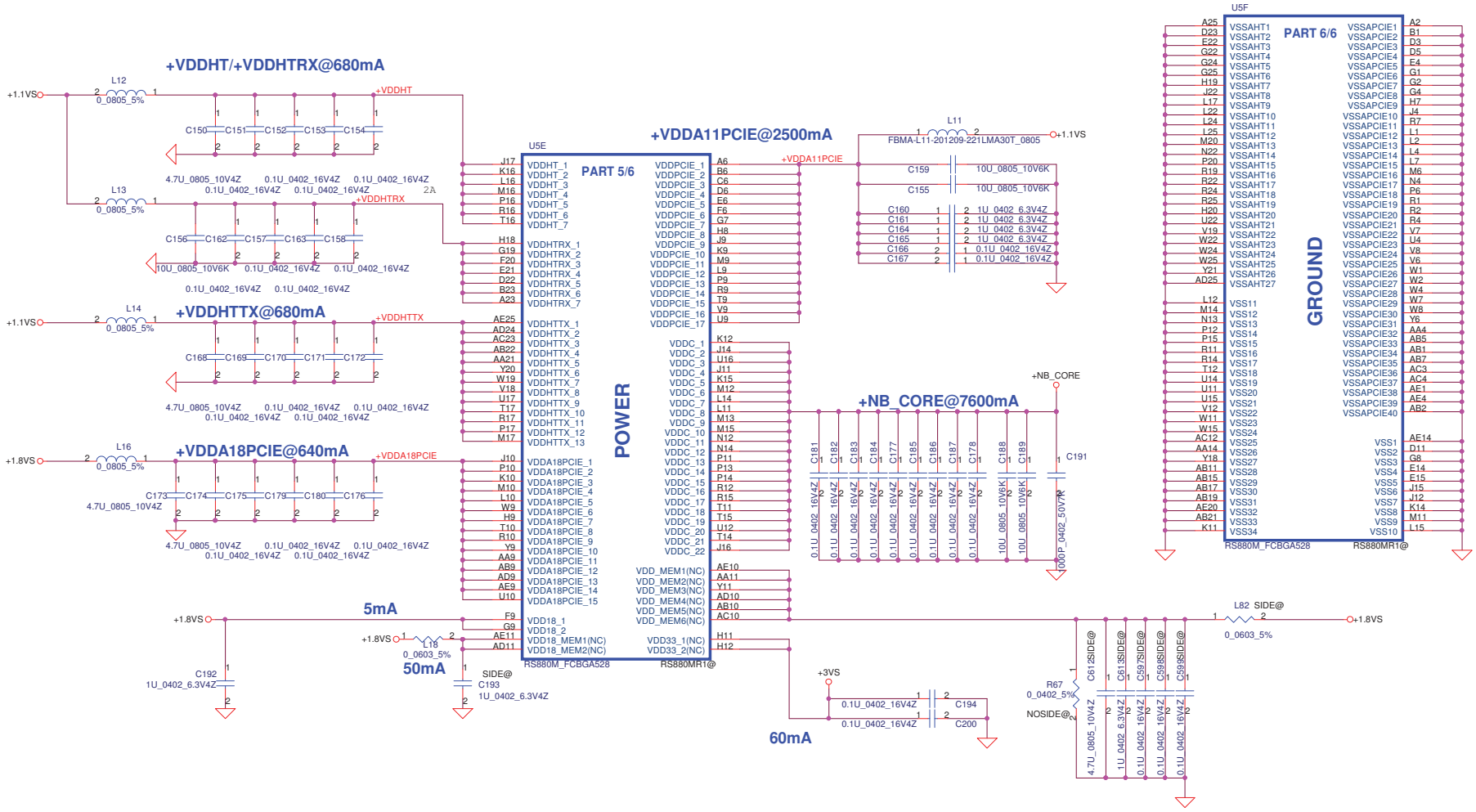
Size: B(28 Custom) | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 12 of 45



Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title: RS880M SIDE PORT			
Size: B(28 Custom)	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 13 of 45		



Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title: RS880MPWR/GND			
Size: Custom	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 14 of 45		

RS880 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K

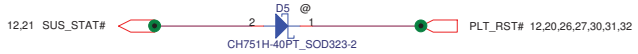
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (RS880)
0 : Enable (RS880)
PIN: RS880-->VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

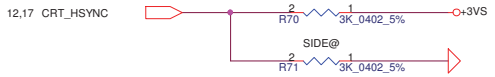
These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS880:SUS_STAT#

RS880 use HSYNC to enable SIDE PORT (internal pull high)



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX881: Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)

0 : Enable (RS880)

Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

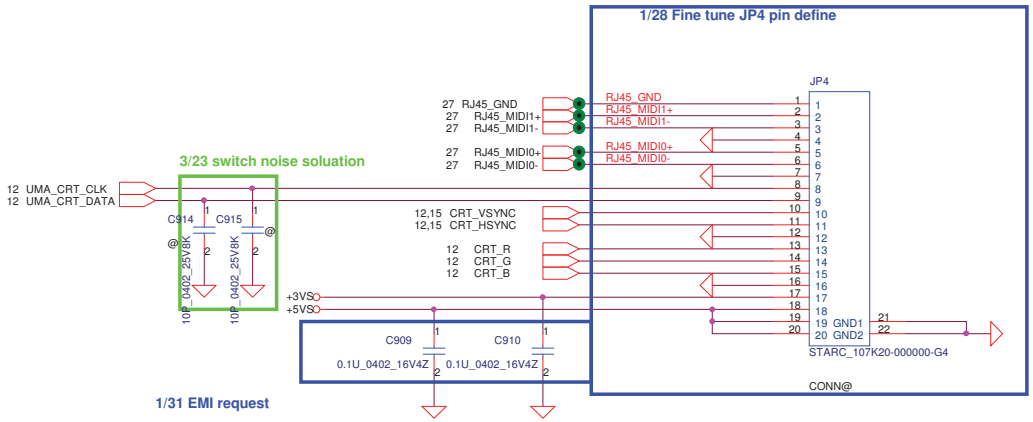
Title	*Compal Electronics, Inc.*	
	RS880M STRAPS	
Size: Custom	Document Number: *LA-6032P*	Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 15 of 45	

Use SB820M internal clock gen

Security Classification	Compal Secret Data		
Issued Date	2009-02-12	Deciphered Date	2009-02-12

Compal Electronics, Inc.			
Title	CLOCK GENERATOR		
Size: B/28 Custom	Document Number: LA-6051P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 16 of 45		

CRT+RJ45 FFC conn
Pin=20pin, pitch=0.5



Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

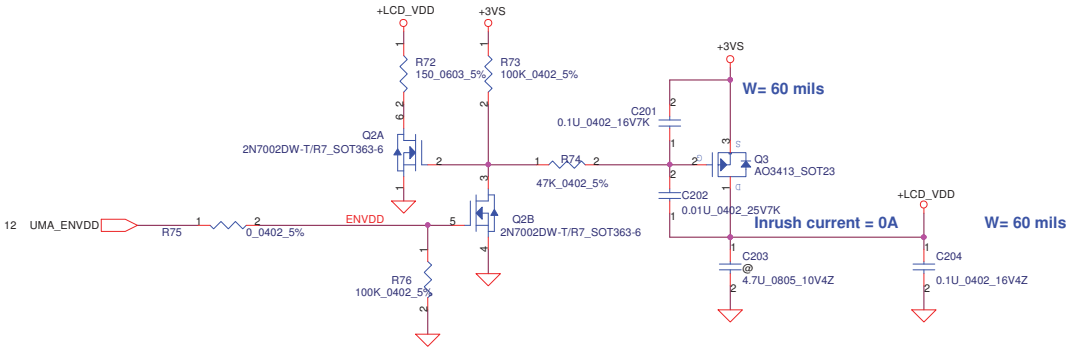
Compal Electronics, Inc.

Title: **CRT/TV-OUT Connector**

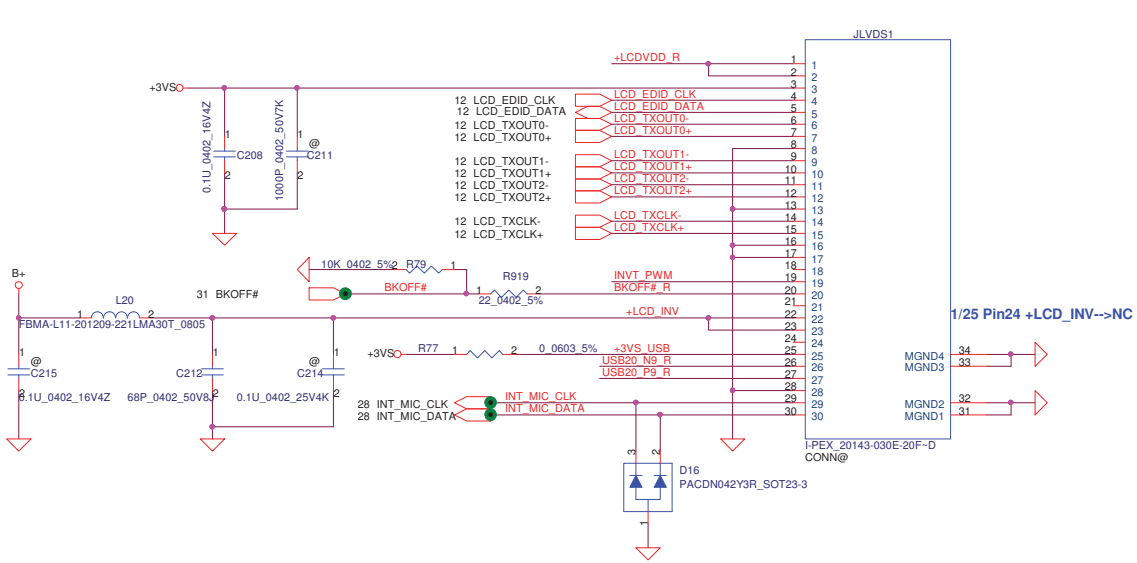
Size: Custom | Document Number: **LA-6032P** | Rev: 1.0

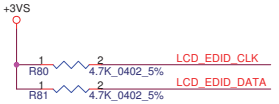
Date: Tuesday, March 23, 2010 | Sheet 17 of 45

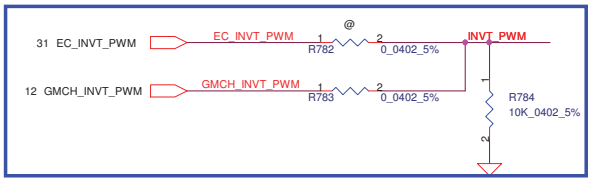
LCD/PANEL BD. Conn.



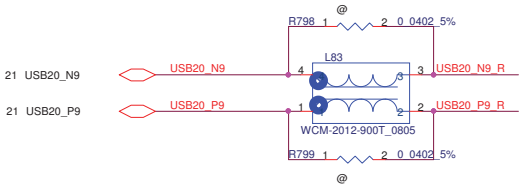
< LVDS Connector >

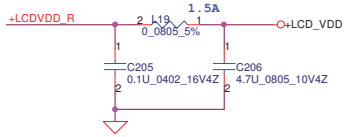






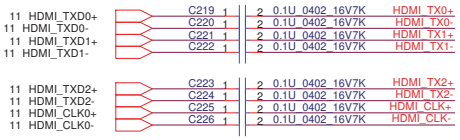
1/19 R782-->@ and R783/R784-->SMT for VB function

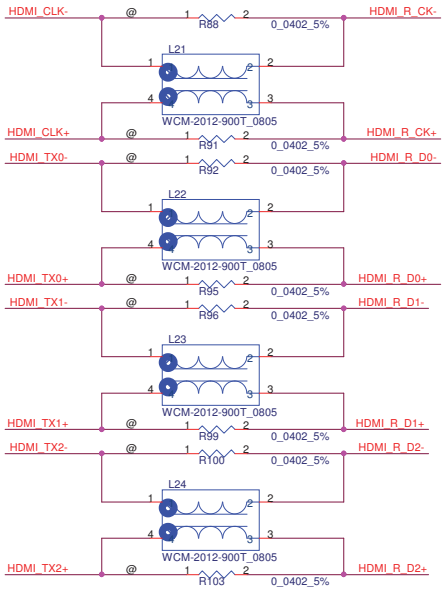


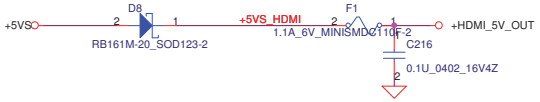


Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

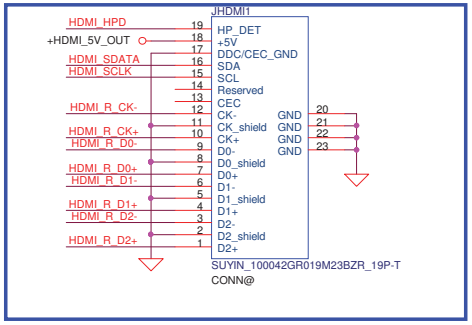
Compal Electronics, Inc.			
Title: LCD CONN.			
Size: C (28 Custom)	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 18 of 45		



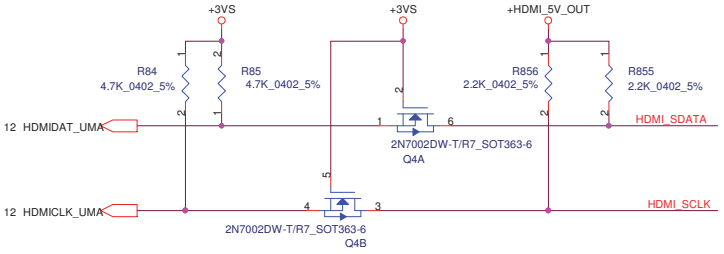


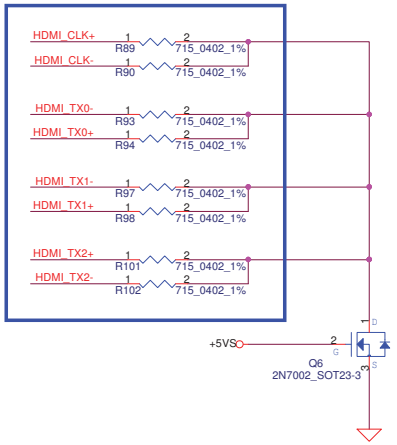


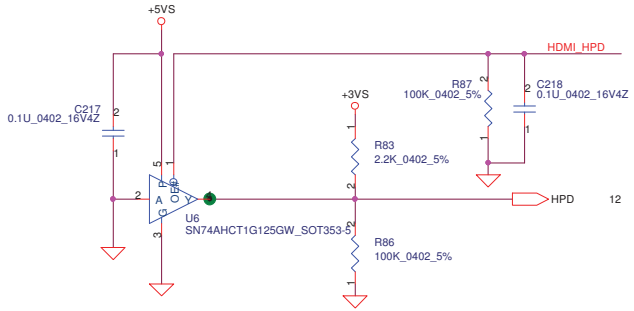
< HDMI Connector >



1/28 Update JHDMI1 footprint







Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: HDMI/CEC

Size: B/28 Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 19 of 45

SB800 Part 1 of 5

U7A

SB820M_FCBGA605

SB820MR1@

PCI CLKS

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

Close to SB within 1"

12/7 Add RS1~RS14 for internal clock gen

NB

NB

NB

CPU

LAN

WLAN

Card reader

2/8 GPIO35-->GPIO40 for 3G_OFF#

3/22 add RTCCLK to KBC 32.768

W=20mils W=20mils W=20mils

2/2 C240 C244 22P-->18P for RTC fail issue

level shift to ISL6265

ISL6265 PWROK input, TTL level: 0.8V~2.0V

When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high

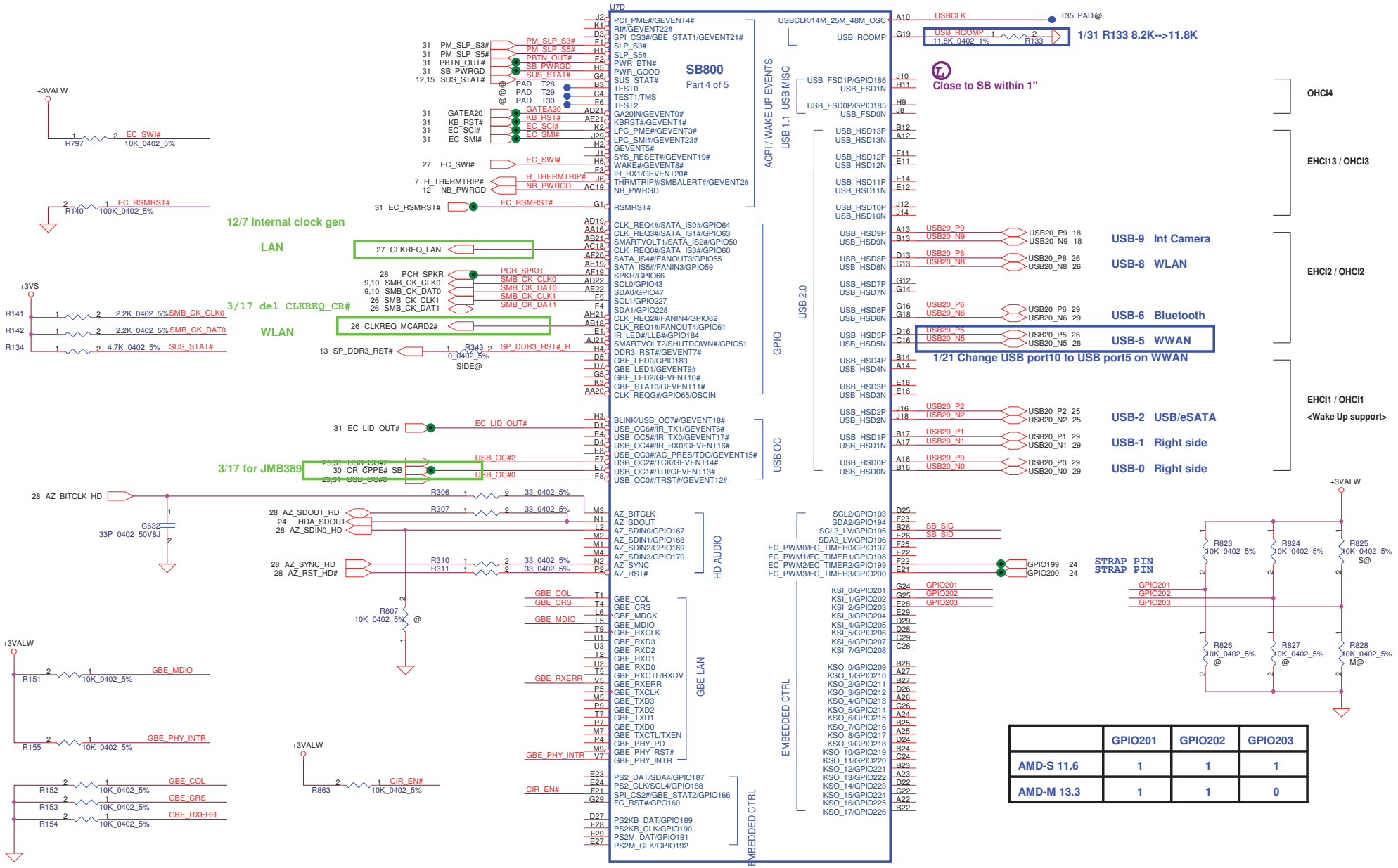
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: SB820-PCIE/PCI/ACPI/LPC/RTC

Size: Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 20 of 45



	GPIO201	GPIO202	GPIO203
AMD-S 11.6	1	1	1
AMD-M 13.3	1	1	0

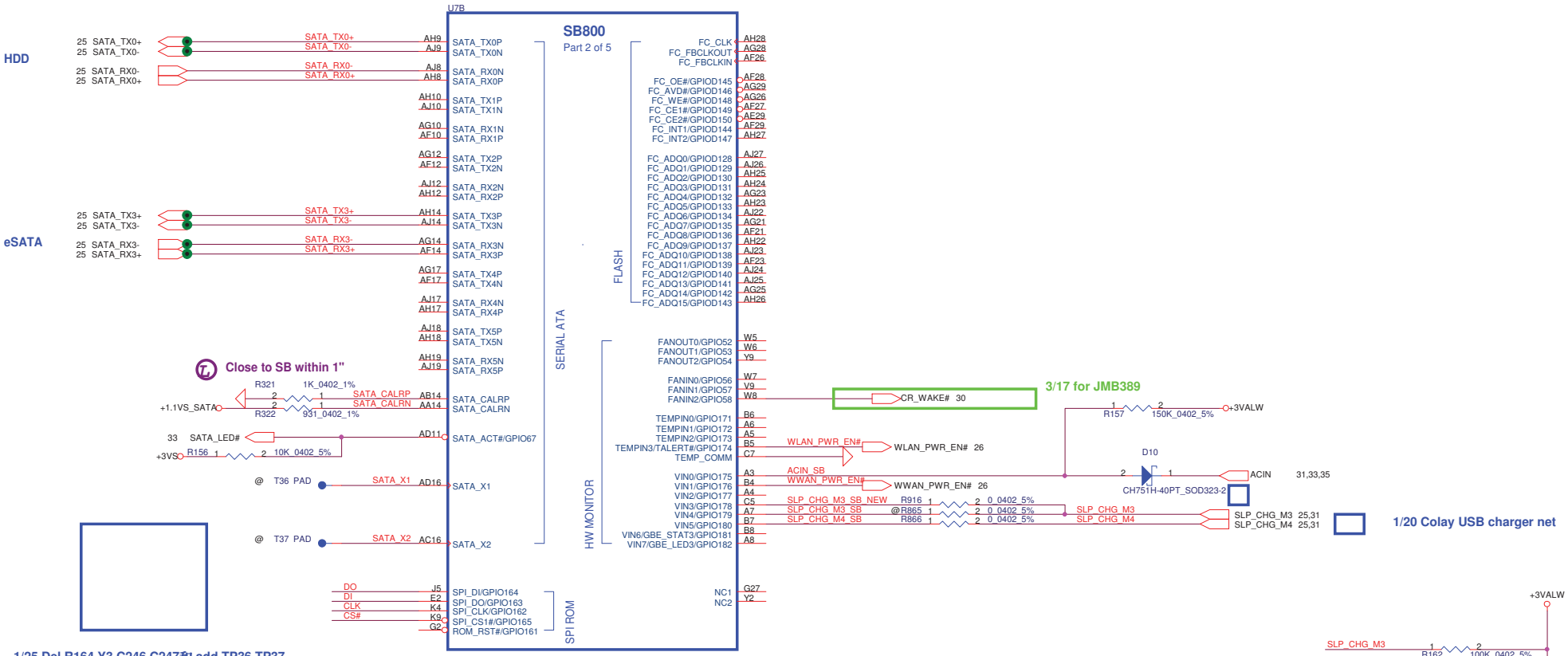
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

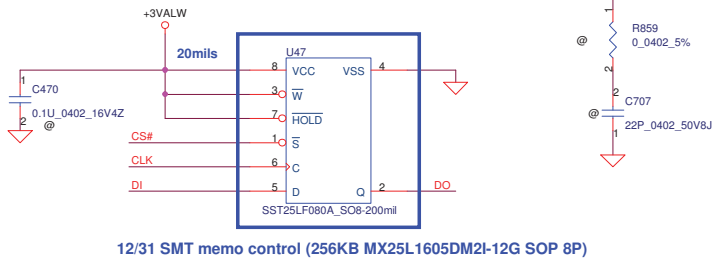
Compal Electronics, Inc.

Title: SB820 USB/HD Audio

Size: Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 21 of 45





12/31 SMT memo control (256KB MX25L1605DM2I-12G SOP 8P)

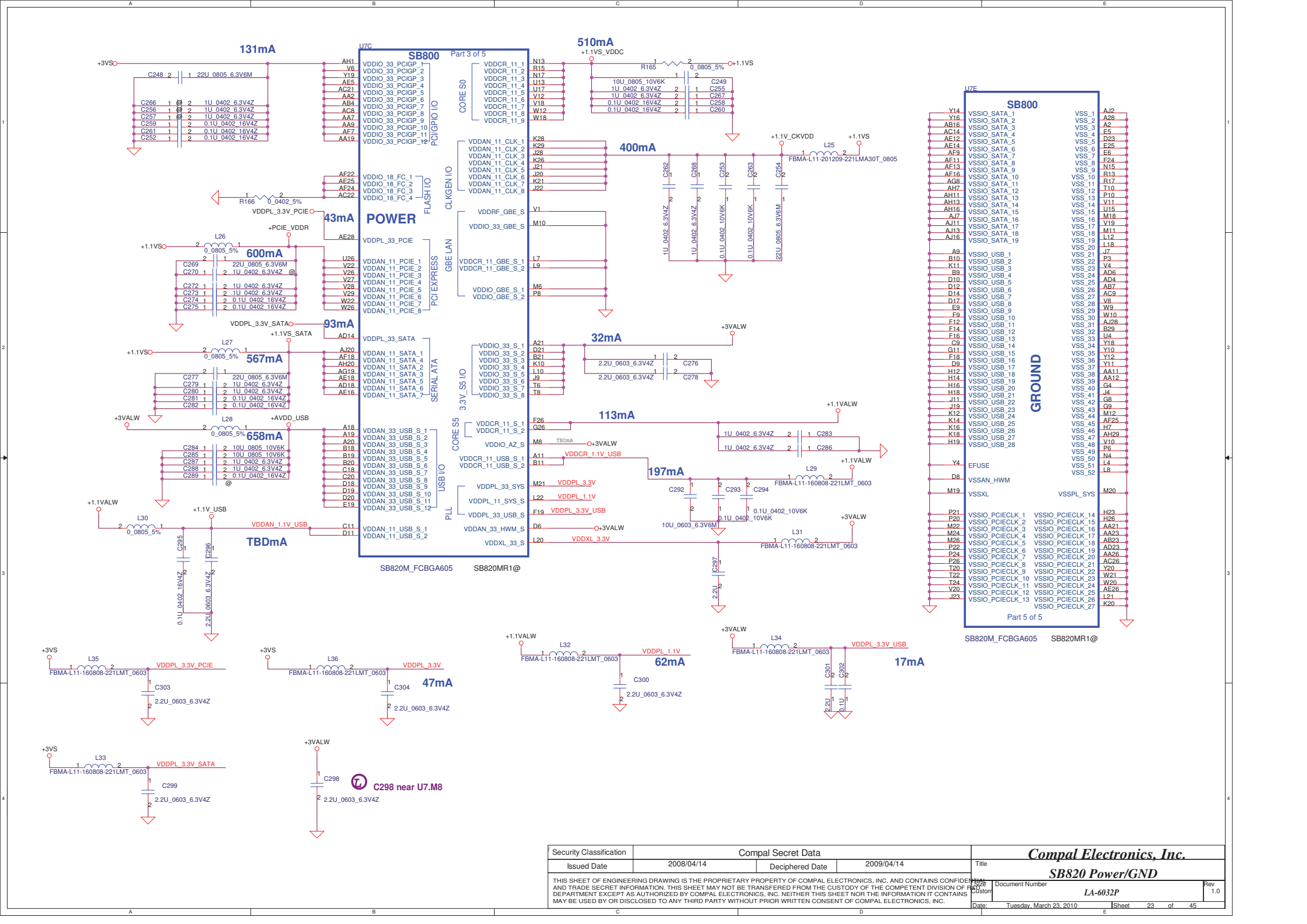
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: SB820 SATA/IDE/SPI

Size: Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 22 of 45



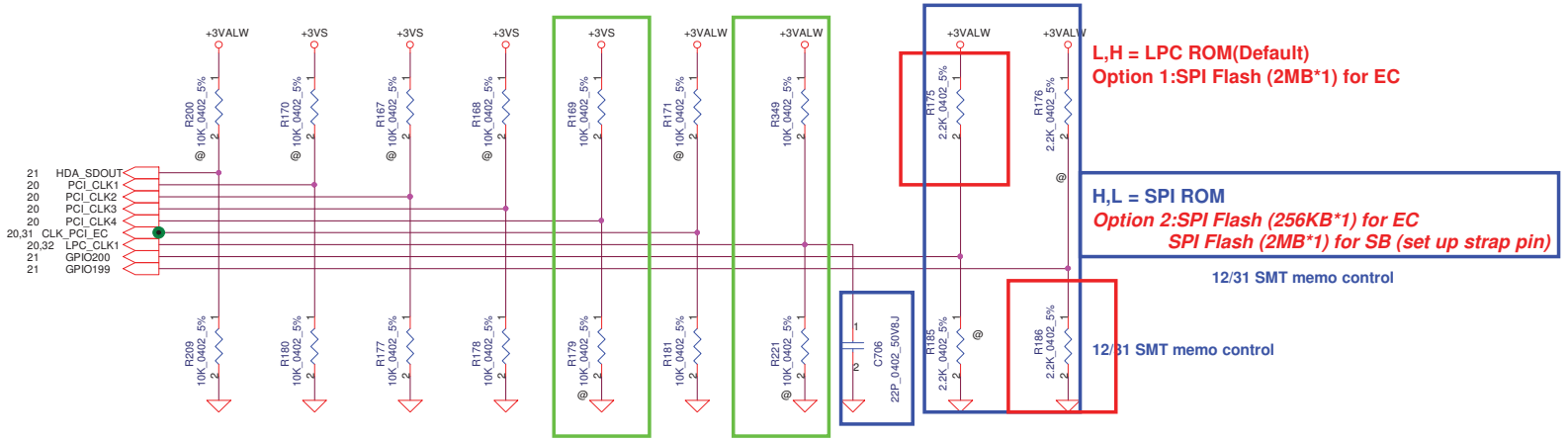
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Title	Compal Electronics, Inc.		
	SB820 Power/GND		
Size: Custom	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 23 of 45		

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1	GPIO200 (EC_PWM3) GPIO199 (EC_PWM2)
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT	H,H = Reserved H,L = SPI ROM(Default)
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE	L,H = LPC ROM L,L = FWH ROM



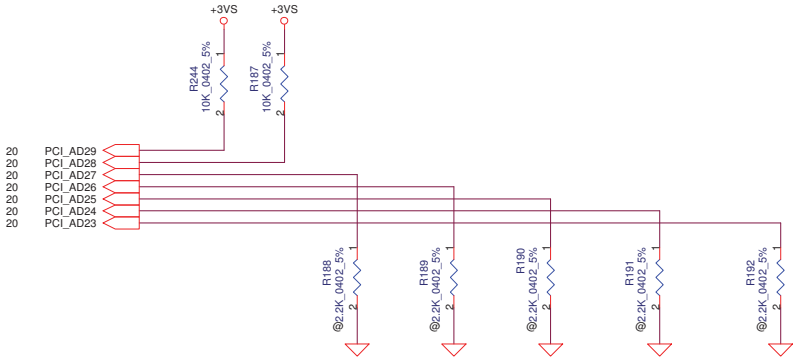
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

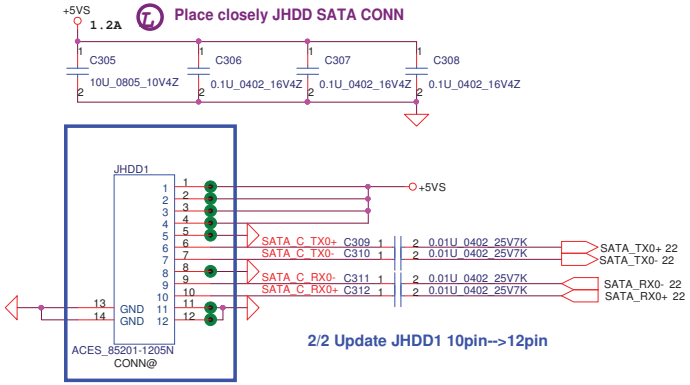
Check AD29,AD28 strap function

check default



Compal Electronics, Inc.			
Title	SB820 STRAPS		
Size: C Custom	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 24 of 45		

SATA transfer board

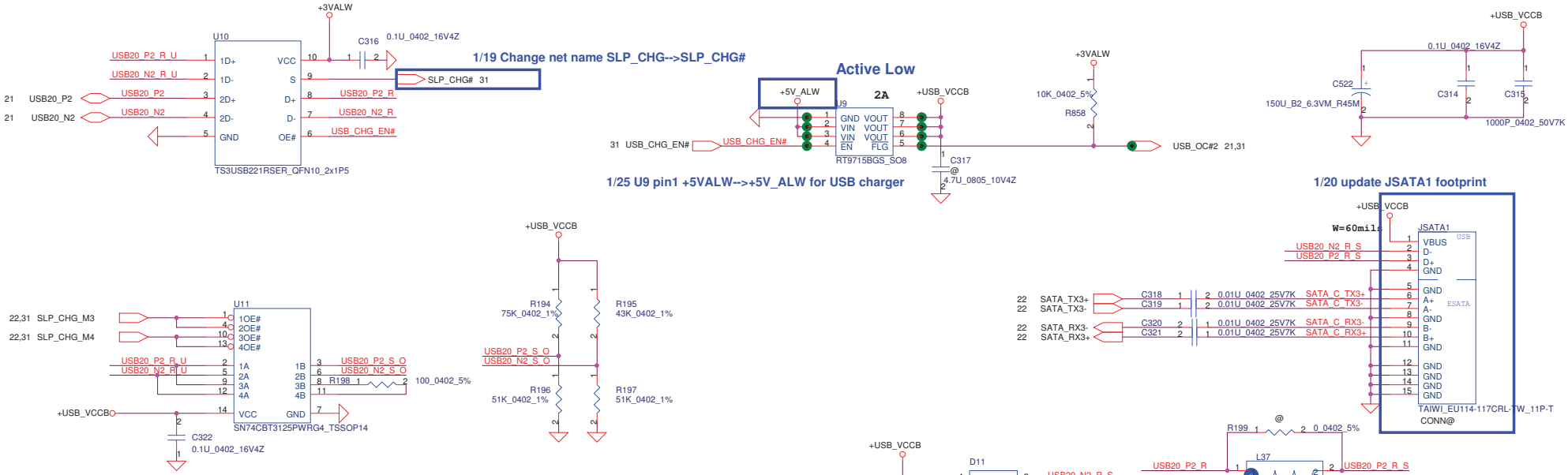


2/2 Update JHDD1 10pin-->12pin

03/11 Del JHDD2

SATA FFC conn
Pin=12pin, pitch=1.0

E-SATA/USB



	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

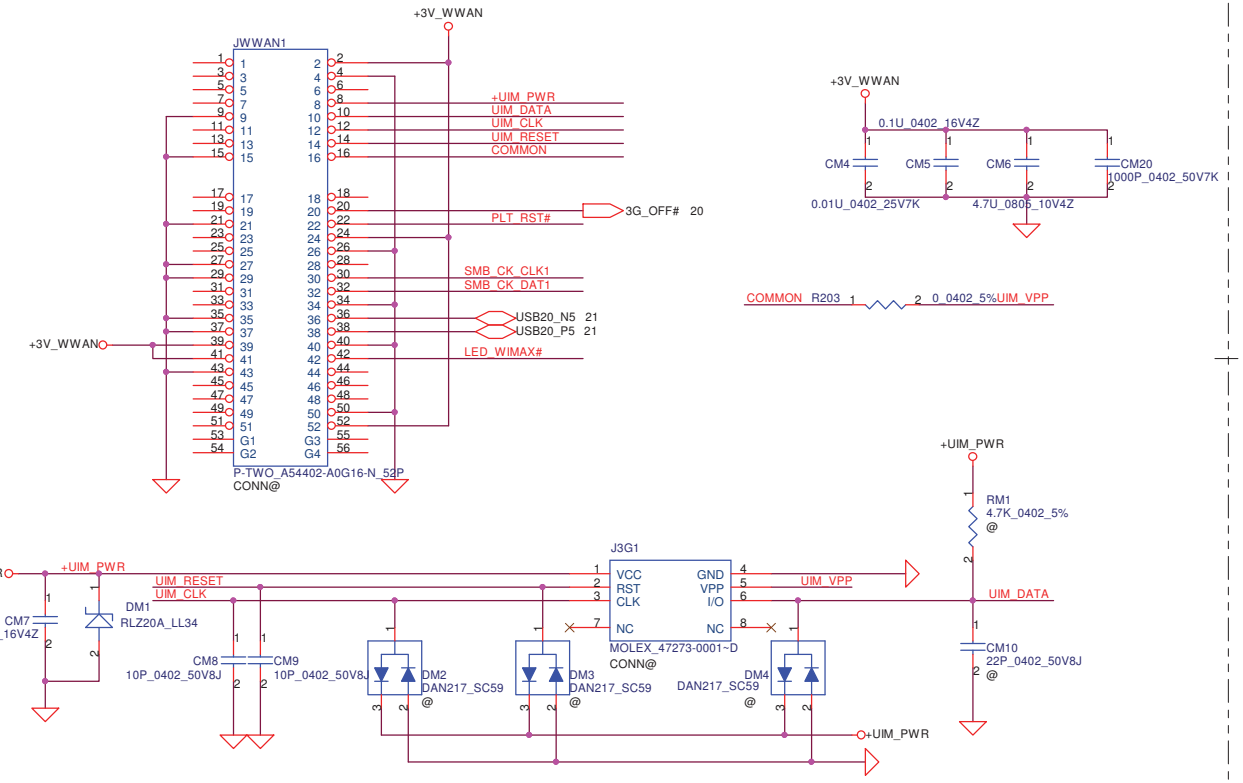
Compal Electronics, Inc.

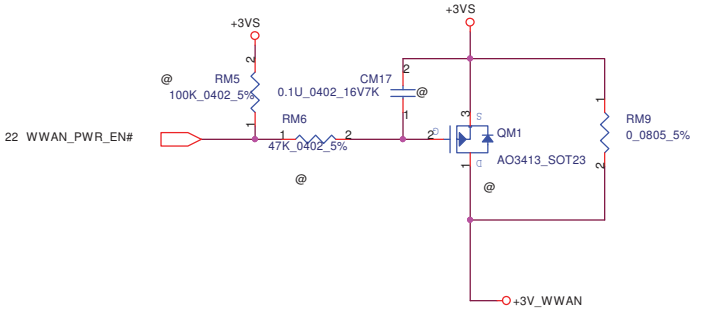
Title: SATA HDD/ODD

Size: Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 25 of 45

PCIe Mini Card-3G/WWAN (Slot 2)

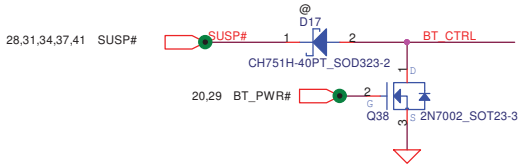




WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

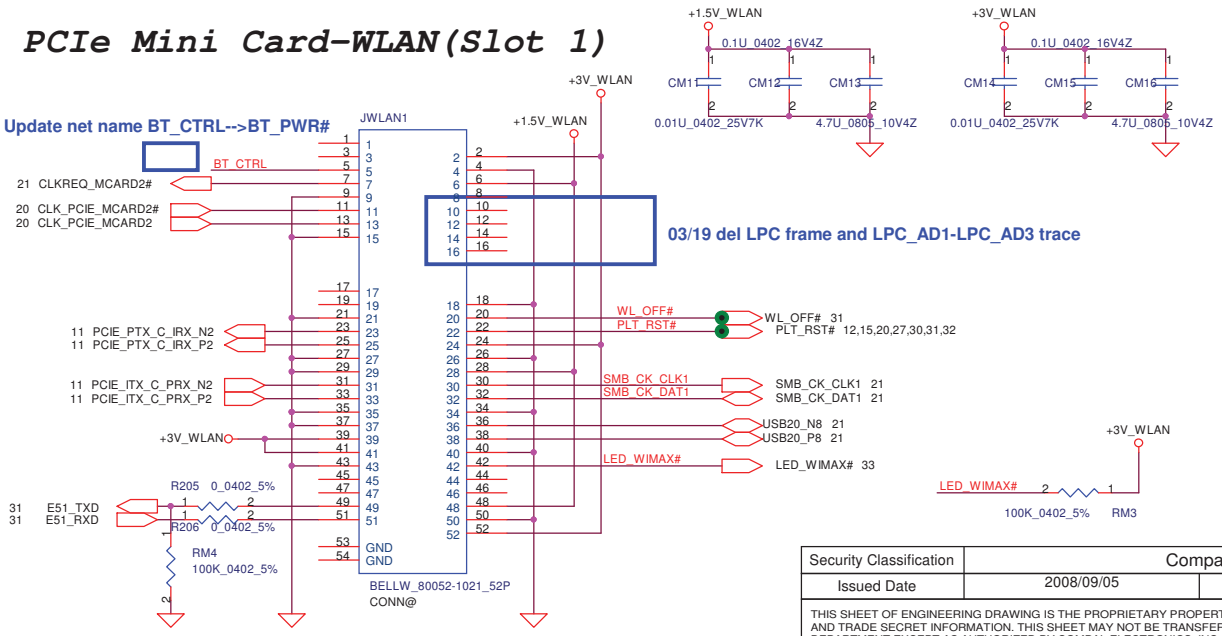
**If +3V_WLAN is +3VS, please remove D17.



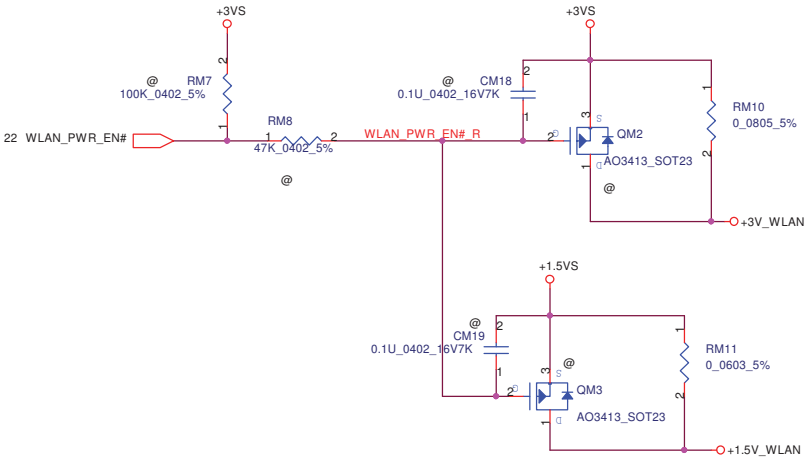
01/21 Add D17 and Q38 for BT control

PCIe Mini Card-WLAN(Slot 1)

01/19 Update net name BT_CTRL-->BT_PWR#



03/19 del LPC frame and LPC_AD1-LPC_AD3 trace



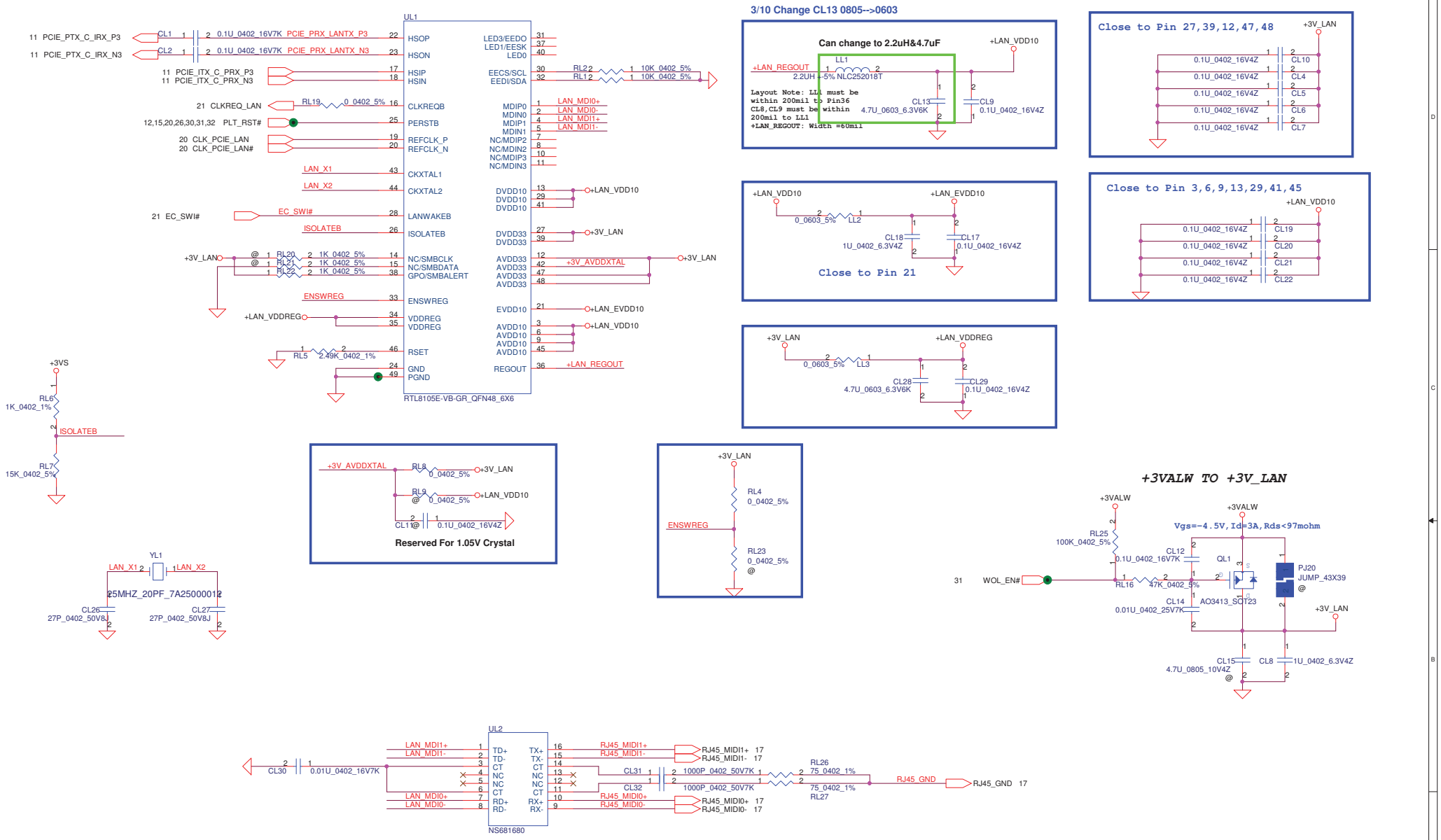
Security Classification	Compal Secret Data		
Issued Date	2008/09/05	Deciphered Date	2009/09/05

Compal Electronics, Inc.

Title: PCIe-WLAN/HDDVD/NAND/NEW

Size	Document Number	Rev
	LA-6032P	1.0

Date: Tuesday, March 23, 2010 Sheet 26 of 45



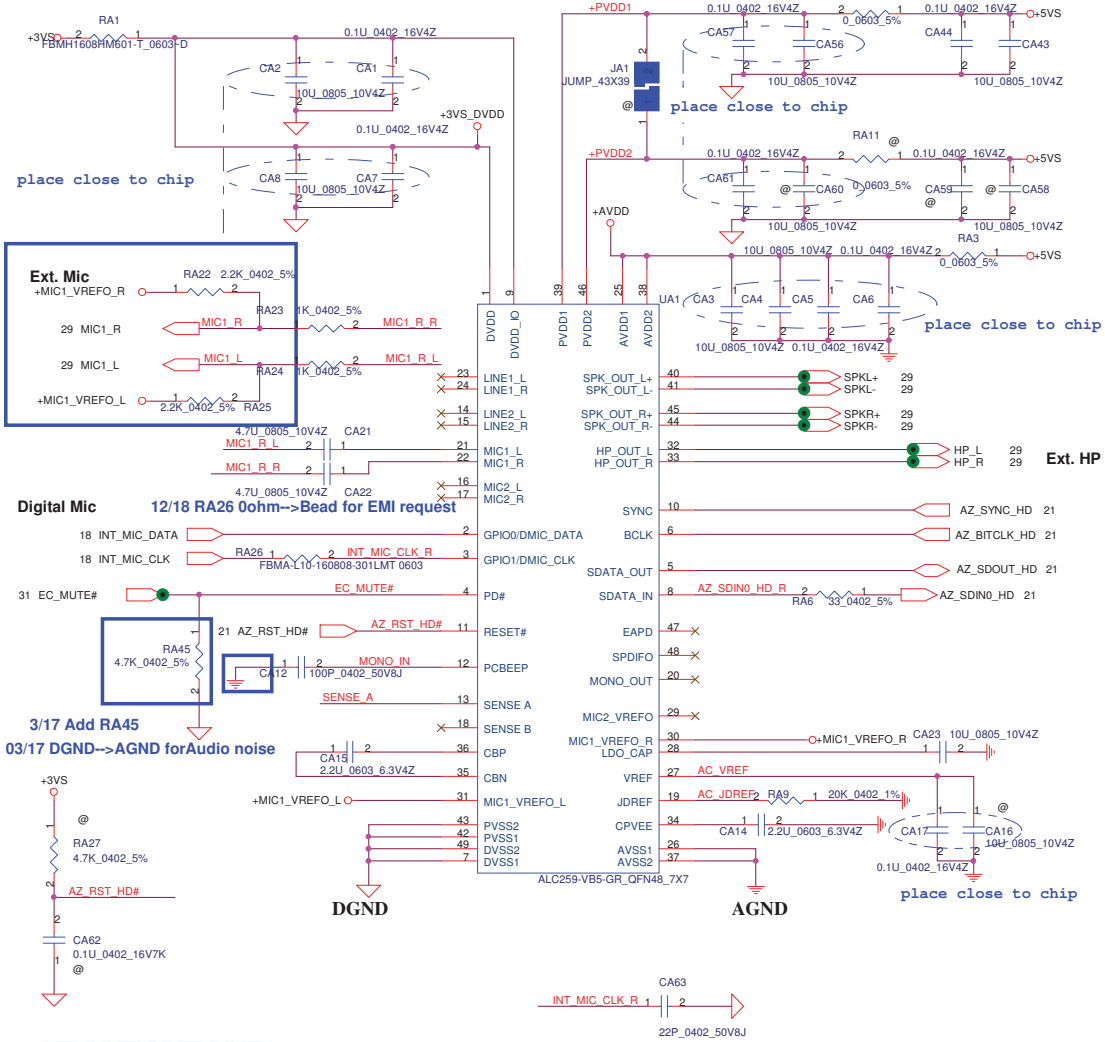
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

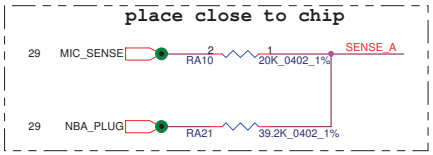
Title: RTL8103EL/RTL8111DL

Size: B2B | Document Number: LA-6032P | Rev: 1.0

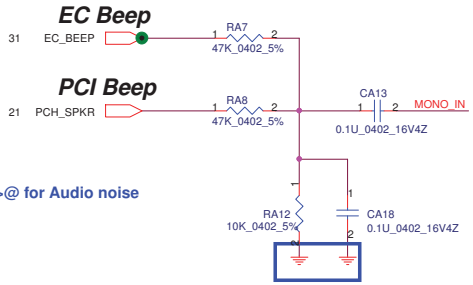
Date: Tuesday, March 23, 2010 | Sheet 27 of 45

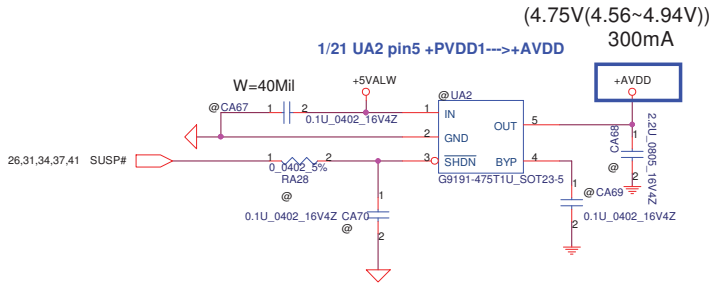


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



Beep sound



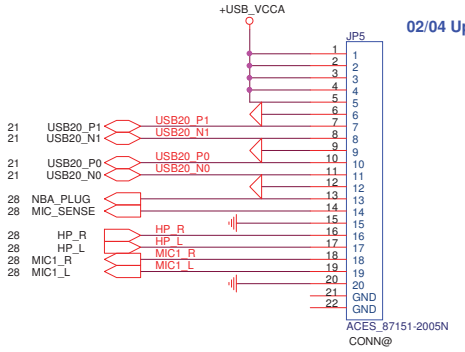


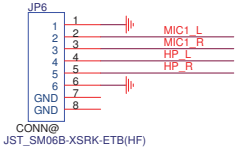
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title: HD Audio ALC272 Codec			
Size: B/28 Custom	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 28 of 45		

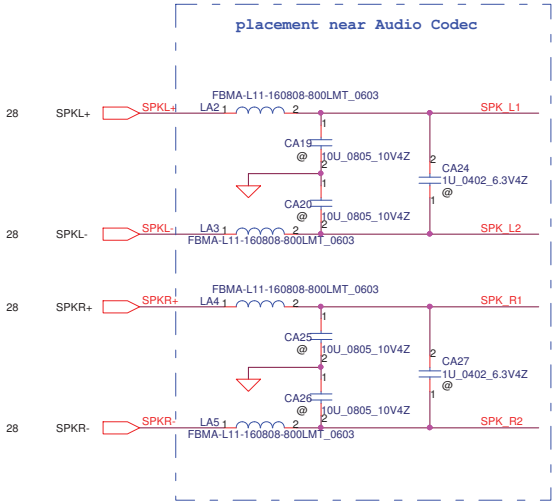
USB+Audio FFC conn
Pin=20pin, pitch=0.5

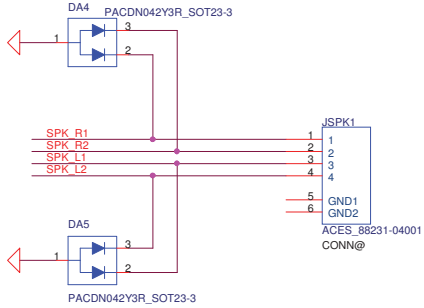
02/04 Update JP5 pin define

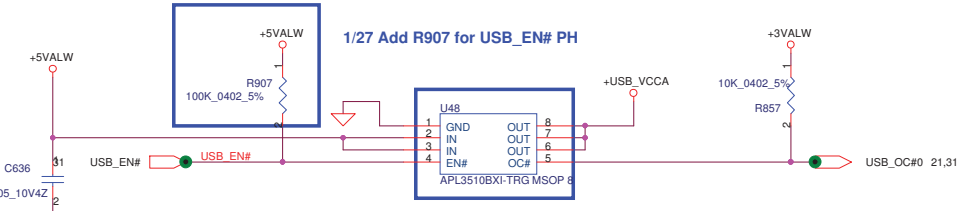




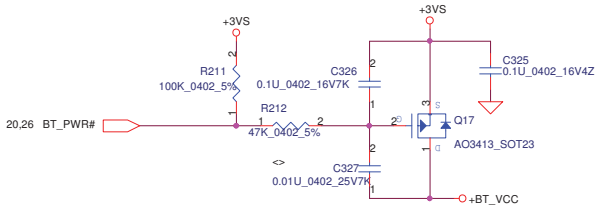
Speaker Connector



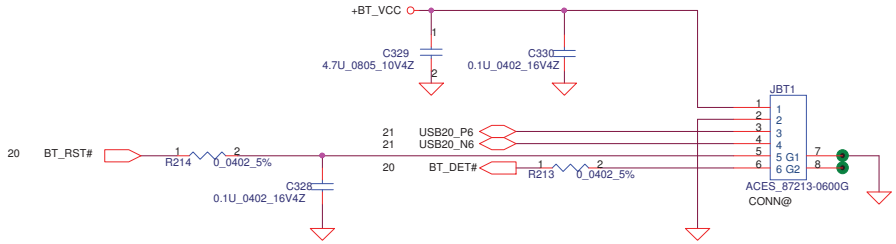




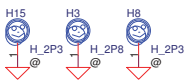
BlueTooth Interface



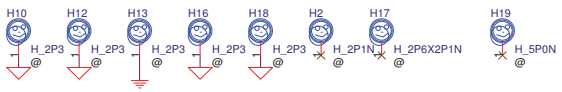
(MAX=200mA)

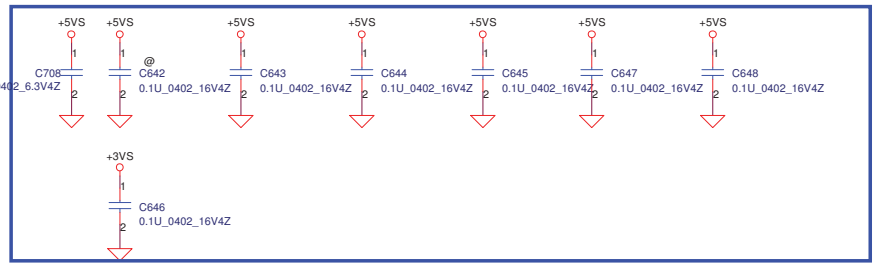


Screw Hole



CPU





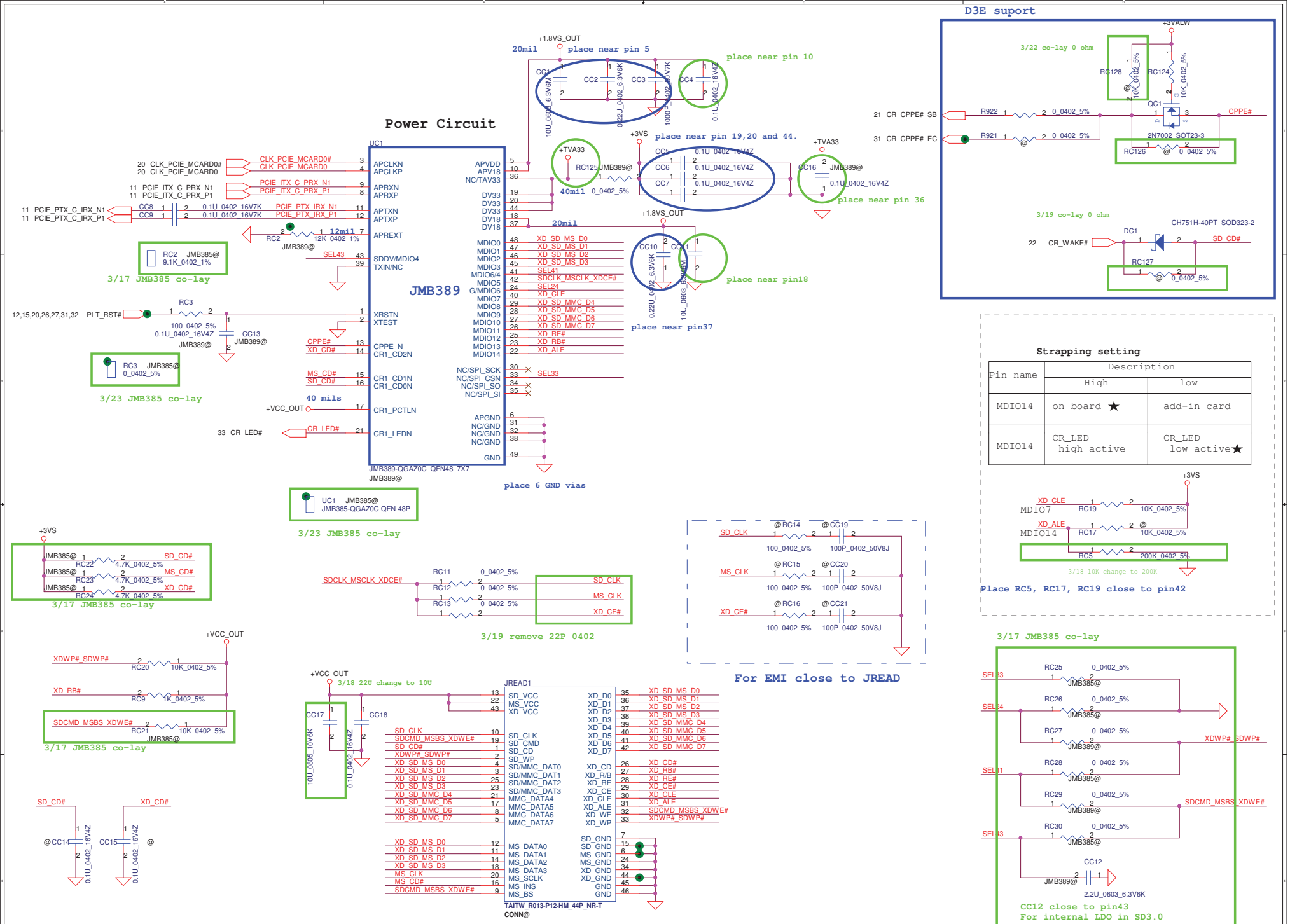
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.

Title: AMP/Audio Jack/HP/SPEAKER/VR

Size: B/A3 Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 29 of 45



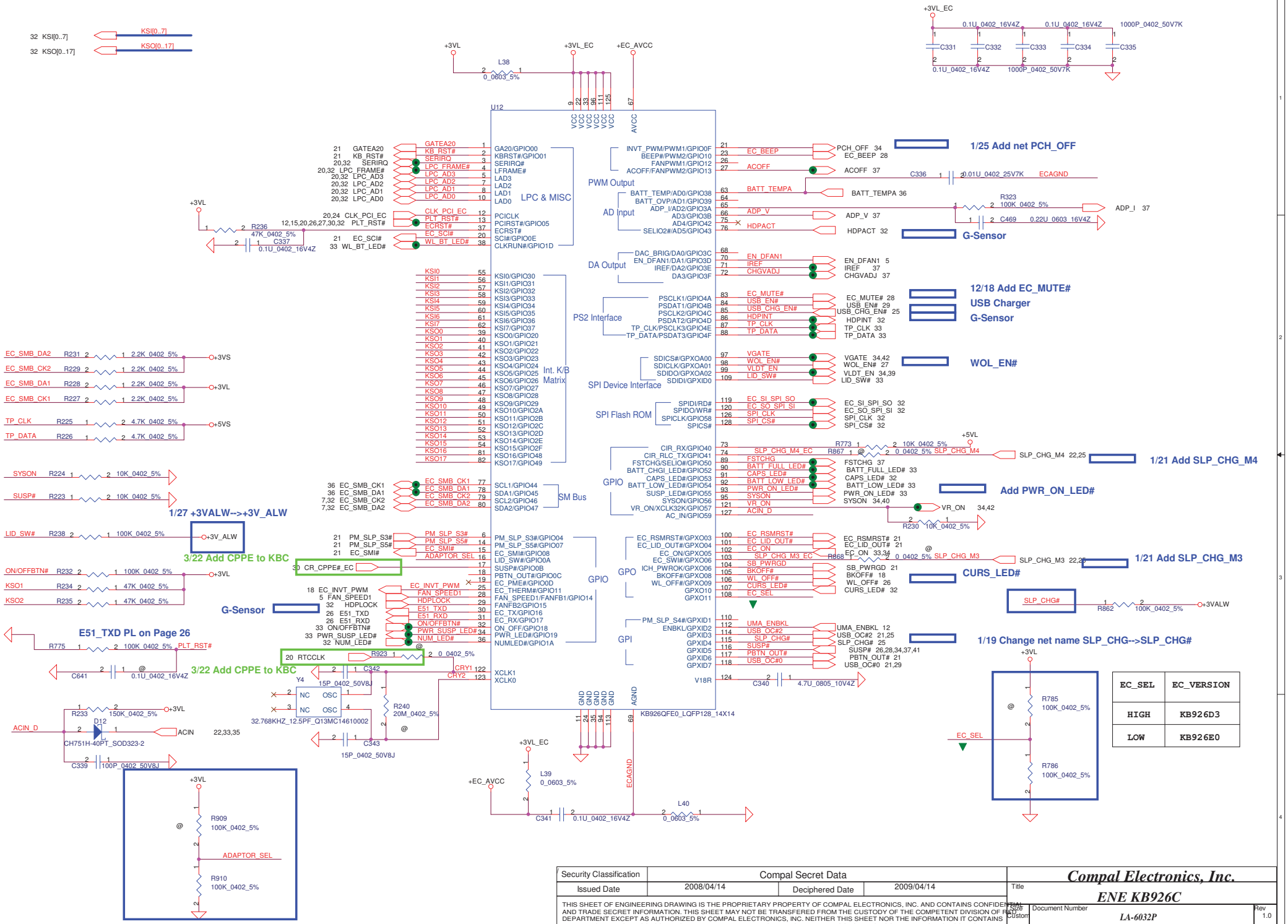
Security Classification	Compal Secret Data		
Issued Date	2010/01/22	Deciphered Date	2011/01/22

Compal Electronics, Inc.

Title: Card Reader JMB389

Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, March 23, 2010 | Sheet 30 of 45



Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

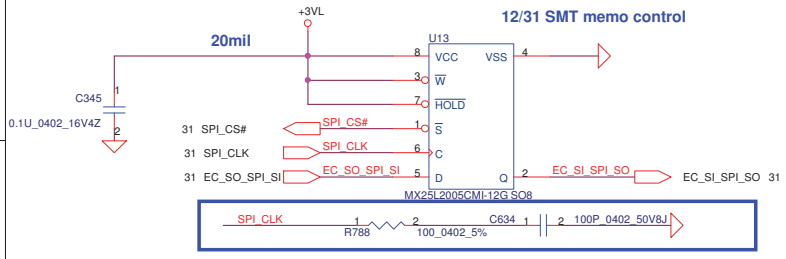
Compal Electronics, Inc.			
Title: ENE KB926C			
Size: Custom	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 31 of 45		

Option 1:SPI Flash (2MB*1) for EC

Option 2:SPI Flash (256KB*1) for EC
SPI Flash (2MB*1) for SB (set up strap pin)

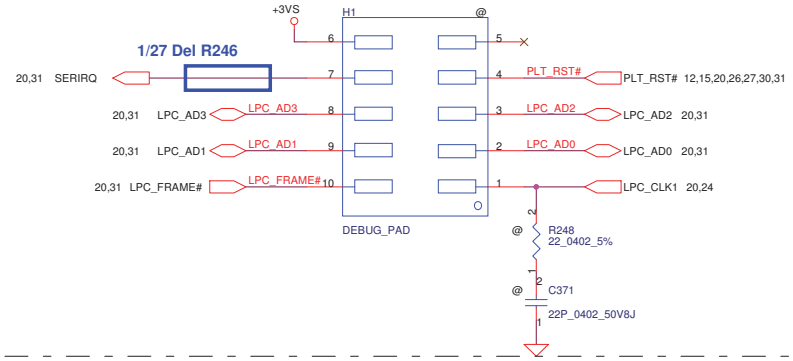
12/31 SMT memo control

SPI Socket: SP07000F500 & SP07000H900
2MB P/N:MXIC SA00002TO00 S IC FL 16M MX25L1605DM2I-12G SOP 8P ROM
256KB P/N:MXIC SA00003GK00 S IC FL 2M MX25L2005CMI-12G SOP 8P

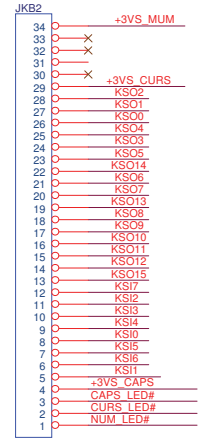


12/18 <BOM>R788 @-->100ohm and C634 @-->100P for RF request

LPC Debug Port (Please place the PAD under DDR DIMM)

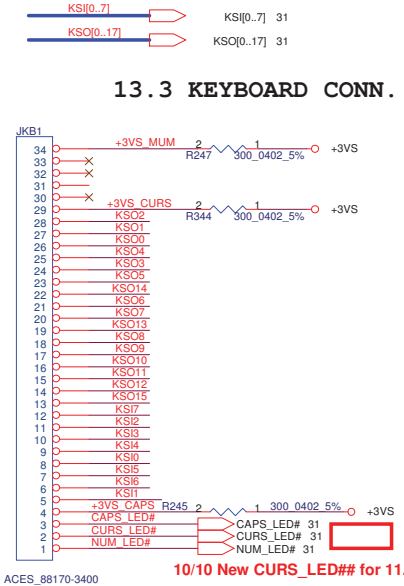


11.6 KEYBOARD CONN.

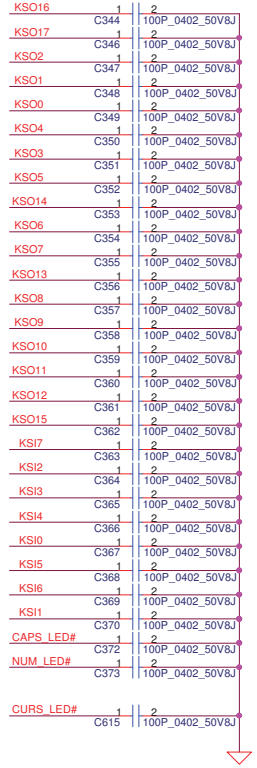


New keyboard

13.3 KEYBOARD CONN.

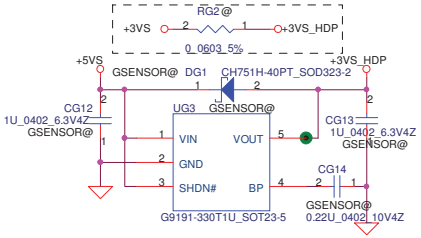


10/10 New CURS_LED## for 11.3&13.6

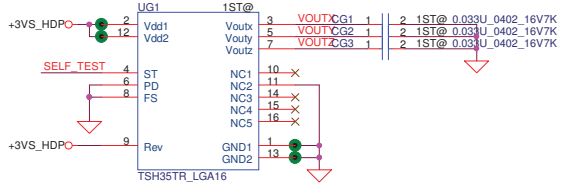


10/10 New CURS_LED# cap for 11.3&13.6

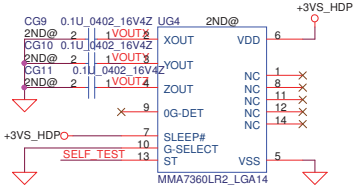
G-Sensor

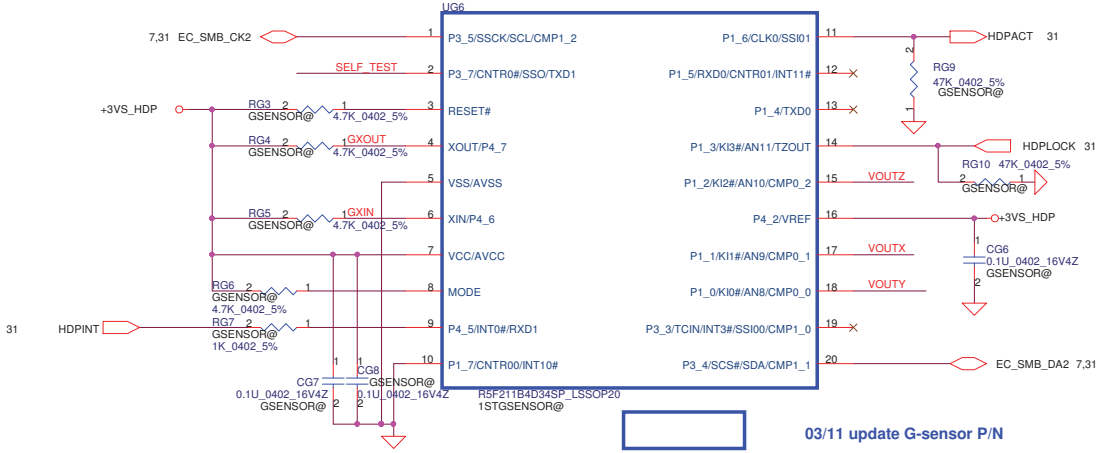


Change U55 to G9191-330T1U



Reserve Freescale



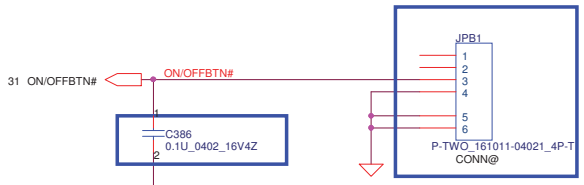


03/11 update G-sensor P/N

Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

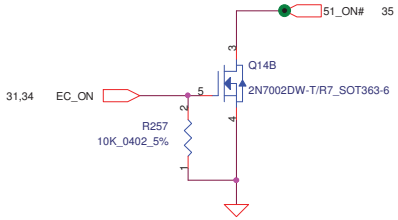
Compal Electronics, Inc.			
Title: SPI/LPC/PS2/MDC/FM/CIR			
Size: Custom	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 32 of 45		

Power Button & Lid switch



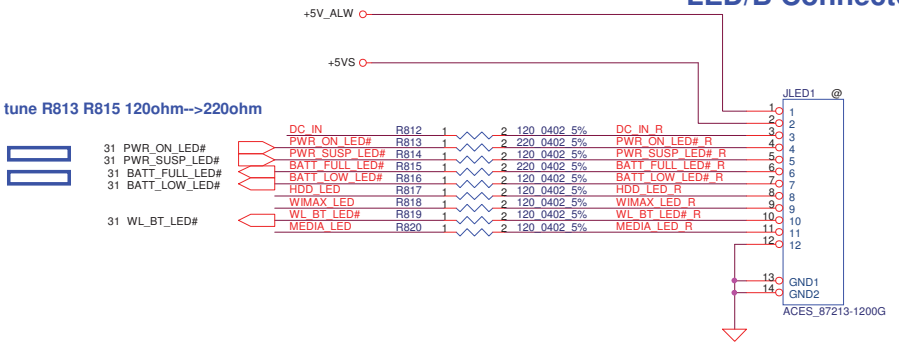
12/15<BOM> C386 @-->0.1u

1/27 Update footprint



LED/B Connector

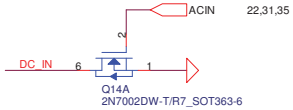
03/10 Fine tune R813 R815 120ohm-->220ohm



1/27 Del R808 R809 R810 R811

1/27 +3VALW-->+3V_ALW and +5VALW-->+5V_ALW

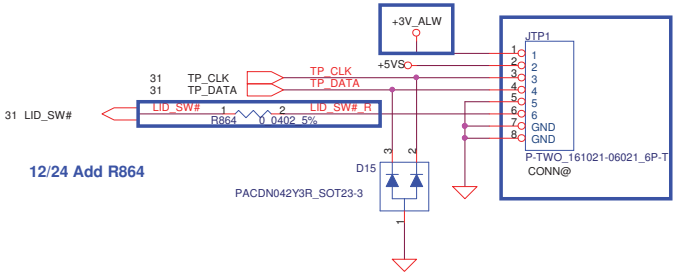
DC-IN LED



Touch/B Connector

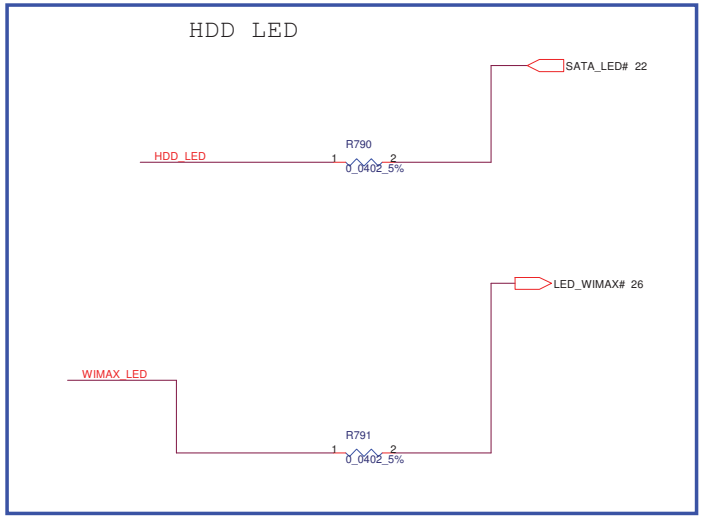
1/27 +3VALW-->+3V_ALW

03/11 Update JTP1 footprint



12/24 Add R864

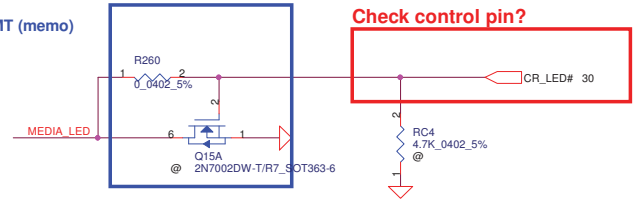
HDD LED



12/17 Q8 Q9 R258 R259-->@, R790 R791-->SMT

03/10 Q15-->@ and R260 @-->SMT (memo)

Check control pin?



Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

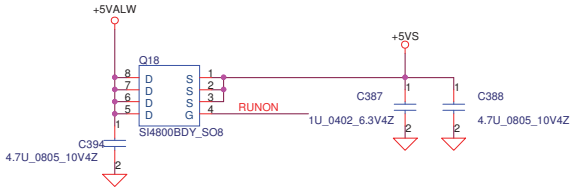
Compal Electronics, Inc.

Title: LED/LID/PB/FB/SCREW HOLE

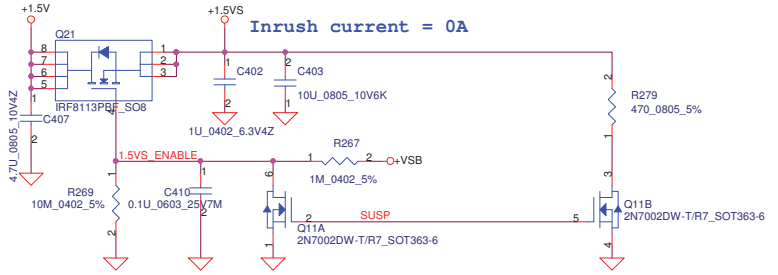
Size: B/28 Custom | Document Number: LA-6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 33 of 45

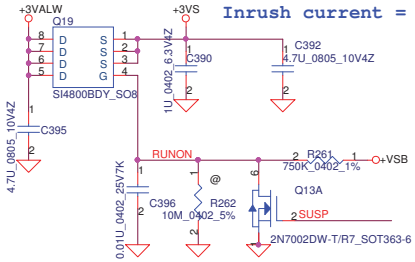
< +5VALW TO +5VS >



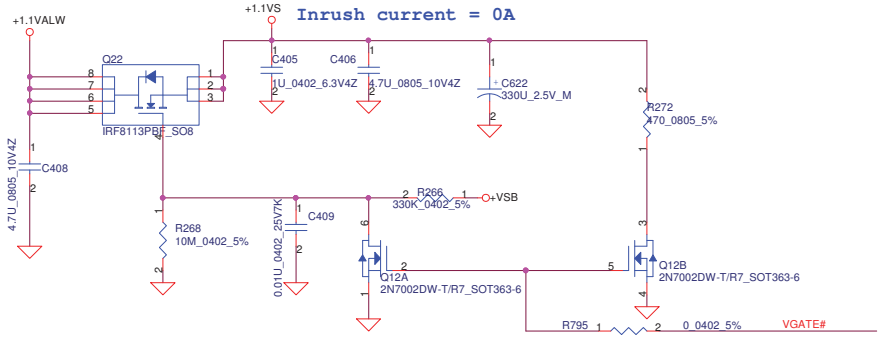
< +1.5V TO +1.5VS >



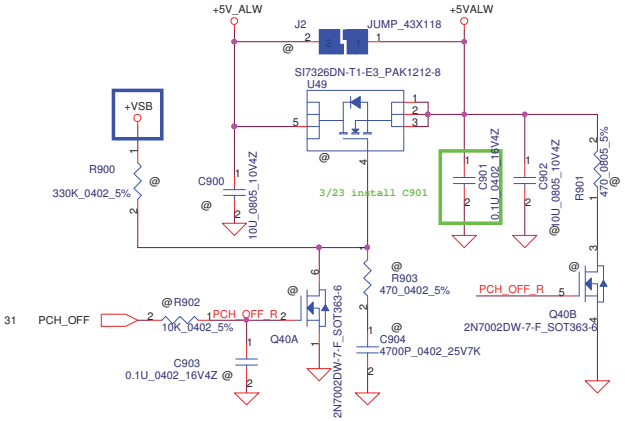
< +3VALW TO +3VS >



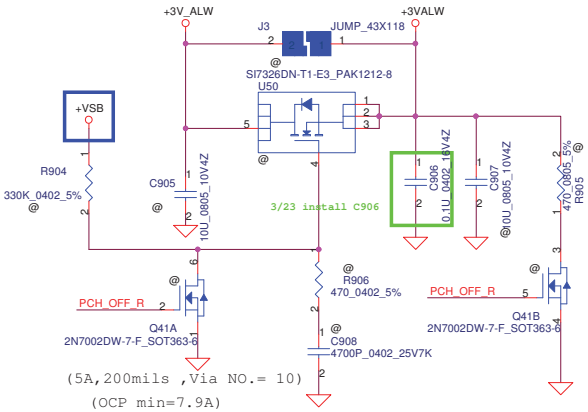
< +1.1VALW TO +1.1VS >



+5V_ALW to +5VALW Transfer

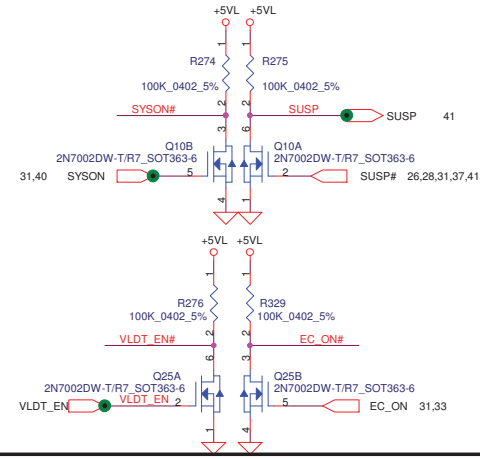


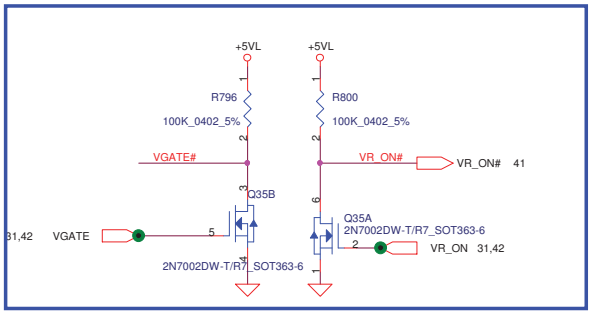
+3V_ALW to +3VALW Transfer



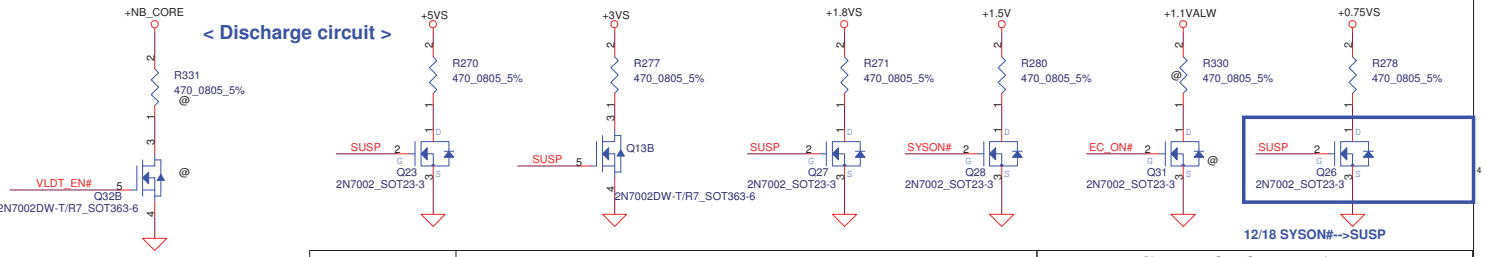
1/25 Add +5V_ALW to +5VALW Transfer
+3V_ALW to +3VALW Transfer

< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >





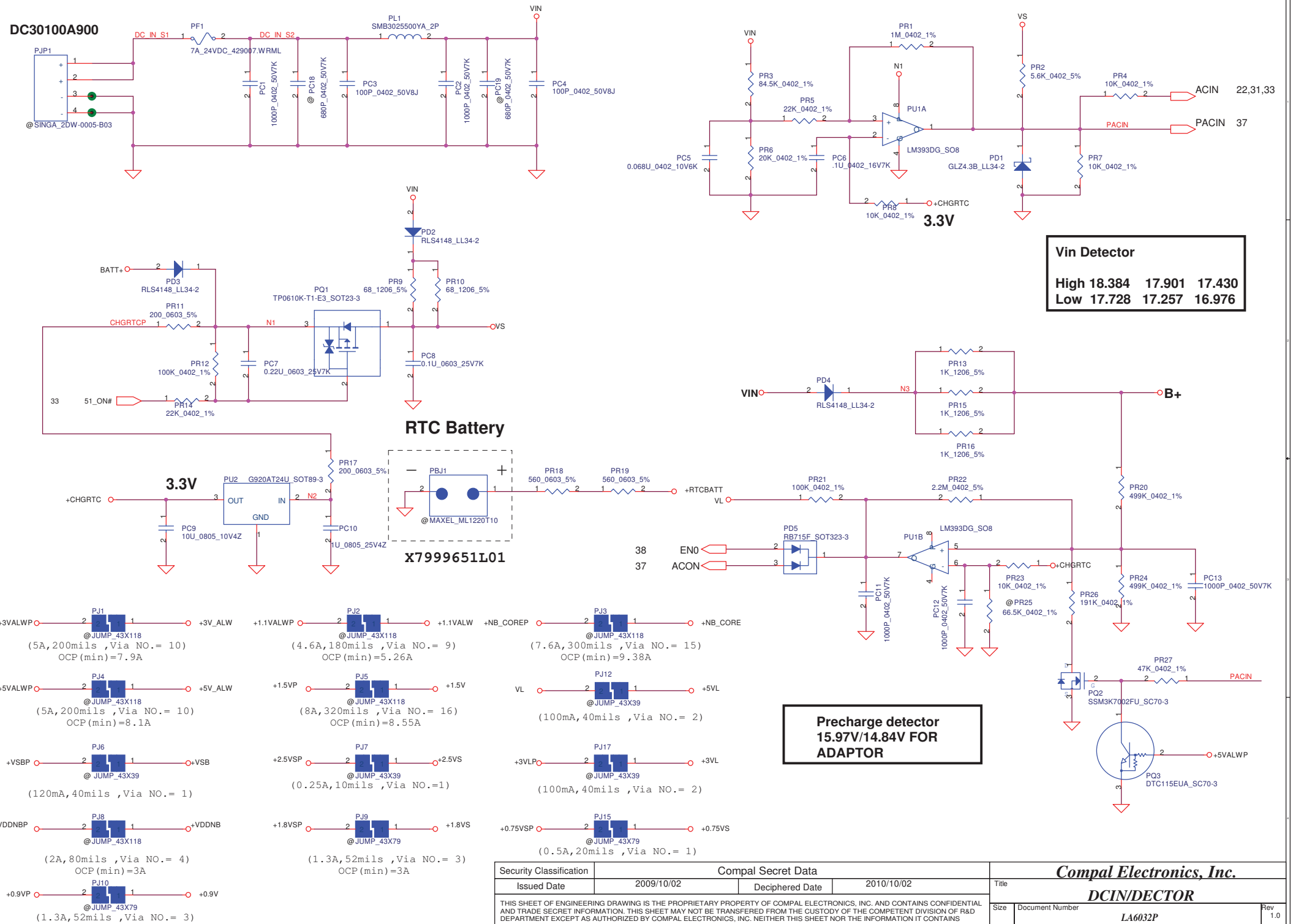
< Discharge circuit >



12/18 SYSON#-->SUSP

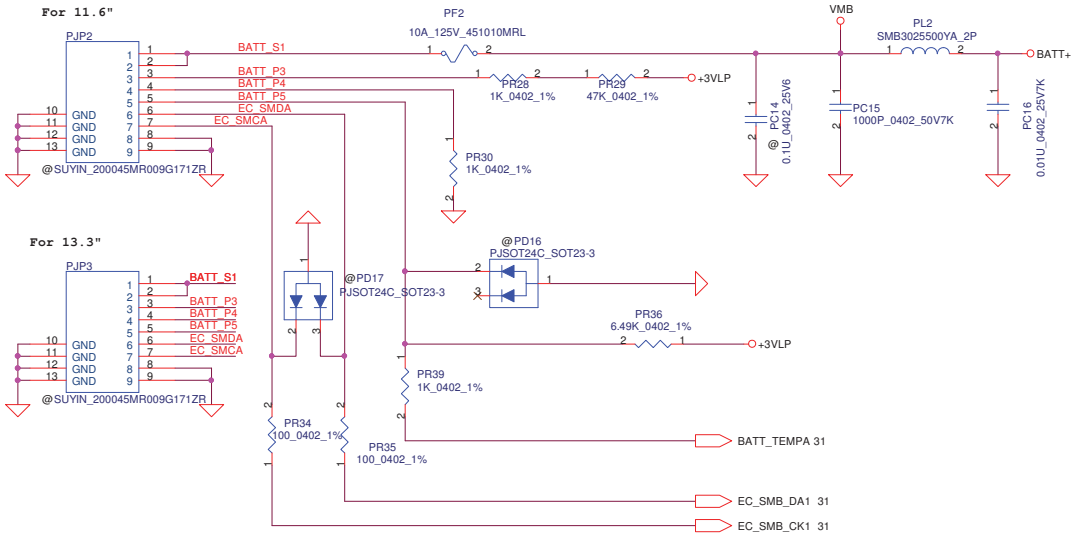
Security Classification	Compal Secret Data		
Issued Date	2008/04/14	Deciphered Date	2009/04/14

Compal Electronics, Inc.			
Title: DC/DC Circuits			
Size: Custom	Document Number: LA-6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 34 of 45		



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title	DCIN/DECTOR		
Size	Document Number	LA6032P	Rev 1.0
Date: Tuesday, March 23, 2010	Sheet 35 of 45		



PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C

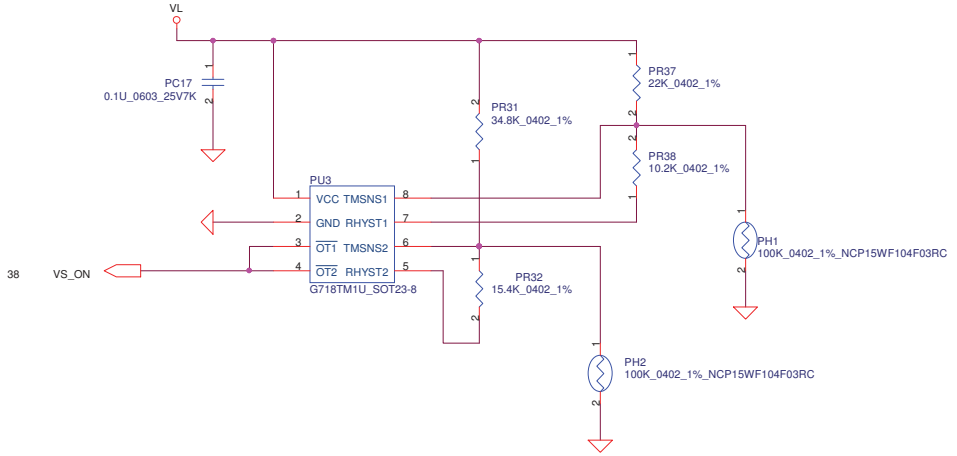
PH2 near main Battery CONN:

BAT thermal protection at 78 degree C

Recovery at 42 degree C

Rset = 3*Rtmh

Rhyst = (Rset* Rtml) / (3*Rtml - Rset)



Rtmh at 92C = 7.71K,Rtml at 56C = 26.1K

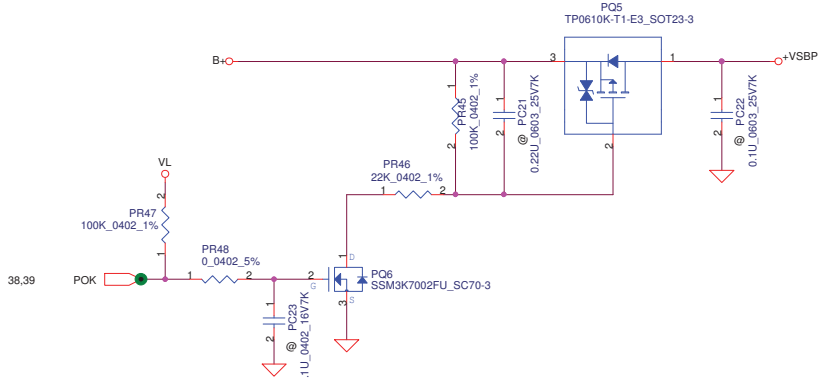
Rset = 3* 7.31 = 21.9K ==> PR37 = 22K

Rhyst = (22K* 26.1K) / (3* 26.1K - 22K) = 10.199K ==> PR38 = 10.2K

Rtmh at 78C = 11.635.K,Rtml at 42C = 46.38K

Rset = 3* 11.635 = 34.91K ==> PR31 = 34.8K

Rhyst = (34.8K* 46.38K) / (3* 46.38K - 34.8K) = 15.468K ==> PR32 = 15.4K



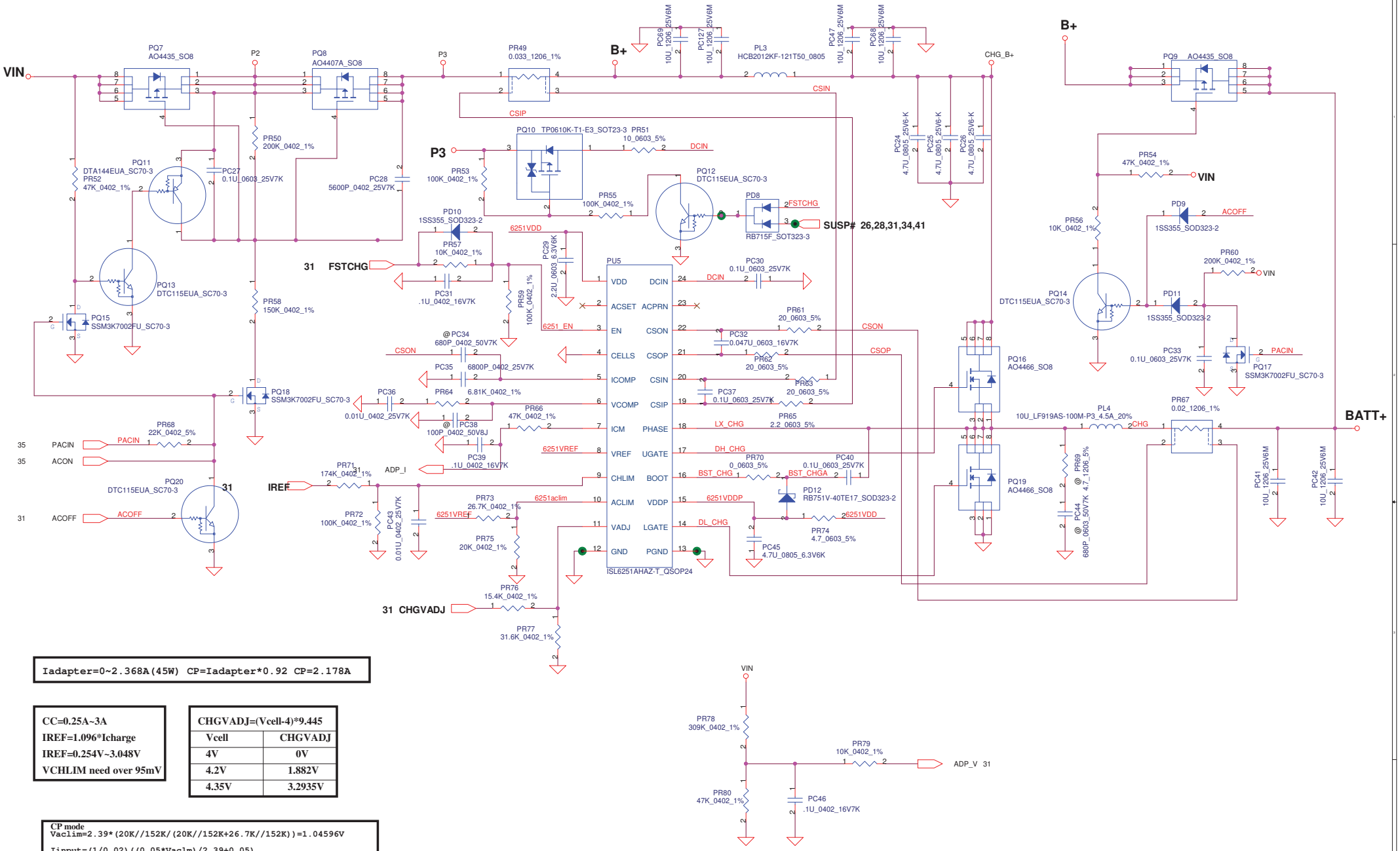
Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size | Document Number: LA6032P | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 36 of 45



Iadapter=0~2.368A(45W) CP=Iadapter*0.92 CP=2.178A

CC=0.25A~3A
IREF=1.096*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode
Vaclim=2.39*(20K//152K/(20K//152K+26.7K//152K))=1.04596V

Iinput=(1/0.02)((0.05*Vaclm)/2.39+0.05)
where Vaclm=1.04596V, Iinput=2.178A

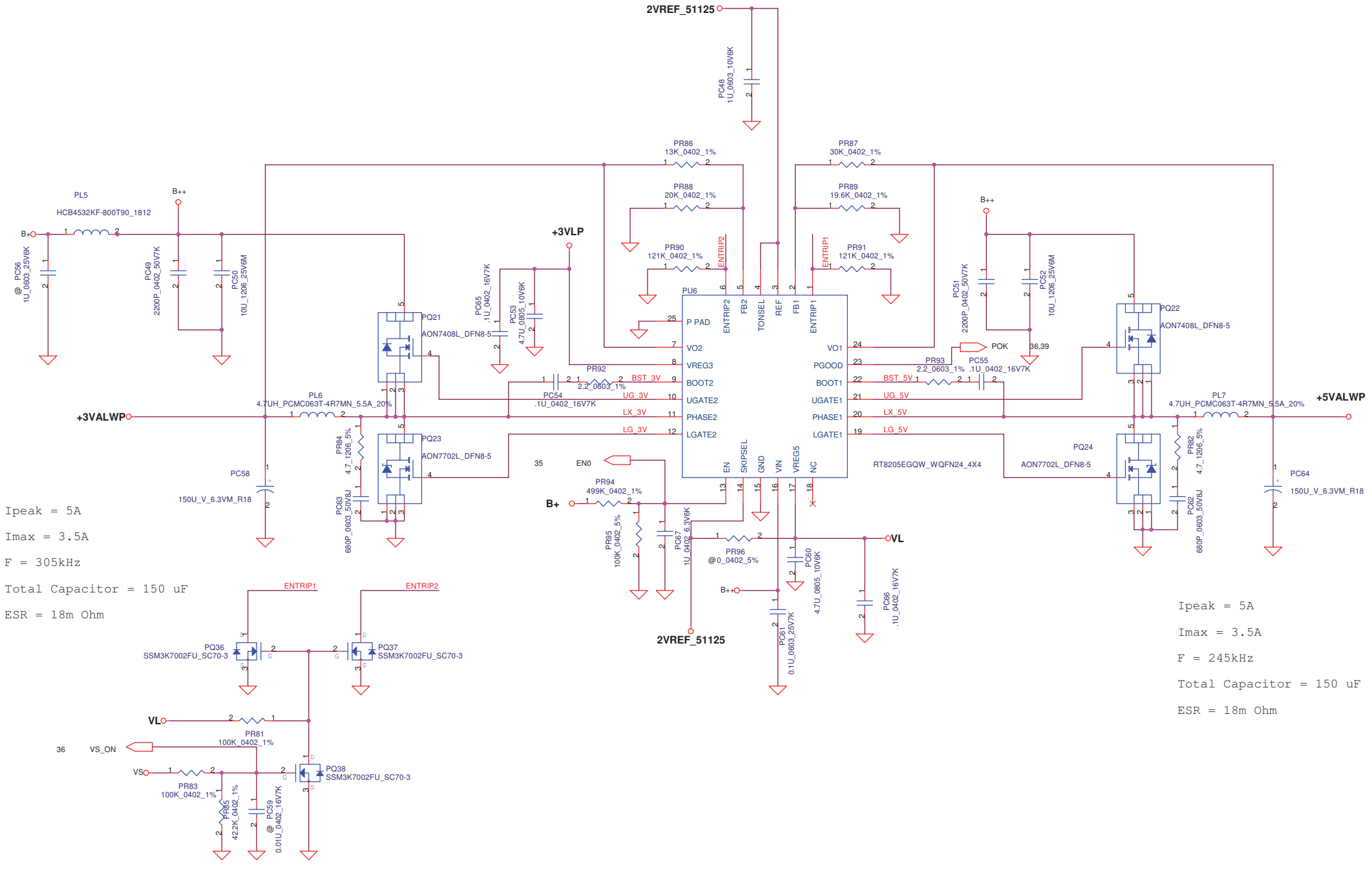
Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: LA6032P | Rev: 1.0

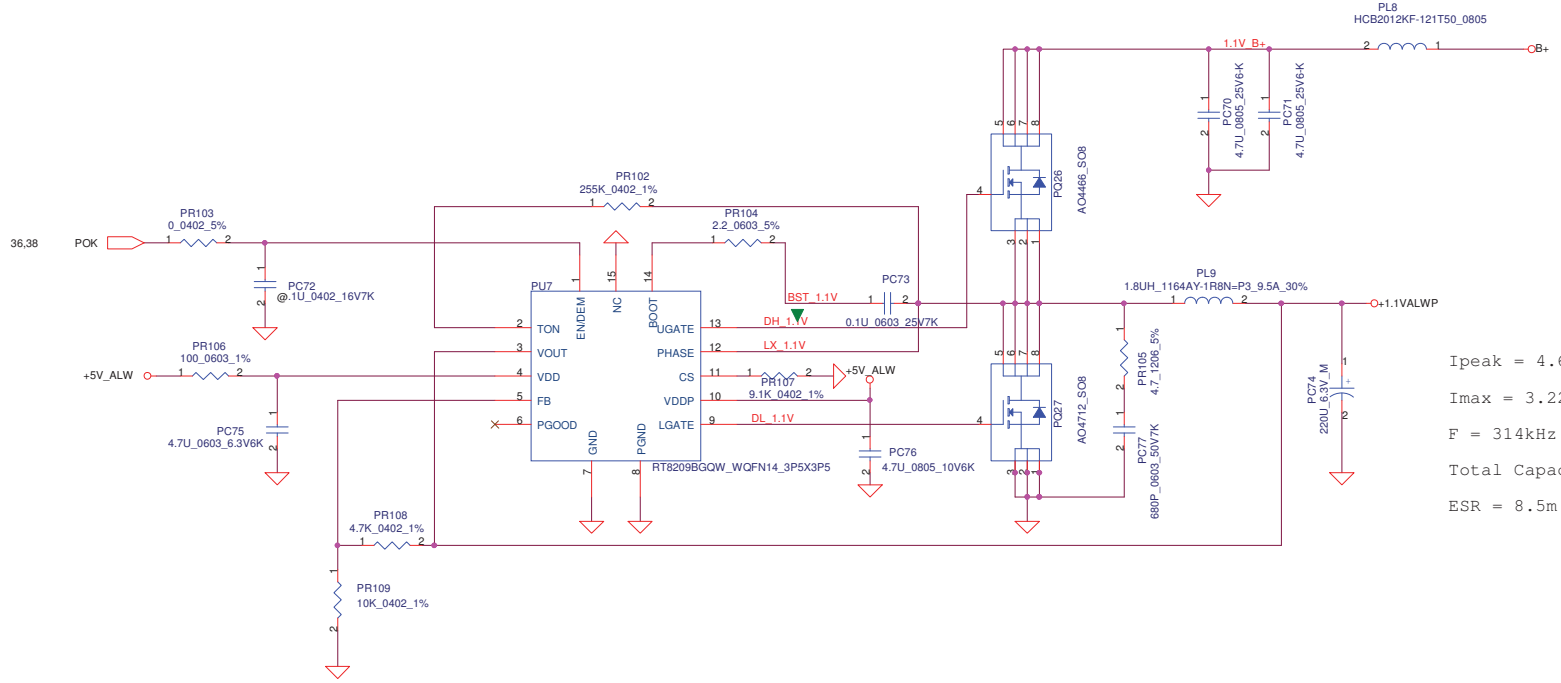
Date: Tuesday, March 23, 2010 | Sheet 37 of 45



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title	+5VALWP/+3VALWP	
Size	Document Number: LA-6032P	Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 38 of 45	



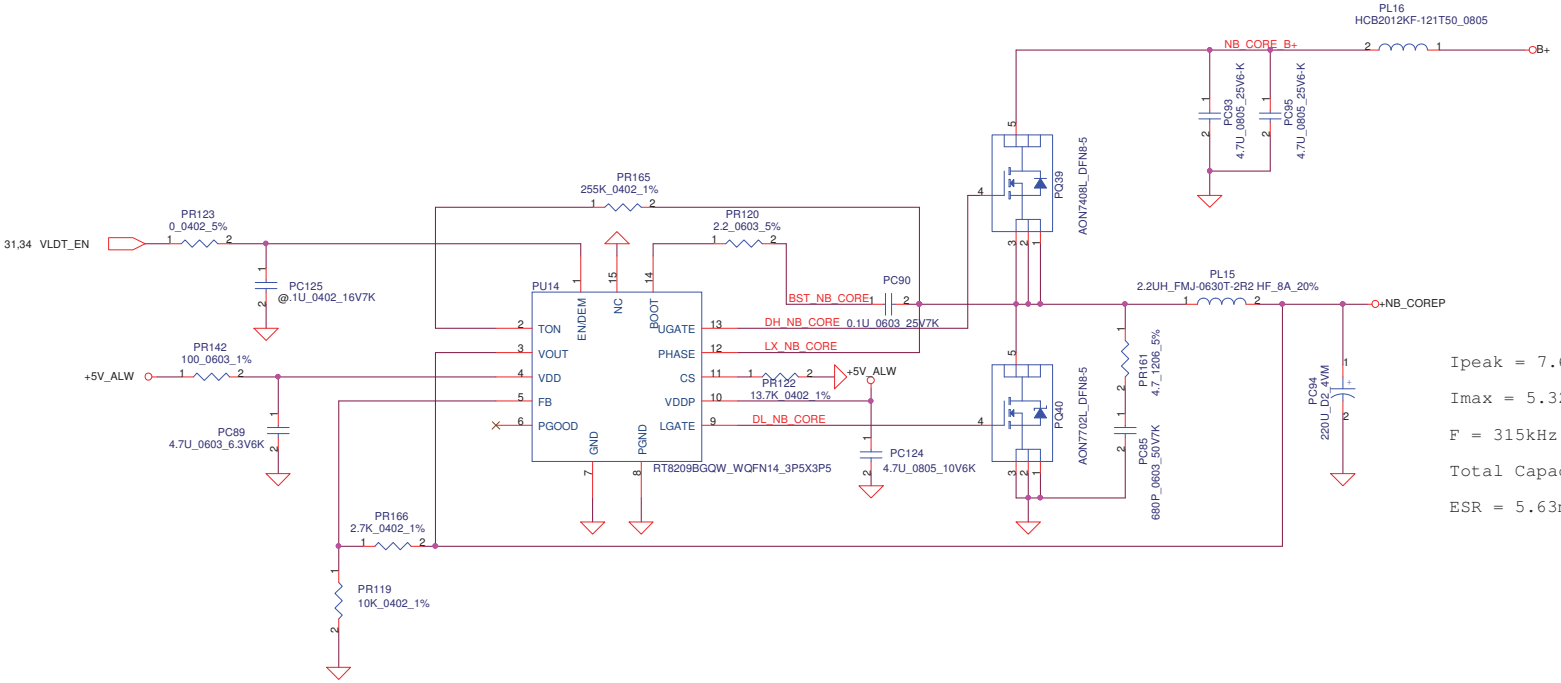
Ipeak = 4.6A

Imax = 3.22A

F = 314kHz

Total Capacitor = 550 uF

ESR = 8.5m Ohm



Ipeak = 7.6A

Imax = 5.32A

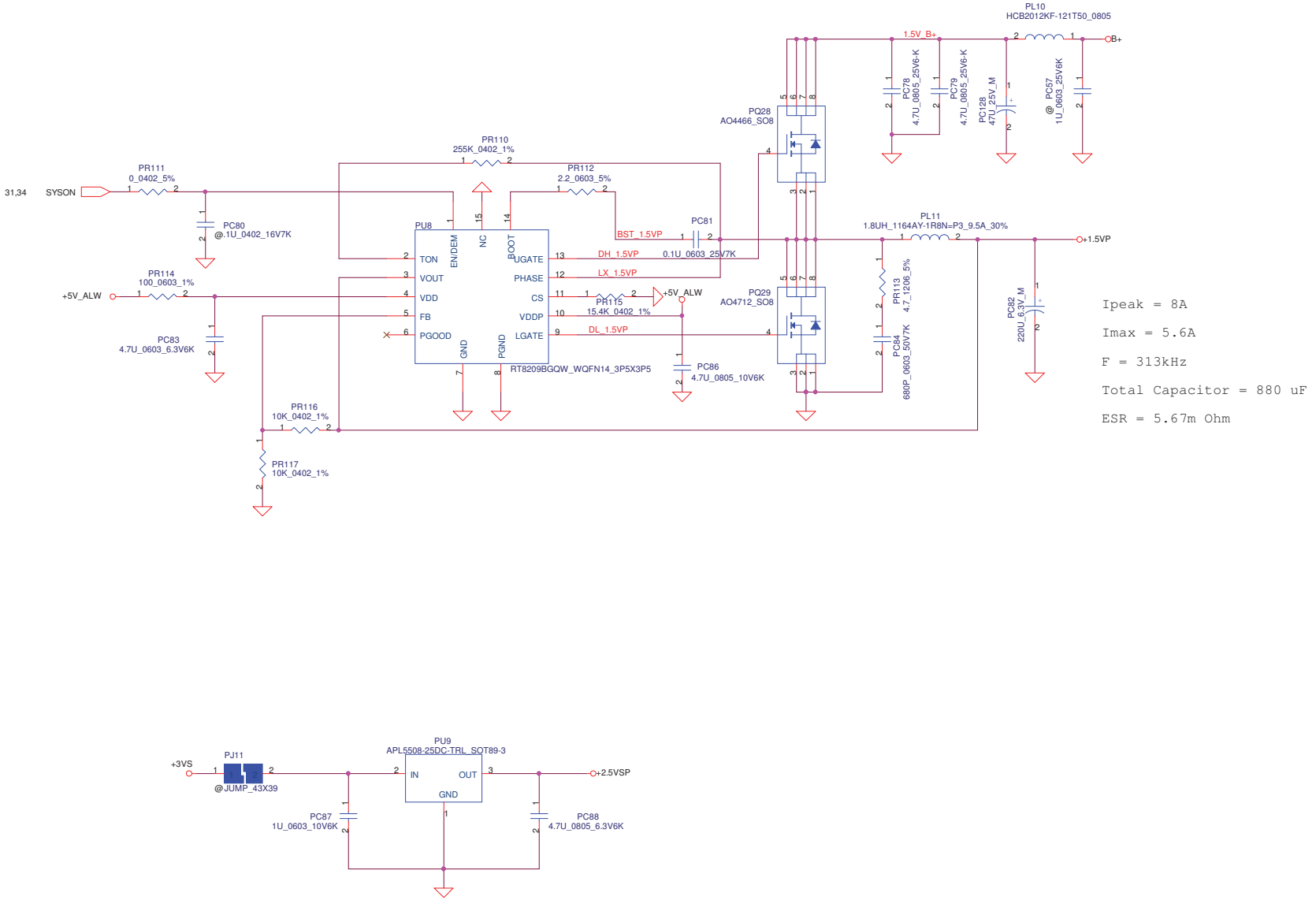
F = 315kHz

Total Capacitor = 550 uF

ESR = 5.63m Ohm

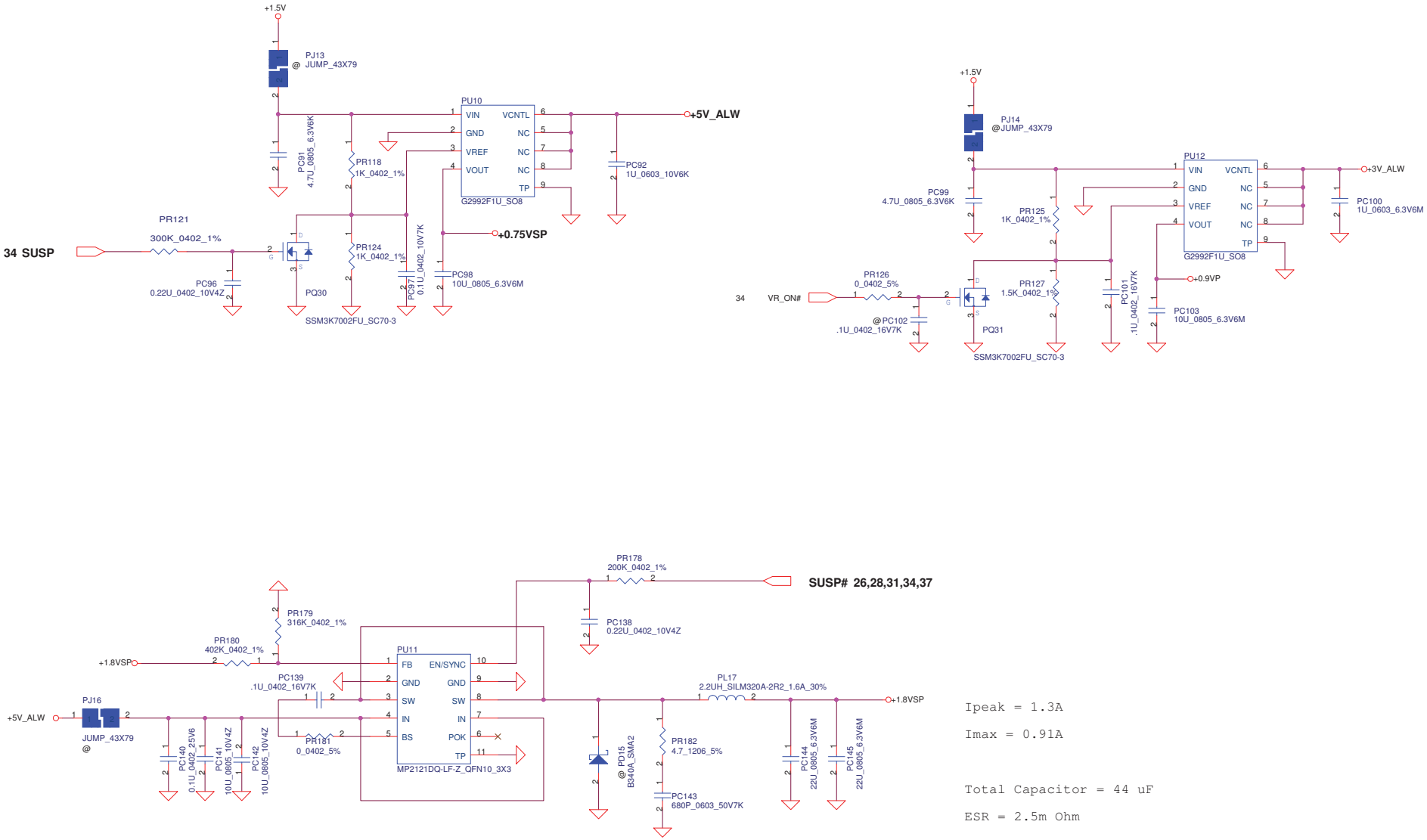
Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title: +1.1VALWP/+NB_COREP			
Size: B/28	Document Number: LA6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 39 of 45		



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title: 1.5VP/2.5VSP			
Size: B	Document Number: LA6032P		Rev: 1.0
Date: Tuesday, March 23, 2010		Sheet 40 of 45	



Ipeak = 1.3A

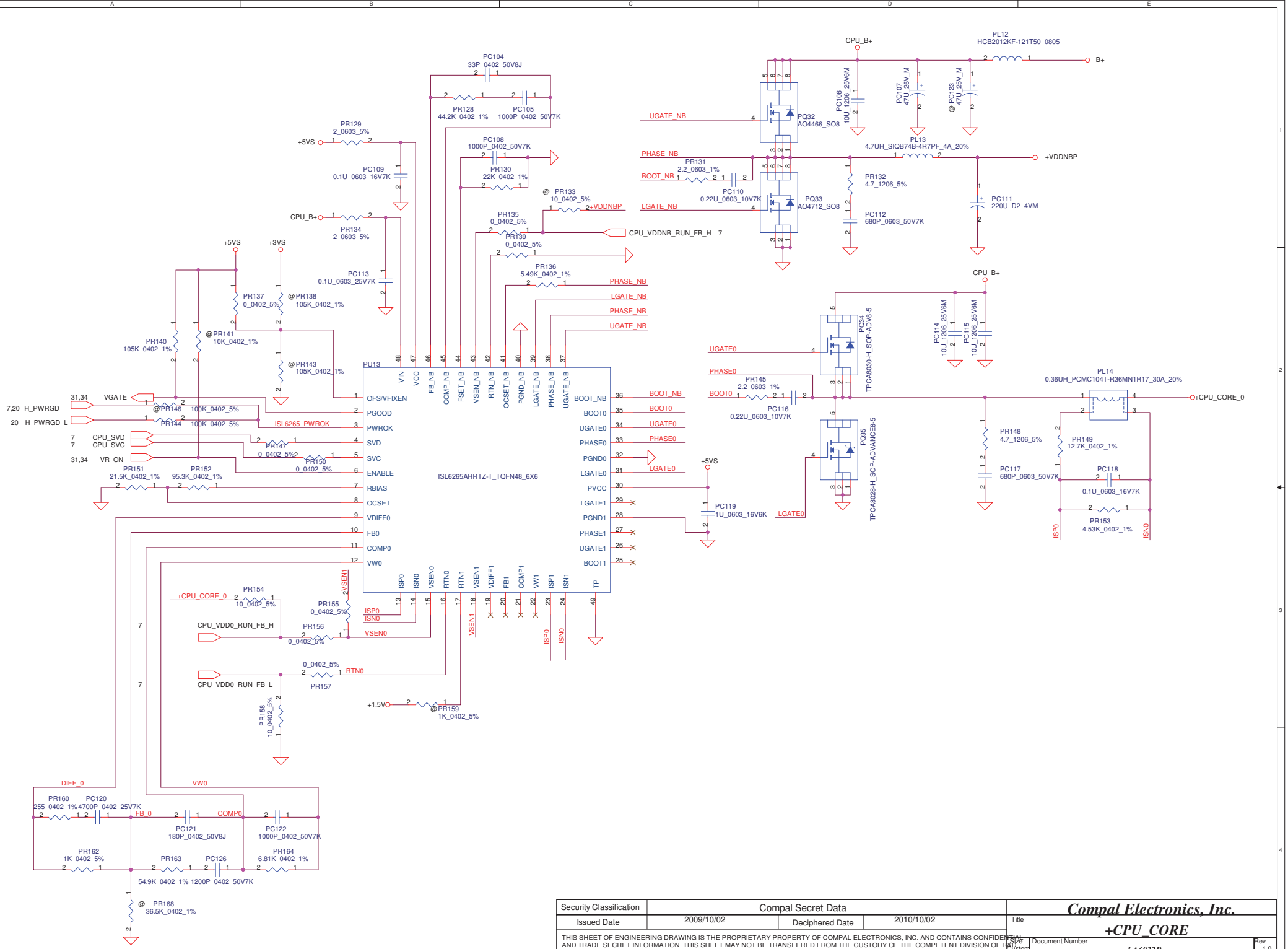
Imax = 0.91A

Total Capacitor = 44 uF

ESR = 2.5m Ohm

Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title	0.75VSP/0.9VP/1.8VSP		
Size	Document Number	LA6032P	Rev 1.0
Date: Tuesday, March 23, 2010	Sheet 41 of 45		



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title: +CPU_CORE			
Size: Custom	Document Number: LA6032P		Rev: 1.0
Date: Tuesday, March 23, 2010	Sheet 42 of 45		

Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
		2009/11/10	POWER		Release
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR31 change to 34.8k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR32 change to 15.4k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR37 change to 22k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR38 change to 10.2k	DVT
P39	CHARGER	2009/12/03	POWER	PC24,25,26 size change to 4.7uf 0805	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR121 change to 300k	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PC96 change to 0.22uf	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR125 change to 1k	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR127 change to 1.5k	DVT
P44	+CPU_CORE	2009/12/03	POWER	Delete PR142	DVT
P44	+CPU_CORE	2009/12/03	POWER	PR131, PR145 change to 2.2 ohm	DVT
P44	+CPU_CORE	2009/12/03	POWER	PR132 change to 4.7_1206_5%	DVT
P44	+CPU_CORE	2009/12/03	POWER	PC112 change to 680P_0603_50V7K	DVT
P39	CHARGER	2010/01/29	POWER	Add PC47,68,69,127 10U_1206_25V6M	PVT
P41	+1.1VALWP/+NB_COREP	2010/02/03	POWER	Add PC70 4.7U_0805_25V6-K	PVT
P41	+1.1VALWP/+NB_COREP	2010/02/03	POWER	PL9 change to 1.8UH_9.5A_30%	PVT
P44	+CPU_CORE	2009/12/03	POWER	PL13 change to 4.7UH_4A_20%	PVT
P37	CHARGER	2009/02/08	POWER	Move PR18,PR19 to connect PBJ1	PVT2

EVT to DVT Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Update JSATA1, JHDMI1 and JREAD1 footprint		ME request	2009/12	EVT->DVT
2	Update DDR_CS0_DIMMB#, DDR_CS1_DIMMB# net	P06	Net contact error on DIMMB	2009/12	EVT->DVT
3	Update DDR_CKE0_DIMMA, DDR_CKE1_DIMMA net	P06	Net contact error on DIMMA	2009/12	EVT->DVT
4	R41~R44 SMT-->@	P07	Fine tune HDT debug pull high R	2009/12	EVT->DVT
5	Del R46 and add R850~R854	P07	For ESD request	2009/12	EVT->DVT
6	Add RS15 RS16 for NBGFX_CLK,NBGFX_CLK#	P12	For internal clock gen	2009/12	EVT->DVT
7	Fine tune RS880M clock	P12	For internal clock gen	2009/12	EVT->DVT
8	Del external clock gen	P16	For internal clock gen	2009/12	EVT->DVT
9	Fine tune pin define JP4 Pin1 Pin2 Pin8-->GND	P17	Add more GND pin	2009/12	EVT->DVT
10	Add R855 R856 for HDMI_SDATA,HDMI_SCLK pull high R	P19	Solve HDMI can not detect	2009/12	EVT->DVT
11	U6 pin5 +5VL-->+5VS and HDMI Dual NMOSx2(Q6 Q7)->Single NMOS (Q6)	P19	Cost down plan	2009/12	EVT->DVT
12	Add RS1~RS14 near SB820M and TP34 TP35	P20	For internal clock gen	2009/12	EVT->DVT
13	C640 @-->22P on CLK_PCI_EC	P20	EMI request	2009/12	EVT->DVT
14	C705 C705 @-->SMT on Y6	P20		2009/12	EVT->DVT
15	R152 R153 R154 pull +3VALW-->pull GND	P21	Follow AMD check list 1.03	2009/12	EVT->DVT
16	Add device clock request pin on SB820M	P21	For internal clock gen	2009/12	EVT->DVT
17	C632 @-->33P on AZ_BITCLK_HD	P21	EMI request	2009/12	EVT->DVT
18	Add WLAN_PWR_EN# and WWAN_PWR_EN# net on SB820M	P22	Power saving request	2009/12	EVT->DVT
19	U47 +3VL-->+3VALW and Y3 R164 C246 C247 SMT->@	P22	25MHz by default	2009/12	EVT->DVT
20	Reaserved R859 C707 on CLK net	P22	EMI request	2009/12	EVT->DVT
21	Fine tune SB820M strap pin	P24	For internal clock gen	2009/12	EVT->DVT
22	Add C706 0.1u on CLK_PCI_EC	P24	EMI request	2009/12	EVT->DVT
23	Del R193 and Add R858 PH on USB_OC#2	P25	Solve the USB hang up issue	2009/12	EVT->DVT
24	Reserved RM5 RM6 CM17 QM1 RM9 for +3V_WWAN power saving	P26	Power saving request	2009/12	EVT->DVT
25	Reserved RM7 RM8 CM18 QM2 RM10 for +3V_WLAN power saving	P26	Power saving request	2009/12	EVT->DVT
26	Reserved CM19 QM3 RM11 for +1.5V_WLAN power saving	P26	Power saving request	2009/12	EVT->DVT
27	RL21 pin2 +3V_LAN-->GND	P27	LAN vender request	2009/12	EVT->DVT
28	Del RA4 RA5	P28	Fine tune Audio HP out voltage	2009/12	EVT->DVT
29	Reserved RA27 CA26 on AZ_RST_HD#	P28	ESD request	2009/12	EVT->DVT
30	Add Q37 R860 R861 and PD# net	P28	Solve Audio PD# control issue	2009/12	EVT->DVT
31	Fine tune JP5 pin define	P29	Solve the USB hnag up issue	2009/12	EVT->DVT
32	Fine tune SPK_L1,SPK_L2,SPK_R1 and SPK_R2 for SPK	P29	Solve SPK pin issue	2009/12	EVT->DVT
33	Add R857 PH USB_OC#0 net	P29	Solve the USB hnag up issue	2009/12	EVT->DVT
34	Add C708 on +5VS	P29	ESD request	2009/12	EVT->DVT
35	Fine tune card reader pin define	P30	ME use new card reader connector	2009/12	EVT->DVT
36	Add EC_MUTE# on KBC926 (U12) 83pin	P31	Solve Audio PD# control issue	2009/12	EVT->DVT
37	Q8 Q9 R258 R259-->@, R790 R791-->SMT	P33	Cost down plan	2009/12	EVT->DVT
38	C386 @-->0.1u on ON/OFFBTN#	P33	EMI request	2009/12	EVT->DVT
39	C410 0.01u_0402_16V-->0.1u_0603_25V and R267 330k->1M	P34	SMT memo	2009/12	EVT->DVT
40	SYSON#-->SUSP on Q26 Pin2	P34	+0.75VS discharge control pin	2009/12	EVT->DVT
41	RA26 0ohm-->Bead (SM010017710) on INT_MIC_CLK	P28	EMI request	2009/12/18	EVT->DVT
42	C632 @-->33P on AZ_BITCLK_HD	P21	EMI request	2009/12/18	EVT->DVT
43	R788 @-->100ohm and C634 @-->100P on SPI_CLK	P32	RF request	2009/12/18	EVT->DVT
44	R789 @-->100ohm and C635 @-->100P on AZ_BITCLK_HD	P28	RF request	2009/12/18	EVT->DVT
45	Add CA63 on INT_MIC_CLK_R	P28	RF request	2009/12/18	EVT->DVT
46	RA1 0ohm-->Bead on Audio power	P28	RF request	2009/12/18	EVT->DVT
47	Add CM20 1000P on +3V_WWAN	P26	RF request	2009/12/18	EVT->DVT
49	Add C709 on 27M_SEL	P16	RF request (EXT only)	2009/12/19	EVT->DVT
49	Fine tune R133 R value 11.8K-->8.2K	P21	Fine tune USB signal	2009/12/22	EVT->DVT
50	<BOM>RA22 RA25 4.7K-->2.2K and CA16 10u-->@	P28	Audio vender request	2009/12/22	EVT->DVT
51	Add BT_PWR# net contact to JWLAN1 pin5	P26	Follow common design	2009/12/23	EVT->DVT
52	Del R161 and SLP_CHG on SB	P22	Follow common design	2009/12/23	EVT->DVT
53	Add SLP_CHG on pin115 and add R862	P31	Follow common design	2009/12/23	EVT->DVT
54	Add UA2 CA67 CA68 CA69	P28	Audio power reserved	2009/12/23	EVT->DVT
55	Add F2 for card reader proetct	P30	H/W request	2009/12/24	EVT->DVT
56	Reserved RA28 CA70	P28	Reserved for fin tune aduio power control	2009/12/24	EVT->DVT
57	Add R863 PH on CIR_EN#	P21	Follow common design	2009/12/24	EVT->DVT
58	Add R864 on LID_SW#	P33	Reserved for ESD protect	2009/12/24	EVT->DVT
59	Modify TP26 TP27-->EVENT#_A and EVENT#_B	P09 P10	Solve layout test point issue	2009/12/25	EVT->DVT
60	C497 SMT-->@	P08	Fine tune CPU_CORE cap	2009/12/25	EVT->DVT

Compal Electronics, Inc.

Title: EE change list-1

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Add D17 and Q38 for BT power control	P26	Follow common design	2010/1/20	DVT->PVT
2	Change net name SLP_CHG-->SLP_CHG#	P25 P31	Follow net rule	2010/1/20	DVT->PVT
3	Need to fine tune R783 and R784	P18	VB function	2010/1/20	DVT->PVT
4	<BOM> SB use 2MB SPI ROM SA00002TO00	P22	Non share ROM	2010/1/20	DVT->PVT
5	<BOM> Update LAN P/N for LAN VB P/N	P27	Vender update P/N	2010/1/20	DVT->PVT
6	<BOM> EC SPI use 256KB SPI ROM SA00003GK00	P32	Non share ROM	2010/1/20	DVT->PVT
7	BT part SMT-->@	P29	IUR no BT device	2010/1/20	DVT->PVT
8	Update JREAD1 footprint (Same as EVT)t	P30	ME request	2010/1/20	DVT->PVT
9	Update JSATA1 footprint TAIWI_EU114-117CRL-TW_11P-T	P25	ME request	2010/1/20	DVT->PVT
10	Update JHDD1 pin4 +5VS-->GND	P25	HW request	2010/1/20	DVT->PVT
11	Del DC to DC +NB_CORE part	P34	HW request	2010/1/20	DVT->PVT
12	Change USB port10 to USB port5 on WWAN	P21	Follow common design	2010/1/20	DVT->PVT
13	Add R865 R866 for SLP_CHGX_M3/M4 on SB	P21	Follow common design	2010/1/20	DVT->PVT
14	Add R867 R868 for SLP_CHGM3/M4 on EC	P31	Follow common design	2010/1/21	DVT->PVT
15	UA2 pin5 +PVDD1-->+AVDD	P28	Reserved for Audio analog power	2010/1/21	DVT->PVT
16	<BOM> U48 SA000008G00-->SA00003DR00 (Same as intel)	P29	HW request	2010/1/21	DVT->PVT
17	Del R164 Y3 C246 C247 and add TP36 TP37	P22	HW request	2010/1/22	DVT->PVT
18	JLVDS1 pin24 +LCD_INV-->NG	P18	Follow common design	2010/1/22	DVT->PVT
19	U9 pin1 +5VALW-->+5V_ALW for USB charge	P25	Follow common design	2010/1/22	DVT->PVT
20	Add C900~C908,R900~R906 Q40 Q41 U49 U50 for power save	P34	Follow common design	2010/1/22	DVT->PVT
21	Update JTP1 footprint--> E-T_6916-Q06N-00R_6P	P33	ME request	2010/1/25	DVT->PVT
22	Update USB20_P10-->USB20_P5 ,USB20_N10-->USB20_N5	P21 P26	Follow common design	2010/1/25	DVT->PVT
23	Update JHDMI1footprint-->SUYIN_100042GR019M23BZR_19P-T	P19	ME request	2010/1/25	DVT->PVT
24	R900 pin 1 and R904 pin1 +B-->+VSB	P34	HW request	2010/1/27	DVT->PVT
25	Add J2 J3 for +3V_ALW and +5V_ALW	P34	HW request	2010/1/27	DVT->PVT
26	R808 pin 1,R809 pin2 +3VALW-->+3V_ALW and +5VALW-->+5V_ALW	P33	HW request	2010/1/27	DVT->PVT
27	Add R907 for USB_EN# PH	P29	HW request	2010/1/27	DVT->PVT
28	Del R808 R809 R811 R810 R258 Q8 R259 Q9	P33	HW request	2010/1/27	DVT->PVT
29	R238 pin1 +3VALW-->+3V_ALW	P31	HW request	2010/1/29	DVT->PVT
30	JTP1 pin1 +3VALW-->+3V_ALW	P33	Follow common design	2010/1/29	DVT->PVT
31	Del R246	P32	HW request	2010/1/29	DVT->PVT
32	Add LPC_FRAME#, LPC_AD, LPC_AD1,LPC_AD2,LPC_AD3 JWAN1	P26	HW request	2010/1/29	DVT->PVT
33	Update JPB1 footprint P-TWO_161011-04021_4P-T	P33	ME request	2010/1/29	DVT->PVT
34	Add JHDD2 ACES_87036-1001-CP_10P	P25	HW request	2010/1/29	DVT->PVT
35	Fine tune JP4 pin define for EMI request	P17	EMI request	2010/1/29	DVT->PVT
36	<BOM> Update UA1 P/N for Audio VB version	P28	Vender update P/N	2010/1/29	DVT->PVT
37	Update JP5 pin define and 20pin-->22pin	P29	HW request	2010/1/30	DVT->PVT
38	<BOM> R133 8.2K-->11.8K same as EVT	P21	HW request	2010/1/31	DVT->PVT
39	Add C909 C910	P17	EMI request	2010/1/31	DVT->PVT
40	Add D18 and R908 on RTC circuit	P20	Follow common design	2010/1/31	DVT->PVT
41	JHDD1 10pin-->12pin	P29	Add more power and GND pin on HDD conn	2010/1/31	DVT->PVT
42	Add R909 R910 for ADAPTOR_SEL	P31	Follow common design	2010/1/31	DVT->PVT
43	Add L41 L42 L43 C911 C912 C913 for EMI request	P12	EMI request	2010/2/2	DVT->PVT
44	C240 C244 22P to 18P	P20	Solve RTC fial issue	2010/2/2	DVT->PVT
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Compal Electronics, Inc.

Title: EE change list-2

Size: A3 | Document Number | Rev

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