

Compal Confidential

Schematics Document

INTEL Auburndale BGA with IBEX core logic

Fossil 2.0 UMA

LA-6161P

2010-05-18

REV:0.5

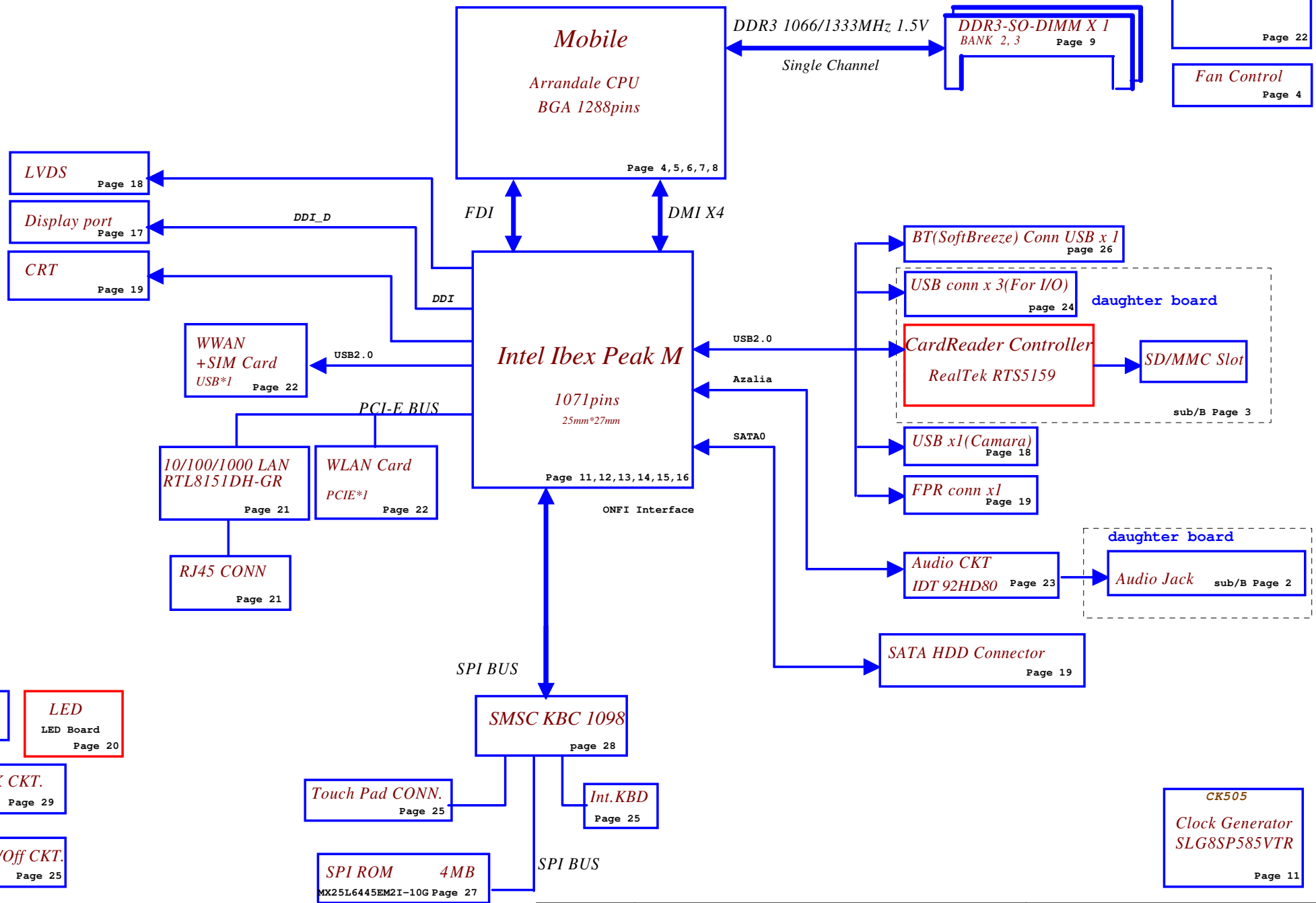
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Fossil 2.0 UMA

XPDP Conn. Page 4

Accelerometer
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Fan Control Page 4



RTC CKT. Page 11

LED
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Power OK CKT. Page 29

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DC/DC Interface CKT. Page 30

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

ULV@ : means just install for ULV CPU

CONN@ : means ME part.

 Layout Notes

07/24 update

 : Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*

SMBUS Control Table

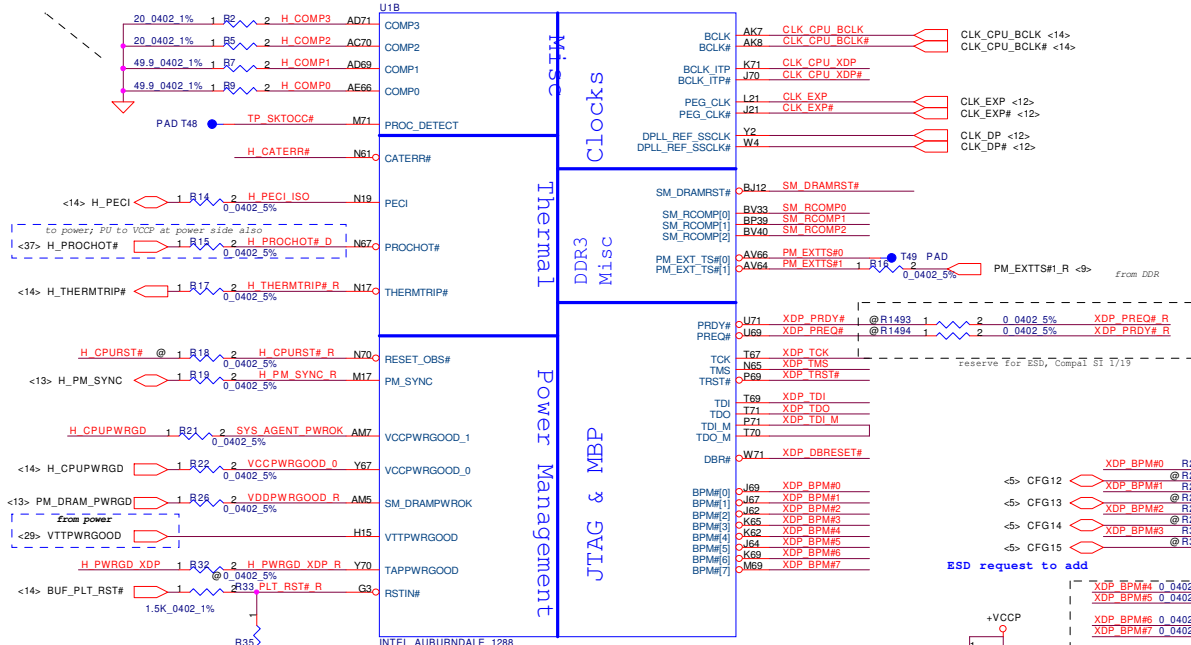
	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	V

Strapping Options Flash

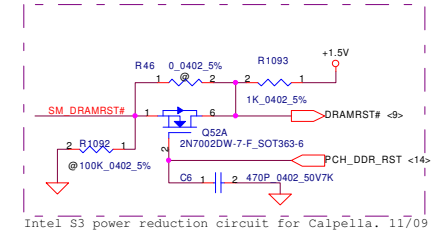
GNT1#	GNT0#	Routing
0	1	Reserved
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI
0	0	Flash Cycles Routed to LPC

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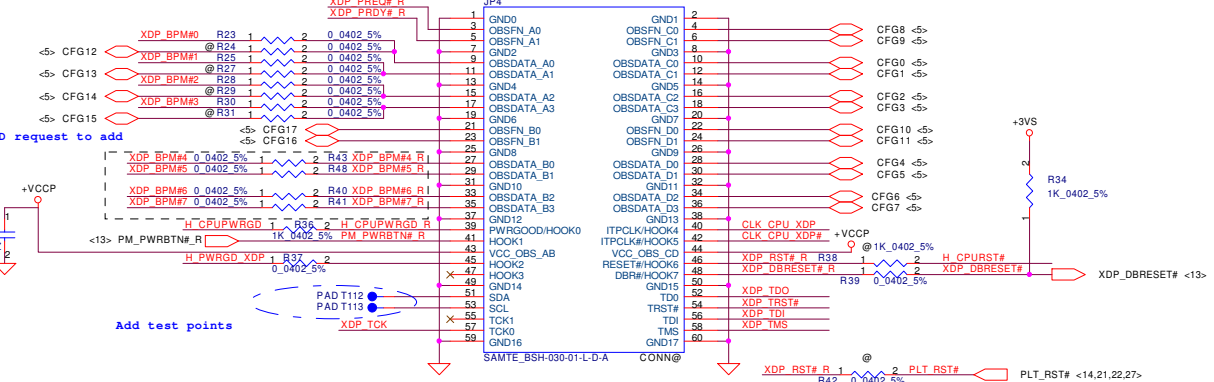
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length < 0.5", spacing 20mil



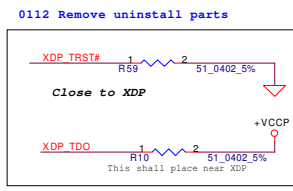
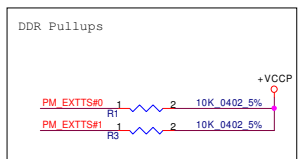
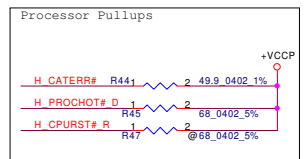
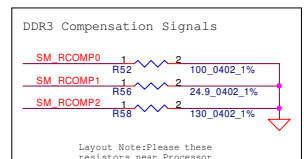
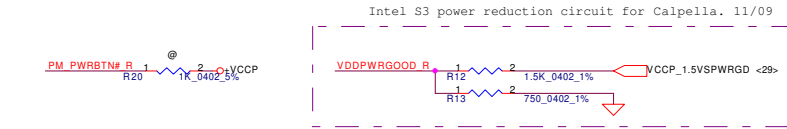
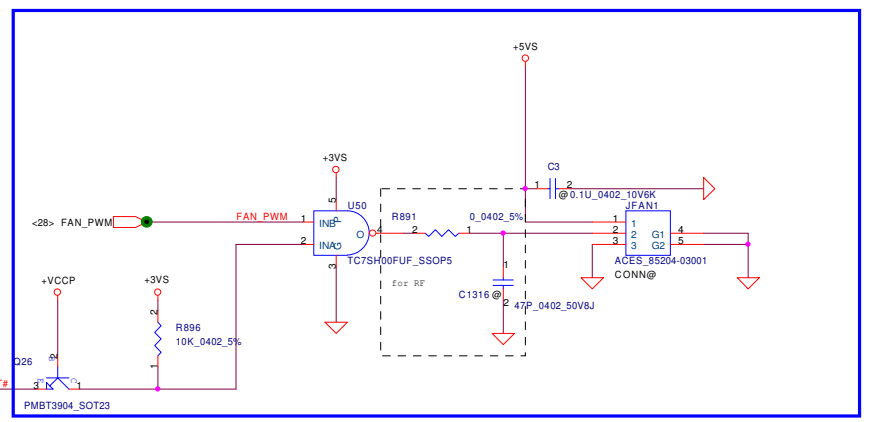
2nd Source :
 SV - i5-540M CPU : 2.53G (K0)
 SV - i5-450M CPU : 2.4G (K0)
 SV - i3-350M CPU : 2.26G (K0)
 SV - i3-370M CPU : 2.4G (K0)
 ULV - U3400 CPU : 1.06G (K0)



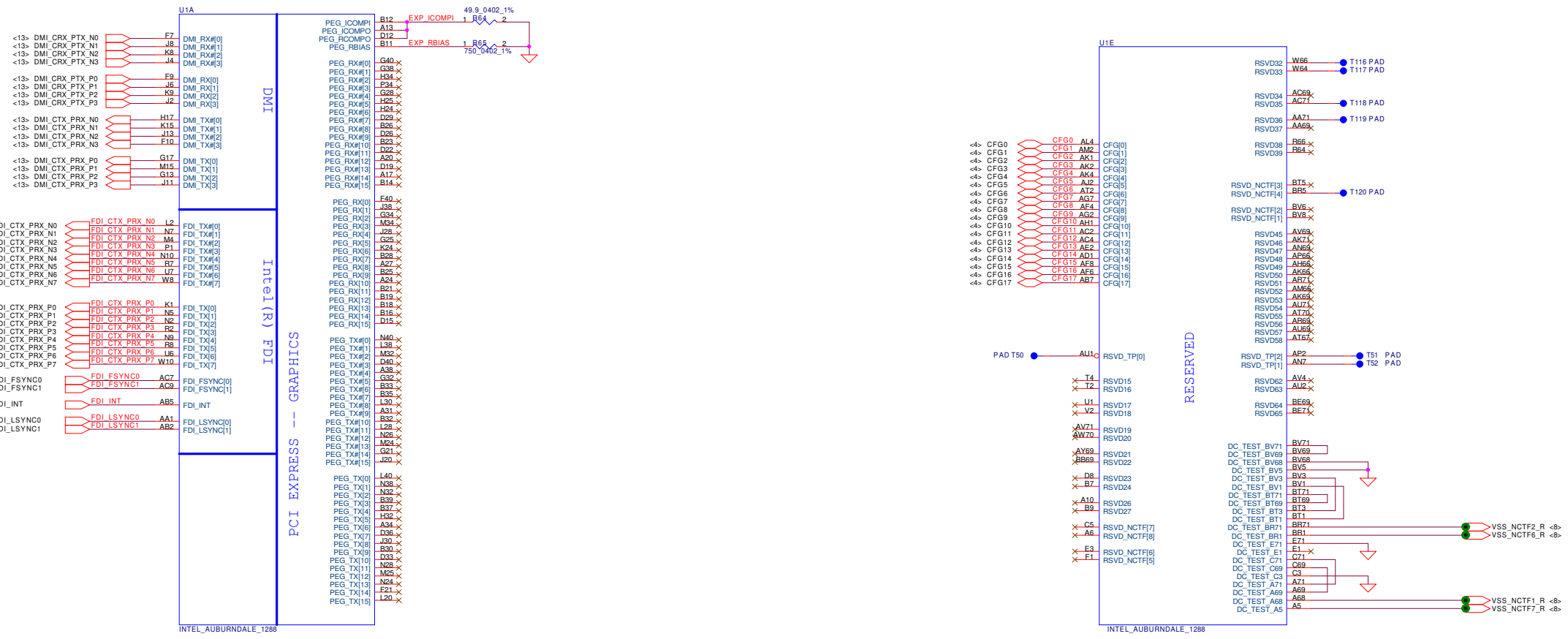
CPU XDP Connector



PWM Fan Control circuit



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CFG Straps for PROCESSOR

CFG0 R68 1 2 @3.01K 0402 1%

PCI-Express Configuration Select
 1: Single PEG
 CFG0
 0: Bifurcation enabled
 Not applicable for Clarksfield Processor

CFG3 R69 1 2 @3.01K 0402 1%

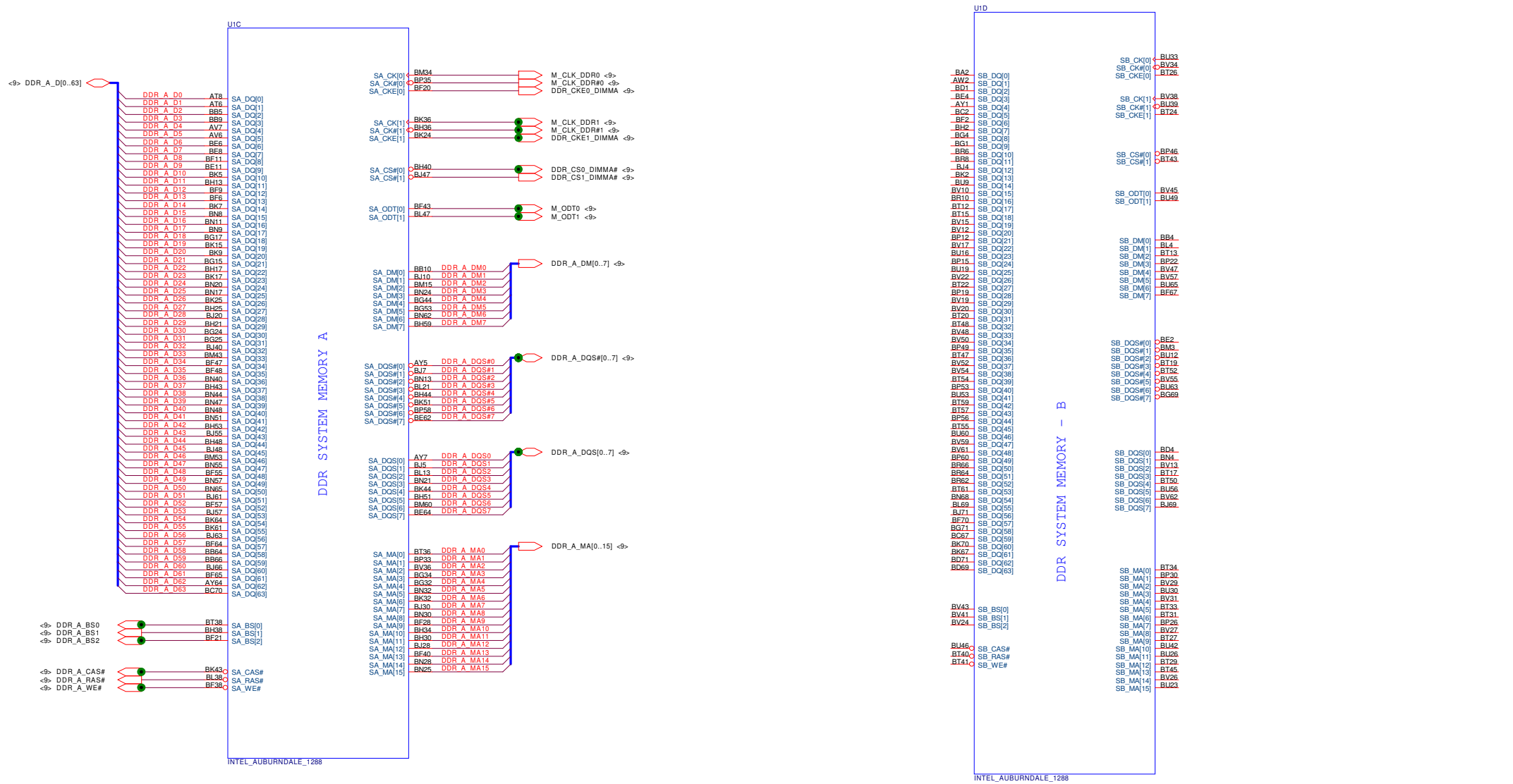
CFG3-PCI Express Static Lane Reversal
 1: Normal Operation
 CFG3
 0: Lane Numbers Reversed
 15 -> 0, 14 -> 1,

CFG4 R70 1 2 3.01K 0402 1%

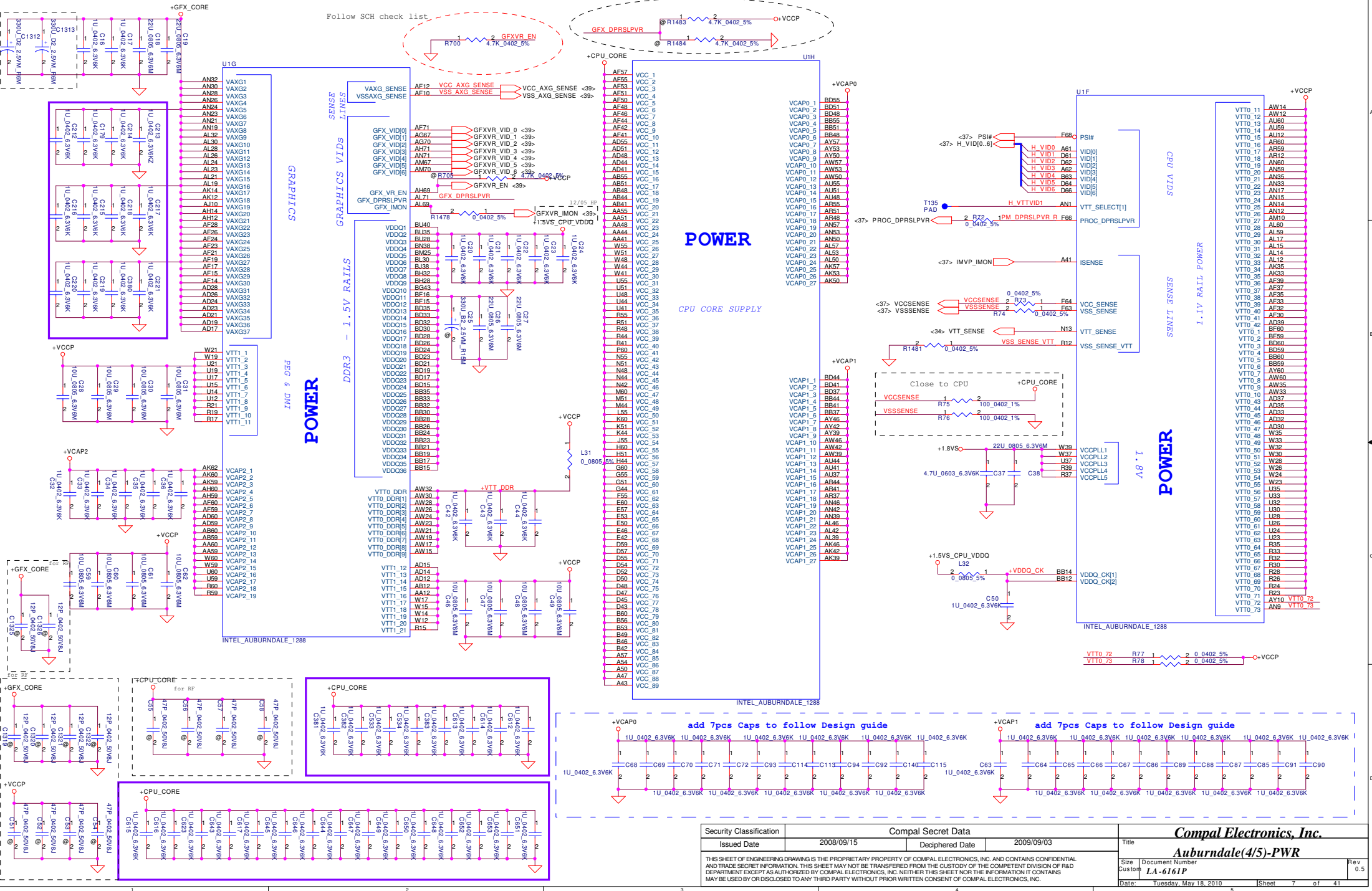
ES1 sample need negative voltage
 ES2 sample contact to GND

CFG4-Display Port Presence
 1: Disabled; No Physical Display Port attached to Embedded Display Port
 CFG4
 0: Enabled; An external Display Port device is connected to the Embedded Display Port

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Follow SCH check list

POWER

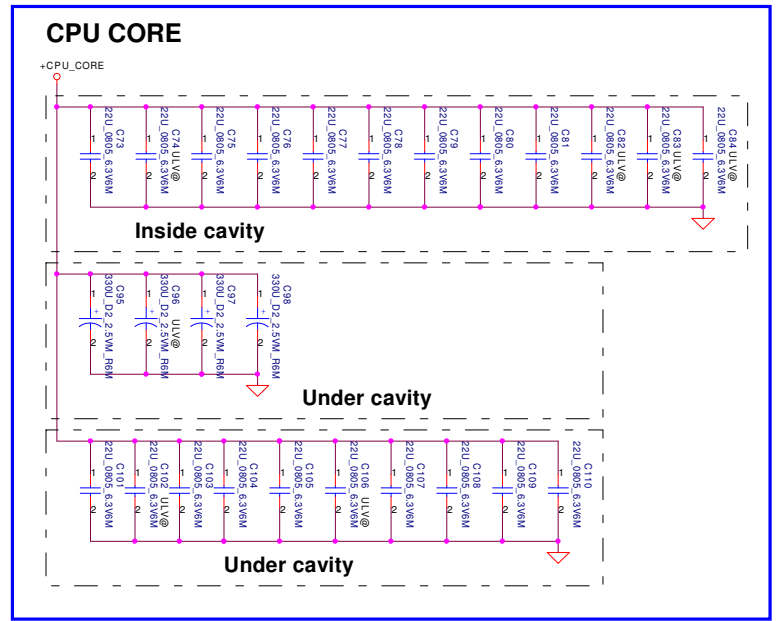
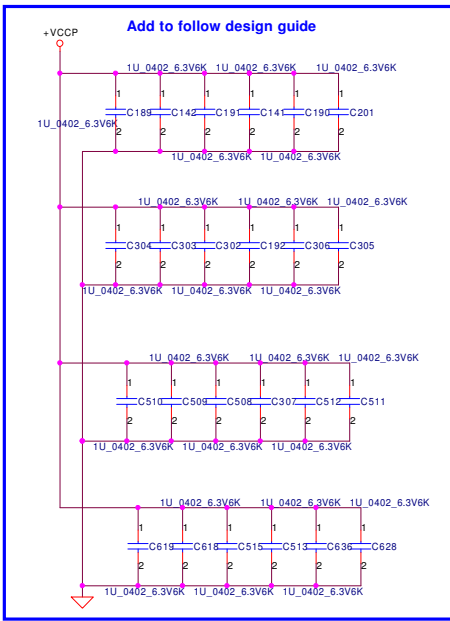
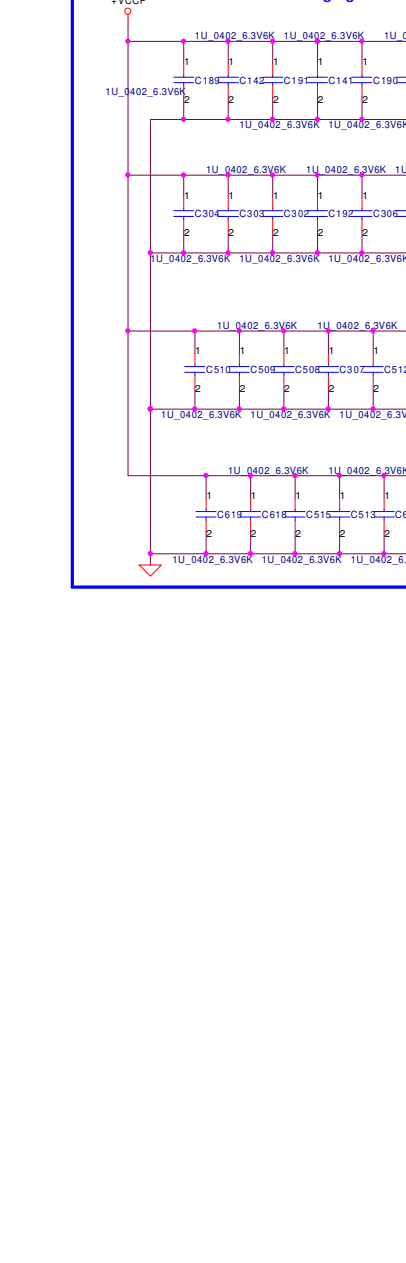
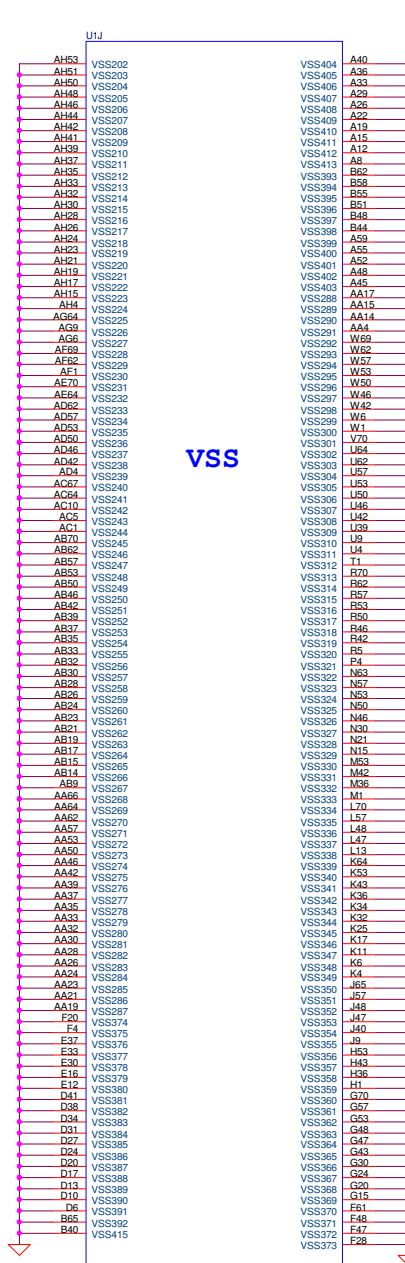
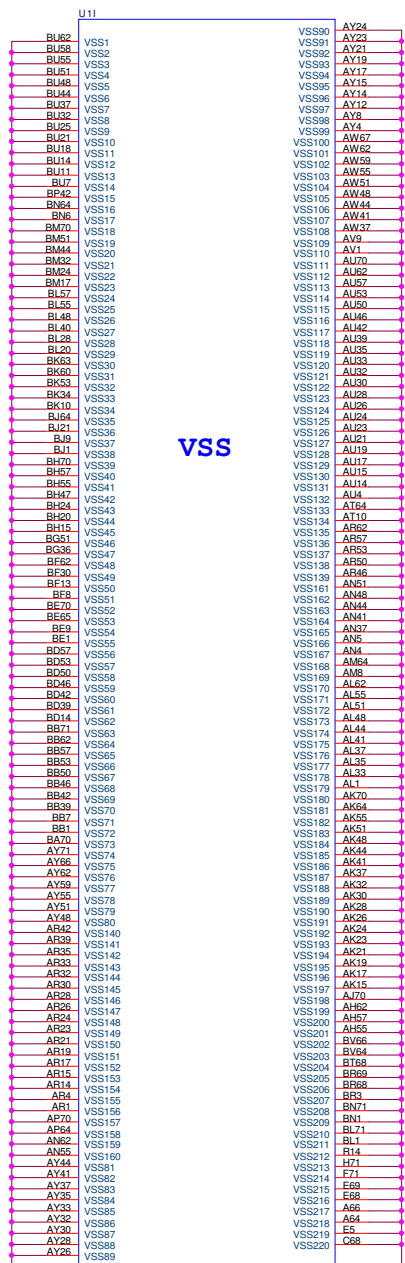
CPU CORE SUPPLY

Close to CPU

add 7pcs Caps to follow Design guide

add 7pcs Caps to follow Design guide

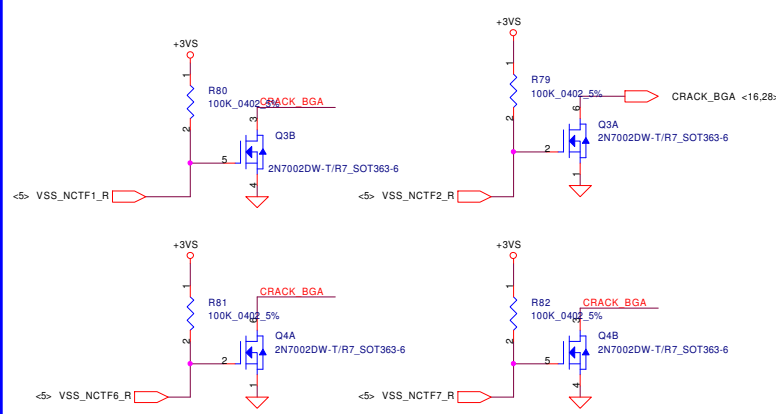
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VSS

VSS

BGA Ball Cracking Prevention and Detection



INTEL_AUBURNDALE_1288

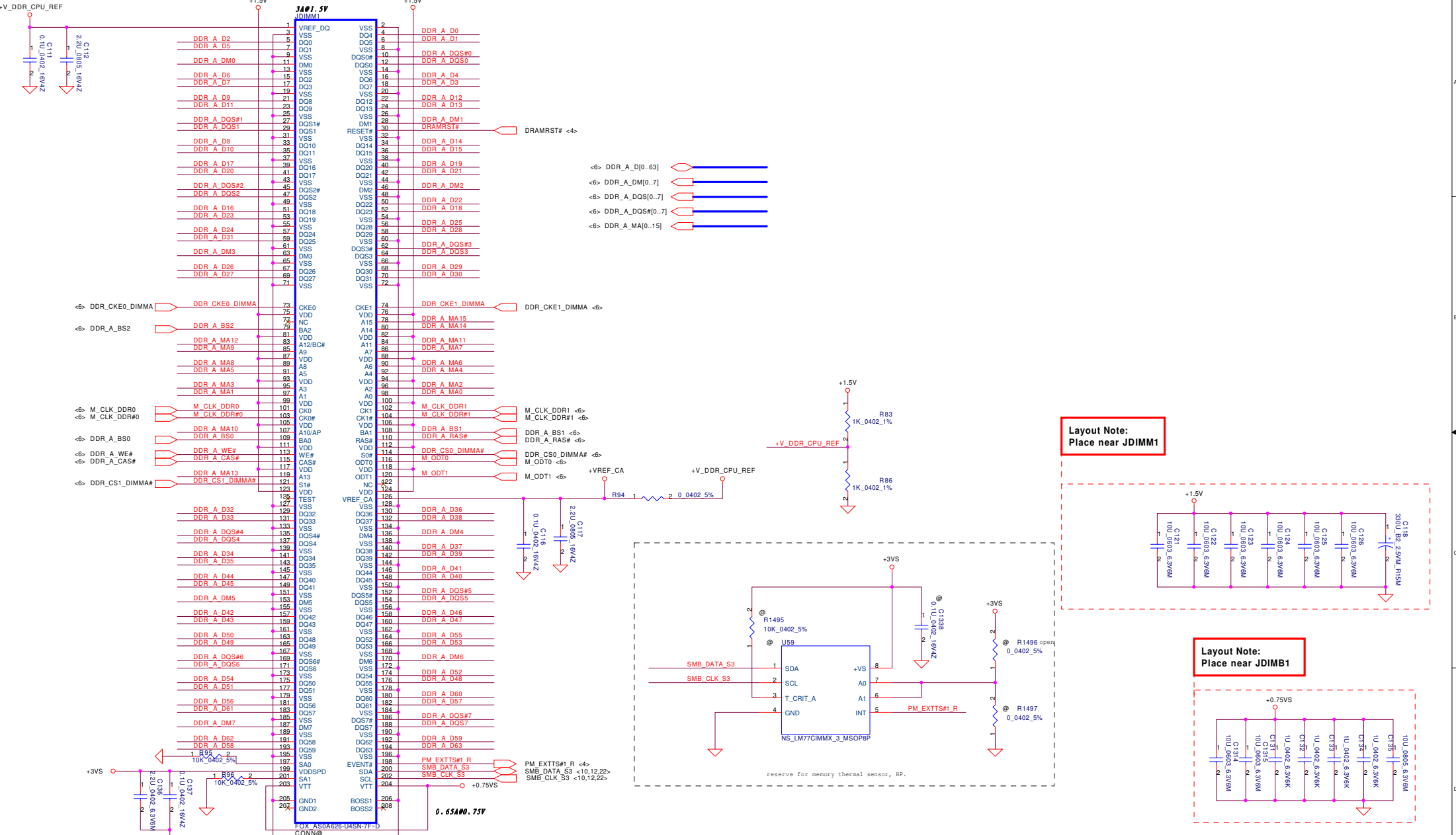
INTEL_AUBURNDALE_1288

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	Auburndale(5/5)-GND/Bypass	
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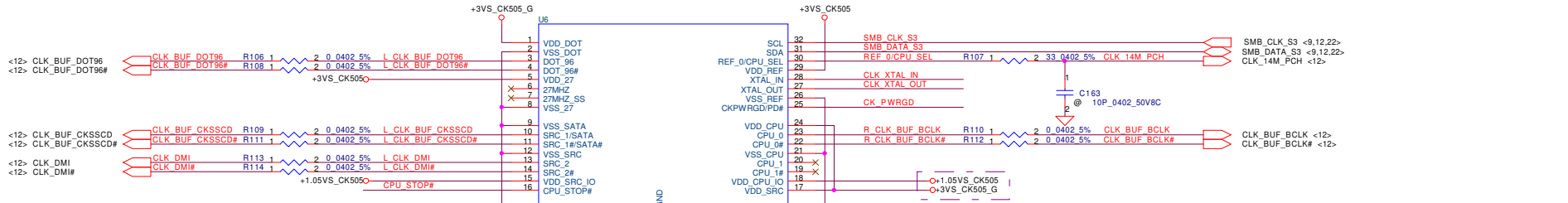
DDR3 SO-DIMM A



Layout Note:
Place near JDIMM1

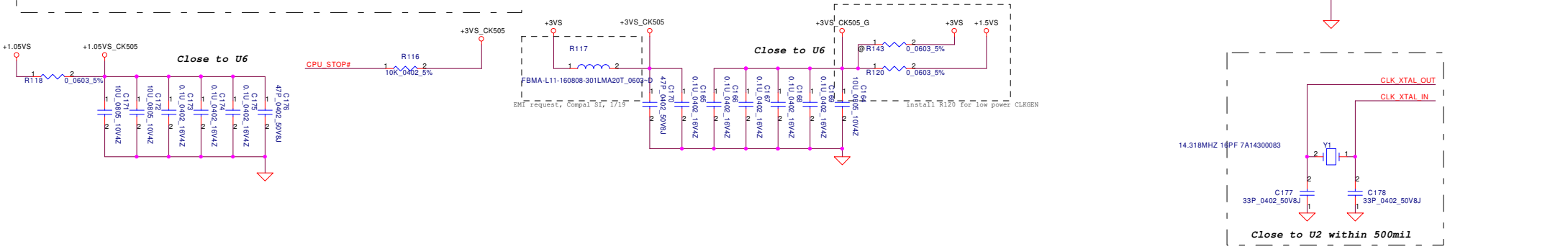
Layout Note:
Place near JDIMB1

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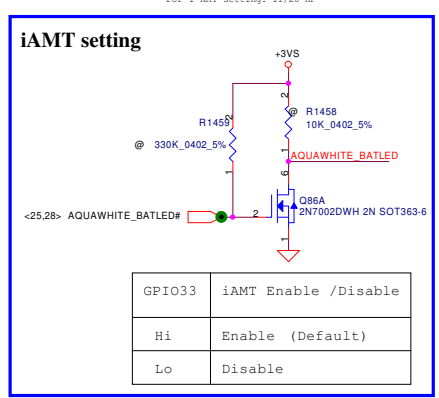
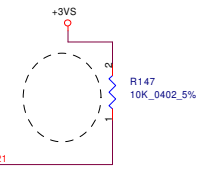
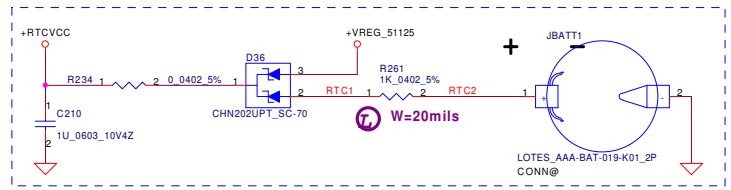
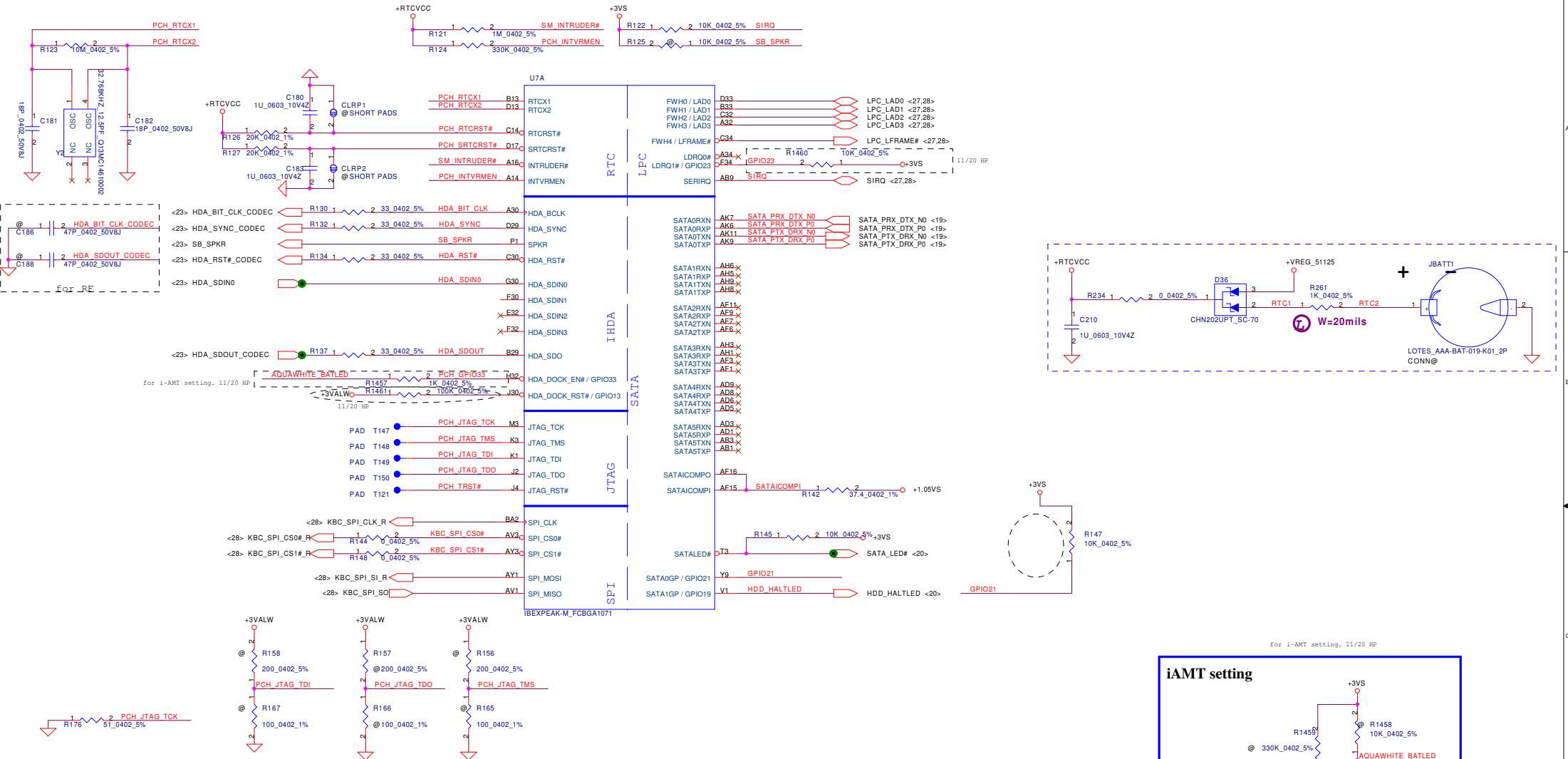


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

2nd Source :
 IDT ICS9LV53197BKFLT MLF 32P
 REALTEK RTM890N-632-VB-GRT QFN 32P



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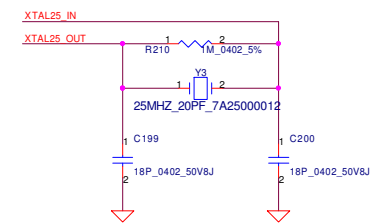
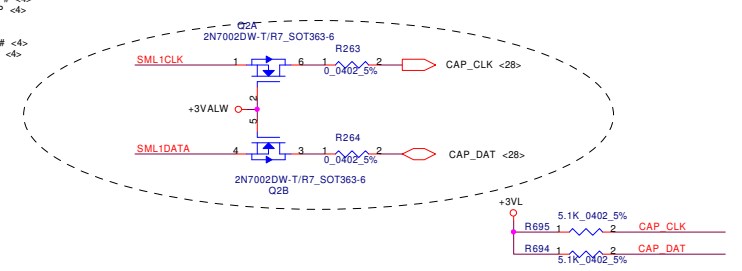
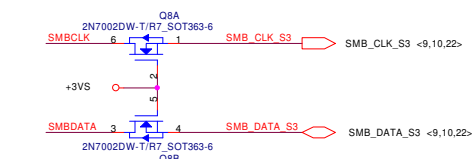
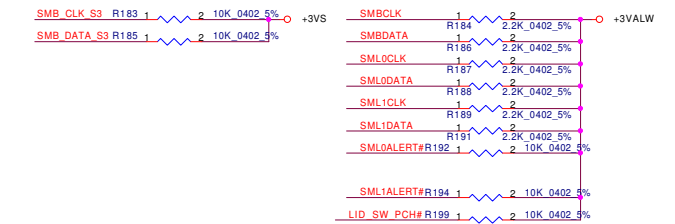
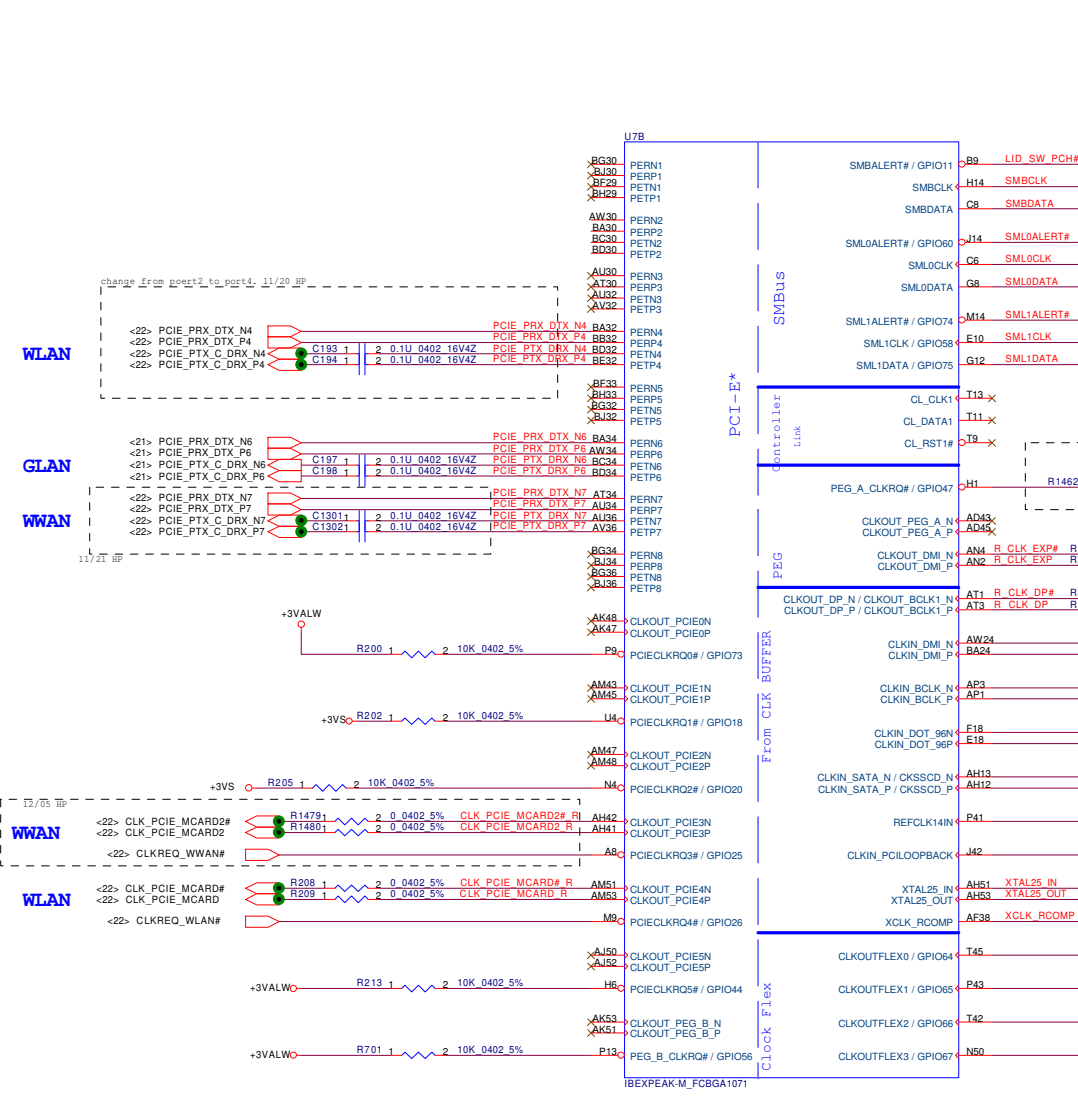
GPIO33	iAMT Enable /Disable
Hi	Enable (Default)
Lo	Disable

for i-AMT setting, 11/20 HP

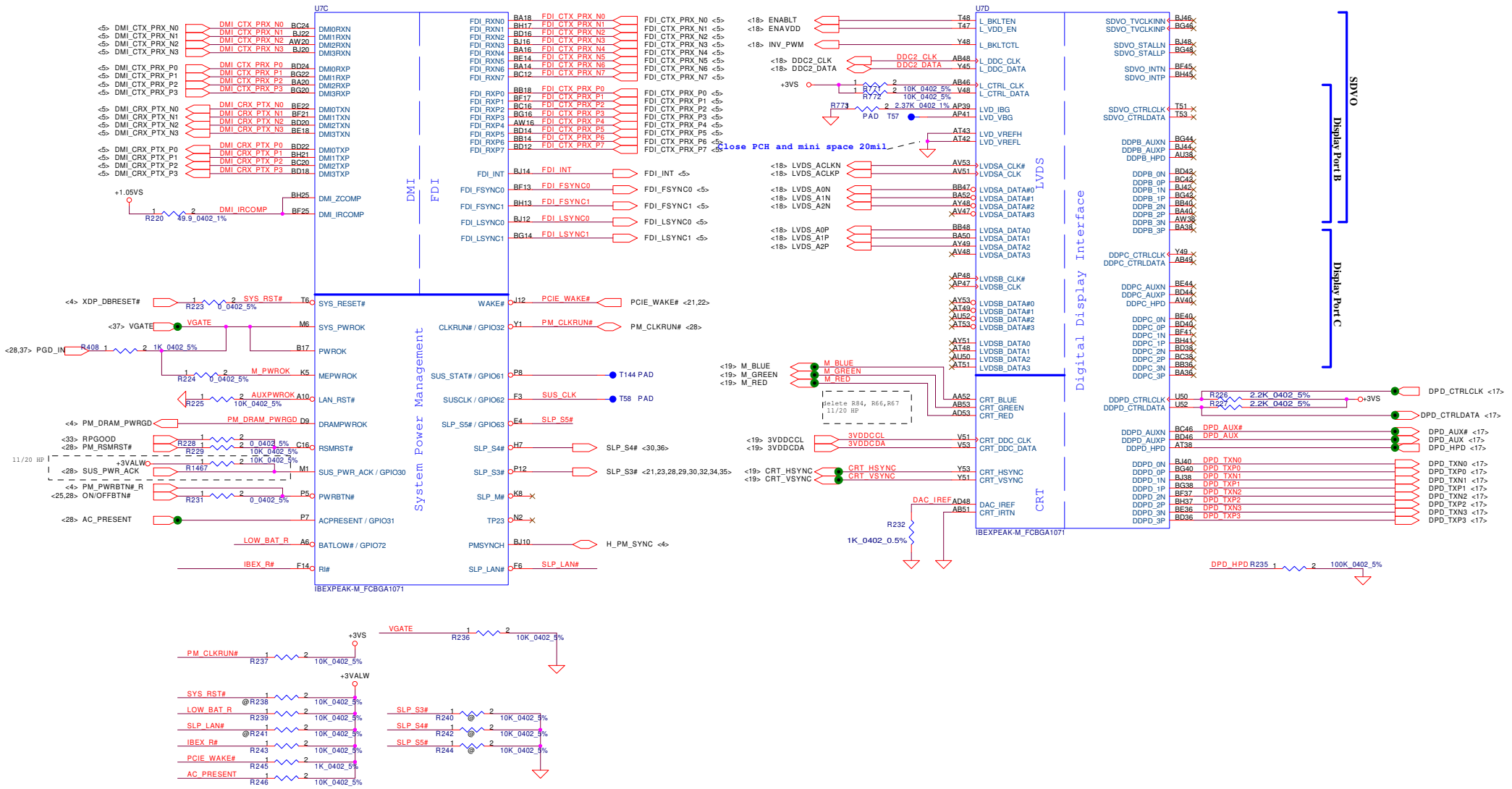
for i-AMT setting, 11/20 HP

PCH Pin	Pre-Production Units			Production
	Ref.	ES1	ES2	
PCH_JTAG_TDO	R157	Unstuff	200 ohm	Unstuff
	R166	Unstuff	100ohm	Unstuff
PCH_JTAG_TDI	R158	200 ohm	200 ohm	Unstuff
	R167	100ohm	100ohm	Unstuff
PCH_JTAG_TMS	R156	200 ohm	200 ohm	Unstuff
	R165	100ohm	100ohm	Unstuff
PCH_JTAG_TCK	R176	51 ohm 5%	51 ohm 5%	51 ohm 5%

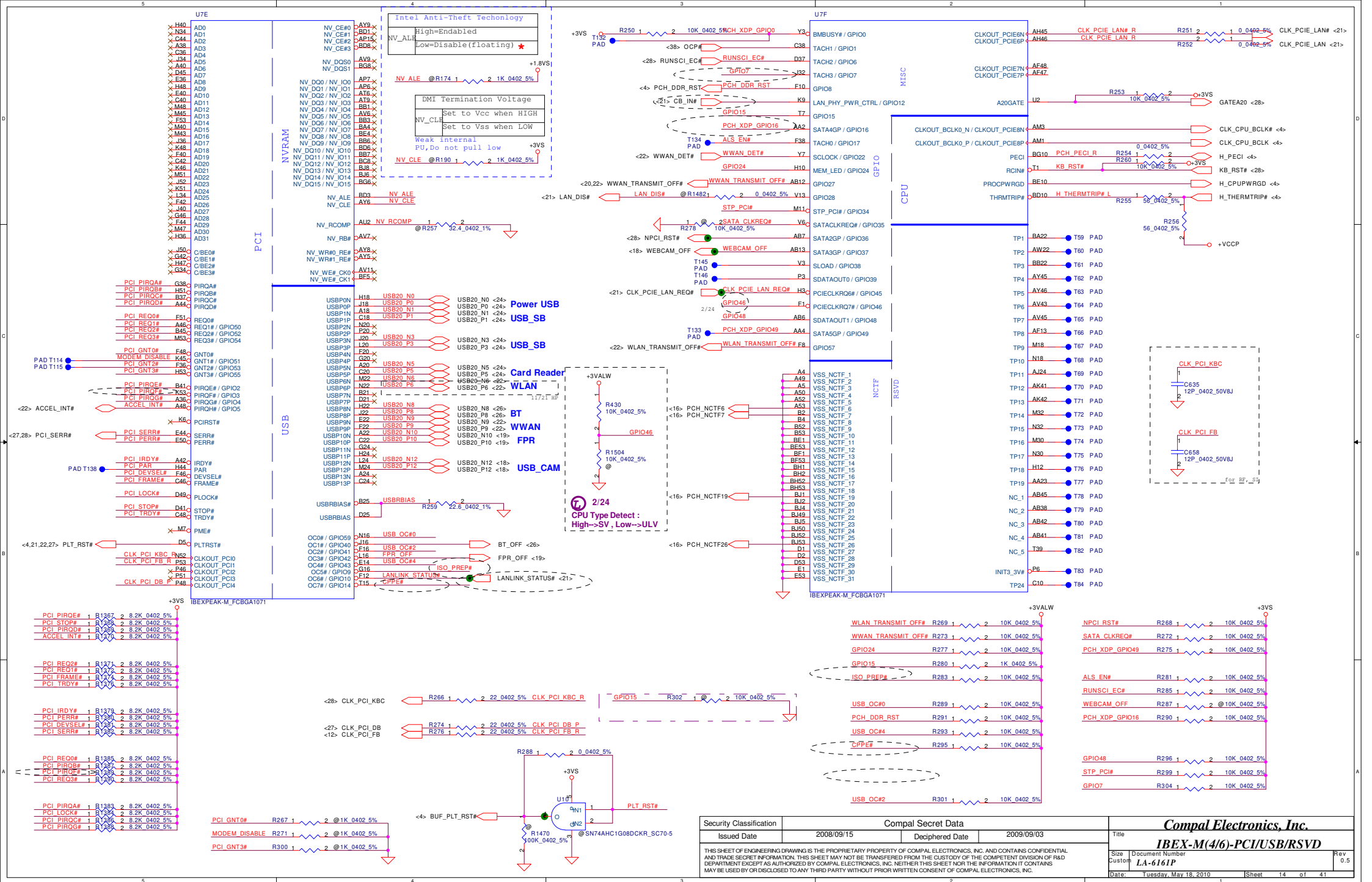
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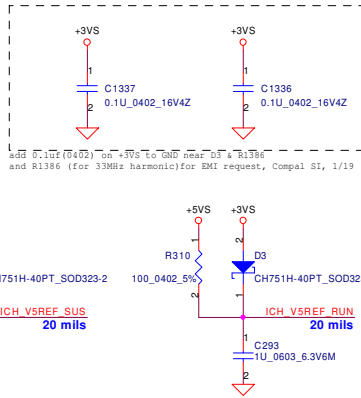
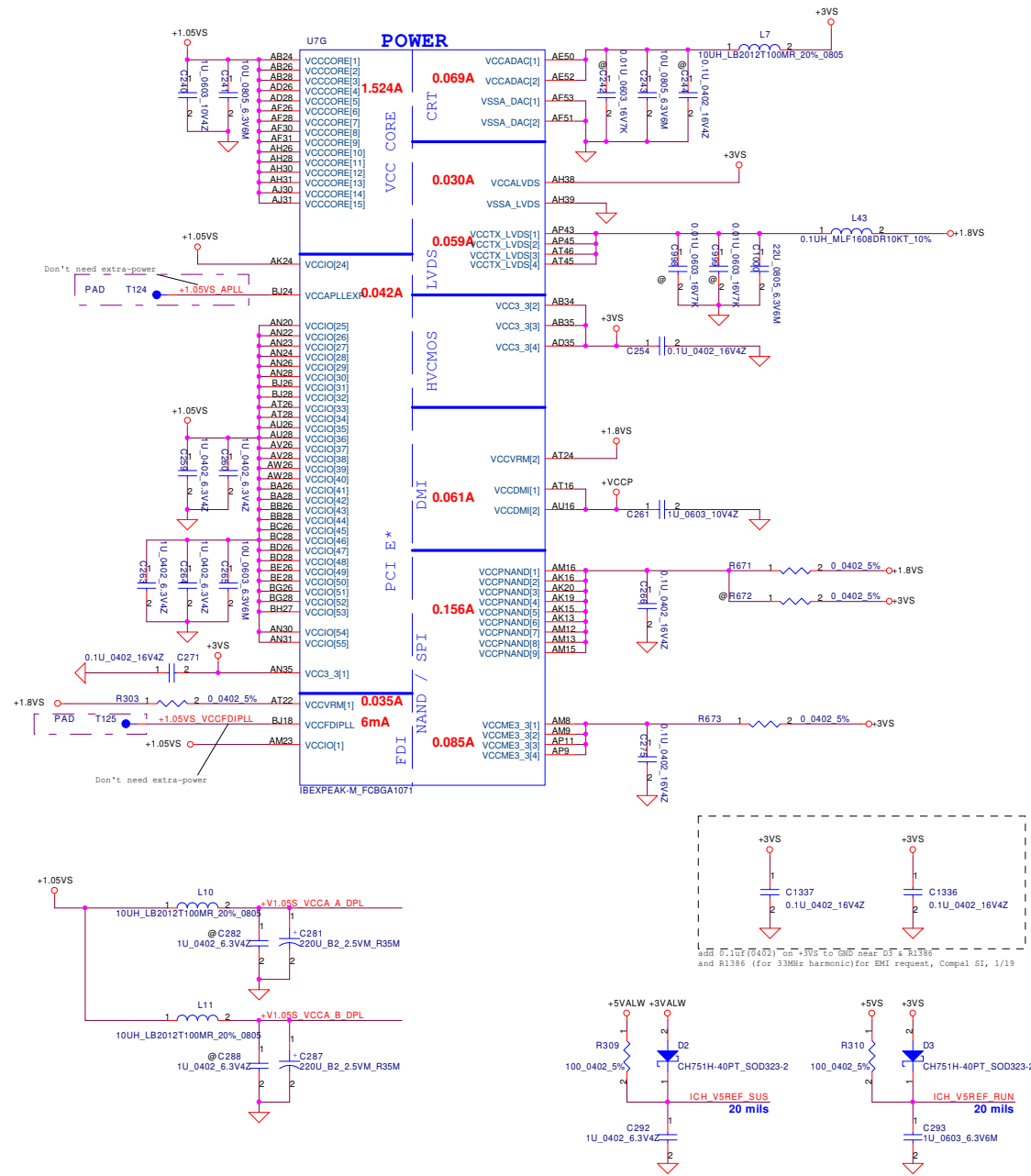
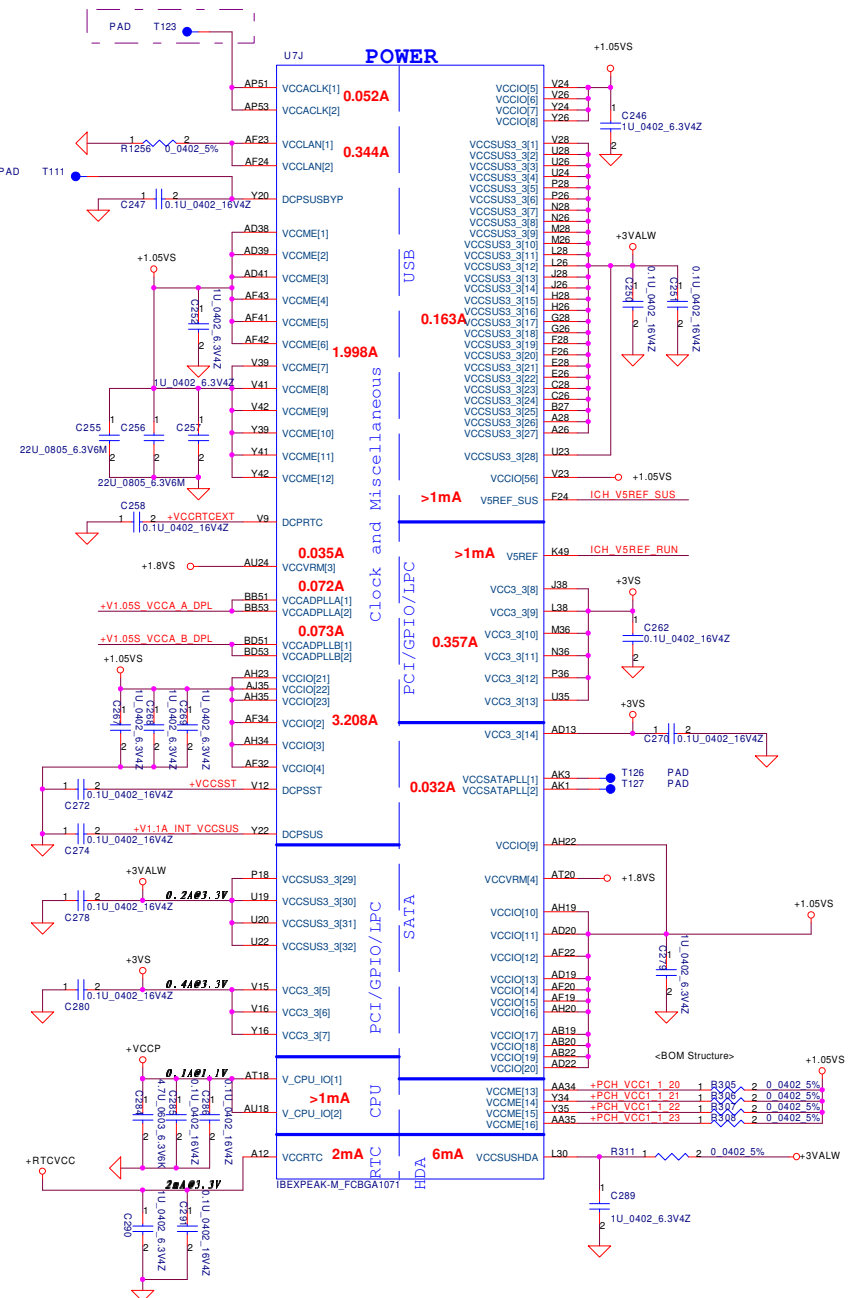
Security Classification	Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2009/09/03	IBEX-M(2/6)-PCI-E/SMBUS/CLK
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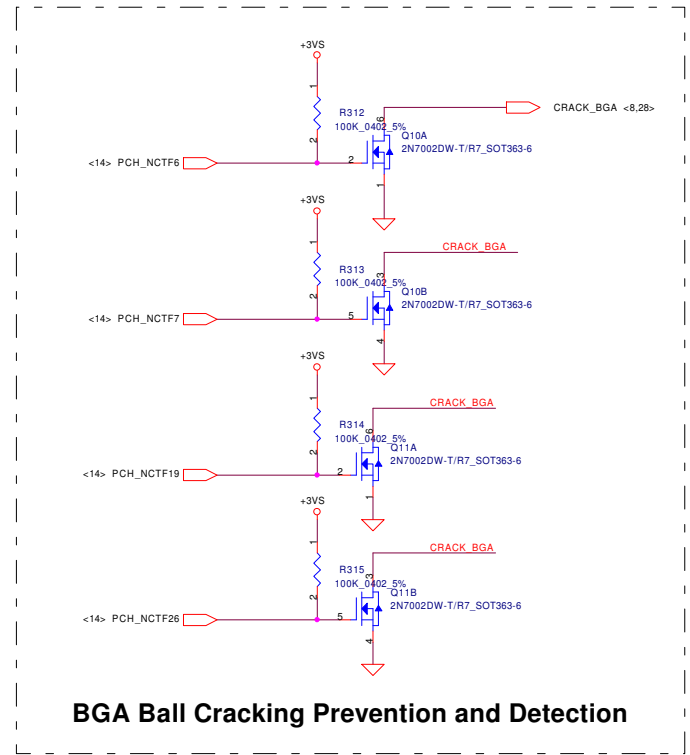
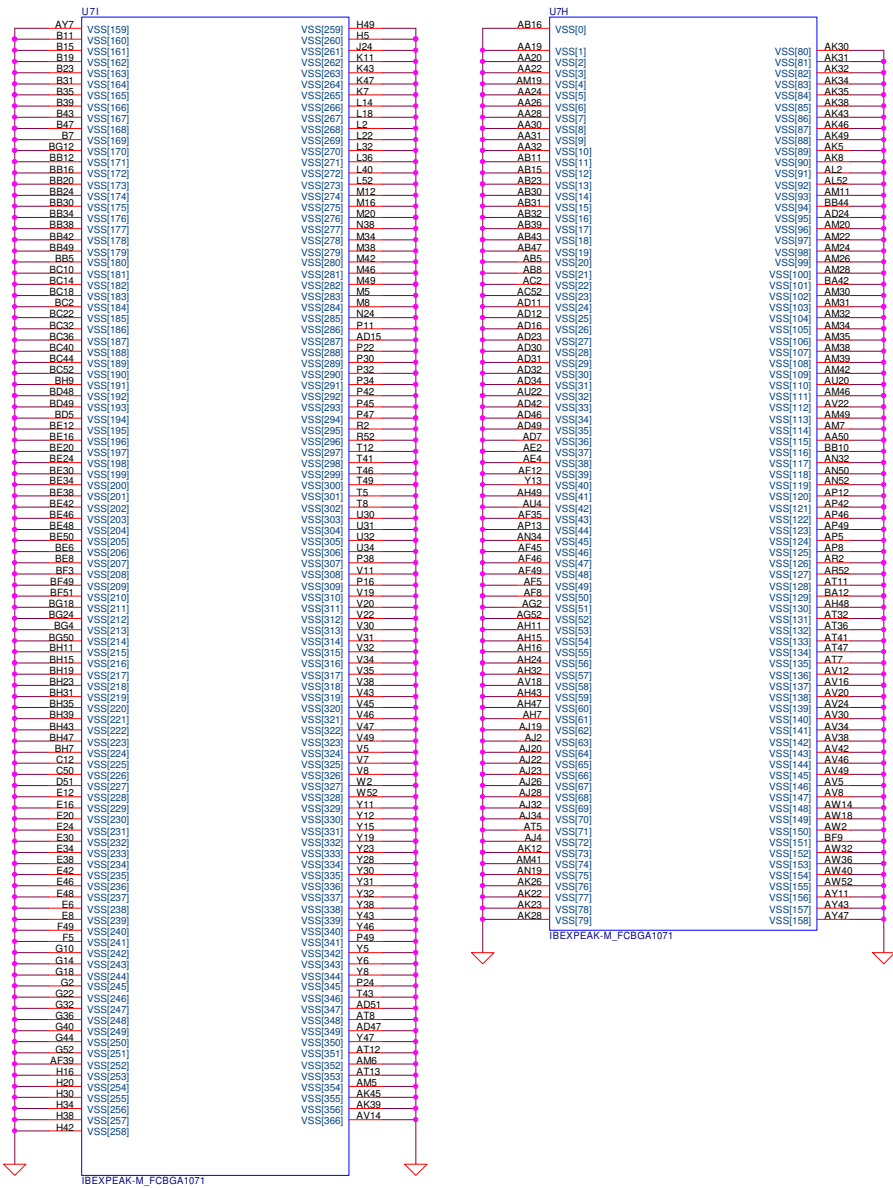
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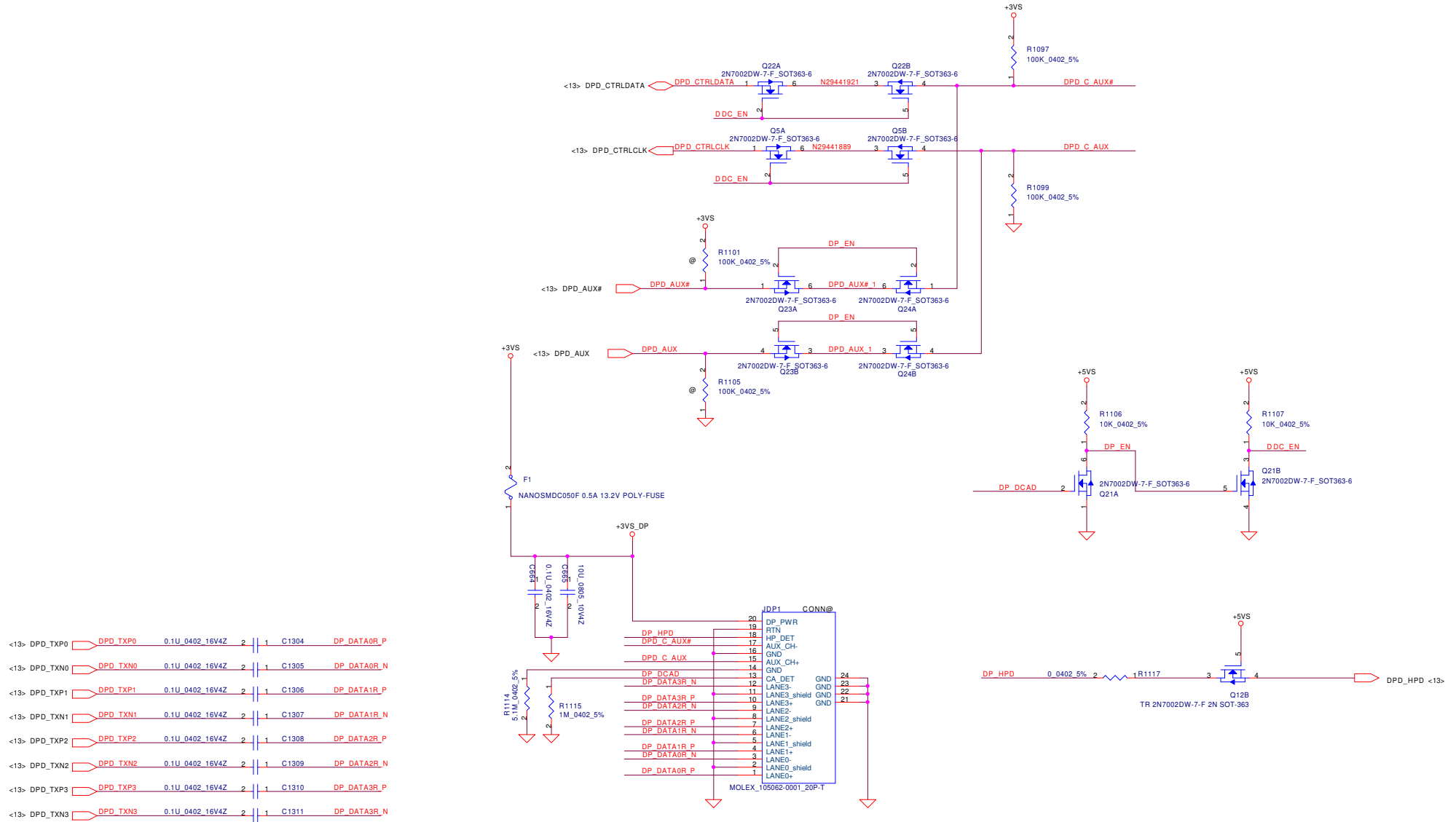
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			Customer	LA-6161P	0.5
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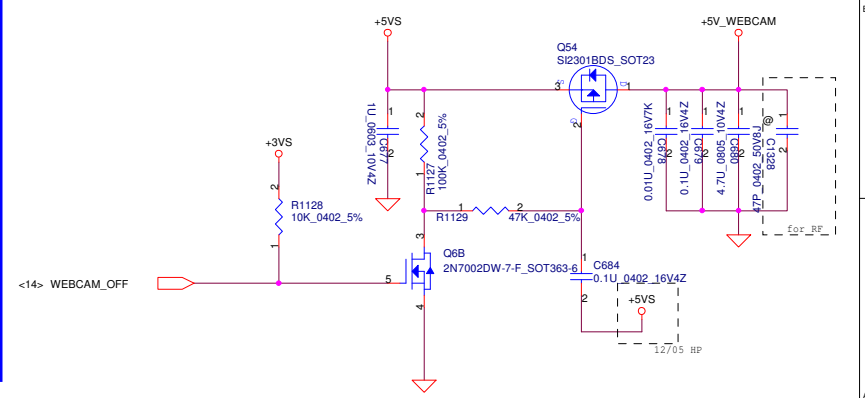
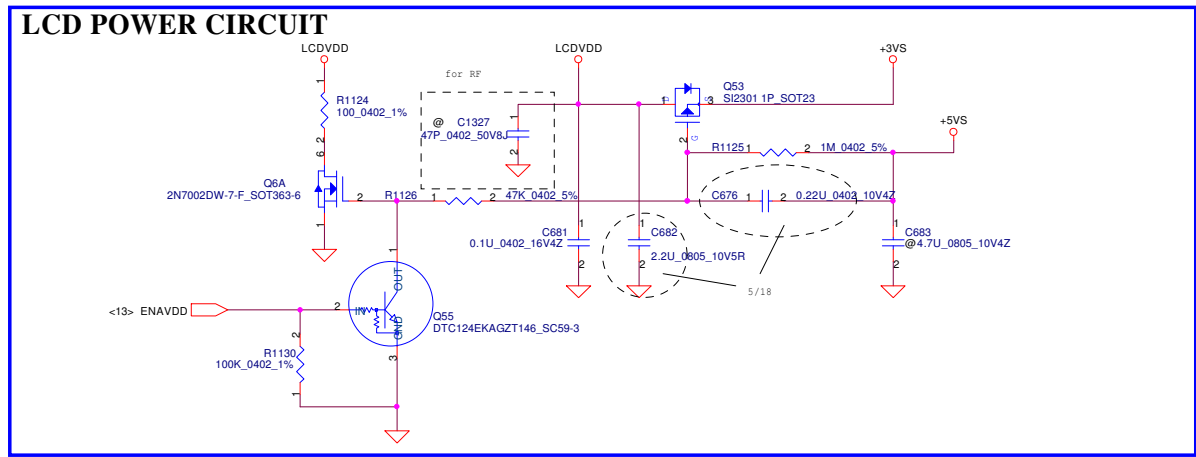
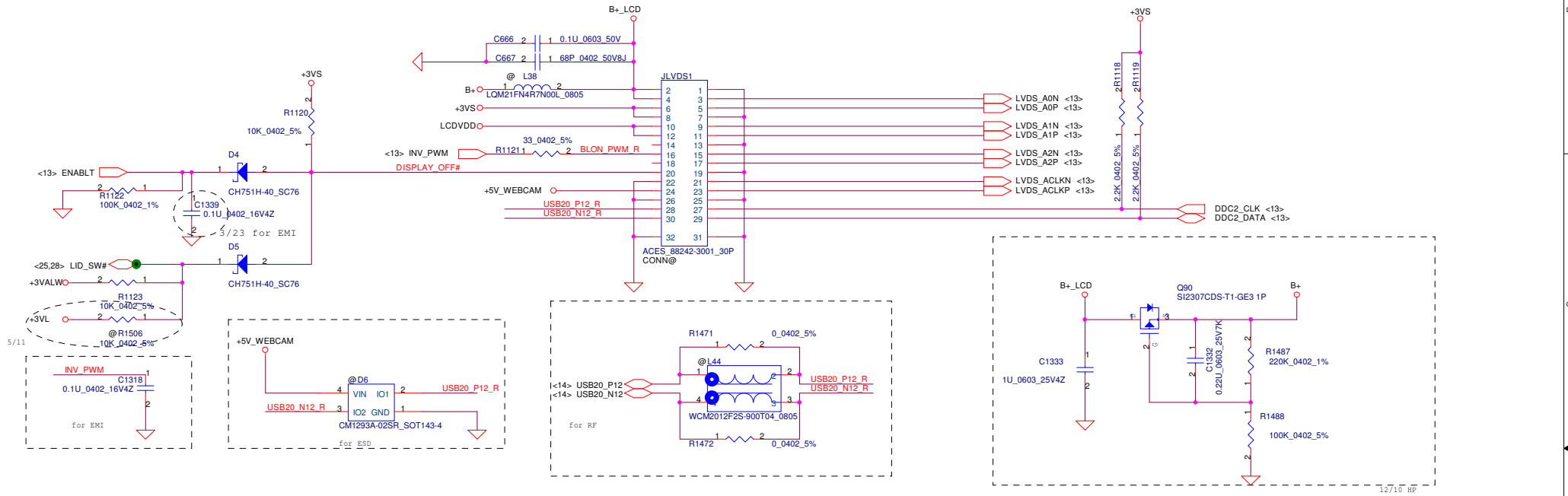


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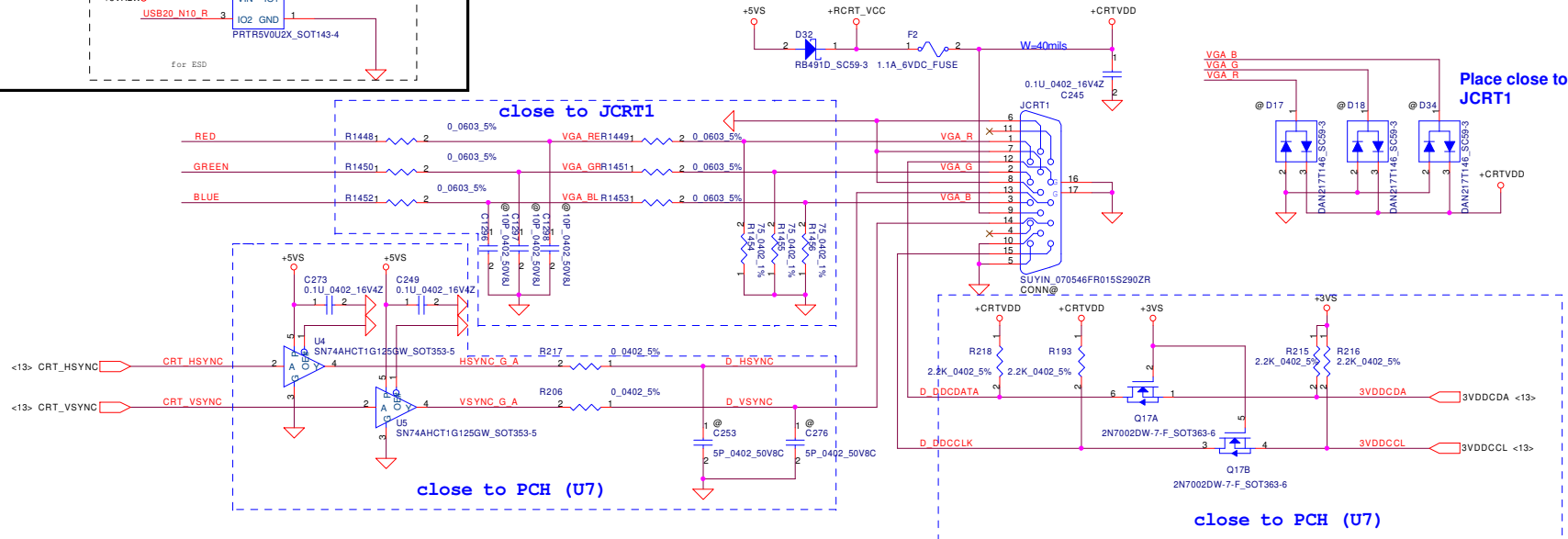
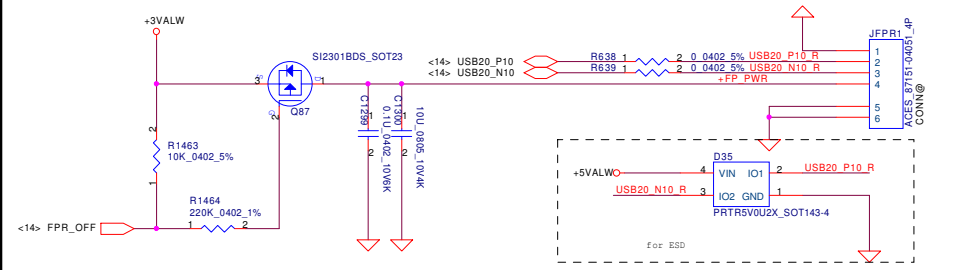
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Issued Date	2009/08/03	Deciphered Date	
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LED/PANEL BD. CONN.

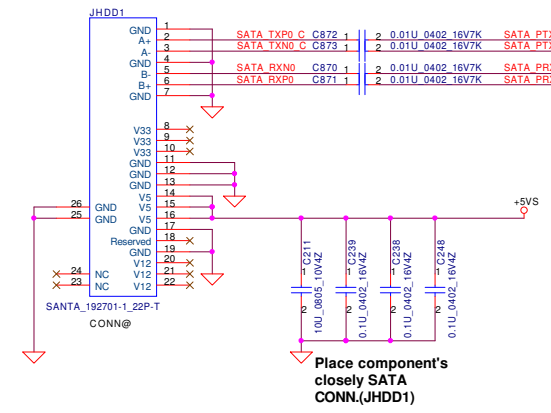


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Issued Date	2009/08/03	Deciphered Date	2009/09/03	LCD CONN & Q-Switch & GPIO Ext.	
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				LA-6161P	Rev 0.5
Date: Tuesday, May 18, 2010				Sheet 18	of 41

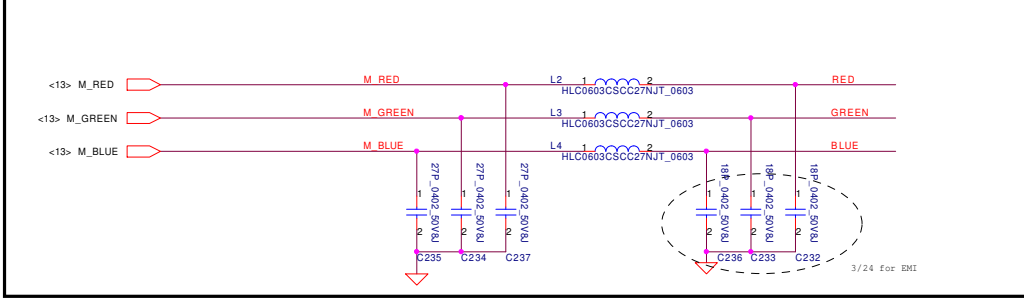
Finger printer



2.5' SATA HDD Connector

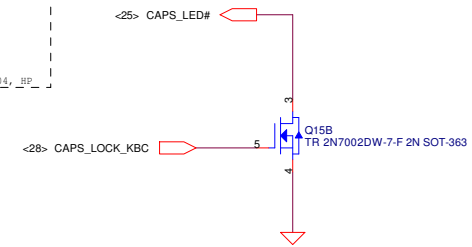
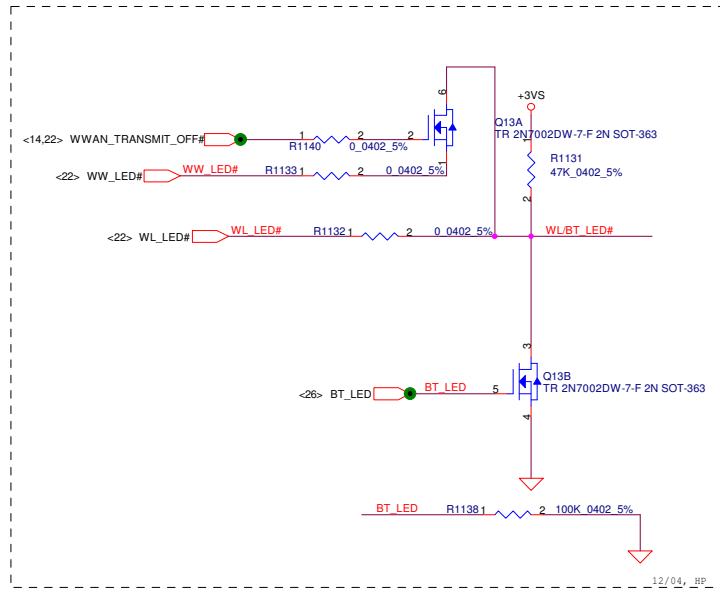
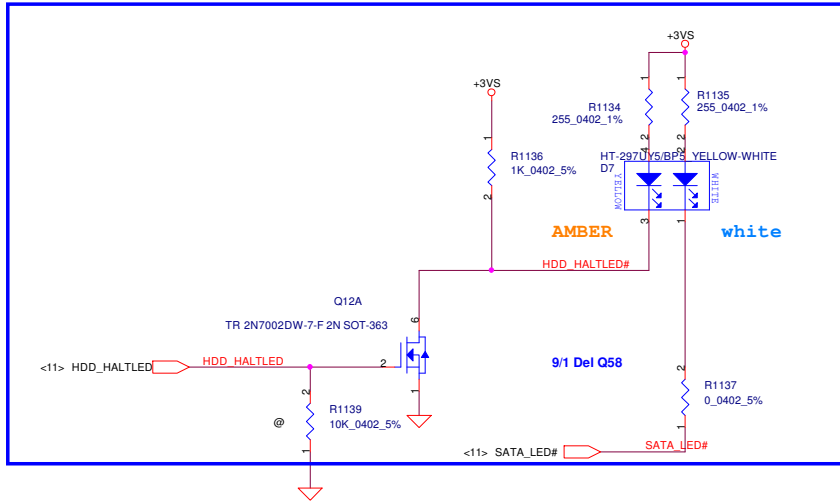


CRT Termination/EMI Filter close to PCH (U7)

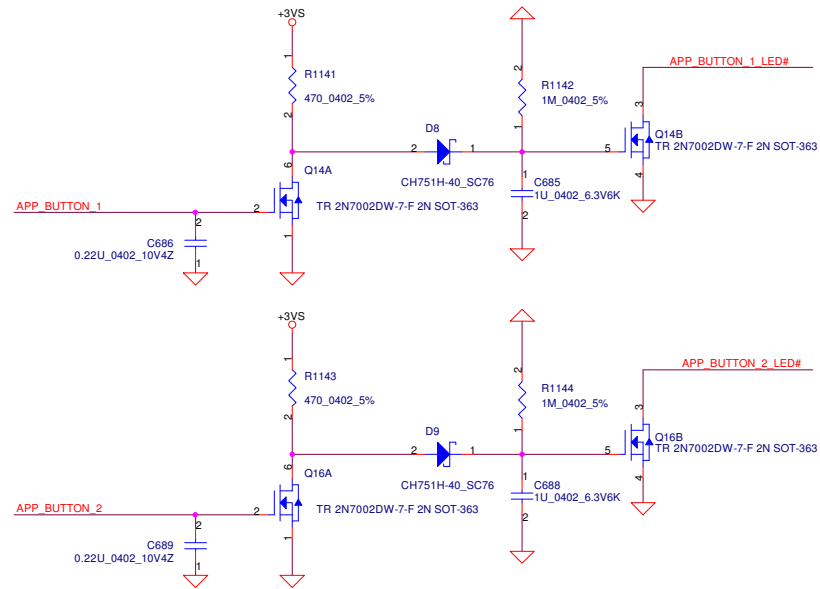
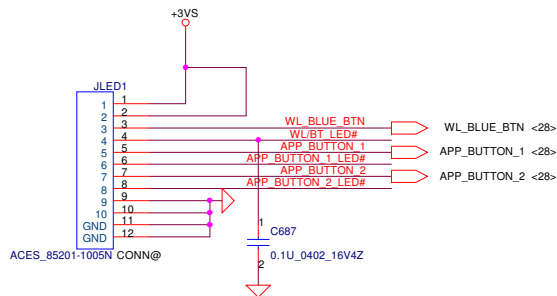


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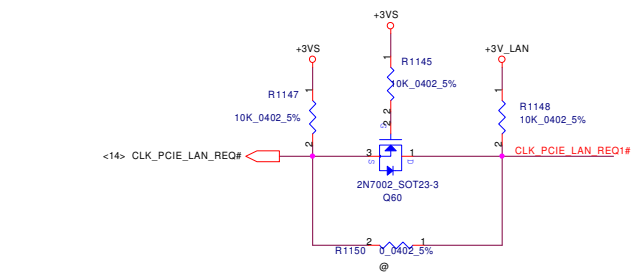
HDD active LED



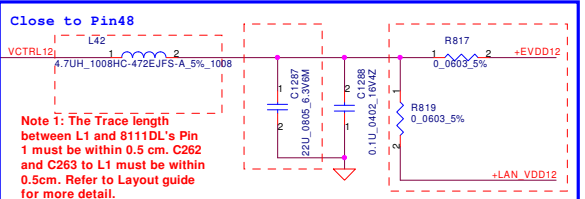
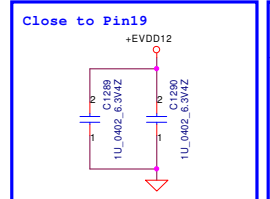
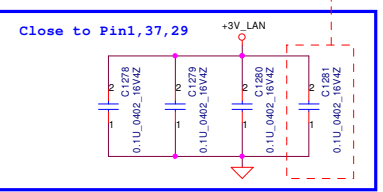
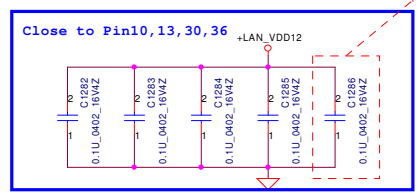
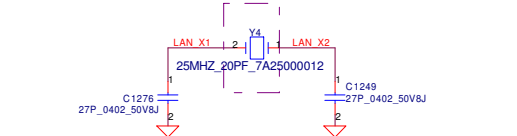
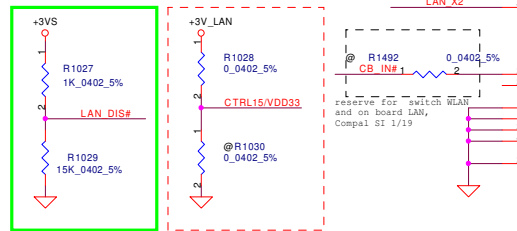
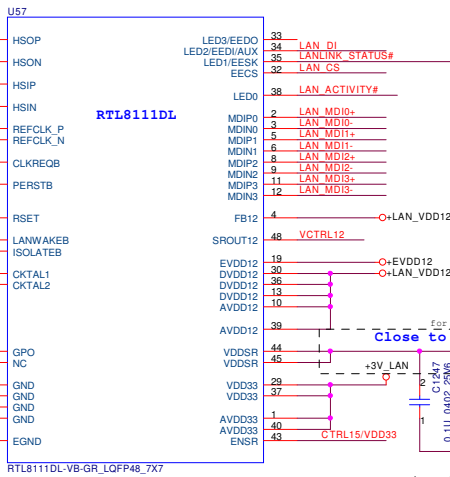
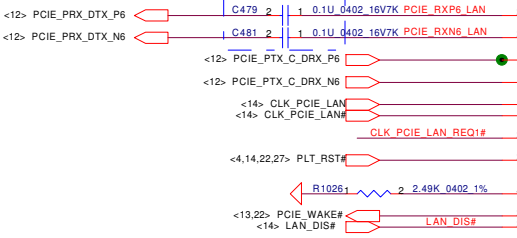
To LED small board



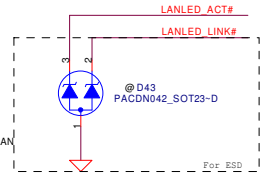
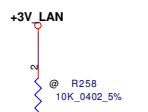
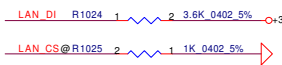
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Issued Date	2009/08/03	Deciphered Date	2009/09/03		
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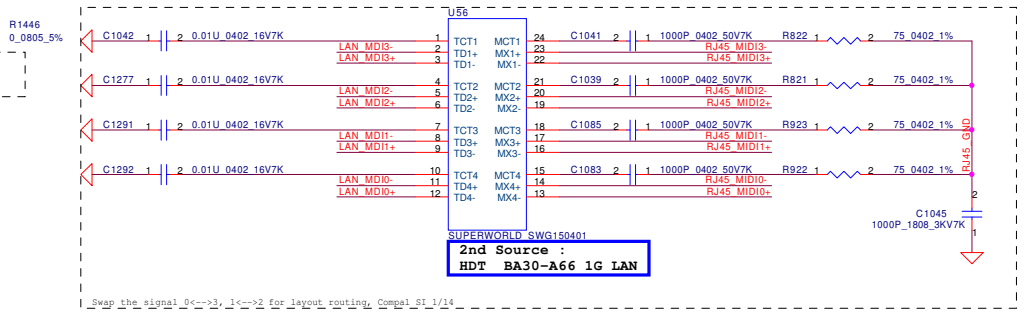
Place Close to Chip



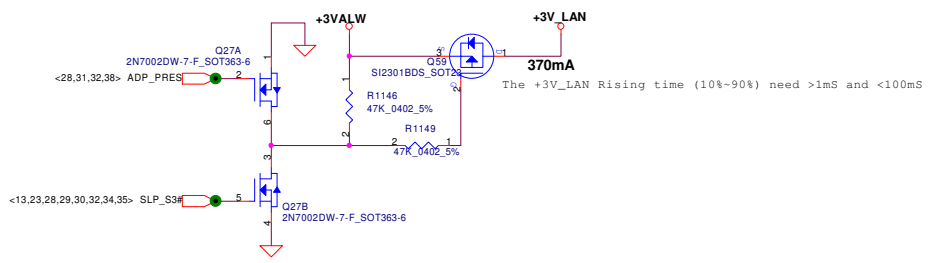
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C262 and C263 to L1 must be within 0.5cm. Refer to Layout guide for more detail.



10/100 and Giga Transformer



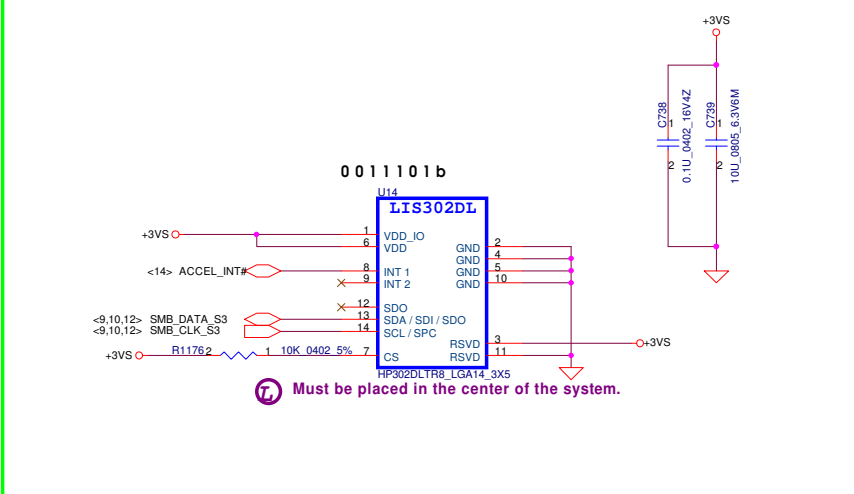
2nd Source : HDT BA30-A66 1G LAN



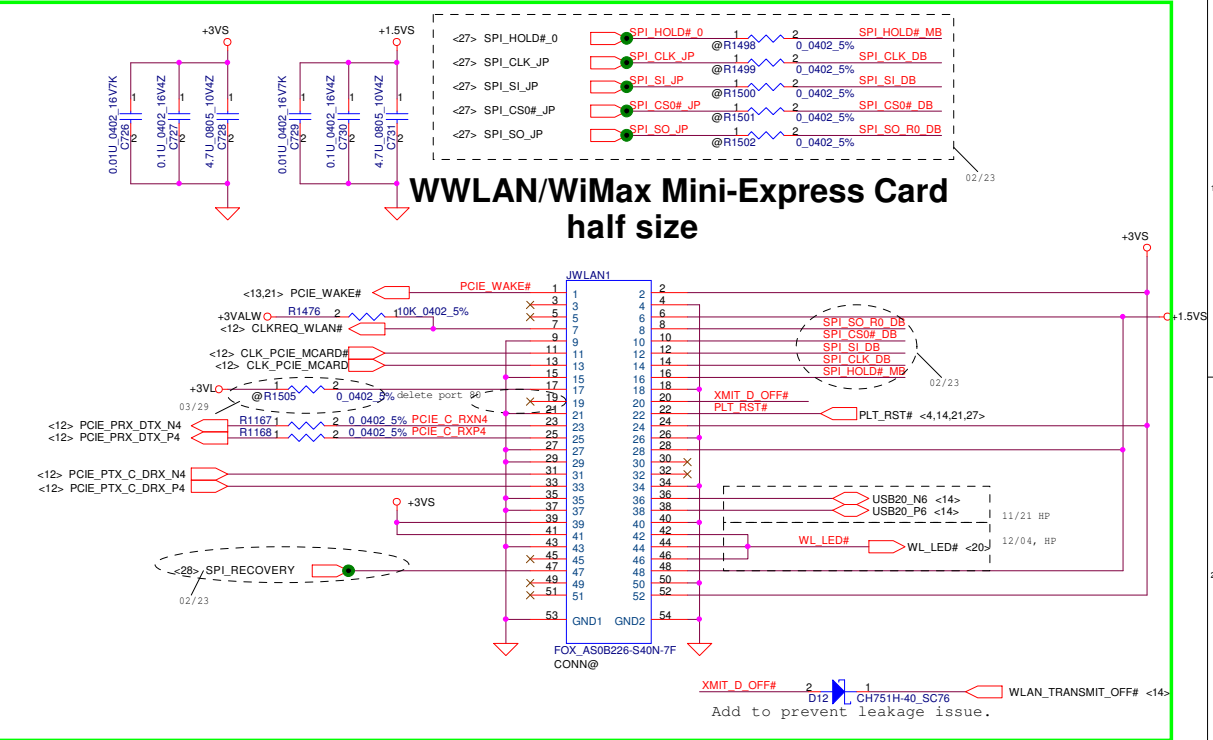
The +3V_LAN Rising time (10%-90%) need >1ms and <100ms

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			Cust	LA-6161P	0.5
Date:	Tuesday, May 18, 2010	Sheet	21	of	41

ACCELEROMETER

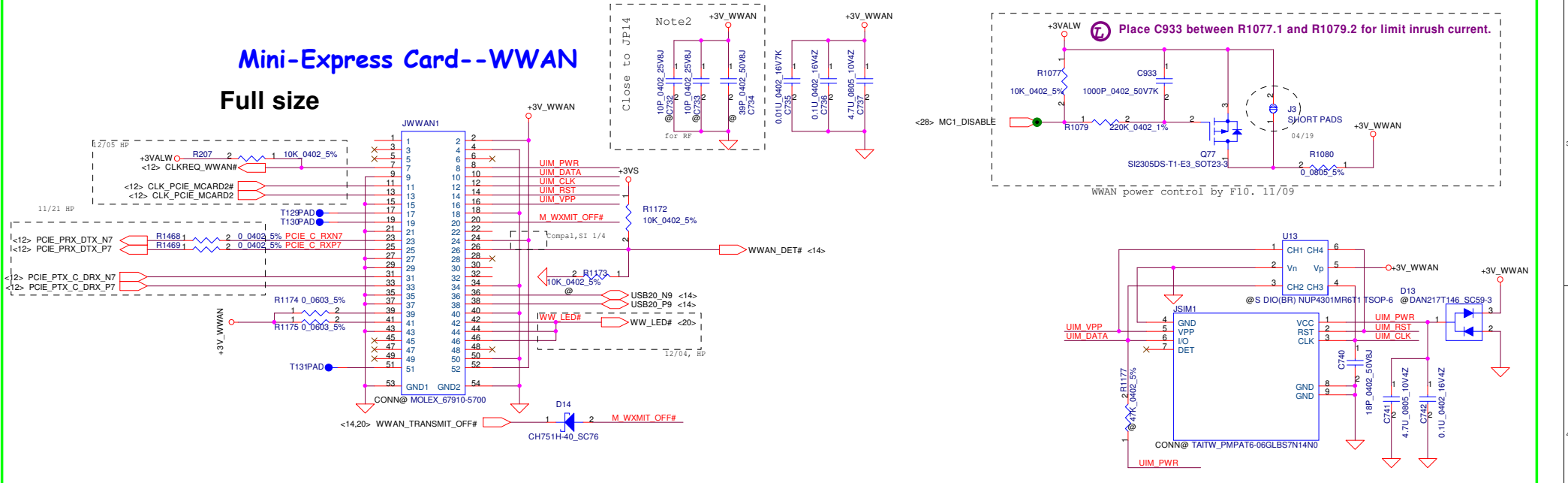


WWLAN/WiMax Mini-Express Card half size

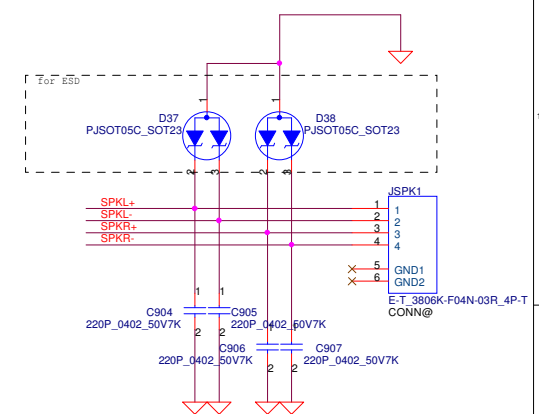
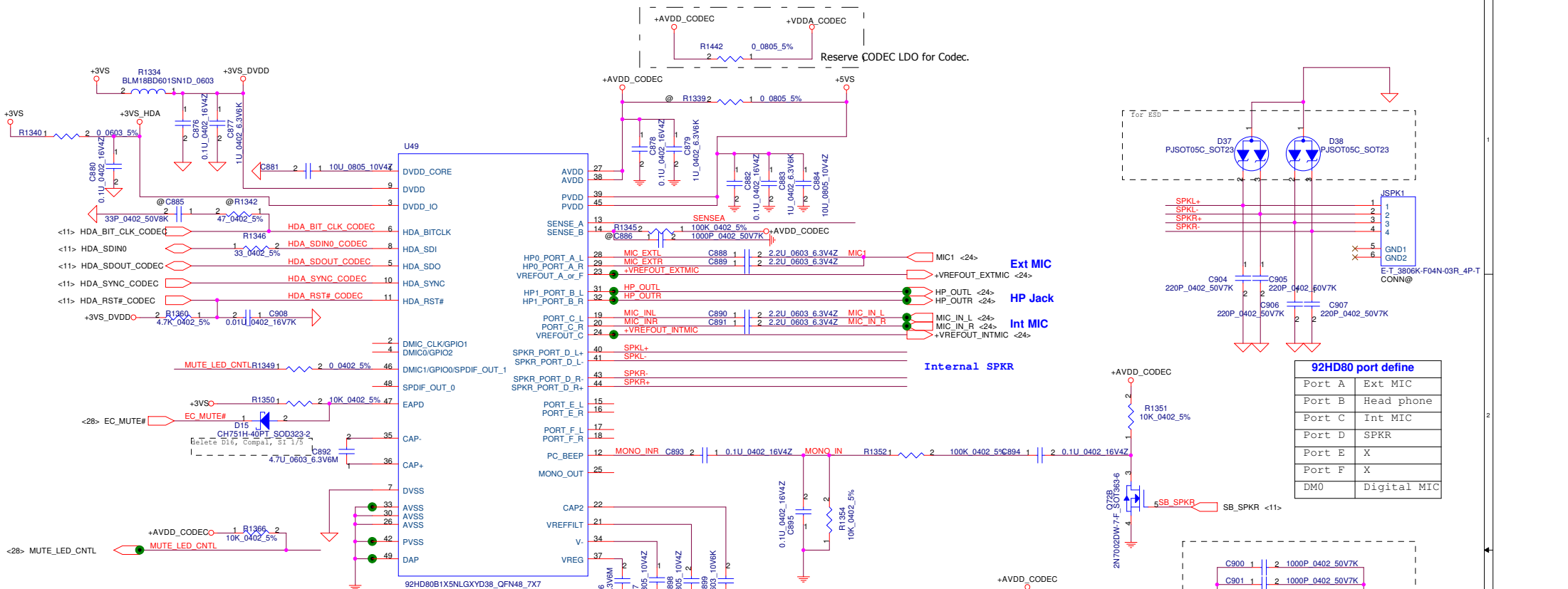


Mini-Express Card--WWAN

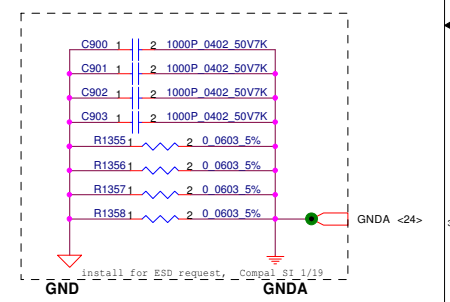
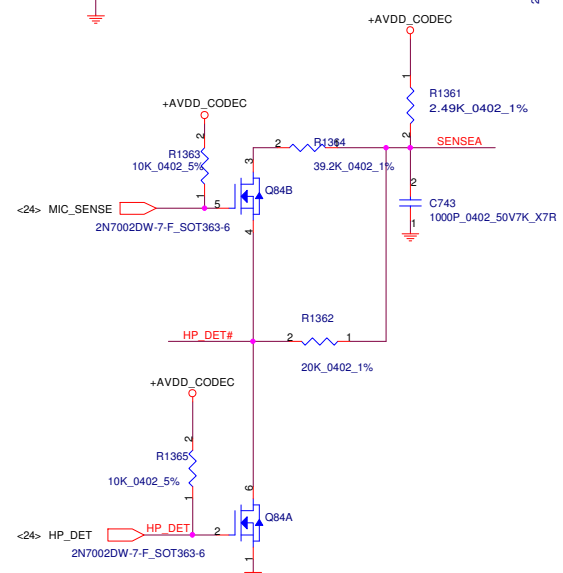
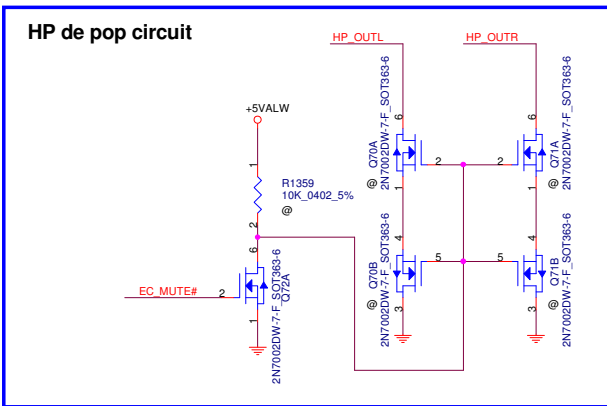
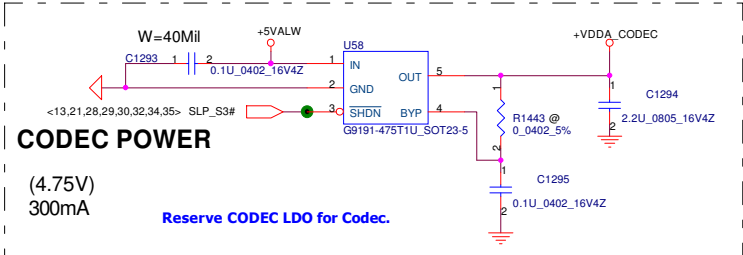
Full size



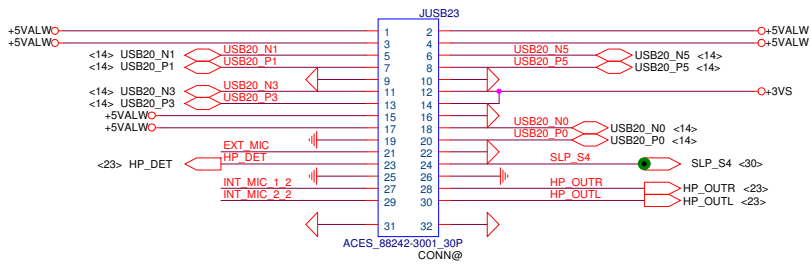
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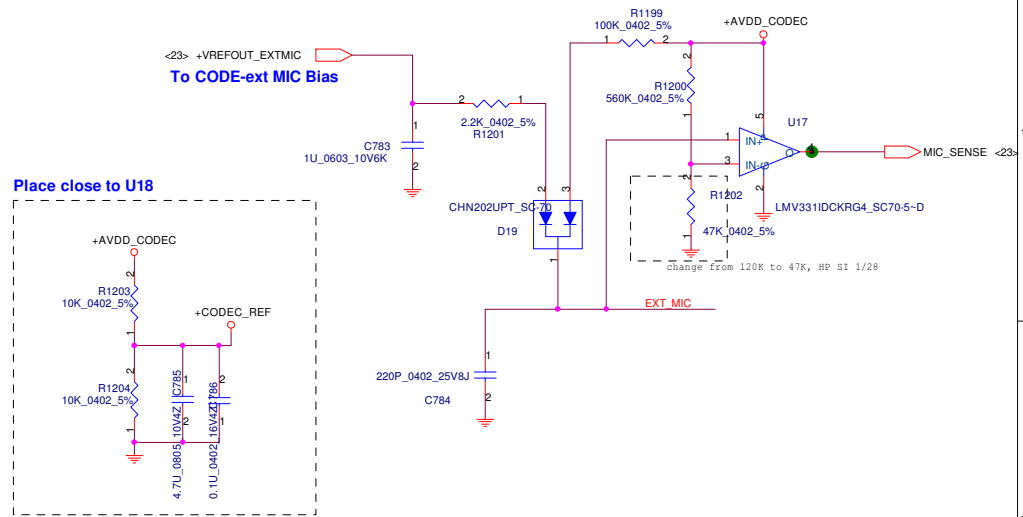
92HD80 port define	
Port A	Ext MIC
Port B	Head phone
Port C	Int MIC
Port D	SPKR
Port E	X
Port F	X
DM0	Digital MIC



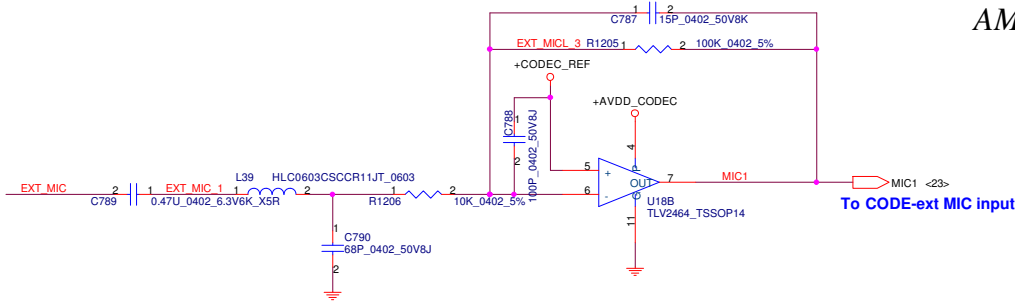
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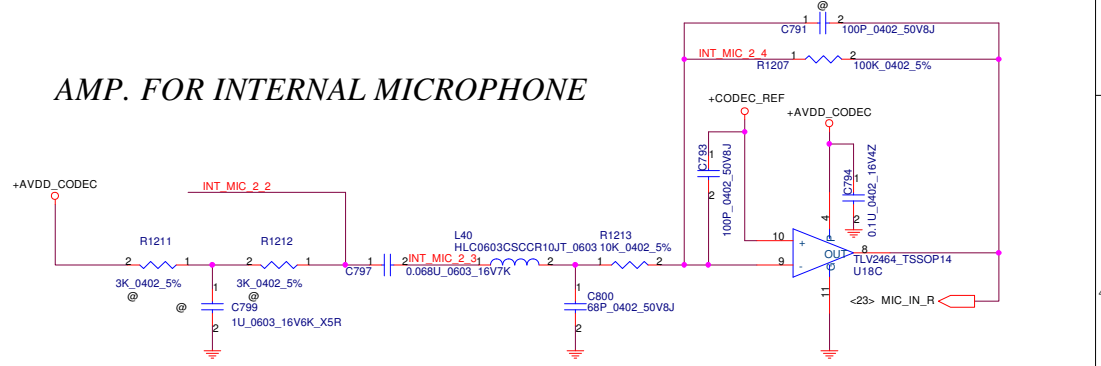
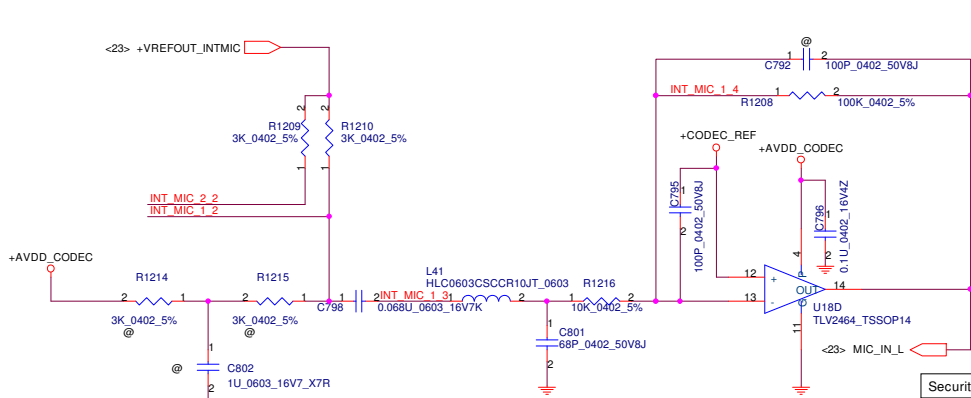
USB I/O connx2 , Audio JACK
Card reader transfer conn



AMP. FOR EXTERNAL MICROPHONE

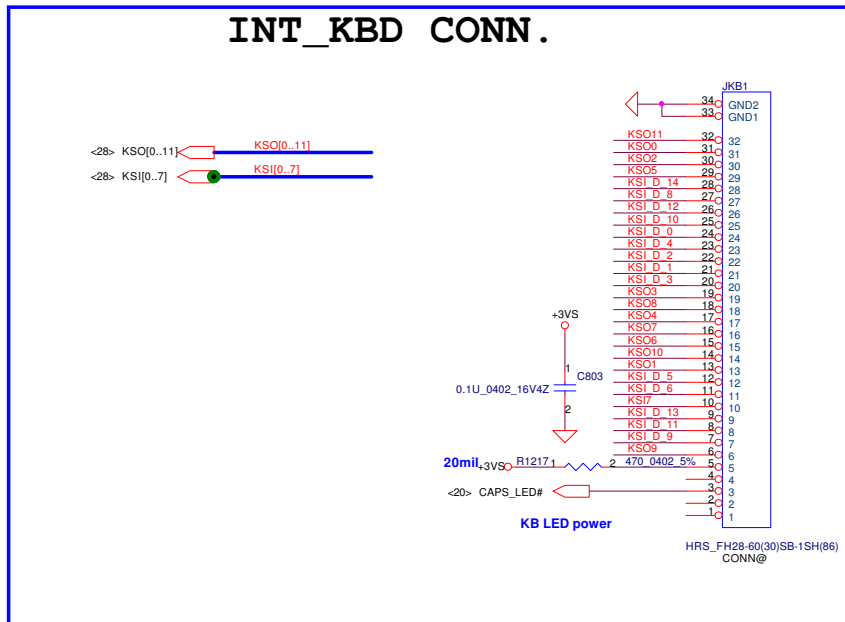


AMP. FOR INTERNAL MICROPHONE



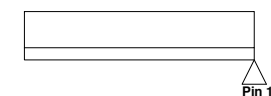
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Issued Date	2009/08/03	Deciphered Date	2009/09/03	Compal Electronics, Inc.		
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INT_KBD CONN.

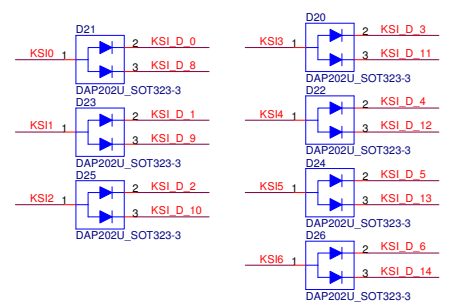


For EMI

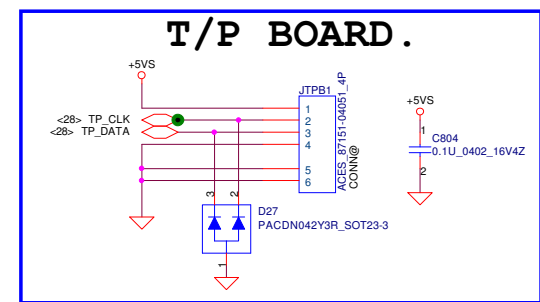
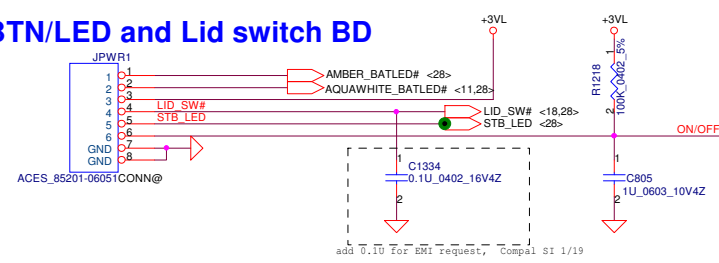
KSO11	@C620	1	2	100P_0402_50V8J
KSO0	@C656	1	2	100P_0402_50V8J
KSO2	@C624	1	2	100P_0402_50V8J
KSO5	@C621	1	2	100P_0402_50V8J
KSI_D_14	@C622	1	2	100P_0402_50V8J
KSI_D_8	@C625	1	2	100P_0402_50V8J
KSI_D_12	@C626	1	2	100P_0402_50V8J
KSI_D_10	@C627	1	2	100P_0402_50V8J
KSI_D_0	@C630	1	2	100P_0402_50V8J
KSI_D_4	@C629	1	2	100P_0402_50V8J
KSI_D_2	@C631	1	2	100P_0402_50V8J
KSI_D_1	@C632	1	2	100P_0402_50V8J
KSI_D_3	@C633	1	2	100P_0402_50V8J
KSO3	@C634	1	2	100P_0402_50V8J
KSO8	@C641	1	2	100P_0402_50V8J
KSO4	@C637	1	2	100P_0402_50V8J
KSO7	@C657	1	2	100P_0402_50V8J
KSO6	@C638	1	2	100P_0402_50V8J
KSO10	@C639	1	2	100P_0402_50V8J
KSO1	@C640	1	2	100P_0402_50V8J
KSI_D_5	@C660	1	2	100P_0402_50V8J
KSI_D_6	@C642	1	2	100P_0402_50V8J
KSI7	@C659	1	2	100P_0402_50V8J
KSI_D_13	@C654	1	2	100P_0402_50V8J
KSI_D_11	@C744	1	2	100P_0402_50V8J
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KSO9	@C724	1	2	100P_0402_50V8J



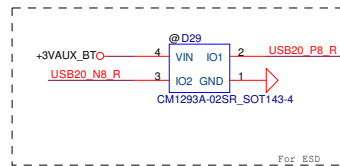
Pin1 reserve , so net name is reserve for Fossil down contact



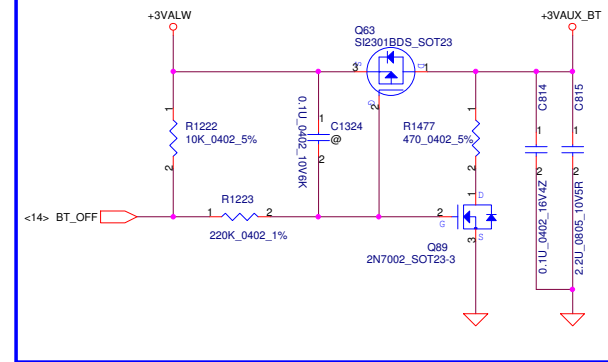
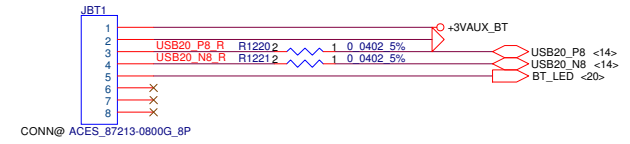
Power BTN/LED and Lid switch BD



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Size	Document Number	Rev		0.5
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Date:	Tuesday, May 18, 2010	Sheet	25 of 41	



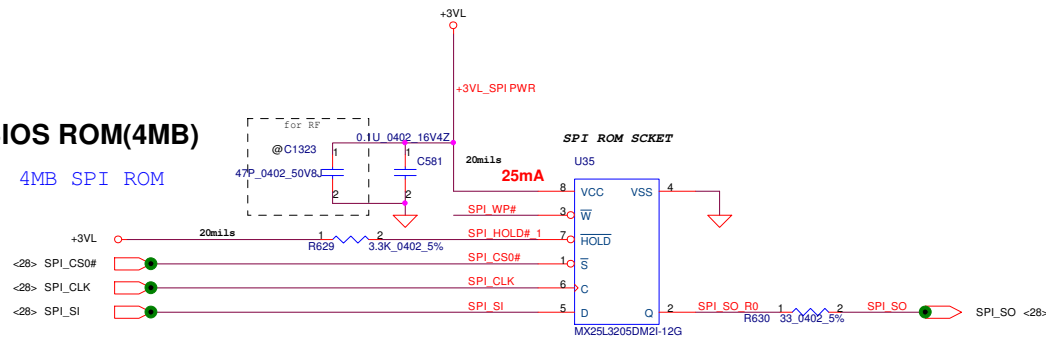
BT (SoftBreeze) Connector



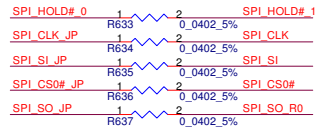
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Issued Date	2009/08/03	Deciphered Date	2009/09/03	Compal Electronics, Inc. USB & BT Connector	
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BIOS ROM(4MB)

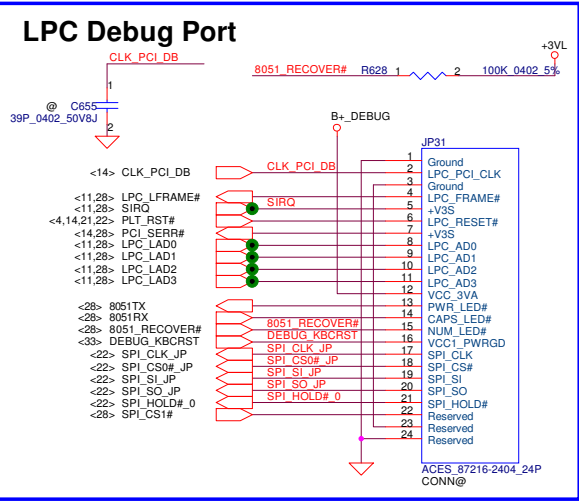
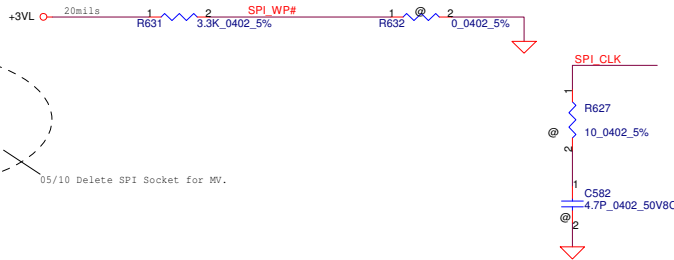
4MB SPI ROM



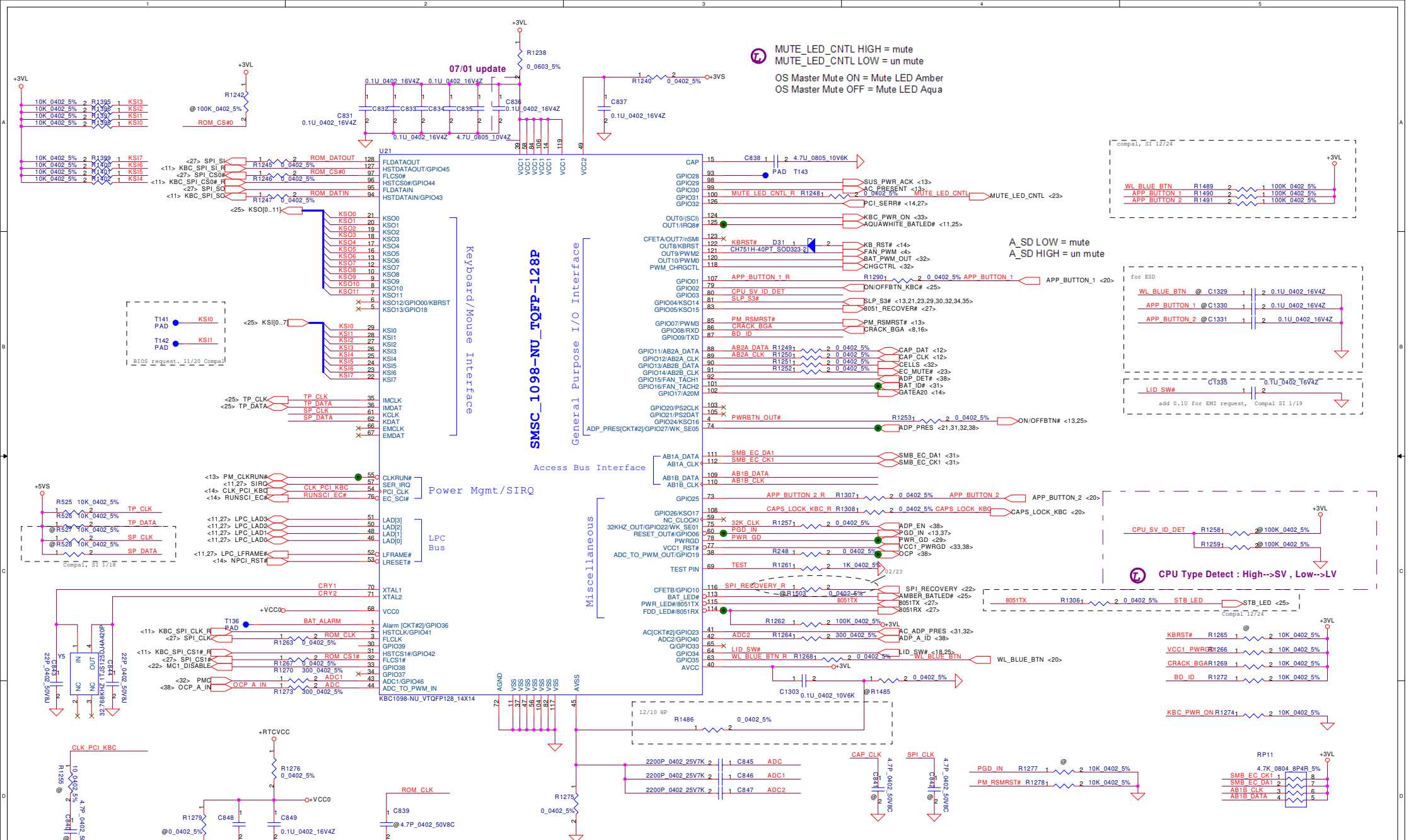
2nd Source :
WINBOND 32M W25Q32BVSSIG
EON 32M EN25F32-100HIP



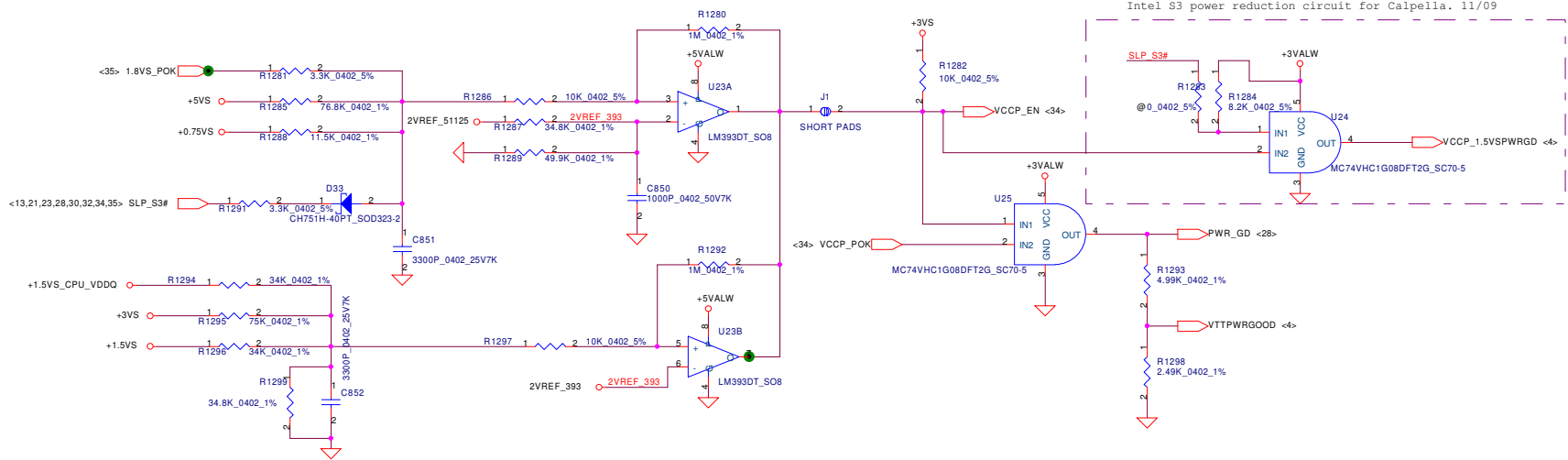
4MB SPI ROM



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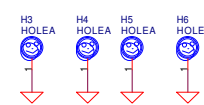
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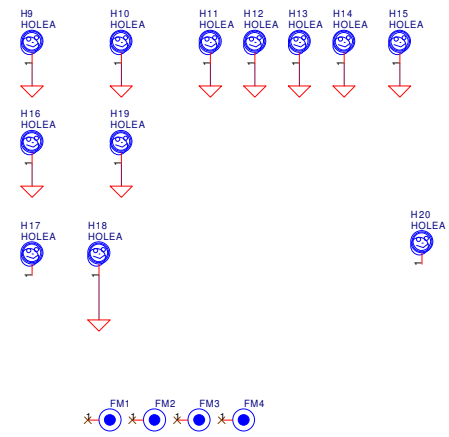
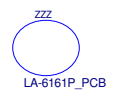
WWAN Card STANDOFF



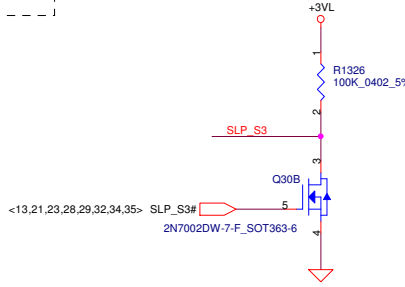
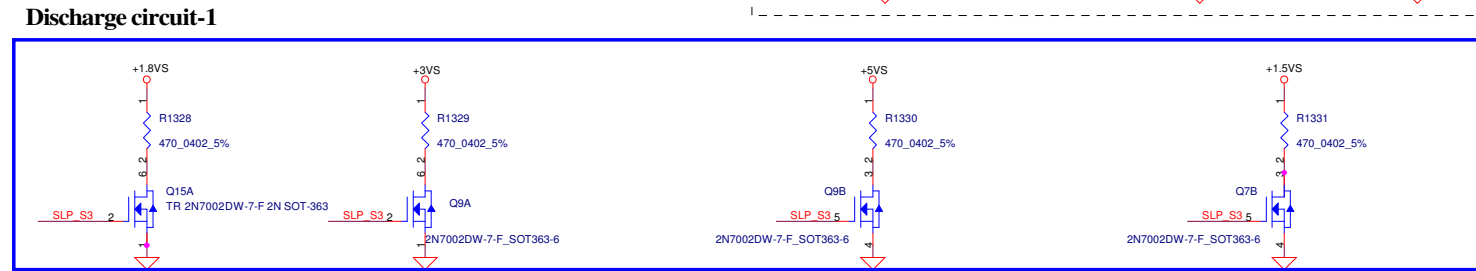
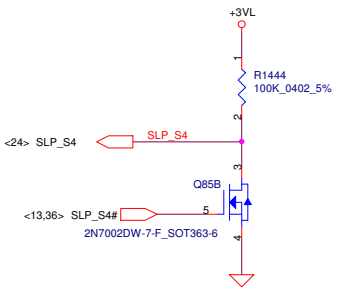
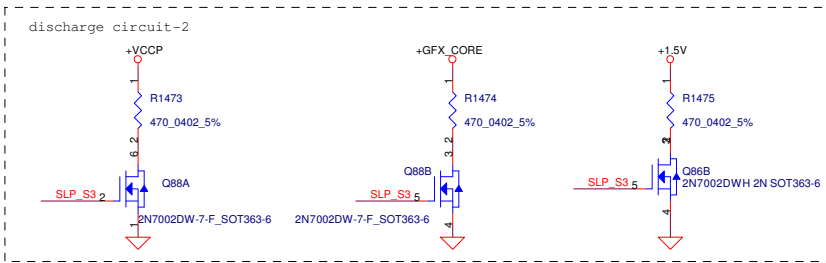
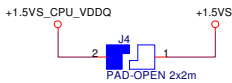
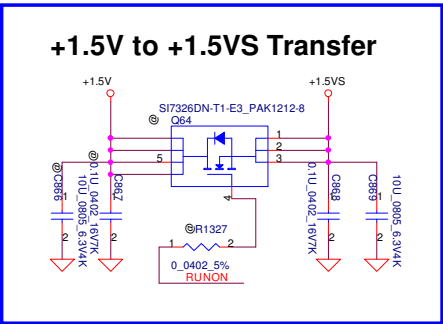
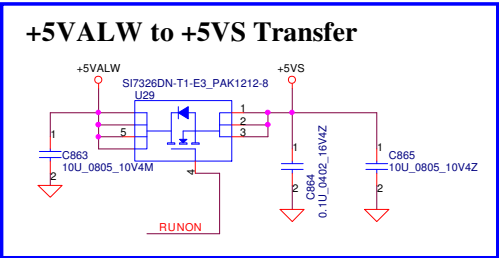
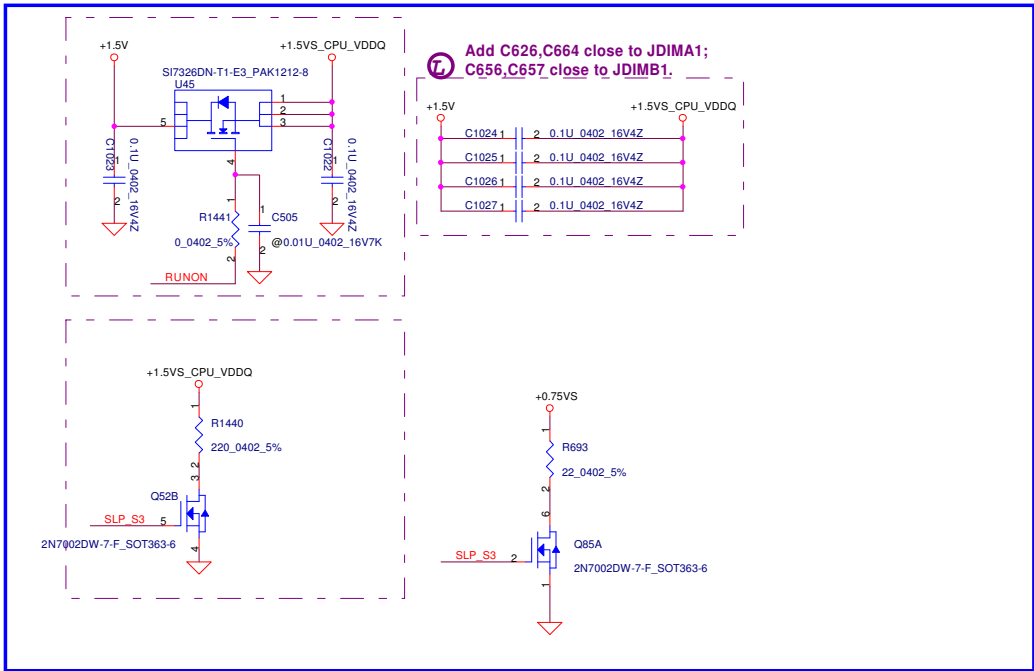
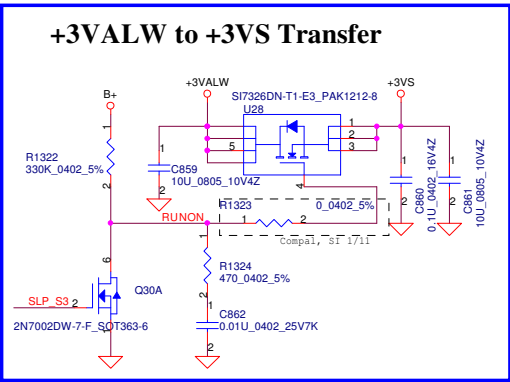
CPU support



WWLAN Card STANDOFF



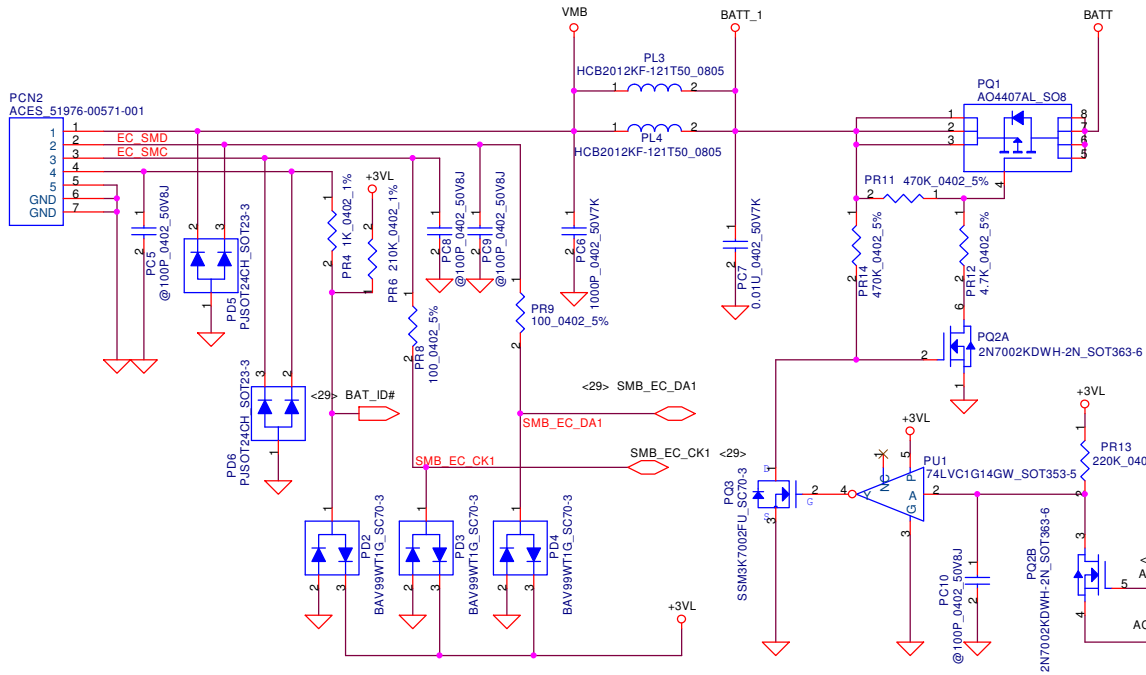
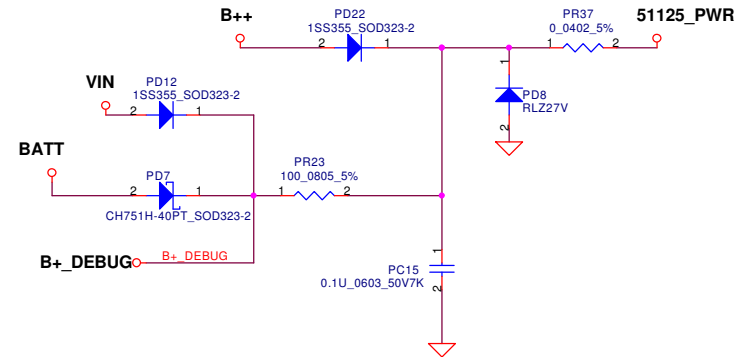
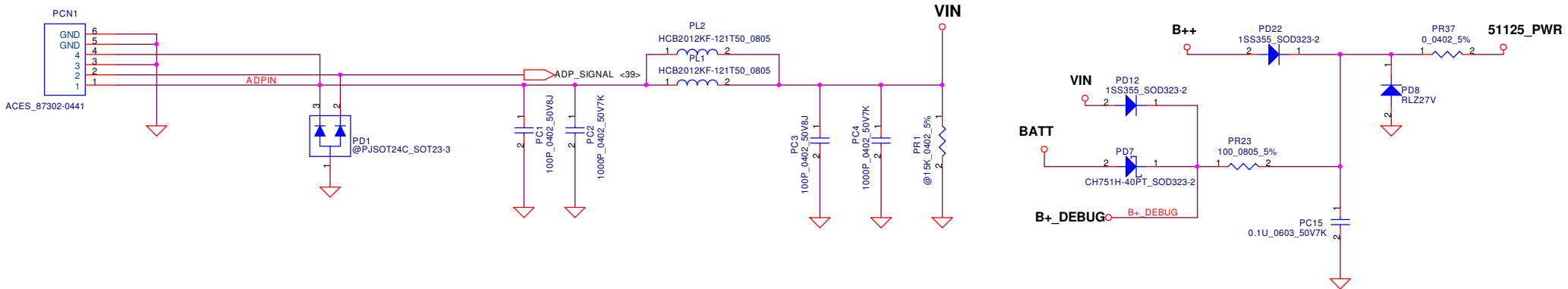
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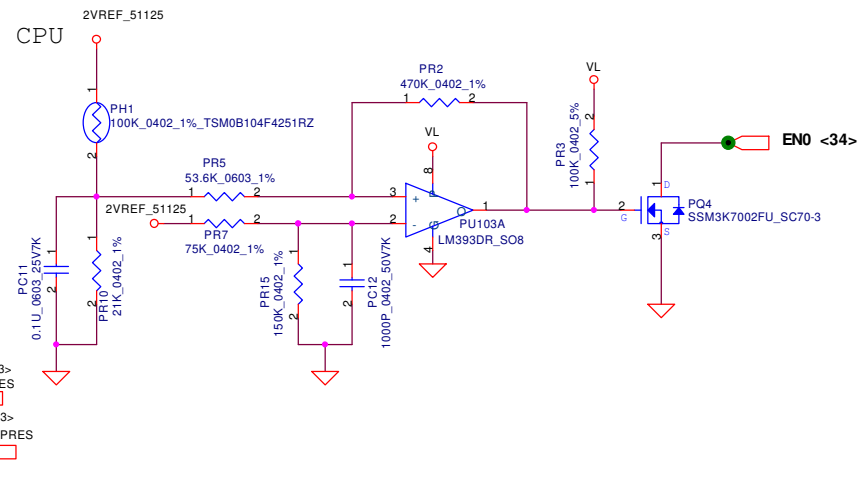
Intel S3 power reduction circuit for Calpella. 11/09

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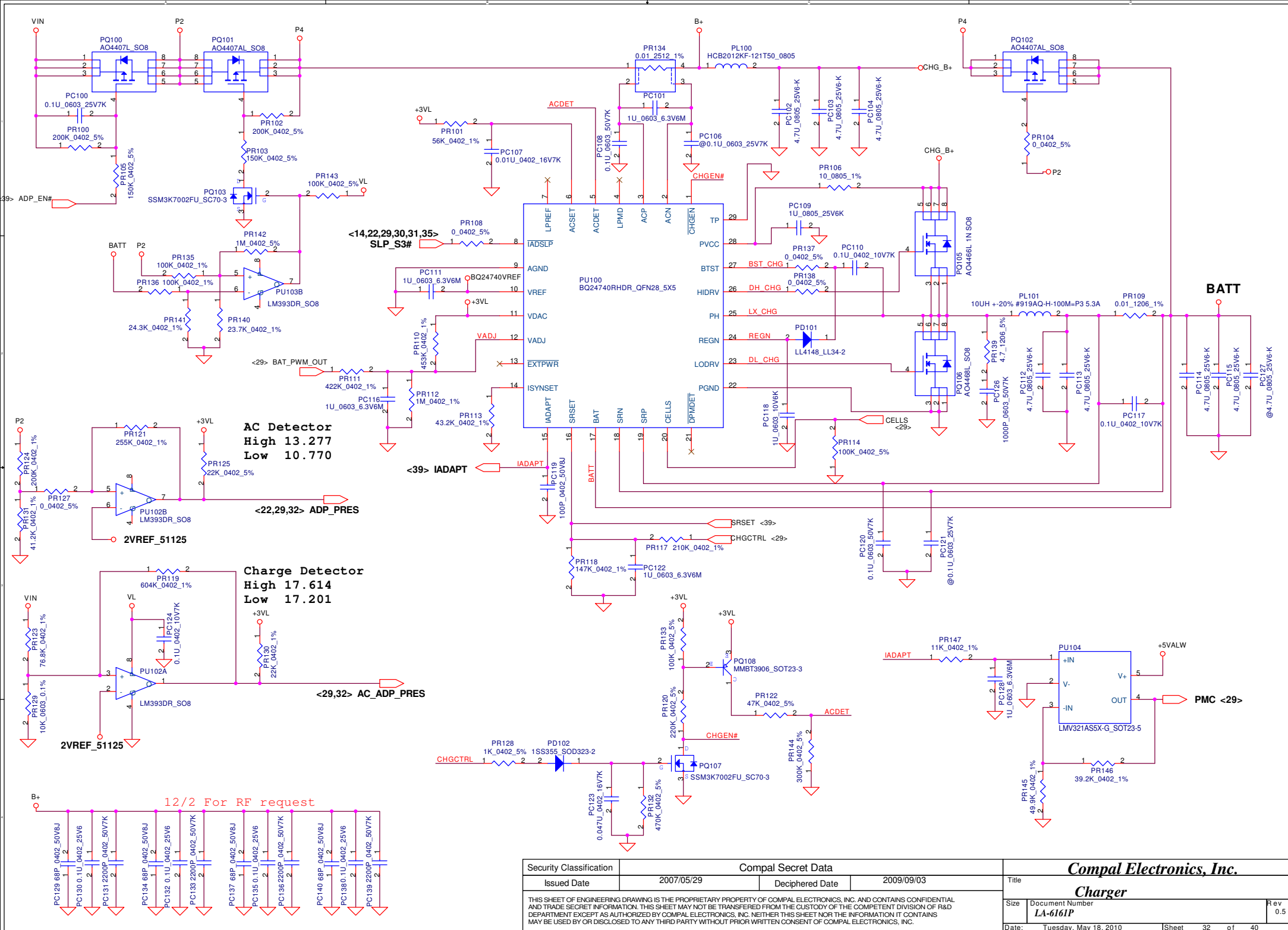
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Compal Electronics, Inc.		
DC/DC Circuits		
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PH1 under CPU bottom side :
 CPU thermal protection at 90 +/- 3 degree C
 Recovery at 47 +/- 3 degree C

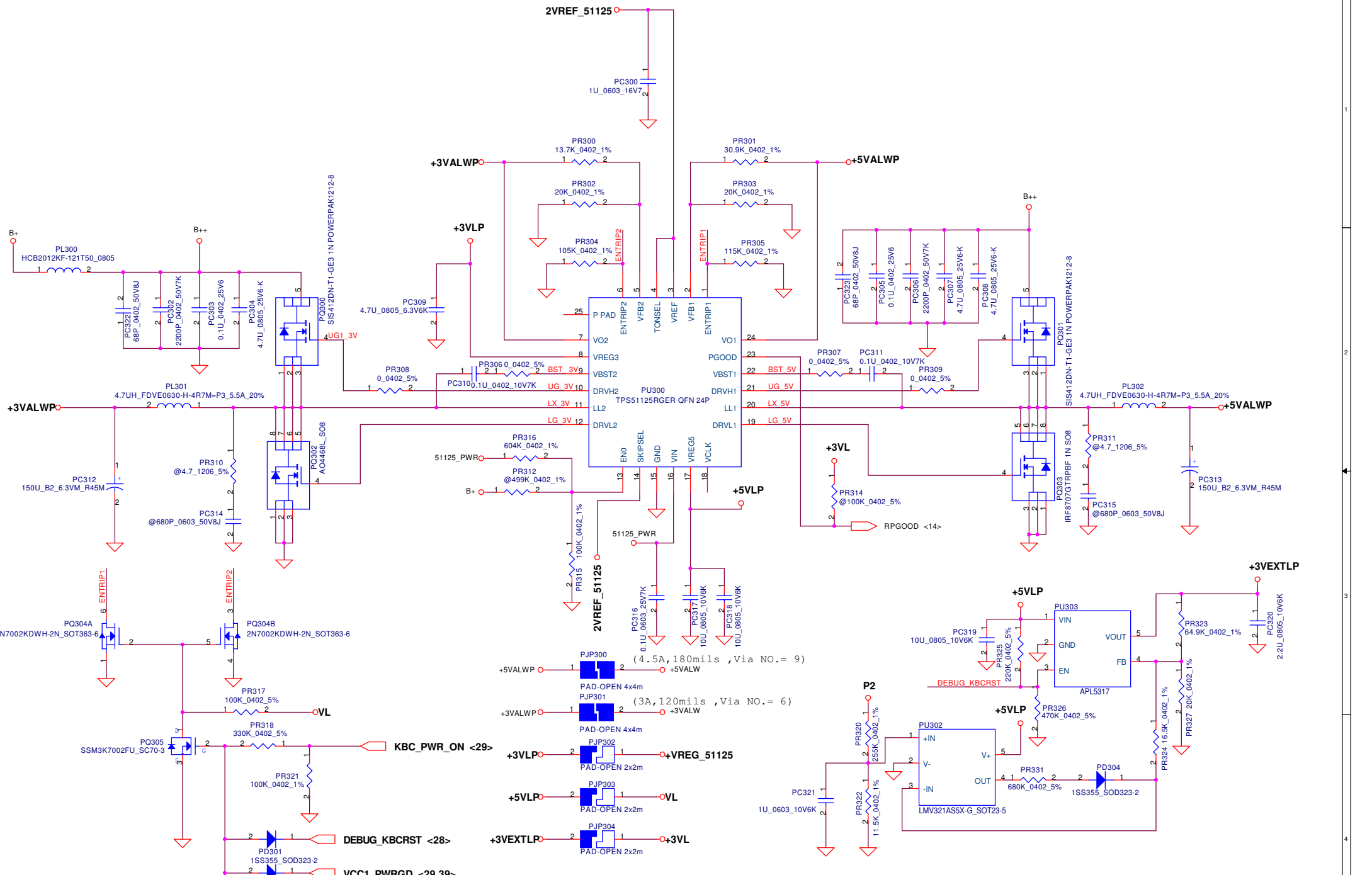


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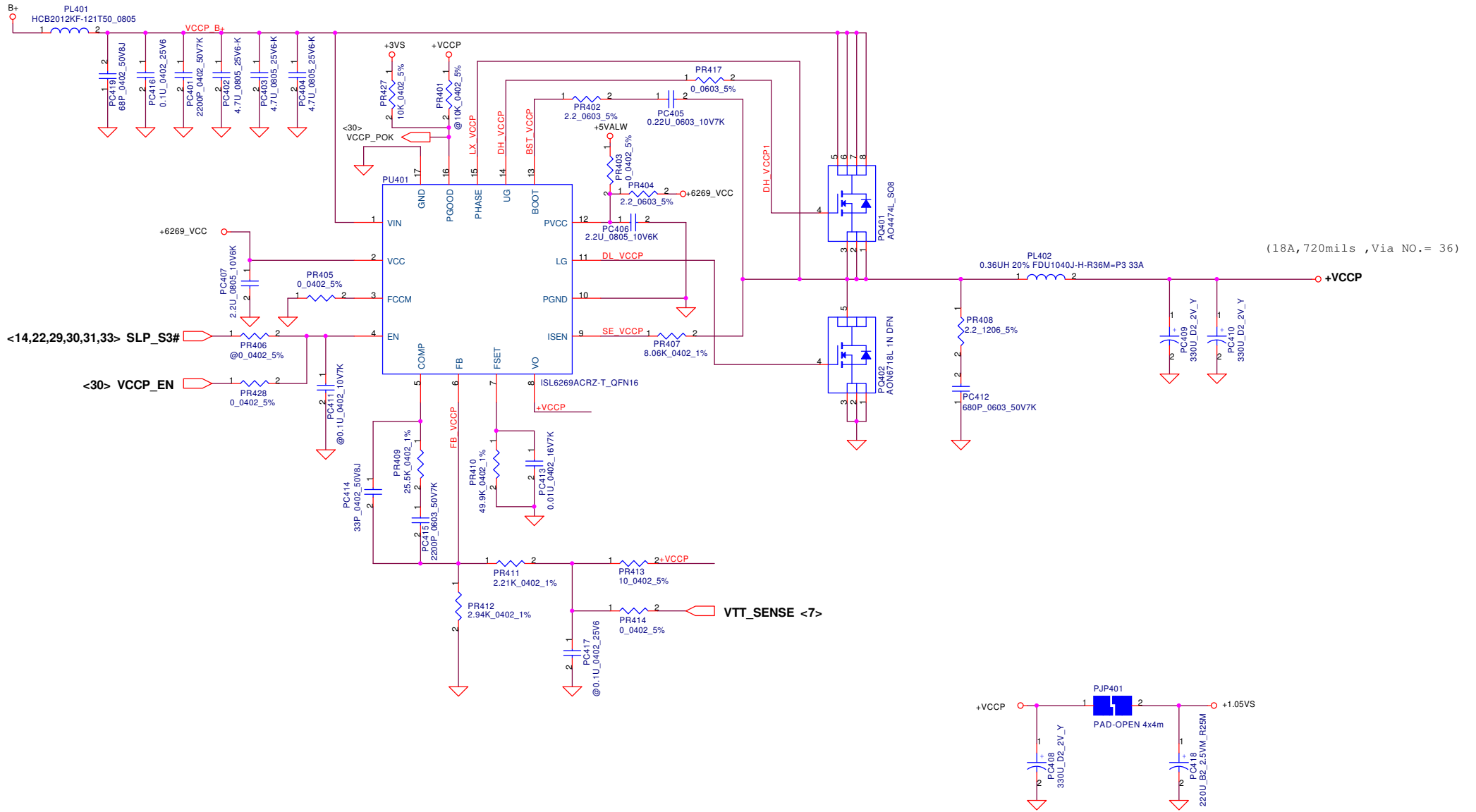
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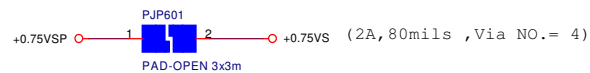
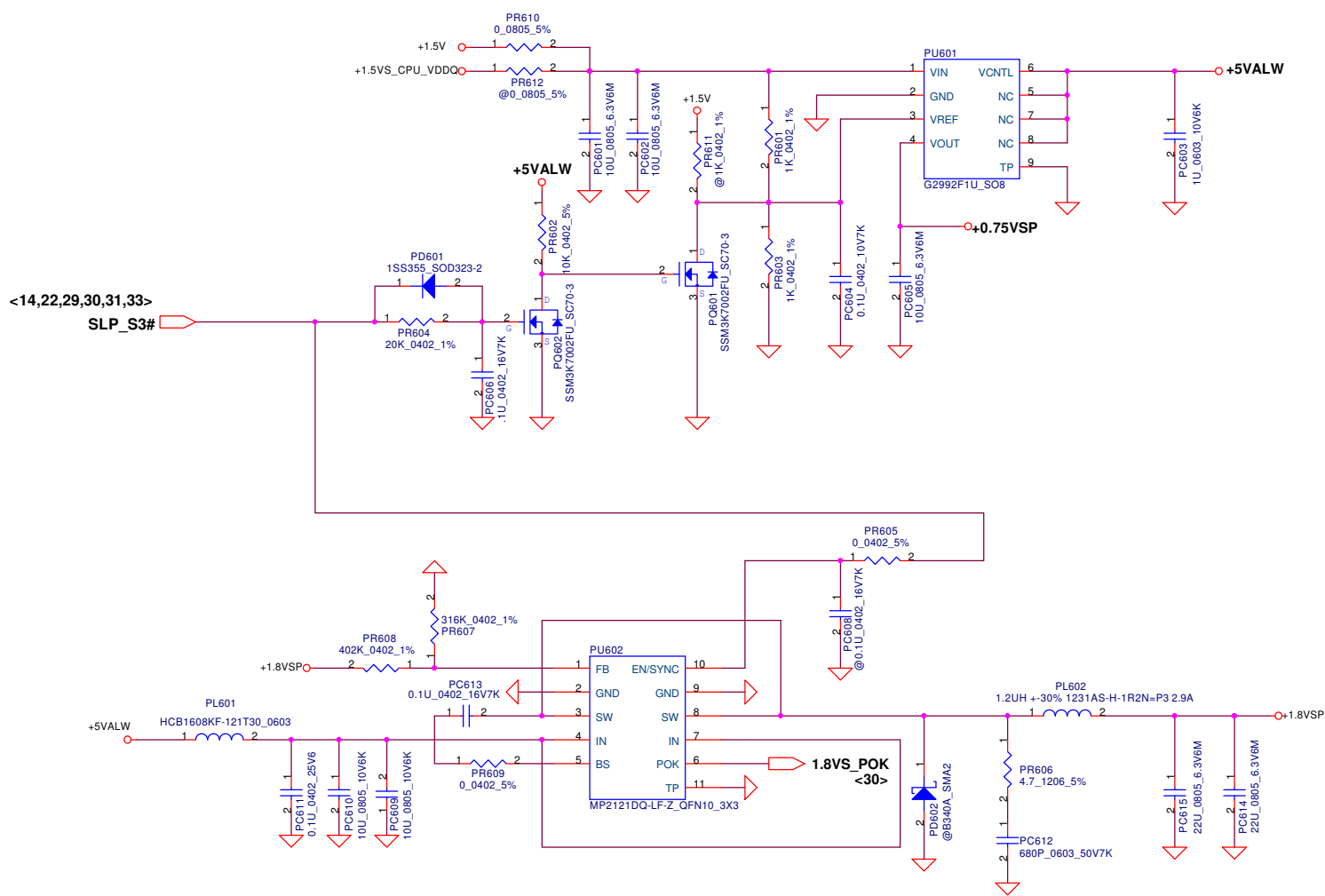


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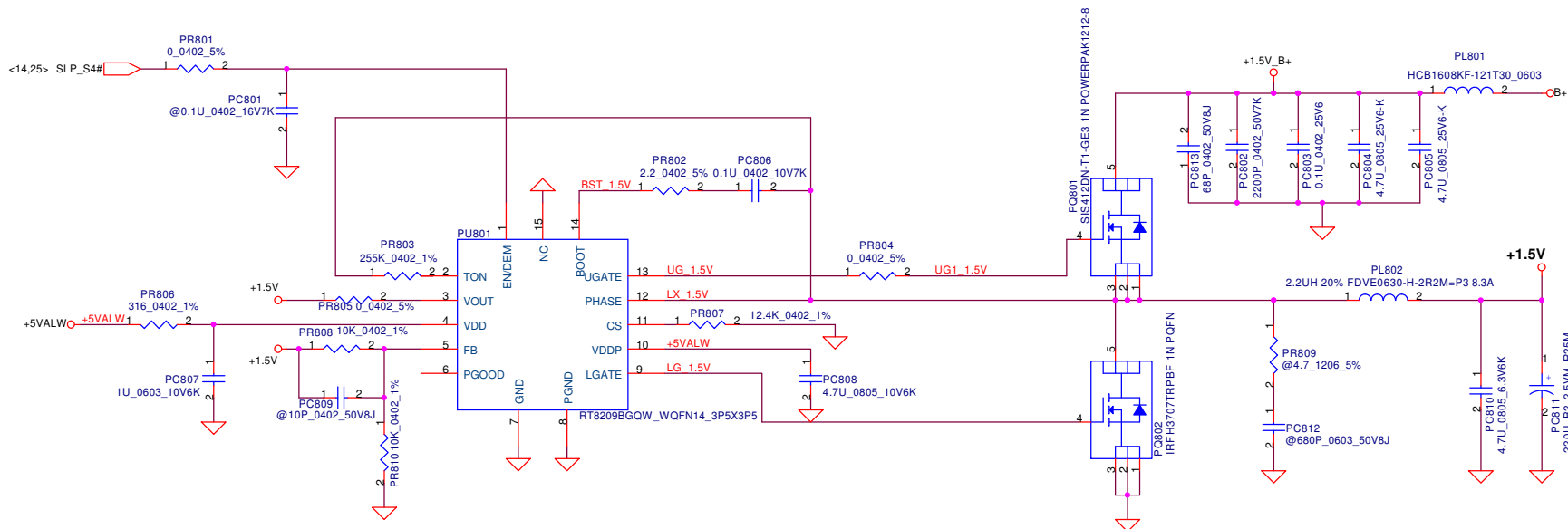
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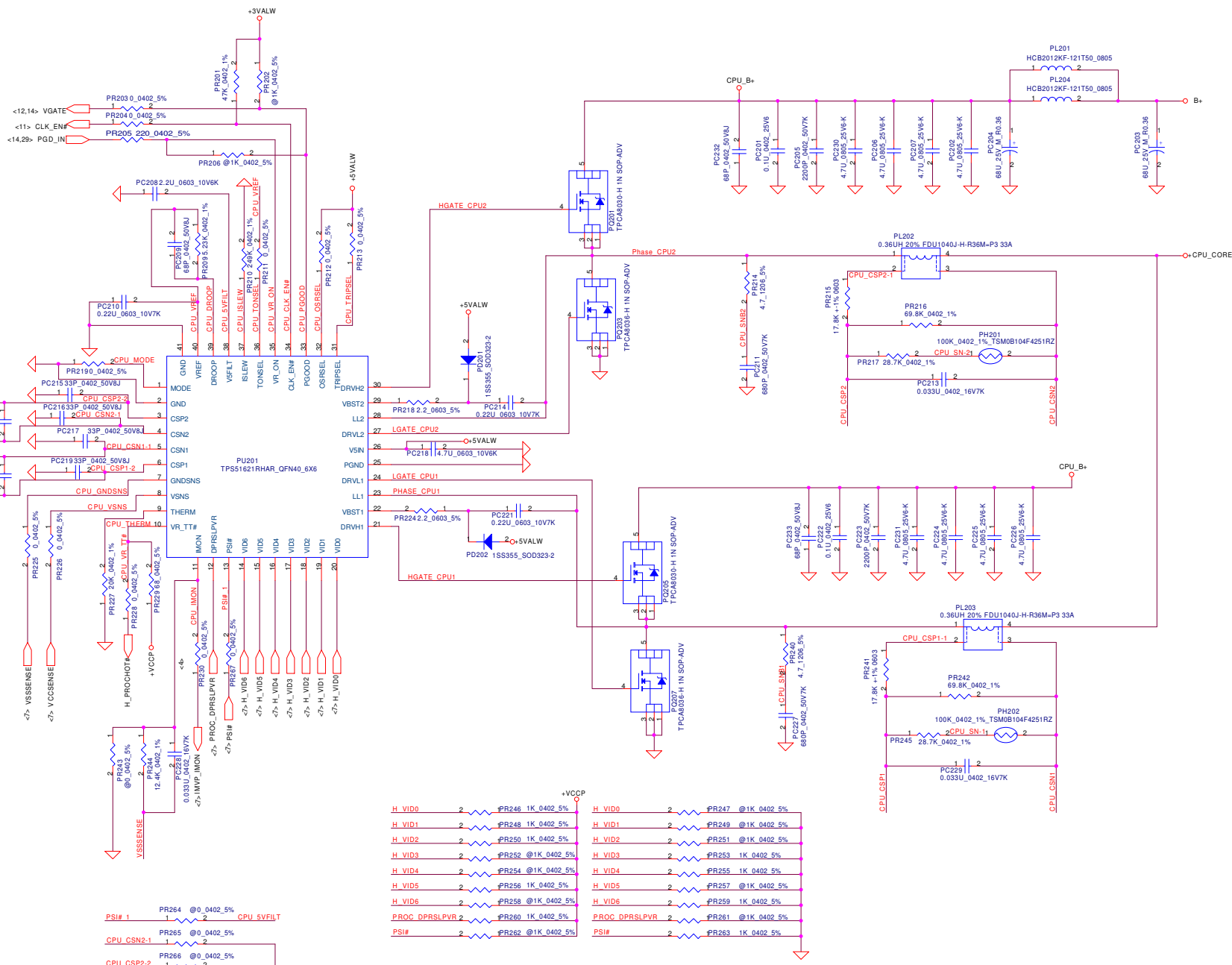
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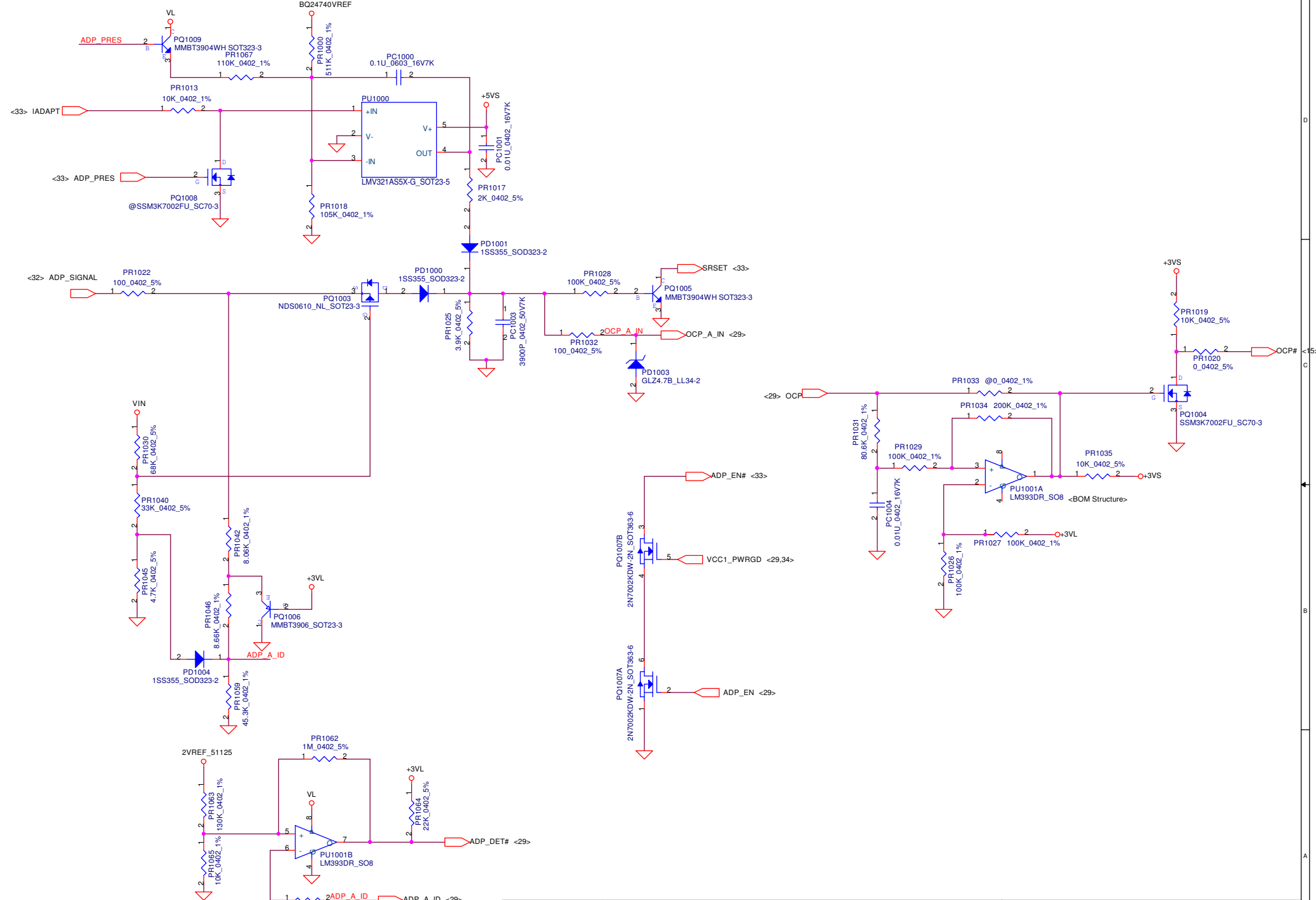
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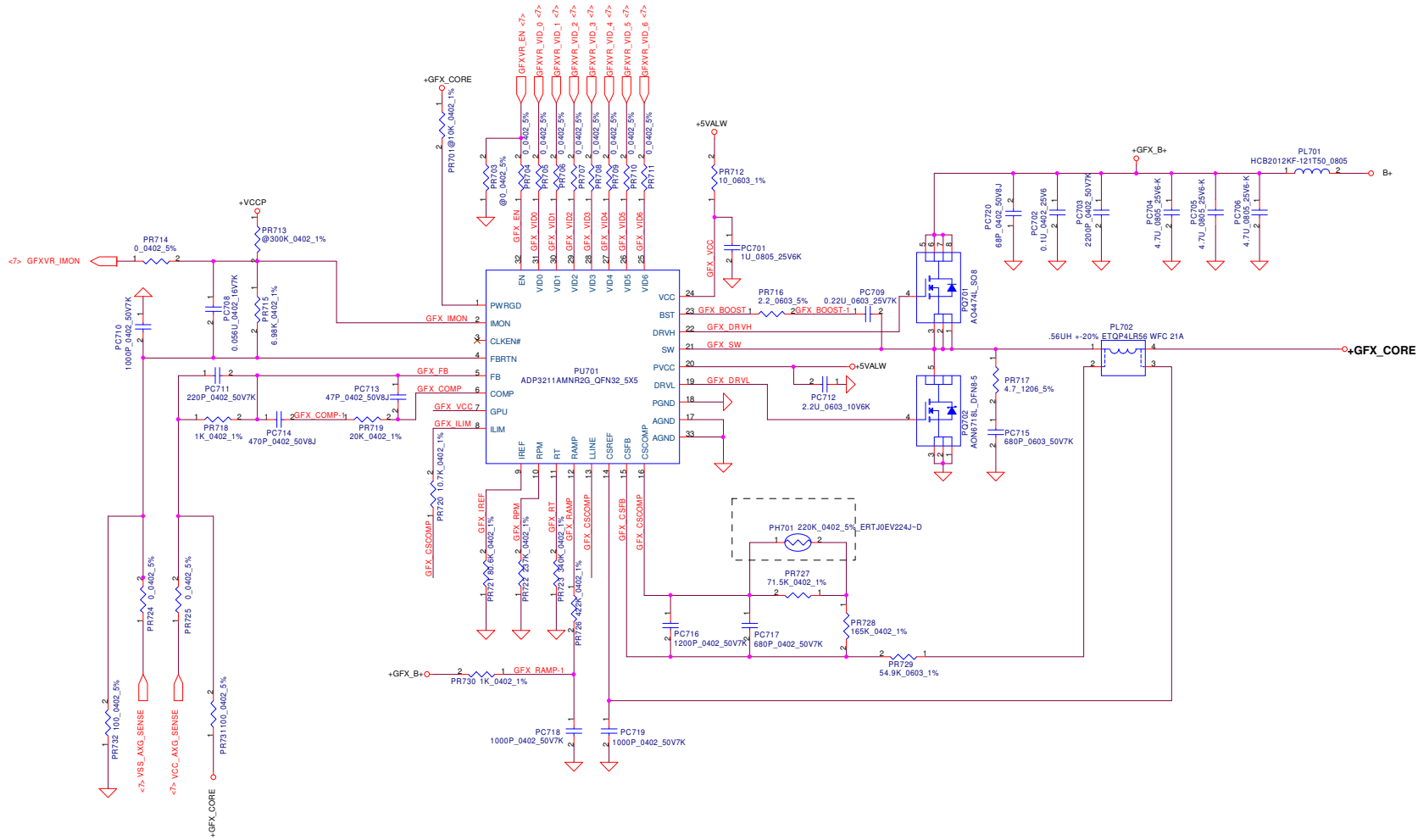
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CPU CORE	
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Item	Reason for change	PG#	Modify List	Date	Phase
1	Tune Loadline and transient response of GFX.	P39	Change PR729 to 54.9k, PC716 to 1200pF, and PC717 to 680pF.	01/27	SI
2	Tune Loadline and transient response of CPU.	P37	Change PR209 to 5.23k.	01/27	SI
3	Add boost resistance for RF team.	P36	Change PR802 to 2.2ohm.	01/28	SI
4	Modify the throttling setting level and action speed.	P38	Change PR1013 to 10k, PR1000 to 511k, PR1018 to 105k, and PC1000 to 0.1uF.	01/28	SI
5	IN AC mode, the performance will reduce through IADAPT without PQ1008.	P38	Add PQ1008.	01/29	SI
6	OTP setting is setted same with other project.	P31	Change PR5 to 53.6k and PR10 to 19.1k.	02/01	SI
7	330uF ESR=9mOhm can pass VCCP ripple spec.	P34	Change PR408, PR409, and PR410 to 330uF_9mOhm.	02/02	SI
8	CPU thermal protection fine-tune.	P31	Change PR10 to 21K from 19.1K	03/26	PV
9	For ULV CPU, need reserved some components.	P37	Add PR264, PR265, PR266 locations which is reserved.	03/26	PV
10	For CPU accuracy get better.	P37	Change PR215 and PR241 to 0603 size and keep 17.8K	03/26	PV
11	For Electrical Noise Issue.	P37	Add PC204, whcih is 68u	03/31	PV
11	For EMI request.	P32	Add snabber, PR139 to 4.7ohm, PC126 to 1n	03/31	PV

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	Quick look/web	12/24	Compal	The LED Status about Wireless/QuickLook3/QuickWeb is abnormal. OTS# 603778	APP_BUTTON_1 APP_BUTTON_2 add 100k ohm pull high to +3VL	0.2
2	28	PWR LED	12/24	Compal	PWR LED can't flash in S3. OTS# 603774	Change STB_LED signal from KBC pin105 to pin115	0.2
3	22	WWAN	1/4	Compal	the LED panel was auto turn on whhen plug in AC. OTS# 603786	correct the JWWAN1 pin24 power rail from +3VS to +3V_WWAN	0.2
4	23	Audio	1/5	Compal	audio no functtion. OTS# 603777	delet D16	0.2
5	22	WLAN	1/6	Compal	Debug port 80 is not used	delete signal of PCI_RST#,CLK_PCI_DEBUG,LPC_LFRAME#,LPC_LAD3,2,1,0 and remove C1317, R270	0.2
6	11, 21		1/6	Compal	resistance too small will impact the SMT line yield rate	change R1457, R1458,R1027 from 0201 to 0402	0.2
7	23	Audio	1/6	Compal	PC_BEEP no sound in DOS mode. OTS# 604314	install Q72 and change R1352 from 4.7K to 100K, change C895 from 0.1U to 0.01U	0.2
8	30	DC-DC	1/11	Compal	power down sequence havv problem with +5VS & +3VS. (+5VS goes to low after +3VS)	change R1323 from 330K to 0 ohm	0.2
9	14	GLAN	1/13	Compal	System can't wake up from S3 & S5.OTS# 605647	remove R1482	0.2
10	14	Transformer	1/14	Compal	EMI noise	Swap the signal of MID0 <->3, MID1<->2 to improve the layout routing. (avoid the trace routing under the T)	0.2
11	9	Transformer	1/21	HP	reserve memory thermal sensor by HP request	reserve U59,R1496,R1497,C1338,R1495	0.2
12	24	Audio	1/28	HP	for the mic detection comparator	change R1202 from 120K to 47K	0.2
13	22	SPI	2/23	Compal	For SPI ROM Recovery	Reserve R1498, R1499, R1500, R1501, R1502, R1503. Add R1504 which is pull down to GND and connect to GP1046.	0.3
14	14	CPU	2/24	Compal	For CPU Type Detect		0.3
15	22	SPI	3/12	Compal	Can't power on with Intel's WLAN card.	Change power pin +3VL from pin 47 to 51.	0.4
16	18	LCD	3/23	Compal	For EMI's request	add 0.1uF (C1339) on ENABLT to GND near R1122.	0.4
17	19	CRT	3/24	Compal	For EMI's request	Change C232, C233, C236 from 6.8pF to 18pF.	0.4
18	18	LCD	5/18	Compal	Fine tune LED power on sequence.	Change C676 to 0.22 uF and C682 to 2.2 uF.	0.5

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