COMPAL CONFIDENTIAL

MODEL NAME : *PAL70*
PCB NO : *LA-6611P (DAA00001W10)*
BOM P/N : *43XXXXXXLXX*
GPIO MAP Version 1010

E3 MACALLAN 13" UMA
BGA Sandy Bridge +
FCBGA PCH Cougar Point-M
2010-01-21
REV : 1.0(A00)

Items	R1 P/N	R3 P/N
CPU 2.5G	SA00004EL2L	SA00004EL3L
CPU 2.6G	SA00004EM2L	SA00004EM3L
CPU 2.7G	SA00004F02L	SA00004F03L
CPU 2.1G	SA00004KP1L	SA00004KP2L
PCH	SA00004IW2L	SA00004IW3L
LAN	SA00003SI4L	SA00003SI5L
USH	SA00003AO1L	SA00003AO2L

@ : Nopop Component

MB Type	BOM P/N	TPM		TCM		With SPI	With TAA
		1@	3@	2@	4@	5@	6@
2.5G CPU TPM EN/ TCM DIS/W TAA	43193431L06	*	*				*
2.5G CPU TPM EN/ TCM DIS/W/SPI	43193431L03	*	*			*	
2.5G CPU TPM DIS/ TCM EN				*	*		*
2.5G CPU TPM DIS/ TCM EN/W/SPI				*	*	*	
2.5G CPU TPM DIS/ TCM DIS			*	*			*
2.5G CPU TPM DIS/ TCM DSI /W/ SPI	43193431L15		*	*		*	
2.6G CPU TPM EN/ TCM DIS/W TAA	43193431L07	*	*				*
2.6G CPU TPM EN/ TCM DIS/W/SPI	43193431L04	*	*			*	
2.6G CPU TPM DIS/ TCM EN				*	*		*
2.6G CPU TPM DIS/ TCM EN/W/SPI				*	*	*	
2.6G CPU TPM DIS/ TCM DIS			*	*			*
2.6G CPU TPM DIS/ TCM DSI /W/ SPI	43193431L16		*	*		*	
2.7G CPU TPM EN/ TCM DIS/W TAA	43193431L08	*	*				*
2.7G CPU TPM EN/ TCM DIS/W/SPI	43193431L05	*	*			*	
2.7G CPU TPM DIS/ TCM EN				*	*		*
2.7G CPU TPM DIS/ TCM EN/W/SPI				*	*	*	
2.7G CPU TPM DIS/ TCM DIS			*	*			*
2.7G CPU TPM DIS/ TCM DSI /W/ SPI	43193431L17		*	*		*	

MB PCB

Part Number	Description
DAA00001W00	PCB PAL70 LA6611

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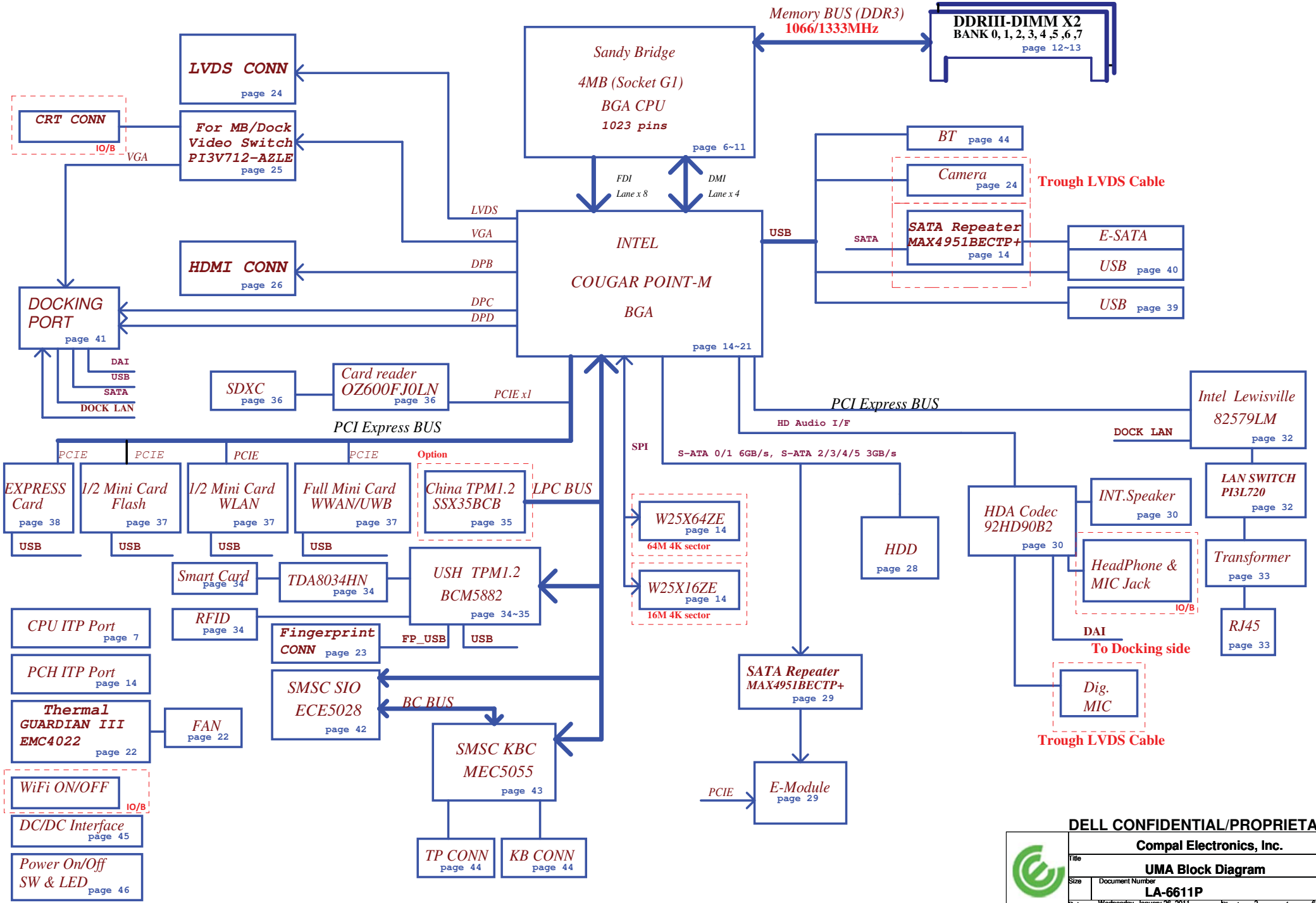
Block Diagram Compal confidential Model: PAL70



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Title	UMA Block Diagram	
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane \ State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

Stack up

Layer	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
SolderMask	min 0.4	0.50
Add Plating	1.30	1.05
Top/L1(signal)	0.5oz(0.68)	0.65
Prepreg	1080LRC	2.65
	0.5oz	0.65
Core	3mil	3.09
L3(IN1)	0.5oz	0.65
Prepreg	1080LRC+1080	5.1
L4(IN2)	1oz	1.35
Core	3mil	3.09
L5(GND2)	1oz	1.35
Prepreg	1080HRC	2.90
L6(IN3)	0.5oz	0.65
Core	6mil	6
L7(IN4)	0.5oz	0.65
Prepreg	1080HRC	2.90
L8(VCC)	1oz	1.35
Core	3mil	3.09
L9(IN5)	1oz	1.35
Prepreg	1080LRC+1080	5.1
L10(IN6)	0.5oz	0.65
Core	3mil	3.09
L11(GND3)	0.5oz	0.65
Prepreg	1080LRC	2.65
Bottom/L12(signal)	0.5oz(0.68)	0.65
Add Plating	1.30	1.05
SolderMask	min 0.4	0.50
Overall Thickness	1.36mm+/-10%	53.36

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Ext Right Side)
	1	none
	2	Right Side (ESATA)
	3	none
	4	WLAN/WIMAX
	5	WWAN/UWB
	6	Flash
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Bluetooth
	12	Camera
	13	none

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

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Title: Index and Config.
Size: Document Number: LA-6611P
Rev: 0.3
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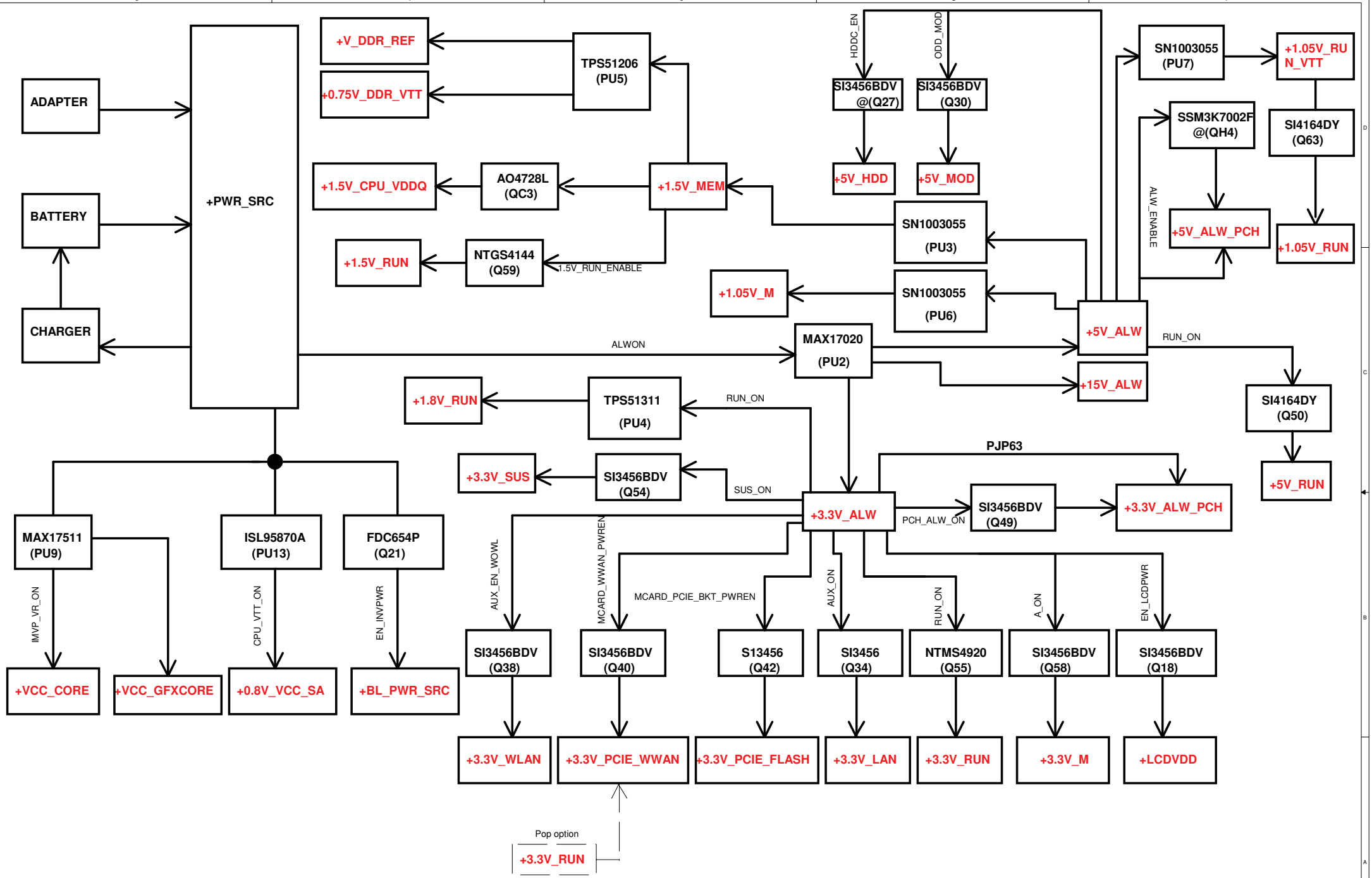

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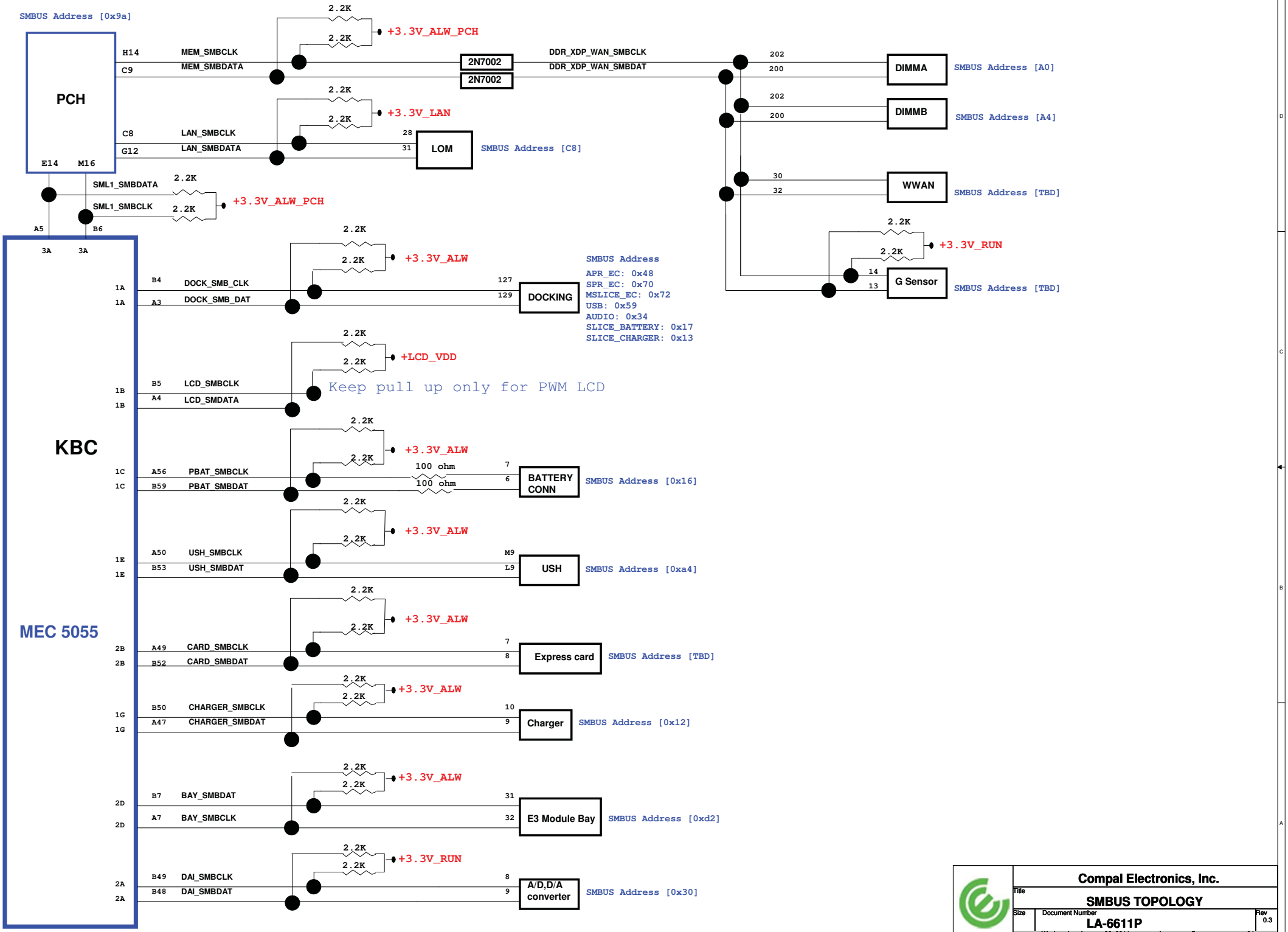

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Title: SMBUS TOPOLOGY

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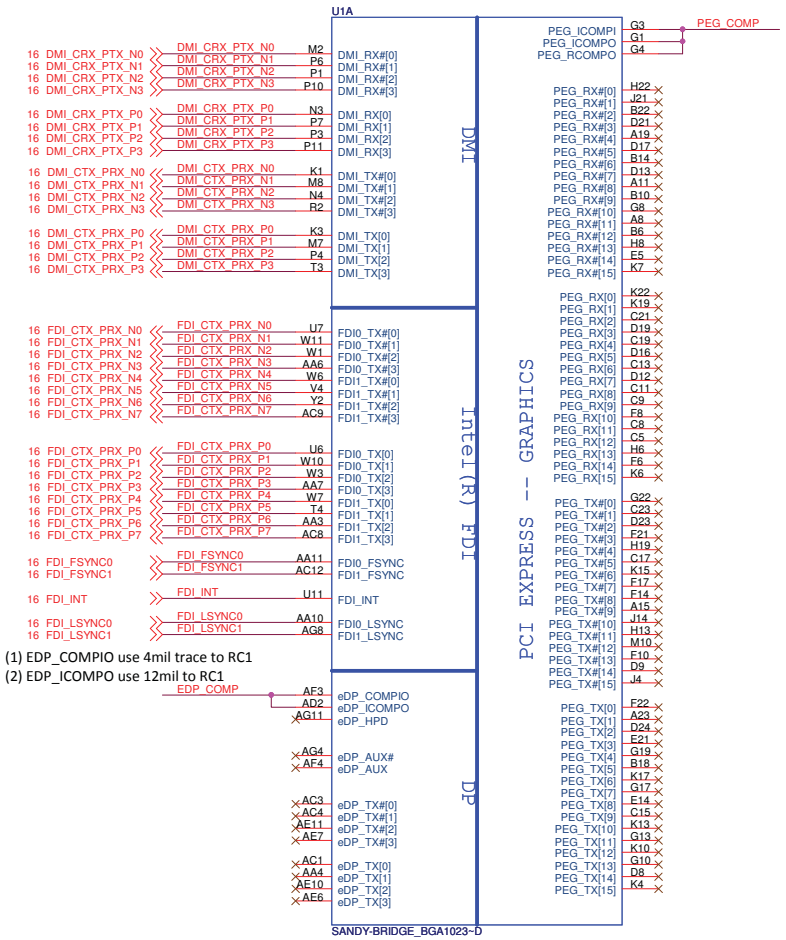
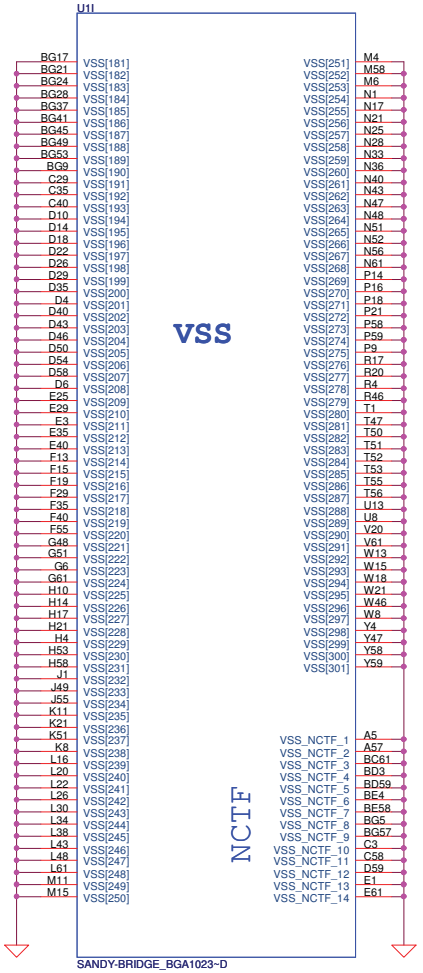
Date: Wednesday, January 26, 2011 | Sheet 5 of 64

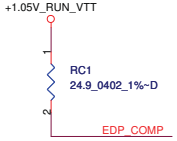
(1)PEG_RCOMPO (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
(2)PEG_ICOMPO use 12mil connect to RC2



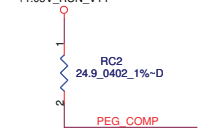
(1) EDP_COMPIO use 4mil trace to RC1
(2) EDP_ICOMPO use 12mil to RC1



DP Compensation



PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

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Title: Sandy Bridge (1/6)

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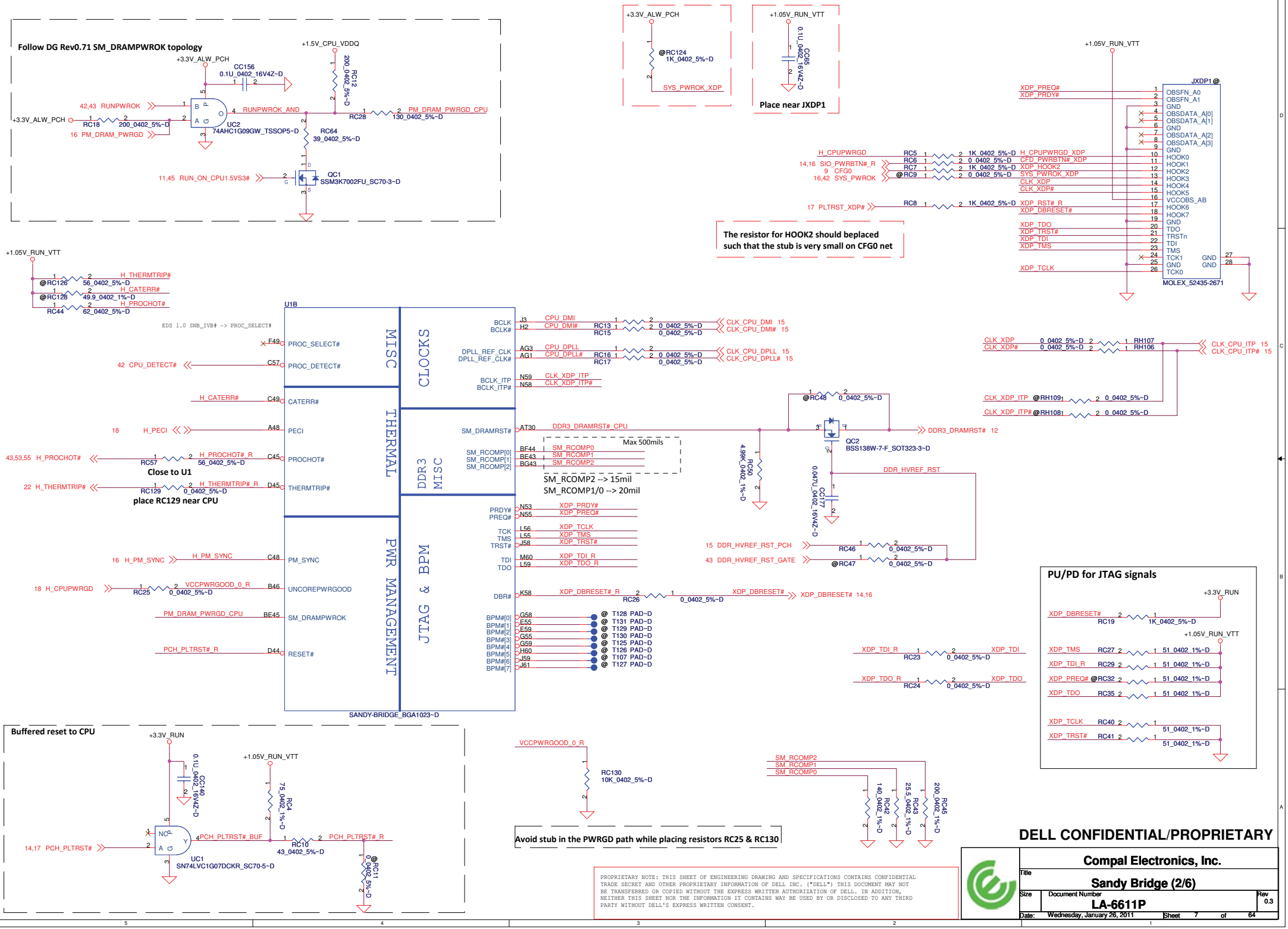
Follow DG Rev0.71 SM_DRAMPWROK topology
+3.3V_ALW_PCH
+1.5V_CPU_VDDQ
CC156 0.1U_0402_16V4Z~D
RC12 200_0402_5%~D
42,43 RUNPWROK
RUNPWROK_AND
PM_DRAM_PWRGD_CPU
RC18 200_0402_5%~D
16 PM_DRAM_PWRGD
UC2 74AHC1G09GW_TSSOP5~D
RC28 130_0402_5%~D
RC64 39_0402_5%~D
11,45 RUN_ON_CPU1.5VS3#
QC1 SSM3K7002FU_SC70-3~D
+3.3V_ALW_PCH
@RC124 1K_0402_5%~D
SYS_PWROK_XDP
+1.05V_RUN_VTT
CC65 0.1U_0402_16V4Z~D
Place near JXDP1
+1.05V_RUN_VTT
JXDP1 @
XDP_PREQ#
XDP_PRDY#
OBSFN_A0
OBSFN_A1
OBSDATA_A[0]
OBSDATA_A[1]
OBSDATA_A[2]
OBSDATA_A[3]
H_CPUPWRGD
14,16 SIO_PWRBTN#_R
9 CFG0
16,42 SYS_PWROK
RC5 1K_0402_5%~D
RC6 0_0402_5%~D
RC7 1K_0402_5%~D
@RC9 0_0402_5%~D
H_CPUPWRGD_XDP
CFD_PWRBTN#_XDP
XDP_HOOK2
SYS_PWROK_XDP
CLK_XDP
CLK_XDP#
17 PLTRST_XDP#
RC8 1K_0402_5%~D
XDP_RST#_R
XDP_DBRESET#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_TCLK
HOOK0
HOOK1
HOOK2
HOOK3
HOOK4
HOOK5
VCCOBS_AB
HOOK6
HOOK7
TDO
TRSTn
TDI
TMS
TCK1
TCK0
GND
MOLEX_52435-2671
The resistor for HOOK2 should beplaced such that the stub is very small on CFG0 net
+1.05V_RUN_VTT
@RC126 56_0402_5%~D
H_THERMTRIP#
@RC128 49.9_0402_1%~D
H_CATERR#
RC44 62_0402_5%~D
H_PROCHOT#
U1B
EDS 1.0 SNB_IVB# -> PROC_SELECT#
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
PROC_SELECT#
42 CPU_DETECT#
PROC_DETECT#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
BCLK_ITP
BCLK_ITP#
J3 CPU_DMI
H2 CPU_DMI#
RC13 RC15 0_0402_5%~D
CLK_CPU_DMI 15
CLK_CPU_DMI# 15
AG3 CPU_DPLL
AG1 CPU_DPLL#
RC16 RC17 0_0402_5%~D
CLK_CPU_DPLL 15
CLK_CPU_DPLL# 15
N59 CLK_XDP_ITP
N58 CLK_XDP_ITP#
CLK_XDP 0_0402_5%~D RH107
CLK_XDP# 0_0402_5%~D RH106
CLK_CPU_ITP 15
CLK_CPU_ITP# 15
CLK_XDP_ITP @RH109 0_0402_5%~D
CLK_XDP_ITP# @RH108 0_0402_5%~D
H_CATERR# C49 CATERR#
18 H_PECI A48 PECI
43,53,55 H_PROCHOT# RC57 H_PROCHOT#_R 56_0402_5%~D C45 PROCHOT#
Close to U1
22 H_THERMTRIP# RC129 0_0402_5%~D H_THERMTRIP#_R D45 THERMTRIP#
place RC129 near CPU
SM_DRAMRST#
AT30 DDR3_DRAMRST#_CPU
@RC48 0_0402_5%~D
QC2 BSS138W-7-F_SOT323-3~D
DDR3_DRAMRST# 12
Max 500mils
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
BF44 SM_RCOMP0
BE43 SM_RCOMP1
BG43 SM_RCOMP2
SM_RCOMP2 --> 15mil
SM_RCOMP1/0 --> 20mil
RC50 4.99K_0402_1%~D
CC177 0.047U_0402_16V4Z~D
DDR_HVREF_RST
15 DDR_HVREF_RST_PCH
RC46 0_0402_5%~D
43 DDR_HVREF_RST_GATE
@RC47 0_0402_5%~D
PRDY#
PREQ#
N53 XDP_PRDY#
N55 XDP_PREQ#
TCK
TMS
TRST#
L56 XDP_TCLK
L55 XDP_TMS
J58 XDP_TRST#
TDI
TDO
M60 XDP_TDI_R
L59 XDP_TDO_R
16 H_PM_SYNC H_PM_SYNC C48 PM_SYNC
18 H_CPUPWRGD RC25 VCCPWRGOOD_0_R 0_0402_5%~D B46 UNCOREPWRGOOD
PM_DRAM_PWRGD_CPU BE45 SM_DRAMPWROK
PCH_PLTRST#_R D44 RESET#
DBR#
K58 XDP_DBRESET#_R
RC26 0_0402_5%~D
XDP_DBRESET# 14,16
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
G58 @ T128 PAD~D
E55 @ T131 PAD~D
E59 @ T129 PAD~D
G55 @ T130 PAD~D
G59 @ T125 PAD~D
H60 @ T126 PAD~D
J59 @ T107 PAD~D
J61 @ T127 PAD~D
SANDY-BRIDGE_BGA1023~D
XDP_TDI_R RC23 0_0402_5%~D XDP_TDI
XDP_TDO_R RC24 0_0402_5%~D XDP_TDO
PU/PD for JTAG signals
+3.3V_RUN
XDP_DBRESET# RC19 1K_0402_5%~D
+1.05V_RUN_VTT
XDP_TMS RC27 51_0402_1%~D
XDP_TDI_R RC29 51_0402_1%~D
XDP_PREQ# @RC32 51_0402_1%~D
XDP_TDO RC35 51_0402_1%~D
XDP_TCLK RC40 51_0402_1%~D
XDP_TRST# RC41 51_0402_1%~D
Buffered reset to CPU
+3.3V_RUN
CC140 0.1U_0402_16V4Z~D
+1.05V_RUN_VTT
RC4 75_0402_1%~D
14,17 PCH_PLTRST#
UC1 SN74LVC1G07DCKR_SC70-5~D
PCH_PLTRST#_BUF
RC10 43_0402_5%~D
PCH_PLTRST#_R
@RC11 0_0402_5%~D
VCCPWRGOOD_0_R
RC130 10K_0402_5%~D
Avoid stub in the PWRGD path while placing resistors RC25 & RC130
SM_RCOMP2
SM_RCOMP1
SM_RCOMP0
RC42 140_0402_1%~D
RC43 255_0402_1%~D
RC45 200_0402_1%~D
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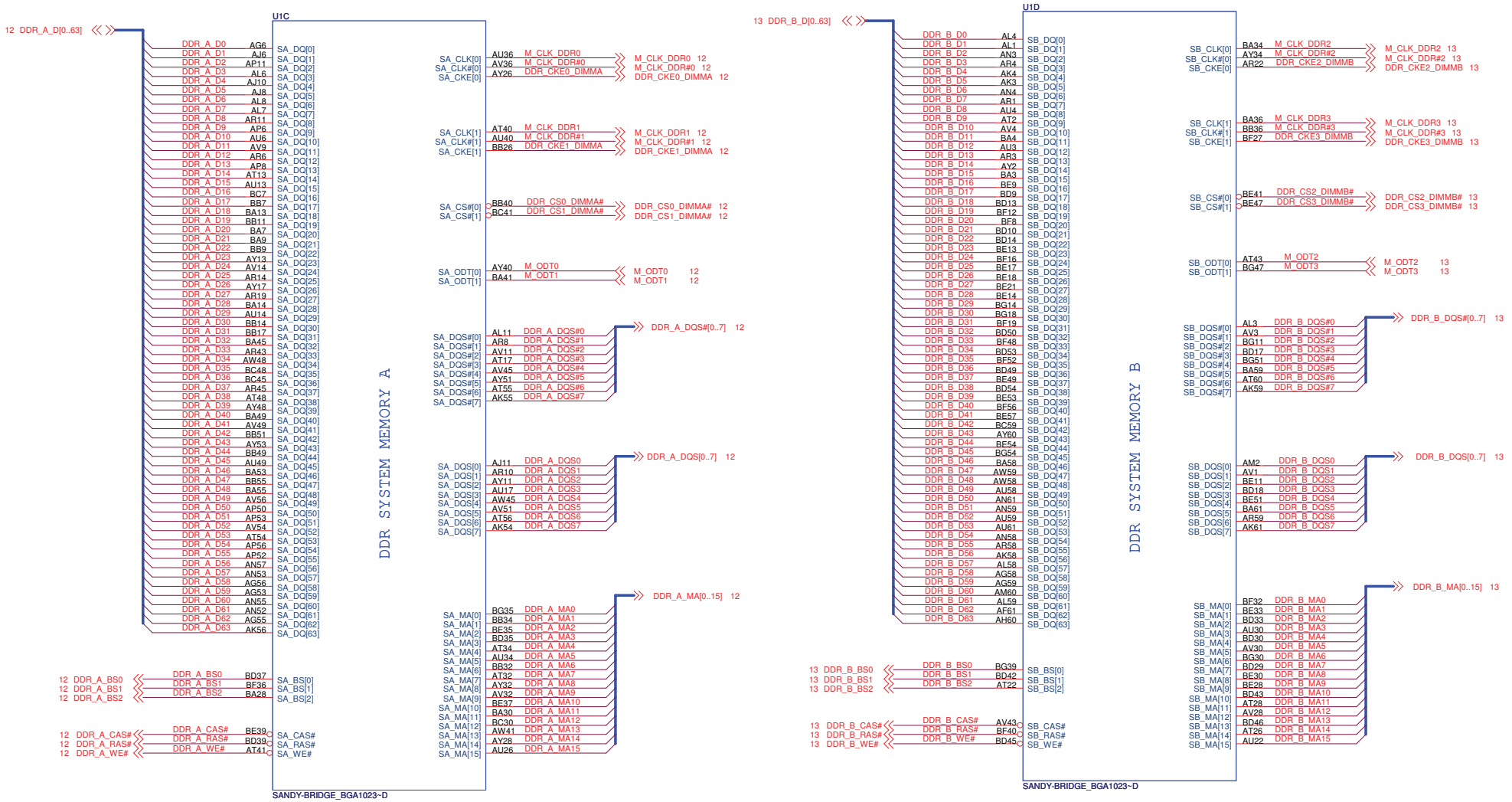

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Title: Sandy Bridge (3/6)

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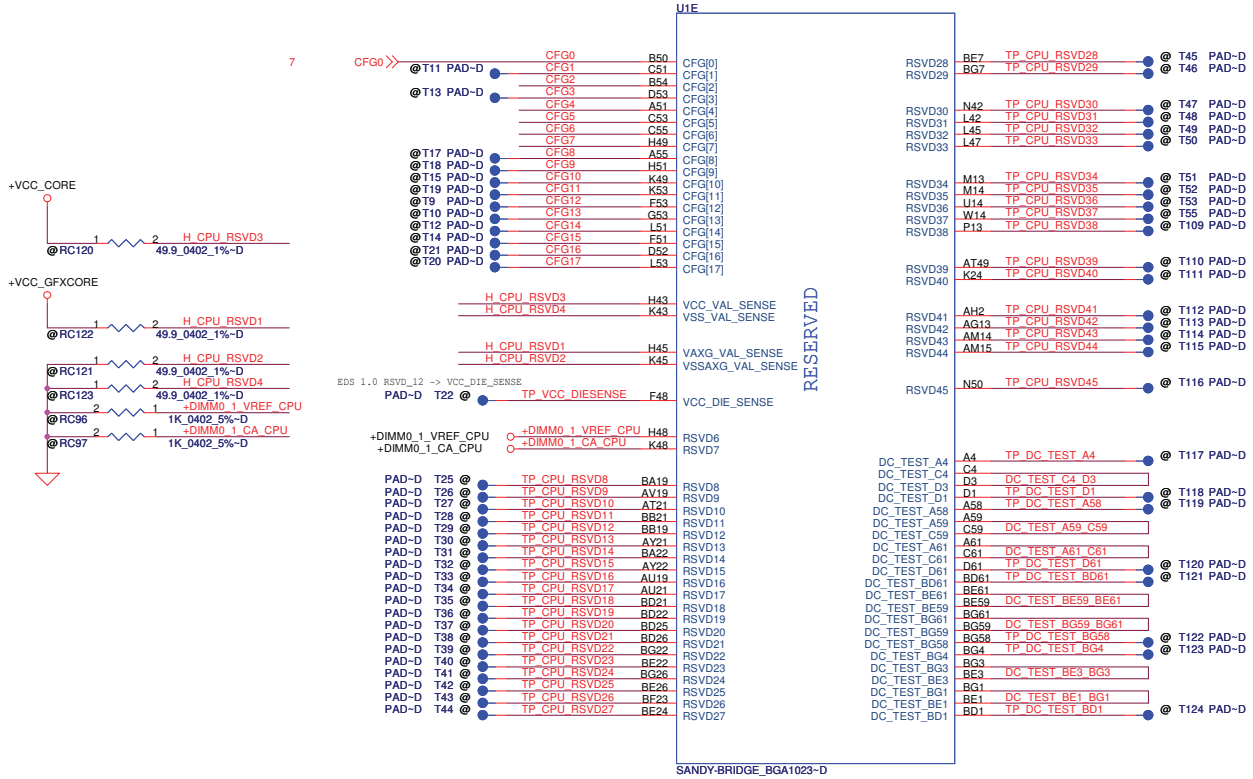
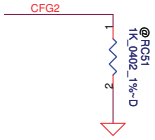
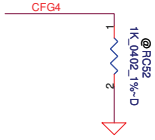


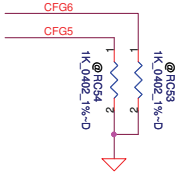
CFG Straps for Processor



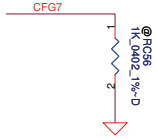
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: Sandy Bridge (4/6)

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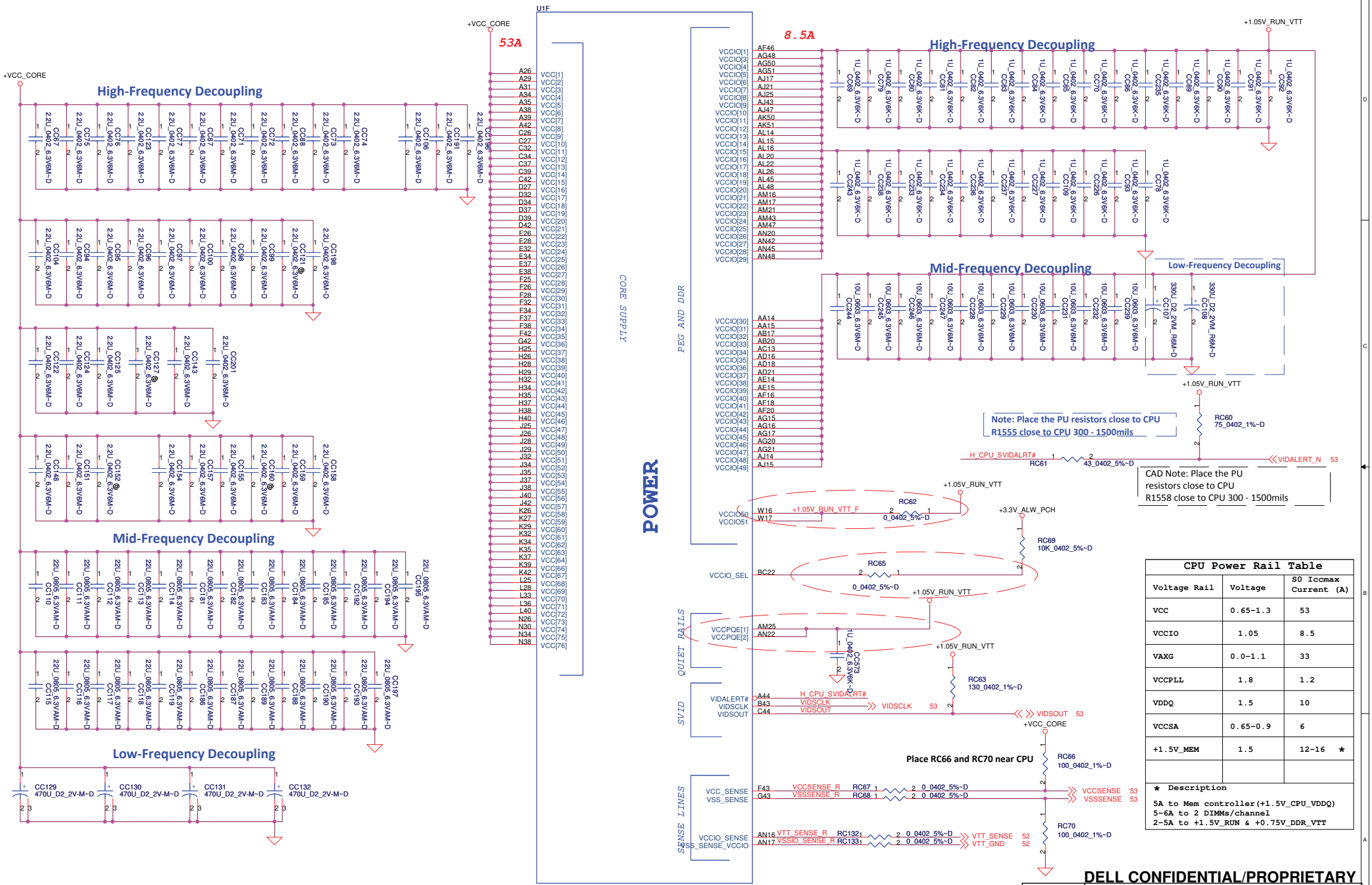

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65~1.3	53
VCCIO	1.05	8.5
VAXG	0.0~1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	10
VCCSA	0.65~0.9	6
+1.5V_MEM	1.5	12-16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

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Title: Sandy Bridge (5/6)

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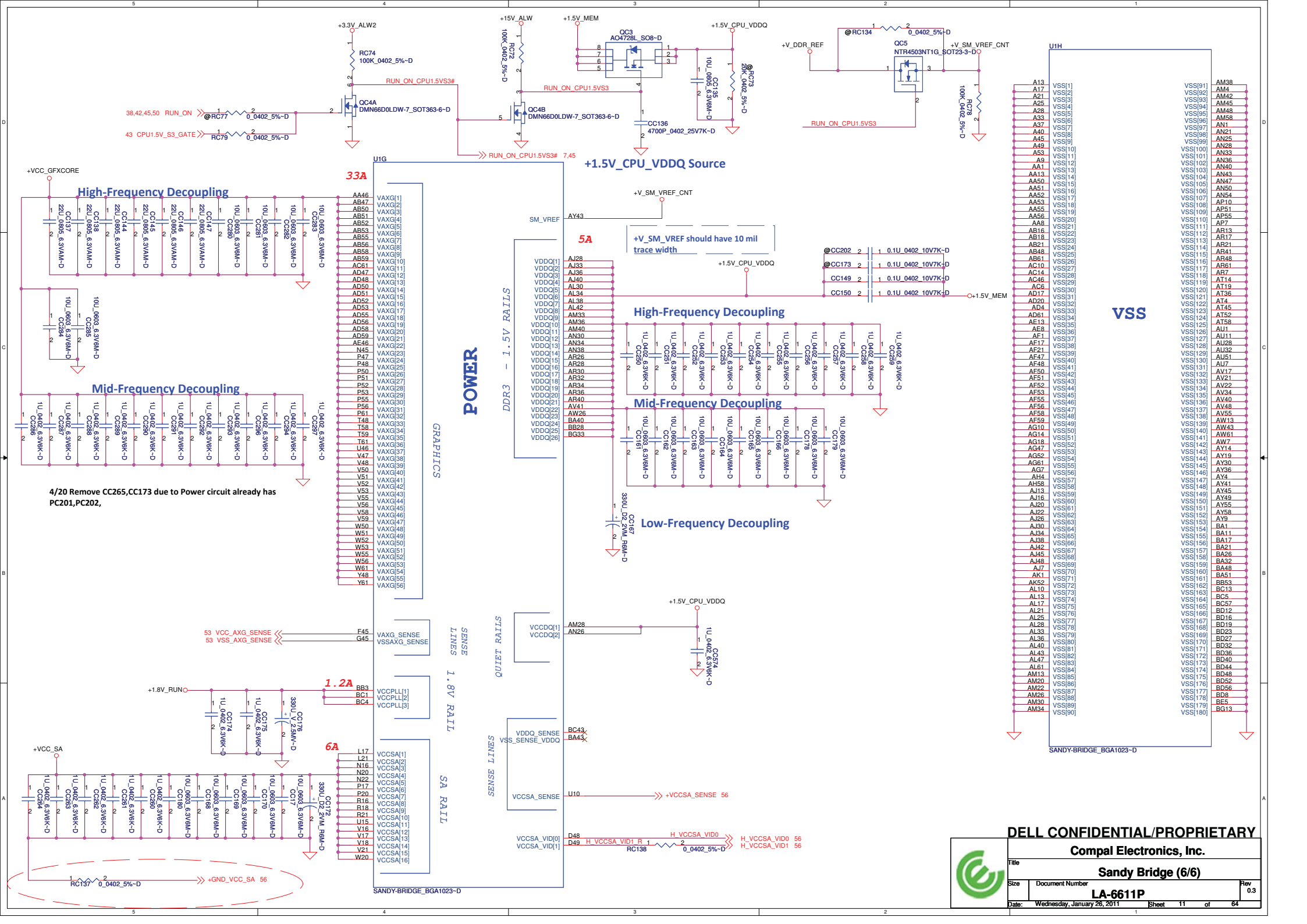
+1.5V_CPU_VDDQ Source
High-Frequency Decoupling
Mid-Frequency Decoupling
Low-Frequency Decoupling
POWER
GRAPHICS
DDR3 - 1.5V RAILS
SENSE LINES
1.8V RAIL
SA RAIL
QUIET RAIL
SENSE LINES
VSS
+V_SM_VREF should have 10 mil trace width
4/20 Remove CC265,CC173 due to Power circuit already has PC201,PC202,
SANDY-BRIDGE_BGA1023~D
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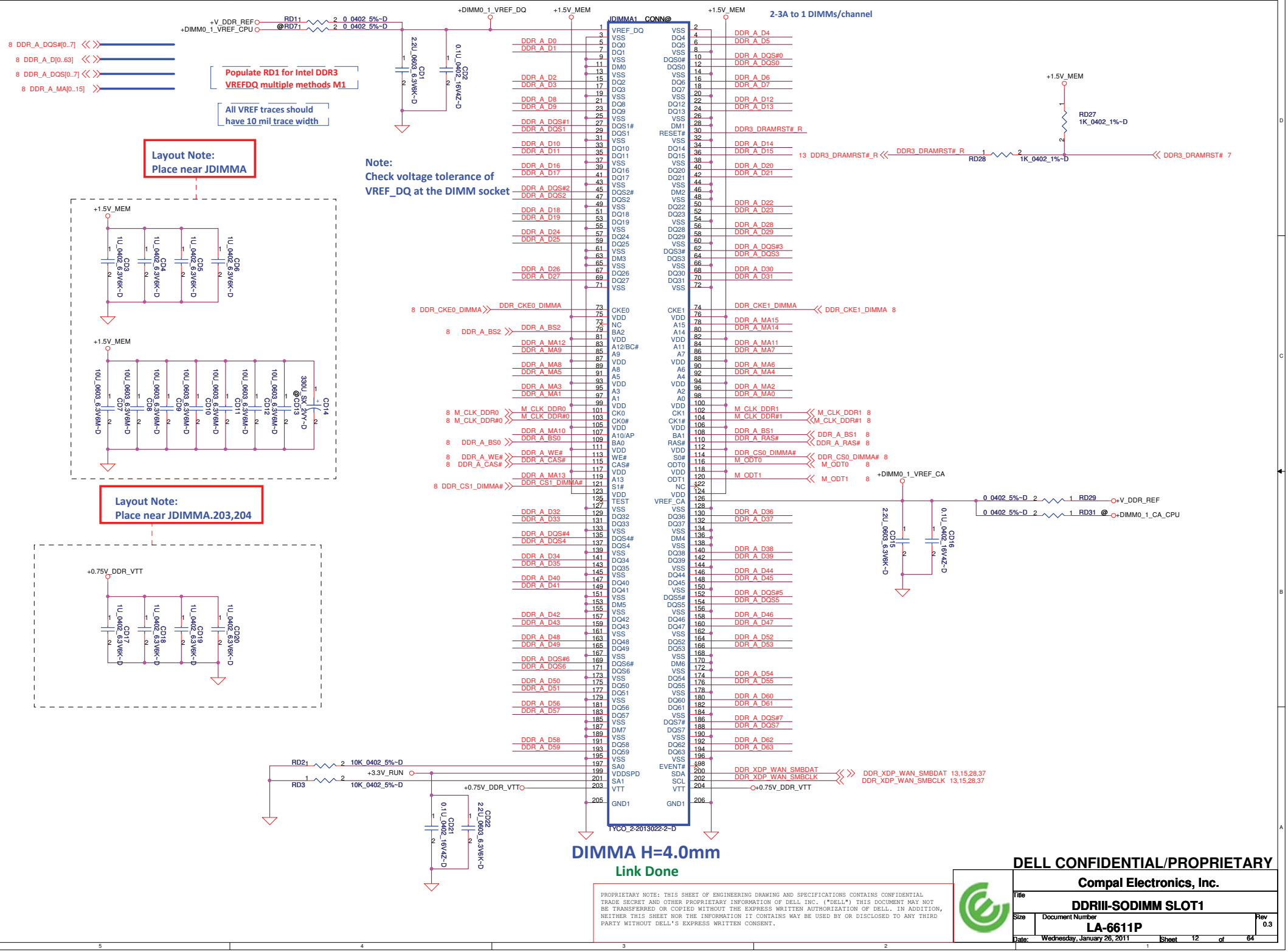
Sandy Bridge (6/6)
LA-6611P
Wednesday, January 26, 2011



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Title: DDRIII-SODIMM SLOT1

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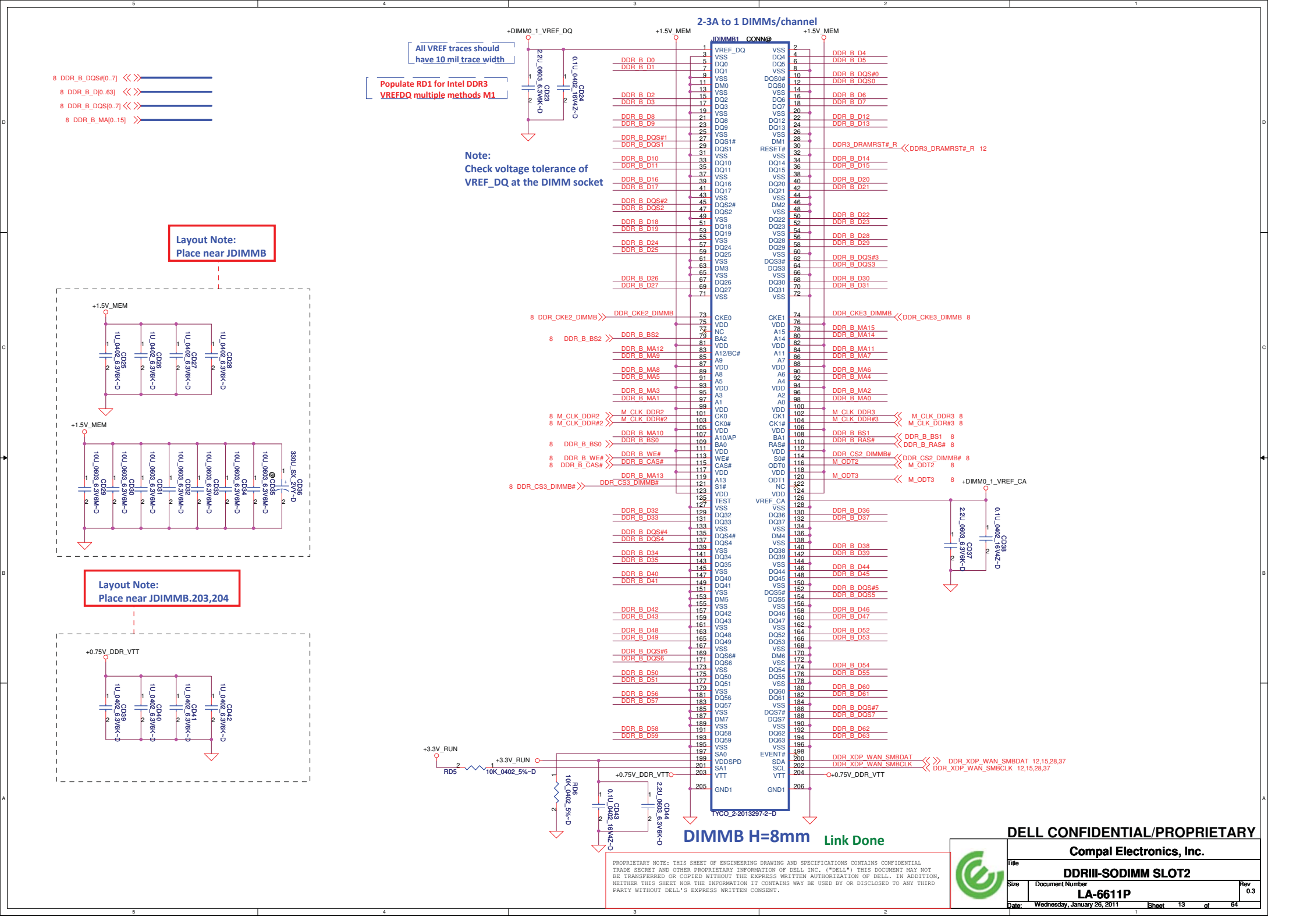
2-3A to 1 DIMMs/channel
All VREF traces should have 10 mil trace width
Populate RD1 for Intel DDR3 VREFDQ multiple methods M1
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket
Layout Note:
Place near JDIMMB
Layout Note:
Place near JDIMMB.203,204
JDIMMB1 CONN@
TYCO_2-2013297-2~D
DIMMB H=8mm
Link Done
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DDRIII-SODIMM SLOT2
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CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs

CH6 close to JXDP2

CH1 close to JXDP2

CMOS place near DIMM

Link Done

200 MIL SO8 64Mb Flash ROM

200 MIL SO8 16Mb Flash ROM

R936 colay R895 for TAA

R944 colay R897 for TAA

R943 colay R900 for TAA

Intel review feed back

HDD

ODD/ E Module Bay

E-SATA

DOCK

BBS_BIT0 - BIOS BOOT STRAP BIT 0

SATA0GP PD simulates the drive status. For proper function of the hot plug, this R1597 must be "No Shunt" when respective drive is removed and "Shunt" after the respective drive is plugged in.

SPI_MOSI
High: Enable Intel Anti-Theft Technology
Left floating: Disable Intel Anti-Theft Technology

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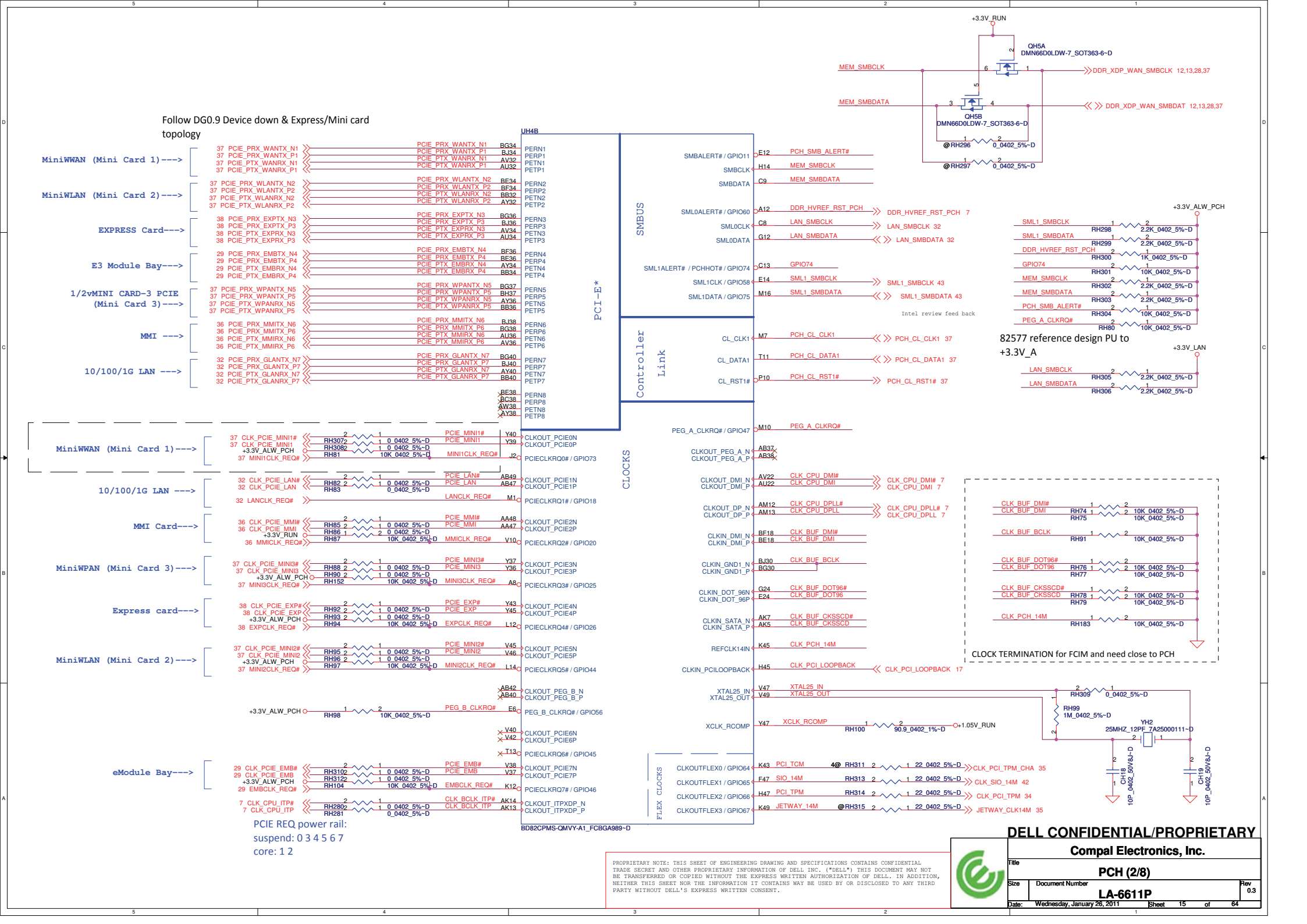
Follow DG0.9 Device down & Express/Mini card topology
MiniWWAN (Mini Card 1)--->
MiniWLAN (Mini Card 2)--->
EXPRESS Card--->
E3 Module Bay--->
1/2vMINI CARD-3 PCIE (Mini Card 3)--->
MMI --->
10/100/1G LAN --->
MiniWWAN (Mini Card 1)--->
10/100/1G LAN --->
MMI Card--->
MiniWPAN (Mini Card 3)--->
Express card--->
MiniWLAN (Mini Card 2)--->
eModule Bay--->
UH4B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
BD82CPMS-QMVY-A1_FCBGA989~D
+3.3V_RUN
QH5A DMN66D0LDW-7_SOT363-6~D
QH5B DMN66D0LDW-7_SOT363-6~D
MEM_SMBCLK
MEM_SMBDATA
DDR_XDP_WAN_SMBCLK 12,13,28,37
DDR_XDP_WAN_SMBDAT 12,13,28,37
@RH296 0_0402_5%~D
@RH297 0_0402_5%~D
+3.3V_ALW_PCH
+3.3V_LAN
82577 reference design PU to +3.3V_A
Intel review feed back
CLOCK TERMINATION for FCIM and need close to PCH
PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2
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PCH (2/8)
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Wednesday, January 26, 2011
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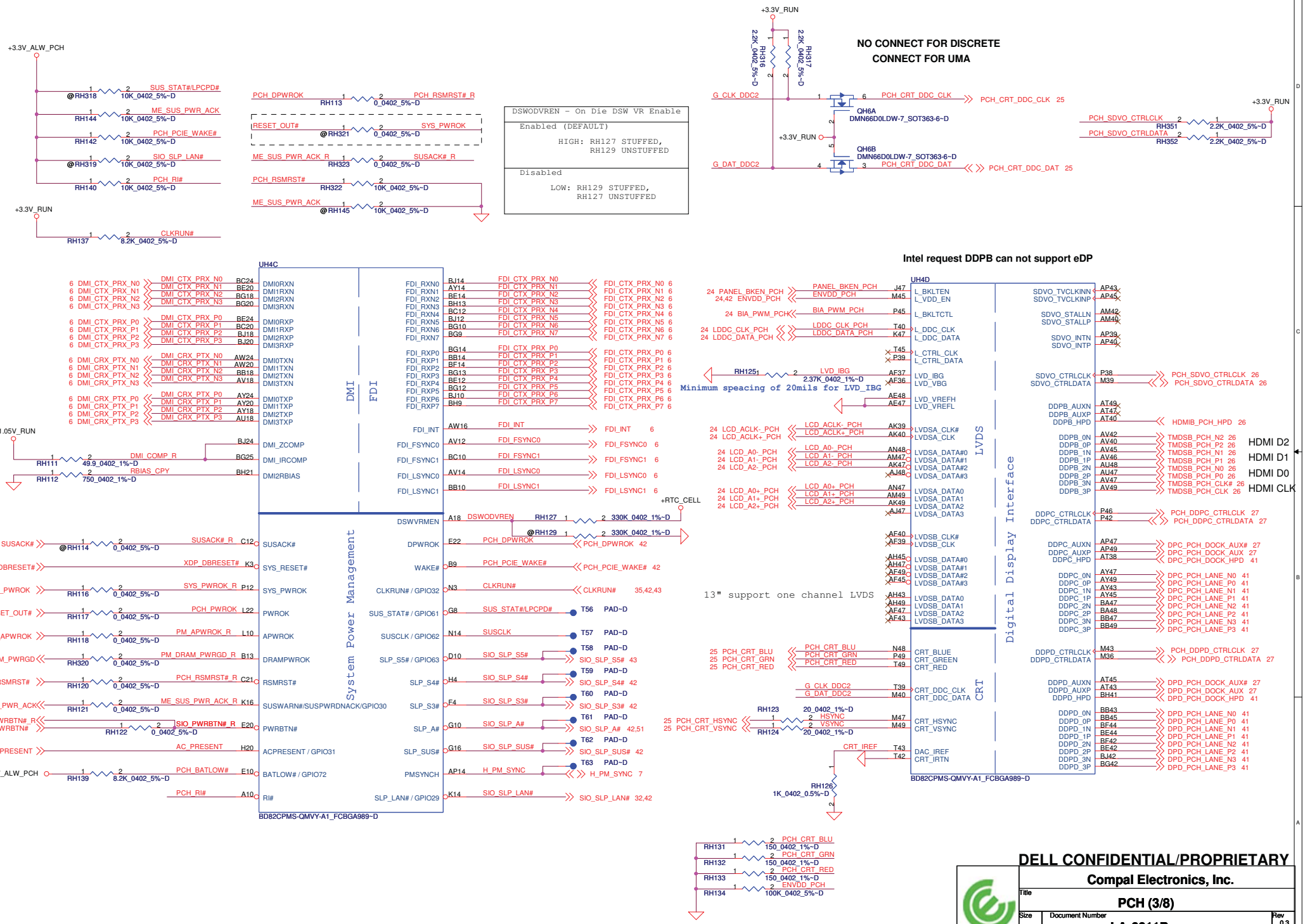
+3.3V_ALW_PCH
SUS_STAT#/LPCPD#
ME_SUS_PWR_ACK
PCH_PCIE_WAKE#
SIO_SLP_LAN#
PCH_RI#
+3.3V_RUN
CLKRUNK#
PCH_DPWROK
RESET_OUT#
SYS_PWROK
ME_SUS_PWR_ACK_R
SUSACK#_R
PCH_RSMRST#
ME_SUS_PWR_ACK
DSWODVREN - On Die DSW VR Enable
Enabled (DEFAULT)
HIGH: RH127 STUFFED, RH129 UNSTUFFED
Disabled
LOW: RH129 STUFFED, RH127 UNSTUFFED
NO CONNECT FOR DISCRETE
CONNECT FOR UMA
G_CLK_DDC2
G_DAT_DDC2
QH6A DMN66D0LDW-7_SOT363-6~D
QH6B DMN66D0LDW-7_SOT363-6~D
PCH_CRT_DDC_CLK
PCH_CRT_DDC_DAT
PCH_SDVO_CTRLCLK
PCH_SDVO_CTRLDATA
Intel request DDPB can not support eDP
UH4C
DMI
FDI
System Power Management
BD82CPMS-QMVY-A1_FCBGA989~D
UH4D
LVDS
Digital Display Interface
CRT
Minimum spacing of 20mils for LVD_IBG
13" support one channel LVDS
HDMI D2
HDMI D1
HDMI D0
HDMI CLK
+RTC_CELL
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PCH (3/8)
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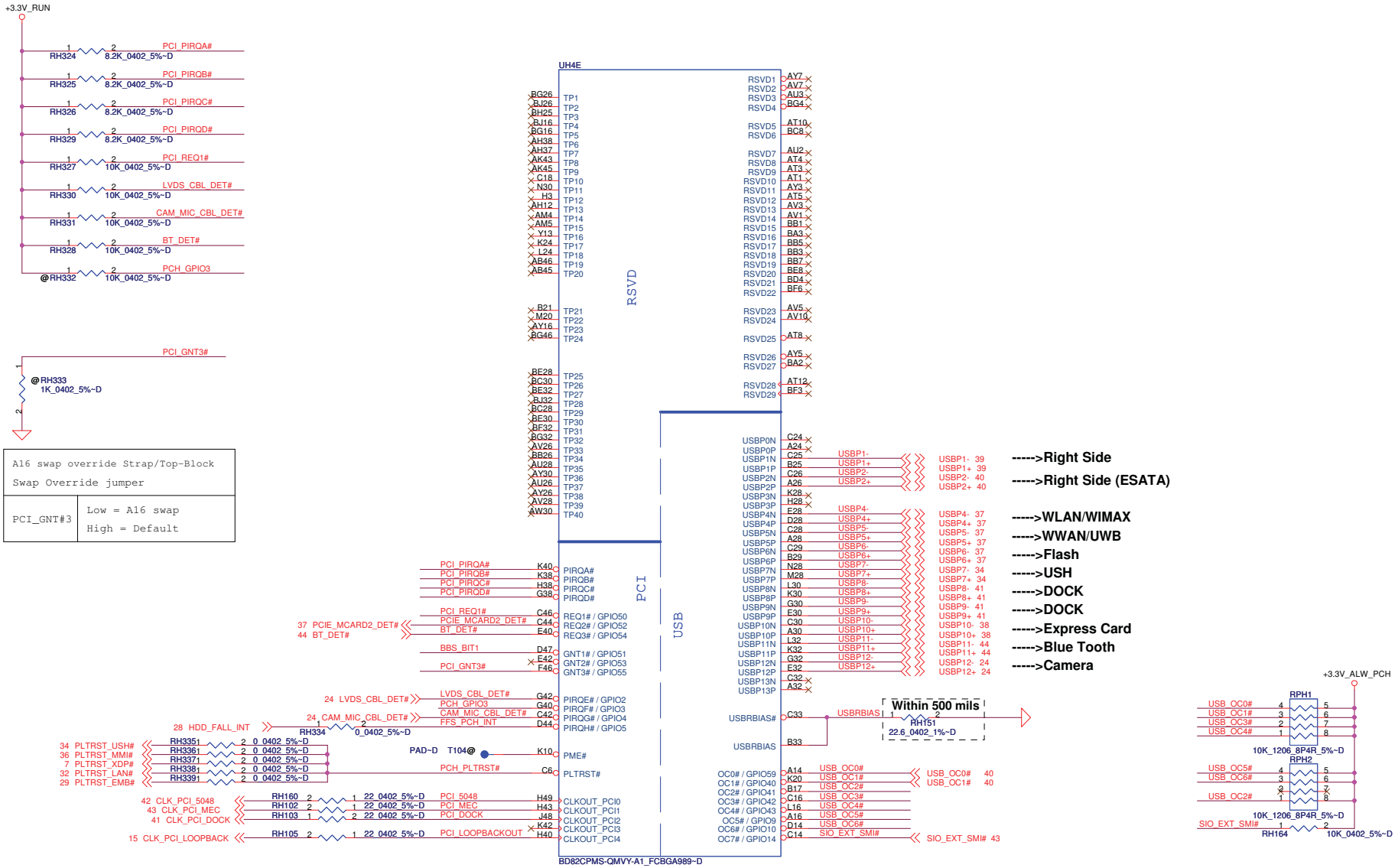

Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

★

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Title: PCH (4/8)

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+3.3V_ALW_PCH

RH355 1 2 4.7K_0402_5%~D

@RH353 1 2 1K_0402_5%~D SLP_ME_CSW_DEV#

+3.3V_RUN

SIO_EXT_SCI# RH263 1 2 10K_0402_5%~D

PLL ON DIE VR ENABLE
ENABLED - HIGH (RH238 UNSTUFFED) DEFAULT DISABLED - LOW (RH238 STUFFED)

+3.3V_ALW_PCH

RH177 1 2 10K_0402_5%~D SIO_EXT_WAKE#

Integrated Clock Chip Enable	
ICC_EN#	HIGH: DISABLED [DEFAULT] LOW: ENABLED

+3.3V_ALW_PCH

RH354 1 2 1K_0402_5%~D PCH_GPIO15

GPIO15

Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality

High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

@RH174 1 2 10K_0402_5%~D PCH_GPIO37

@RH175 1 2 10K_0402_5%~D PCH_GPIO36

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

UH4F

43 SIO_EXT_SCI#	SIO_EXT_SCI# RH259 1 2 0_0402_5%~D SIO_EXT_SCI#_R	T7	BMBUSY# / GPIO0
	PCH_GPIO1	A42	TACH1 / GPIO1
31 IO_LOOP#	IO_LOOP#	H36	TACH2 / GPIO6
31 LEDB_DET#	LEDB_DET#	E38	TACH3 / GPIO7
42 SIO_EXT_WAKE#	SIO_EXT_WAKE#	C10	GPIO8
32 PM_LANPHY_ENABLE	PM_LANPHY_ENABLE	C4	LAN_PHY_PWR_CTRL / GPIO12
	PCH_GPIO15	G2	GPIO15
	PCH_GPIO16	U2	SATA4GP / GPIO16
	GPIO17	D40	TACH0 / GPIO17
31 MEDIA_DET#	MEDIA_DET#	T5	SCLOCK / GPIO22
37 PCIE_MCARD1_DET#	PCIE_MCARD1_DET#	E8	GPIO24 / MEM_LED
38 EXPRCRD_DET#	EXPRCRD_DET#	E16	GPIO27
42 SLP_ME_CSW_DEV#	SLP_ME_CSW_DEV#	P8	GPIO28
	PCH_GPIO34	K1	STP_PCI# / GPIO34
37 USB_MCARD1_DET#	USB_MCARD1_DET#	K4	GPIO35
	PCH_GPIO36	V8	SATA2GP / GPIO36
	PCH_GPIO37	M5	SATA3GP / GPIO37
	TPM_ID0	N2	SLOAD / GPIO38
	TPM_ID1	M3	SDATAOUT0 / GPIO39
28 FFS_INT2	FFS_INT2	V13	SDATAOUT1 / GPIO48
42 TEMP_ALERT#	TEMP_ALERT#	V3	SATA5GP / GPIO49
44 KB_DET#	KB_DET#	D6	GPIO57

GPIO

	C40	CONTACTLESS_DET#	TACH4 / GPIO68
	B41	PCH_GPIO69	TACH5 / GPIO69
	C41	PCIE_MCARD3_DET#	TACH6 / GPIO70
	A40	USB_MCARD2_DET#	TACH7 / GPIO71

CPU/MISC

	P4	SIO_A20GATE	A20GATE
	AU16	H_PECI_R RH159 1 2 0_0402_5%~D	PECI
	P5	SIO_RCIN#	RCIN#
	AY11	H_CPUPWRGD	PROCPWRGD
	AY10	PCH_THRMTRIP#_R	THRMTRIP#
	T14	INIT3_3V#	INIT3_3V#
	AY1	DF_TVS	DF_TVS
	AH8		TS_VSS1
	AK11		TS_VSS2
	AH10		TS_VSS3
	AK10		TS_VSS4
	P37	NC_1	NC_1

SIO_A20GATE 43 — RH261 1 2 0_0402_5%~D — PECI_EC 43

H_PECI 7

H_CPUPWRGD 7

+1.05V_RUN_VTT

RH262 2 1 56_0402_5%~D

PAD~D T106 @

CH97 0.1U_0402_16V4Z~D

PAD~D T108 @

NCTF

VSS_NCTF_1	A4	VSS_NCTF_1	
VSS_NCTF_2	A44	VSS_NCTF_2	
VSS_NCTF_3	A45	VSS_NCTF_3	
VSS_NCTF_4	A46	VSS_NCTF_4	
VSS_NCTF_5	A5	VSS_NCTF_5	
VSS_NCTF_6	A6	VSS_NCTF_6	
VSS_NCTF_7	B3	VSS_NCTF_7	
VSS_NCTF_8	B47	VSS_NCTF_8	
VSS_NCTF_9	BD1	VSS_NCTF_9	
VSS_NCTF_10	BD49	VSS_NCTF_10	
VSS_NCTF_11	BE1	VSS_NCTF_11	
VSS_NCTF_12	BE49	VSS_NCTF_12	
VSS_NCTF_13	BF1	VSS_NCTF_13	
VSS_NCTF_14	BF49	VSS_NCTF_14	
	BG2	VSS_NCTF_15	VSS_NCTF_15
	BG48	VSS_NCTF_16	VSS_NCTF_16
	BH3	VSS_NCTF_17	VSS_NCTF_17
	BH47	VSS_NCTF_18	VSS_NCTF_18
	BJ4	VSS_NCTF_19	VSS_NCTF_19
	BJ44	VSS_NCTF_20	VSS_NCTF_20
	BJ45	VSS_NCTF_21	VSS_NCTF_21
	BJ46	VSS_NCTF_22	VSS_NCTF_22
	BJ5	VSS_NCTF_23	VSS_NCTF_23
	BJ6	VSS_NCTF_24	VSS_NCTF_24
	C2	VSS_NCTF_25	VSS_NCTF_25
	C48	VSS_NCTF_26	VSS_NCTF_26
	D1	VSS_NCTF_27	VSS_NCTF_27
	D49	VSS_NCTF_28	VSS_NCTF_28
	E1	VSS_NCTF_29	VSS_NCTF_29
	E49	VSS_NCTF_30	VSS_NCTF_30
	F1	VSS_NCTF_31	VSS_NCTF_31
	F49	VSS_NCTF_32	VSS_NCTF_32

BD82CPMS-QMVY-A1_FCBGA989~D

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

+3.3V_RUN

CONTACTLESS_DET# RH256 1 2 10K_0402_1%~D

SIO_A20GATE RH158 2 1 10K_0402_5%~D

SIO_RCIN# RH203 2 1 10K_0402_5%~D

PCH_GPIO1 RH254 2 1 10K_0402_5%~D

PCH_GPIO34 RH165 2 1 10K_0402_5%~D

EXPRCRD_DET# RH241 1 2 10K_0402_5%~D

GPIO27 (EXPRCRD_DET#)
Default = Do not connect (floating)
High (1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCH_GPIO69 RH260 1 2 1.5K_0402_1%~D

+VCCDFTERM

RH149 2.2K_0402_5%~D

DF_TVS_R RH150 1 2 0_0402_5%~D DF_TVS

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

+3.3V_RUN

@RH171 2 1 10K_0402_5%~D PCH_GPIO36

@RH173 2 1 1K_0402_1%~D PCH_GPIO37

RH265 2 1 10K_0402_5%~D PCH_GPIO16

RH266 2 1 10K_0402_5%~D TEMP_ALERT#

RH272 1 2 10K_0402_5%~D MEDIA_DET#

RH269 1 2 8.2K_0402_5%~D GPIO17

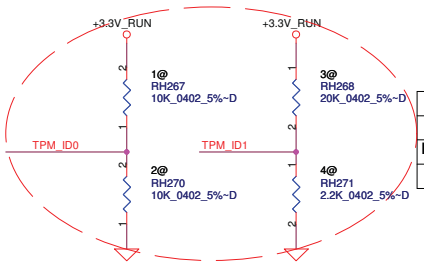
RH163 1 2 10K_0402_5%~D IO_LOOP#

RH273 1 2 10K_0402_5%~D LEDB_DET#

+3.3V_ALW_PCH

RH170 2 1 10K_0402_5%~D KB_DET#

Need to modify follow TPM BOM config.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH2.0	1	1

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Compal Electronics, Inc.

Title: **PCH (5/8)**

Size | Document Number: **LA-6611P** | Rev: 0.3

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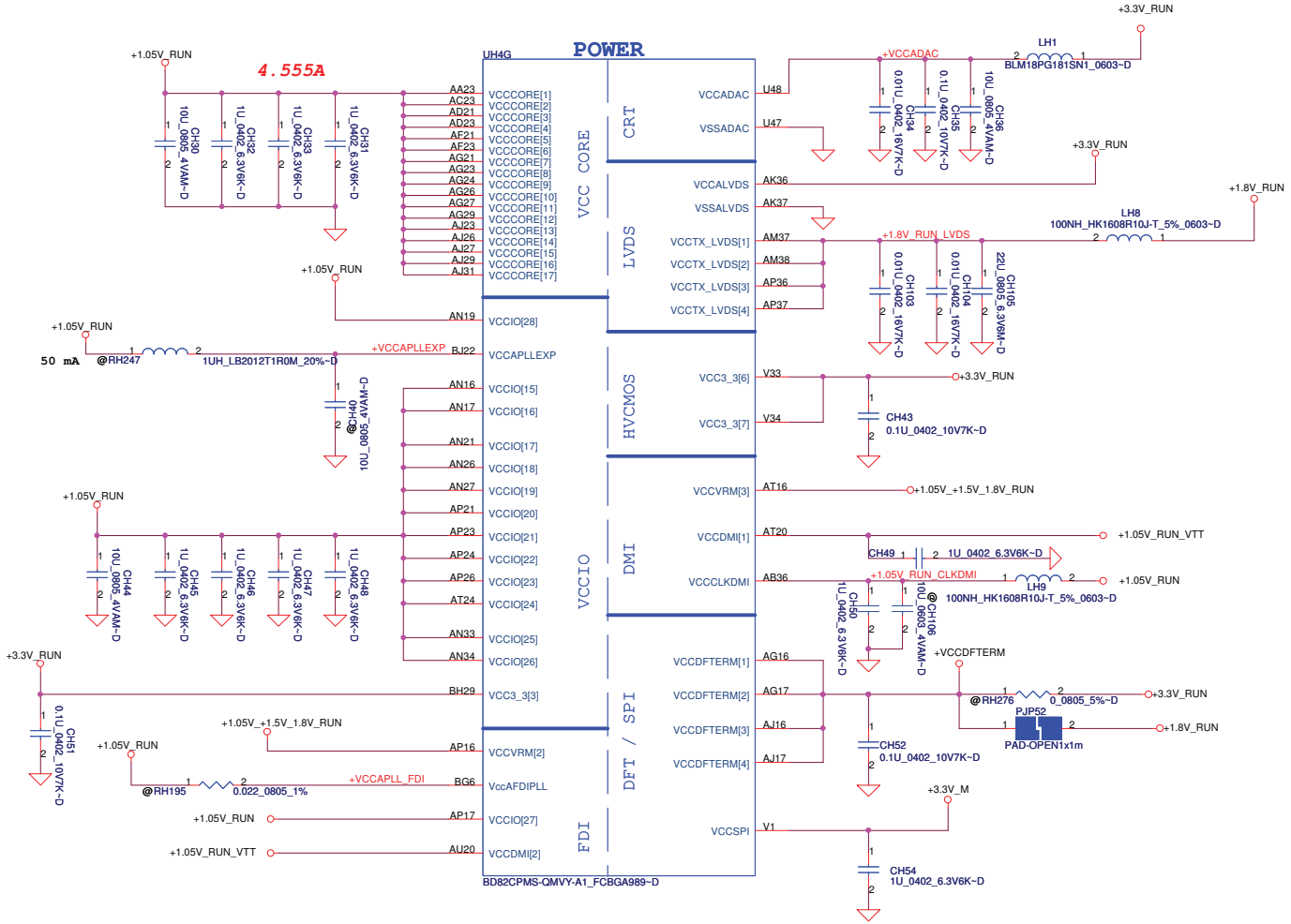

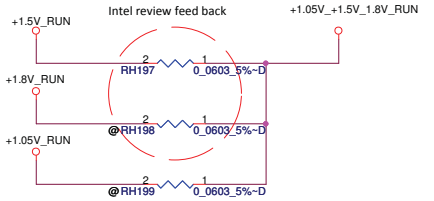

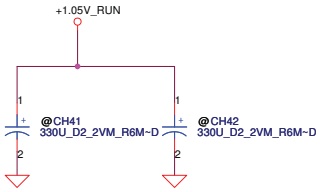

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
+VCCDFTERM	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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Title: PCH (6/8)

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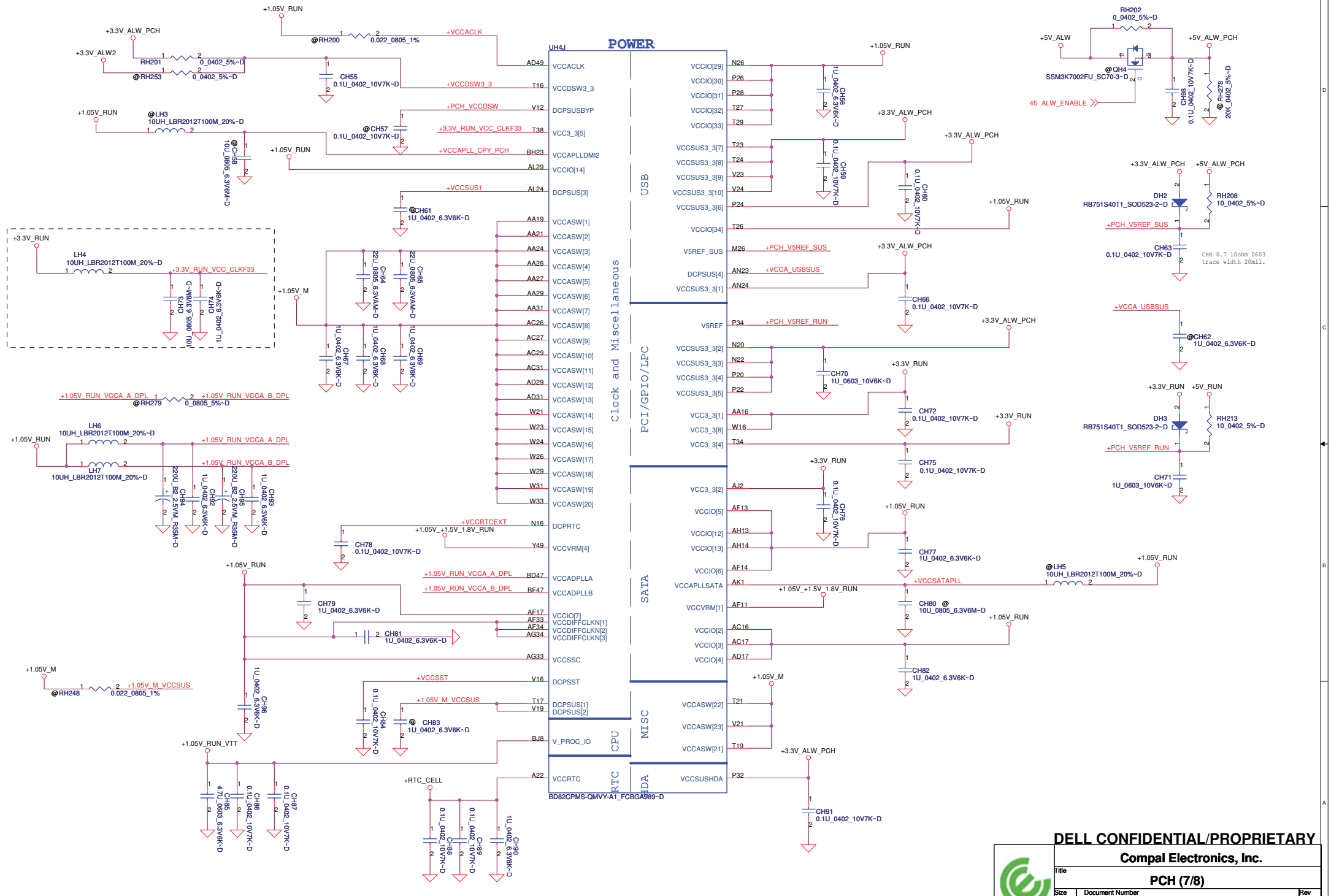
POWER
UH4J
BD82CPMS-QMVY-A1_FCBGA989~D
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
VCCACLK
VCCDSW3_3
DCPSUSBYP
VCC3_3[5]
VCCAPLLDMI2
VCCIO[14]
DCPSUS[3]
VCCASW[1]
VCCASW[2]
VCCASW[3]
VCCASW[4]
VCCASW[5]
VCCASW[6]
VCCASW[7]
VCCASW[8]
VCCASW[9]
VCCASW[10]
VCCASW[11]
VCCASW[12]
VCCASW[13]
VCCASW[14]
VCCASW[15]
VCCASW[16]
VCCASW[17]
VCCASW[18]
VCCASW[19]
VCCASW[20]
DCPRTC
VCCVRM[4]
VCCADPLLA
VCCADPLLB
VCCIO[7]
VCCDIFFCLKN[1]
VCCDIFFCLKN[2]
VCCDIFFCLKN[3]
VCCSSC
DCPSST
DCPSUS[1]
DCPSUS[2]
V_PROC_IO
VCCRTC
VCCIO[29]
VCCIO[30]
VCCIO[31]
VCCIO[32]
VCCIO[33]
VCCSUS3_3[7]
VCCSUS3_3[8]
VCCSUS3_3[9]
VCCSUS3_3[10]
VCCSUS3_3[6]
VCCIO[34]
V5REF_SUS
DCPSUS[4]
VCCSUS3_3[1]
V5REF
VCCSUS3_3[2]
VCCSUS3_3[3]
VCCSUS3_3[4]
VCCSUS3_3[5]
VCC3_3[1]
VCC3_3[8]
VCC3_3[4]
VCC3_3[2]
VCCIO[5]
VCCIO[12]
VCCIO[13]
VCCIO[6]
VCCAPLLSATA
VCCVRM[1]
VCCIO[2]
VCCIO[3]
VCCIO[4]
VCCASW[22]
VCCASW[23]
VCCASW[21]
VCCSUSHDA
+1.05V_RUN
+3.3V_ALW_PCH
+3.3V_ALW2
+VCCACLK
+VCCDSW3_3
+PCH_VCCDSW
+3.3V_RUN_VCC_CLKF33
+VCCAPLL_CPY_PCH
+VCCSUS1
+3.3V_RUN
+1.05V_M
+1.05V_RUN_VCCA_A_DPL
+1.05V_RUN_VCCA_B_DPL
+VCCRTCEXT
+1.05V_+1.5V_1.8V_RUN
+VCCSST
+1.05V_M_VCCSUS
+1.05V_RUN_VTT
+RTC_CELL
+PCH_V5REF_SUS
+VCCA_USBSUS
+PCH_V5REF_RUN
+VCCSATAPLL
+5V_ALW
+5V_ALW_PCH
+5V_RUN
45_ALW_ENABLE
CRB 0.7 10ohm 0603 trace width 20mil.
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PCH (7/8)
LA-6611P
Rev 0.3
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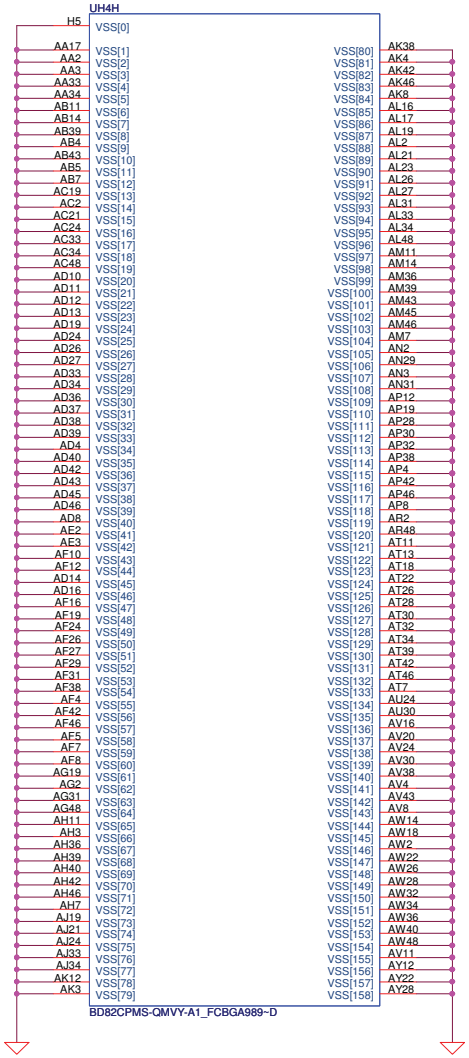

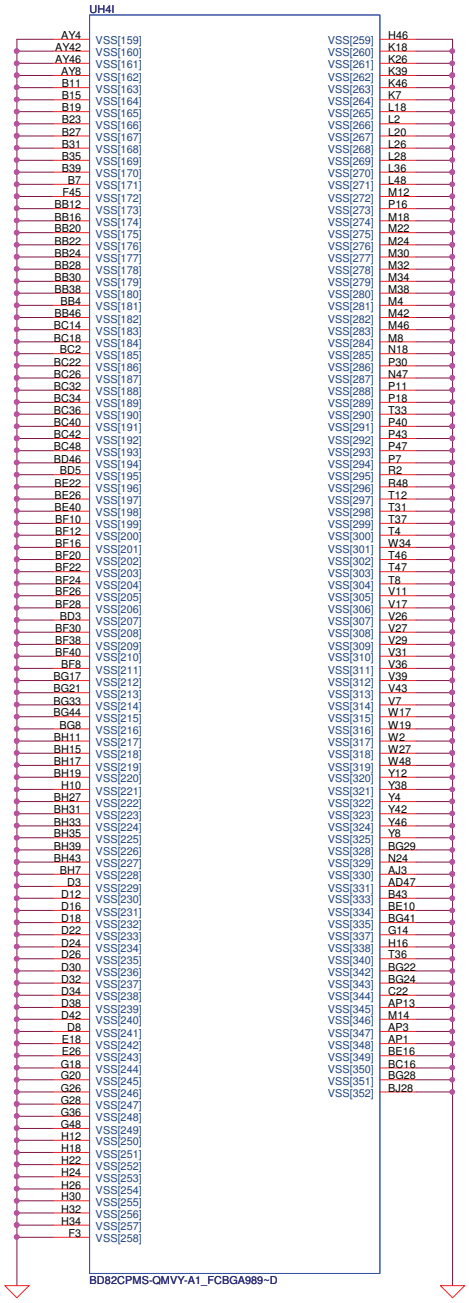

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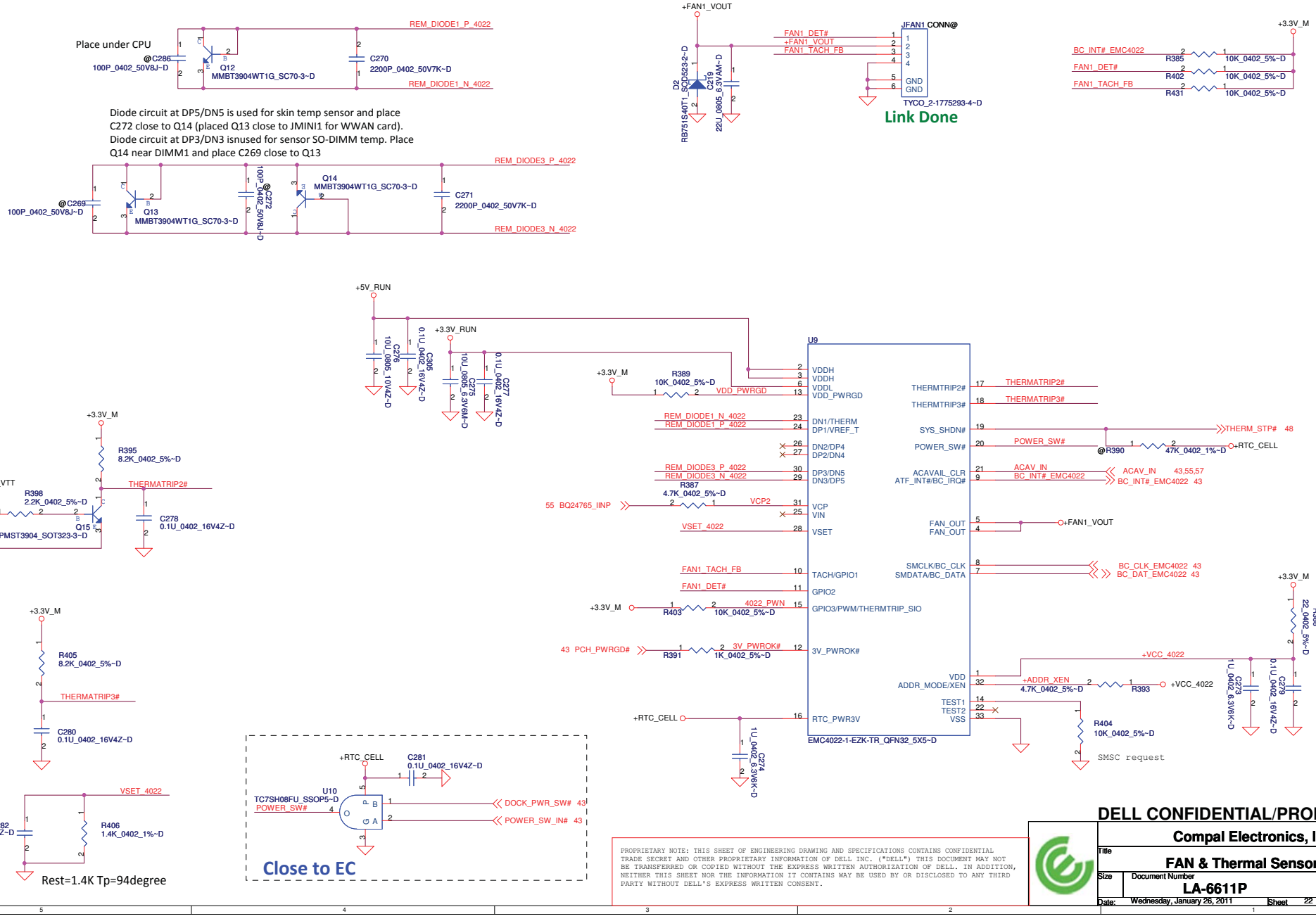
Title	PCH (8/8)	
Size	Document Number: LA-6611P	Rev: 0.3
Date: Wednesday, January 26, 2011	Sheet 21 of 64	



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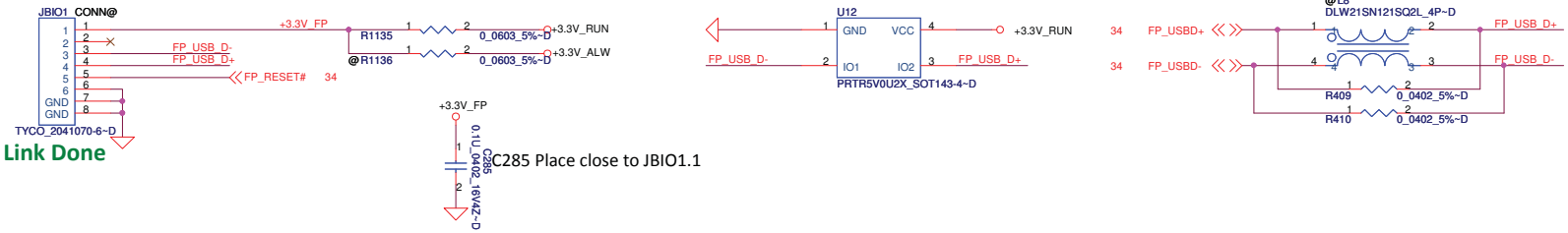
Compal Electronics, Inc.

Title: FAN & Thermal Sensor

Size: | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 22 of 64

Fingerprint CONN.



Link Done

C285 Place close to JBIO1.1

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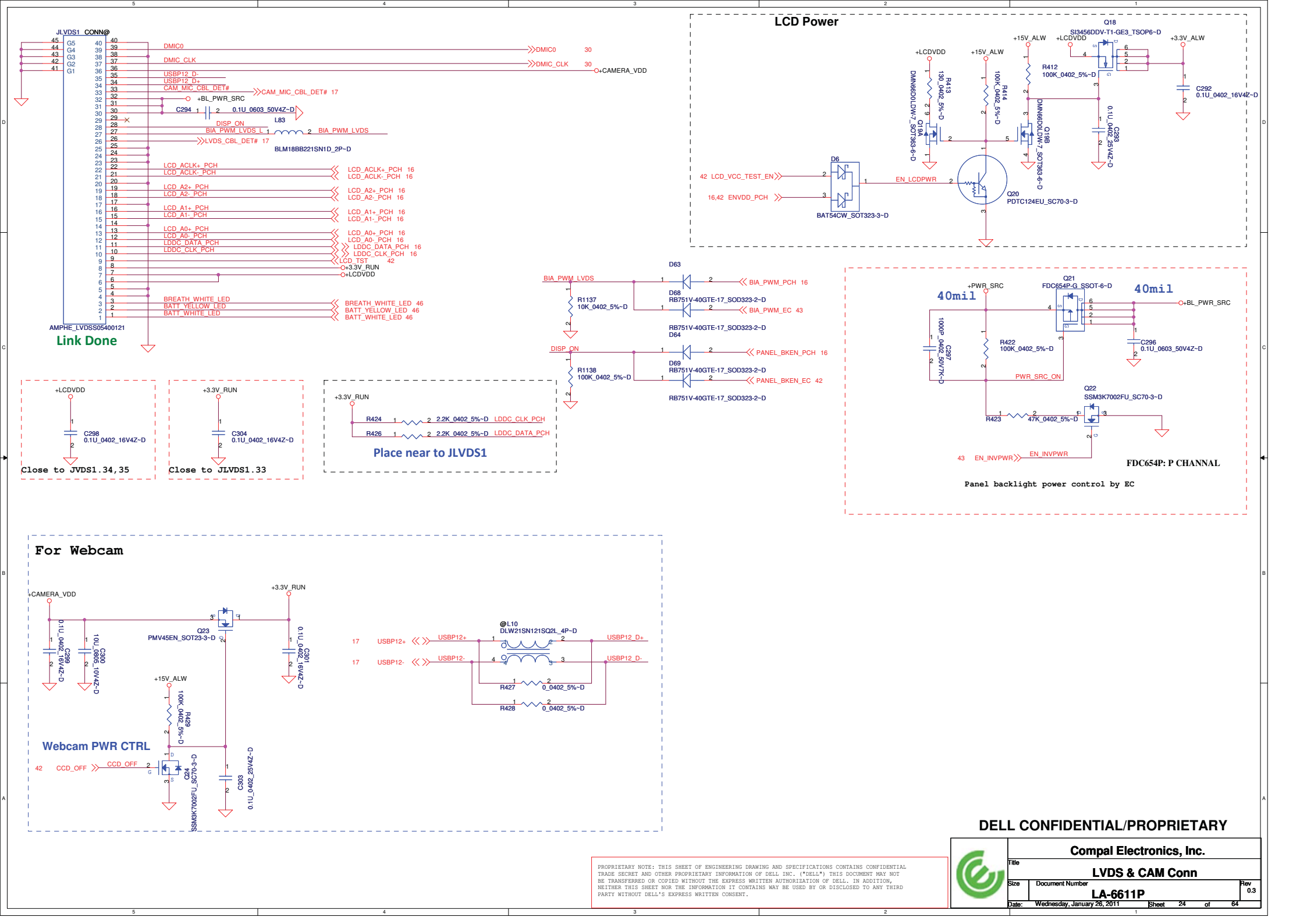
Compal Electronics, Inc.		
Title: FP Conn.		
Size	Document Number: LA-6611P	Rev: 0.3
Date: Wednesday, January 26, 2011	Sheet 23 of 64	



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Compal Electronics, Inc.	
Title	LVDS & CAM Conn
Size	Document Number: LA-6611P
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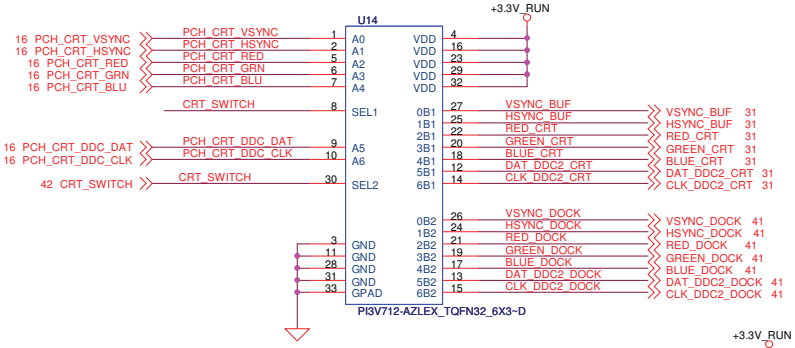
VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

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Compal Electronics, Inc.

Title: CRT switch

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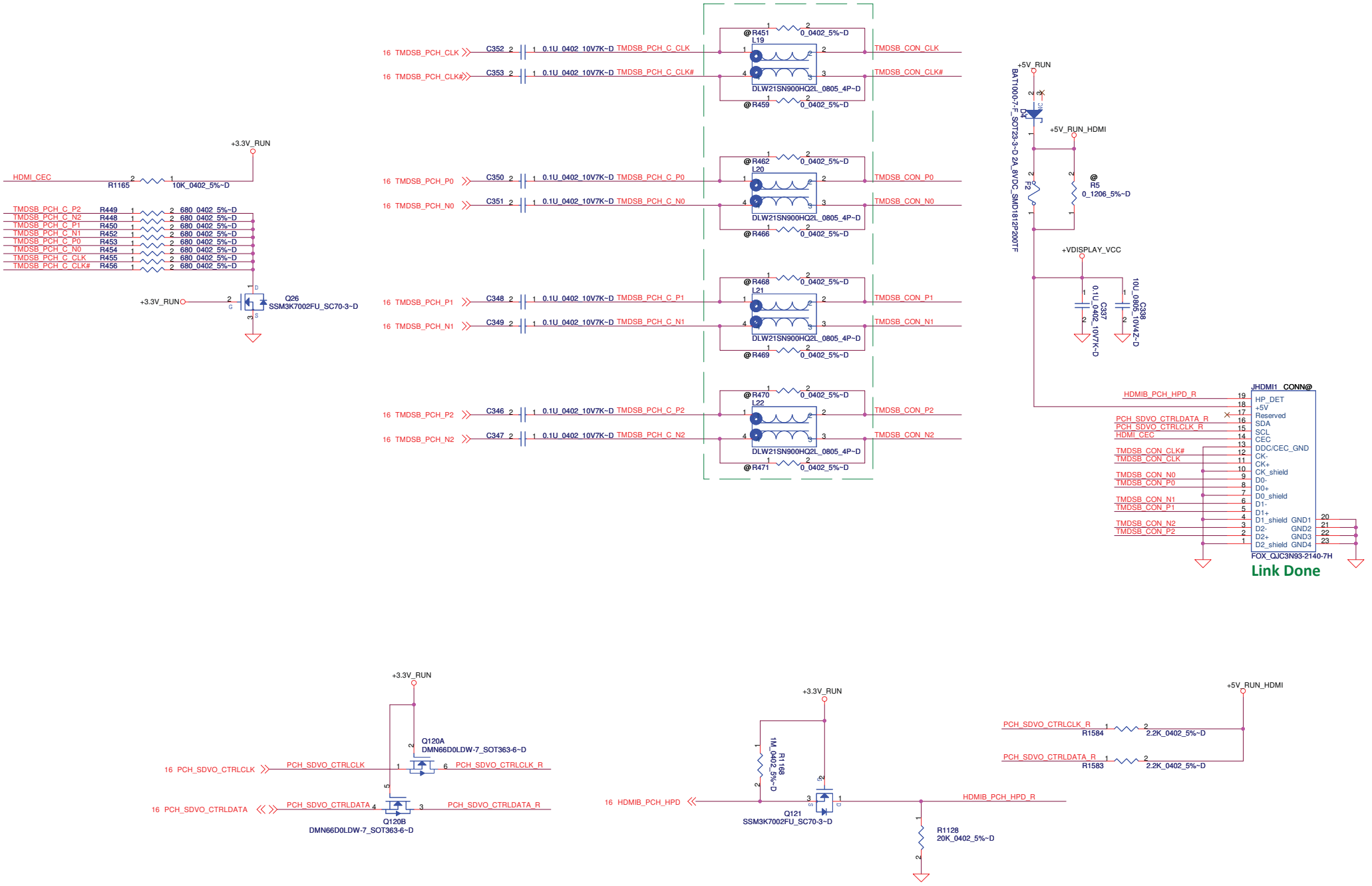

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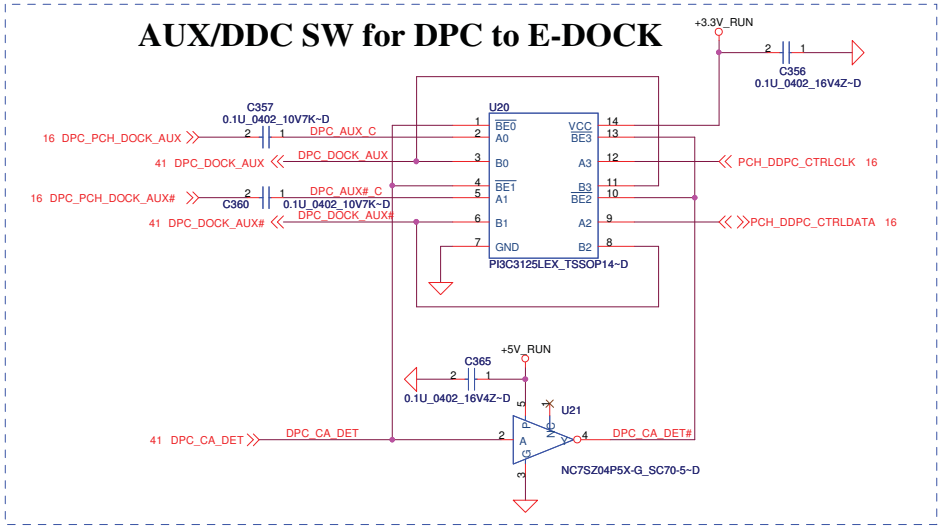
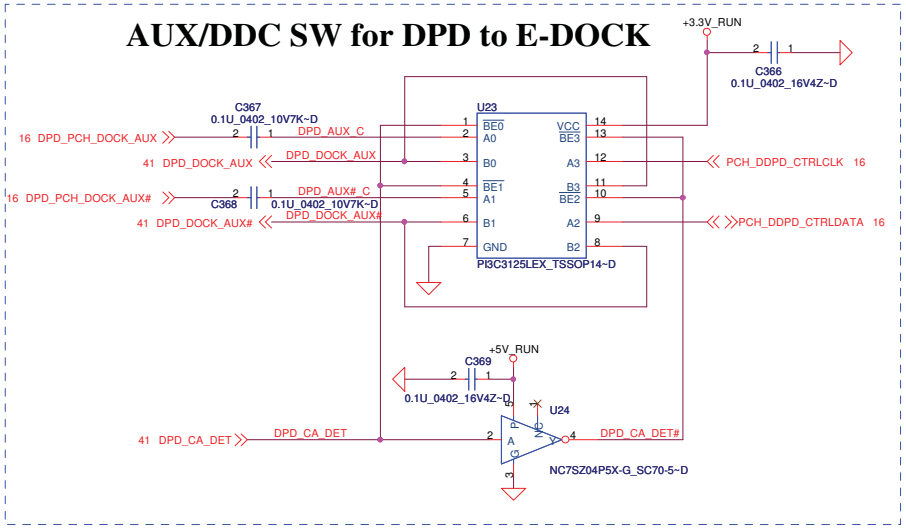
Compal Electronics, Inc.

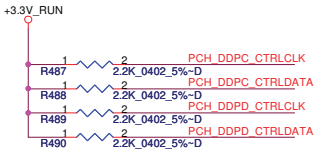
Title: HDMI port

Size | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 26 of 64







Intel WW18 Strapping option

Intel WW18 Strapping option

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Compal Electronics, Inc.	
Title	DP SW
Size	Document Number: LA-6611P
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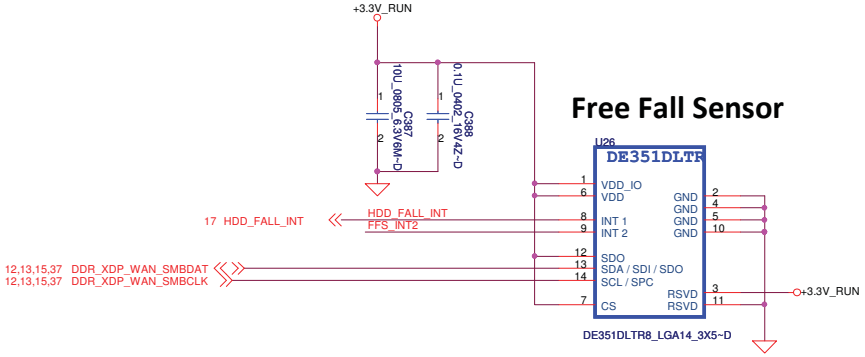

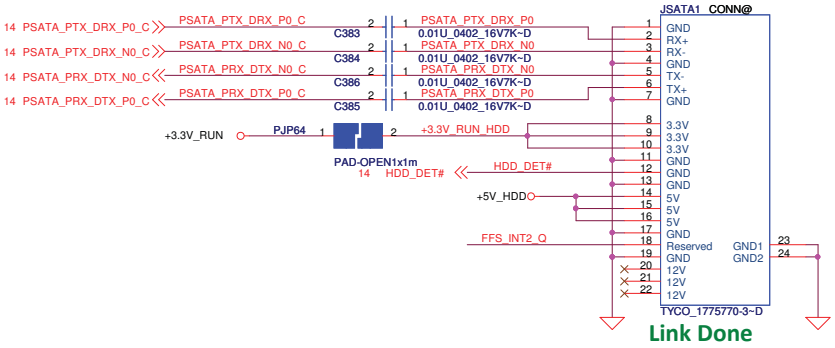

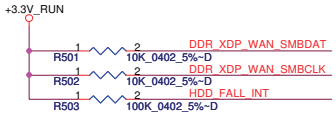

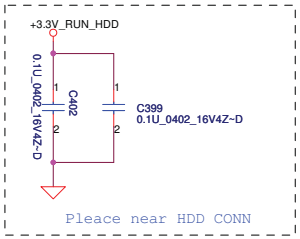

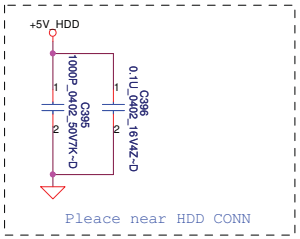

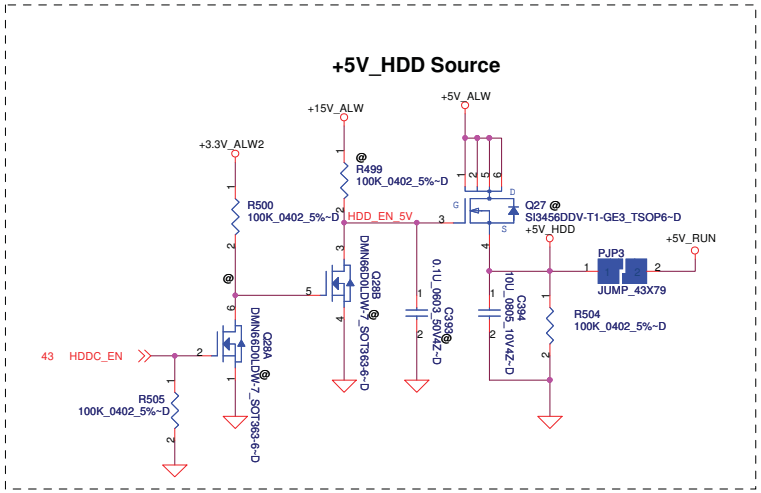

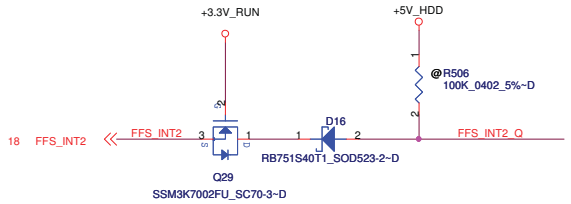

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Compal Electronics, Inc.

Title: HDD CONNECTOR

Size | Document Number: LA-6611P | Rev: 0.3

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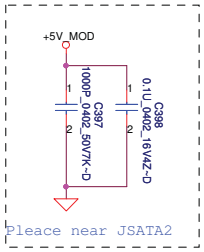
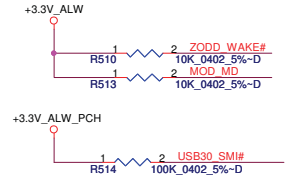
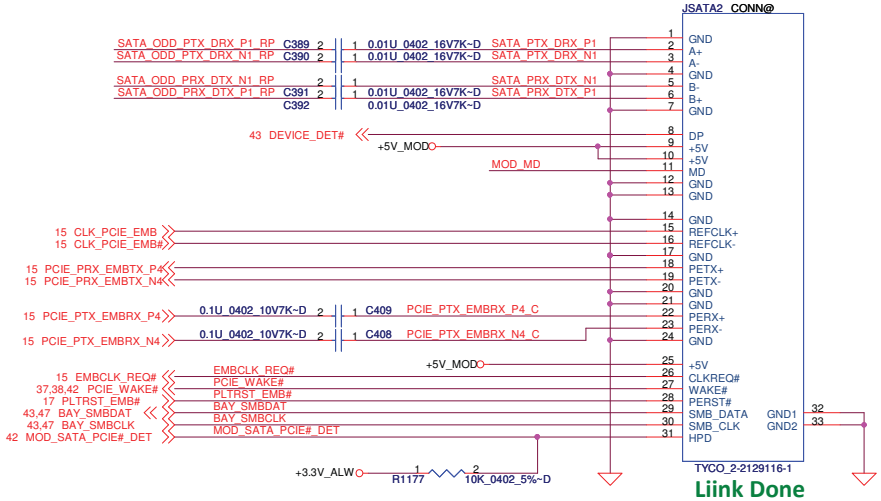
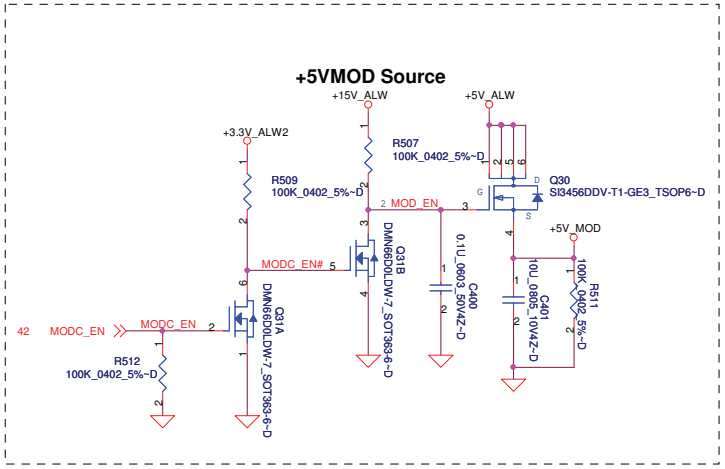
For ODD

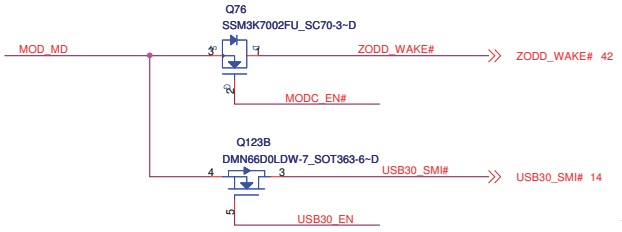


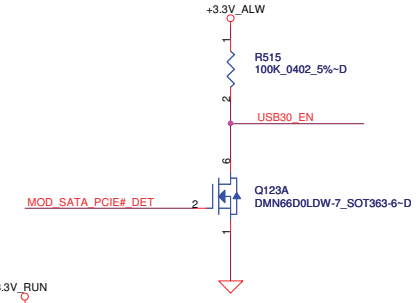




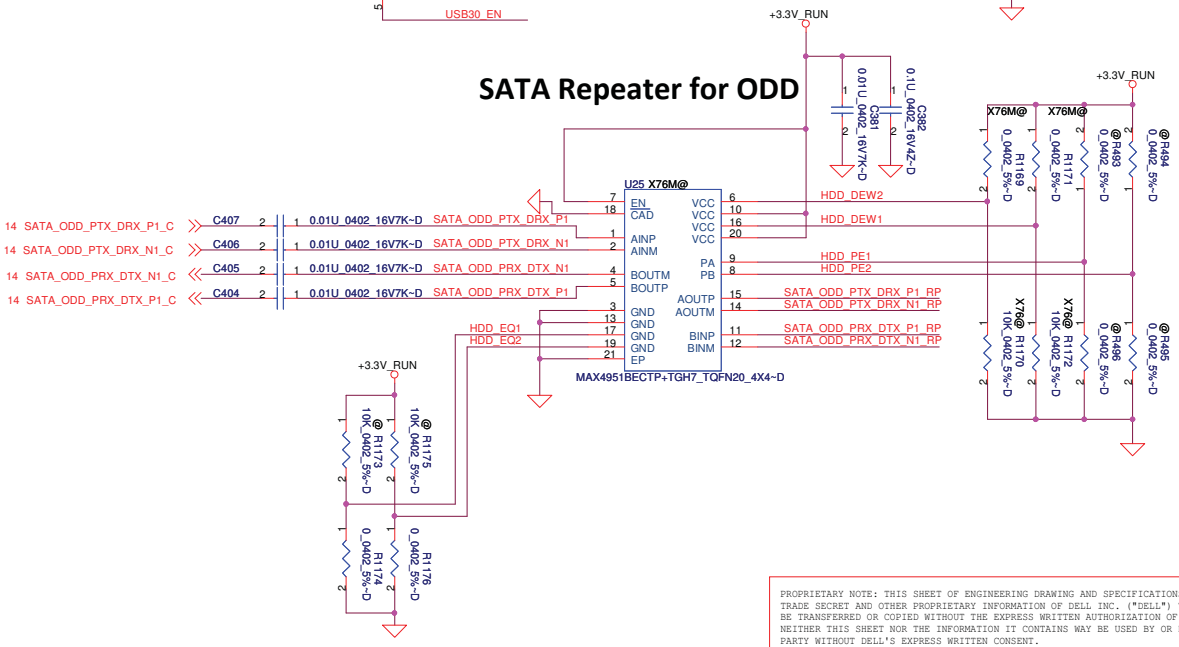
Liink Done







SATA Repeater for ODD



SA00003LH1L SA00003ZX0L

	MAXIM	TI
R1169 R1171	pop	depop
R1170 R1172	depop	pop

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DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: ODD CONNECTOR

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Internal Speakers Header

20 mils trace

INT_SPK_L+ L78 BLM18BD121SN1D_2P~D INT_SPKL_L+
INT_SPK_L- L79 BLM18BD121SN1D_2P~D INT_SPKL_L-
INT_SPK_R+ L80 BLM18BD121SN1D_2P~D INT_SPKR_R+
INT_SPK_R- L81 BLM18BD121SN1D_2P~D INT_SPKR_R-

C973 680P_0402_50V7K~D
C974 680P_0402_50V7K~D
C975 680P_0402_50V7K~D
C976 680P_0402_50V7K~D

Link Done
Speaker Connector

JSPK1 Conn@
TYCO_2-1775765-4

DVDD_IO should match with HDA Bus level

+3.3V_RUN

C951 0.1U_0402_16V4Z~D
C952 1U_0603_10V6K~D
C953 0.1U_0402_16V4Z~D
C954 10U_0805_10V6K~D

Place C951~C961 close to Codec

U72
92HD90B2X5NLGXAX8_QFN48_7X7~D

DVDD_CORE	1
DVDD_IO	3
DVDD	9
BITCLK	6
SDATA_OUT	5
SYNC	10
SDATA_IN	8
RESET#	11
I2S_MCLK	15
I2S_SCLK	16
I2S_DOUT	17
I2S_LRCLK	18
I2S_DIN	24
No Connect	19
No Connect	20
EAPD	47
DVSS	7
PVSS	42
GND	49
AVDD1	27
AVDD2	38
PVDD	45
PVDD	39
SENSE_A	13
SENSE_B	14
PORTA_L	28
PORTA_R	29
VrefOut_A	23
PORTB_L	31
PORTB_R	32
PORTD_+L	40
PORTD_-L	41
PORTD_+R	44
PORTD_-R	43
MONO_OUT	25
PC_BEEP	12
DMIC_CLK/GPIO 1	2
DMIC_0/GPIO 2	4
DMIC1/GPIO0/SPDIFOUT1	46
SPDIFOUT0//GPIO3/Aux_Out	48
CAP+	36
CAP-	35
VREFFILT	21
CAP2	22
V-	34
Vreg	37
AVSS1	26
AVSS	30
AVSS	33

14 PCH_AZ_CODEC_BITCLK → PCH_AZ_CODEC_BITCLK
14 PCH_AZ_CODEC_SDOUT → PCH_AZ_CODEC_SDOUT
14 PCH_AZ_CODEC_SYNC → PCH_AZ_CODEC_SYNC
14 PCH_AZ_CODEC_SDIN0 → Place R1096 close to codec → R1096 33_0402_5%~D → PCH_AZ_CODEC_SDIN0_R
14 PCH_AZ_CODEC_RST# → PCH_AZ_CODEC_RST#

I2S_12MHZ
I2S_BCLK
I2S_DO → Place R1097 close to codec → R1097 33_0402_5%~D → I2S_DO_R
I2S_LRCLK
I2S_DI#

42 AUD_NB_MUTE# → +3.3V_RUN → R1099 10K_0402_5%~D

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

+5V_RUN → R961 0_0805_5%~D

L77 BLM21PG600SN1D_0805~D

+VDDA_AVDD
C955 10U_0805_10V6K~D
C956 1U_0603_10V6K~D
C957 0.1U_0402_16V4Z~D
C1172 1U_0603_10V6K~D
C1173 0.1U_0402_16V4Z~D

+VDDA_PVDD
C858 10U_0805_10V6K~D
C859 0.1U_0402_16V4Z~D
C860 10U_0805_10V6K~D
C861 0.1U_0402_16V4Z~D

AUD_SENSE_A
AUD_SENSE_B

MIC_IN_L C1155 1U_0402_6.3V6K~D MIC_IN_R 31
+VREFOUT
AUD_HP_OUT_L R1143 2.2K_0402_5%~D AUD_HP_OUT_L 31
AUD_HP_OUT_R AUD_HP_OUT_R 31

INT_SPK_L+
INT_SPK_L-
INT_SPK_R+
INT_SPK_R-

AUD_PC_BEEP
C1113 0.1U_0402_16V4Z~D SPKR_R → R1119 100K_0402_5%~D SPKR 14
C1114 0.1U_0402_16V4Z~D BEEP_R → R1120 100K_0402_5%~D BEEP 43

DMIC_CLK_R L82 BLM18BB221SN1D_2P~D DMIC_CLK DMIC0 24 24
@R1141 10K_0402_5%~D
@R1142 10K_0402_5%~D

C962 4.7U_0603_10V6K~D
Place C962 close to Codec

Place C963~C966 close to Codec
C963 4.7U_0603_10V6K~D
C964 4.7U_0603_10V6K~D
C965 1U_0603_10V6K~D
C966 10U_0805_10V6K~D

+VREFOUT
C1180 1U_0603_10V6K~D

Close to U72 pin5
PCH_AZ_CODEC_SDOUT
@R1077 47_0402_5%~D
@C978 0.1U_0402_10V7K~D

Close to U72 pin6
PCH_AZ_CODEC_BITCLK
@R1076 10_0402_5%~D
@C977 10P_0402_50V8J~D

Place closely to Pin 13.

+VDDA_AVDD
AUD_SENSE_A
R1083 2.49K_0402_1%~D
R1086 20K_0402_1%~D
C980 1000P_0402_50V7K~D
+3.3V_RUN
R1087 100K_0402_5%~D
5 AUD_HP_NB_SENSE
Q107B DMN66D0LDW-7_SOT363-6~D
AUD_HP_NB_SENSE 31,42

Add for solve pop noise and detect issue

Place closely to Pin 14

+VDDA_AVDD
AUD_SENSE_B
R1078 2.49K_0402_1%~D
+3.3V_RUN
R1079 39.2K_0402_1%~D
R1081 100K_0402_5%~D
R1080 20K_0402_1%~D
C979 1000P_0402_50V7K~D
+3.3V_RUN
R1082 100K_0402_5%~D
42 DOCK_HP_DET
Q106A DMN66D0LDW-7_SOT363-6~D
Q106B DMN66D0LDW-7_SOT363-6~D
DOCK_MIC_DET 42

Port	Function
A	External MIC
B	HearPhone Out
C	Dock Audio
D	Internal SPK

Tie Analog Ground to Digital ground under codec by a single point
PJP62
PAD-OPEN1x1m

place at GNDA and DGND plane
C267 0.1U_0402_16V4Z~D
C283 0.1U_0402_16V4Z~D
C284 0.1U_0402_16V4Z~D

MCLK[2:0]	Frequency (MHz)	PLL clock divisor	suggested sample rate	Notes
000	24	NA	96KHz	HD Audio BitClk
001	12	NA	48KHz	HD Audio BitClk/2
010	22.5792	5	88.2KHz	
011	11.2896	10	44.1KHz	

Resistor	SENSE_A	SENSE_B
39.2K	PORT A (HP0)	PORT E
20K	PORT B (HP1)	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

+3.3V_RUN
C1103 0.1U_0402_10V7K~D

U73
CD74HC366M96_SO16~D

VCC	16
1A	2
2A	4
3A	6
4A	10
5A	12
6A	14
OE1#	1
OE2#	15
GND	8
1Y#	3
2Y#	5
3Y#	7
4Y#	9
5Y#	11
6Y#	13

I2S_BCLK
I2S_LRCLK
I2S_DO
I2S_12MHZ
I2S_DI#
42 EN_I2S_NB_CODEC#
R1110 1K_0402_5%~D

@D54 DA204U_SOT323-3~D
@D55 DA204U_SOT323-3~D
@D56 DA204U_SOT323-3~D
@D57 DA204U_SOT323-3~D

DAI_BCLK# 41
DAI_LRCK# 41
DAI_DO# 41
DAI_12MHZ# 41
DAI_DI 41

+3.3V_RUN
@D58 DA204U_SOT323-3~D

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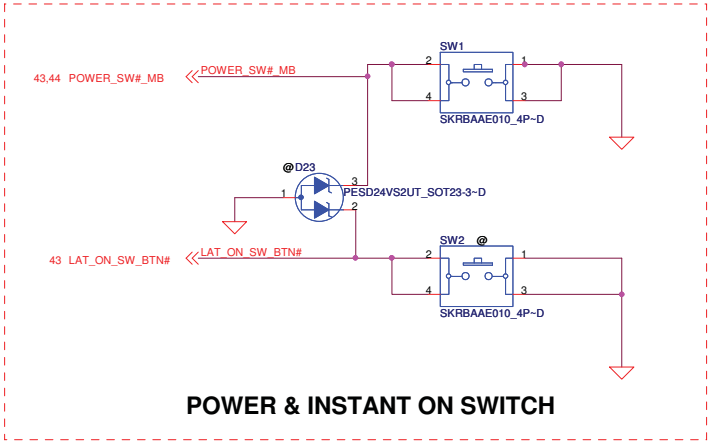
Compal Electronics, Inc.
Title: Azalia (HD) Codec
Size: Document Number: LA-6611P
Rev: 0.3
Date: Wednesday, January 26, 2011
Sheet 30 of 64

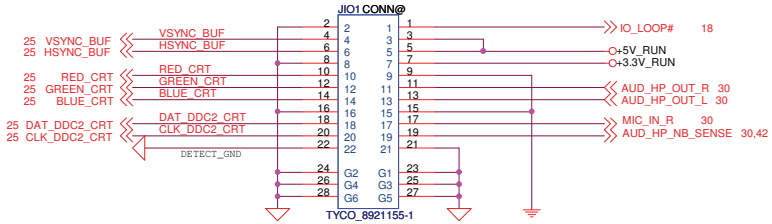


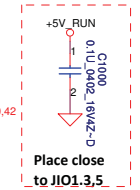
POWER & INSTANT ON SWITCH

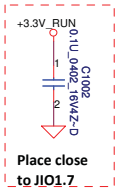
I/O board CONN.

LS-6611P

Link Done



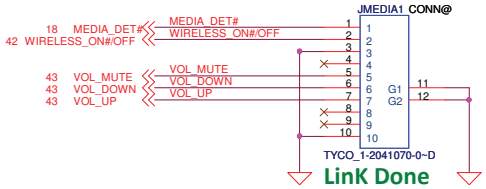




Defult on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

Media Board

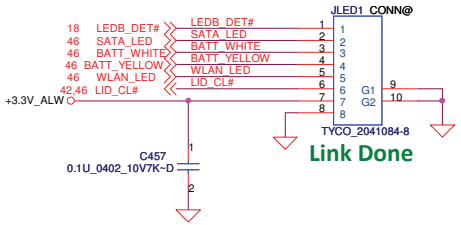
LS-6613P



LinK Done

LED Board with Lid

LS-6612P



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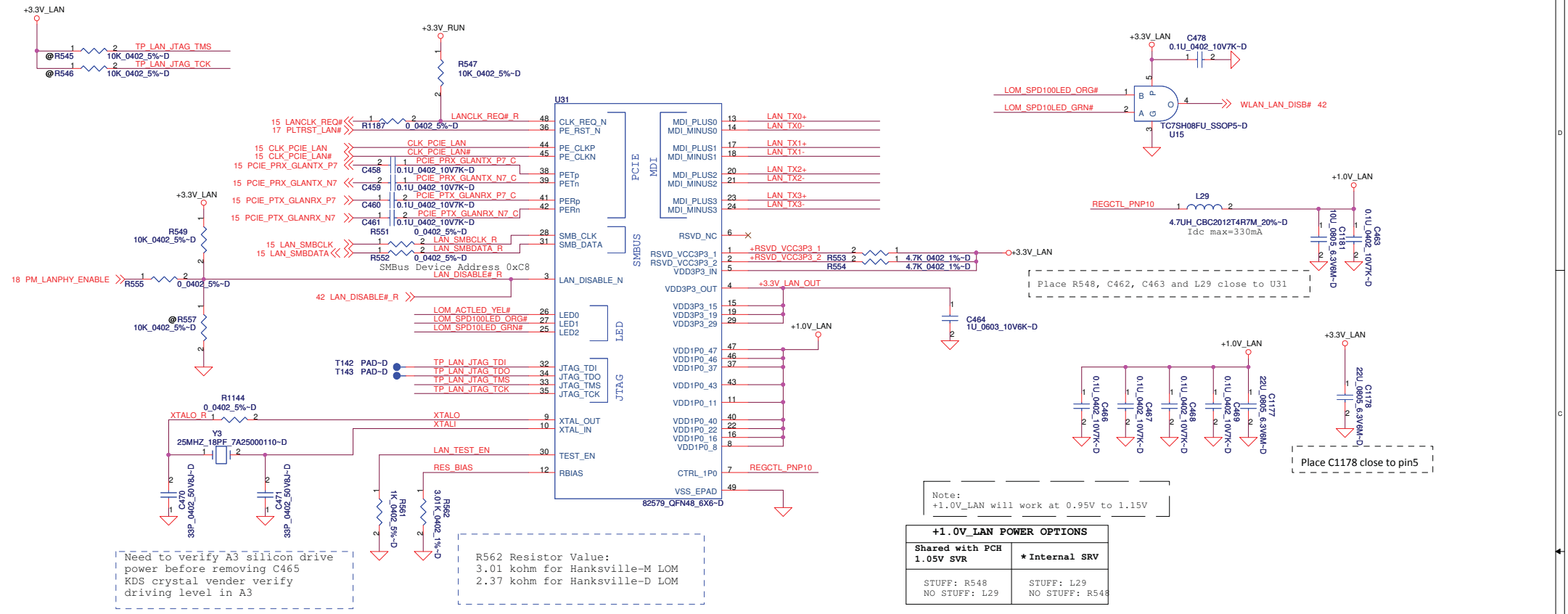
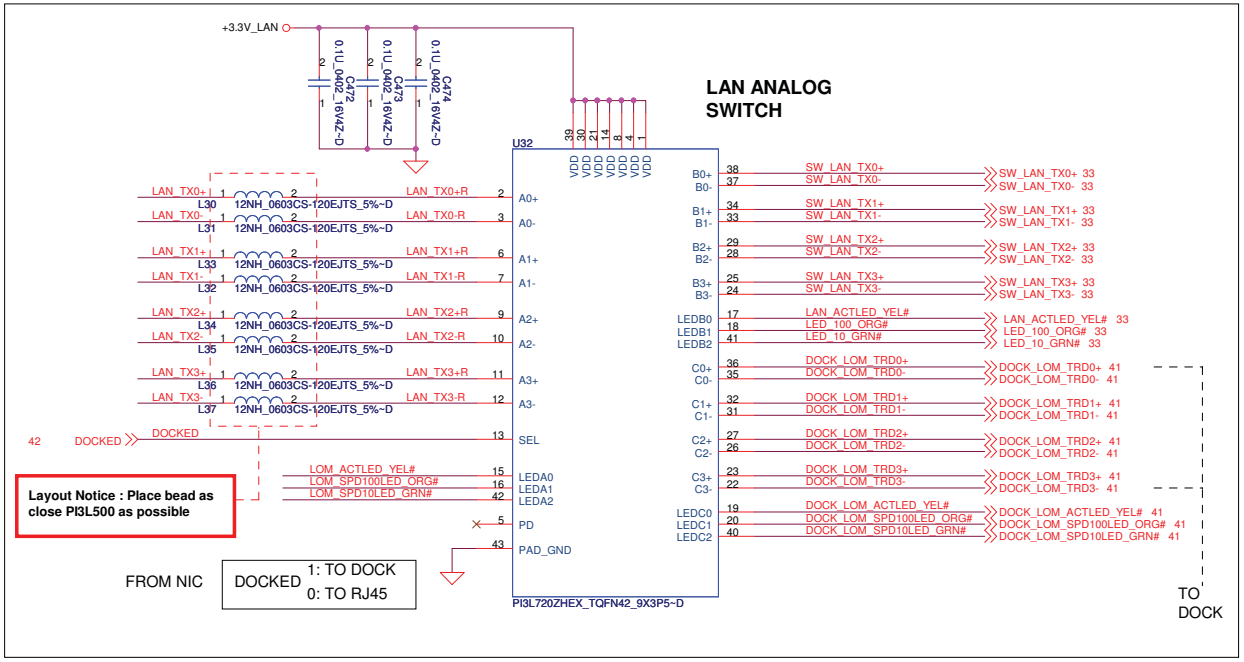
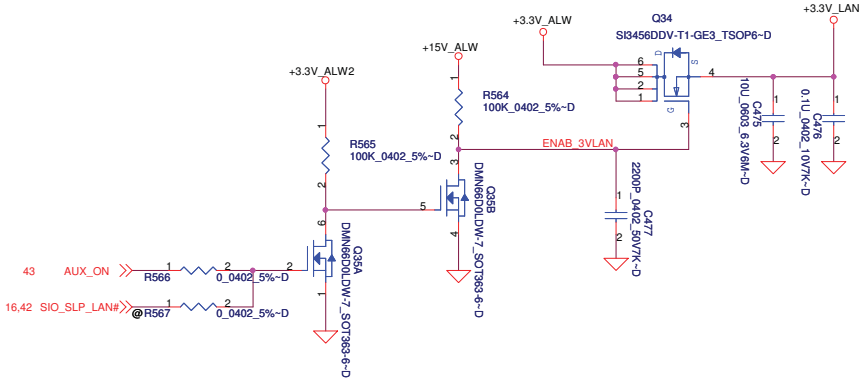
Compal Electronics, Inc.

Title	IO/Sniffer/LID	
Size	Document Number LA-6611P	Rev 0.3
Date: Wednesday, January 26, 2011	Sheet 31 of 64	



+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548





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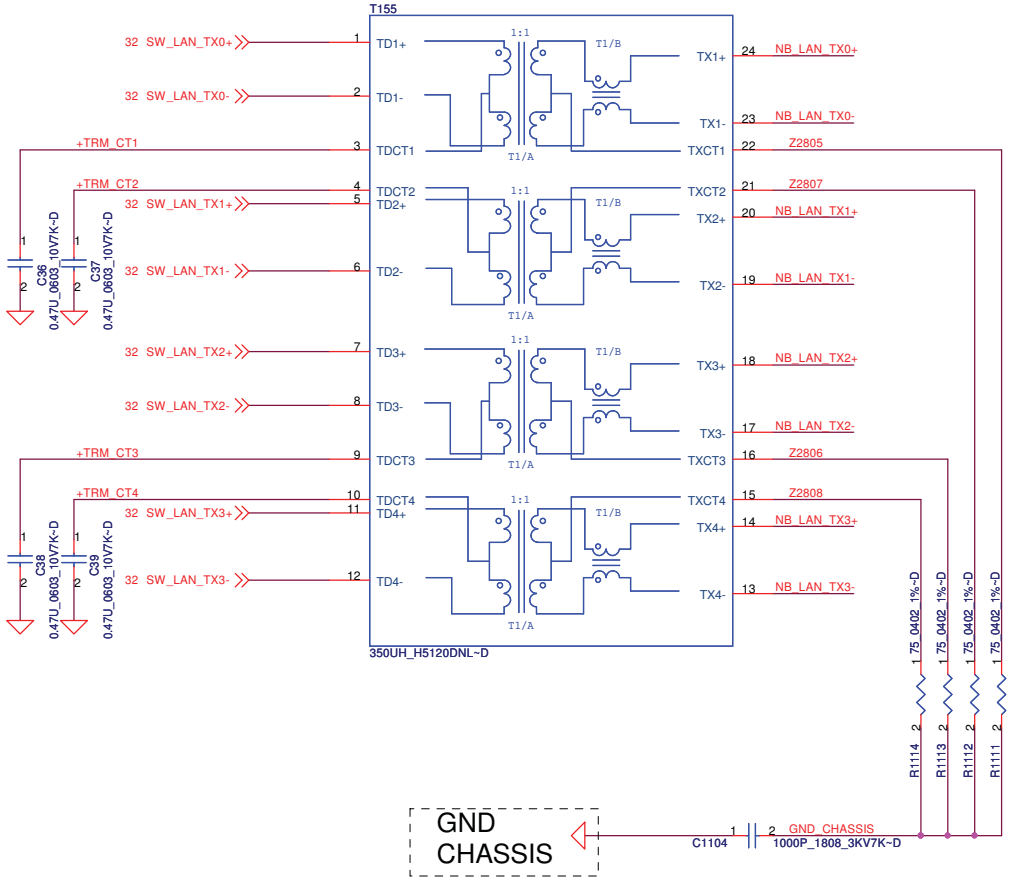
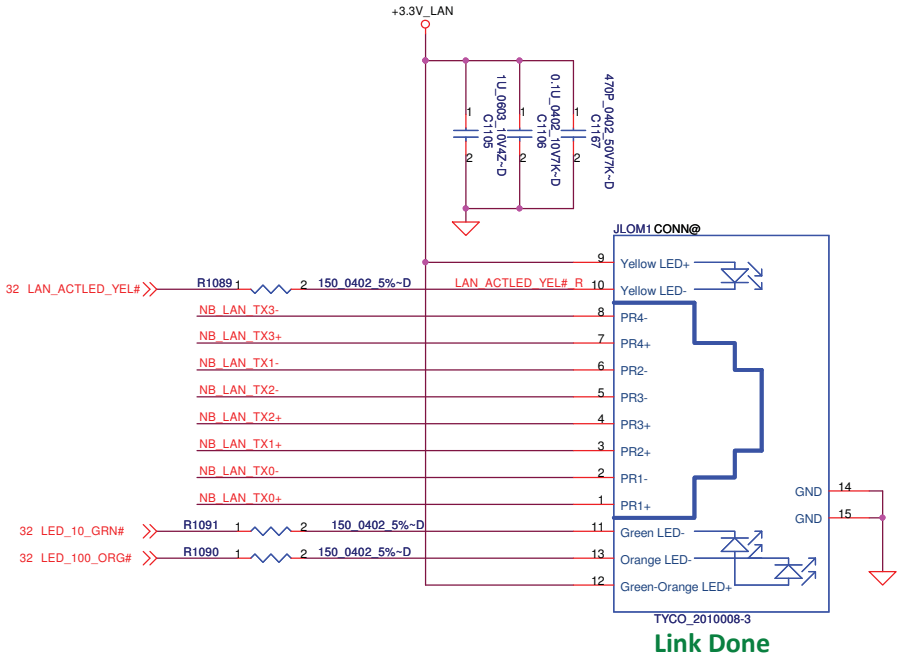
Compal Electronics, Inc.	
Title	Intel 82579 (Hanksville) / LAN SW
Size	Document Number: LA-6611P
Rev	0.3
Date: Wednesday, January 26, 2011	Sheet 32 of 64





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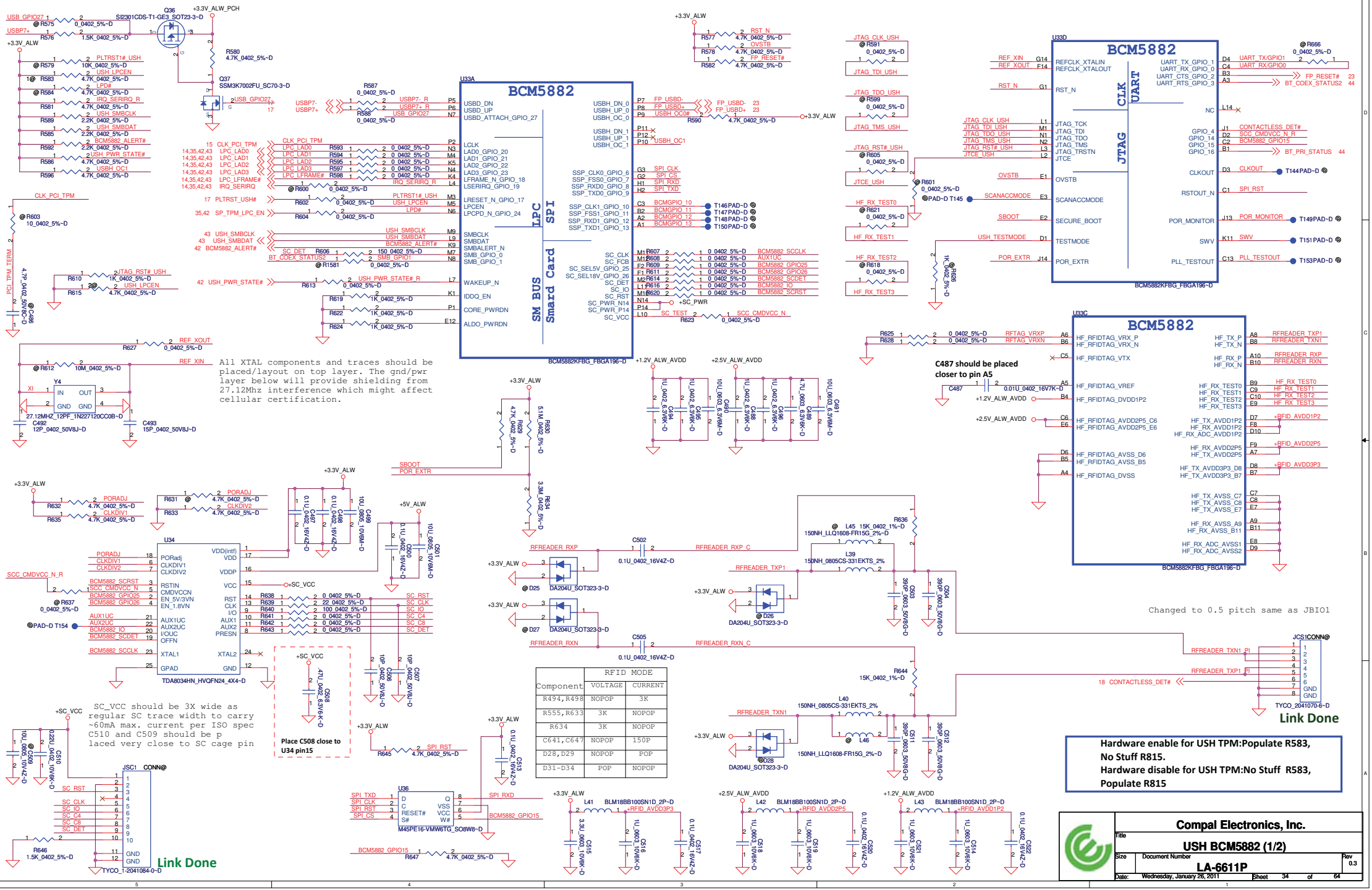
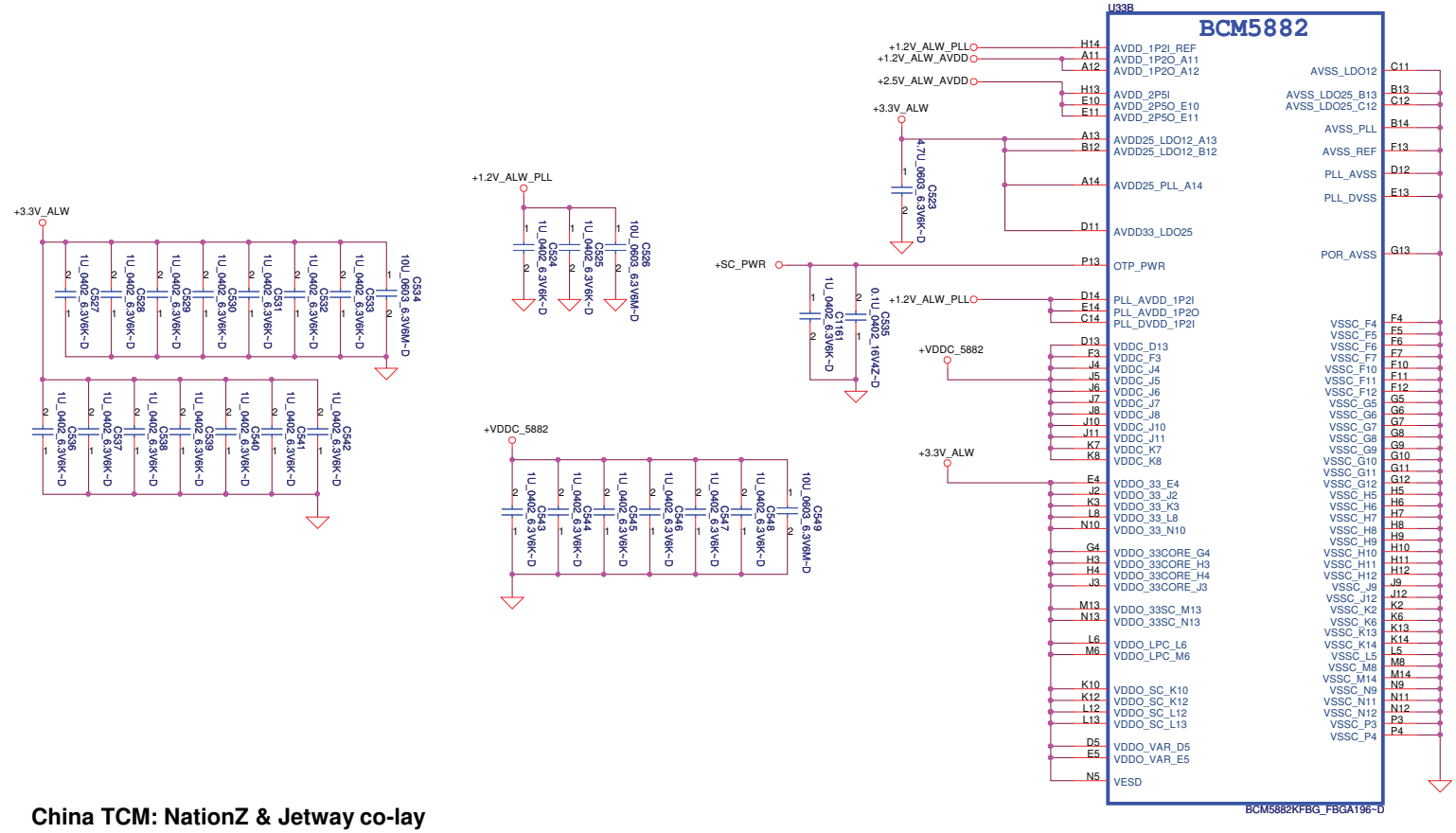
Compal Electronics, Inc.

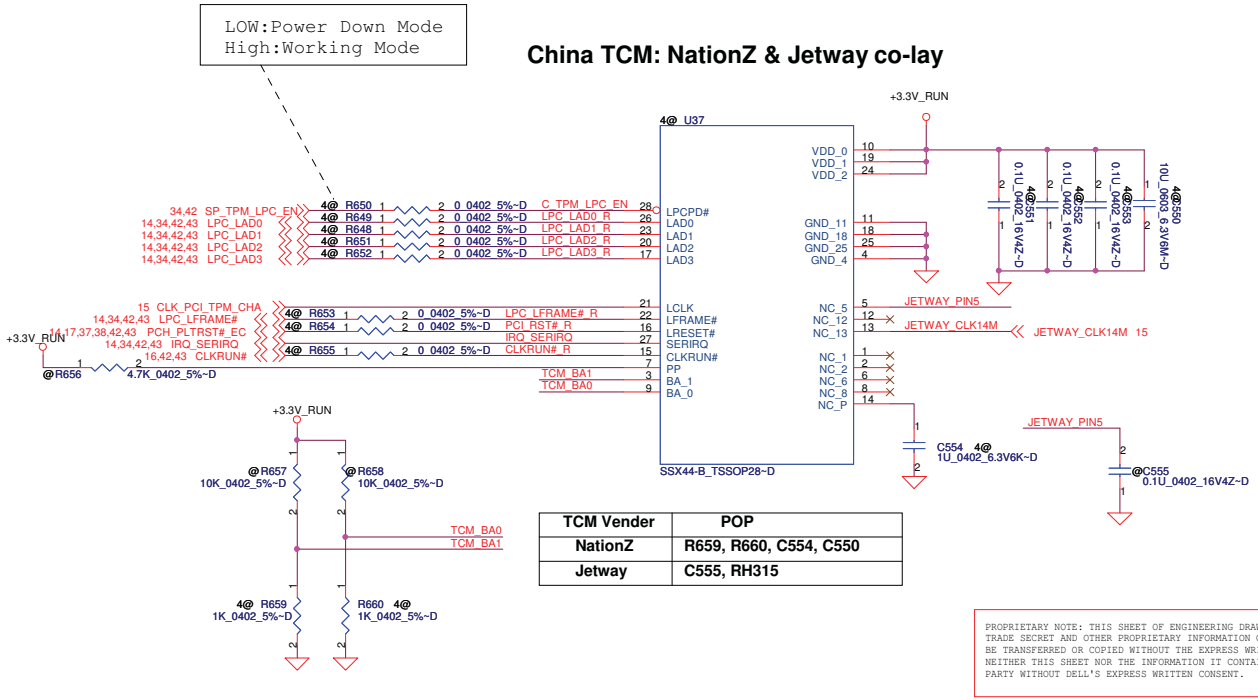
Title: RJ45

Size: | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 33 of 64


BCM5882
BCM5882KFBG_FBGA196~D
All XTAL components and traces should be placed/layout on top layer. The gnd/pwr layer below will provide shielding from 27.12Mhz interference which might affect cellular certification.
C487 should be placed closer to pin A5
Changed to 0.5 pitch same as JBIO1
SC_VCC should be 3X wide as regular SC trace width to carry ~60mA max. current per ISO spec C510 and C509 should be p laced very close to SC cage pin
Place C508 close to U34 pin15
Link Done
Link Done
Hardware enable for USH TPM:Populate R583, No Stuff R815.
Hardware disable for USH TPM:No Stuff R583, Populate R815
TDA8034HN_HVQFN24_4X4~D
M45PE16-VMW6TG_SO8W8~D
TYCO_1-2041084-0~D
TYCO_2041070-6~D
RFID MODE
Component
VOLTAGE
CURRENT
R494,R498
NOPOP
3K
R555,R633
3K
NOPOP
R634
3K
NOPOP
C641,C647
NOPOP
150P
D28,D29
NOPOP
POP
D31~D34
POP
NOPOP
Compal Electronics, Inc.
USH BCM5882 (1/2)
LA-6611P
Wednesday, January 26, 2011
34
64
0.3





TCM Vender	POP
NationZ	R659, R660, C554, C550
Jetway	C555, RH315

USH BCM5882 and China TCM Z8H172T Option

PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
USH_LPCEN	PU R583	@	POP	@
	PD R615	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R772	@	@	@
PCH GPIO39 ->TPM_ID1	PU RH268	@	@	POP
	PD RH271	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU RH267	POP	POP	@
	PD RH270	@	@	POP

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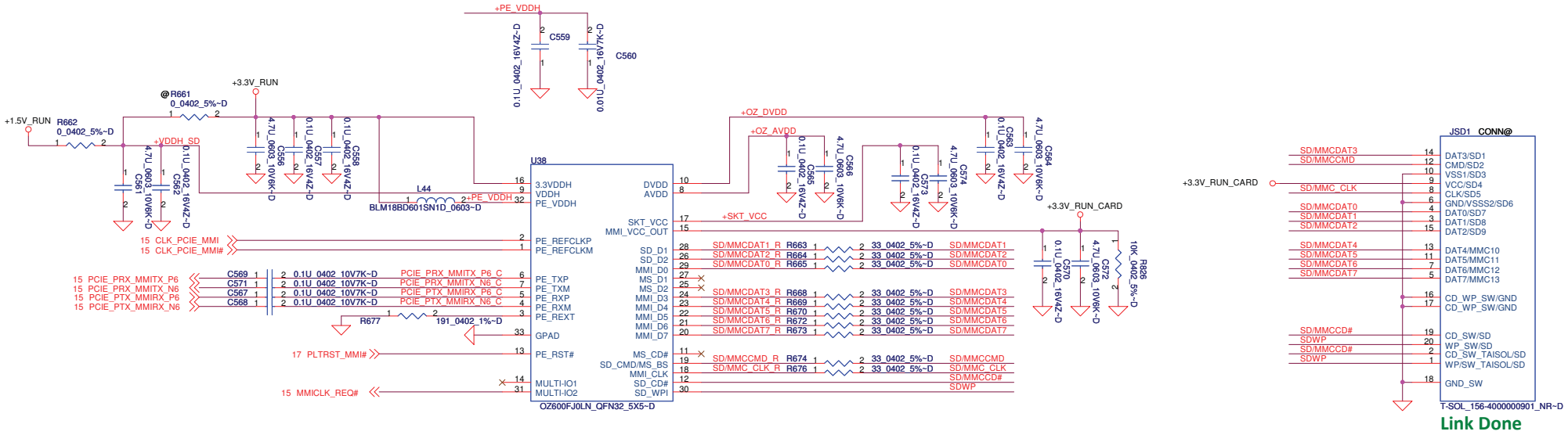
Compal Electronics, Inc.

Title: USH BCM5882 (2/2)

Size: | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 35 of 64



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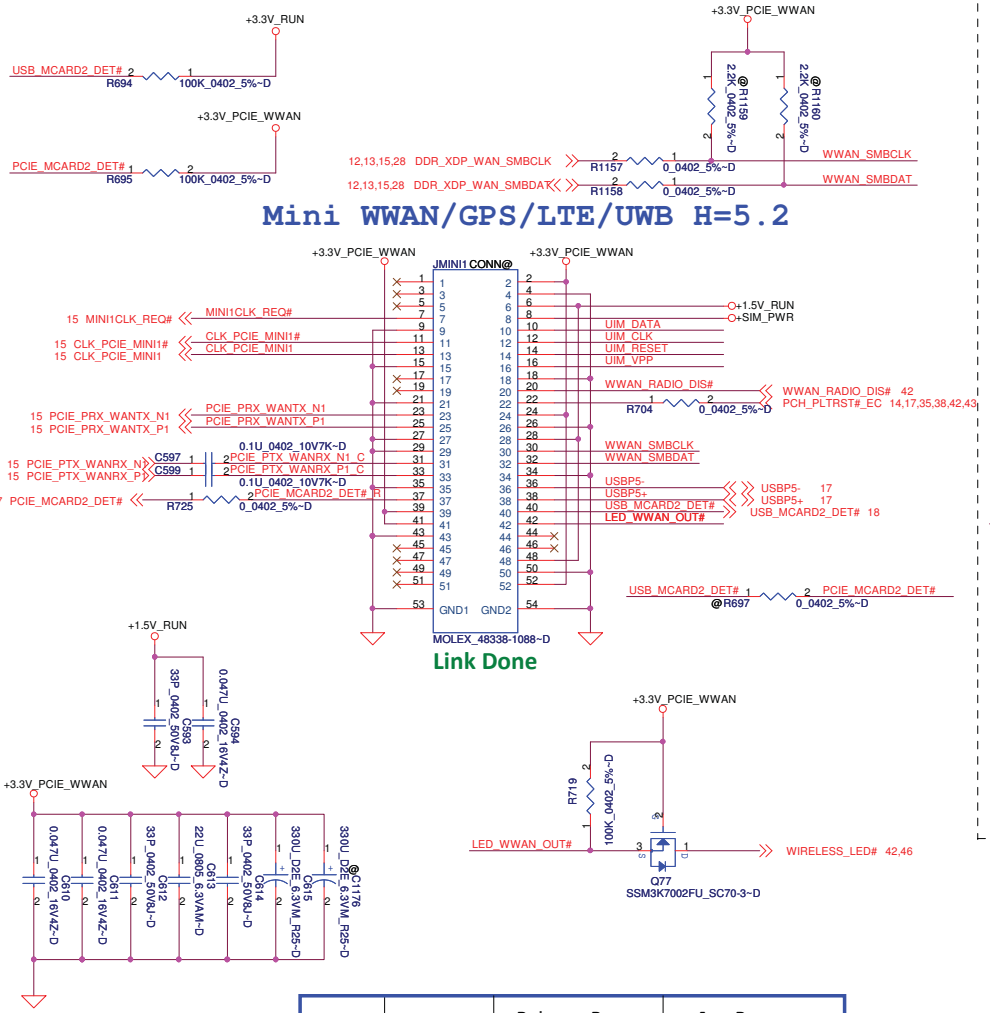
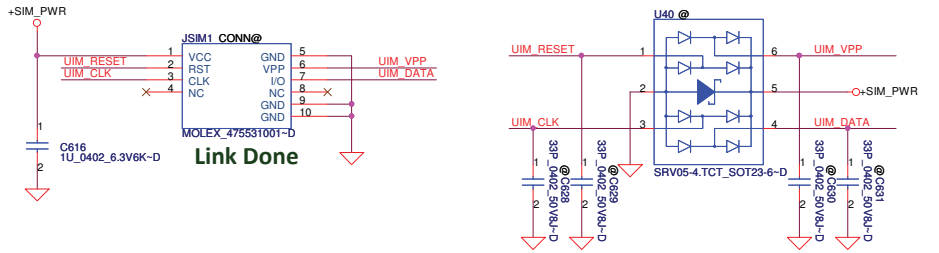
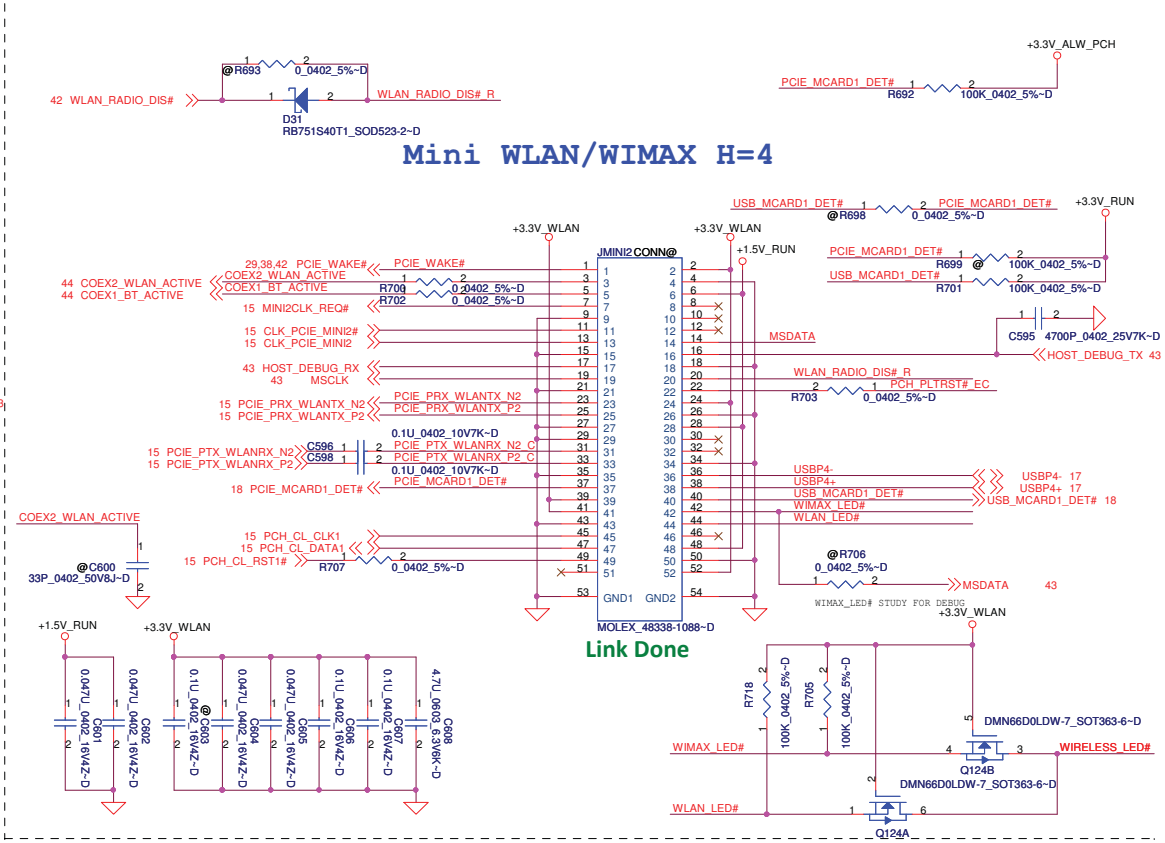
Compal Electronics, Inc.

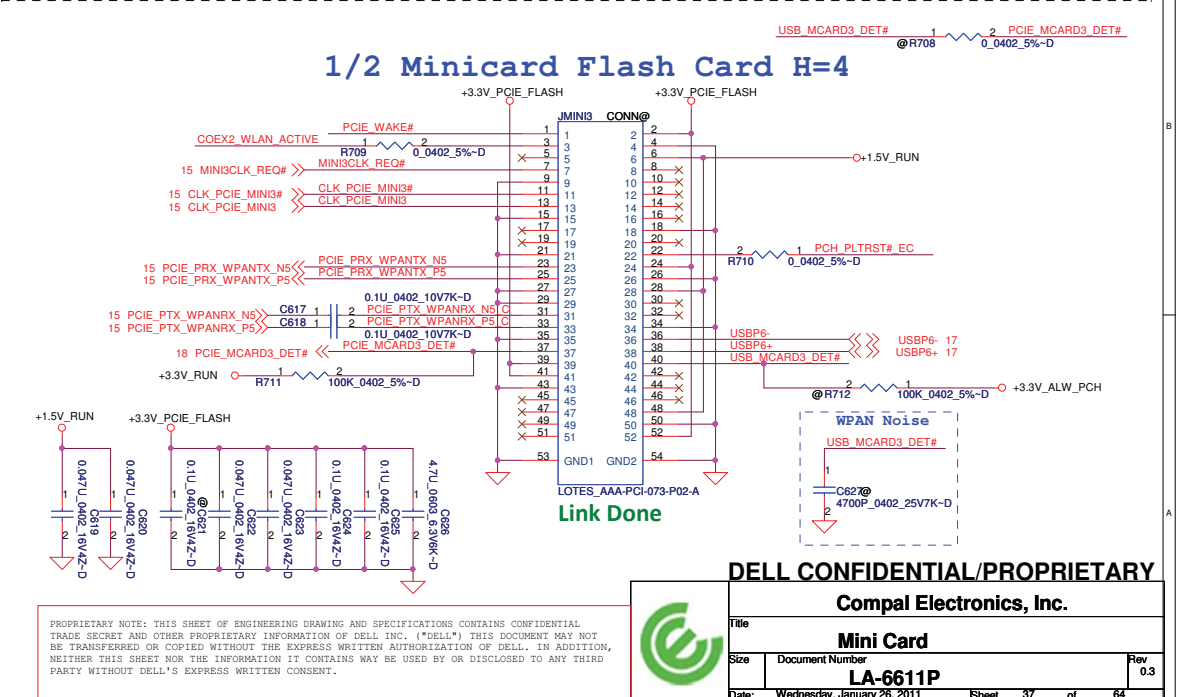
Title	OZ600FJ0	
Size	Document Number LA-6591P	Rev 0.3
Date: Wednesday, January 26, 2011	Sheet 36 of 64	



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA







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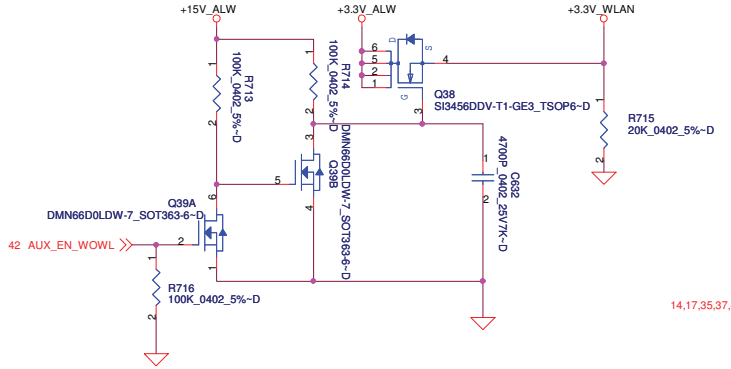
Compal Electronics, Inc.

Title: Mini Card

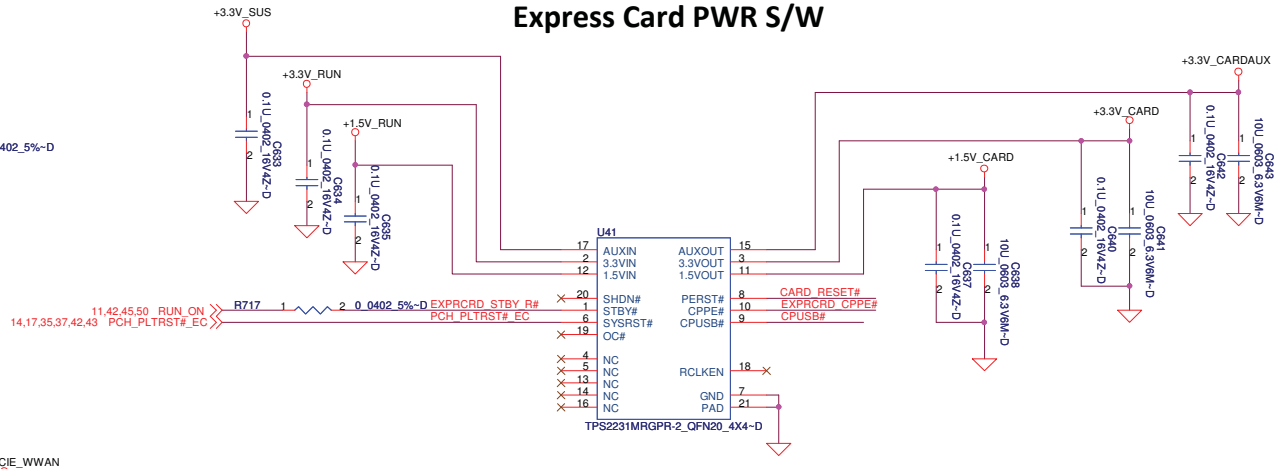
Size | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 37 of 64

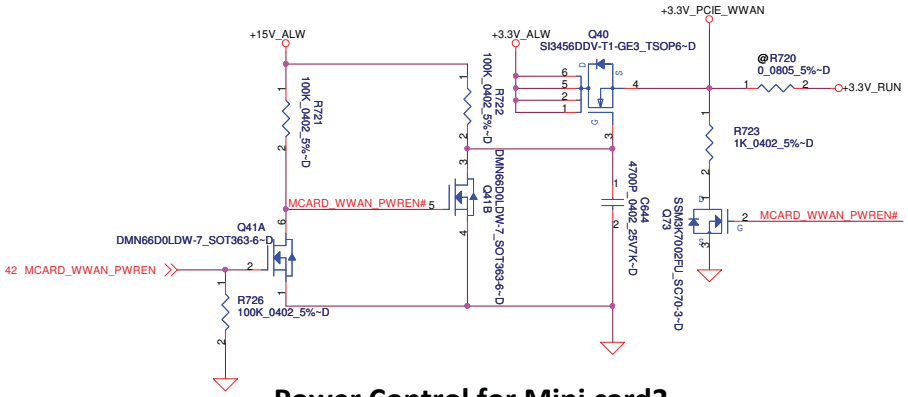
Power Control for Mini card2



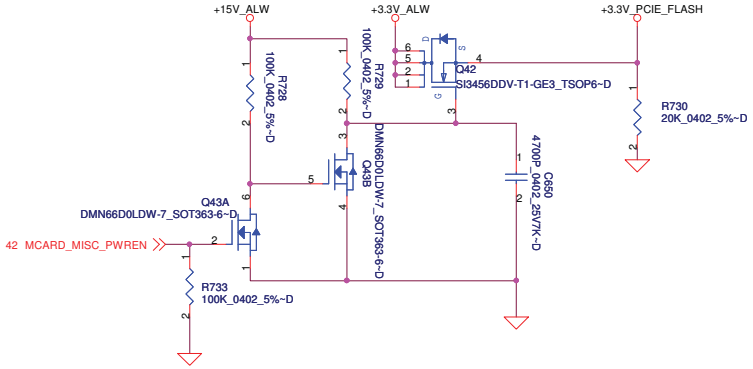
Express Card PWR S/W

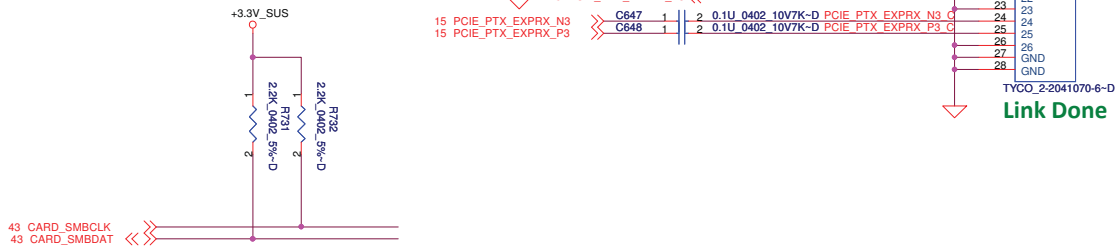


Power Control for Mini card1



Power Control for Mini card3





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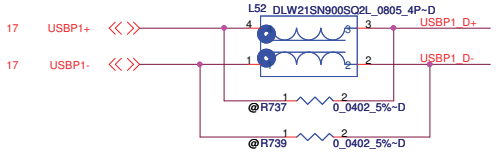
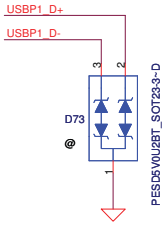
Compal Electronics, Inc.

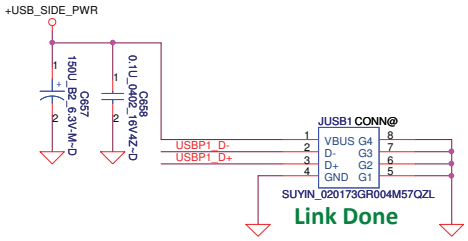
Title: PCIE-SATA SW / PCIE PWR

Size | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 38 of 64







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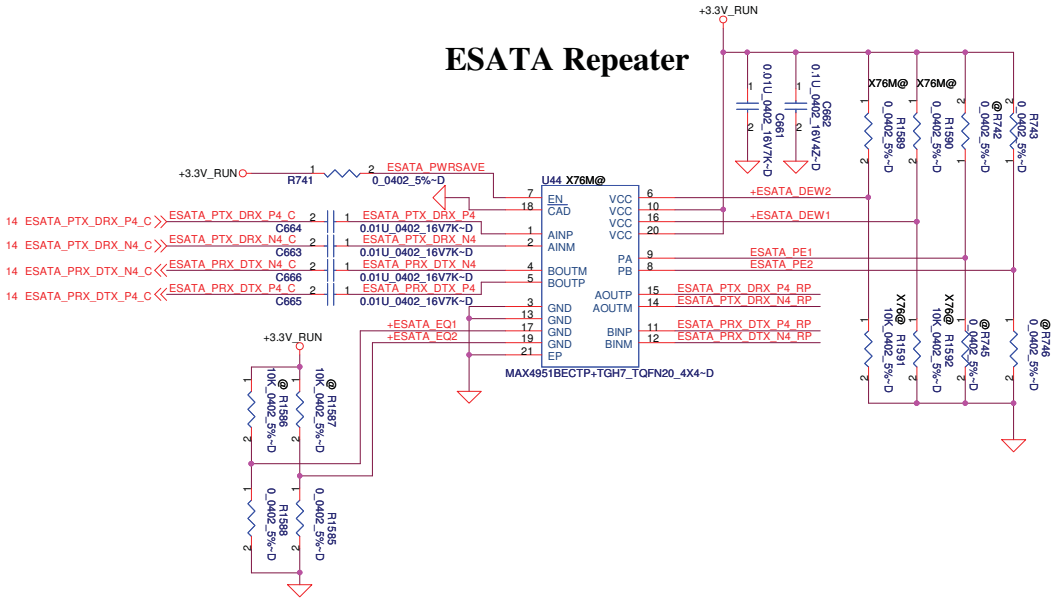
Compal Electronics, Inc.

Title: USB x1

Size | Document Number: LA-6611P | Rev: 0.3

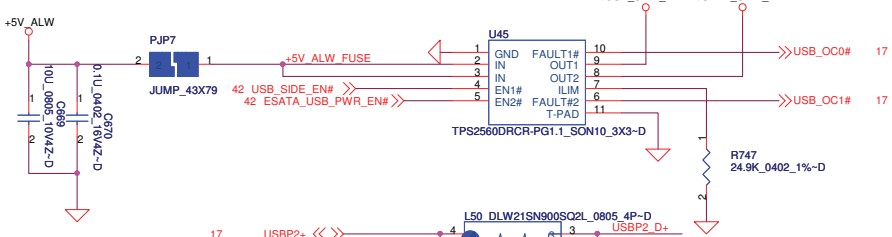
Date: Wednesday, January 26, 2011 | Sheet 39 of 64

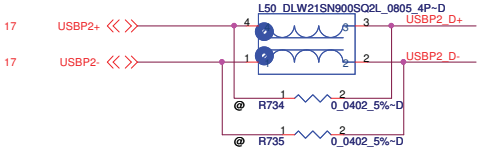
ESATA Repeater

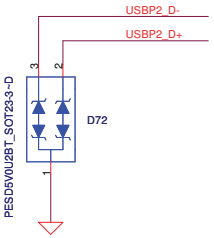


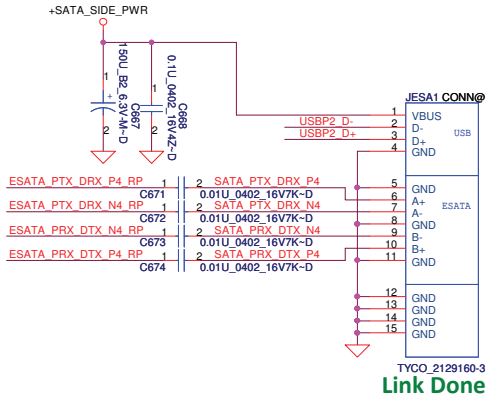
SA00003LH1L SA00003ZX0L

	MAXIM	TI
R1589 R1590	pop	depop
R1591 R1592	depop	pop









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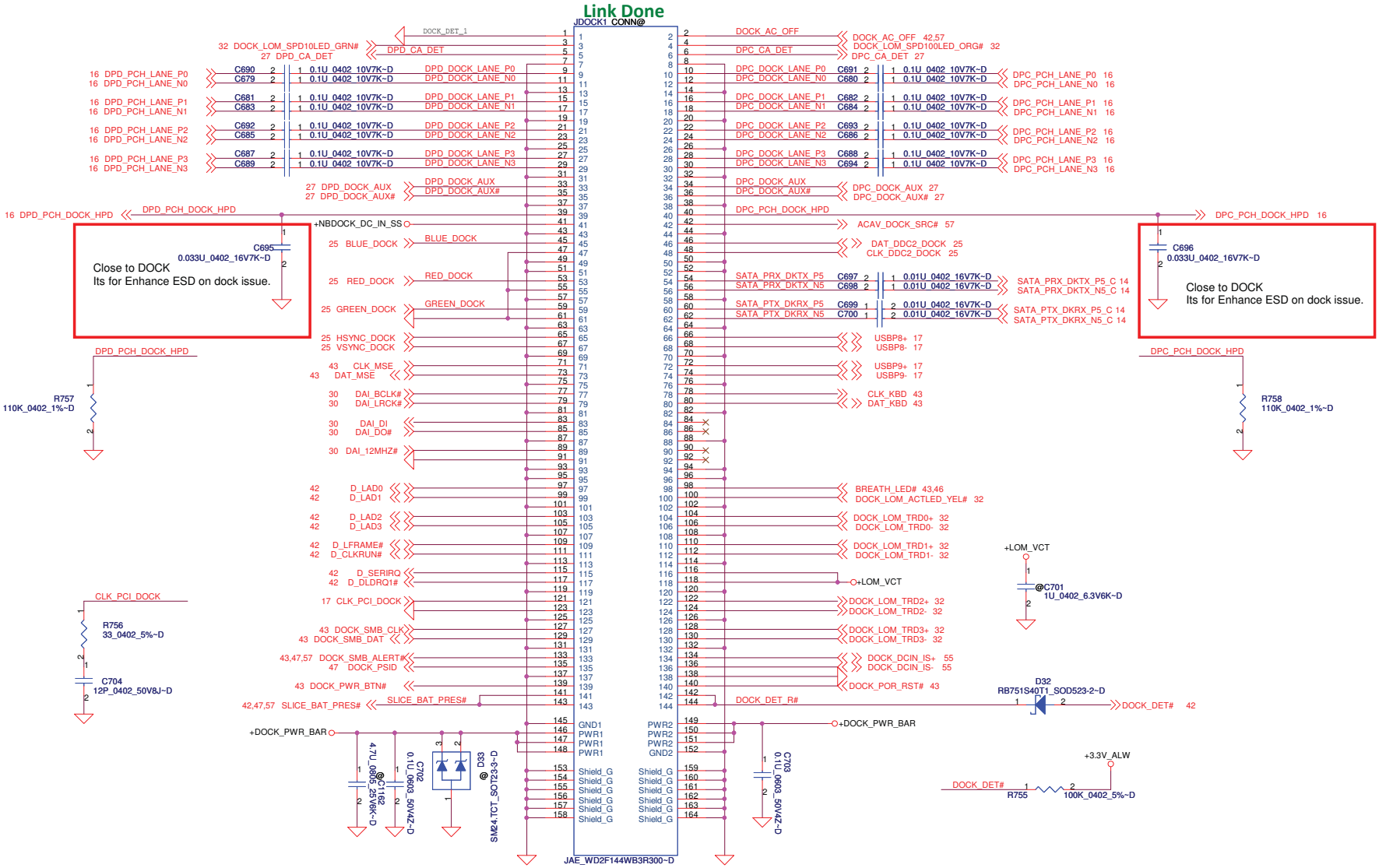
Compal Electronics, Inc.

Title: USB/ESATA/IO

Size | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 40 of 64



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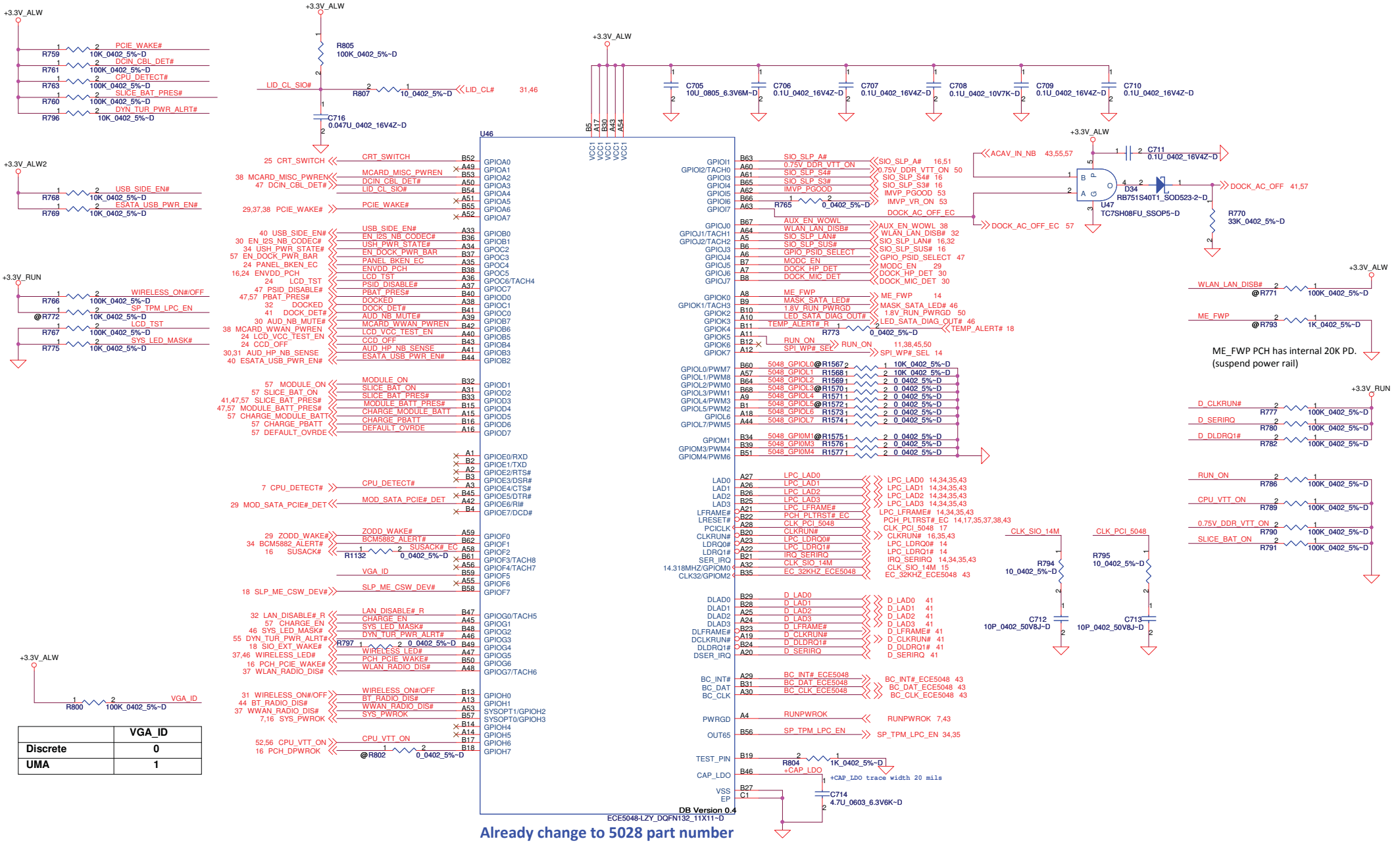
Compal Electronics, Inc.

Title: DOCKING CONN

Size | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 41 of 64



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Compal Electronics, Inc.

Title: ECE5048

Size | Document Number: LA-6611P | Rev: 0.3

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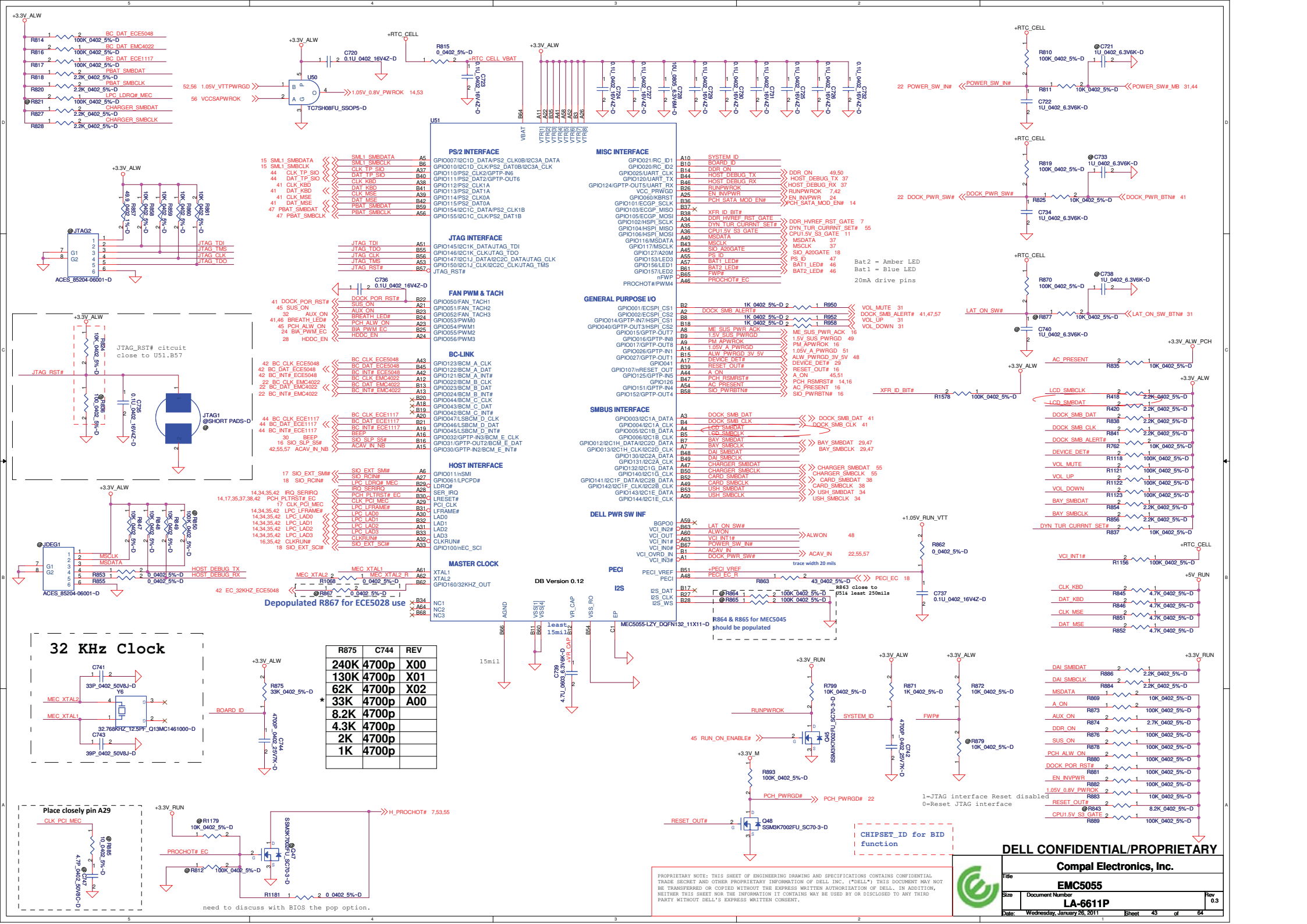

R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

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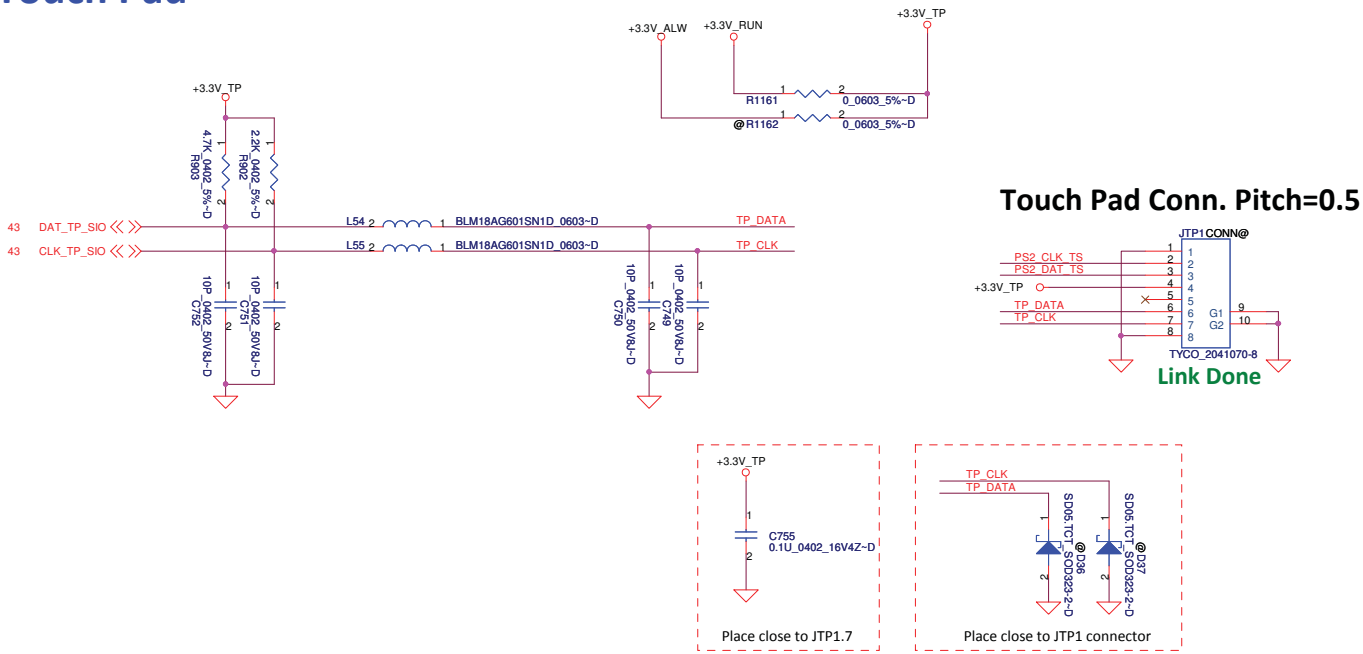
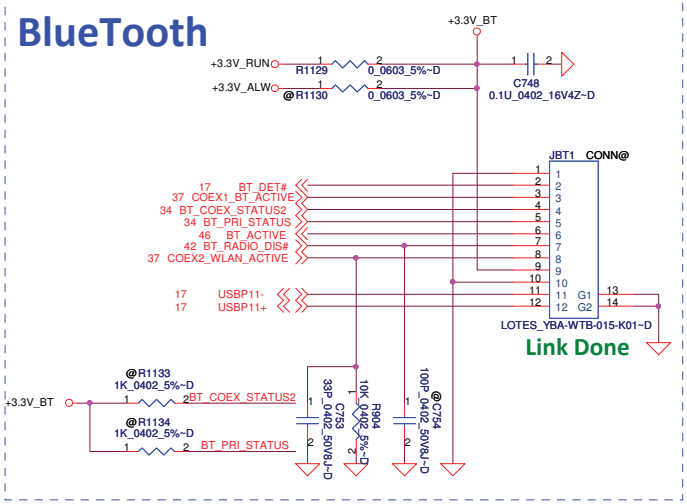
Touch Pad



Touch Pad Conn. Pitch=0.5

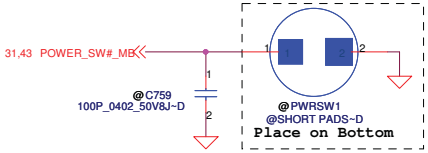
Link Done

BlueTooth



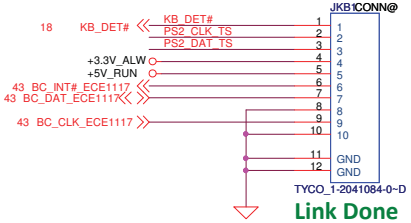
Link Done

Power Switch for debug



Keyboard

KB Conn. Pitch=1.0mm



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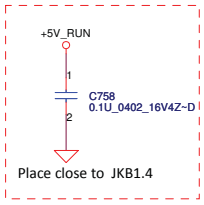

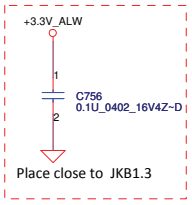

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Compal Electronics, Inc.	
Title	Int KB/Touch PAD/BT
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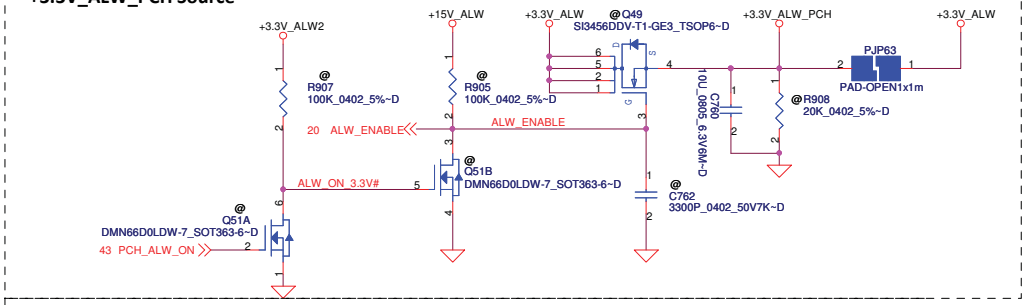
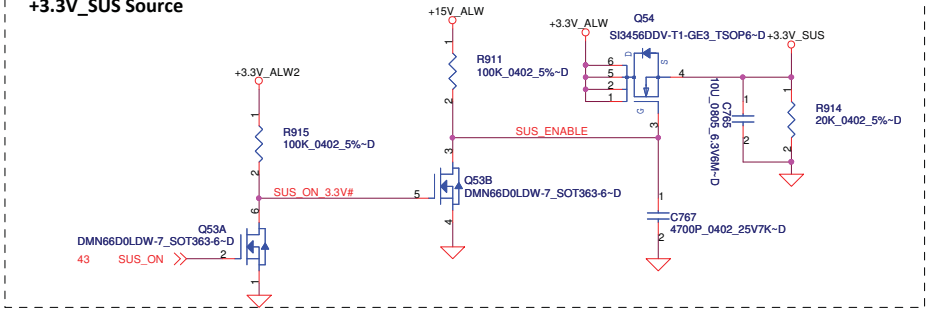
DC/DC Interface

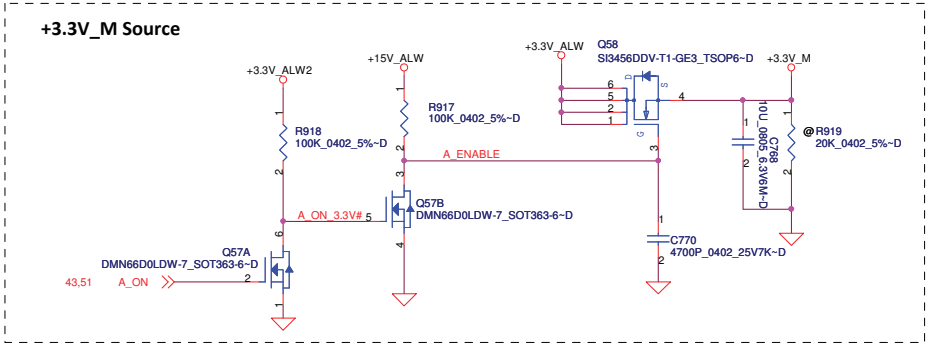
+3.3V_ALW_PCH Source



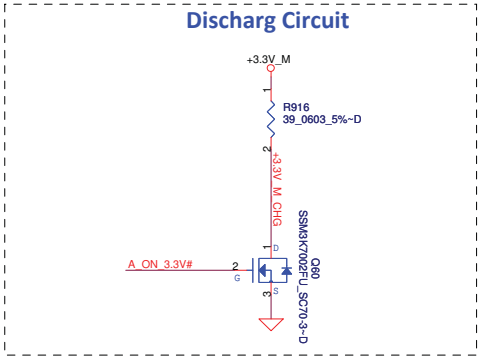
+3.3V_SUS Source



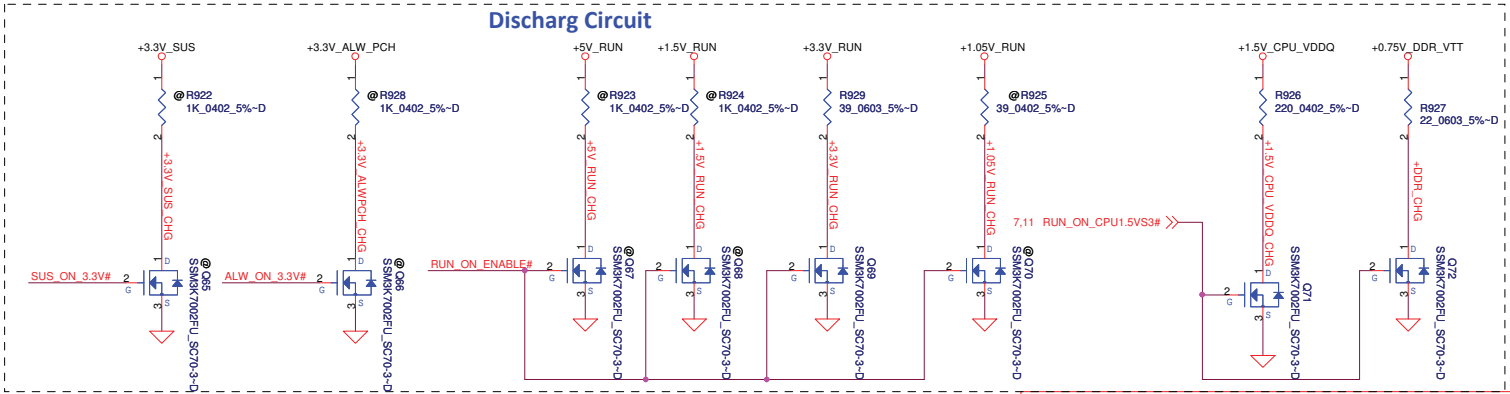
+3.3V_M Source



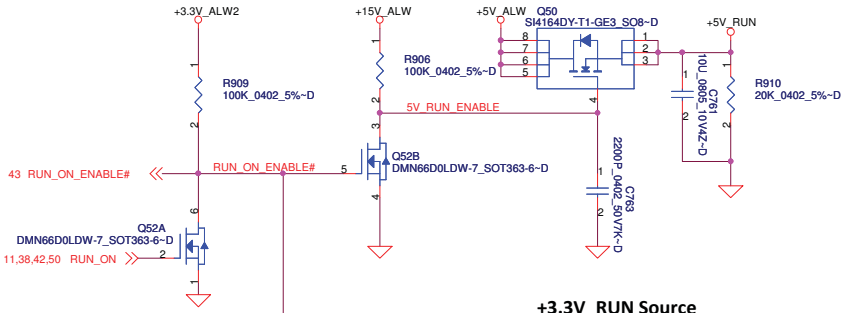
Discharg Circuit



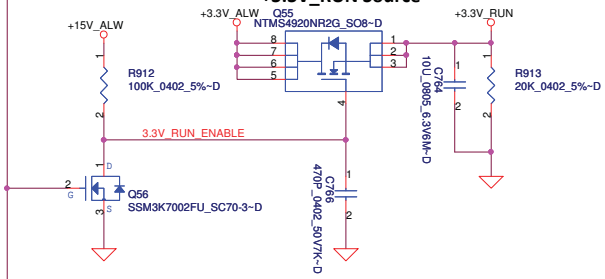
Discharg Circuit



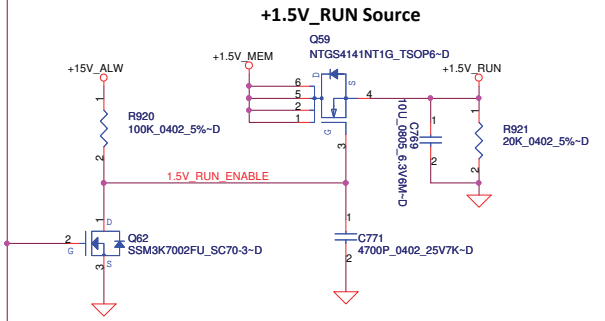
+5V_RUN Source



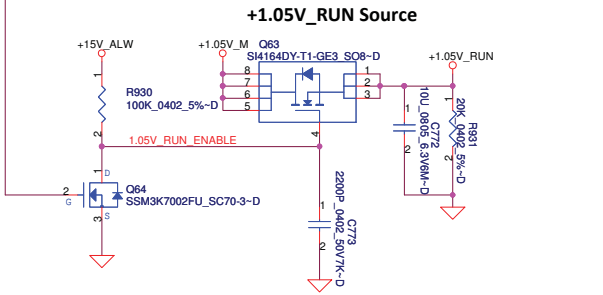
+3.3V_RUN Source



+1.5V_RUN Source



+1.05V_RUN Source



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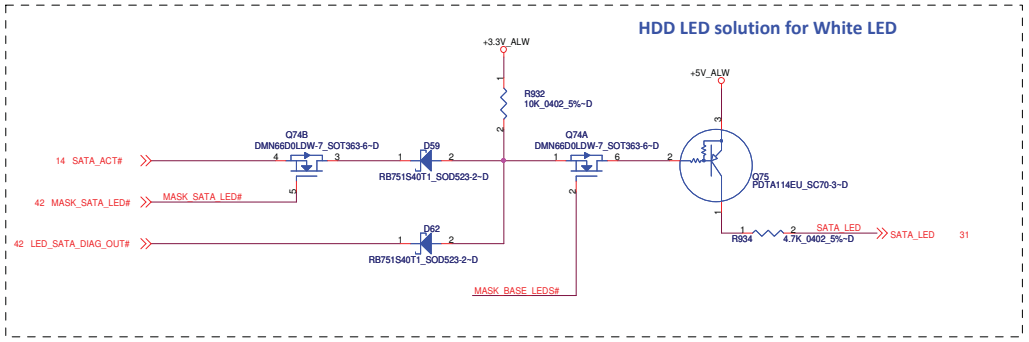
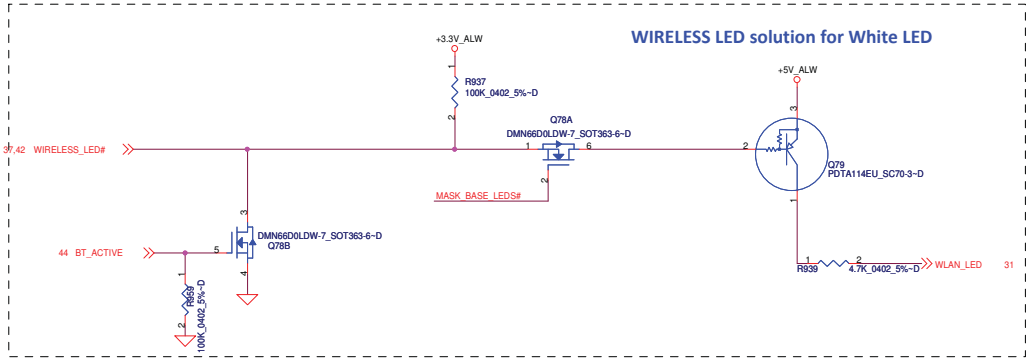
Compal Electronics, Inc.

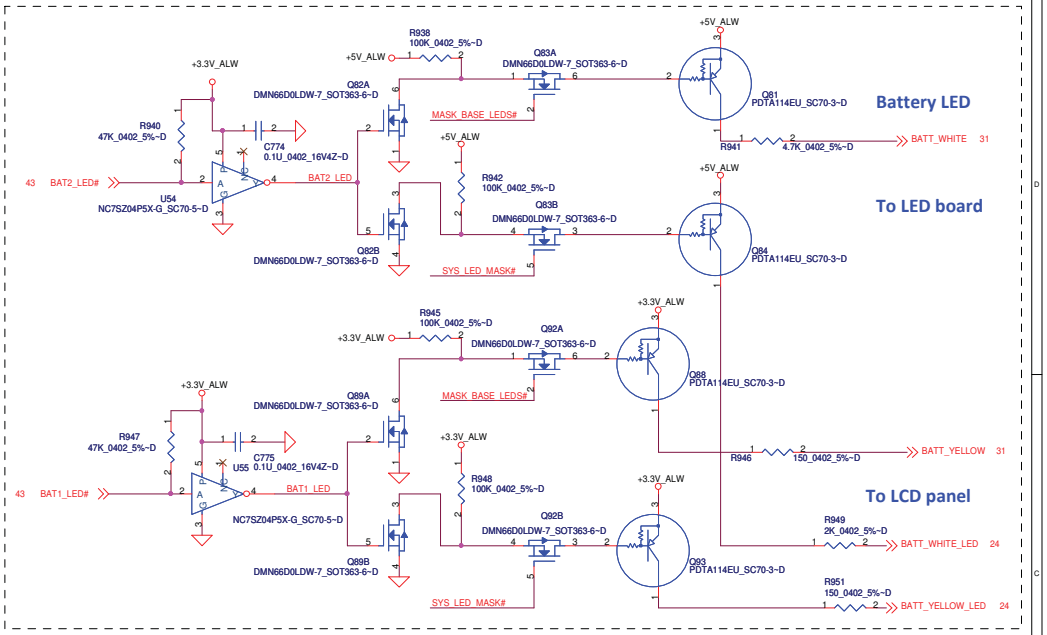
Title: POWER CONTROL

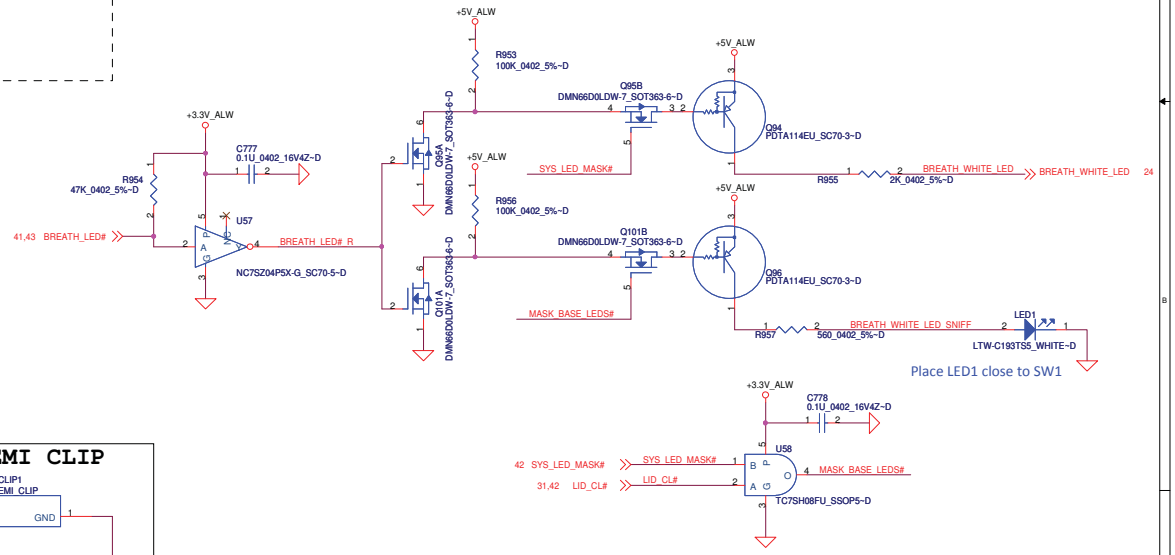
Size | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 45 of 64

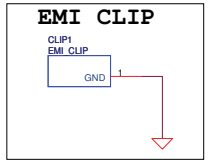


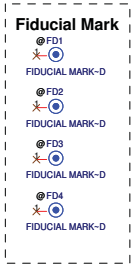


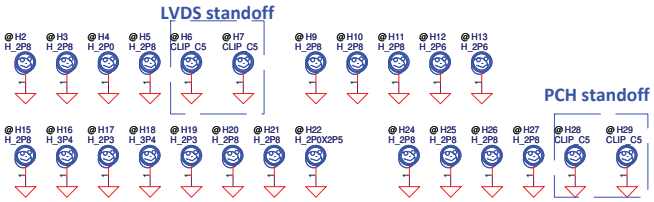




LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1







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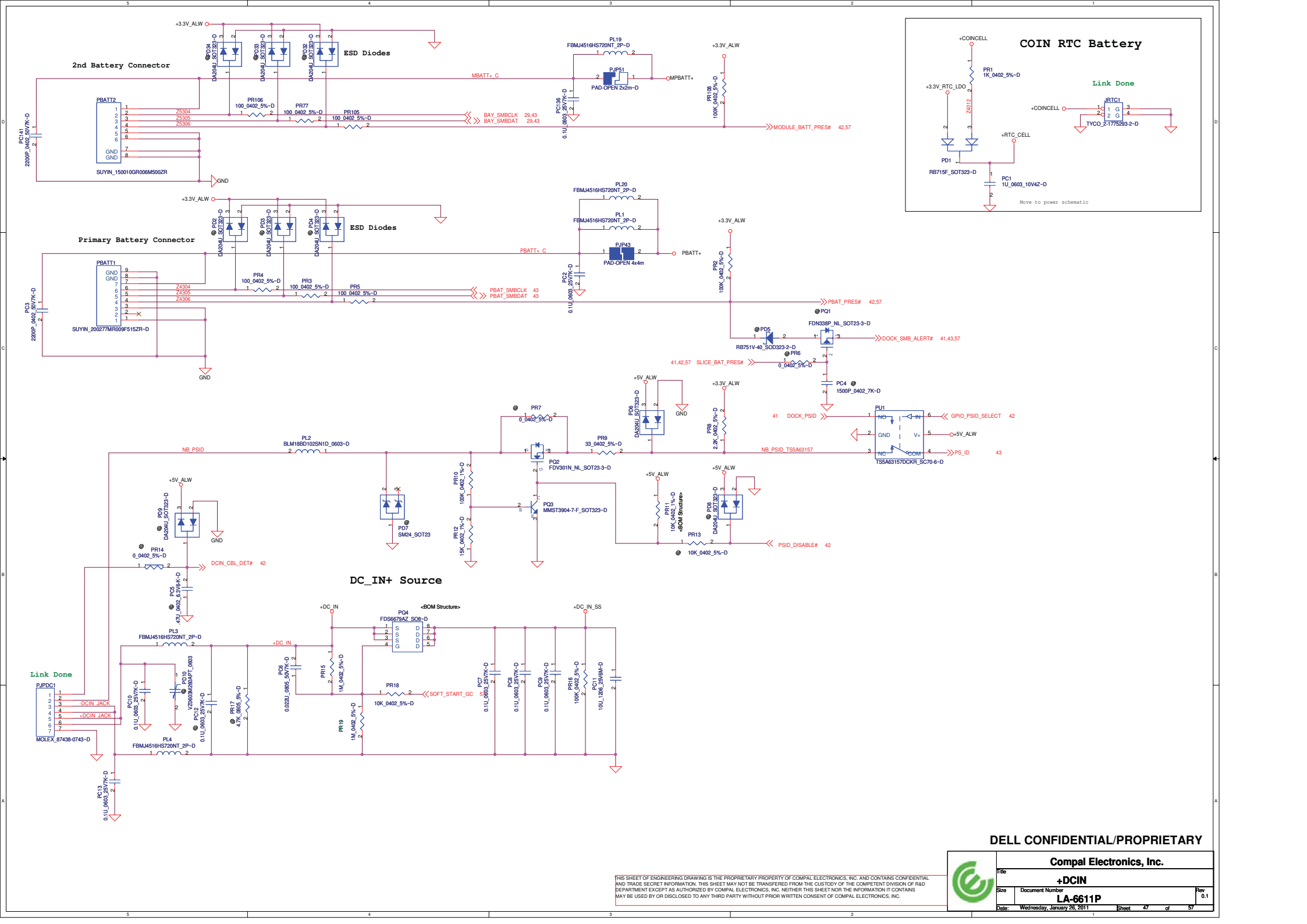
Compal Electronics, Inc.

Title: PAD & ME & LED

Size: | Document Number: LA-6611P | Rev: 0.3

Date: Wednesday, January 26, 2011 | Sheet 46 of 64



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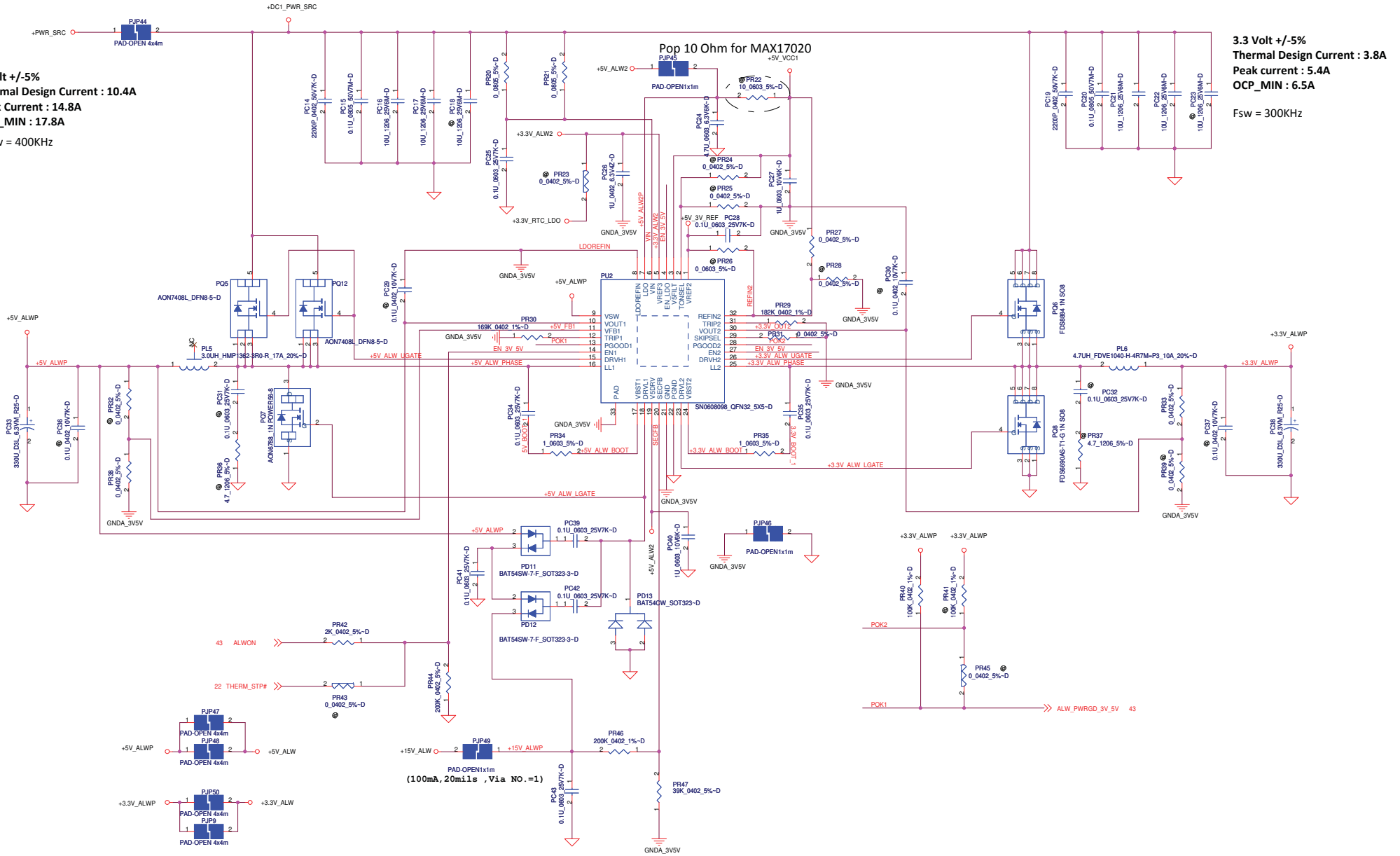
Compal Electronics, Inc.		
Title	+DCIN	
Size	Document Number LA-6611P	Rev 0.1
Date: Wednesday, January 26, 2011	Sheet 47 of 57	

+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/ +3.3V_RTC_LDO



		PU2	PR22
Main	X7629631L90	SN0608098	un-pop
2nd	X7629631L91	MAX8878	10_ohm

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Compal Electronics, Inc.

Title: DC/DC +3V/ +5V

Size: | Document Number: LA-6611P | Rev: 0.1

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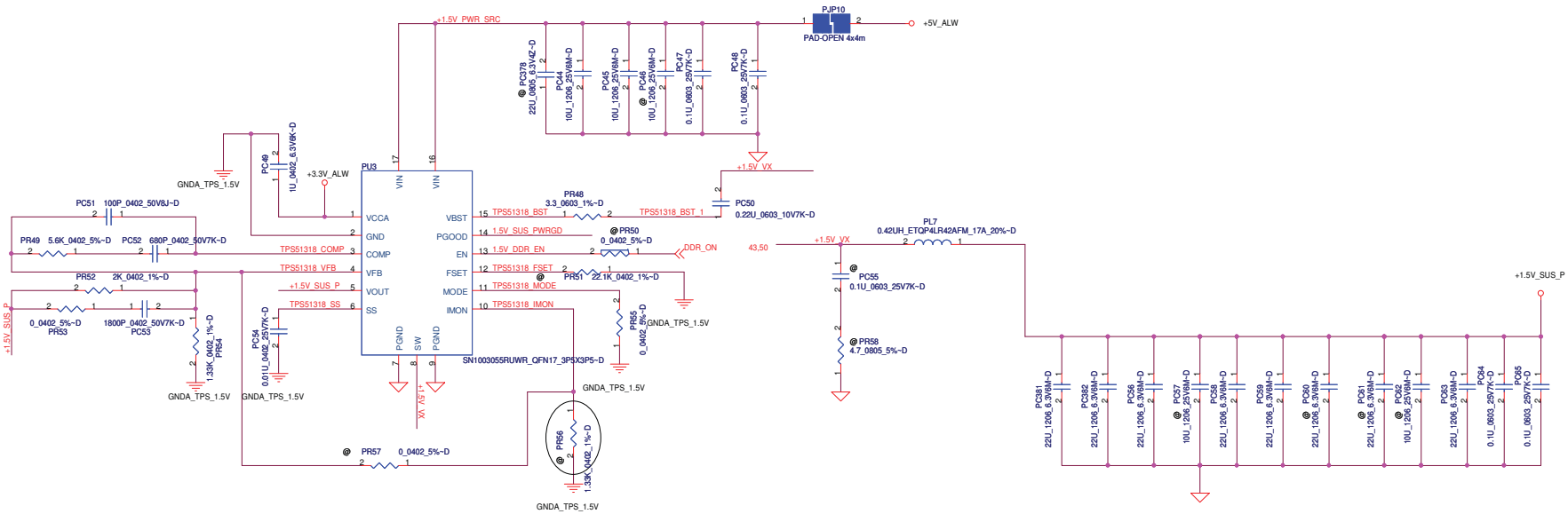
+1.5V_SUS_P(TPS51318)

1.5 Volt +/-5%
Thermal Design Current: 9.8A
Peak current: 13.9
OCP_MIN:16.7A



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Compal Electronics, Inc.

Title: +1.5V_MEM

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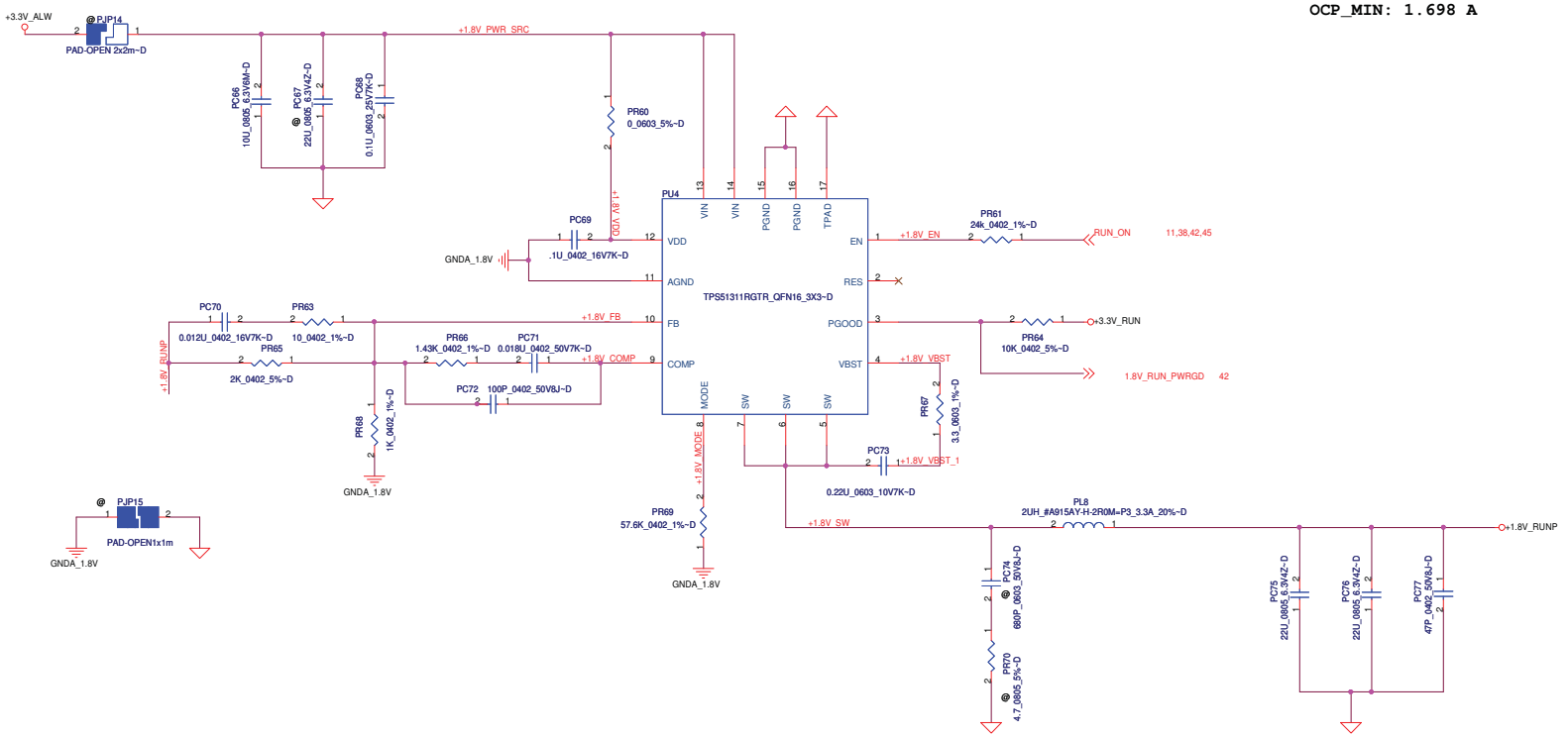
+1.8V_RUNP

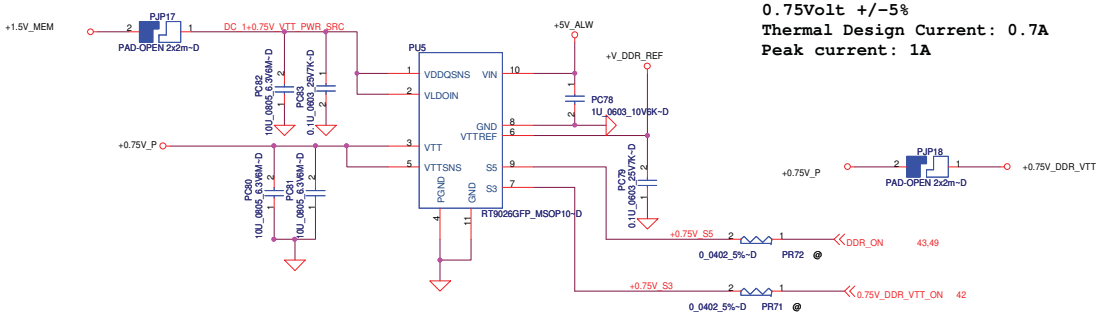
1.8 Volt +/-5%
Thermal Design Current: 0.99 A
Peak current: 1.415 A
OCP_MIN: 1.698 A



+0.75V_DDR_VTT

DDR3 Termination

0.75Volt +/-5%
Thermal Design Current: 0.7A
Peak current: 1A



VOUT=1.8V
L=3.3uF
Fsw=290KHz
D=0.092
Input Ripple Current=TDC*(D*(1-D))^0.5=0.884A
Output Ripple Current=1.707A
Output Ripple Voltage=1.707*15m=20.5mV

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Compal Electronics, Inc.

Title	+0.75V_DDR_VT/+1.8V_RUN	
Size	Document Number: LA-6611P	Rev: 0.1
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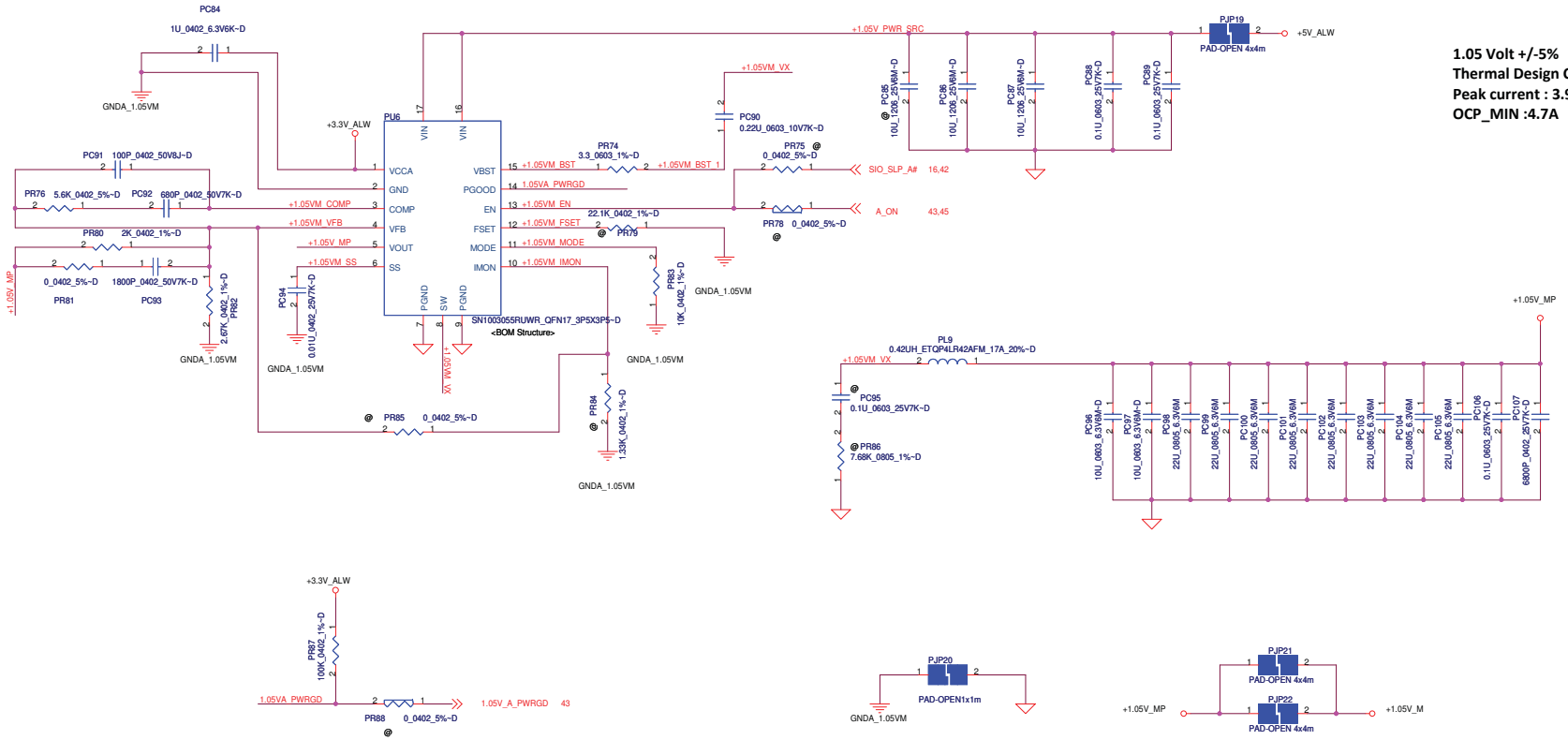
+1.05V_M



1.05 Volt +/-5%
Thermal Design Current : 2.7A
Peak current : 3.9A
OCP_MIN :4.7A

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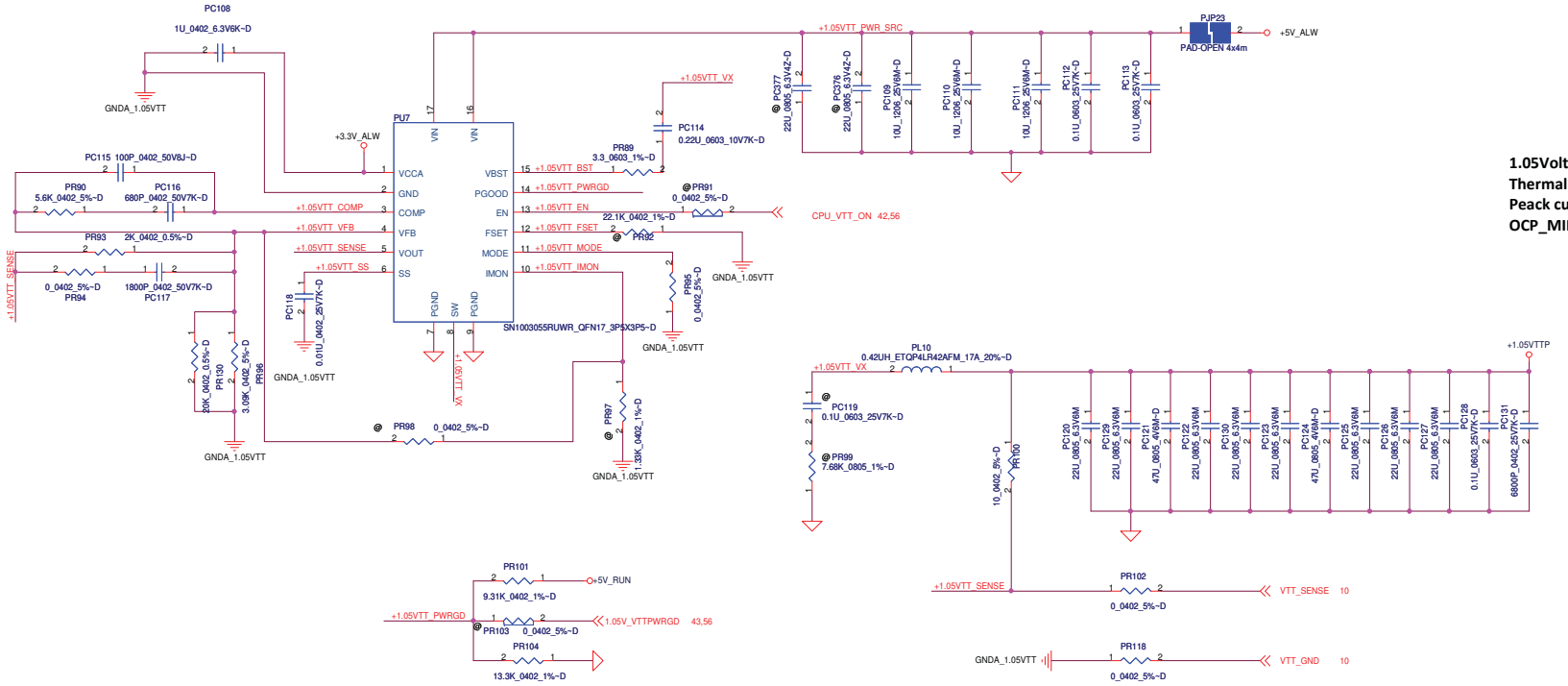
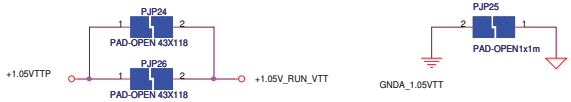
Compal Electronics, Inc.		
Title: +1.05V_M		
Size	Document Number: LA-6611P	Rev: 0.1
Date: Wednesday, January 26, 2011	Sheet 51 of 57	

+1.05VTT





1.05Volt +/-5%
Thermal Design Current : 9.2A
Peack current : 13.1A
OCP_MIN : 15.8A

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Compal Electronics, Inc.

Title	ISL95870A +1.05V_RUN_VTT	
Size	Document Number: LA-6611P	Rev: 0.1
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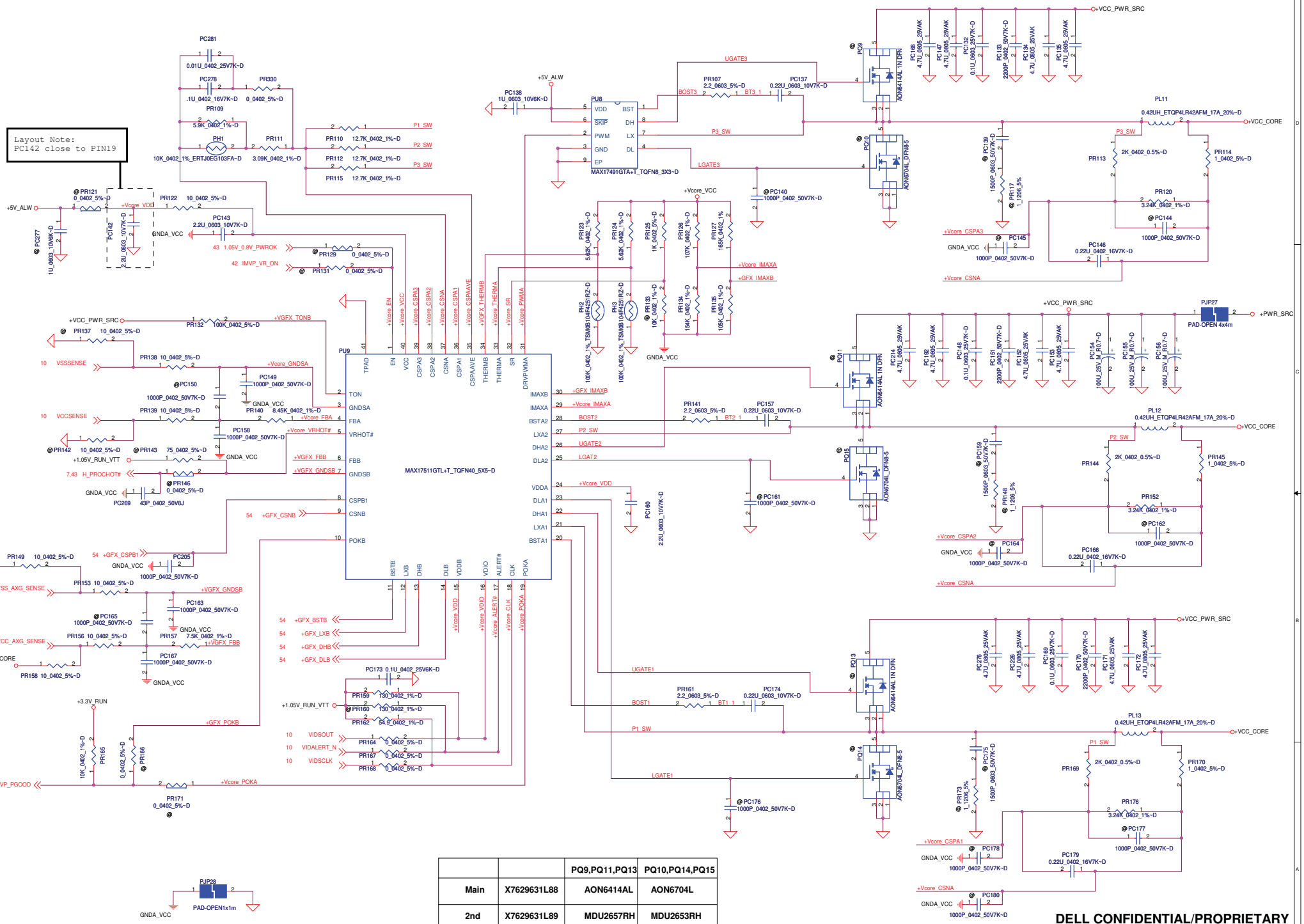

		PQ9,PQ11,PQ13	PQ10,PQ14,PQ15
Main	X7629631L88	AON6414AL	AON6704L
2nd	X7629631L89	MDU2657RH	MDU2653RH

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Compal Electronics, Inc.

Title: Vcore

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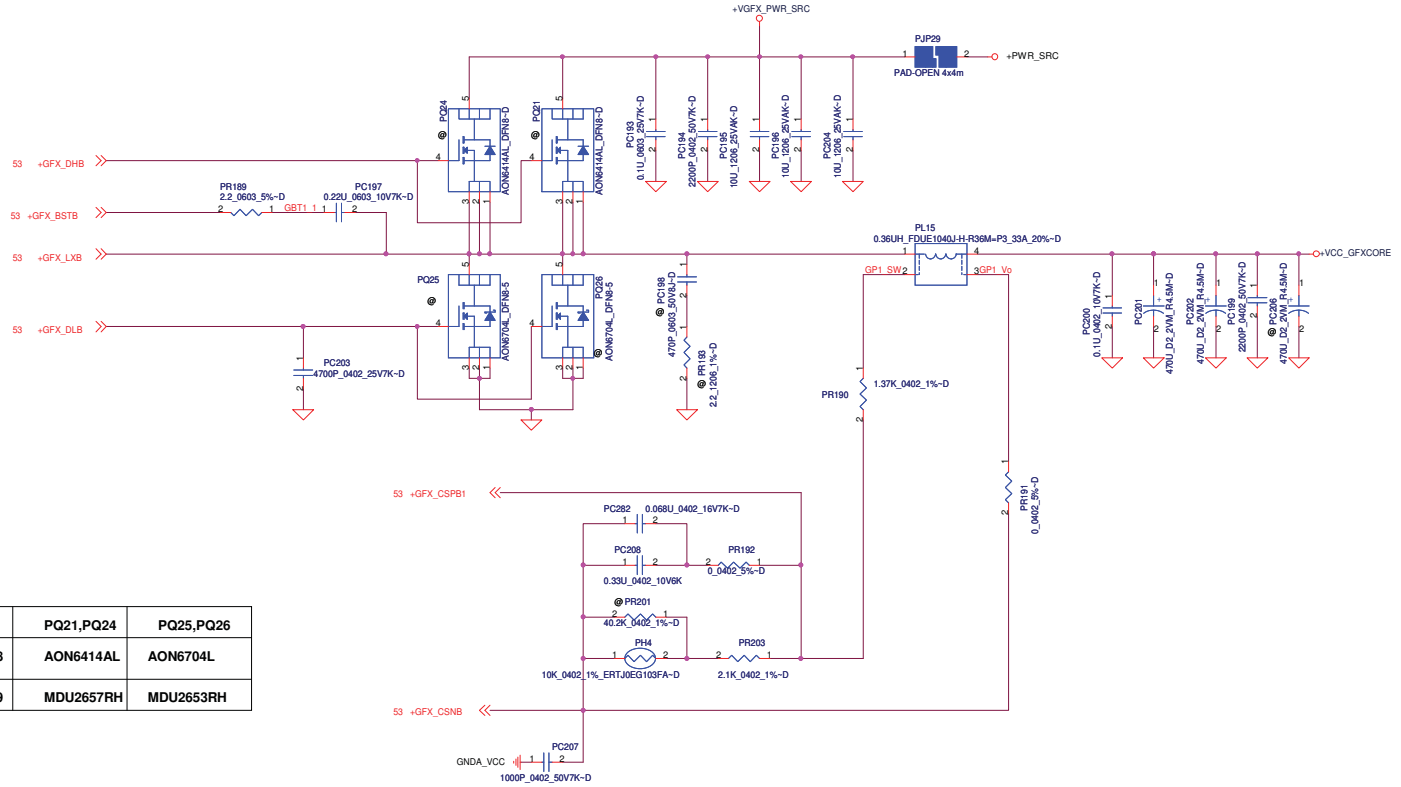
Date: Wednesday, January 26, 2011 | Sheet 53 of 57



		PQ21,PQ24	PQ25,PQ26
Main	X7629631L88	AON6414AL	AON6704L
2nd	X7629631L89	MDU2657RH	MDU2653RH

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Title: ISL95870A +1.05V_RUN_VTT

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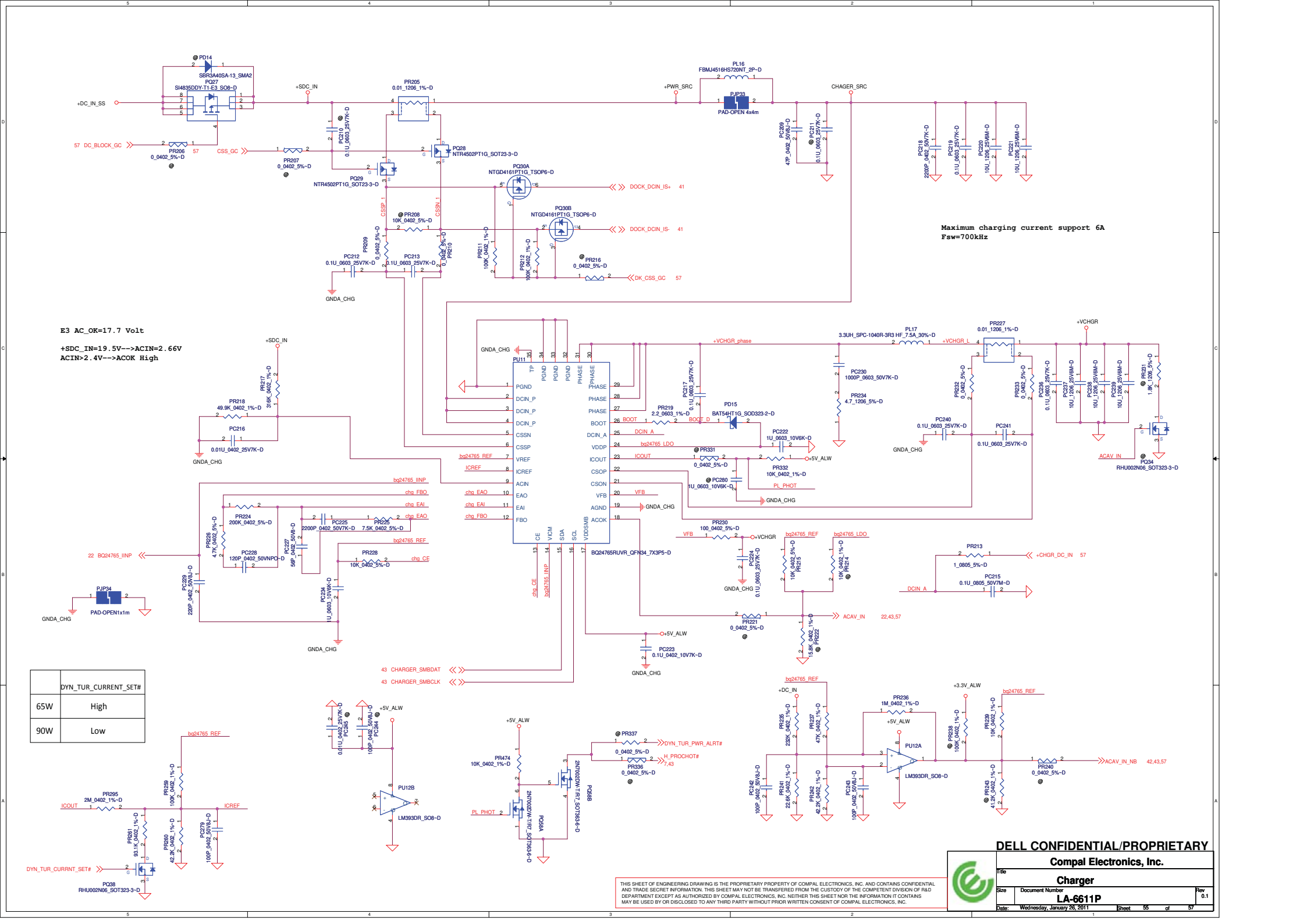
Maximum charging current support 6A
Fsw=700kHz
E3 AC_OK=17.7 Volt
+SDC_IN=19.5V-->ACIN=2.66V
ACIN>2.4V-->ACOK High
DYN_TUR_CURRENT_SET#
65W High
90W Low
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Compal Electronics, Inc.
Charger
LA-6611P
Rev 0.1
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	0.9V	0.85V
VCCSA_VID_1	0	1

output voltage adjustable network

1.05Volt +/-5%
Thermal Design Current : 4.2A
Peack current : 6A
OCP_MIN : 7.2A

de-pop for BGA1023 0.85V

de-pop for BGA1023 0.85V

PU13 TPS51461RGER_QFN24_4X4~D

PJP35 PAD-OPEN 43X118

PJP38 PAD-OPEN 4x4m

PJP37 PAD-OPEN1x1m

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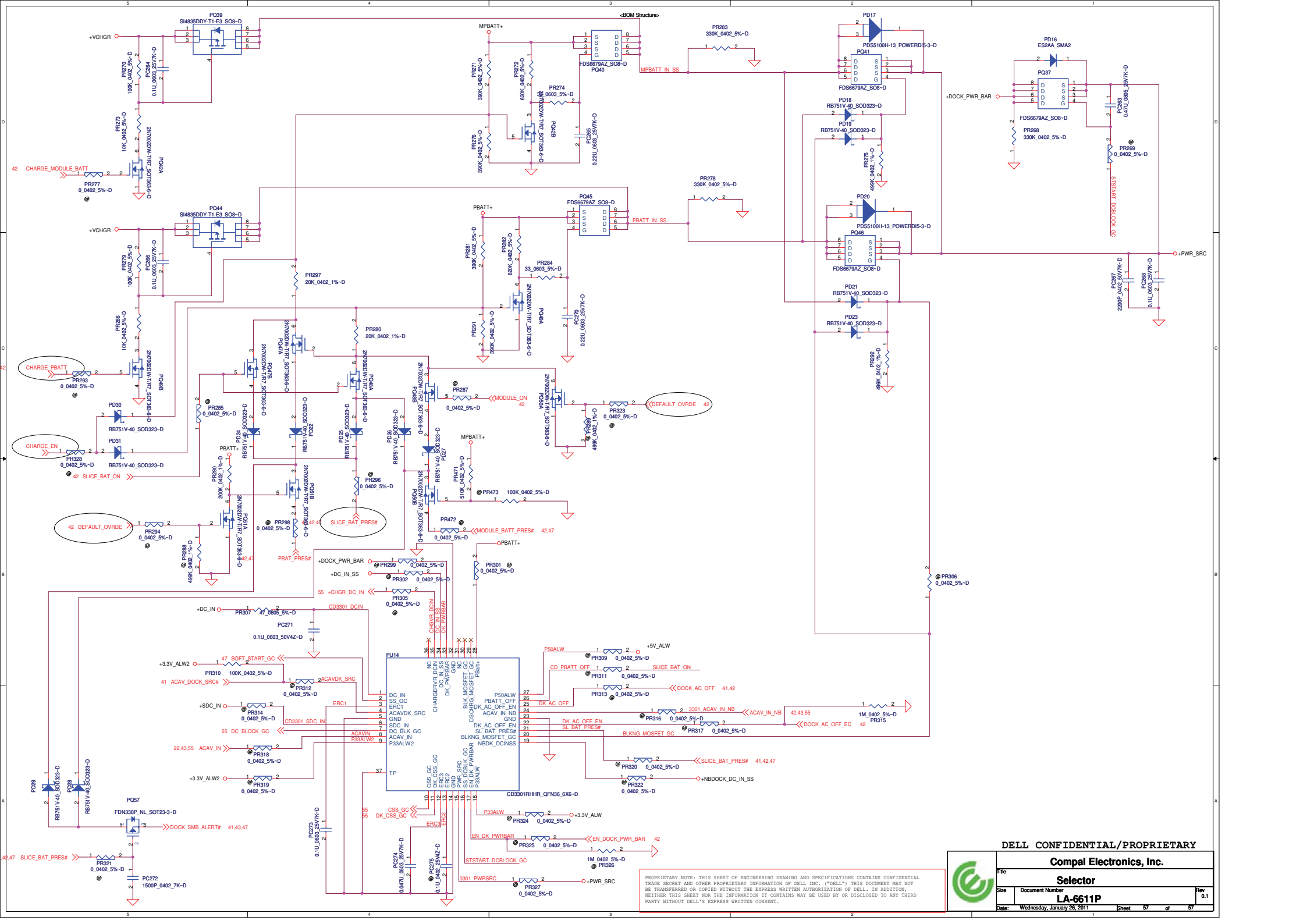
<BOM Structure>
PU14
CD3301RHHR_QFN36_6X6~D
PQ57
FDN338P_NL_SOT23-3~D
PQ40
PQ41
PQ42A
PQ42B
PQ43
PQ44
PQ45
PQ46
PQ47A
PQ47B
PQ48A
PQ48B
PQ49A
PQ49B
PQ50A
PQ50B
PQ51A
PQ51B
PD16
ES2AA_SMA2
PD17
PDS5100H-13_POWERDI5-3~D
PD18
PD19
PD20
PD21
PD23
PD24
PD25
PD26
PD27
PD28
PD29
PD30
PD31
RB751V-40_SOD323~D
FDS6679AZ_SO8~D
SI4835DDY-T1-E3_SO8~D
2N7002DW-T/R7_SOT363-6~D
+VCHGR
MPBATT+
PBATT+
+PWR_SRC
+DOCK_PWR_BAR
MPBATT_IN_SS
PBATT_IN_SS
CHARGE_MODULE_BATT
CHARGE_PBATT
CHARGE_EN
DEFAULT_OVRDE
MODULE_ON
SLICE_BAT_ON
SLICE_BAT_PRES#
MODULE_BATT_PRES#
PBAT_PRES#
+DC_IN_SS
+DC_IN
+CHGR_DC_IN
CD3301_DCIN
+3.3V_ALW2
+5V_ALW
+SDC_IN
CD3301_SDC_IN
DC_BLOCK_GC
ACAV_IN
ACAV_DOCK_SRC#
ACAVDK_SRC
ERC1
DOCK_SMB_ALERT#
DOCK_AC_OFF
DOCK_AC_OFF_EC
ACAV_IN_NB
3301_ACAV_IN_NB
DK_AC_OFF
DK_AC_OFF_EN
SL_BAT_PRES#
BLKNG_MOSFET_GC
+NBDOCK_DC_IN_SS
CSS_GC
DK_CSS_GC
P50ALW
P33ALW
EN_DK_PWRBAR
EN_DOCK_PWR_BAR
STSTART_DCBLOCK_GC
3301_PWRSRC
PR270 10K_0402_5%~D
PR271 390K_0402_5%~D
PR272 630K_0402_5%~D
PR273 10K_0402_5%~D
PR274 33_0603_5%~D
PR275 499K_0402_1%~D
PR276 390K_0402_5%~D
PR277 0_0402_5%~D
PR278 330K_0402_5%~D
PR279 10K_0402_5%~D
PR280 20K_0402_1%~D
PR281 390K_0402_5%~D
PR282 630K_0402_5%~D
PR283 330K_0402_5%~D
PR284 33_0603_5%~D
PR285 0_0402_5%~D
PR286 10K_0402_5%~D
PR287 0_0402_5%~D
PR288 499K_0402_1%~D
PR289 499K_0402_1%~D
PR290 200K_0402_1%~D
PR291 390K_0402_5%~D
PR292 499K_0402_1%~D
PR293 0_0402_5%~D
PR294 0_0402_5%~D
PR296 0_0402_5%~D
PR297 20K_0402_1%~D
PR299 0_0402_5%~D
PR301 0_0402_5%~D
PR302 0_0402_5%~D
PR305 0_0402_5%~D
PR306 0_0402_5%~D
PR307 47_0805_5%~D
PR309 0_0402_5%~D
PR310 100K_0402_5%~D
PR311 0_0402_5%~D
PR312 0_0402_5%~D
PR313 0_0402_5%~D
PR314 0_0402_5%~D
PR315 1M_0402_5%~D
PR316 0_0402_5%~D
PR317 0_0402_5%~D
PR318 0_0402_5%~D
PR319 0_0402_5%~D
PR320 0_0402_5%~D
PR321 0_0402_5%~D
PR322 0_0402_5%~D
PR323 0_0402_5%~D
PR324 0_0402_5%~D
PR325 0_0402_5%~D
PR326 1M_0402_5%~D
PR327 0_0402_5%~D
PR328 0_0402_5%~D
PR471 510K_0402_5%~D
PR472 0_0402_5%~D
PR473 100K_0402_5%~D
PC262 0.1U_0603_25V7K~D
PC263 0.47U_0805_25V7K~D
PC265 0.22U_0603_25V7K~D
PC266 0.1U_0603_25V7K~D
PC267 2200P_0402_50V7K~D
PC268 0.1U_0603_25V7K~D
PC270 0.22U_0603_25V7K~D
PC271 0.1U_0603_50V4Z~D
PC272 1500P_0402_7K~D
PC273 0.1U_0603_25V7K~D
PC274 0.047U_0603_25V7K~D
PC275 0.1U_0402_25V4Z~D
PC284 0.1U_0603_25V7K~D
PD22 RB751V-40_SOD323~D
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	14	HW	7/13/2010	COMPAL	Modify TAA SPI ROM topology	Add R933 0 ohm & Remove SPI_HOLD#0 and SPI_WP#0 connect to JP1	X01
2	11,56	HW	7/22/2010	COMPAL	Modify net name	Change +0.8V_VCC_SA to +VCC_SA	X01
3	22,25,28 32,42,43 45,11,20 37,11,	HW	7/22/2010	COMPAL	Follow PPM recommendation to change material	Change capacitors from 10uF_0805_10V_Y5V to 10uF_0805_6.3V_X5R: C305,C316,C387,C1181, C705,C728,C760,C764, C765,C768,C769,C772,CC135,CH58,CH73,CH80 Change capacitors from 10uF_0805_6.3V to 10uF_0603_6.3V: C475,C638,C641,C643 Change resistors to 0402 size: RC134, RH201,RH253,RH208,RH213 Delete RH192 and add PJP52	X01
4	14	HW	7/22/2010	COMPAL	De-pop PCH XDP	De-pop RH36,RH283,RH21,RH24,CH1,CH6	X01
5	14,29,43	HW	7/22/2010	COMPAL	Modify Module Bay circuit	Change net name ODD_DET# to PCH_SATA_MOD_EN#, r and USB_MCARD3_DET# to remove R1069,R1182,R1188,R425, Add R513,Q76,Q123B, change BAY SM bus PU rail to +3.3V_ALW	X01
6	18	HW	7/22/2010	COMPAL	Follow Intel Design Guide Rev1.0	Change RH149 to 1k and RH150 to 4.7k	X01
7	22	HW	7/22/2010	COMPAL	Change MAX8731_IINP connection	Change to VCP	X01
8	22	HW	7/22/2010	SMSC	Per SMSC request	Add R404 10K pull down of TEST1 pin	X01
9	26	HW	7/22/2010	COMPAL	For Safety request	Add D4 and R5 co-lay with F2,	X01
10	40	HW	7/22/2010	COMPAL	Change ESATA repeater	Add R1585~R1588, and change U44 to MAX4951BECTP	X01
11	30	HW	7/22/2010	COMPAL	Change codec to ZB version	Change Codec part number to SA00003ZZ1L and stuff C962	X01
12	34	HW	7/22/2010	COMPAL	Change RFID capacitors for more popular	Change C502,C505 from 1uF to 0.1uF	X01
13	24,46	HW	7/22/2010	COMPAL	Correct net name for LED signal	Modify signal name BREATH_BLUE_LED to BREATH_WHITE_LED and BREATH_BLUE_LED_SNIFF to BREATH_WHITE_LED_SNIFF	X01
14	42	HW	7/22/2010	COMPAL	Add 0 ohm resistor for SUSACK#	Add R1132 and add net name SUSACK#_EC	X01
15	32	HW	7/22/2010	INTEL	Remove useless resistors	Remove R556, R558, R559, R560 and short it.	X01
16	32,28,29 38,45	HW	7/22/2010	COMPAL	Change part for Halogen free	Change Q18,Q27,Q30,Q34,Q38,Q40,Q42,Q49,Q54,Q58 to HF part	X01
17	10	HW	7/22/2010	COMPAL	CC129~CC134 D2T LESR5M EOL	Change CC129~CC134 to SGA00004X0L	X01
18	37	HW	7/22/2010	COMPAL	Modify Module Bay circuit	De-pop C627,R712	X01
19	7	HW	7/22/2010	COMPAL	For support XDP device	De-pop RC9	X01
20	42	HW	7/22/2010	COMPAL	Base on GPIO map to modify	Change SLICE_BAT_PRES# pull up power rail from +3.3V_ALW2 to +3.3V_ALW	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	43	HW	7/22/2010	COMPAL	Base on GPIO map to modify	Add R889 for CPU1.5V_S3_GATE pull down	X01
22	15,18	HW	7/22/2010	COMPAL	Base on GPIO map to modify	Remove RH238,RH172 and change connection form SLP_ME_CSW_DEV# from GPIO45 to GPIO28	X01
23	24	HW	7/22/2010	COMPAL	PWM function	Remove R1139,R1140 and add D68,D69, pop R1137	X01
24	37,46	HW	7/22/2010	COMPAL	Modify LED circuit	Remove R1578,R1579,R1580,D42,D60,D61, add Q77,Q124,R705,R718,R719	X01
25	15,32	HW	7/22/2010	COMPAL	EOL concern	Change Y3 and YH2 from 1Y725000CE1A to 7A25000110	X01
26	24,27,46	HW	7/22/2010	COMPAL	Change part for Halogen free part	Change QC5 to NTR4501NT1G, U21,U24,U54,U55,U57 change to NC7SZ04P5X-G, Q21 change to FDC654P-G	X01
27	36	HW	7/22/2010	O2-Mirco	Add discharge circuit for +3.3V_RUN_CARD	Add R826 on +3.3V_RUN_CARD	X01
28	31,42,46	HW	7/22/2010	COMPAL	Remove mute function and LED	Remove R1109,Q119,Q105,Q102,R1059,R1061	X01
29	17,18,43	HW HW	7/22/2010 7/22/2010	COMPAL COMPAL	To solve back drive issue	Remove USB_OC7# signal and RH254, change connection from PCH GPIO1 to GPIO14,and change RH164 pull up power rail from +3.3V_RUN to +3.3V_ALW_PCH	X01
30	18	HW	7/22/2010	COMPAL	Add pull up for PCH GPIO1	Change RH254 to 10K and pull high to +3.3V_RUN	X01
31	29,45	HW	7/22/2010	COMPAL	For cost saving	Add PJP63,RH202, no stuff QH4,Q49,RH278,R908	X01
32	42	HW	7/22/2010	COMPAL	Follow GPIO 0720	Add DYN_TUR_PWR_ALRT# up power rail and change R796 pull from +3.3V_RUN to +3.3V_ALW	X01
33	43	HW	7/22/2010	COMPAL	Follow GPIO 0720	Add DYN_TUR_CURRNT_SET# up power rail and change R837 pull from +3.3V_RUN to +3.3V_ALW	X01
34	28,46	HW	7/22/2010	COMPAL	Part leverage select	Change D16,D59,D62 to SC100000S0L	X01
35	14	HW	7/22/2010	COMPAL	Follow Intel XDP design guide	Change RH43,RH44,RH45 to 200 ohm	X01
36	24,40	HW	7/22/2010	INTEL	Change material for small size	Change C300,C669 from 1206 16V to 0805 10V	X01
37	39,40	HW	7/22/2010	COMPAL	Remove useless capacitors	Remove C1151~C1154	X01
38	37	HW	7/22/2010	COMPAL	Add 0 ohm R on PCIE_MCARD2_DET#	Add R725	X01
39	43	HW	7/22/2010	COMPAL	Follow GPIO MAP 0720	Add R1578 for XFR.	X01
40	42	HW	7/22/2010	COMPAL	Add 0 ohm for TEMP_ALERT#	Add R773	X01
41	44	HW	7/22/2010	COMPAL	Solution +1.5V_RUN voltage drop issue	Change Q59 from SI3456BDV to NTGS4141NT1G	X01
42	46	HW	7/27/2010	COMPAL	Add pull down 100k on BT_ACTIVE	Add R959	

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44	40	HW	7/27/2010	COMPAL	Follow Vender request.	R1589~R1592	X01
45	43	HW	7/27/2010	COMPAL	BID change	Change R875 to 130K	X01
45	22	HW	7/27/2010	COMPAL	Chnage thermal diode connection	Remove C268	X01
46	18,30	HW	7/28/2010	COMPAL	Remove SPEAKER_DET# PAID.	Chnage SPEAKER_DET# to GPIO17, and change speaker connector to SP02000H900	X01
47	14,47	HW	7/28/2010	COMPAL	Remove RTC_DET# PAID.	Remove RH31, add T132	X01
48	22	HW	7/28/2010	COMPAL	Follow connector list	change FAN connector to SP02000TI00	X01
49	33	HW	7/28/2010	COMPAL	Follow connector list	Re-link RJ45 symbol	X01
50	44	HW	7/28/2010	COMPAL	Follow connector list	Chnage keyboard connector to pitch 1	X01
51	34	HW	7/28/2010	COMPAL	Remove Broadcom debug connector	Remove JBRCM1 and add R666 no stuff	X01
52	47	HW	7/28/2010	COMPAL	Change RTC connector	Change to TYCO_2-1775293-2	X01
53	43	HW	08/05/2010	COMPAL	Change signal net name	Change 0.8V_VCCPWROK net name to VCCSAPWROK	X01
54	30	HW	08/13/2010	COMPAL	Fix Speaker EMI issue	Change R1183~R1186 to L78~L81 pop C973~C976,C267,C283 and C284	X01
55	39,40	HW	08/13/2010	COMPAL	Fix USB EMI issue	pop L50,L52,depop R737,R739,R734,R735	X01
56	29	HW	08/13/2010	COMPAL	Change ODD repeater	Chnage ODD repesater to MAX4951B and R1174,R1176,R1169,R1171 to 0 ohm	X01
57	43	HW	08/13/2010	COMPAL	EOL concern	Change Y6 to SJ132P7KW1L same as YH1	X01
58	22	HW	08/13/2010	COMPAL	Change FAN conn type for ME request	change FAN connector to SP02000CB0L	X01
59	14	HW	08/13/2010	COMPAL	Change TAA topology	redefine JP1 TAA pin define	X01
60	10	HW	08/16/2010	COMPAL	Follow PPDG1.2 Vcore 2.2uf 0402 QTY from 55 to 35 pcs	remove CC199,CC103,CC120,CC142,CC141,CC171,CC139,CC134,CC133,CC200 CC101,CC128,CC153,CC102,CC126,CC105 16pcs depop 4 pcs CC152,CC121,CC127 and CC160	X01
61	18	HW	08/16/2010	COMPAL	Follow INTEL DG DF_TVS pull high value	Change RH150 to 0 ohm RH149 to 2.2K ohm	X01
62	14 15 43	HW	08/16/2010	COMPAL	Crystal EA	Change C743=39pF CH2,CH3=15pF CH18,CH19=10pF and YH2 to SJ100008E0L	X01
63	22	HW	08/17/2010	COMPAL	reserve cap for CPU remote diode	Add C286	X01
64	14	HW	08/17/2010	COMPAL	reserve Resistance and Cap for SPI EA	Add CH107,CH108,R935	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
65	34	HW	8/20/2010	COMPAL	BRCM request RFID filter need have 400mA max	Change L39 and L40 to SHI0000CH0L.Reserve L45,L46 colay	X01
66	14	HW	8/23/2010	COMPAL	Improve SPI EA for SPI_CLK	Change R899 and R897 to 56 ohm	X01
67	30	HW	8/23/2010	COMPAL	Follow connector list	Change Speaker CONN to SP021007221	X01
68	42	HW	8/24/2010	COMPAL	RF noise	pop R794 R795 to 10 ohm,C712 C713 to 10p	X01
69	14	HW	8/25/2010	COMPAL	Improve SPI power path	Always pop C745	X01
70	36	HW	8/25/2010	COMPAL	O2 recommend add cap for +PE_VDDH	add C559 0.1uF C560 0.01uF	X01
71	14 18	HW	8/26/2010	COMPAL	Follow INTEL DPDG	reserve RH31,RH355 for GPIO19/GPIO28	X01
72	14	HW	8/27/2010	COMPAL	remove double reserve cap for BIT_CLK	remove CH100	X01
73	16	HW	8/27/2010	COMPAL	reserve ME_SUS_PWR_ACK pull down	reserve RH145	X01
74	26	HW	8/27/2010	COMPAL	Follow INTEL HDMI DG	remove R1164,R458,R1128-->20K add R1593 depop D65	X01
75	11	HW	8/30/2010	COMPAL	Change QC5 VGS to 20V part	Change QC5 to SB00000HK0L	X01
76	37	HW	9/1/2010	COMPAL	Depop SIM card ESD diode	Depop U40	X01
77	24	HW	10/6/2010	COMPAL	Change RB751V to HF part	Change D63,D64,D68,D69 to SCS00004L0L	X02
78	24	HW	10/6/2010	COMPAL	AUO panel can't adjust brightness	Change R1137 from 100k to 10k	X02
79	14,18	HW	10/6/2010	Intel	Follow DG1.5 and schematic check list rev1	Add RH41,depop RC96 and RC97,change RH177 to 10K	X02
80	30,31	HW	10/6/2010	IDT	To solve pop noise and detect issue	Add U6,Q33,Q46,D70,D71,R425,R33,R38,R430,R352,R1088,C967,C307,C308,R161	X02
81	32,42	HW	10/11/2010	COMPAL	LOM Cable Detect function	add U15, C478 change TP_DET# netname to WLAN_LAN_DISB# JTP1 pin1 change to GND	X02
82	42	HW	10/11/2010	COMPAL	Change Board ID to X02	Change R875 to 62K	X02
83	17	HW	10/11/2010	Intel	Follow Intel check list rev1.2	Add @RH332	X02
84	46	HW	10/11/2010	COMPAL	LED brightness test result	Change R957 to 560,R941,R939,R934 to 4.7k,R955,R949 to 2K	X02
85	24, 30	HW	10/19/2010	EMI	EMI issue for PWM and DMIC_CLK	Add L83,change R1582 to L82	X02
86	30	HW	10/19/2010	COMPAL	Change Codec rev to YA	Change U72 to SA00003ZZ2L	X02
87	32	HW	10/19/2010	COMPAL	Change LAN stepping to C0	Change U31 to SA00003SI2L	X02
88	39,40	HW	10/19/2010	ESD	PT ESD test result	Change U91,U92 to D72,D73. Pop D73	X02
89	24	HW	10/19/2010	Compal	PT ESD test result	remove D7,D8,DE1~DE4	X02

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90	32	HW	10/19/2010	COMPAL	IEEE test result	Change L30~L37 to 12nH	X02
91	28	HW	10/19/2010	COMPAL	Support SSD hard drive	Add PJP64,C399,C402	X02
92	31,43	HW	10/19/2010	COMPAL	Non-support Latitude on	depop SW2,C740,R877	X02
93	22	HW	10/19/2010	COMPAL	Change OTP set to 91 degree	Change R406 to 1.15k	X02
94	26	HW	10/20/2010	COMPAL	HDMI SDVO CTRL PU same as 14"	del D65,R1593	X02
95	30,42	HW	10/20/2010	COMPAL	GPIO map change AUD_NB_MUTE to AUD_NB_MUTE#	change AUD_NB_MUTE to AUD_NB_MUTE#	X02
96	14	HW	10/26/2010	COMPAL	Follow Intel CRB FAB2 PCH XDP schematic	Add @RH284	X02
97	41	HW	11/1/2010	COMPAL	EMI dock clk issue	pop R756=33ohm C704=12pf	X02
98	18	HW	11/1/2010	COMPAL	Follow schmaitc check list	depop RH174 RH175	X02
99	14	HW	11/8/2010	COMPAL	For easy control TAA/nonTAA BOM	Add R936 colay R895,R944 colay R897,R943 colay R900	X02
100	15	HW	11/8/2010	COMPAL	DF416400 AMT_Run MEflow Stress test fai	depop RH296 RH297,pop QH5 RH302,RH303	X02
101	25	HW	11/10/2010	COMPAL	Pericom VGA SW high EOS failure rate	Change C321,C318 from 0.1uF to 0.01uF(pin4,pin23)	X02
102	6-11,14-21	HW	11/10/2010	COMPAL	Change CPU PCH PN to QS sample	Change UH4 PN to SA00004IW1L ,U1 PN to SA00004EL1L	X02
103	46	HW	11/10/2010	ME	Change KB screw hole	Change H12 H13 from 2.3 to 2.6	X02
104	22	HW	11/10/2010	COMPAL	Thermal request change OTP set to 94 degree	Change R406 to 1.4k	X02
105	28	HW	11/18/2010	COMPAL	Follow Intel CRB SMBUS PU value	Change R501 R502 from 2.2k to 10k	X02
106	28,45	HW	11/19/2010	COMPAL	For cost saving(+5V_HDD / +3.3V_ALW_PCH)	De-pop R499,R500,C393,Q28,R905,R907,C762,Q51	X02
107	17,39	HW	12/23/2010	COMPAL	SW WHQL request USB debug need USB port1	Change USB port0 to port1	A00
108	43	HW	12/27/2010	COMPAL	Change Board ID to A00	Change R875 to 33k	A00
109	43	HW	12/27/2010	COMPAL	To solve backdrive issue	Pop Q45	A00
200	34-35	HW	12/27/2010	COMPAL	Change USH chip to CID7	Change U33 to SA00003AO2L	A00
201	30-31	HW	1/3/2011	COMPAL	remove MIC external detect	del U6,Q33,Q46,D70,D71,R425,R33,R38,R430,R352,R1088,C967,C307,C308,R161	A00
202	14	HW	1/5/2011	COMPAL	For cost saving	De-pop RH47,RH48,RH49,RH288	A00
203	22	HW	1/18/2011	COMPAL	Same as 14	Change R385 to 10K	A00
204	44	HW	1/21/2011	COMPAL	DF445509:TP will malfunction intermittently.	Change R902 to 2.2K	A00

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	+DCIN	7/15	Compal	System can't recognize battery issue	Change PBATT2 Pin2 connection from Z4304 to Z5304 Change PBATT2 Pin2 connection from Z4305 to Z5305 Change PBATT2 Pin2 connection from Z4306 to Z5306	
2	47	+DCIN	7/15	Compal	System can't recognize battery issue	Change PR77 pin2 connection from BAY_SMBCLK to BAY_SMBDAT	
3	55	Charger	7/15	Compal	System can't recognize battery issue	Change PU11 pin 15 connection from CHARGER_SMBCLK to CHARGER_SMBDAT Change PU11 pin 16 connection from CHARGER_SMBDAT to CHARGER_SMBCLK	
4	47	+DCIN	8/4	Compal	Follow Macallan 14 for new battery cell	Change PL1 from SM01002078L to SM010009C8L and add PL20 Change PL19 from SM01002078L to SM010009C8L	
5	48	3/5V	8/4	Compal	Follow Macallan 14	Change PC24 from 4.7u/6.3V/0805 (SE093475K8L) to 4.7u/6.3V/0603 (SE107475K8L)	
6	47	+DCIN	8/4	Compal	RTC remove detect function (7/29 EE mail)	Delete JRTC1 pin2 RTC_DET# connection	
7	56	+VCC_SA	8/4	Compal	Follow Macallan 14 VCCSA not fix at 0.8V. change net name from +0.8V_VCC_SA to +VCC_SA	Change +0.8V_VCC net name to +VCCSA_P Change 0.8V_VCCPWROK net name to VCCSAPWROK	
8	55	Charger	8/4	Compal	Follow Macallan 14	Depop PD14 SBR3A40SA (SC100003J00)	
9	57	Selector	8/4	Compal	Follow Macallan 14 Leakage issue on PD16	Change PD16 from SBR3A40SA (SC100003J00) to ES2AA (SC100005A0L)	
10	55	Charger	8/4	Compal	Follow Macallan 14 Add adapter protection circuit for turbo mode	Add PU11 pin8 connection ICREF Add PU11 pin23 connection ICOUT Add PR259,PR260,PR261,PR295, PR331,PR332 Add PC279,PC280 Add PQ38	
11	56	VCCSA	8/18	Intel	Intel change BGA1023 VID table VID0 0 VID1 1 voltage from 0.8V to 0.85V	Change VID setting	
12	53,54	Vcore, VGFX	8/18	Maxim	Reserve 0402 cap pad for transient fine tune	Add PC281 and PC282 0402 cap location	
13	53,54	Vcore, VGFX	8/18	Maxim	change setting for Pass2 sample	Change PR330 from 2_ohm to 0_ohm Change PR127 from 150K_ohm to 165K_ohm Change PR135 from 100K_ohm to 105K_ohm Change PR157 from 8.66K_ohm to 10.2K_ohm Change PR190 from 1.43K_ohm to 1.37K_ohm Change PR192 from 2_ohm to 0_ohm de-pop PR201 Change PR110 PR112 PR115 from 12.7K_ohm to 13.3K_ohm	
14	53,54	Vcore, VGFX	8/18	Compal	Change PQ9 PQ10 PQ11 to prevent COS issue	Change PQ9 form CSD86350Q5D to PQ9 AON6414AL + PQ10 AON6704L Change PQ10 form CSD86350Q5D to PQ11 AON6414AL + PQ15 AON6704L Change PQ11 form CSD86350Q5D to PQ3 AON6414AL + PQ14 AON6704L	
15	56	VCCSA	8/23	TI	Change Thermal pad to PGND	Change PU13 pin 25 from GNDA_VCCSA to PGND	
16	56	VCCSA	8/23	TI	For batter output voltage accuracy	Add PC383 from PR247 pin2 to PU13 pin2	
17	55	Charger	8/24	Dell	Add turbo mode adapter protection by H_PROCHOT#	Add PR336 PR337 for pop opton to select H_PROCHOT# or DYN_TUR_PWR_ALRT#	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
18	50	+0.75_DDR_VT/ +1.8V_RUN	8/26	TI	for more phase margin	Change PC71 from 1800pF to 18nF	
19	47	+DCIN	9/1	Dell	reduce leakage current	Change PR2 PR108 from 10K_ohm to 100K_ohm	
20	56	VCCSA	9/1	Intel	Intel update VCCSA voltage change only for UL ULV type. our project is SV type hence keep no change	de-pop PR250 PR251 PR252 PR333 PR334 PR335 pop PR264 PR265 PR266 PR300	
21	51	1.05V_M	10/20	Compal	22u/1206/6.3V COS issue	Change PC98~PC105 from 22u/1206 (SE077226M8L) to 22u/0805 (SE00000110L)	
22	52	1.05V_RUN_VTT	10/20	Compal	22u/1206/6.3V COS issue	Change PC120~PC127 PC129 PC130 from 22u/1206 (SE077226M8L) to 22u/0805 (SE00000110L)	
23	51	1.05V_M	10/20	TI	TI IC OCP setting value change (as PT memo)	Change PR83 from SD03457628L 57.6K_ohm 0402 to SD03410028L 10K_ohm 0402	
24	53	Vcore	11/05	Maxim	Initial voltage accurate	PR110 PR112 PR115 change from 13.3K_ohm to 12.7K_ohm PR109 change from 6.49K_ohm to 5.9K_ohm	
25	53	Vcore	11/05	Maxim	Load line modify Transient compensation	PR140 change from 9.76K_ohm to 8.45K_ohm PC281 pop 10n	
26	53,54	Vcore,VGFX	11/05	Maxim	Load line modify Transient compensation	PR157 change form 10.2K_ohm to 7.5K_ohm PC282 pop 68nF	
27	57	Selector	11/10	Compal	Fine tune main and media battery switching to slice battery transient time (follow 14")	Change PC270 and PC265 from 1uF (SE00000698L) to 0.22uF (SE000005Z8L)	
28	55	Charger	11/10	Compal	Change adapter protection circuit trip point. (Adapter rated current + 0.75A) (follow 14")	Change PR295 from 1.87M (SD00000WN0L) to 649K (SD03464938L) Change PR261 from 73.2K (SD00000B18L) to 95.3k (SD03495328L)	
29	55	Charger	11/10	Compal	Change adapter protection event to HW from SW	Pop PR336 De-pop PR332 PR337	

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