

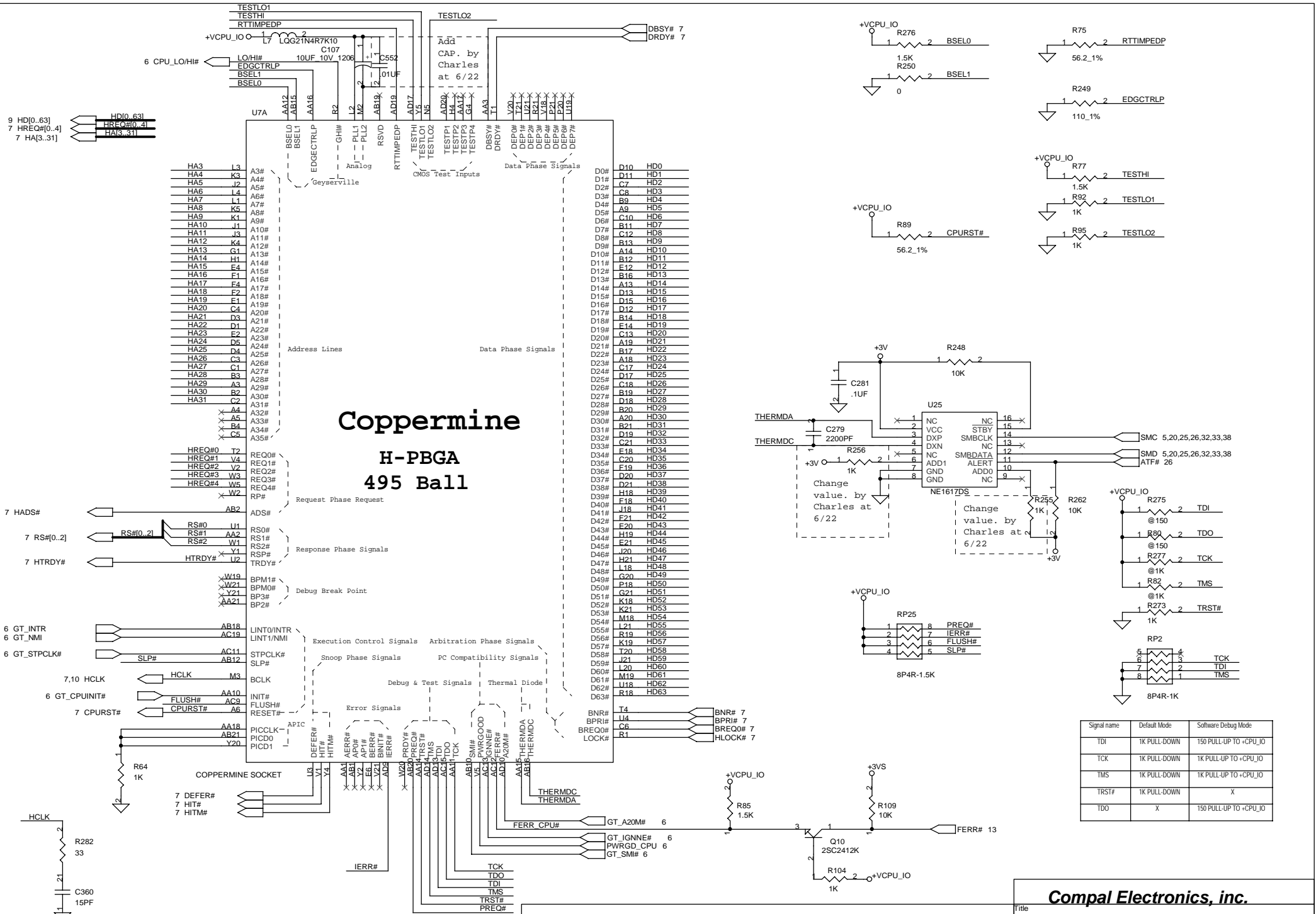
# *Hurricane 1.6*

*N32N LA-733 REV. 4A SCHEMATIC DOCUMENT*  
*uPGA2 COPPERMINE with Geyserville*

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Title			
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# Coppermine

## H-PBGA

### 495 Ball

Signal name	Default Mode	Software Debug Mode
TDI	1K PULL-DOWN	150 PULL-UP TO +CPU_IO
TCK	1K PULL-DOWN	1K PULL-UP TO +CPU_IO
TMS	1K PULL-DOWN	1K PULL-UP TO +CPU_IO
TRST#	1K PULL-DOWN	X
TDO	X	150 PULL-UP TO +CPU_IO

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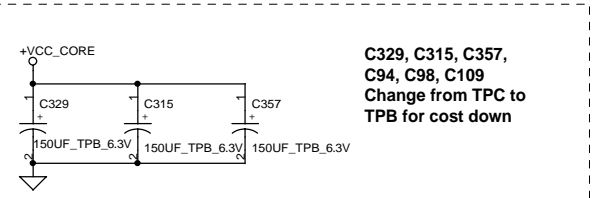
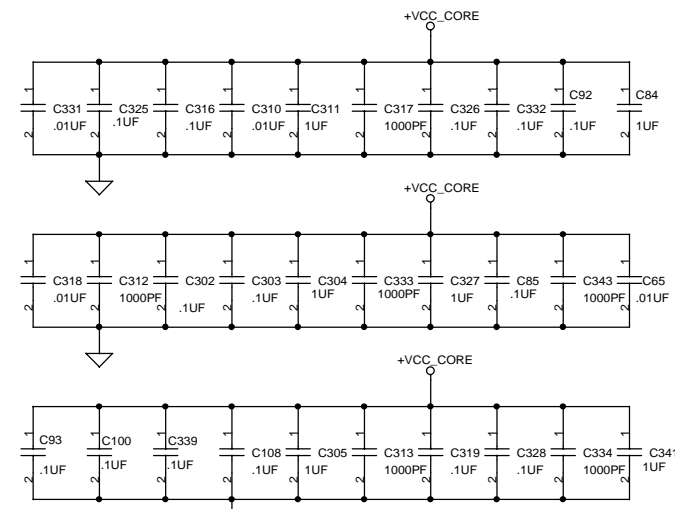
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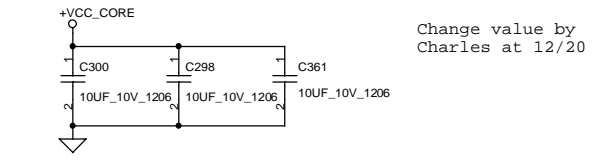
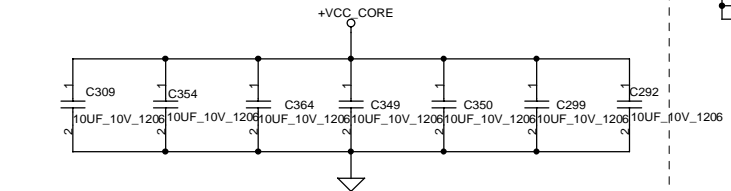
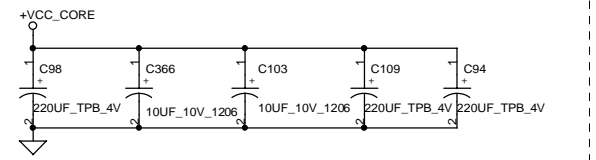
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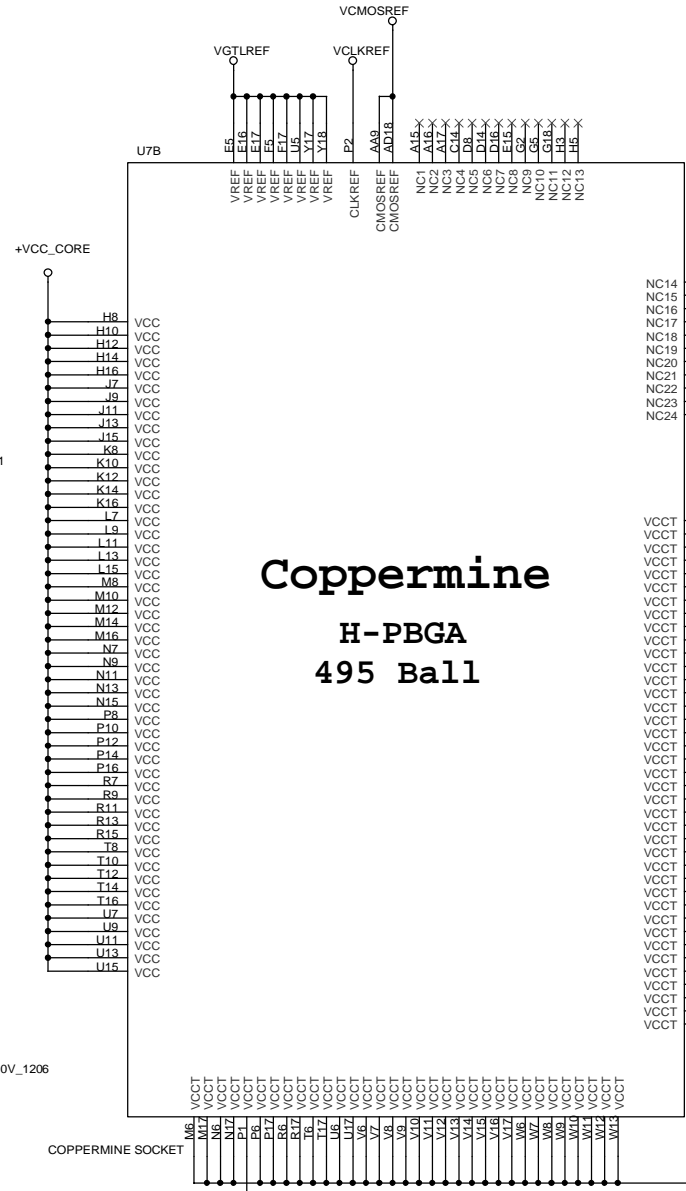
Rev 4C



**C329, C315, C357,  
C94, C98, C109**  
Change from TPC to  
TPB for cost down



Change value by  
Charles at 12/20

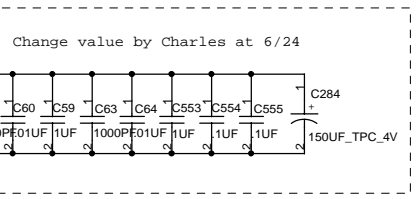
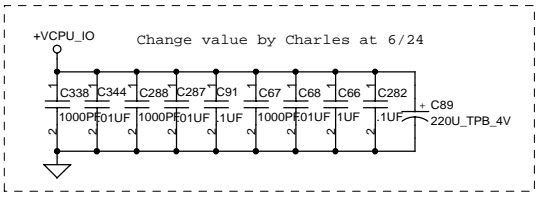
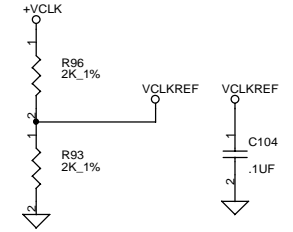
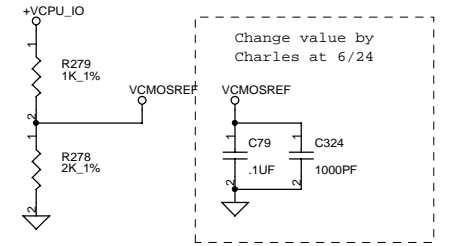
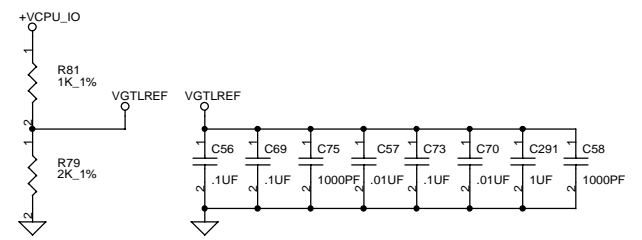


# Coppermine

## H-PBGA

### 495 Ball

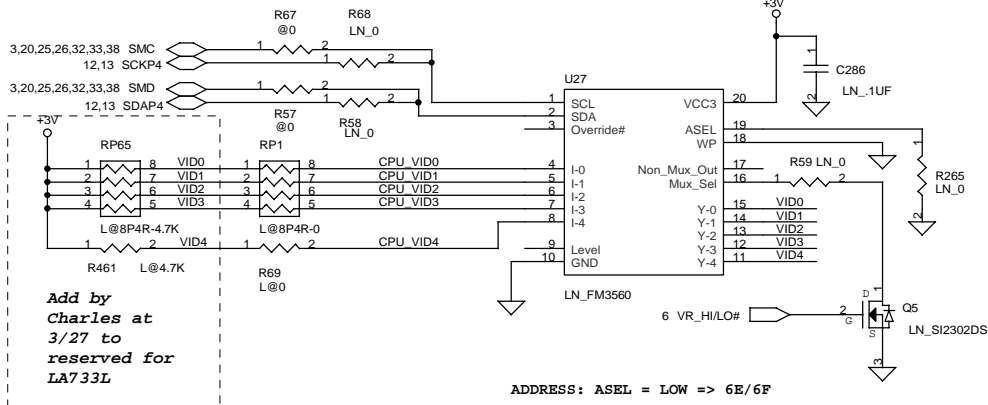
+VCC\_CORE  
Change by  
Charles at 9/2



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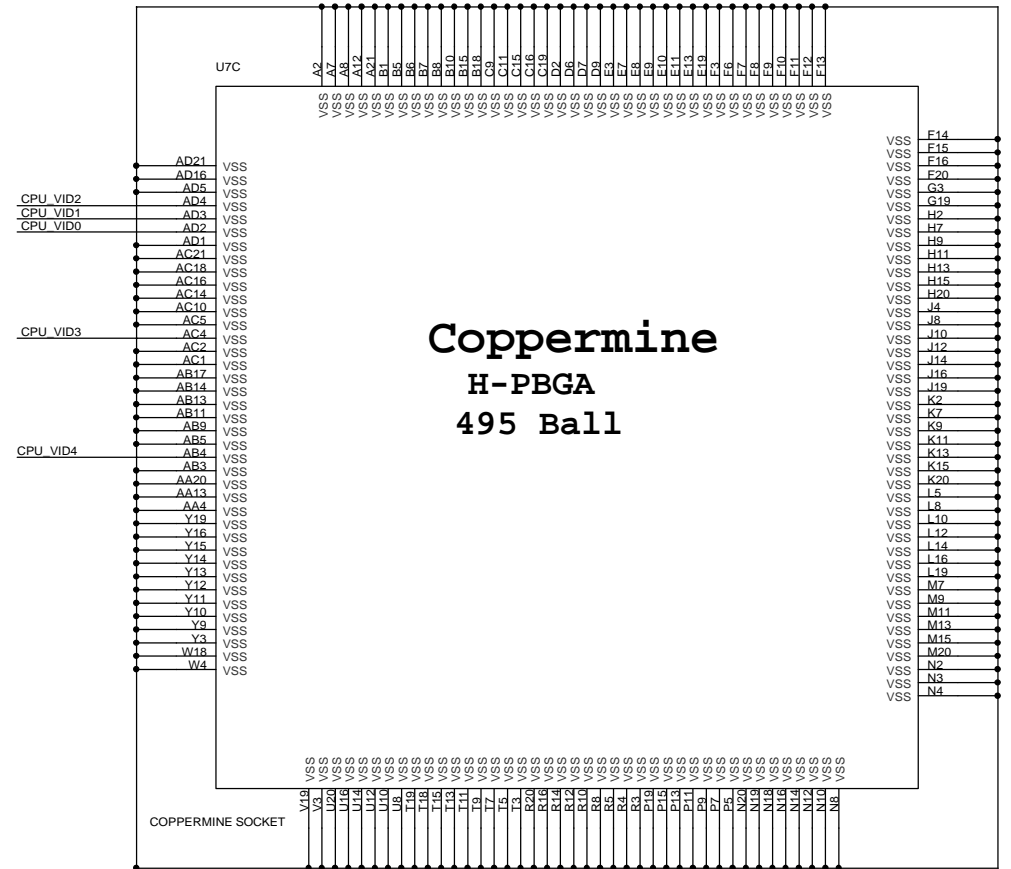
VID[0..4] → VID[0..4] 36



Add by Charles at 3/27 to reserved for LA733L

ADDRESS: ASEL = LOW => 6E/6F

VID4	VID3	VID2	VID1	VID0	+VCC_CORE
0	1	1	1	0	1.3V
0	1	1	0	1	1.35V
0	1	0	1	0	1.5V
0	1	0	0	1	1.55V
0	1	0	0	0	1.6V
0	0	1	1	1	1.65V
0	0	1	1	0	1.70V
0	0	1	0	1	1.75V
0	0	1	0	0	1.80V
0	0	0	1	1	1.85V



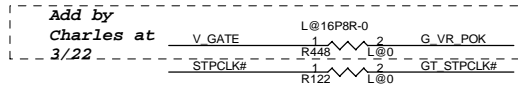
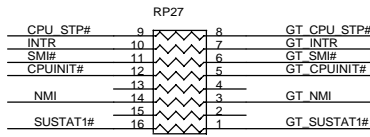
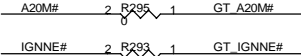
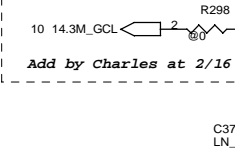
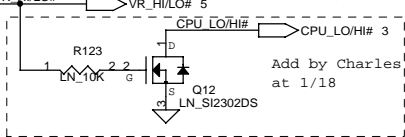
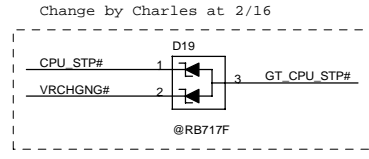
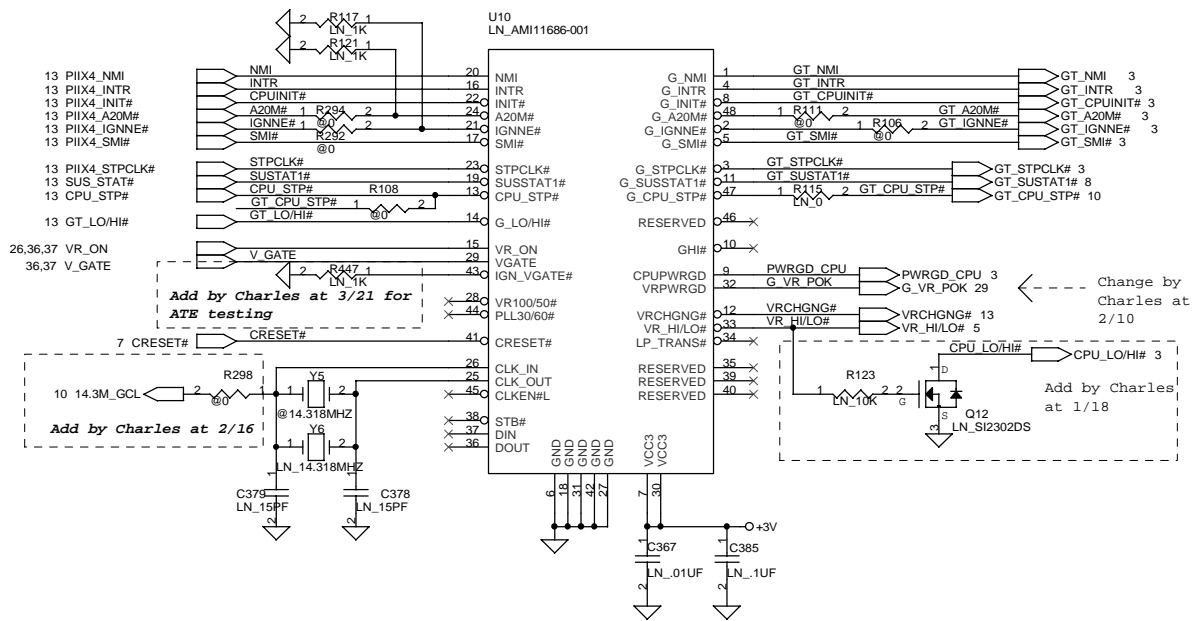
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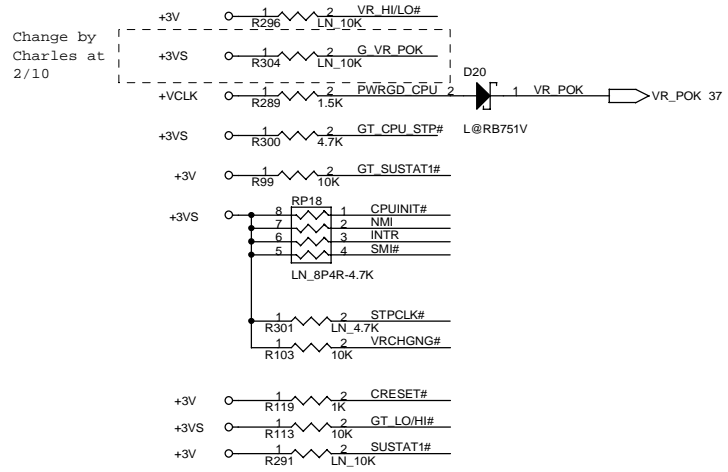
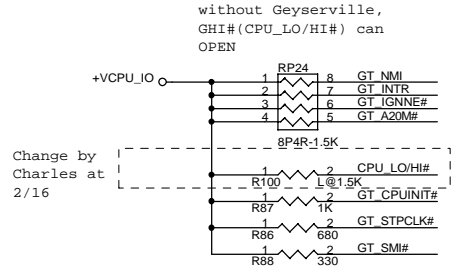
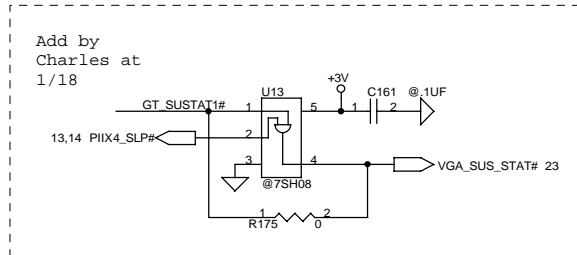
Title: SCHEMATIC, M/B LA-733

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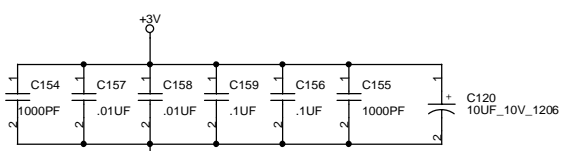
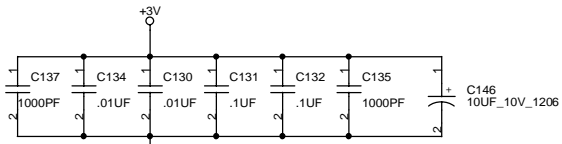


for without Geyserville



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SCHEMATIC, M/B LA-733	
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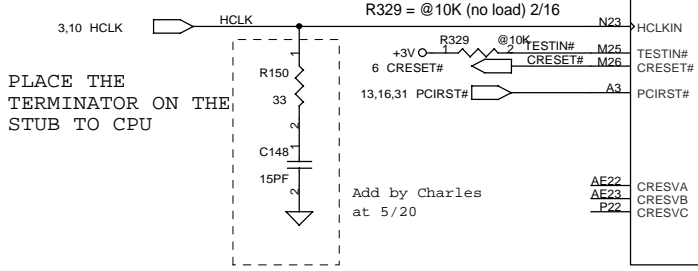
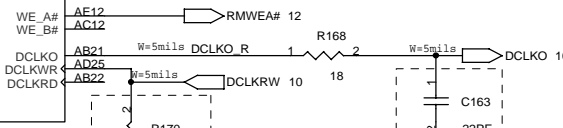
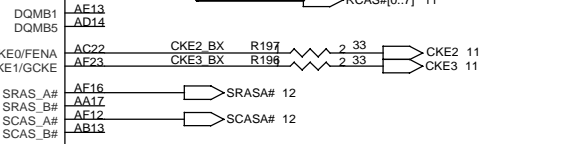
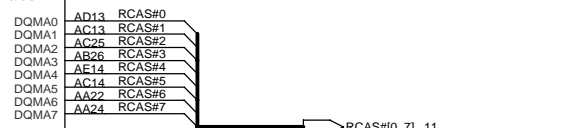
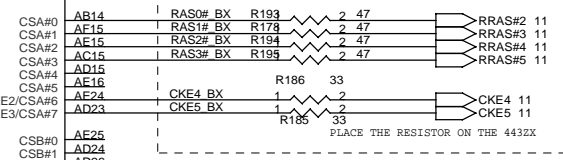
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HA4	H22	HA#4
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HA7	G24	HA#7
HA8	F26	HA#8
HA9	G26	HA#9
HA10	G22	HA#10
HA11	F22	HA#11
HA12	F23	HA#12
HA13	F24	HA#13
HA14	F25	HA#14
HA15	F23	HA#15
HA16	F26	HA#16
HA17	F25	HA#17
HA18	D25	HA#18
HA19	D26	HA#19
HA20	B25	HA#20
HA21	C26	HA#21
HA22	A25	HA#22
HA23	C25	HA#23
HA24	A24	HA#24
HA25	D24	HA#25
HA26	C23	HA#26
HA27	B24	HA#27
HA28	C24	HA#28
HA29	A23	HA#29
HA30	F22	HA#30
HA31	D23	HA#31

82443ZXM-100  
492 BGA

HOST INTERFACE

DRAM INTERFACE

MAA0	AE17
MAA1	AB16
MAA2	AE17
MAA3	AC17
MAA4	AE18
MAA5	AE19
MAA6	AE19
MAA7	AC18
MAA8	AC19
MAA9	AE20
MAA10	AD20
MAA11	AE21
MAA12	AC21
MAA13	AE25
MAB#0	AD16 MMA0
MAB#1	AC16 MMA1
MAB#2	AD17 MMA2
MAB#3	AB17 MMA3
MAB#4	AE18 MMA4
MAB#5	AD19 MMA5
MAB#6	AB19 MMA6
MAB#7	AE20 MMA8
MAB#8	AC20 MMA9
MAB#9	AD20 MMA10
MAB#10	AE21 MMA11
MAB#11	AD21 MMA12
MAB#12	AE22 MMA13
MAB#13	



PLACE THE TERMINATOR ON THE STUB TO CPU

Add by Charles at 5/20

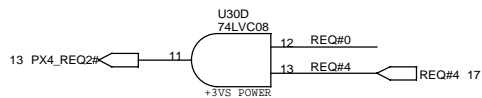
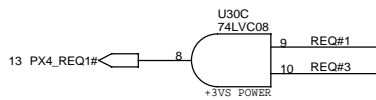
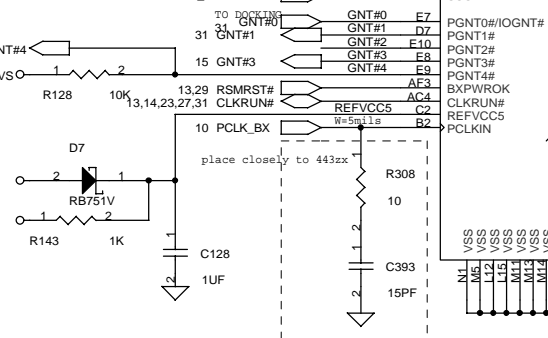
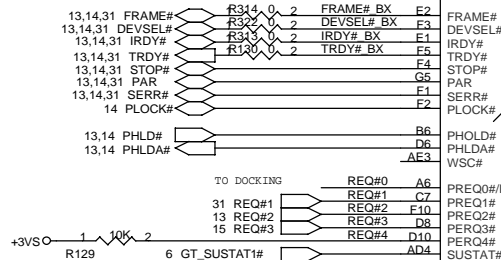
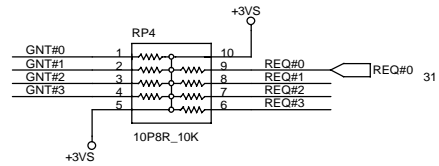
place closely to 443zx

Add by Charles at 5/20

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AD0	K6	AD0	VDD
AD1	K2	AD1	VDD
AD2	K4	AD2	VDD
AD3	K3	AD3	VDD
AD4	K5	AD4	VDD
AD5	J1	AD5	VDD
AD6	J2	AD6	VDD
AD7	H2	AD7	VDD
AD8	H1	AD8	VDD
AD9	J5	AD9	VDD
AD10	H3	AD10	VDD
AD11	H5	AD11	VDD
AD12	H4	AD12	VDD
AD13	G1	AD13	VDD
AD14	G2	AD14	VDD
AD15	G4	AD15	VDD
AD16	D1	AD16	VDD
AD17	D3	AD17	VDD
AD18	D2	AD18	VDD
AD19	C1	AD19	VDD
AD20	A2	AD20	VDD
AD21	C3	AD21	VDD
AD22	B3	AD22	VDD
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AD26	D5	AD26	VDD
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AD28	B5	AD28	VDD
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AD30	E6	AD30	VDD
AD31	C6	AD31	VDD

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C/BE#1	G3	C/BE#1	F3
C/BE#2	F4	C/BE#2	E1
C/BE#3	C4	C/BE#3	E5
FRAME#	E2	FRAME#	E2
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IRDY#	E1	IRDY#	E1
TRDY#	F5	TRDY#	F5
STOP#	F4	STOP#	F4
PAR	G5	PAR	G5
SERR#	F1	SERR#	F1
PLOCK#	E2	PLOCK#	E2
PHOLD#	B6	PHOLD#	B6
PHLDA#	D6	PHLDA#	D6
WSC#	AE3	WSC#	AE3
REQ#0	A6	REQ#0	A6
REQ#1	C7	REQ#1	C7
REQ#2	F10	REQ#2	F10
REQ#3	D8	REQ#3	D8
PERQ#3	D10	PERQ#3	D10
SUSTAT#	A4	SUSTAT#	A4
PGNT0#	E7	PGNT0#	E7
PGNT1#	D7	PGNT1#	D7
PGNT2#	E10	PGNT2#	E10
PGNT3#	E8	PGNT3#	E8
PGNT4#	E9	PGNT4#	E9
CLKRUN#	E2	CLKRUN#	E2
PCLKIN	B2	PCLKIN	B2

PCI INTERFACE

PCI ARB & PWR MGT

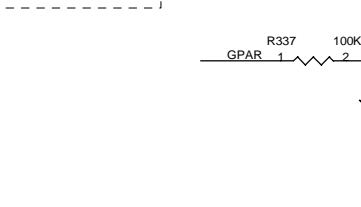
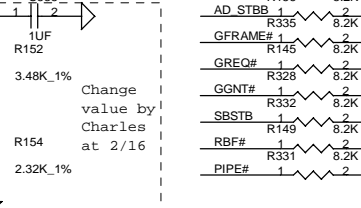
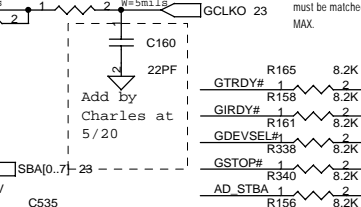
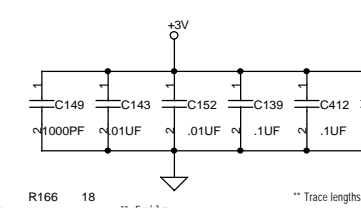
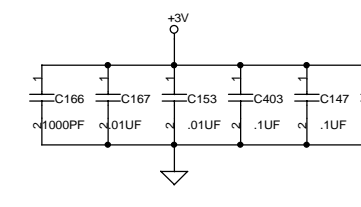
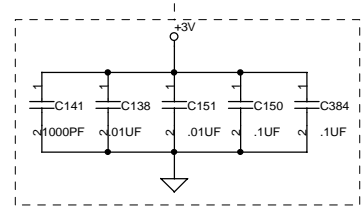
82443ZXM-100  
492 BGA

AGP INTERFACE

GAD0	AB5	GAD0	VDD
GAD1	K2	GAD1	VDD
GAD2	GAD3	GAD2	VDD
GAD3	AD1	GAD3	VDD
GAD4	AC3	GAD4	VDD
GAD5	AC3	GAD5	VDD
GAD6	AC1	GAD6	VDD
GAD7	AB4	GAD7	VDD
GAD8	AB1	GAD8	VDD
GAD9	AA5	GAD9	VDD
GAD10	AA3	GAD10	VDD
GAD11	AA4	GAD11	VDD
GAD12	AA2	GAD12	VDD
GAD13	AA1	GAD13	VDD
GAD14	Y5	GAD14	VDD
GAD15	Y3	GAD15	VDD
GAD16	W1	GAD16	VDD
GAD17	V2	GAD17	VDD
GAD18	W2	GAD18	VDD
GAD19	LJ5	GAD19	VDD
GAD20	V1	GAD20	VDD
GAD21	LJ4	GAD21	VDD
GAD22	LJ3	GAD22	VDD
GAD23	LJ1	GAD23	VDD
GAD24	T3	GAD24	VDD
GAD25	T4	GAD25	VDD
GAD26	T2	GAD26	VDD
GAD27	T1	GAD27	VDD
GAD28	LJ6	GAD28	VDD
GAD29	R3	GAD29	VDD
GAD30	R4	GAD30	VDD
GAD31	R2	GAD31	VDD

GC/BE#0	AB2	GC/BE#0	23
GC/BE#1	Y4	GC/BE#1	23
GC/BE#2	V4	GC/BE#2	23
GC/BE#3	LJ2	GC/BE#3	23
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GTRDY#	W4	GTRDY#	23
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GPAR	Y2	GPAR	23
GREQ#	L5	GREQ#	23
GGNT#	L3	GGNT#	23
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GCLKIN	N5	GCLKIN	23
PIPE#	M3	PIPE#	23
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SBA5	P3	SBA5	23
SBA6	R1	SBA6	23
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ST2	L1	ST2	23
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AD_STBB	IT5	AD_STBB	23
SBSTB	N3	SBSTB	23
AGPREFV	N4	AGPREFV	23

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VSS	M2	VSS	VSS
VSS	M3	VSS	VSS
VSS	M4	VSS	VSS
VSS	M5	VSS	VSS
VSS	M6	VSS	VSS
VSS	M7	VSS	VSS
VSS	M8	VSS	VSS
VSS	M9	VSS	VSS
VSS	M10	VSS	VSS
VSS	M11	VSS	VSS
VSS	M12	VSS	VSS
VSS	M13	VSS	VSS
VSS	M14	VSS	VSS
VSS	M15	VSS	VSS
VSS	M16	VSS	VSS
VSS	M17	VSS	VSS
VSS	M18	VSS	VSS
VSS	M19	VSS	VSS
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VSS	M37	VSS	VSS
VSS	M38	VSS	VSS
VSS	M39	VSS	VSS
VSS	M40	VSS	VSS
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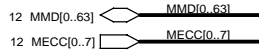
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Size: B, Document Number: 401138, Rev: 4C

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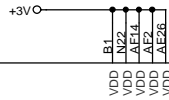


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MMD18	W23	MD18
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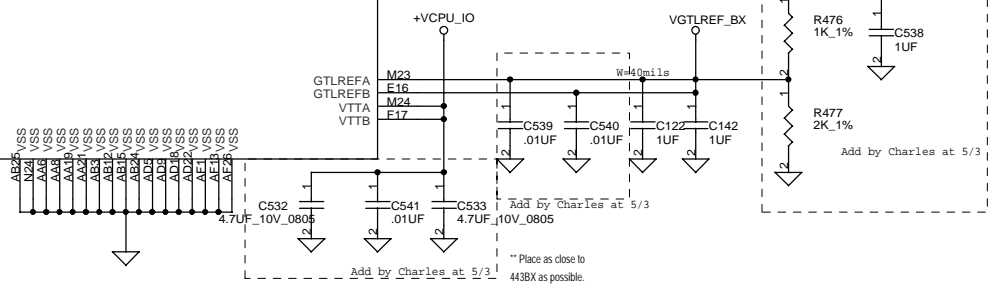
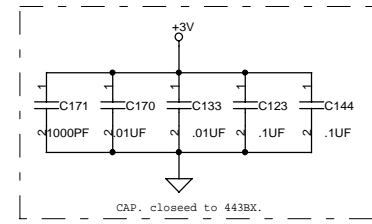
82443ZXM-100  
492 BGA

MEMORY DATA BUS

HOST DATA BUS



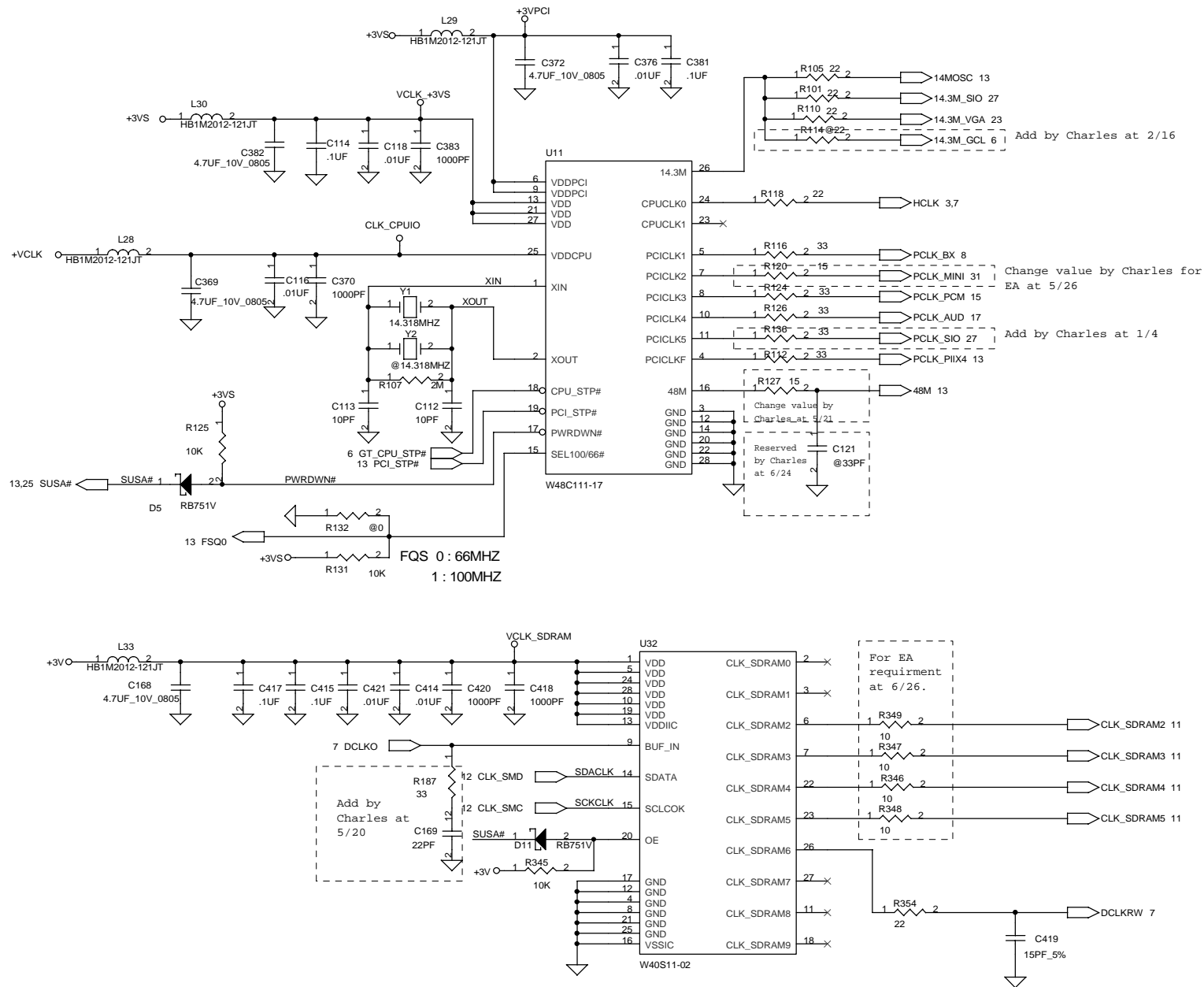
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HD#6	A21	HD6
HD#7	C20	HD7
HD#8	B21	HD8
HD#9	E20	HD9
HD#10	A20	HD10
HD#11	E19	HD11
HD#12	B20	HD12
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HD#62	A8	HD62
HD#63	B9	HD63



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# CLOCK GENERATOR & BUFFER



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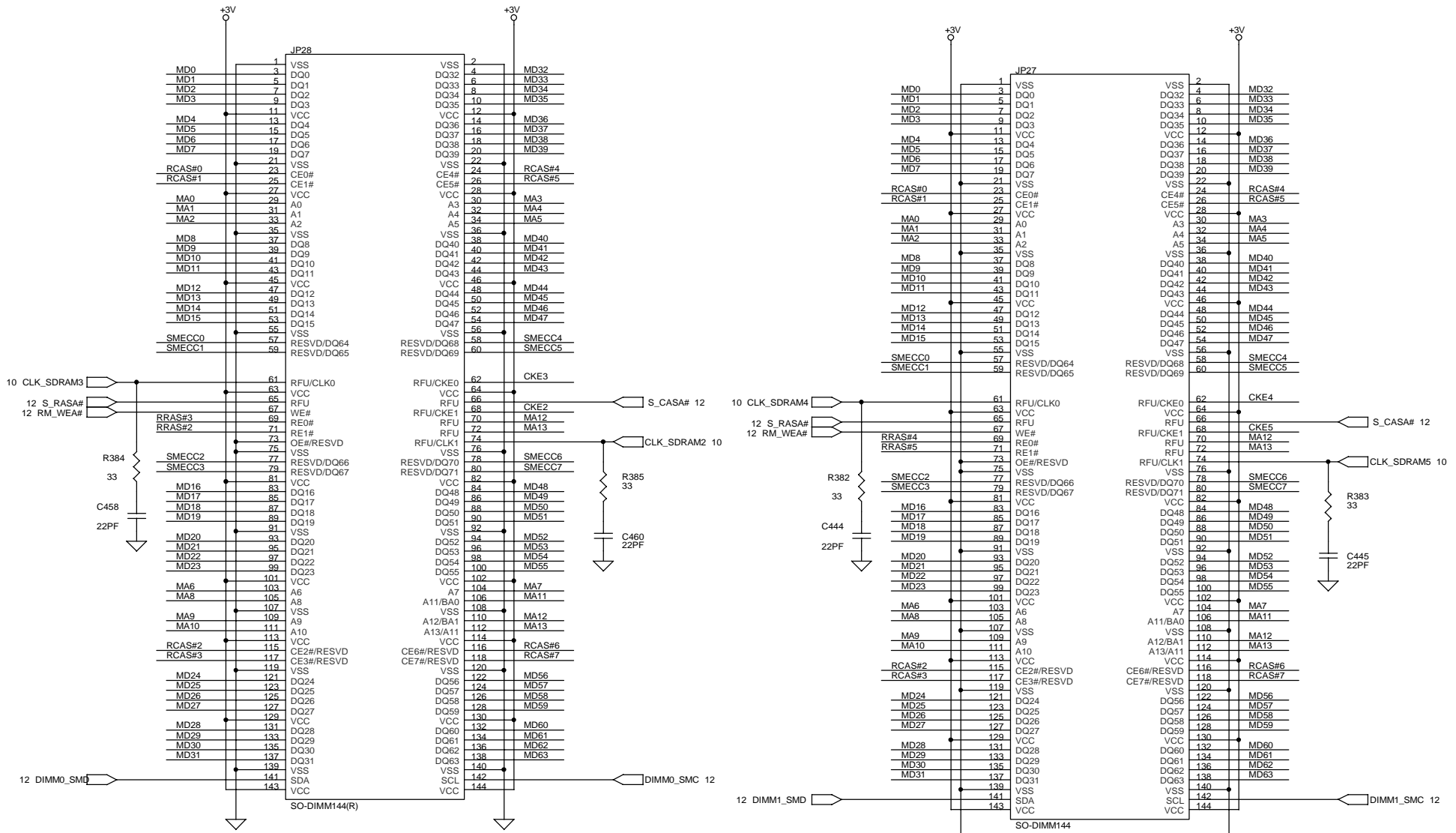
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# SO-DIM 144 PINS RAM MODULE CONN.



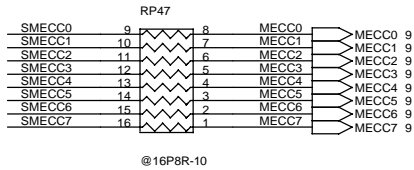
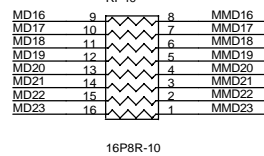
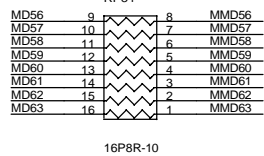
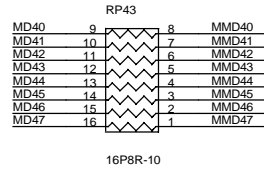
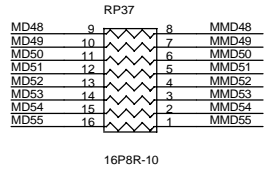
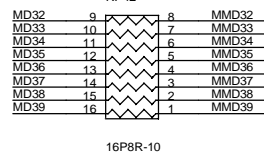
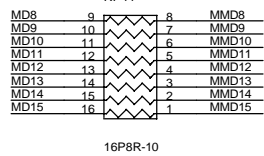
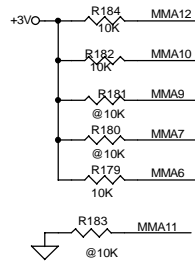
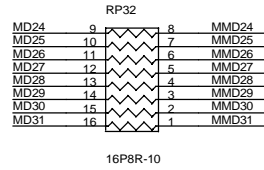
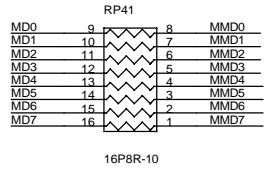
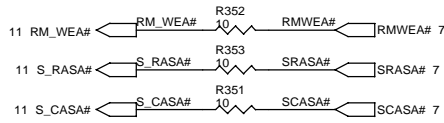
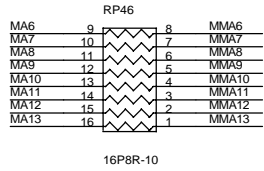
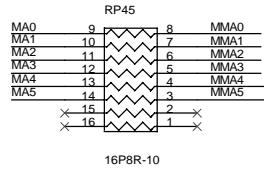
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- 12 MD[0..63]  $\leftarrow$  MMD[0..63]
- 12 MA[0..13]  $\leftarrow$  MA[0..13]
- 7 RRAS#[2..5]  $\leftarrow$  RRAS#[2..5]
- 7 CKE[2..5]  $\leftarrow$  CKE[2..5]
- 12 SMECC[0..7]  $\leftarrow$  SMECC[0..7]

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# SO-DIM 144 PINS RAM MODULE CONN.

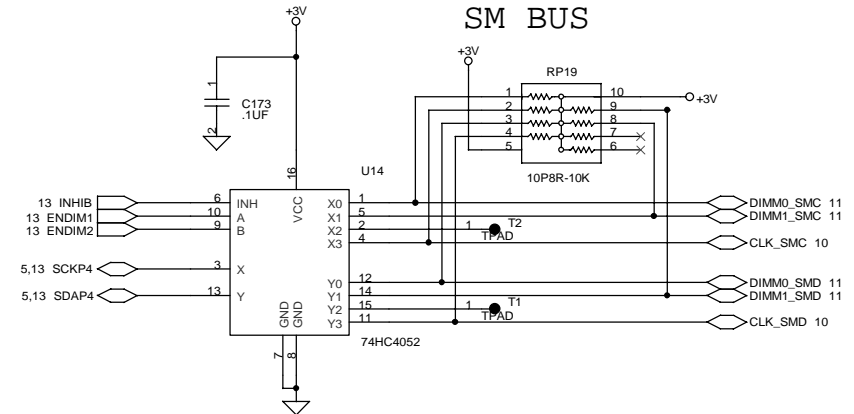
Charles add new Damping resistor for address bus and control signals at 6/21



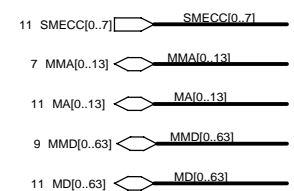
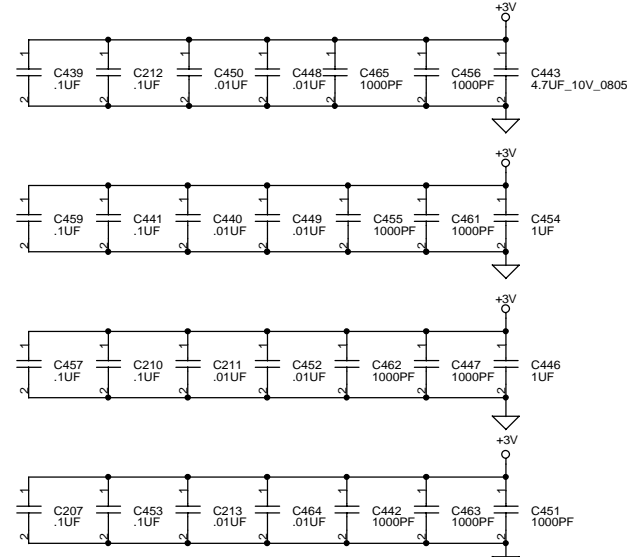
RP47 change to be no load. 2/16

Placement near to 440ZXM

## SM BUS



Pin Name	Function	Low	High	Int. Res. 50K
MMA12	Host Freq. Select	66MHz	100MHz	Pulldown
MMA11	In-Order Queue Depth Enable	1 No Pipe-line	4 Max	Pullup
MMA10	Quick Start Select	Stop Clock Mode	Quick Start Mode	Pulldown
MMA9	AGP	Enable	Disable	Pulldown
MMA7	MM Config	Normal Oper.	Tri-states certain Memory signal	Pulldown
MMA6	Host Bus Buffer Mode Select	Desktop GTL+	Mobile Low Power GTL+	Pulldown



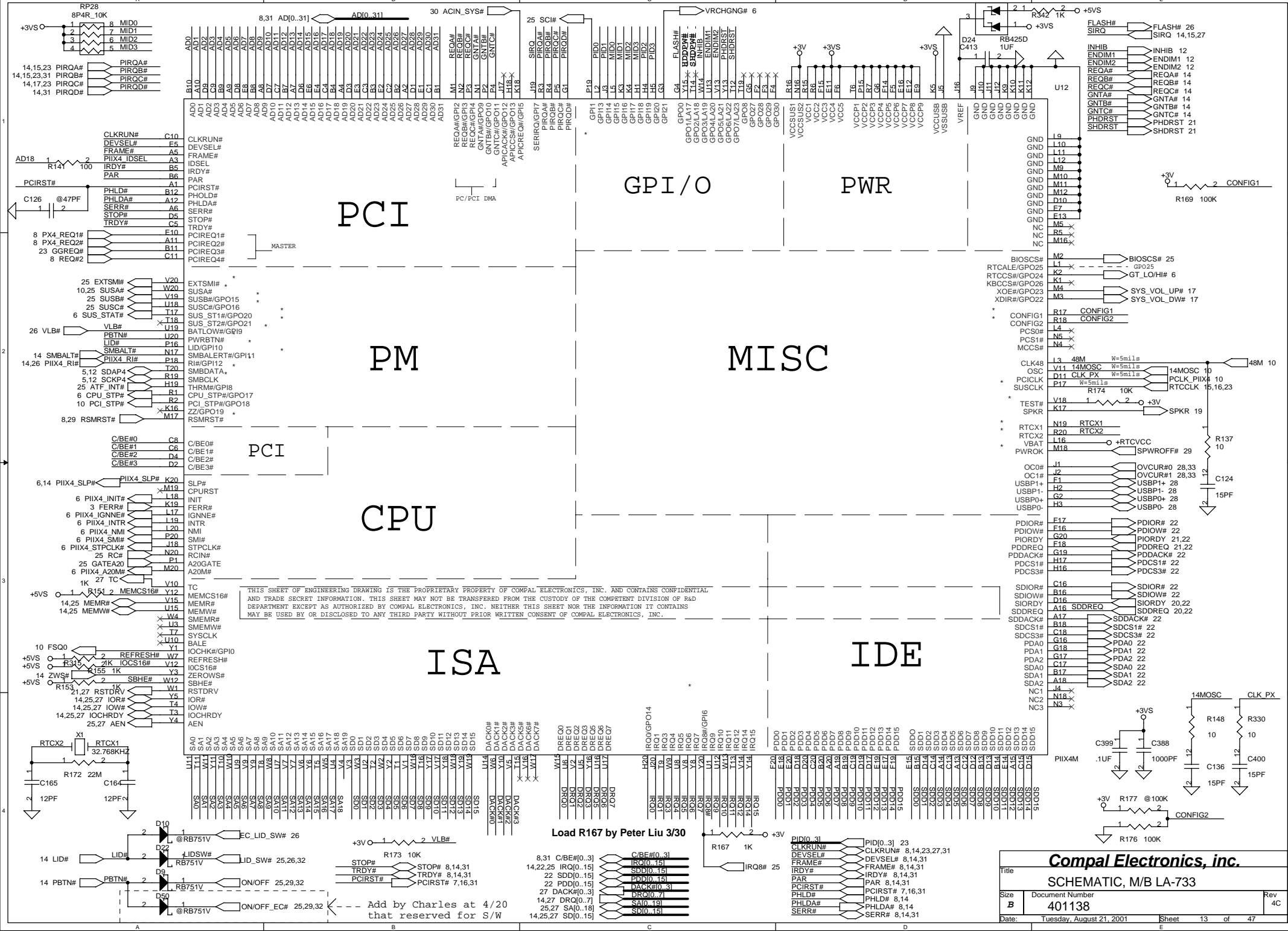
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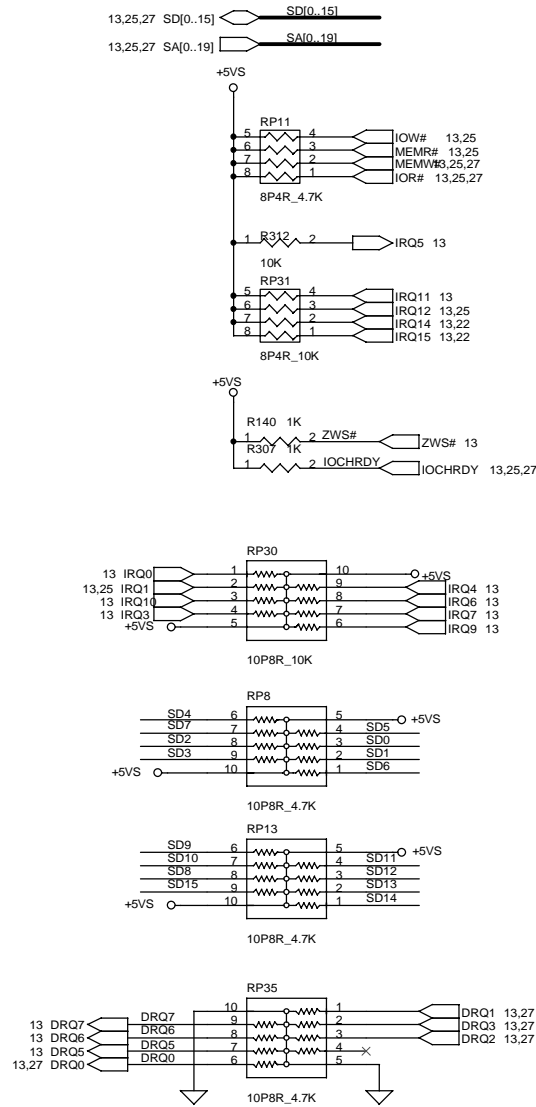
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Load R167 by Peter Liu 3/30

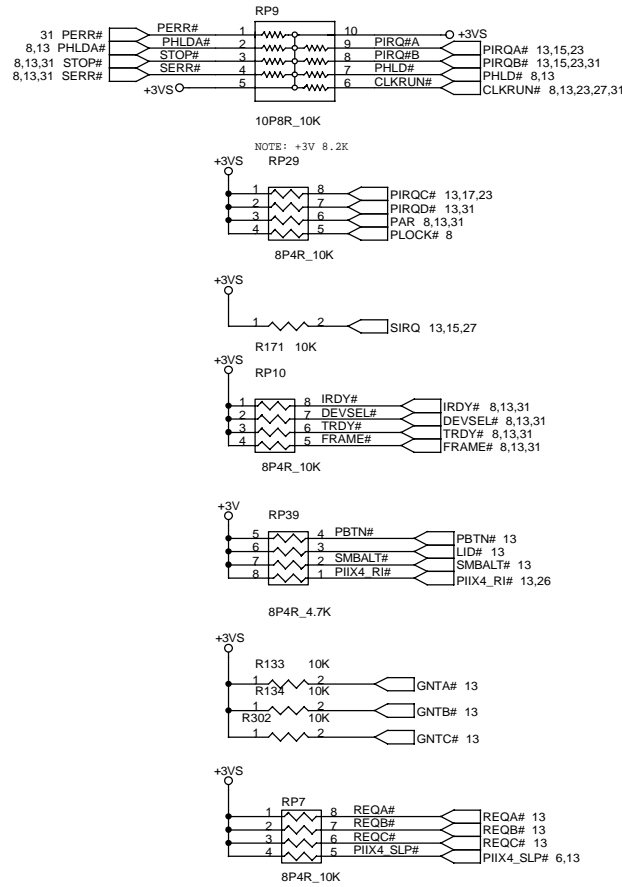
Add by Charles at 4/20 that reserved for S/W

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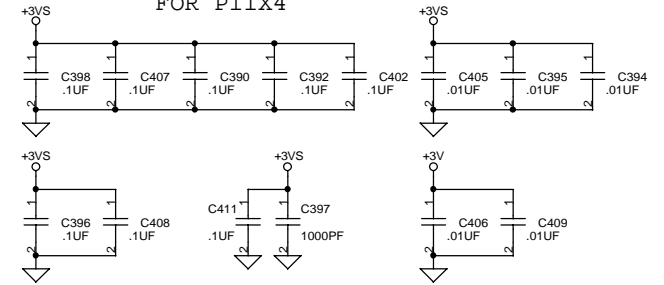
# ISA BUS Pull-up



# PCI BUS Pull-up



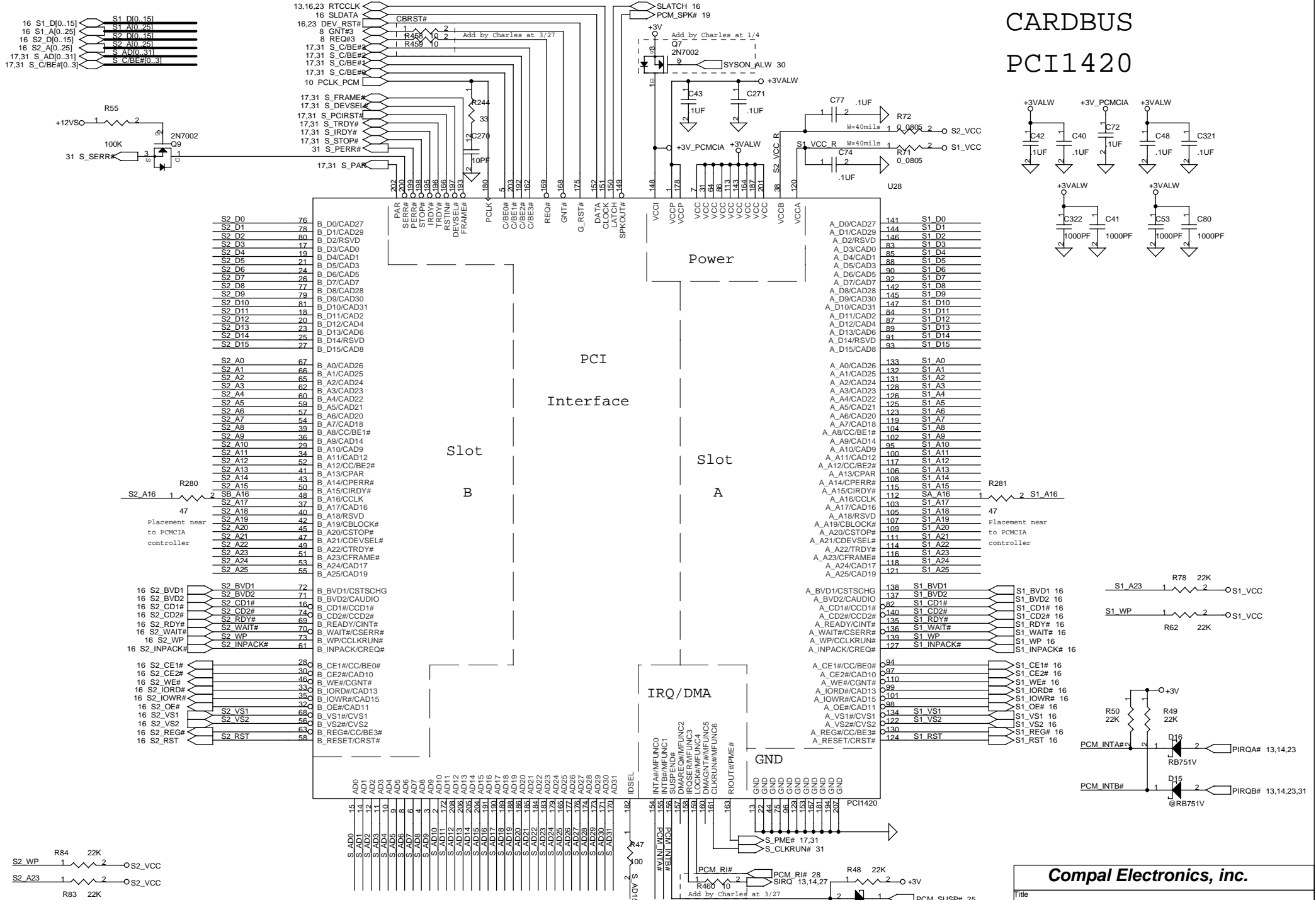
# FOR PIIX4



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# CARDBUS PCI1420



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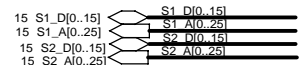
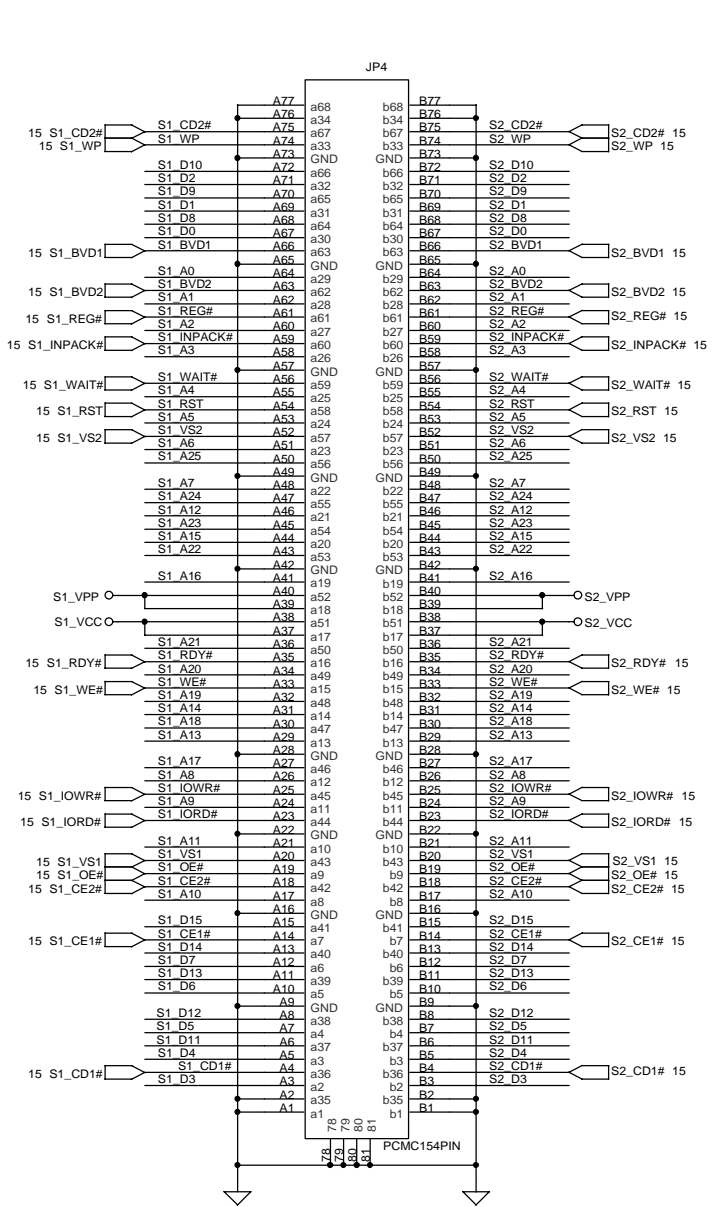
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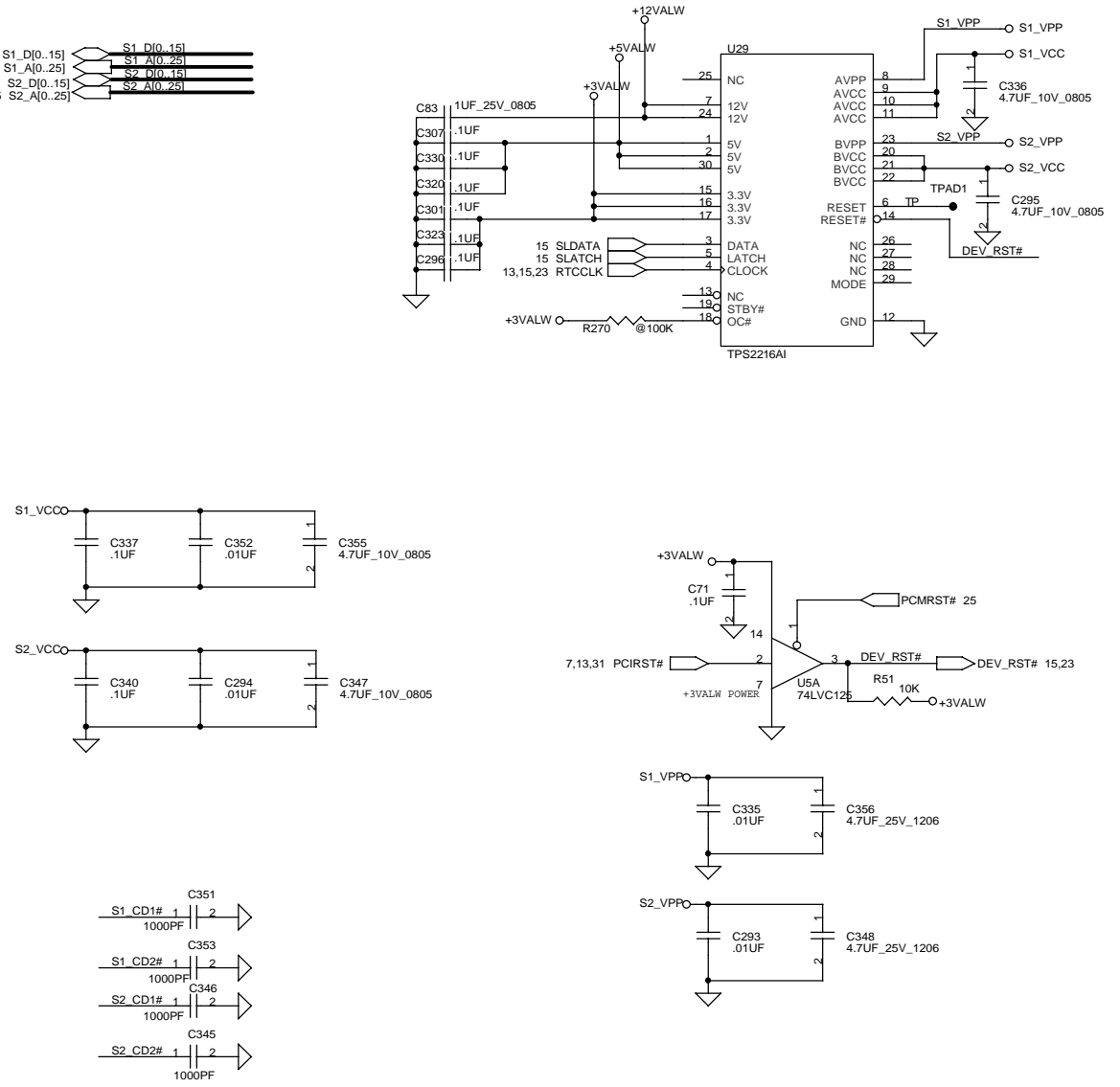
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# CARDBUS

# SOCKET



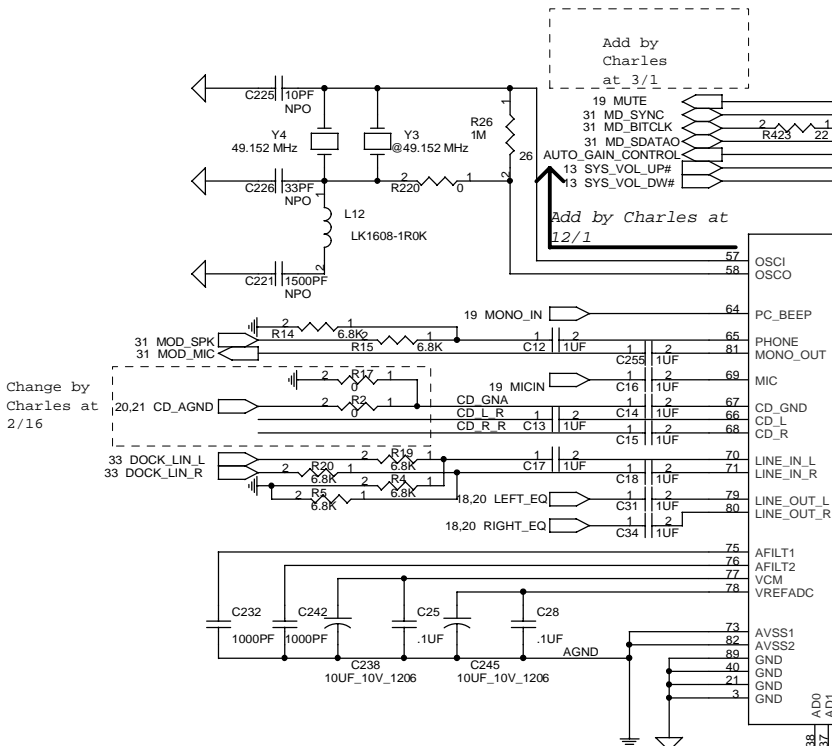
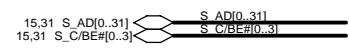
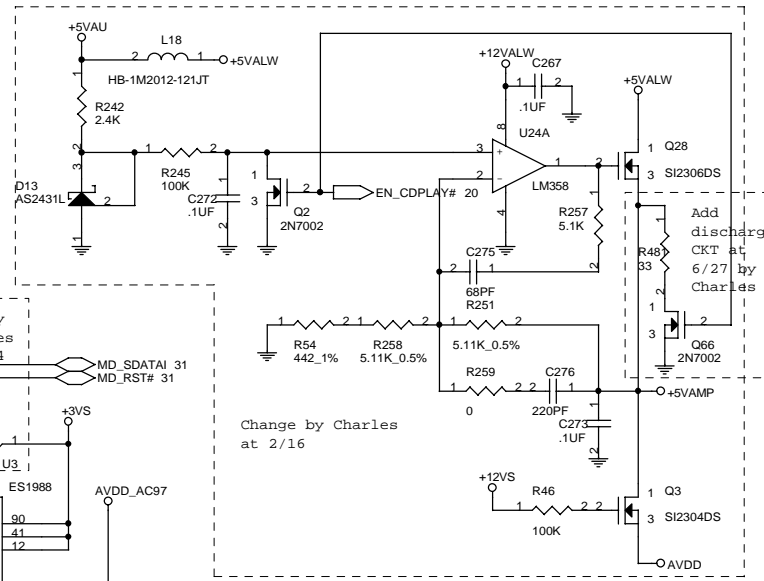
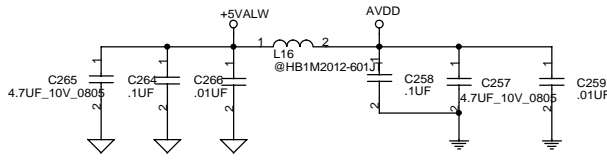
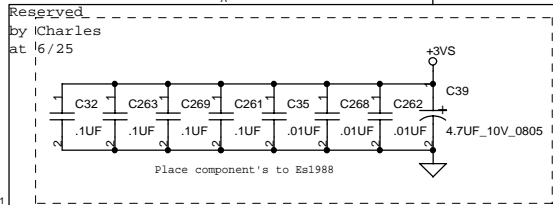
# PCMCIA POWER CTRL.



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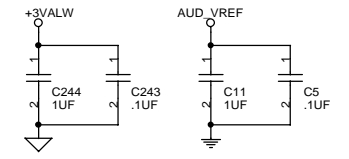
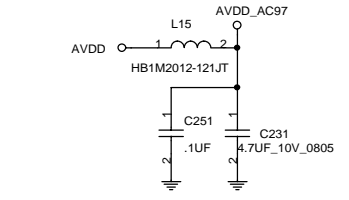
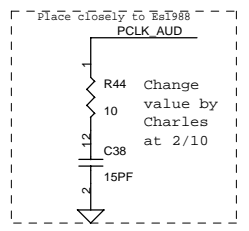
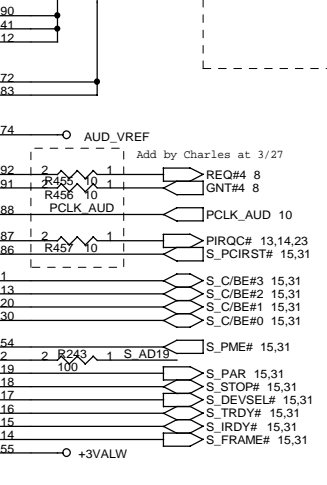
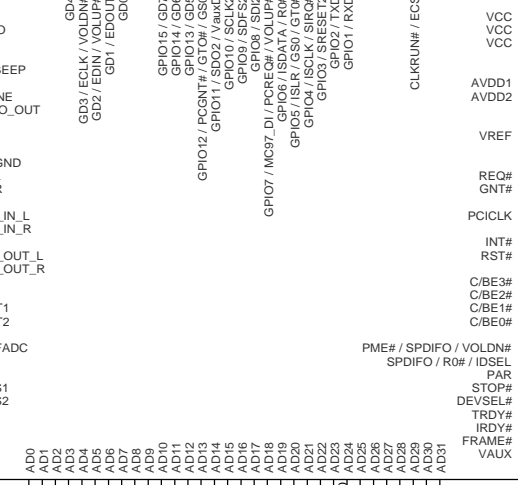
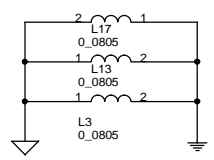
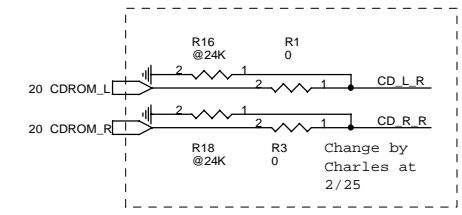


Delete for D3 cold

Add by Charles at 1/4

Change by Charles at 2/16

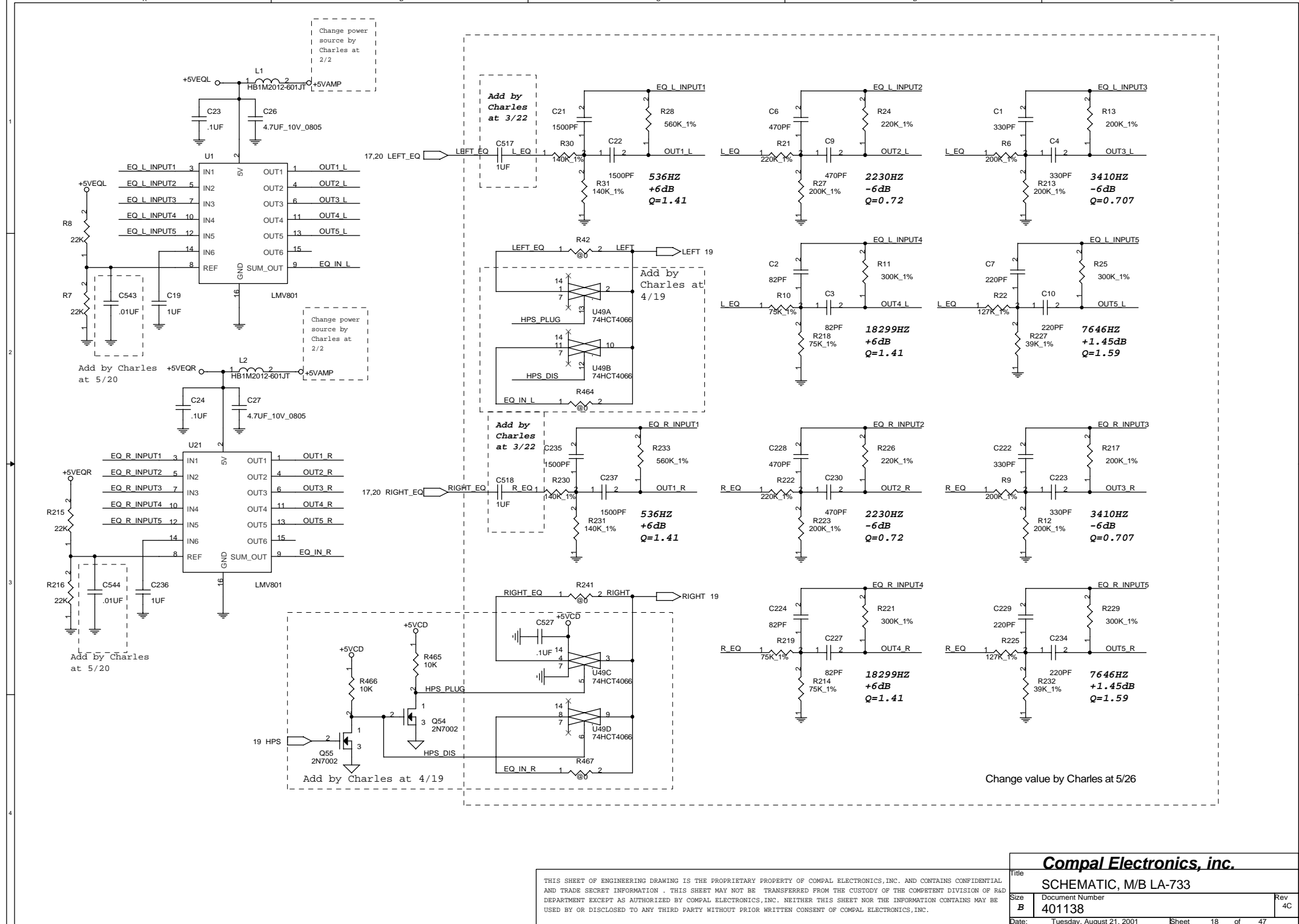
Add by Charles at 3/27



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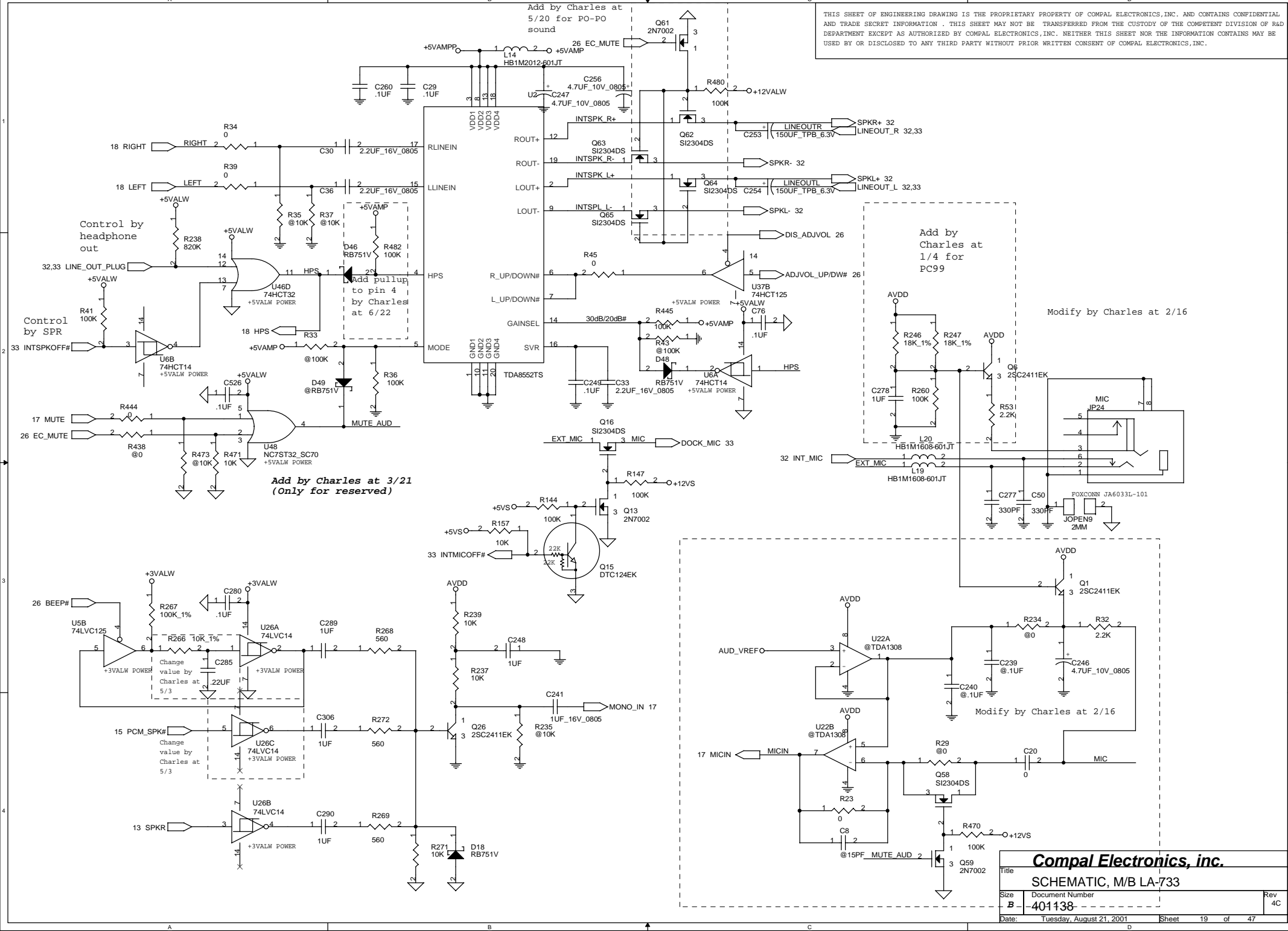


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Add by Charles at 5/20 for PO-PO sound

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Add by Charles at 1/4 for PC99

Modify by Charles at 2/16

Add by Charles at 3/21 (Only for reserved)

Modify by Charles at 2/16

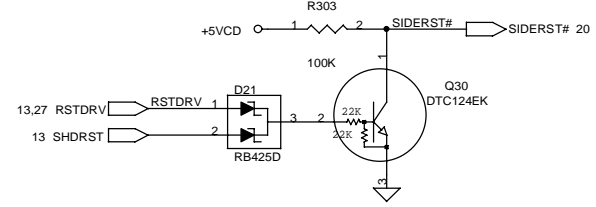
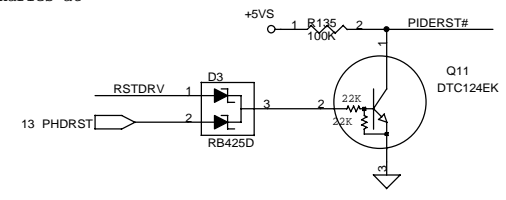
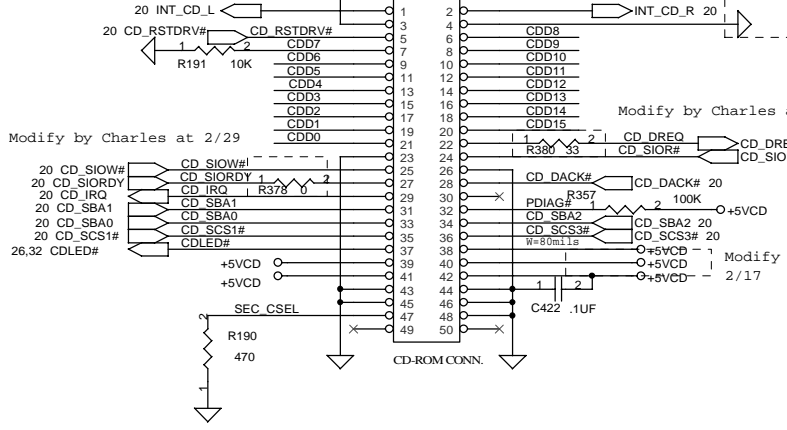
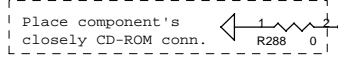
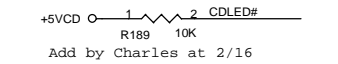
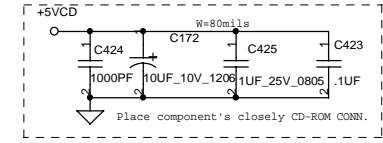
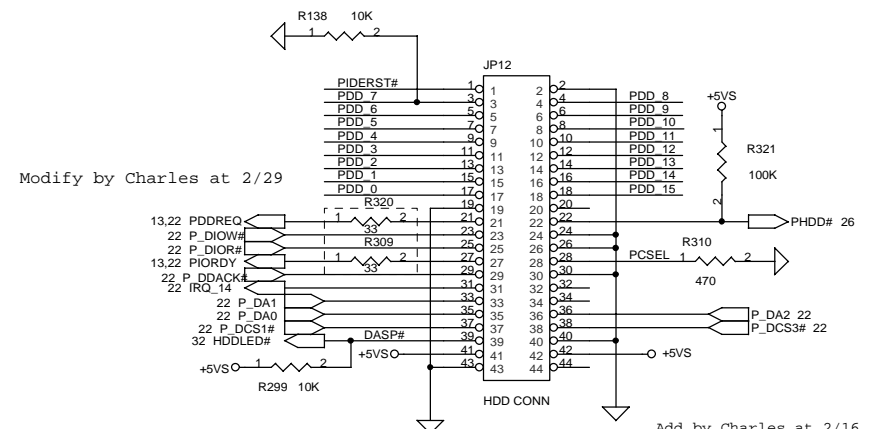
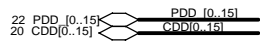
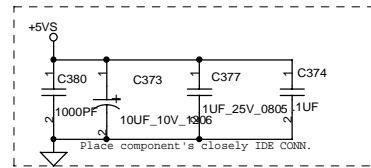
**Compal Electronics, inc.**

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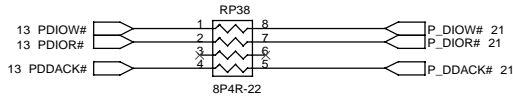
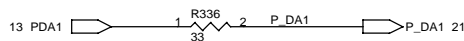
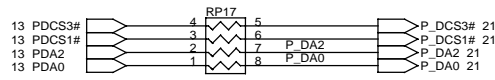
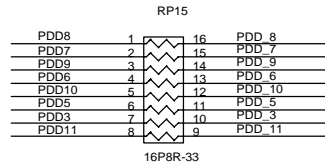
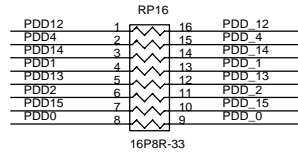
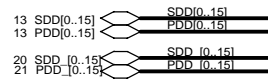
# IDE, CD-ROM & FDD Module CONN.



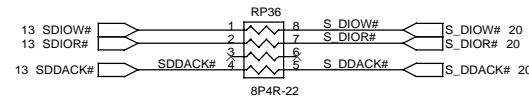
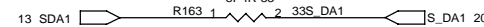
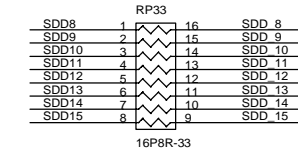
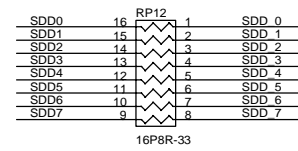
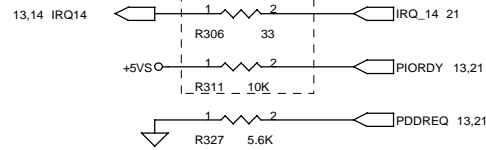
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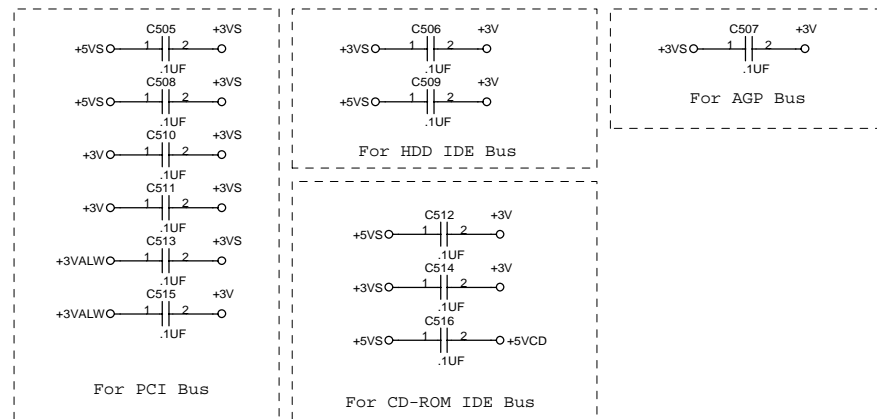
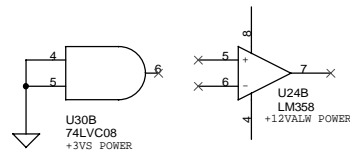
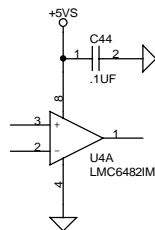
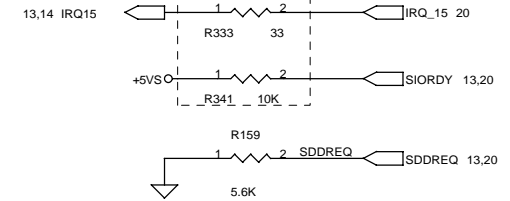
**IDE Series Resistor**  
Place them close PIIX4M



Modify by Charles at 2/29



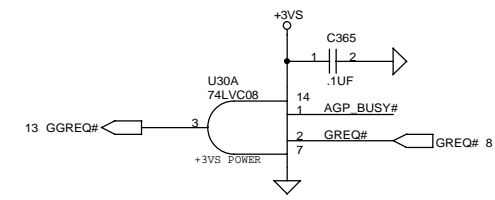
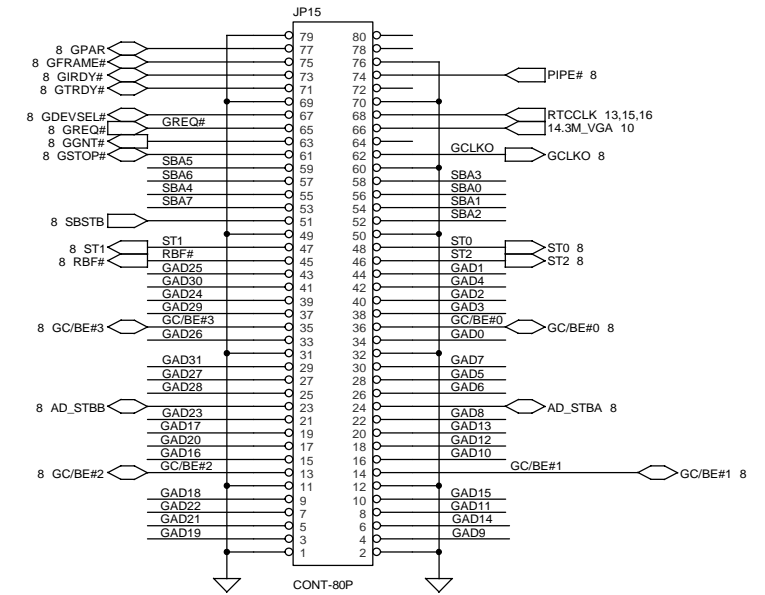
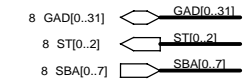
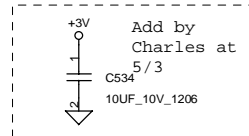
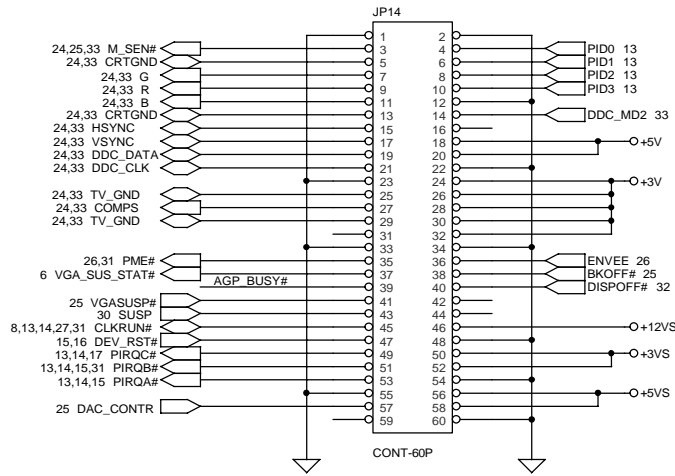
Modify by Charles at 2/29



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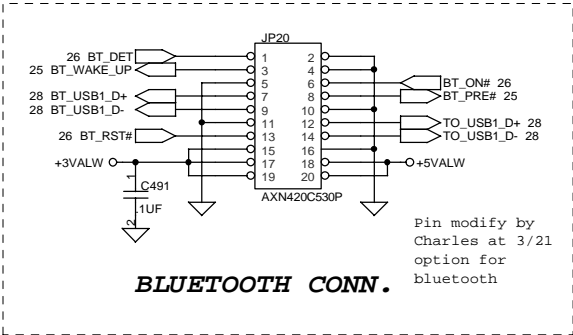
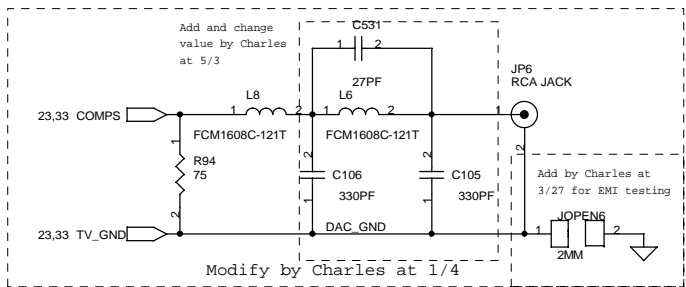
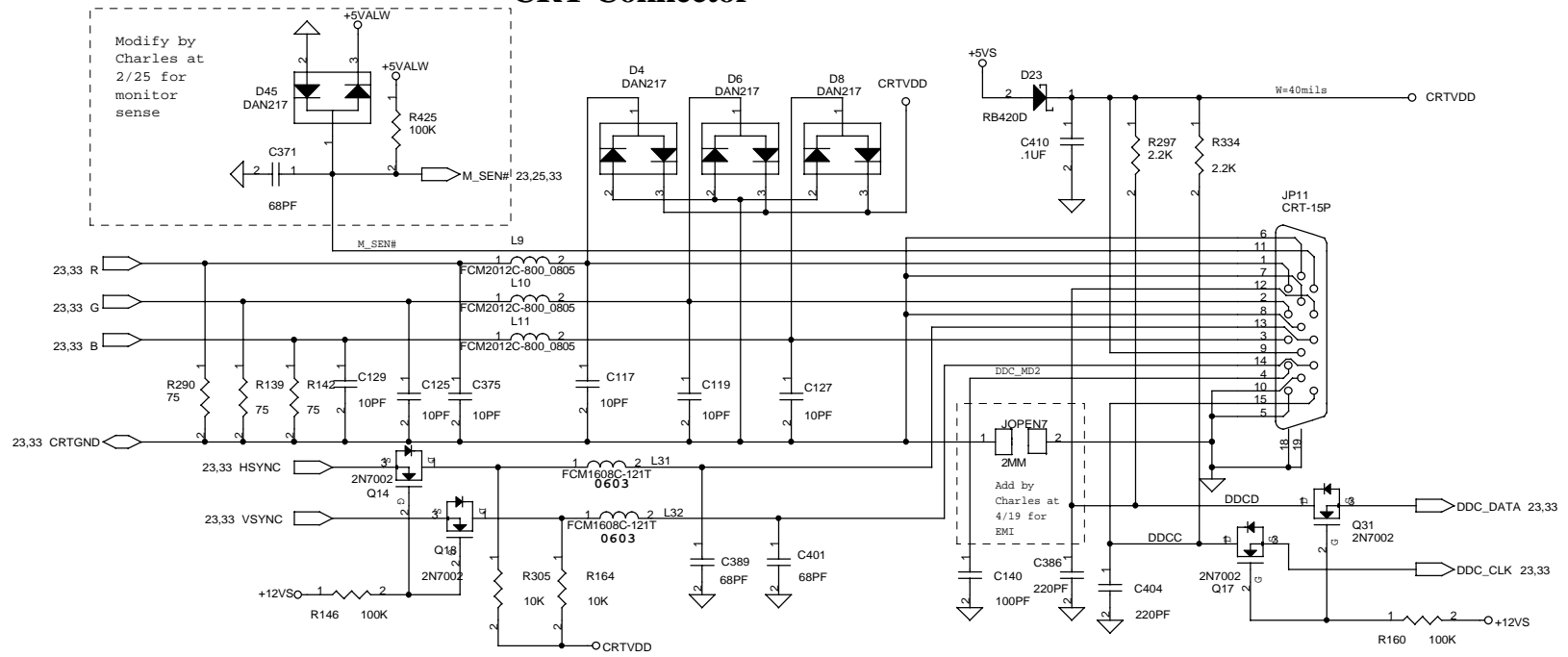
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# CRT Connector



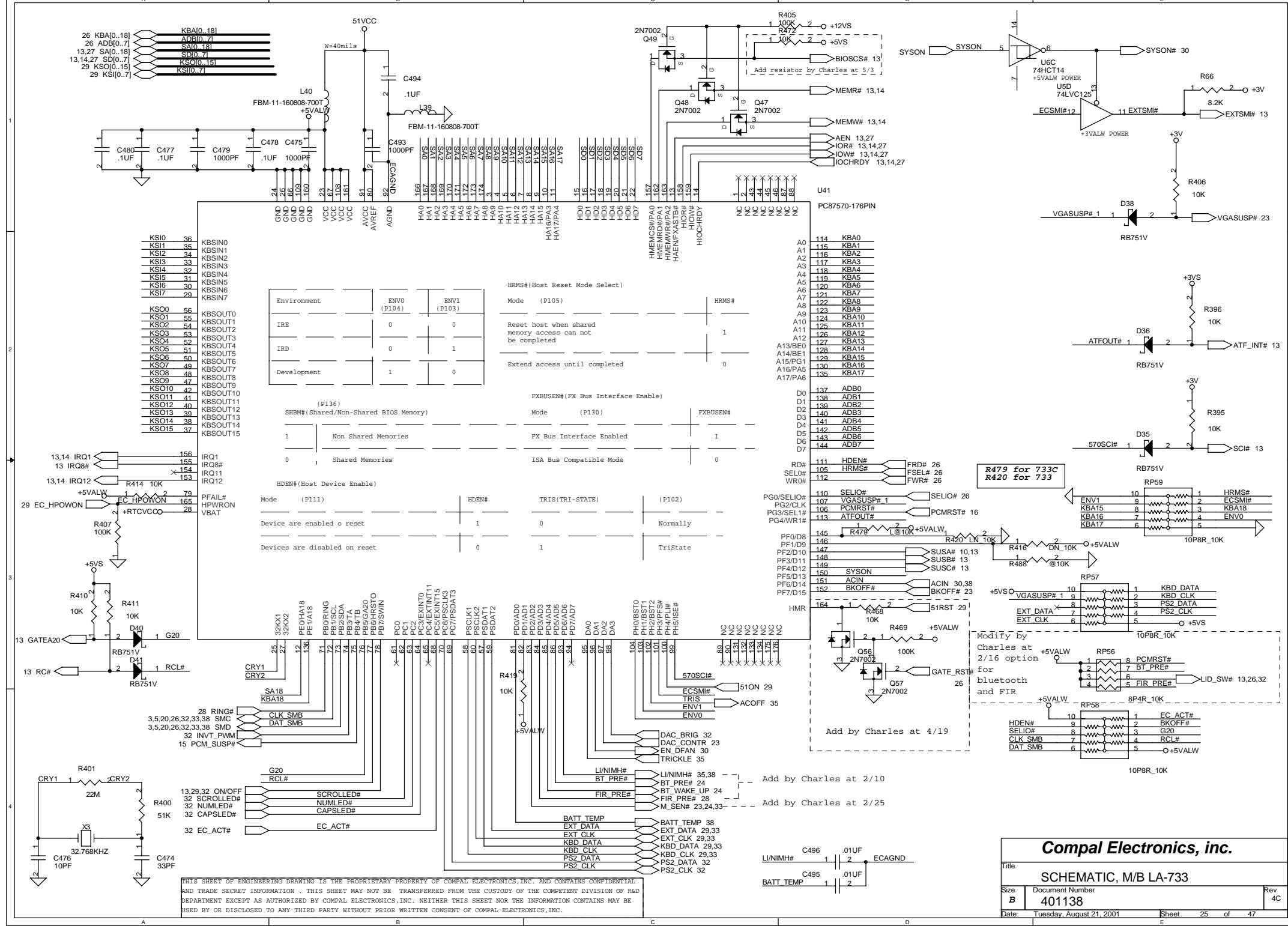
**Compal Electronics, inc.**

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KSI0	36	KBSIN0
KSI1	35	KBSIN1
KSI2	34	KBSIN2
KSI3	33	KBSIN3
KSI4	32	KBSIN4
KSI5	31	KBSIN5
KSI6	30	KBSIN6
KSI7	29	KBSIN7
KSO0	56	KBSOUT0
KSO1	55	KBSOUT1
KSO2	54	KBSOUT2
KSO3	53	KBSOUT3
KSO4	52	KBSOUT4
KSO5	51	KBSOUT5
KSO6	50	KBSOUT6
KSO7	49	KBSOUT7
KSO8	48	KBSOUT8
KSO9	47	KBSOUT9
KSO10	46	KBSOUT10
KSO11	45	KBSOUT11
KSO12	44	KBSOUT12
KSO13	43	KBSOUT13
KSO14	42	KBSOUT14
KSO15	41	KBSOUT15

Environment	ENV0 (P104)	ENV1 (P103)	Mode (P105)	HRMS#
IRE	0	0	Reset host when shared memory access can not be completed	1
IRD	0	1	Extend access until completed	0
Development	1	0		

SHEM# (Shared/Non-Shared BIOS Memory)	Mode (P130)	FXBUSEN#
1 Non Shared Memories	FX Bus Interface Enabled	1
0 Shared Memories	ISA Bus Compatible Mode	0

Mode (P111)	HDEN#	TRIS (TRI-STATE) (P102)
Device are enabled o reset	1	0 Normally
Devices are disabled on reset	0	1 TriState

A0	114	KBA0
A1	115	KBA1
A2	116	KBA2
A3	117	KBA3
A4	118	KBA4
A5	119	KBA5
A6	120	KBA6
A7	121	KBA7
A8	122	KBA8
A9	123	KBA9
A10	124	KBA10
A11	125	KBA11
A12	126	KBA12
A13/BE0	127	KBA13
A14/BE1	128	KBA14
A15/PG1	129	KBA15
A16/PA5	130	KBA16
A17/PA6	135	KBA17
D0	137	ADB0
D1	138	ADB1
D2	139	ADB2
D3	140	ADB3
D4	141	ADB4
D5	142	ADB5
D6	143	ADB6
D7	144	ADB7
RD#	111	HDEN#
SEL0#	105	HRMS#
WR0#	112	FSEL# 26
		FWR# 26
PG0/SEL0#	110	SELIO# 26
PG2/CLK	107	VGASUSP# 1
PG3/SEL1#	106	PCMRST#
PG4/WR1#	113	ATFOUT#
PF0/D8	145	R479 L@10K +5VALW
PF1/D9	146	R420 LN 10K
PF2/D10	147	SUSA# 10,13
PF3/D11	148	SUSB# 13
PF4/D12	149	SYSON
PF5/D13	150	ACIN
PF6/D14	151	ACIN
PF7/D15	152	BKOFF# 23
HMR	164	R468 10K
		R469 +5VALW
		Q56 2N7002
		Q57 2N7002
		GATE_RST# 26
		570SCI# 13
		ECSMI# 12
		TRIS ENV1
		ACOFF# 35
		DAC_BRIG 32
		DAC_CONTR 23
		EN_DFN 30
		TRICKLE 35
		LI/NIMH#
		BT_PRE#
		LI/NIMH# 35,38
		BT_PRE# 24
		BT_WAKE_UP 24
		FIR_PRE# 28
		M_SEN# 23,24,33
		BATT_TEMP
		EXT_DATA 29,33
		EXT_CLK 29,33
		KBD_DATA 29,33
		KBD_CLK 29,33
		PS2_DATA 32
		PS2_CLK 32

R479 for 733C  
R420 for 733

Modify by Charles at 2/16 option for bluetooth and FIR

Add by Charles at 2/10

Add by Charles at 2/25

**Compal Electronics, inc.**

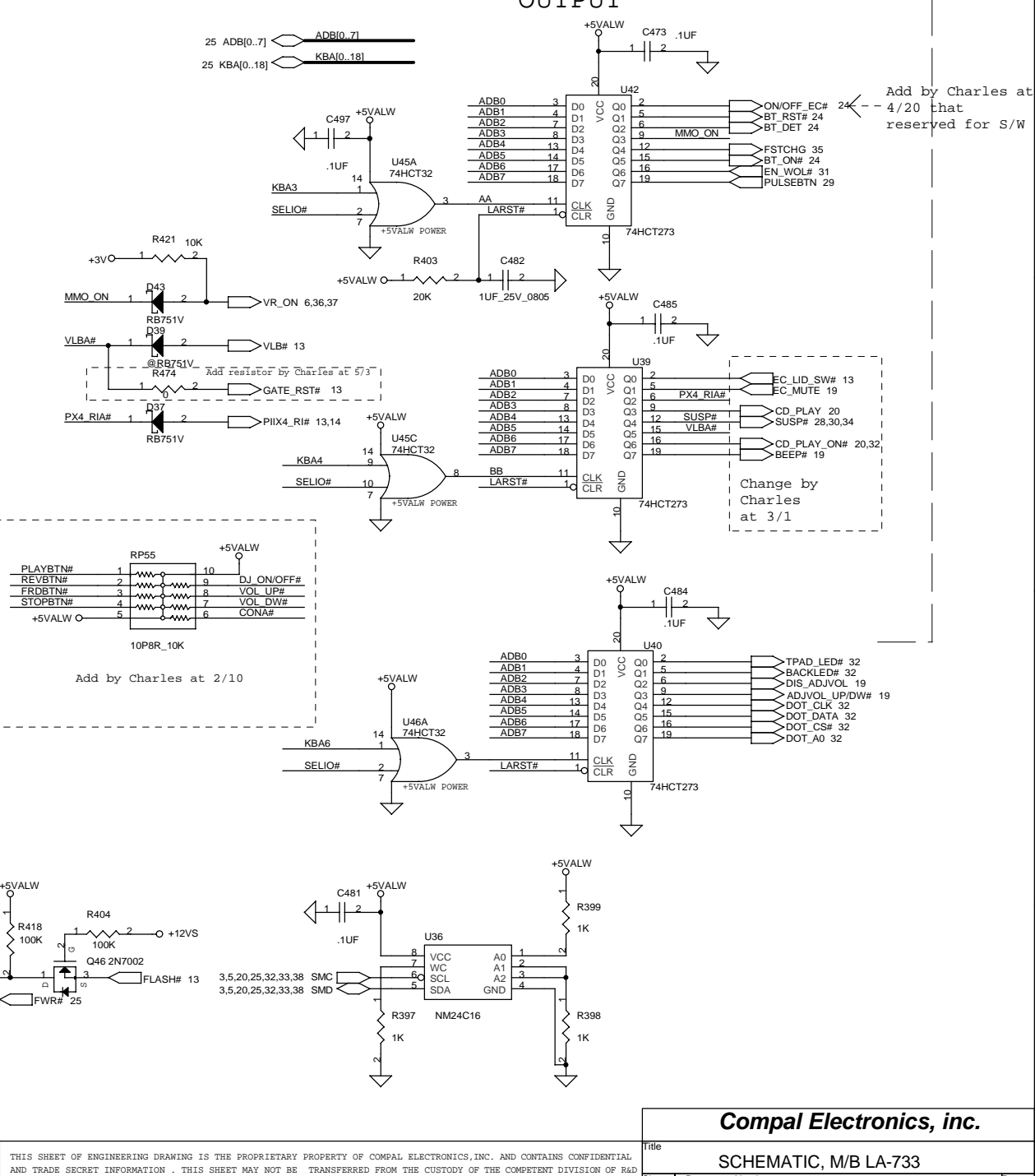
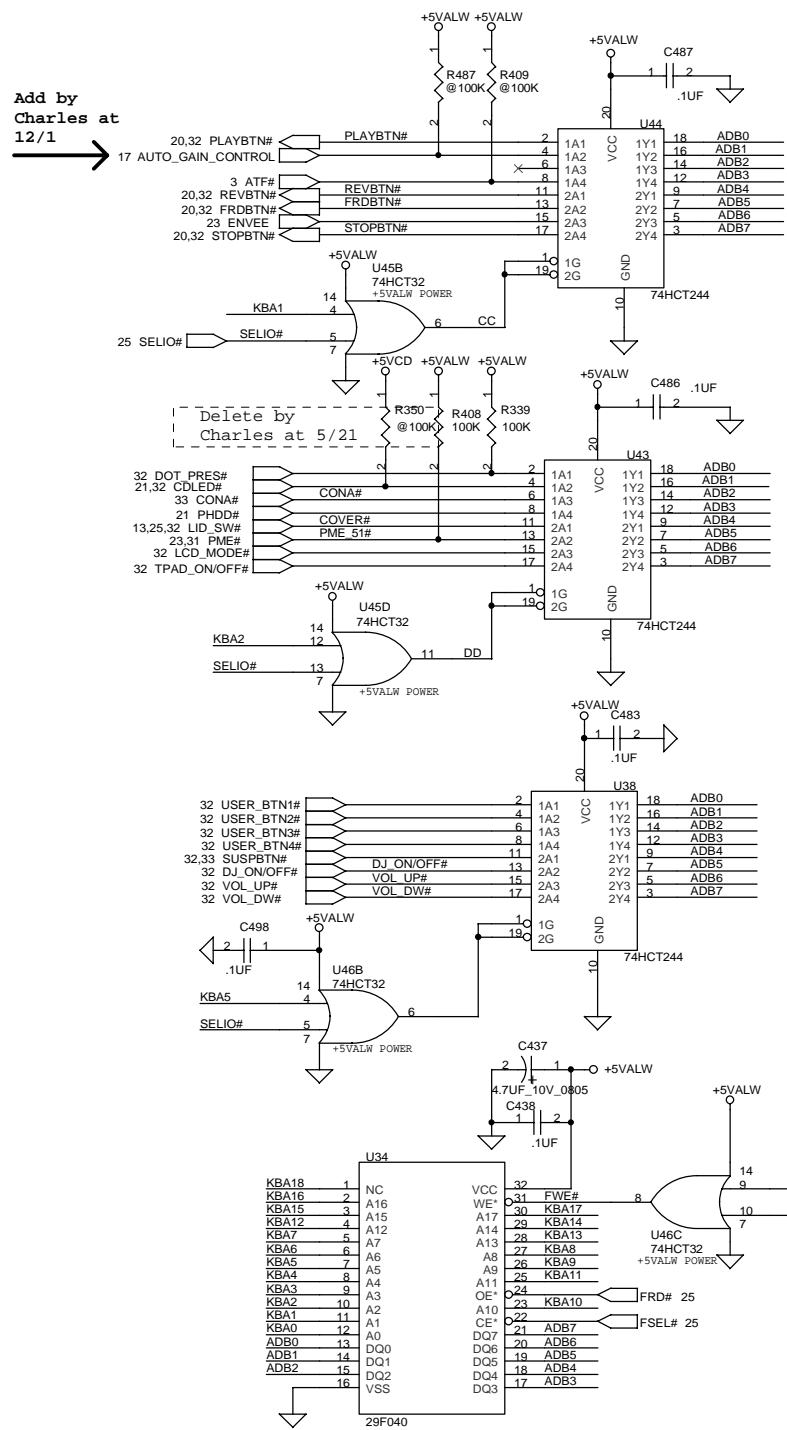
Title: SCHEMATIC, M/B LA-733

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- INPUT

OUTPUT

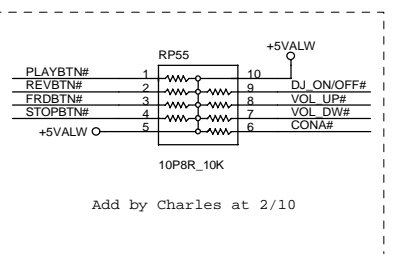


Add by Charles at 12/1

Add by Charles at 4/20 that reserved for S/W

Delete by Charles at 5/21

Change by Charles at 3/1

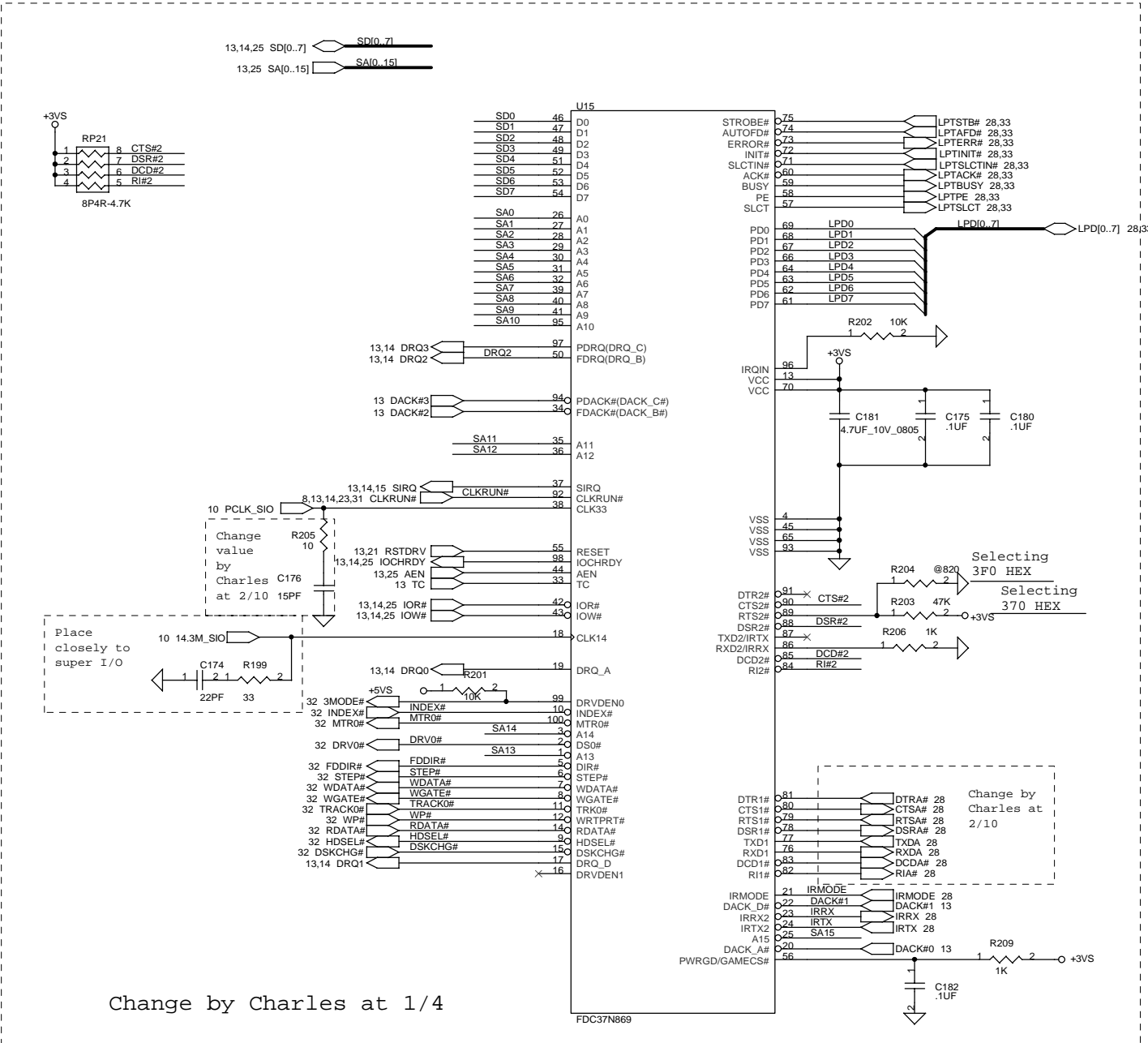


Add by Charles at 2/10

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# SUPER I/O 37N869



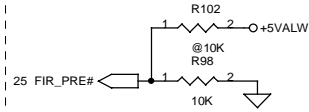
Change by Charles at 1/4

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# SERIAL / PARALLEL PORT FIR / USB CONNECTOR

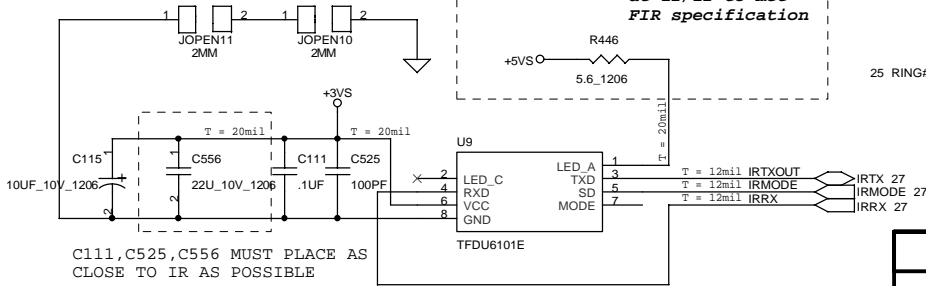
Change by Charles at 5/20



+5VS FOR INCREASING LED'S  
LIGHT AND THE COMMUNICATION  
DISTANCE

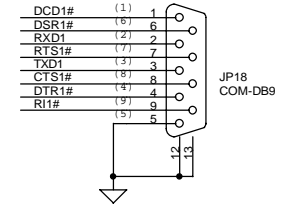
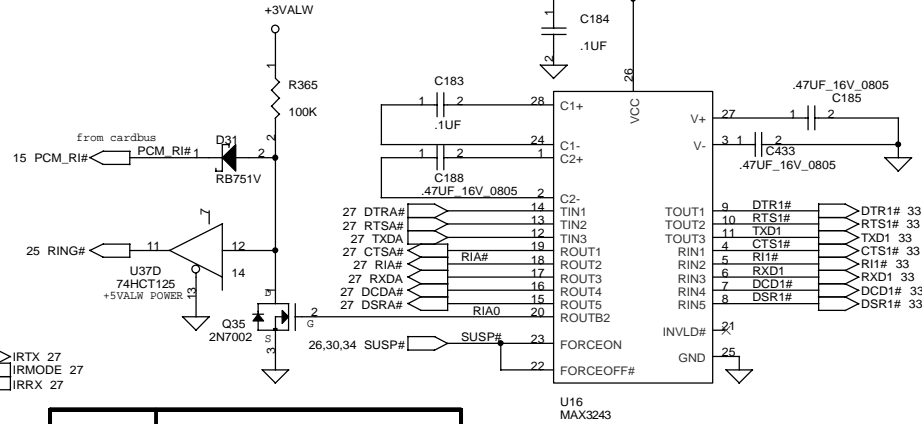
## FIR Module

Change by Charles  
at 12/12 to met  
FIR specification

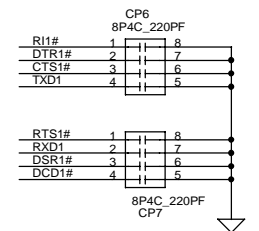


C111, C525, C556 MUST PLACE AS  
CLOSE TO IR AS POSSIBLE

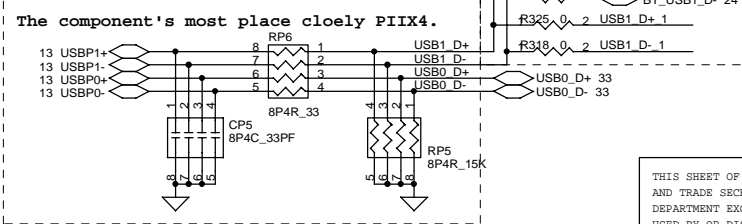
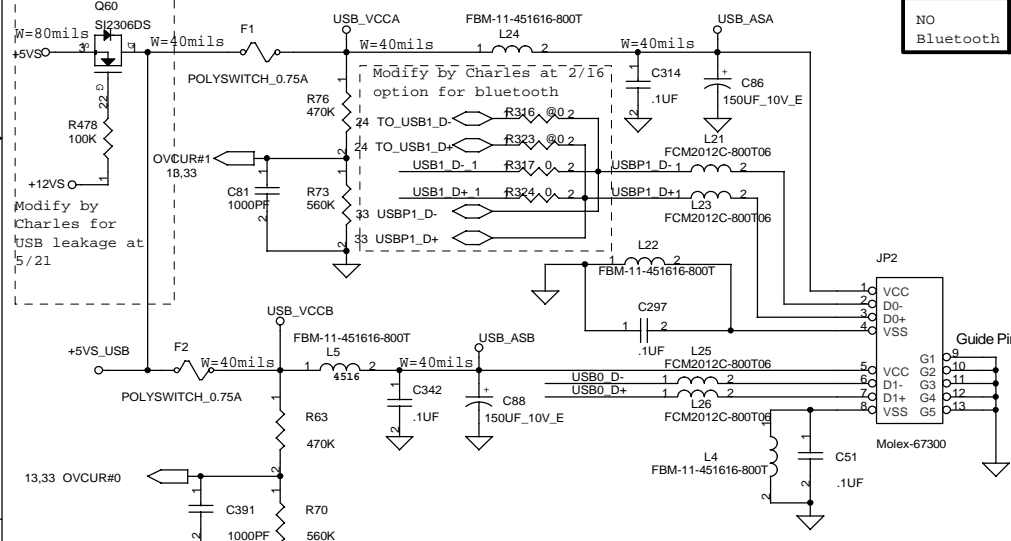
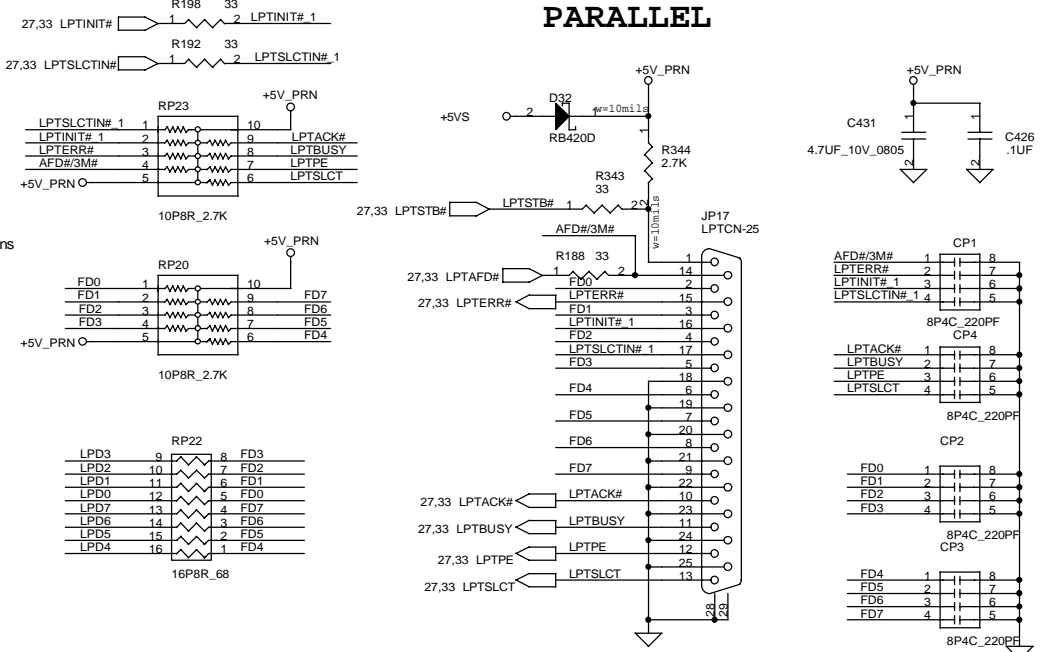
## SERIAL



Resistor Location	
Bluetooth	R316, R323, R326, R319
NO Bluetooth	R317, R324, R325, R318



## PARALLEL



The component's most place cloely PIIX4.

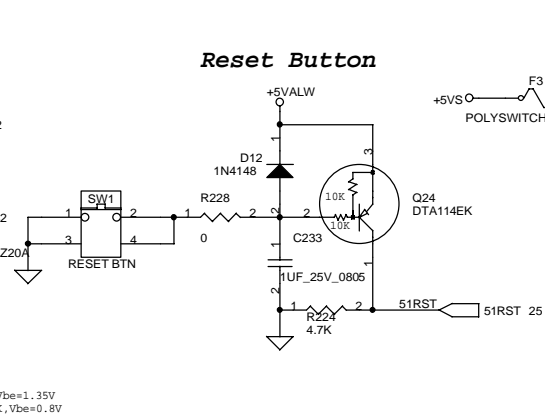
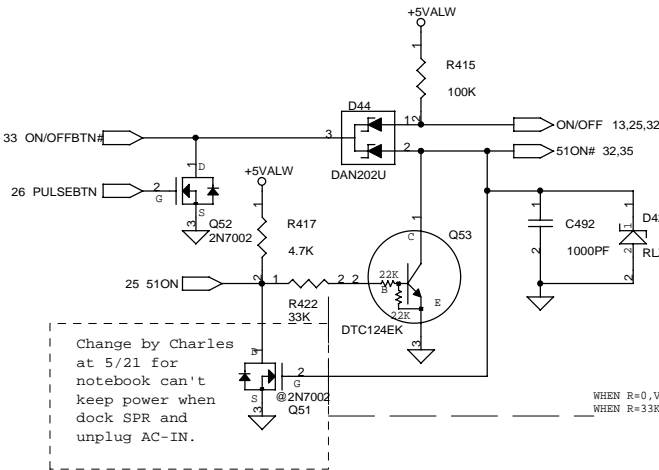
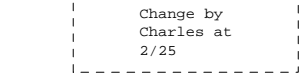
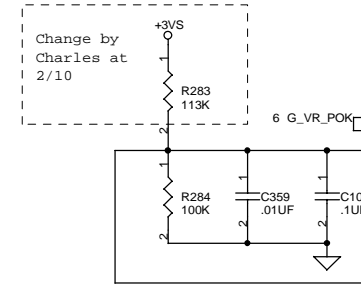
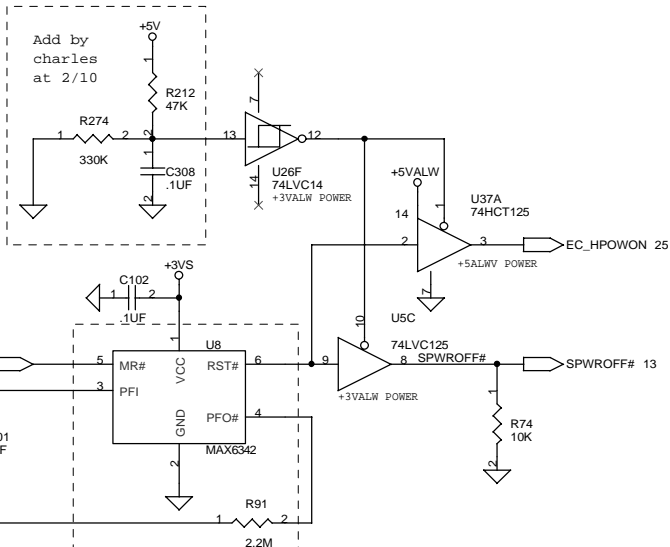
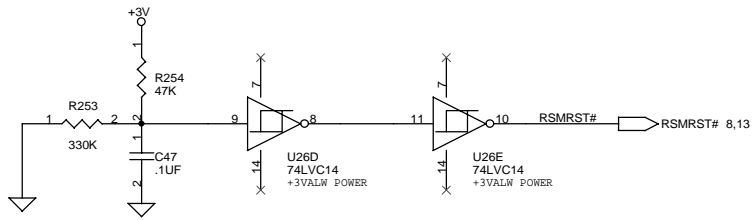
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Size: B Document Number: 401138 Rev: 4C

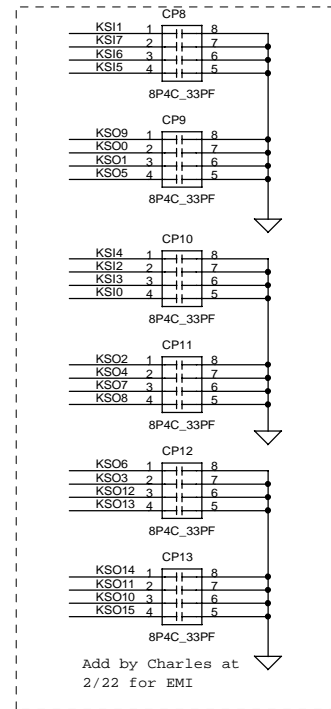
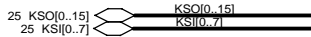
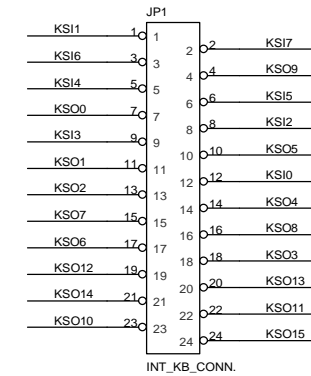
Date: Tuesday, August 21, 2001 Sheet: 28 of 47



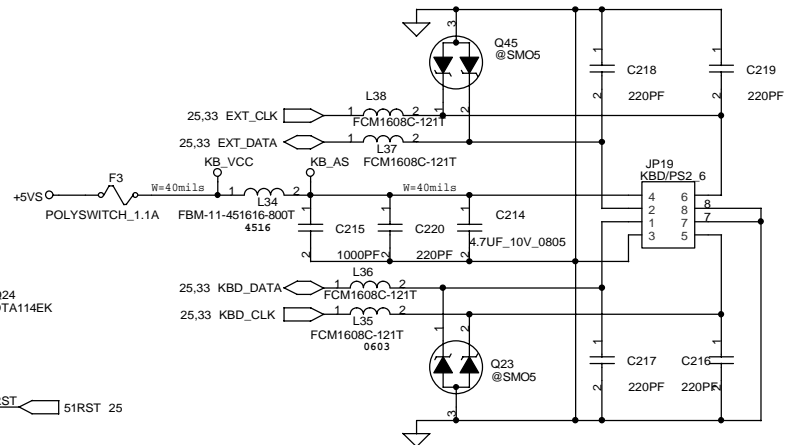
**Reset Button**

WHEN R=0, Vbe=1.35V  
WHEN R=33K, Vbe=0.8V

**INT\_KBD CONN.**



**PS2 CONN.**

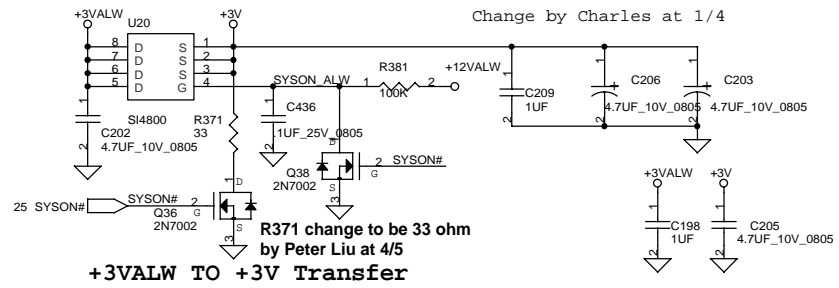


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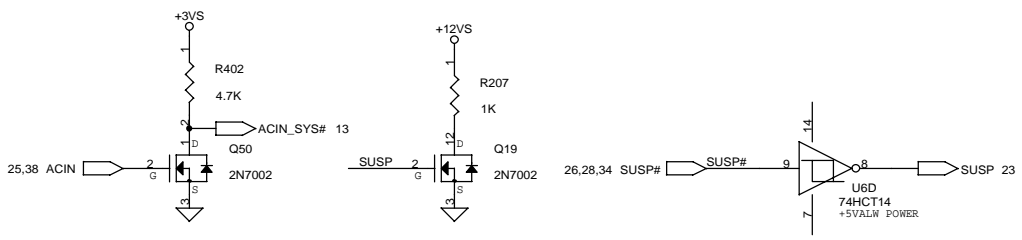
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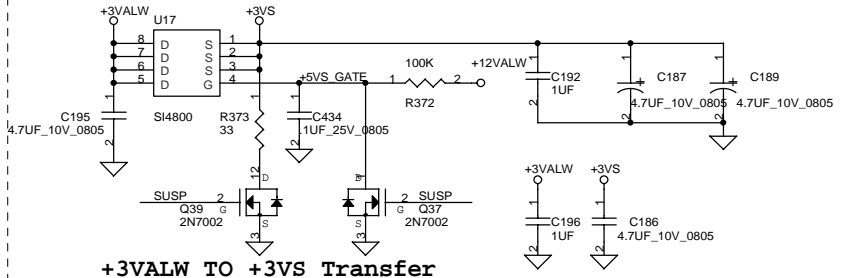
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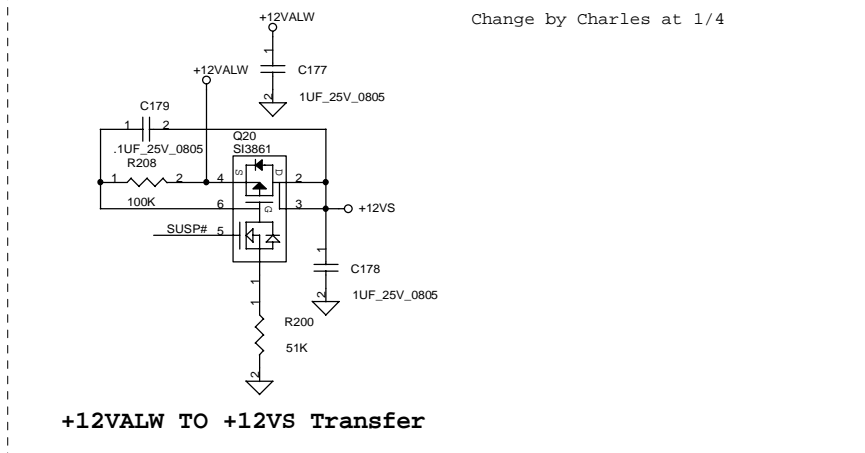
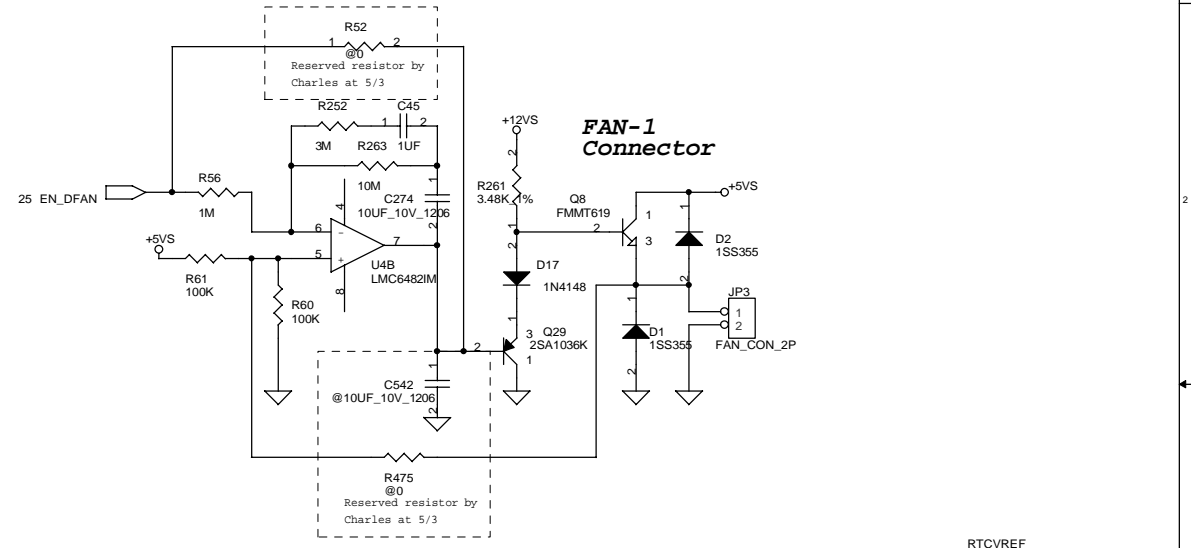
**+3VALW TO +3V Transfer**



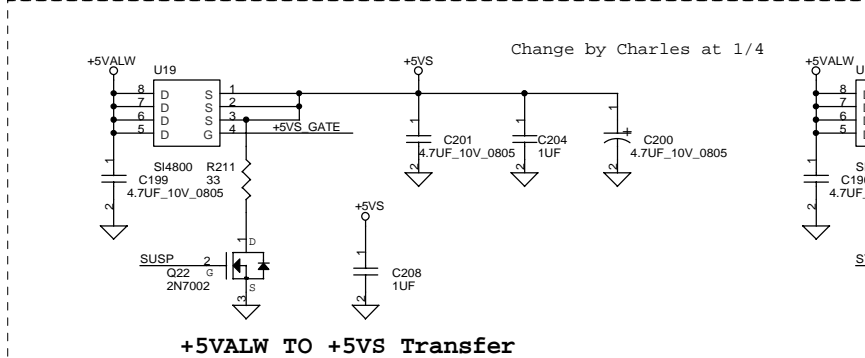
**RESET & SUSPEND CKT**



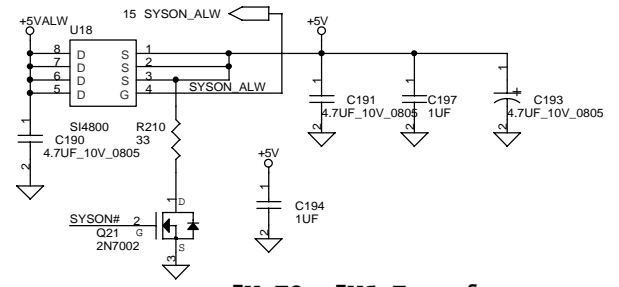
**+3VALW TO +3VS Transfer**



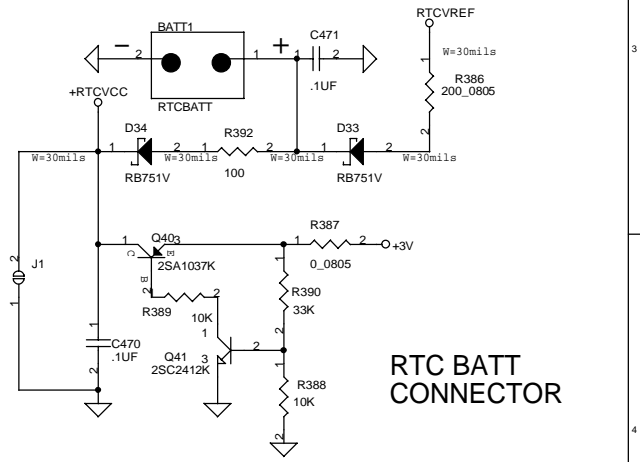
**+12VALW TO +12VS Transfer**



**+5VALW TO +5VS Transfer**



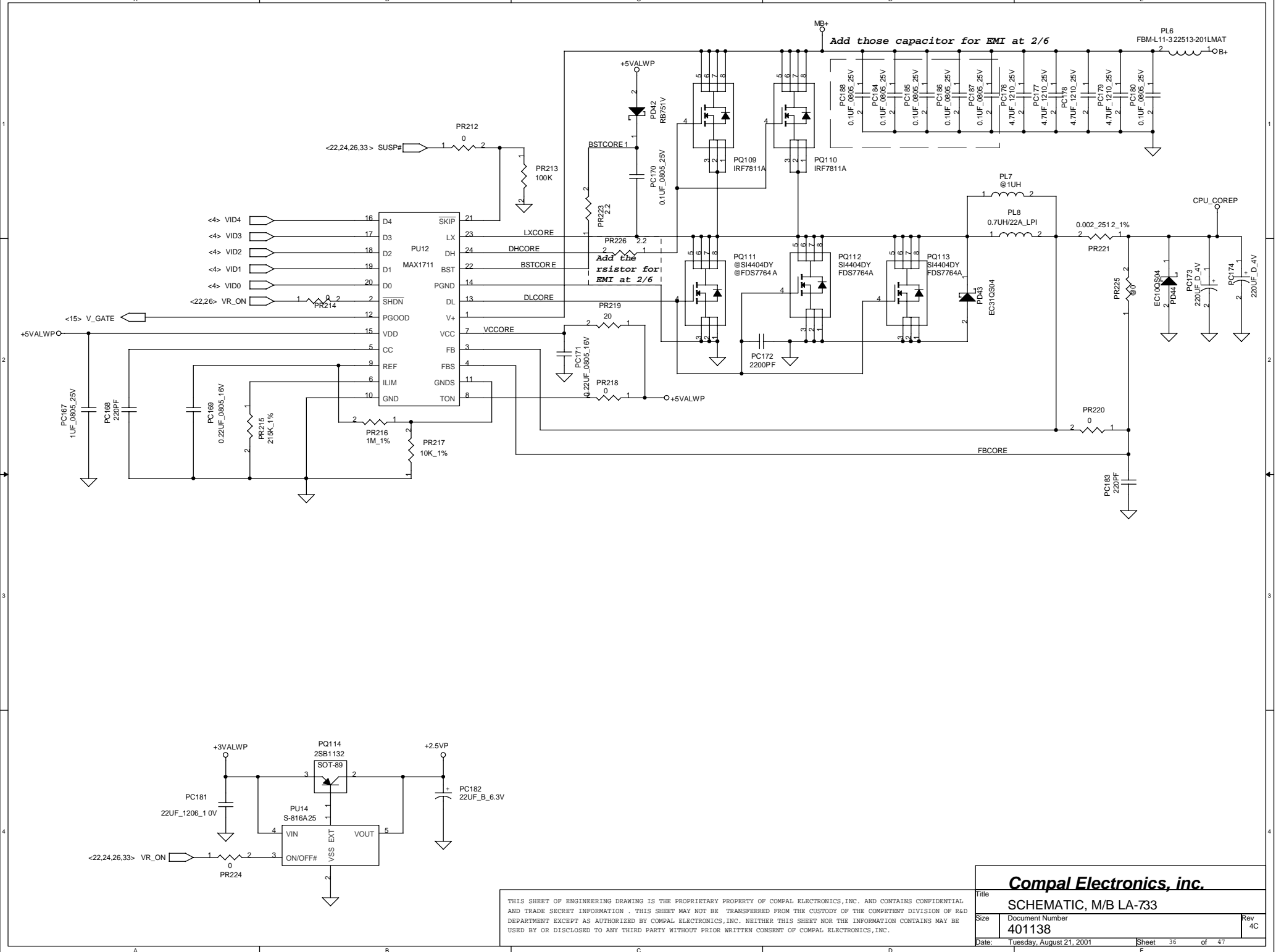
**+5V TO +5VS Transfer**



**RTC BATT CONNECTOR**

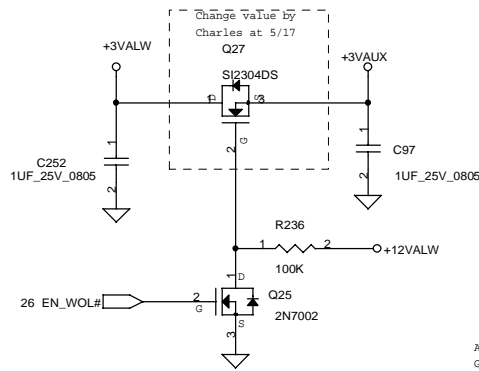
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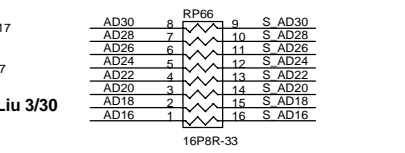
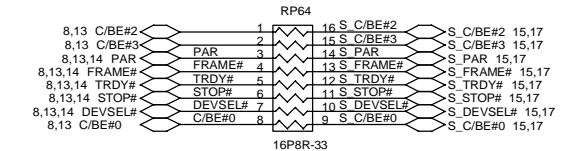
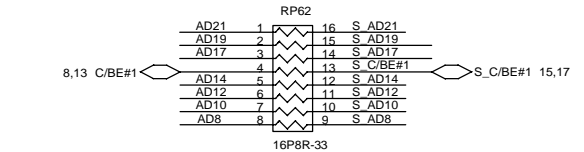
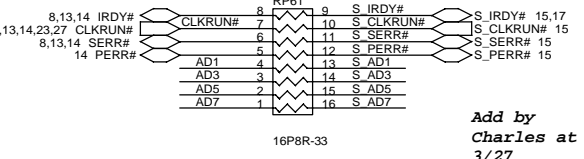
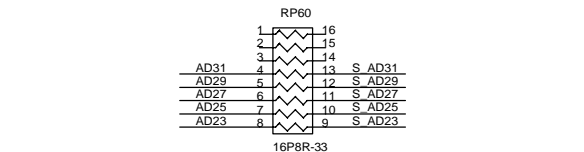
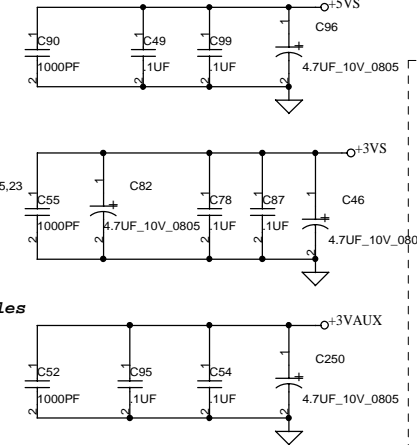
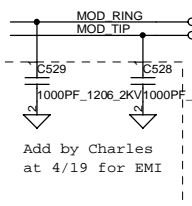
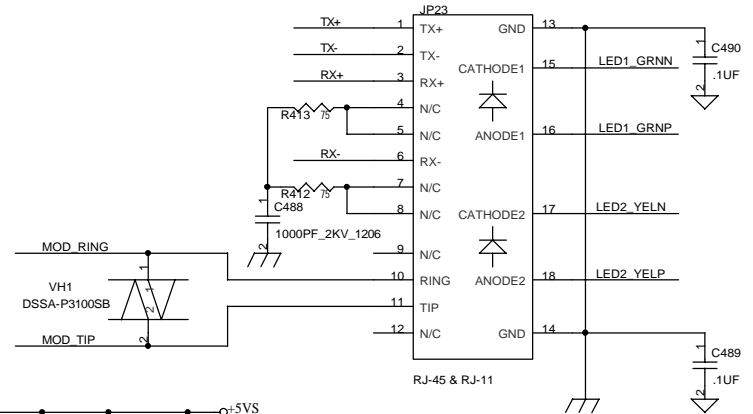
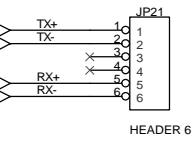
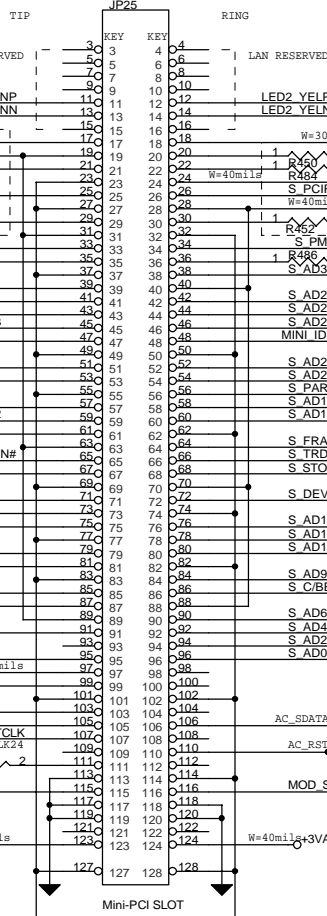


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**IDSEL : AD27**

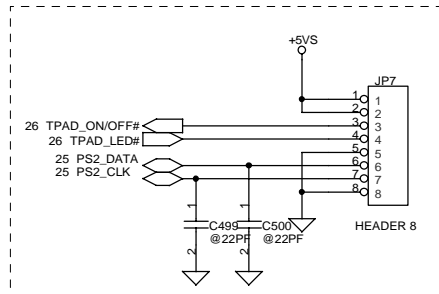
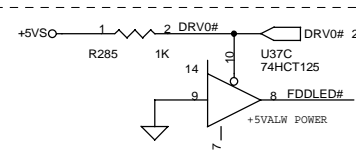
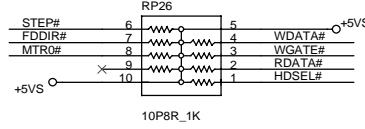
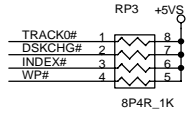
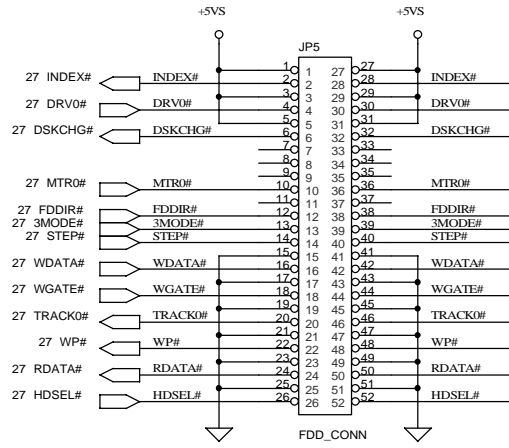


Add R462,R463 by Peter Liu 3/30

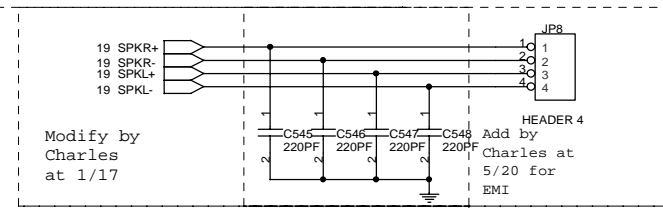
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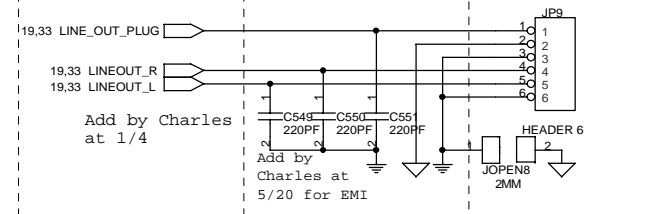


Add by Charles at 2/22 for EMI



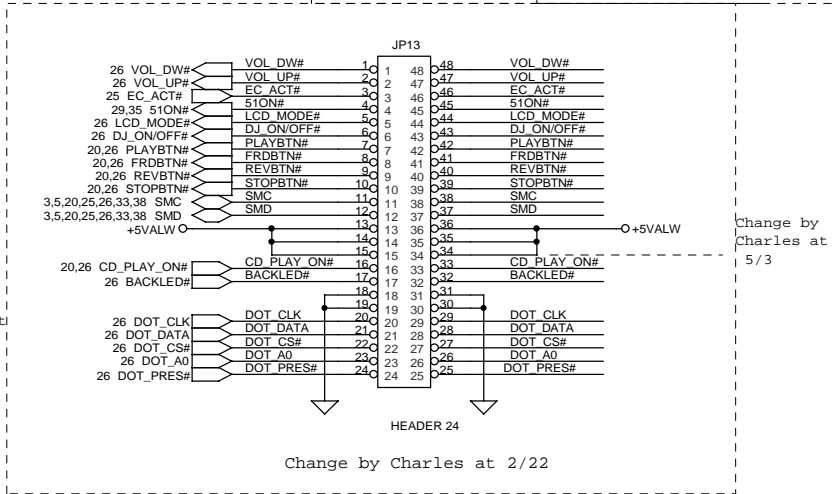
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Add by Charles at 5/20 for EMI



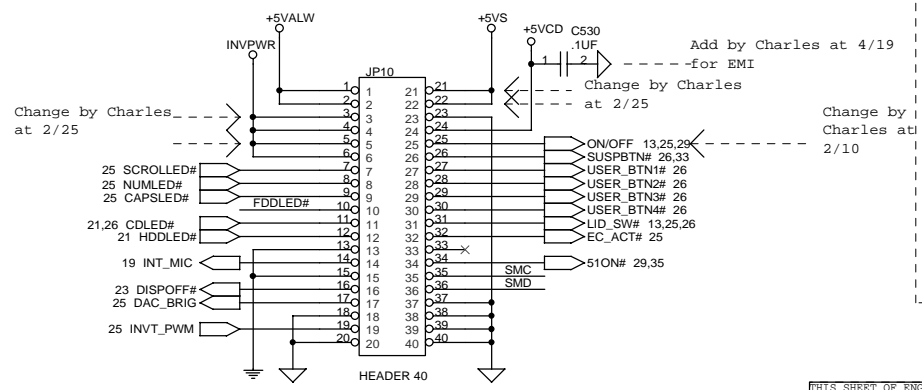
Add by Charles at 1/4

Add by Charles at 5/20 for EMI



Change by Charles at 5/3

Change by Charles at 2/22



Change by Charles at 2/25

Add by Charles at 4/19 for EMI

Change by Charles at 2/25

Change by Charles at 2/10

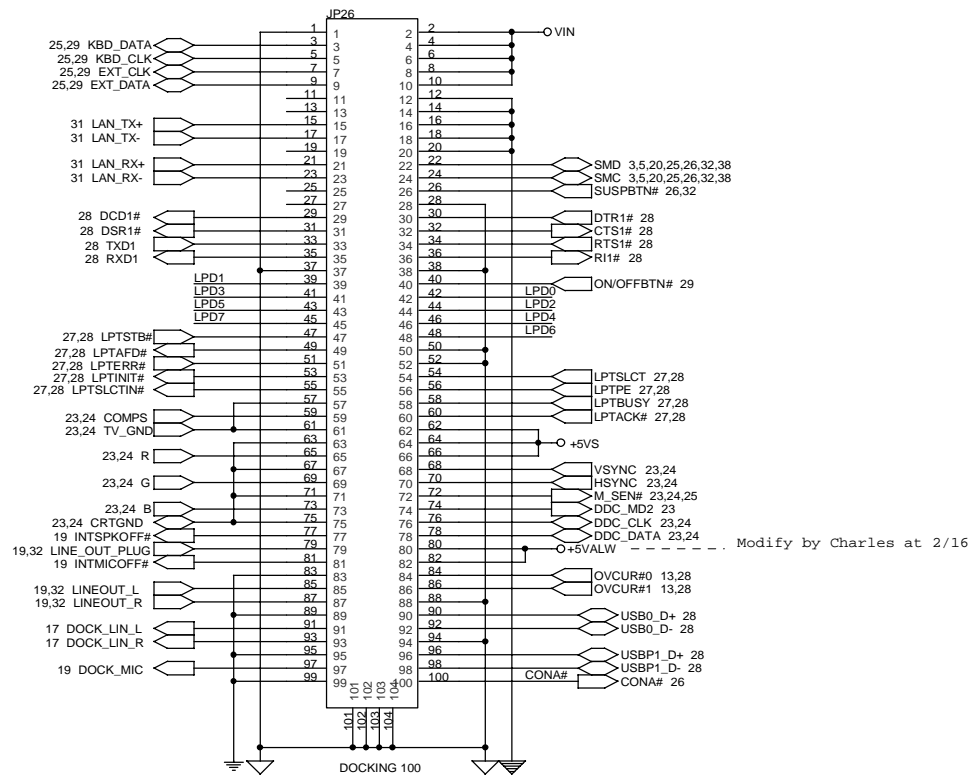
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# DOCKING 100 PIN



27,28 LPD[0..7]

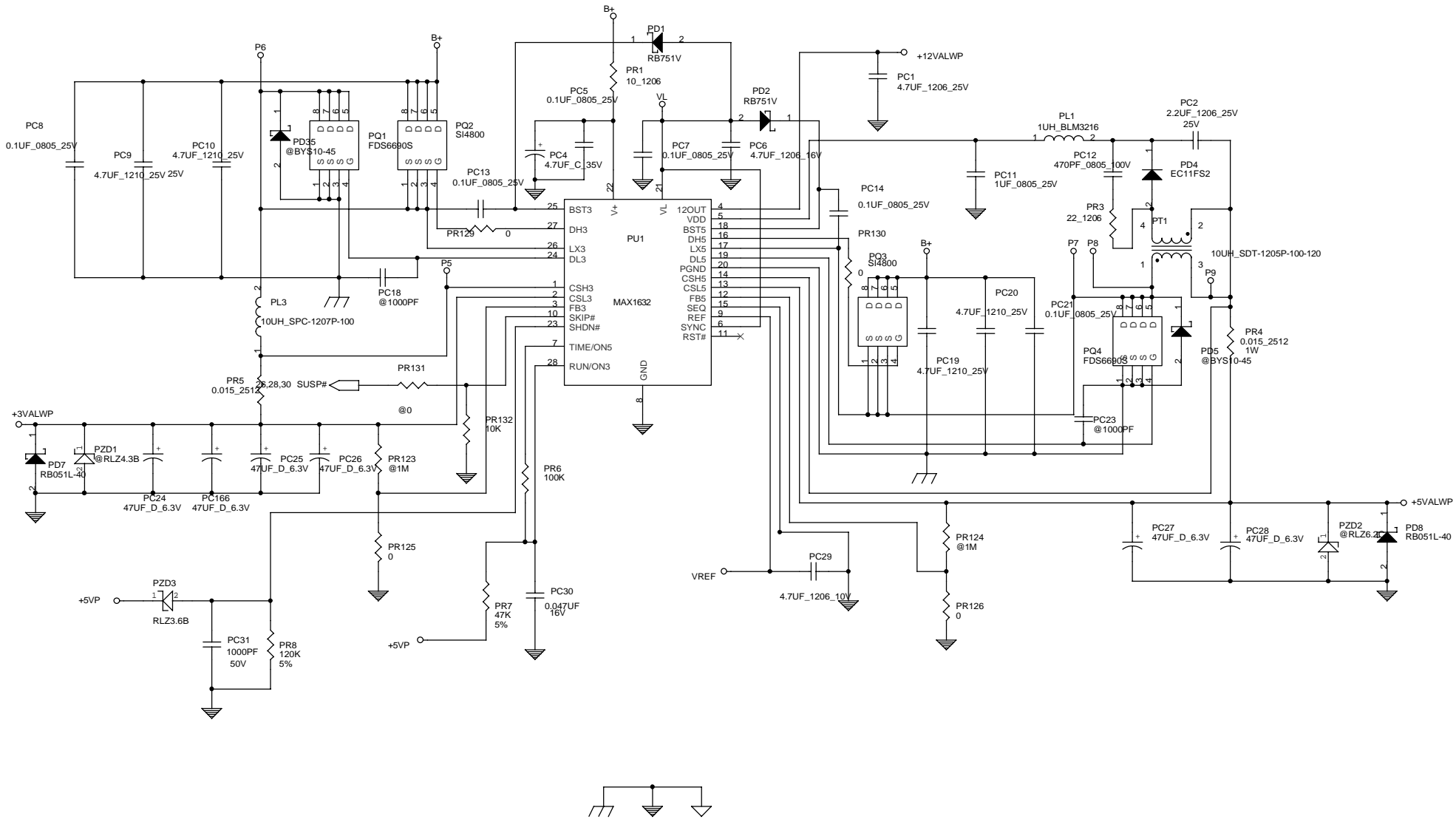


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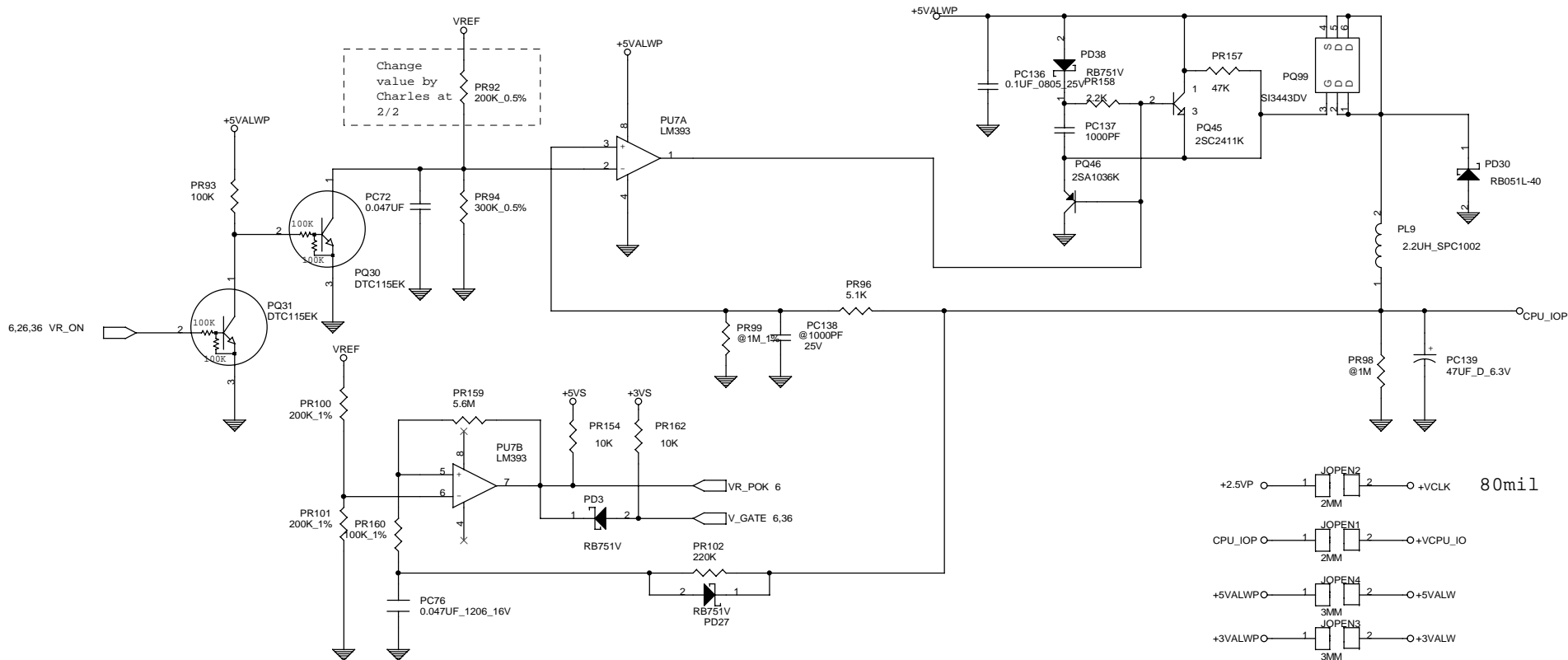
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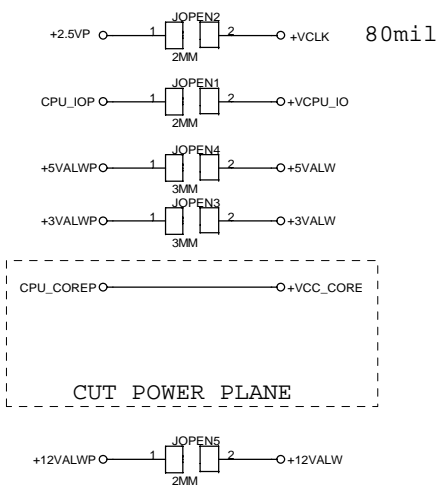
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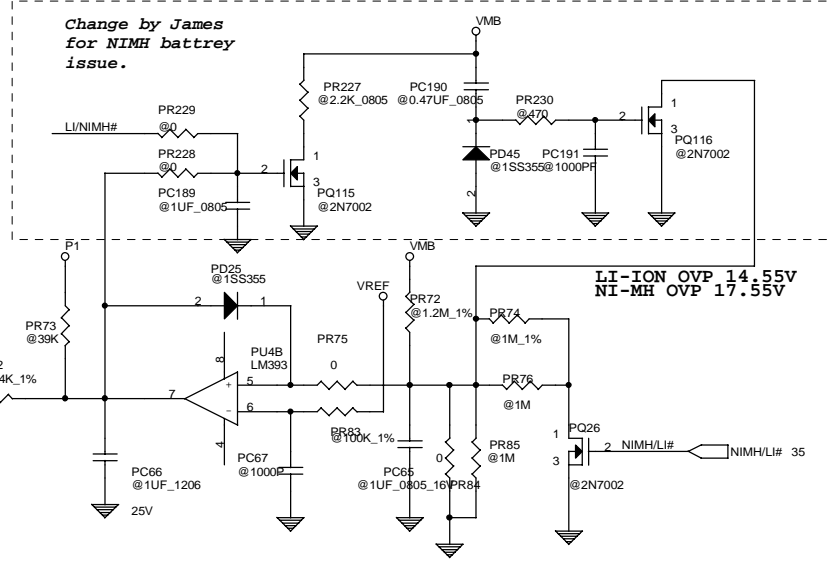
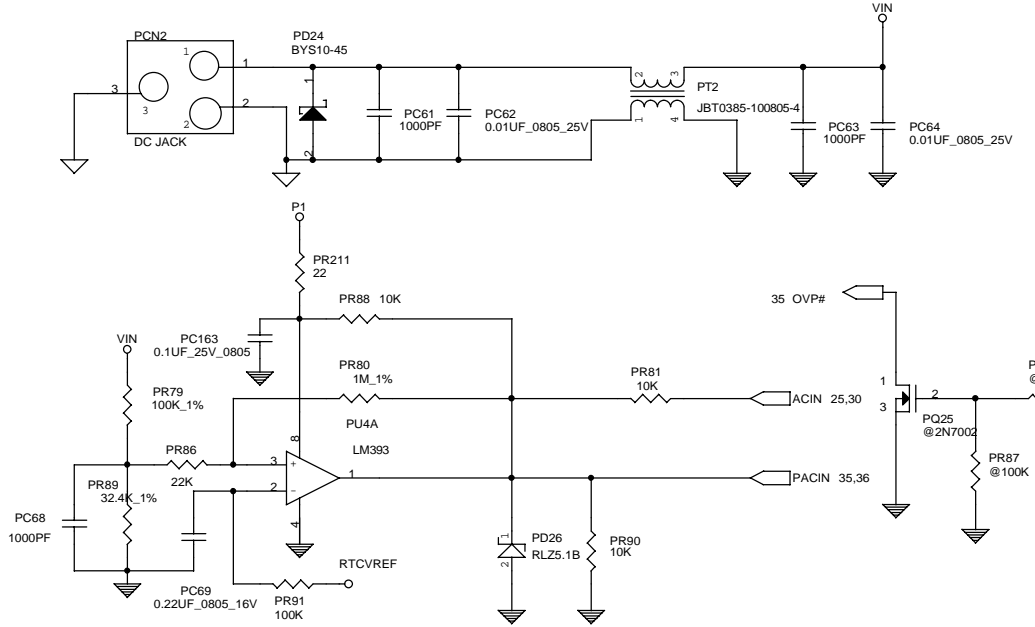
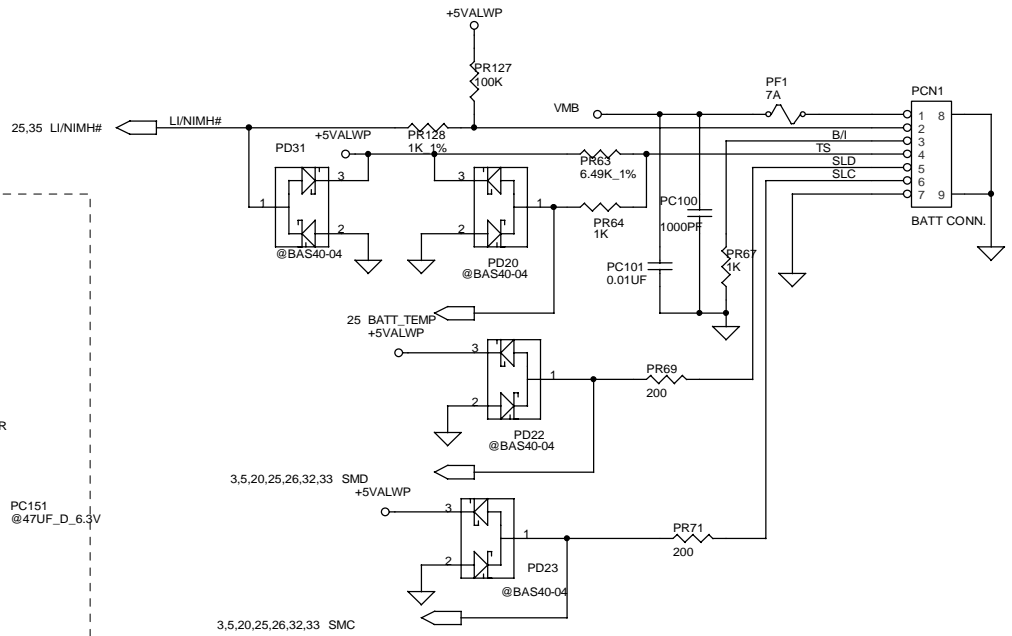
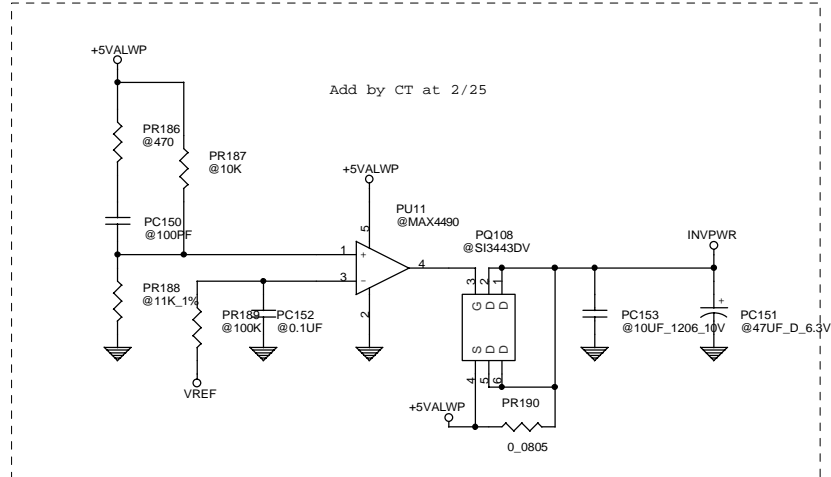


Change value by Charles at 2/2



CUT POWER PLANE

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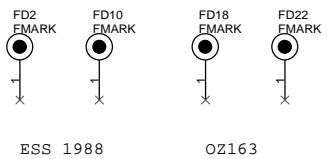
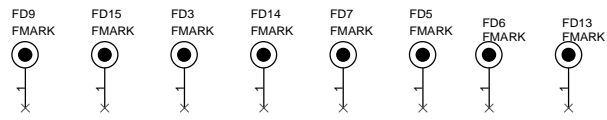
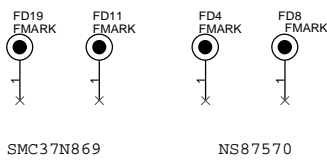
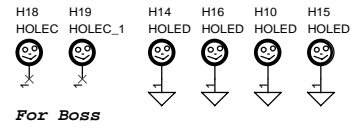
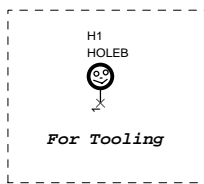
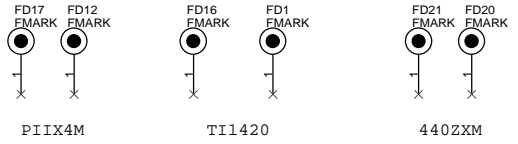
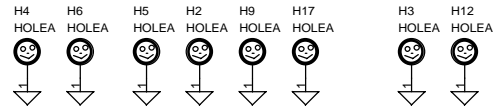
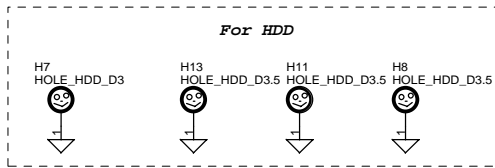


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HOLEA : Hole 3mm +0mm -0.05mm, With ring 8mm PTH  
HOLEB : Hole 3mm +/- 0.05mm, With ring 8mm, NPTH  
HOLEC : Hole 4.5mm, NPTH  
HOLED : Hole 5.2mm, with ring 8mm PTH

**For HDD**



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# P.I.R. (1) LIST

## Revision History

Date: 2000/01/14 REV#: 0.2 Description: A1-TEST TO A2-TEST

1. PAGE 5 - R388, RP2, R71, R59 delete placement, U38 pin 18 connect to ground, Q2 changed value to SI2302DS.
2. PAGE 6 - R346, R350, R347 delete placement and Y3 and Y4 both pin 2 direct connection U9 pin 25. L27, C371, C373 delete placement and U9 pin 7 and 30 direct connection +3V power.
3. PAGE 6 - R336, R357, R345, R112 delete placement and RP56 pin 16 change connection signal from "VGA\_SUS\_STAT#" to "SUSTAT1#", RP56 pin 1 signal short to "VGA\_SUS\_STAT#" signal, Q59 (SI2302DS), R452 (10K) add for Intel's Geyserville issue.
4. PAGE 6 - "VR\_HI/LO#" signal add R443 (10K) pullhigh to +3V power, "GT\_SUSTAT1#" signal add R444 (10K) pullhigh to +3V power, R353 and R107 delete placement, "SUSTAT1#" signal add R445 (10K) pullhigh to +3V power.
5. PAGE 6 - R119 delete placement and RP19 pin 1 change signal from "IGNNE#" to "CPUINIT#", "PWRGD\_CPU" signal of R356 serial D45 (RB751V) to "VR\_POK" signal.
6. PAGE 6 - U9 pin 29 change signal from "VR\_POK" to "V\_GATE", U9 pin 32 change signal from "V\_GOOD" to "VR\_POK".
7. PAGE 7 - R175 and R177 delete placement, R189 change connection signal from "RRAS#4" to "RRAS#2", R176 change connection signal from "RRAS#5" to "RRAS#3", R190 change connection signal from "RRAS#2" to "RRAS#4", R191 change connection signal from "RRAS#3" to "RRAS#5".
8. PAGE 7 - R192 pin 1 change connection U34 pin AC22, R184 pin 1 change connection U34 pin AF23.
9. PAGE 9 - R83 and R338 delete placement, U34 pin M24 and pin F17 change power source from "+VCC\_CORE" to "+VCPU\_IO".
10. PAGE 10 - Signal "PCLK\_SIO" add R427 (22) connection to U10 pin 11.
11. PAGE 11 - JP23 pin 61 change signal to "CLK\_SDRAM3", JP23 pin 74 change signal to "CLK\_SDRAM2", JP23 pin 69 change signal to "RRAS#3", JP23 pin 71 change signal to "RRAS#2", JP23 pin 62 change signal to "CKE3", JP23 pin 68 change signal to "CKE2".
12. PAGE 13 - U11 pin P16 change signal to "LID#".
13. PAGE 15 - U37 pin 148 used a 2N7002 to gattting leakage by "SYS\_ALW" signal.
14. PAGE 17 - R398, R403, C494, R44, U42 delete placement, C465, C466, C467 change power source from +8VS to +5VS and serial L44 (HB1M2012-601JT) to AVDD power, U3 pin 39 add R44 (10K) pullhigh to +3VS power, R1, R2, R3 changed value to 20K, R16, R17, R18 changed value to 24K.
15. PAGE 18 - R8, R7, R425, R426 change value to 22K, C22, C23, C503, C500 change value to 470PF, C6, C10, C510, C508 change value to 8200PF, C1, C4, C515, C514 change value to 4700PF, C2, C3, C513, C509 change value to 150PF, C7, C11, C507, C502 change value to 68PF.
16. PAGE 19 - Audio AMP. changed to TDA8552, JP1 pin 3 add bais CKT (R429, R430, R428, C517), C9 delete placement and U43 pin 7 connect signal "MICIN", Gattting internal MIC CKT changed to new one.
17. PAGE 20 - R258, R263, R267 delete placement, U32 pin 93 connect signal "SIORDY", U32 pin 12 connect signal "IRQ\_15", U32 pin 12 connect signal "SDDREQ", Q39 change value to 2N7002 and gate by "CD\_PLAY\_ON#", Q32, Q31 change value to 2N7002, U30 changed value to SI4800, R455 (100K), Q60(2N7002) add part to control U30.
18. PAGE 21 - JP11 pin 44 change to no connection, JP11 pin 21 serial R431 (82), JP11 pin 27 serial R432 (82), JP15 pin 27 serial R258 (82), JP15 pin 22 serial R267 (82).
19. PAGE 22 - R322 and R160 both changed value to 5.6K.
20. PAGE 24 - C109 pin 2 change connection to L9 pin 2, JP6 pin 2 change connection to C109 pin 1 and signal "TV\_GND".
21. PAGE 25 - U24 pin 94 changed to no connection.
22. PAGE 26 - U25 pin 2 and pin5 changed to no connection, U25 pin 9 connect signal "CD\_PLAY", U25 pin 16 change connection signal "CD\_PLAY\_ON#".
23. PAGE 27 - Super I/O change to SMC37N869 CKT.
24. PAGE 28 - R278 and R207 delete placement.
25. PAGE 29 - U35 pin 4 change connection signal "VR\_POK", U39 pin 13 add pullhigh R448(10K) to +3V power.
26. PAGE 30 - U18, U15, U17, U16 changed value to SI4800, Q11 changed value to SI3861, C202, C204, C203, C183, C184, C196 changed value to 4.7UF, C210, C208, C294, R264, C182, C185, C299, R270, C309, C209, C207, C278, R255, C199, C195, C297, R265 delete placement.
27. PAGE 30 - R266, Q35, R47, Q1, C198, C190, R211, R209, Q14, Q16, C197, C194, C218, C215, R213, R212, Q17, Q18, C217, C216 delete placement.
28. PAGE 32 - Delete battery status LED CKT, signal "DRV0#" add level-shift CKT, JP12 changed pin difinition, JP9 pin 21 and pin 22 change to no connection, JP9 pin 13 and pin 15 connect to "AGND", JP9 pin 14 change connection to signal "INT\_MIC", JP9 pin 12 change connection to signal "HDDLED#" and add JP29 to support headphone board.
29. PAGE 33 - JP25 delete placement, JP26 pin 15, pin 17, pin 21, pin 23 direct connection to JP22 in page 31.
29. PAGE 17 - AVDD power supply change by MOS.

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# P.I.R. (2) LIST

## Revision History

Date: 2000/02/14 REV#: 0.3 Description: A2-TEST TO B-TEST

02/25/2000

1. PAGE 6 - Q12 (GCL\_S12302DS) swap pin 1, 3.
2. PAGE 6 - U10 (GCL\_AM11686-001) pin 32 and R304 (10K) changed connection net to "G\_VR\_POK", R304 changed pull-high power source from +3V to +3VS.
3. PAGE 10 - R127 changed value from 22 to 10 Ohm, C121 (33PF) change to reserved in PCB.
4. PAGE 17 - R44 changed value form 33 to 10 Ohm, C38 changed value from 22 to 15PF.
5. PAGE 17 - Audio has one clean power source changed to two, one (+5VAMP) for AMP. and EQ, other (AVDD) for CODEC.
6. PAGE 18 - R8, R215, U1 and U21 changed power source from +5VCD to +5VAMP.
7. PAGE 19 - U2 changed power source from +5VCD to +5VAMP.
8. PAGE 19 - Q6 pin 3 add a serial resistor (2.2K) to connect JP1 pin 3 and 2.
9. PAGE 20 - Q42, Q43 and Q32 swap pin 1 and 3, U33 (OZ163) pin 56 change 1K pull-down ground to 10K pull-high +5VCD of R366.
10. PAGE 25 -U41 (87570) add "FIR\_PRE#" signal at pin 84, RP56 (8P4R\_10K) add "FIR\_PRE#" signal at pin 5 and "BT\_PRE#" signal at pin 7.
11. PAGE 26 - "PLAYBTN#", "REVBTN#", FRDBTN#, STOPBTN#, "DJ\_ON/OFF#", VOL\_UP#, VOL\_DW# and "CONA#" signals add RP55 pull-high array.
12. PAGE 27 - R205 change value from 33 to 10 ohm, C176 change value from 10 to 15PF.
13. PAGE 27 - U15 pin 81 changed to connect to "DTRA#" signal, pin 80 changed to connect to "CTSA#" signal, pin 79 changed to connect to "RTSA#" signal, pin 78 changed to connect to "DSRA#" signal, pin 77 changed to connect to "TXDA" signal, pin 76 changed to connect to "RXDA" signal, pin 83 changed to connect to "DCDA#" signal.
14. PAGE 29 - U8 pin 11 changed to connect to "FIR\_PRE#" signal.
15. PAGE 29 - U8 (MAX708) pin 1 changed to connect to "G\_VR\_POK" signal, R283 changed value from 240K to 113K and pin 1 changed to connect to +3VS power, U8 (MAX708) pin 5 serial a resistor (2.2M) to R283 pin 2.
16. PAGE 29 - U26F (74LVC14) pin 13 add one +5V RC delay CKT.
17. PAGE 32 - JP12 pin 17 changed power source from +5VS to +5VALW, JP12 pin 17 changed signal from NC to "DOT\_PRE#", JP9 pin 25 changed signal from "ON/OFFBTN#" to "ON/OFF" (Old components' references).
18. PAGE 33 - JP26 pin 80 and 82 changed power source from +5V to +5VALW.

02/18/2000

1. SpeedStep Workarond for CPU\_STP# timing (page 6)
    - add D19 (@RB717), pin1 connect CPU\_STP#, pin2 connectVRCHGNG#, pin3 connectGCL\_CPUSTP#
  2. Remove CPU\_LO/H# pull high (CPU had internal pull high) (page 6)
    - no load R100 (@GCL\_1.5K)
  3. Reserve 14.318MHz from Clock generator to Geyserville control logic (page 6,10)
    - add R298 (@GCL\_0) serial on the trace 14.3M\_GCL
    - U11 pin26 add a serial R114 (@22) on 14.3M\_GCL
  4. Remove North Bridge TESTIN# pull high (according to updated RDDP) (page 7)
    - no load R329 (@10K)
  5. No connection DCLKRD input of the North Bridge (arrording to RDDP) (page 6)
    - let U31 pin AB22 to be NC
  6. Change AGPREF to meet RDDP (page 8)
    - R152 change value from 1K\_1% to be 3.48K\_1%
    - R154 change value from 2K\_1% to be 2.32K\_1%
  7. Redundance ECC serial resistors remove (page 12)
    - no load RP47 (@16P8R-10)
  8. Improve PLLX4 32KHz crystal RC value for more reliable (page 13)
    - R172 change value from 1M to be 22M
    - C164,C165 change value from 22PF to be 12PF
  9. MIC circuit improve (page 19)
    - add a serial R53 (2.2K) on Q6 pin3
    - no load U22,C8,C239,C240,R234
    - change R29 from 10K to be 0 ohm
    - change R32 from 2K to be 2.2K
    - connect JP24 pin2,3 together
    - change R23 from 27K to be 0 ohm
    - change C20 from 1UF to be 0 ohm
    - add Q1 (2S2411EK) just like Q56 but only pin3 connect to R32 pin1
  10. For layout space improve (page 20)
    - C429 change value from 10UF\_10V\_1206 to be 1UF\_0603
    - R359 change from 10K to be 100K
  11. CD\_AGND improvement (page 21)
    - add R356 (0\_0603 ohm) between CD\_AGND & GND (at the middle of the trace)
    - add R288 (0\_0603 ohm) between CD\_AGND & GND (close CD-ROM module)
  12. Modify BlueTooth connector definition
    - pin 1 : NC -> BT\_DET
    - pin 3 : NC -> BT\_WAKE\_UP
    - pin 7 : NC -> BT\_USB1\_D+
    - pin 9 : NC -> BT\_USB\_D-
    - pin 13 : NC -> BT\_RST#
    - pin 6 : GND -> BT\_ON#
    - pin 8 : NC -> BT\_PRE#
    - pin 10 : BT\_PRE# -> GND
    - pin 12: BT\_WAKE\_UP -> TO\_USB1\_D+
    - pin 14 : NC -> TO\_USB1\_D-
    - pin 16 : BT\_ON# -> GND
    - pin 18 : BT\_RST# -> NC
    - pin 20 : BT\_DET -> NC
- add R317,R324,R318,R325 (0 ohm) & R316,R323,R319,R326 (@0) for USB1 signals switching (BlueTooth or non-BlueTooth)

1. Issue A2C008 : Can't mute completely (Page 20)
  - add resistor divider R1(20K-serial), R16 (24K-to AGND) on INT\_CD\_L
  - add resistor divider R3(20K-serial), R18 (24K-to AGND) on INT\_CD\_R
  - add C502 (1UF\_0603) to decouple the small signal of INT\_CD\_L
  - add C503 (1UF\_0603) to decouple the small signal of INT\_CD\_R
  - add R426,R427 (both @10K) on INT\_CD\_L small signal voltage divider to be 2.5V (reserved)
  - add R428,R429 (both @10K) on INT\_CD\_R small signal voltage divider to be 2.5V (reserved)
  - add R436,R437 (both @10K) on LEFT\_EQ and RIGHT\_EQ for noise improvement (reserved)
  - add R432,R433 (@24K,@20K) on CDROM\_L for noise improvement (reserved)
  - add R434,R435 (@24K,@20K) on CDROM\_R for noise improvement (reserved)
2. Correct CD-ROM CD\_AGND pin assignment (page 21)
  - change JP16 pin4 connection from CD\_AGND to GND
3. No load D20(level shift gate for VR\_POK) for Geyservelli inside (page 6)
4. Add amplify mute AMP\_MUTE for reservation only (page 17,19)
  - add Q54 (@FDV301), R430(@100K), R431(@10K)
  - AMP\_MUTE was inverse from the output of ESS1988 pin63
  - AMP\_MUTE was connected to TDA8552TS pin5
5. Add M\_SEN# for CRT monitor detection (page24,25)
  - add D45(DAN217), R425(100K), C371(68PF)
  - M\_SEN# was coming from JP11 pin11
  - M\_SEN# was going to EC pin83
6. Exchange IR module pin11 and pin13 (page 28)
  - pin11 will be GND
7. Add CP8,9,10,11,12,13 (@8P4C\_22PF) on keyboard signals for reserve(page 29)
8. Change MAX708 to be MAX6342 for cost improvement (page 29)
9. Delete three beads HB1M1608-121JT on Mini-PCI connector pin28,19,123 (pass through) (page 31)
10. MD\_BITCLK improvement for EMI (page 17,31)
  - add R423(22 ohm) serial on MD\_BITCLK(nearby ESS1988)
  - add R424(10 ohm), C501(15PF) AC termination on MD\_BITCLK (nearby Mini-PCI CN)
11. Internal PS2 signals add two decouple CAPs for EMI improvement
  - C499(@22PF) on PS2\_CLK
  - C500(@22PF) on PS2\_DATA
12. Dot-Matrix connector change from 30 pins 0.5 pitch to 24 pins 1.0 pitch (page 32)
13. Switch Board change pin definition for Inverter Power (page 32)
  - JP10 pin3,4,5,6 change from +5VS to be INVPPWR
  - JP10 pin21,22 change from NC to be +5VS

02/29/2000

1. Modify the references of some components for easy layout
  - R433 <=> R1 => R433=20K,R1=0 ohm
  - R432 <=> R16 => R432=24K,R16=@24K
  - R435 <=> R3 => R435=20K,R3=0 ohm
  - R434 <=> R18 => R434=24K,R18=@24K
2. Scheme correct (page 6)
  - D19 pin3 change net from GCL\_CPUSTP# to CPU\_CPU\_STP#
  - D20 pin1 add a output module VR\_POK for external connection
3. A2H001 & A2C045 (CD-ROM copy compare fail & low performance)
  - IRQ14 damping R306 change from 82 ohm to 33 ohm
  - IRQ15 damping R333 change from 82 ohm to 33 ohm
  - PIORDY damping R309 change from 82 ohm to 33 ohm
  - PIORDY pull high R311 change from 1K ohm to 10K ohm
  - SIORDY damping R378 change from 82 ohm to 0 ohm
  - SIORDY pull high R341 change from 1K ohm to 10K ohm
  - PDDREQ damping R320 change from 82 ohm to 33 ohm
  - CD\_DREQ damping R380 change from 82 ohm to 33 ohm

03/01/2000

1. Add MUTE function for amplify (page 17,19,26)
  - add "MUTE" signal on U3 pin63
  - add "EC\_MUTE" signal on U39 pin5
  - add U47 (NC7ST32-SC70) to "OR" "MUTE" & "EC\_MUTE" (U47 pin1 = "MUTE", pin2 = "EC\_MUTE", pin4 connect to U2(Amplify) pin5)
  - add C504(0.1UF) for U47 power decoupling
  - add R438(0 ohm) serial on "EC\_MUTE" for reserve only
  - no load R36 to be @0 ohm (original pull down on U2 pin5)
2. Add some CAPs for noise cross reference (help for EMI & signal quality)
  - for PCI BUS on +3VS,+5VS : C505,C508 (0.1UF); on +3VS,+3V : C510,C511 (0.1UF); on +3VS,+3VALW : C513 (0.1UF) on +3V,+3VALW : C515 (0.1UF)
  - for CD-ROM IDE BUS on +3V,+5VS : C512 (0.1UF); on +3VS,+3V : C514 (0.1UF); on +5VS,+5VCD : C516 (0.1UF)
  - for HDD IDE BUS on +3VS,+3V : C506 (0.1UF); on +5VS,+3V : C509 (0.1UF)
  - for AGP BUS on +3V,+3VS : C507 (0.1UF)

03/08/2000

1. Improve EQ quality (page 18)
  - R31,R231 change from 120K to 12K
  - R27,R223 change from 120K to 20K
  - R213,R12 change from 120K to 16K
  - R218,R214 change from 120K to 24K
  - R227,R232 change from 120K to 1.5K
  - C21,C22,C235,C237 change from 470PF to 3300PF
  - C1,C4,C222,C223 change from 4700PF to 5600PF
  - R28,R233 change from 1M to 180K
  - R24,R226 change from 1M to 270K
  - R13,R217 change from 1M to 240K
  - R11,R221 change from 1M to 330K
  - R25,R229 change from 1M to 24K
  - C6,C9,C228,C230 change from 8200PF to 3300PF
  - C2,C3,C224,C227 change from 150PF to 180PF
  - C7,C10,C229,C234 change from 68PF to 0.22UF

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# P.I.R. (3) LIST

## Revision History

Date: 2000/03/23 REV#: 0.4 Description: B1-TEST TO B2-TEST

### 03/23/2000

1. Correct ON/OFF button signal for PIIx4 (page 13)
  - D9 pin1 change connection from ON/OFFBTN# to ON/OFF
2. Correct DM\_ON signal for OZ163 direct CD-PLAY function (page 20)
  - change D26 pin1 from CD\_PLAY\_ON# to DM\_ON
3. Correct Bluetooth power supply (page 24)
  - JP20 pin15,17,19 change connection from +3VS to +3VALW
  - JP20 pin18,20 change connection from N.C. to +5VALW for USB hub on Bluetooth module
4. Add a option resistor for G\_VR\_POK for 733L while Geyservilli ASIC was no load (page 6)
  - add R448 L@0, pin1 connect V\_GATE, pin2 connect G\_VR\_POK
5. For Factory ATE testing (page 6)
  - change R117,R121 from LN\_0 to LN\_1K
  - add R447 LN\_1K on U10 pin43
6. Improvement for Issue A2C008 (page 20)
  - change R432,R434 from 24K to 33K
  - add C517,C518 1UF\_0603 serial in front of the EQ for LEFT\_EQ & RIGHT\_EQ respectively
7. Improve the reserved "MUTE" function (page 19)
  - add R445 100K
  - add D46,D48,D49 RB751V
  - add R444 @0
  - add C526 @.1UF
  - add U48 @NC7ST32
  - no load R43,R33 to be @100K
  - no load R235 to be @10K

### 03/28/2000

1. Reserve Pull high for VID[0..4] (page 5)
  - add RP65 @8P4R-4.7K & R461 @4.7K
2. Improve PCI signal quality (add damping resistors)
  - for miniPCI : add RP60,RP61,RP62,RP63,RP64,Rp66 16P8R-33 ohm (page 31)
  - for miniPCI : R453,R454 33 ohm & R450R452,R449,R451 10 ohm (page 31)
  - for PCI1420 : R458,R459,R460 10 ohm (page 15)
  - for ESS1988 : R455,R456,R451 10 ohm (page 17)
3. Add pad junction for TV\_GND for EMI request (page 24)
  - add JOPEN6 2MM for TV\_GND

### 03/30/2000

1. FIR module change from HP3600 to VISHAY TFDS6101E (page 28)
  - change R286 from LN\_2.2\_1206 to @LN\_3.3\_1206 (change to be on load)
  - change R97 from LN\_560 to LN\_0\_0805
  - delete R287 (original @0)
  - change R102 from original LN\_0 to 100K
  - change C111 from LN\_220PF to LN\_0.1UF
  - delete C368 (original LN\_0.47UF\_16V\_0805)
  - change U9 from LN\_HSDL\_3600 to LN\_TFDS6101E
  - add R446 LN\_3.3\_1206
  - add C525 LN\_100PF

### 03/30/2000

2. MODEM can't work was caused by the mal-reset of MD\_RST# (page 31)
  - add R462 @0 for MD\_RST#
  - add R463 0 for PCIRST# (default)
3. CMOS data lost (caused by +5VALW undershoot too big while unplug the AC) (page 34)
  - change PD8 from BYS10-45 to RB051L40 (the same as PD30)
4. IRQ8 need to pullhigh (because BIOS change the programming method) (page 13)
  - load R167 1K

### 04/05/2000

1. Speed up the +3V discharge time (page 30)
  - R371 change from 470 ohm to 33 ohm

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# P.I.R. (4) LIST

## Revision History

Date: 2000/04/20 REV#: 0.5 Description: B2-TEST TO B3-TEST

### 04/20/2000

1. Correct MOS switch (74HCT4066) for switching headphone or Int. speaker (page 18)
  - Add Q55 and Q54(2N7002) to use "HPS" signal to switching L-R channel.
  - Add R466 (10K) and R465 (10K) pullhigh +5VCD
  - Add one MOS switch (74HCT4066) to switching L-R channel.
  - Add R464 (@0) and R464 (@0) only for reserved, that can bypass MOS switch.
2. Add MOS to gattig MIC signal (page 19).
  - Add Q58(SI2304DS) and Q59(2N7002) to disconnect MIC. signal.
  - Add R470(100K) pullhigh resistor.
  - Add R471(10K) pulldown resistor.
  - Add R473(@10K) pulldown resistor.
  - Load R444(0), C526(.1UF) and U48(NC7ST32) for control "MUTE\_AUD" signal
  - No load R29(0).
3. Add JOPEN for EMI (page 24)
4. Add pullhigh resistor for "BIOSCS#" signal (page 25)
  - add R472 (10K).
5. Add a diod to reserved for S/W (page 13)
  - add D50 (@RB751V).
6. Add capicator on JP22 (RJ11) for EMI request. (page 31)
  - add C529 and C529 (1000PF\_2KV\_1206).
7. Add capicator on JP10 "+5VCD" power pin for EMI request. (page 32)
  - add C530(0.1UF).
8. Change EQ RC value. (page 18)
9. Add damping capicator C532 and C533 (1UF) on U31 power pin VTTA(M24) and VTTB(F17) for WIN98 Multi-task will be halt. (page 9)
  - add C532, C533(1UF).
10. Diconnect MIC Jack (JP24) pin 3 and pin 2 for EXT. MIC can't record voice. (page 19)
11. Add capicator and change value for TV-OUT quility. (page 24)
  - add C531(27PF).
  - change C106 and C105 value (330PF).
12. Add CKT for gattig ME-OFF reset. (page 25)
  - add Q56 and Q57(2N7002).
  - add R468 (10K).
  - add R469 (100K).
  - add R474 (0).
13. Add resistor reserved for FAN control function. (page 30)
  - add R475(@0).
14. Add +5VALW power pin at LCD status board connector (JP13) pin 15 and 34. (page 32)
15. Add ATE and function testing point.
16. Change RC value for beep sound is very loud. (page 19)
  - change value R266(10K\_1%).
  - change value C285(.22UF).
  - "PCM\_SPK#" signal change to connect U26 pin 5 and C306 pin 1 change to connect U26 pin 6.

### 05/03/2000

17. Add more damping capicator in +VCPU\_IO and VGTLREF\_BX. (page 9)
  - add C541, C539, C540 (.01UF).
  - add C538 (1UF).
  - add R476 (1K).
  - add R477 (2K).
  - change value C532, C533 (4.7UF).
  - change value C122, C142 (1UF).
18. Add more damping capicator in +3V. (page 23)
  - add C534 (10UF).
19. Modify and reserved for FAN control function. (page 30)
  - add C542 (@10UF).
  - direct to connect Q29 pin 2, U4 pin7 and C274 pin 2.
  - remove R52 (0) and the resistor reserved for connect "EN\_DFAN" signal and Q29 pin 2.

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# P.I.R. (5) LIST

## Revision History

Date: 2000/06/15      REV#: 1.0      Description: B3-TEST TO C-TEST

### 05/20/2000

1. Fix high pitch noise issue (page 18)
  - Add C543 and C544 (0.01UF).
2. Fix PO-PO sound noise when power on (page 19).
  - Add Q62, Q63, Q64, Q65 (SI2304DS).
  - Add Q61(2N7002).
  - Add R480(100K).
3. Fix USB power leakage (page 28)
  - Add Q60(SI2306DS).
  - Add R478(100K).
4. Fix CD-direct play will into sleep mode after 2 second (page 20)
  - Delete R362 (10K).
  - Add R364 (10K).
5. Fix 733 and 733C can't identify M/B (page 25)
  - Add R479 (@10K).
6. For EMI change (page 32).
  - Add C545, C546, C547, C548, C549, C550, C551 (220PF).
7. BOM change for EMI.
  - C121 (@33PF --> 33PF) and R127 (10 --> 15 Ohm) for "48M" (page 10).
  - C148 (@15PF --> 15PF) and R150 (@10 --> 33 Ohm) for "HCLK" (page 7).
  - C163 (@22PF --> 22PF) for "DCLKO" (page 7).
  - C160 (@22PF --> 22PF) for "GCLKO" (page 8).
  - C169 (@10PF --> 22PF) and R187 (@33 --> 33 Ohm) for "DCLKO" (page 10).
  - C444, C445, C460, C458 (@15PF --> 22PF) for SDRAM\_CLK (page 11).
  - R384, R385, R382, R383 (@33 --> 33 Ohm) for SDRAM\_CLK (page 11).
8. Change value for FIR setting. (page 28)
  - R98 (0 --> 10K).
  - R102 (100K --> @10K).
9. Delete double pullup in "CDLED#" signal (The signal already had R189 pullup in page 21). (page 26)
  - R350 (100K --> @100K).
10. Fix unplug AC-IN in SPR then system shut down. (page 29)
  - Q51 (2N7002 --> @2N7002).
11. Fix "GCLKO" signal waveform quility on the EA report. (page 8)
  - R162 (10 --> 22).
12. Fix "PCLK\_MINI" signal waveform quility on the EA report. (page 10)
  - R120 (33 --> 15).

### 06/08/2000

13. Fix IR noise. (page 28)
  - C110 (10UF\_10V\_1206 --> @10UF\_10V\_1206).

### 06/15/2000

14. Fix "CLK\_SDRAM2"-"CLK\_SDRAM5" signal waveform quility on the EA report. (page 10)
  - R346, R347, R348, R349 (22 --> 15 Ohm ).

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# P.I.R. (6) LIST

## Revision History

Date: 2000/06/26 REV#: 2.0 Description: C-TEST TO MP-TEST

### 05/20/2000

1. Fix winstone99 will be hang issue (page 4)
  - Add C553(1UF), C554(1000PF) and C555(.01UF) for "CPU\_IO" power.
  - Change value C338, C288, C67, C63, C61 and C324 from 0.1UF to 1000PF for "CPU\_IO" power.
  - Change value C344, C287, C68, C64 and C60 from 0.1UF to 0.01UF for "CPU\_IO" power.
  - Change value C62, C59 and C66 from 0.1UF to 1UF for "CPU\_IO" power.
2. Fix noise sound when plug-in headphone (page 17).
  - Add Q66(2N7002).
  - Add R481(33).
3. Fix T.P mouse move cause audio noise (page 17)
  - Delete L17, L13 and L3 (0\_0805).
4. Fix U2 pin 4 floting problem (page 19)
  - Add R482 (100K).
5. Fix +5VCD discharge slowly problem (page 20)
  - Change R391 value from 470 to 33 Ohm.
6. Fix EA problem (page 10)
  - Change value R346, R347, R348 and R349 from 22 to 10 Ohm for memory clock.
  - Delete C121 (33PF) for 48M clock.

### 11/03/2000 ( Modify for N32N-733B )

1. BOM modified for N32N-733B (page 20,28,32,33)
  - Change RP49 from "8P4R-10K" to "BN\_8P4R-10K".
  - Change RP48 from "10P8R\_10K" to "BN\_10P8R\_10K".
  - Change RP51,RP53 from "10P8R\_4.7K" to "BN\_10P8R\_4.7K".
  - Change RP52 from "@16P8R\_33" to "B@16P8R\_33".
  - Change RP54,RP50 from "@16P8R\_0" to "B@16P8R\_0".
  - Change R361 from "1M" to "BN\_1M".
  - Change R359,R394 from "100K" to "BN\_100K".
  - Change R361 from "1M" to "BN\_1M".
  - Change R360,R363,R364,R366,R367,R368,R98 from "10K" to "BN\_10K".
  - Change R102 from "@10K" to "B@10K".
  - Change R355 from "1K" to "BN\_1K".
  - Change R375 from "5.6K" to "BN\_5.6K".
  - Change R374 from "47K" to "BN\_47K".
  - Change R97 from "0\_0805" to "BN\_0\_0805".
  - Change R446 from "3.3\_1206" to "BN\_3.3\_1206".
  - Change R369 from "33" to "BN\_33".
  - Change R370 from "@33" to "B@33".
  - Change R379,R376,R377 from "@0" to "B@0".
  - Change L41 from "HB1M2012-601JT" to "BN\_HB1M2012-601JT".
  - Change X2 from "8MHZ" to "BN\_8MHZ".

### 11/03/2000 ( Modify for N32N-733B )

- Change C427,C428 from "10PF" to "BN\_10PF".
- Change C115 from "10UF\_10V\_1206" to "BN\_10UF\_10V\_1206".
- Change C111,C430,C432,C435 from ".1UF" to "BN\_.1UF".
- Change C525 from "100PF" to "BN\_100PF".
- Change D25 from "1N4148" to "BN\_1N4148".
- Change D26,D27,D28,D29,D30 from "RB751V" to "BN\_RB751V".
- Change U33 from "OZ163" to "BN\_OZ163".
- Change U9 from "TFDU6101E" to "BN\_TFDU6101E".
- Change JP13 from "HEADER24" to "BN\_HEADER24".
- Change JP26 from "DOCKING 100" to "BN\_DOCKING 100".
- Change Q33,Q34,Q44 from "2N7002" to "BN\_2N7002".

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## Revision History

Date: 2000/12/20 REV#: 3.0 Description: C2-TEST for H1.6/MP-TEST for H1.5

### 12/20/2000

1. Fix C0-step after CPU (page 4)
  - Change U7 P1 pin power source from "+VCPU\_IO" to "+VCC\_CORE".
2. Mini-PCI add 4 signal for 802.11b combo module (page 31)
  - Add R483(10) for "REQ#0" signal on pin 21 of Mini-PCI connector (JP25) .
  - Add R485(100) for "S\_AD26" signal for IDSEL on pin 43 of Mini-PCI connector (JP25) .
  - Add R484(10) for "GNT#0" signal on pin 22 of Mini-PCI connector (JP25) .
  - Add R486(10) for "PME#" signal for 802.11b device on pin 36 of Mini PCI connector (JP25) .
3. Fix Microphone feedback sound issue
  - Add new signal (AUTO\_GAIN\_CONTROL) output from U3 (ESS1988) pin 49 (Page 17) that connect U44 pin 4 (Page 26).
4. Capacitor change value to met Intel 1GHz CPU requirement (page 4)
  - C299, C300 change value from 1UF to 10UF.
  - C292, C354 change value from 0.1UF to 10UF.
  - C309, C350, C364, C361 change value from 0.01UF to 10UF.
  - C298, C349 change value from 1000PF to 10UF.

### 12/26/2000 Power Change List For Hurricane 1.6

1. Use MAX1711 instead of AD3421 (Control PWM IC) and AD3410 (Driver) in CPU-CORE circuitry. (page 36)
2. One MOSFET (FDS7764A) is reserved for 21.1A peak current in 1GHz Intel CPU. (page 36)
3. PU14 is added for 2.5V CLK\_VCC (The Linear regulator is included in AD3421 for original LA733 design). (page 36)

Date: 2000/02/02 REV#: 4.0 Description: MP-TEST

### 02/02/2001

1. Fix 1GHz CPU voltage transient issue (page 4)
  - C555, C319, C326 and C303 change value from 0.01UF to 0.1UF.
  - C554 and C325 change value from 1000PF to 0.1UF.
2. Del R97 (0 ohm\_0805) because of PCB trace connected. (page 28)

### 02/02/2001 Power Change List For Hurricane 1.6

1. PR92 change value from 174K to 200K for "CPU\_IO" voltage down from 1.58V to 1.5V. (page 37)
2. PR215 change value from 150K to 215K for current limit protection. (page 36)
3. Add PR226 (2.2 Ohm) for EMI requirement. (page 36)
4. Add PC184, PC185, PC186, PC187 and PC188 6 pcs capacitor those value all are 0.1UF\_0805\_25V for EMI requirement. (page 36)
5. Add one circuit for EMI requirement. (page 38)
  - Add PQ116 (2N7002).
  - Add PC190 (0.47UF\_0805) and PC191 (1000PF).
  - Add PD45 (ISSS355).
  - Add PR230 (470 Ohm).
  - Reserved PR229 (0 Ohm), PR228 (0 Ohm) and PR227 (2.2K\_0805).
  - Reserved PQ115 (2N7002).
  - Reserved PC189 (1UF\_0805).

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# P.I.R. (8) LIST

## Revision History

Date: 2001/03/05      REV#:    4A      Description: C3-TEST for H1.6/MP-TEST for H1.5

### 03/05/2001

1. Modify the Res.'s value to meet U36 NM24C16 2nd source's SPEC (Page 26) .
  - R397,R398,R399 change value from 100K ohm to 1K ohm .
2. Modify the FIR related C.K.T. to fix the nun-work issue (Page 28) .
  - Cut the connection between C115.2,C111.2,C525.2,U9.8 and GND signal .
  - Connect C115.2,C111.2,C525.2,U9.8 to JOPEN11.1 .
  - Connect JOPEN11.2 to JOPEN10.1 .
  - Connect JOPEN10.2 to GND signal near C98 side .
3. Make a table to show the H1.5/H1.6 ID selection (Page 25) .
  - Remove R416(10K ohm),R479(10K ohm) and add R420(10K ohm) when selected for H1.6 Celeron .
  - Remove R416(10K ohm),R420(10K ohm) and add R479(10K ohm) when selected for H1.6 PIII .
  - Remove R479(10K ohm) and add R420(10K ohm),R416(10K ohm) when selected for H1.5 PIII .
  - Remove R420(10K ohm) and add R479(10K ohm),R416(10K ohm) when selected for H1.5 Celeron .
4. Add three resistors for EMI solution (Page 17) .
  - Add L17,L13,L3 (0 ohm 0805) to fix the EMI issue .

### 03/09/2001

1. Add R488 10K ohm Res. for platform ID (Page 25) .
  - C3-test (REV:4A) M/B lose it . It will be put into REV:4B M/B and rework on REV:4A .

### 03/19/2001

1. Return the making table for showing the H1.5/H1.6 ID selection action (Page 25) .
  - Add R416(10K ohm),R479(10K ohm) and remove R420(10K ohm) when selected for H1.6 Celeron .
  - Add R416(10K ohm),R420(10K ohm) and remove R479(10K ohm) when selected for H1.6 PIII .
  - Remove R479(10K ohm) and add R420(10K ohm),R416(10K ohm) when selected for H1.5 PIII .
  - Remove R420(10K ohm) and add R479(10K ohm),R416(10K ohm) when selected for H1.5 Celeron .
2. Cancel R488 10K ohm Res. rework for platform ID (Page 25) .
  - C3-test cancel the R488(10K ohm) rework for platform ID selection action but still reserve that to connect GND on REV:4B PCB for future .
3. Change PR181 from 22uF\_6.3V Tan. Cap. to 22uF\_10V Ceramic Cap. for ME (Page 36)

### 03/21/2001

1. Add CAP to fix FIR issue (Page 28) .
  - Add C556(22U\_10V\_1206) to close C111 ASAP on REV:4B PCB . Put C556 to close C111 on REV:4A PCB by rework this time .

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