

Compal Confidential

QAZ00 (Shuriken 13.3) M/B Schematics Document

Intel Sandy Bridge ULV Processor with DDRIII + Cougar Point PCH SFF

LA-7531P

Date : 2011/04/10
Version 0.1 modify

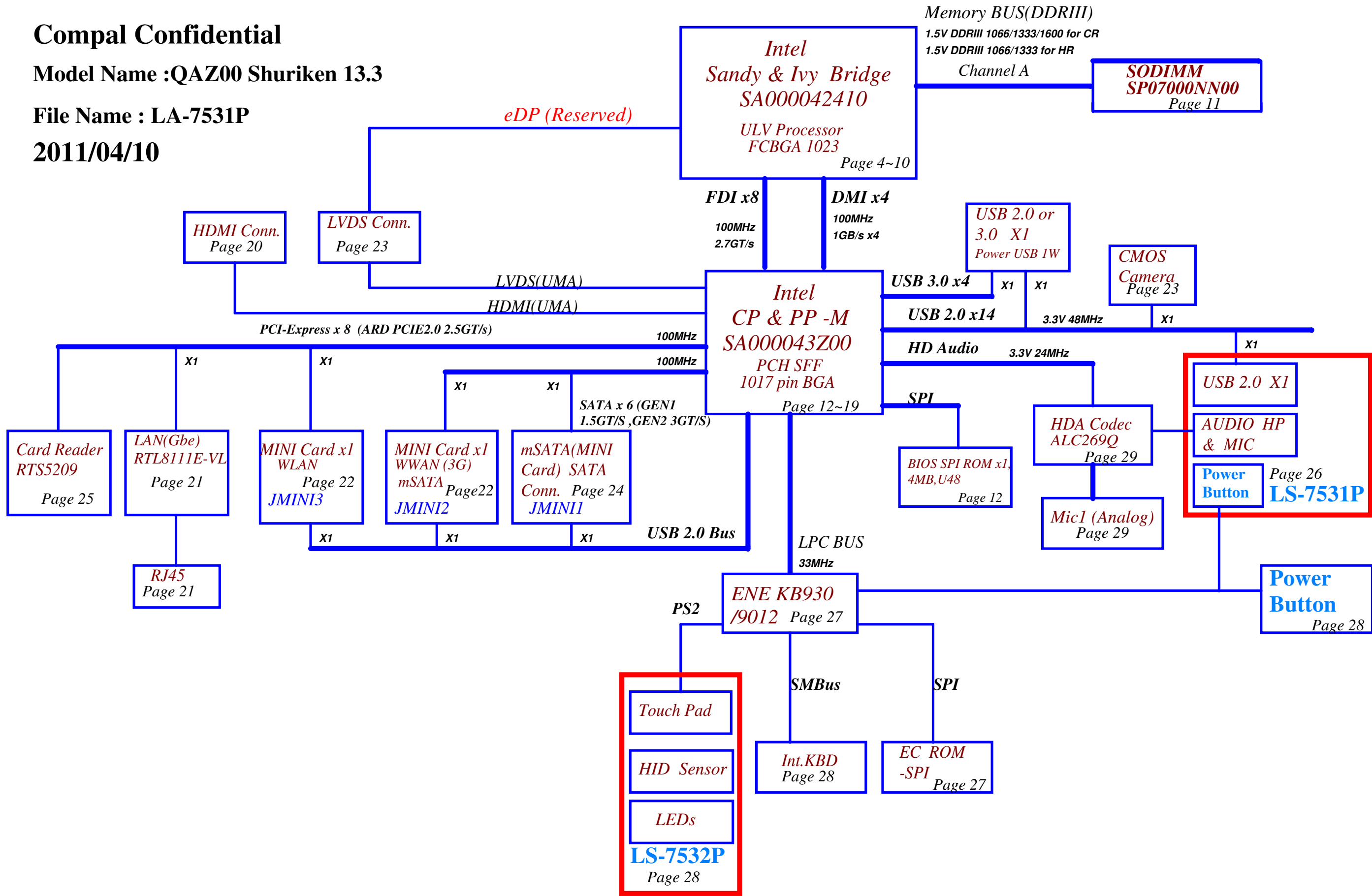
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Issued Date	2010/08/03	Deciphered Date	Title Cover Page	
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Model Name : QAZ00 Shuriken 13.3

File Name : LA-7531P

2011/04/10



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
Mini Card1	
Mini Card2	
Mini Card3	

2011/04/07 Modify

SMBUS Control Table

	SOURCE	BATT	MIINI1	MINI2	MINI3	SODIMM	EC_SMB_CK2 PCH_SMBDATA	PCH_SMBCLK PCH_SMBDATA
EC_SMB_CK1 EC_SMB_DA1	KB930	V	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	X	X	X	O	V
PCH_SMBCLK PCH_SMBDATA	PCH	X	V	V	V	V	V	O
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	X	X	X	X



CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JMINI1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table 2011/04/09 Check

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	
		1	USB/B (Right Side)
		2	
		3	Camera
		4	Mini Card(WLAN)
		5	WWAN (3G)
		6	
EHCI2	UHCI3	7	mSATA
		8	
		9	USB/B (Right Side)
		10	
		11	
		12	
		13	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	CARD READER	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

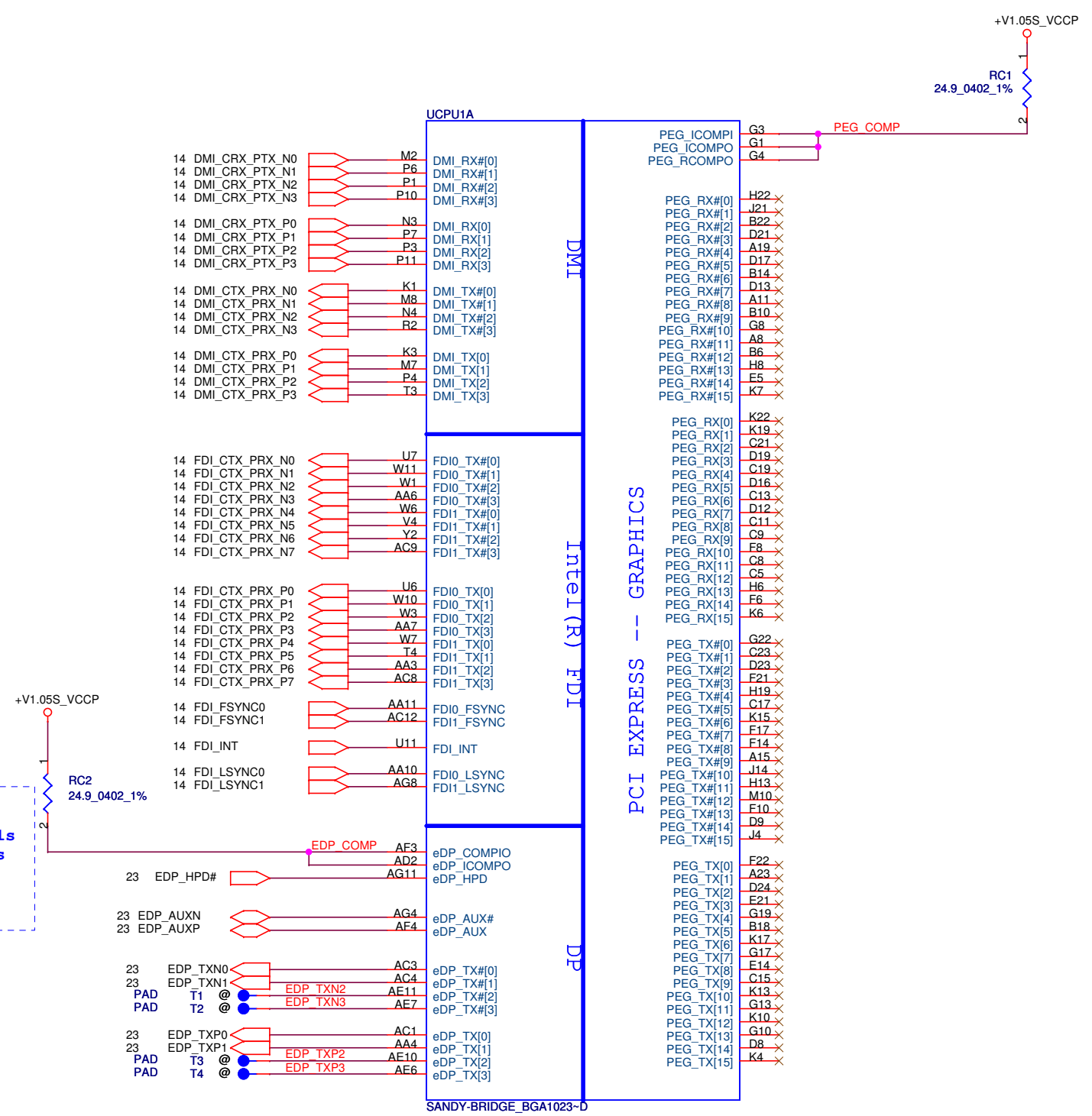
Symbol Note :
 : means Digital Ground
 : means Analog Ground

Option	@		HDMI@		EMI@
UMA	X	X	V	X	X

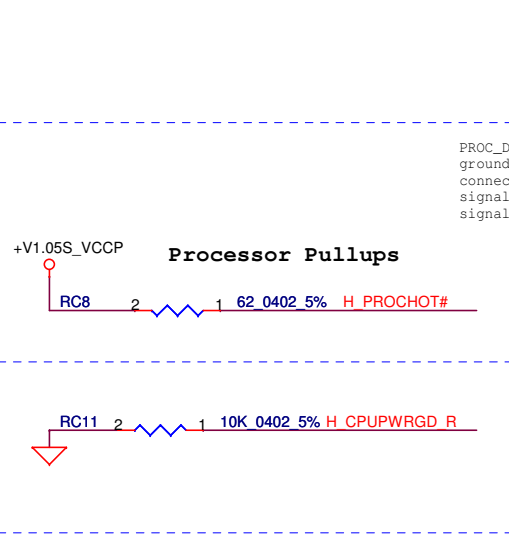
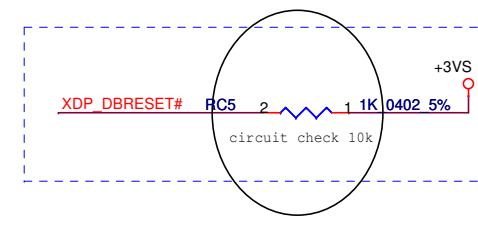
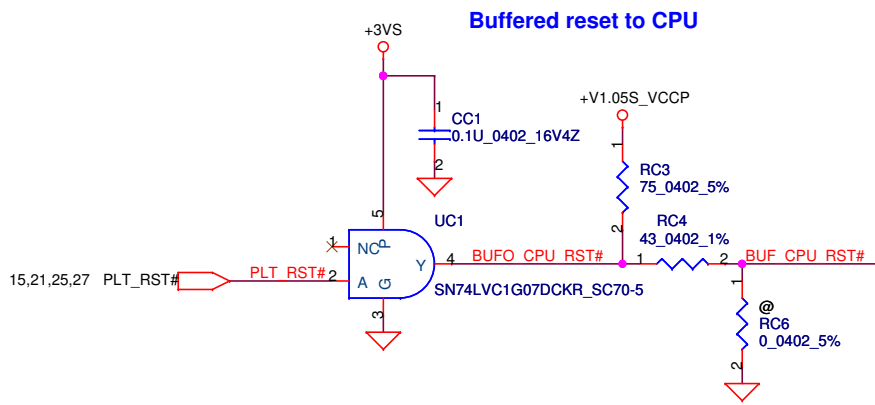
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eDP_COMPPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

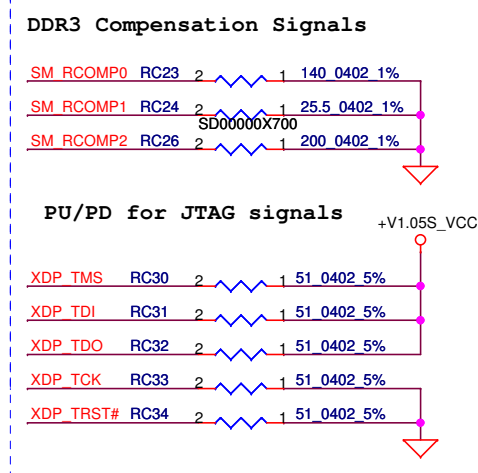
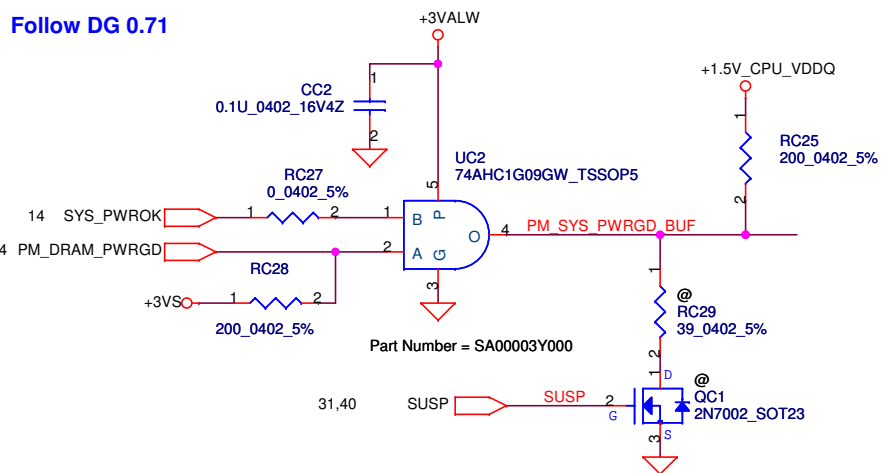
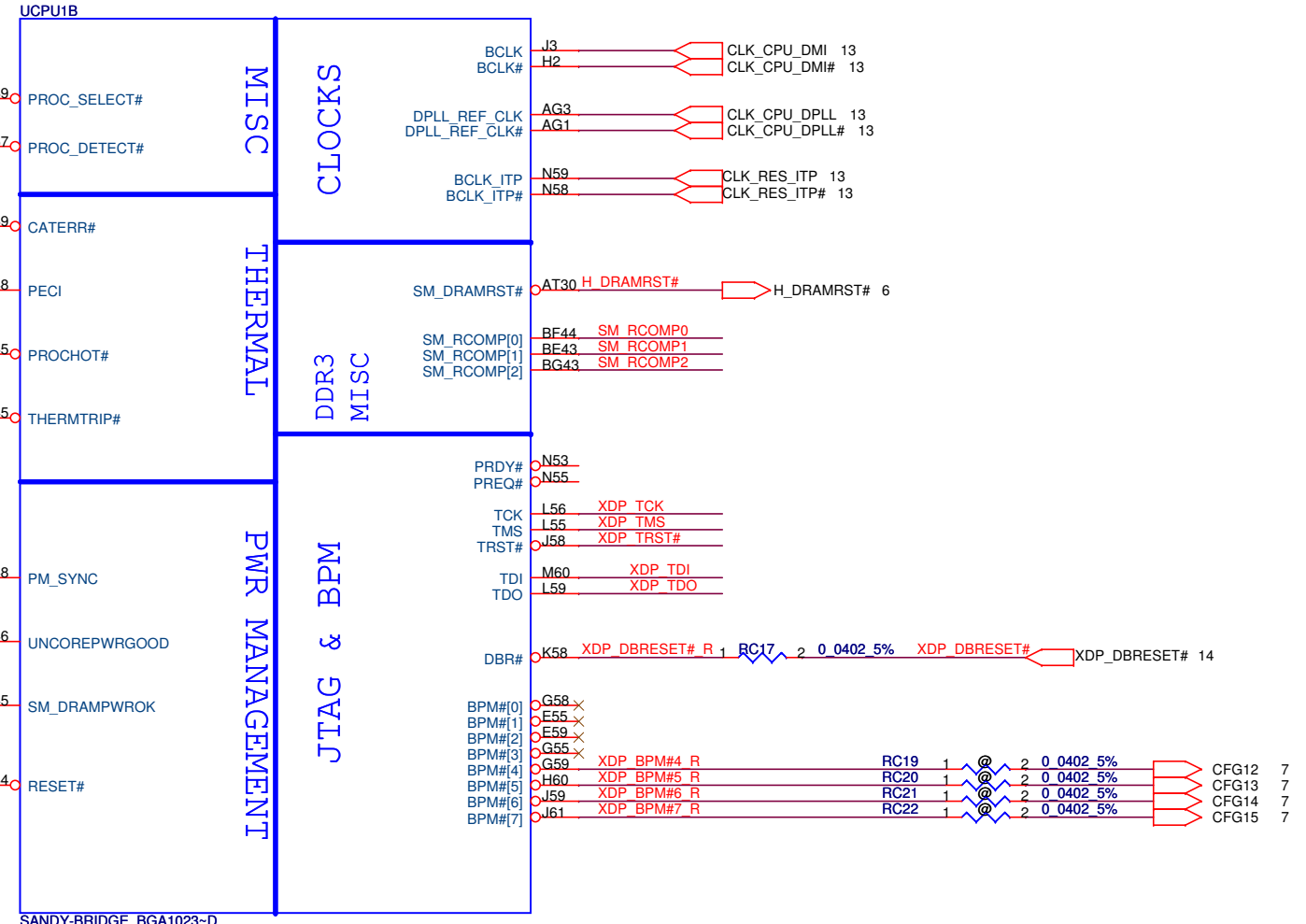
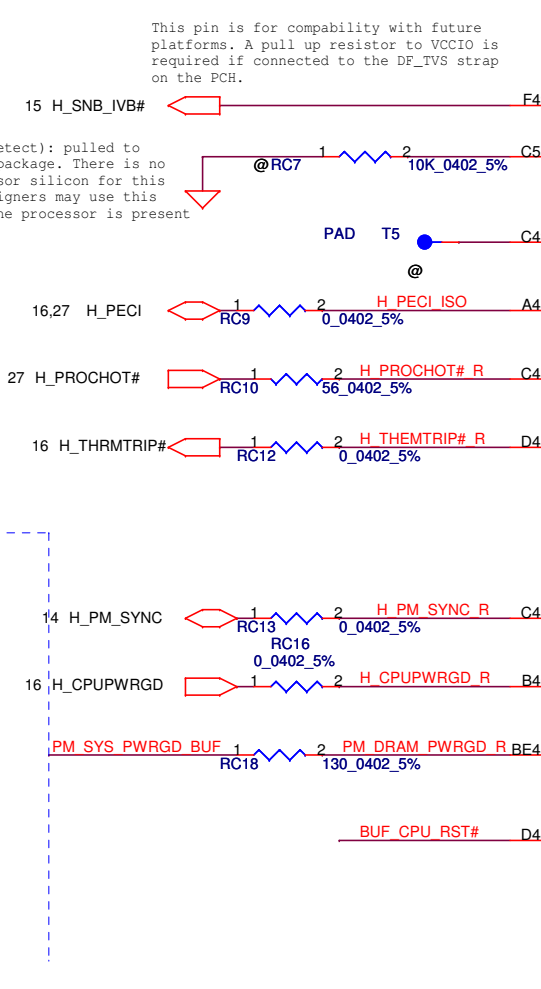
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



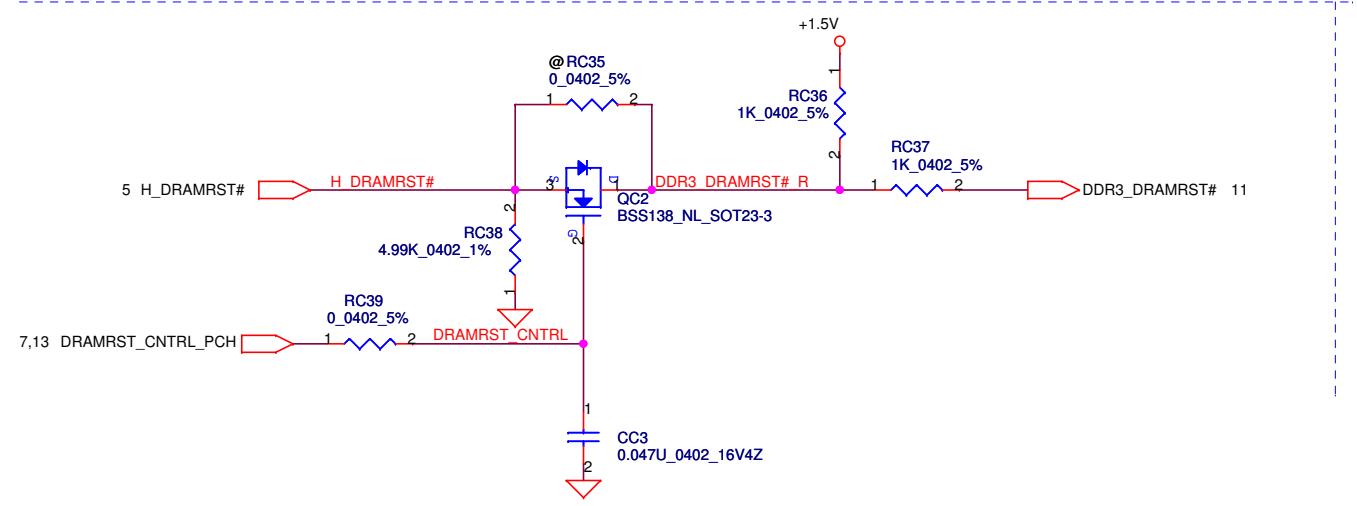
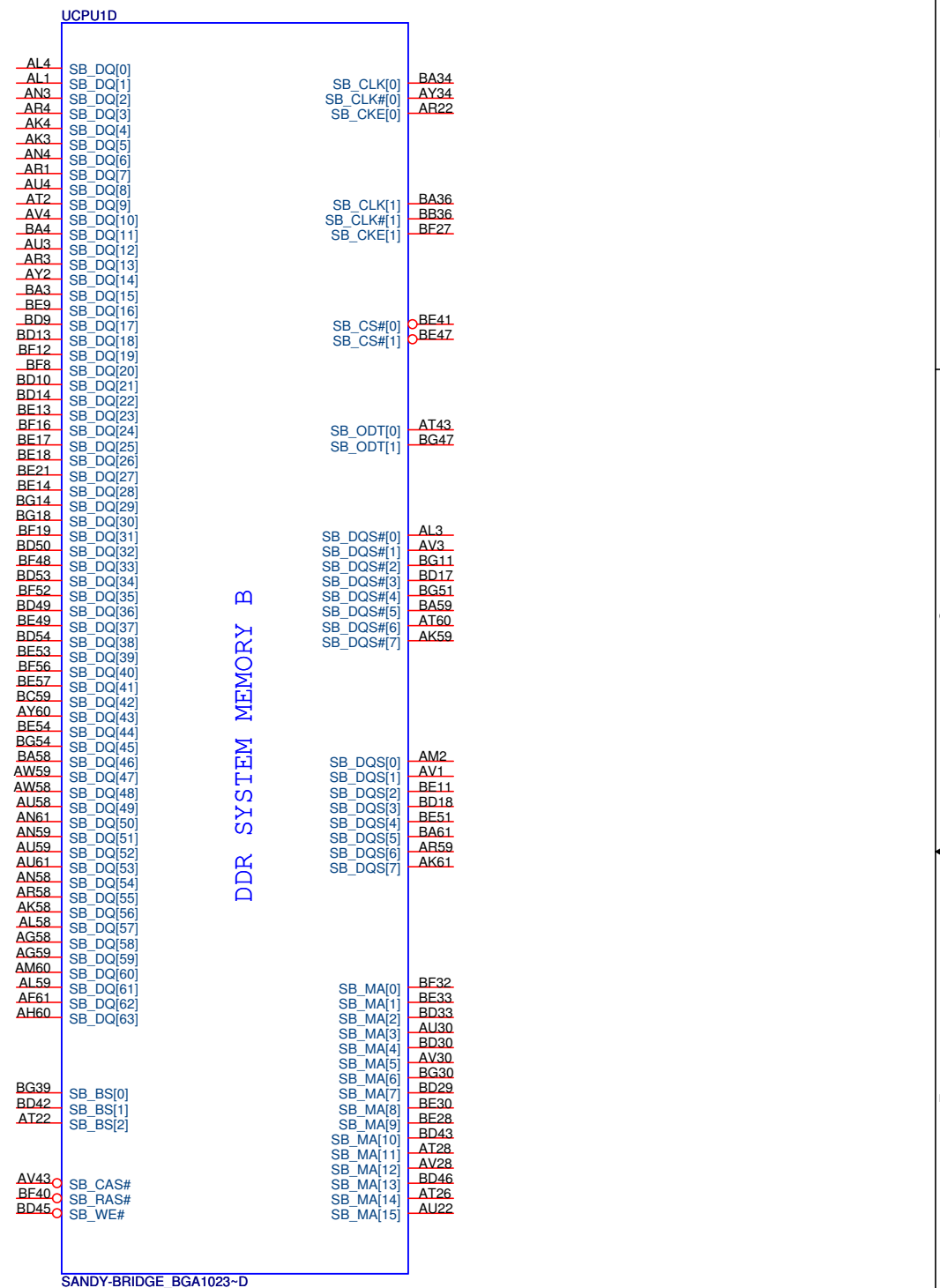
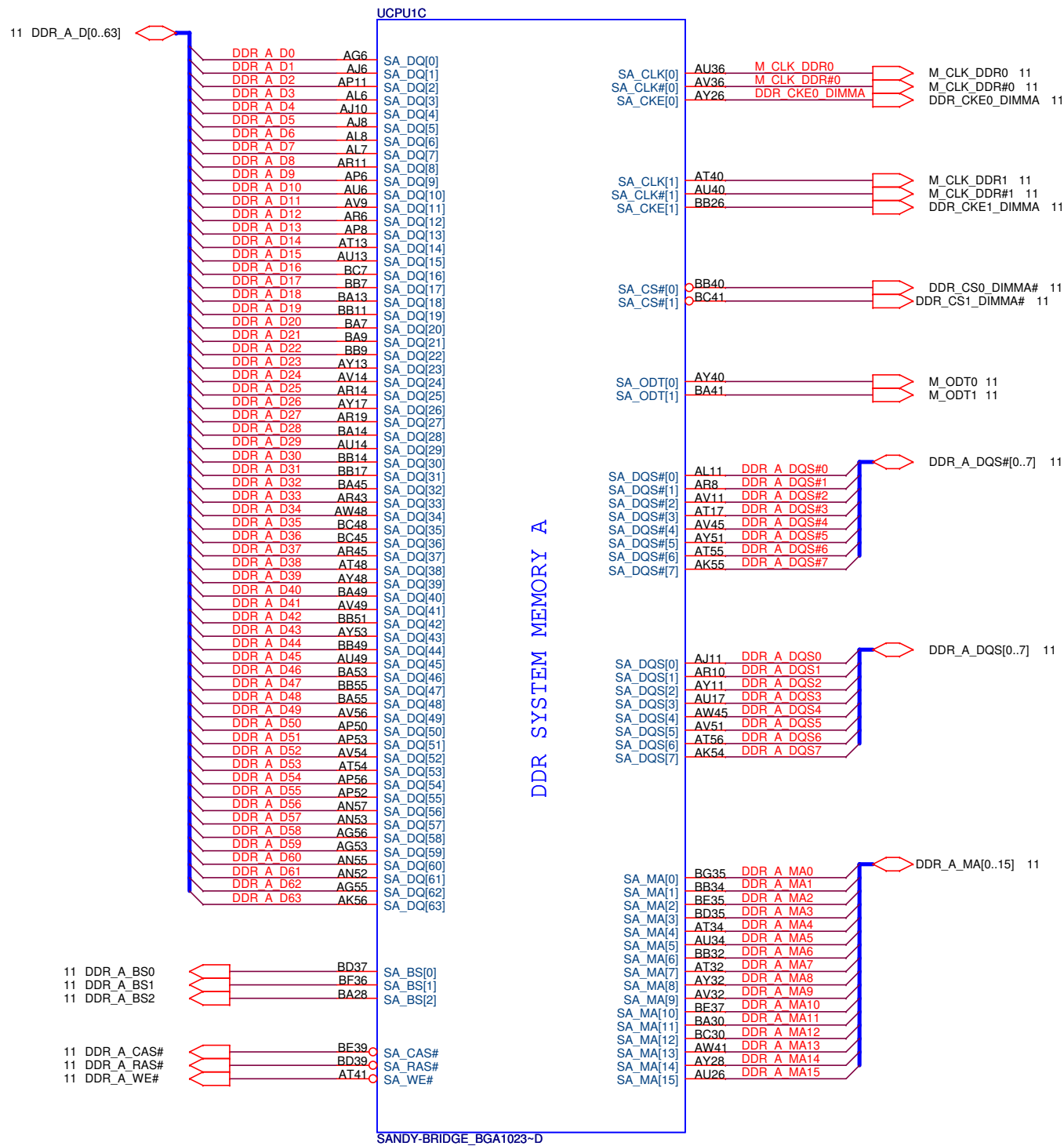
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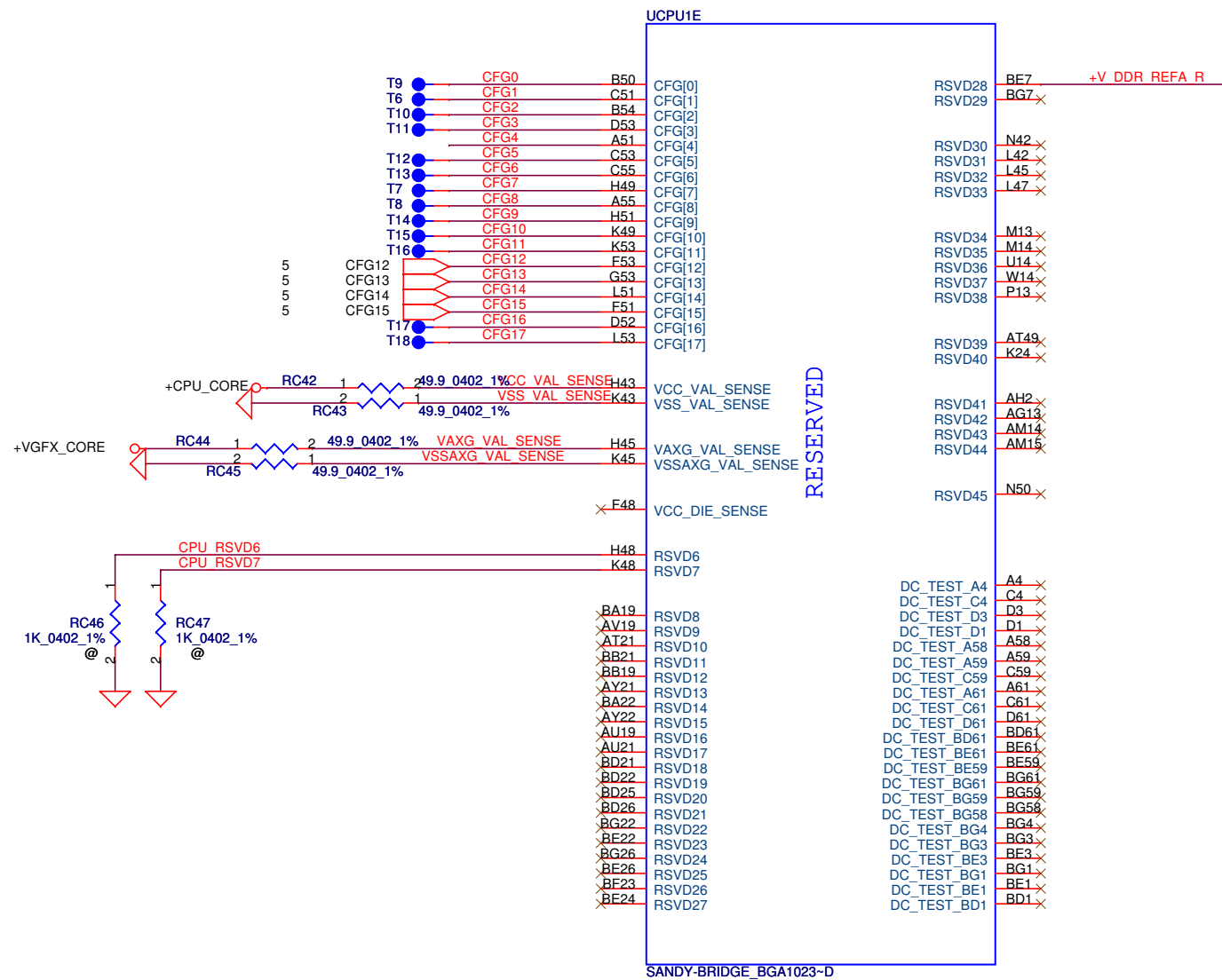
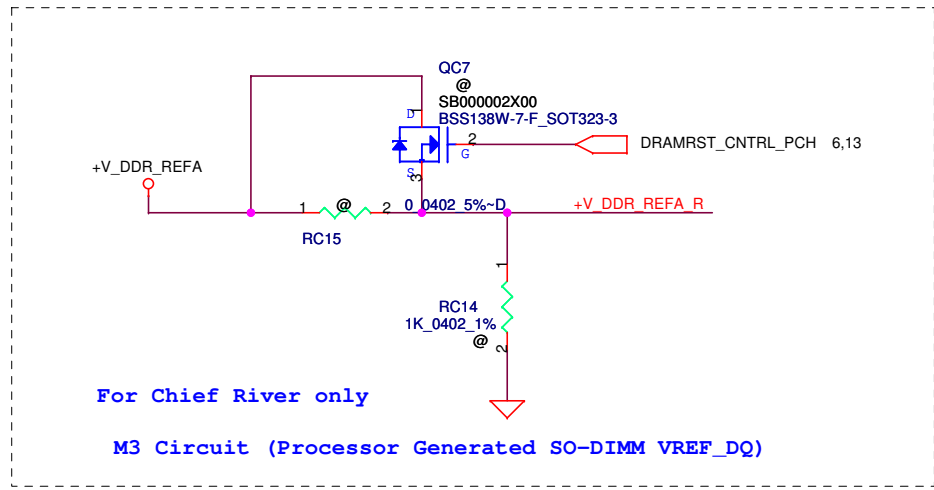
PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present



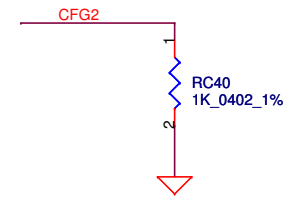
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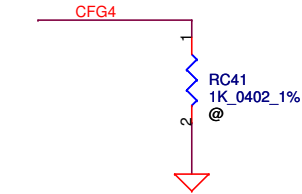
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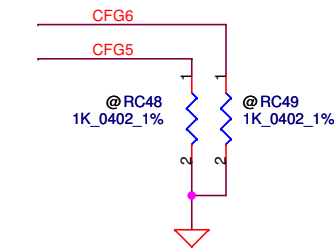
CFG Straps for Processor



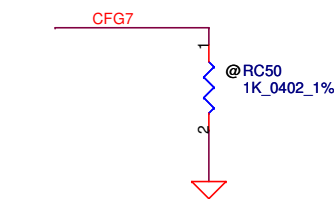
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



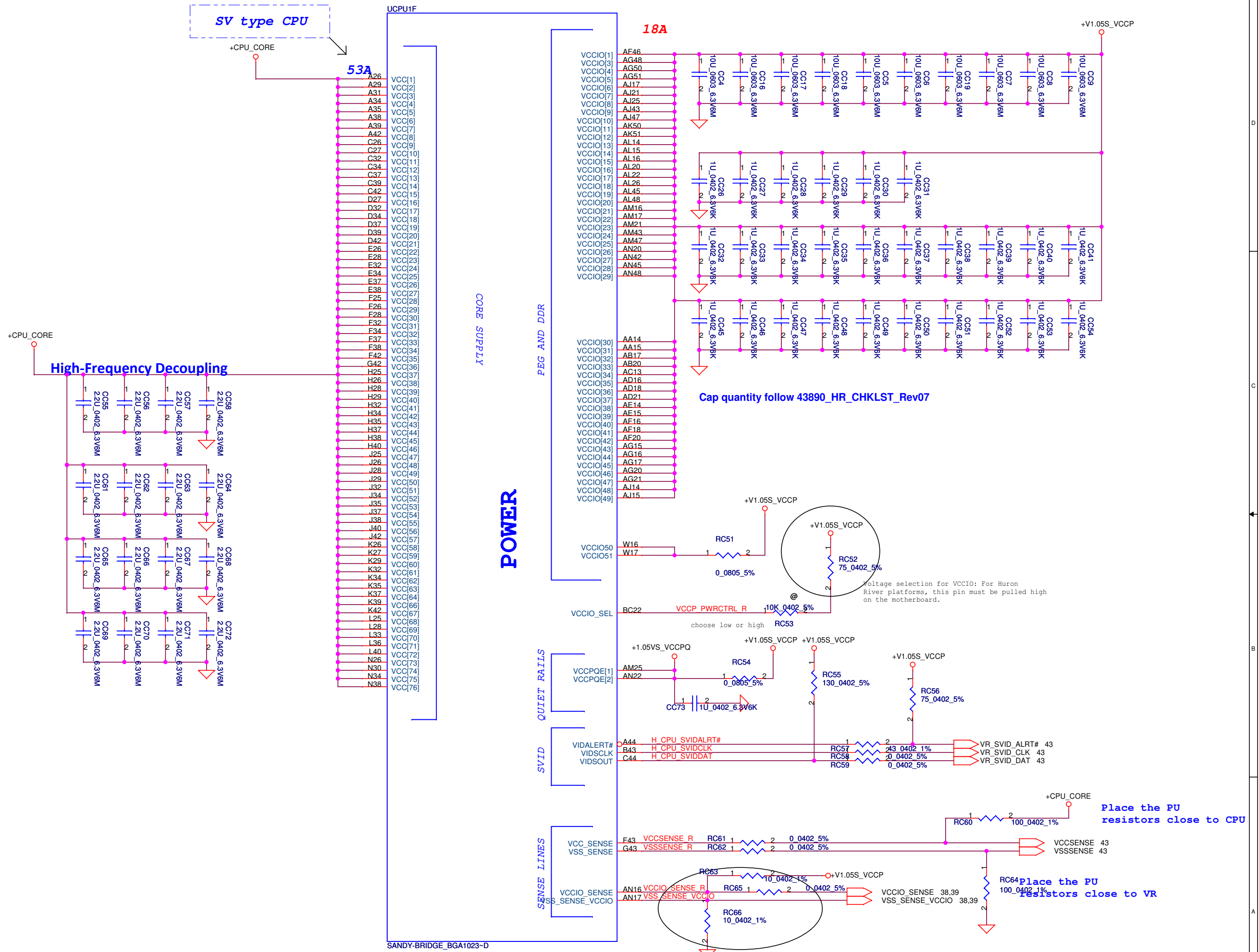
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



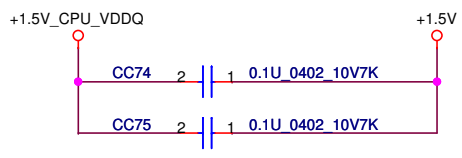
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



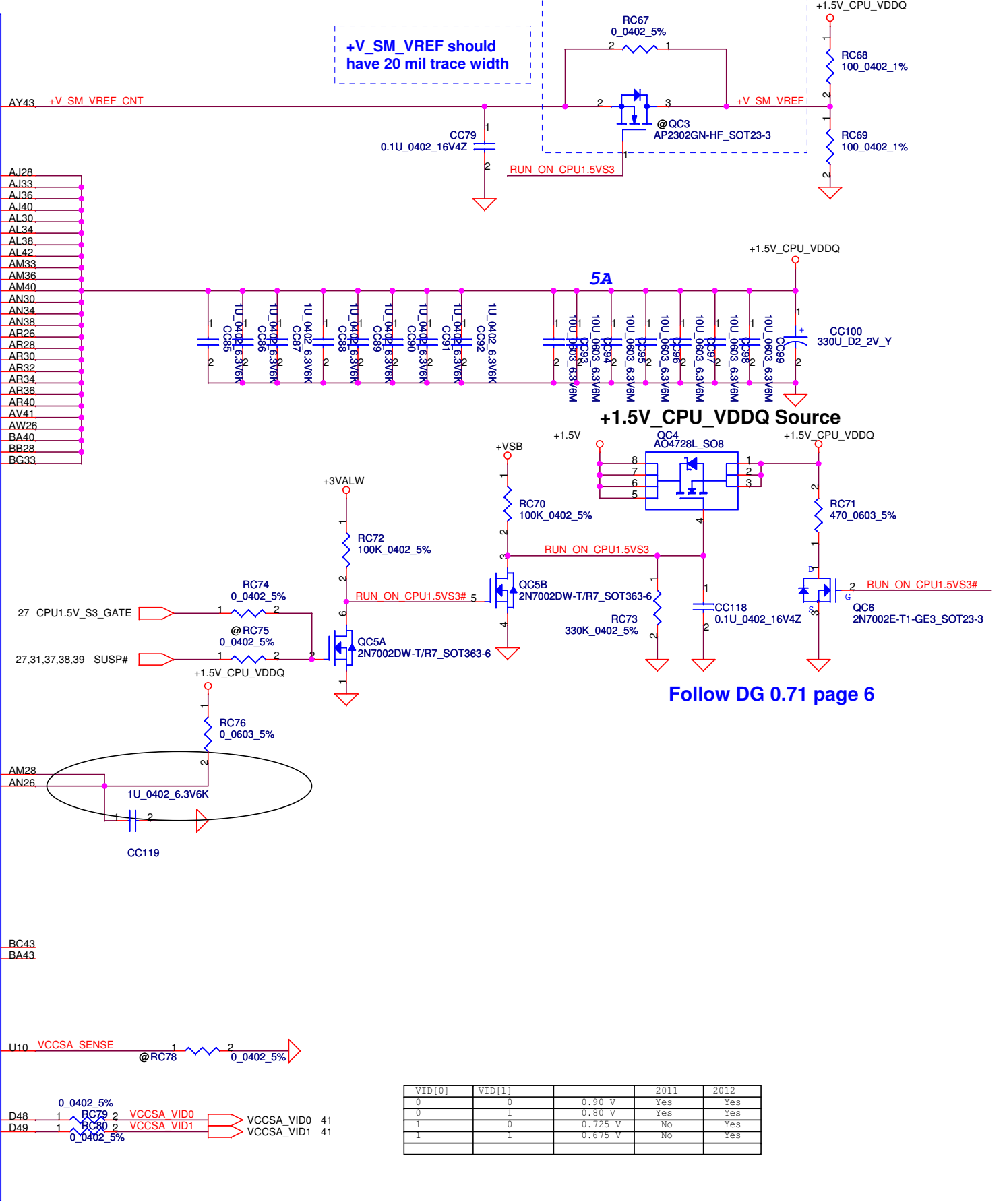
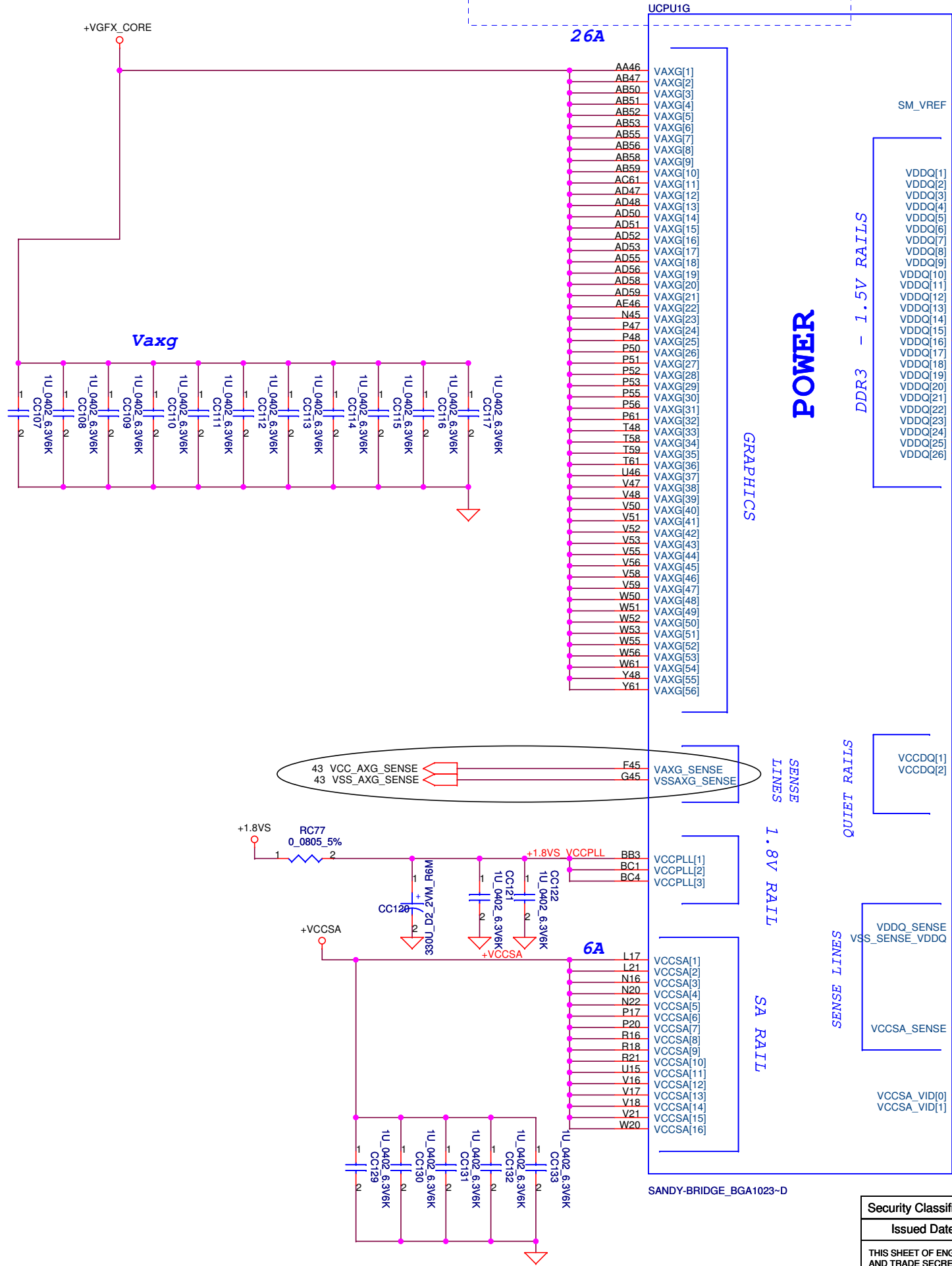
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

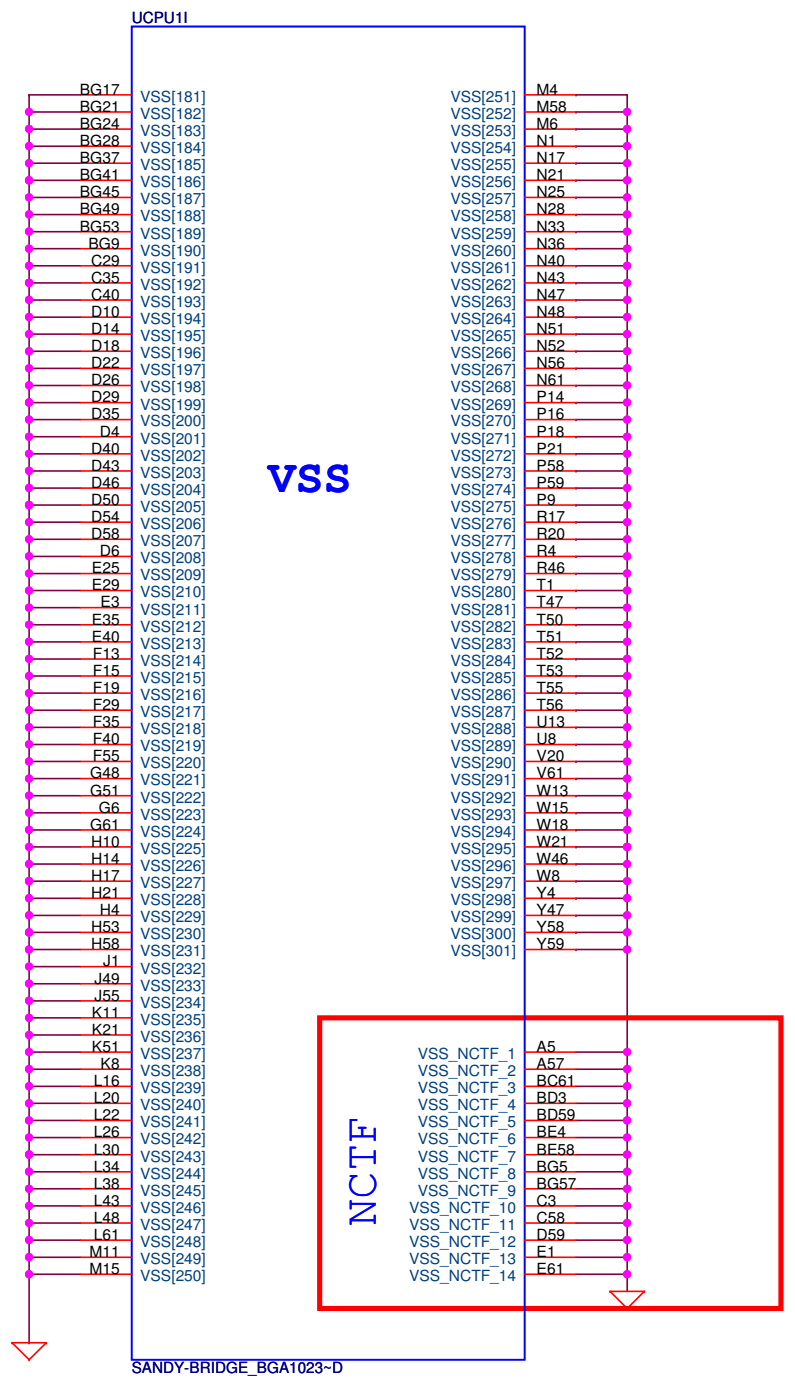
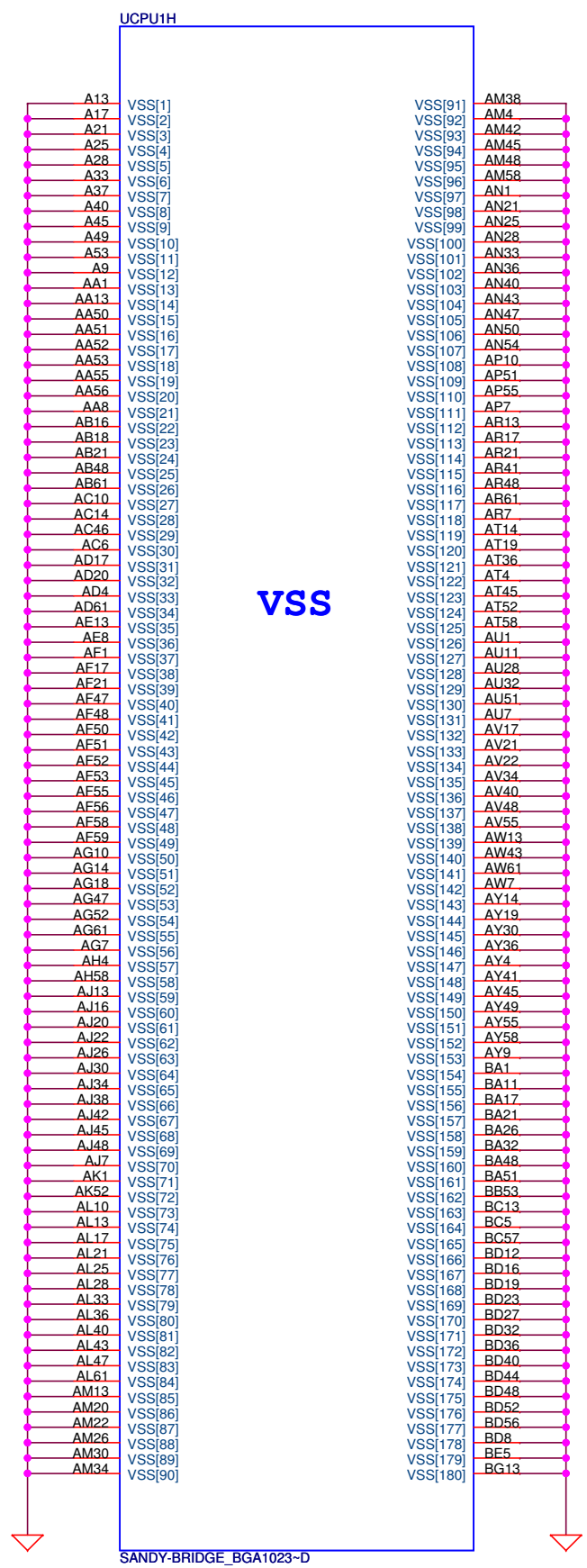


+V_SM_VREF should have 20 mil trace width

Follow DG 0.71 page 6

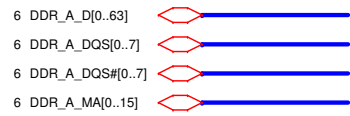
VID[0]	VID[1]	Voltage	2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

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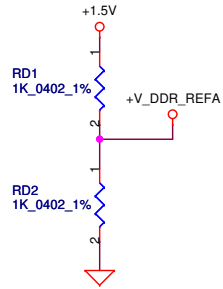


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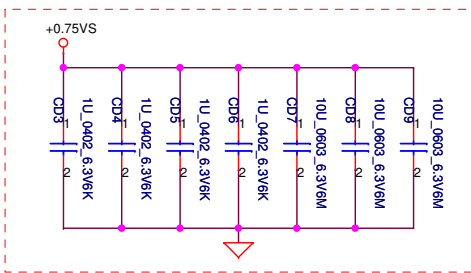
DDR3 SO-DIMM A



Delete DDR_A_DM[0..7]

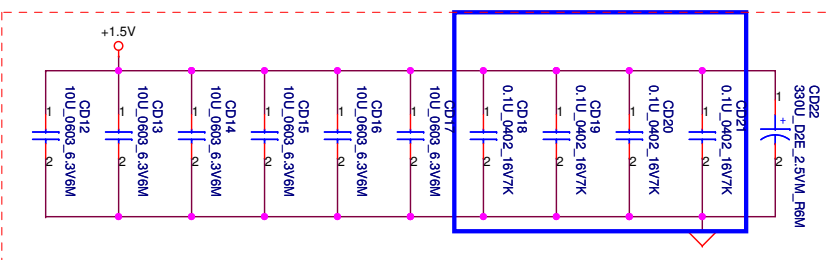


Layout Note:
Place near JDIMM1.203 & JDIMM1.204



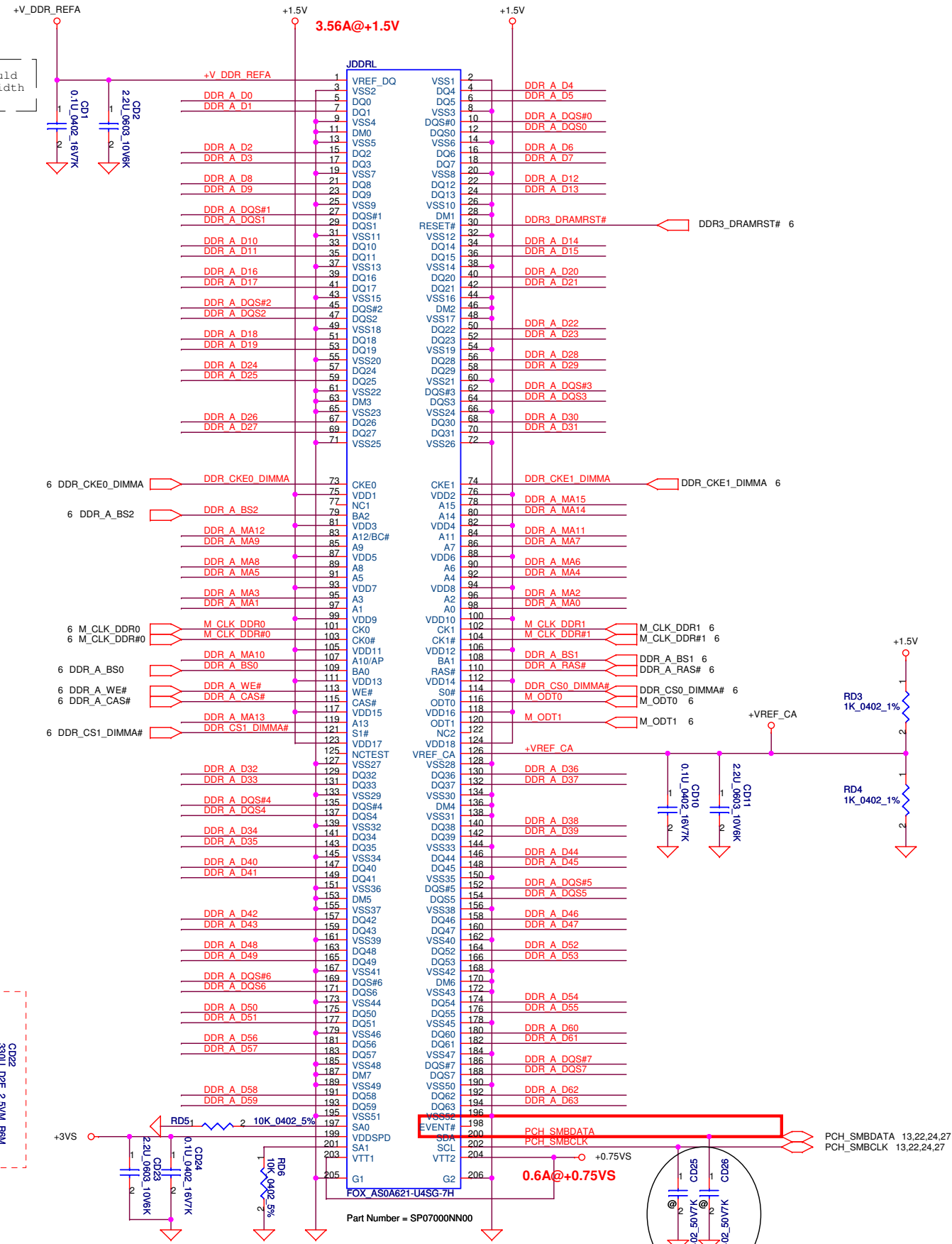
Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



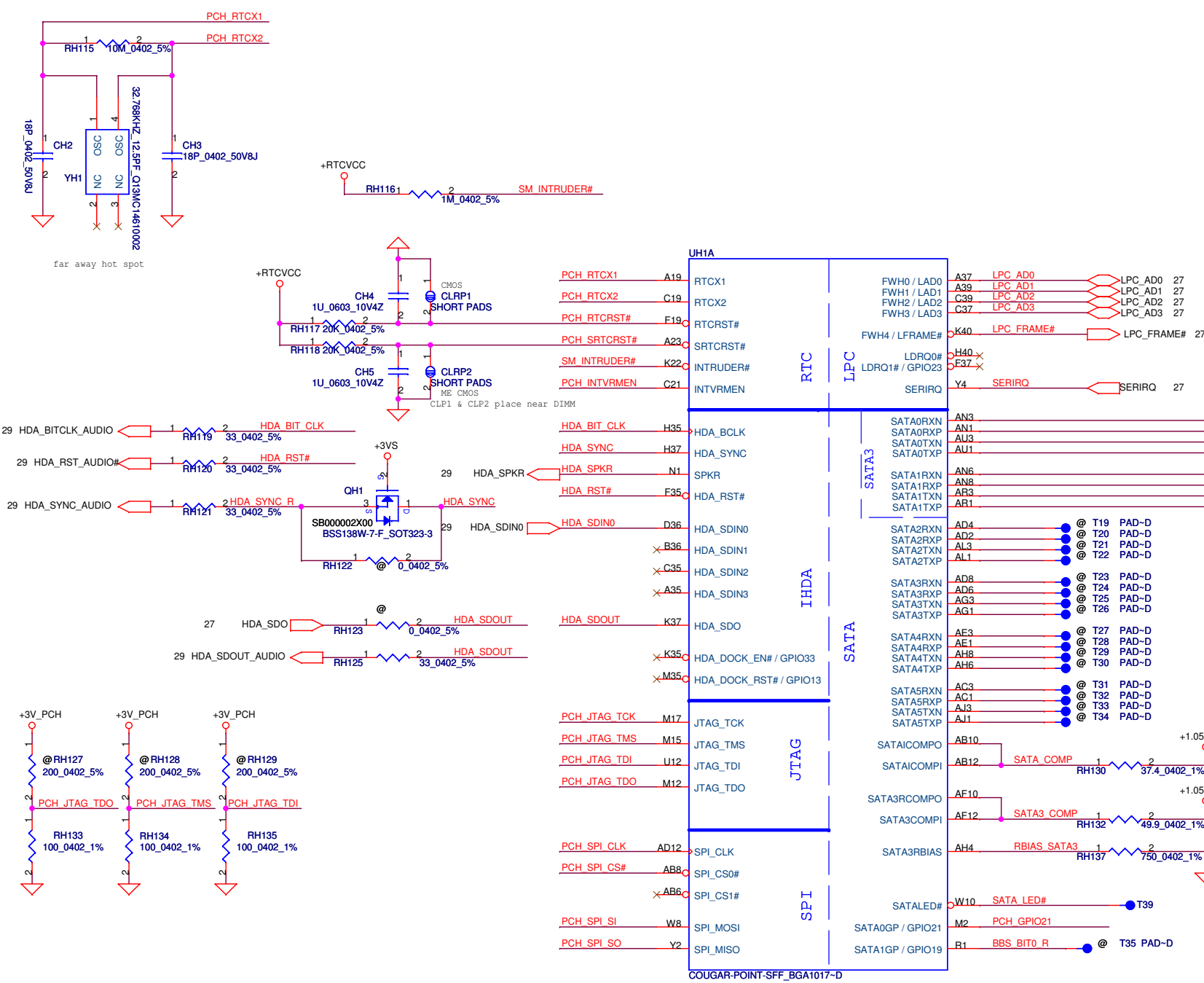
DDR3 SO-DIMM A

All VREF traces should have 10 mil trace width

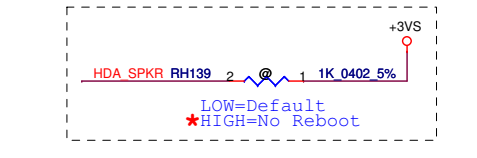
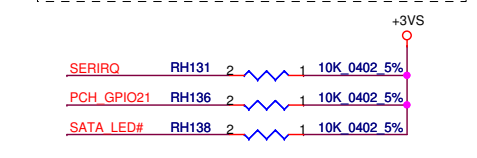
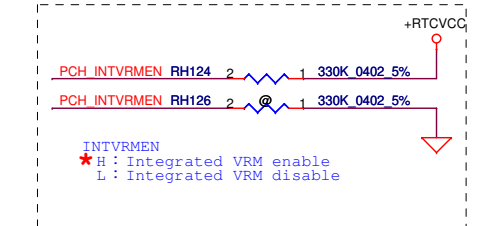


TOP SLOT

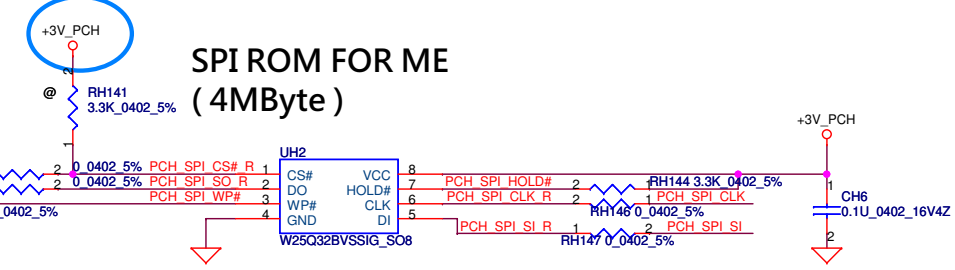
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msATA PAGE24
Combo MMAX & msATA mini Card



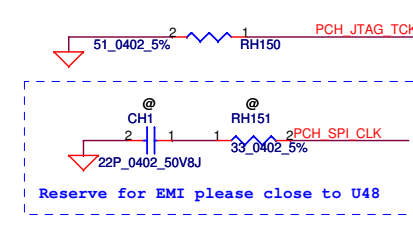
SPI ROM FOR ME (4MByte)



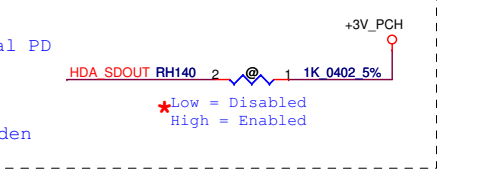
SPI BIOS Pinout

(1) CS#	(5) DIO
(2) DO	(6) CLK
(3) WP#	(7) HOLD#
(4) GND	(8) VCC

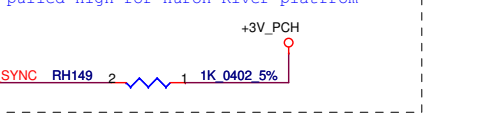
W25X32



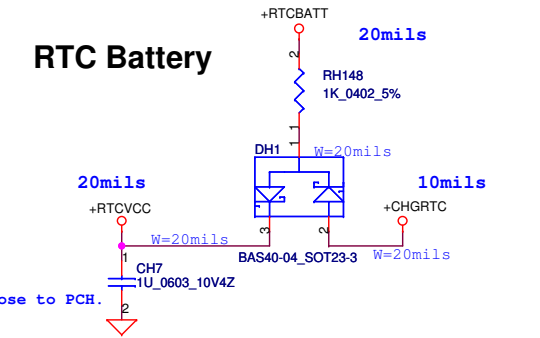
HDA_SDO
ME debug mode, this signal has a weak internal PD
L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden



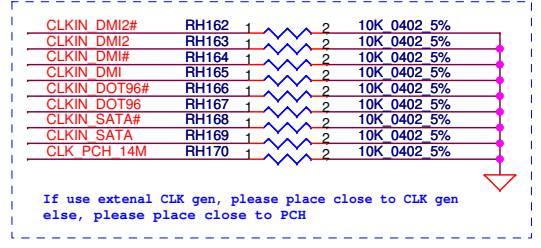
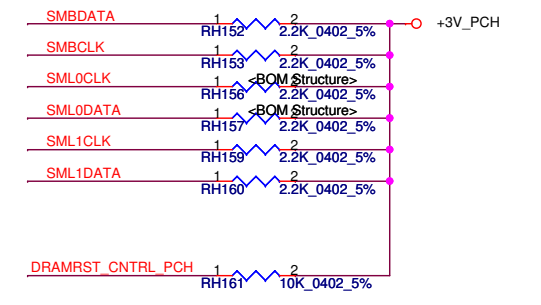
HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by 1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platform



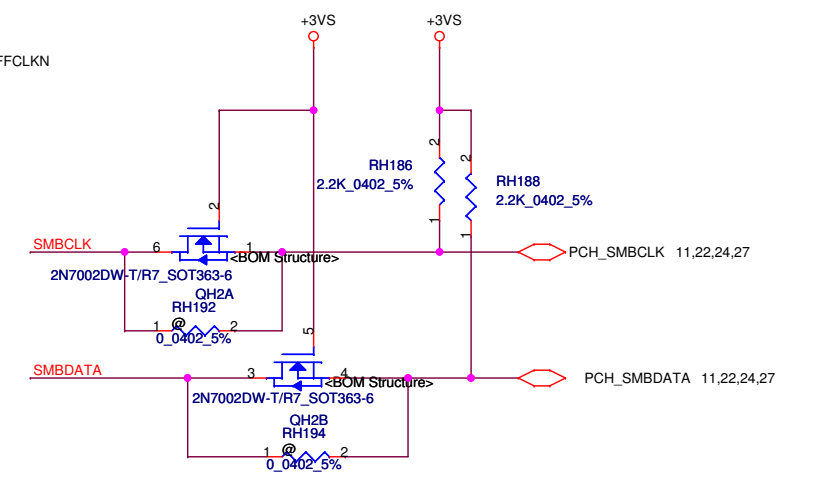
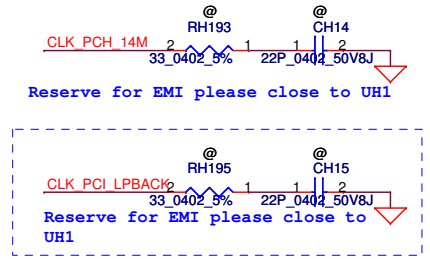
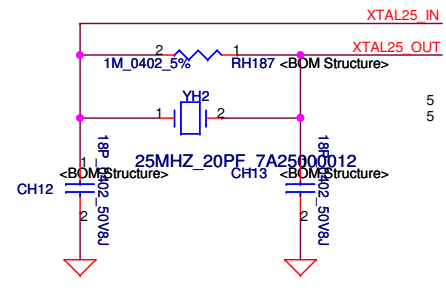
RTC Battery



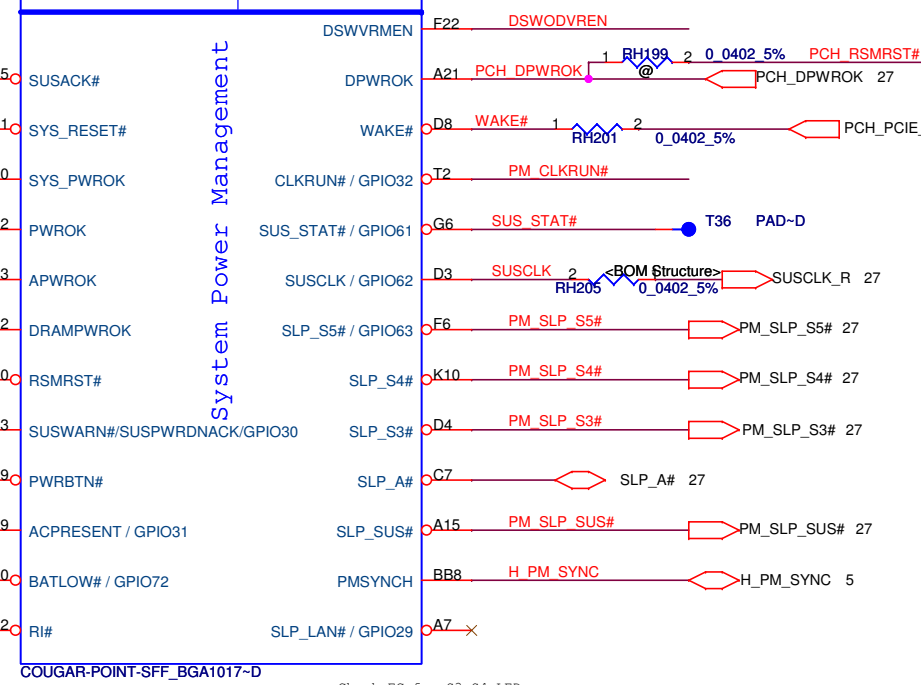
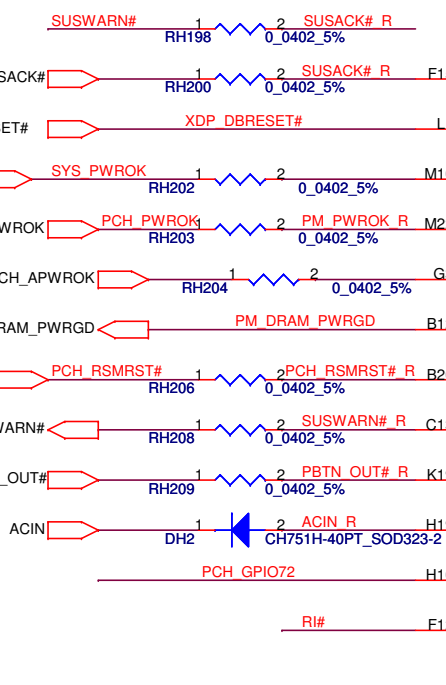
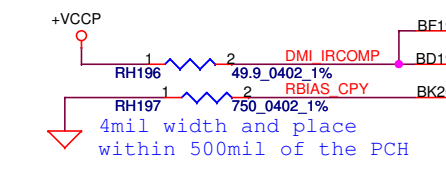
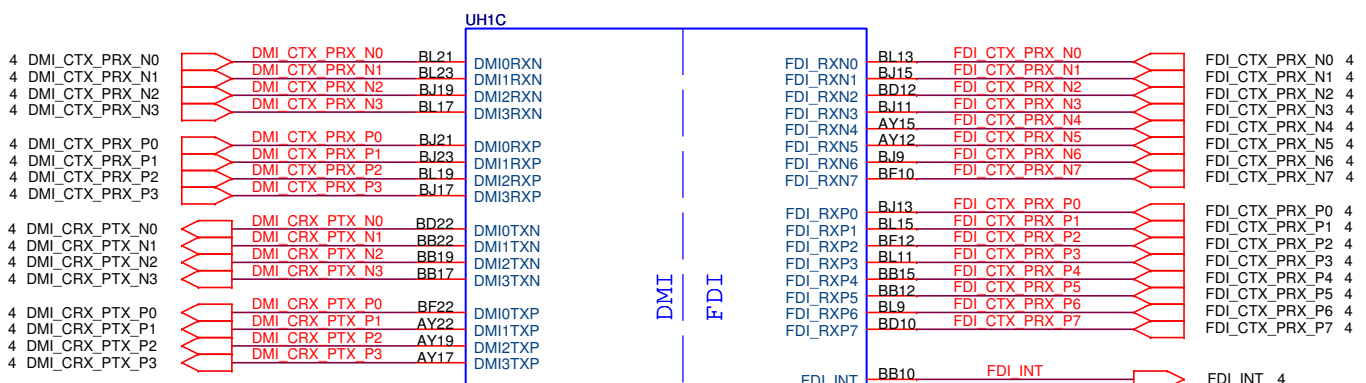
Security Classification	Compal Secret Data		Title	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	PCH (1/8) SATA,HDA,SPI, LPC
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				Document Number
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				0.1
				Date:
				Sunday, April 10, 2011
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				12 of 45



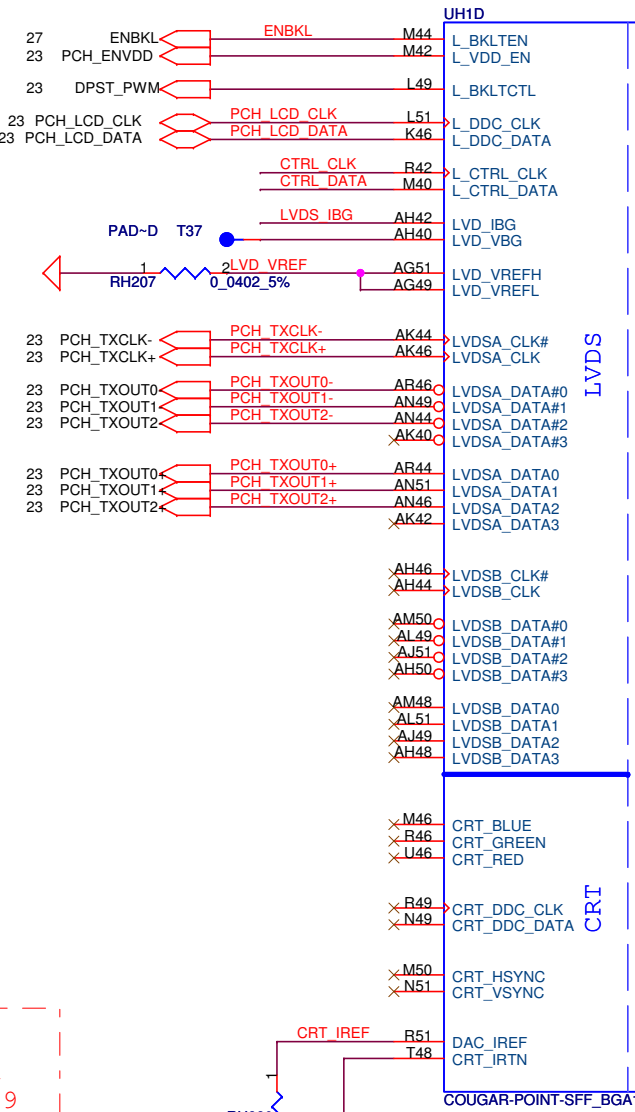
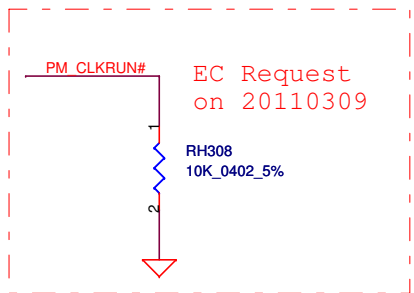
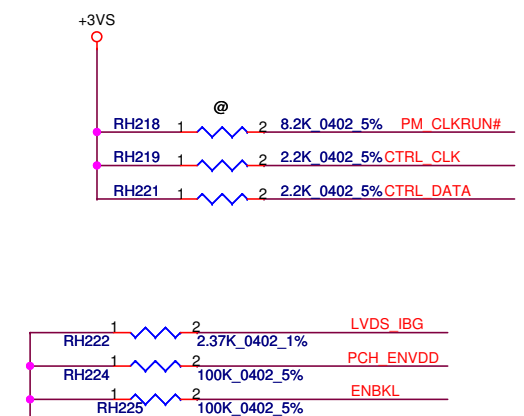
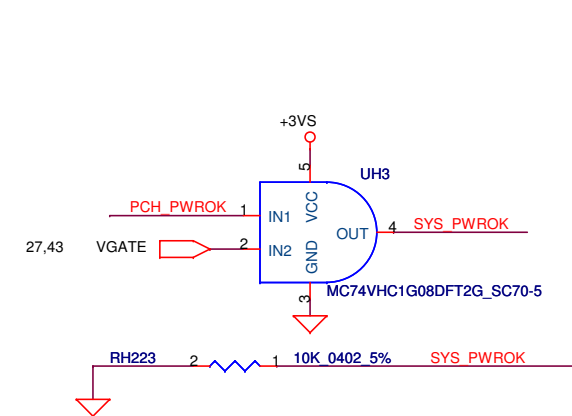
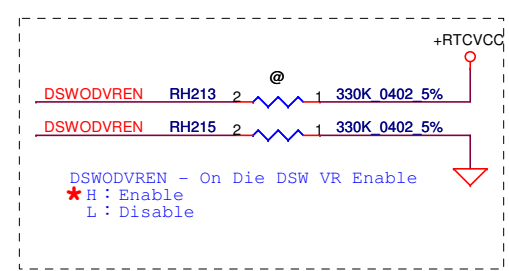
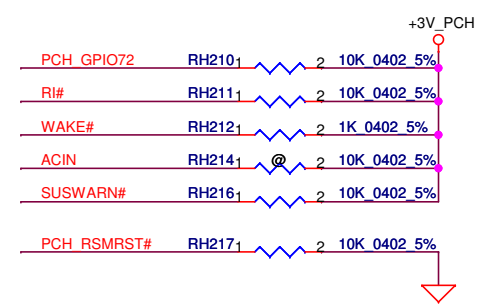
Total device
20090512
add double mosfet prevent
ATI M92 electric leakage



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Size	Document Number	LA-7531P		Rev
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Date:	Sunday, April 10, 2011	Sheet	13	of 45

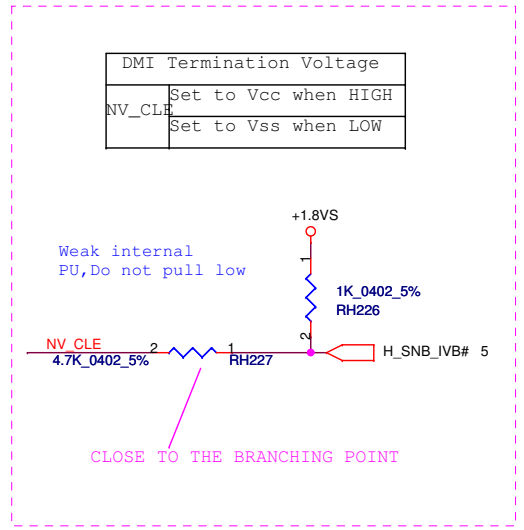
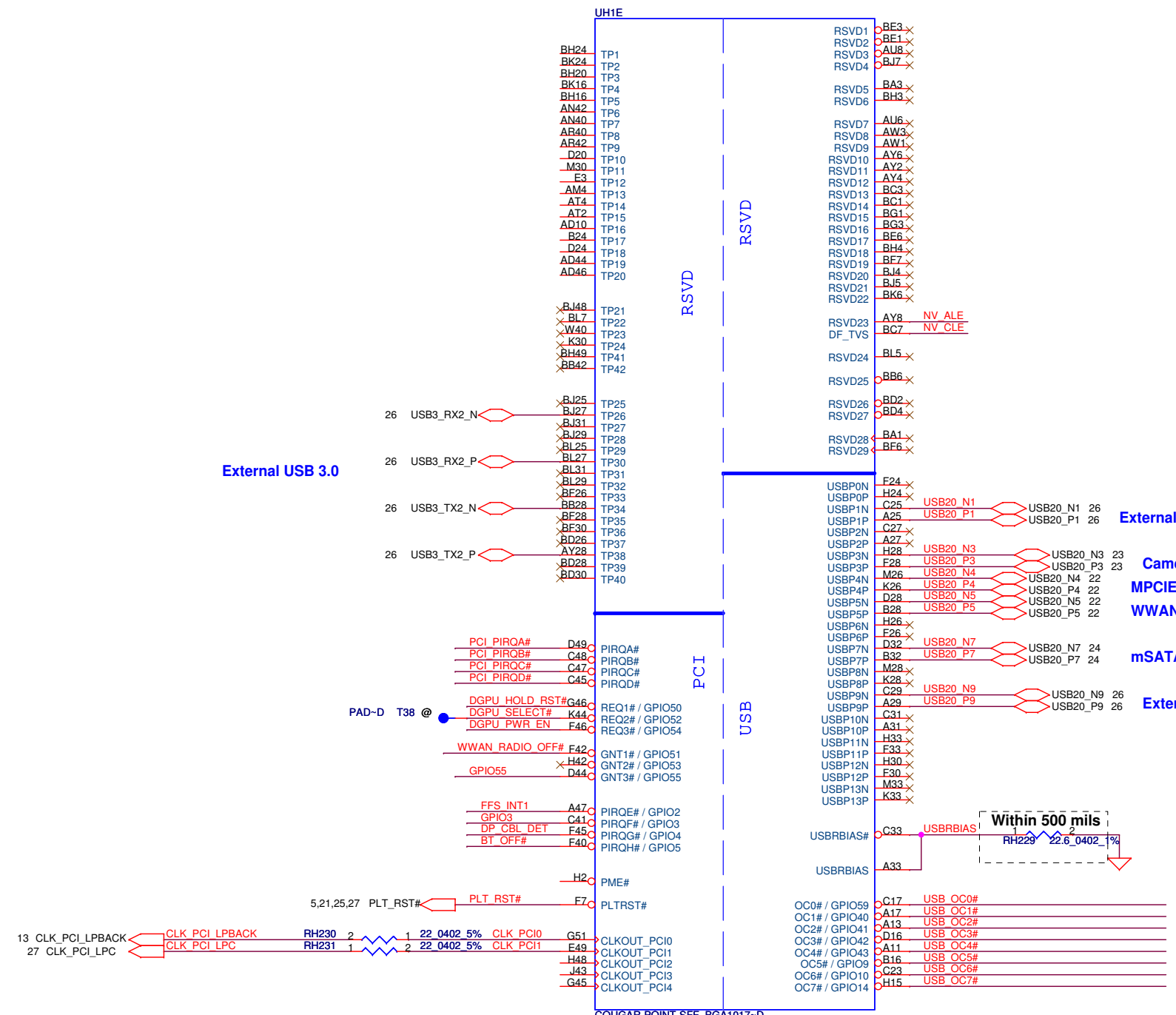


COUGAR-POINT-SFF_BGA1017-D
Part Number = SA000043Z00
Check EC for S3 S4 LED

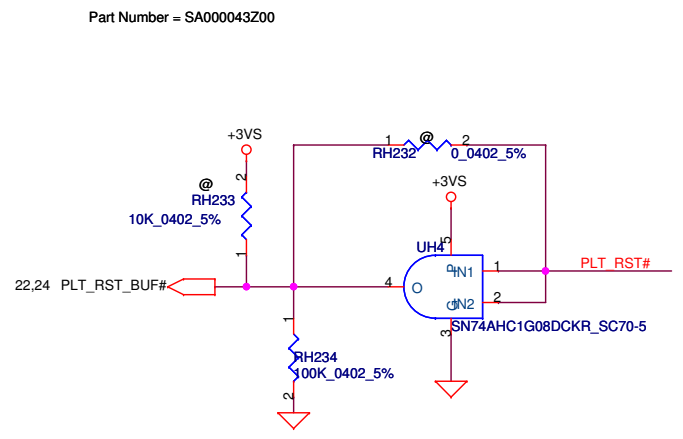
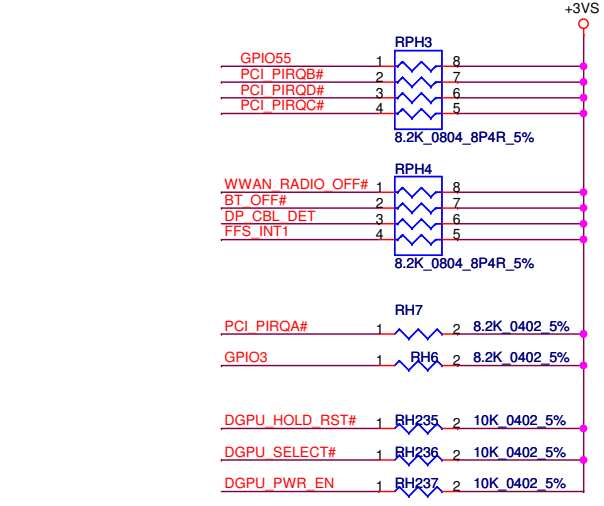
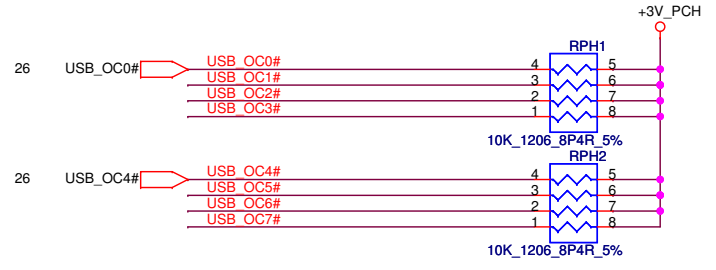
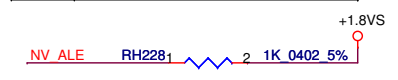


COUGAR-POINT-SFF_BGA1017-D
PART_NUMBER = SA000043Z00

Security Classification	Compal Secret Data		Title	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	PCH (3/8) DMI,FDI,PM,GFX,DP
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				0.1
				Date
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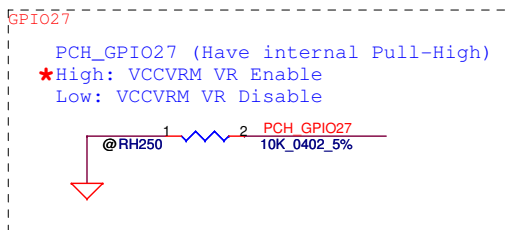
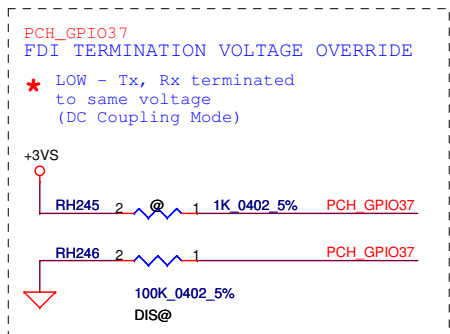
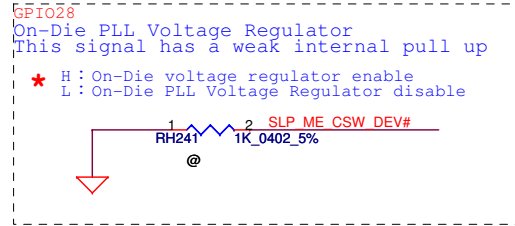


Intel Anti-Theft Techonlogy	
NV_ALE	High=Enabled
NV_ALE	Low=Disable(floating) *



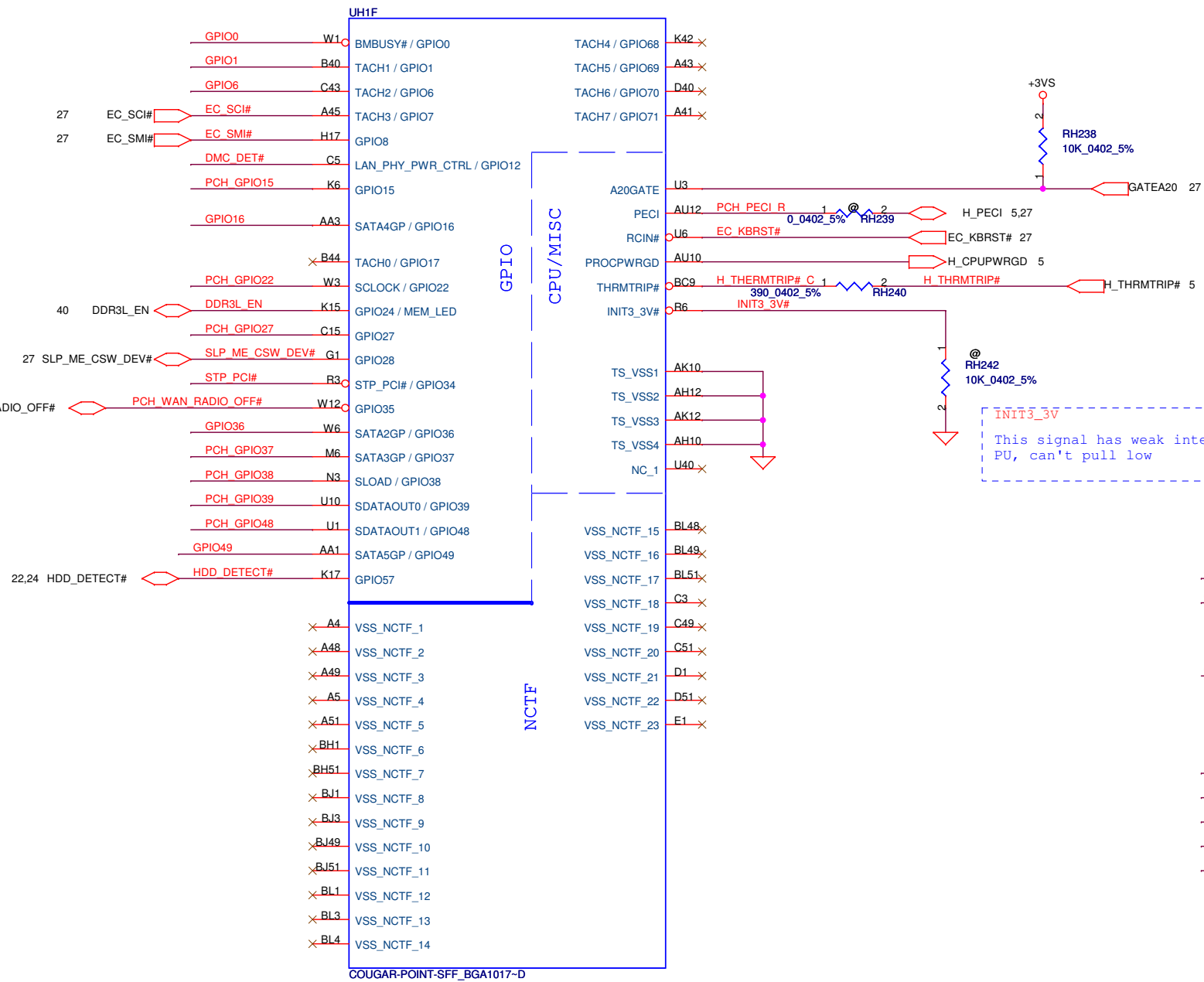
(For USB Port 9)

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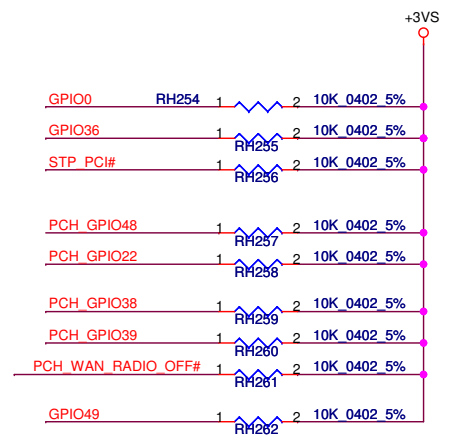
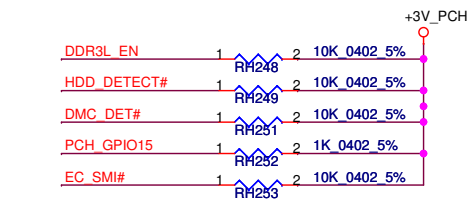
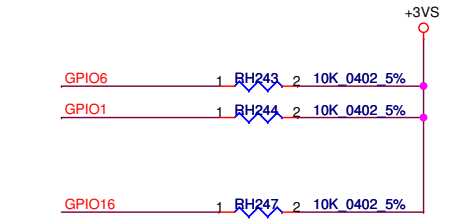


PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

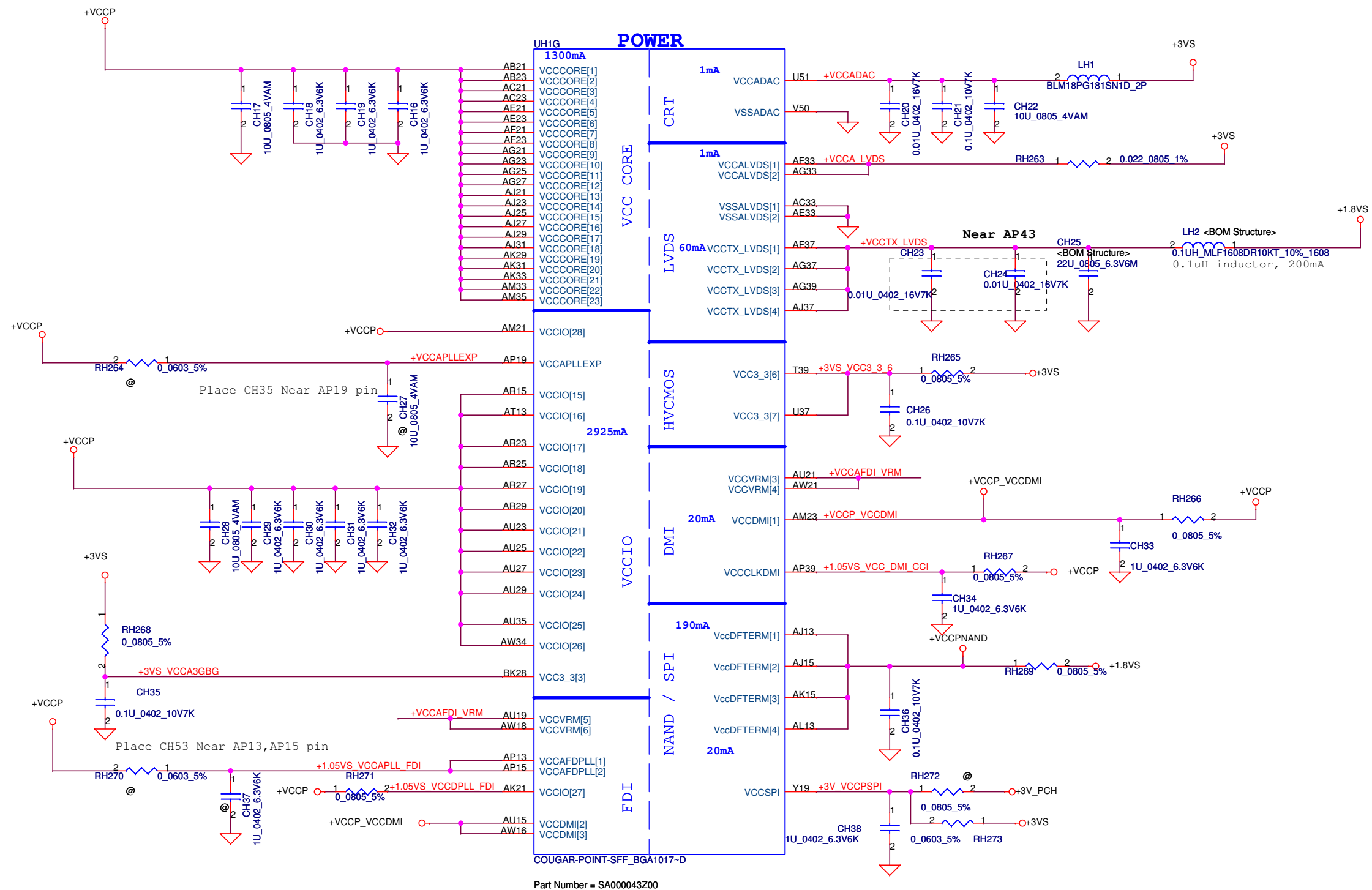
Please refer to Huron River Debug Board DG 0.5



Part Number = SA000043200

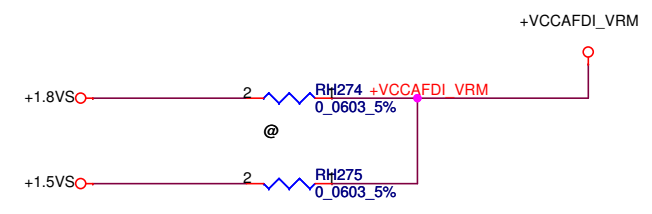


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Size	Document Number	Date		Sheet	Rev
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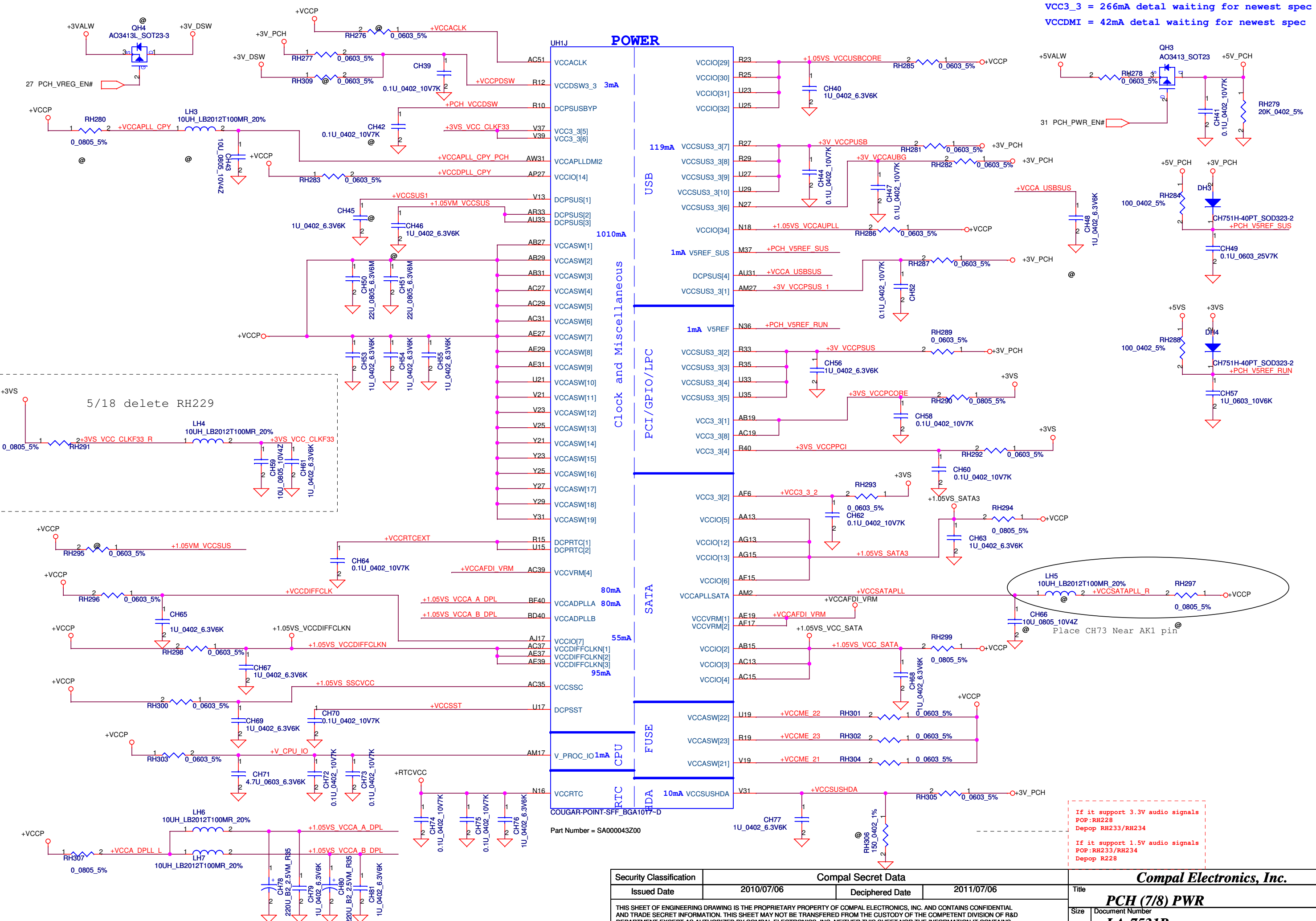
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detail waiting for newest spec



5/18 modified

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

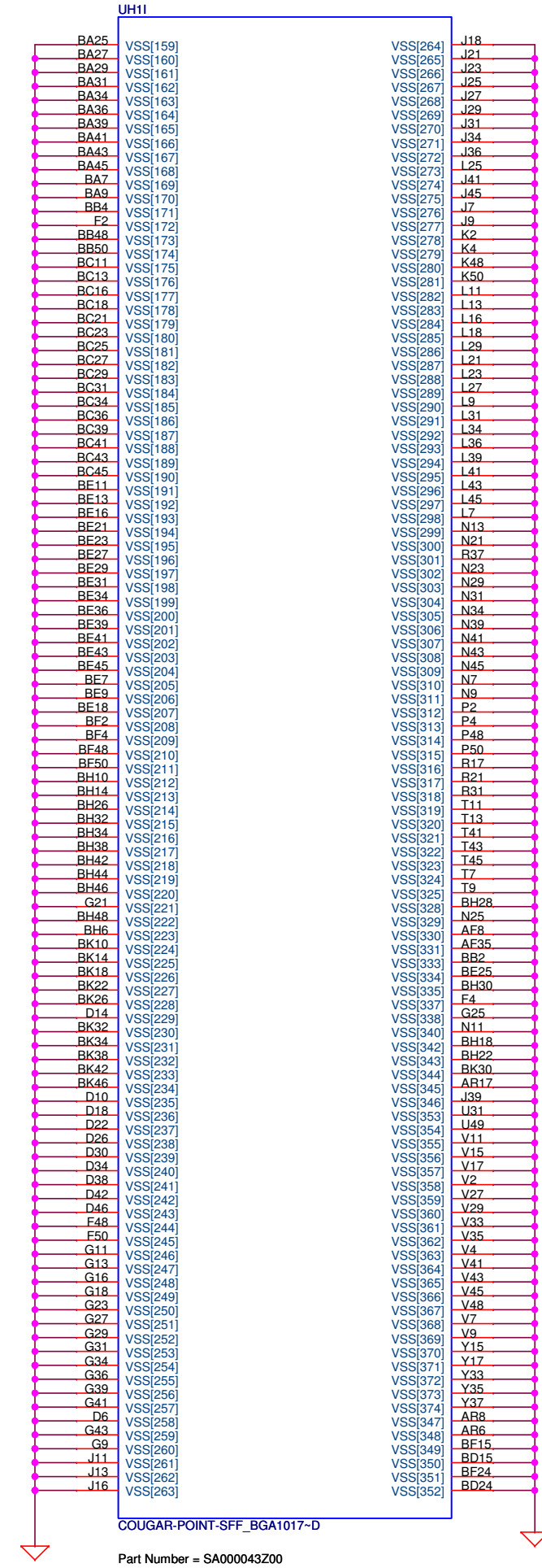
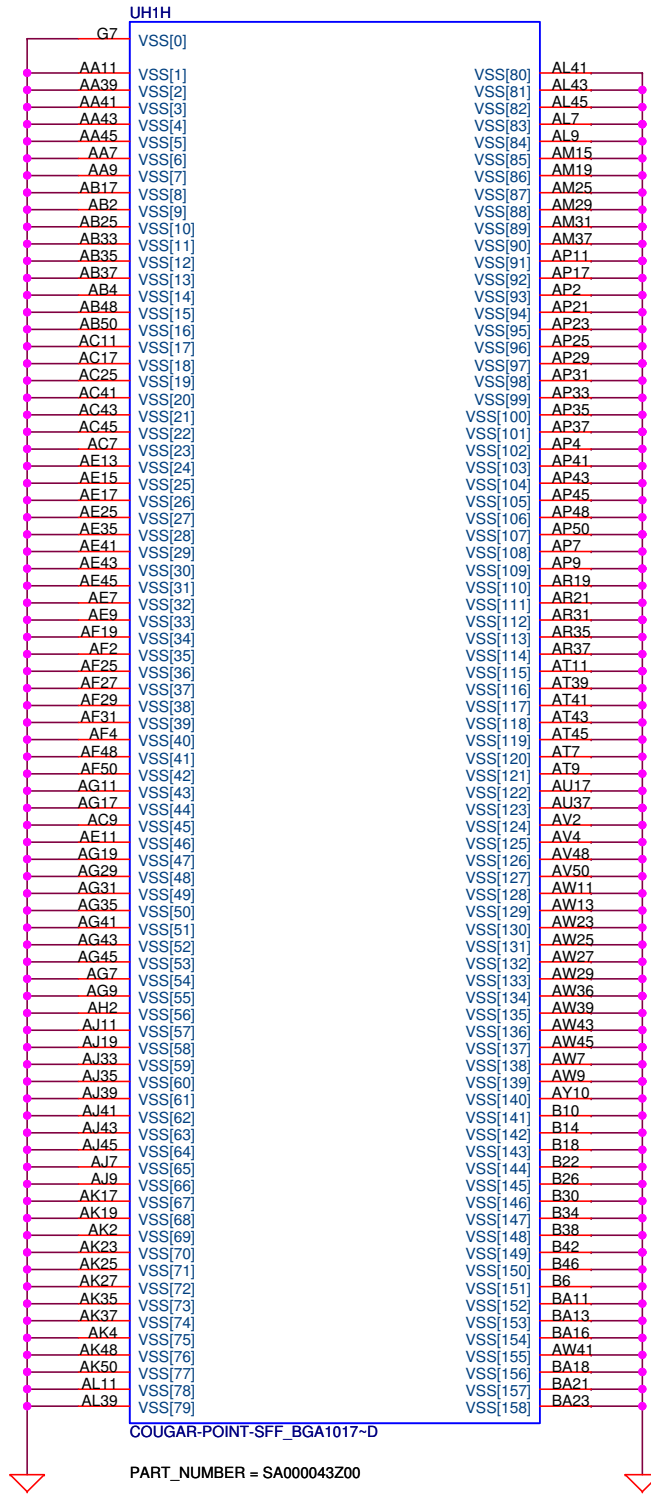


5/18 delete RH229

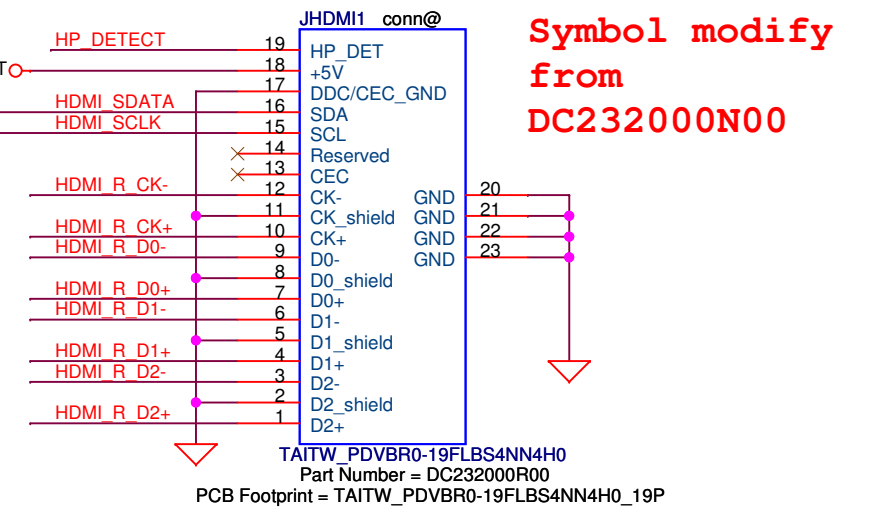
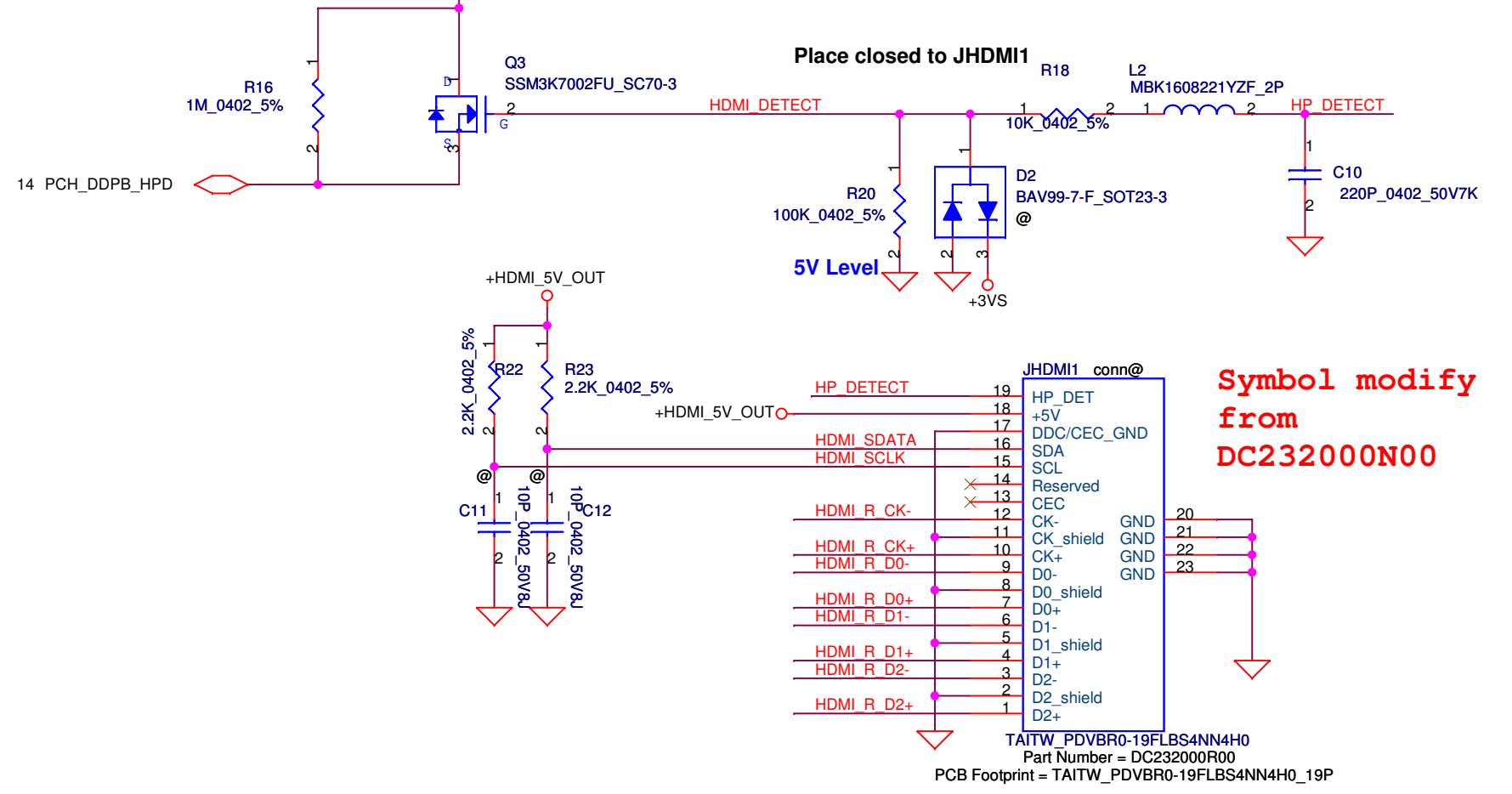
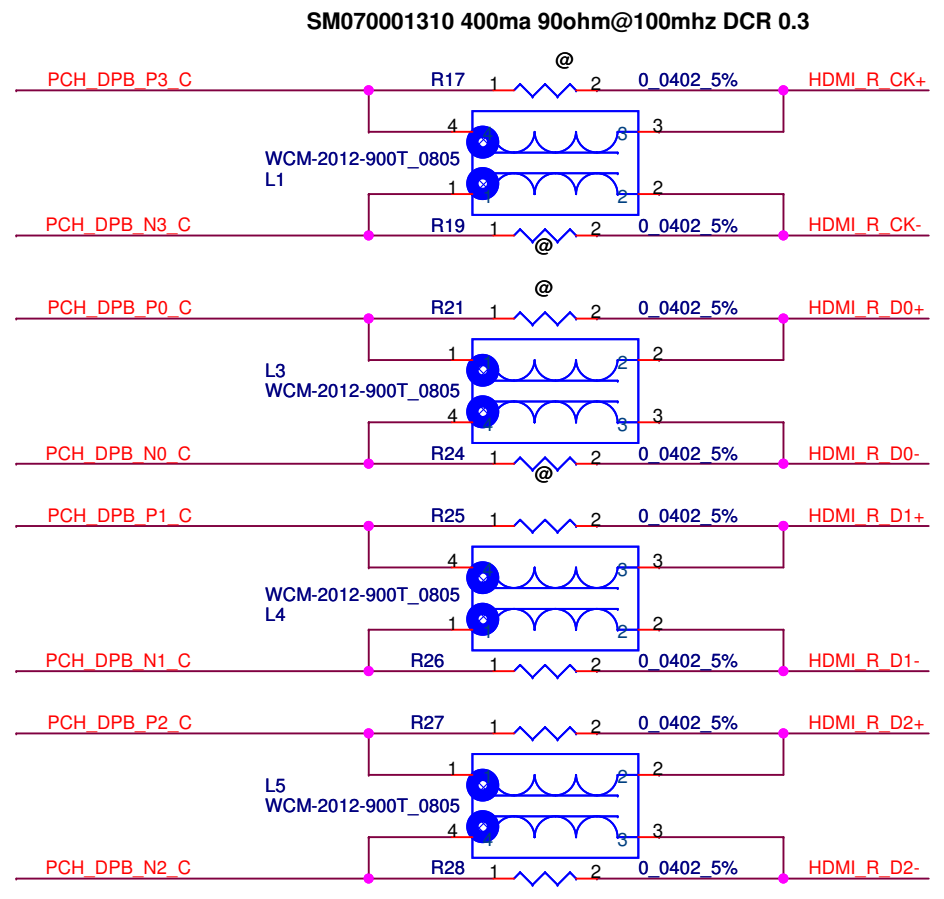
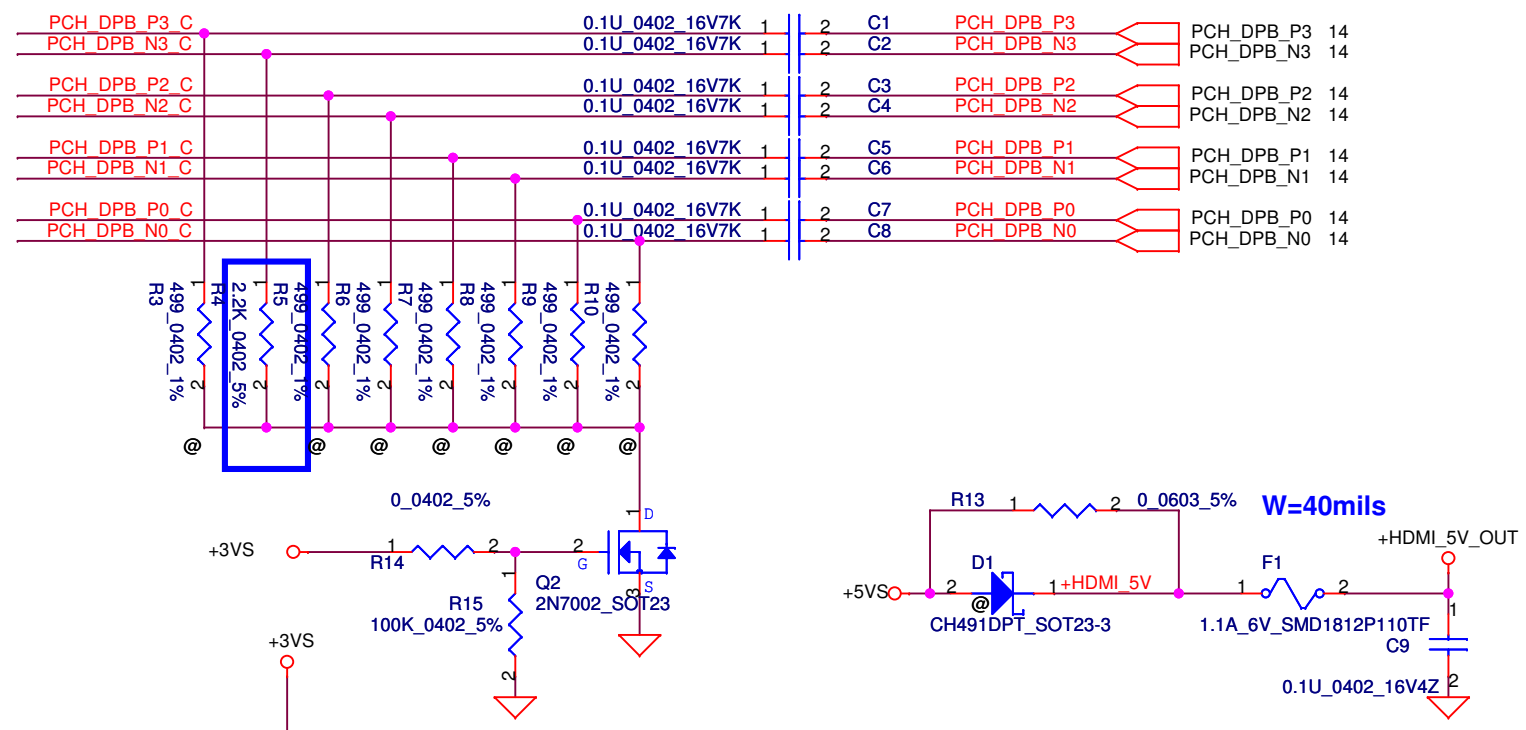
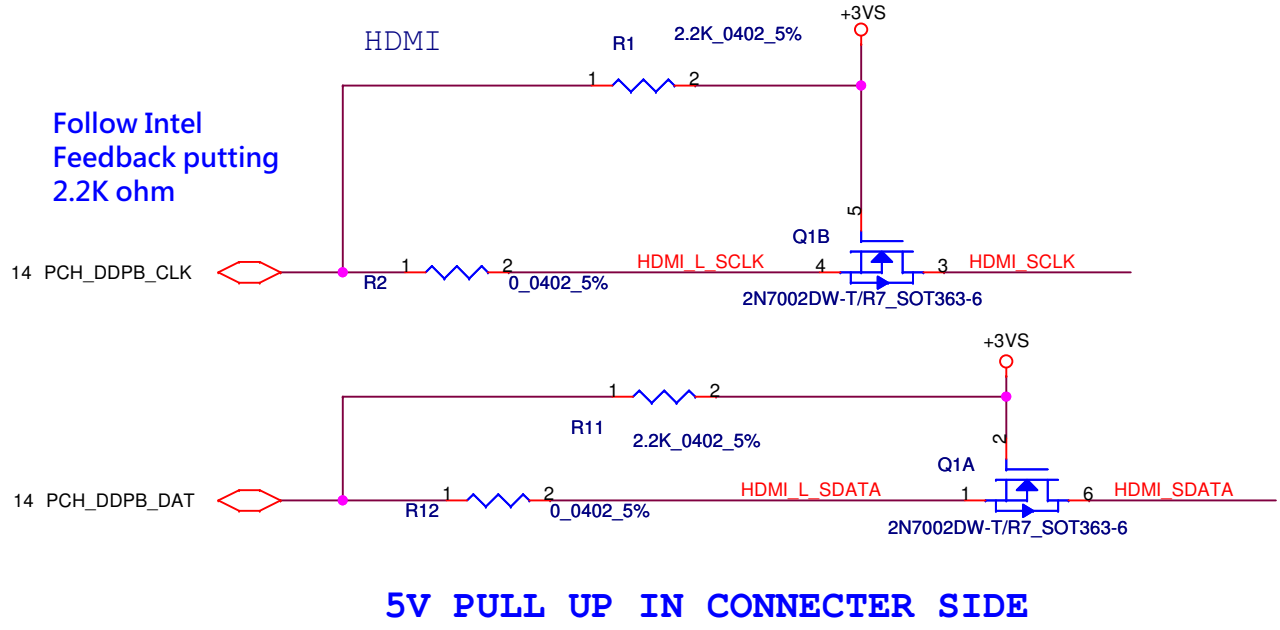
If it support 3.3V audio signals
POP: RH228
Depop RH233/RH234

If it support 1.5V audio signals
POP: RH233/RH234
Depop R228

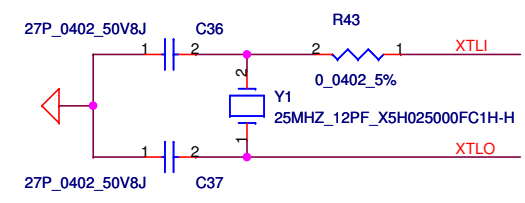
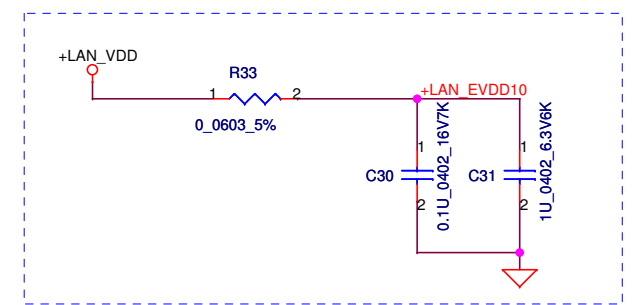
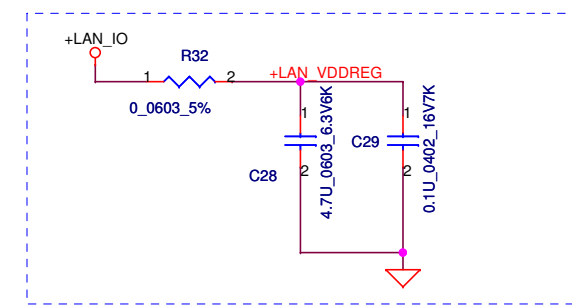
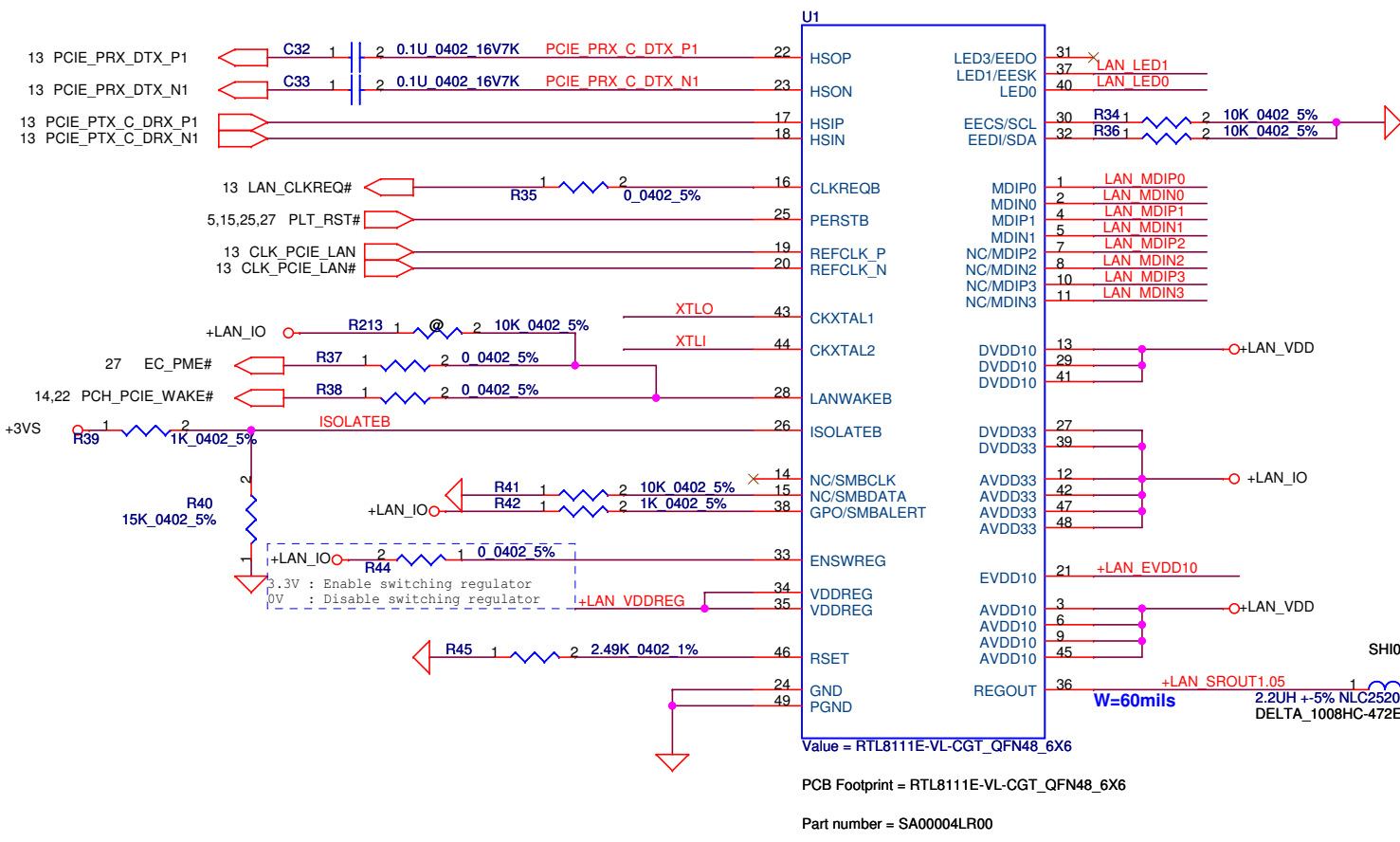
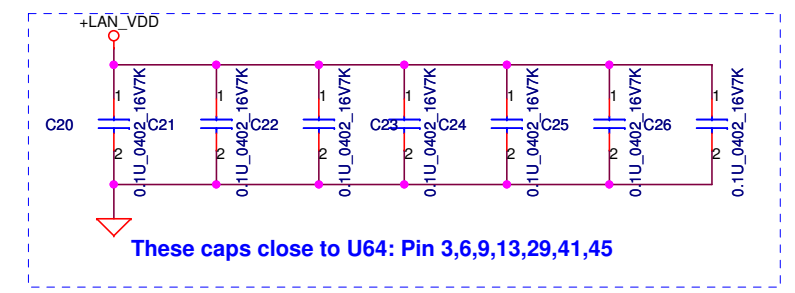
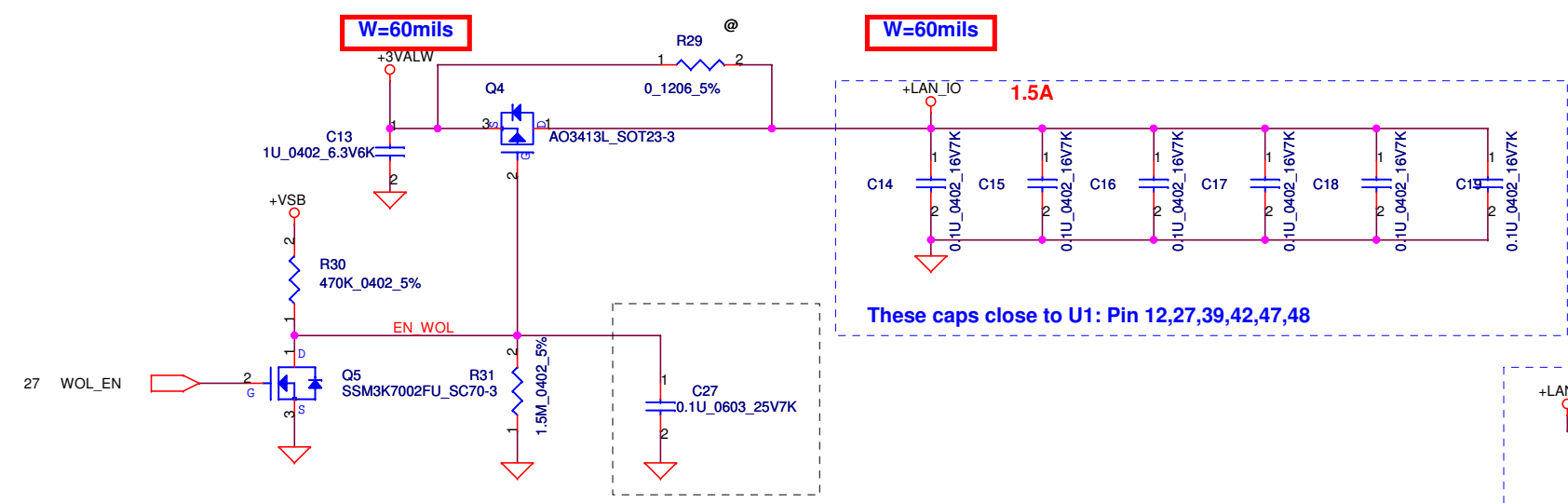
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Issued Date	2010/07/06	Deciphered Date	2011/07/06	Title
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Date: Sunday, April 10, 2011			Sheet 18 of 45	



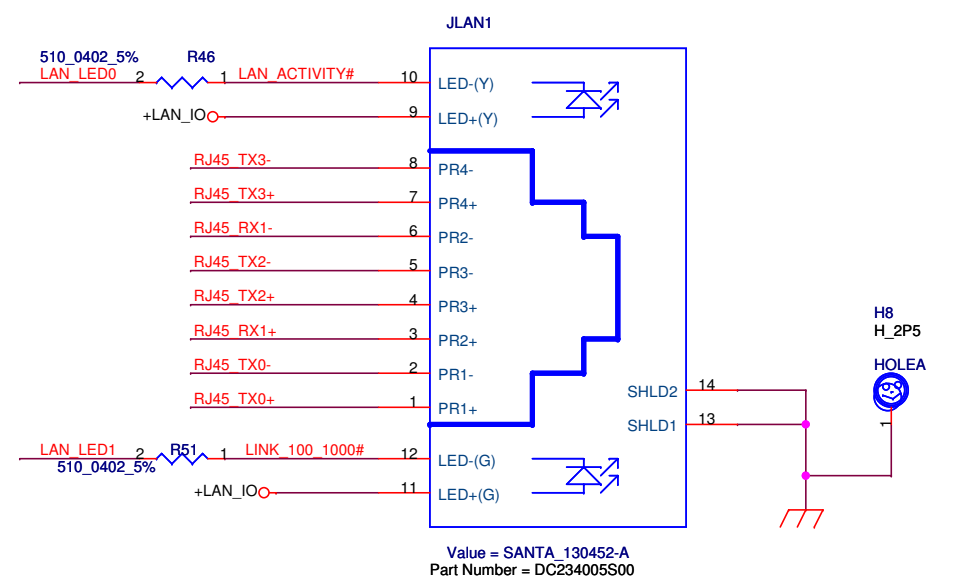
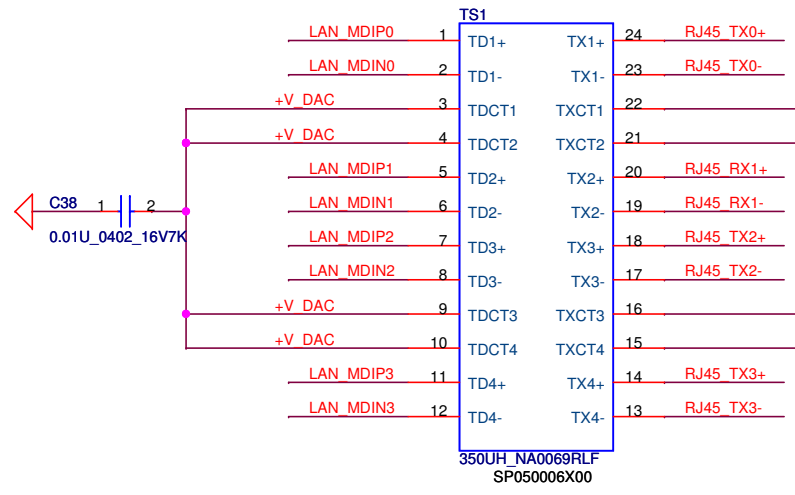
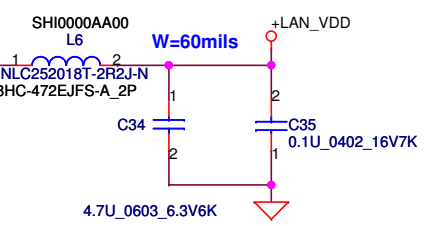
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Issued Date	2010/07/06	Deciphered Date	2011/07/06	Title
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Date: Thursday, April 07, 2011				Sheet 19 of 45



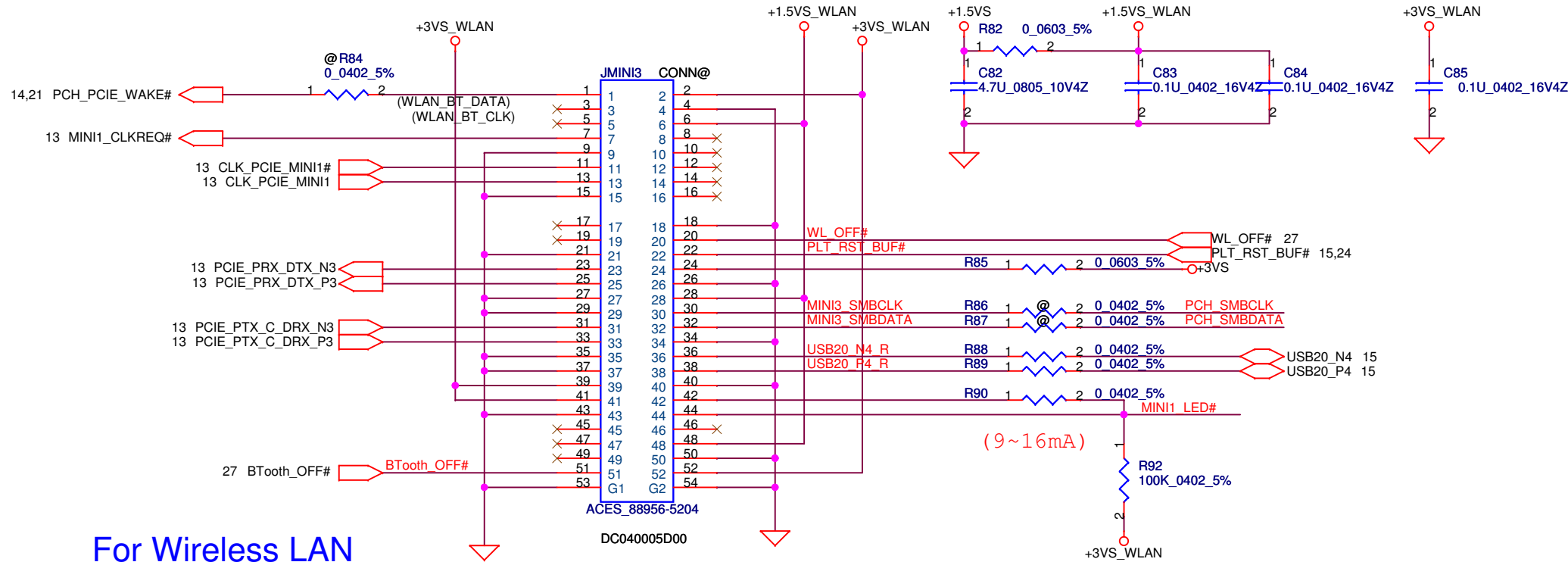
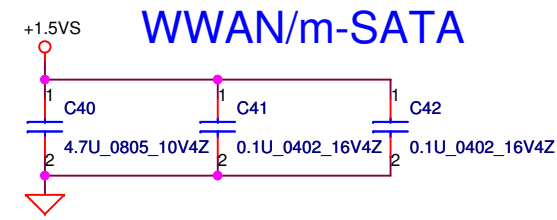
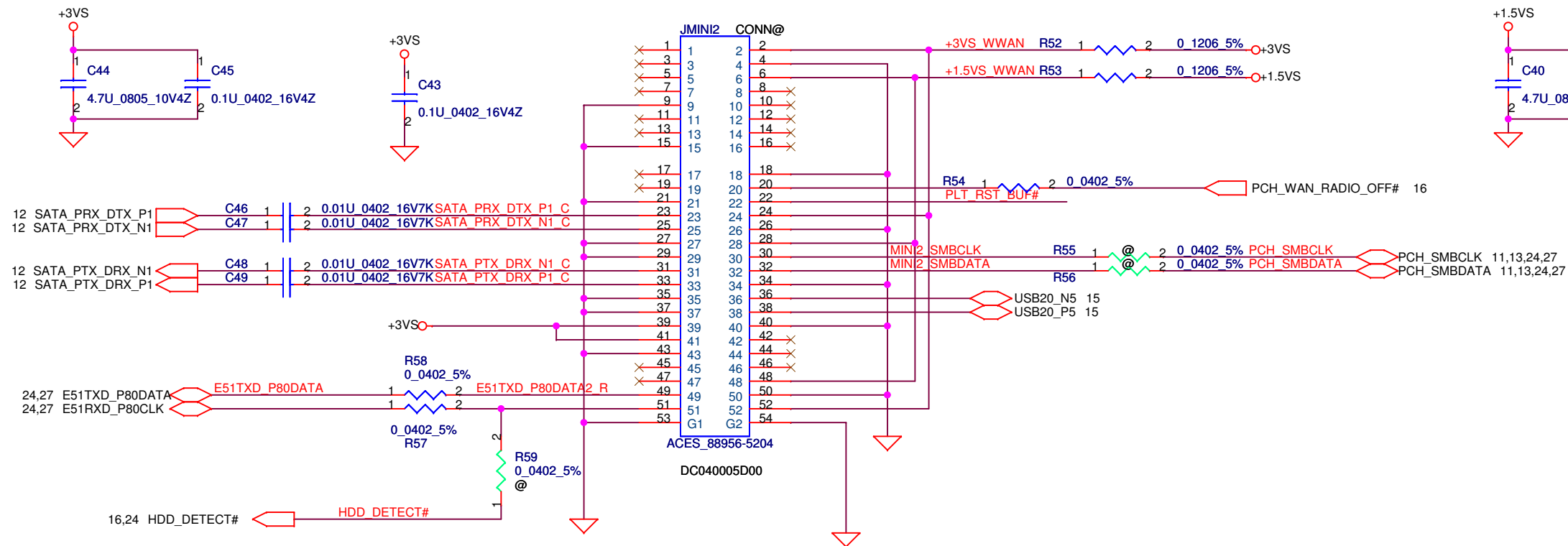
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Issued Date	2010/07/06	Deciphered Date	2011/07/06	Title
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				Size
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H_2P5 (6.0)

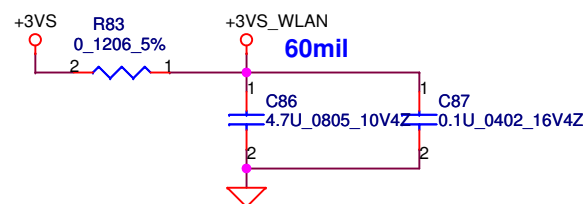


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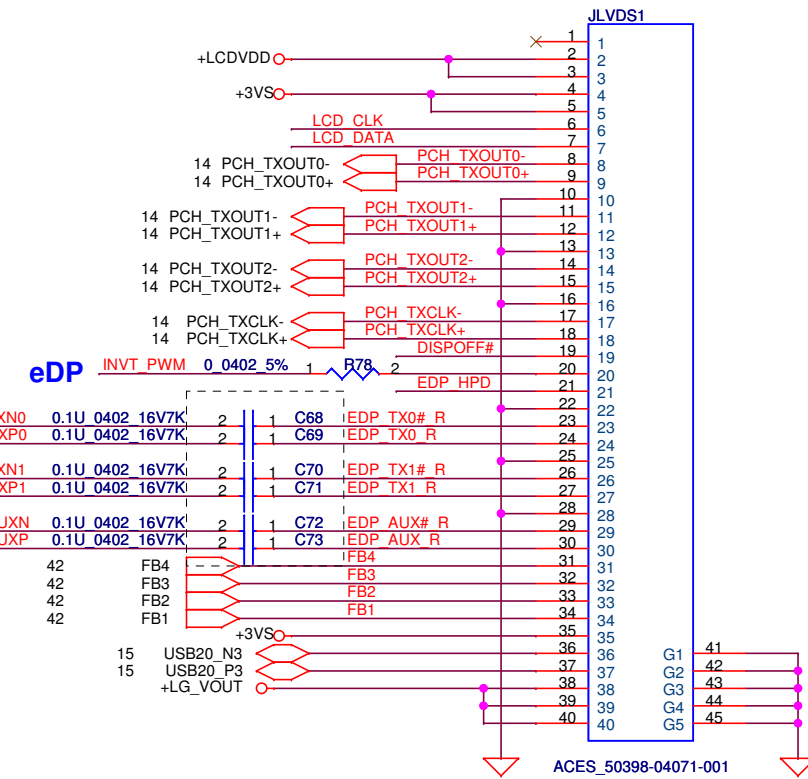
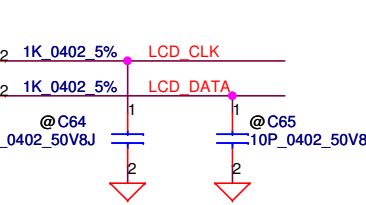
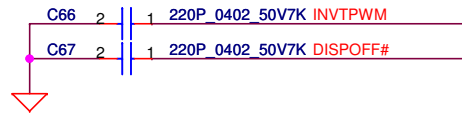
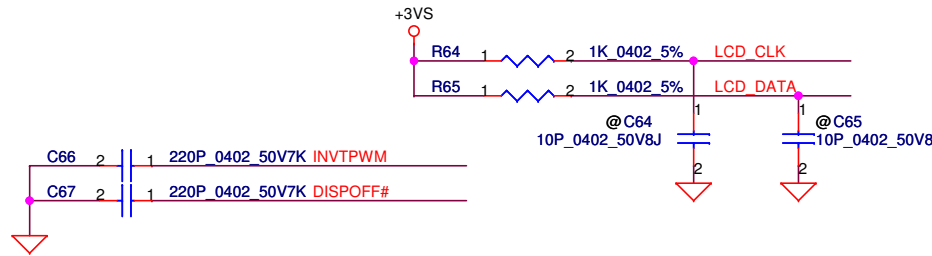
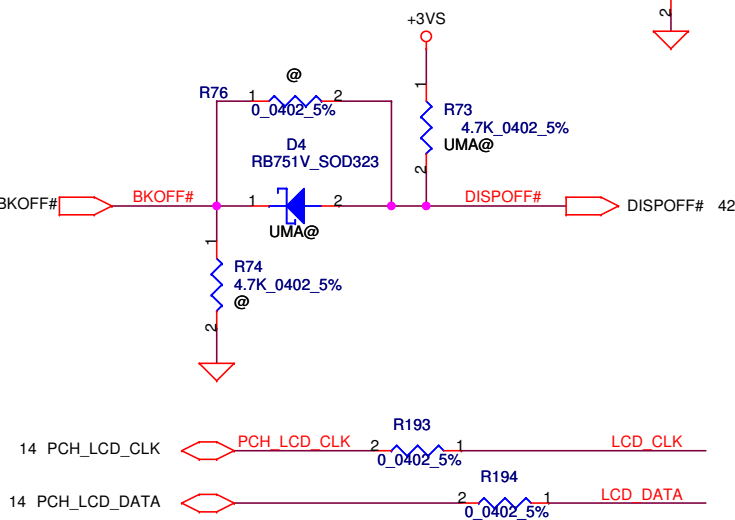
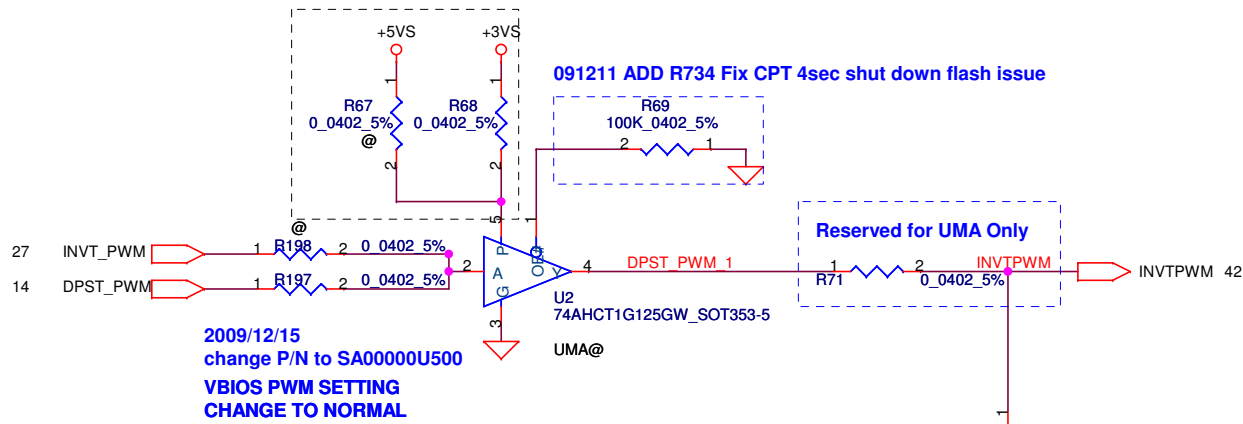
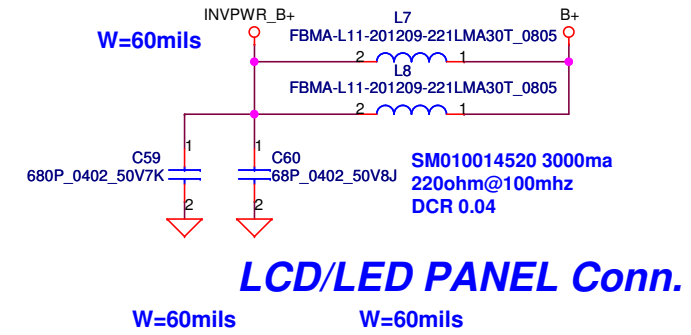
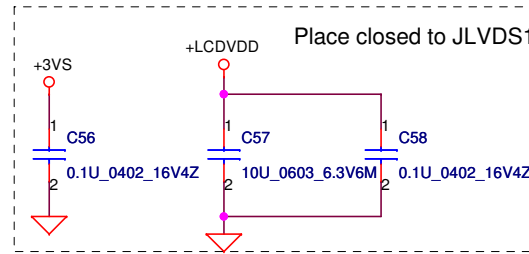
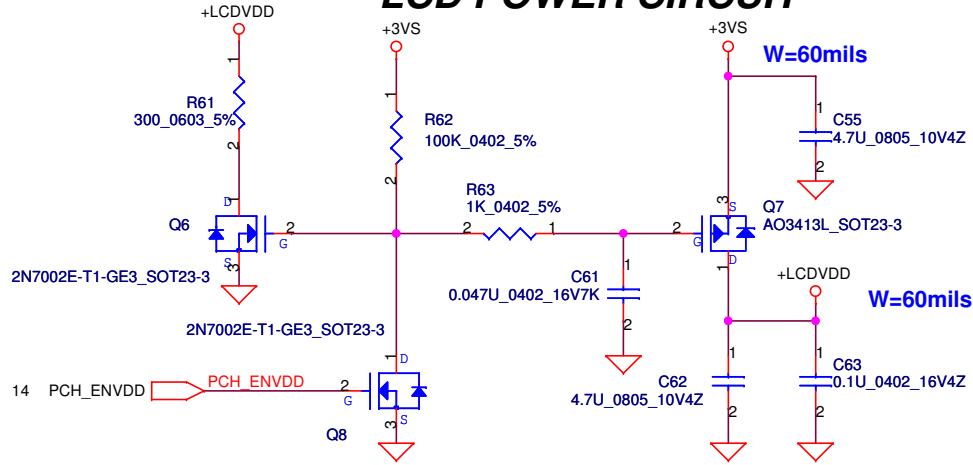
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For Wireless LAN



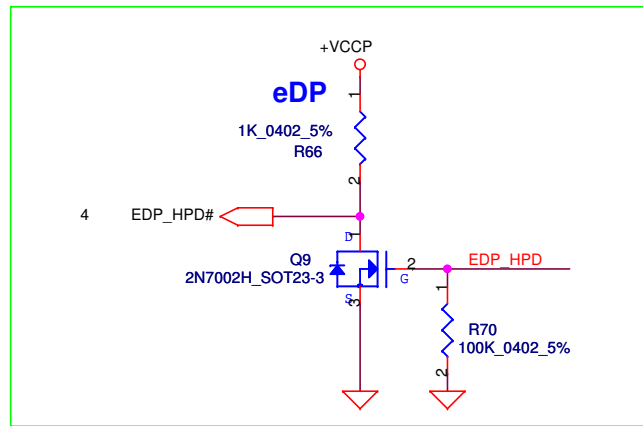
Security Classification	Compal Secret Data		Title	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	
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Compal Electronics, Inc. MiniCard WWAN & Wlan			Size	Rev
Document Number LA-7531P			0.1	
Date:	Sunday, April 10, 2011	Sheet	22	of 45

LCD POWER CIRCUIT



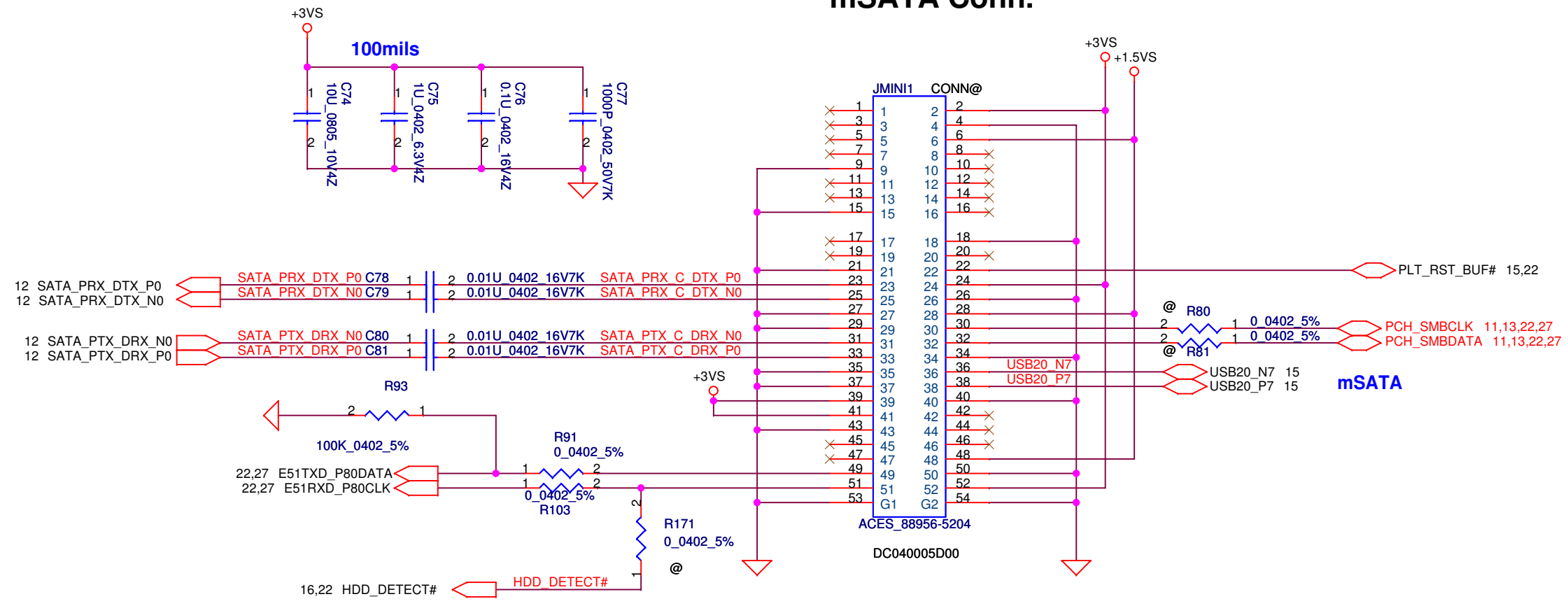
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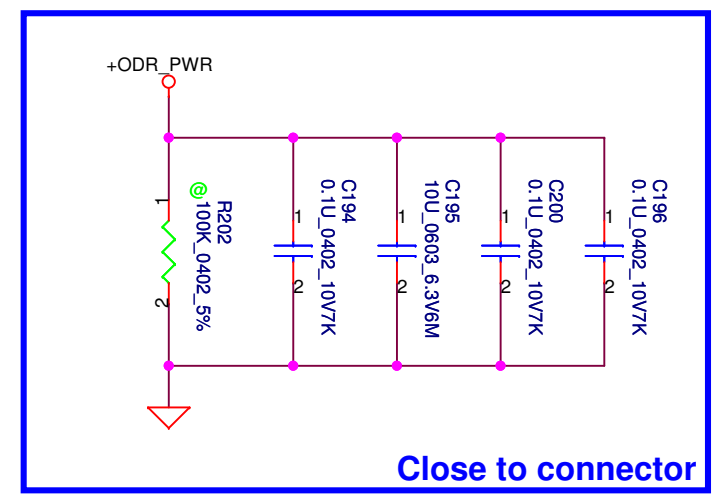
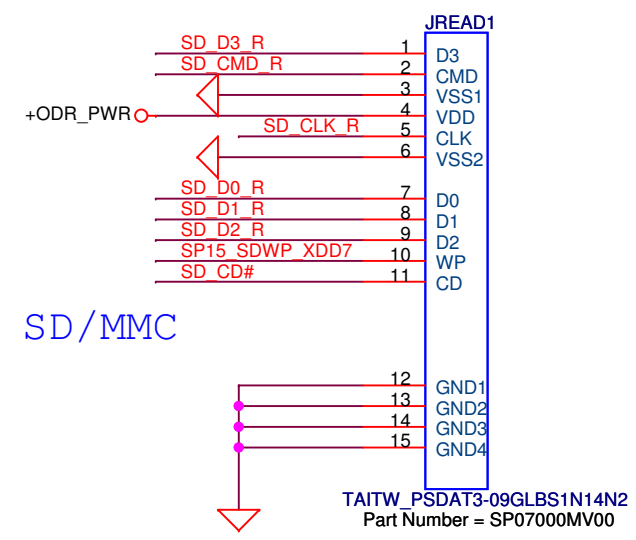
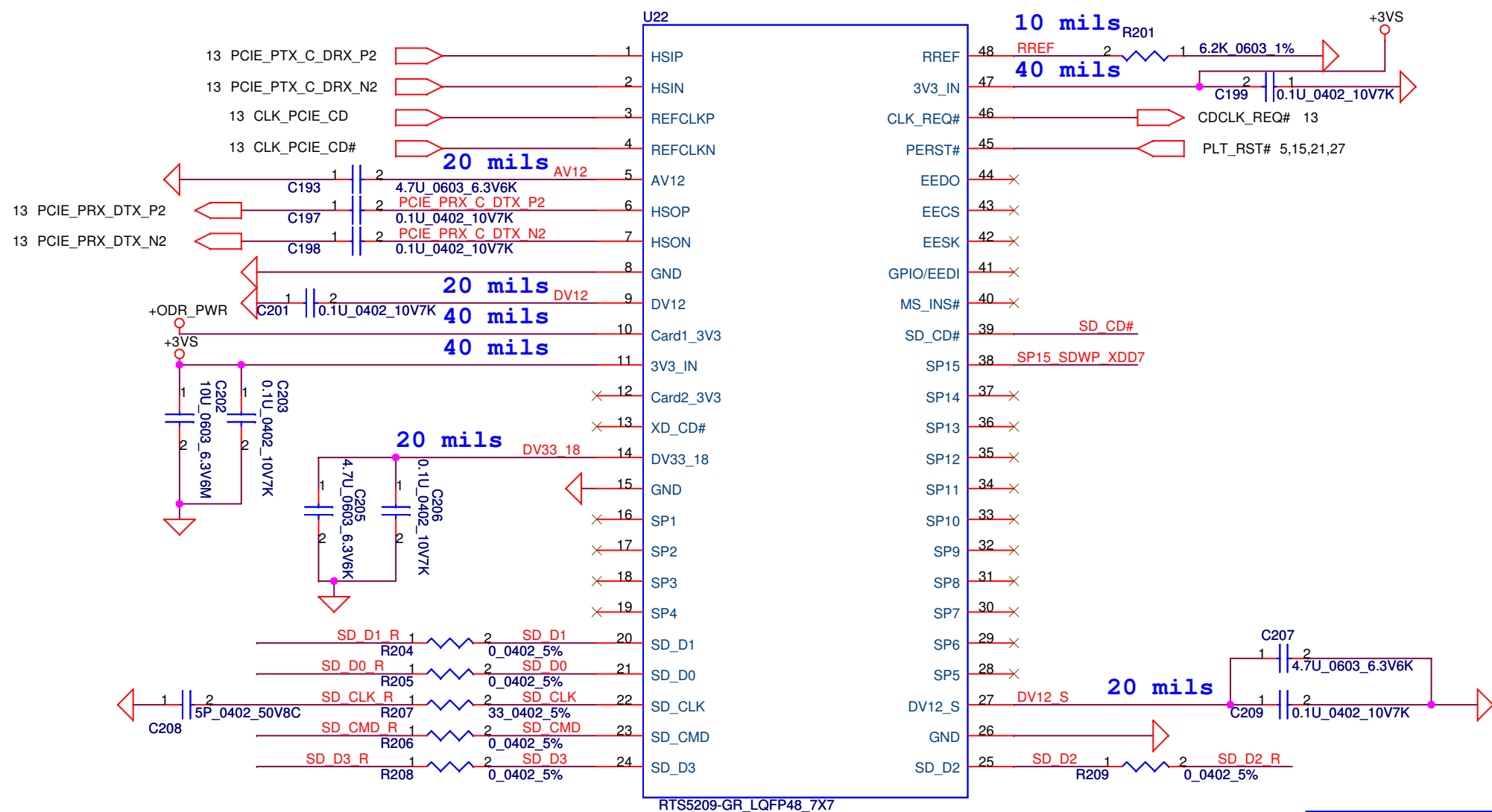


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				LA-7531P	Rev 0.1
				Date: Sunday, April 10, 2011	Sheet 23 of 45

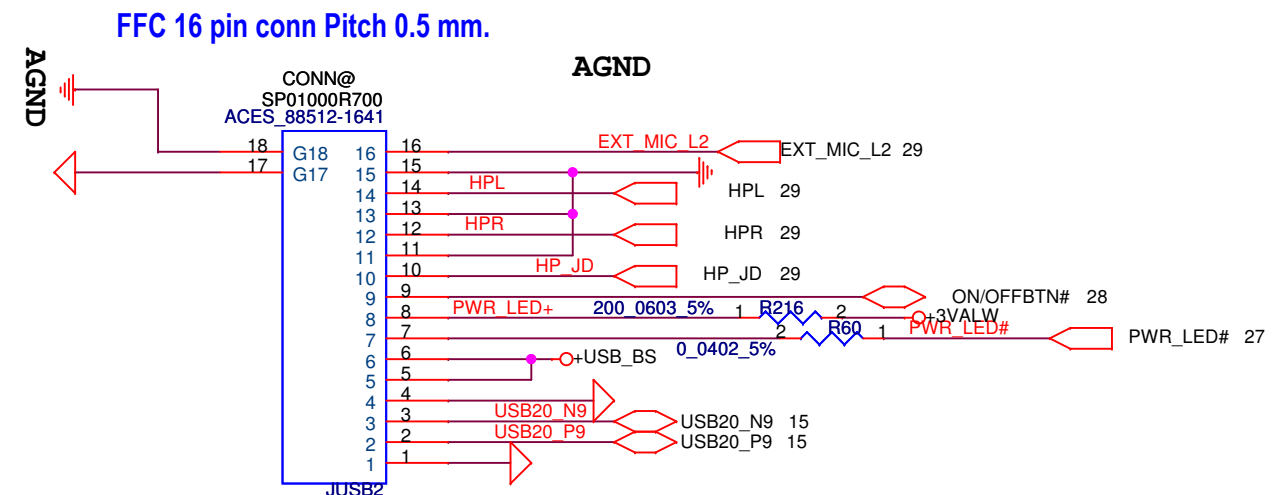
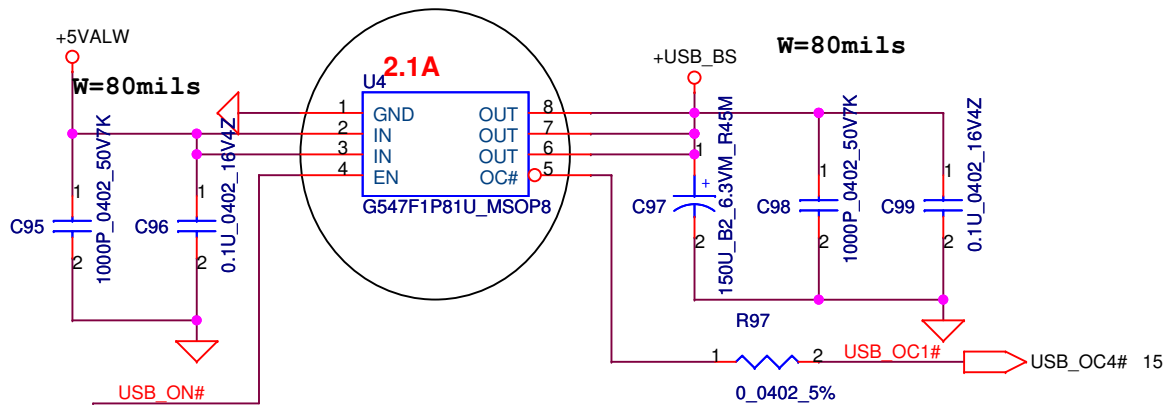
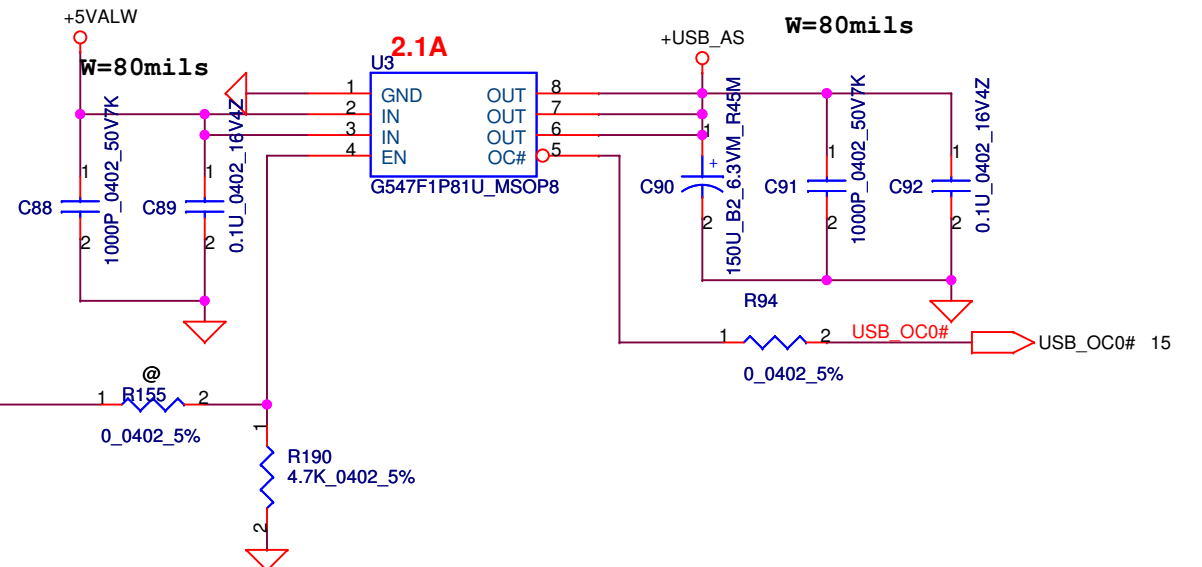
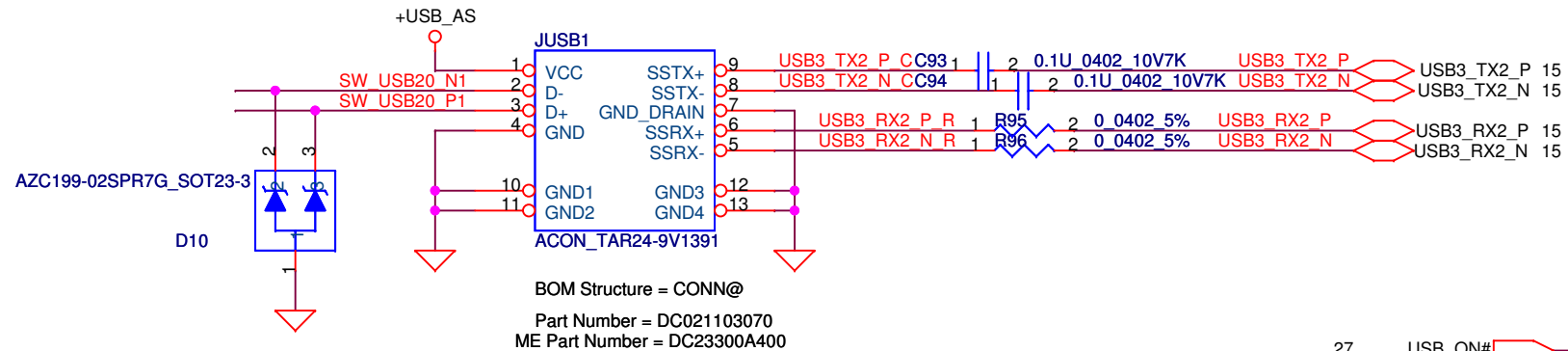
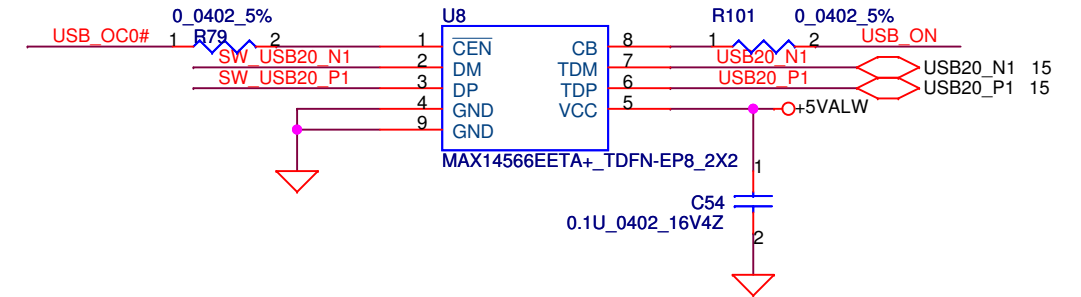
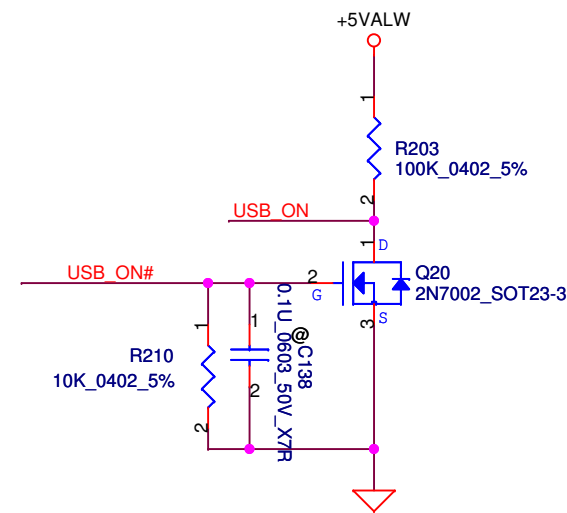
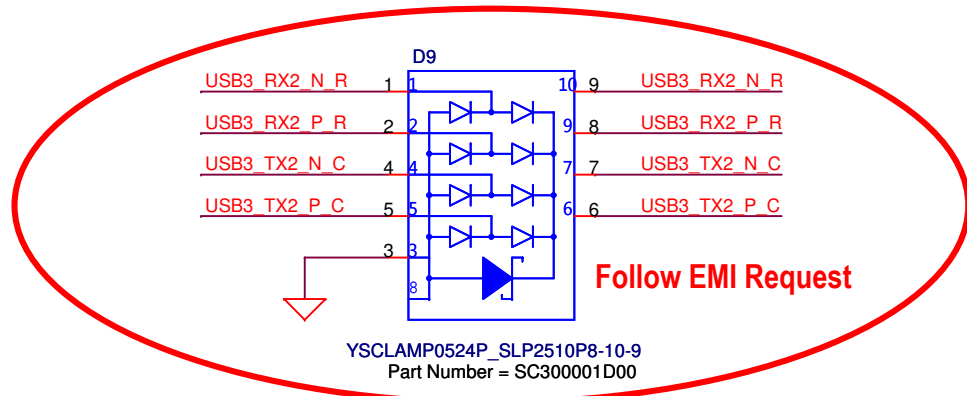
mSATA Conn.



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			Size B	Document Number	Rev
				LA-7531P	0.1
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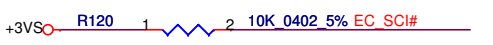
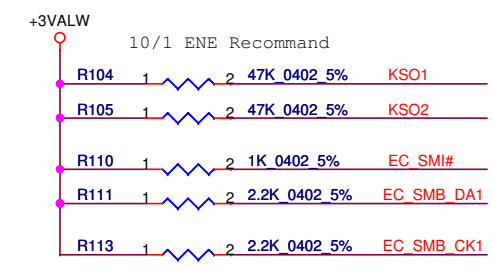
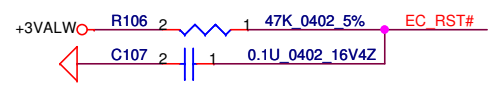
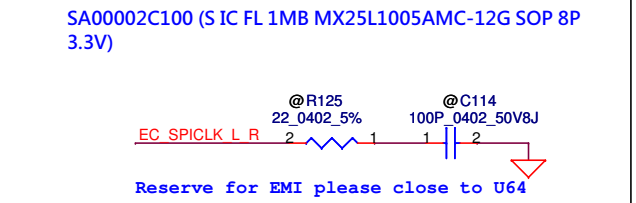
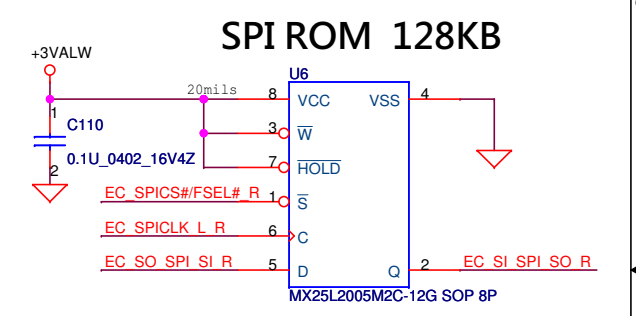
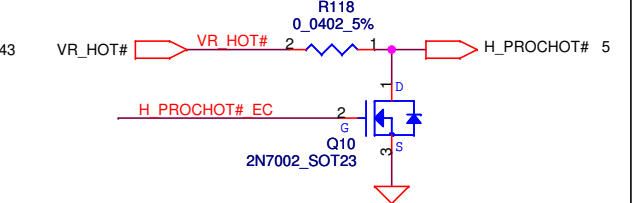
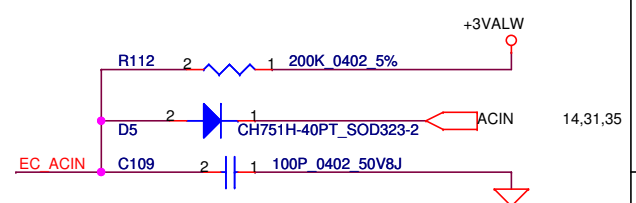
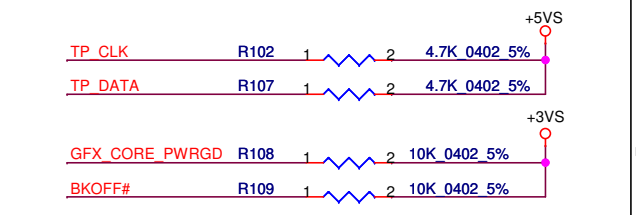
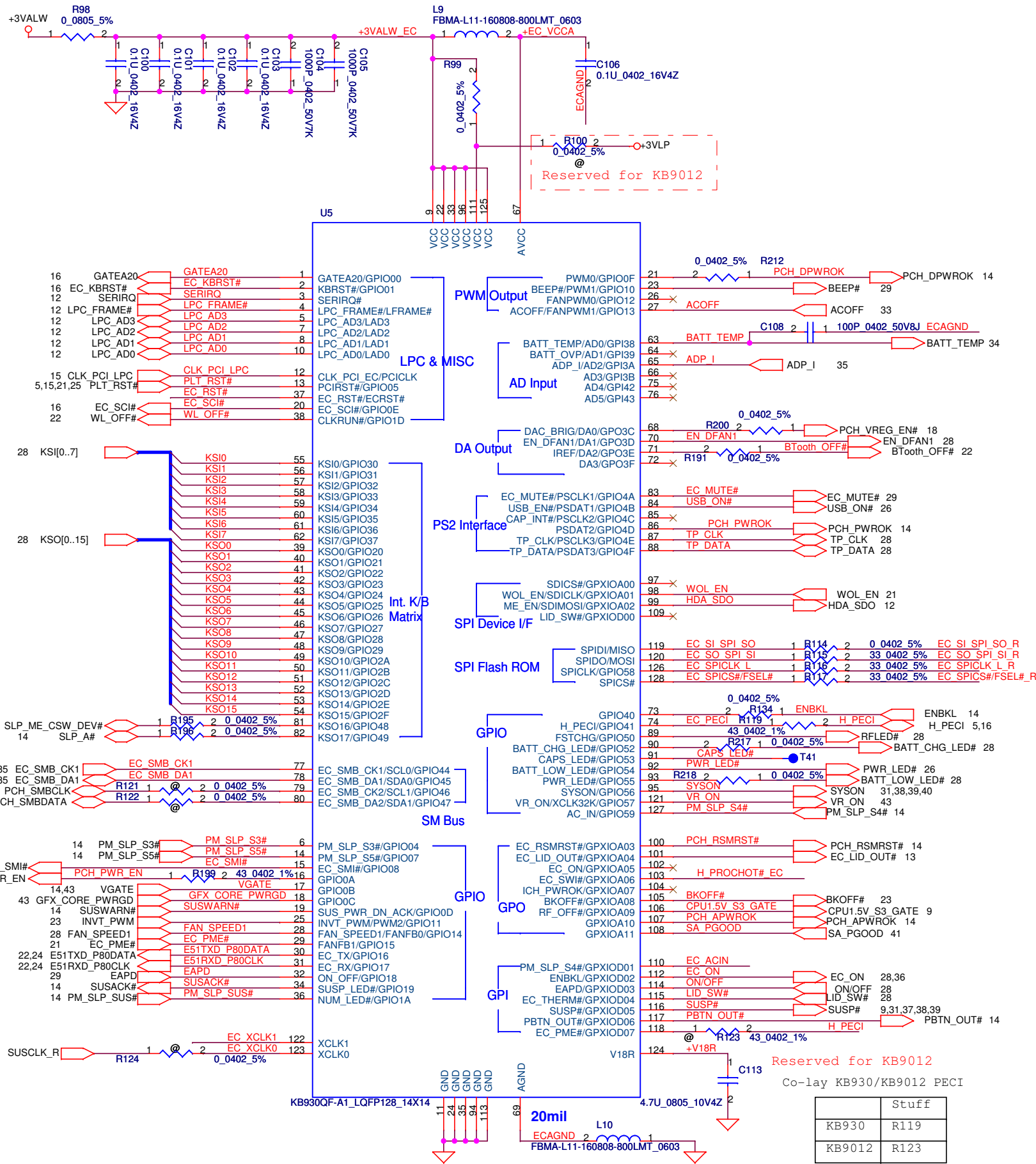


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				LA-7531P	
				Date:	Sunday, April 10, 2011
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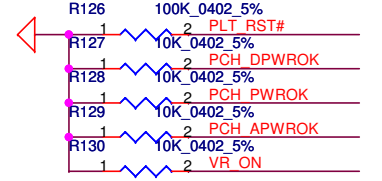
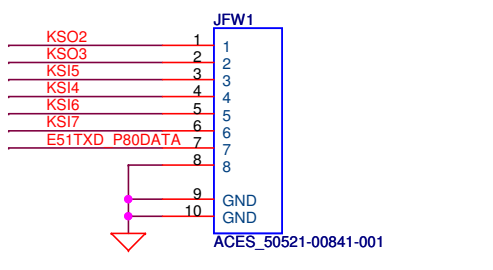
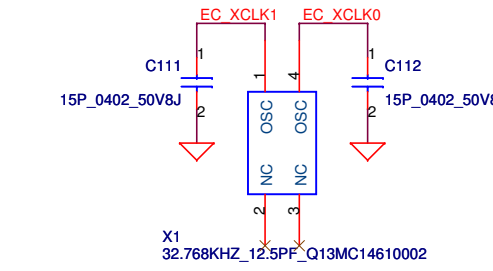


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2011/04/09

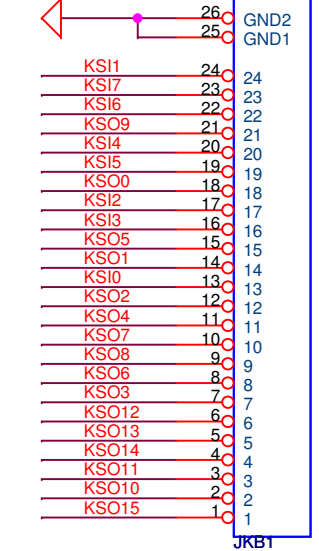
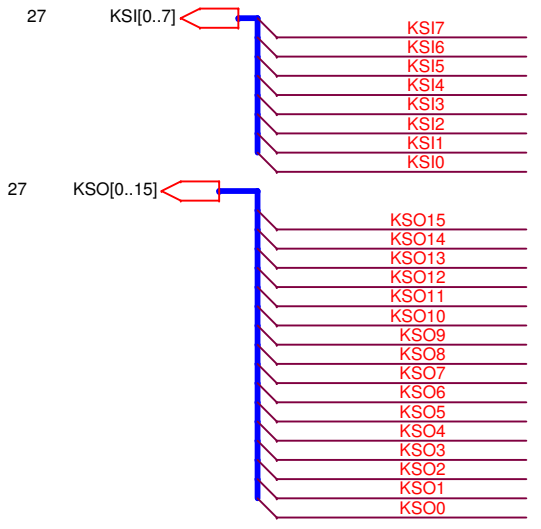
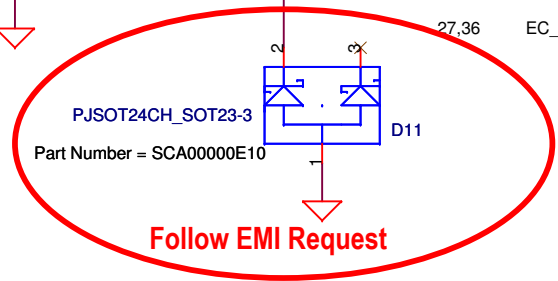
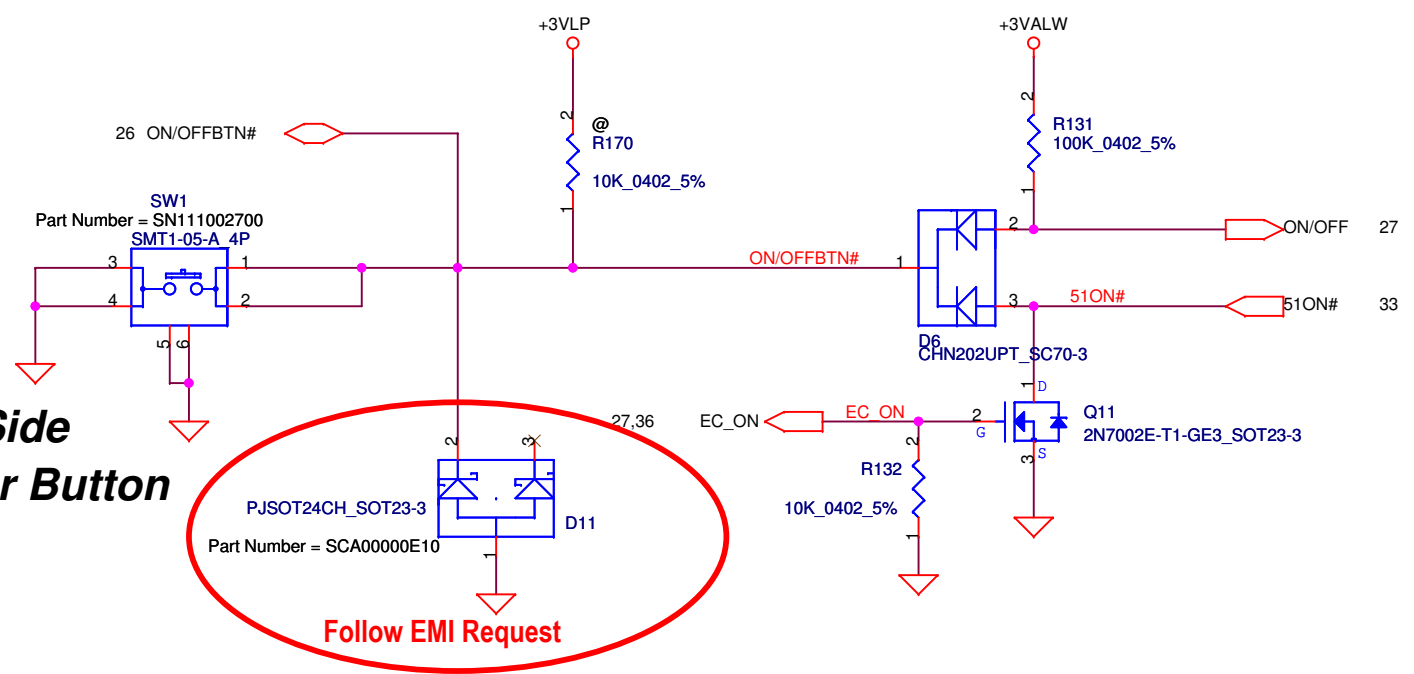


To prevent debug card unwork issue.

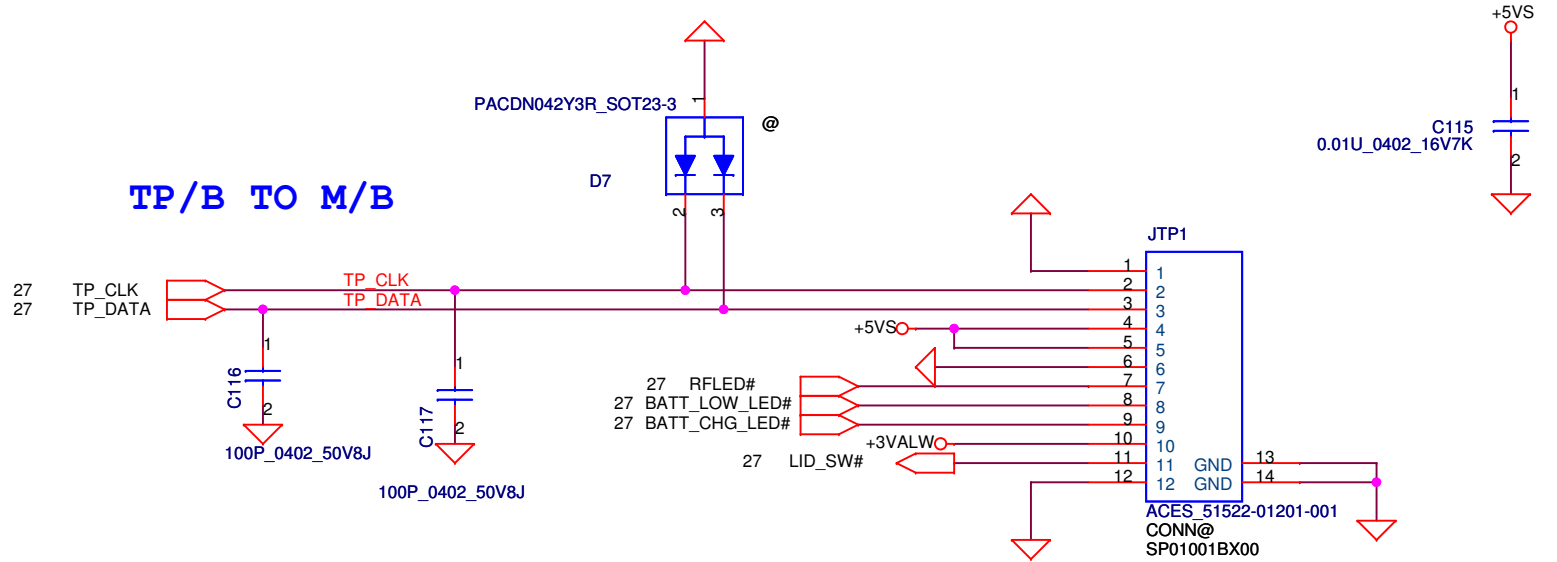


Co-layer	Stuff
KB930	R119
KB9012	R123

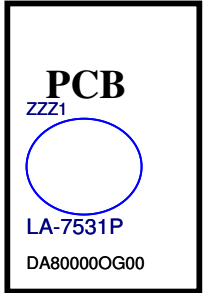
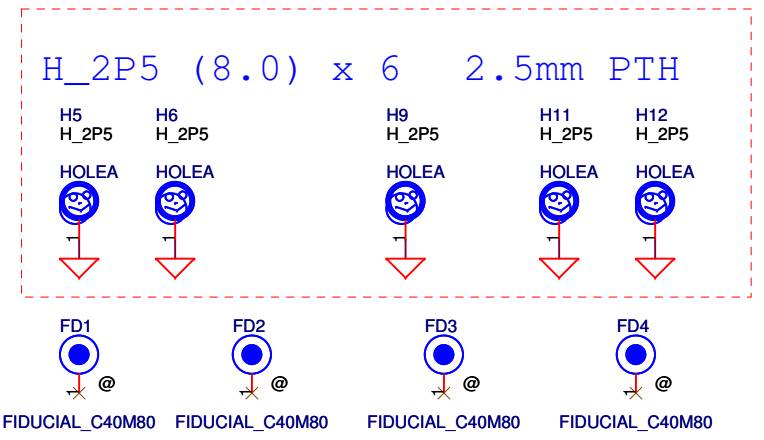
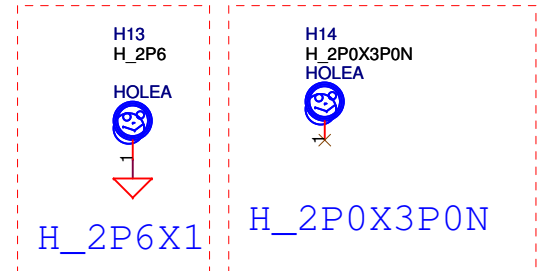
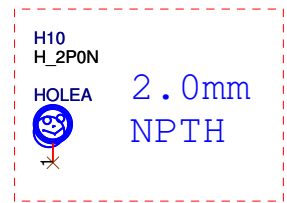
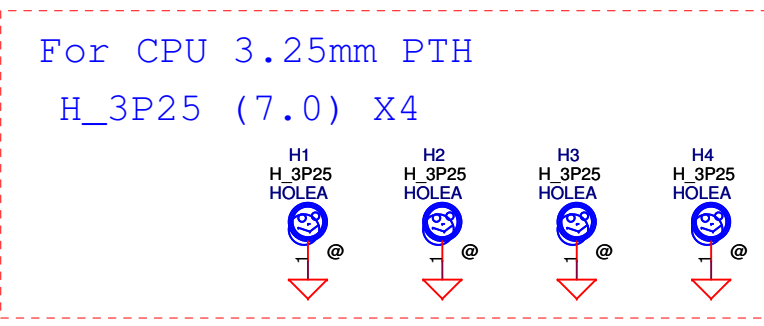
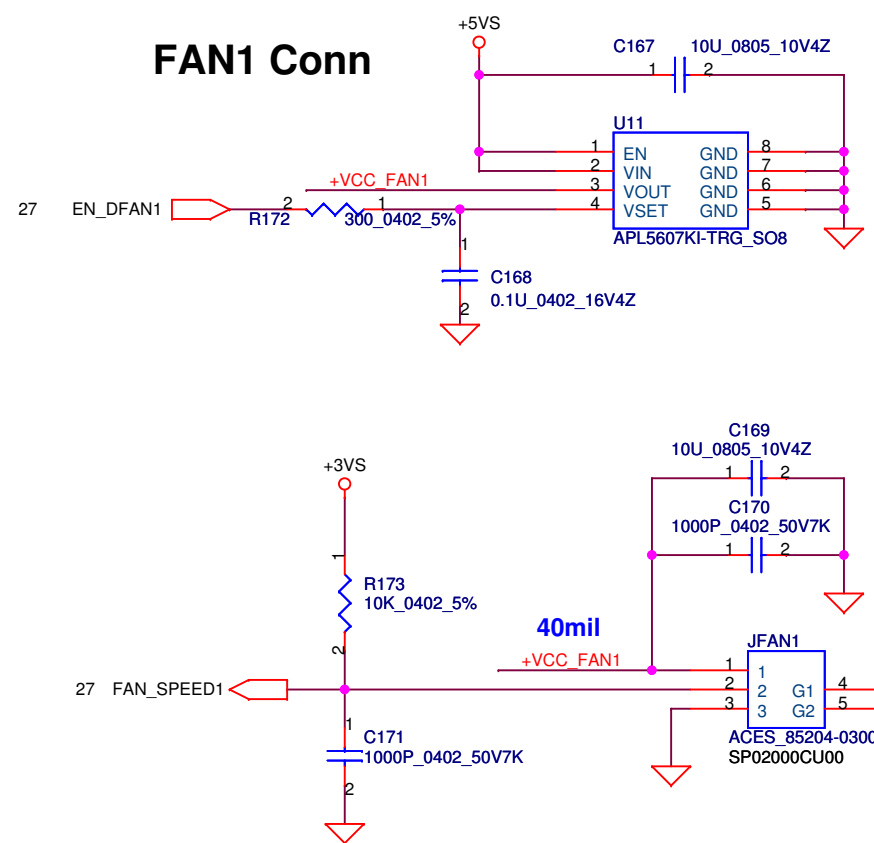
Top Side Power Button



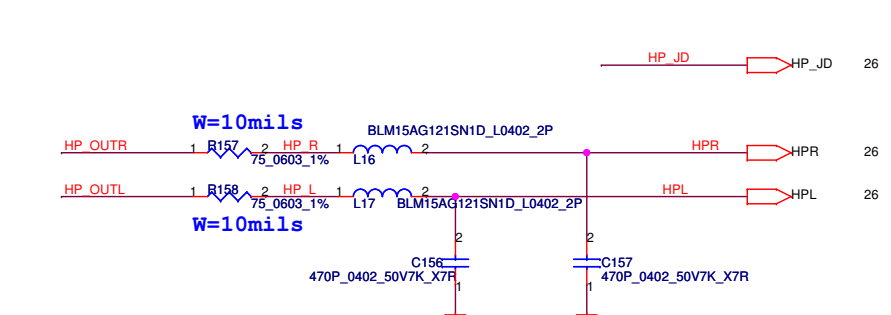
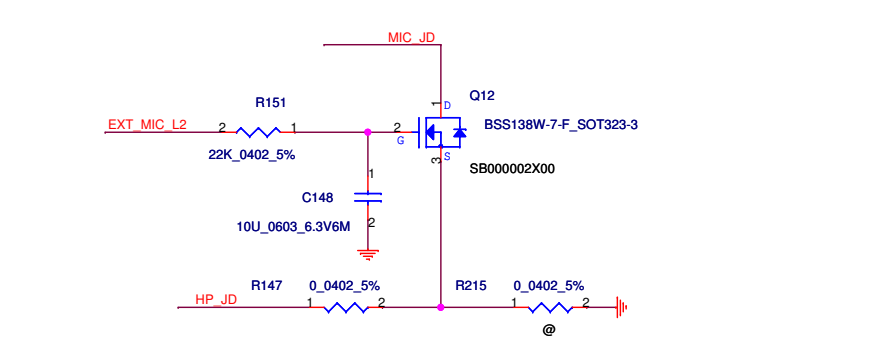
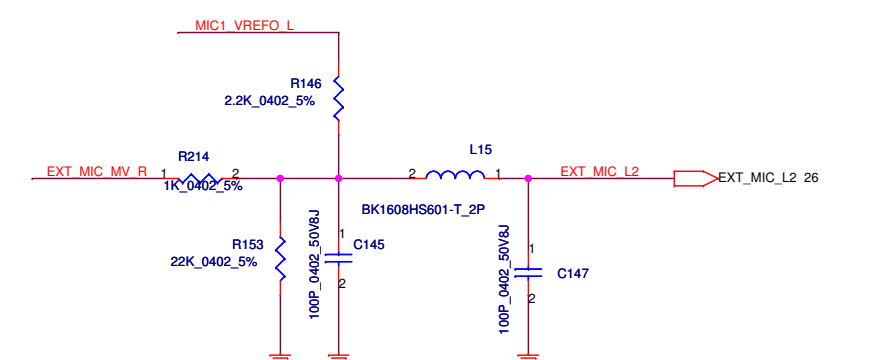
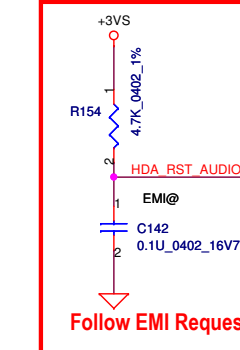
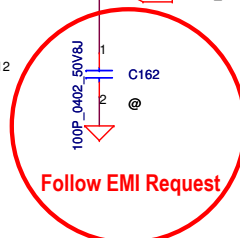
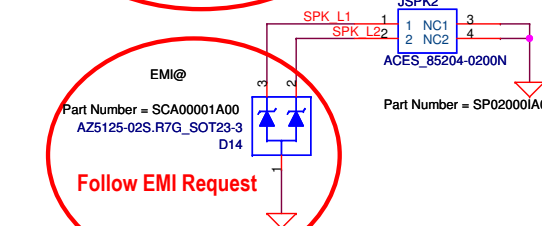
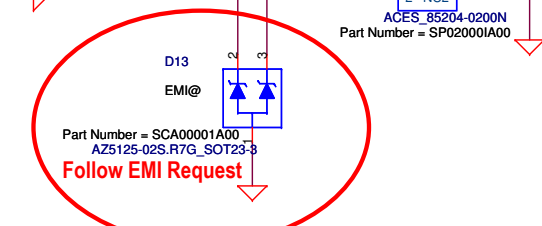
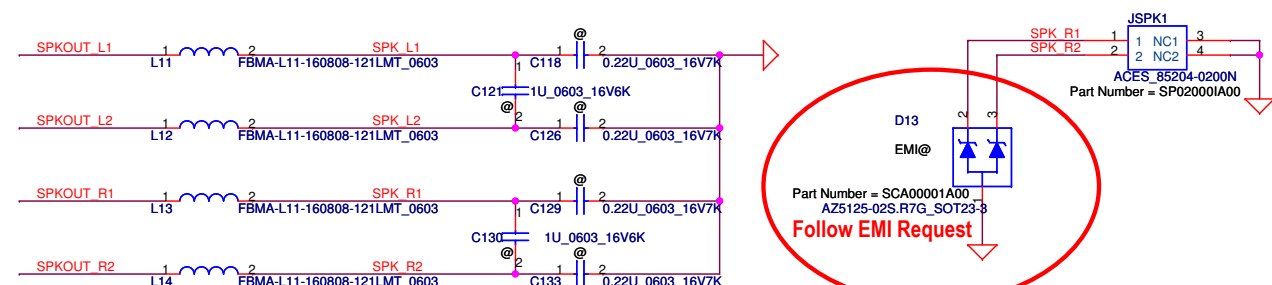
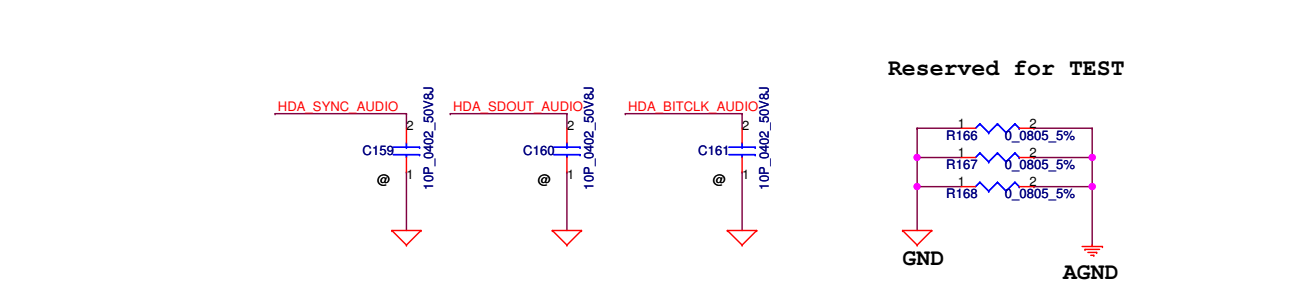
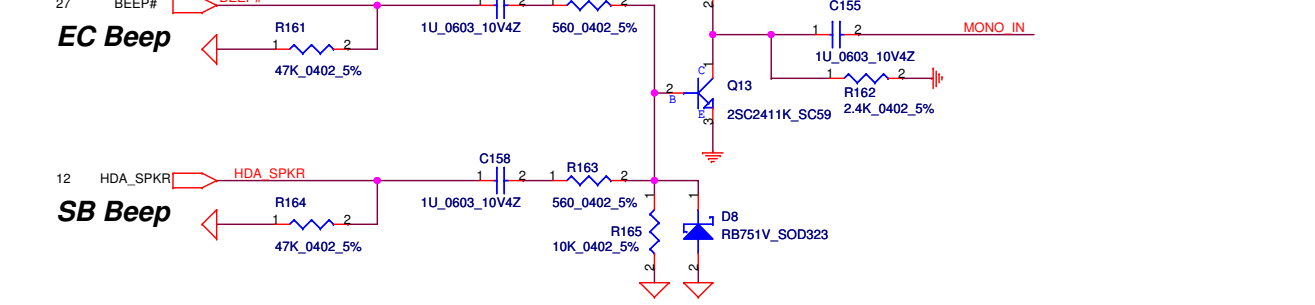
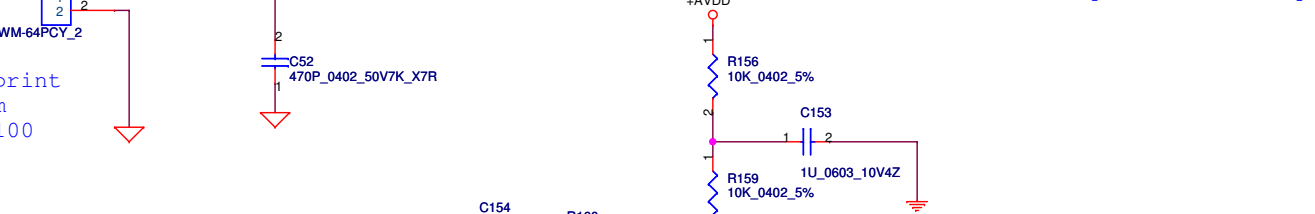
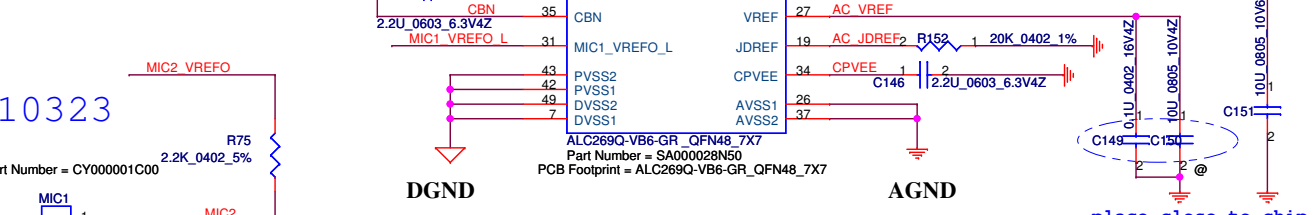
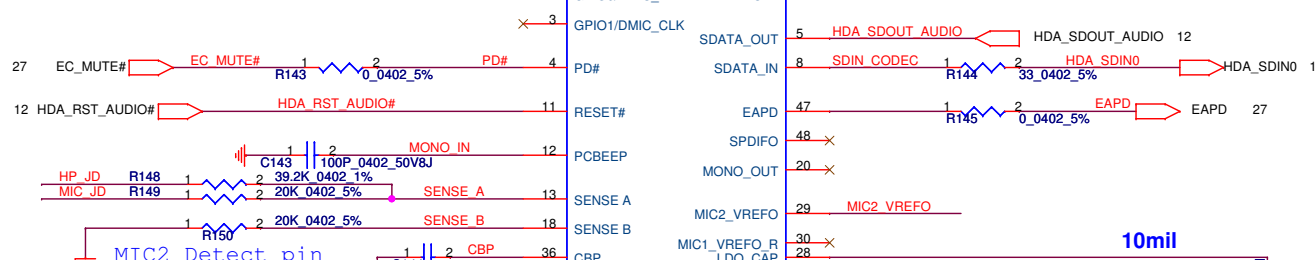
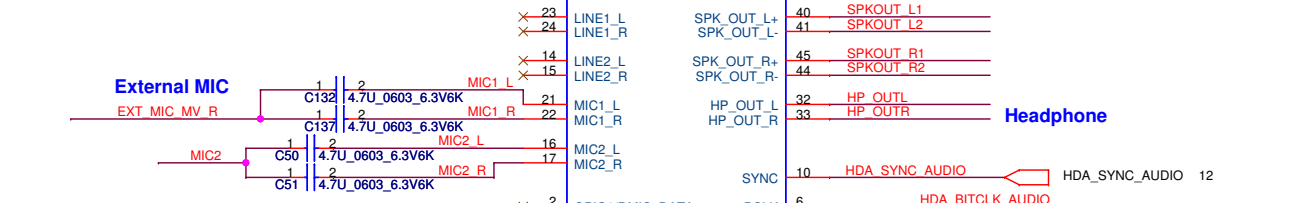
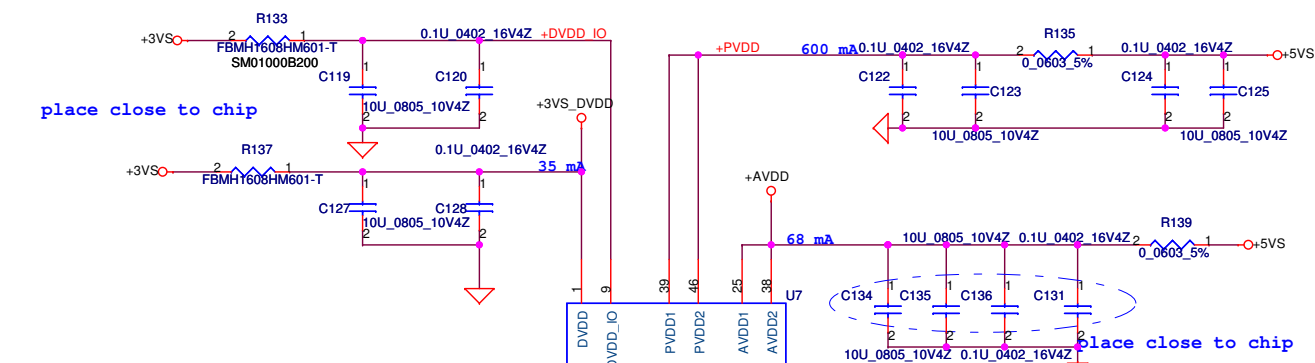
TP/B TO M/B



FAN1 Conn

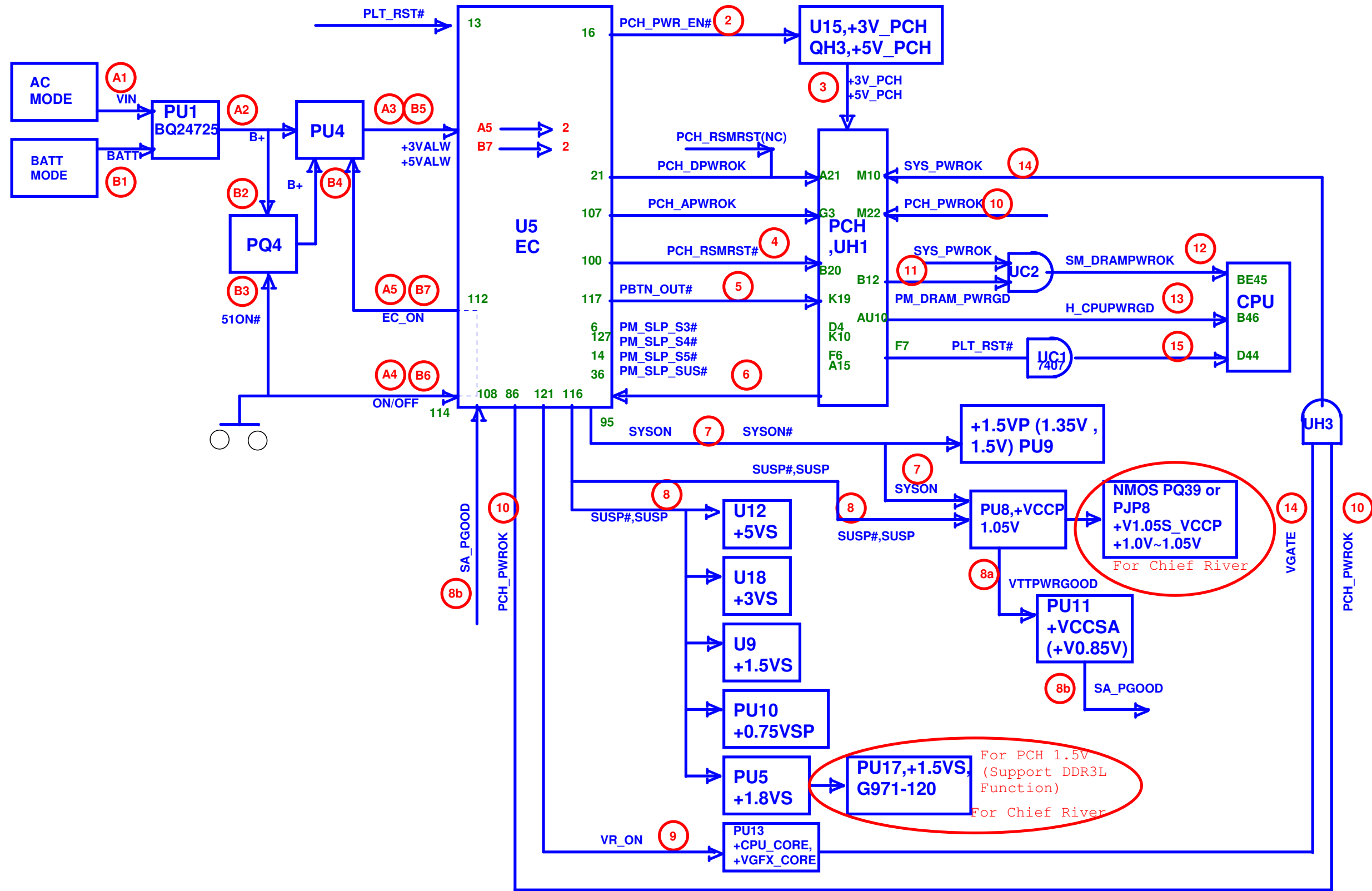


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				Size	Document Number	Rev	
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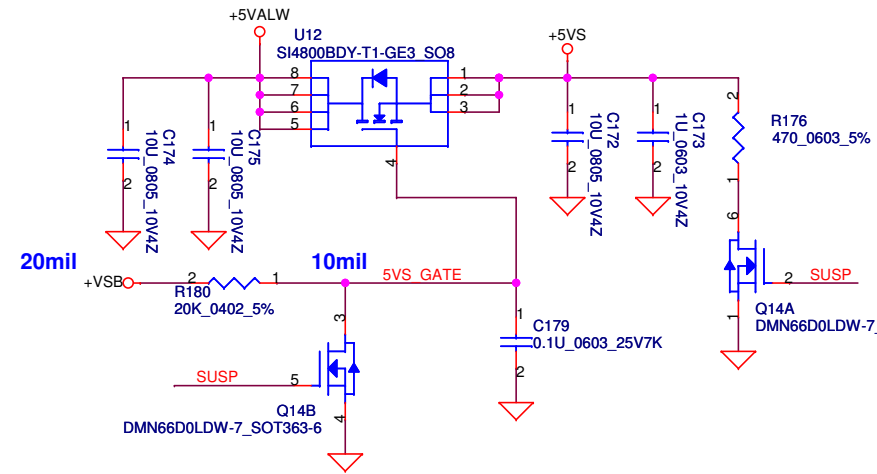
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Size	Document Number	Rev		
C	LA-7531P	0.1		
Date:	Sunday, April 10, 2011	Sheet	29	of 45

LA-7531P Power Sequence 2011/04/10

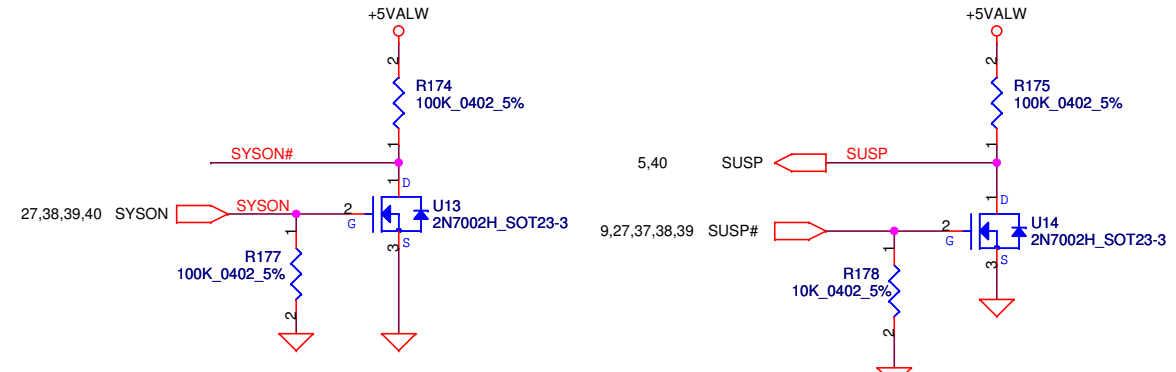
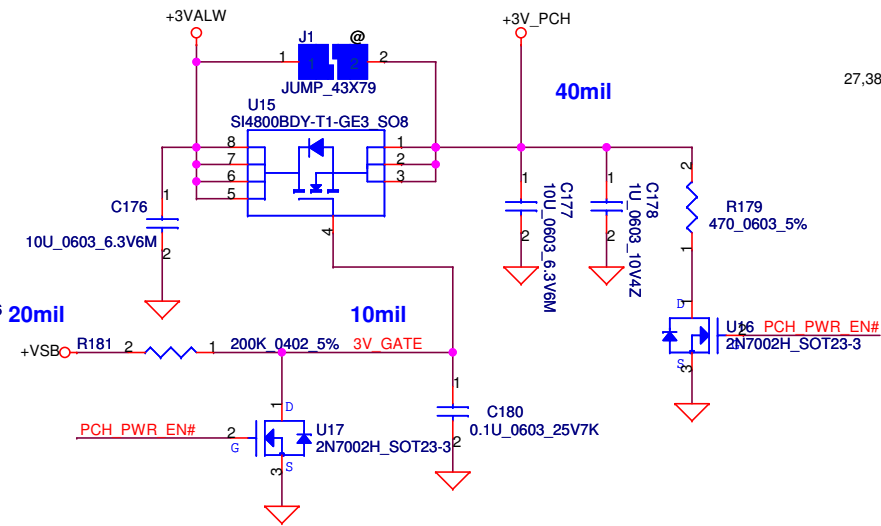


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Size	Custom	Document Number	LA-7531P	Rev
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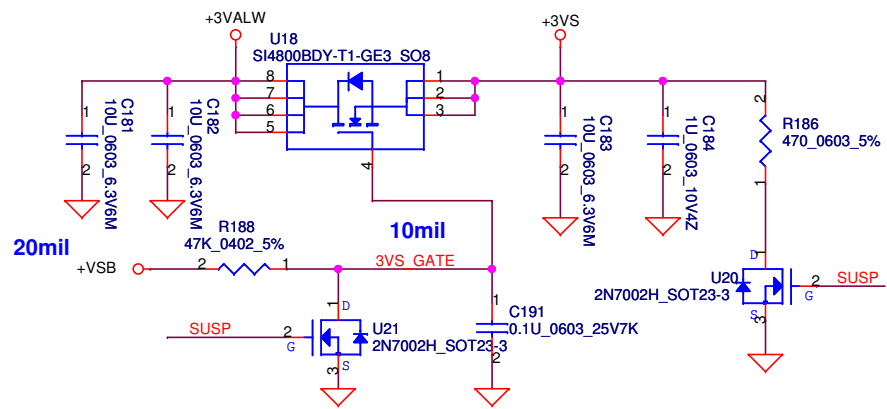
+5VALW TO +5VS



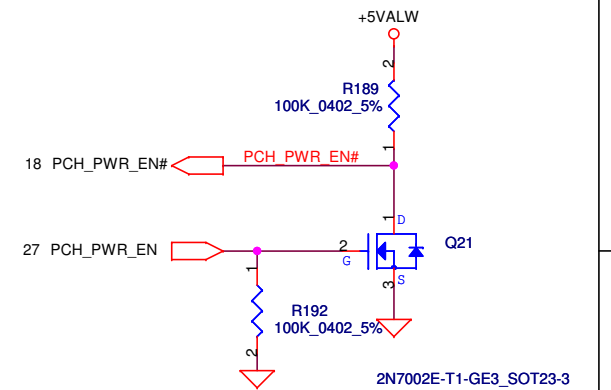
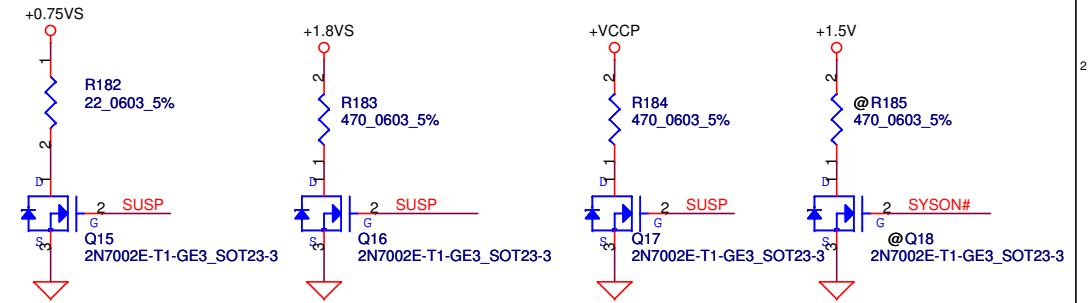
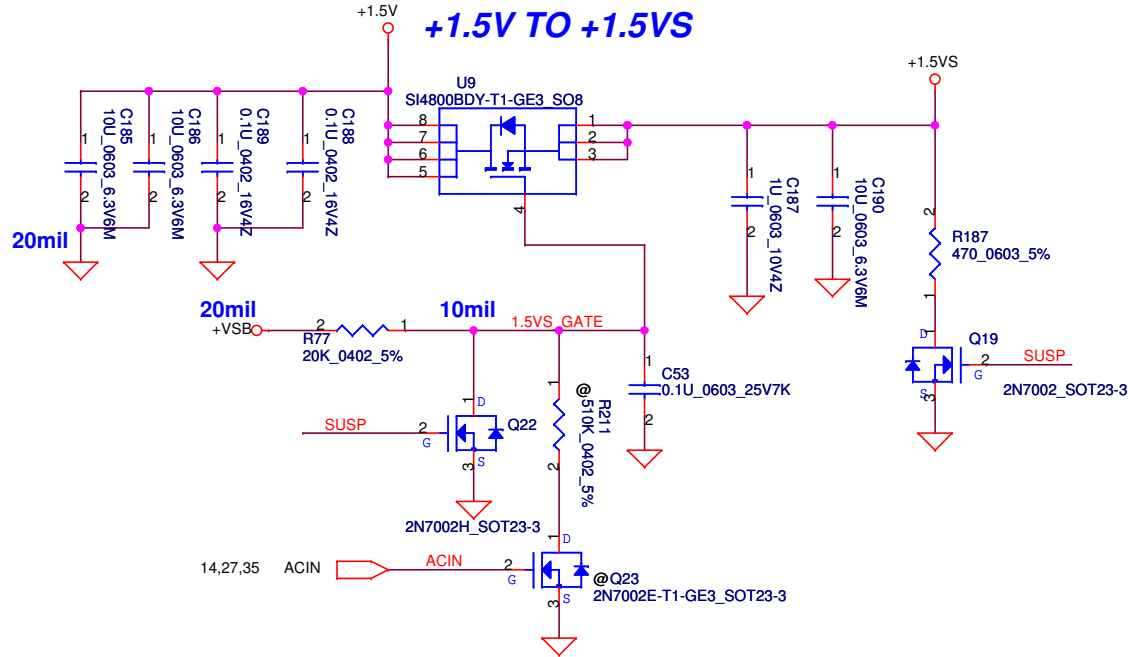
+3VALW TO +3VALW(PCH AUX Power)
Short J1 for PCH VCCSUS3.3



+3VALW TO +3VS



+1.5V TO +1.5VS



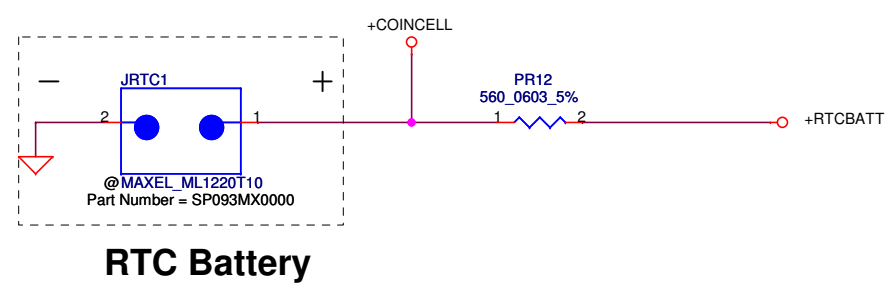
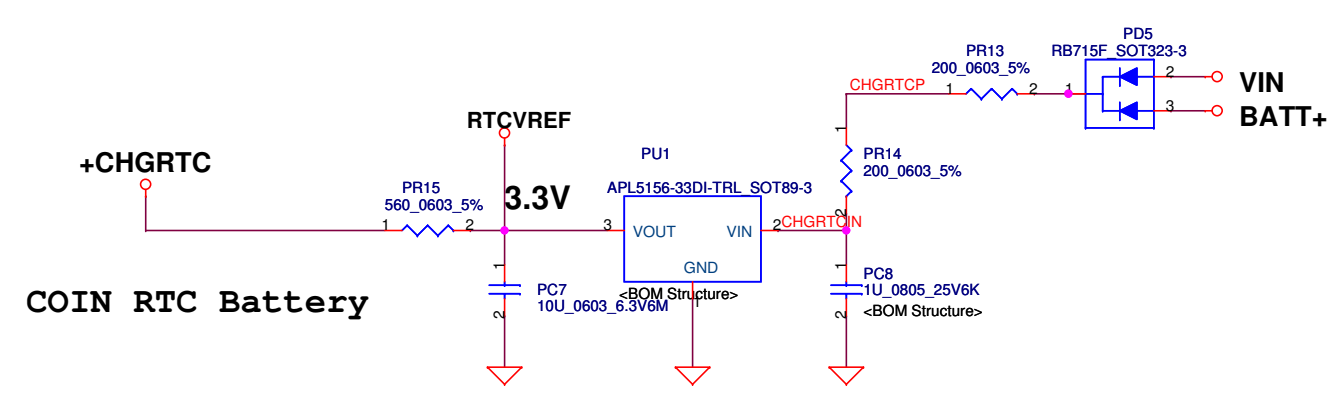
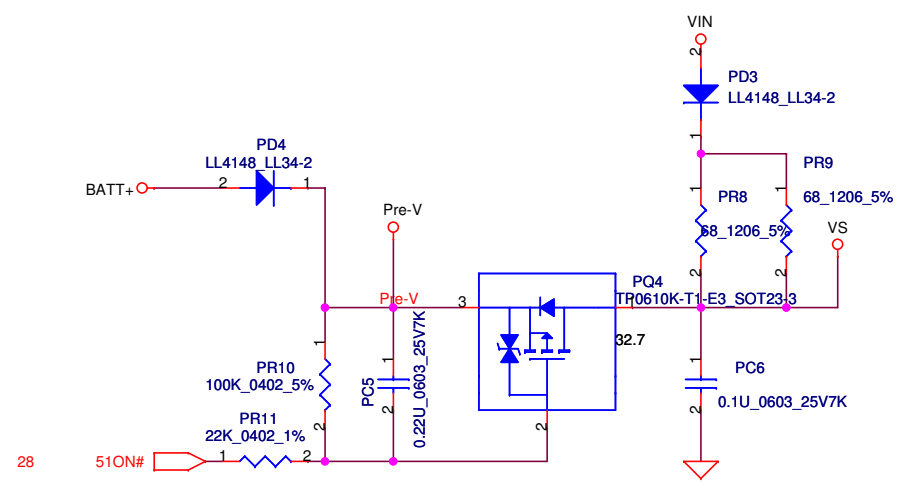
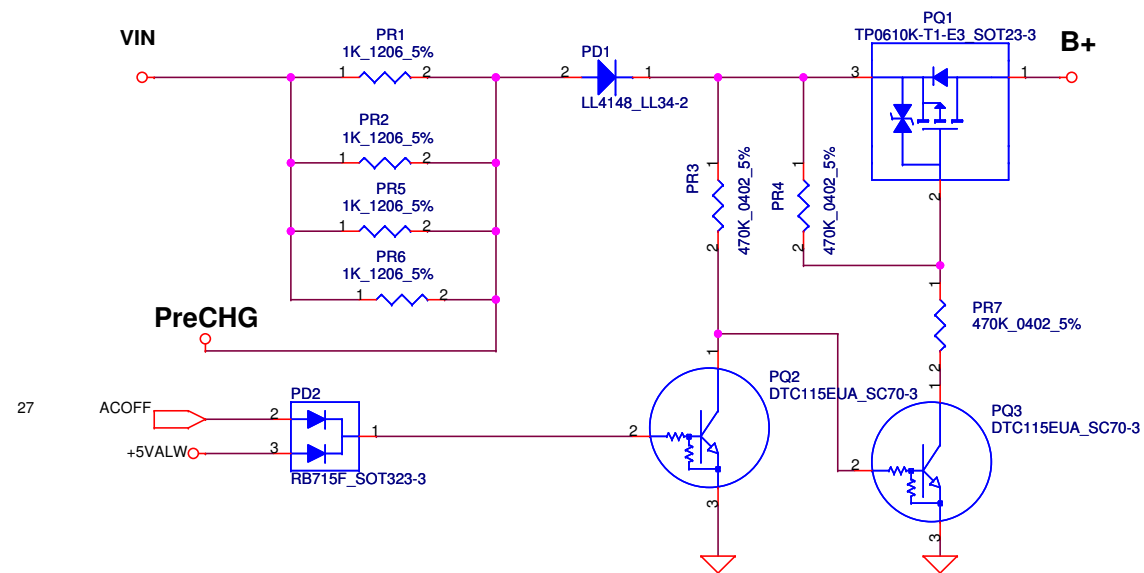
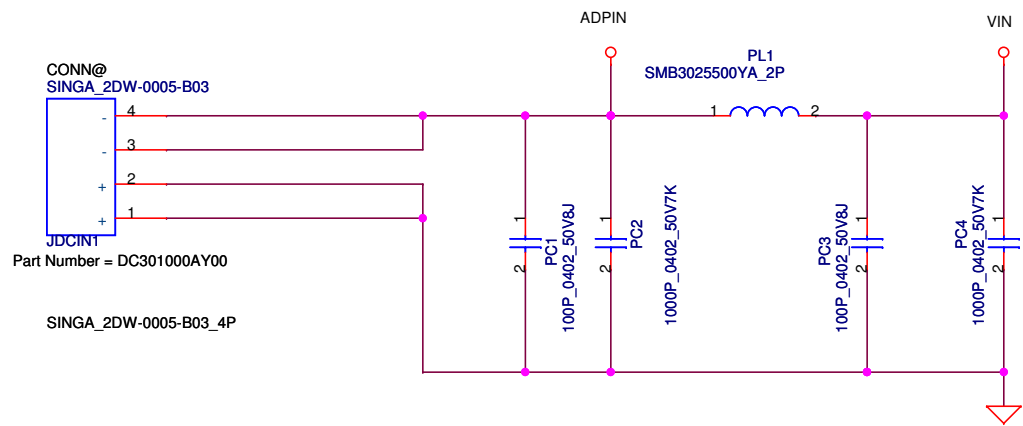
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				Size
			LA-7531P	0.1
Date: Sunday, April 10, 2011		Sheet 31 of 45		

Version Change List (P. I. R. List)

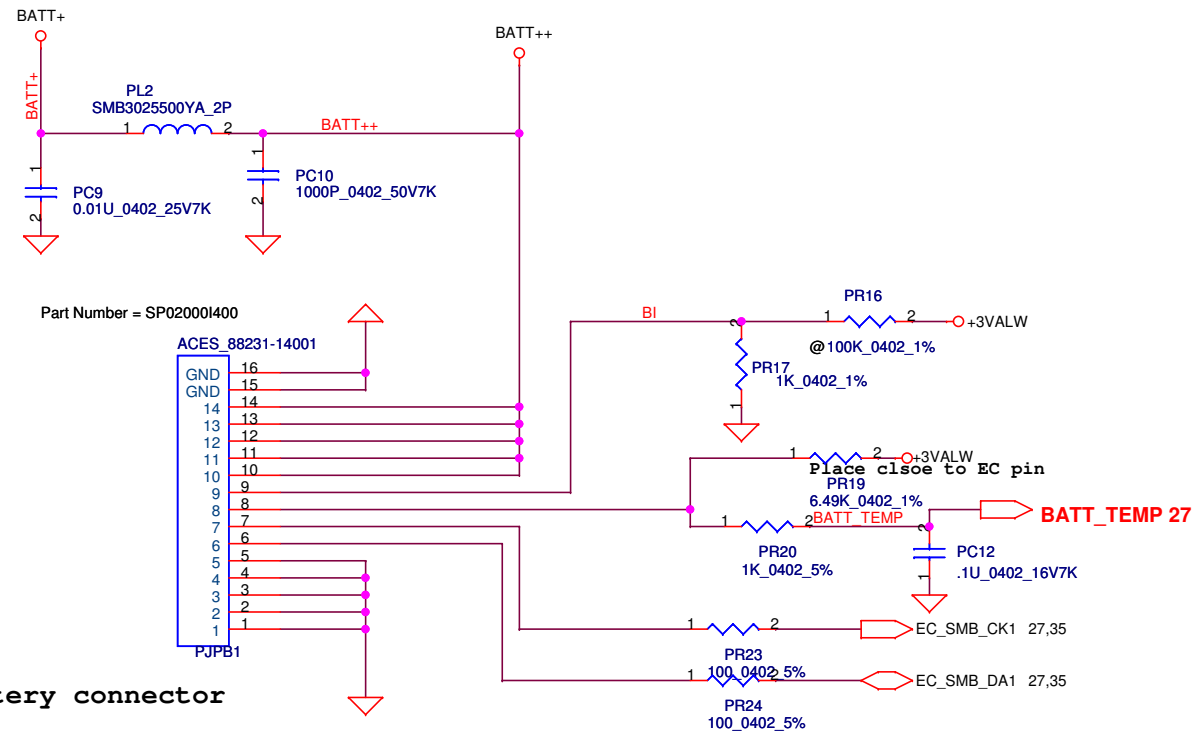
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1	xx	xxx	2011/02/XX	XXXX XXXX	XXXX		Rev01

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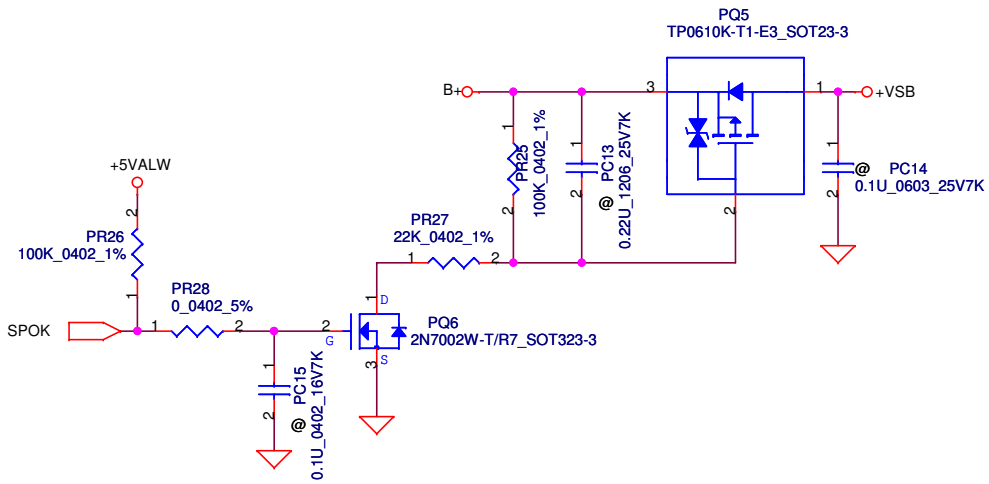
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			Date: Tuesday, March 15, 2011	Rev 0.1



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				Document Number LA-7531P
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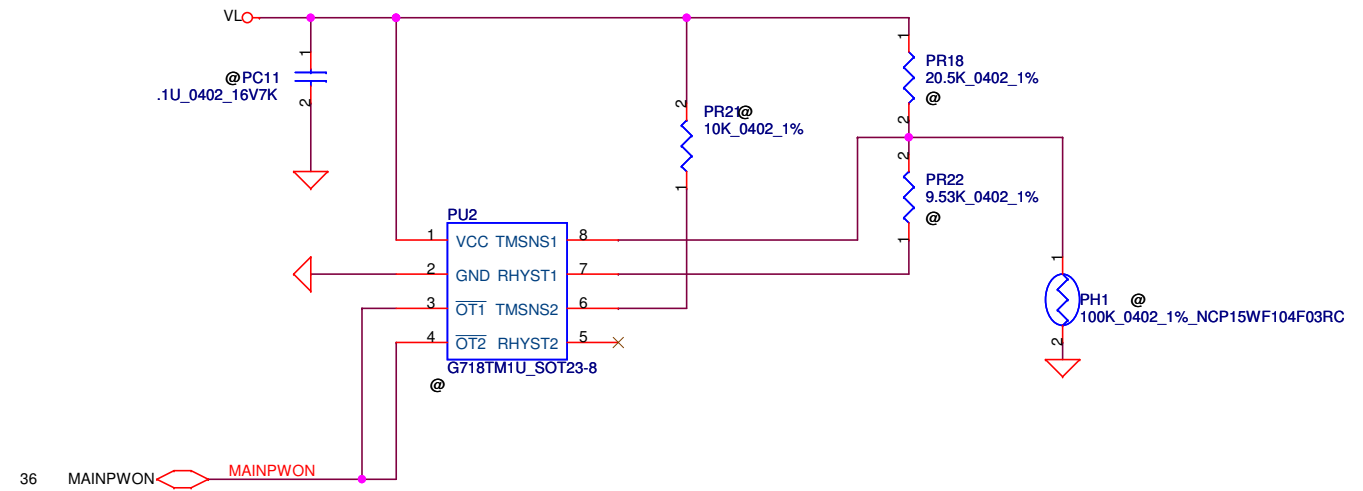


PJPB1 battery connector



Battery Connect/OTP

PH3 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 50 degree C

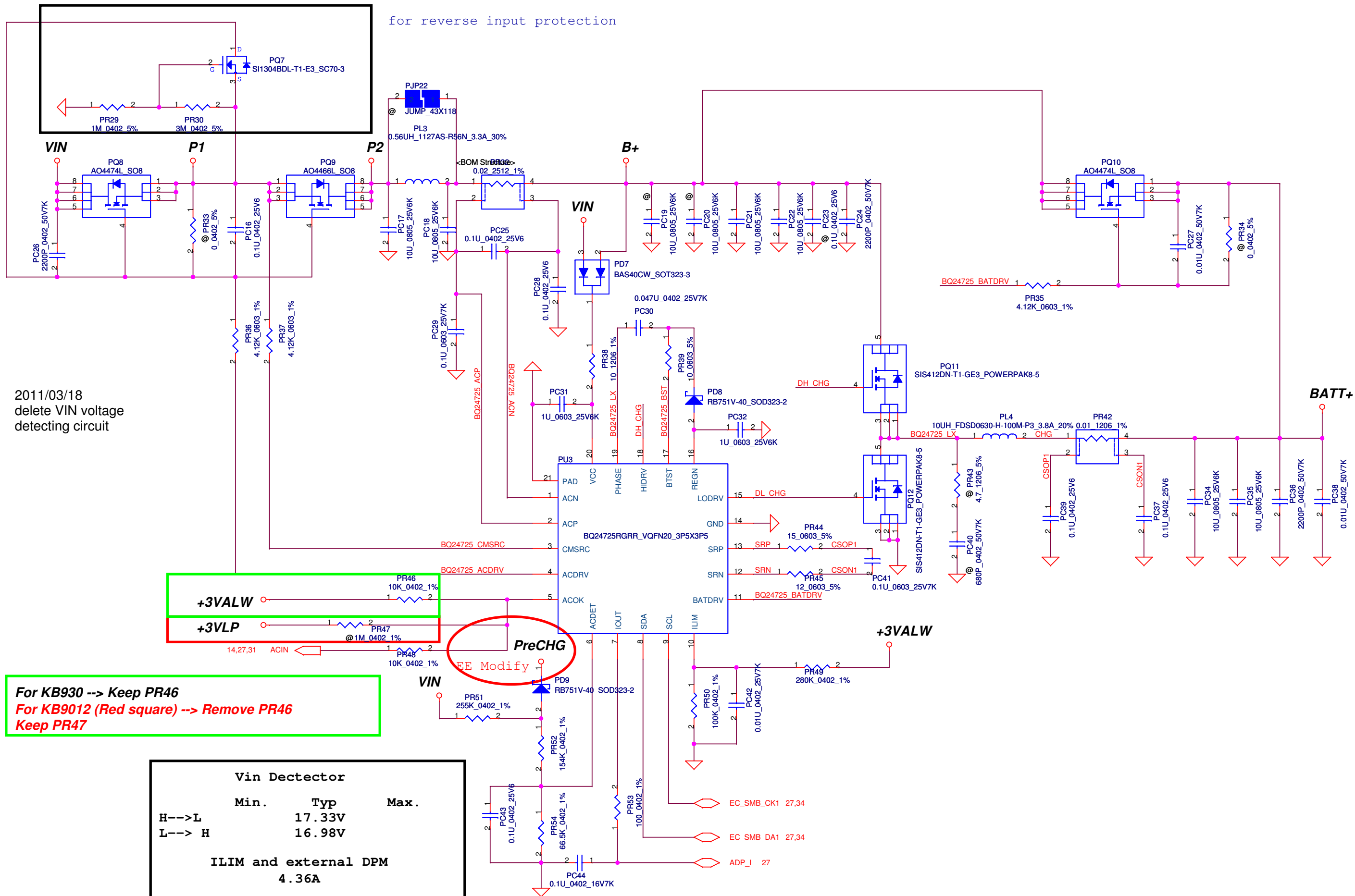


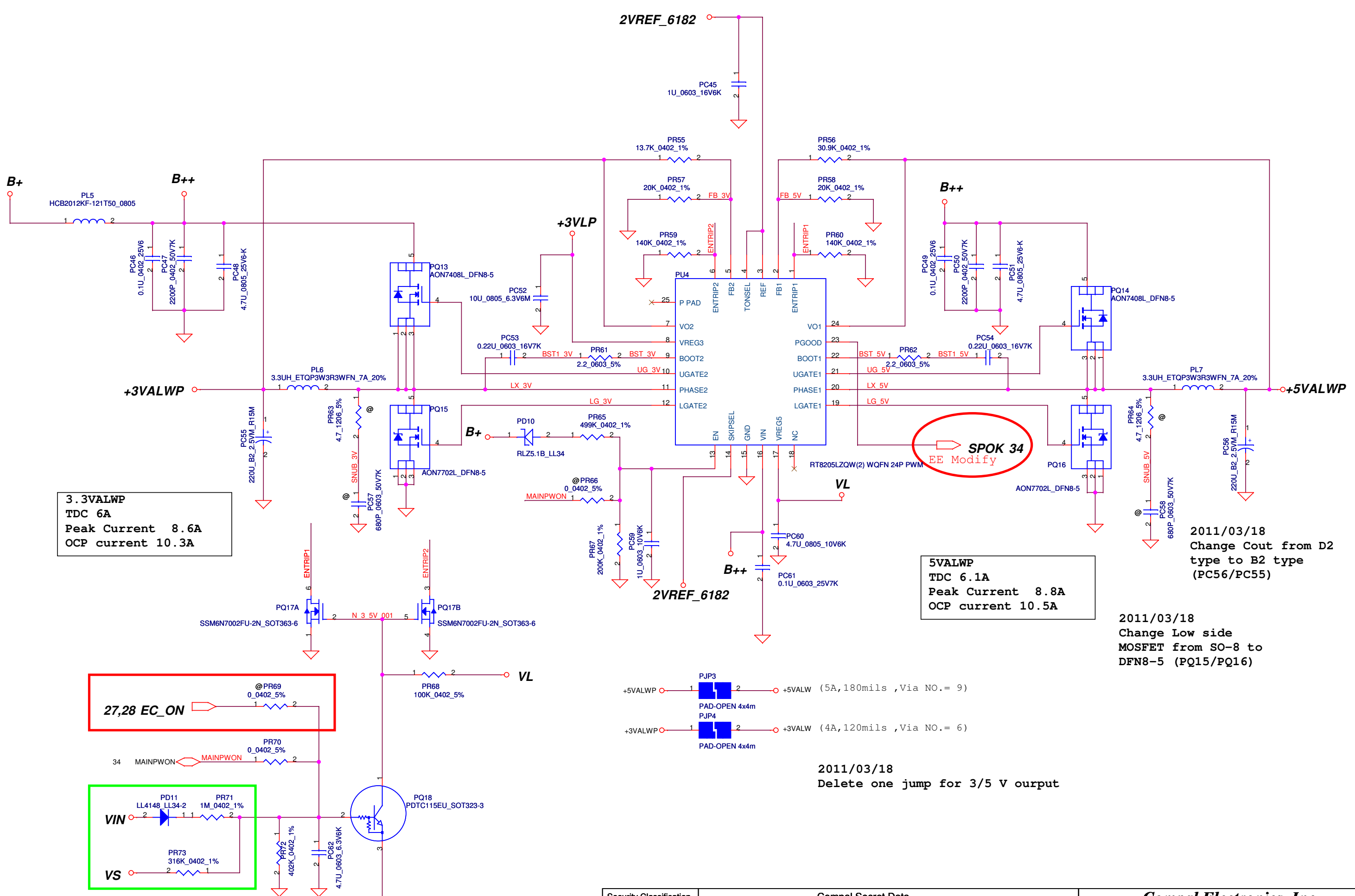
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3. 3VALWP
TDC 6A
Peak Current 8.6A
OCP current 10.3A

5VALWP
TDC 6.1A
Peak Current 8.8A
OCP current 10.5A

2011/03/18
Change Cout from D2
type to B2 type
(PC56/PC55)

2011/03/18
Change Low side
MOSFET from SO-8 to
DFN8-5 (PQ15/PQ16)

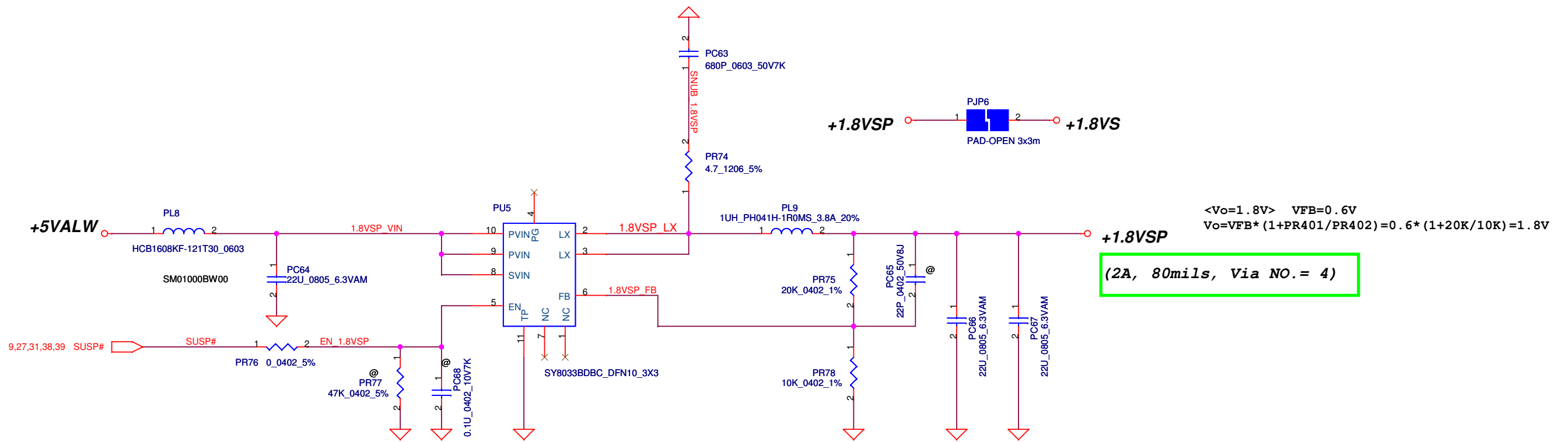
2011/03/18
Delete one jump for 3/5 V output

27,28 EC_ON

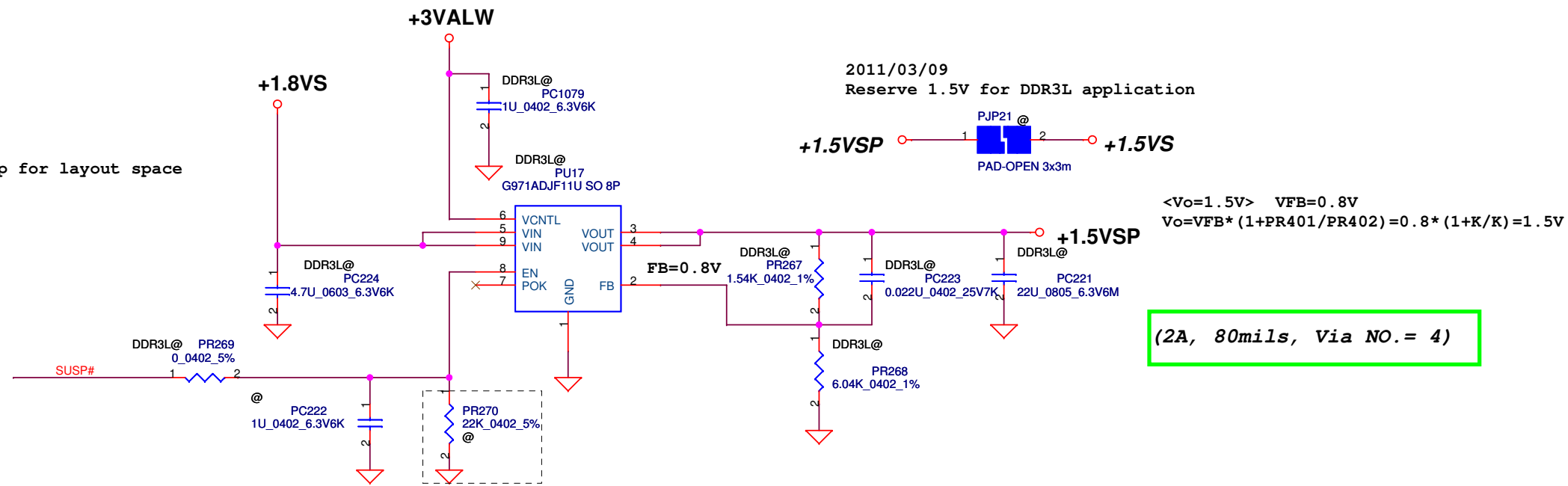
VIN
VS

For KB930 --> Keep PD8, PR53, PR52, Remove PR76
For KB9012 (Red square) --> Remove PD8, PR53, PR52
Keep PR76

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Issued Date	2007/08/02	Deciphered Date	2008/08/02	PWR-3VALWP/5VALWP	
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				Custom	0.1
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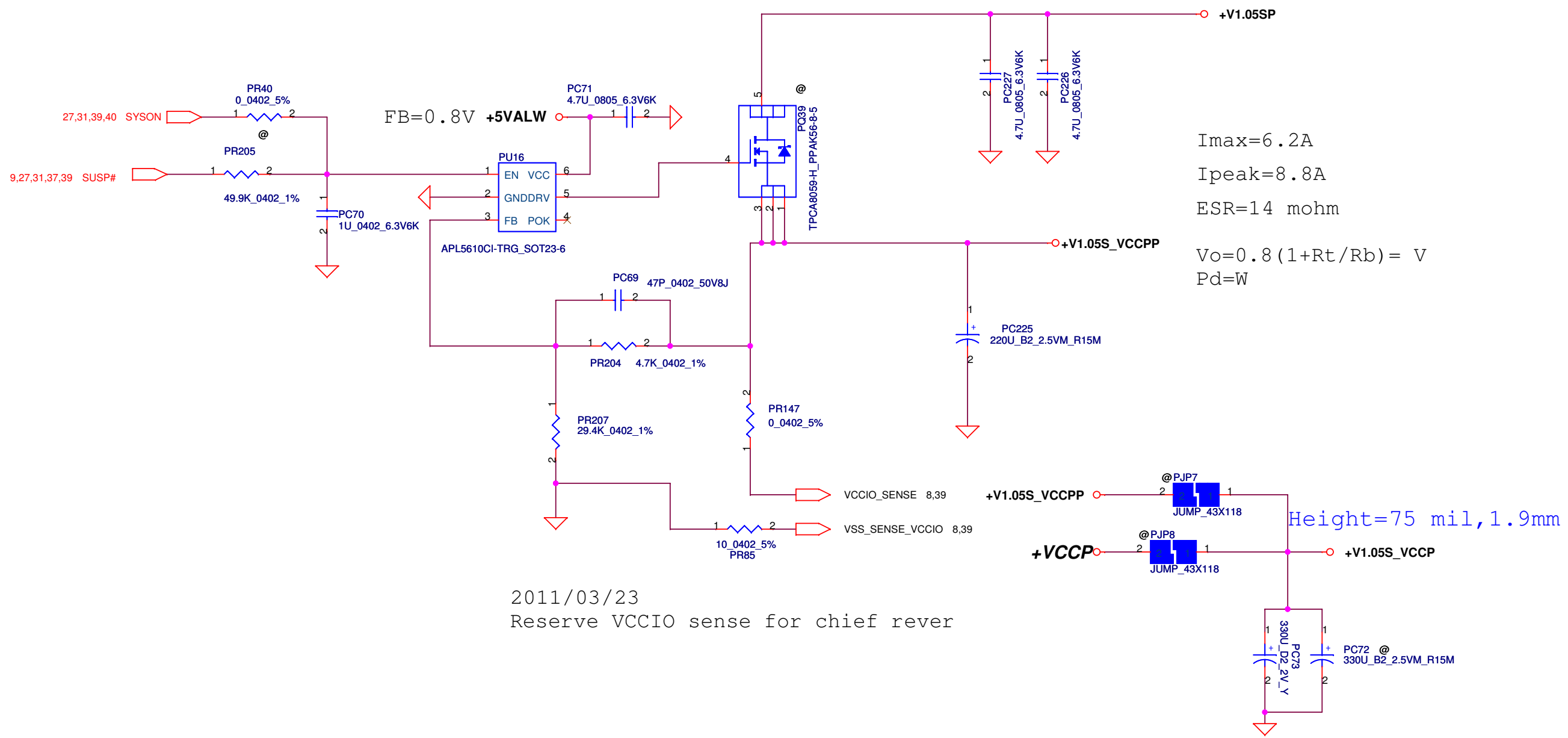
2011/03/23
Delete jump for layout space



I_{en}=10uA, V_{th}=0.3V, notice the res. and pull high voltage from HW

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2011/03/15
 Change Cout to D2 type
 Change PQ26 to TPCA8059 (Rds-on)
 2011/03/18
 Change Cout from D2 type to B2
 typt
 2011/03/22
 delete input jump



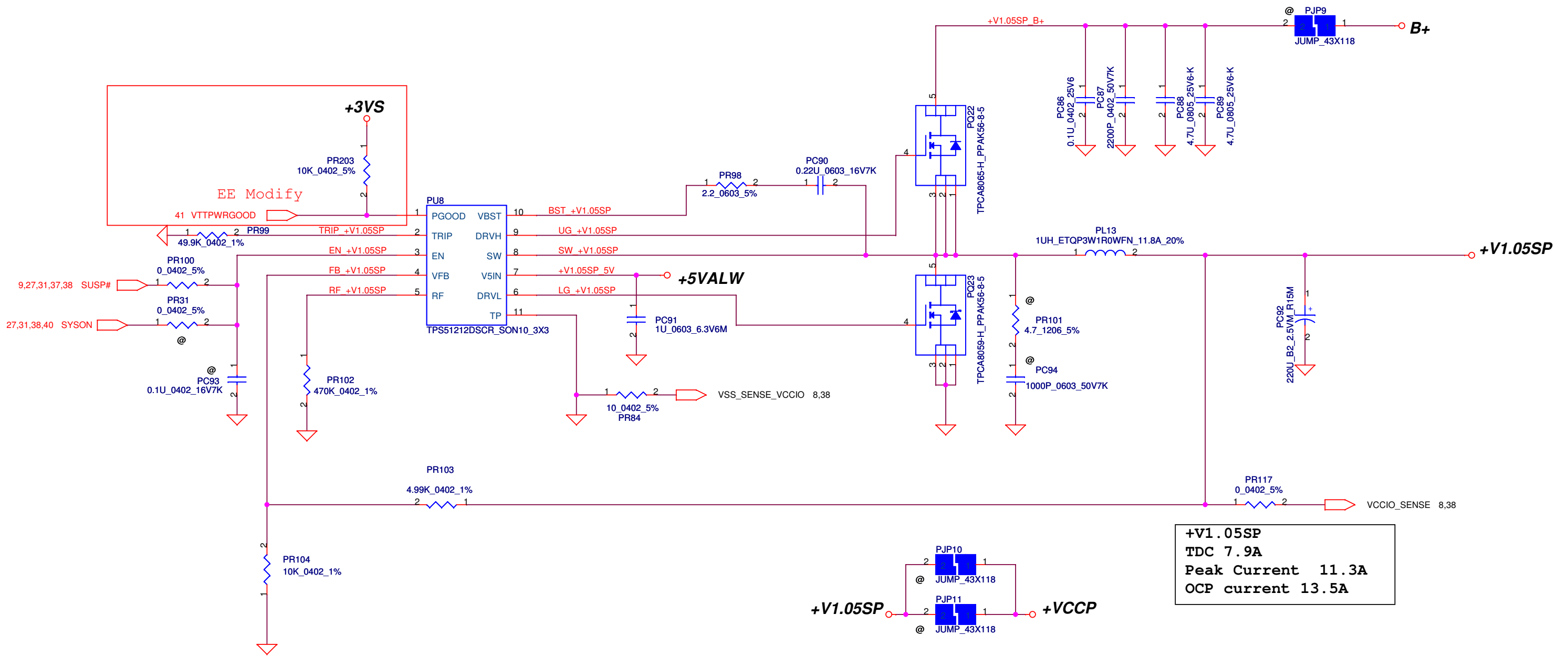
$I_{max}=6.2A$
 $I_{peak}=8.8A$
 $ESR=14\text{ mohm}$
 $V_o=0.8(1+R_t/R_b)=V$
 $P_d=W$

Height=75 mil, 1.9mm

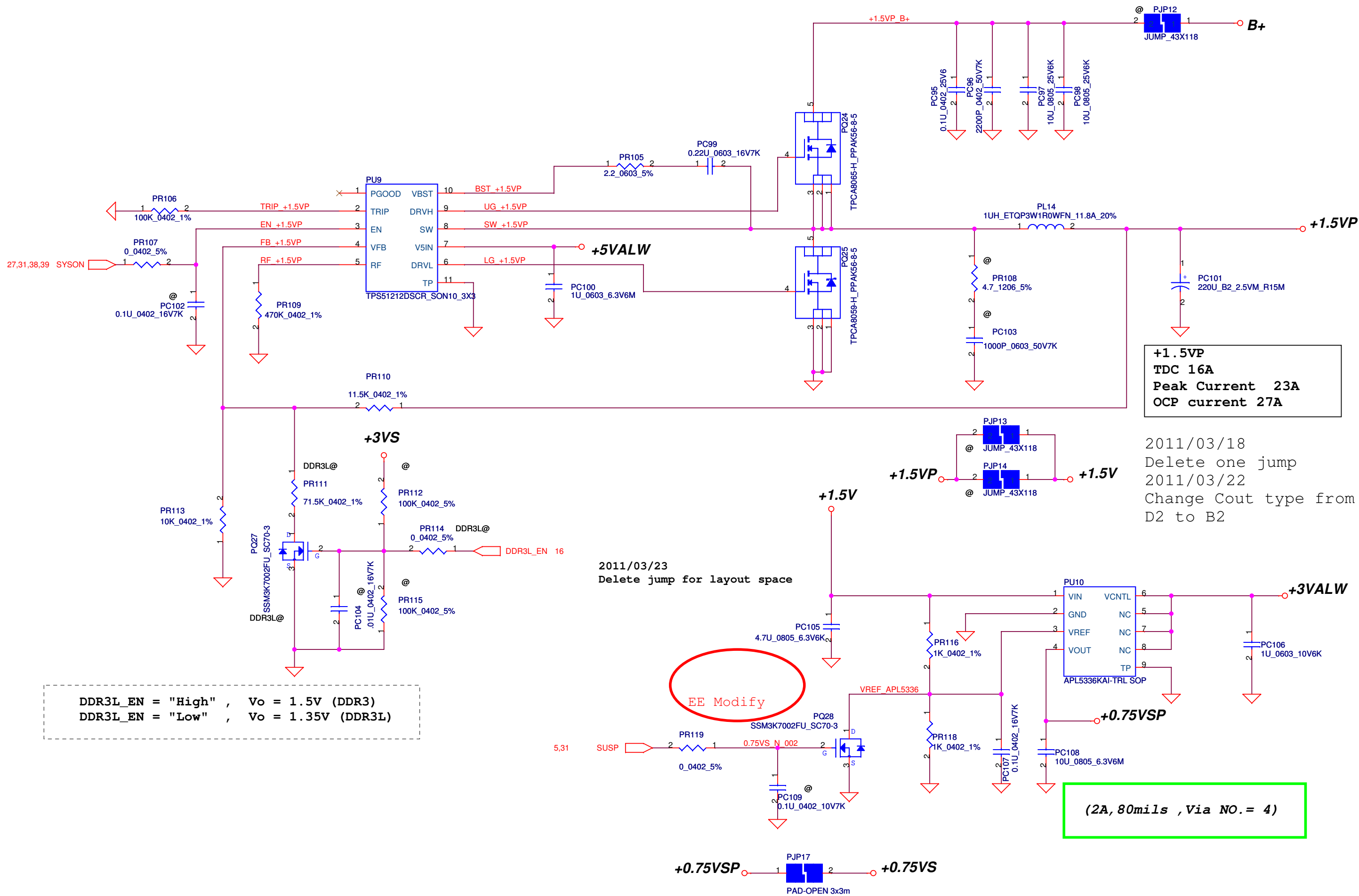
2011/03/23
 Reserve VCCIO sense for chief rever

2011/03/18
 Change PR72 form D2 type to B2 type.
 need to take care the ESR differentia

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				Size	Document Number	Rev
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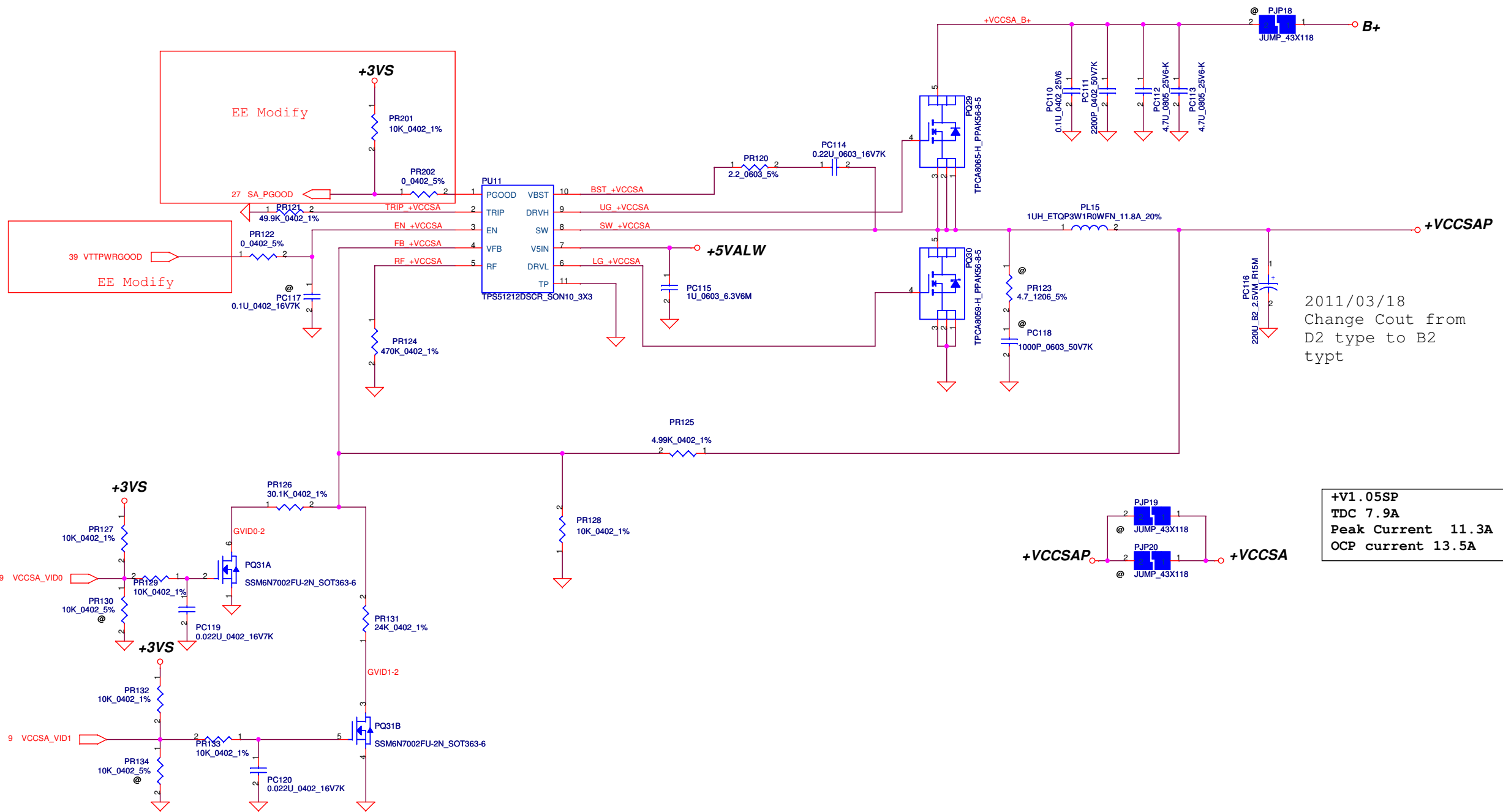


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				Size Custom
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+VCC_SAP
 TDC 4.2A
 Peak Current 6A
 OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

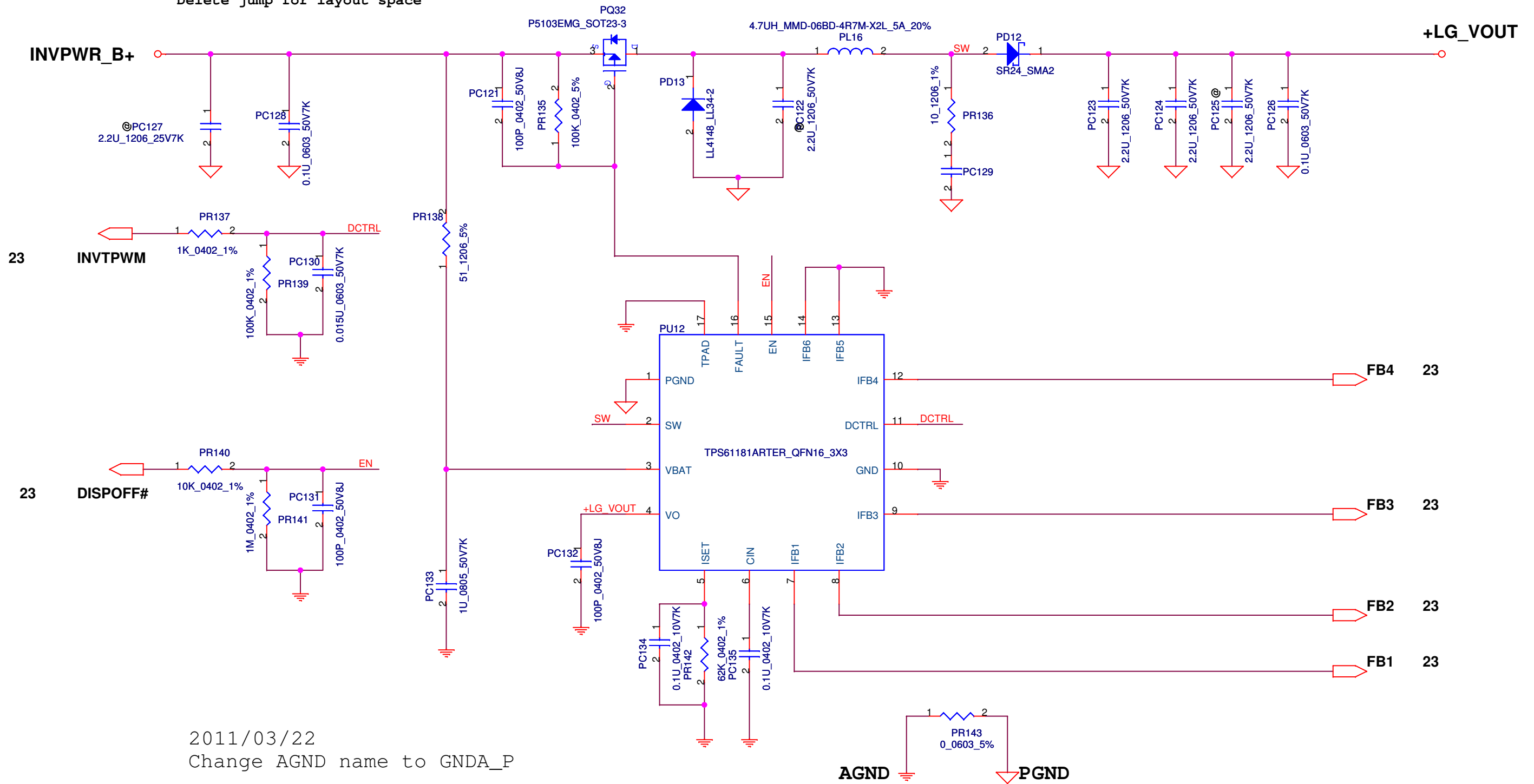


2011/03/18
 Change Cout from
 D2 type to B2
 typt

+V1.05SP
 TDC 7.9A
 Peak Current 11.3A
 OCP current 13.5A

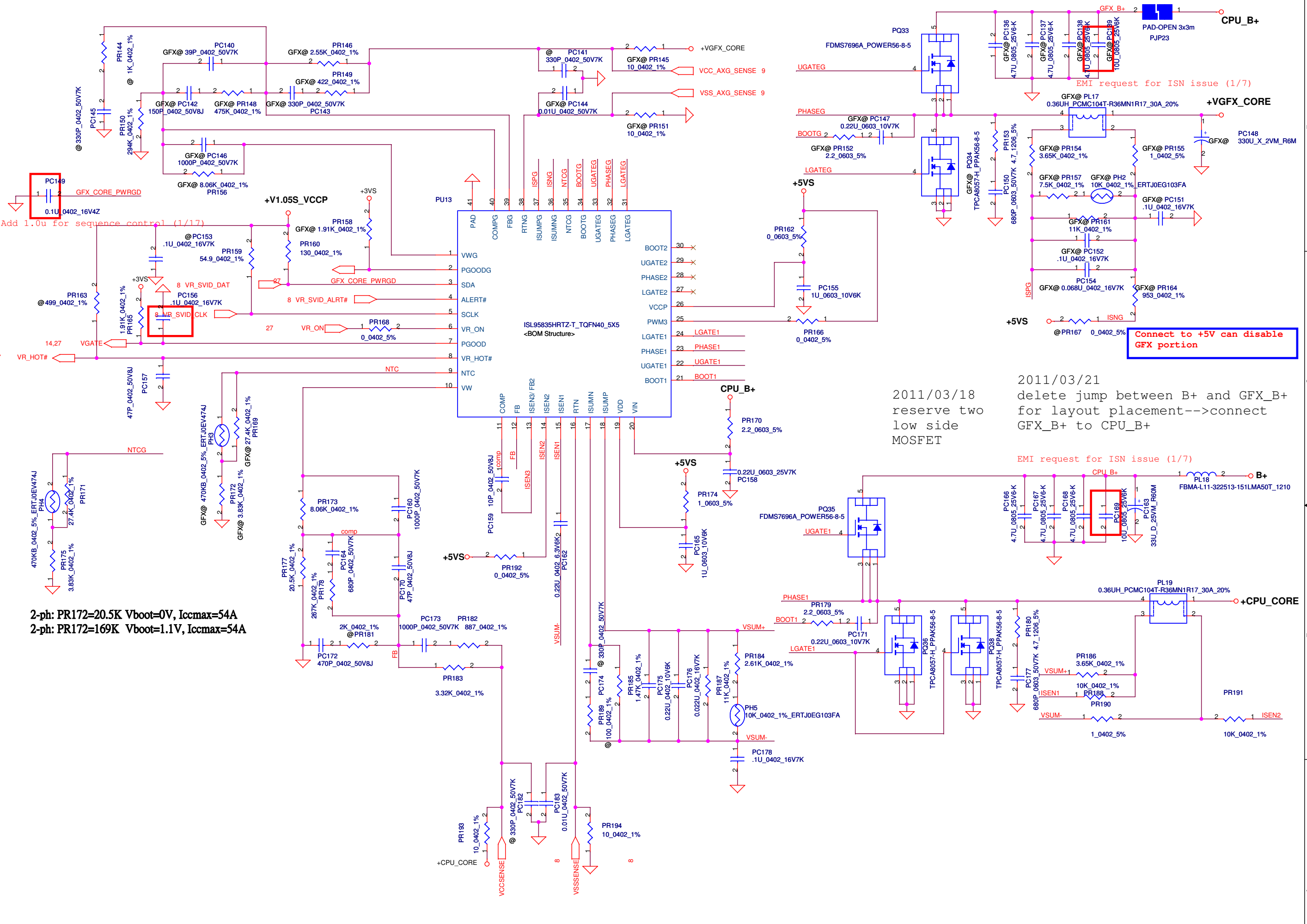
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2011/03/23
Delete jump for layout space



2011/03/22
Change AGND name to GNDA_P

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				Size B
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2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
 2-ph: PR172=169K Vboot=1.1V, Iccmax=54A

+CPU_CORE
 Iocp=40A, IccMAX=28A
 Load line=1.9mohm
 DCR=1.1mohm

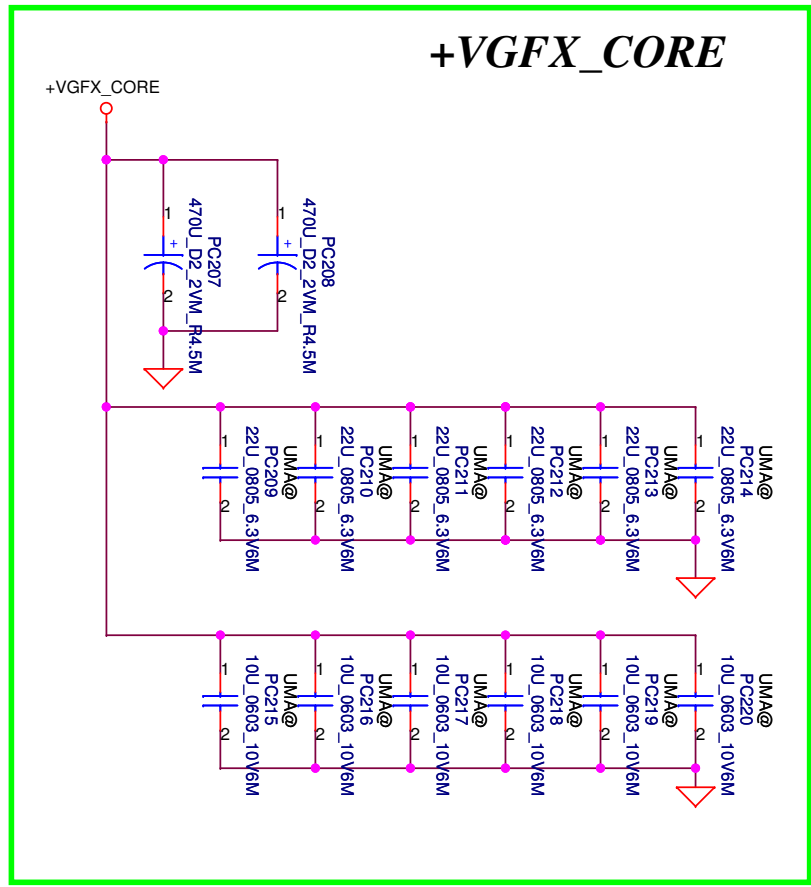
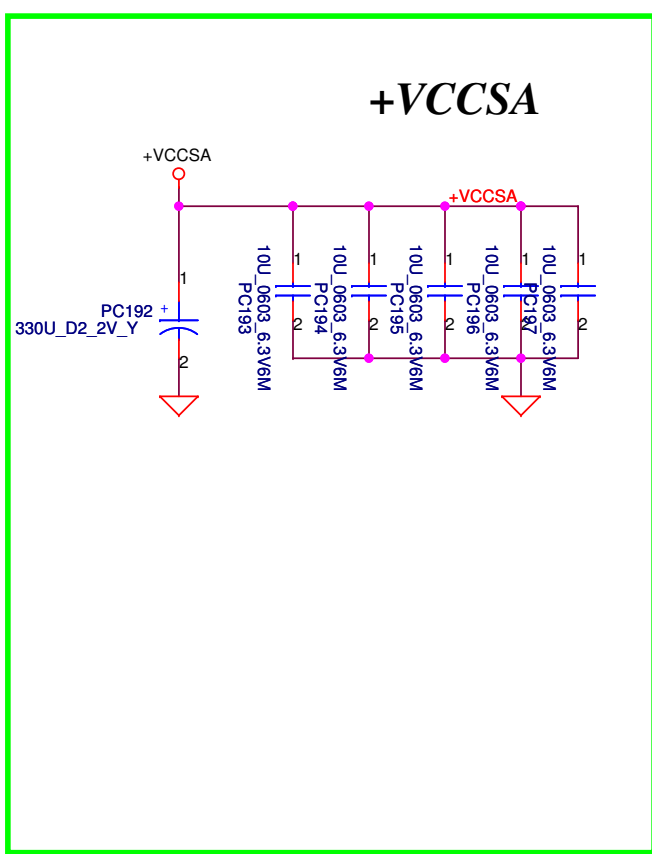
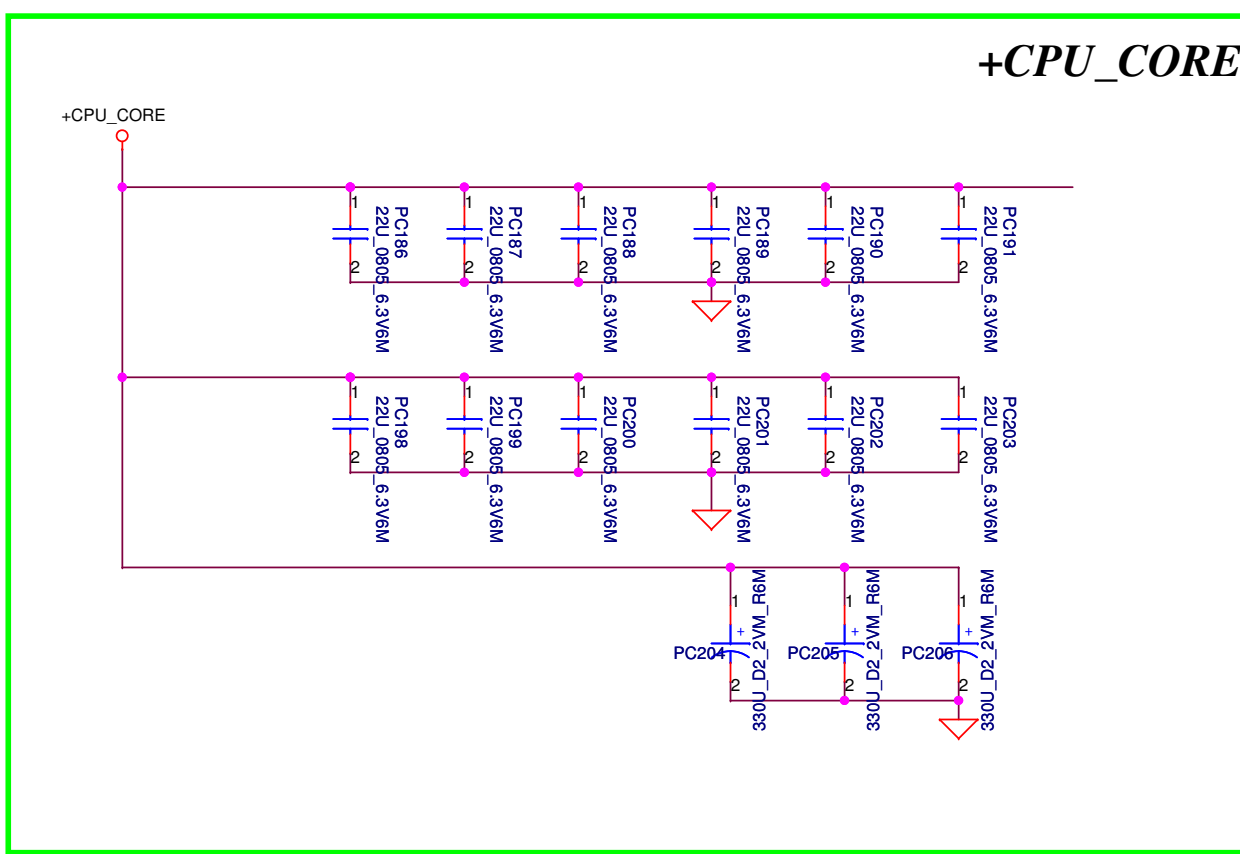
+GFX_CORE
 Iocp=20A, IccMAX=13A
 Load line=3.9mohm
 DCR=1.1mohm

2011/03/18
 reserve two
 low side
 MOSFET

2011/03/21
 delete jump between B+ and GFX_B+
 for layout placement-->connect
 GFX_B+ to CPU_B+

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<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>

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