

# Compal Confidential

Model Name : QILE1 & QILE2  
File Name : LA-8131P, LA-8132P  
BOM P/N:

**QILE1:**  
4319GG39L01 : SMT MB A8131 QILE1 DIS-N13P  
4319GG39L02 : SMT MB A8131 QILE1 DIS GPU-N13M  
4319GG39L03 : SMT MB A8131 QILE1 UMA

**QILE2:**  
4319GJ39L01 : SMT MB A8133 QILE2 DIS-N13P  
4319GJ39L02 : SMT MB A8133 QILE2 DIS GPU-N13M  
4319GJ39L03 : SMT MB A8133 QILE2 UMA

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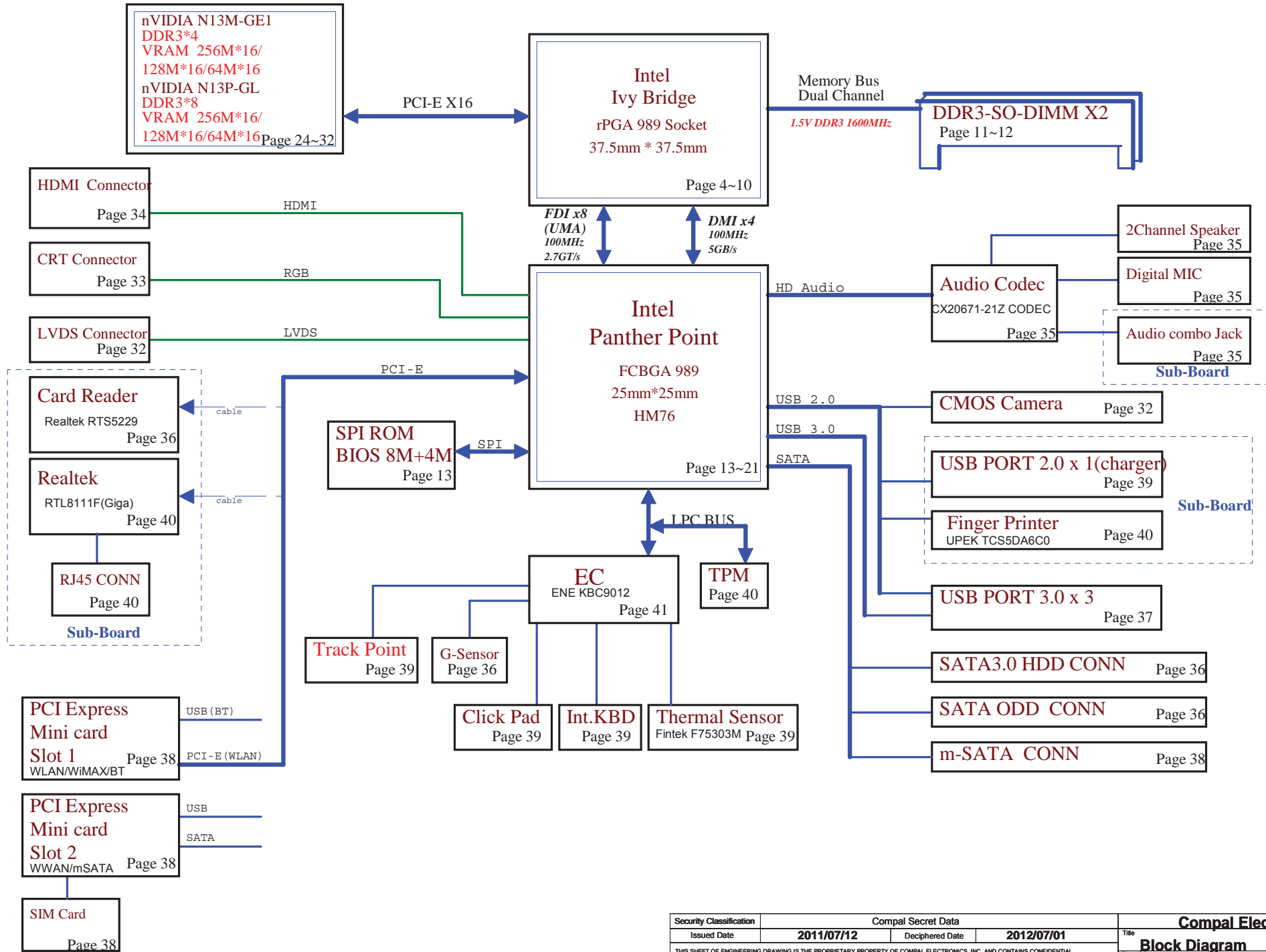
## M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH  
GPU nVIDIA N13M-GE1 / N13P-GL

2011-12-20

REV:0.6

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				Document Number	LA-8131P



### Voltage Rails

power plane	State	+B	+5VALW	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0		○	○	○	○	○	○ M3 Supported
S3		○	○	○	○	✗	○ M3 Supported
S5 S4/AC		○	○	✗	✗	✗	○ M3 Supported
S5 S4/ Battery only		✗	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist		✗	✗	✗	✗	✗	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	
7	

### EC SM Bus1 address

Device	Address
Smart Battery	0001 011x b

### EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

### PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

### USB Port Table

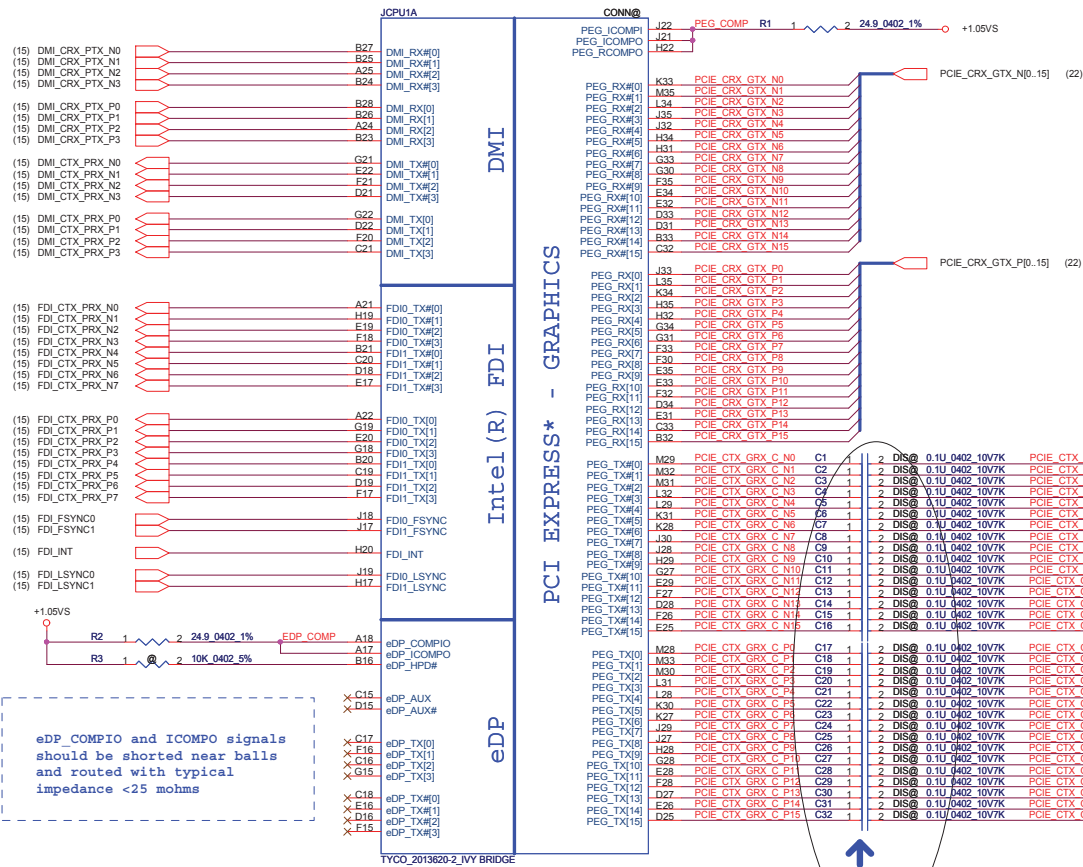
	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB 3.0 Port (Left Side)
		2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port (Left Side)
		4	
		5	Camera
EHCI2	UHCI3	6	
		7	
		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN/BT)
		11	FPR
		12	Mini Card(WWAN)
UHCI6	13	Blue Tooth	

### BOM Structure Table

BTO Item	BOM Structure
Connector	CONN@
45 LEVEL	45@
Unpop	@
nVidia	DIS@
INTEL DD3 M3	M3@
SIM Card Slot	3G@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N13M	N13M@
GPU N13P	N13MP

### SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SMLOCLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	



PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

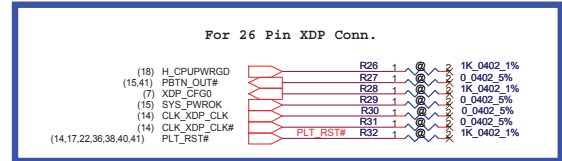
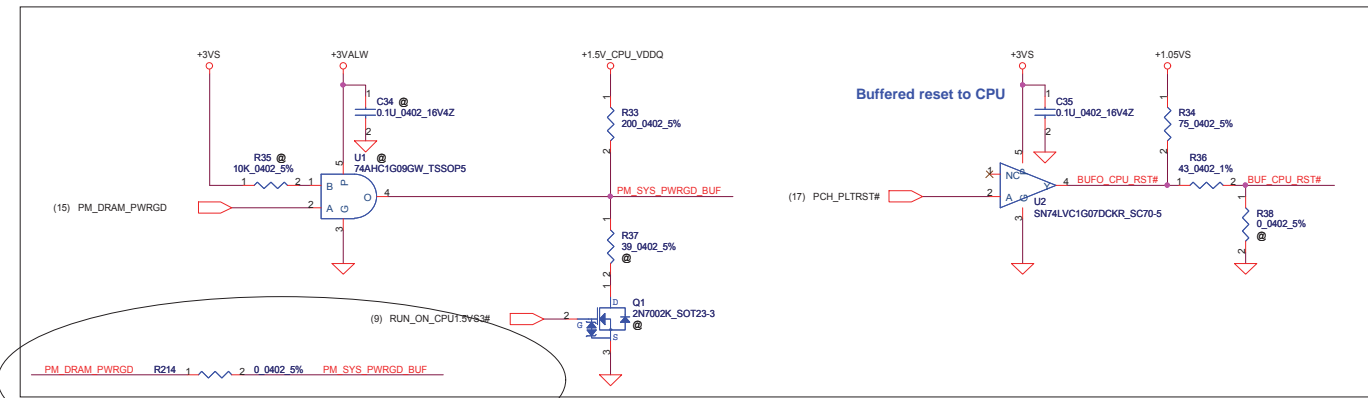
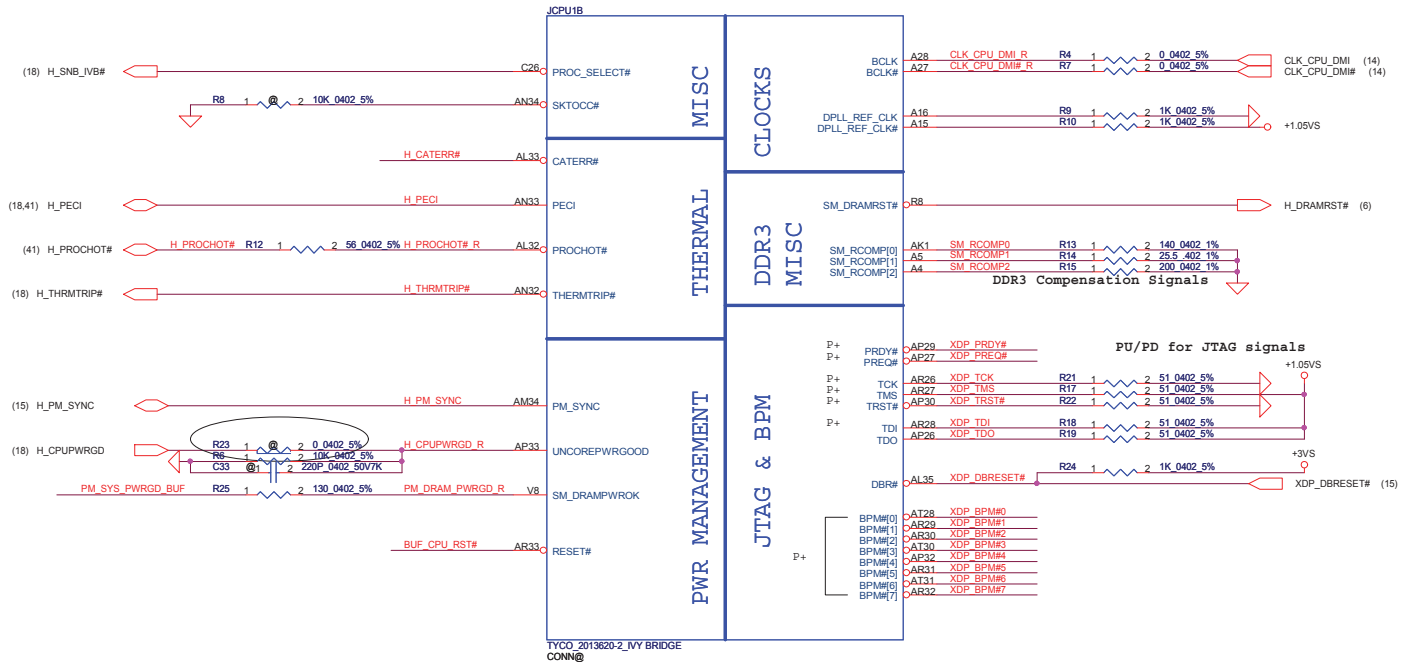
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

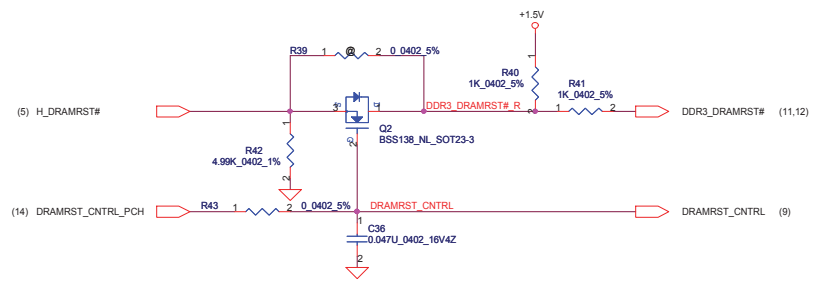
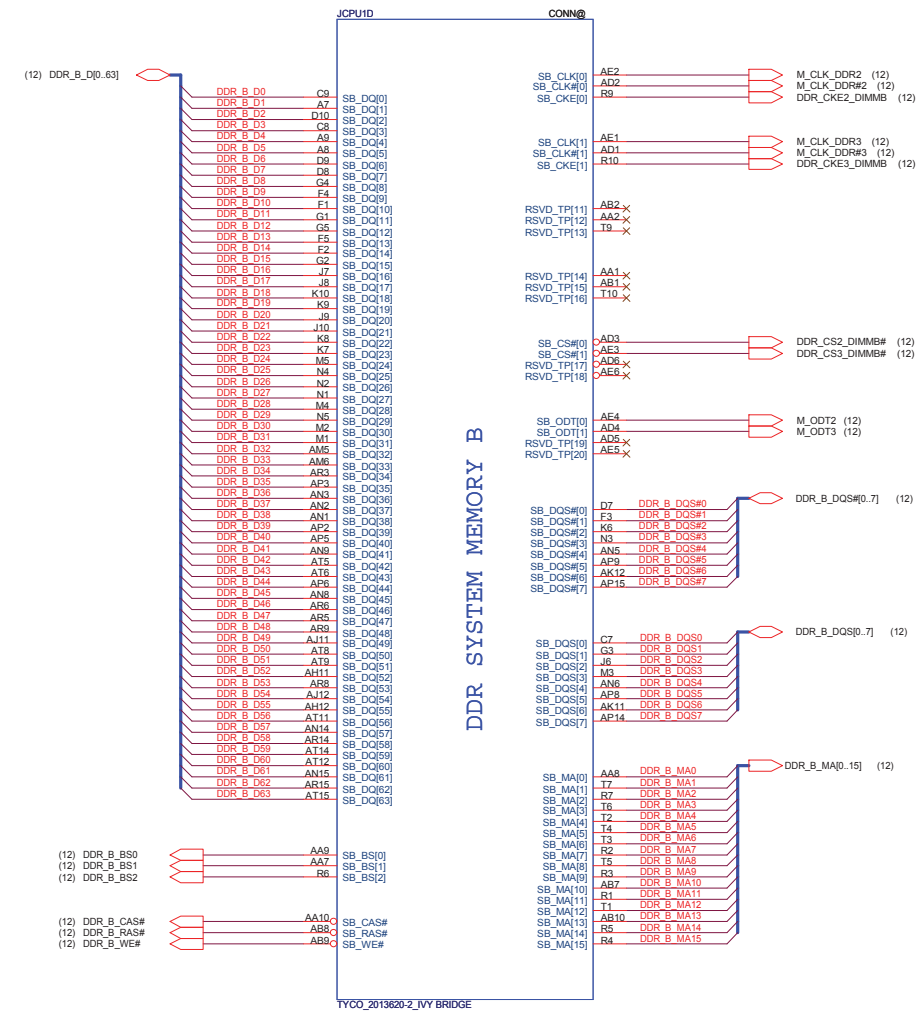
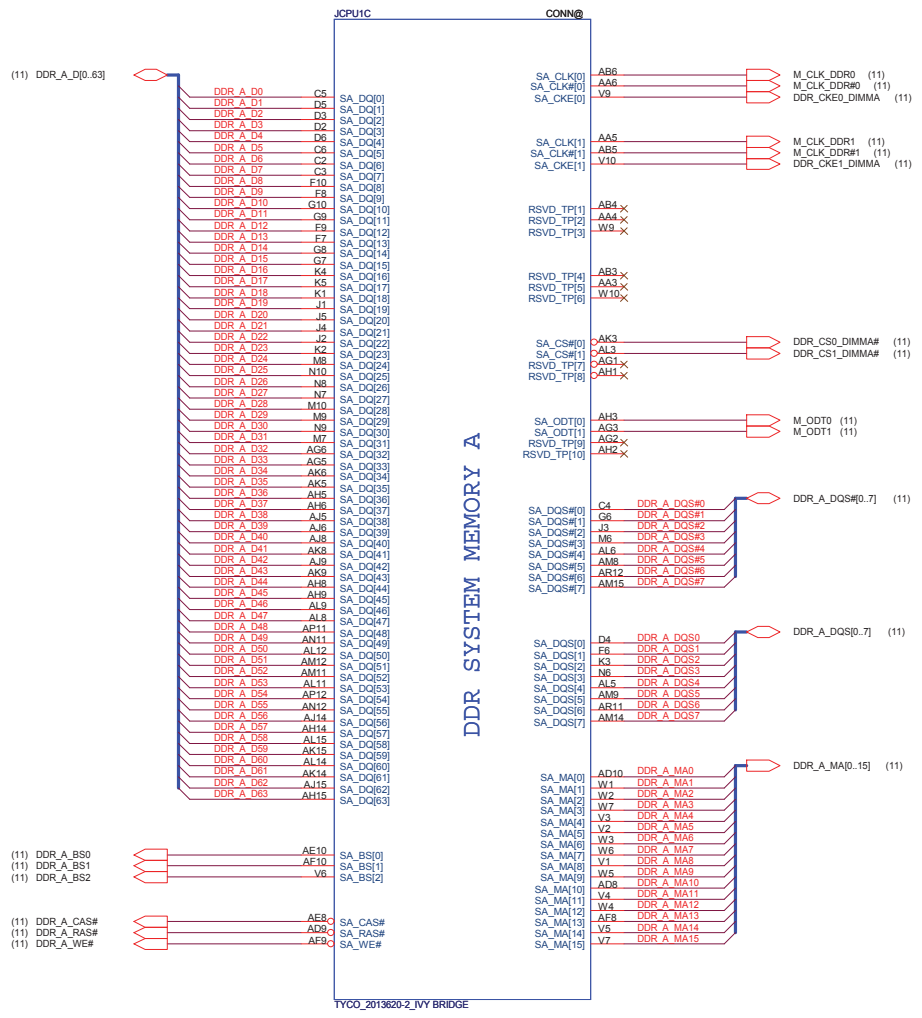
eDP COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Nvidia support PCIe Gen2

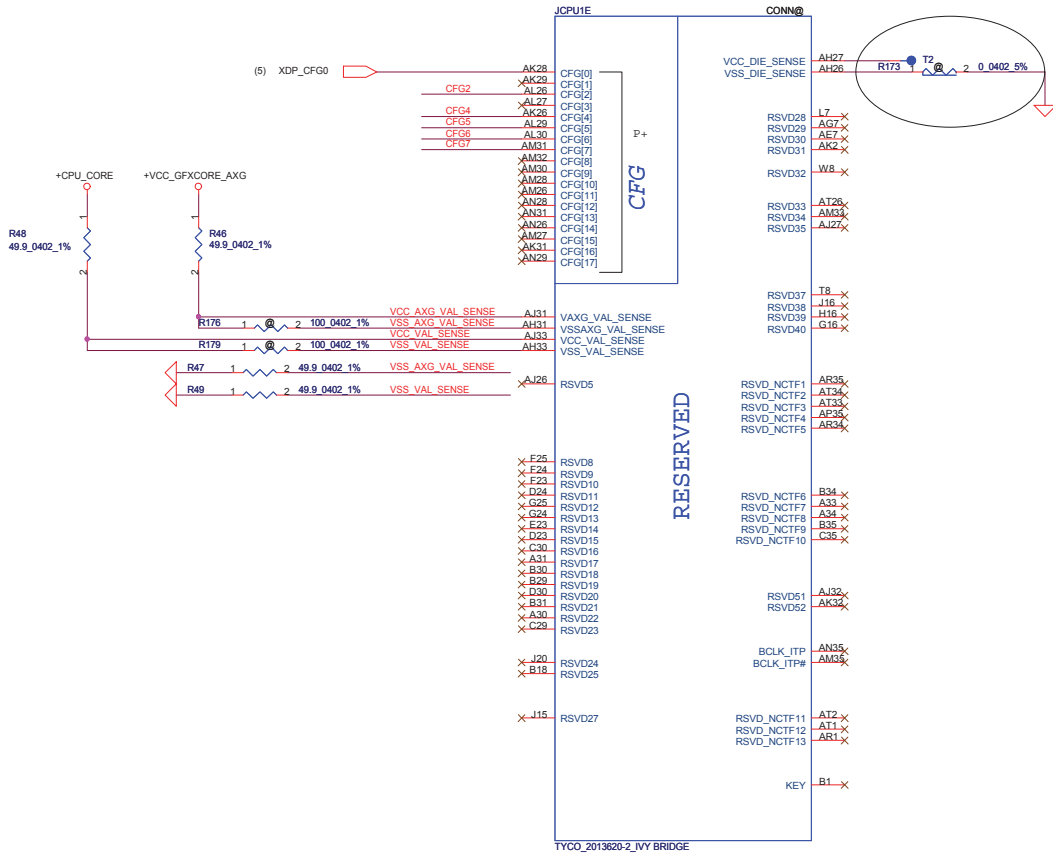
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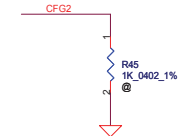
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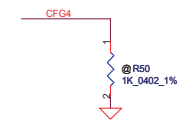
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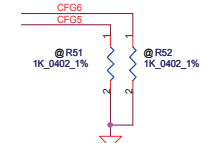
### CFG Straps for Processor



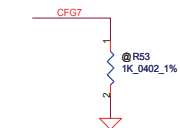
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<ul style="list-style-type: none"> <li>* 1: Normal Operation; Lane # definition matches socket pin map definition</li> <li>0: Lane Reversed</li> </ul>



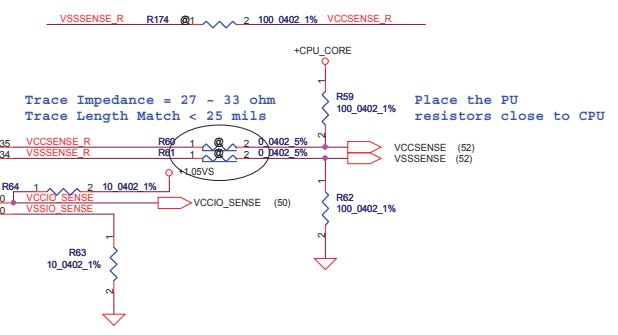
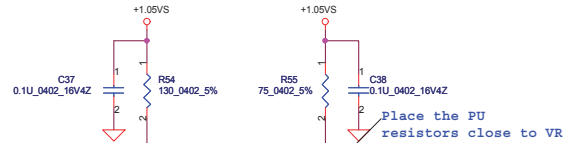
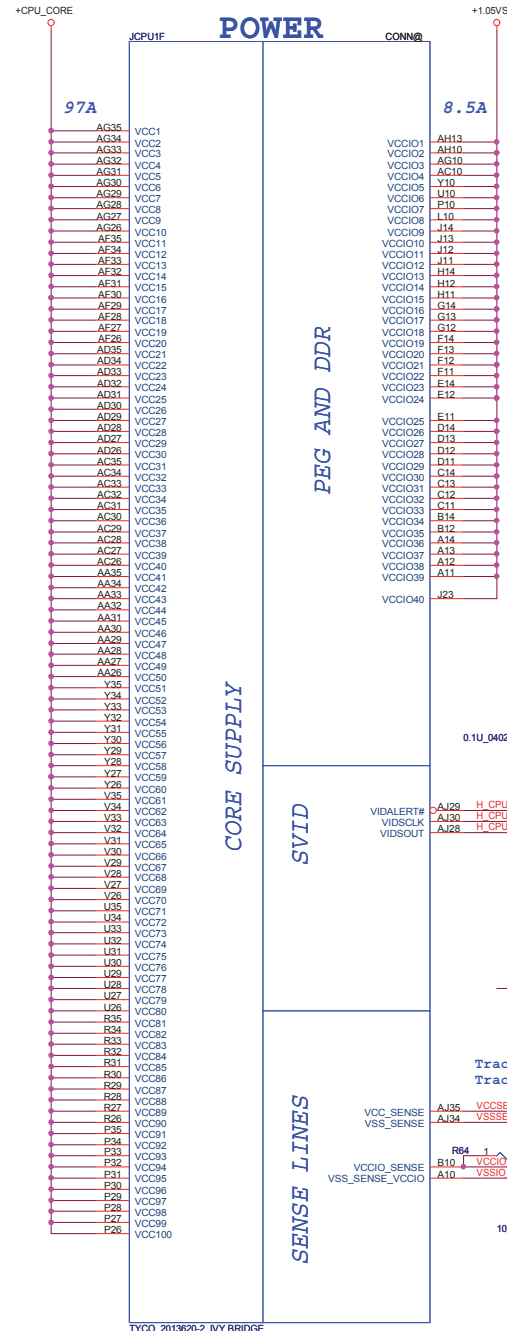
Display Port Presence Strap	
CFG4	<ul style="list-style-type: none"> <li>* 1 : Disabled; No Physical Display Port attached to Embedded Display Port</li> <li>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</li> </ul>



PCIe Port Bifurcation Straps	
CFG[6:5]	<ul style="list-style-type: none"> <li>*11: (Default) x16 - Device 1 functions 1 and 2 disabled</li> <li>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</li> <li>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</li> <li>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</li> </ul>



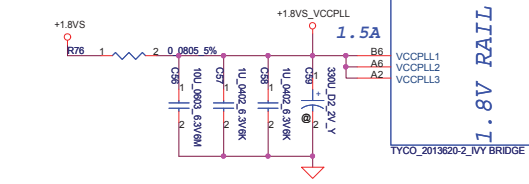
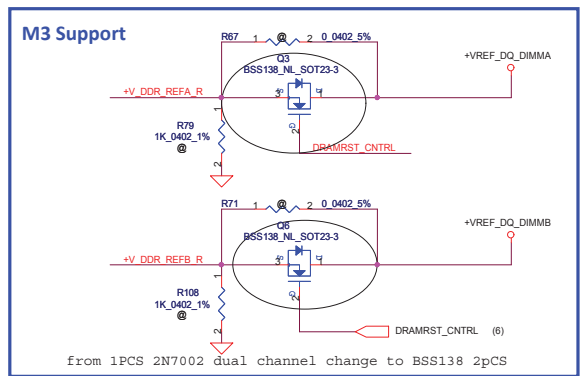
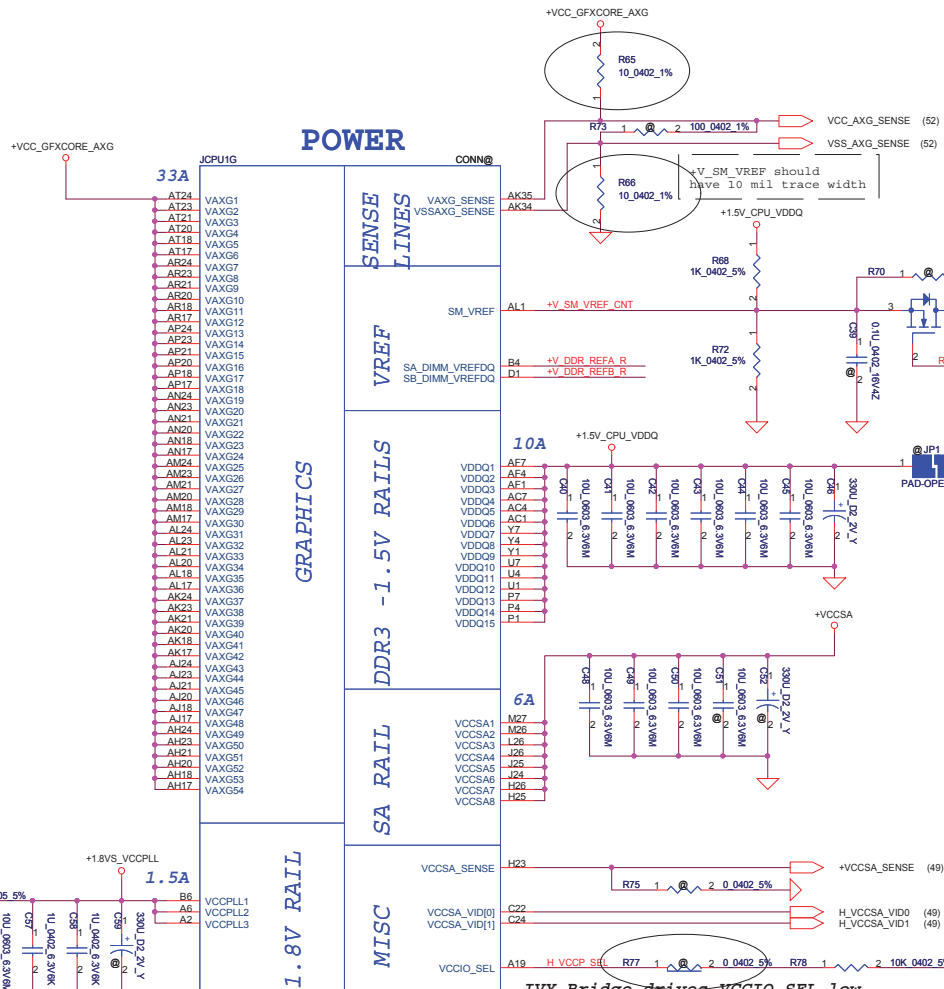
PEG DEFER TRAINING	
CFG7	<ul style="list-style-type: none"> <li>1: (Default) PEG Train immediately following xxRESETB de assertion</li> <li>0: PEG Wait for BIOS for training</li> </ul>



TYCO\_2013620-2\_IVY BRIDGE

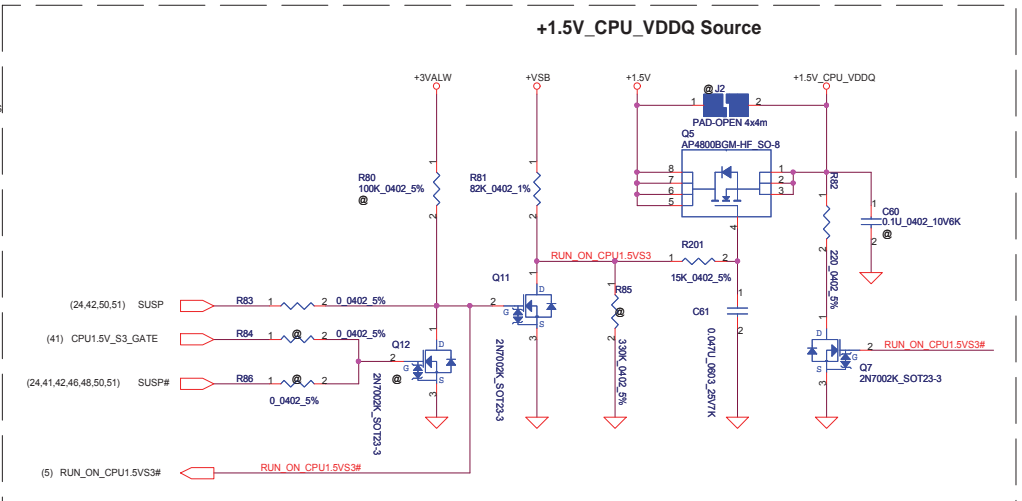
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IVY Bridge drives VCCIO\_SEL low  
VCCP\_PWRCTRL:0

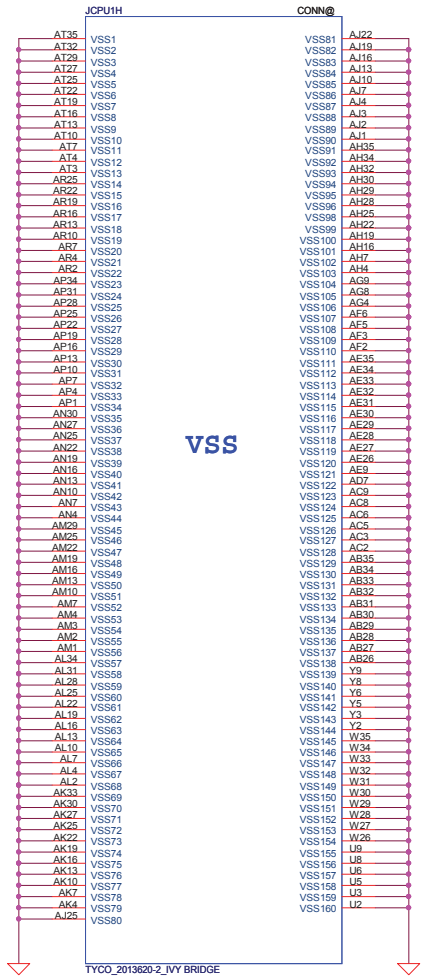
Sandy Bridge is NC for A19  
VCCP\_PWRCTRL:1



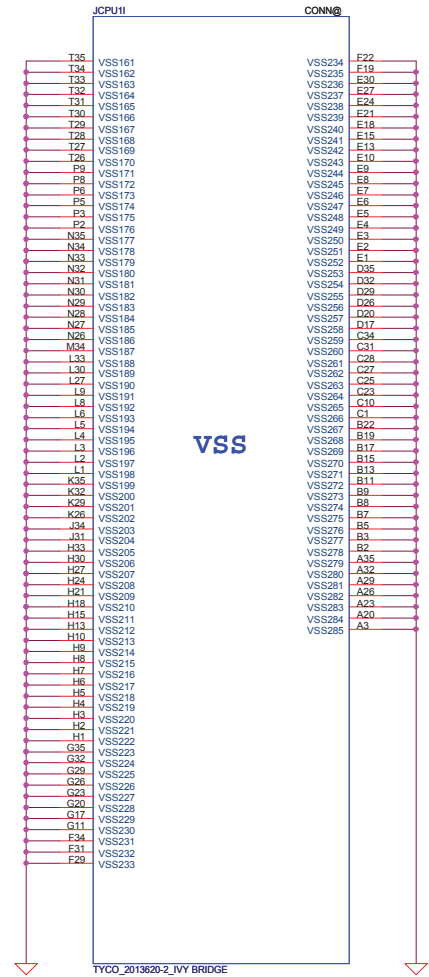
**Vaxg**

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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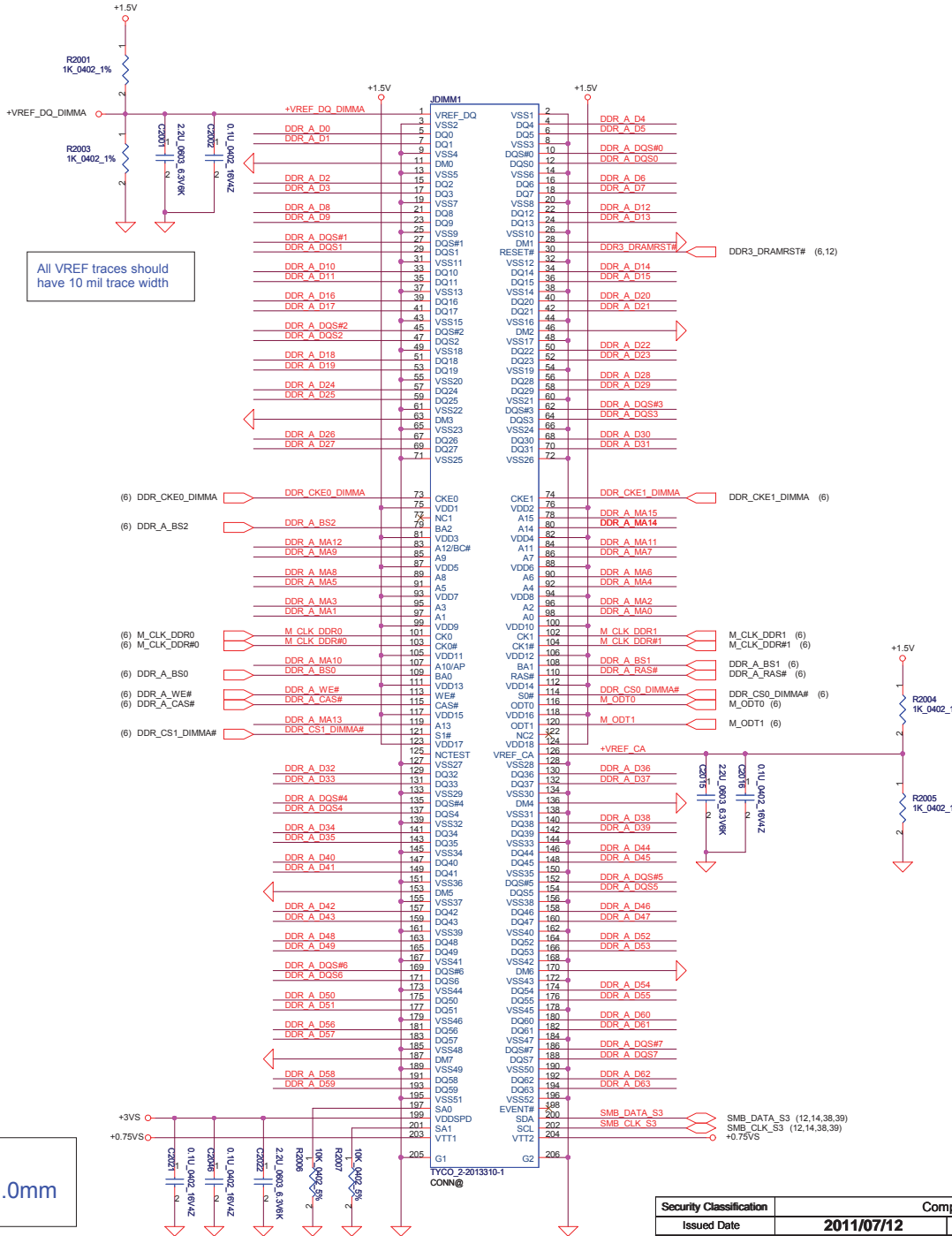


TYCO\_2013620-2\_IVY BRIDGE



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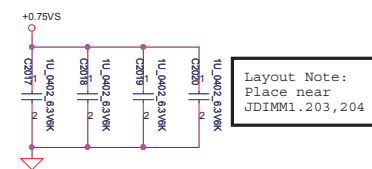
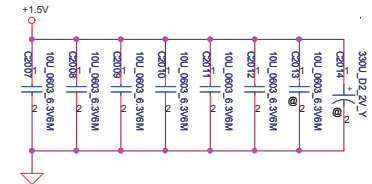
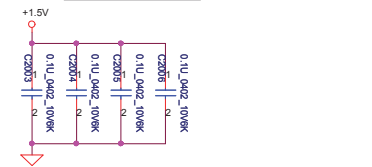


All VREF traces should have 10 mil trace width

<Address: 00>  
DIMM\_A Reserve H:4.0mm

- DDR\_A\_DQS#(0..7) (6)
- DDR\_A\_DQS(0..7) (6)
- DDR\_A\_DQ(0..63) (6)
- DDR\_MA(0..15) (6)

Layout Note:  
Place near  
JDIMM1

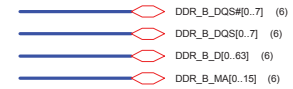
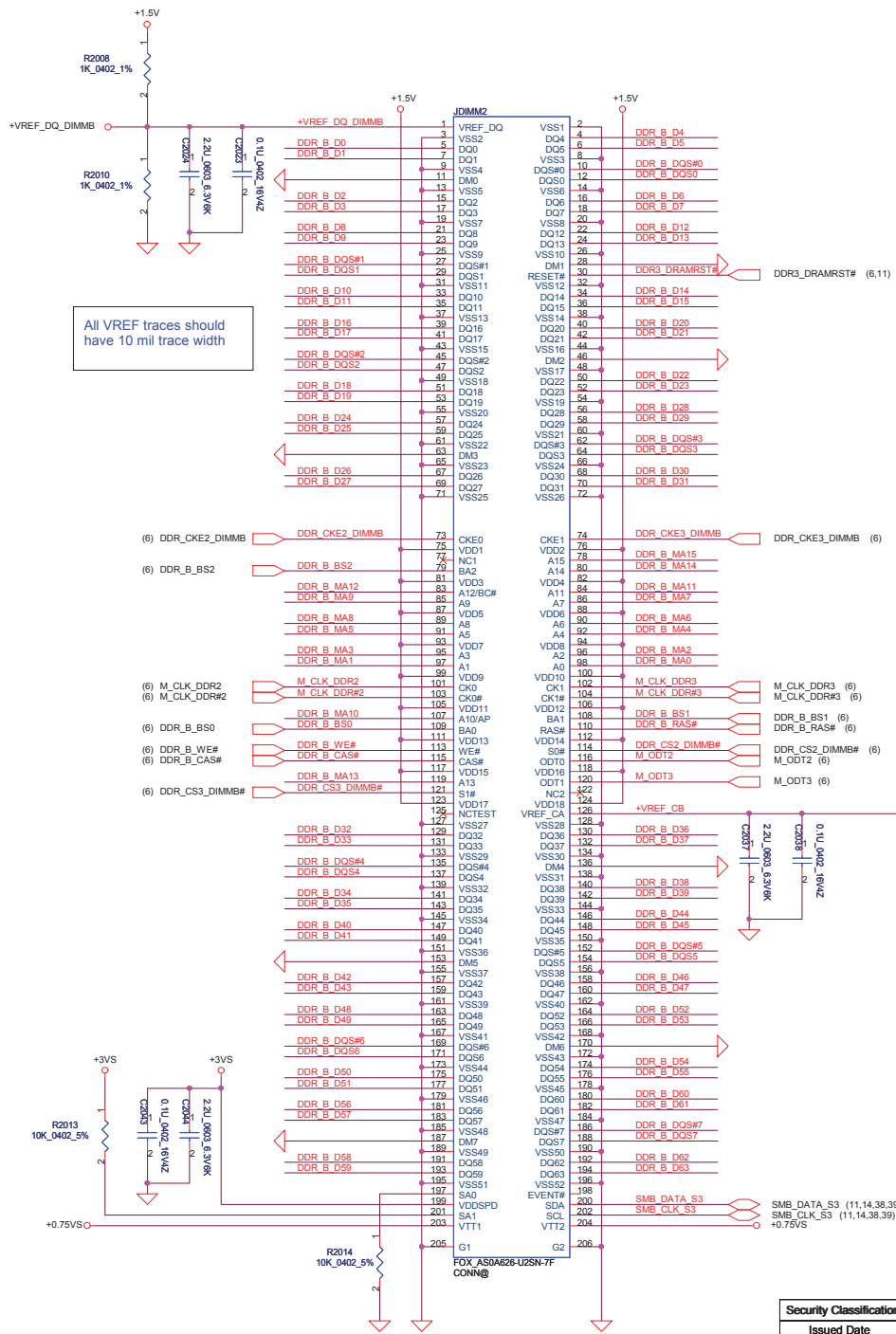


Layout Note:  
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JDIMM1. 203, 204

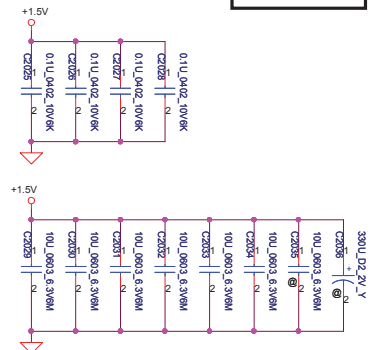
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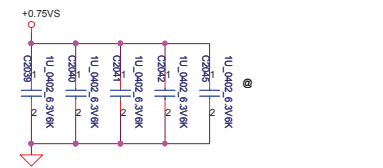
LA-8131P



Layout Note:  
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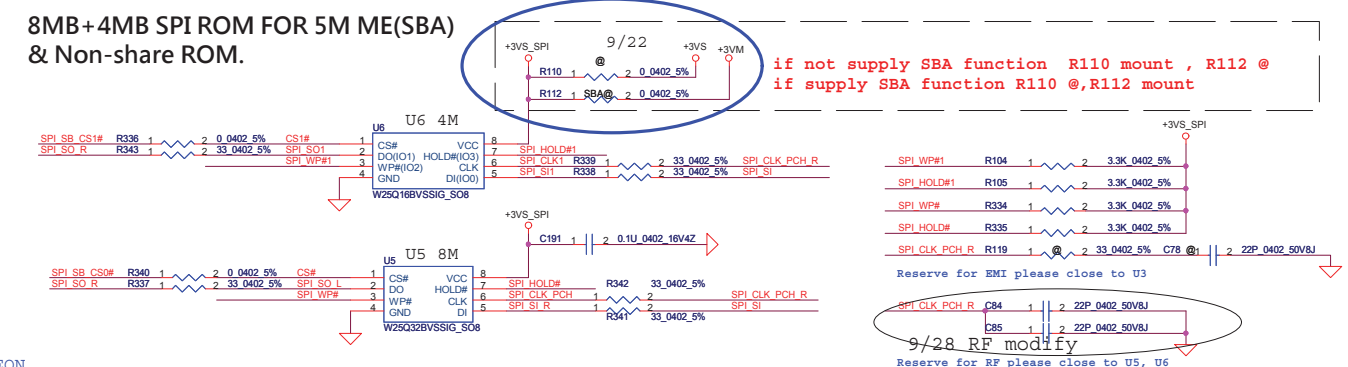
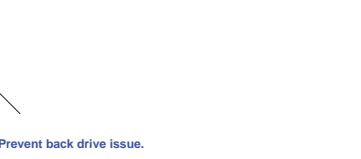
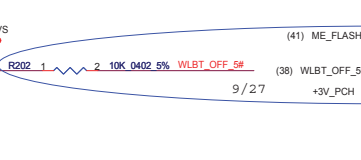
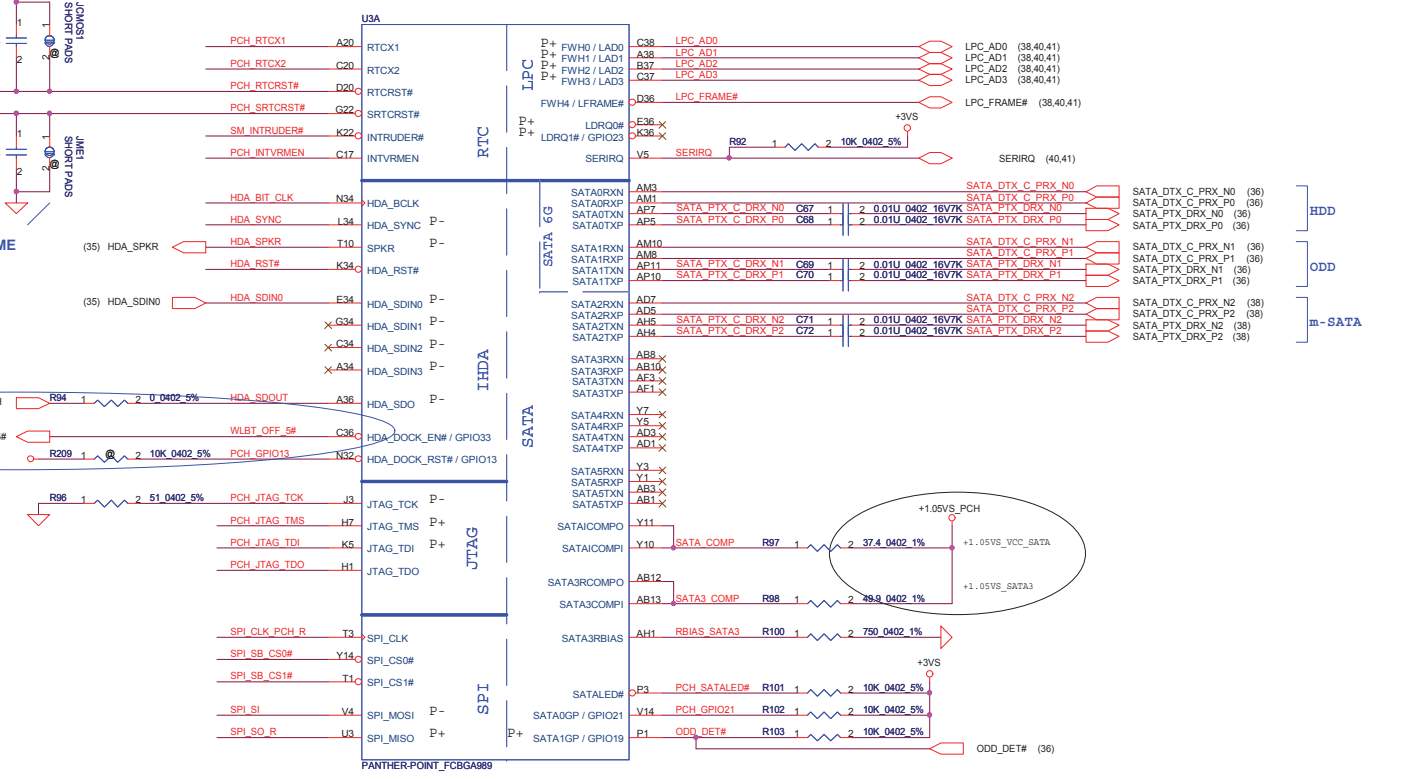
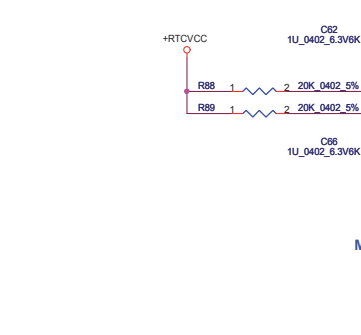
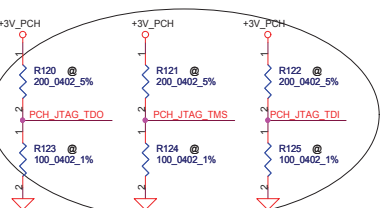
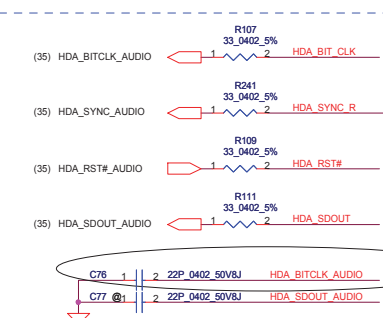
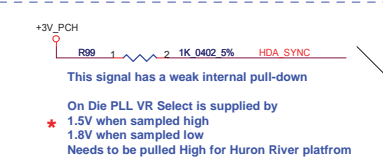
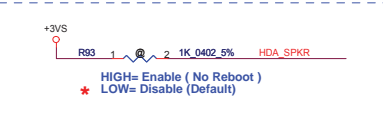
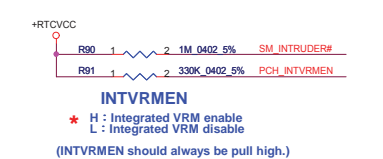
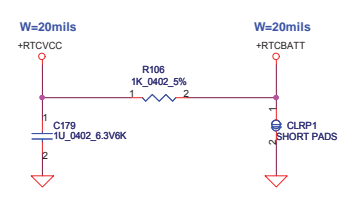
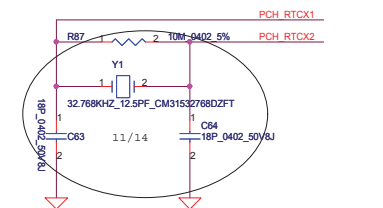
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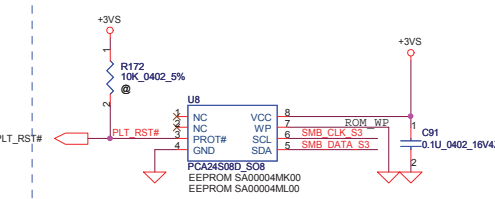
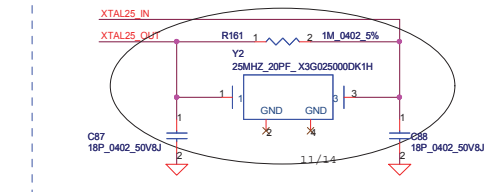
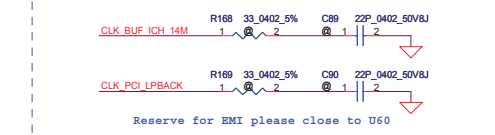
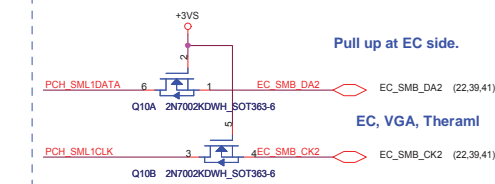
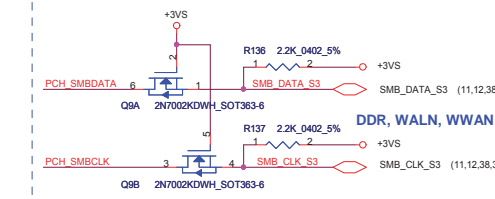
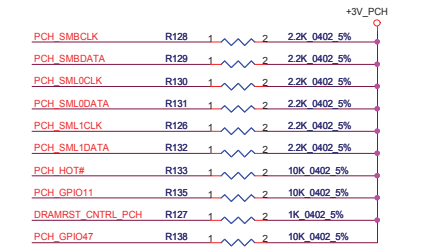
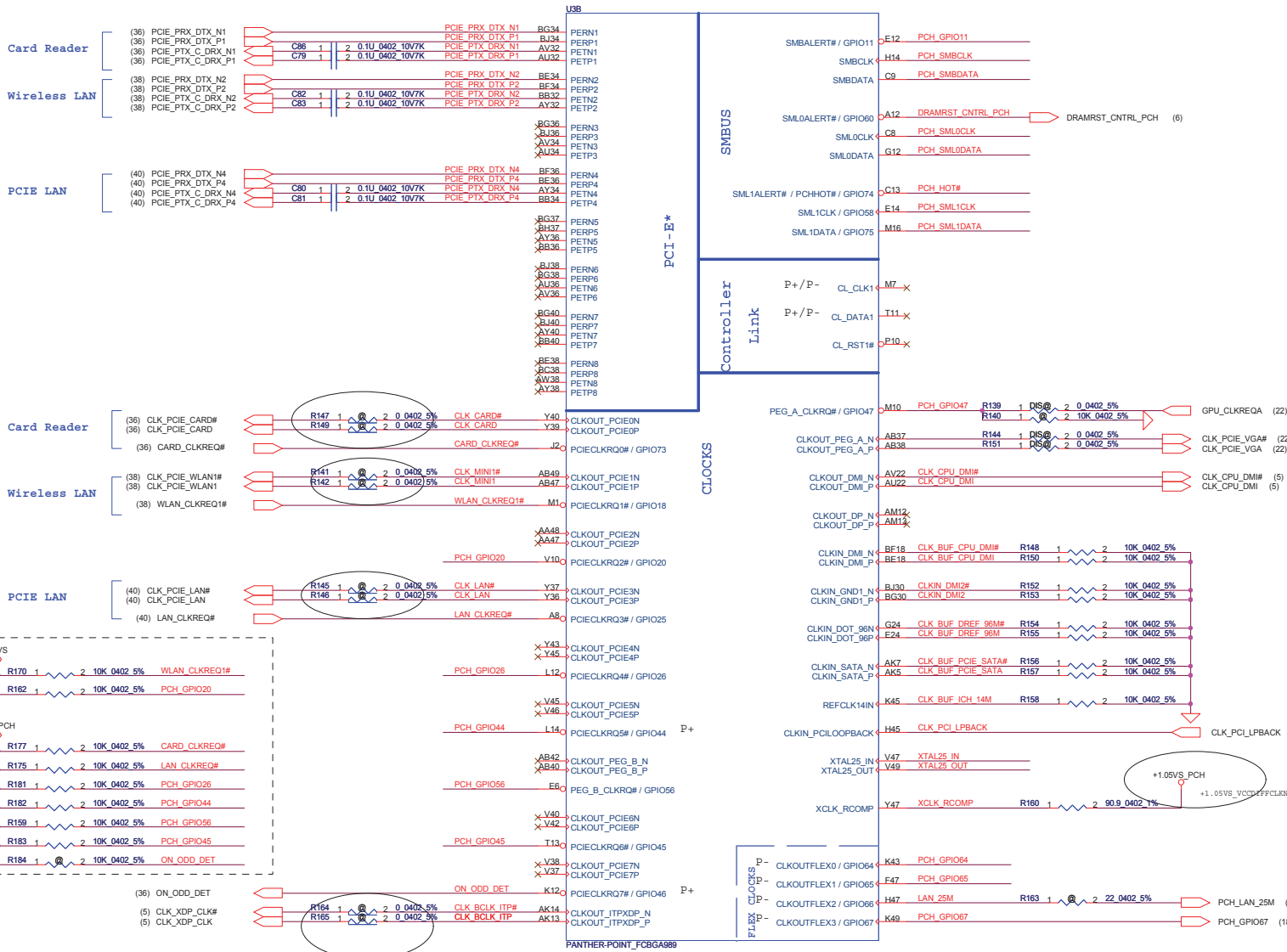
Compal Electronics, Inc.

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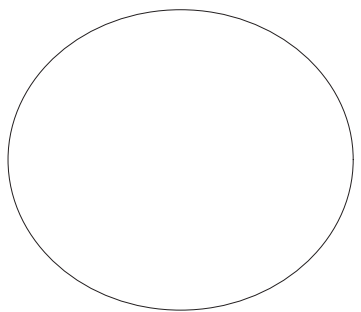
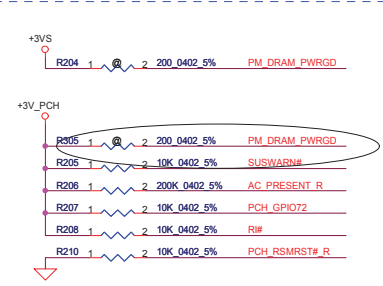
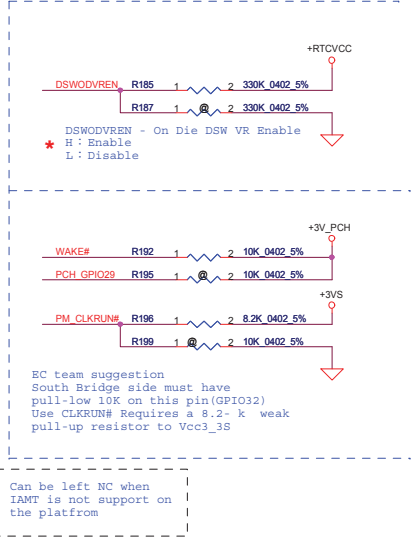
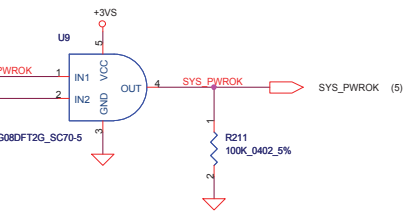
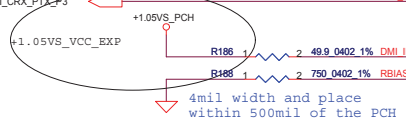
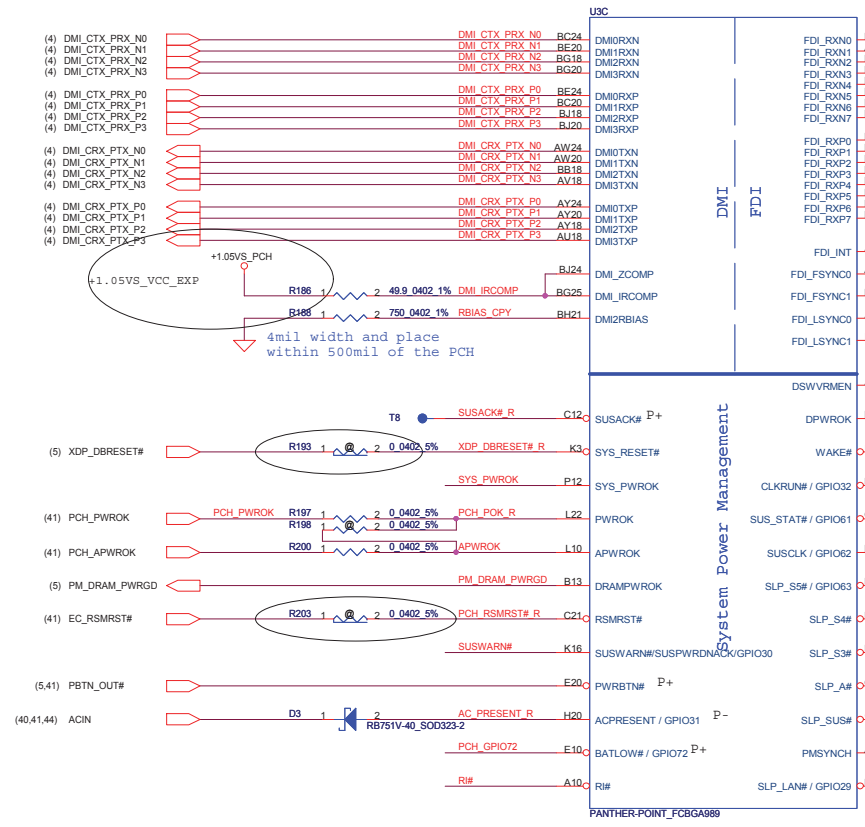


EON  
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 4M:SA00004LI00 S IC FL 32M EN25Q32B-104HIP SOP 8P

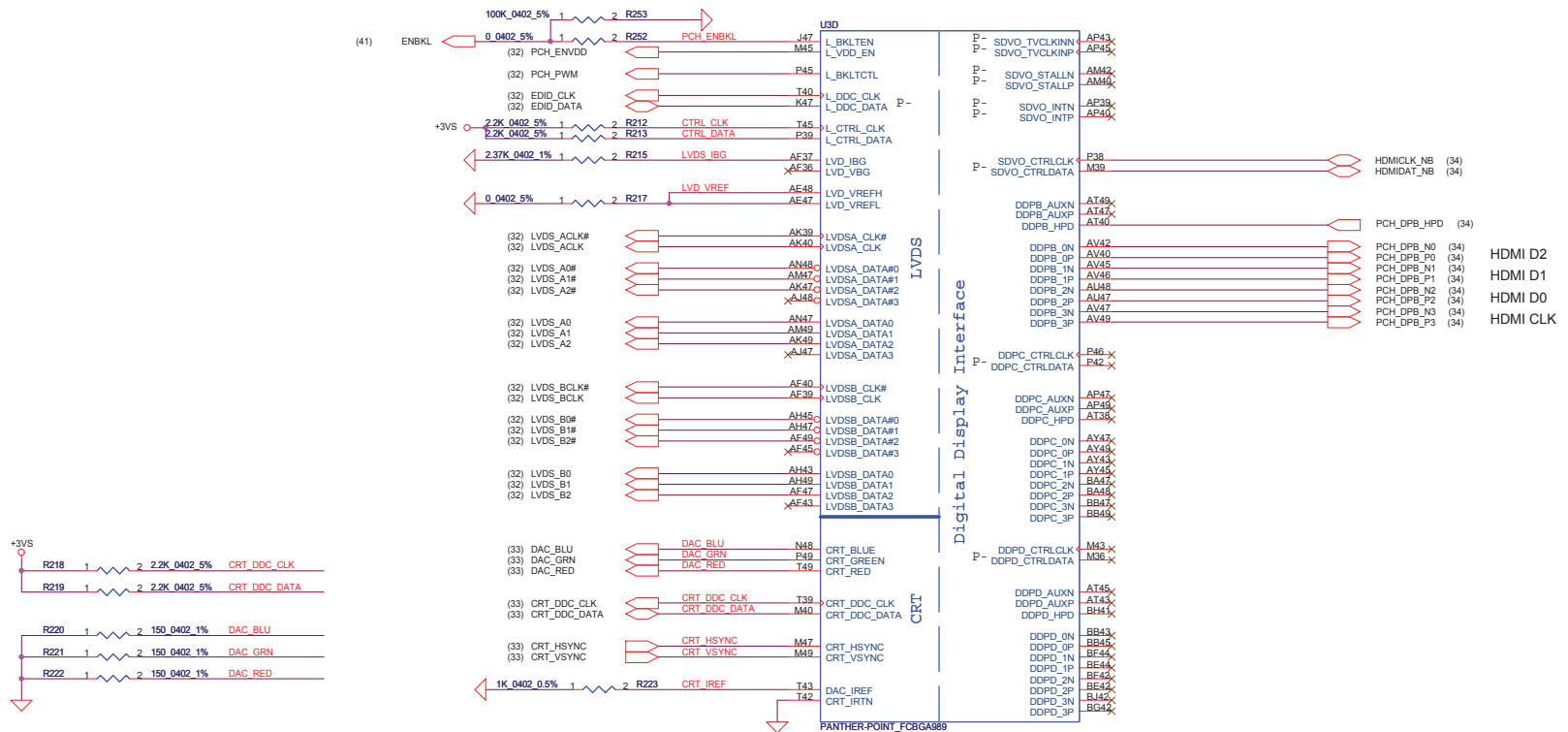
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Issued Date	<b>2011/07/12</b>	Deciphered Date	<b>2012/07/01</b>	Title	<b>PCH (1/9) SATA,HDA,SPI, LPC</b>
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<b>Issued Date</b>	2011/07/12	<b>Deciphered Date</b>	2012/07/01	<b>Title</b>
				<b>PCH (2/8) PCIE, SMBUS, CLK</b>
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<b>Date</b>	Friday, January 08, 2012	<b>Sheet</b>	14	<b>of</b> 58

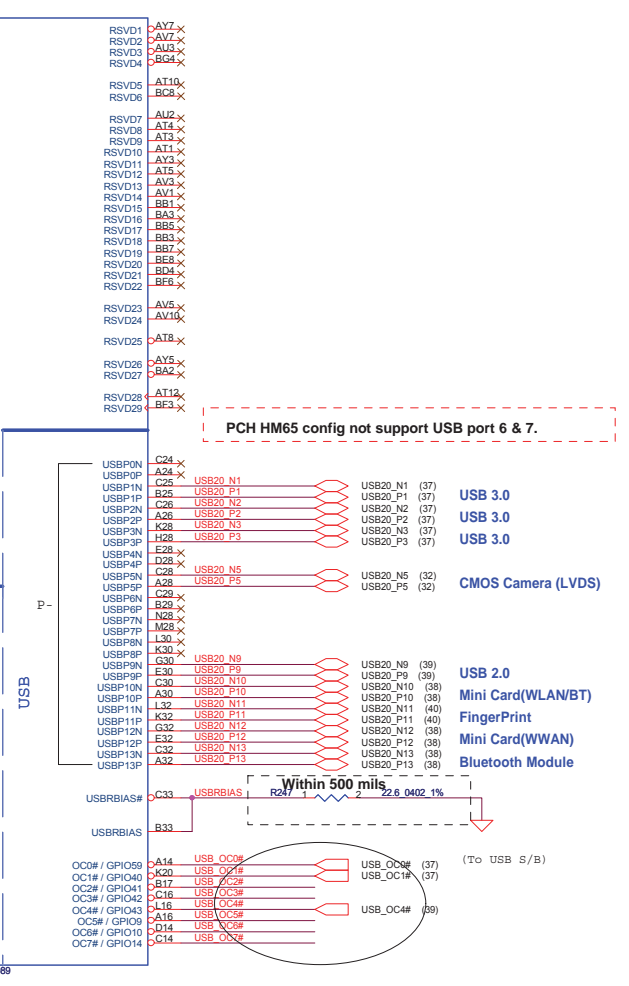
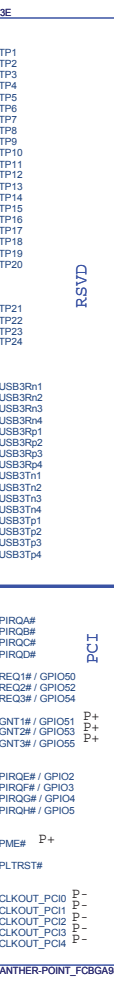
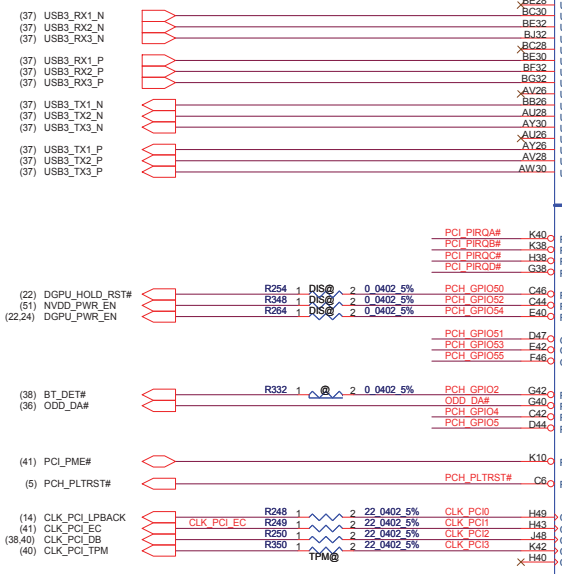
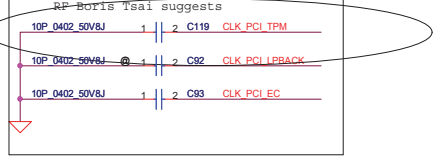
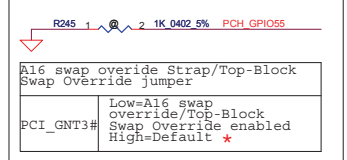
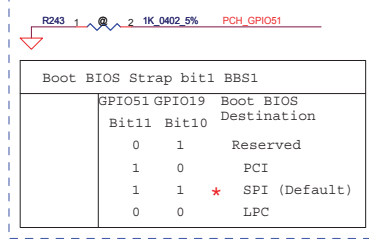
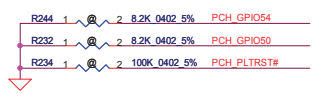
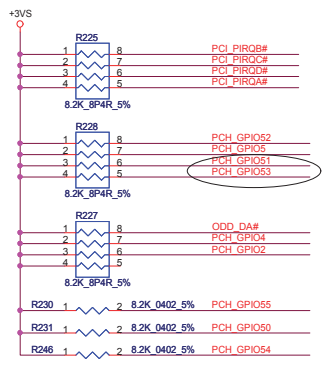


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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PCH (4/9) LVDS,CRT,DP,HDMI
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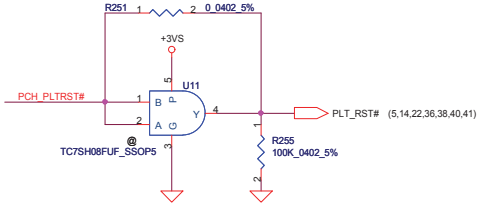




PCH HM65 config not support USB port 6 & 7.

Within 500 mils

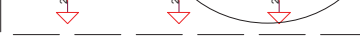
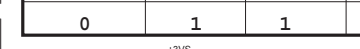
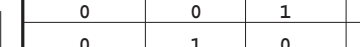
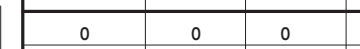
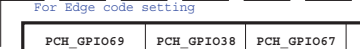
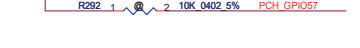
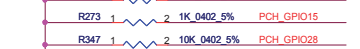
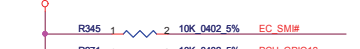
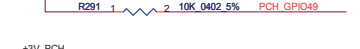
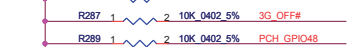
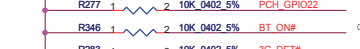
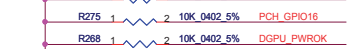
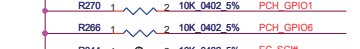
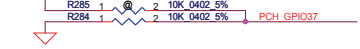
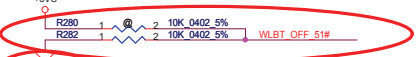
OC[0..3] use for EHCT1  
OC[4..7] use for EHCT2



**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
\* H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable

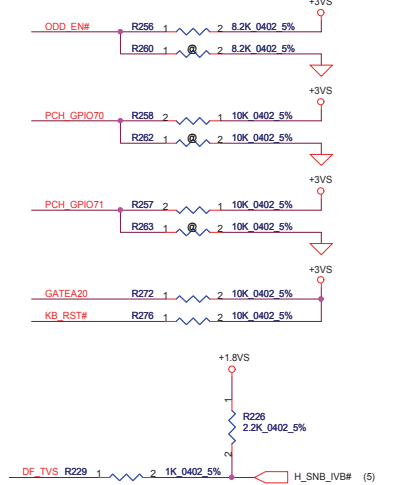
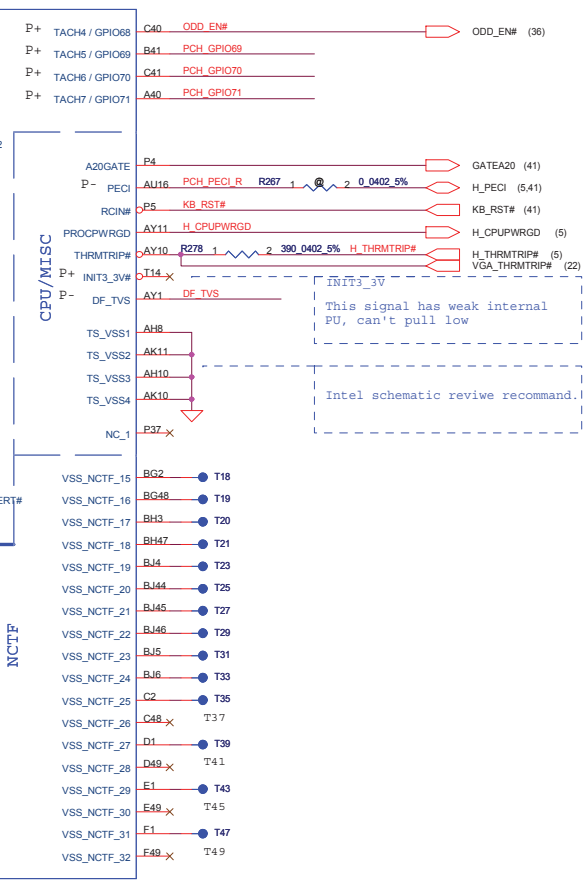
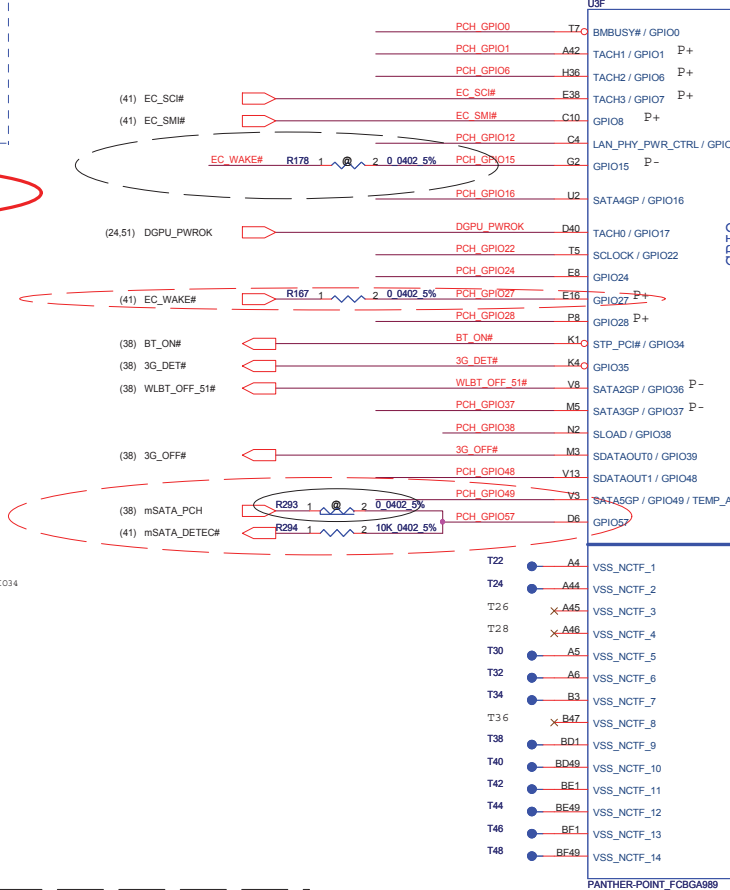
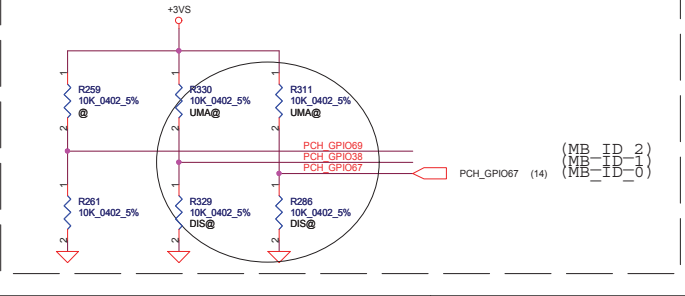


**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
\* H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable



For Edge code setting

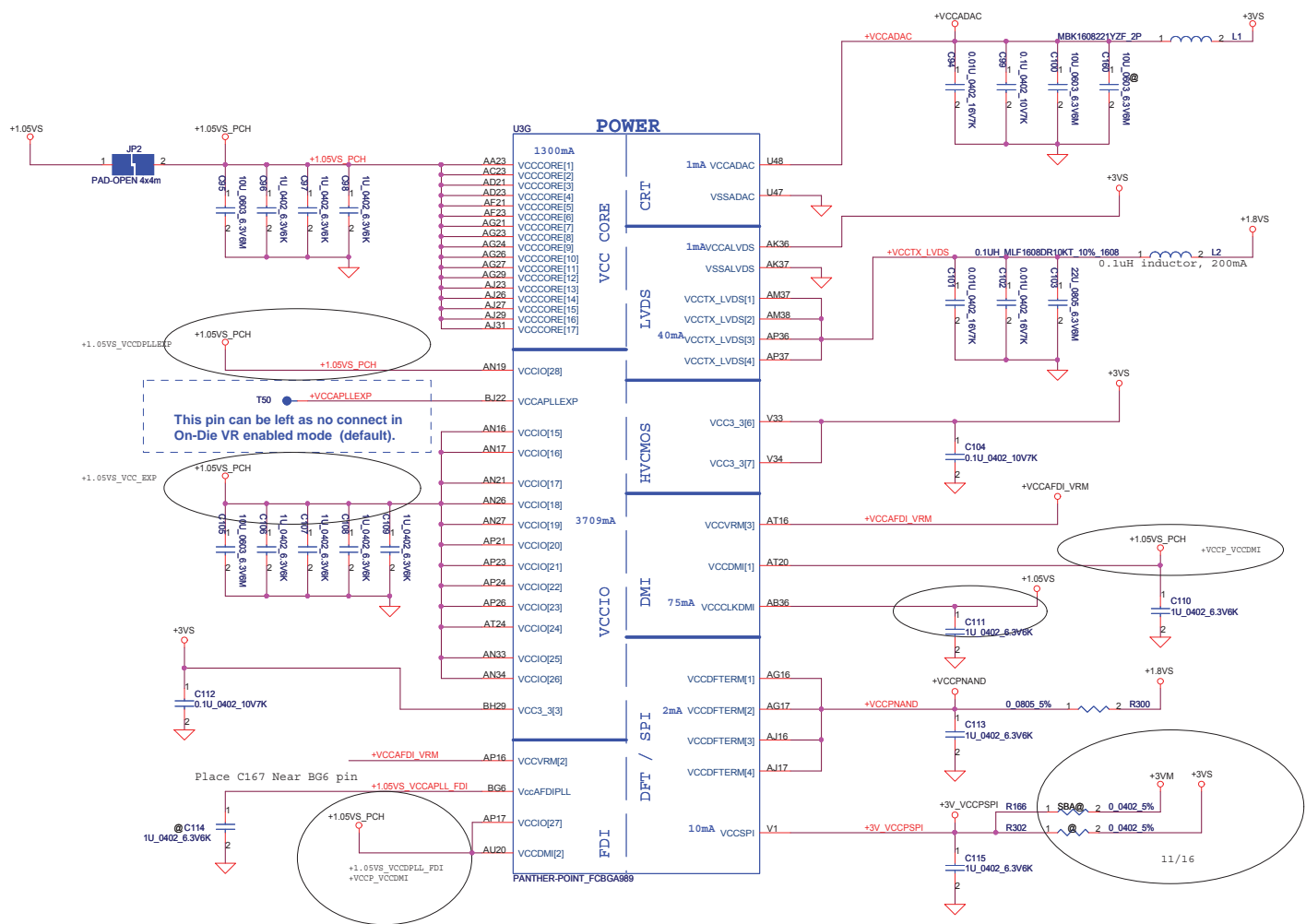
PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA



DMI Termination Voltage

INV_CLB	Set to Vcc when HIGH
	Set to Vss when LOW

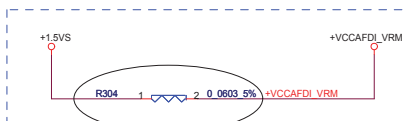
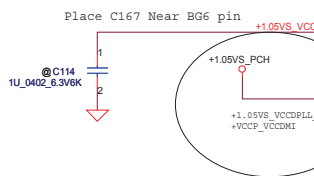
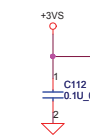
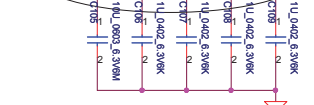
CLOSE TO THE BRANCHING POINT



+1.05VS\_VCCDFLLEXP

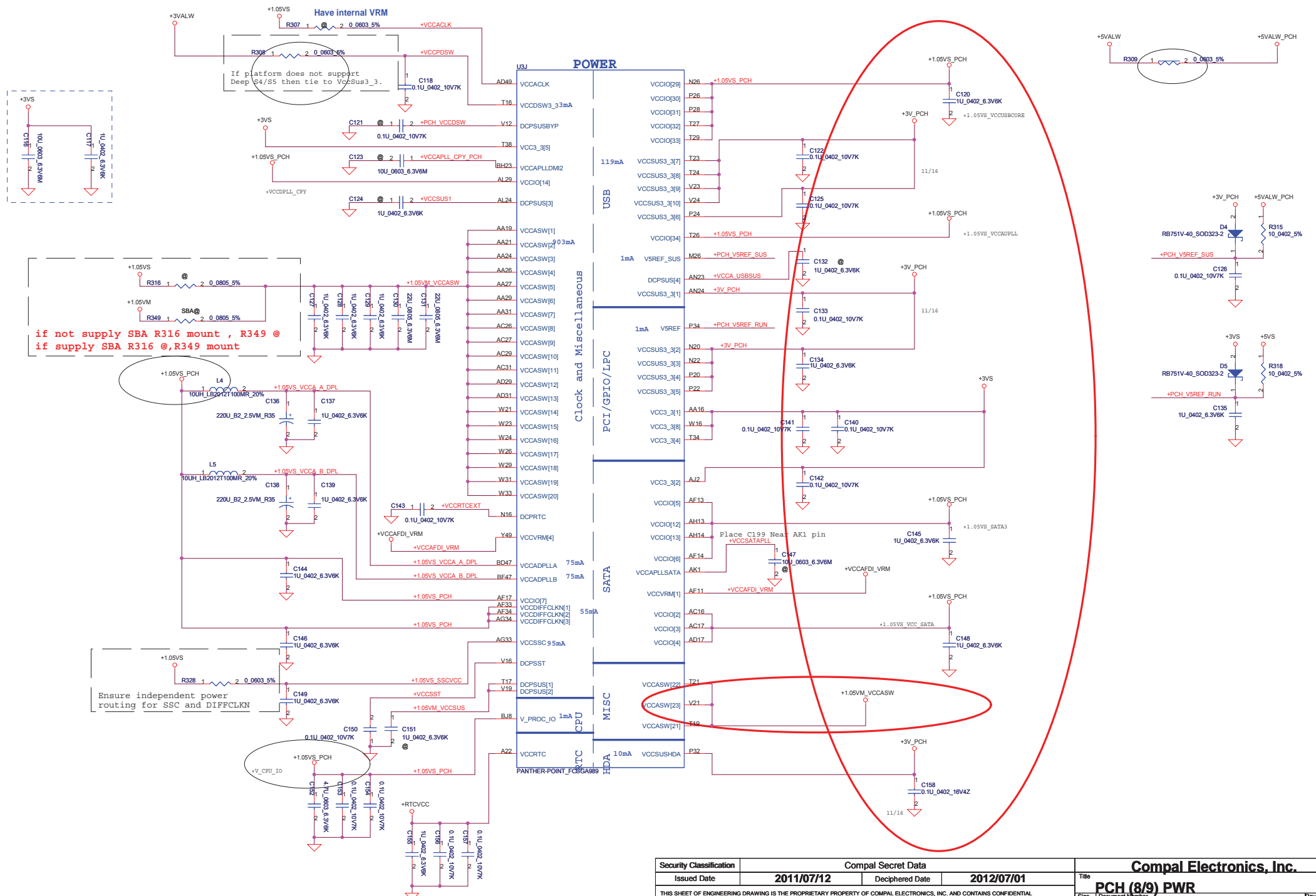
T50  
 This pin can be left as no connect in On-Die VR enabled mode (default).

+1.05VS\_VCC\_EXP



VCCVRM==>1.5V FOR MOBILE  
 VCCVRM==>1.8V FOR DESKTOP  
 VCCVRM = 160mA detail waiting for newest spec

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				Custom	LA-8131P
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				Date	Friday, January 08, 2012
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U9H		U9I	
H5	VSS[0]	AK38	VSS[80]
AA17	VSS[11]	AK4	VSS[81]
AA2	VSS[2]	AK42	VSS[82]
AA3	VSS[3]	AK6	VSS[83]
AA34	VSS[4]	AL16	VSS[84]
AB11	VSS[5]	AL17	VSS[85]
AB14	VSS[6]	AL19	VSS[86]
AB39	VSS[7]	AL2	VSS[87]
AB4	VSS[8]	AL21	VSS[88]
AB43	VSS[9]	AL23	VSS[89]
AB5	VSS[10]	AL26	VSS[90]
AB7	VSS[11]	AM11	VSS[91]
AC19	VSS[13]	AL27	VSS[92]
AC2	VSS[14]	AL31	VSS[93]
AC21	VSS[15]	AL33	VSS[94]
AC24	VSS[16]	AL34	VSS[95]
AC33	VSS[17]	AL48	VSS[96]
AC34	VSS[18]	AM14	VSS[97]
AC48	VSS[19]	AM36	VSS[98]
AD10	VSS[20]	AM39	VSS[99]
AD11	VSS[21]	AM43	VSS[100]
AD12	VSS[22]	AM45	VSS[101]
AD13	VSS[23]	AM6	VSS[102]
AD19	VSS[24]	AM7	VSS[103]
AD24	VSS[25]	AN2	VSS[104]
AD26	VSS[26]	AN29	VSS[105]
AD27	VSS[27]	AN3	VSS[106]
AD33	VSS[28]	AN31	VSS[107]
AD34	VSS[29]	AN32	VSS[108]
AD36	VSS[30]	AP12	VSS[109]
AD37	VSS[31]	AP19	VSS[110]
AD38	VSS[32]	AP28	VSS[111]
AD39	VSS[33]	AP30	VSS[112]
AD4	VSS[34]	AP32	VSS[113]
AD40	VSS[35]	AP38	VSS[114]
AD42	VSS[36]	AP4	VSS[115]
AD43	VSS[37]	AP42	VSS[116]
AD45	VSS[38]	AP46	VSS[117]
AD46	VSS[39]	AP8	VSS[118]
AD8	VSS[40]	AR2	VSS[119]
AE2	VSS[41]	AR48	VSS[120]
AE3	VSS[42]	AT11	VSS[121]
AE10	VSS[43]	AT13	VSS[122]
AE12	VSS[44]	AT18	VSS[123]
AE14	VSS[45]	AT22	VSS[124]
AE16	VSS[46]	AT26	VSS[125]
AE19	VSS[47]	AT28	VSS[126]
AE24	VSS[48]	AT30	VSS[127]
AE29	VSS[49]	AT32	VSS[128]
AE26	VSS[50]	AT34	VSS[129]
AE27	VSS[51]	AT39	VSS[130]
AE29	VSS[52]	AT42	VSS[131]
AE31	VSS[53]	AT46	VSS[132]
AE38	VSS[54]	ATT	VSS[133]
AE4	VSS[55]	AU24	VSS[134]
AE42	VSS[56]	AU30	VSS[135]
AE46	VSS[57]	AV16	VSS[136]
AE5	VSS[58]	AV20	VSS[137]
AE7	VSS[59]	AV24	VSS[138]
AE8	VSS[60]	AV30	VSS[139]
AG19	VSS[61]	AV4	VSS[140]
AG2	VSS[62]	AV4	VSS[141]
AG31	VSS[63]	AV43	VSS[142]
AG48	VSS[64]	AW	VSS[143]
AH11	VSS[65]	AW14	VSS[144]
AH3	VSS[66]	AW18	VSS[145]
AH36	VSS[67]	AW2	VSS[146]
AH39	VSS[68]	AW22	VSS[147]
AH40	VSS[69]	AW26	VSS[148]
AH42	VSS[70]	AW28	VSS[149]
AH46	VSS[71]	AW32	VSS[150]
AH7	VSS[72]	AW34	VSS[151]
AJ19	VSS[73]	AW36	VSS[152]
AJ21	VSS[74]	AW40	VSS[153]
AJ24	VSS[75]	AW48	VSS[154]
AJ33	VSS[76]	AV11	VSS[155]
AJ34	VSS[77]	AY12	VSS[156]
AK12	VSS[78]	AY22	VSS[157]
AK3	VSS[79]	AY28	VSS[158]

PANTHER-POINT\_FCBGA989

U9H		U9I	
AY4	VSS[159]	VSS[259]	H46
AY42	VSS[160]	K18	VSS[260]
AY46	VSS[161]	K26	VSS[261]
AY8	VSS[162]	K39	VSS[262]
B11	VSS[163]	K46	VSS[263]
B15	VSS[164]	L18	VSS[264]
B19	VSS[165]	L20	VSS[265]
B23	VSS[166]	L26	VSS[266]
B27	VSS[167]	L28	VSS[267]
B30	VSS[168]	L36	VSS[268]
B35	VSS[169]	L45	VSS[269]
B7	VSS[170]	M12	VSS[270]
F45	VSS[171]	F16	VSS[271]
BB12	VSS[172]	M18	VSS[272]
BB16	VSS[173]	M22	VSS[273]
BB20	VSS[174]	M24	VSS[274]
BB22	VSS[175]	M30	VSS[275]
BB28	VSS[176]	M32	VSS[276]
BB30	VSS[177]	M34	VSS[277]
BB38	VSS[178]	M38	VSS[278]
BB4	VSS[179]	M4	VSS[279]
BB46	VSS[180]	M42	VSS[280]
BC14	VSS[181]	M46	VSS[281]
BC18	VSS[182]	M8	VSS[282]
BC2	VSS[183]	N18	VSS[283]
BC26	VSS[184]	P30	VSS[284]
BC28	VSS[185]	P47	VSS[285]
BC32	VSS[186]	P11	VSS[286]
BC34	VSS[187]	P18	VSS[287]
BC36	VSS[188]	P32	VSS[288]
BC40	VSS[189]	P40	VSS[289]
BC42	VSS[190]	P43	VSS[290]
BC48	VSS[191]	P7	VSS[291]
BD5	VSS[192]	R2	VSS[292]
BE22	VSS[193]	R48	VSS[293]
BE40	VSS[194]	T12	VSS[294]
BE42	VSS[195]	T31	VSS[295]
BE44	VSS[196]	T37	VSS[296]
BE10	VSS[197]	T4	VSS[297]
BE12	VSS[198]	W34	VSS[298]
BE20	VSS[199]	T46	VSS[299]
BE22	VSS[200]	T8	VSS[300]
BE24	VSS[201]	V11	VSS[301]
BE26	VSS[202]	V17	VSS[302]
BE28	VSS[203]	V28	VSS[303]
BE30	VSS[204]	V27	VSS[304]
BE32	VSS[205]	V29	VSS[305]
BE34	VSS[206]	V31	VSS[306]
BE36	VSS[207]	V39	VSS[307]
BE38	VSS[208]	V43	VSS[308]
BE40	VSS[209]	V7	VSS[309]
BE42	VSS[210]	W17	VSS[310]
BE44	VSS[211]	W19	VSS[311]
BG17	VSS[212]	W27	VSS[312]
BG21	VSS[213]	W48	VSS[313]
BG33	VSS[214]	X12	VSS[314]
BG44	VSS[215]	X38	VSS[315]
BG8	VSS[216]	Y4	VSS[316]
BH11	VSS[217]	Y42	VSS[317]
BH15	VSS[218]	Y46	VSS[318]
BH17	VSS[219]	Y8	VSS[319]
BH19	VSS[220]	BC29	VSS[320]
BH27	VSS[221]	N24	VSS[321]
BH31	VSS[222]	AJ3	VSS[322]
BH33	VSS[223]	AD47	VSS[323]
BH35	VSS[224]	B43	VSS[324]
BH39	VSS[225]	BE10	VSS[325]
BH43	VSS[226]	BG41	VSS[326]
BH7	VSS[227]	G14	VSS[327]
D3	VSS[228]	H16	VSS[328]
D12	VSS[229]	I36	VSS[329]
D16	VSS[230]	BC22	VSS[330]
D18	VSS[231]	C22	VSS[331]
D22	VSS[232]	AP13	VSS[332]
D26	VSS[233]	M14	VSS[333]
D28	VSS[234]	AP3	VSS[334]
D30	VSS[235]	AP1	VSS[335]
D32	VSS[236]	BE16	VSS[336]
D34	VSS[237]	BC16	VSS[337]
D38	VSS[238]	BG28	VSS[338]
D42	VSS[239]	BJ28	VSS[339]
D48	VSS[240]		
E18	VSS[241]		
E26	VSS[242]		
E28	VSS[243]		
E38	VSS[244]		
G18	VSS[245]		
G20	VSS[246]		
G26	VSS[247]		
G28	VSS[248]		
G48	VSS[249]		
H12	VSS[250]		
H18	VSS[251]		
H22	VSS[252]		
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

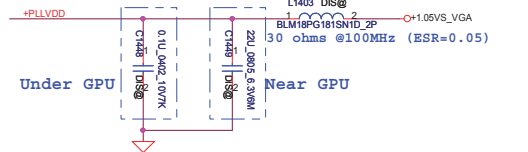
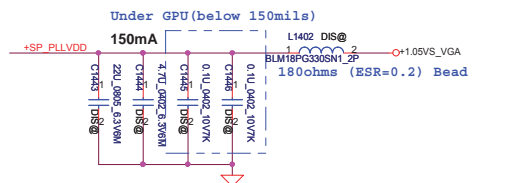
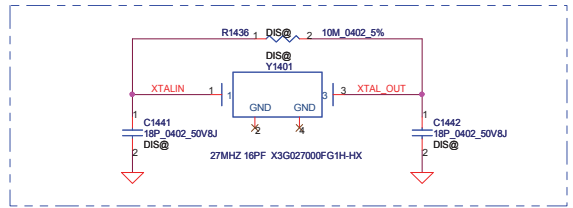
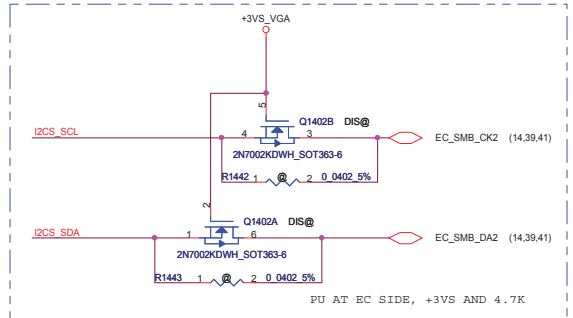
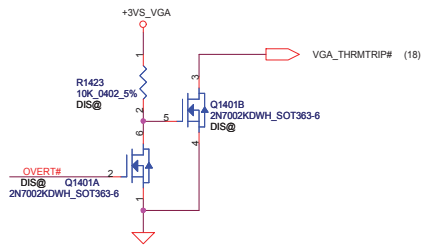
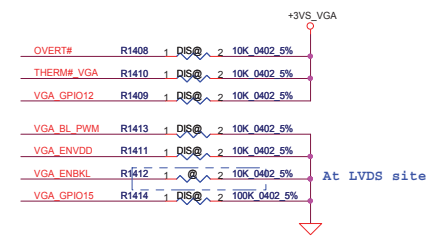
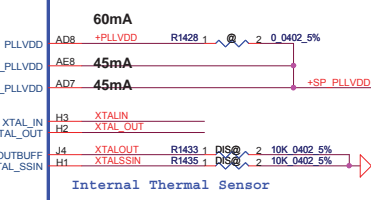
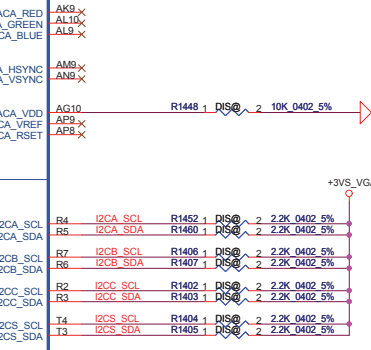
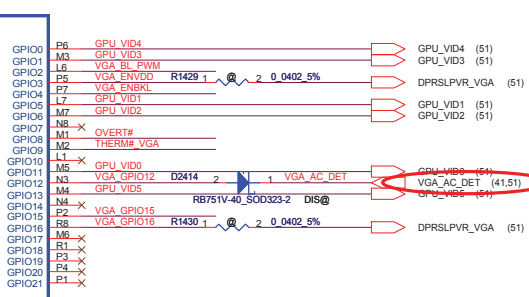
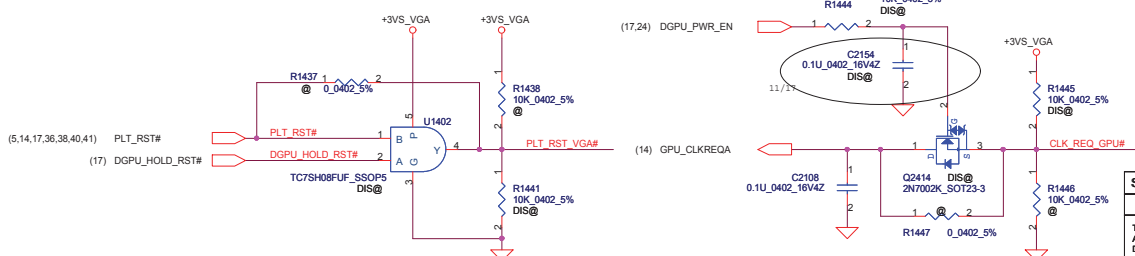
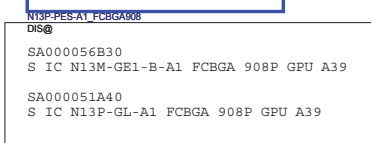
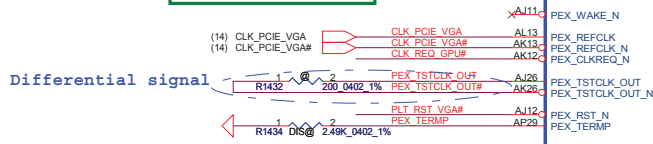
PANTHER-POINT\_FCBGA989

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Size	Custom	Document Number	LA-8131P	Rev	0.6
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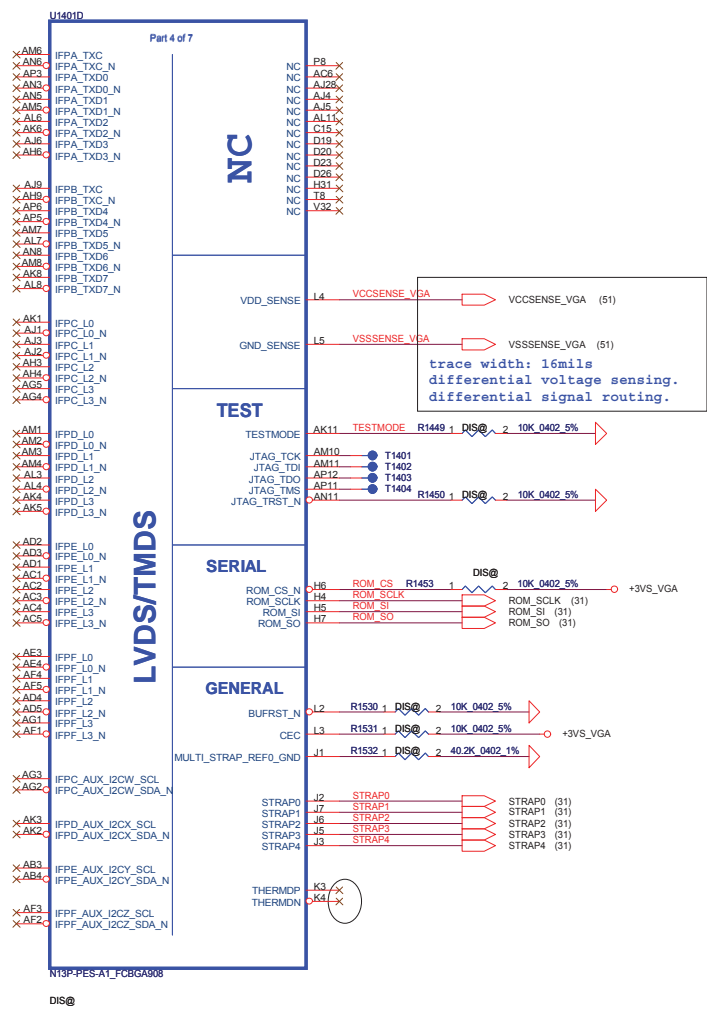
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- (4) PCIE\_CTX\_GRX\_P0..15] PCIE\_CTX\_GRX\_P0..15]
- (4) PCIE\_CRX\_GTX\_N0..15] PCIE\_CRX\_GTX\_N0..15]
- (4) PCIE\_CRX\_GTX\_P0..15] PCIE\_CRX\_GTX\_P0..15]

PCIE_CTX_GRX_N0..15]		PCIE_CTX_GRX_P0..15]		PCIE_CRX_GTX_N0..15]		PCIE_CRX_GTX_P0..15]	
PCIE_CTX_GRX_N0	AN12	PEX_RX0	AK14	PCIE_CRX_GTX_N0	AK14	PEX_TX0	AK14
PCIE_CTX_GRX_N1	AN12	PEX_RX0_N	AK14	PCIE_CRX_GTX_P0	AK14	PEX_TX0_N	AK14
PCIE_CTX_GRX_N2	AN14	PEX_RX1	AK16	PCIE_CRX_GTX_N1	AK16	PEX_TX1	AK16
PCIE_CTX_GRX_N3	AN14	PEX_RX1_N	AK16	PCIE_CRX_GTX_P1	AK16	PEX_TX1_N	AK16
PCIE_CTX_GRX_N4	AN16	PEX_RX2	AK18	PCIE_CRX_GTX_N2	AK18	PEX_TX2	AK18
PCIE_CTX_GRX_N5	AN16	PEX_RX2_N	AK18	PCIE_CRX_GTX_P2	AK18	PEX_TX2_N	AK18
PCIE_CTX_GRX_N6	AN18	PEX_RX3	AK20	PCIE_CRX_GTX_N3	AK20	PEX_TX3	AK20
PCIE_CTX_GRX_N7	AN18	PEX_RX3_N	AK20	PCIE_CRX_GTX_P3	AK20	PEX_TX3_N	AK20
PCIE_CTX_GRX_N8	AN20	PEX_RX4	AK22	PCIE_CRX_GTX_N4	AK22	PEX_TX4	AK22
PCIE_CTX_GRX_N9	AN20	PEX_RX4_N	AK22	PCIE_CRX_GTX_P4	AK22	PEX_TX4_N	AK22
PCIE_CTX_GRX_N10	AN22	PEX_RX5	AK24	PCIE_CRX_GTX_N5	AK24	PEX_TX5	AK24
PCIE_CTX_GRX_N11	AN22	PEX_RX5_N	AK24	PCIE_CRX_GTX_P5	AK24	PEX_TX5_N	AK24
PCIE_CTX_GRX_N12	AN24	PEX_RX6	AK26	PCIE_CRX_GTX_N6	AK26	PEX_TX6	AK26
PCIE_CTX_GRX_N13	AN24	PEX_RX6_N	AK26	PCIE_CRX_GTX_P6	AK26	PEX_TX6_N	AK26
PCIE_CTX_GRX_N14	AN26	PEX_RX7	AK28	PCIE_CRX_GTX_N7	AK28	PEX_TX7	AK28
PCIE_CTX_GRX_N15	AN26	PEX_RX7_N	AK28	PCIE_CRX_GTX_P7	AK28	PEX_TX7_N	AK28

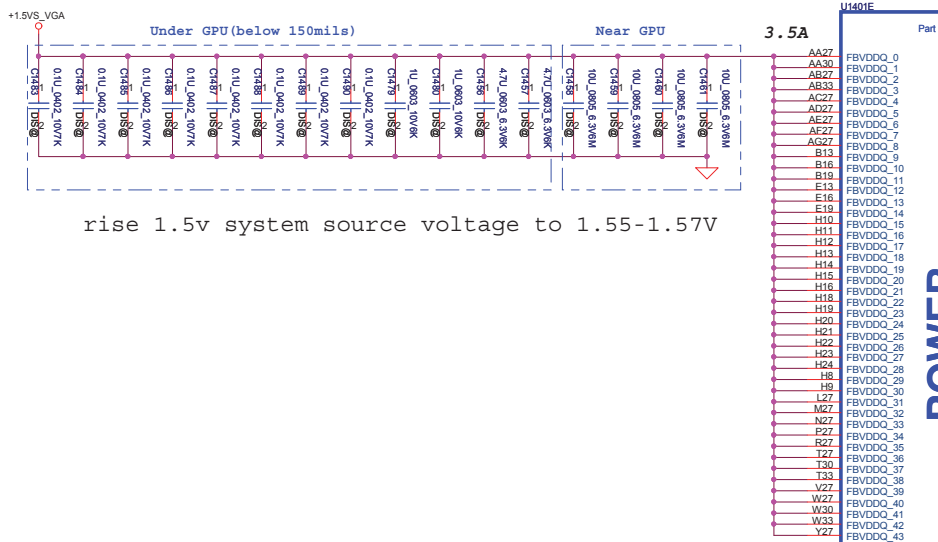
DIS@		DIS@	
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PCIE_CRX_GTX_P1	C1403	PCIE_CRX_C_GTX_P1	AK16
PCIE_CRX_GTX_N1	C1404	PCIE_CRX_C_GTX_N1	AK16
PCIE_CRX_GTX_P2	C1405	PCIE_CRX_C_GTX_P2	AK18
PCIE_CRX_GTX_N2	C1406	PCIE_CRX_C_GTX_N2	AK18
PCIE_CRX_GTX_P3	C1407	PCIE_CRX_C_GTX_P3	AK20
PCIE_CRX_GTX_N3	C1408	PCIE_CRX_C_GTX_N3	AK20
PCIE_CRX_GTX_P4	C1410	PCIE_CRX_C_GTX_P4	AK22
PCIE_CRX_GTX_N4	C1411	PCIE_CRX_C_GTX_N4	AK22
PCIE_CRX_GTX_P5	C1412	PCIE_CRX_C_GTX_P5	AK24
PCIE_CRX_GTX_N5	C1413	PCIE_CRX_C_GTX_N5	AK24
PCIE_CRX_GTX_P6	C1414	PCIE_CRX_C_GTX_P6	AK26
PCIE_CRX_GTX_N6	C1415	PCIE_CRX_C_GTX_N6	AK26
PCIE_CRX_GTX_P7	C1416	PCIE_CRX_C_GTX_P7	AK28
PCIE_CRX_GTX_N7	C1417	PCIE_CRX_C_GTX_N7	AK28
PCIE_CRX_GTX_P8	C1418	PCIE_CRX_C_GTX_P8	AK30
PCIE_CRX_GTX_N8	C1419	PCIE_CRX_C_GTX_N8	AK30
PCIE_CRX_GTX_P9	C1420	PCIE_CRX_C_GTX_P9	AK32
PCIE_CRX_GTX_N9	C1421	PCIE_CRX_C_GTX_N9	AK32
PCIE_CRX_GTX_P10	C1422	PCIE_CRX_C_GTX_P10	AK34
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PCIE_CRX_GTX_P11	C1424	PCIE_CRX_C_GTX_P11	AK36
PCIE_CRX_GTX_N11	C1425	PCIE_CRX_C_GTX_N11	AK36
PCIE_CRX_GTX_P12	C1426	PCIE_CRX_C_GTX_P12	AK38
PCIE_CRX_GTX_N12	C1427	PCIE_CRX_C_GTX_N12	AK38
PCIE_CRX_GTX_P13	C1428	PCIE_CRX_C_GTX_P13	AK40
PCIE_CRX_GTX_N13	C1429	PCIE_CRX_C_GTX_N13	AK40
PCIE_CRX_GTX_P14	C1430	PCIE_CRX_C_GTX_P14	AK42
PCIE_CRX_GTX_N14	C1431	PCIE_CRX_C_GTX_N14	AK42
PCIE_CRX_GTX_P15	C1432	PCIE_CRX_C_GTX_P15	AK44
PCIE_CRX_GTX_N15	C1433	PCIE_CRX_C_GTX_N15	AK44



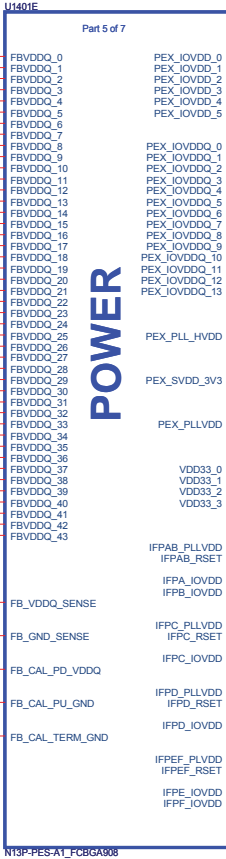
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N13X-PCIE/DAC/GPIO
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				Date	Friday, January 08, 2012
				Sheet	22 of 58



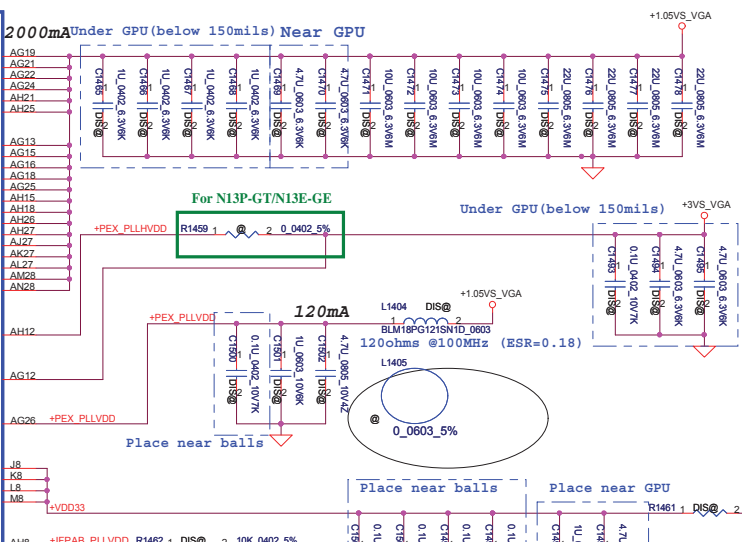
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title N13X-LVDS/HDM/DP/THM	
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rise 1.5v system source voltage to 1.55-1.57V



**POWER**



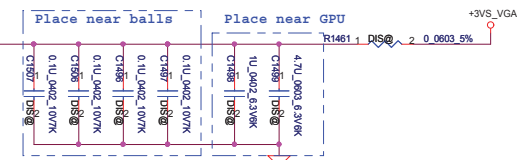
For N13P-GT/N13E-GE

120mA

Place near balls

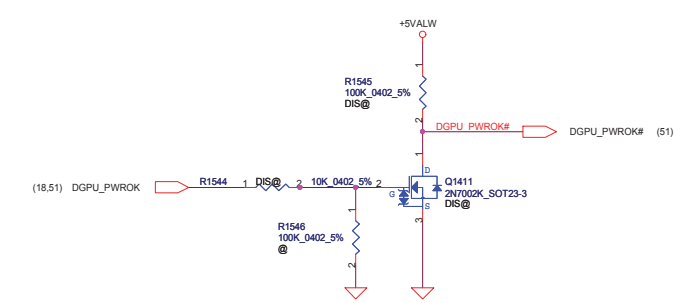
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

Place near balls

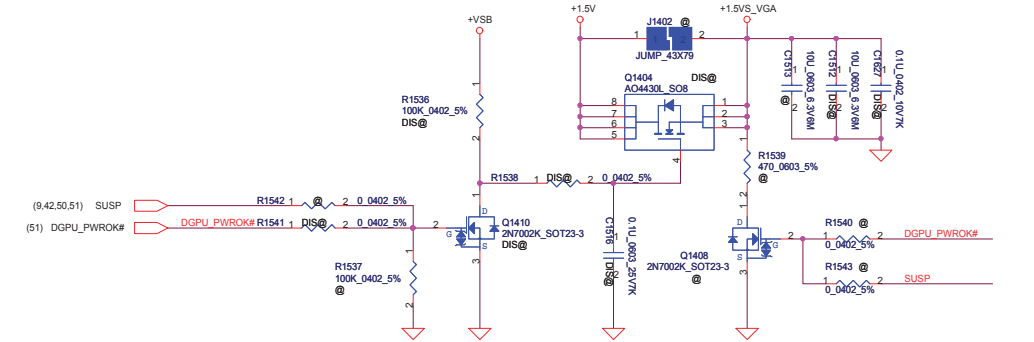


Place near balls

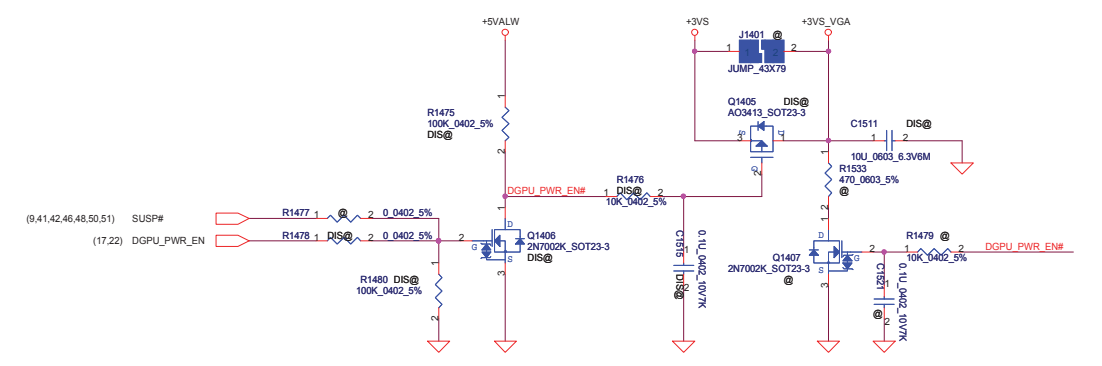
Place near GPU



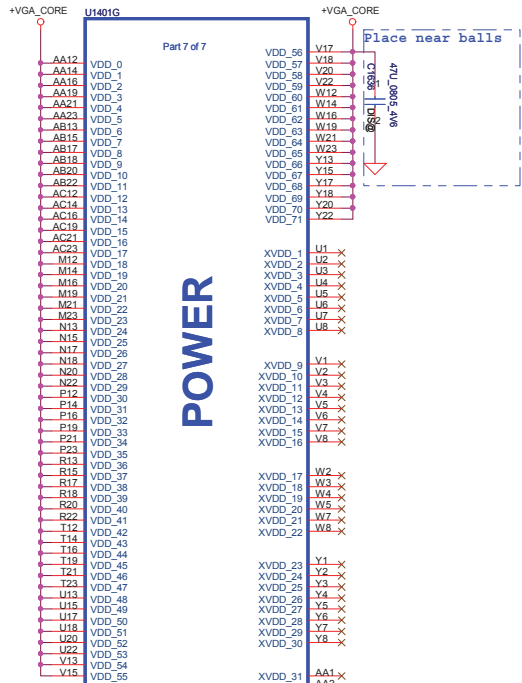
**+1.5V to +1.5VS\_VGA**



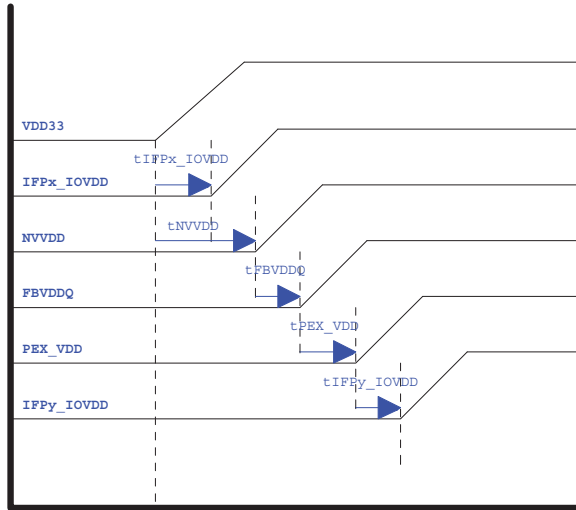
**+3VS to +3VS\_VGA**





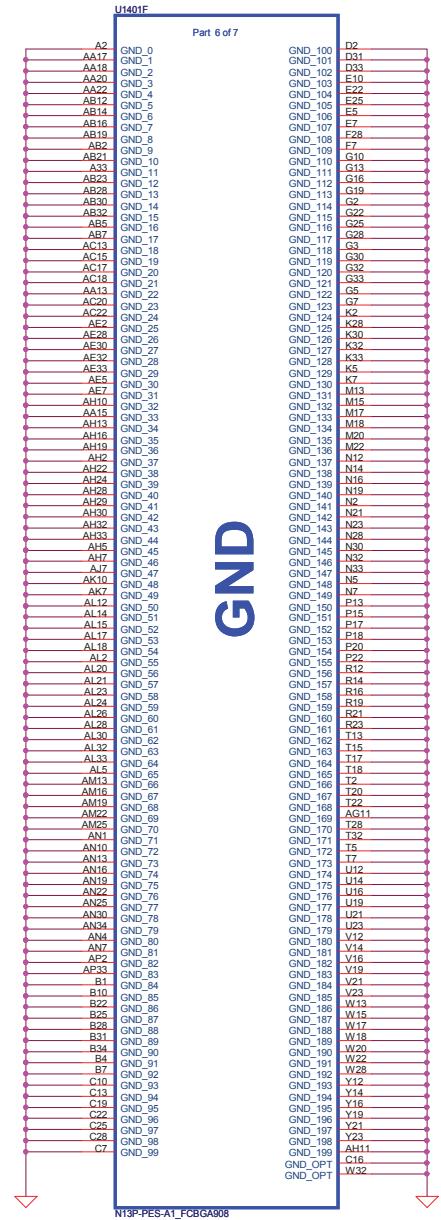


**POWER**



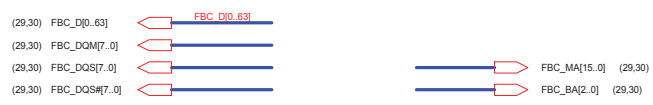
**NV Recommended Power On Sequencing Order**

X=A and B  
Y=C,D,E and F



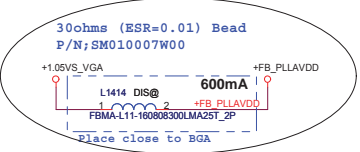
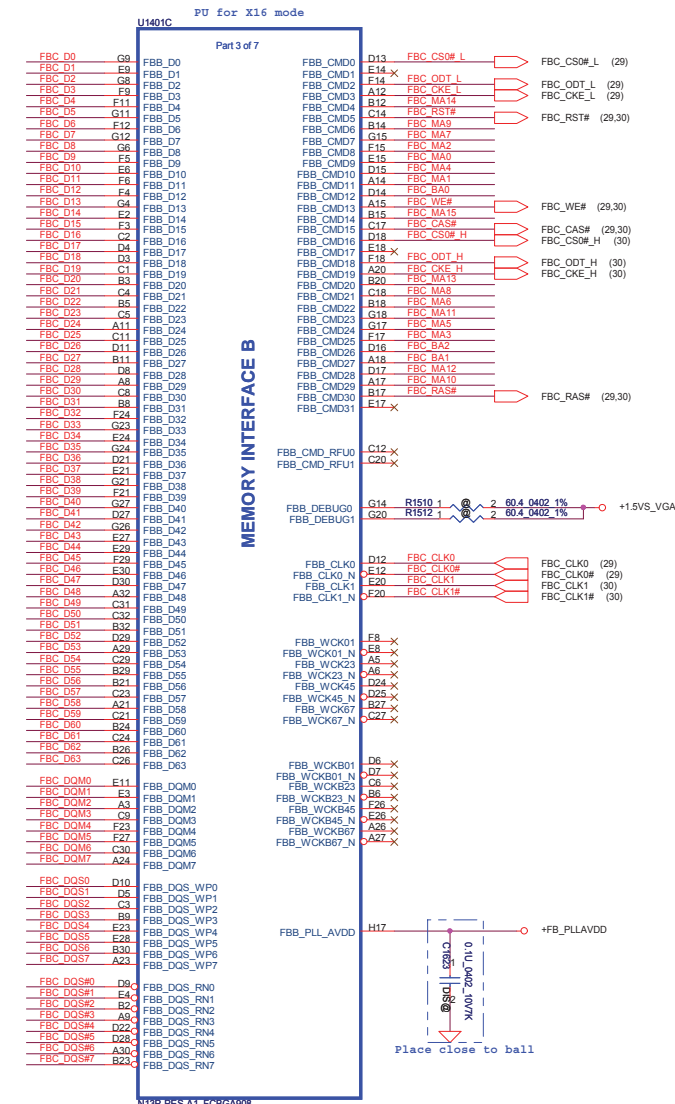
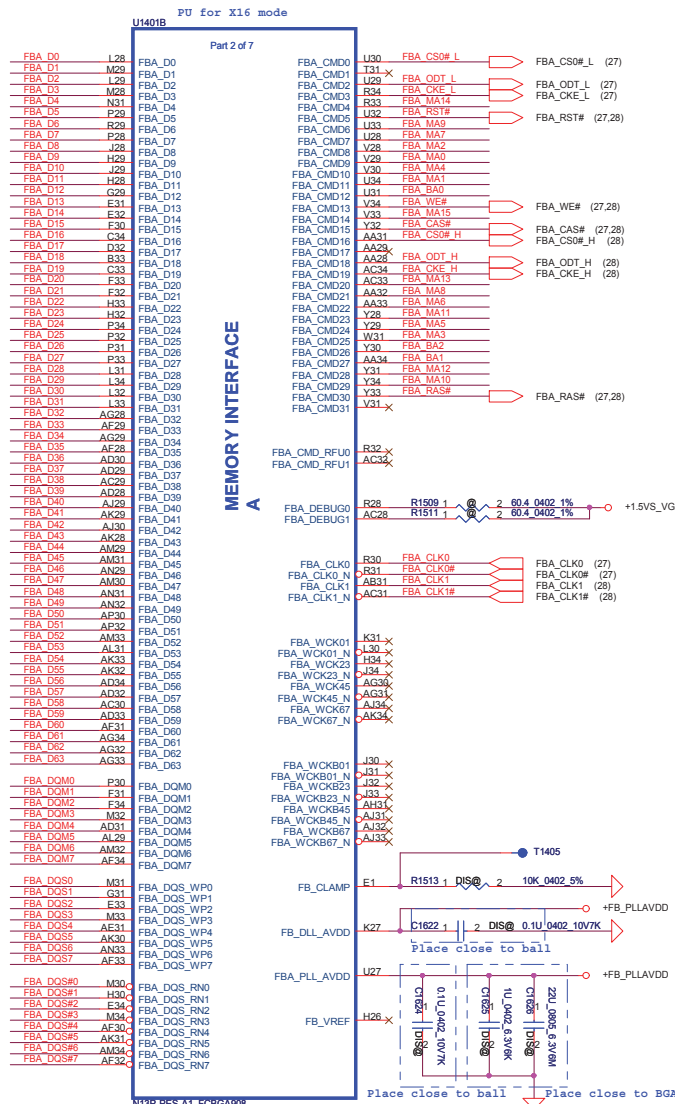
**GND**

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Date	Friday, January 08, 2012	Sheet	25	of		58	

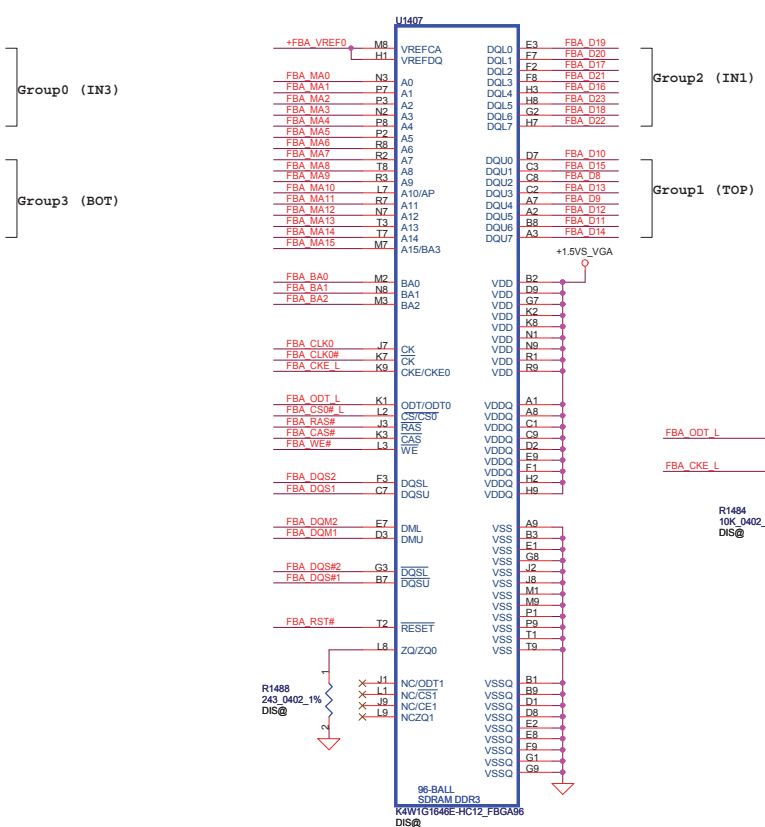
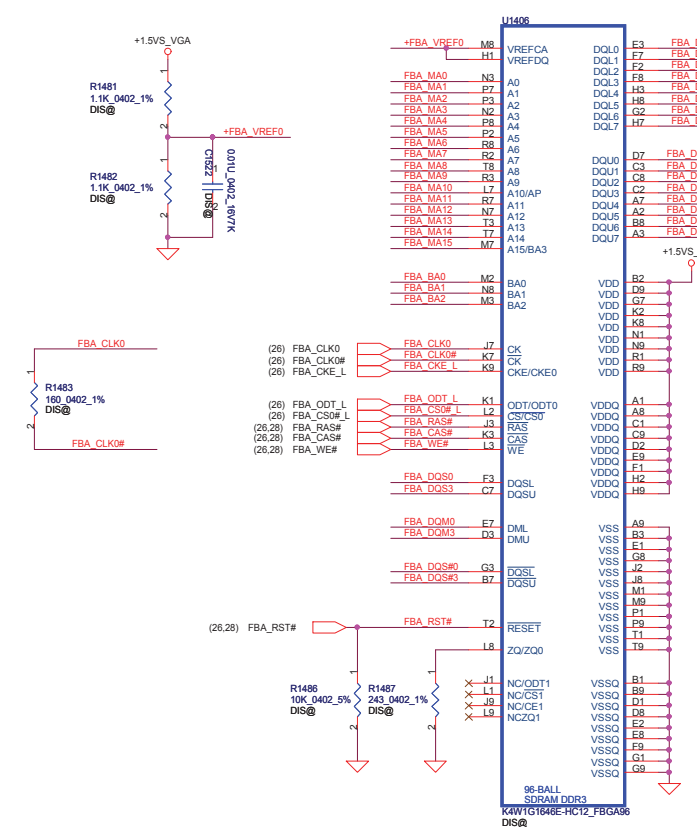
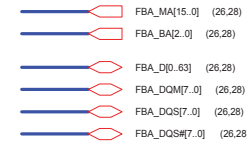


Mode D - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
FbX_CMD0	CS0#_L	
FbX_CMD1		CS0#_L (29)
FbX_CMD2	ODT_L	
FbX_CMD3	CKE_L	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE#	WE#
FbX_CMD14	A15	A15
FbX_CMD15	CAS#	CAS#
FbX_CMD16		CS0#_H
FbX_CMD17		
FbX_CMD18		ODT_H
FbX_CMD19		CKE_H
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS#	RAS#

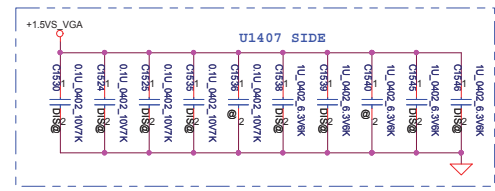
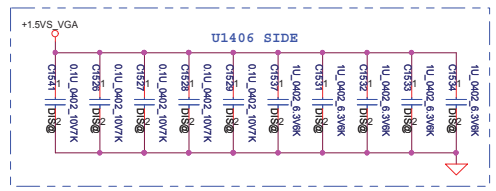


# Memory Partition A - Lower 32 bits

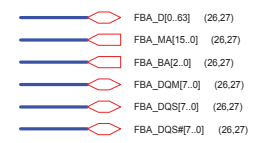
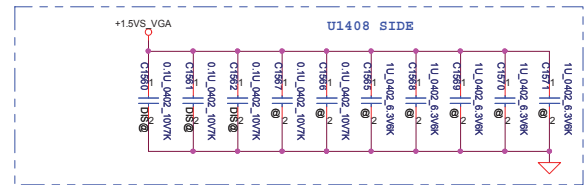
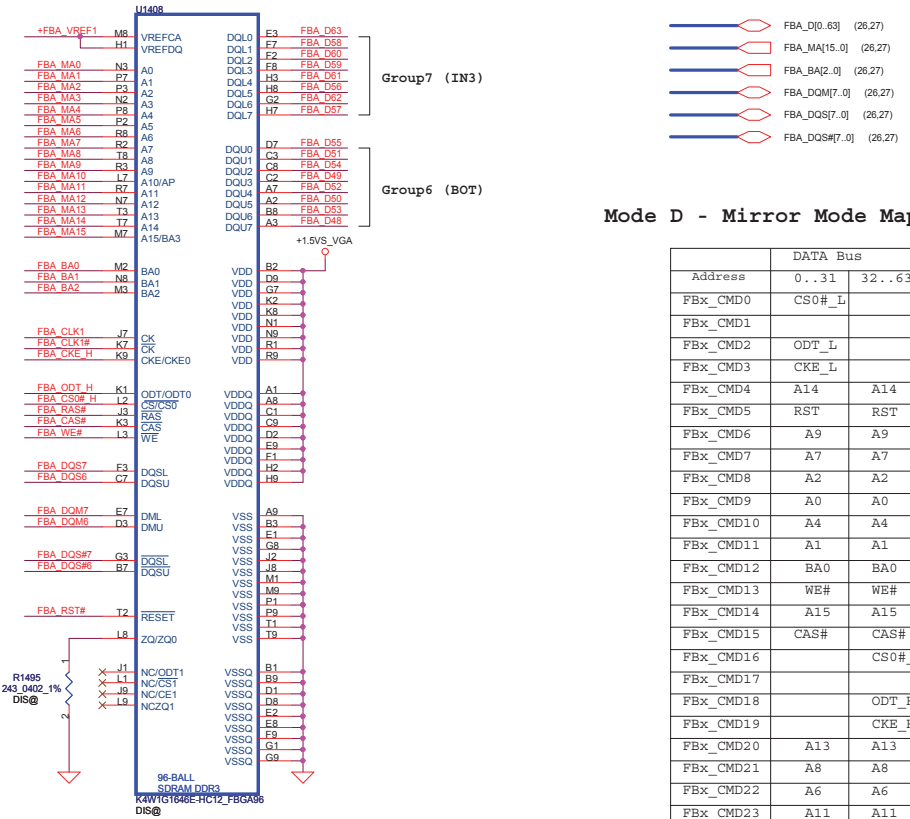
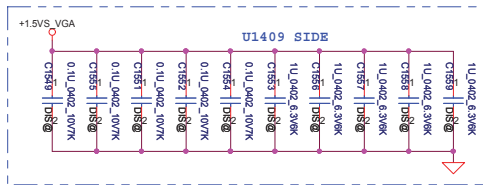
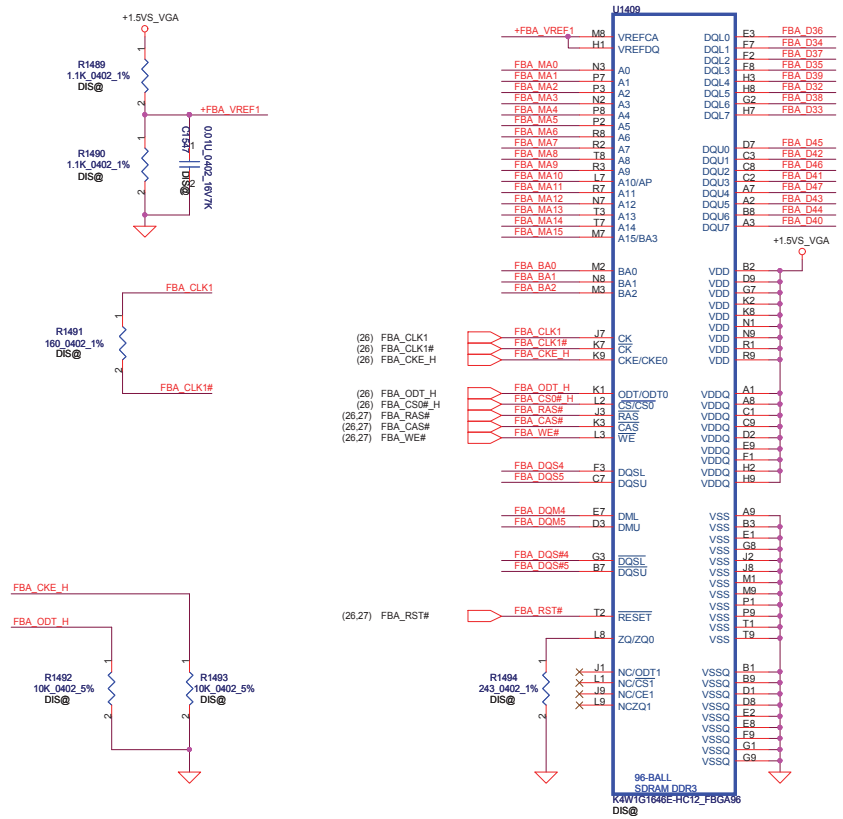


## Mode D - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FbX_CMD0	CS0#_L
FbX_CMD1	
FbX_CMD2	ODT_L
FbX_CMD3	CKE_L
FbX_CMD4	A14 A14
FbX_CMD5	RST RST
FbX_CMD6	A9 A9
FbX_CMD7	A7 A7
FbX_CMD8	A2 A2
FbX_CMD9	A0 A0
FbX_CMD10	A4 A4
FbX_CMD11	A1 A1
FbX_CMD12	BA0 BA0
FbX_CMD13	WE# WE#
FbX_CMD14	A15 A15
FbX_CMD15	CAS# CAS#
FbX_CMD16	CS0#_H
FbX_CMD17	
FbX_CMD18	ODT_H
FbX_CMD19	CHE_H
FbX_CMD20	A13 A13
FbX_CMD21	A8 A8
FbX_CMD22	A6 A6
FbX_CMD23	A11 A11
FbX_CMD24	A5 A5
FbX_CMD25	A3 A3
FbX_CMD26	BA2 BA2
FbX_CMD27	BA1 BA1
FbX_CMD28	A12 A12
FbX_CMD29	A10 A10
FbX_CMD30	RAS# RAS#



# Memory Partition A - Upper 32 bits

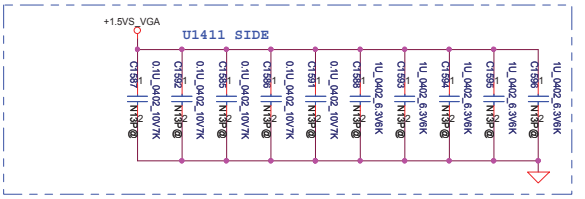
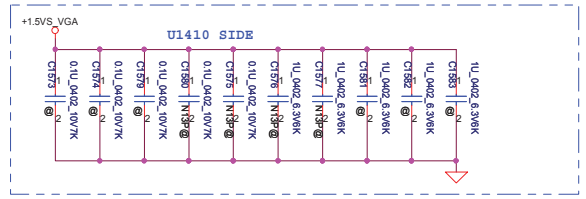
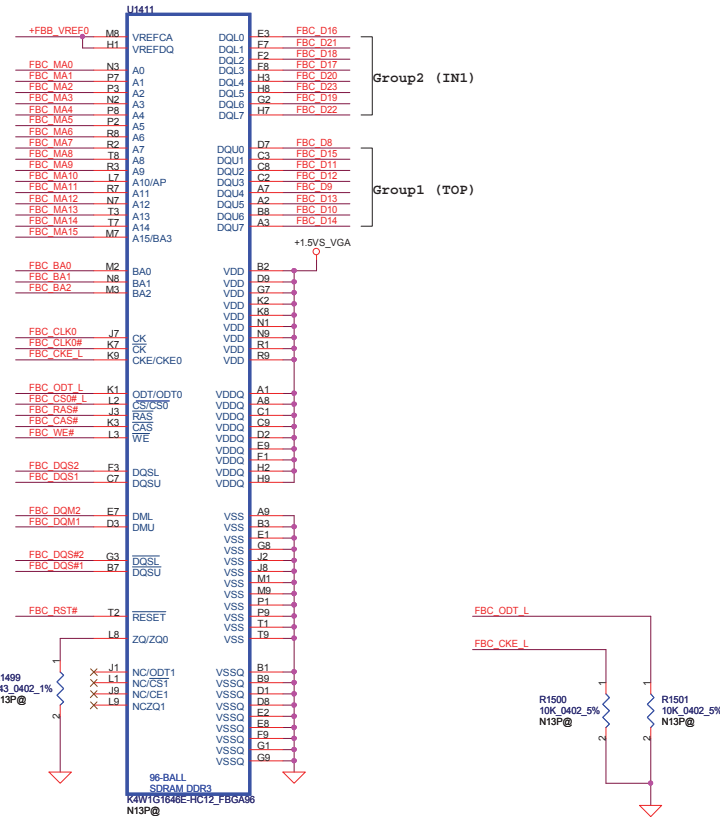
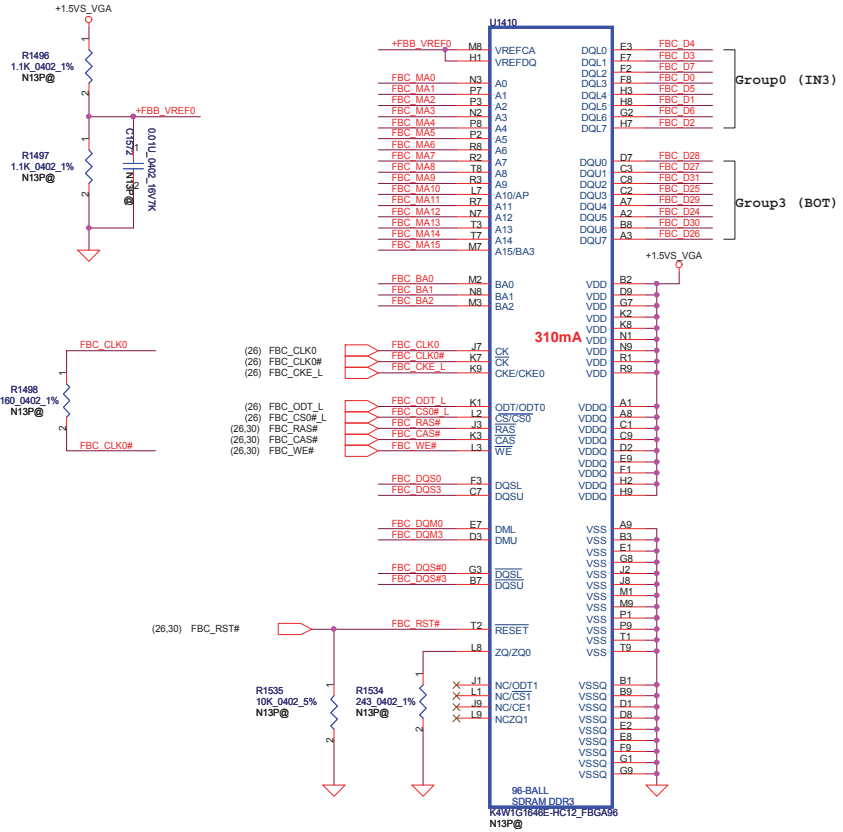


Mode D - Mirror Mode Mapping

Address	DATA Bus	
0..31	32..63	
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#_H	
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19	CKE_H	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

# Memory Partition C - Lower 32 bits

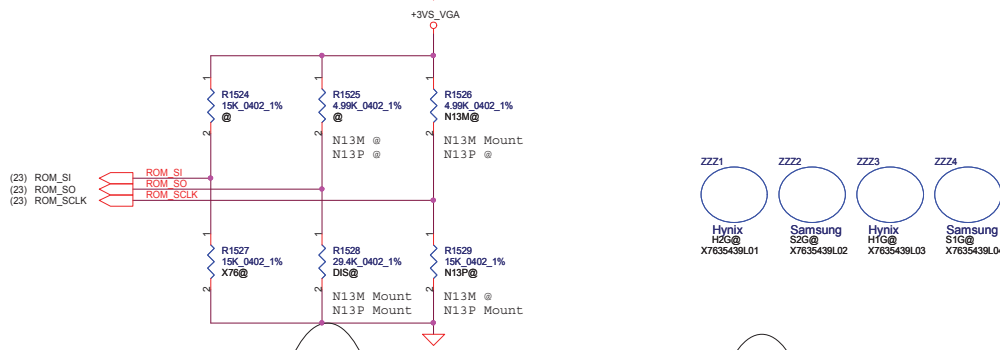
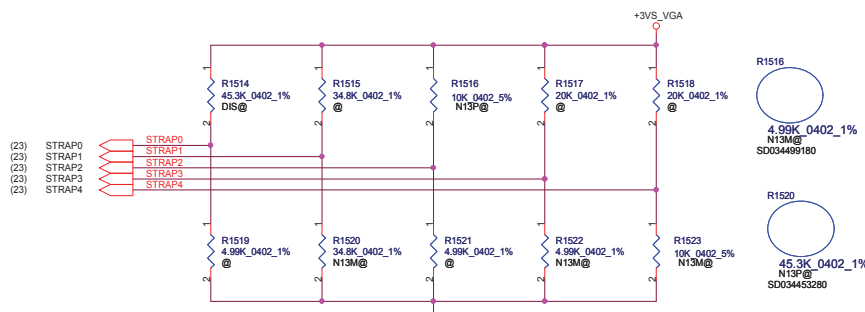
- FBC\_D[0..63] (26,30)
- FBC\_MA[15..0] (26,30)
- FBC\_BA[2..0] (26,30)
- FBC\_DQM[7..0] (26,30)
- FBC\_DQS[7..0] (26,30)
- FBC\_DQS[7..0] (26,30)



## Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS0#_L	
FbX_CMD1		
FbX_CMD2	ODT_L	
FbX_CMD3	CKE_L	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE#	WE#
FbX_CMD14	A15	A15
FbX_CMD15	CAS#	CAS#
FbX_CMD16		CS0#_H
FbX_CMD17		
FbX_CMD18		ODT_H
FbX_CMD19		CKE_H
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS#	RAS#





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

PB 0 BAR SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

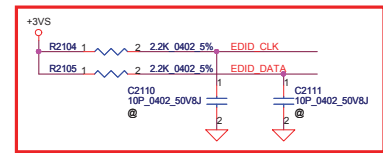
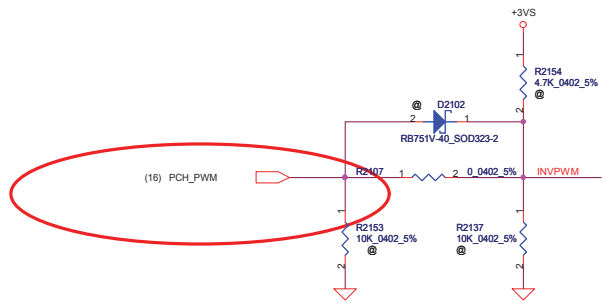
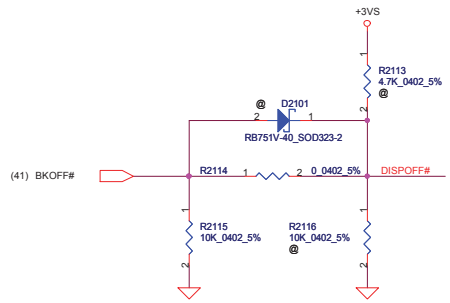
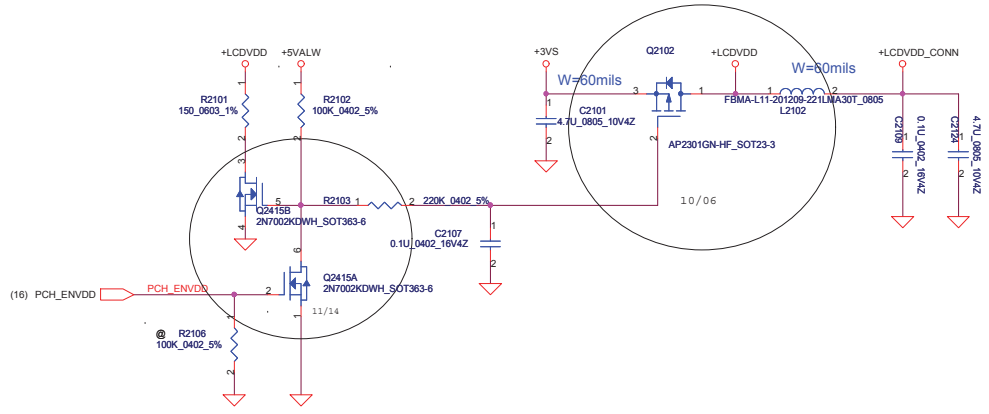
GPU	FB Memory gDDR3	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GL	Samsung 900MHz K4W1G1646G-BC11	PD 10K	PD 15K	PD 20K	PU 45K	PD 45K	PU 10K	NC	NC
	64Mx16						PU 45K (ES)		
	Hynix 900MHz H5TQ1G63DFR-11C	PD 10K	PD 15K	PD 15K	PU 45K	PD 45K	PU 10K	NC	NC
	64Mx16						PU 45K (ES)		
N13M-GE1	Samsung 900MHz K4W2G1646C-HC11	PD 10K	PD 15K	PD 45K	PU 45K	PD 45K	PU 10K	NC	NC
	128Mx16						PU 45K (ES)		
	Hynix 900MHz H5TQ2G63BFR-11C	PD 10K	PD 15K	PD 35K	PU 45K	PD 45K	PU 10K	NC	NC
	128Mx16						PU 45K (ES)		

GPU	FB Memory gDDR3	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1	Samsung 900MHz K4W1G1646G-BC11	PD 30K	PU 5K	PD 20K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	64Mx16								
	Hynix 900MHz H5TQ1G63DFR-11C	PD 30K	PU 5K	PD 15K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	64Mx16								
N13M-GE1	Samsung 900MHz K4W2G1646C-HC11	PD 30K	PU 5K	PD 45K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	128Mx16								
	Hynix 900MHz H5TQ2G63BFR-11C	PD 30K	PU 5K	PD 35K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	128Mx16								

9/27  
from 15K to 5K

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				Custom	0.6
				Date	Friday, January 08, 2012
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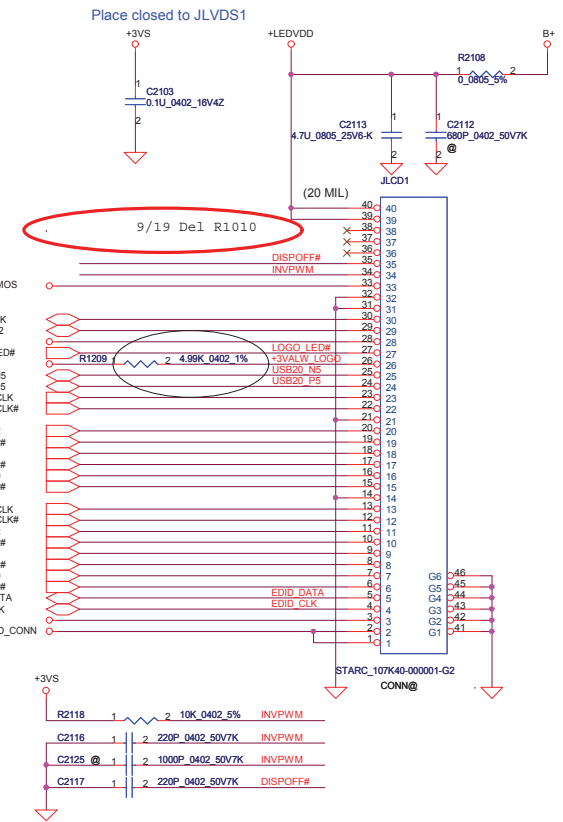
# LCD POWER CIRCUIT



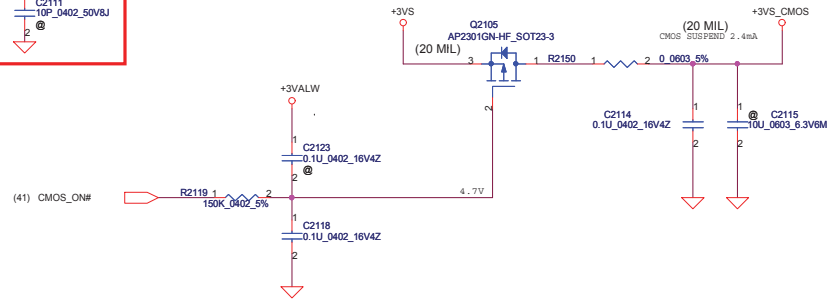
A LOGO RED LIGHT  
CMOS

# LCD/LED PANEL Conn.

PN:SP01000XE00

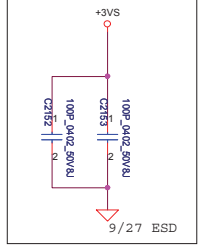
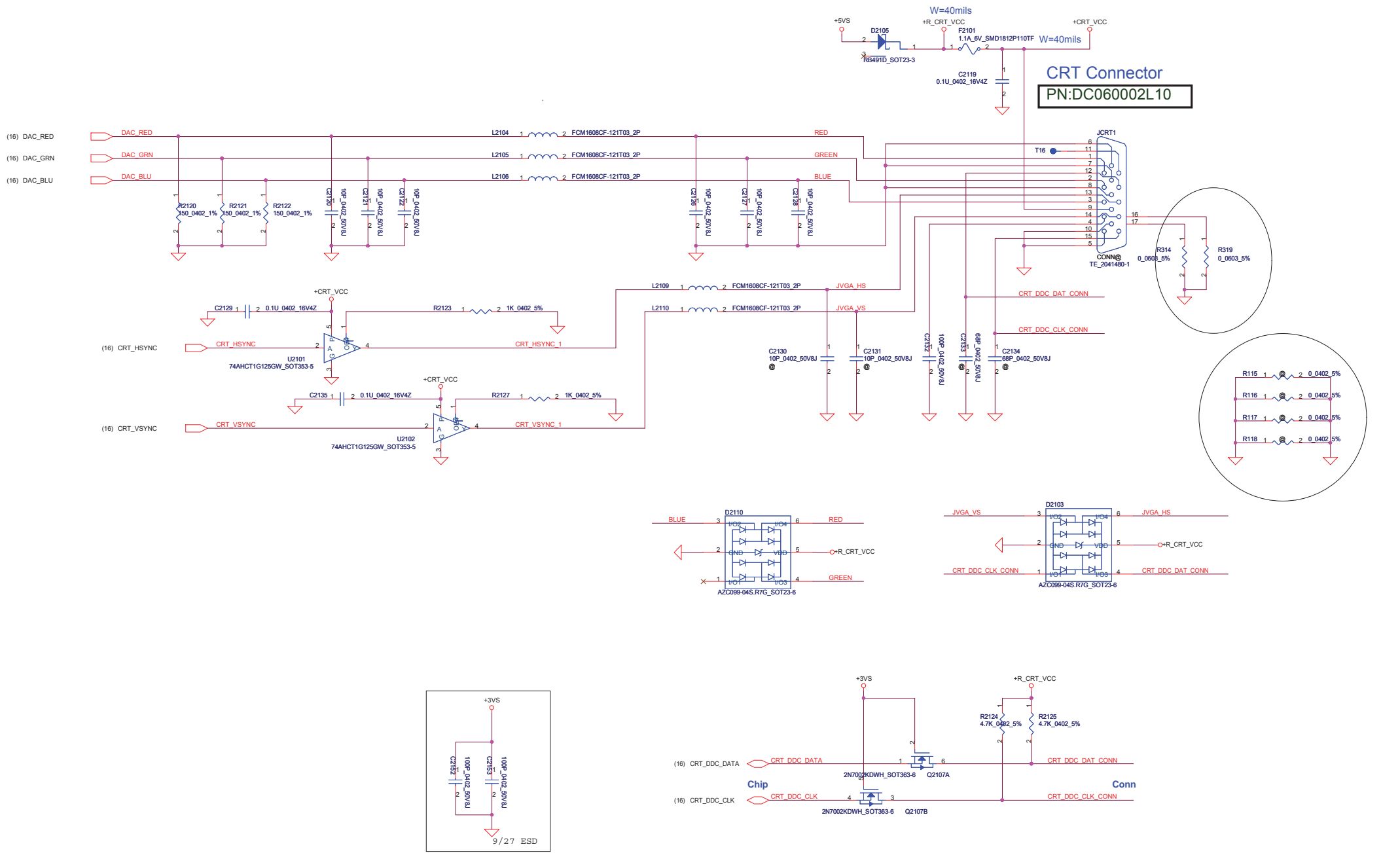


# CMOS Camera Conn

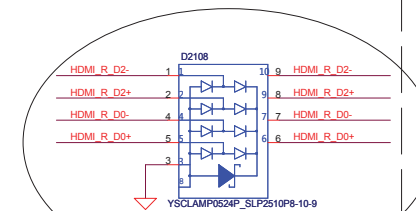
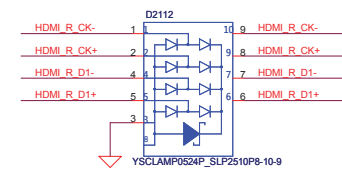
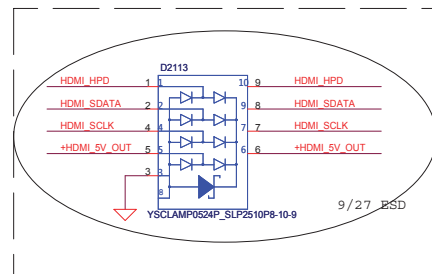
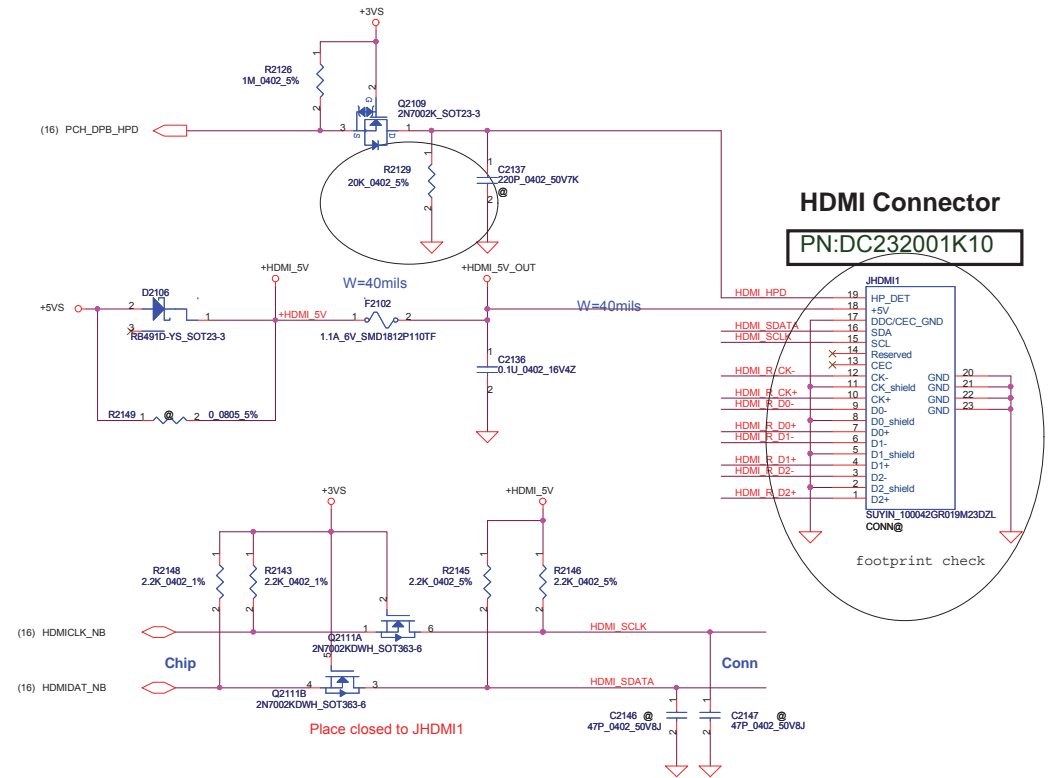
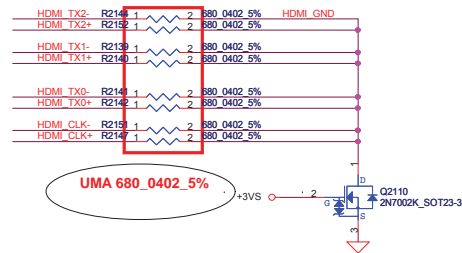
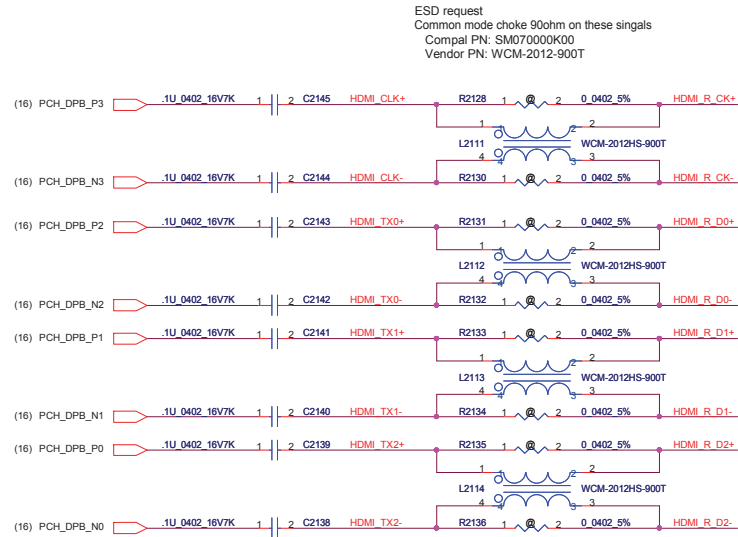


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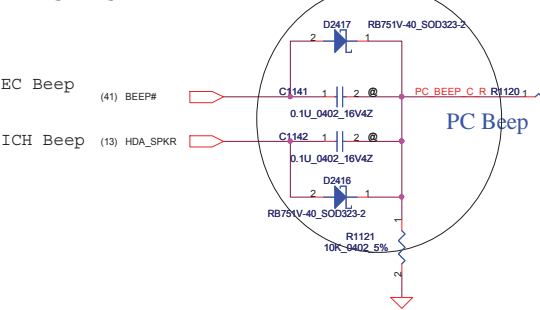
<b>Security Classification</b>		Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title <b>CRT Connector</b>	
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	HDMI Connector	
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Custom		LA-8131P	0.6	Date:	Tuesday, January 10, 2012
				Sheet	34 of 58

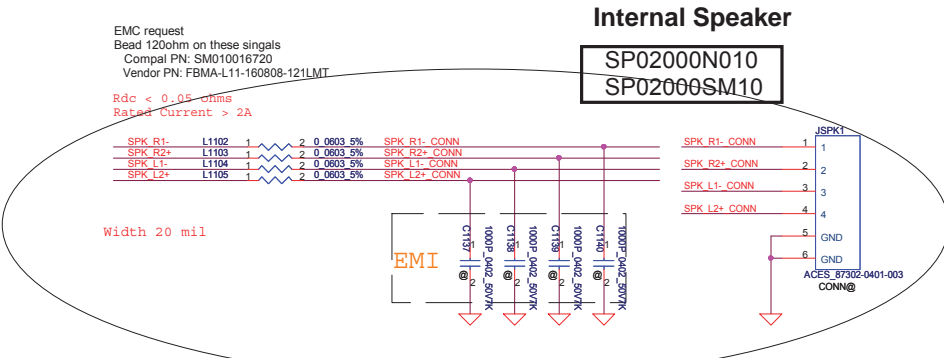
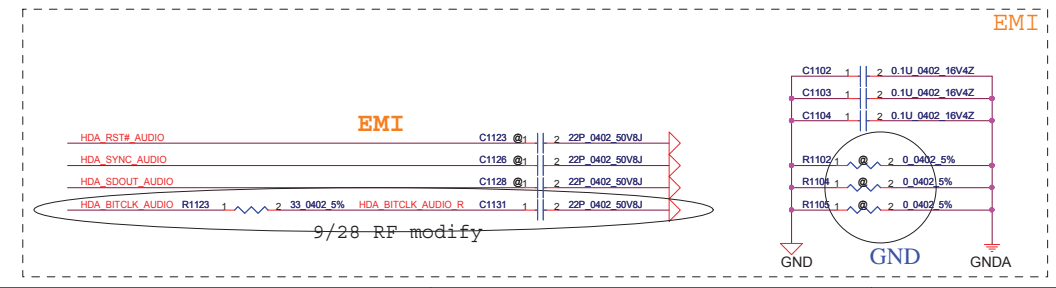
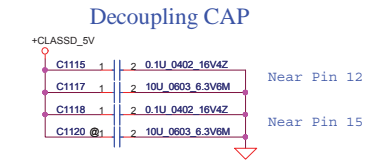
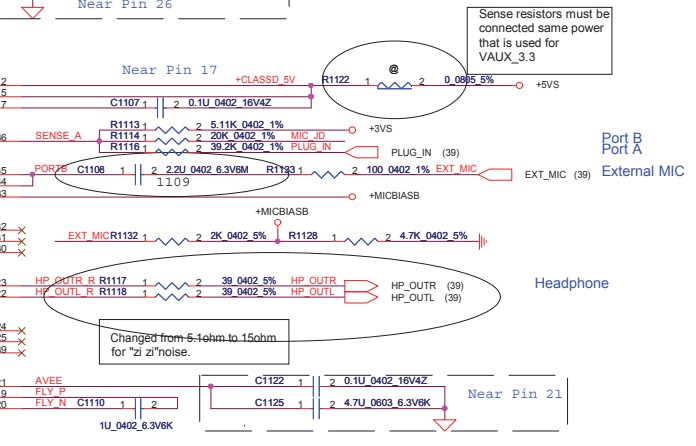
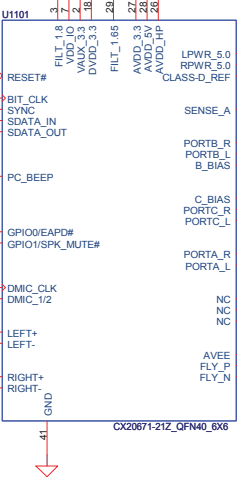
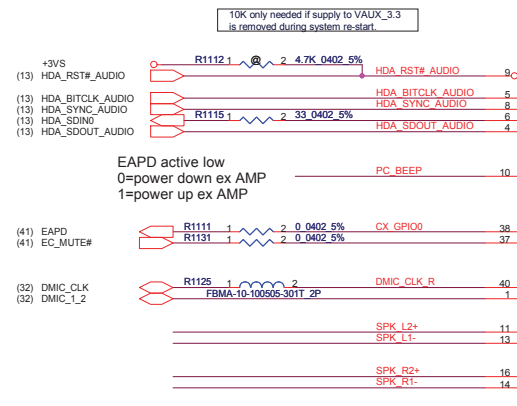
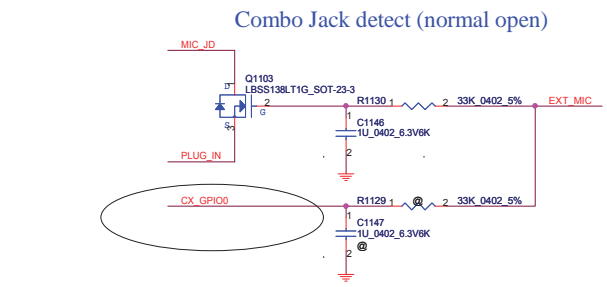
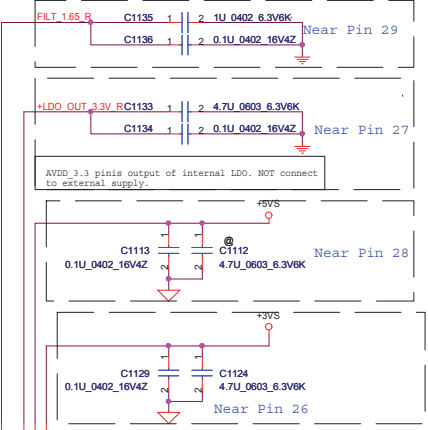
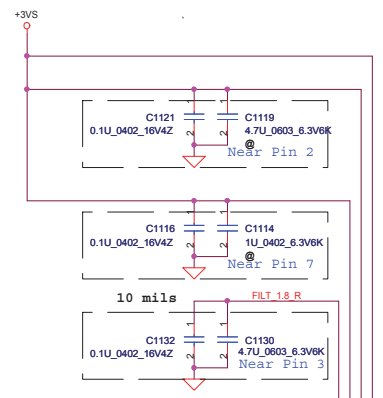
CX20671  
High Definition Audio Codec SoC  
With Integrated Class-D Stereo  
Amplifier.

An integrated 5 V to 3.3 V Low-dropout  
voltage regulator (LDO).  
An integrated 3.3 V to 1.8V Low-dropout  
voltage regulator (LDO).



EC Beep (41) BEEP#  
ICH Beep (13) HDA\_SPKR

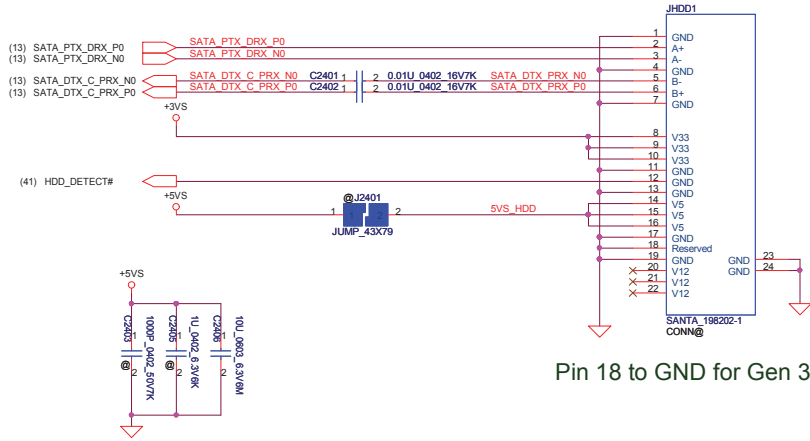
Layout Note: Path from +5VS to Pin12,  
Pin15 must be very low  
resistance (<0.01 ohms)  
To support Wake-on-Jack or Wake-on-Ring, the CODEC  
VAUX\_3.3 & VDD\_IO pins must be powered by a rail that  
is not removed unless AC power is removed.  
\*DSH page#2 has more detail.



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Size	Custom	Document Number	LA-8131P	Rev	0.6
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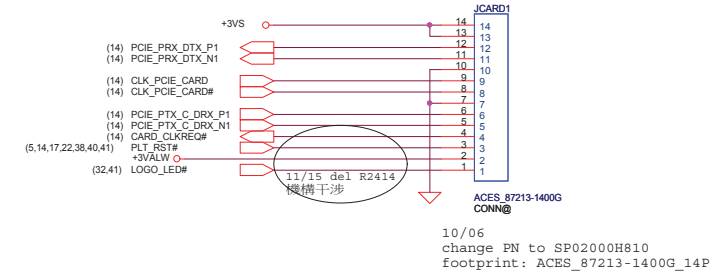
### SATA HDD CONN.

PN:DC010004C00



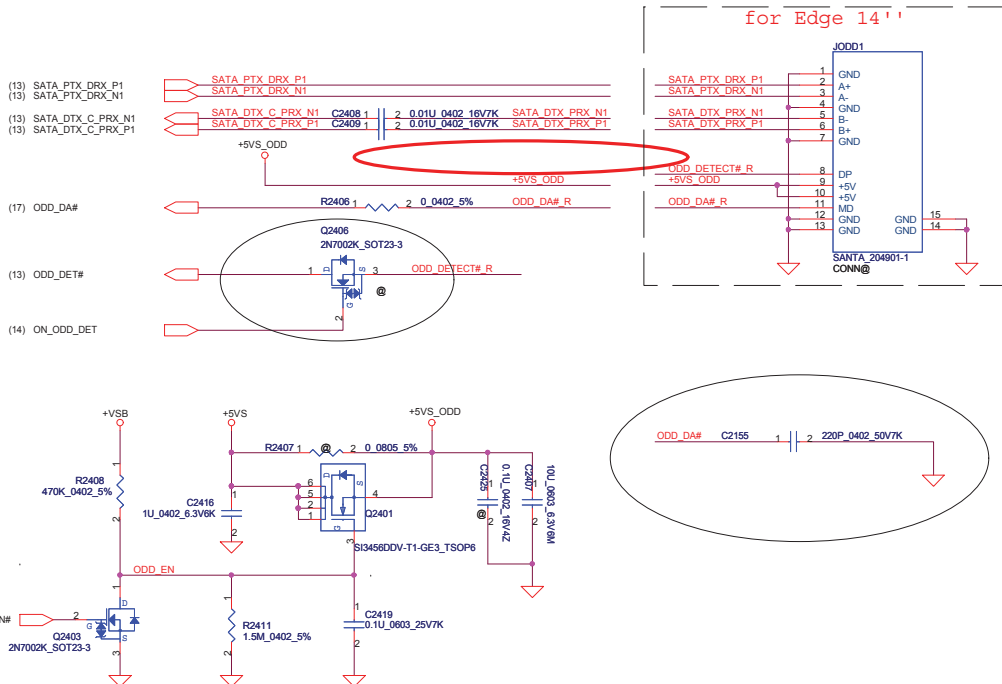
### Card Reader CONN.

PN:SP01001BF00

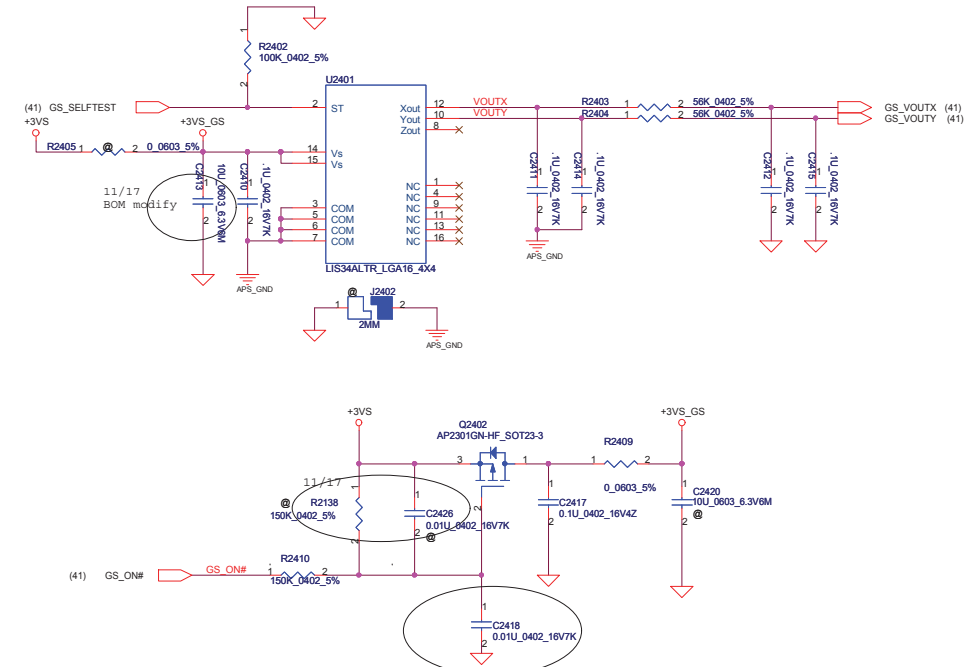


### SATA ODD CONN.

PN:SP01000TU10

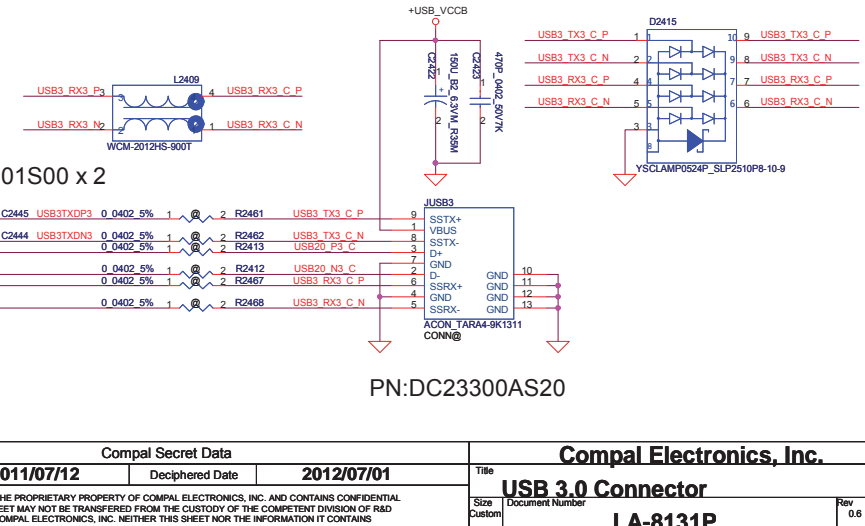
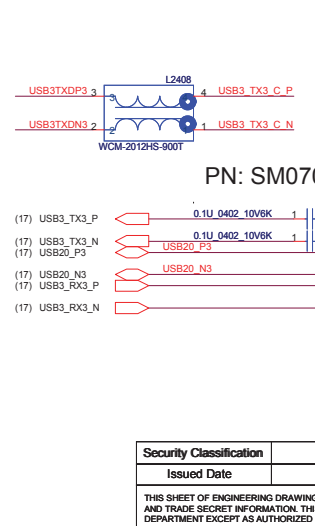
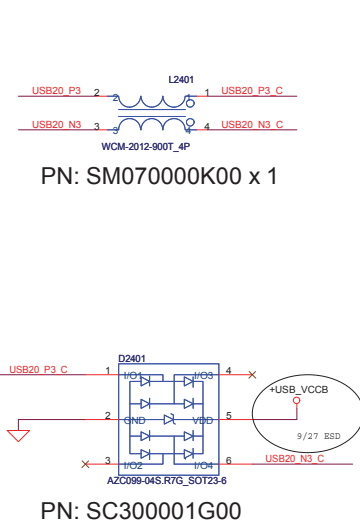
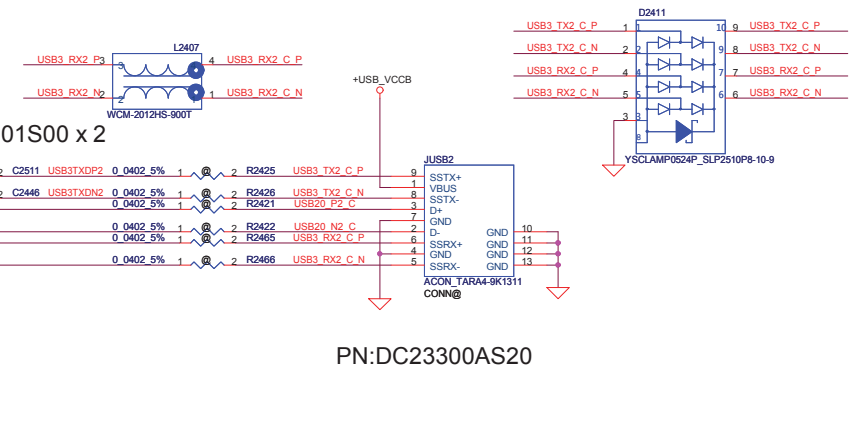
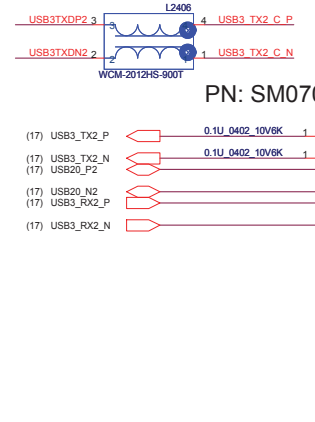
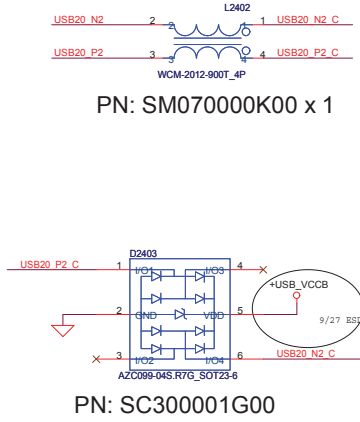
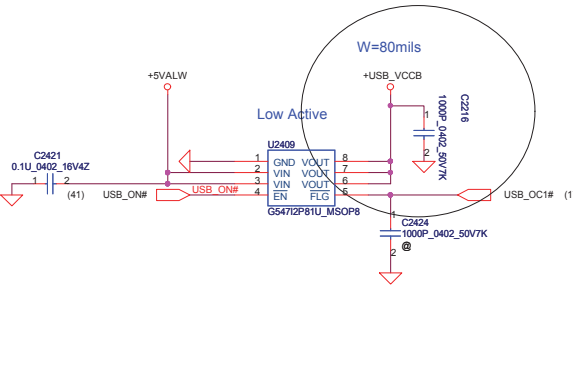
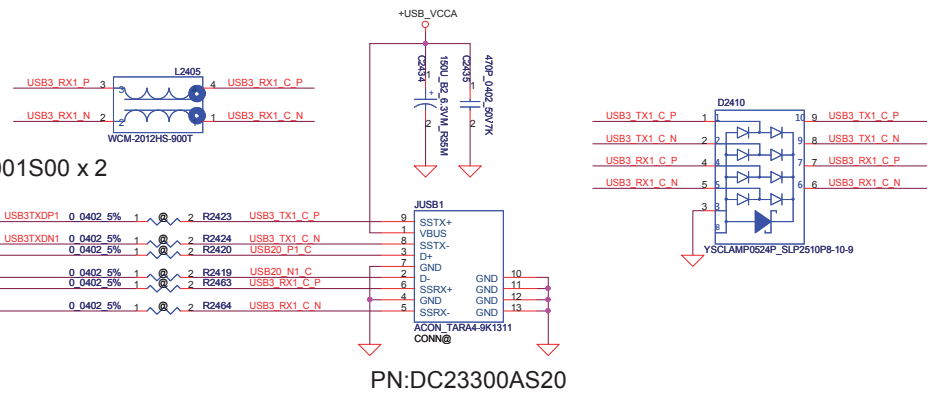
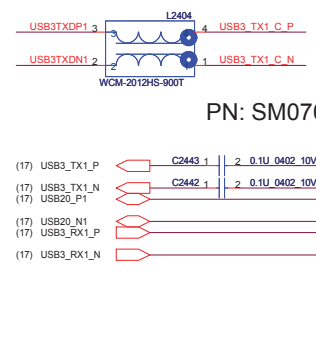
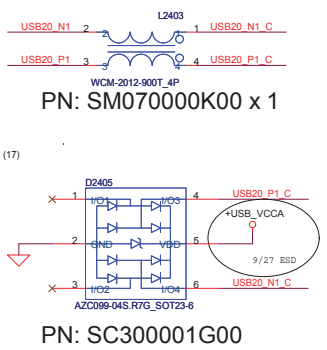
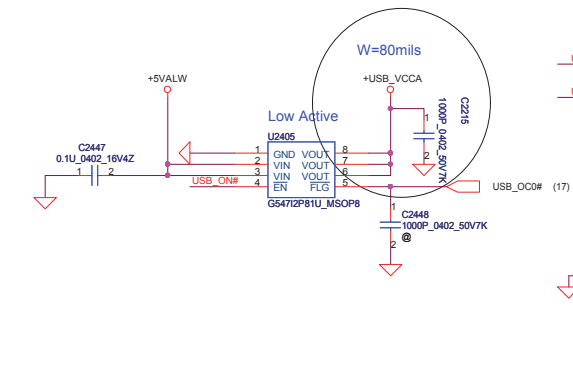


### APS G-Sensor



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Issued Date	2011/07/12	Deciphered Date	2012/07/01	HDD/ODD/Card reader/G-Sensor			
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				Custom	LA-8131P	06	
Date:	Friday, January 08, 2012	Sheet	38	of 58			

**USB 3.0 Conn.**

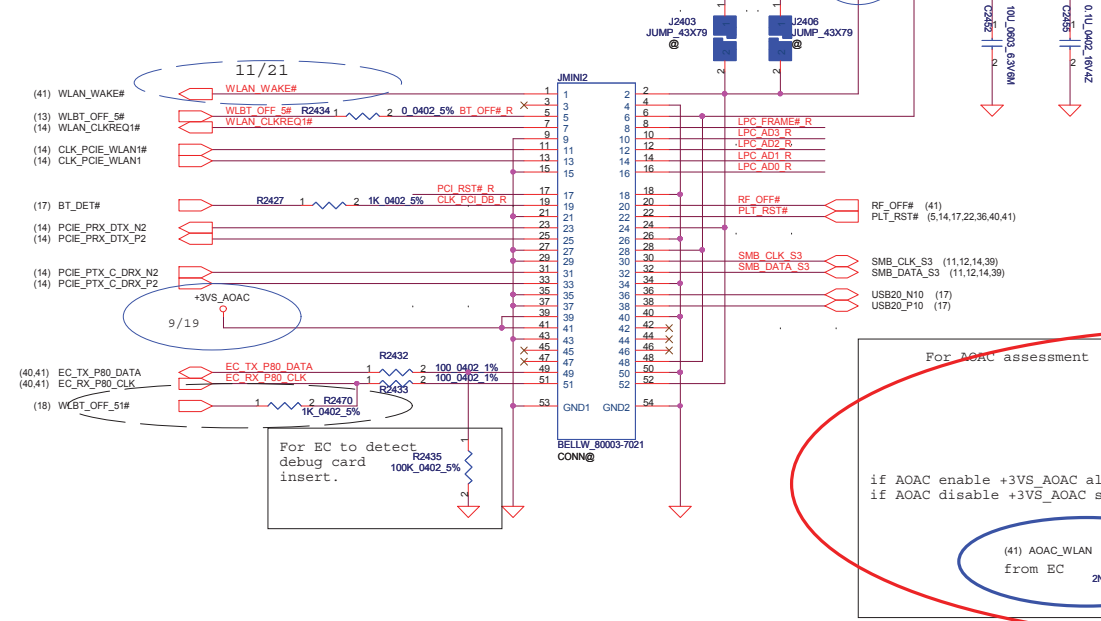


<b>Security Classification</b>		Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	USB 3.0 Connector
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Size	Custom	Date	Friday, January 08, 2012	Sheet	37 of 58
				Rev	0.6
				Part Number	LA-8131P

# Mini-Express Card for WLAN/WiMAX(Half)

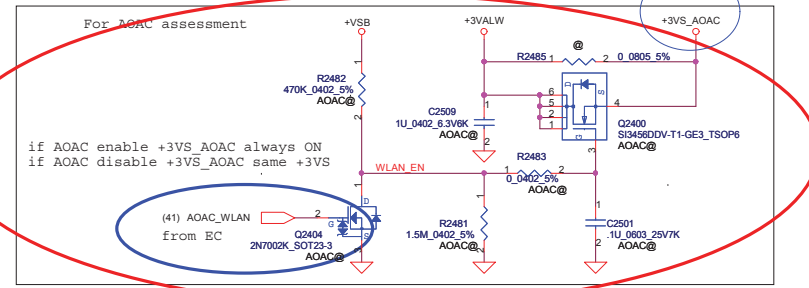
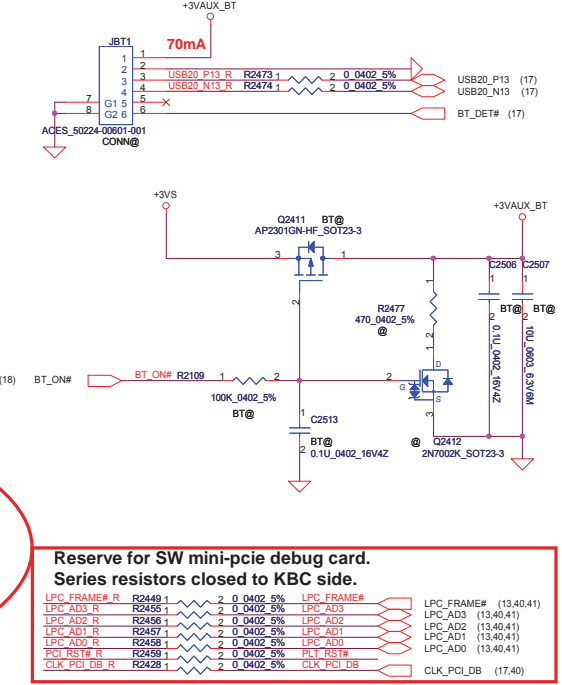
## Mini-Express Card(WLAN/WiMAX)

PN:SP07000JP00



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

### BT Connector

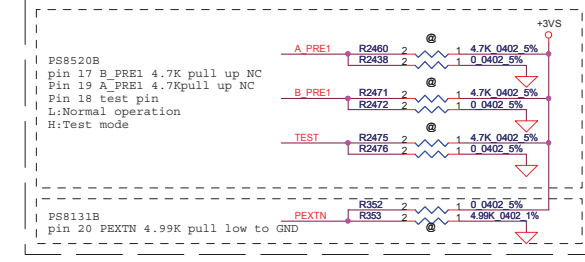
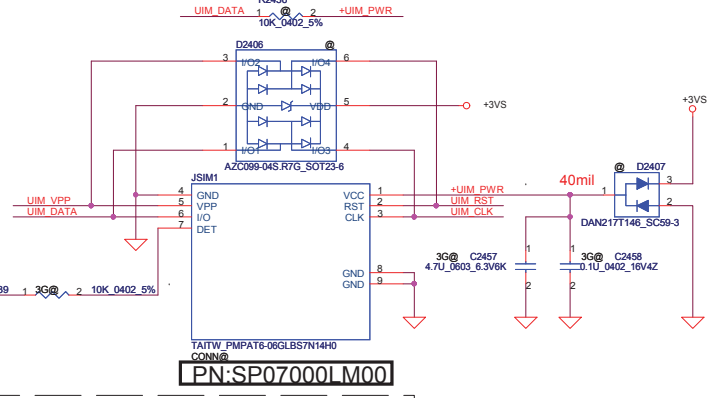
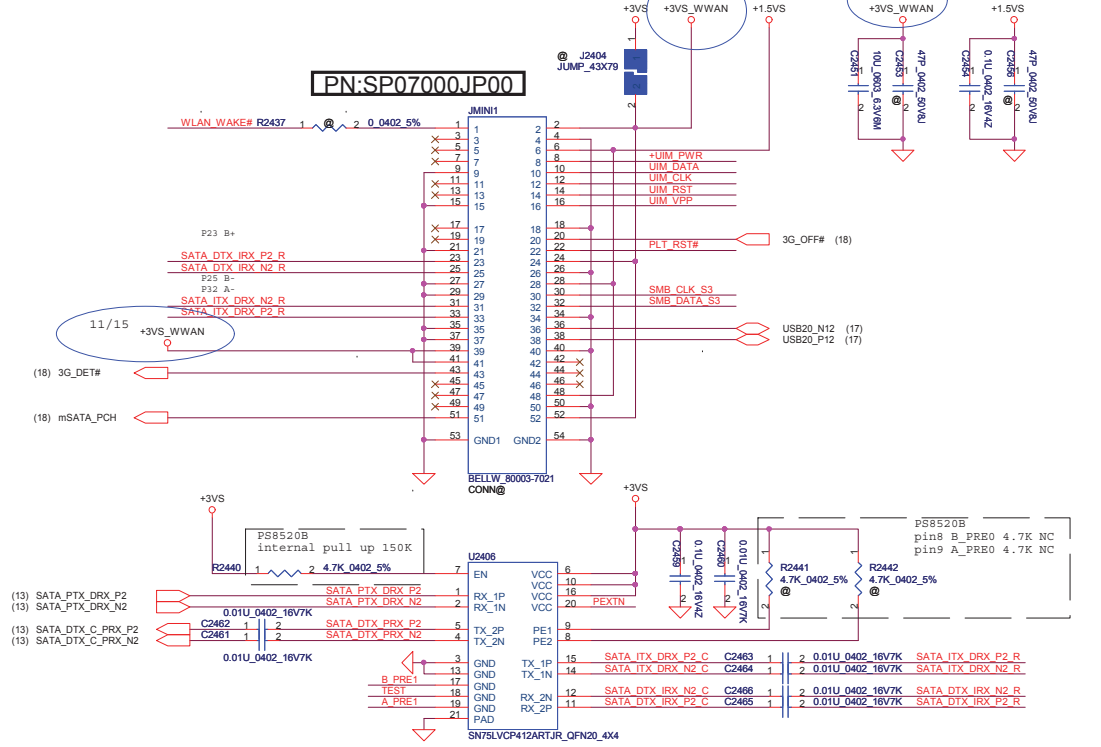


Reserve for SW mini-pcie debug card. Series resistors closed to KBC side.

LPC_FRAME#_R	R2449	2	0.0402 5%	LPC_FRAME#	(13,40,41)	
LPC_ADS_R	R2455	1	2	0.0402 5%	LPC_ADS	(13,40,41)
LPC_AD2_R	R2456	1	2	0.0402 5%	LPC_AD2	(13,40,41)
LPC_AD1_R	R2457	1	2	0.0402 5%	LPC_AD1	(13,40,41)
LPC_ADD_R	R2458	1	2	0.0402 5%	LPC_ADD	(13,40,41)
PLT_RST#_R	R2459	1	2	0.0402 5%	PLT_RST#	(13,40,41)
CLK_PCI_DB_R	R2428	1	2	0.0402 5%	CLK_PCI_DB	(17,40)

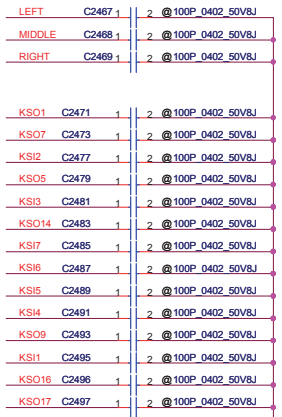
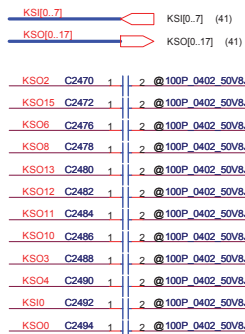
# Mini-Express Card for WWAN/mSATA(Full)

PN:SP07000JP00



Security Classification	Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	WLAN and WWAN/mSATA
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Size Custom			Document Number	
			LA-8131P	
Date: Tuesday, January 10, 2012 Sheet 38 of 58				

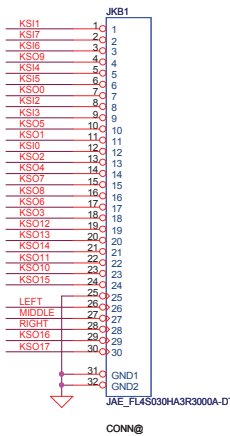
### INT\_KBD Conn.



CONN PIN define need double check

Reserve for ESD.

### PN:SP01000YH00

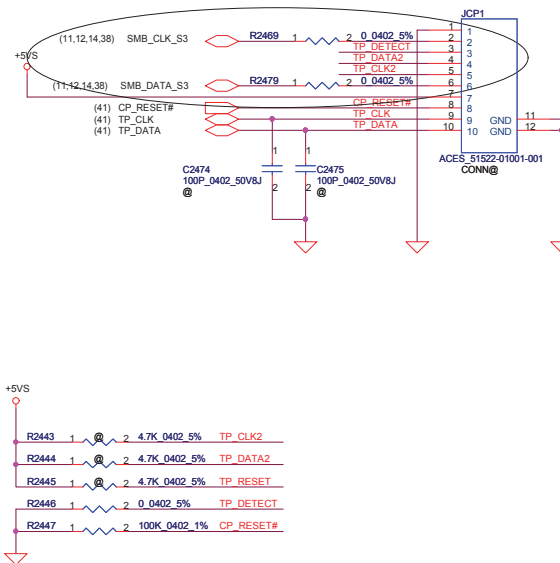


M1(Left BUTTON)  
M2(Center BUTTON)  
M3(Right BUTTON)

CONN@

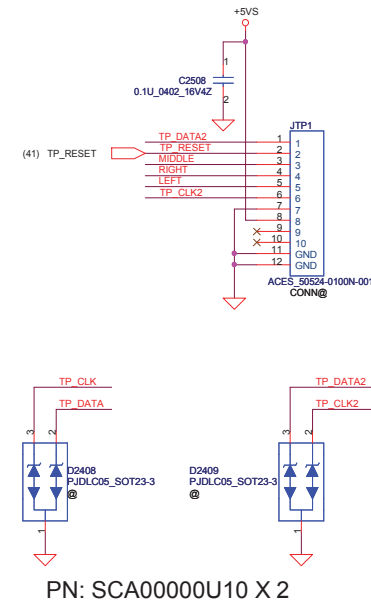
### Click pad

#### PN:SP01001AL00



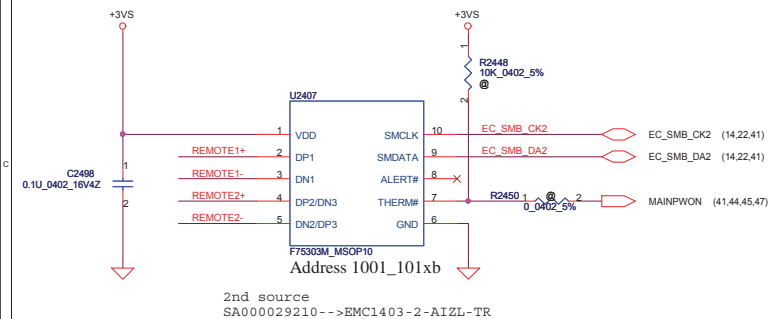
### Track point

#### PN:SP01001CH00



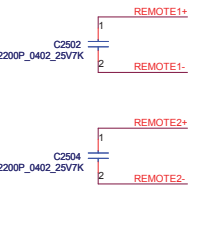
PN: SCA00000U10 X 2

### Fintek thermal sensor placed near by TOP DDR3

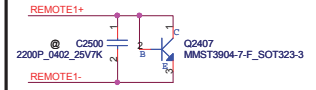


2nd source  
SA000029210-->EMC1403-2-AIZL-TR

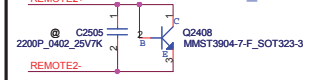
#### Close U2407



#### BOTTOM DDR3

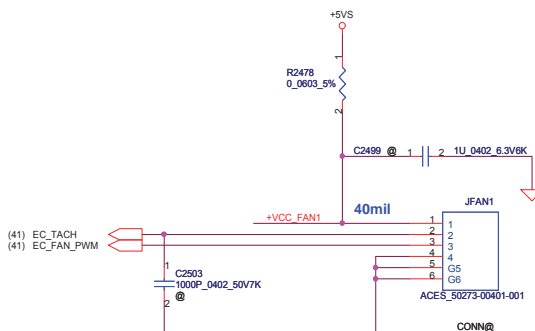


#### TOP CPU\_CORE



REMOTE1,2+/- :  
 Trace width/space:10/10 mil  
 Trace length:<8"

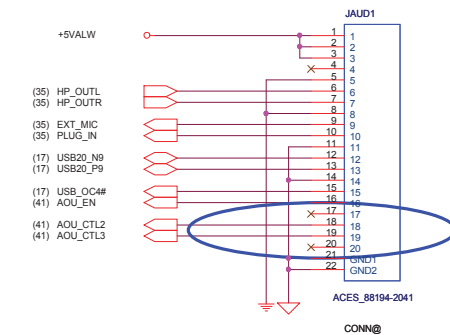
### FAN CONN.



#### PN:SP02000U900

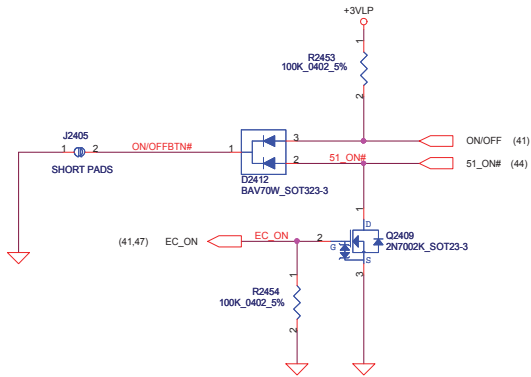
### Audio Board

#### PN:SP011108040

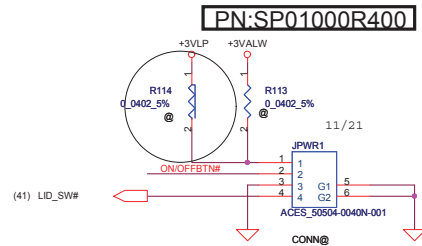


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Issued Date	2011/07/12	Deciphered Date	2012/07/01	KB/TP/Thermal Sensor/Audio	
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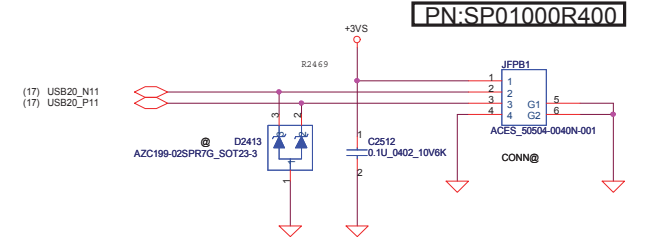
### Power Button



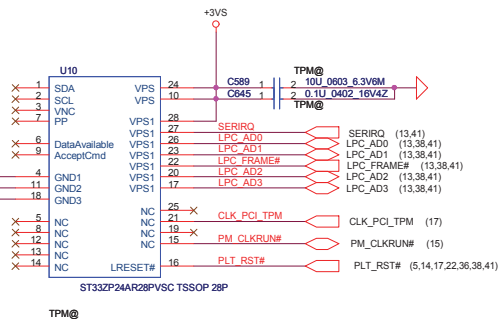
### Power Button CONN.



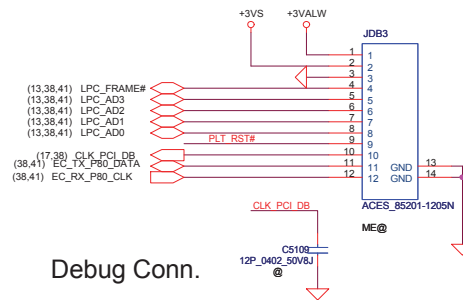
### Finger Print Board



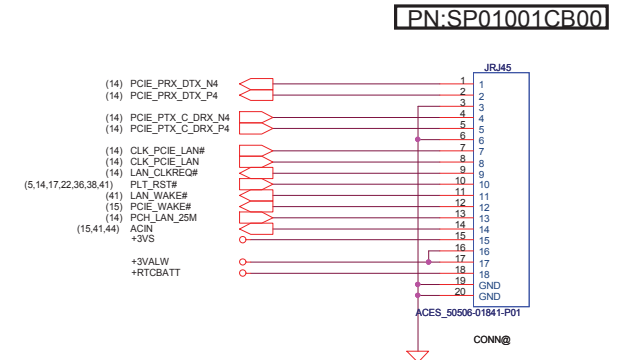
### TPM



### Debug Conn.

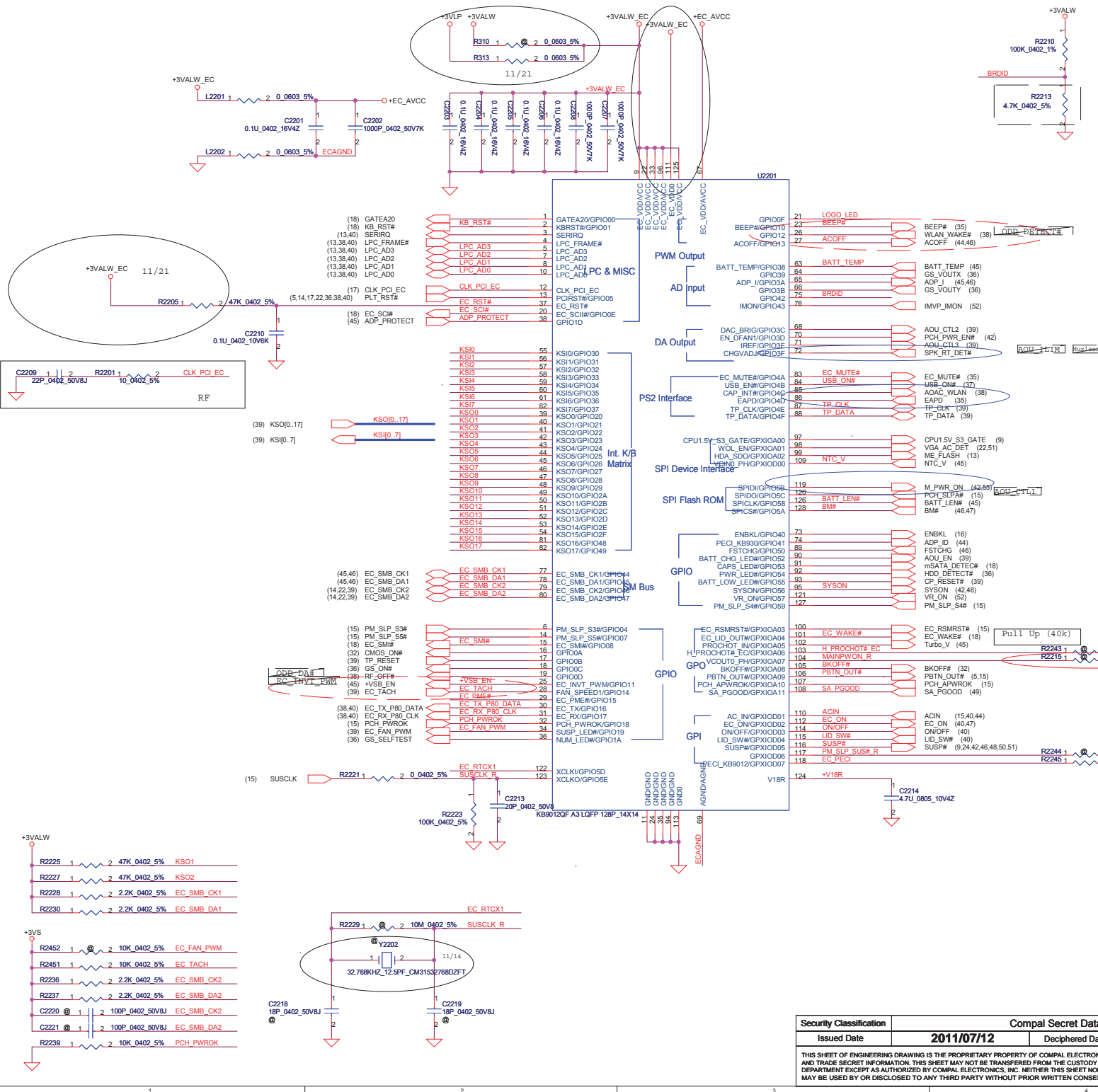


### RJ45 Board



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				Date		Tuesday, January 10, 2012	
				Sheet		40 of 58	
				Date		Tuesday, January 10, 2012	
				Sheet		40 of 58	



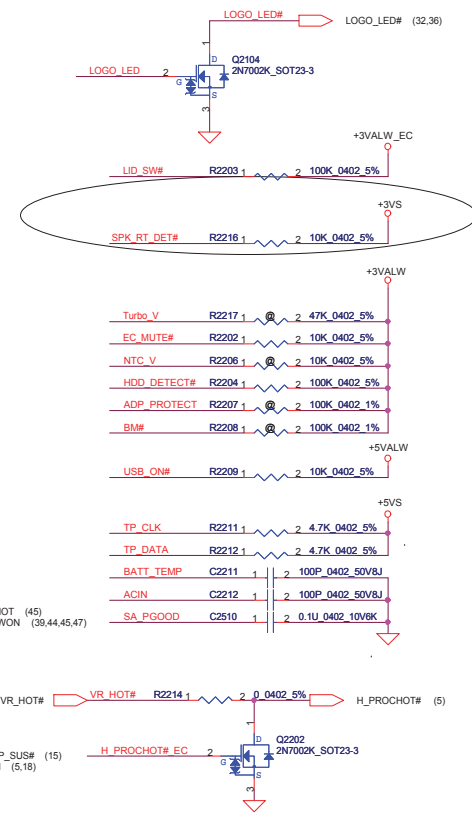


Vcc	3.3V +/- 5%
R2210	100K +/- 1%

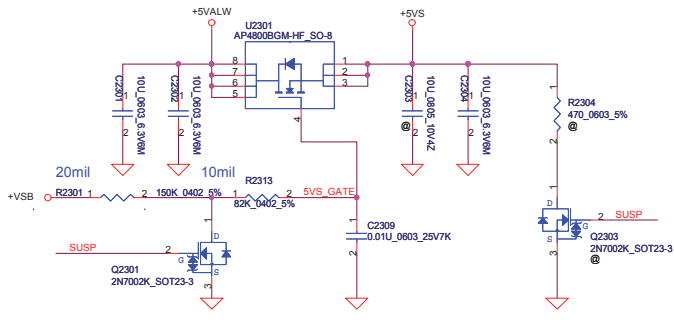
Board ID	R2213	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SIT2
2	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SIT1
3	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
4	33K +/- 5%	0.712 V	0.819 V	0.875 V	SDV

SD028330280 S RES 1/16W 33K +-5% 0402  
SD028180280 S RES 1/16W 18K +-5% 0402  
SD028820180 S RES 1/16W 8.2K +-5% 0402  
SD028470180 S RES 1/16W 4.7K +-5% 0402

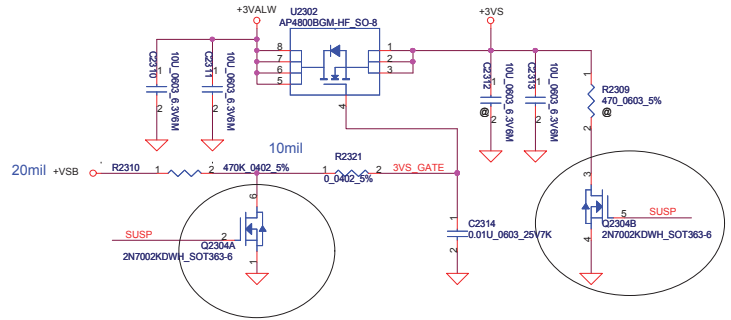


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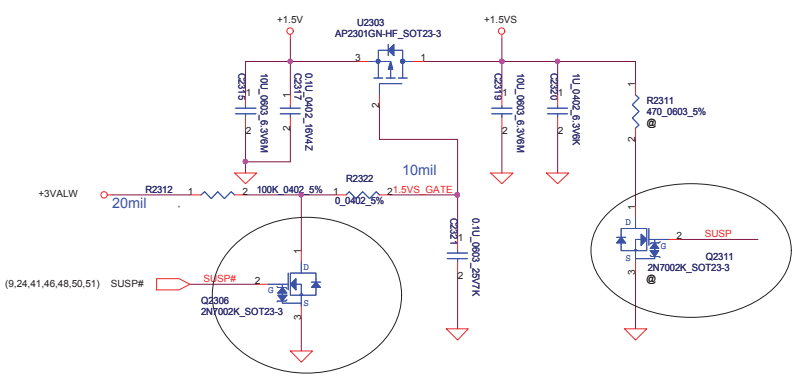
**+5VALW TO +5VS**



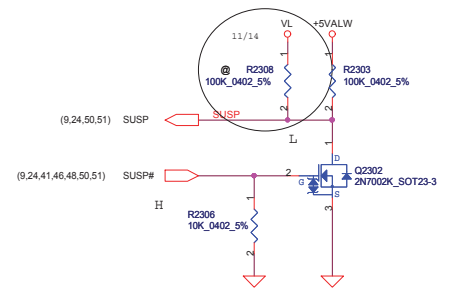
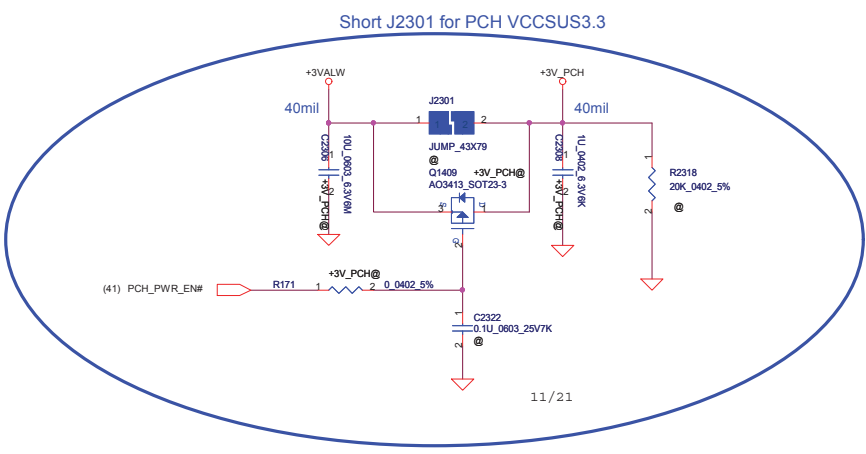
**+3VALW TO +3VS**



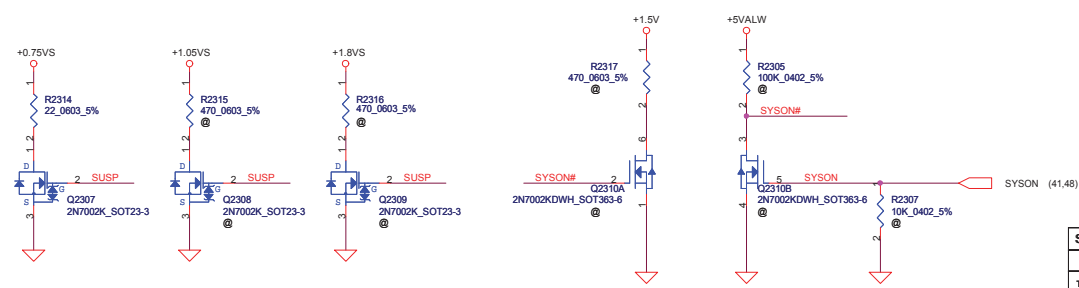
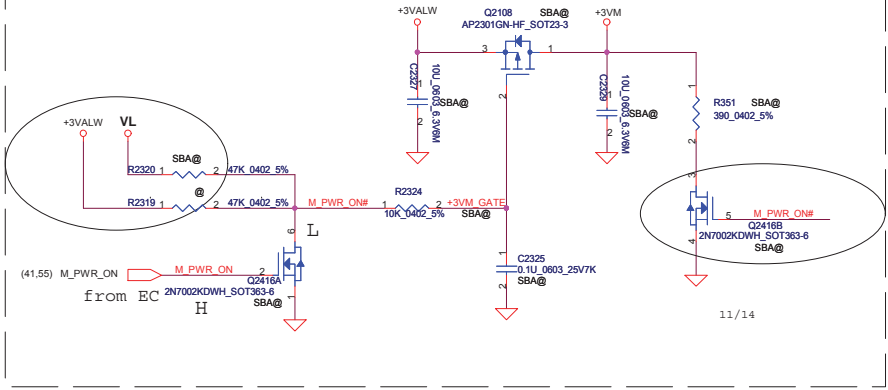
**+1.5V to +1.5VS**



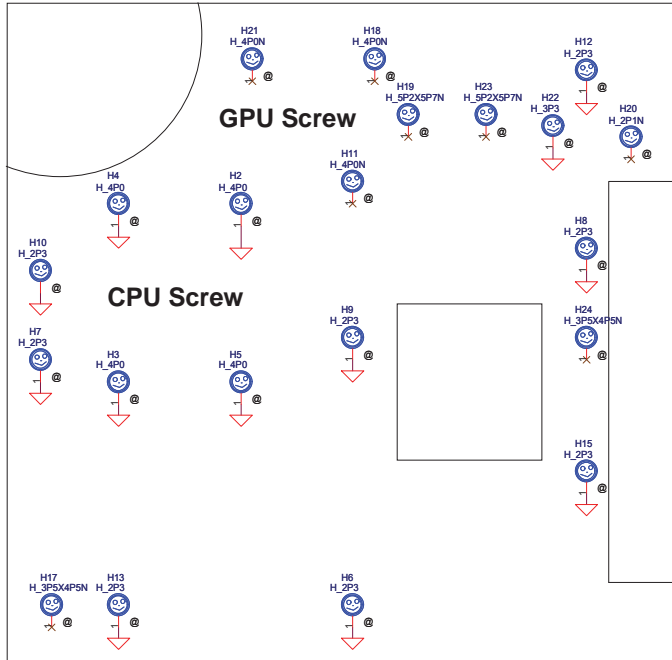
**+3VALW TO +3VALW(PCH AUX Power)**



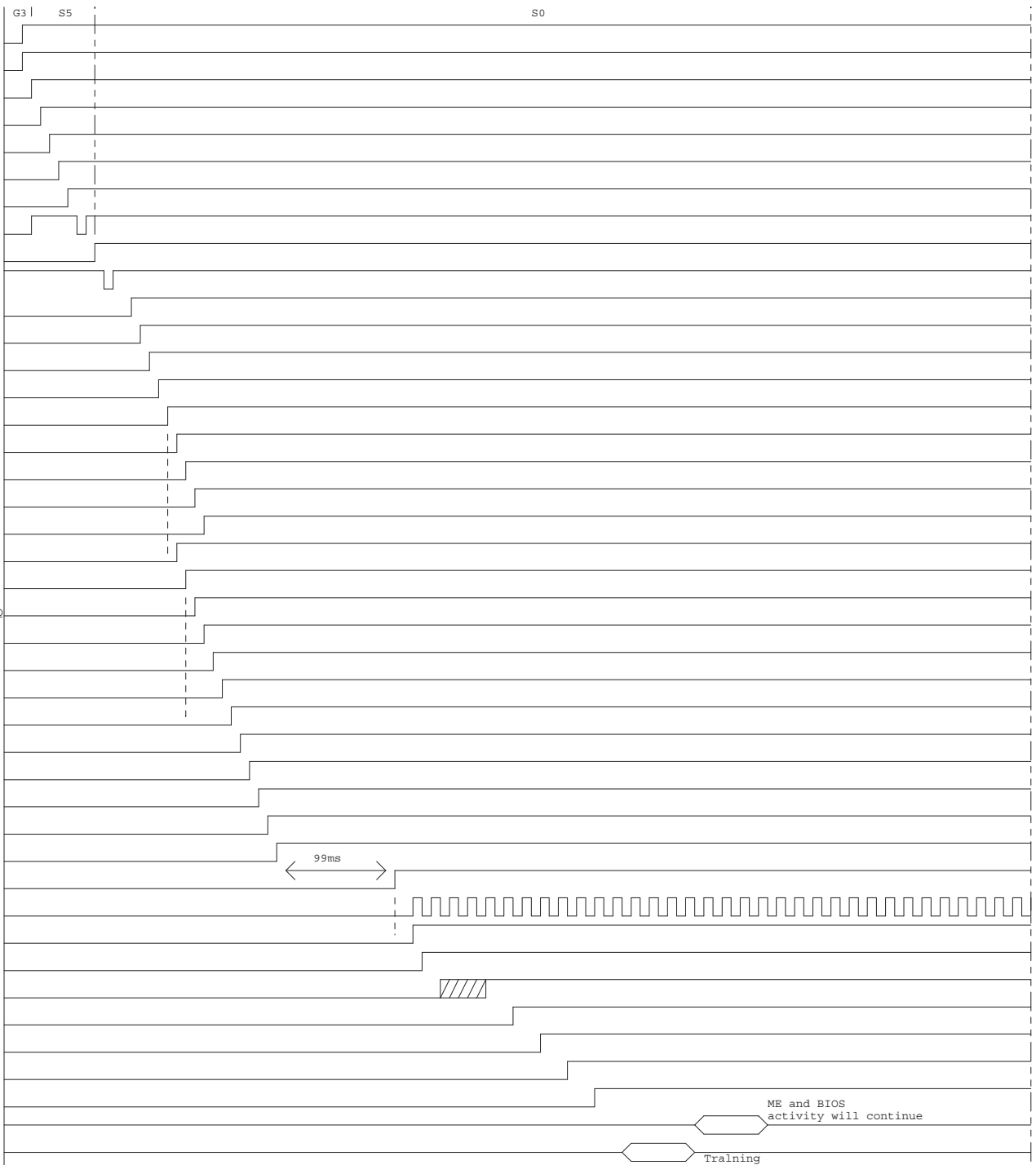
**FOR SBA Function POWER(always mount)**



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<b>Date:</b>	Tuesday, January 10, 2012	<b>Sheet</b>	42	<b>of</b>	58



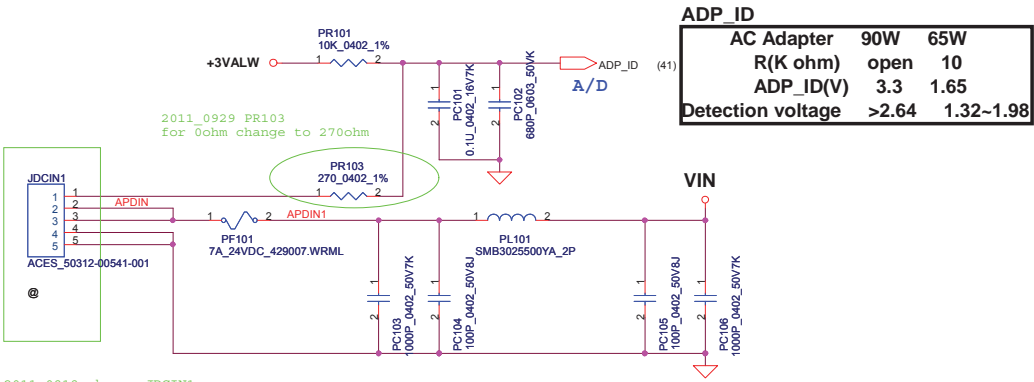
- RTC
- RTCST
- EC\_111 pin
- EC\_ON
- MAINPWON
- +5VALW
- +3VALW/VCCDSW
- ON/OFF#
- EC\_RSMRST#
- PBTN\_OUT#
- SLP\_S5#
- SLP\_S4#
- SYSON
- SYSON
- PCH\_SLPA#
- M\_PWR\_ON
- +3VM
- +1.05VM
- PCH\_APWROK
- SLP\_S3#
- SUSP#
- +1.5V\_CPU\_VDDQ
- +1.8VS
- +5VS
- +3VS
- +1.5VS
- +0.75VS
- +V1.05VS (VCCP)
- +VCCSA
- SA\_PGOOD
- VR\_ON
- PCH\_POK
- PCH\_CLKOUT
- DRAMPWROK
- H\_CPUPWRGD
- CPU\_VID
- CPU\_CORE
- VGATE
- SYS\_PWROK
- BUF\_PLT\_RST#
- SPI
- DMI



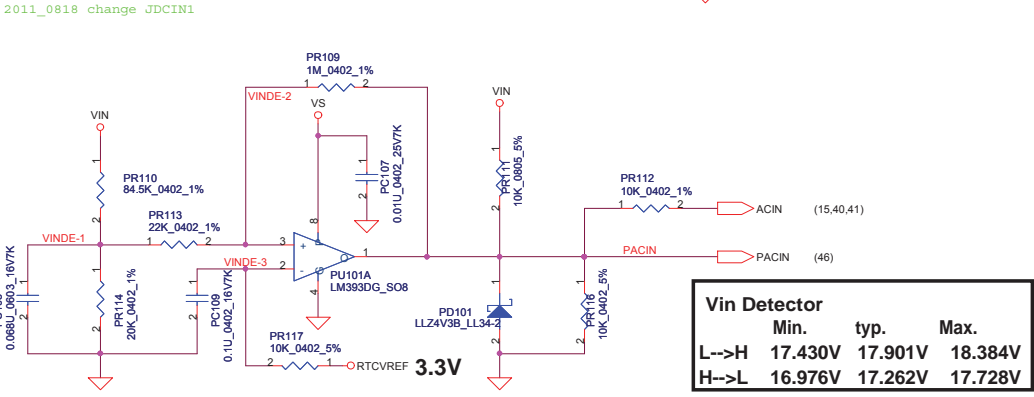
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Size	Document Number	Rev	0.6
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ME and BIOS activity will continue

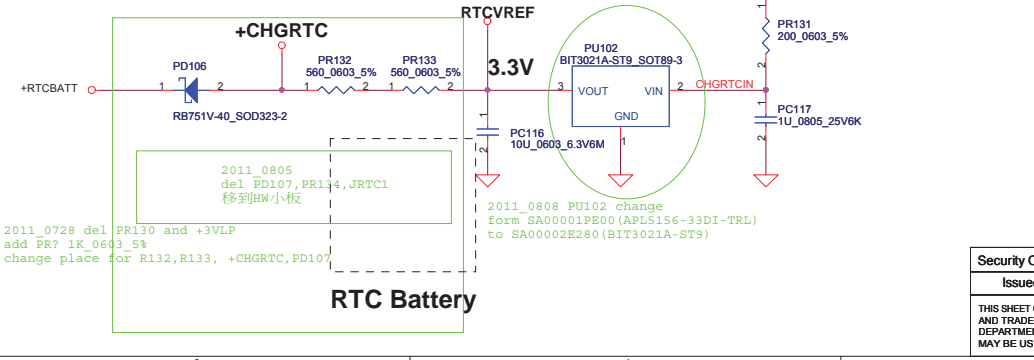
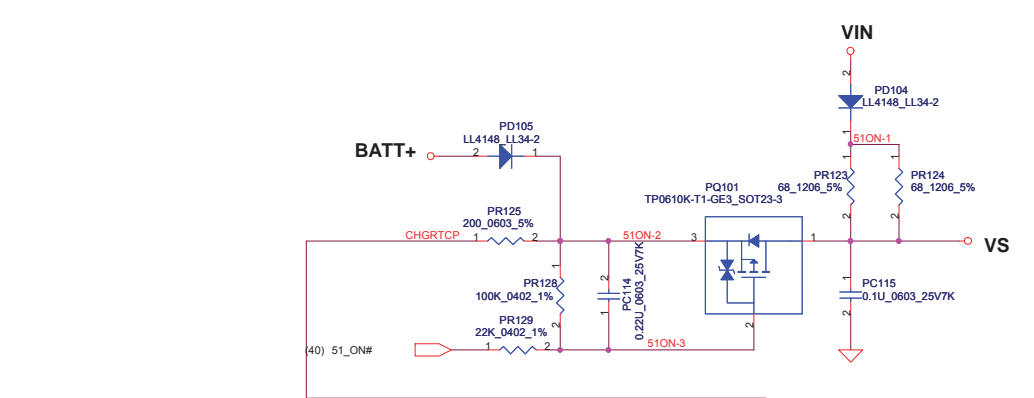
Training



ADP_ID	
AC Adapter	90W 65W
R(K ohm)	open 10
ADP_ID(V)	3.3 1.65
Detection voltage	>2.64 1.32~1.98



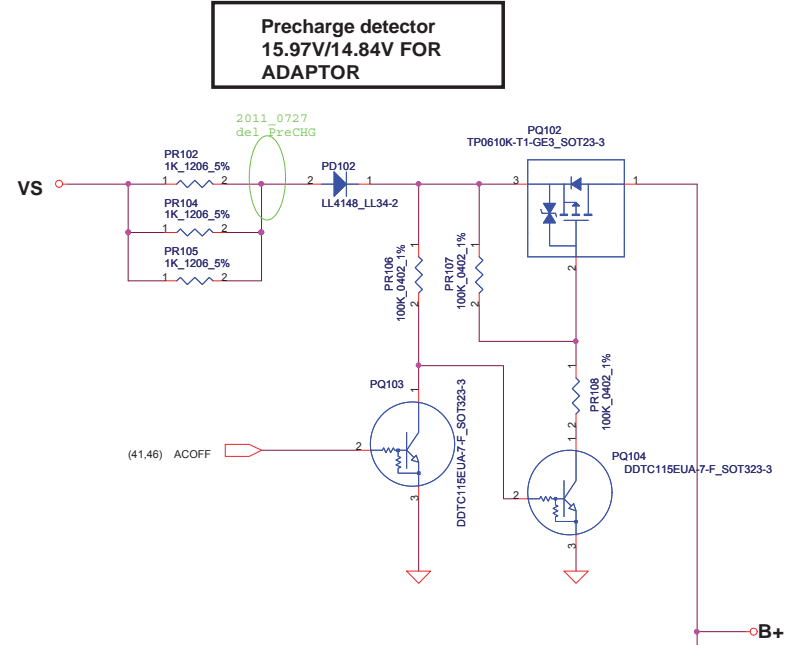
Vin Detector	
	Min. typ. Max.
L-->H	17.430V 17.901V 18.384V
H-->L	16.976V 17.262V 17.728V



2011\_0728 del PR130 and +3VLP  
add PR? 1K\_0603\_5%  
change place for R132,R133, +CHGRTC,PD107

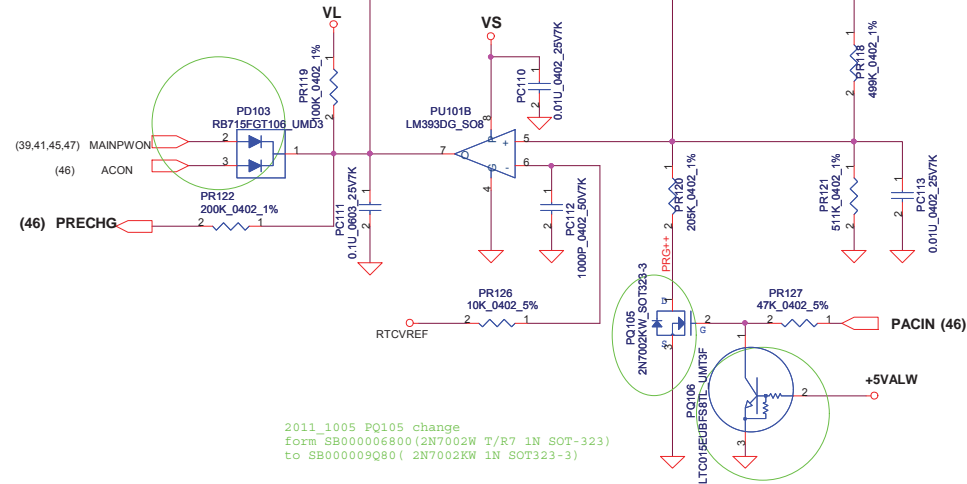
2011\_0805  
del PD107,PR134,JRTC1  
移到HW小板

2011\_0808 PU102 change  
form SA00001PE00 (APL5156-33DI-TRL)  
to SA00002E280 (BIT3021A-ST9)



Precharge detector  
15.97V/14.84V FOR  
ADAPTOR

2011\_1005 PD103 change  
form SCSB715P000 (S SCH DIO RB715P UMD3)  
to SCSB715P010 (S SCH DIO RB715FGT106 UMD3)



ACIN	
Precharge detector	
	Min. typ. Max.
L-->H	14.991V 15.381V 15.782V
H-->L	13.860V 14.247V 14.621V

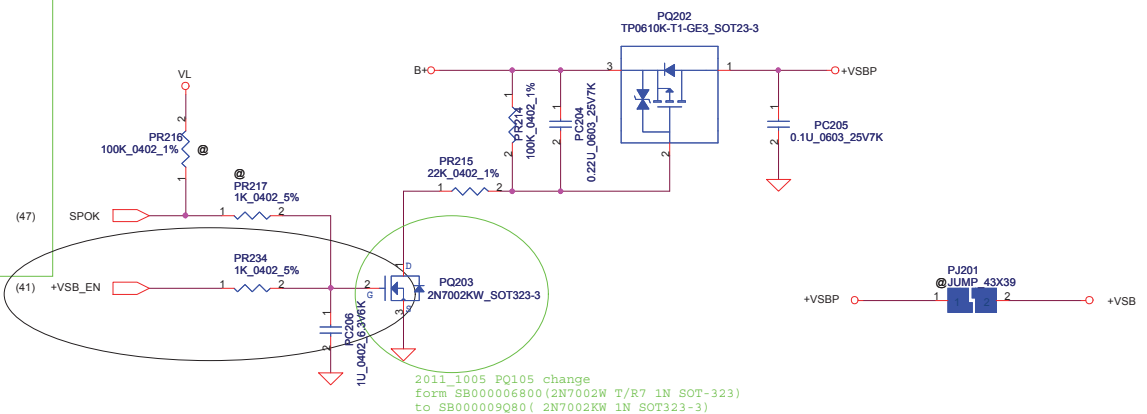
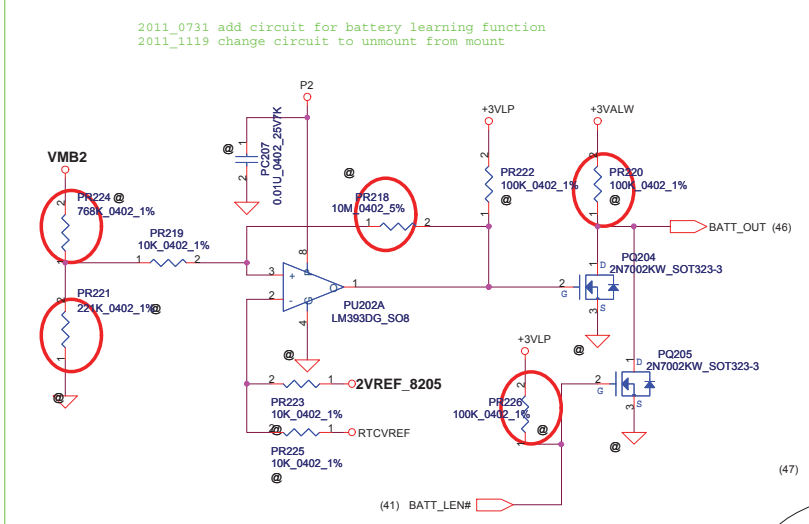
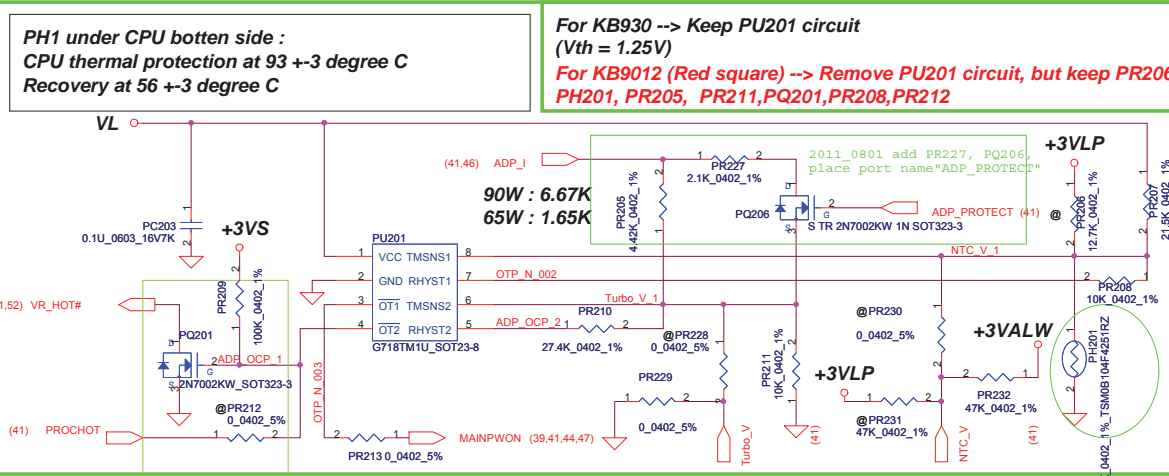
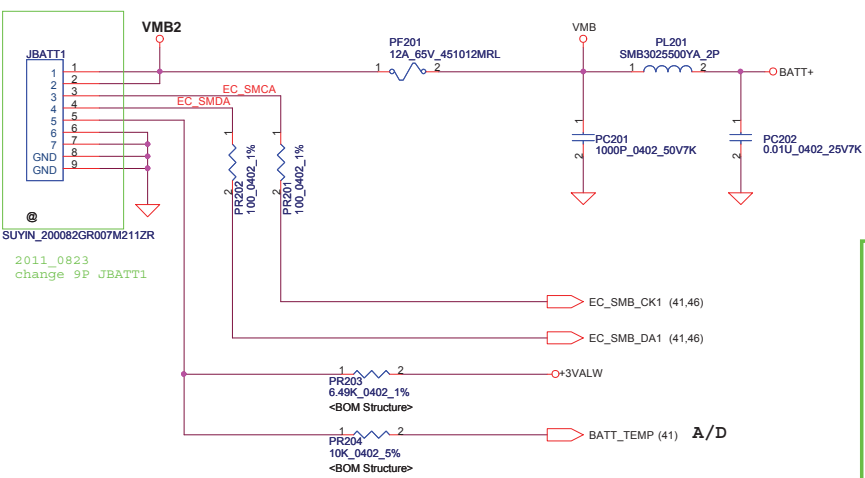
BATT ONLY	
Precharge detector	
	Min. typ. Max.
L-->H	7.196V 7.349V 7.505V
H-->L	6.138V 6.214V 6.056V

2011\_1005 PQ105 form  
SB301150000  
(S TR DTC115EUA NPN (UMT3))  
change to SB00000RM00  
(S TR LTC015EUBFS8TL NPN UMT3F)

Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date
		2012/07/01

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Compal Electronics, Inc.		
Title <b>PWR DCIN / Vin Detector /Pre-charge</b>		
Size	Document Number	Rev
Customer	<b>LA-8133P</b>	0.6
Date:	Friday, January 06, 2012	Sheet 44 of 58

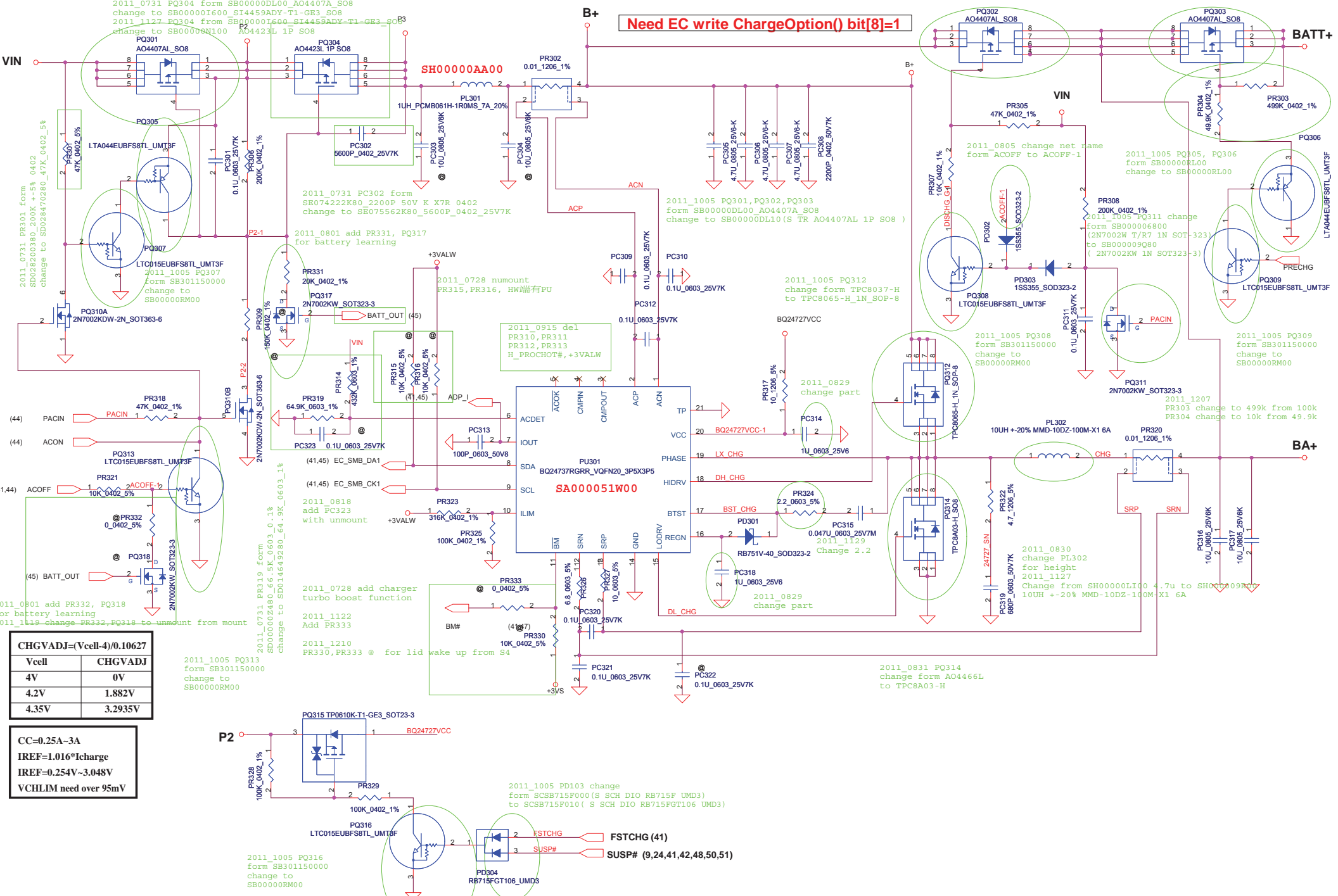


Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date
		2012/07/01

Compal Electronics, Inc.		
PWR-BATTERY CONN/OTP		
Title	LA-8133P	Rev
Size	Document Number	0.6
Customer		
Date:	Tuesday, January 10, 2012	Sheet 45 of 58

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**Need EC write ChargeOption() bit[8]=1**



**CHGVADJ=(Vcell-4)/0.10627**

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

**CC=0.25A-3A**  
**IREF=1.016\*Icharge**  
**IREF=0.254V-3.048V**  
**VCHLIM need over 95mV**

2011\_0731 PR319 form SB000002490.66 5K 0.603 0.1% change to SD014649290.64 9K 0.603 0.1%

2011\_0731 PC302 form SB074222K80.2200P 50V K X7R 0402 change to SB075562K80\_5600P\_0402\_25V7K

2011\_0801 add PR332, PQ318 for battery learning

2011\_1119 change PR332, PQ318 to unmount from mount

2011\_0801 add PR332, PQ318 for battery learning

2011\_1122 Add PR333

2011\_1210 PR330, PR333 @ for lid wake up from S4

2011\_0731 PC313 form SB301150000 change to SB00000RM00

2011\_0731 PC313 form SB074222K80.2200P 50V K X7R 0402 change to SB075562K80\_5600P\_0402\_25V7K

2011\_0801 add PR331, PQ317 for battery learning

2011\_0728 numount PR315, PR316, HW端有PU

2011\_0915 del PR310, PR311, PR312, PR313 H\_PROCHOT#, +3VALW

2011\_0829 change part

2011\_0829 change part

2011\_0830 change PL302 for height 2011\_1127 change from SH00000L100 4.7u to SH000009R00 100UH +20% MMD-10DZ-100M-X1 6A

2011\_0831 PQ314 change form AO4466L to TPC9A03-H

2011\_1005 PQ312 change form TPC8037-H to TPC8065-H\_1N\_SOP-8

2011\_1005 PQ308 form SB301150000 change to SB00000RM00

2011\_1005 PQ305, PQ306 form SB00000RL00 change to SB00000RL00

2011\_1005 PQ309 form SB301150000 change to SB00000RM00

2011\_1207 PR303 change to 499k from 100k PR304 change to 10k from 49.9k

2011\_1005 PQ311 change form SB000006800 (2N7002W T/R7 1N SOT-323) to SB000009Q80 (2N7002KW 1N SOT323-3)

2011\_0829 change part

2011\_0829 change part

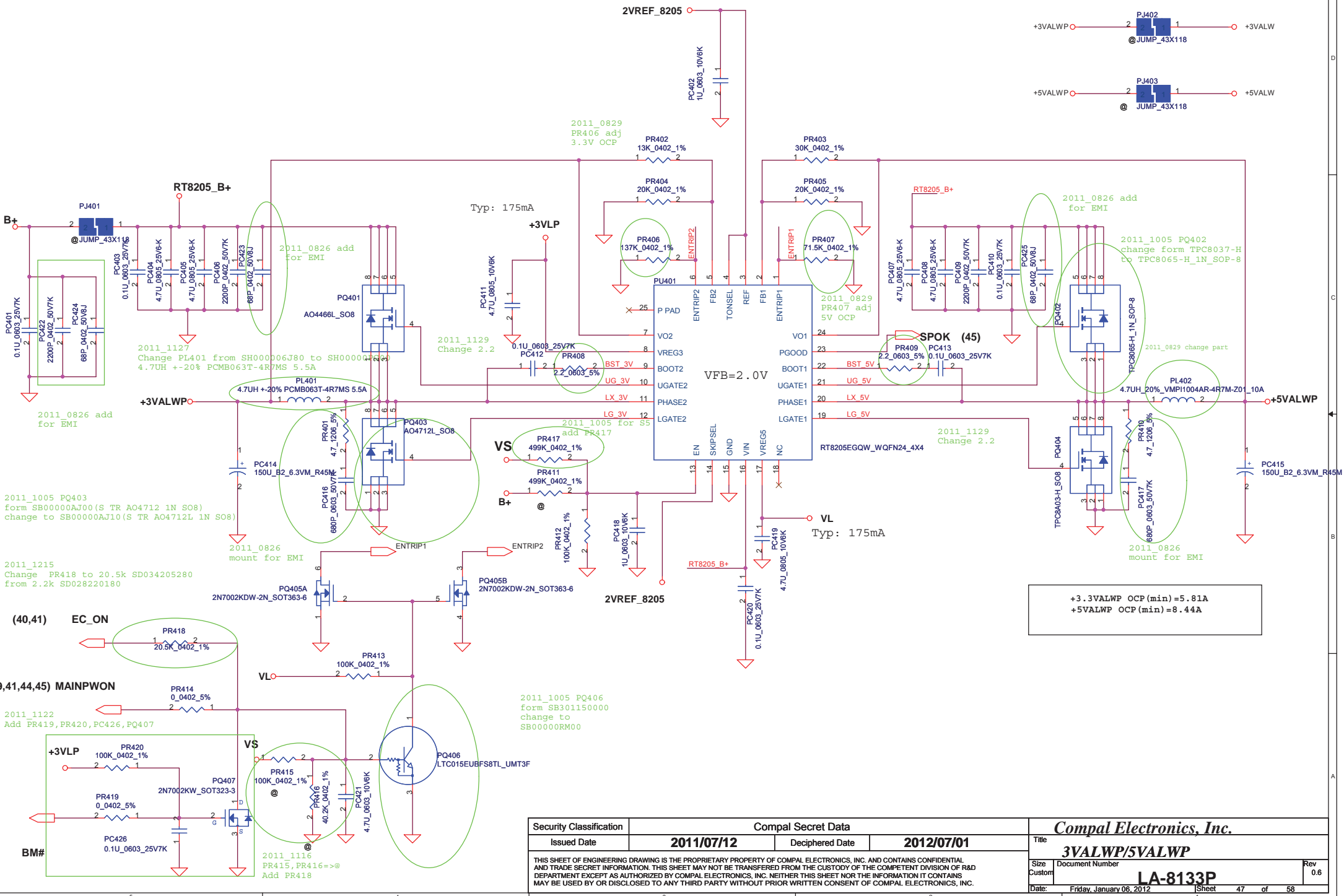
2011\_0831 PQ314 change form AO4466L to TPC9A03-H

2011\_1005 PD103 change form SCSB715P000(S SCH DIO RB715F UMD3) to SCSB715P010(S SCH DIO RB715FGT106 UMD3)

2011\_1005 PQ316 form SB301150000 change to SB00000RM00

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Size	Document Number	Date: Friday, January 06, 2012		Sheet	46 of 58	
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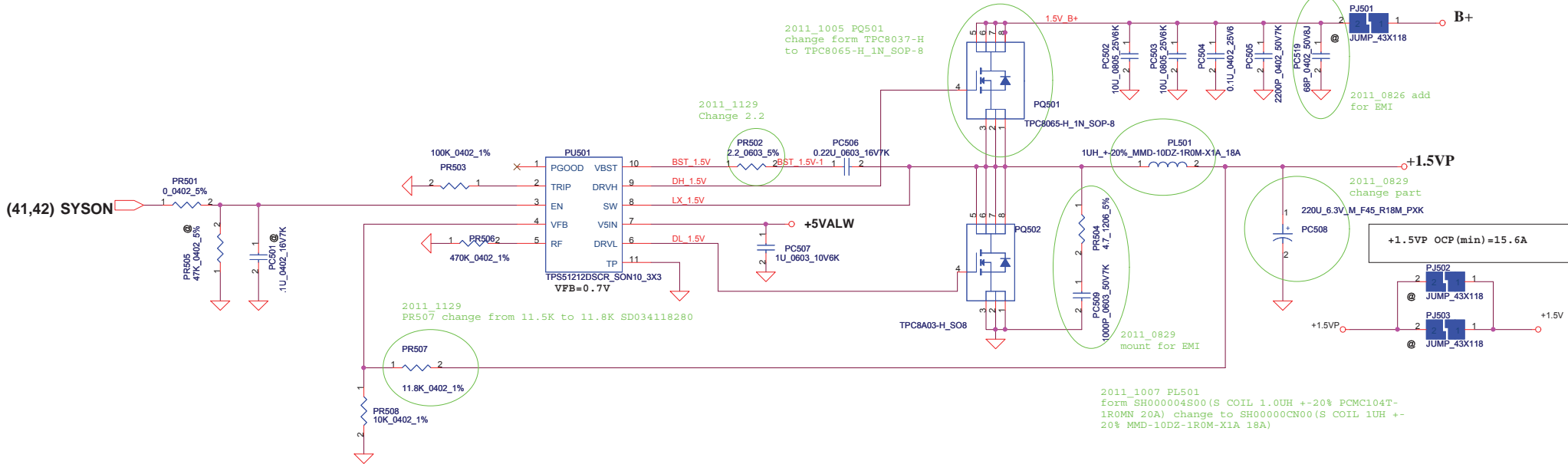
Note:  
 Use TPS51125 IC can remove RTC referenece LDO  
 Use TPS51427 IC must keep RTC referenece LDO



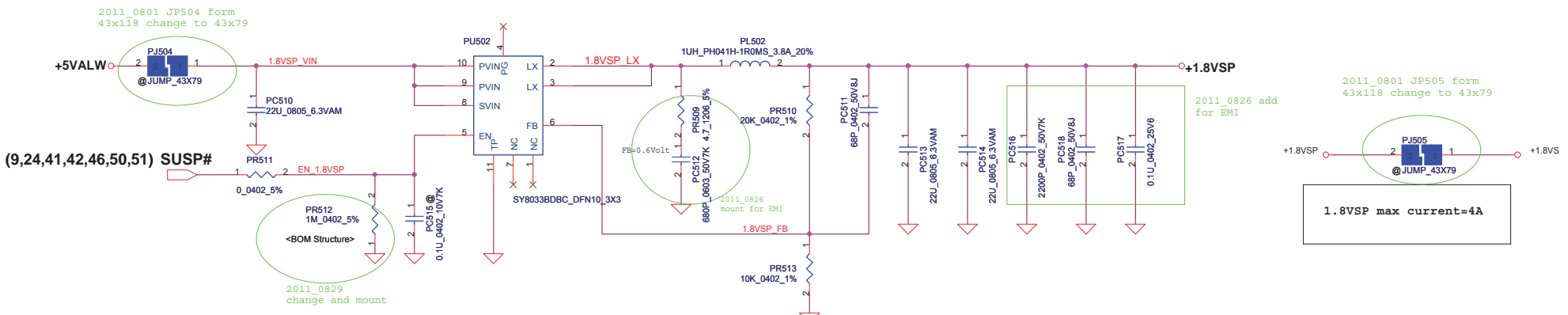
+3.3VALWP OCP (min)=5.81A  
 +5VALWP OCP (min)=8.44A

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				Rev	0.6

(41,42) SYSON



(9,24,41,42,46,50,51) SUSP#



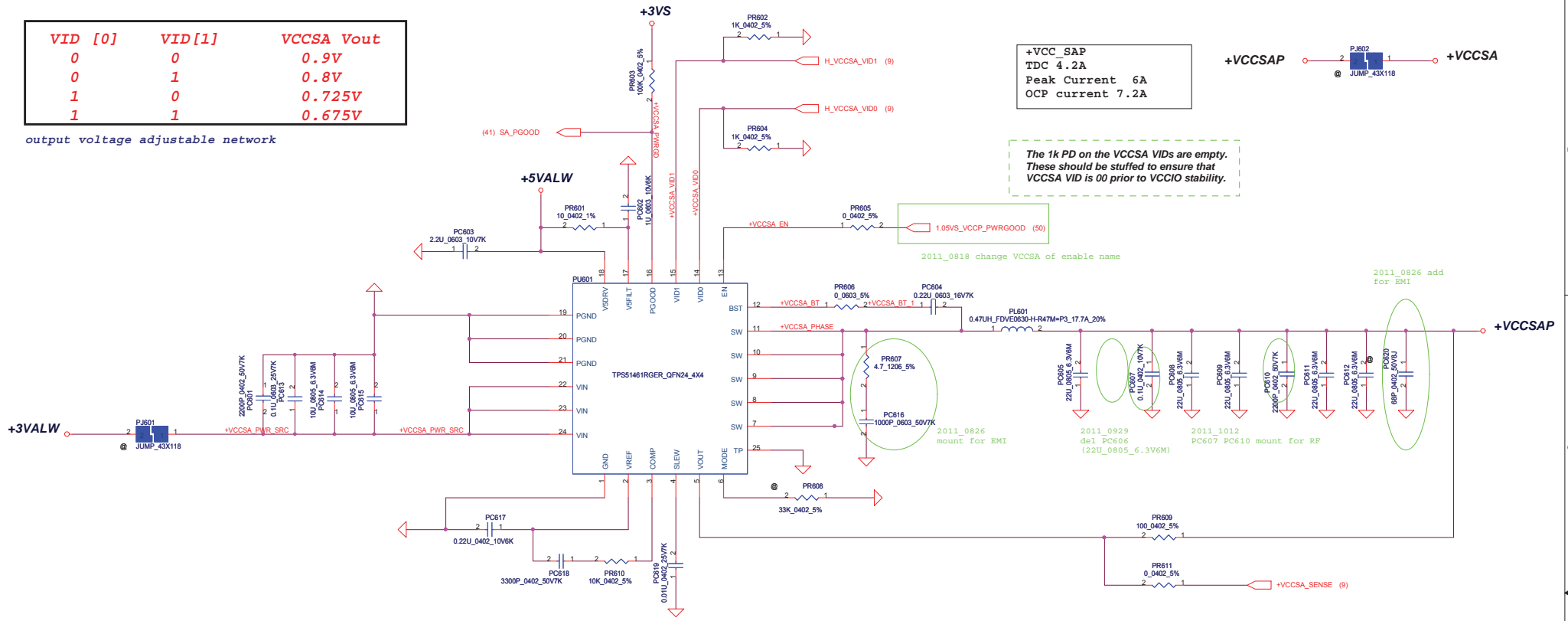
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Issued Date	2011/07/12	Deciphered Date	2012/07/01
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Compal Electronics, Inc.		
Title <b>PWR-+1.5VP/+1.8VSP</b>		
Size Custom	Document Number <b>LA-8133P</b>	Rev 0.6
Date: Friday, January 06, 2012	Sheet 48	of 58

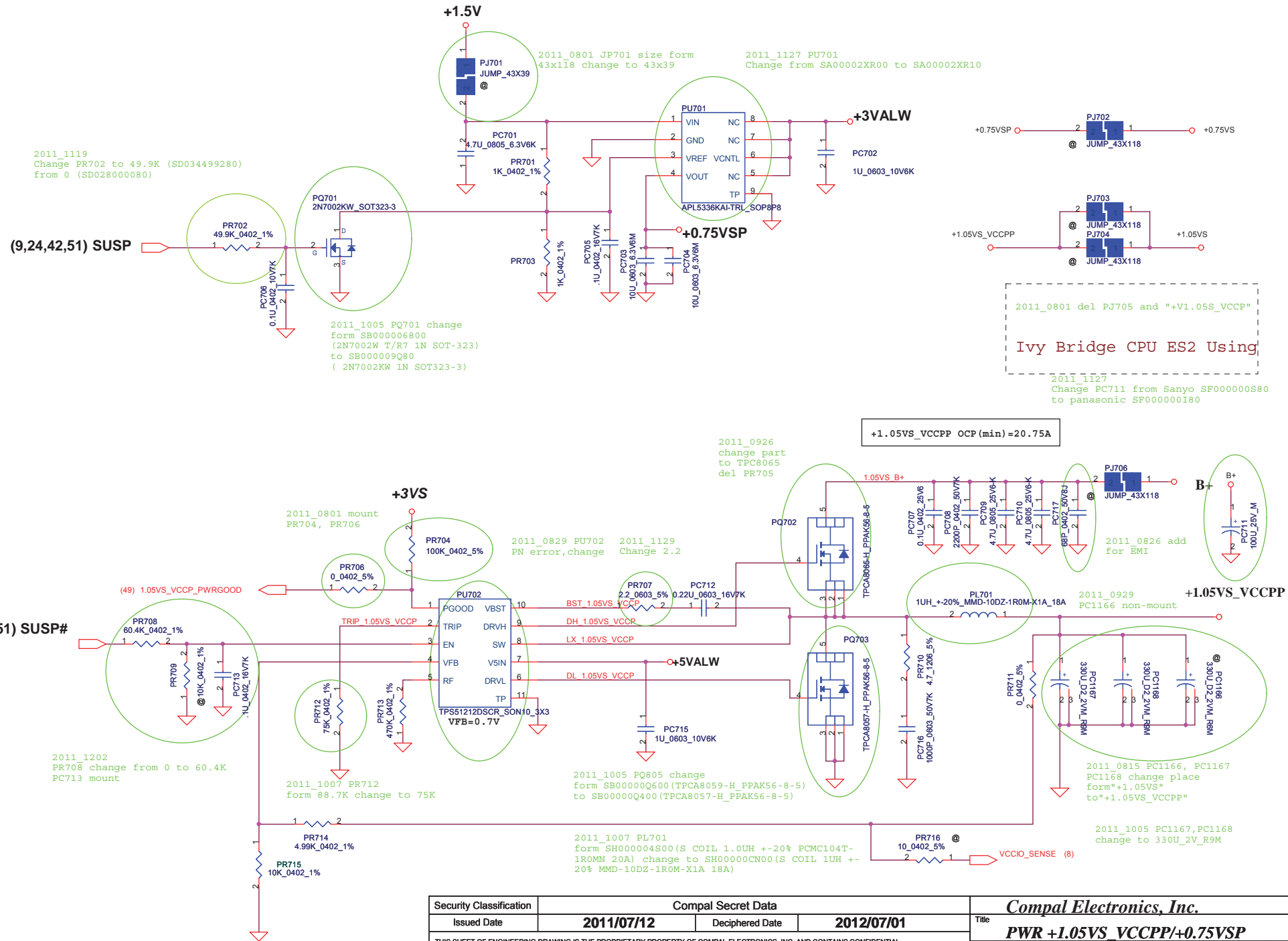


VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

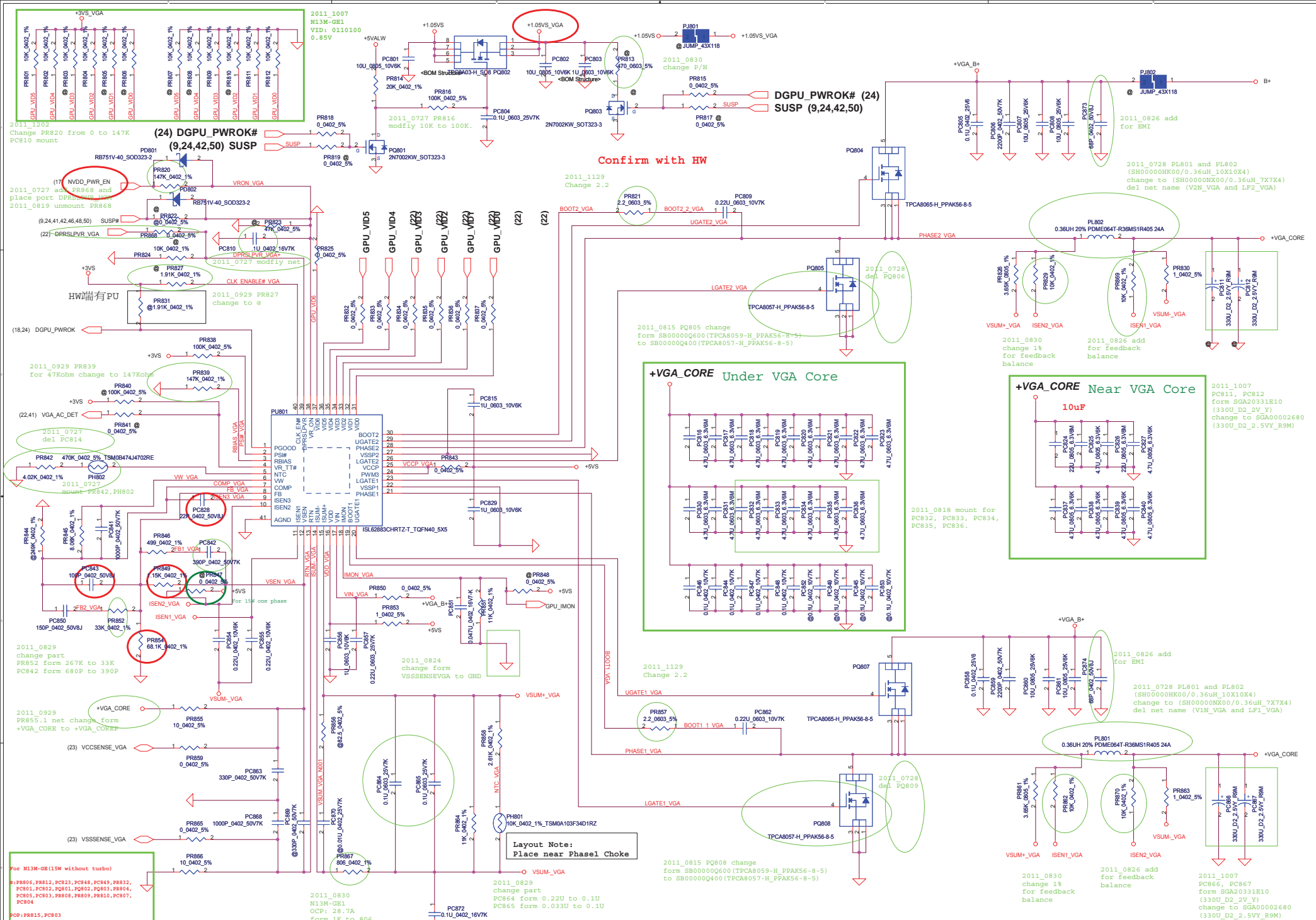
output voltage adjustable network



2011\_0801 del +V1.05S\_VCCPP circuit

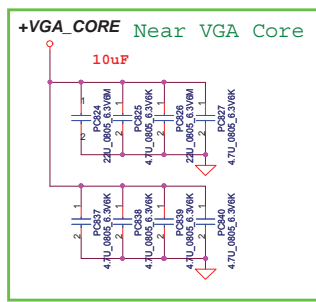
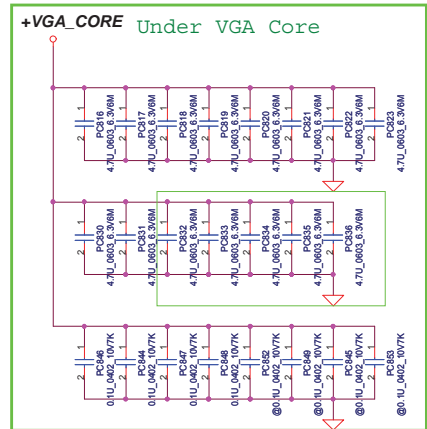


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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PWR +1.05VS_VCCPP/+0.75VSP
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				<b>LA-8133P</b>	



(24) DGPU\_PWROK# (9,24,42,50) SUSP

Confirm with HW



Layout Note:  
Place near Phase1 Choke

For N13M-GB1 (without turbo)  
 PR806->PR812, PC823, PC848, PC849, PR832,  
 PC831, PC802, PQ801, PQ802, PQ803, PR814,  
 PC805, PC803, PR808, PR809, PR810, PC807,  
 PC804  
 POP: PR815, PC803  
 PR816->120K (SD034120380)  
 PR820->1.69K (SD00002B80)  
 PR822->22K (SD03422080)  
 PR837->46K (SD03486080)  
 PC858->0.1uF (SD026104M80)  
 PC859->0.068uF (SD02608380)  
 PR850->22.1K (SD03422180)

2011\_0815 PQ808 change  
 form SB000000400 (TPCA8059-H\_PPAK56-8-5)  
 to SB000000400 (TPCA8057-H\_PPAK56-8-5)

2011\_0829  
 change part  
 PC864 form 0.22U to 0.1U  
 PC865 form 0.033U to 0.1U

2011\_0830  
 N13M-GB1  
 OCP: 28.7A  
 form 1K to 806

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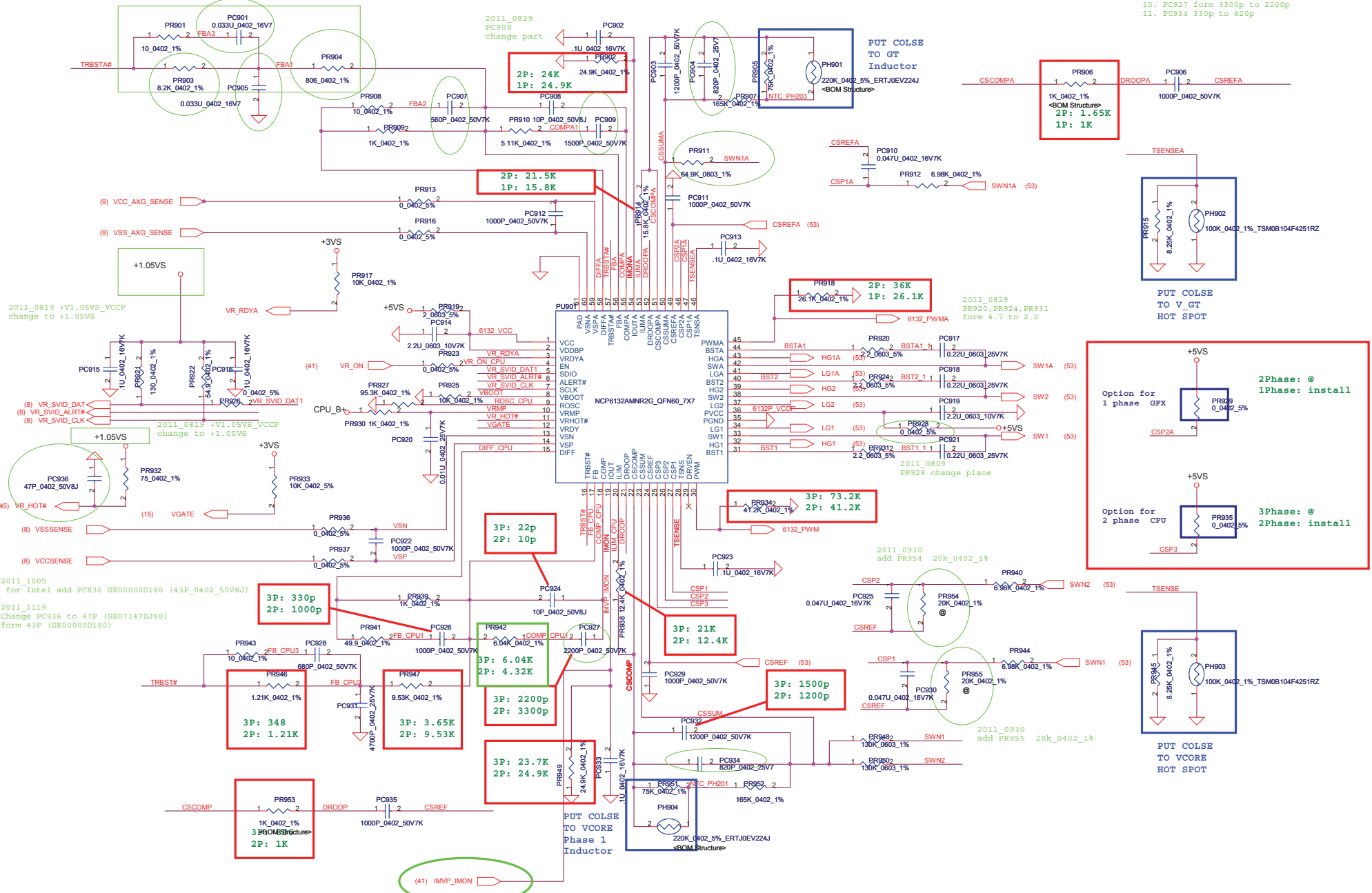
Compal Electronics, Inc.	
Title	PWR - VGA CORE
Size	Document Number LA-8131P
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2011\_0830  
PC901, PC905, PR901, PR903, PR904 mount

2011\_1119  
Change PC901, PC905 to 0.033u (SE076333K80)  
from 0.033u (SE076333KNO)

2011\_0829  
PC909  
change part

- 2011\_1007 for function test
1. modify PR903 form 1.21K to 8.2K,
  2. PC905 form 4700p to 33n,
  3. PC901 form 680p to 33n,
  4. PR904 form 10.7K to 806,
  5. PC907 form 330p to 560p
  6. PC909 form 3300p to 1500p
  7. PC904 form 330p to 820p
  8. PR911 form 63.4K to 66.5K
  9. PR942 form 4.32K to 6.04K
  10. PC927 form 3300p to 2200p
  11. PC934 330p to 820p



2011\_0819 +V1.05VS\_VCCP  
change to +1.05VS

(8) VR\_SVID\_DAT  
(8) VR\_SVID\_ALRT#  
(8) VR\_SVID\_CLK

2011\_0819 +V1.05VS\_VCCP  
change to +1.05VS

(41,45) VR\_HOT#

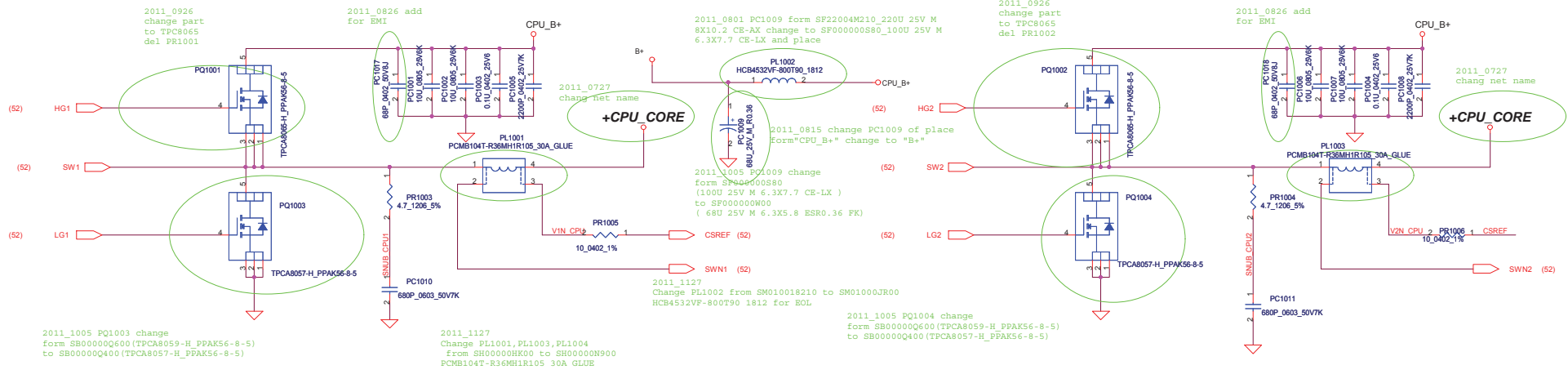
2011\_1005  
for Intel add PC836 SE00000D180 (43P\_0402\_50V8J)

2011\_1119  
Change PC936 to 47P (SE071470J80)  
form 43P (SE00000D180)

(41) IMP\_IMON

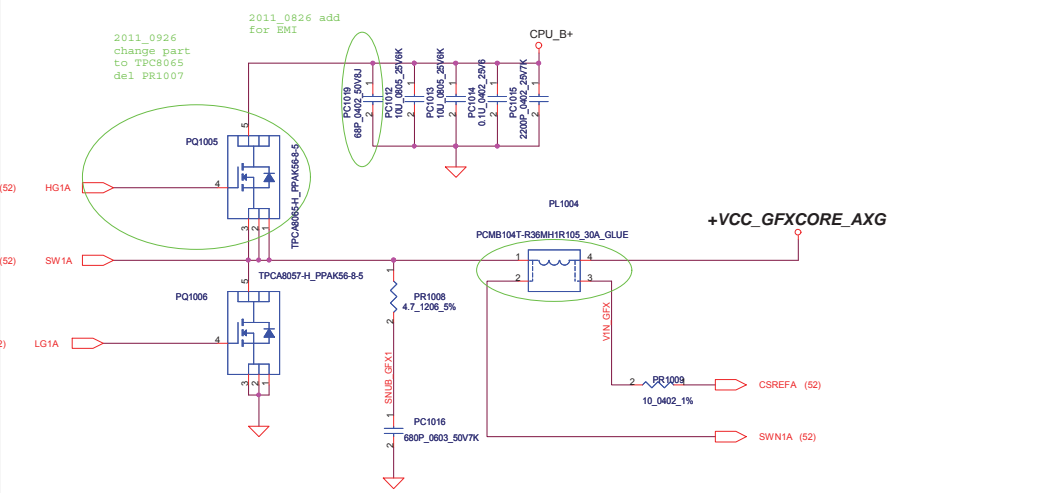
Security Classification		Compal Secret Data	
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Compal Electronics, Inc.		
Title <b>PWR-CPU_CORE1</b>		
Size Custom	Document Number <b>IA-8133P</b>	Rev 0.6
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QC 45W CPU  
VID1=0.9V  
IccMax=94A  
Icc\_Dyn=66A  
Icc\_TDC=52A  
R\_LL=1.9m ohm  
OCP-110A

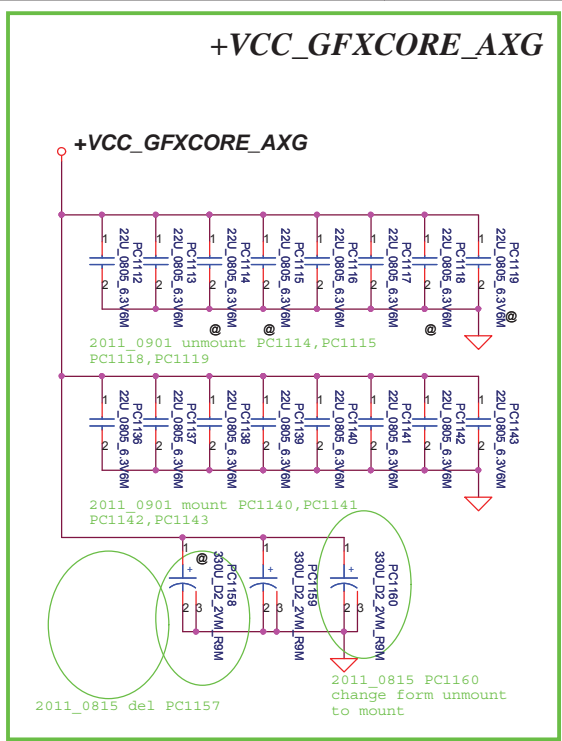
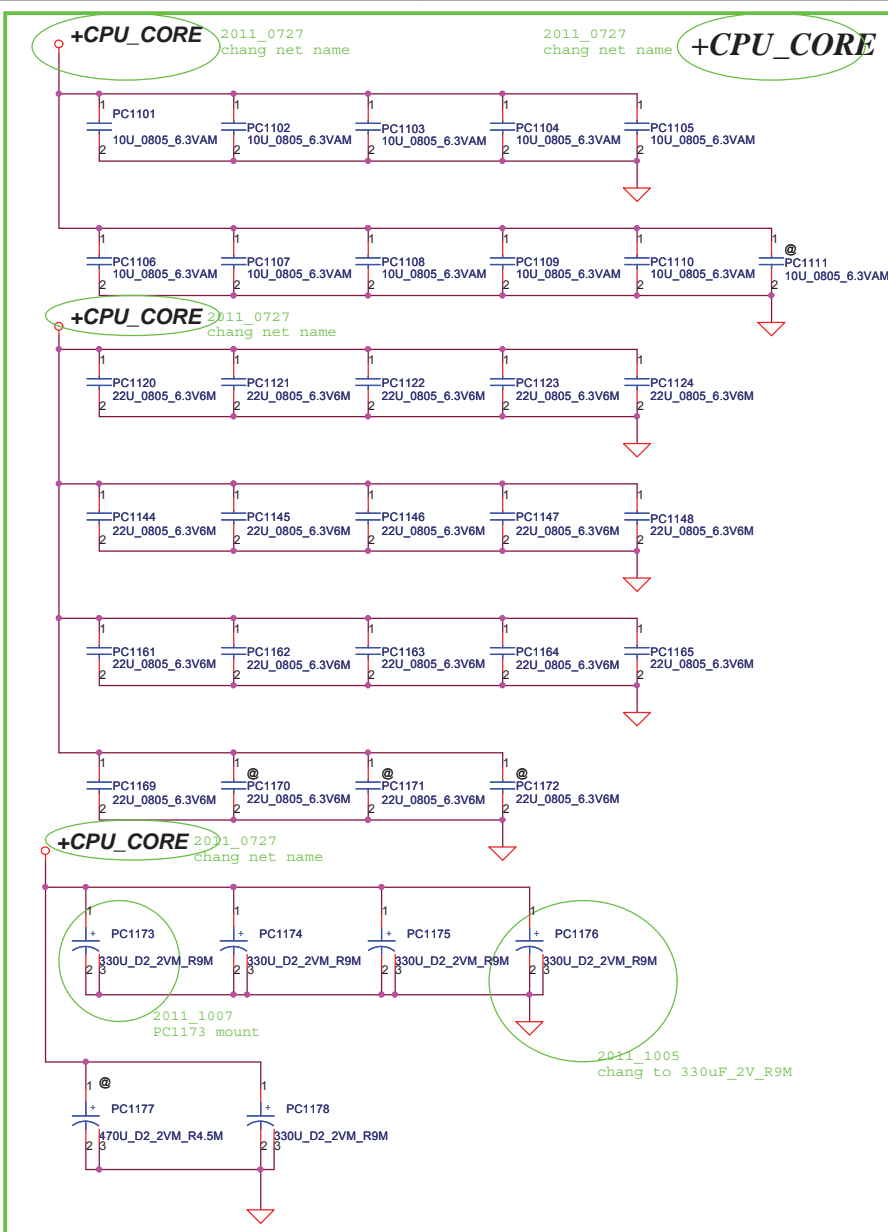
DC 35W CPU  
VID1=1.05V  
IccMax=53A  
Icc\_Dyn=43A  
Icc\_TDC=36A  
R\_LL=1.9m ohm  
OCP-65A



QC 45W GT2  
VID1=1.23V  
IccMax=46A  
Icc\_Dyn=37A  
Icc\_TDC=38A  
R\_LL=3.9m ohm  
OCP-55A

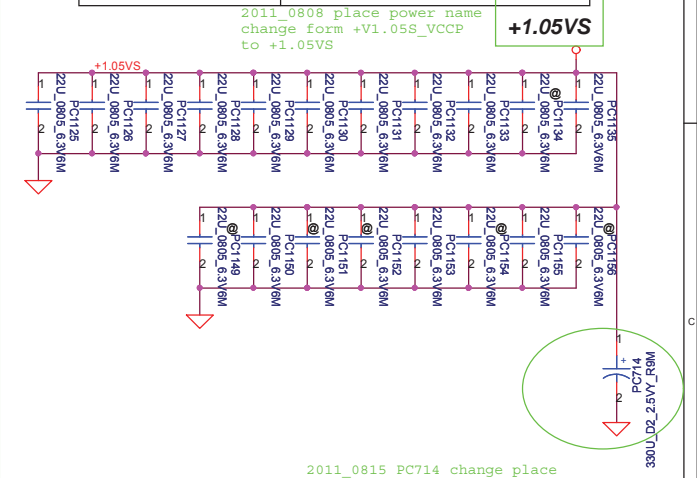
DC 35W GT2  
VID1=1.23V  
IccMax=33A  
Icc\_Dyn=20.2A  
Icc\_TDC=21.5A  
R\_LL=3.9m ohm  
OCP-40A

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Size	Document Number	LA-8133P		Rev	0.8
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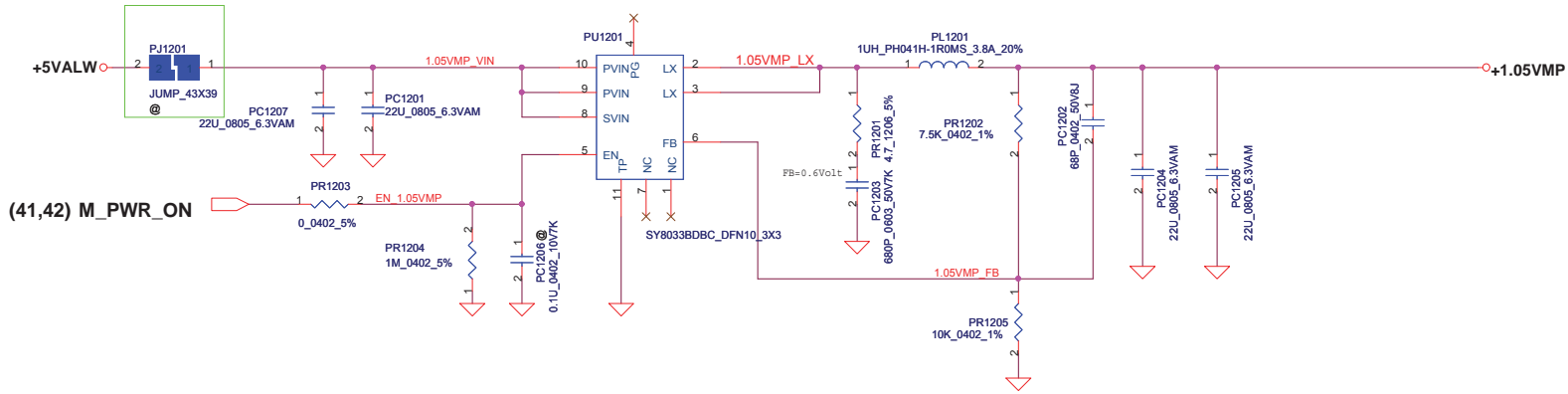
Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

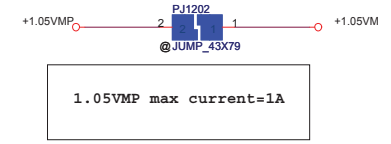


2011\_1007  
PC714  
form SGA00001Q802  
(S POLY C 330U 2V M X LESR6M SX H1.9)  
change to SGA00002680  
(330U\_D2\_2.5VY\_R9M)

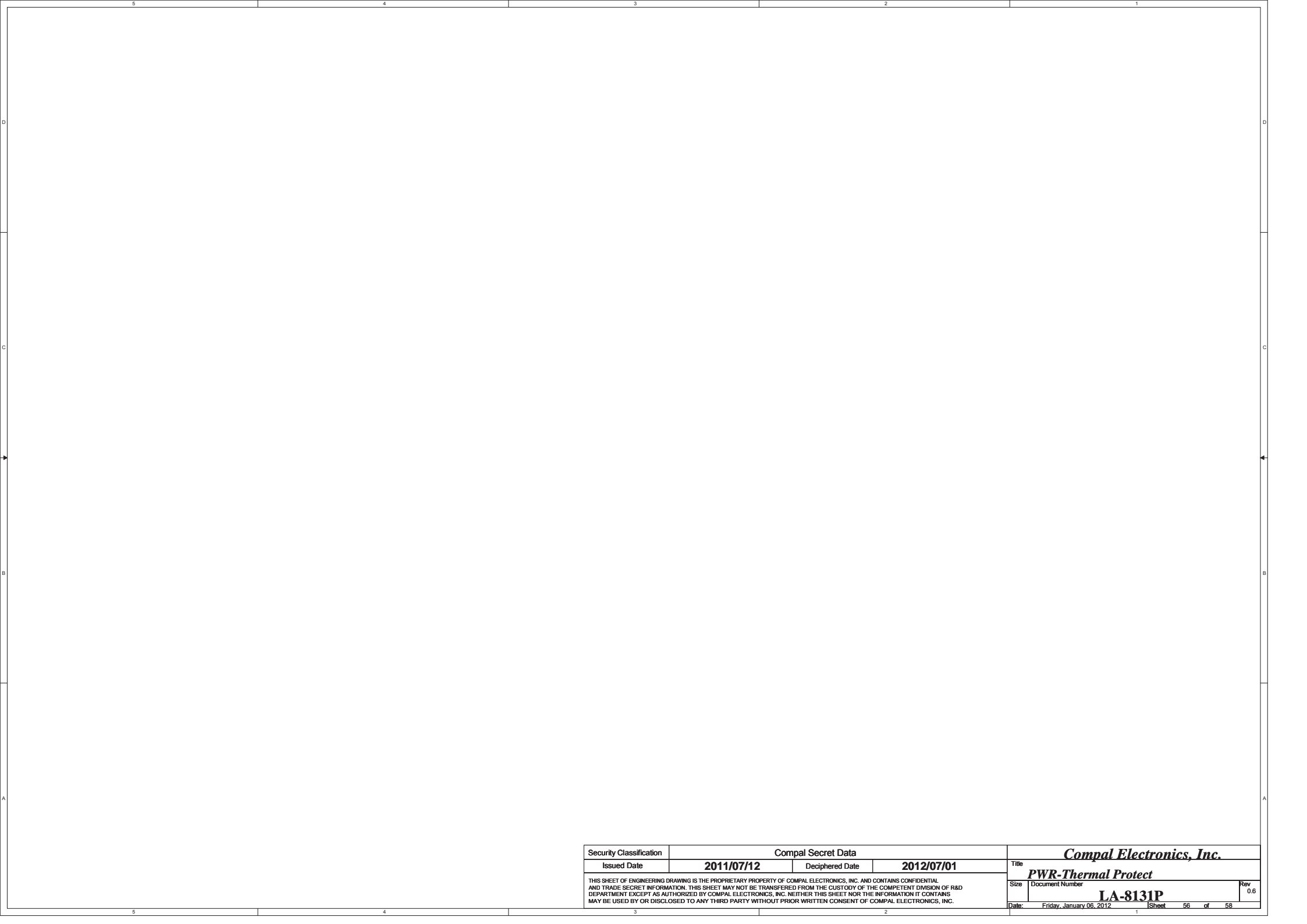
2011\_0923 JUMP form 43X79 change to 43X79



(41,42) M\_PWR\_ON



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				<i>PWR-Thermal Protect</i>					
				Size	Document Number	Rev			
					0.6				
				Date:	Friday, January 06, 2012	Sheet	56	of	58



**Version change list (P.I.R. List)**

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Date: Friday, January 06, 2012		

**Version Change List (P.I.R. List)**

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power
	2011/09/15	No2		V		Del Q2305	Del SYSON#
	2011/09/15	No3		V		Add EC pin 119(M_PWR_ON) for SBA function	Add SBA function
	2011/09/15	No4		V		Add EC pin 120(PCH_SLP#) from PCH to EC for SBA function	Add SBA function
	2011/09/15	No5		V		Add EC pin72 (Muxless_STAT) for GPU STAT	Add Muxless_STAT function
	2011/09/15	No6		V		Del PR310, PR311, PR312, PR313, net name:"H_PROCHOT#", +3VALW.	PWR-CHARGER-BQ24727
	2011/09/15	No7	V			mount PC832	
	2011/09/15	No8		V	V	Add R2482,Q2404,C2509,R2481,R2485,Q2400,R2483,C2501	AOAC Function
	2011/09/15	No9		V	V	change net name BT_OFF# to BT_ON# and change PCH EN GPIO from GPIO34 to GPIO36 R280 from @ to mount,R282 from mount to @	BT Function
	2011/09/15	No10		V	V	change net name(Mini-Express) from BT_OFF# to WLBT_OFF# PCH EN GPIO change to GPIO34	BT Function
	2011/09/19	No11		V	V	change +3VS WLAN net name to +3VS_AOAC change +3VS_WWAN net name to +3VS_AOAC	AOAC Function
	2011/09/19	No12		V	V	Del R1010 for LVDS CONN plug high voltage	LVDS CONN
	2011/09/19	No13		V	V	R1102,R1104,R1105 from @ to mount fix MIC(ECR97236)issue	MIC function
	2011/09/19	No14		V	V	Add R2470 for 80 port function	80 port function
	2011/09/19	No15		V	V	Del R2476 Add Q2405	BT Function
	2011/09/20	No16		V	V	Add power schematic 9/15 again modify RF PC423, PC425, PC519, PC620, PC717, PC573, PC574, PC424, PC518, PC1017, PC1018, PC1019, PC422, PC516, PC517 modify POWER在VGA的PWM IC 加的零件PR869, PR870	
	2011/09/22	No17		V	V	Add U10,CS89,C645 for TPM function	TPM function
	2011/09/22	No18		V	V	Add R110,R112 for SPI POWER choose(SBA function)	
	2011/09/23	No19		V	V	modify power page 44-57(PJ1201 JUMP form 43X79 change to 43X79)	
	2011/09/26	No20		V	V	change CPU footprint from TYCO 2013620-2 989P-T to TYCO 2013620-2 989P-T-A39 change PCH footprint from PANTHER-POINT_FCBGA_989P-T to PANTHER-POINT_FCBGA_989P-T-A39 change GPU footprint N13P-PES-A1_FCBGA_908P to N13P-PES-A1_FCBGA_908P-A39 change VRAM footprint K4W1G1646E-HC12_FBGA_96P to K4W1G1646E-HC12_FBGA_96P-A39	
	2011/09/26	No21		V	V	change PCH_GPIO24(R288) pull up to +3V_PCH	
	2011/09/26	No22		V	V	change P18 (R311,R330,R286,R329) for UMA and Optimus memon	
	2011/09/26	No23		V	V	change net name PCH_THRMTRIP#_R to VGA_THRMTRIP#	
	2011/09/26	No24		V	V	PQ702 change to TPC8065,Del PR705 PQ1001,PQ1002,PQ1005 change to TPC8065,Del PR1001,PR1002,PR1007	
	2011/09/26	No25		V	V	p43 change Q2304 dual channel 2n7002 to single channel Q2304,Q2305(Q2305 @) p43 change Q2306 dual channel 2n7002 to single channel Q2306,Q2311(Q2311 @)	
	2011/09/27	No27	V			modify EC Board ID R2213 to 18K	
	2011/09/27	No28		V	V	net name CX_GPIO0 connect to U1101 pin 38	
	2011/09/27	No29		V	V	Add C2152,C2153,D2113 for ESD	
	2011/09/27	No30		V	V	change NVIDIA N13M ROM_SCLK from 15K PU to 5K PU	
	2011/09/27	No31		V	V	change ESD part D2401,D2403,D2405 power from +SVALW to +USB VCCA	
	2011/09/27	No32		V	V	Add C2108 for GPU_CLKREQA	
	2011/09/27	No33		V	V	Add Q2406 , modify R2401,Change PCH_GPIO19 to ODD_DET#,for zero power ODD	
	2011/09/27	No34		V	V	change WLBT_OFF# to PCH_GPIO34	
	2011/09/27	No35		V	V	change PCH_GPIO34 to WLBT_OFF#(mini card pin5)	
	2011/09/27	No36		V	V	change BT_ON# connect to WLBT_OFF#(mini card pin51)	
	2011/09/28	No37		V	V	C76 , R1123 , c1131 , R2201,C2209 C84,C85 from @ to mount for RF team	
	2011/09/29	No38		V	V	R1529 change to 15K	
	2011/09/29	No39		V	V	Add CONN JDB3 fo debug	
	2011/09/29	No40		V	V	Add R2460,R2438,R2471,R2472,R2475,R2476 for PS8520B	
	2011/09/29	No41		V	V	change D2403 ,D2401 power to +USB_VCCB,and del D2403 ,D2401,D2405 Pin3 net	
	2011/09/29	No42		V	V	change power schematic del PC606 (22U_0805_6.3V6M) PR855:1 net change form +VGA_CORE to +VGA_COREP PR827 mount change to @ (non-mount) PR839 for 47Kohm change to 147Kohm PR103 for 0ohm change to 270ohm PC1166 non-mount,PC1173 non-mount,PC1158 non-mount	
	2011/09/29	No44		V	V	Add Q2313,C2305,C2306,C2307,C2308,R2318,R2320,R2320,C2322 for +3V_PCH change CRT CONN to DC061109231(footprint pin modify) Add PR954,PR955	
	2011/09/29	No45		V	V	Add H16,H27 change Q2304,Q2305 to Q2304 modify PTH H11,H18 ,H21 Del T10 for SUS_STAT(SLP_S3# 走不出来)	
	2011/10/04	No46		V	V	reserve R352,R353 for SATA re-drive PS-8131B change net name from WLBT_OFF to WLBT_OFF_5# modify PCH_GPIO34 connect to BT_ON# for BT module modify PCH_GPIO36 from BT_ON# connect to WLBT_OFF_51# for mini card BT combo module change Q2301 to 2N7002	
	2011/10/05	No47		V	V	Del R2469,T49,T45,T41,T37,T36,T28,T26 for ME 限高0 changer power net +3VS_FP to +3VS update power schematics P44-P57	
	2011/10/06	No48		V	V	change Q1202 part to SB000007H10. change JCARD1 FN to SP02000H810 footprint: ACES_87213-1400G_14P change some CONN part NO. for ME CONN list Add D2416	

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