QFKAA

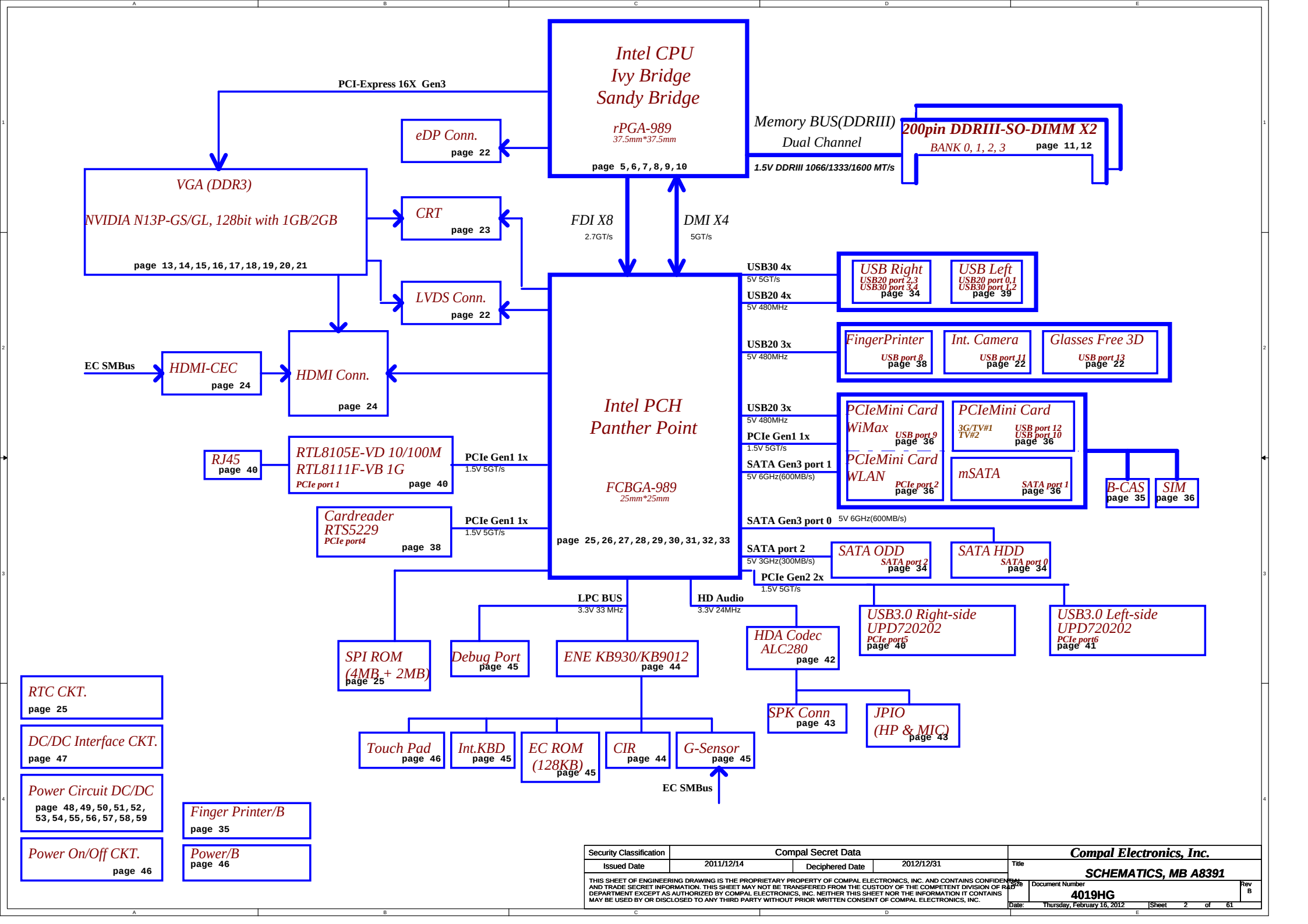
Yosemite 10FG

LA-8391P REV 1.0 Schematic

Intel Processor(Ivy Bridge / Sandy Bridge)
PCH(Panther Point)
2012-02-02 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.		
Title: *SCHEMATICS, MB A8391*		
Size: Custom	Document Number: 4019HG	Rev: B
Date: Thursday, February 16, 2012	Sheet 1 of 61	



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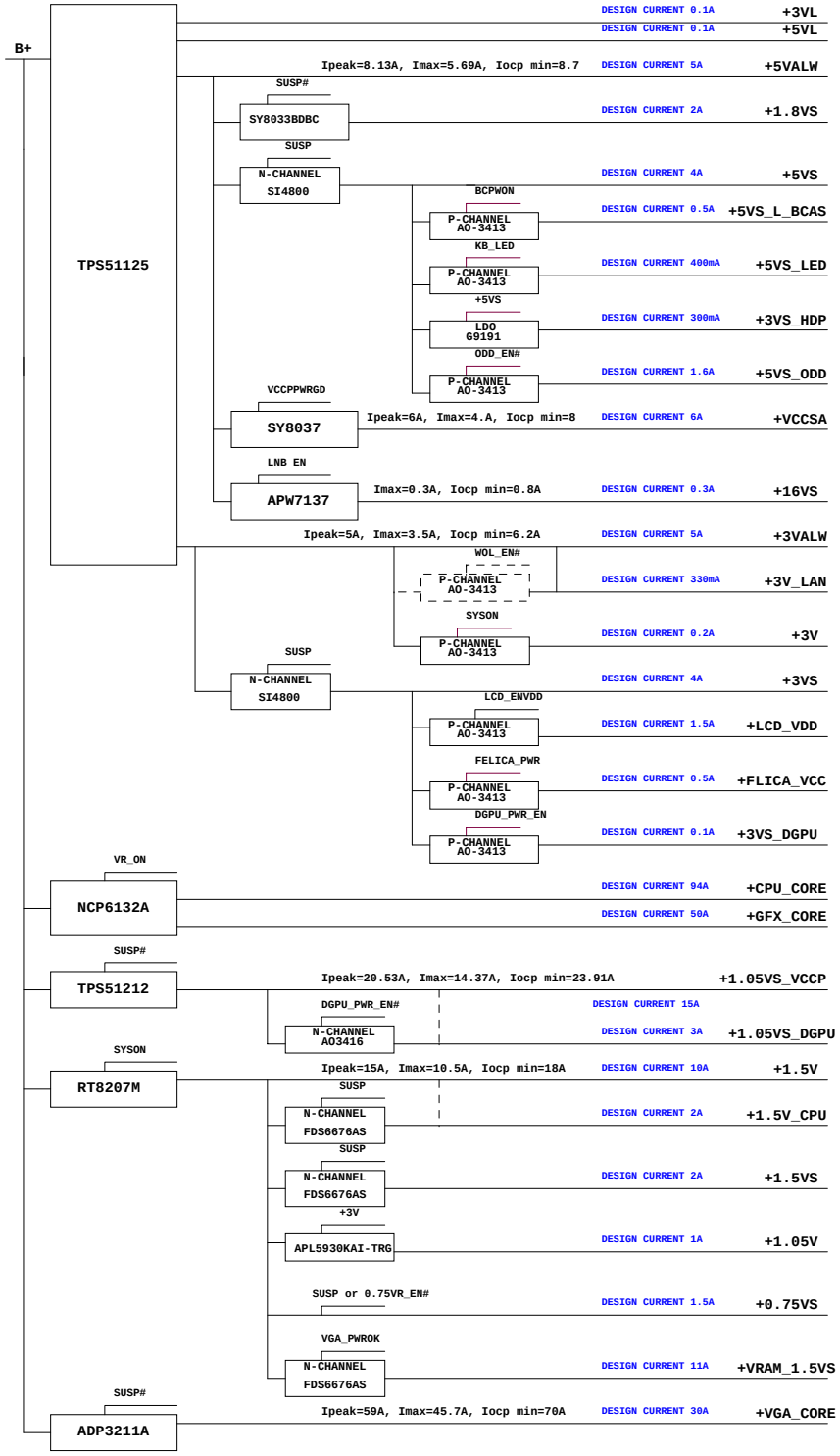
Date: Thursday, February 16, 2012 | Sheet 2 of 61



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Size: | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 3 of 61

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b

Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b

Platform	SKU	CPU	PCH	VGA
Calpella	Discrete (DIS@)	Clarksfield/ Arrandale	HM76@/HM77@	N13PGSR1@/N13PGLR1@
	Optimus (OPT@)	Arrandale	HM76@/HM77@	N13PGSR1@/N13PGLR1@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	CIR@	KBL@

Function	G-SENSOR	SKU		LVDS			Camera & Mic
description	G-SENSOR	SKU		2D HD/FHD Panel	2D HD eDP	3D Panel	Camera & Mic
explain	G-SENSOR	Discrete	Optimus	Optimus	Optimus	Discrete	Camera & Mic
BTO	GSENSOR@	DIS@	OPT@	LVDS2D@	OPTFHD@	IEDP@	3D@	CAM@

Function	GPU		
description	N13P-GS	N13P-GL	
explain	N13PGS	N13PGL	
BTO	N13PGSR1@	N13PGLR1@	

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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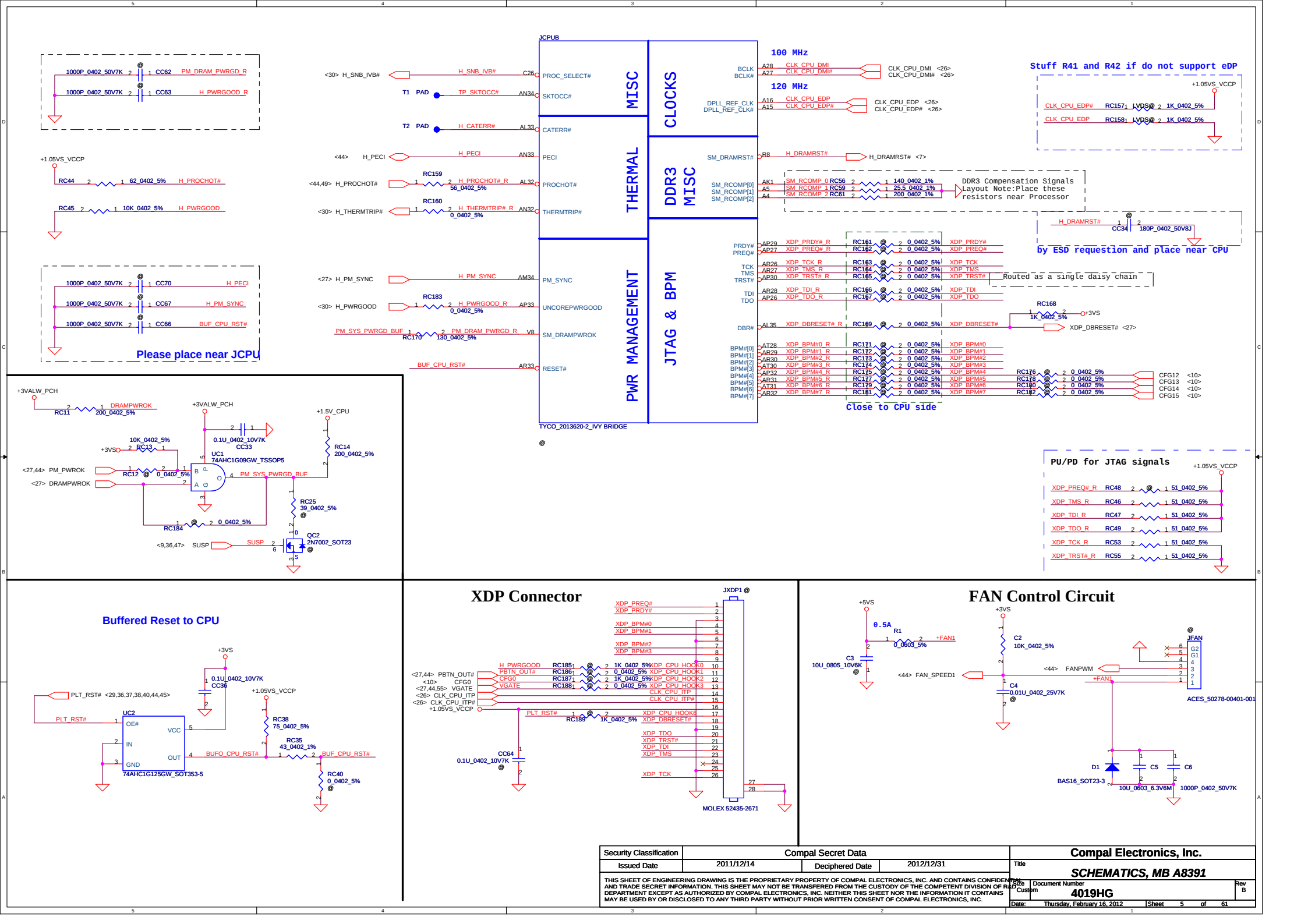
Size: Custom | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 4 of 61



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Custom	4019HG		B
Date:	Thursday, February 16, 2012	Sheet	5 of 61

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

+1.05VS_VCCP
RC1 24.9_0402_1%

JCPUA

PEG_ICOMPI J22 — PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

DMI
<27> DMI_PTX_CRX_N0 — DMI_PTX_CRX_N0 B27 — DMI_RX#[0]
<27> DMI_PTX_CRX_N1 — DMI_PTX_CRX_N1 B25 — DMI_RX#[1]
<27> DMI_PTX_CRX_N2 — DMI_PTX_CRX_N2 A25 — DMI_RX#[2]
<27> DMI_PTX_CRX_N3 — DMI_PTX_CRX_N3 B24 — DMI_RX#[3]
<27> DMI_PTX_CRX_P0 — DMI_PTX_CRX_P0 B28 — DMI_RX[0]
<27> DMI_PTX_CRX_P1 — DMI_PTX_CRX_P1 B26 — DMI_RX[1]
<27> DMI_PTX_CRX_P2 — DMI_PTX_CRX_P2 A24 — DMI_RX[2]
<27> DMI_PTX_CRX_P3 — DMI_PTX_CRX_P3 B23 — DMI_RX[3]
<27> DMI_CTX_PRX_N0 — DMI_CTX_PRX_N0 G21 — DMI_TX#[0]
<27> DMI_CTX_PRX_N1 — DMI_CTX_PRX_N1 E22 — DMI_TX#[1]
<27> DMI_CTX_PRX_N2 — DMI_CTX_PRX_N2 F21 — DMI_TX#[2]
<27> DMI_CTX_PRX_N3 — DMI_CTX_PRX_N3 D21 — DMI_TX#[3]
<27> DMI_CTX_PRX_P0 — DMI_CTX_PRX_P0 G22 — DMI_TX[0]
<27> DMI_CTX_PRX_P1 — DMI_CTX_PRX_P1 D22 — DMI_TX[1]
<27> DMI_CTX_PRX_P2 — DMI_CTX_PRX_P2 F20 — DMI_TX[2]
<27> DMI_CTX_PRX_P3 — DMI_CTX_PRX_P3 C21 — DMI_TX[3]

Intel(R) FDI
<27> FDI_CTX_PRX_N0 — FDI_CTX_PRX_N0 A21 — FDI0_TX#[0]
<27> FDI_CTX_PRX_N1 — FDI_CTX_PRX_N1 H19 — FDI0_TX#[1]
<27> FDI_CTX_PRX_N2 — FDI_CTX_PRX_N2 E19 — FDI0_TX#[2]
<27> FDI_CTX_PRX_N3 — FDI_CTX_PRX_N3 F18 — FDI0_TX#[3]
<27> FDI_CTX_PRX_N4 — FDI_CTX_PRX_N4 B21 — FDI1_TX#[0]
<27> FDI_CTX_PRX_N5 — FDI_CTX_PRX_N5 C20 — FDI1_TX#[1]
<27> FDI_CTX_PRX_N6 — FDI_CTX_PRX_N6 D18 — FDI1_TX#[2]
<27> FDI_CTX_PRX_N7 — FDI_CTX_PRX_N7 E17 — FDI1_TX#[3]
<27> FDI_CTX_PRX_P0 — FDI_CTX_PRX_P0 A22 — FDI0_TX[0]
<27> FDI_CTX_PRX_P1 — FDI_CTX_PRX_P1 G19 — FDI0_TX[1]
<27> FDI_CTX_PRX_P2 — FDI_CTX_PRX_P2 E20 — FDI0_TX[2]
<27> FDI_CTX_PRX_P3 — FDI_CTX_PRX_P3 G18 — FDI0_TX[3]
<27> FDI_CTX_PRX_P4 — FDI_CTX_PRX_P4 B20 — FDI1_TX[0]
<27> FDI_CTX_PRX_P5 — FDI_CTX_PRX_P5 C19 — FDI1_TX[1]
<27> FDI_CTX_PRX_P6 — FDI_CTX_PRX_P6 D19 — FDI1_TX[2]
<27> FDI_CTX_PRX_P7 — FDI_CTX_PRX_P7 F17 — FDI1_TX[3]
<27> FDI_FSYNC0 — FDI_FSYNC0 J18 — FDI0_FSYNC
<27> FDI_FSYNC1 — FDI_FSYNC1 J17 — FDI1_FSYNC
<27> FDI_INT — FDI_INT H20 — FDI_INT
<27> FDI_LSYNC0 — FDI_LSYNC0 J19 — FDI0_LSYNC
<27> FDI_LSYNC1 — FDI_LSYNC1 H17 — FDI1_LSYNC

eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

+1.05VS_VCCP — RC2 24.9_0402_1% — EDP_COMP A18 — eDP_COMPIO
H_EDP_HPD# B16 — eDP_HPD#
<22> H_EDP_AUXP — C15 — eDP_AUX
<22> H_EDP_AUXN — D15 — eDP_AUX#
<22> H_EDP_TXP0 — C17 — eDP_TX[0]
<22> H_EDP_TXP1 — F16 — eDP_TX[1]
C16 — eDP_TX[2]
G15 — eDP_TX[3]
<22> H_EDP_TXN0 — C18 — eDP_TX#[0]
<22> H_EDP_TXN1 — E16 — eDP_TX#[1]
D16 — eDP_TX#[2]
F15 — eDP_TX#[3]

eDP
TYCO_2013620-2_IVY BRIDGE
@

PCI EXPRESS* - GRAPHICS

PEG_RX#[0] K33 PCIE_GTX_C_CRX_N0
PEG_RX#[1] M35 PCIE_GTX_C_CRX_N1
PEG_RX#[2] L34 PCIE_GTX_C_CRX_N2
PEG_RX#[3] J35 PCIE_GTX_C_CRX_N3
PEG_RX#[4] J32 PCIE_GTX_C_CRX_N4
PEG_RX#[5] H34 PCIE_GTX_C_CRX_N5
PEG_RX#[6] H31 PCIE_GTX_C_CRX_N6
PEG_RX#[7] G33 PCIE_GTX_C_CRX_N7
PEG_RX#[8] G30 PCIE_GTX_C_CRX_N8
PEG_RX#[9] F35 PCIE_GTX_C_CRX_N9
PEG_RX#[10] E34 PCIE_GTX_C_CRX_N10
PEG_RX#[11] E32 PCIE_GTX_C_CRX_N11
PEG_RX#[12] D33 PCIE_GTX_C_CRX_N12
PEG_RX#[13] D31 PCIE_GTX_C_CRX_N13
PEG_RX#[14] B33 PCIE_GTX_C_CRX_N14
PEG_RX#[15] C32 PCIE_GTX_C_CRX_N15
→ PCIE_GTX_C_CRX_N[0..15] <13>

PEG_RX[0] J33 PCIE_GTX_C_CRX_P0
PEG_RX[1] L35 PCIE_GTX_C_CRX_P1
PEG_RX[2] K34 PCIE_GTX_C_CRX_P2
PEG_RX[3] H35 PCIE_GTX_C_CRX_P3
PEG_RX[4] H32 PCIE_GTX_C_CRX_P4
PEG_RX[5] G34 PCIE_GTX_C_CRX_P5
PEG_RX[6] G31 PCIE_GTX_C_CRX_P6
PEG_RX[7] F33 PCIE_GTX_C_CRX_P7
PEG_RX[8] F30 PCIE_GTX_C_CRX_P8
PEG_RX[9] E35 PCIE_GTX_C_CRX_P9
PEG_RX[10] E33 PCIE_GTX_C_CRX_P10
PEG_RX[11] F32 PCIE_GTX_C_CRX_P11
PEG_RX[12] D34 PCIE_GTX_C_CRX_P12
PEG_RX[13] E31 PCIE_GTX_C_CRX_P13
PEG_RX[14] C33 PCIE_GTX_C_CRX_P14
PEG_RX[15] B32 PCIE_GTX_C_CRX_P15
→ PCIE_GTX_C_CRX_P[0..15] <13>

PEG_TX#[0] M29 PCIE_CTX_GRX_N0 — CC9 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N0
PEG_TX#[1] M32 PCIE_CTX_GRX_N1 — CC11 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N1
PEG_TX#[2] M31 PCIE_CTX_GRX_N2 — CC16 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N2
PEG_TX#[3] L32 PCIE_CTX_GRX_N3 — CC20 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N3
PEG_TX#[4] L29 PCIE_CTX_GRX_N4 — CC27 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N4
PEG_TX#[5] K31 PCIE_CTX_GRX_N5 — CC30 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N5
PEG_TX#[6] K28 PCIE_CTX_GRX_N6 — CC1 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N6
PEG_TX#[7] J30 PCIE_CTX_GRX_N7 — CC4 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N7
PEG_TX#[8] J28 PCIE_CTX_GRX_N8 — CC15 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N8
PEG_TX#[9] H29 PCIE_CTX_GRX_N9 — CC18 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N9
PEG_TX#[10] G27 PCIE_CTX_GRX_N10 — CC22 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N10
PEG_TX#[11] E29 PCIE_CTX_GRX_N11 — CC24 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N11
PEG_TX#[12] F27 PCIE_CTX_GRX_N12 — CC29 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N12
PEG_TX#[13] D28 PCIE_CTX_GRX_N13 — CC26 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N13
PEG_TX#[14] F26 PCIE_CTX_GRX_N14 — CC3 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N14
PEG_TX#[15] E25 PCIE_CTX_GRX_N15 — CC32 0.22U_0402_16V7K — PCIE_CTX_C_GRX_N15
→ PCIE_CTX_C_GRX_N[0..15] <13>

PEG_TX[0] M28 PCIE_CTX_GRX_P0 — CC10 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P0
PEG_TX[1] M33 PCIE_CTX_GRX_P1 — CC5 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P1
PEG_TX[2] M30 PCIE_CTX_GRX_P2 — CC6 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P2
PEG_TX[3] L31 PCIE_CTX_GRX_P3 — CC7 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P3
PEG_TX[4] L28 PCIE_CTX_GRX_P4 — CC12 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P4
PEG_TX[5] K30 PCIE_CTX_GRX_P5 — CC9 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P5
PEG_TX[6] K27 PCIE_CTX_GRX_P6 — CC19 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P6
PEG_TX[7] J29 PCIE_CTX_GRX_P7 — CC14 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P7
PEG_TX[8] J27 PCIE_CTX_GRX_P8 — CC13 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P8
PEG_TX[9] H28 PCIE_CTX_GRX_P9 — CC17 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P9
PEG_TX[10] G28 PCIE_CTX_GRX_P10 — CC21 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P10
PEG_TX[11] E28 PCIE_CTX_GRX_P11 — CC23 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P11
PEG_TX[12] F28 PCIE_CTX_GRX_P12 — CC28 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P12
PEG_TX[13] D27 PCIE_CTX_GRX_P13 — CC25 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P13
PEG_TX[14] E26 PCIE_CTX_GRX_P14 — CC2 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P14
PEG_TX[15] D25 PCIE_CTX_GRX_P15 — CC31 0.22U_0402_16V7K — PCIE_CTX_C_GRX_P15
→ PCIE_CTX_C_GRX_P[0..15] <13>

	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	180 nF~265 nF
NV N13X	Gen1/2/3	Suggest 220 nF

Close to CPU

FDI_INT — DIS@ RC191 1K_0402_5%
FDI_FSYNC0 — DIS@ RC192 1K_0402_5%
FDI_FSYNC1 — DIS@ RC193 1K_0402_5%
FDI_LSYNC0 — DIS@ RC194 1K_0402_5%
FDI_LSYNC1 — DIS@ RC195 1K_0402_5%

+1.05VS_VCCP — RC3 1K_0402_5% — H_EDP_HPD#
<22> CPU_EDP_HPD — 2N7002_SOT23-3 QC1 IEDP@
IEDP@ RC4 100K_0402_5%

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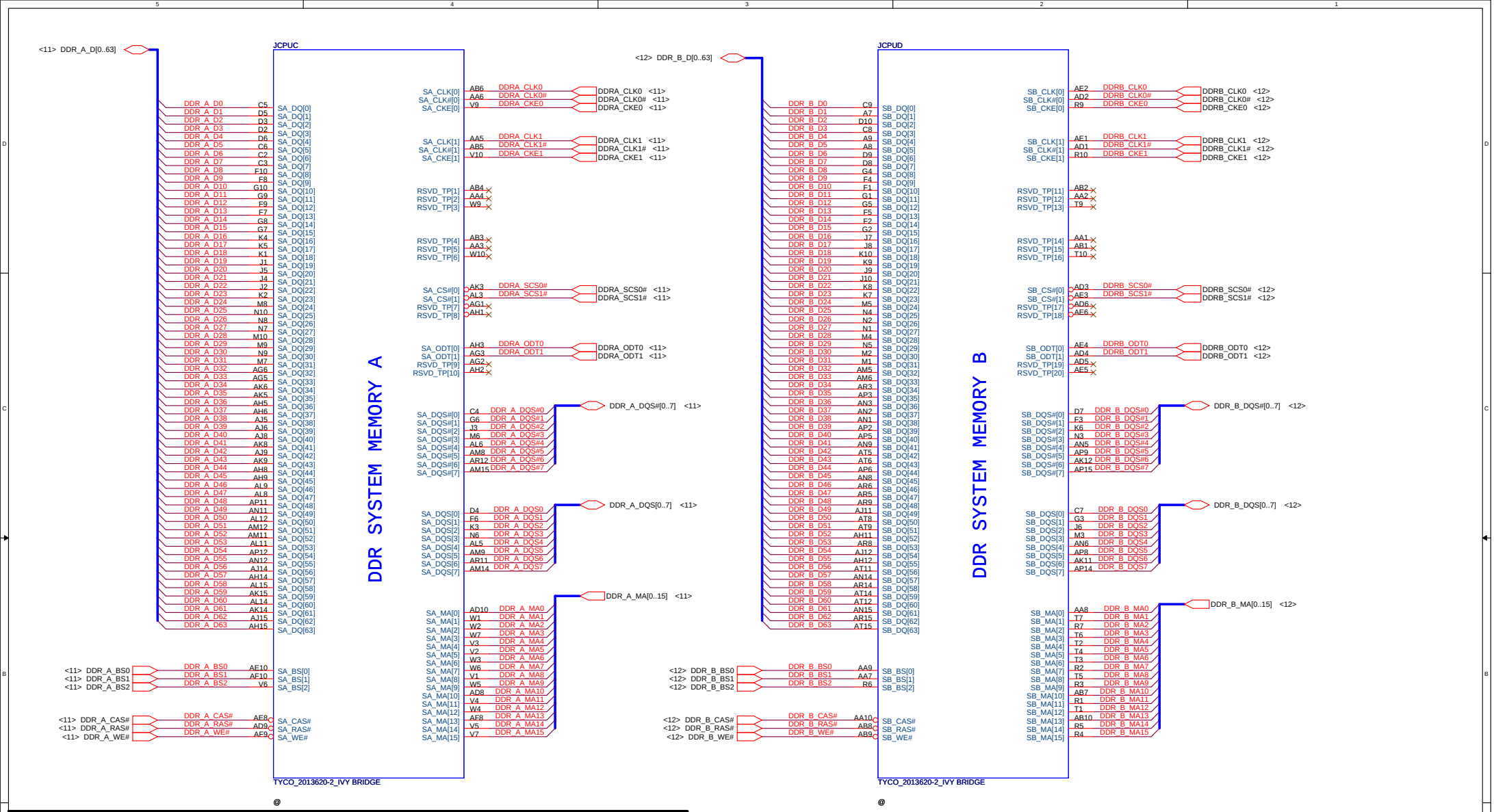

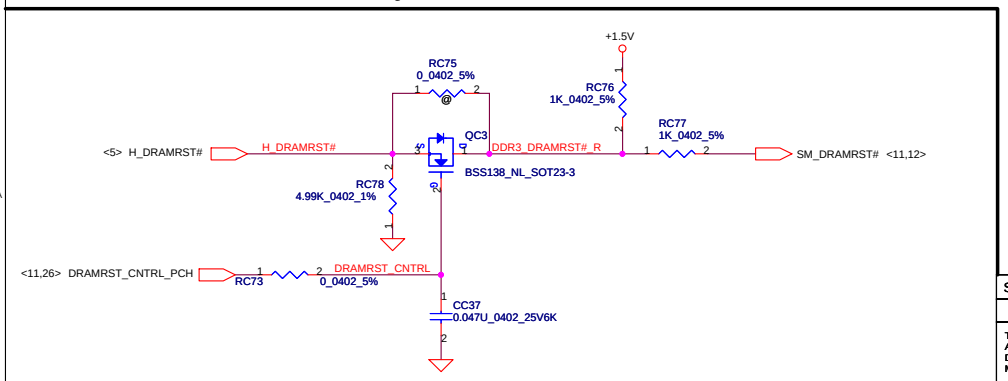

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Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 Sheet 7 of 61

POWER

+CPU_CORE

JCPUF

CORE SUPPLY

97A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

+1.05VS_VCCP

8.5A

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

Reserve 0.1u to avoid noise

+1.05VS_VCCP
0.1U_0402_10V7K
CC50
@
RC91
130_0402_5%

+1.05VS_VCCP
0.1U_0402_10V7K
CC49
@
RC89
75_0402_5%

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

RC90 43_0402_1%
RC88 0_0402_5%
RC92 0_0402_5%

VR_SVID_ALRT# <55>
VR_SVID_CLK <55>
VR_SVID_DAT <55>

Pull high resistor on VR side

SENSE LINES

+CPU_CORE
RC93
100_0402_1%
Close to CPU

VCC_SENSE AJ35 VCCSENSE_R RC94 0_0402_5%
VSS_SENSE AJ34 VSSSENSE_R RC95 0_0402_5%

VCCSENSE <55>
VSSSENSE <55>

VCCIO_SENSE B10 VCCIO_SENSE
VSS_SENSE_VCCIO A10

VCCIO_SENSE <53>

RC97
100_0402_1%

RC96
10_0402_1%
RC98
10_0402_1%
+1.05VS_VCCP
Close to CPU

@TYCO_2013620-2_IVY BRIDGE

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Issued Date	2011/12/14	Deciphered Date	2012/12/31

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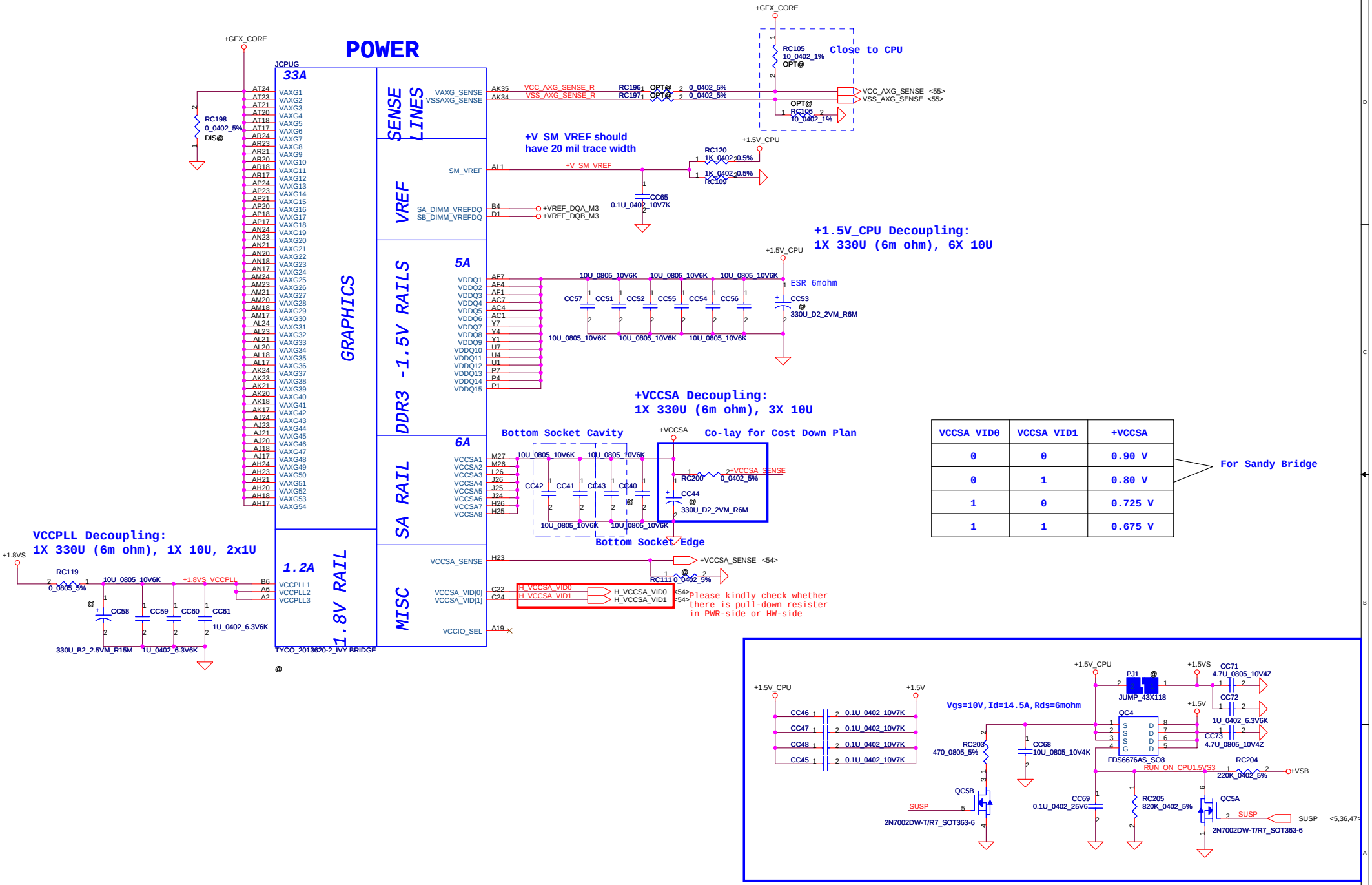
Title: SCHEMATICS, MB A8391

Size: Custom | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 8 of 61

POWER



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge

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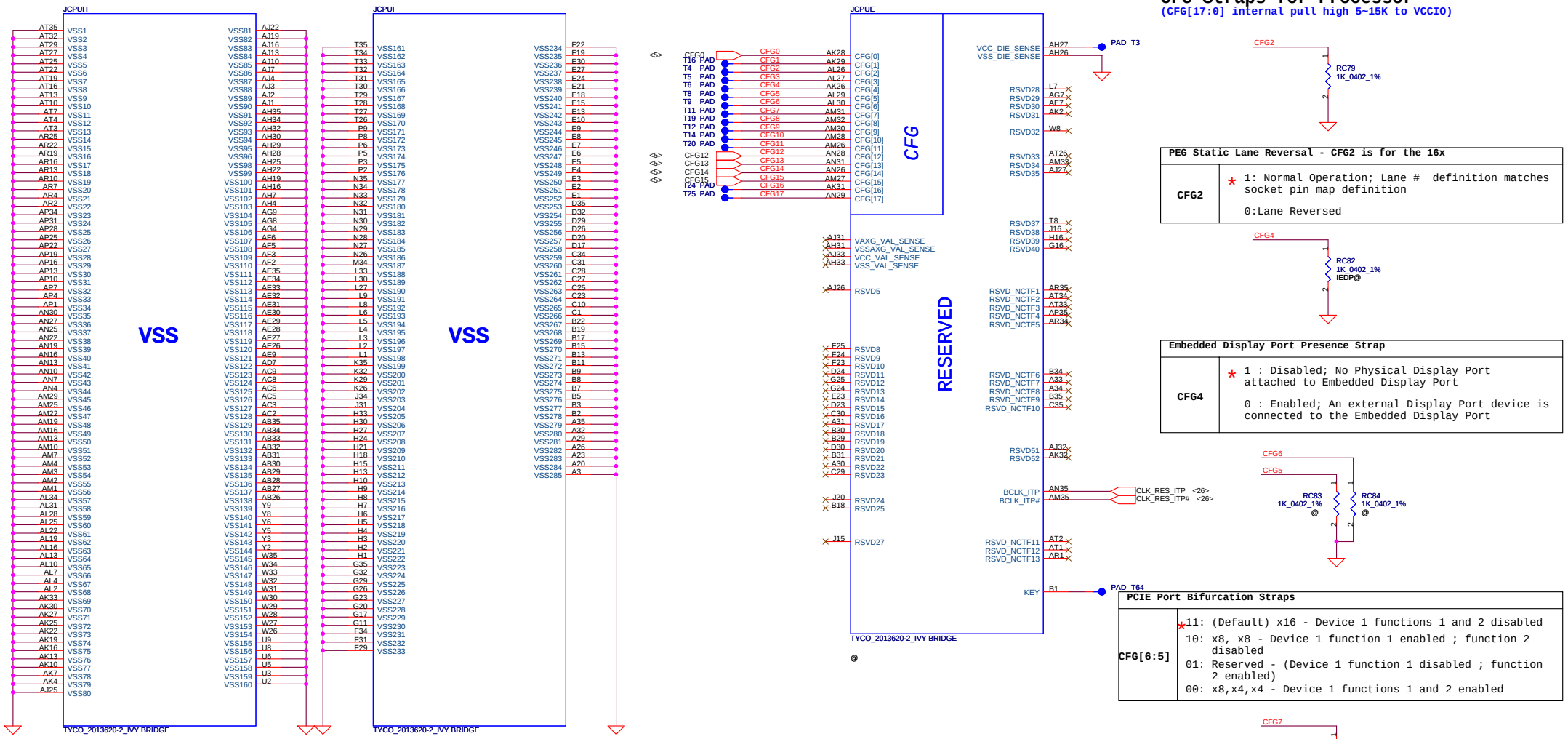
Title	SCHEMATICS, MB A8391
Size: Custom	Document Number: 4019HG
Rev: B	
Date: Thursday, February 16, 2012	Sheet 9 of 61

CFG Straps for Processor

(CFG[17:0] internal pull high 5~15K to VCCIO)



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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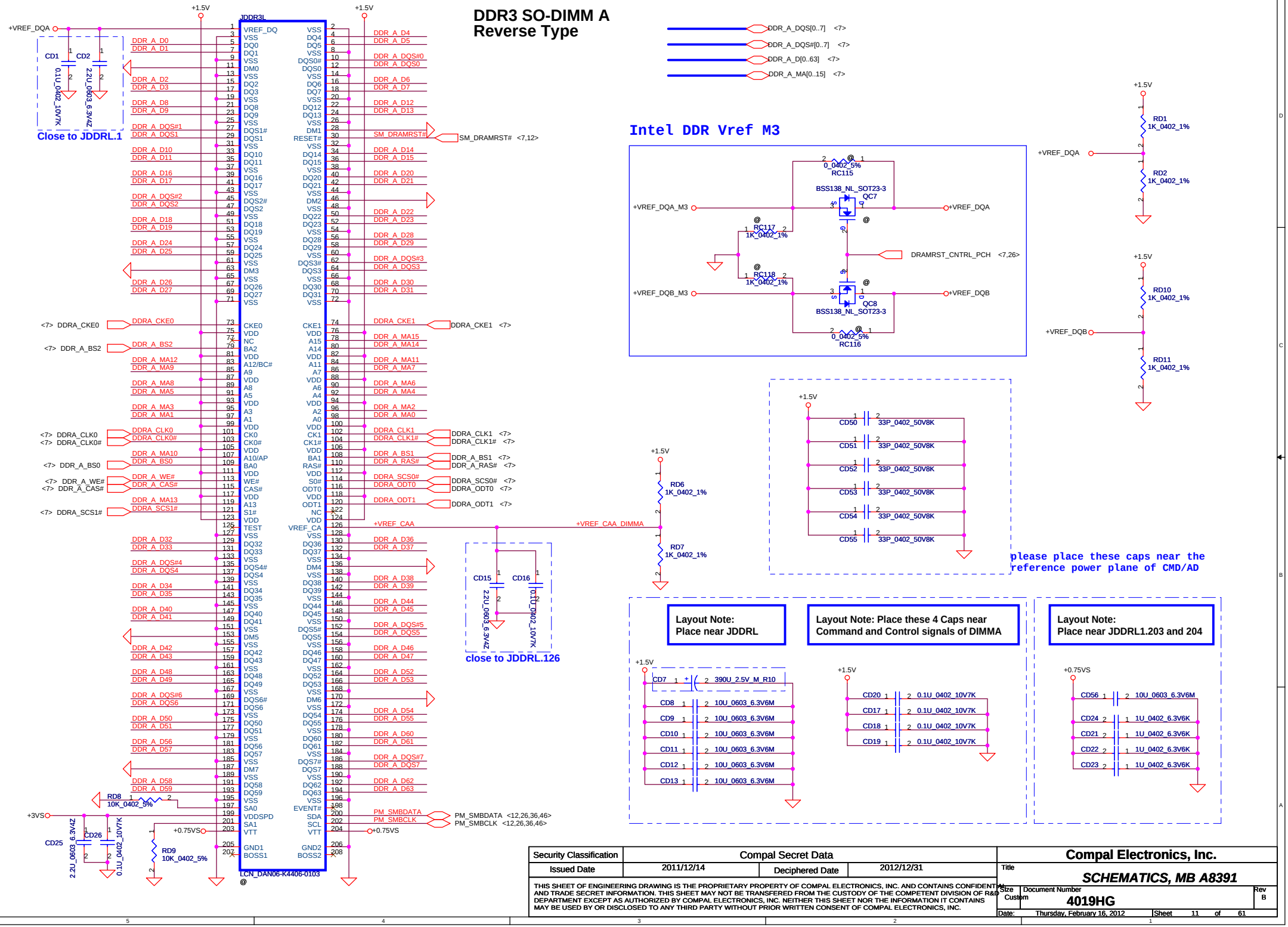
Title: ***SCHEMATICS, MB A8391***

Size: Custom | Document Number: **4019HG** | Rev: B

Date: Thursday, February 16, 2012 | Sheet 10 of 61

DDR3 SO-DIMM A
Reverse Type



DDR_A_DQS[0..7] <7>
DDR_A_DQS#[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_MA[0..15] <7>

Intel DDR Vref M3

please place these caps near the reference power plane of CMD/AD

Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

Layout Note:
Place near JDDRL1.203 and 204

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Issued Date	2011/12/14	Deciphered Date	2012/12/31

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Title: ***SCHEMATICS, MB A8391***

Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 | Sheet 11 of 61

Reverse Type
DDR3 SO-DIMM B

JDDR3H

FOX_AS0A626-UASN-7F_204P

Close to JDDRH.1

Close to JDDRH.126

DDR_B_DQS#[0..7] <7>
DDR_B_DQS[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

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Issued Date	2011/12/14	Deciphered Date	2012/12/31

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Title: ***SCHEMATICS, MB A8391***

Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 | Sheet 12 of 61

UV4A

Part 1 of 7

PCI EXPRESS

GPIO

DACs

I2C

CLK

N13P-PES-A2_FCBGA908
N13PGSR1@

EC GPS_DOWN# must be OD\Low to avoid leakage on OPT SKU.

120mA

LVDS

Internal Thermal Sensor

CV1971 under GPU close to ball : ADB

CV38,CV40, CV41 under GPU close to ball : AE8,AD7

Close to GPU

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Deciphered Date	2012/12/31

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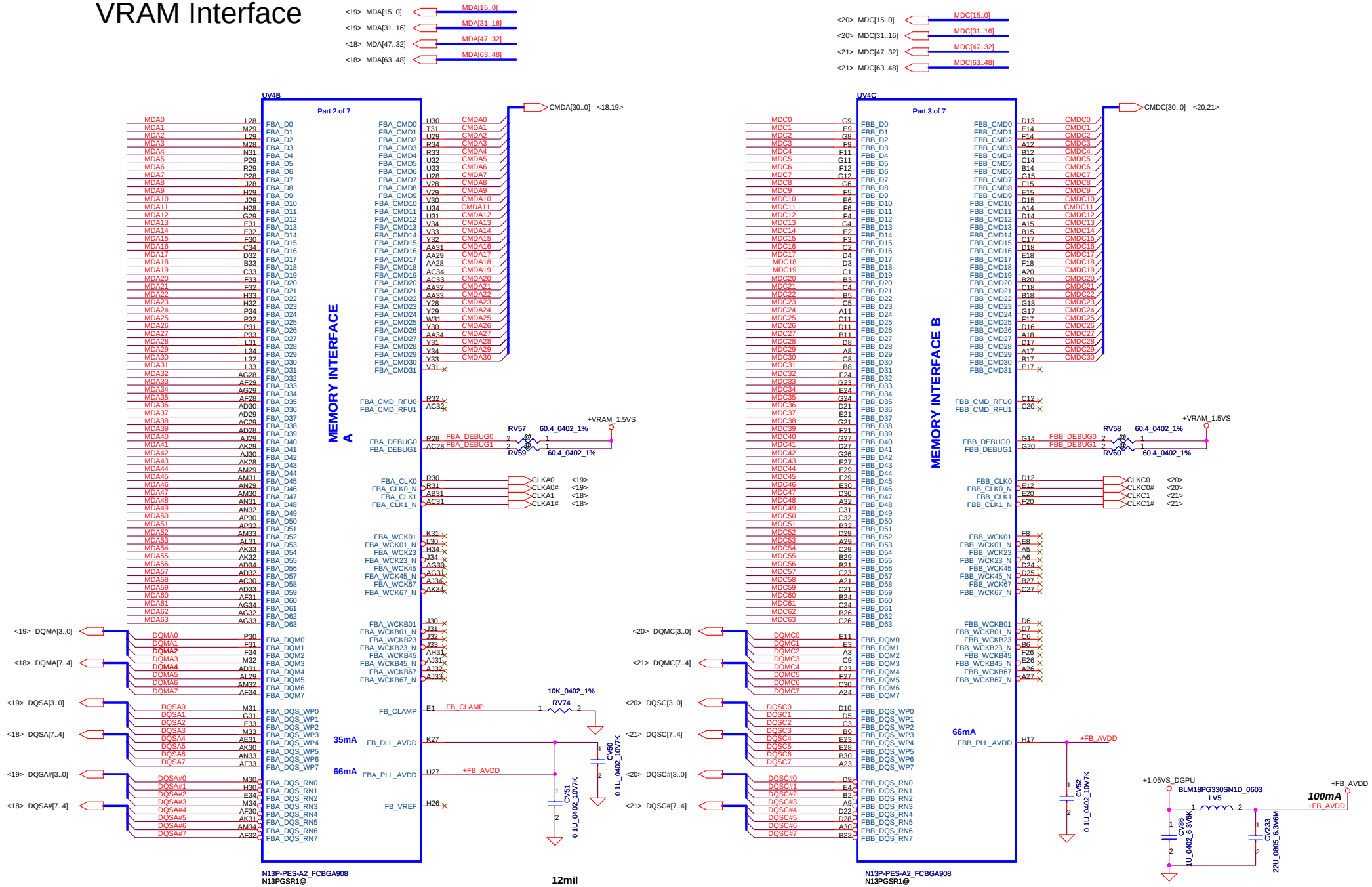
Size: Custom | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 13 of 61

VRAM Interface



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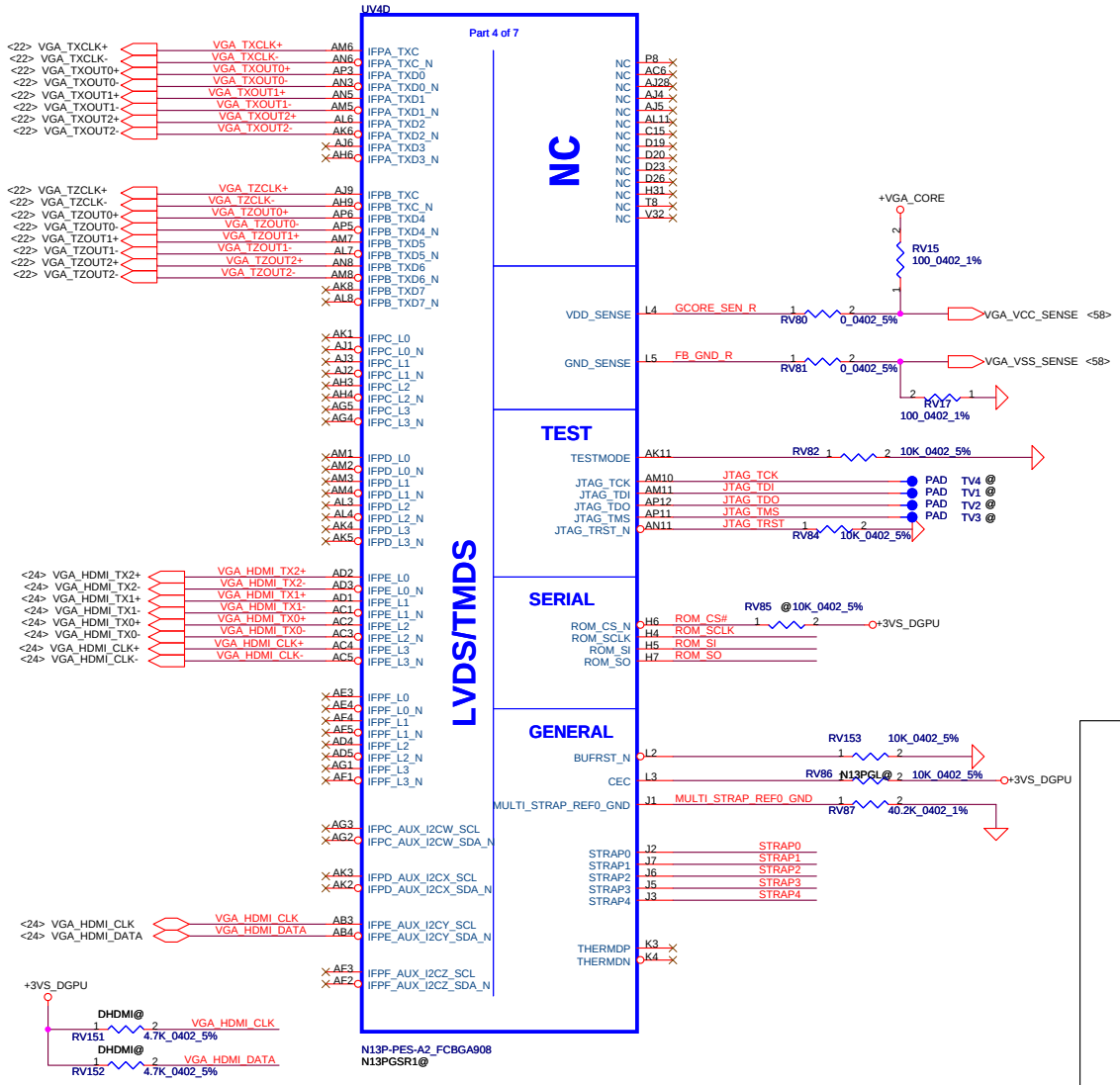
Title: SCHEMATICS, MB A8391			
Size: Custom	Document Number: 4019HG		Rev: B
Date: Thursday, February 16, 2012	Sheet 14 of 61		

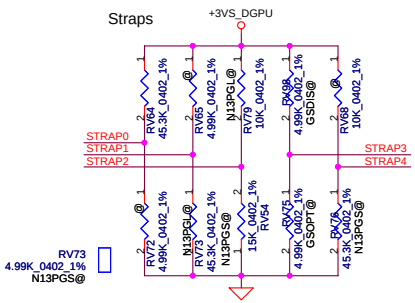
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417 for GL , FB[1]	FB_0_BAR_SIZE for GL , FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**SLOT_CLK_CFG for GL PCI_DEVID[5]**	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

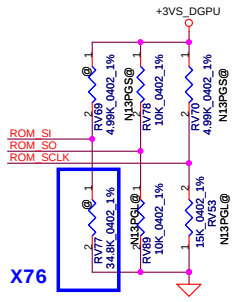
SKU	Device ID	biit5 to bit0
N13P-GL ES2	0x0DE9	101001
N13P-GS ES1	0x0FDB	011011
N13P-GS QS	0x0FD2	010010

Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



MULTI LEVEL STRAPS





N13P-GL/GS/GT/LP ROM_SI			
Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	RV77 PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003YO00	2GB	0110	RV77 PD 34.8k (SD034348280)
Hynix (900MHZ) 128MX16 H5TQ2G63DFR-11C SA00003YO70	2GB	0101	RV77 PD 30k (SD034300280)
Samsung (900MHZ) 64MX16 K4W1G1646G-BC11 SA00004GS00	1GB	0011	RV77 PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	RV77 PD 45.3K (SD034453280)
Samsung (900MHZ) 128M16 K4W2G1646E-HC11 SA000047QC0	2GB		

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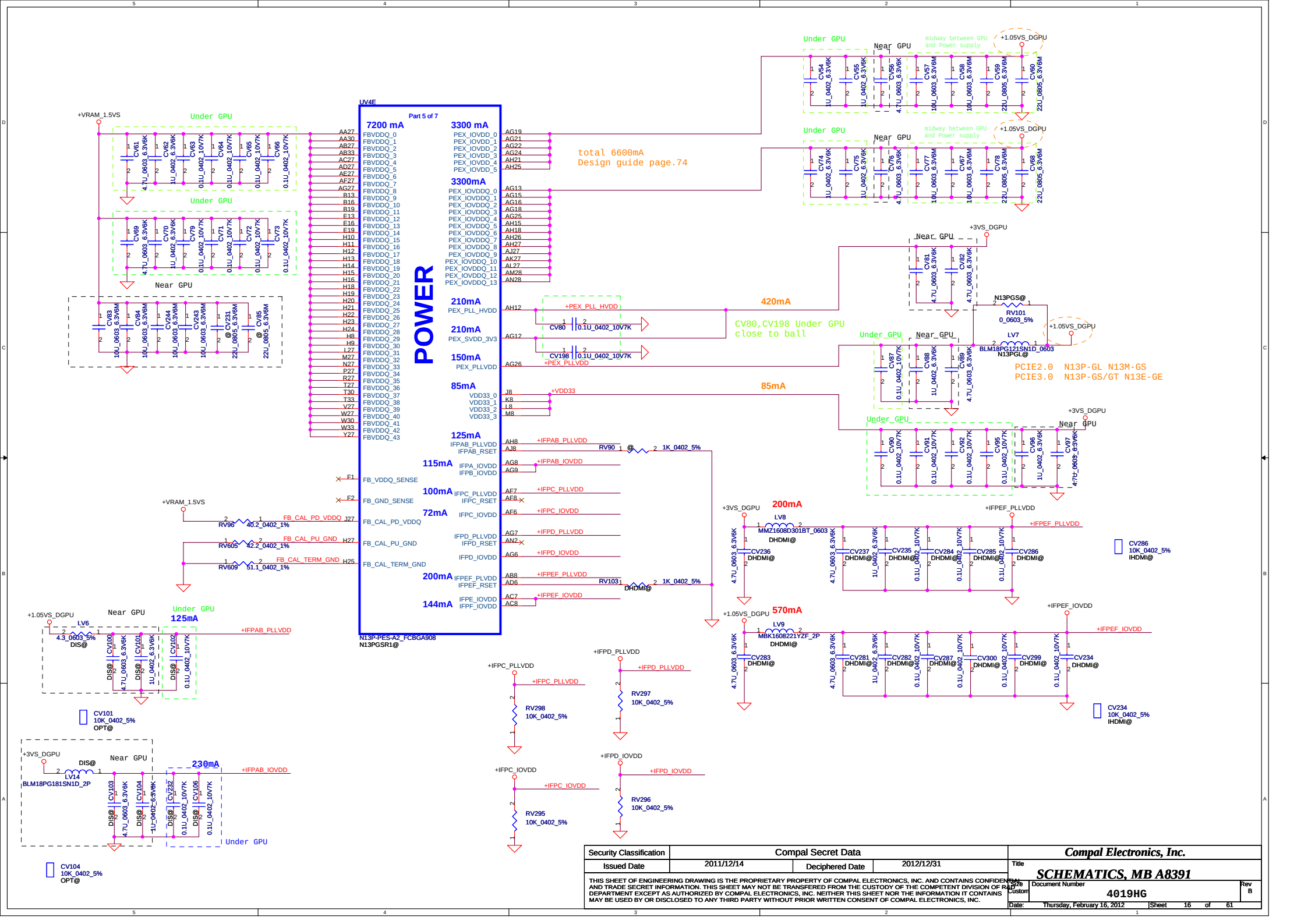
Size: Custom | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 15 of 61



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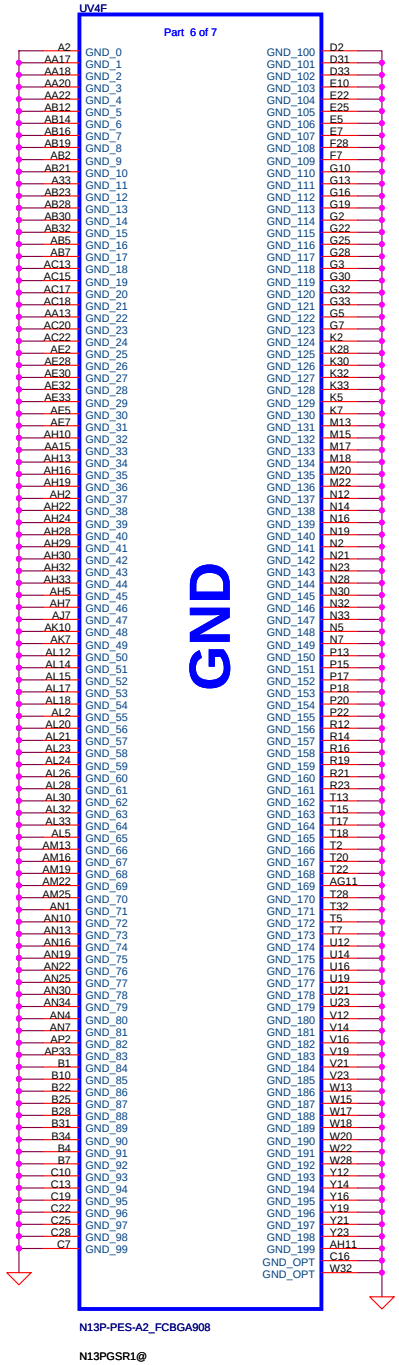
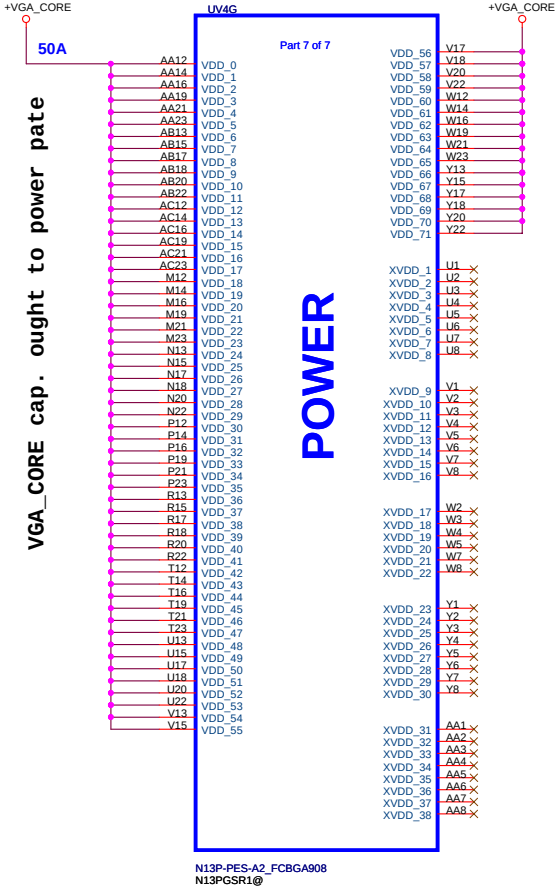
Size: Custom	Document Number: 4019HG
Rev: B	
Date: Thursday, February 16, 2012	Sheet 16 of 61





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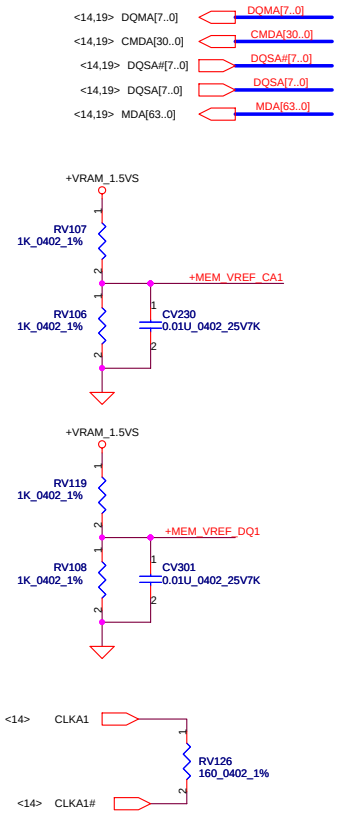
Title: SCHEMATICS, MB A8391

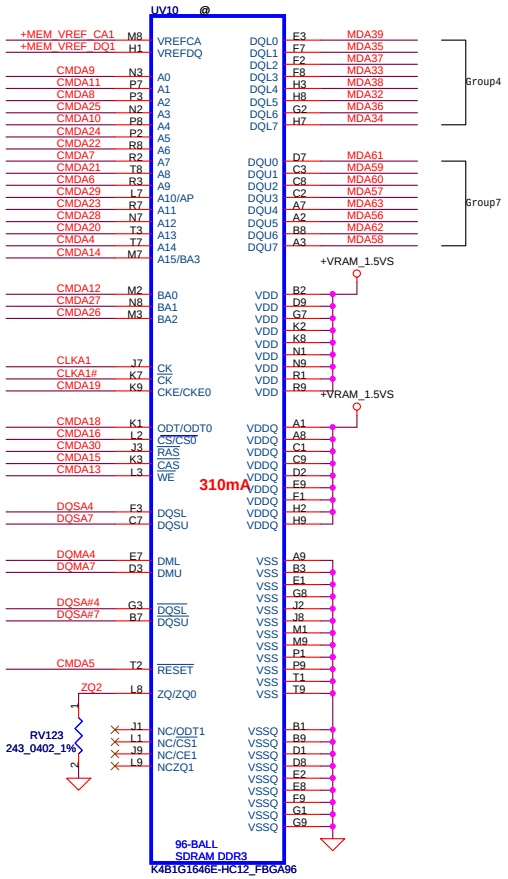
Size	Document Number	Rev
Custom	4019HG	B

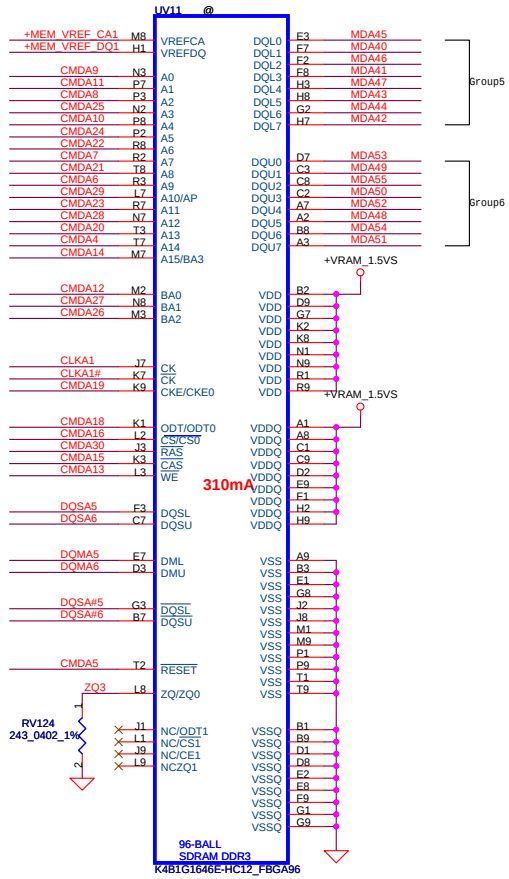
Date: Thursday, February 16, 2012 Sheet 17 of 61

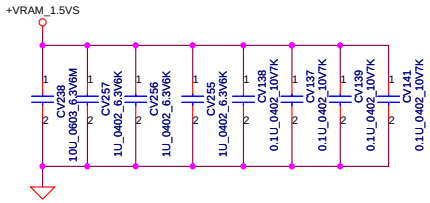
VRAM DDR3 chips (1GB)

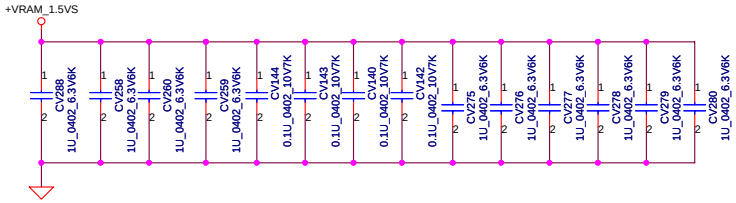
64Mx16 DDR3 *8==>1GB











Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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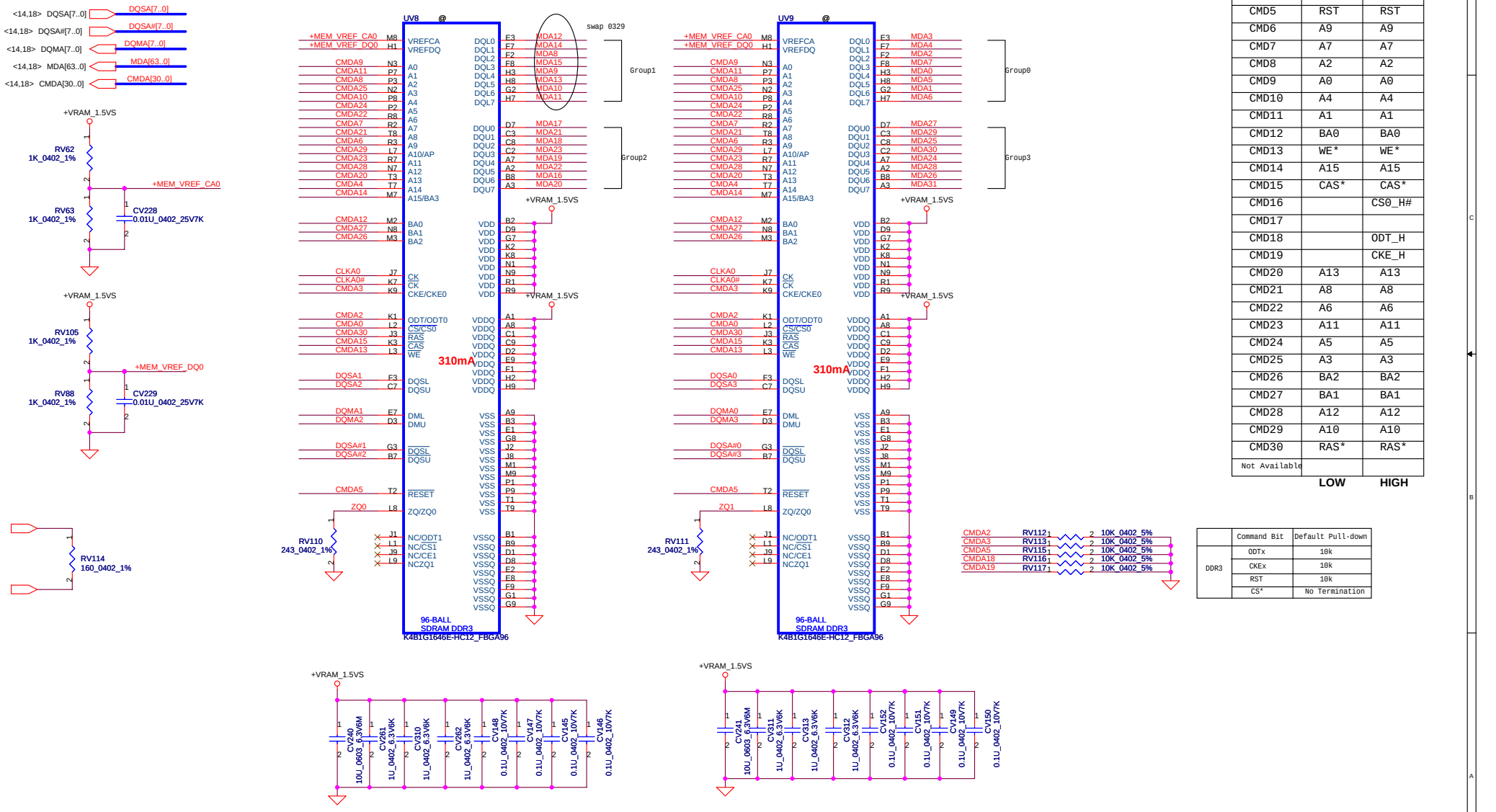
			Date: Thursday, February 16, 2012 / Sheet 18 of 61

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
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CMD1		
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CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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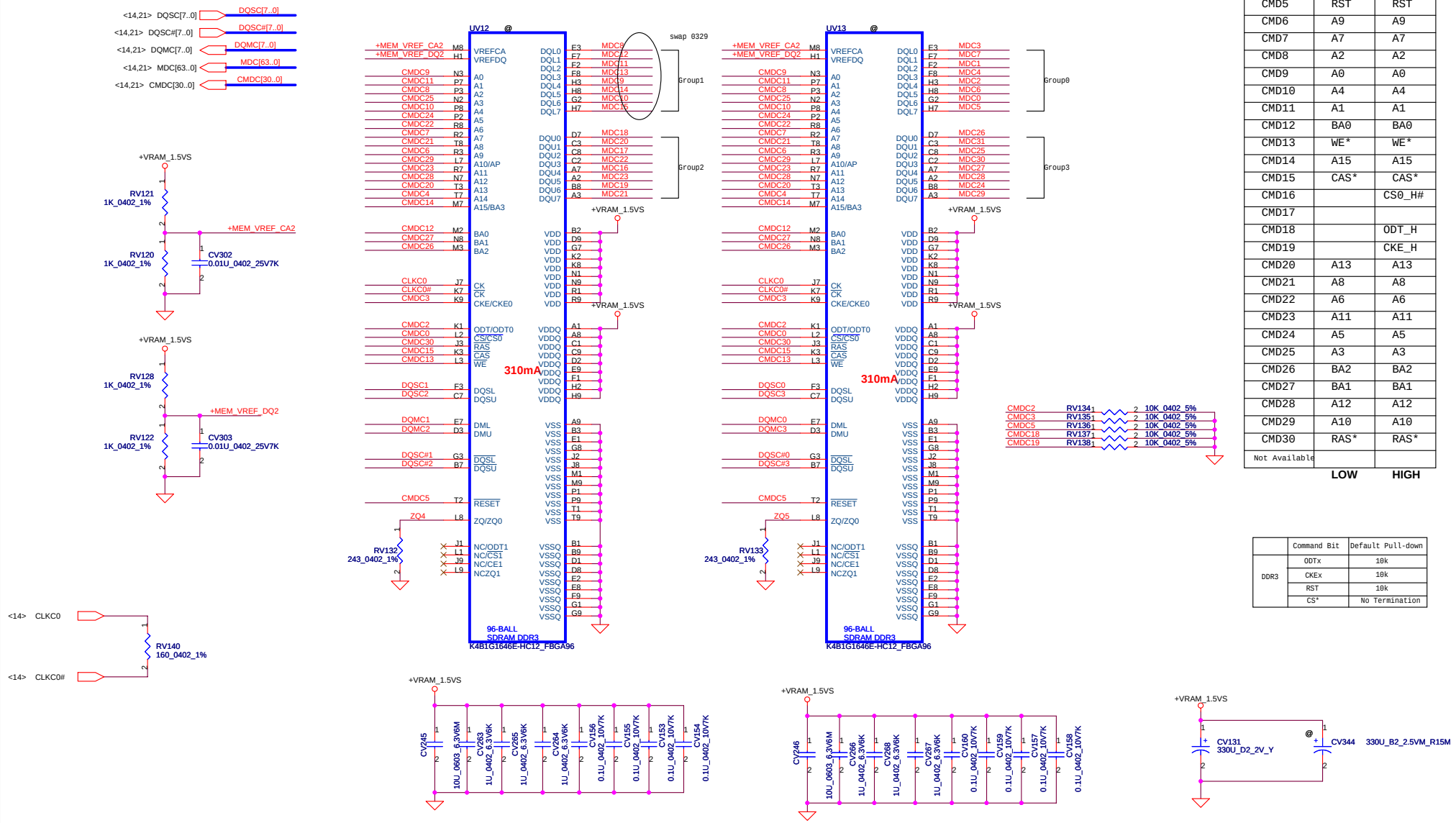
			Date: Thursday, February 16, 2012 / Sheet 19 of 61

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
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CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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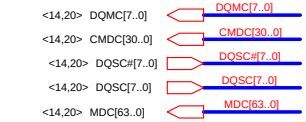
Title: SCHEMATICS, MB A8391

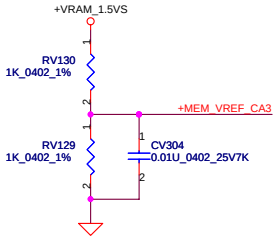
Size: Custom | Document Number: 4019HG | Rev: B

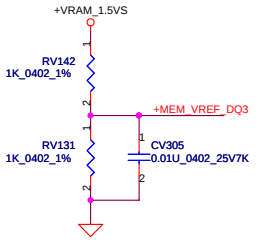
Date: Thursday, February 16, 2012 | Sheet 20 of 61

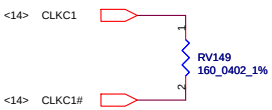
VRAM DDR3 chips (1GB)

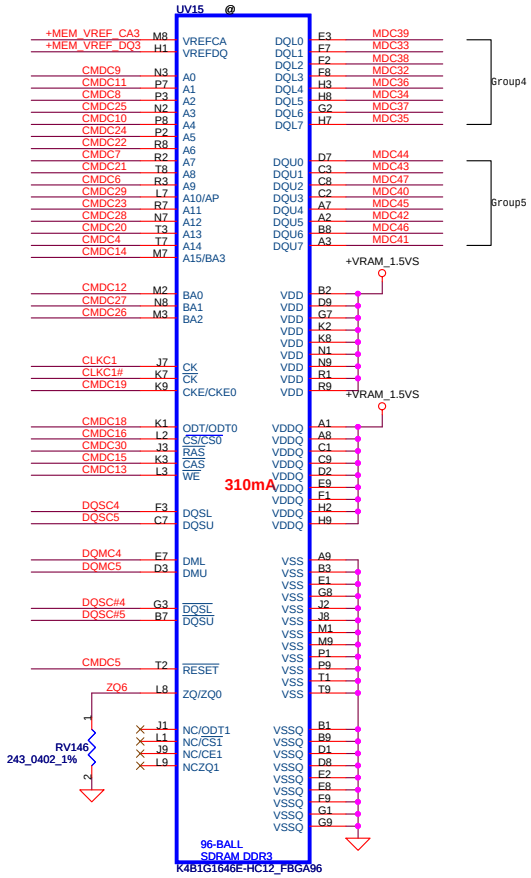
64Mx16 DDR3 *8==>1GB

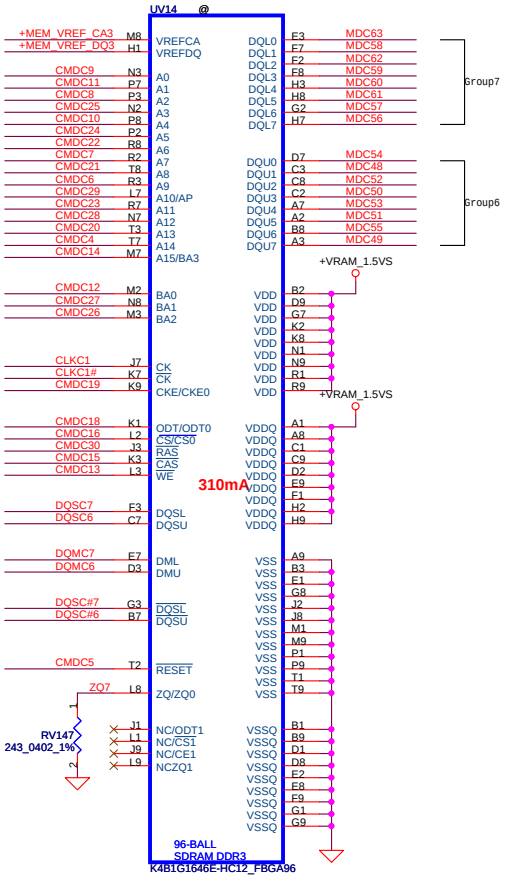


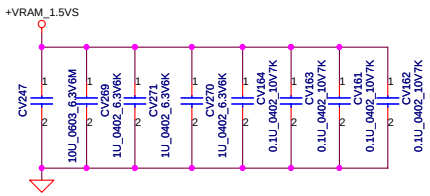


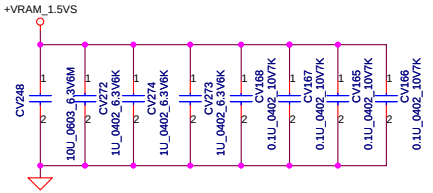












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CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

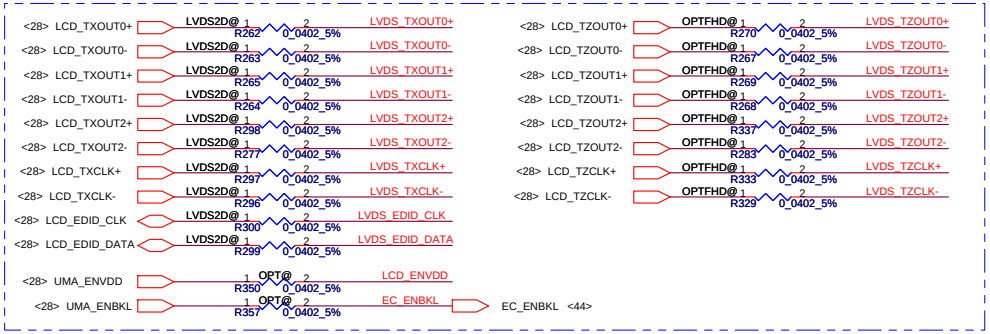
Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

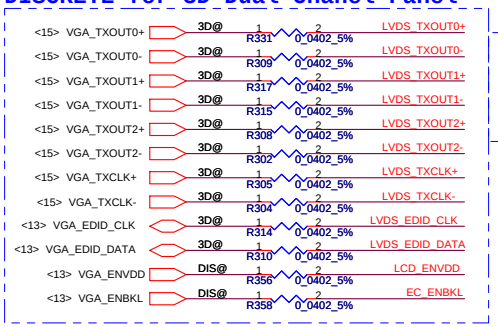
Size: Custom | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 21 of 61

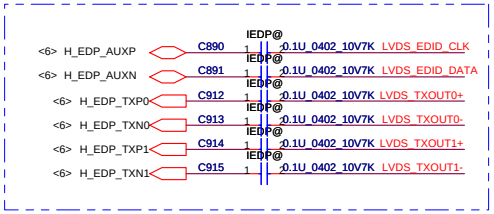
OPTIMUS for 2D HD/FHD Panel



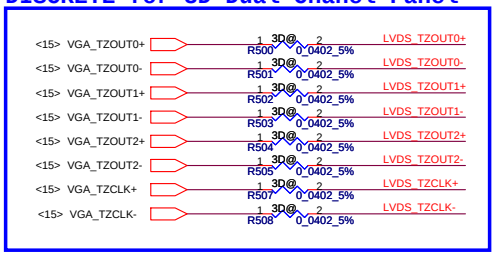
DISCRETE for 3D Dual Chanel Panel



OPT for 2D HD eDP Panel

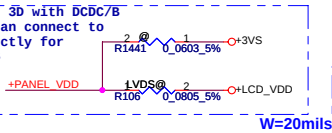


DISCRETE for 3D Dual Chanel Panel

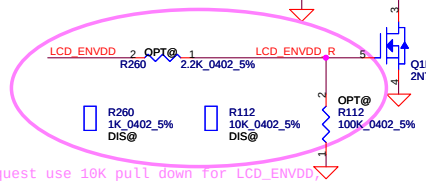


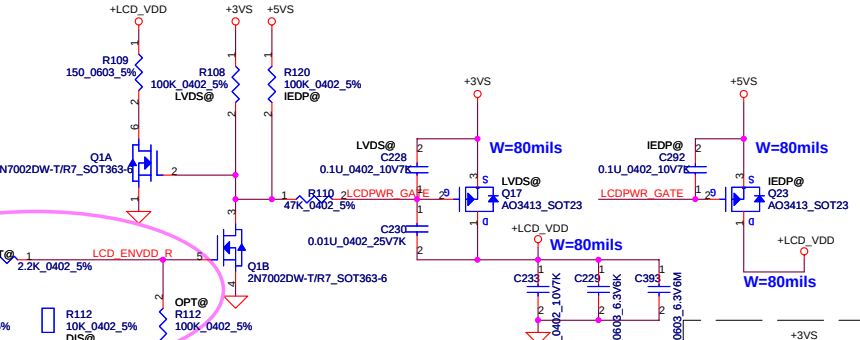
LCD/PANEL BD. Conn.

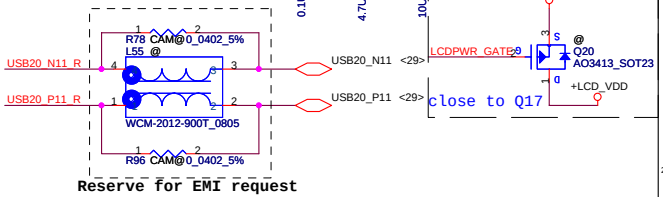
only need for 3D with DCDC/B
,JLVDS Pin8 can connect to
+LCV_VDD directly for
3D w/o DCDC/B



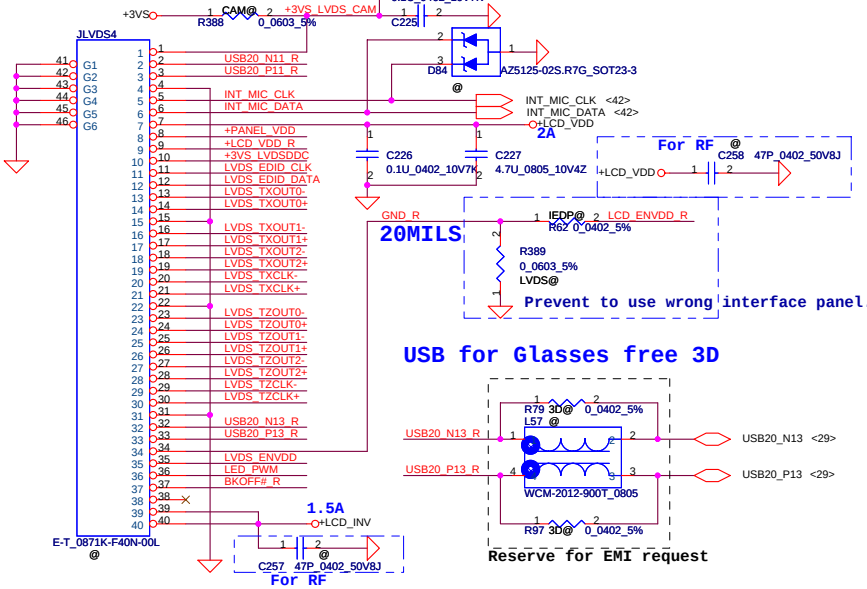
due to NV request use 10K pull down for LCD_ENVDD
we separate BOM for OPT/DIS SKU



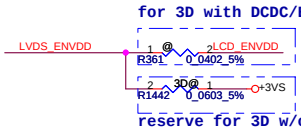




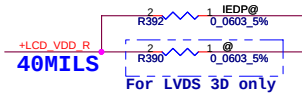
Reserve for EMI request



for 3D with DCDC/B



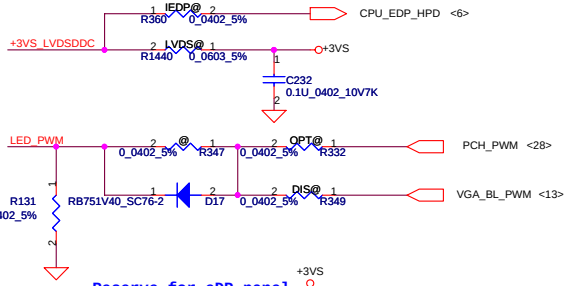
reserve for 3D w/o DCDC/B



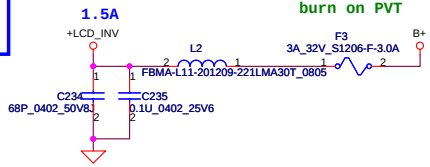
For LVDS 3D only

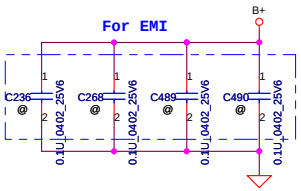
USB for Glasses free 3D

Reserve for EMI request



Add F3 to prevent
burn on PVT



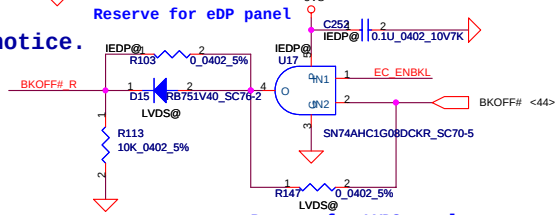


LVDS & eDP cable pine definition notice.

Prevent to use wrong interface panel.

	LVDS cable MB side Pin 22	eDP cable MB side Pin 22
LVDS	GND	
eDP		NC

Reserve for eDP panel

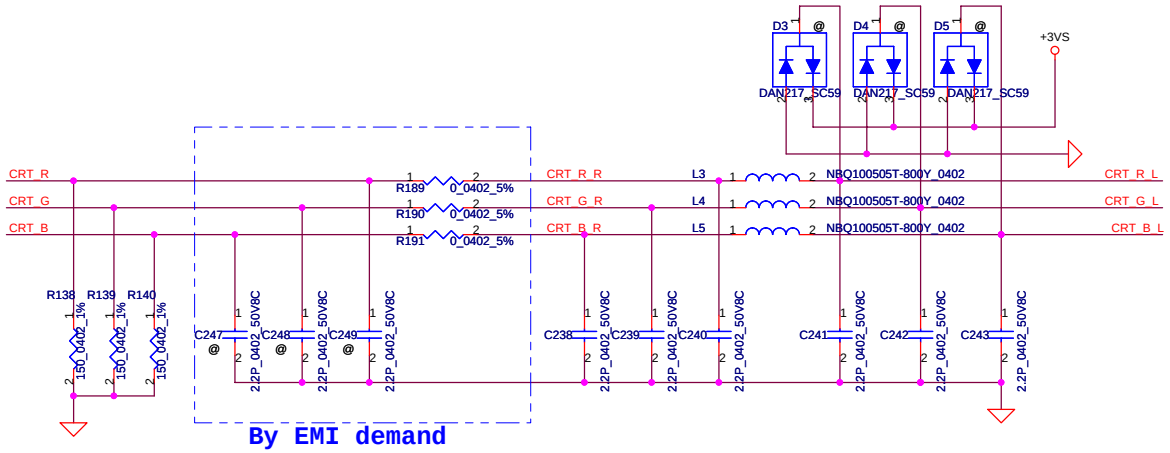


Reserve for LVDS panel

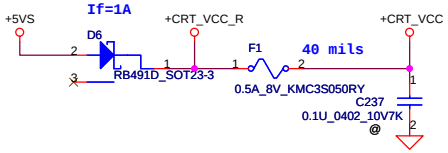
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

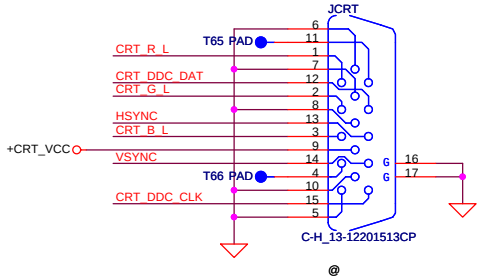
Compal Electronics, Inc.	
Title	SCHEMATICS, MB A8391
Size: Custom	Document Number: 4019HG
Rev	B
Date: Thursday, February 16, 2012	Sheet 22 of 61

CRT CONNECTOR

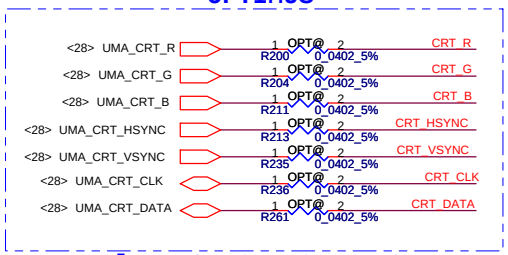


By EMI demand



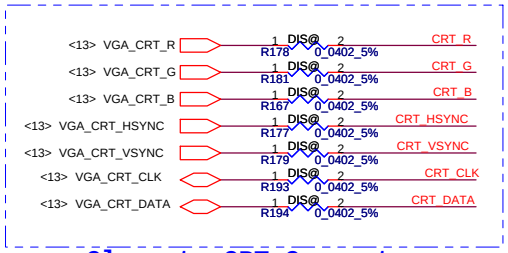


OPTIMUS

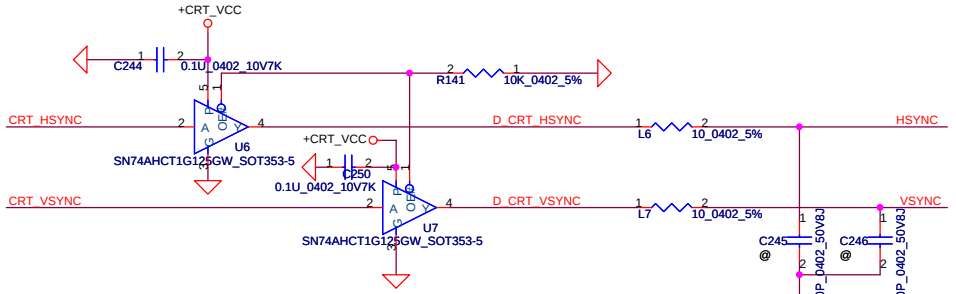


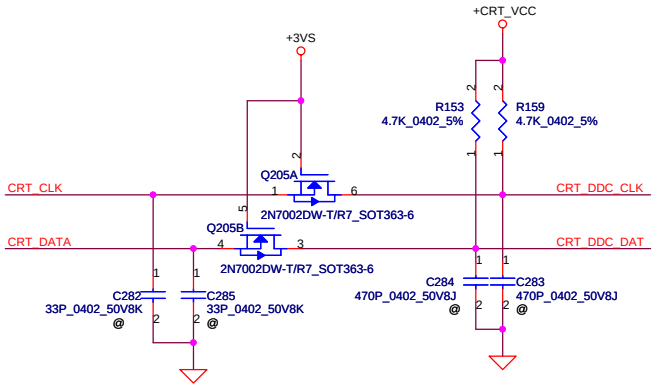
Close to CRT Connector

DISCRETE



Close to CRT Connector





Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

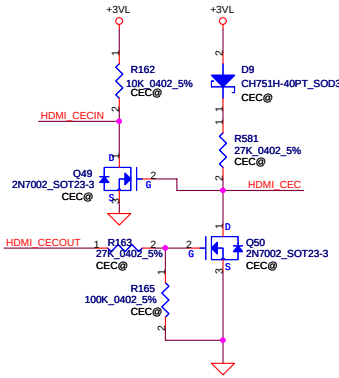
Compal Electronics, Inc.

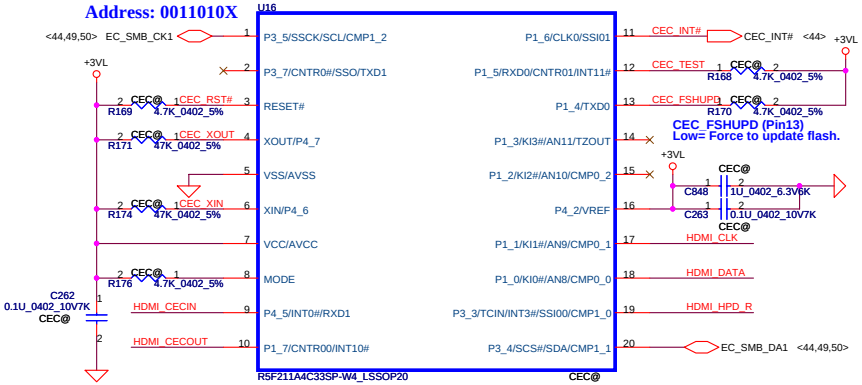
Title: *SCHEMATICS, MB A8391*

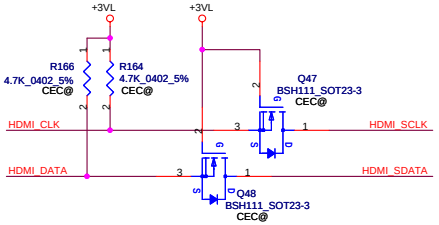
Size | Document Number: **4019HG** | Rev: B

Date: Thursday, February 16, 2012 | Sheet 23 of 61

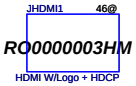
HDMI CEC Controller





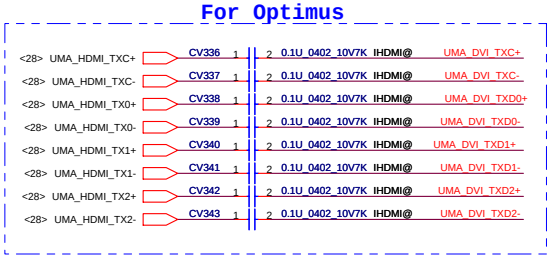


HDMI Royalty

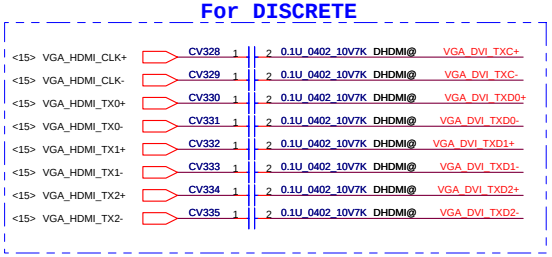


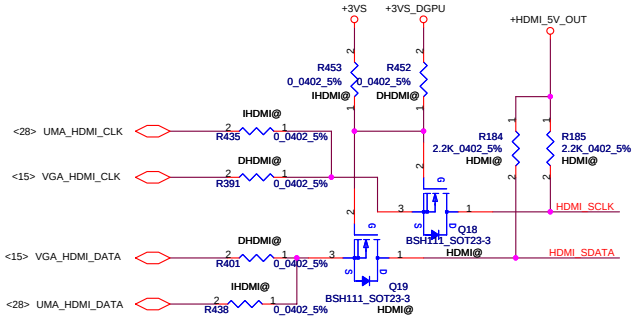
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

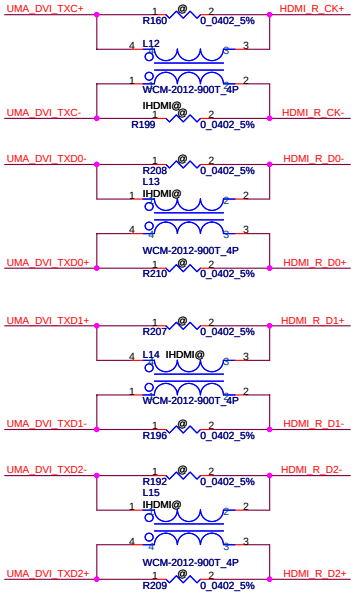
For Optimus

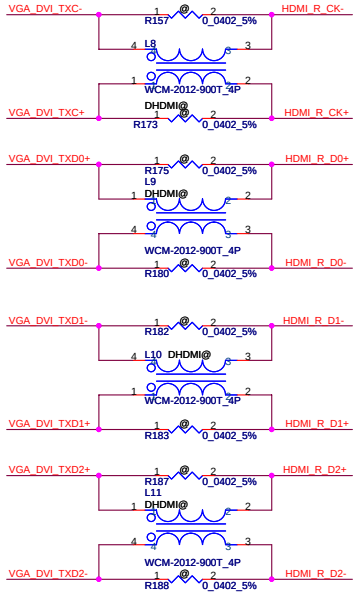


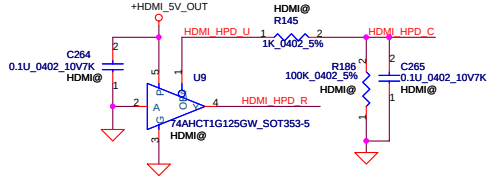
For DISCRETE

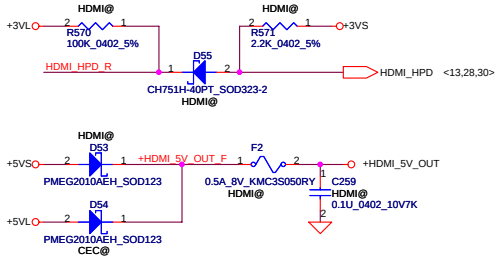






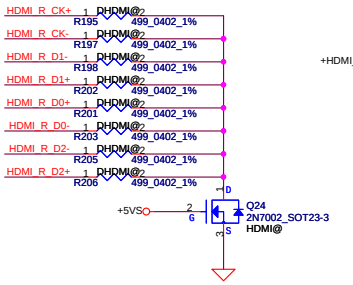




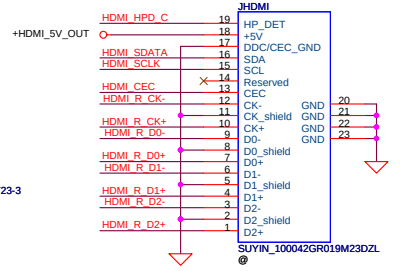


R195 680_0402_5% IHDMI@	R197 680_0402_5% IHDMI@		
R198 680_0402_5% IHDMI@	R202 680_0402_5% IHDMI@		
R201 680_0402_5% IHDMI@	R203 680_0402_5% IHDMI@		
R205 680_0402_5% IHDMI@	R206 680_0402_5% IHDMI@		

07/10/2010
Intel DG P.132



HDMI Connector



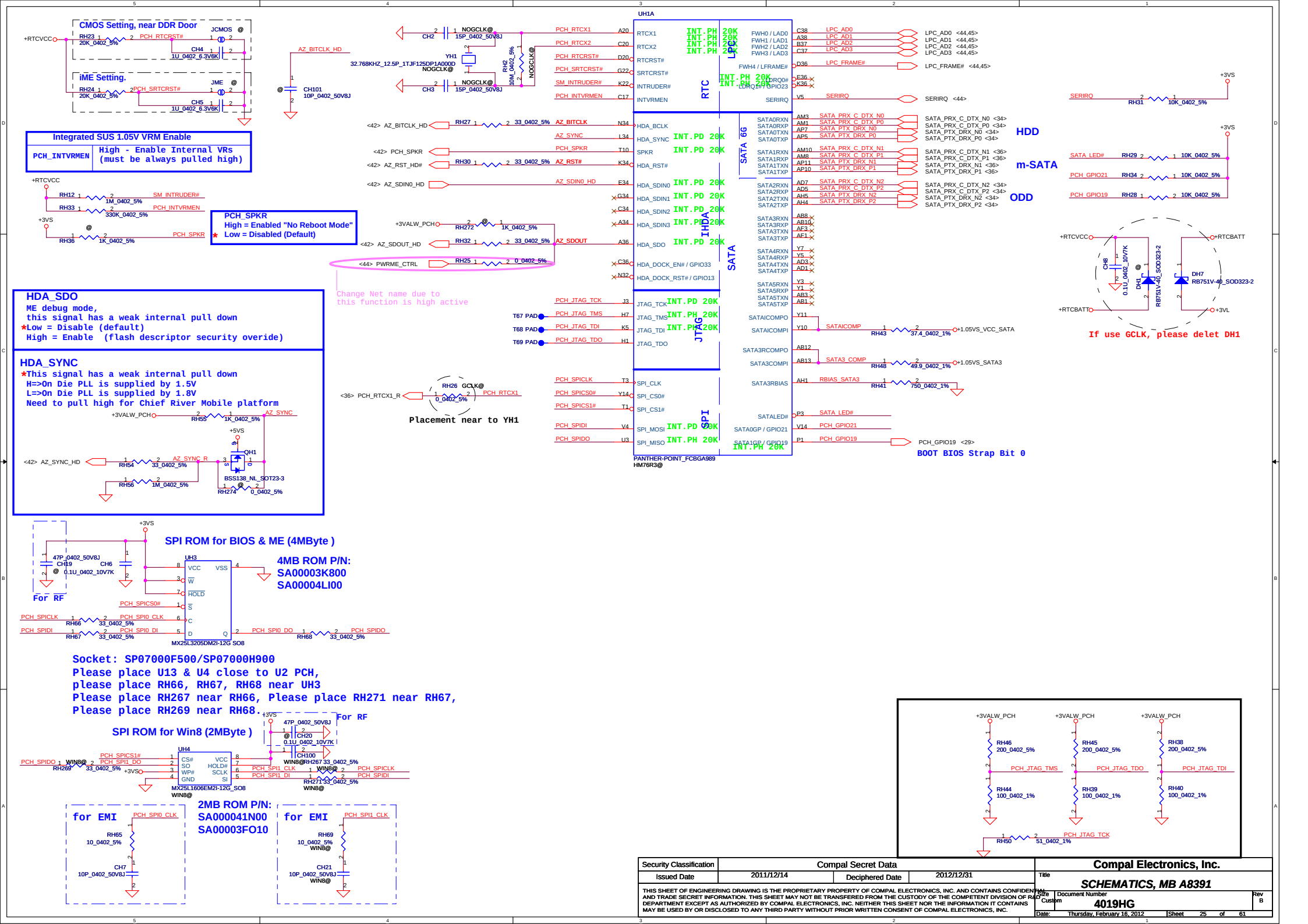
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8391**

Size	Document Number	Rev
	4019HG	B

Date: Thursday, February 16, 2012 Sheet 24 of 61



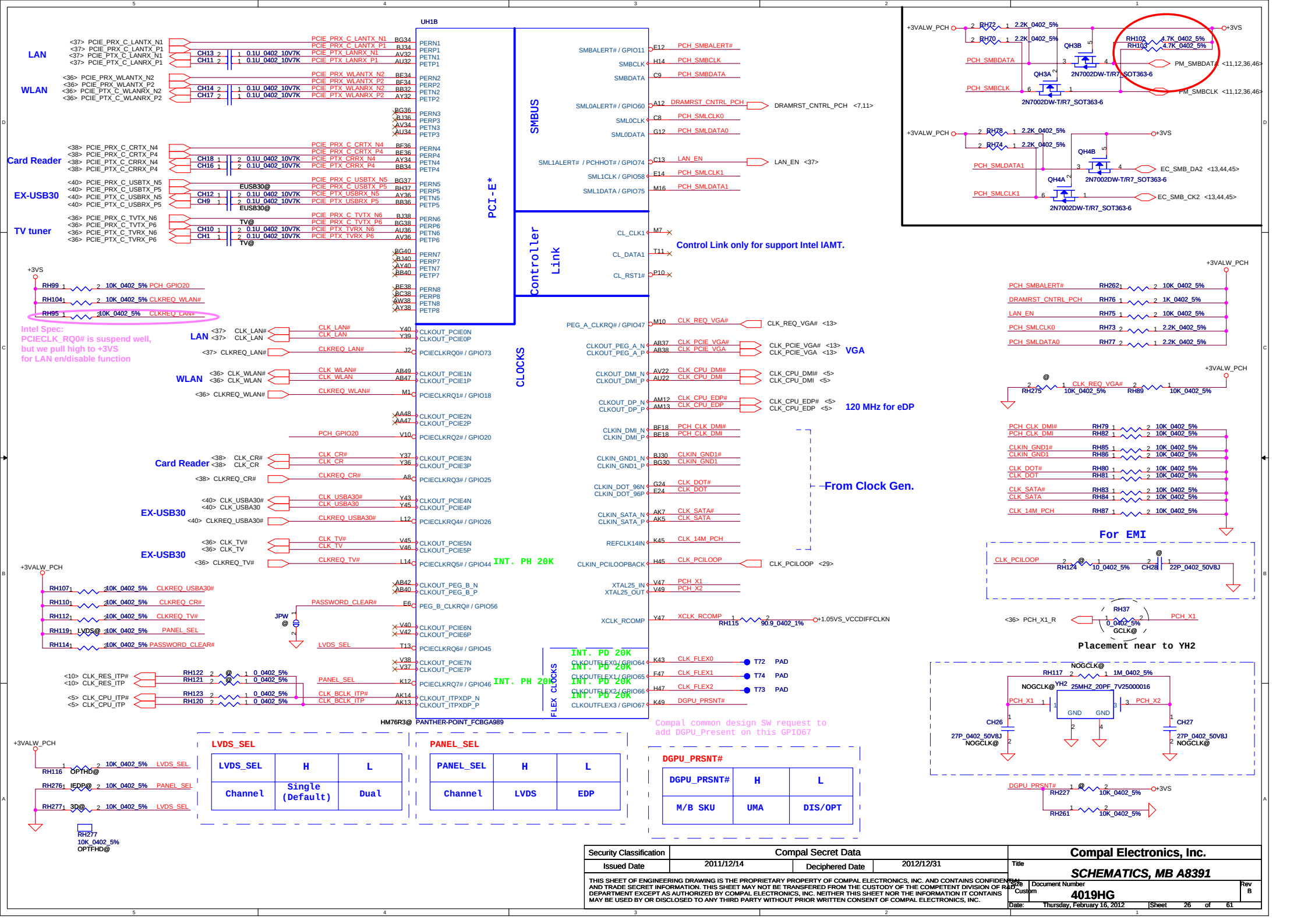
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

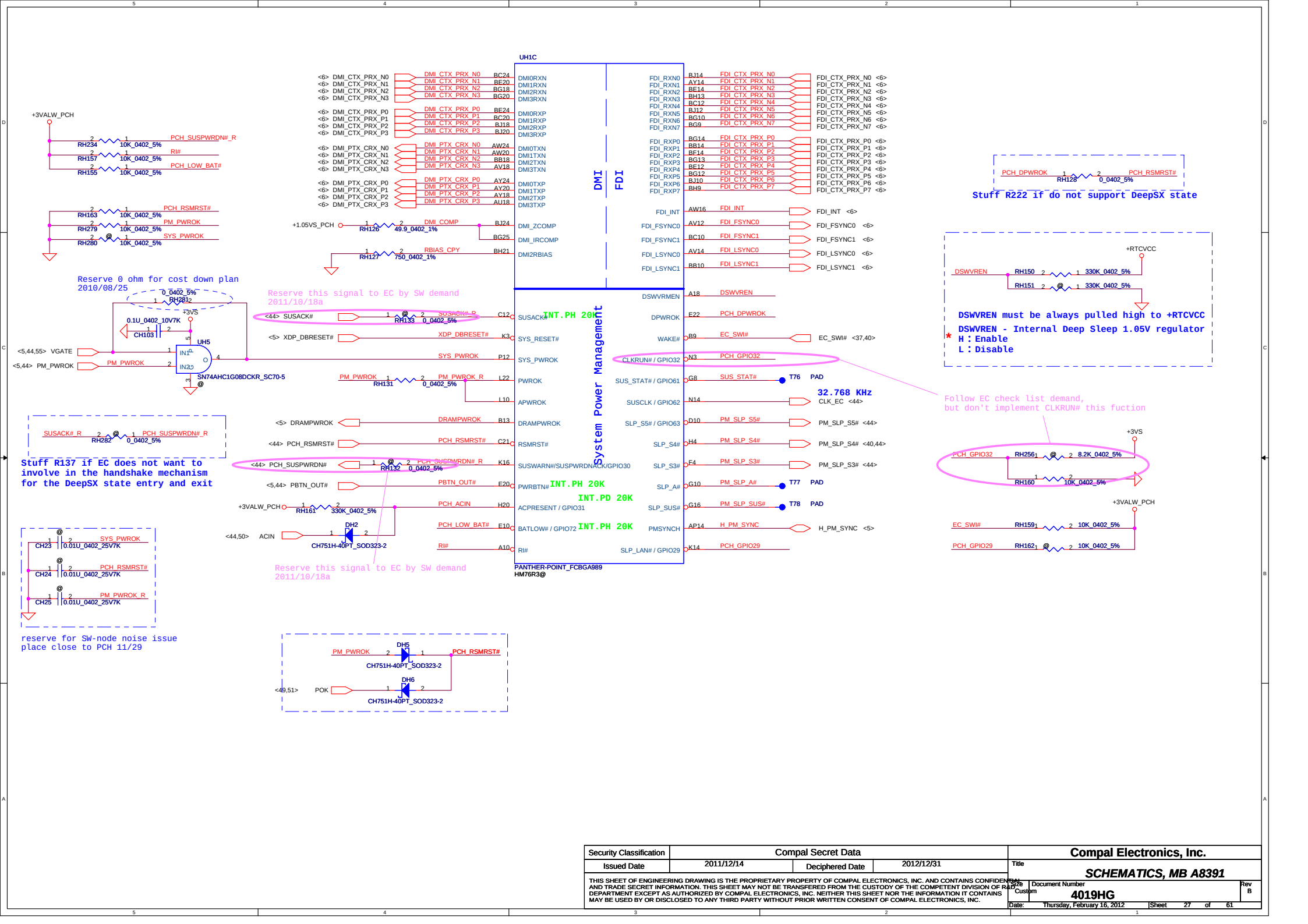
Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8391**

Size: Custom | Document Number: **4019HG** | Rev: B

Date: Thursday, February 16, 2012 | Sheet 25 of 61


UH1B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
LAN
WLAN
Card Reader
EX-USB30
TV tuner
VGA
From Clock Gen.
120 MHz for eDP
Control Link only for support Intel IAMT.
Intel Spec:
PCIECLK_RQ0# is suspend well, but we pull high to +3VS for LAN en/disable function
INT. PH 20K
INT. PD 20K
Compal common design SW request to add DGPU_Present on this GPIO67
For EMI
Placement near to YH2
HM76R3@ PANTHER-POINT_FCBGA989
LVDS_SEL
PANEL_SEL
DGPU_PRSNT#
Compal Electronics, Inc.
SCHEMATICS, MB A8391
4019HG
Security Classification
Compal Secret Data
Issued Date
2011/12/14
Deciphered Date
2012/12/31
Thursday, February 16, 2012
Sheet 26 of 61



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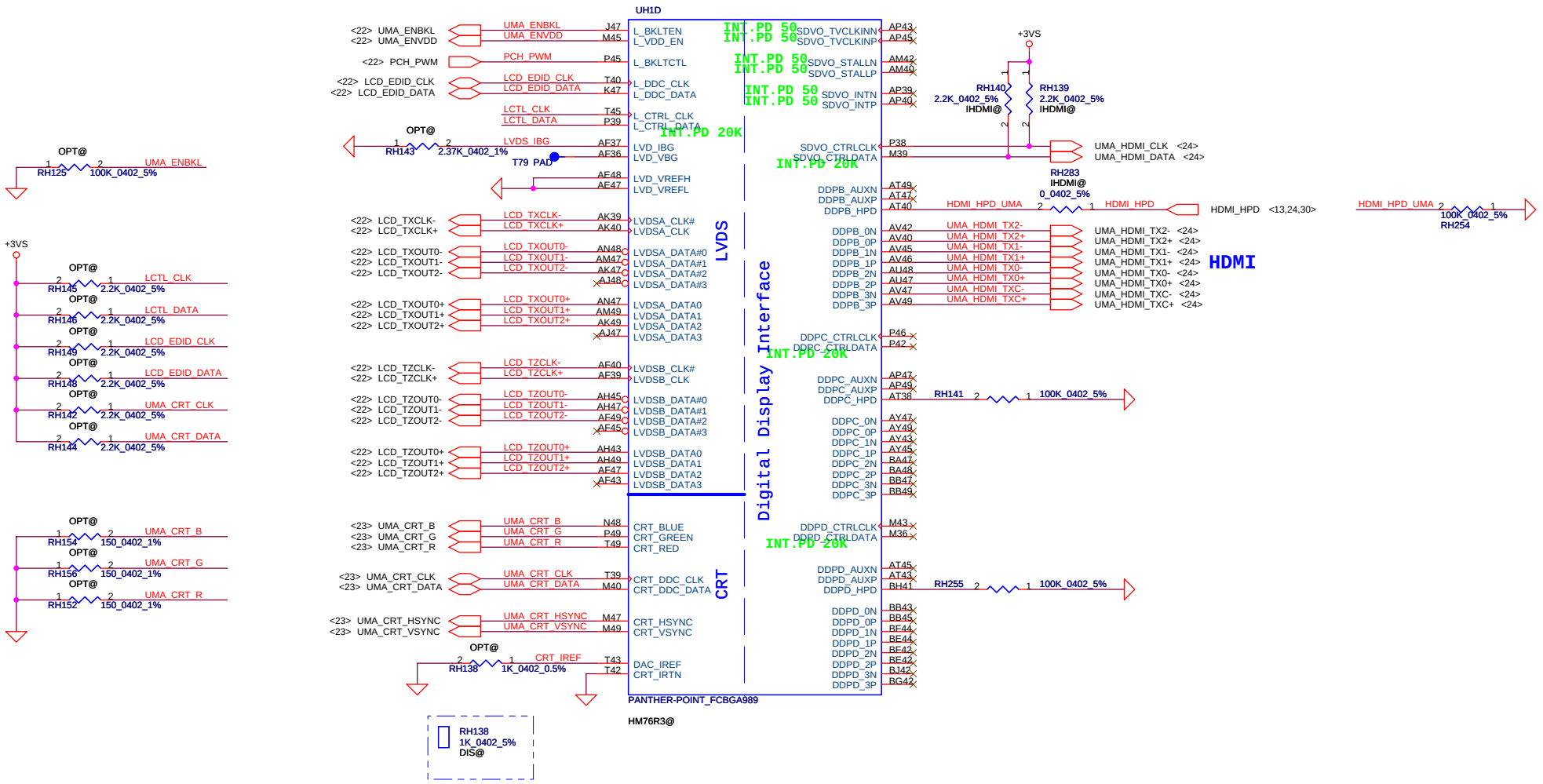
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8391		
Size: Custom	Document Number: 4019HG		Rev: B
Date: Thursday, February 16, 2012	Sheet 27 of 61		



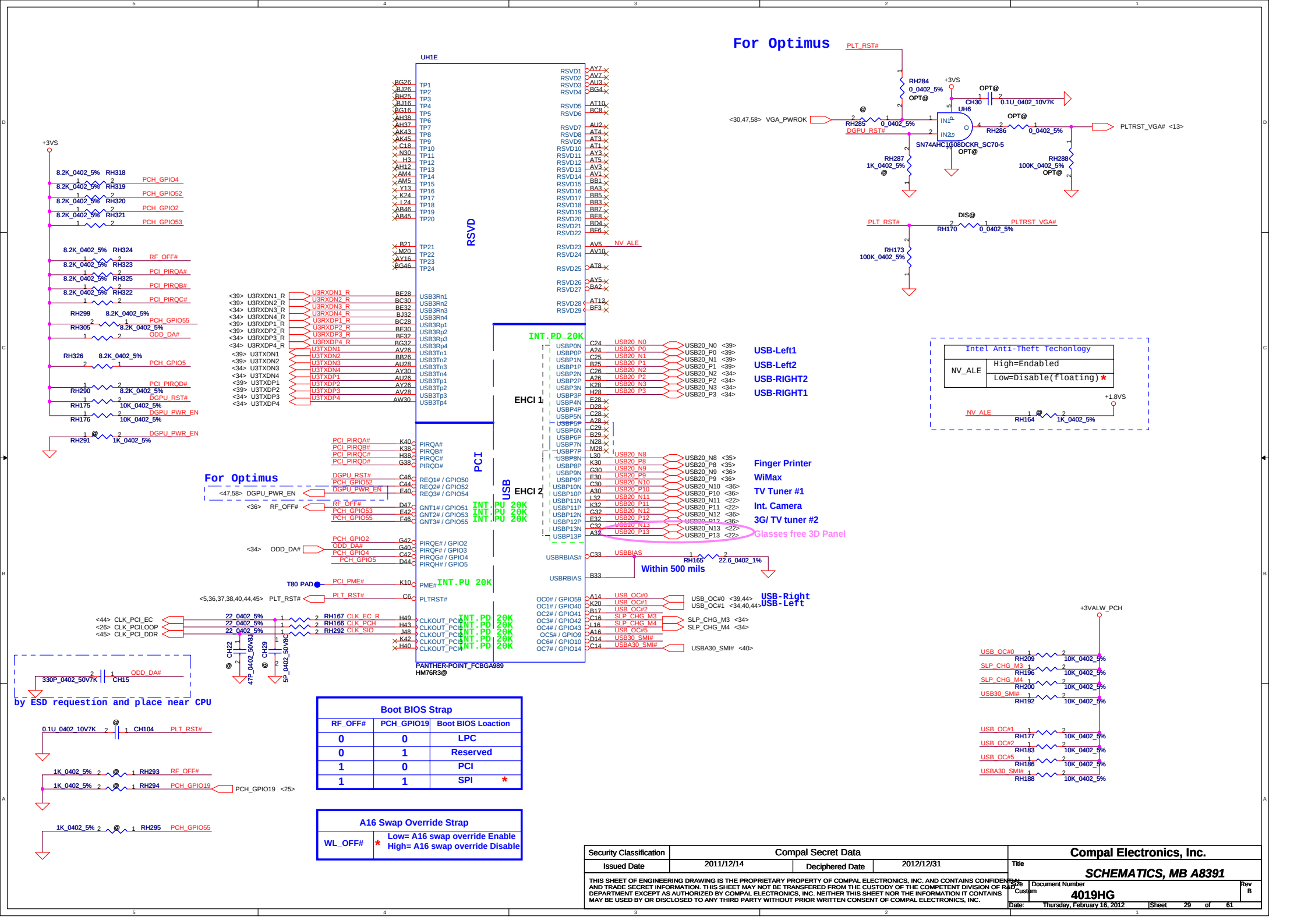
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

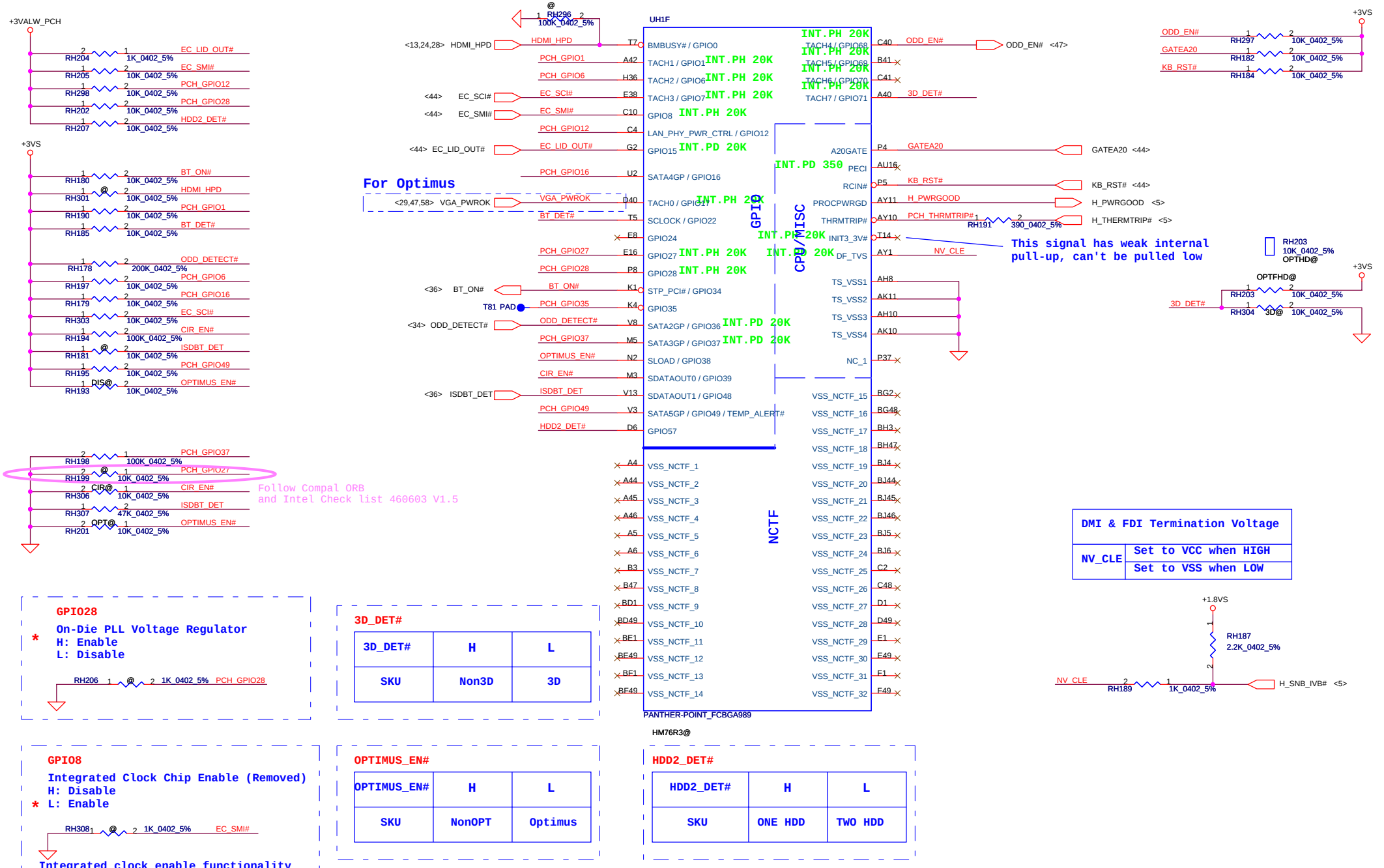
Compal Electronics, Inc.

Title: ***SCHEMATICS, MB A8391***

Size: Custom | Document Number: **4019HG** | Rev: B

Date: Thursday, February 16, 2012 | Sheet 28 of 61


For Optimus
UH1E
RSVD
PCI
USB
EHCI 1
EHCI 2
PANTHER-POINT_FCBGA989
HM76R3@
INT.PD_20K
INT.PU 20K
INT.PD 20K
USB-Left1
USB-Left2
USB-RIGHT2
USB-RIGHT1
Finger Printer
WiMax
TV Tuner #1
Int. Camera
3G/ TV tuner #2
Glasses free 3D Panel
USB-Right
USB-Left
Within 500 mils
For Optimus
by ESD requestion and place near CPU
Intel Anti-Theft Techonlogy
NV_ALE
High=Endabled
Low=Disable(floating)*
Boot BIOS Strap
RF_OFF#
PCH_GPIO19
Boot BIOS Loaction
0 0 LPC
0 1 Reserved
1 0 PCI
1 1 SPI *
A16 Swap Override Strap
WL_OFF# * Low= A16 swap override Enable
High= A16 swap override Disable
Security Classification
Compal Secret Data
Issued Date
2011/12/14
Deciphered Date
2012/12/31
Compal Electronics, Inc.
SCHEMATICS, MB A8391
4019HG
Size Custom
Rev B
Date: Thursday, February 16, 2012
Sheet 29 of 61



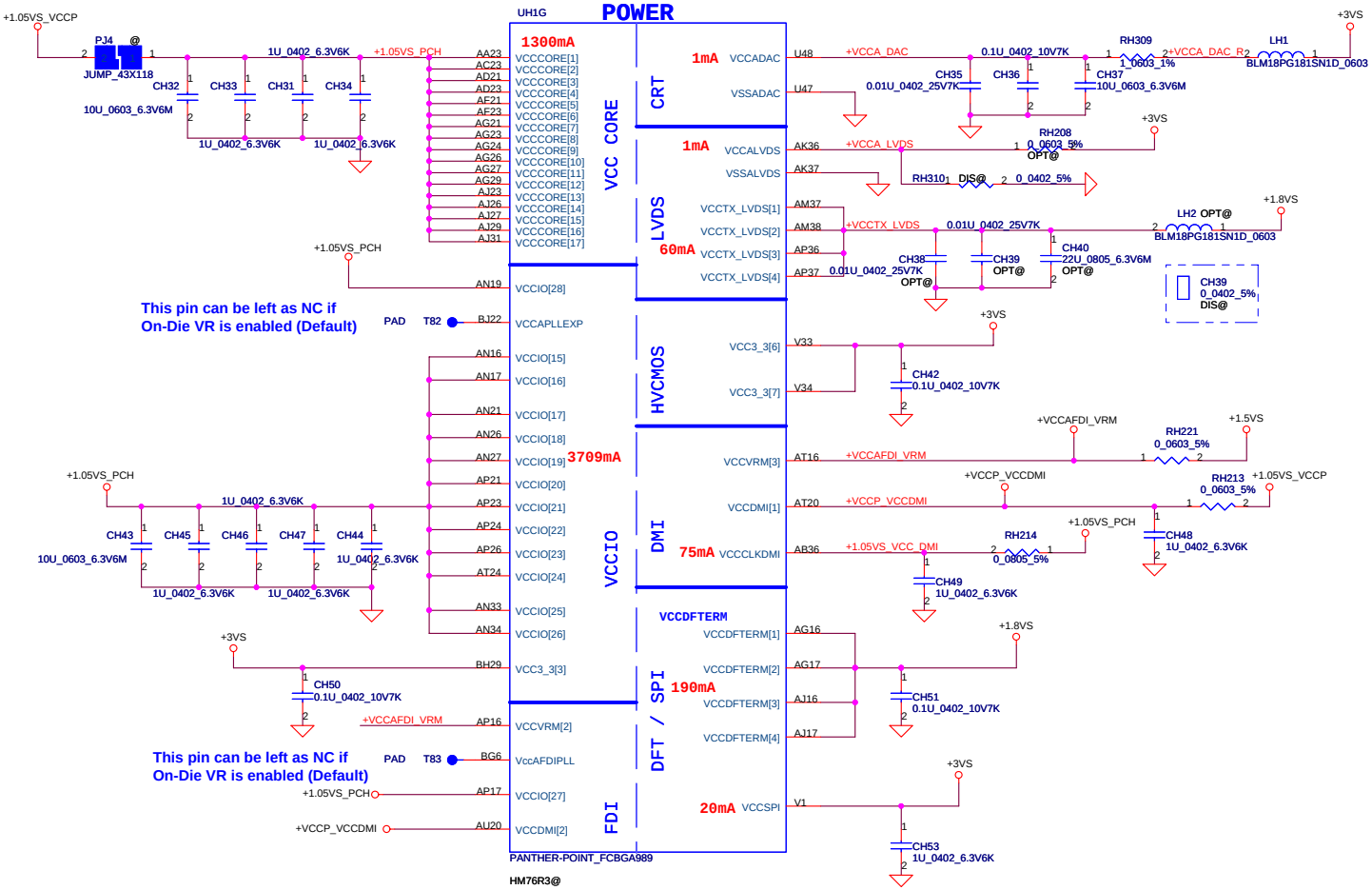
DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

3D_DET#	H	L
SKU	Non3D	3D

OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

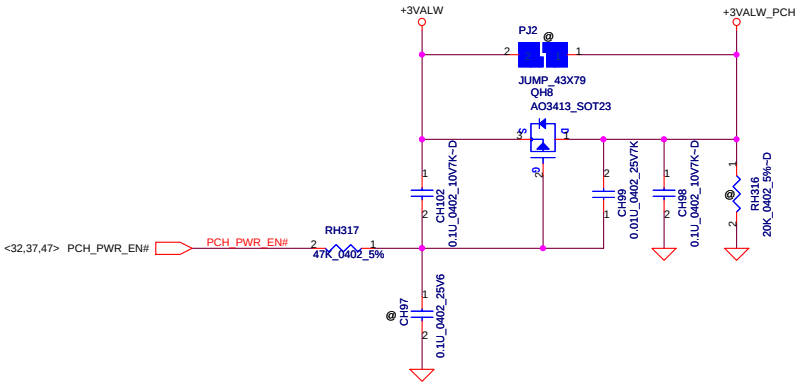
HDD2_DET#	H	L
SKU	ONE HDD	TWO HDD

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/12/14	Deciphered Date	2012/12/31
Title	SCHEMATICS, MB A8391		
Size B	Document Number 4019HG		Rev B
Date: Thursday, February 16, 2012	Sheet 30 of 61		



PCH Power Rail Table Refer to PCH EDS R1.0		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

+3VALW to +3V_PCH



Security Classification	Compal Secret Data		
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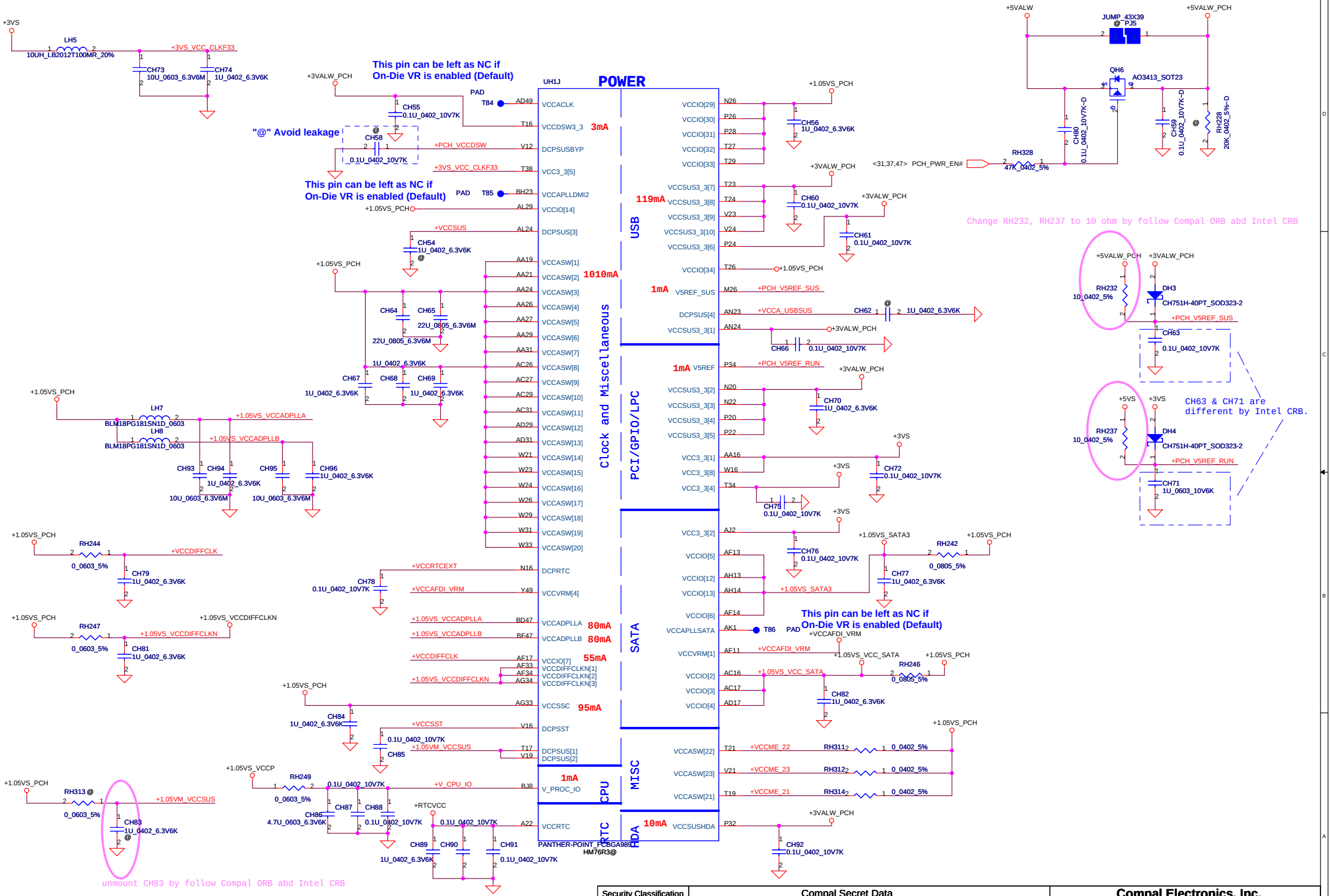
Compal Electronics, Inc.

Title: ***SCHEMATICS, MB A8391***

Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 Sheet 31 of 61



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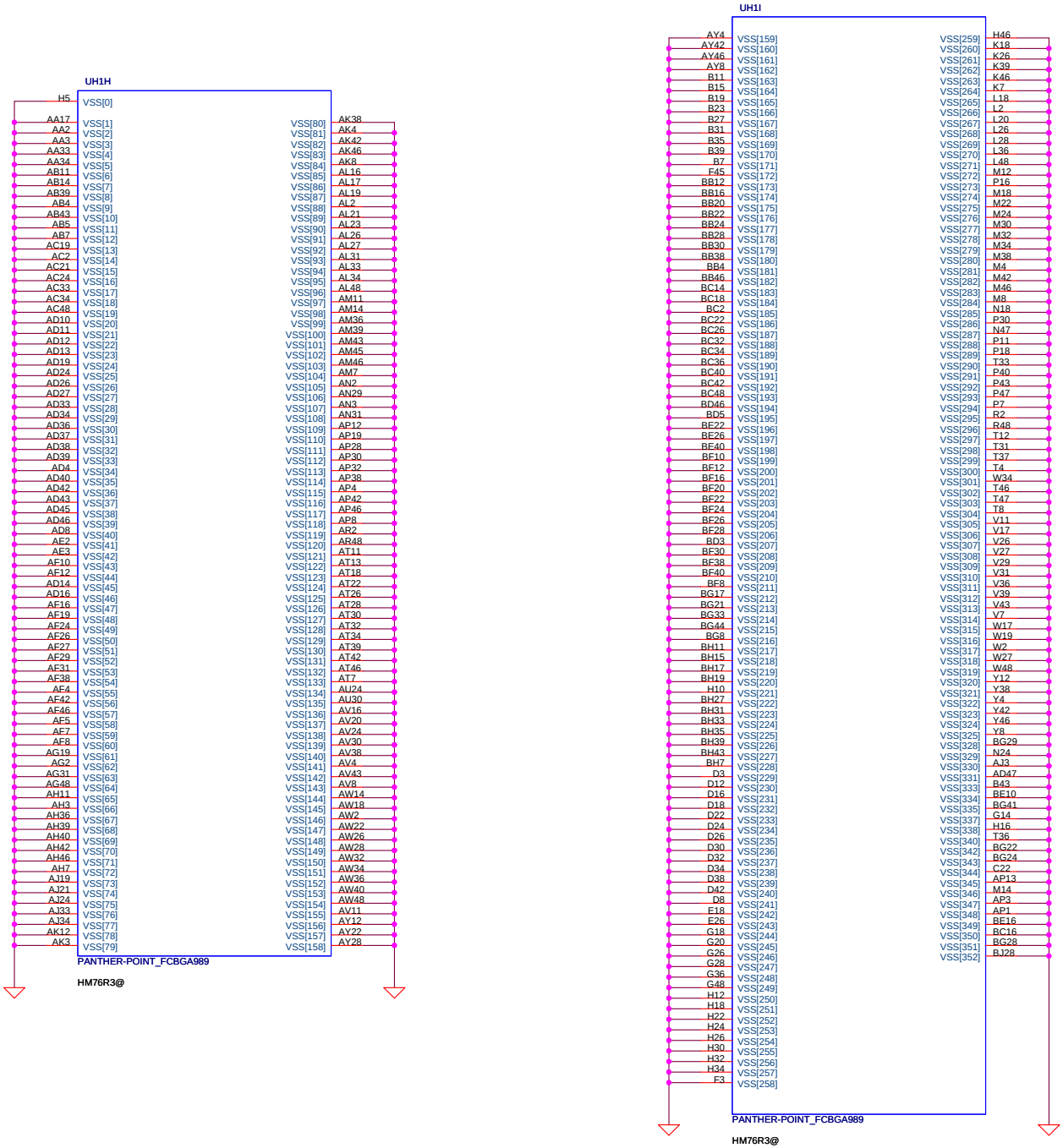
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8391		
Size	Custom	Document Number	4019HG
Rev	B		
Date:	Thursday, February 16, 2012	Sheet	32 of 61



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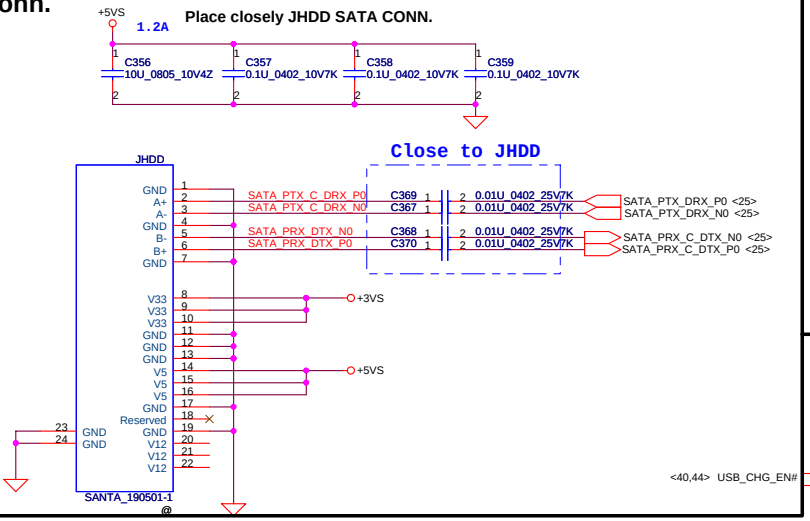
Title: ***SCHEMATICS, MB A8391***

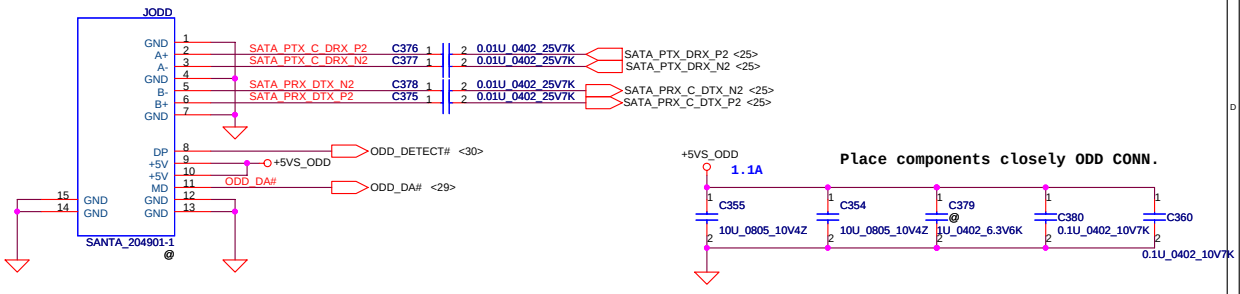
Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 Sheet 33 of 61

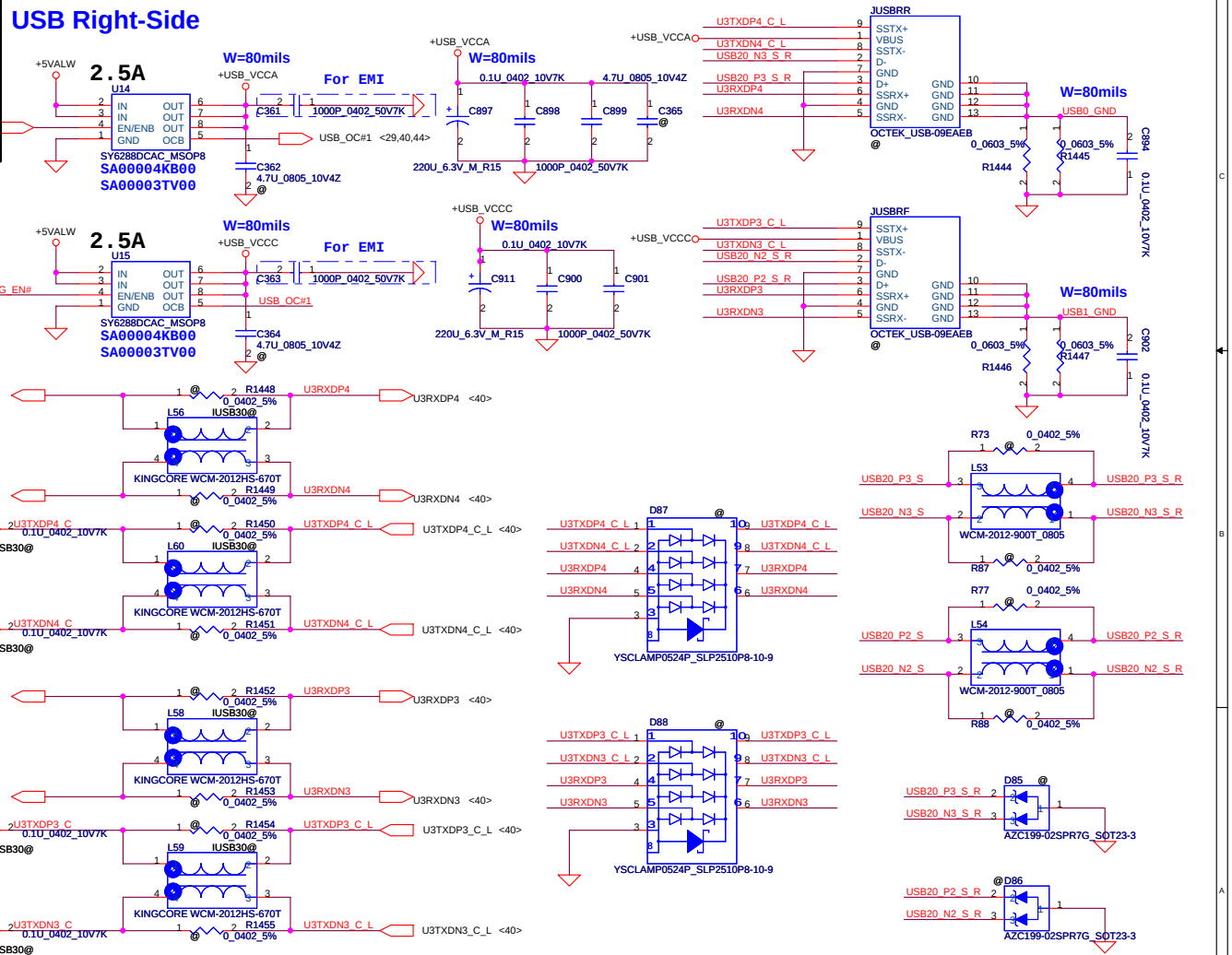
SATA HDD Conn.



SATA ODD Conn

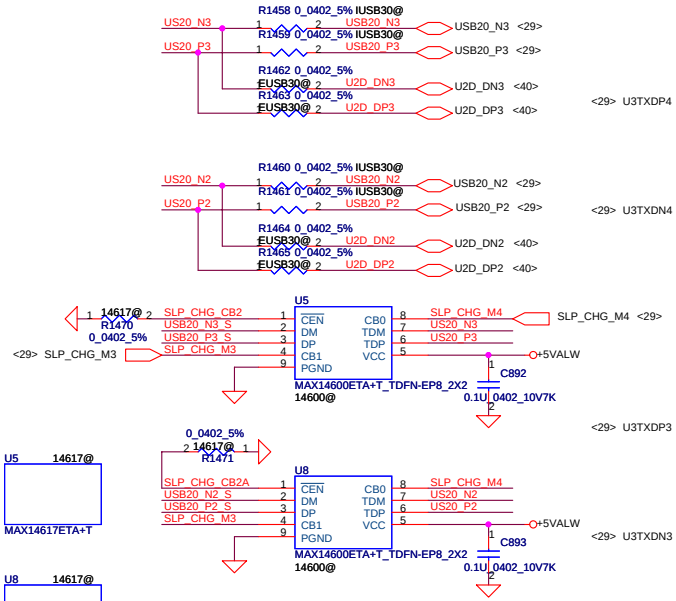


USB Right-Side



USB Sleep & Charge Auto-Mode/Mode3

MAX14600 & MAX14617			
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	CB2 (14617 only)	STATUS
0	0	0	AUTO MODE
0	1	0	Force Dedicated charger mode (MODE3)
1	0	0	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM
1	1	0	Pass-Through (USB) Mode with CDP Emulation: Auto Connect DP/DM to TDP/TDM depending on CDP status
X	X	1	Force Apple 2A Charger Mode: Apple 2A resistor dividers



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

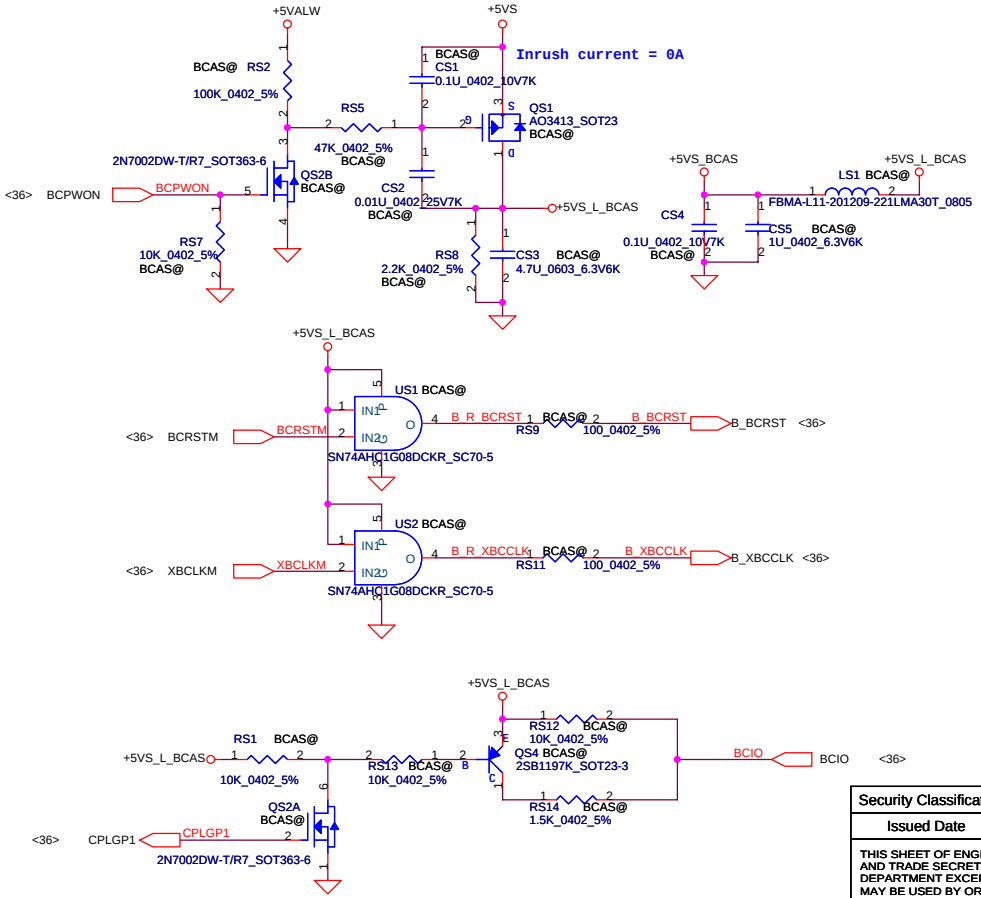
Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8391**

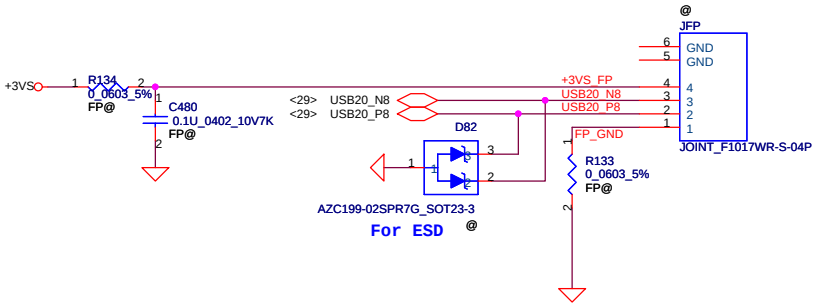
Size: | Document Number: **4019HG** | Rev: **B**

Date: Thursday, February 16, 2012 | Sheet 34 of 61

B-CAS Circuit



Finger printer



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: SCHEMATICS, MB A8391			
Size	Document Number: 4019HG		Rev: B
Date: Thursday, February 16, 2012	Sheet 35 of 61		

Slot 1 Half PCIe Mini Card-WLAN/ WiMax

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H

For RF

For SED

40 mils

120 mils

2.75A

USB--TV#2

USB--3G/TV#1

B-CAS

Close to J3GTV

Add BCCDET pull down

please place near J3GTV

For isolate Intel Rainbow Peak and Compal Debug Card.

WLAN/ WiFi

WiMax

Debug card using

To avoid LED flashing

SA000058Z00

EMI request 11/06

EMI request 12/17

Reserved for Swing Level adjustment (Close GCLK side)

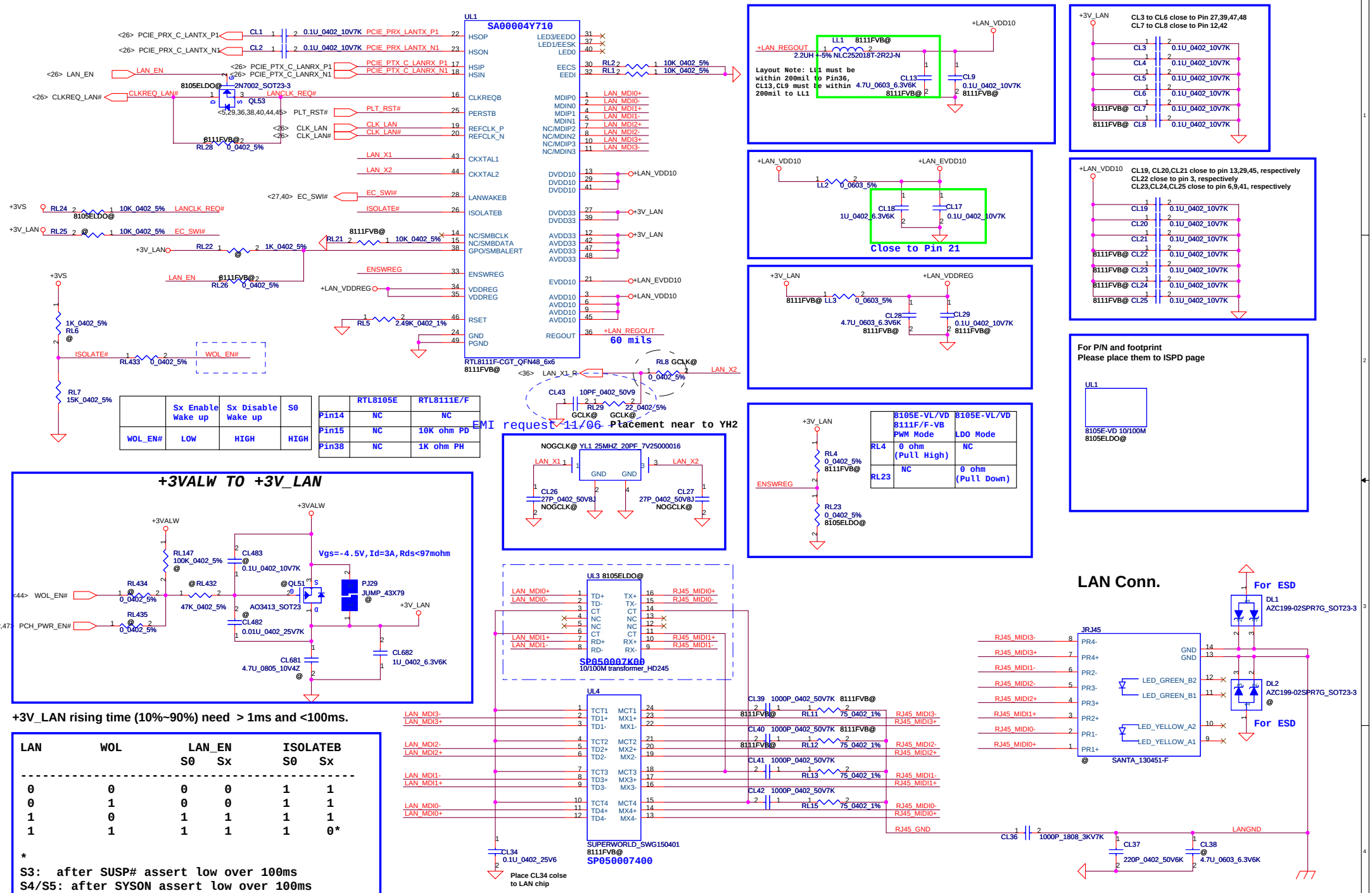
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

Size | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 36 of 61



	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

	RTL8105E	RTL8111E/F
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PH

	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VD LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

Security Classification	Compal Secret Data	
Issued Date	2011/12/14	Deciphered Date 2012/12/31

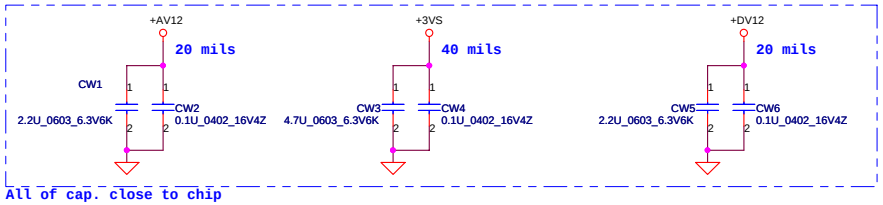
Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

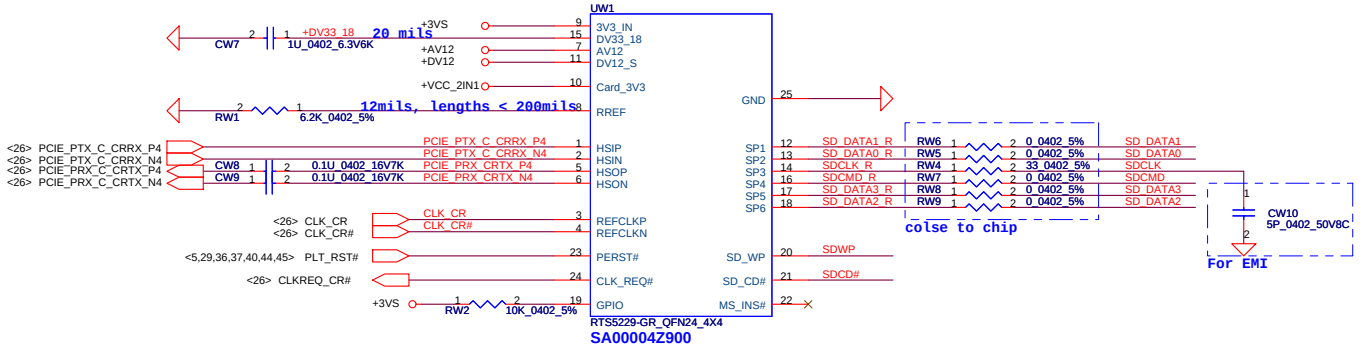
Size: Custom | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 37 of 61

All of cap. close to chip

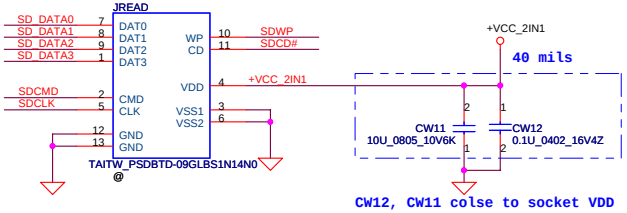


All of cap. close to chip



< 2 in 1 Card Reader >

Connector on bottom side



CW12, CW11 colse to socket VDD

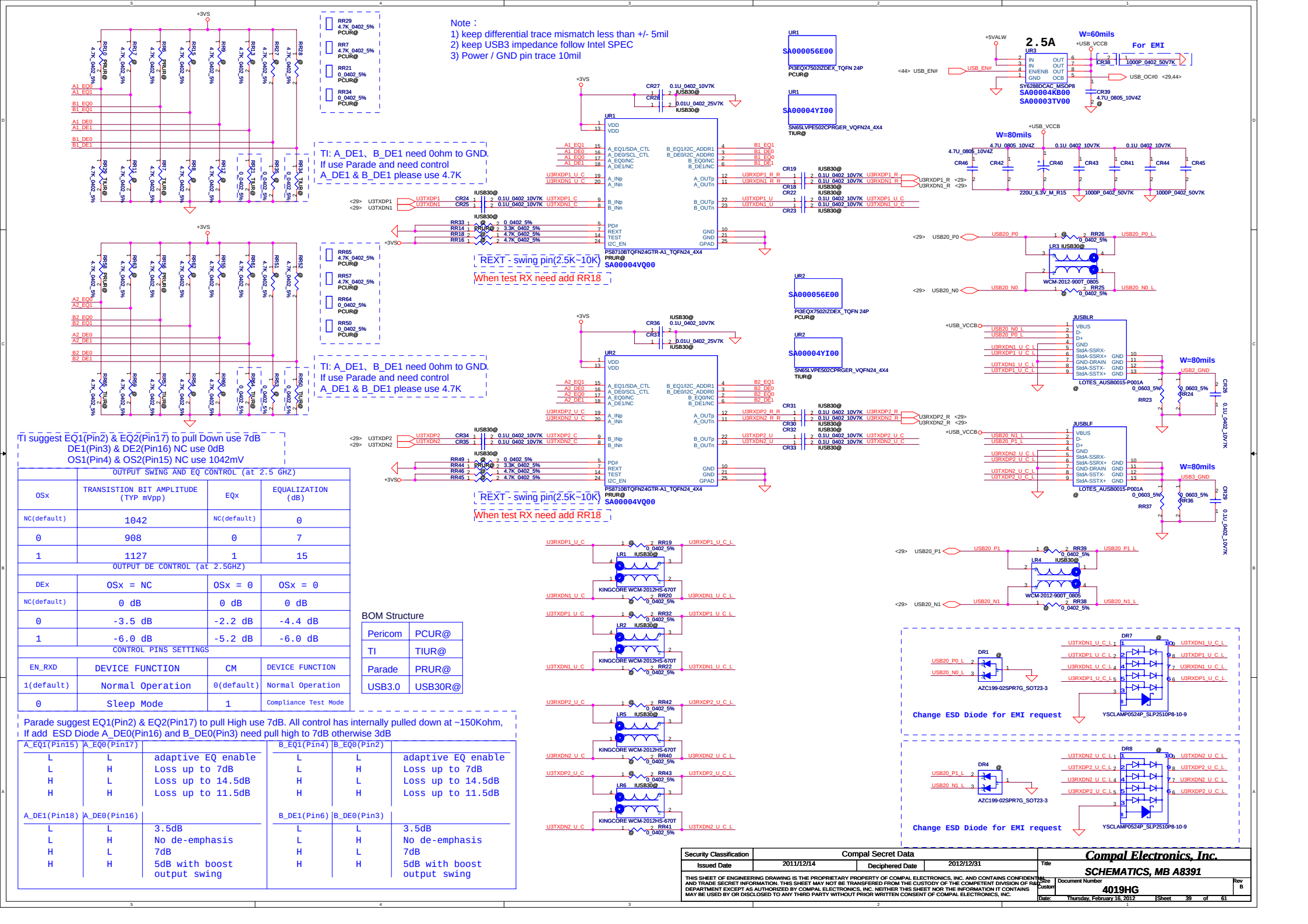
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

Size: Custom | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 38 of 61



TI suggest EQ1(Pin2) & EQ2(Pin17) to pull Down use 7dB
DE1(Pin3) & DE2(Pin16) NC use 0dB
OS1(Pin4) & OS2(Pin15) NC use 1042mV

OUTPUT SWING AND EQ CONTROL (at 2.5 GHZ)			
OSx	TRANSISTION BIT AMPLITUDE (TYP mVpp)	EQx	EQUALIZATION (dB)
NC(default)	1042	NC(default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5GHZ)			
DEx	OSx = NC	OSx = 0	OSx = 0
NC(default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION	CM	DEVICE FUNCTION
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode

BOM Structure

Pericom	PCUR@
TI	TIUR@
Parade	PRUR@
USB3.0	USB30R@

Parade suggest EQ1(Pin2) & EQ2(Pin17) to pull High use 7dB. All control has internally pulled down at ~150Kohm,
If add ESD Diode A_DE0(Pin16) and B_DE0(Pin3) need pull high to 7dB otherwise 3dB

A_EQ1(Pin15)	A_EQ0(Pin17)	
L	L	adaptive EQ enable
L	H	Loss up to 7dB
H	L	Loss up to 14.5dB
H	H	Loss up to 11.5dB

B_EQ1(Pin4)	B_EQ0(Pin2)	
L	L	adaptive EQ enable
L	H	Loss up to 7dB
H	L	Loss up to 14.5dB
H	H	Loss up to 11.5dB

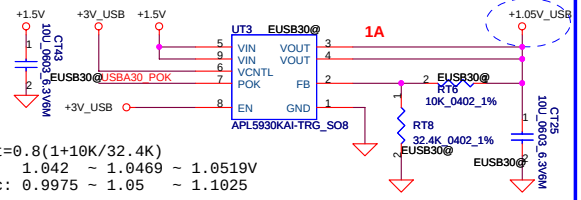
A_DE1(Pin18)	A_DE0(Pin16)	
L	L	3.5dB
L	H	No de-emphasis
H	L	7dB
H	H	5dB with boost output swing

B_DE1(Pin6)	B_DE0(Pin3)	
L	L	3.5dB
L	H	No de-emphasis
H	L	7dB
H	H	5dB with boost output swing

Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

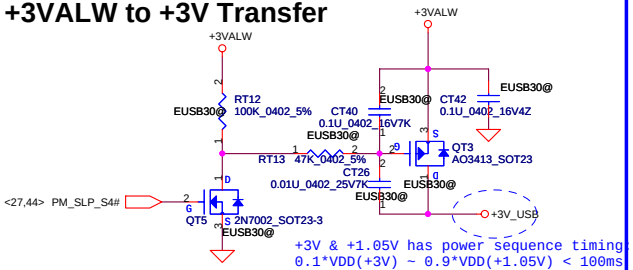
Title	Compal Electronics, Inc.
	SCHEMATICS, MB A8391
Size: Custom	Document Number: 4019HG
Rev: B	
Date: Thursday, February 16, 2012	Sheet 39 of 61

+1.5V to +1.05V Transfer

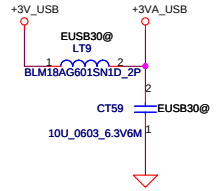


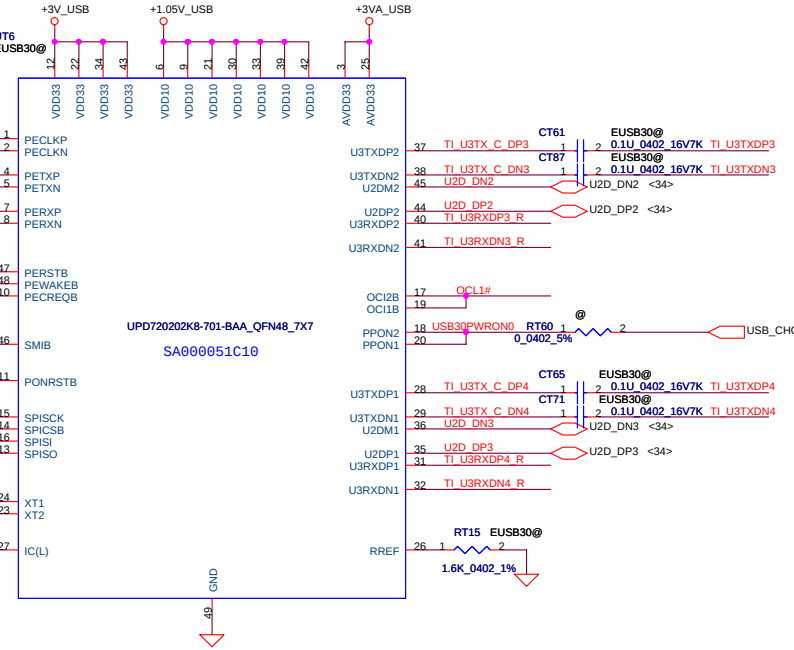
Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

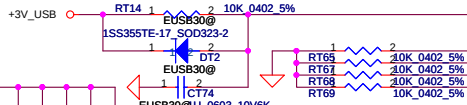


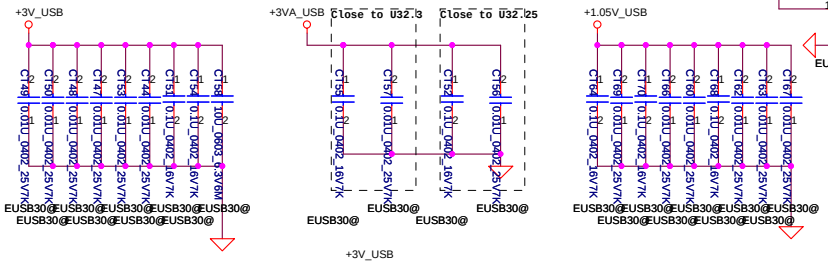
+3V & +1.05V has power sequence timing:
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms

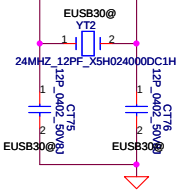


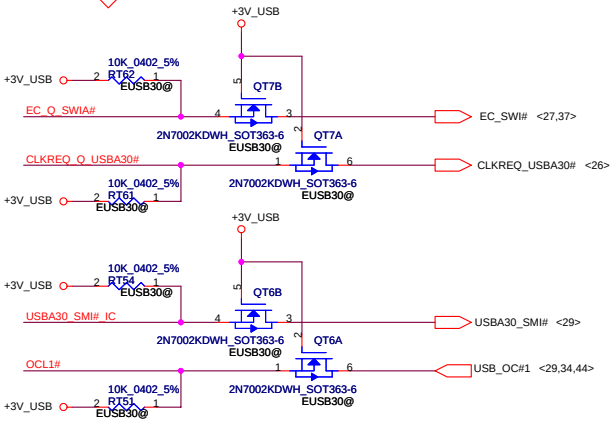


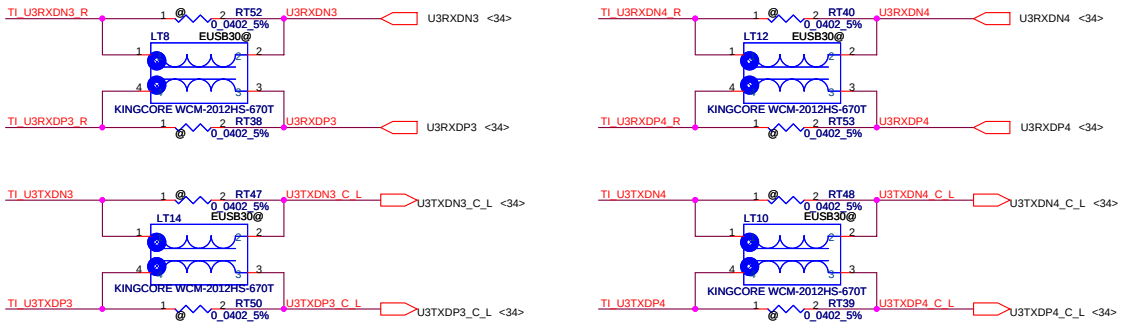
UPD720202:
SMIB Low active











Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: ***SCHEMATICS, MB A8391***

Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 | Sheet 40 of 61

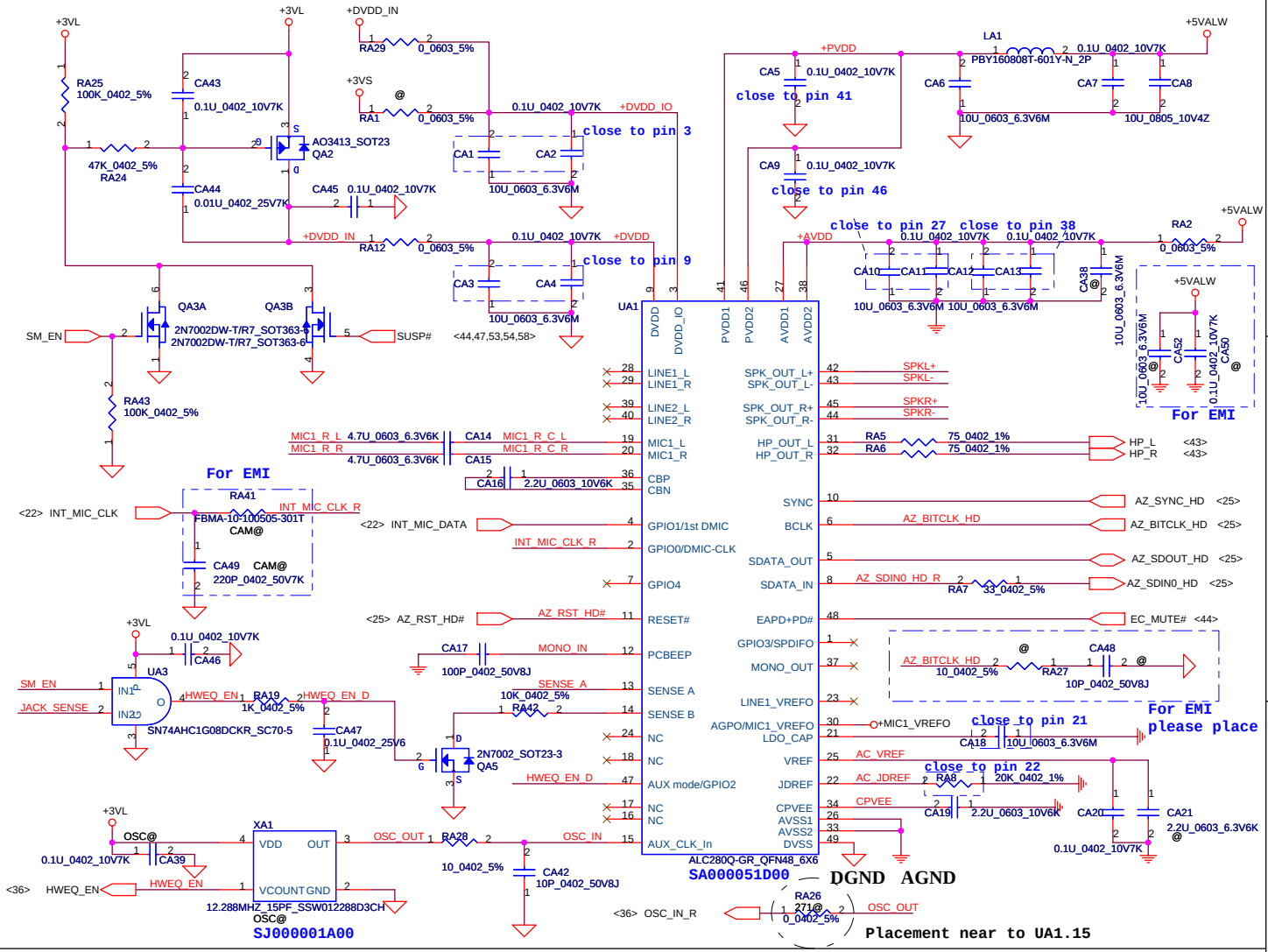
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

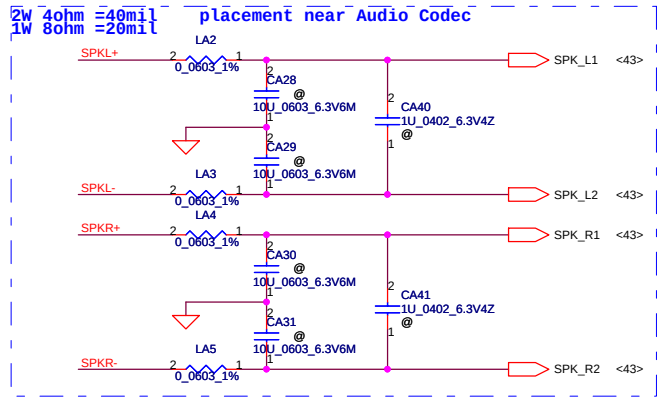
Compal Electronics, Inc.

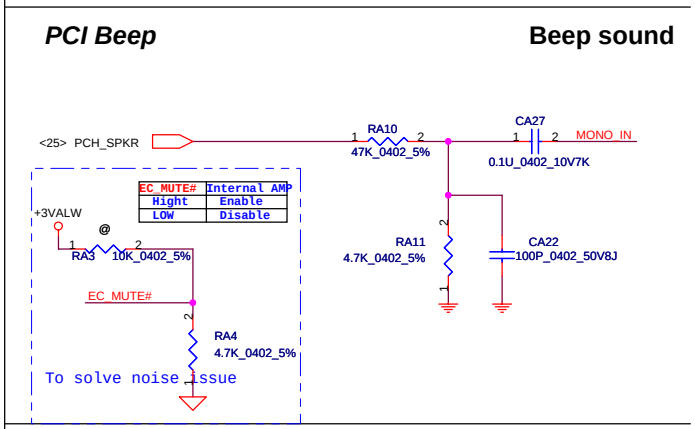
Title: ***SCHEMATICS, MB A8391***

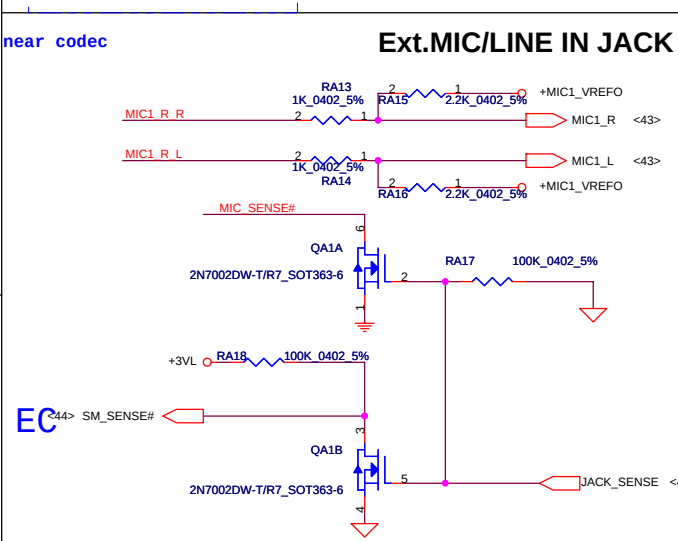
Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 | Sheet 41 of 61

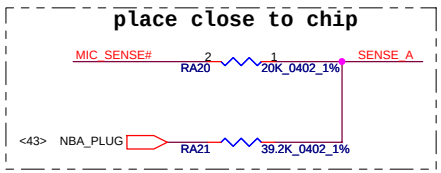


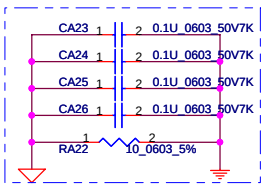






Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 31, 32)	Headphone out
	20K	PORT-B (PIN 19, 20)	Ext. MIC
	10K	PORT-C (PIN 28, 29)	
	5.1K	PORT-E	
SENSE B	39.2K		
	20K		
	10K		

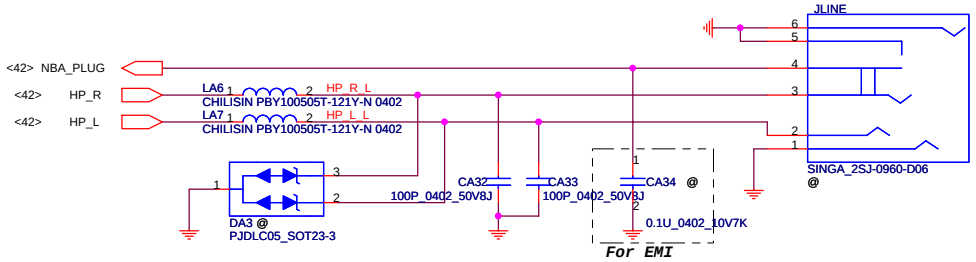




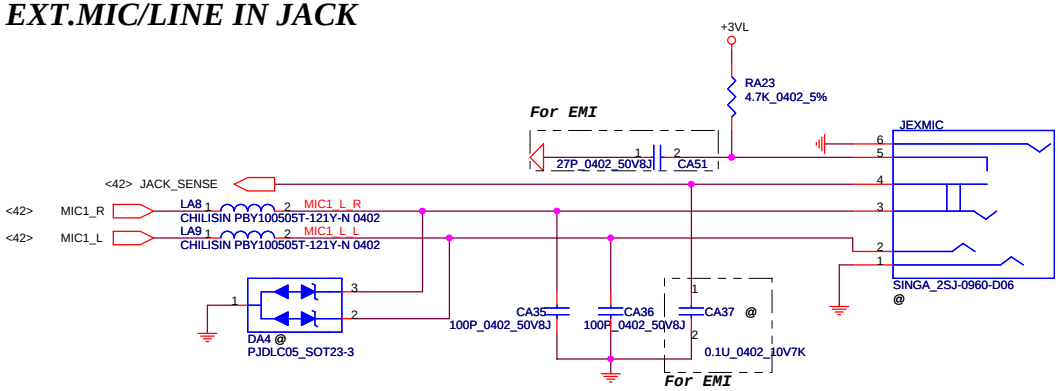
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8391		
Size	Document Number	4019HG	Rev B
Date: Thursday, February 16, 2012	Sheet 42 of 61		

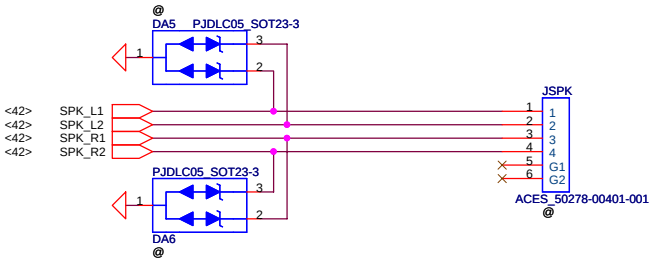
HeadPhone/LINE OUT JACK



EXT.MIC/LINE IN JACK



SPK CONN.



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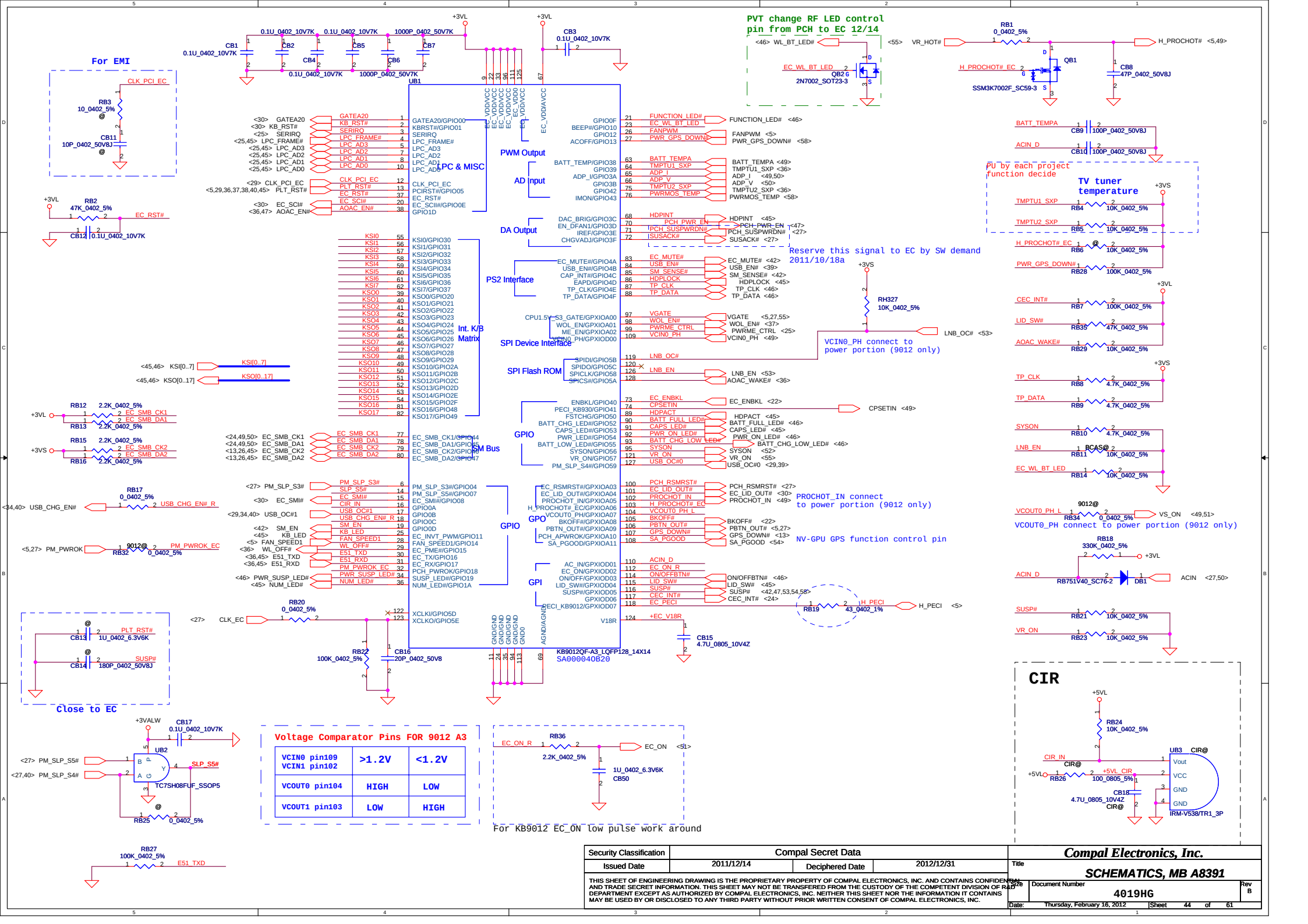
Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

Size | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 43 of 61



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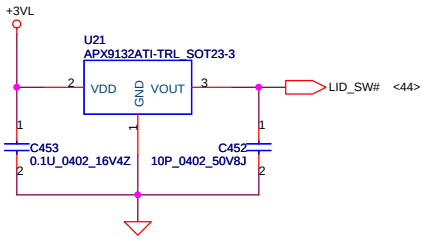
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8391		
Size	Document Number	4019HG	Rev B
Date: Thursday, February 16, 2012	Sheet 44 of 61		

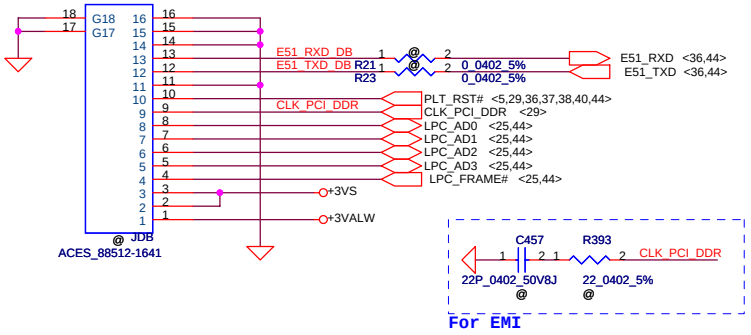
SPI Flash (128KB)

Lid SW

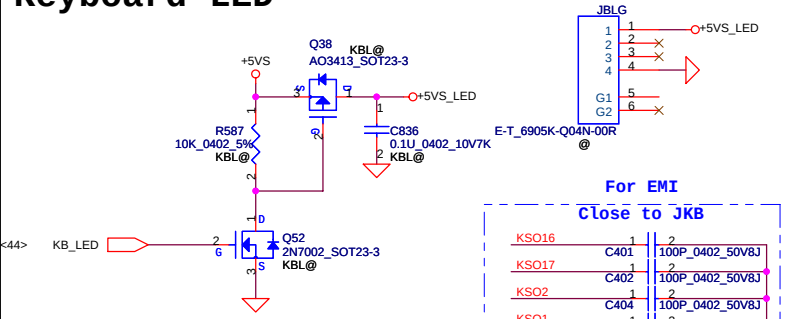


LPC Debug Port

Place the PAD under DDR DIMM.

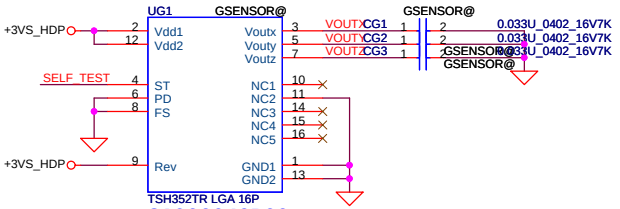


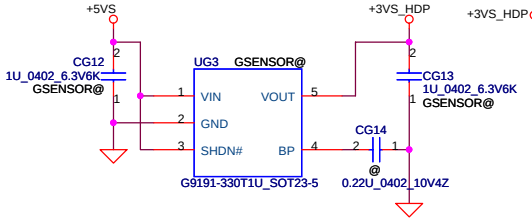
Keyboard LED

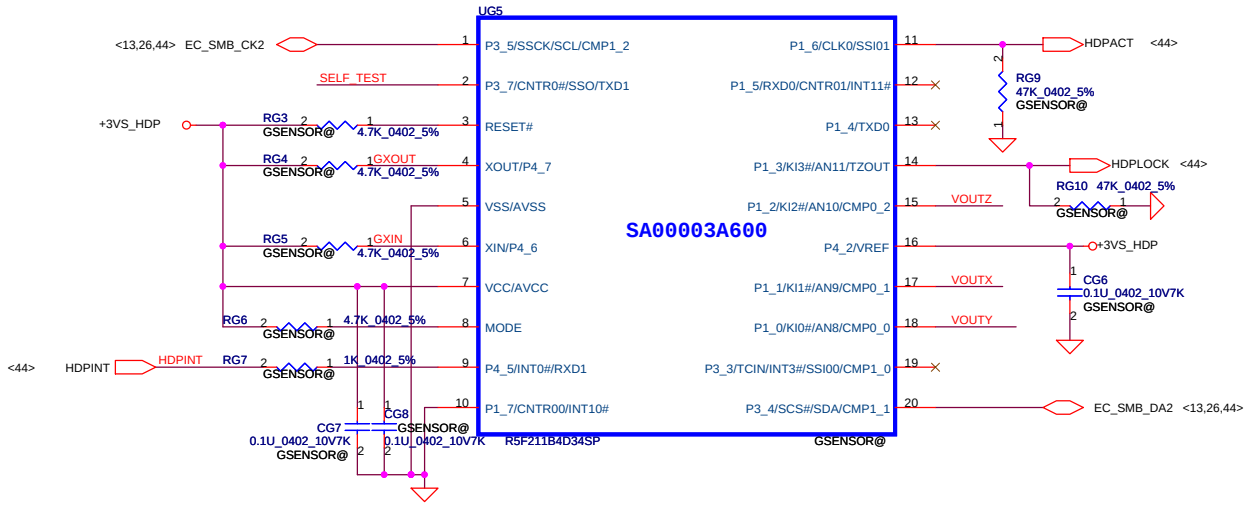


KEYBOARD CONN.

G-Sensor







Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

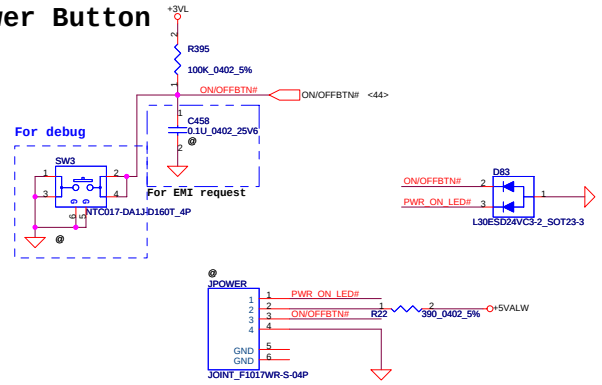
Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

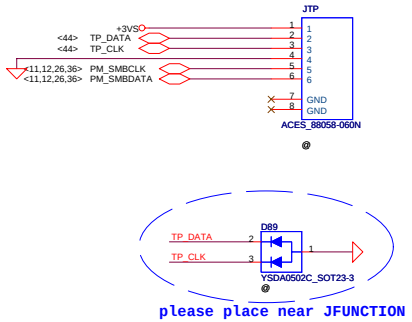
Size | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 45 of 61

Power Button

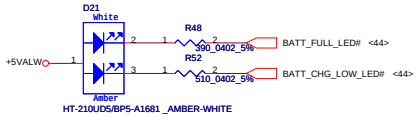


Touchpad Connector



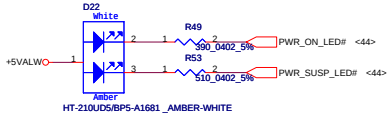
please place near JFUNCTION

BATT CHARGE /FULL LED & AC IN

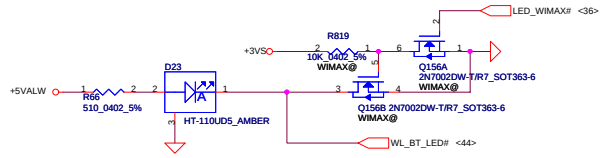


White LED bright when AC-adaptor is plugged and a Battery is full charged
Amber LED bright when charging battery from AC-adaptor
Amber LED blink during Critical Low battery

POWER LED



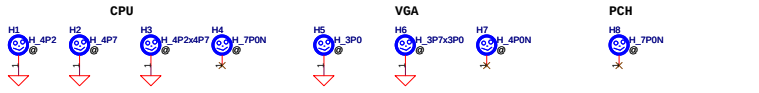
WiMAX LED



ESD solution

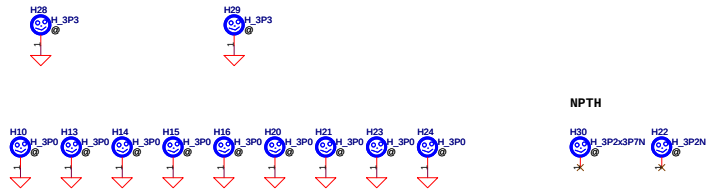
EMI solution

Screw Hole

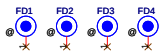


MINI CARD -- 3G

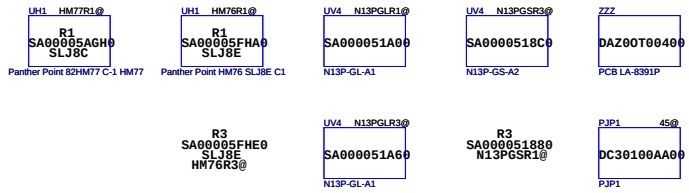
MINI CARD -- WLAN



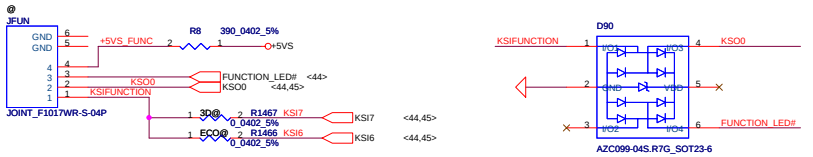
PCB Fedical Mark PAD



ISPD



FUNCTION/B Connector



Green LED SC500009S00 VF=2.8V~3.15V, Isink<15mA

White LED SC500004W00 VF=2.75V~3.15V, Isink<15mA

please place near JFUNCTION

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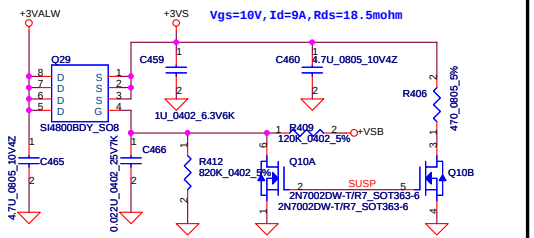
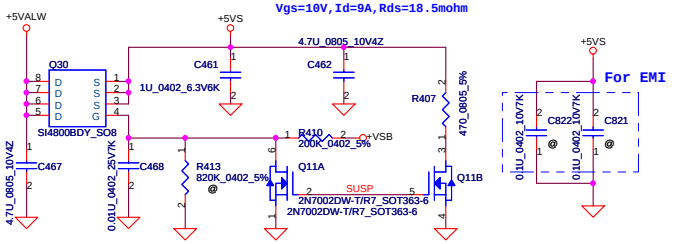
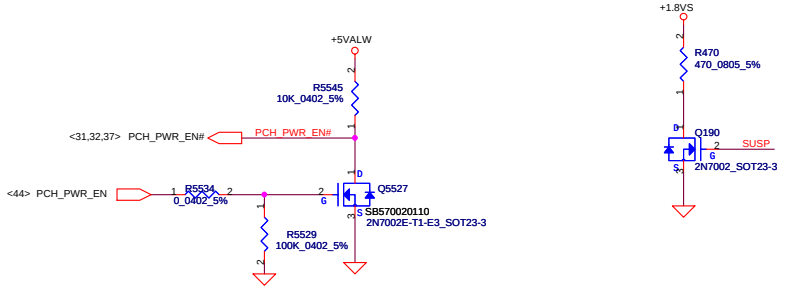
+3VALW TO +3VS

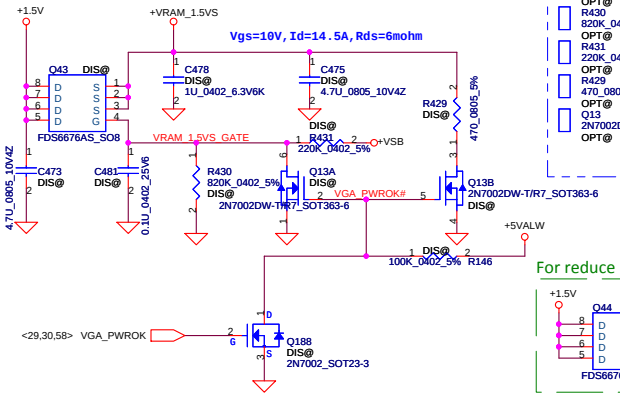


+5VALW TO +5VS



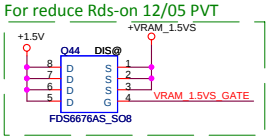


+1.5V to +VRAM_1.5VS

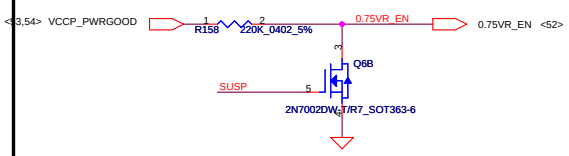


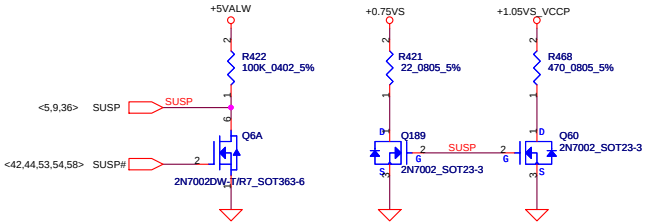
Q43 FDS6676AS_SO8 OPT@		C473 4.7U_0805_10V4Z OPT@	
C481 0.1U_0402_25V6 OPT@		C478 1U_0402_6.3V6K OPT@	
R430 820K_0402_5% OPT@		C475 4.7U_0805_10V4Z OPT@	
R431 220K_0402_5% OPT@		R146 100K_0402_5% OPT@	
R429 470_0805_5% OPT@		Q188 2N7002_SOT23-3 OPT@	
Q13 2N7002DW-T/R7_SOT363-6 OPT@		Q44 FDS6676AS_SO8 OPT@	

For reduce Rds-on 12/05 PVT



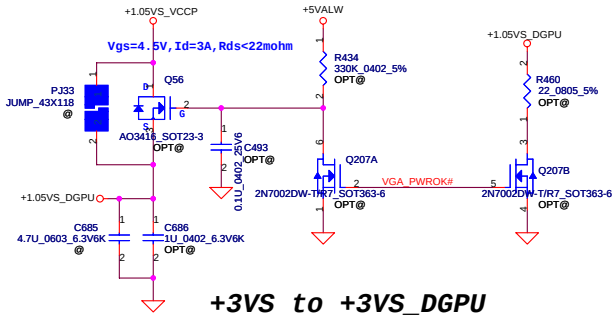
For S3 CPU Power Saving



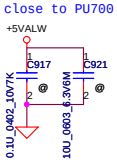


+1.05VS_VCCP to +1.05VS_DGPU

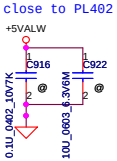
Short PJ33 for Discrete SKUs



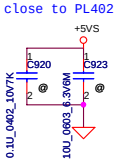
close to PU700



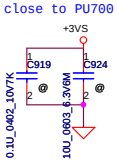
close to PL402



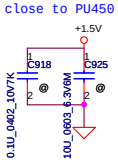
close to PL402



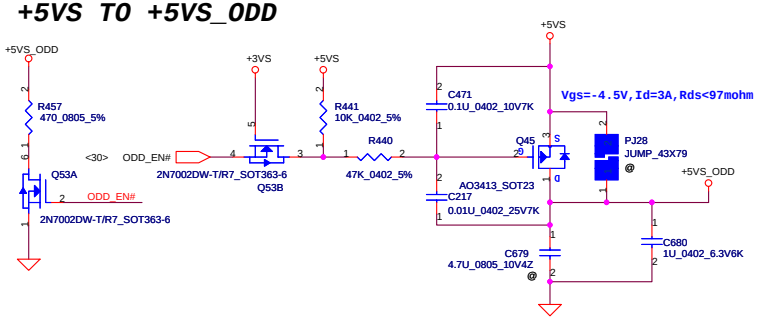
close to PU700



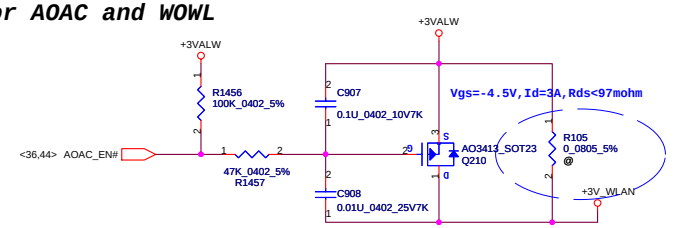
close to PU450



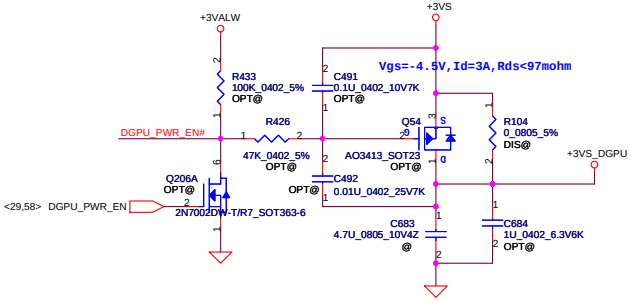
+5VS TO +5VS_ODD

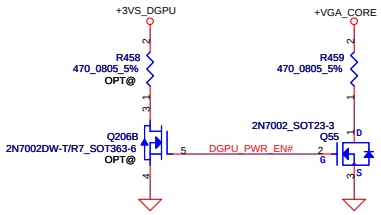


+3VALW TO +3V_WLAN for AOAC and WOWL



+3VS to +3VS_DGPU





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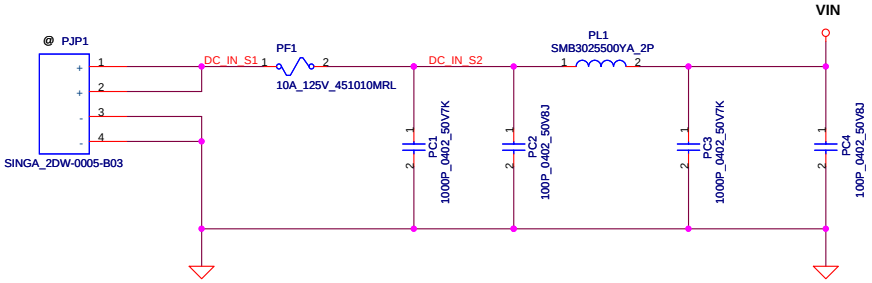
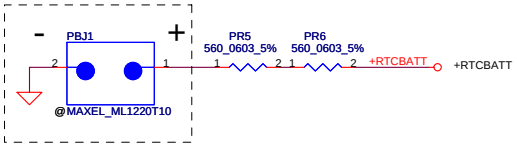
Title: SCHEMATICS, MB A8391

Size	Document Number	Rev
	4019HG	B

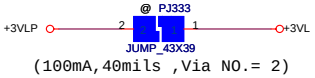
Date: Thursday, February 16, 2012 Sheet 47 of 61



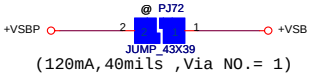
RTC Battery



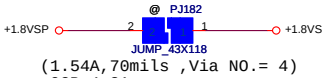
SP093MX0000



(100mA,40mils ,Via NO.= 2)

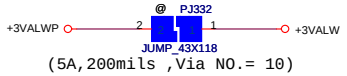


(120mA,40mils ,Via NO.= 1)

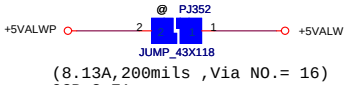


(1.54A,70mils ,Via NO.= 4)
OCP=4.2A

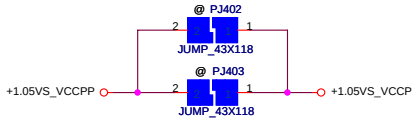
(0.5A,40mils ,Via NO.= 1)



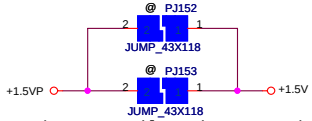
(5A,200mils ,Via NO.= 10)
OCP=6.2A



(8.13A,200mils ,Via NO.= 16)
OCP=8.7A



(17A,680mils ,Via NO.=34)
OCP=23.91A



(15A, 600mils ,Via NO.= 30)
OCP=18A

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

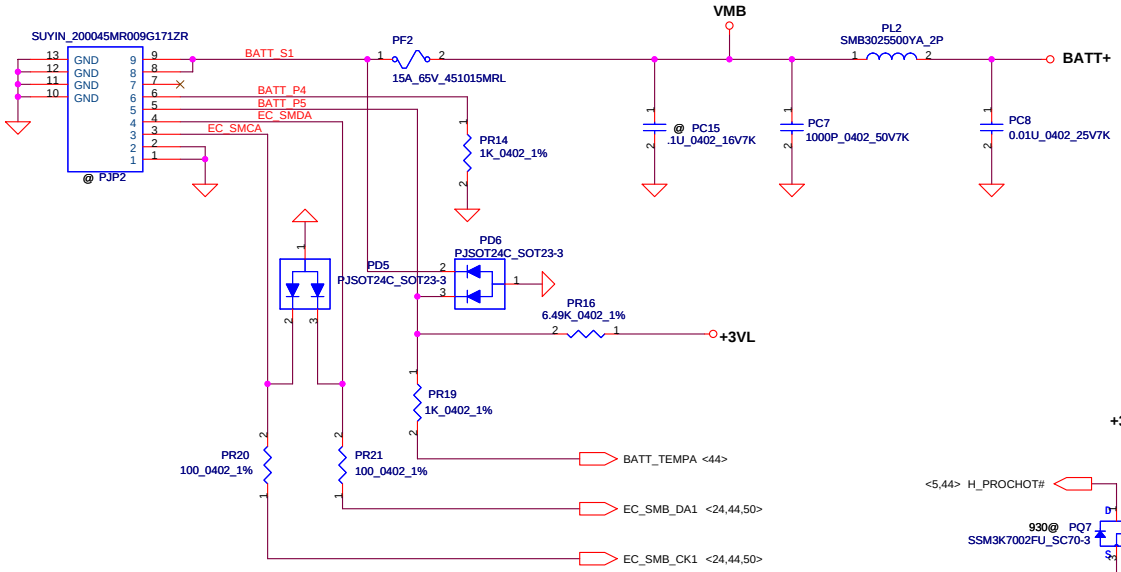
Size | Document Number: 4019HG | Rev: B

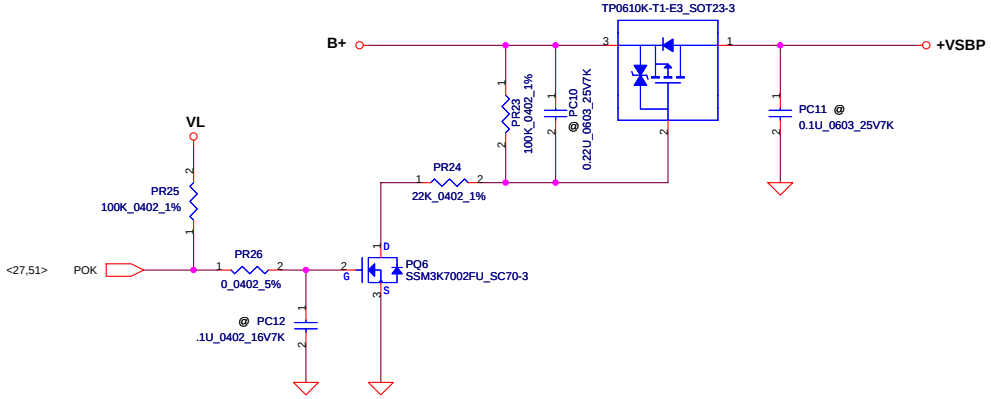
Date: Thursday, February 16, 2012 | Sheet 48 of 61

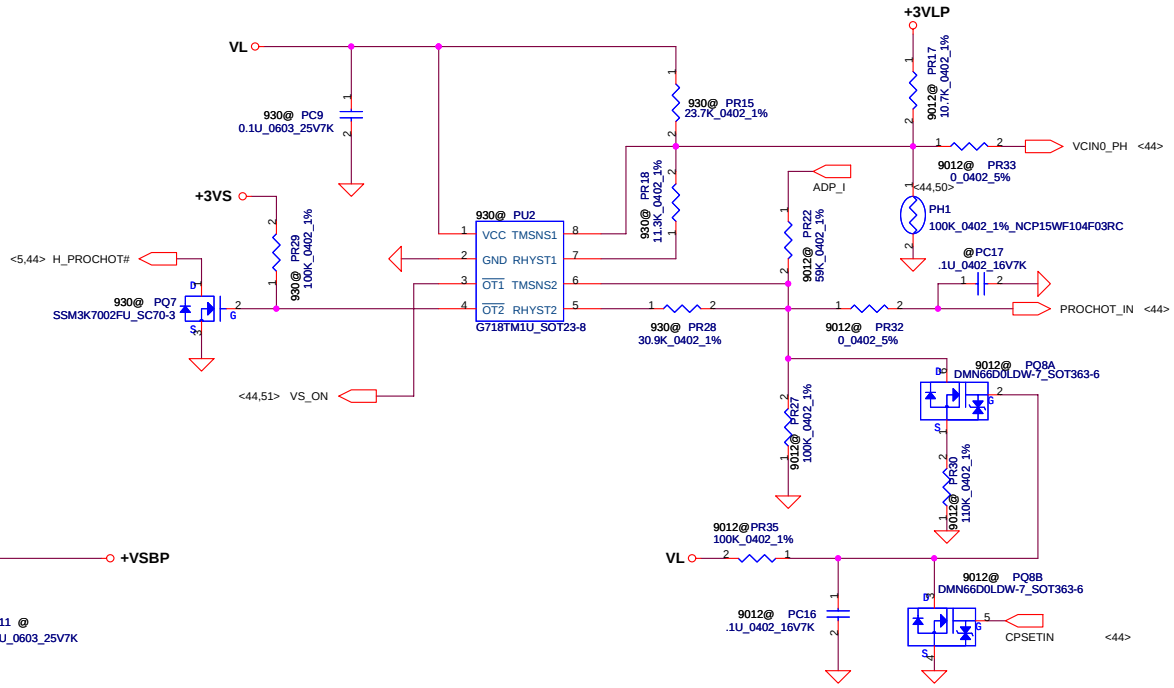
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
Rset = 3 * 7.87K = 23.61K ==> 23.7K
Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K







Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.504V	62.5W	1.308V

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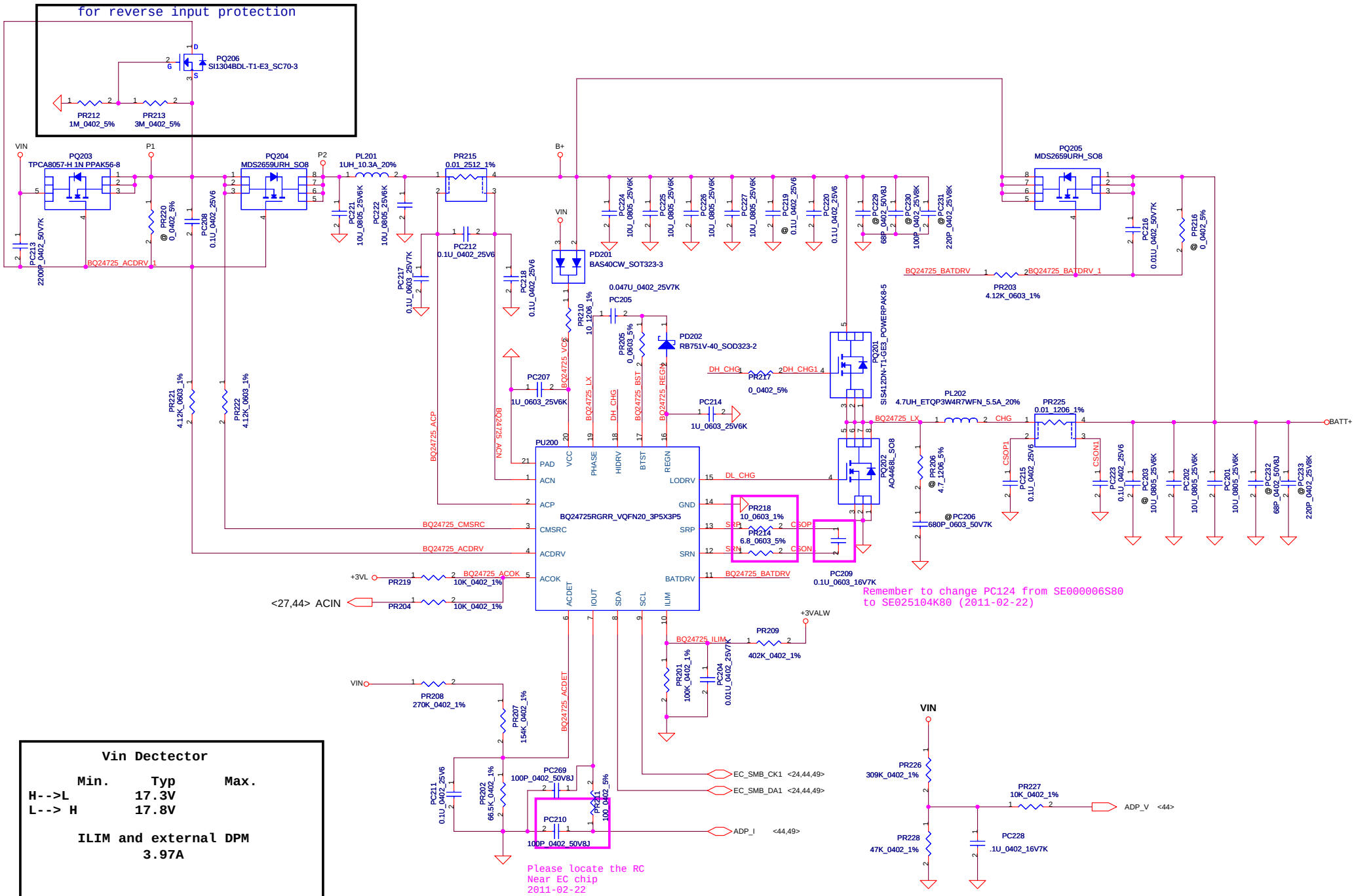
Title: SCHEMATICS, MB A8391

Size | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 49 of 61



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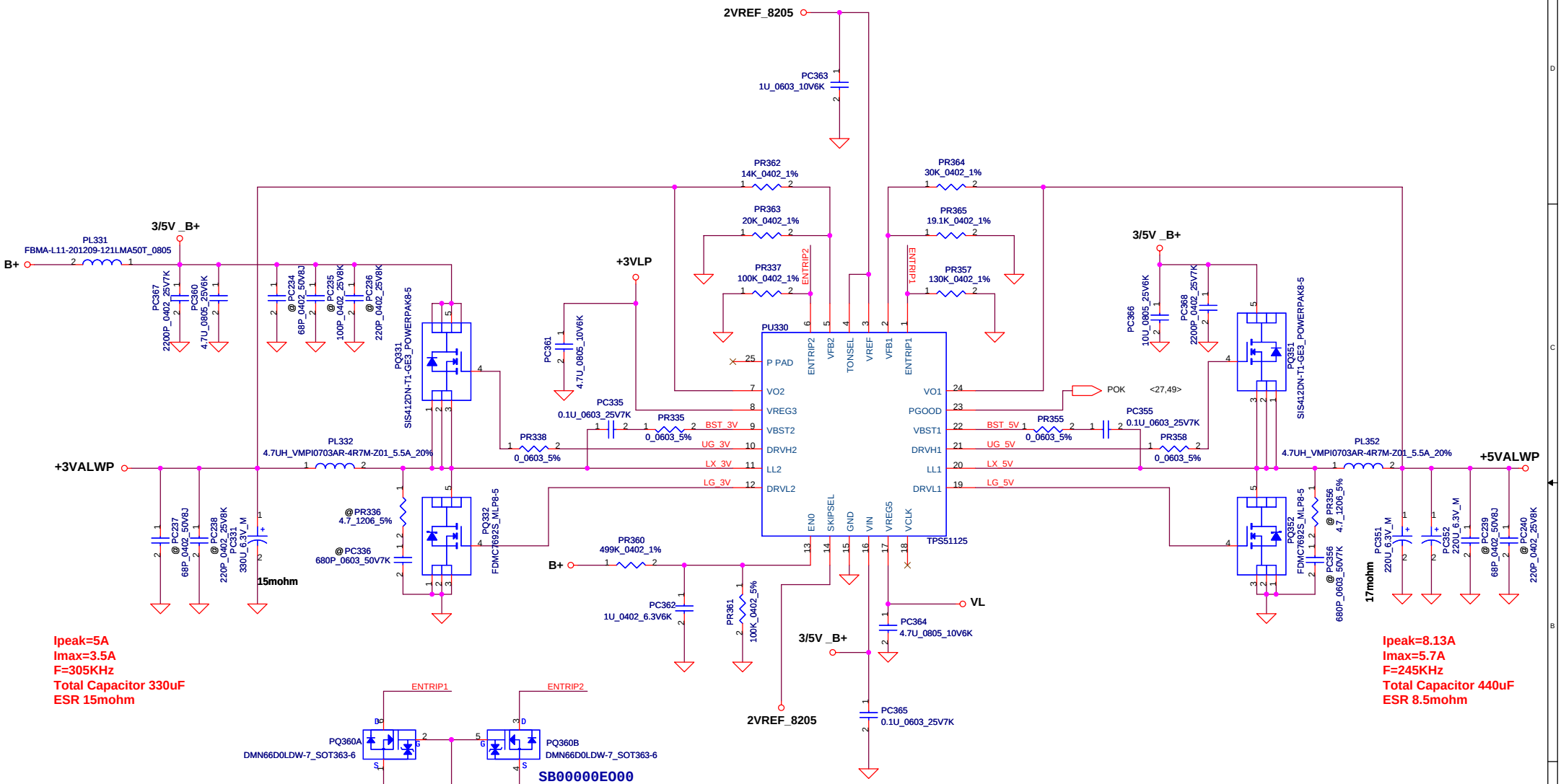
Size: Document Number: 4019HG Rev: B

Date: Thursday, February 16, 2012 Sheet 50 of 61



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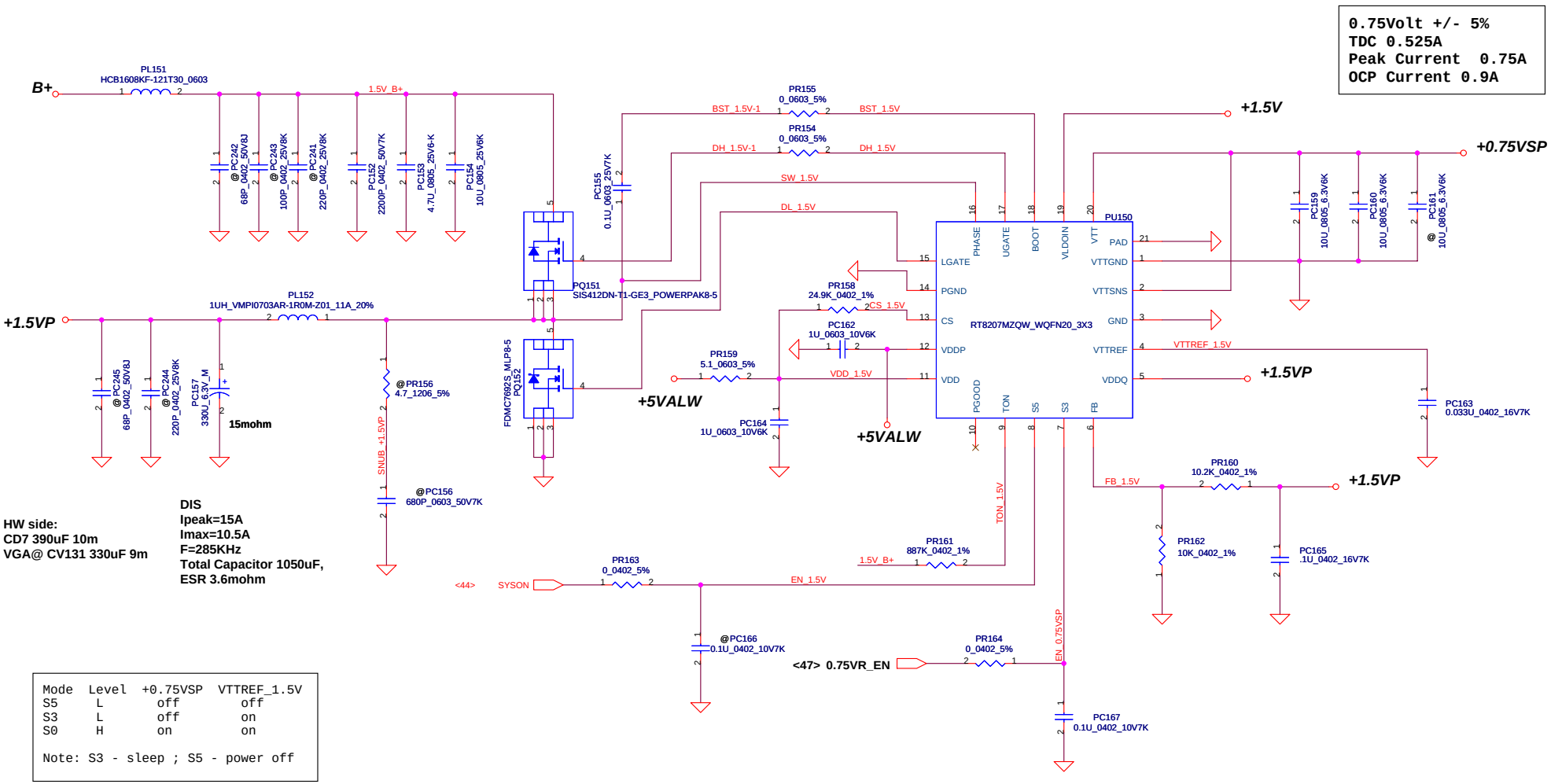
Title: SCHEMATICS, MB A8391

Size | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 51 of 61



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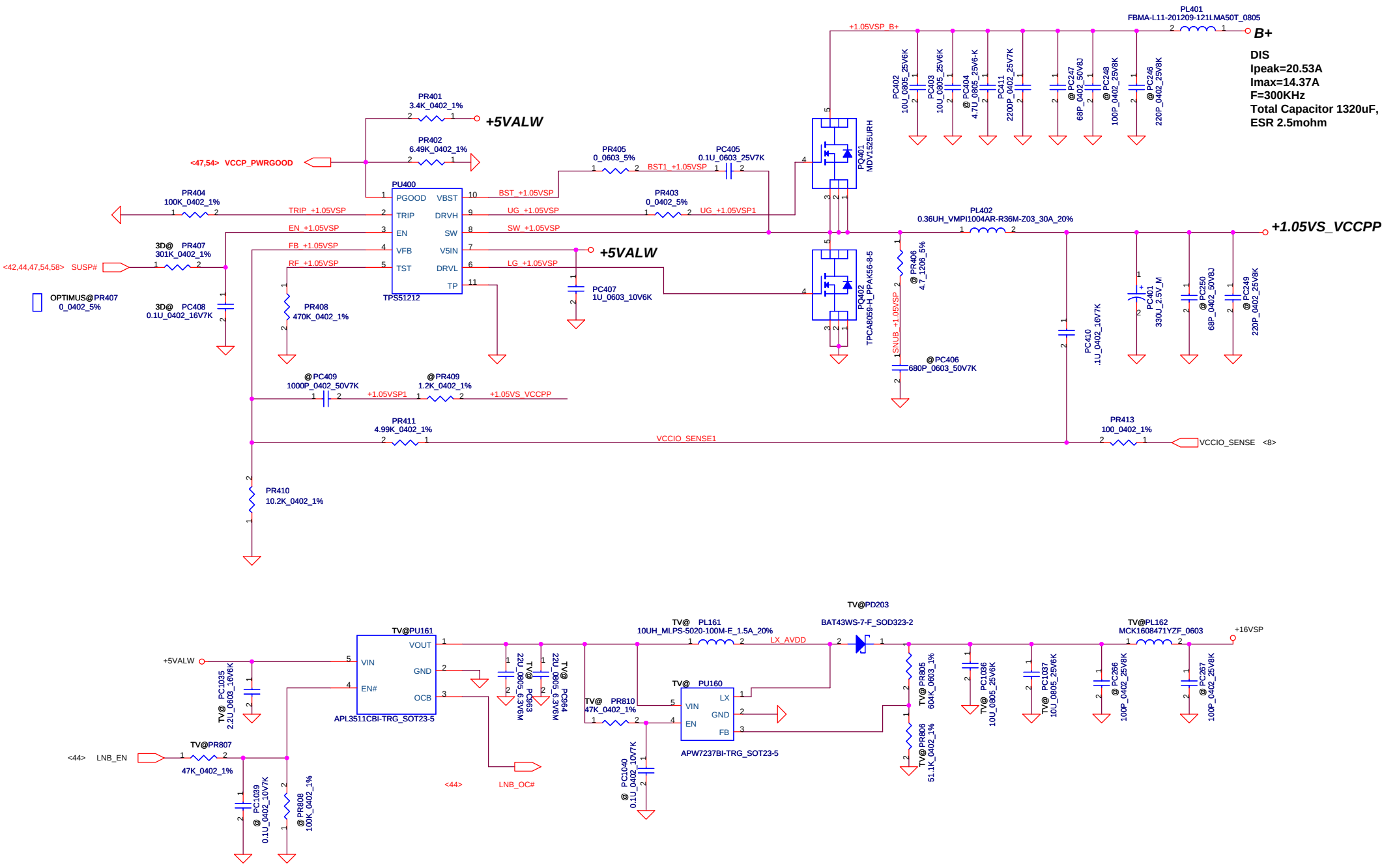
Title: SCHEMATICS, MB A8391

Size | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 52 of 61



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Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8391**

Size	Document Number	Rev
Custom	4019HG	B

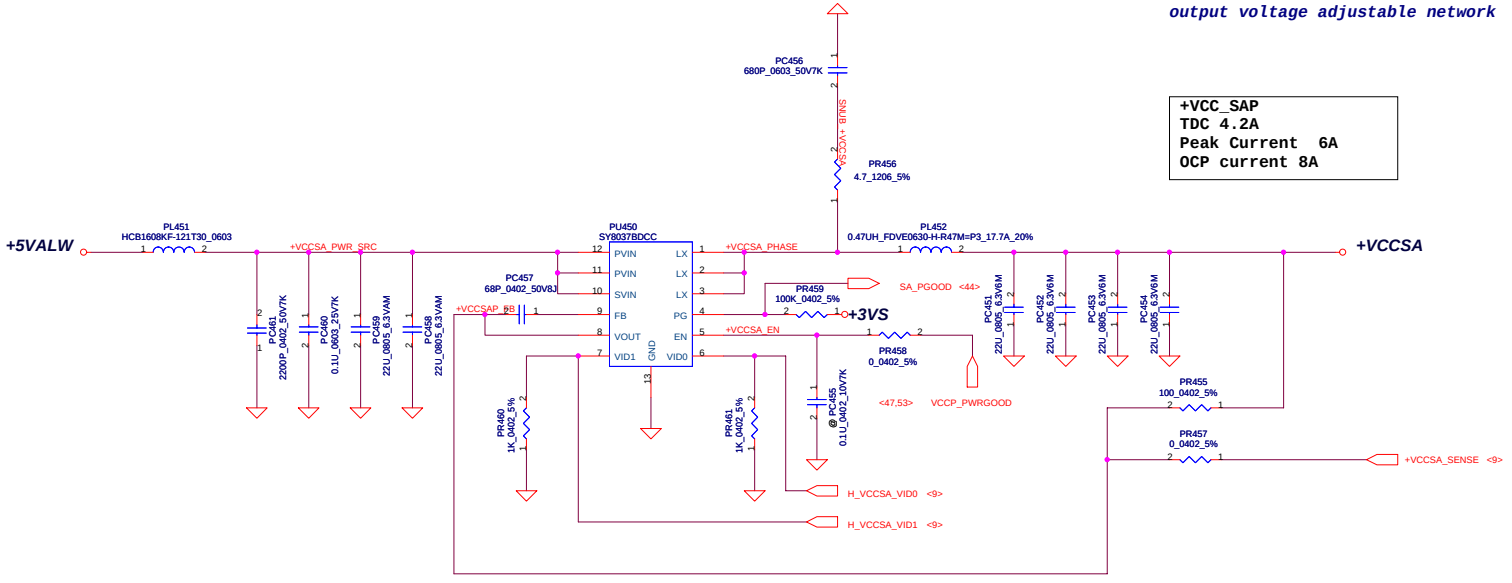
Date: Thursday, February 16, 2012 | Sheet 53 of 61

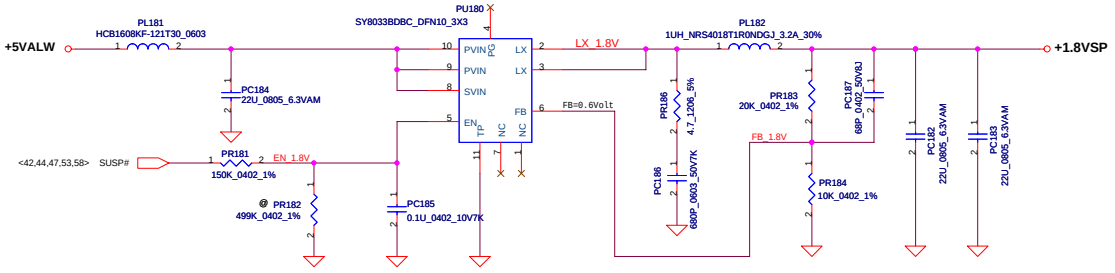
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 8A





Ipeak=1.308A
ILIM = 4A
F=1MHz

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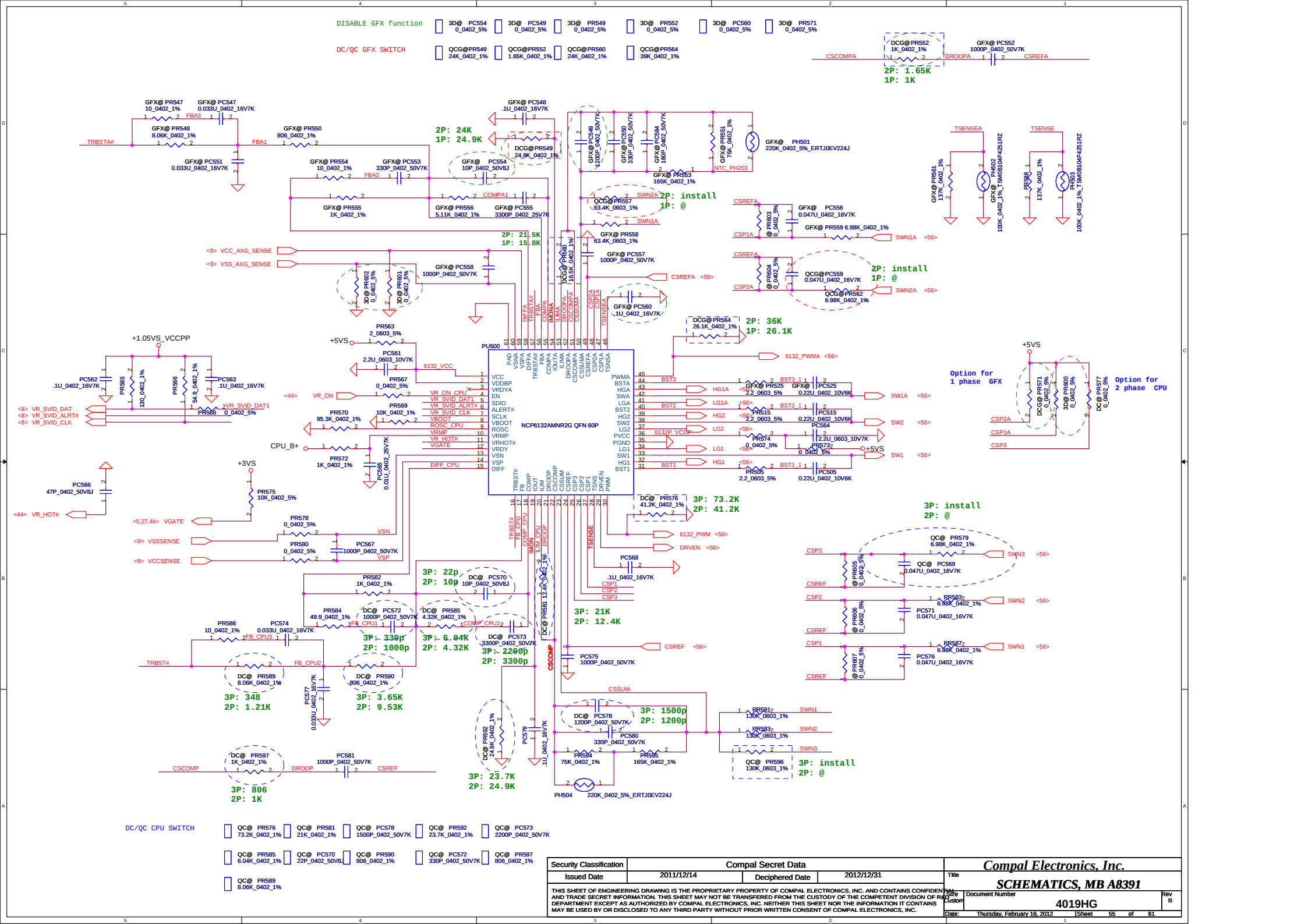
Compal Electronics, Inc.

Title: **SCHEMATICS, MB A8391**

Size	Document Number	Rev
C	4019HG	B

Date: Thursday, February 16, 2012 | Sheet 54 of 61



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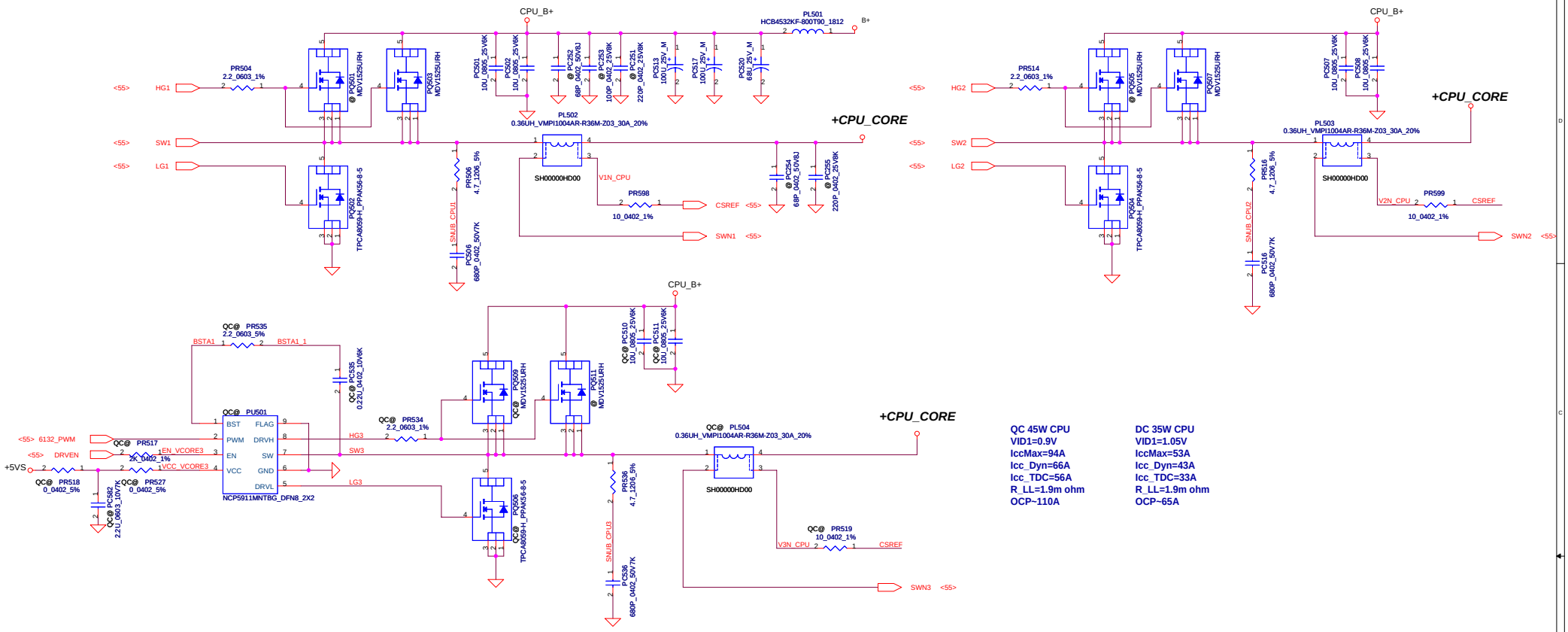
Title: SCHEMATICS, MB A8391

Size: Custom	Document Number: 4019HG	Rev: B
Date: Thursday, February 16, 2012	Sheet 55 of 61	



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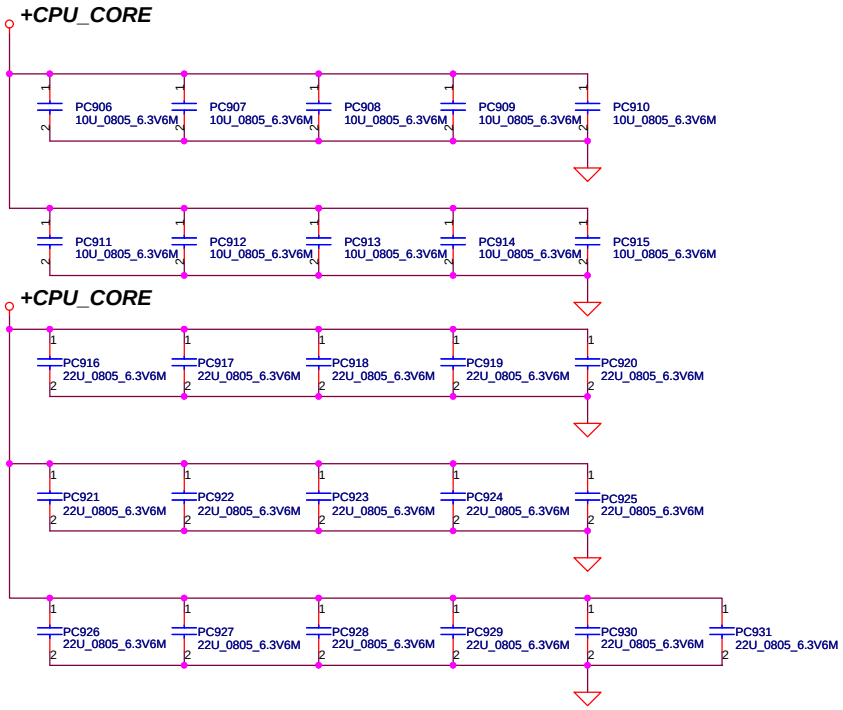
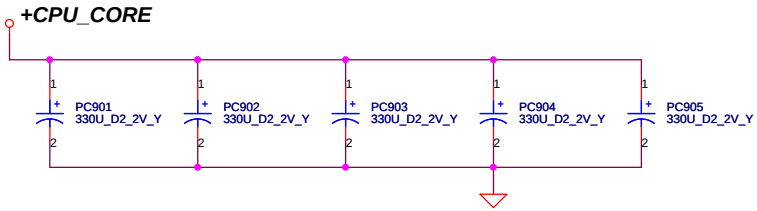
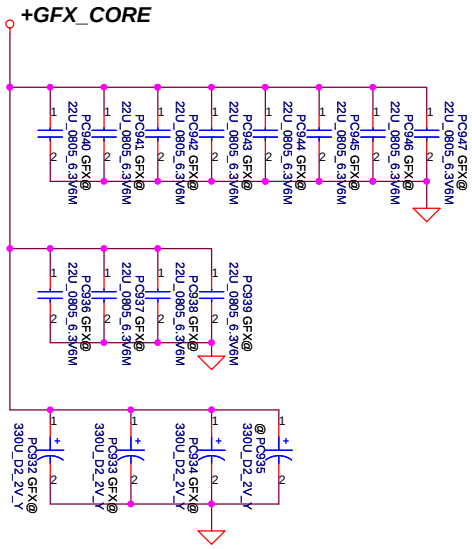
Title: SCHEMATICS, MB A8391

Size	Document Number	Rev
C	4019HG	B

Date: Thursday, February 16, 2012 | Sheet 56 of 61

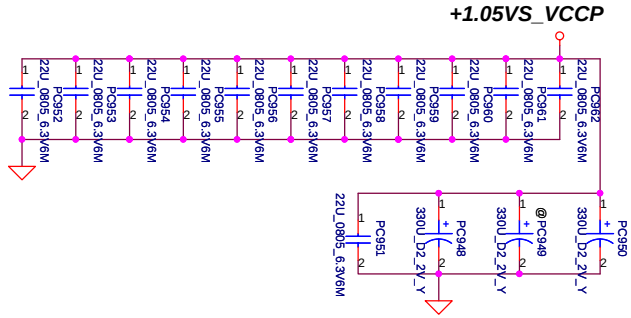






Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

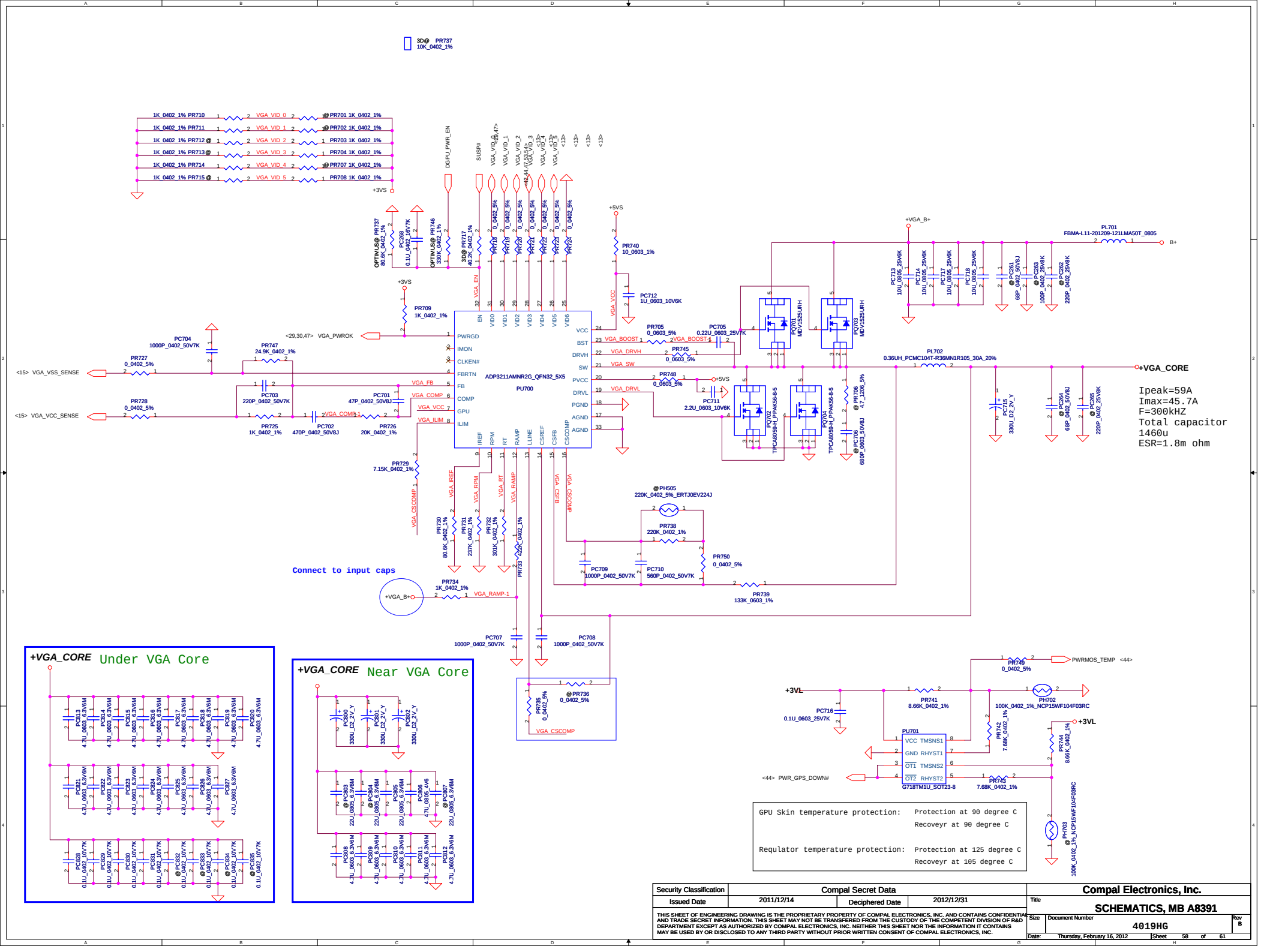
Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATICS, MB A8391

Size | Document Number: 4019HG | Rev: B

Date: Thursday, February 16, 2012 | Sheet 57 of 61



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/12/14	Deciphered Date	2012/12/31

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Title	SCHEMATICS, MB A8391		
Size	Document Number 4019HG		Rev B
Date: Thursday, February 16, 2012	Sheet 58 of 61		

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PU330 to RT8205L	Change source
2.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16VSP	Change PU400 to RT8237C	Change source
3.	2011/09/29	P54-PWR_+VCCSAP/1.8VSP	Change PU450 to SY8037B	Change source
4.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change HMOS to MDV1525	Change source
5.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16VSP	Change HMOS to MDV1525	Change source
6.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Change PD5,PD6 to SCA00001G00	ESD team request
7.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR589 from 348 to 8.06k	FAE suggestion
8.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR590 from 3.65k to 806	FAE suggestion
10.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC574 from 680P to 0.033u	FAE suggestion
11.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC577 from 4700P to 0.033u	FAE suggestion
12.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR548 from 1.21k to 8.06k	FAE suggestion
13.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR550 from 10.7k to 806	FAE suggestion
14.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC547 from 680P to 0.033u	FAE suggestion
15.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC551 from 4700P to 0.033u	FAE suggestion
16.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Add snubber and boost resistor	For 3x3 H-MOS solution
17.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR22 120k,PR27 100k, PR32 0 Ohm	For 120W adapter protect(9012)
18.	2011/09/29	P58-PWR_VGA_CORE	Remove PC803, PC804 add PC806 47u	For Nvidia suggestion
19.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PC360 to SE000006R80	Change source
20.	2011/09/29	P58-PWR_VGA_CORE	Change PC702 to SE00000H180	Change source
21.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR17 14k, PR33 0 Ohm	For CPU temperature protect(9012)
22.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Add PR373 0 Ohm	For 3/5 V always power on(9012)

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Title: ***SCHEMATICS, MB A8391***

Size	Document Number	Rev
Custom	4019HG	B

Date: Thursday, February 16, 2012 | Sheet 59 of 61

HW PIR (Product Improve Record)

QFKAA LA-8391P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2011/11/11

Item	Page	Date	Request	Solution
1)	44	2011/9/27	in order to add one AD channel for PWR VR protect of GPU GPS	change PWR_GPS_DOWN# to EC GPIO43. change HDPACT to EC_GPIO50
2)	44	2011/9/27	in order to reduce BOM	change CB50 to SE000000K80
3)	15	2011/9/27	for N13PGL strap pin by NV review	modify VRAM Table change RV77 to @ due to it is for X76 change RV98 to @ for N13PGL change RV76 to @ for N13PGL change RV73 to 45.3k (SD034453280) for N13PGL change RV89 to 34.8k (SD034348280) for N13PGL
4)	15	2011/9/28	for N13PGL strap pin by NV review	change RV89 to 30k (SD034300280) for N13PGL
5)	15	2011/9/28	for N13PGS strap pin by NV review	change RV73 BOM sstructure to N13PGS@(34.8K) & N13PGL@(45.3K) change RV54 to @ change RV79 BOM sstructure to N13PGS@(20K) & N13PGL@(10K) change RV76 to 10K and N13PGS@ change RV98 to GSDIS@ change RV75 to GSOPT@
6)	22	2011/9/29B	by ESD demand	change D84 to SCA00001L00
7)	35	2011/9/29B	by ESD demand	change D82 to SCA00001L00
8)	37	2011/9/29B	by ESD demand	change D92 to SCA00001L00
9)	05	2011/10/05A	follow HW4 check list	reserve decoupling cap CC66, CC67, CC70 for H_PM_SYNC & H_PECI, BUF_CPU_RST#
11)	28	2011/10/05A	by Customer demand	add LVDS dual channel signal
12)	22	2011/10/05A	by Customer demand	add LVDS dual channel signal and 0ohm: R267 R268 R269 R270 R283 R329 R333 R337 (OPTFHD@) and R500 R501 R502 R503 R504 R505 R507 R508 (3D@)
13)	26	2011/10/05A	by Customer demand	add RH277 BOM structure : OPTFHD@
14)	47	2011/10/05A	follow HW4 check list	add unused Dual MOS: Q7B,Q6B
15)	15	2011/10/18a	by NV demaend	change RV89 to 10k (SD034100280) for N13PGL
16)	10	2011/10/18a	for PEG reversal	change RC79 from @ to always mount
17)	44	2011/10/18a	discuss with EC	change Function_LED from EC_GPIO4D, PIN86 to EC_GPIO11, PIN25 change HDPLOCK from EC_GPIO11, PIN25 to EC_GPIO4D, PIN86 add GPUPWR_SKIN# on EC_GPIO13, pin27 change PWRMOS_TEMP from EC_GPIO50, PIN89 to EC_GPIO43, PIN76 change HDPACT from EC_GPIO43, PIN76 to EC_GPIO50, PIN89 change RB28 pin1 from PWR_GPS_DOWN# to GPUPWR_SKIN# reserve SUSACK# and PCH_SUSPWRDN# by SW demand
18)	27	2011/10/18a	by SW ME demand	change PCH_SUSPWRDN_R to PCH_SUSPWRDN#_R add PCH_SUSPWRDN# to EC and RH132 remove T75 change SUSACK# to SUSACK#_R add RH133 and SUSACK# to EC
19)	46	2011/11/1	new touch pad add new function	add JTP connector Pin 5 (PM_SMBCLK) , Pin6 (PM_SMBDATA)
20)	36	2011/11/1	TV tuner(BCAS) 16V reserve	add RM15 and RM16 reserve for TV tuner (BCAS)
21)	42	2011/11/1	avoid SM_EN floating	reserve RA43 for SM_EN 100K pull down reserve
22)	42	2011/11/1	for vendor request	exchange location of RA28 and CA42
23)	42	2011/11/1	for vendor request	RA26 pin2 change name from OSC_IN to OSC_OUT
24)	42	2011/11/1	for vendor request, S&M HP need shut down	delete DA1. add RA19 ,QA5 ,RA42 ,
25)	32	2011/11/2	for lot6 0.5W power consumption	delete CH57 ,PJ3 then add PJ5, QH6, CH59, RH228
26)	47	2011/11/2	for lot6 0.5W power consumption	add R5545, Q5527, R5529, R5534
27)	47	2011/11/3	for NV power sequence	R434 change from 220K to 330K
28)	47	2011/11/3	for NV power sequence	change net name from DGPU_PWR_EN# to VGA_PWROK#
29)	32	2011/11/3	for lot6 0.5W power consumption	reserve RH228
30)	46	2011/11/3	for lot6 0.5W power consumption	change D21 power from +5VL to +5VALW
31)	44	2011/11/7	for lot6 0.5W power consumption	add EC pin 70 for PCH_PWR_EN
32)	29	2011/11/7	for NV sequence	delete RH287 for NV sequence
33)	29	2011/11/7	for NV sequence	RH175 change to always mount
34)	29	2011/11/7	for TV tuner 16VS over current Pin	delete RH174 and RH1
35)	29	2011/11/7	for TV tuner 16VS over current Pin	change PCH D44 ball trace name to LNB_OC#
36)	29	2011/11/7	for TV tuner 16VS over current Pin	add RH326 for LNB_OC# pull high
37)	42	2011/11/9	for vendor request	exchange CA42 and RA28 location
38)	40	2011/11/9	for vendor request	add RT67 RT68 RT69 RT70 RT72 RT73
39)	36	2011/11/9	for EMI request	reserve CCL10 for EMI request
40)	37	2011/11/9	for EMI request	reserver RL29 CL43 for EMI request
41)	29	2011/11/9	EC common core for WL_OFF#	PCH pin F46 and RH299 chagne net name from WL_OFF# to PCH_GPIO55
42)	44	2011/11/9	EC common core for WL_OFF#	change EC pin 29 net name from CPSETIN to WL_OFF#
43)	36	2011/11/9	EC common core for WL_OFF#	add R5546 for WL_OFF# pull high to +3V_WLAN
44)	44	2011/11/9	EC common core for WL_OFF#	CPSETIN signal change from EC pin 29 to EC pin 74
45)	44	2011/11/9	LNB_OC# change from PCH pin D44 to EC pin 119	add RH327 pull high to +3VS for LNB_OC#
46)	36	2011/11/15	for vendor demand	change YCL1 from SJ10000CU00 to SJ10000EF00, CCL4 and CCL5 from 30pF to 15pF
47)	15	2011/11/15	for NV recommend	change BOM structure of RV54 from @ to N13PGS@
48)	47	2011/11/15c	for NV DG demand	change R460 from 470ohm to 22ohm
49)	36	2011/11/15d	by EMI demand	change BOM structure of CCL10 from @ to GCLK@
50)	37	2011/11/15d	by EMI demand	change BOM structure of RL29, CL43 from @ to GCLK@

Compal Electronics, Inc.			
Title	SCHEMATICS, MB A8391		
Size: Custom	Document Number: 4019HG		Rev: B
Date: Thursday, February 16, 2012	Sheet 60 of 61		

HW PIR (Product Improve Record)

QFKAA LA-8391P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3
GERBER-OUT DATE: 2011/12/22

Item	Page	Date	Request	Solution
1)	27	2011/11/29a	For DVT hang	Add CH23 CH24 CH25 for SW-node noise.
2)	13	2011/11/29a	For ME request	Change location from JLVDS to JLVDS4
3)	47	2011/12/05a	For reduce Rds-on of +VRAM_1.5VS	Add Q44
4)	05	2011/12/07a	For leakage	Change from +3VALW to +3VALW_PCH of UC1
5)	44	2011/12/13a	For design change	Change LNB_EN from PCH to EC and delte RH315, add RB11
6)	24	2011/12/13a	For HDMI leakage	Change Pin 5 of U9 from +5VL to +HDMI_5V_OUT
7)	44	2011/12/13a	For design change RF LED control pin	Change RF LED control pin from PCH to EC.
8)	35	2011/12/15a	For ME request	Change JFP/JPOWER/JFUN from zif to non-zif
9)	40	2011/12/15a	For adjust EXT USB3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
10)	41	2011/12/15a	For adjust EXT USB3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
11)	22	2011/12/17a	For prevent LVDS burn issue	Add F3 (Poly fuse to prevent burn)
12)	46	2011/12/19a	For ME delete stand-off	Delete H25,H26,H27
13)	46	2011/12/19a	For Wimax flash issue	Change +5VS to +3VS of Wimax LED
14)	46	2011/12/19a	For layout request	Add net name +5VS_FUNC with Function conn power pin
15)	15	2011/12/20a	For NV request	Change RV76 from 10K to 20K
16)	46	2011/12/21a	For power rail change	Change WiMAX LED power rail from +5VS to +5VALW
17)	16	2011/12/22a	For NV request	Change LV6 from bead to 4.3ohm resistor
18)	29	2011/12/22a	For EMI request	Add CH29 for EMI request

QFKAA LA-8391P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0
GERBER-OUT DATE: 2012/02/02

Item	Page	Date	Request	Solution
1)	36	2012/01/12a	For GCLK	Add CCL13(0.1u) for +3VALW
2)	15	2012/01/12a	For NV suggestion	Change RV 76 from 20K to 45K(Support GEN3)
3)	36	2012/01/12a	For MSATA pin define.	Add RM30 (MSATA define that Pin22 is reserve, so other function need to add PLT_RST#).
4)	36	2012/01/18a	For GLCK	Change CCL13 from +3VLAW to +3VALW_GCLK
5)	41	2012/01/30a	For TV tuner use PCIE interface	Add RM31~RM35 and QM2
6)	26	2012/01/30a	For TV tuner use PCIE interface	Change PCIE 6 from USB to TV tuner
7)	26	2012/01/30a	For TV tuner use PCIE interface	Change CLK_USB30 to CLK_TV and CLKREQ_USB30# to CLKREQ_TV#
8)	11	2012/01/30a	For M1 only	Unmount RC117/RC118/QC7/QC8
9)	46	2012/01/30a	For MP	Unmount SW3
10)	15	2012/01/30a	For NV suggestion	Change RV 73 to 5K
11)	43	2012/01/30a	For EMI request	Add CA51
12)	41	2012/01/30a	For Internal USB30 only	Delete Page 41

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Title	*SCHEMATICS, MB A8391*		
Size: Custom	Document Number: 4019HG		Rev: B
Date: Thursday, February 16, 2012	Sheet 61 of 61		