Model Name : Q3ZMC
File Name : LA-8481P

Compal Confidential

Q3ZMC UMA M/B Schematics Document

Intel Ivy/Sandy Bridge SFF BGA 1023p Processor
/Panther Point 989p PCH
/ DDR3L Memory Down *8

2012-04-11

REV:1.0(MP SMT)

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

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Title: Cover Page

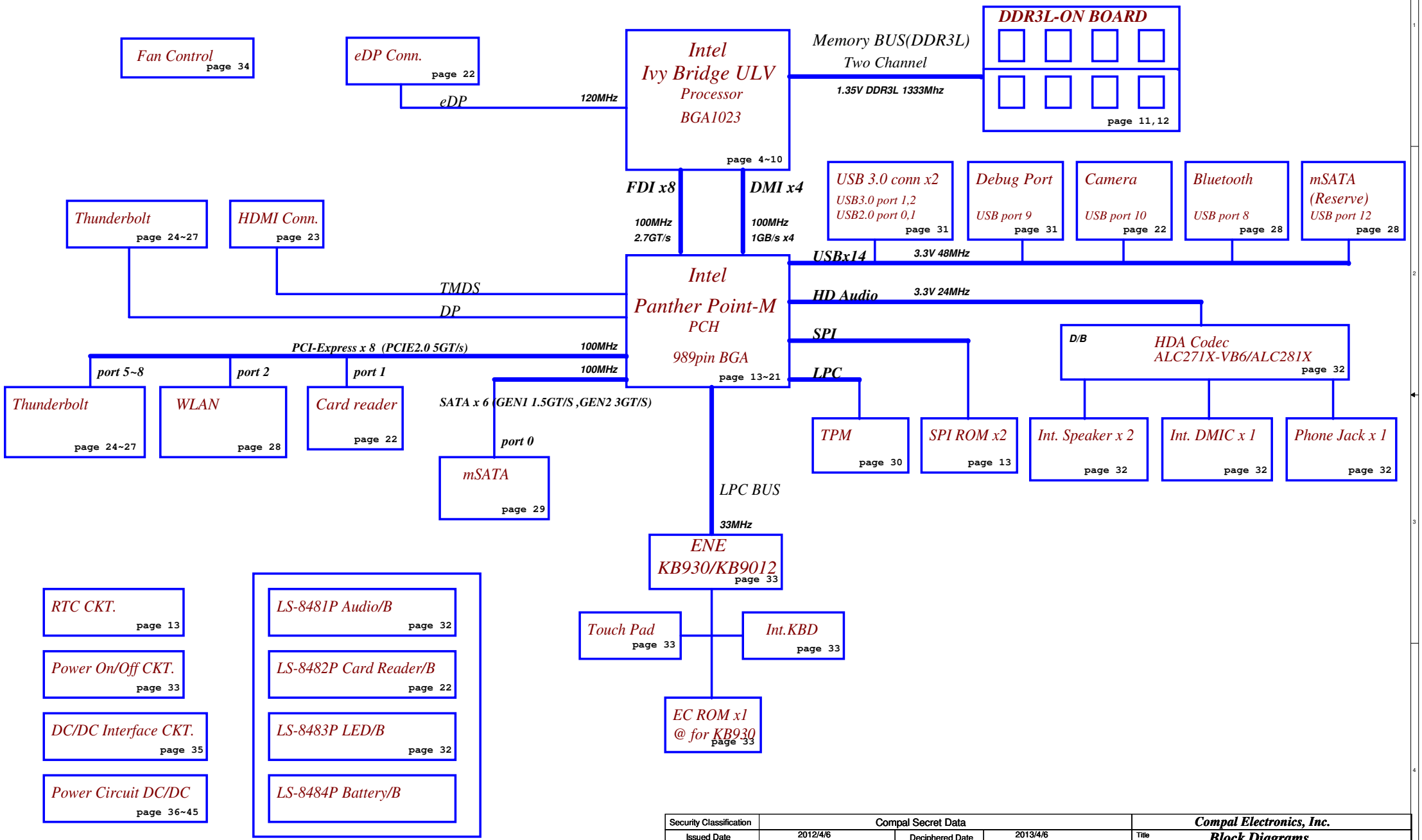
Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 1 of 51

PCB

ZZZ1

LA-8481P
DAZ0NS00100



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

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Title: Block Diagrams

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.35VS	+1.35V to +1.35VS switched power rail	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.5VS	+1.5VSP to +1.5VS power rail for PCH	ON	OFF	OFF
+1.8VS	+3VALW to 1.8VS switched power rail for PCH	ON	OFF	OFF
+3VALW	+3VALWP to +3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Resistor)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW always on power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device		Address
ChannelA	A0	1010 000X
ChannelB	A4	1010 010X

BOM Config
4319HNBOL01:UMA@/DDR3L@/eDP@/USB3.0@/9012@/TB@/IVB@/HM77@/DS3@/TXM@/TPM@/128@/
4319HNBOL02:UMA@/DDR3L@/eDP@/USB3.0@/9012@/TB@/IVB@/HM77@/DS3@/TXM@/TPM@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1,0.2
1	0.3 DVT:unknown MCU+MKS Motor,With TB IC
2	0.4 PVT1:PADAUK MCU+MKS Motor,Without TB IC
3	0.4 PVT2:PADAUK MCU+MKS Motor,With TB IC
4	1.0
5	
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	USB port (Rear side 3.0)
		1	USB port (Rear side 3.0)
	UHCI1	2	
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	Debug Port
	UHCI5	10	Camera
		11	
	UHCI6	12	mSATA(Reserve)
		13	BlueTooth

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA	UMA@
CPU	IVB@
PCH	HM77@
DDR3	DDR3@
DDR3L	DDR3L@
On Board DRAM	X76@
128bit RAM	128@
eDP	eDP@
LVDS	LVDS@
USB2.0 Conn	USB2.0@
USB3.0 Conn	USB3.0@
Thunderbolt	TB@
KB930	930@
KB9012	9012@
Normal S3	S3@
Deep S3	DS3@
TPM+TCM	TXM@
TPM	TPM@
TCM	TCM@

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Title: Notes List

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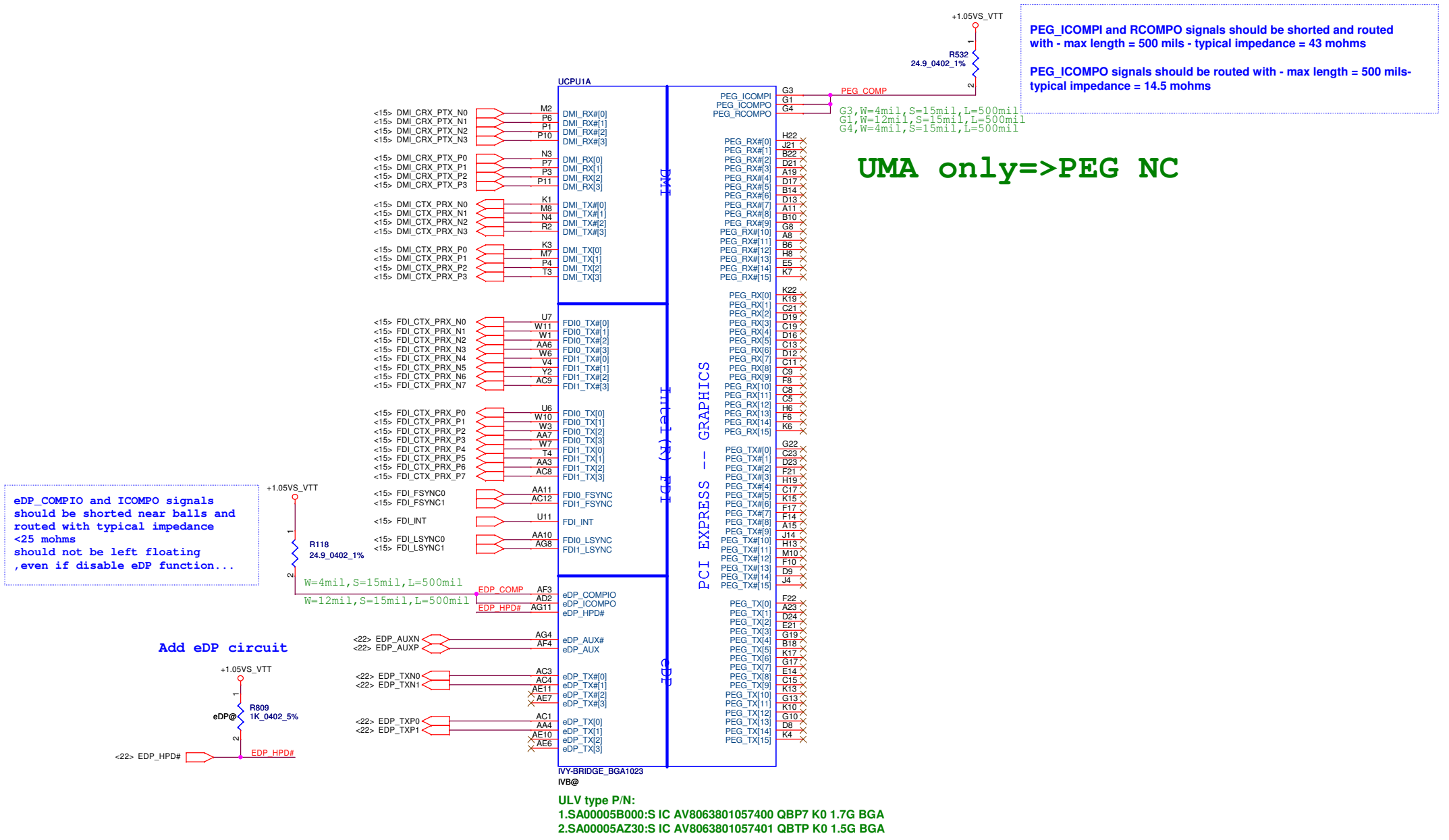

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.			
Title	PROCESSOR(1/7) DMI,FDI,PEG		
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PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.2 & CRB1.0

C784 2 1 0.1U_0402_10V7K H_CPUPWRGD
@
R223 2 1 10K_0402_5% H_CPUPWRGD

PROC_SELECT#
Future platforms,PH VCPLL and connect to PCH DF_TVS

偵測CPU有無安裝

XBOX 三紅功能

Processor Pullups follow CRB1.0

+1.05VS_VTT R220 2 1 62_0402_5%
<32> H_PROCHOT# H_PROCHOT# R216 56_0402_5% H_PROCHOT#_R

<18,32> H_PECI H_PECI

<18> H_THRMTRIP#

UCPU1B

<17> H_SNB_IVB# F49 PROC_SELECT#
C57 PROC_DETECT#
T1 PAD @ H_CATERR# C49 CATERR#
H_PECI A48 PECI
H_PROCHOT# C45 PROCHOT#
D45 THERMTRIP#

MISC
THERMAL
PWR MANAGEMENT

CLOCKS
BCLK J3 BCLK H2 CLK_CPU_DMI <14> CLK_CPU_DMI# <14>
DPLL_REF_CLK AG3 CLK_CPU_DPLL DPLL_REF_CLK# AG1 CLK_CPU_DPLL# CLK_CPU_DPLL <14> CLK_CPU_DPLL# <14>

DDR3 MISC
SM_DRAMRST# AT30 SM_DRAMRST# SM_DRAMRST# <6>
SM_RCOMP[0] BF44 SM_RCOMP0 R149 2 1 140_0402_1%
SM_RCOMP[1] BE43 SM_RCOMP1 R486 2 1 25.5_0402_1%
SM_RCOMP[2] BG43 SM_RCOMP2 R484 2 1 200_0402_1%

DDR3 Compensation Signals
Trace:10mil ,Spacing:13mil, Max.Length:500mil

JTAG & BPM
PRDY# N53
PREQ# N55
TCK L56 XDP_TCK @PAD T2
TMS L55 XDP_TMS @PAD T3
TRST# J58 XDP_TRST# @PAD T4
TDI M60 XDP_TDI @PAD T5
TDO L59 XDP_TDO @PAD T6
DBR# K58 XDP_DBRESET#
BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61

XDP_DBRESET# <15>
C102 100P_0201_25V8J
For EMI

<15> H_PM_SYNC C48 PM_SYNC
@R80 0_0402_5%
<18> H_CPUPWRGD H_CPUPWRGD_R B46 UNCOREPWRGOOD
UNCOREPWRGOOD:除了CPU_CORE以外的電OK
PM_DRAM_PWRGD_R BE45 SM_DRAMPWROK
SM_DRAMPWROK:DRAM power ok
BUF_CPU_RST# D44 RESET#

IVY-BRIDGE_BGA1023
IVB@

Checklist1.0 P.64 Processor Graphis Disable Guide
DIS only SKU or UMA eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

+1.05VS_VTT
CLK_CPU_DPLL# R116 2 @ 1 1K_0402_5%
CLK_CPU_DPLL R117 2 @ 1 1K_0402_5%

+3VS
XDP_DBRESET# R569 2 1 1K_0402_5%

CRB1.0 PH 1K +3VS
Check list 1.0 PH 5K +3VS
Check list 1.2 PH 10K +3VS
Debug port DG1.1-1.2 50~5K ohm

Follow DG 1.2 & CRB1.0
Buffered reset to CPU

Use open drain MOS:
+1.05VS_VTT PH pop 75ohm
series resister pop 43ohm

+3VS
C396 0.1U_0201_10V6K
U15
SN74LVC1G07DCKR_SC70-5
+1.05VS_VTT
R226 75_0402_5%
R227 43_0402_1%
<17,22,24,30,32> PLT_RST#
BUFO_CPU_RST#
BUF_CPU_RST#
@ R225 0_0402_5%

RESET#:都ok後請CPU做reset

Follow DG 1.2 & CRB1.0

Use open drain MOS:
+1.35VS PH pop 200ohm
series resister pop 130ohm

+3VALW
C101 0.1U_0402_16V4Z
U5
MC74VHC1G09DFT2G_SC70-5
<15> SYS_PWROK
<15> PM_DRAM_PWRGD
PM_SYS_PWRGD_BUF
+1.35VS
R88 200_0402_5%
R97 130_0402_5%
PM_DRAM_PWRGD_R
R829 39_0402_5% @
Q74 SSM3K7002FU_SC70-3 @
<35,40> SUSP

PM_DRAM_PWRGD
C787 100P_0201_25V8J

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.
Title: PROCESSOR(2/7) PM,XDP,CLK
Size: Custom
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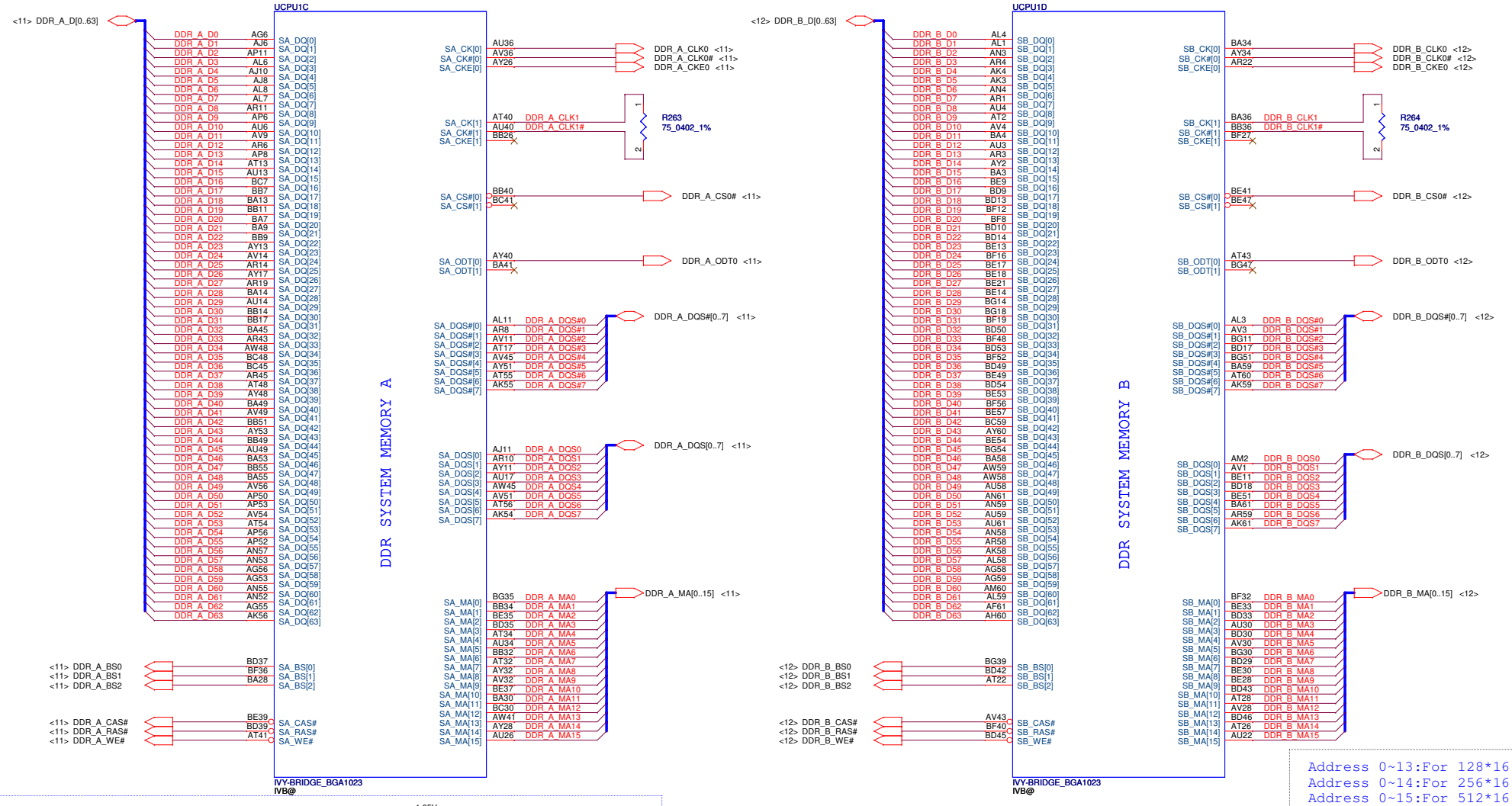
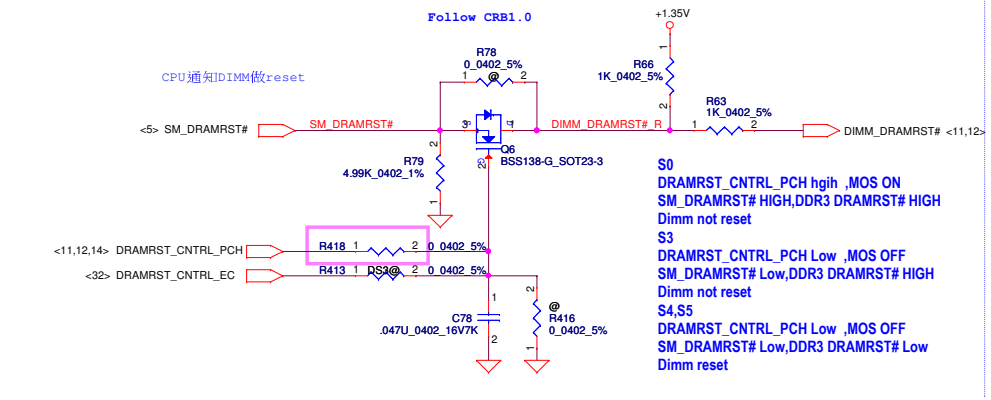
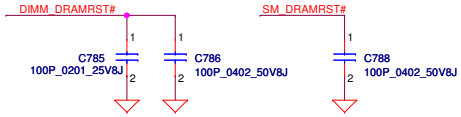


Address 0~13:For 128*16
Address 0~14:For 256*16
Address 0~15:For 512*16





Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

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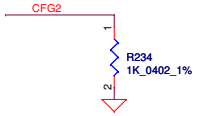
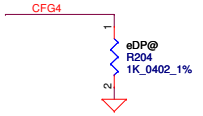
Default "1",EDS R1.0 P.88

CFG Straps for Processor

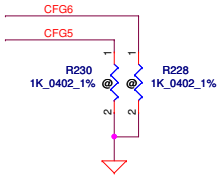
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



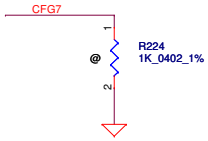
eDP enable	
CFG4	* 1:Disable 0:Enable

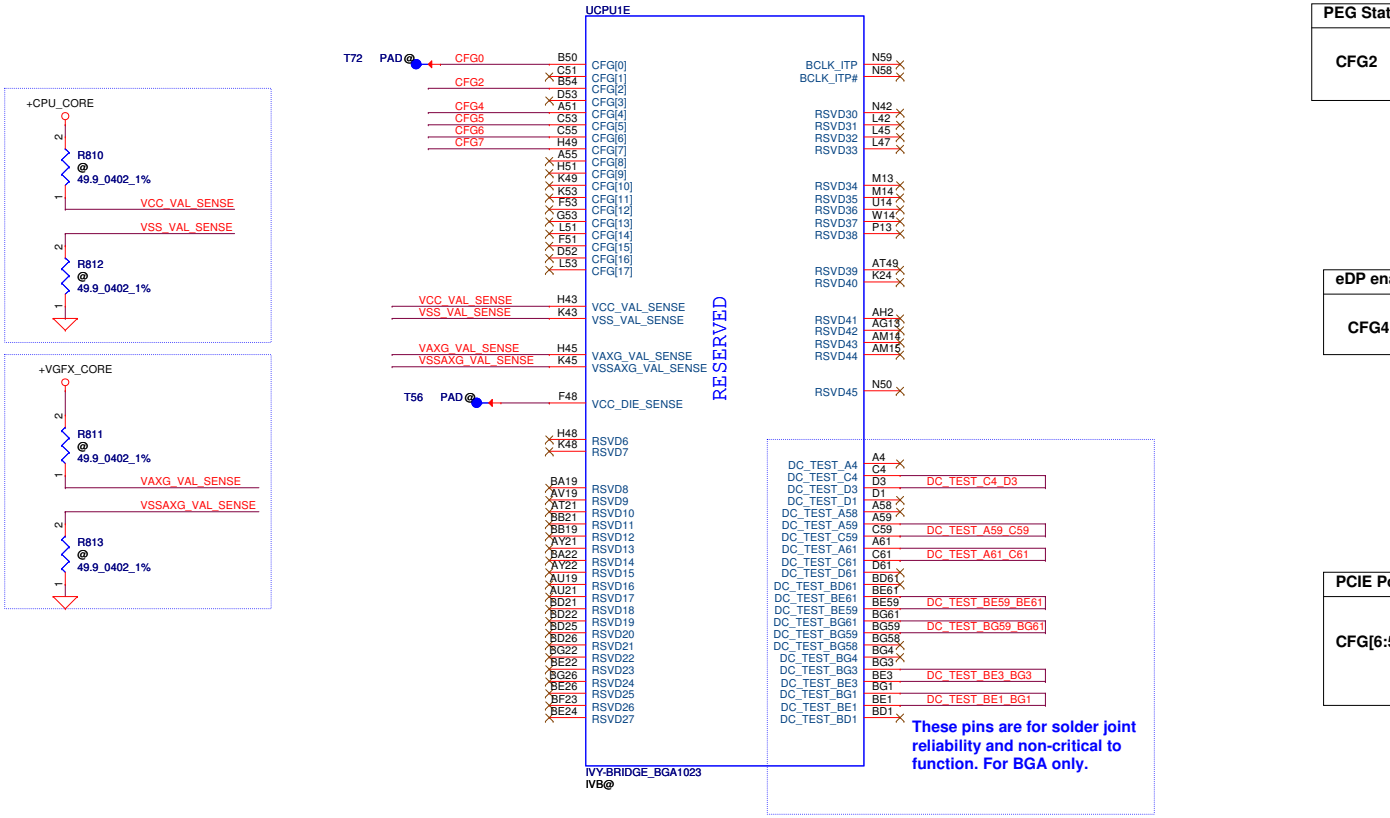


PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	CRB1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

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POWER

INTEL Recommend VCC
3*330uF,12*22uF(0805),16*2.2uF(0402)
PD0.9

ULV SC/DC 33A

8.5A

UCPU1F

+CPU_CORE

CORE SUPPLY

VCC[1] A26
VCC[2] A29
VCC[3] A31
VCC[4] A34
VCC[5] A35
VCC[6] A38
VCC[7] A39
VCC[8] A42
VCC[9] C26
VCC[10] C27
VCC[11] C32
VCC[12] C34
VCC[13] C37
VCC[14] C39
VCC[15] C42
VCC[16] D27
VCC[17] D32
VCC[18] D34
VCC[19] D37
VCC[20] D39
VCC[21] D42
VCC[22] E26
VCC[23] E28
VCC[24] E32
VCC[25] E34
VCC[26] E37
VCC[27] E38
VCC[28] F25
VCC[29] F26
VCC[30] F28
VCC[31] F32
VCC[32] F34
VCC[33] F37
VCC[34] F38
VCC[35] F42
VCC[36] G42
VCC[37] H25
VCC[38] H26
VCC[39] H28
VCC[40] H29
VCC[41] H32
VCC[42] H34
VCC[43] H35
VCC[44] H37
VCC[45] H38
VCC[46] H40
VCC[47] J25
VCC[48] J26
VCC[49] J28
VCC[50] J29
VCC[51] J32
VCC[52] J34
VCC[53] J35
VCC[54] J37
VCC[55] J38
VCC[56] J40
VCC[57] J42
VCC[58] K26
VCC[59] K27
VCC[60] K29
VCC[61] K32
VCC[62] K34
VCC[63] K35
VCC[64] K37
VCC[66] K39
VCC[67] K42
VCC[68] L25
VCC[69] L28
VCC[70] L33
VCC[71] L36
VCC[72] L40
VCC[73] N26
VCC[74] N30
VCC[75] N34
VCC[76] N38

PEG IO AND DDR IO

+1.05VS_VTT

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] AJ17
VCCIO[7] AJ21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

INTEL Recommend VCCIO
PD 0.9

330uF 1+1
10uF (0603) *5
1uF (0201) *16

+1.05VS_VTT

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AF16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

330uF 1
10uF (0603) *5
1uF (0201) *10

+1.05VS_VTT

VCCIO50 W16
VCCIO51 W17

+3VALW

R521 10K_0402_5%

VCCIO_SEL

R520 10K_0402_5% @

VCCIO_SEL For 2012 CPU support		
A19	*	1 : +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL

BC22 VCCIO_SEL_R R582 1 @ 2 0_0402_5%

QUIET RAILS

+1.05VS_VTT

VCCPQE[1] AM25
VCCPQE[2] AN22

C951 1U_0201_4V6M

+1.05VS_VTT

R574 130_0402_5%

Check List R1.5
VIDALERT#:75ohm ±5% pull-up to VCCIO close to IMVP7
VIDSCLK: 55ohm ±5% pull-up to VCCIO close to IMVP7
VIDSOUT: 130ohm ±5% pull-up to VCCIO close to CPU
130ohm ±5% pull-up to VCCIO close to IMVP7

SVID

VIDALERT# A44 H_CPU_SVIDALRT# R576 1 2 43_0402_1% VR_SVID_ALRT# <43>
VIDSCLK B43 H_CPU_SVIDCLK R577 1 @ 2 0_0402_5% VR_SVID_CLK <43>
VIDSOUT C44 H_CPU_SVIDDAT R578 1 @ 2 0_0402_5% VR_SVID_DAT <43>

+CPU_CORE

Place the PU,PD
resistors close to CPU

R588 100_0402_1%

SENSE LINES

VCC_SENSE F43 VCCSENSE_R R579 1 @ 2 0_0402_5%
VSS_SENSE G43 VSSSENSE_R R581 1 @ 2 0_0402_5%

VCCSENSE <43>
VSSSENSE <43>

+1.05VS_VTT

R107 1 2 10_0402_5%

VCCIO_SENSE AN16 VCCIO_SENSE
VSS_SENSE_VCCIO AN17 VSSIO_SENSE

VCCIO_SENSE <41>

R589 100_0402_1%

Check List R1.5
VCCSENSE:100ohm ±1% pull-up to VCC near processor.
VSSSENSE:100ohm ±1% pull-down to GND near processor.

R105 10_0402_5%

Should change to connect from
power cirucit & layout differential
with VCCIO_SENSE.

IVY-BRIDGE_BGA1023
IVB@

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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POWER

ULV SC/DC GT1: 18A
GT2: 33A

INTEL Recommend VAXG
2*330uF,5*22uF(0805),6*10uF(0603),6*1uF(0402)
PD 0.9

+VGFX_CORE

UCPU1G

VAXG[1] AA46
VAXG[2] AB47
VAXG[3] AB50
VAXG[4] AB51
VAXG[5] AB52
VAXG[6] AB53
VAXG[7] AB55
VAXG[8] AB56
VAXG[9] AB58
VAXG[10] AB59
VAXG[11] AC61
VAXG[12] AD47
VAXG[13] AD48
VAXG[14] AD50
VAXG[15] AD51
VAXG[16] AD52
VAXG[17] AD53
VAXG[18] AD55
VAXG[19] AD56
VAXG[20] AD58
VAXG[21] AD59
VAXG[22] AE46
VAXG[23] N45
VAXG[24] P47
VAXG[25] P48
VAXG[26] P50
VAXG[27] P51
VAXG[28] P52
VAXG[29] P53
VAXG[30] P55
VAXG[31] P56
VAXG[32] P61
VAXG[33] T48
VAXG[34] T58
VAXG[35] T59
VAXG[36] T61
VAXG[37] U46
VAXG[38] V47
VAXG[39] V48
VAXG[40] V50
VAXG[41] V51
VAXG[42] V52
VAXG[43] V53
VAXG[44] V55
VAXG[45] V56
VAXG[46] V58
VAXG[47] V59
VAXG[48] W50
VAXG[49] W51
VAXG[50] W52
VAXG[51] W53
VAXG[52] W55
VAXG[53] W56
VAXG[54] W61
VAXG[55] Y48
VAXG[56] Y61

GRAPHICS

Check List R1.5
VCCAXG_SENSE:100ohm ±5% pull-up to VCC near processor.
VSSAXG_SENSE:100ohm ±5% pull-down to GND near processor.

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD 0.9

+VGFX_CORE
R381 100_0402_5%
<43> VCC_AXG_SENSE
<43> VSS_AXG_SENSE
F45 VAXG_SENSE
G45 VSSAXG_SENSE
R396 100_0402_5%

SENSE LINES

+1.8VS
R477 0_0805_5%
+1.8VS_VCCPLL
1.2A
C606 220U_B2_2.5VM_R15M SGA00004I00
C583 1U_0201_4V6M
C584 1U_0201_4V6M
BB3 VCCPLL[1]
BC1 VCCPLL[2]
BC4 VCCPLL[3]

1.8V RAIL

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.9

+VCCSA
6A
C607 330U_B2_2VM_R15M SGA00004400
C998 1U_0201_4V6M
C999 1U_0201_4V6M
C1181 1U_0201_4V6M
C1180 1U_0201_4V6M
C1179 1U_0201_4V6M
L17 VCCSA[1]
L21 VCCSA[2]
N16 VCCSA[3]
N20 VCCSA[4]
N22 VCCSA[5]
P17 VCCSA[6]
P20 VCCSA[7]
R16 VCCSA[8]
R18 VCCSA[9]
R21 VCCSA[10]
U15 VCCSA[11]
V16 VCCSA[12]
V17 VCCSA[13]
V18 VCCSA[14]
V21 VCCSA[15]
W20 VCCSA[16]

SA RAIL

C995 10U_0603_6.3Y6M
C996 10U_0603_6.3Y6M
C997 10U_0603_6.3Y6M

IVY-BRIDGE_BGA1023
IVB@

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandey bridge not support M3,
Check list1.0 & CRB say can NC

VREF

SM_VREF AY43
+V_SM_VREF
BE7 SA_DIMM_VREFDQ
BG7 SB_DIMM_VREFDQ
SA_DIMM_VREFDQ <11>
SB_DIMM_VREFDQ <12>
C647 0.1U_0201_10V6K
@ R69 1K_0402_1%
@ R68 1K_0402_1%

+V_SM_VREF should have 20 mil trace width

+1.35VS
R534 1K_0402_5%
R540 1K_0402_5%

DDR3 - 1.5V RAILS

5A
VDDQ[1] AJ28
VDDQ[2] AJ33
VDDQ[3] AJ36
VDDQ[4] AJ40
VDDQ[5] AL30
VDDQ[6] AL34
VDDQ[7] AL38
VDDQ[8] AL42
VDDQ[9] AM33
VDDQ[10] AM36
VDDQ[11] AM40
VDDQ[12] AN30
VDDQ[13] AN34
VDDQ[14] AN38
VDDQ[15] AR26
VDDQ[16] AR28
VDDQ[17] AR30
VDDQ[18] AR32
VDDQ[19] AR34
VDDQ[20] AR36
VDDQ[21] AR40
VDDQ[22] AV41
VDDQ[23] AW26
VDDQ[24] BA40
VDDQ[25] BB28
VDDQ[26] BG33

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.9

Short for +1.35VS to +1.35V_CPU_VDDQ

+1.35VS
C977 1U_0201_4V6M
C978 1U_0201_4V6M
C979 1U_0201_4V6M
C980 1U_0201_4V6M
C981 1U_0201_4V6M
C982 1U_0201_4V6M
C983 1U_0201_4V6M
C984 1U_0201_4V6M
C988 1U_0201_4V6M
C991 1U_0201_4V6M
C599 330U_B2_2VM_R15M SGA00004400

Place BOT OUT Conn

C990 10U_0603_6.3V6M
C989 10U_0603_6.3V6M
C987 10U_0603_6.3V6M
C970 10U_0603_6.3V6M

C1002 0.1U_0201_10V6K
C986 0.1U_0201_10V6K
C1010 0.1U_0201_10V6K
C1007 0.1U_0201_10V6K
C1008 0.1U_0201_10V6K
C1006 0.1U_0201_10V6K
C994 0.1U_0201_10V6K
C1009 0.1U_0201_10V6K
C992 0.1U_0201_10V6K
C993 0.1U_0201_10V6K

QUIET RAILS

VCCDQ[1] AM28
VCCDQ[2] AN26
+1.35VS
C985 1U_0201_4V6M

SENSE LINES

VDDQ_SENSE BC43
VSS_SENSE_VDDQ BA43

SENSE LINES

VCCSA_SENSE U10
CPU EDS1.3 P.93
VCCSA_VID0 Must PD
VCCSA_SENSE <42>

VCCSA VID lines

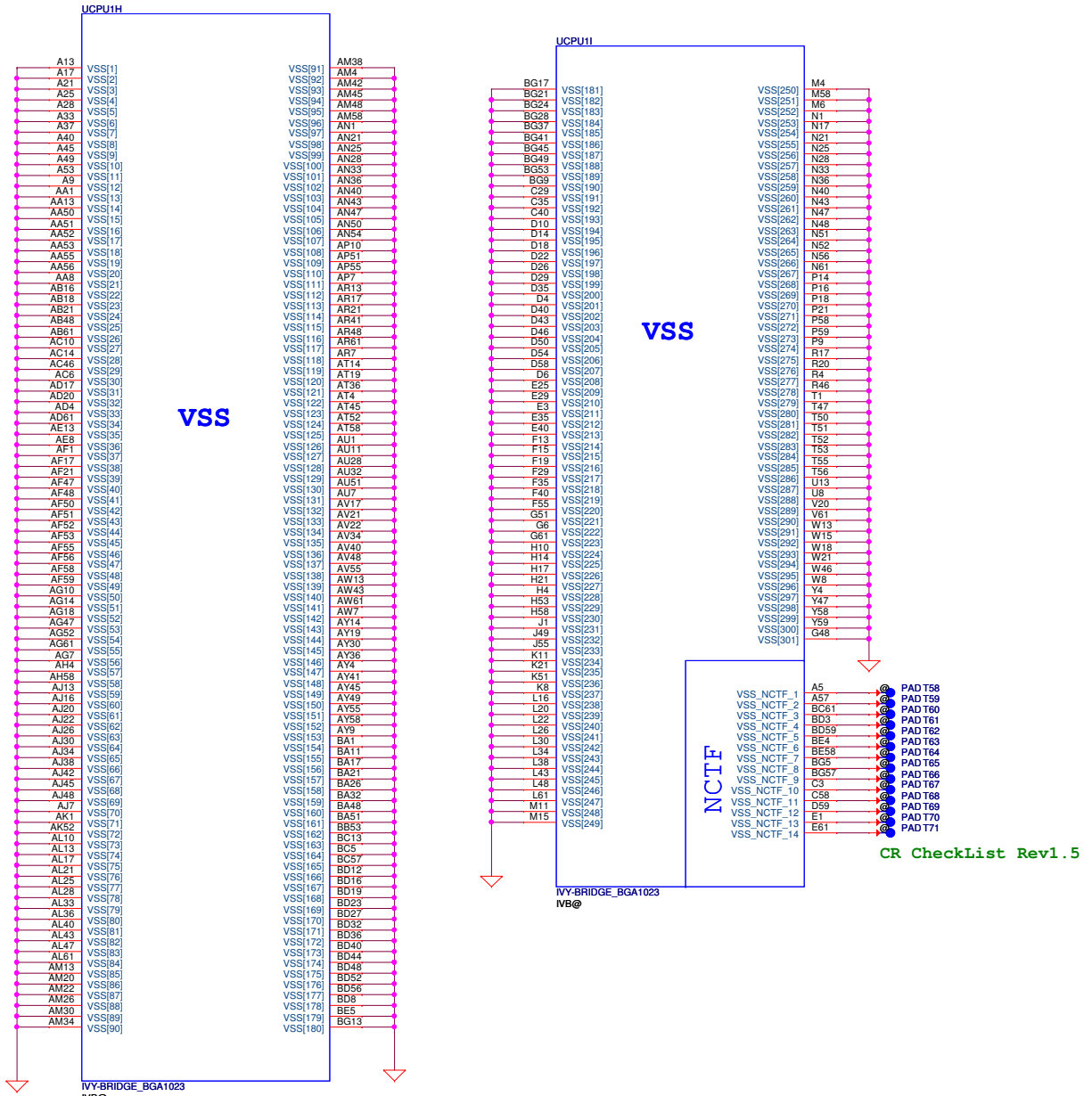
VCCSA_VID[0] D48
VCCSA_VID[1] D49
H_VCCSA_VID0 <42>
H_VCCSA_VID1 <42>
R129 0_0402_5% @

VCCSA_VID
For 2012 future CPU
VCCSA voltage select

VCCSA					
VID0	VID1	Vout	SNB	IVB	ULV
0	0	0.9V	V	V	V
0	1	0.8V	V	V	
		0.85V			V
1	0	0.725V	X	V	V
1	1	0.675V	X	V	V

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.
Title: PROCESSOR(6/7) PWR
Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0
Date: Thursday, April 12, 2012 | Sheet 9 of 51



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

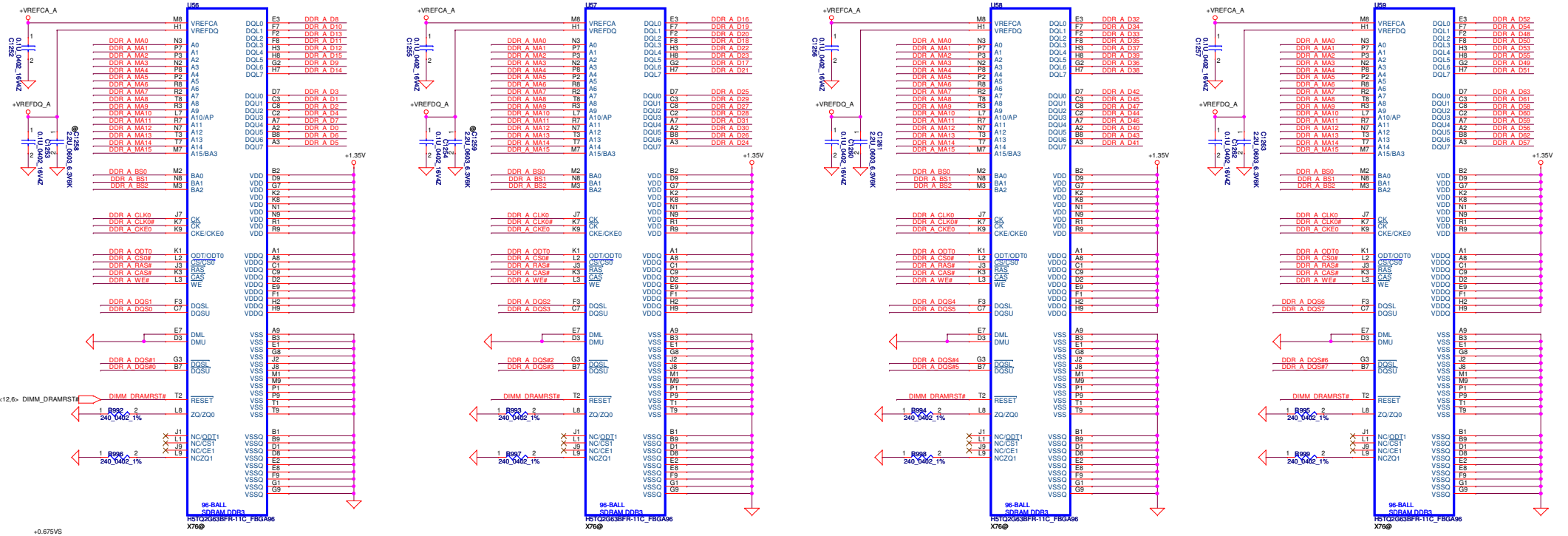
Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 10 of 51

Channel A

<6> DDR_A_MA[0..15] — DDR_A_MA[0..15]
<6> DDR_A_DQS#[0..7] — DDR_A_DQS#[0..7]
<6> DDR_A_DQS[0..7] — DDR_A_DQS[0..7]
<6> DDR_A_D[0..63] — DDR_A_D[0..63]



+0.675VS

C1519 10U_0603_6.3V6M

+0.675VS

C1482 0.1U_0201_10V6K
C1481 0.1U_0201_10V6K
C1480 1U_0201_4V6M
C1479 1U_0201_4V6M
C1513 0.1U_0201_10V6K
C1512 0.1U_0201_10V6K
C1511 1U_0201_4V6M

Layout Note:
Place near each memory part

+1.35V

C1466 0.1U_0201_10V6K
C1476 1U_0402_6.3V6K
C1477 1U_0402_6.3V6K
C1467 0.1U_0201_10V6K
C1470 0.1U_0201_10V6K
C1471 1U_0402_6.3V6K
C1478 1U_0402_6.3V6K
C1468 1U_0402_6.3V6K

+1.35V

C1469 10U_0603_6.3V6M
C1479 10U_0603_6.3V6M
C1463 10U_0603_6.3V6M
C1475 10U_0603_6.3V6M
C1465 10U_0603_6.3V6M
C1472 10U_0603_6.3V6M
C1471 10U_0603_6.3V6M
C1474 10U_0603_6.3V6M
@C1464 330U_D2_2V_Y

near U56 near U57 near U58 near U59

M3 support

<9> SA_DIMM_VREFDQ — @R1105 0_0402_5%
BSS138_NL_SOT23-3 — Q78
<12,14,6> DRAMRST_CNTRL_PCH
R1106 1K_0402_1%
R1104 1K_0402_1%
+VREFDQ_A
C1481 2.2U_0603_6.3V6K
C1161 0.1U_0402_16V4Z

+1.35V

R1108 1K_0402_1%
R1107 1K_0402_1%
+VREFCA_A
C1483 0.1U_0402_16V4Z
C1482 2.2U_0603_6.3V6K

DDR3 CTL/ADD Termination

+0.675VS

R284 36_0201_1% — DDR_A_RAS# <6>
R290 36_0201_1% — DDR_A_CAS# <6>
R291 36_0201_1% — DDR_A_ODT0 <6>
R294 36_0201_1% — DDR_A_CKE0 <6>
R295 36_0201_1% — DDR_A_WE# <6>
R296 36_0201_1% — DDR_A_CS0# <6>
R297 36_0201_1% — DDR_A_BS2 <6>
R298 36_0201_1% — DDR_A_BS0 <6>
R301 36_0201_1% — DDR_A_MA12
R303 36_0201_1% — DDR_A_MA0
R304 36_0201_1% — DDR_A_BS1 <6>
R306 36_0201_1% — DDR_A_MA3
R309 36_0201_1% — DDR_A_MA1
R311 36_0201_1% — DDR_A_MA2
R312 36_0201_1% — DDR_A_MA4
R313 36_0201_1% — DDR_A_MA5
R315 36_0201_1% — DDR_A_MA11
R317 36_0201_1% — DDR_A_MA9
R318 36_0201_1% — DDR_A_MA14
R319 36_0201_1% — DDR_A_MA13
R323 36_0201_1% — DDR_A_MA6
R325 36_0201_1% — DDR_A_MA7
R332 36_0201_1% — DDR_A_MA8
R333 36_0201_1% — DDR_A_MA15
R342 36_0201_1%

DDR3 CLK Termination

C1458 0.1U_0402_16V4Z
R1102 30.1_0402_1%
R1103 30.1_0402_1%
END topology
<6> DDR_A_CLK0
C1457 1.8P_0201_50V8C
<6> DDR_A_CLK0#

1.CAD Note: Cterm= 1.6pF should be kept near feeding point of first SDRAM

2.CAD Note: Rtt= 30.1ohms, Ctt= 0.1uF should be kept within 600mils from last SDRAM

Delete U70 SPD EEROM circuit
SA00004KS00
S IC EE 2K AT24C02C-XHM-T TSSOP 8P

External DDR Thermal Sensor

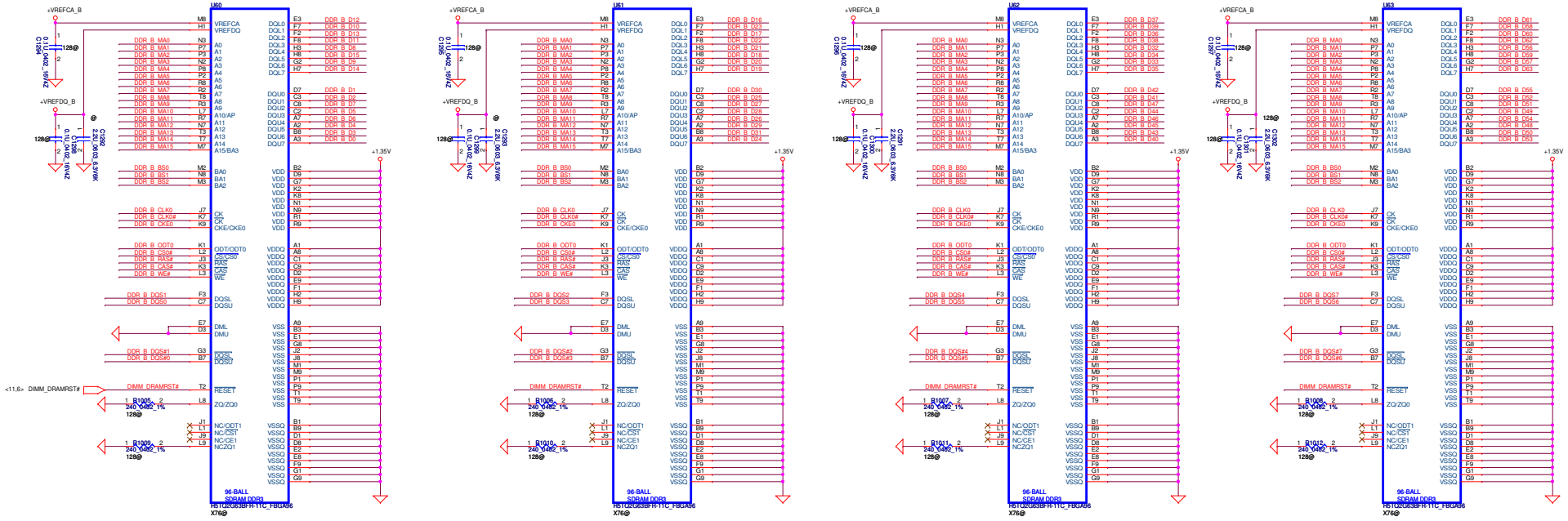
+3VS
C97 0.1U_0402_16V4Z
U4
VDD SCLK EC_SMB_CK2 <14,24,32>
D+ SDATA EC_SMB_DA2 <14,24,32>
D- ALERT# +3VS
THERM# GND
R546 15K_0402_5%
W83L771AWG-2 TSSOP8P
SA00003PU00

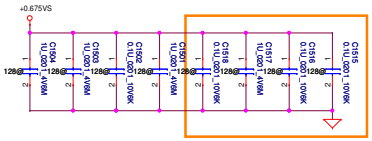
SA00003PU00
S IC W83L771AWG-2 TSSOP 8P SENSOR

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/4/6	Deciphered Date 2013/4/6	Title DDRIII DIMMA

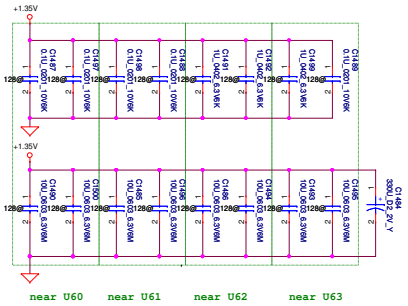
Size	Document Number	Rev
Custom	Q3ZMC M/B LA-8481P Schematic	1.0
Date: Thursday, April 12, 2012	Sheet 11 of 51	

Channel B

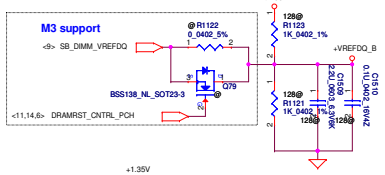


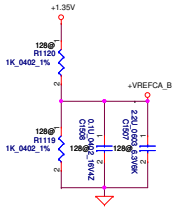


Layout Note:
Place near each memory part

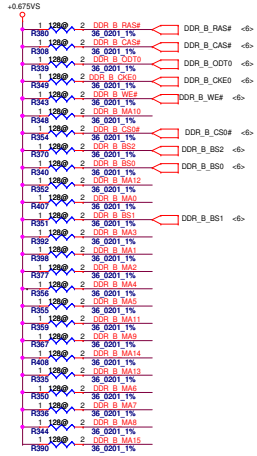


near U60 near U61 near U62 near U63



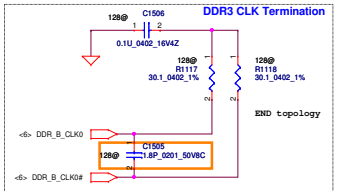


DDR3 CTL/ADD Termination



Delete U71 SPD EEROM circuit
SA00004KS00
S IC EE 2K AT24C02C-XHM-T TSSOP 8P

DDR3 CLK Termination

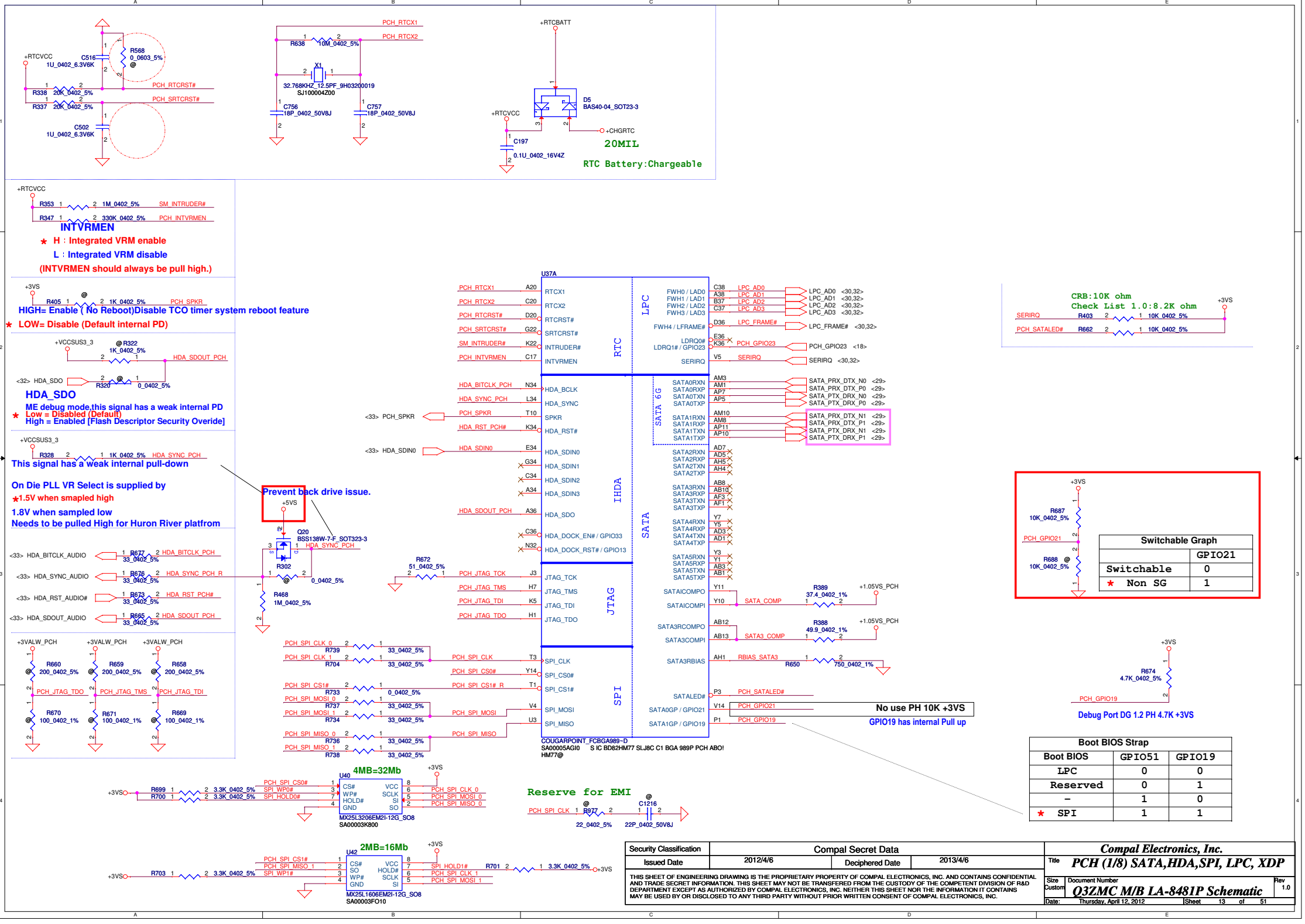


1.CAD Note: Cterm= 1.6pF should be kept near feeding point of first SDRAM

2.CAD Note: Rtt= 30.1ohms, Ctt= 0.1uF should be kept within 600mils from last SDRAM

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/4/6	Deciphered Date 2013/4/6	Title DDRIII DIMMB

Size Custom	Document Number Q3ZMC M/B LA-8481P Schematic		Rev 1.0
Date: Thursday, April 12, 2012	Sheet 12 of 51		



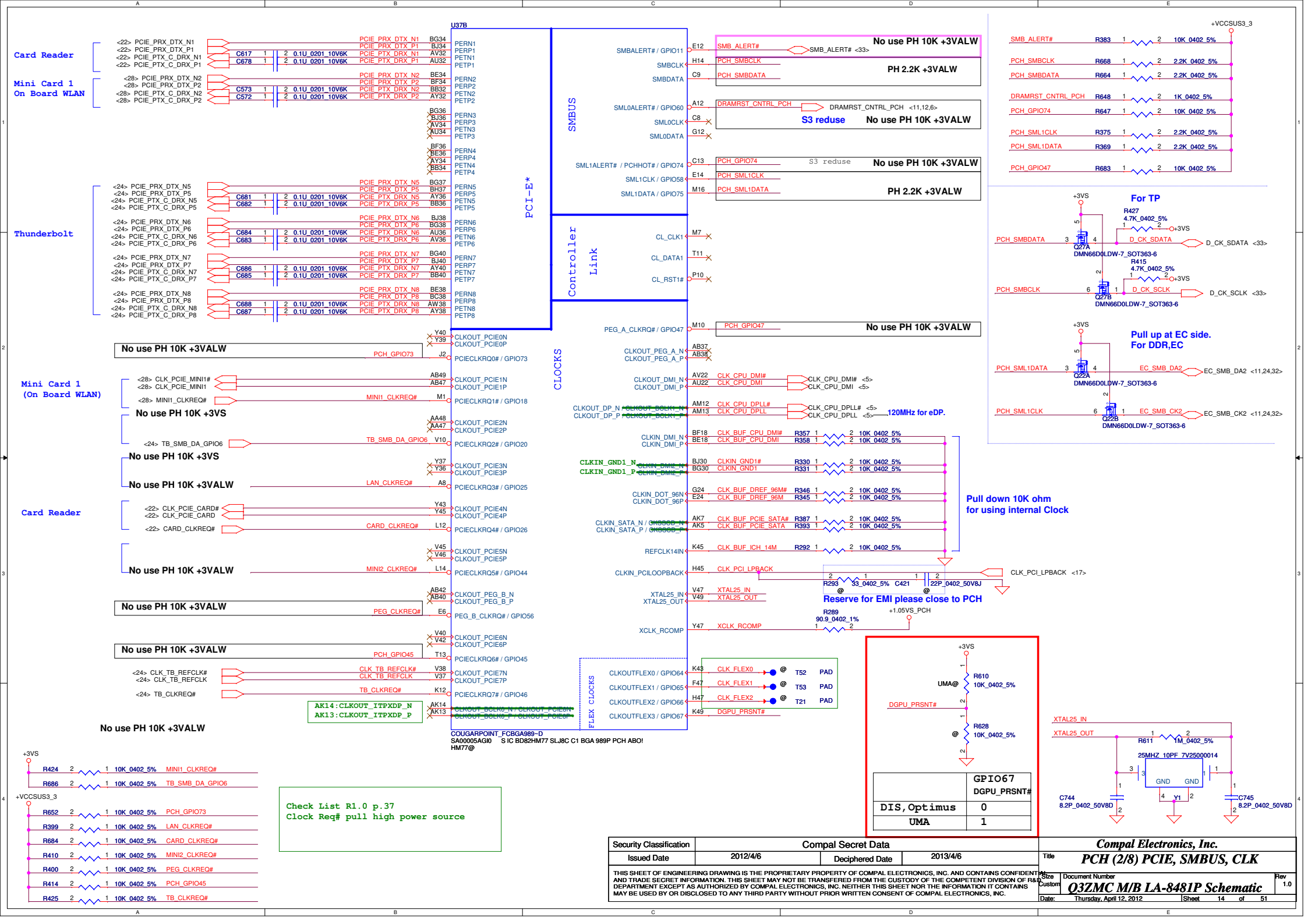
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

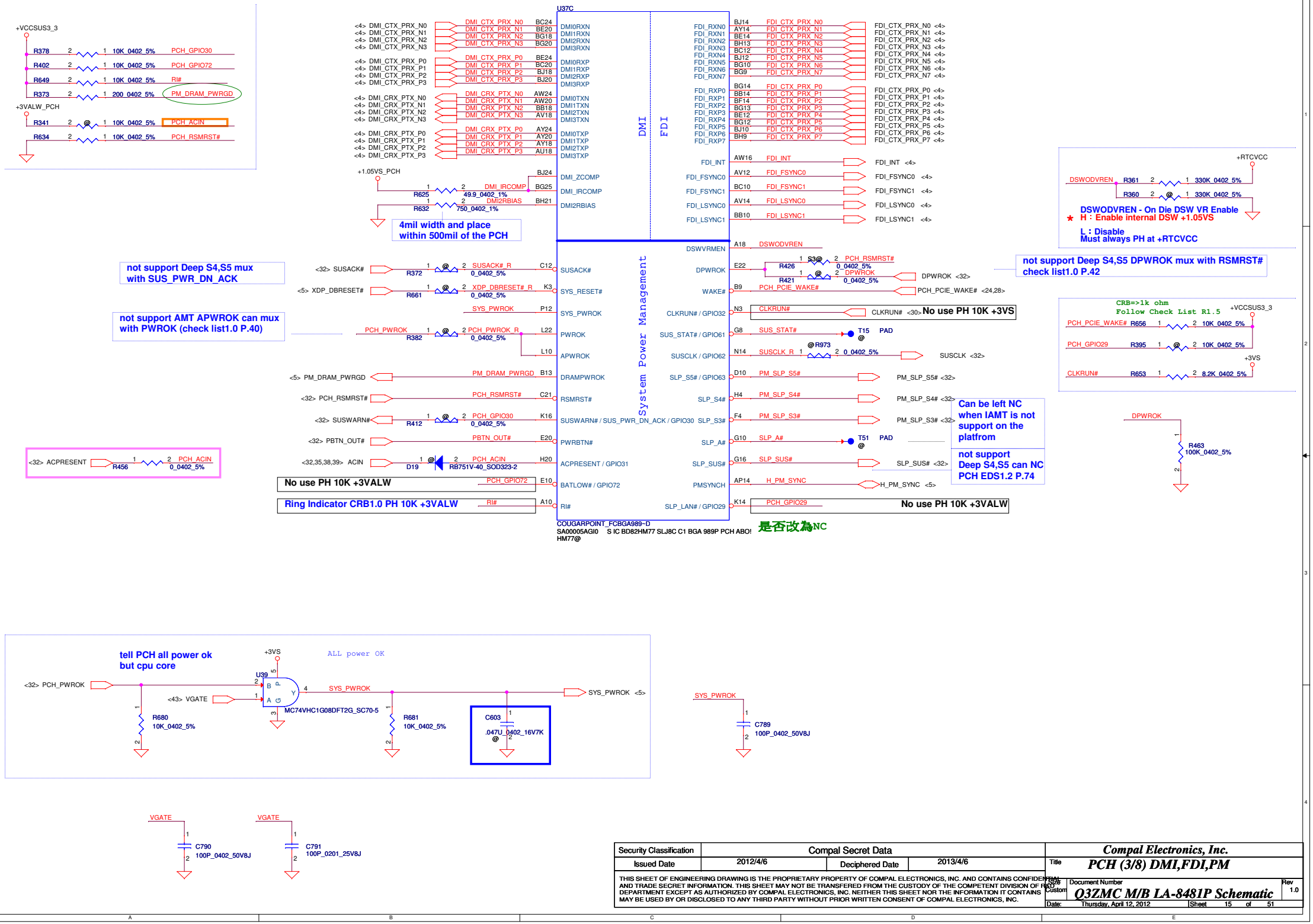
Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 13 of 51


Card Reader
Mini Card 1
On Board WLAN
Thunderbolt
Mini Card 1
(On Board WLAN)
Card Reader
U37B
PCI-E*
SMBUS
Controller
Link
CLOCKS
FLEX CLOCKS
No use PH 10K +3VALW
No use PH 10K +3VS
PH 2.2K +3VALW
S3 reduse
For TP
Pull up at EC side.
For DDR,EC
Pull down 10K ohm
for using internal Clock
Reserve for EMI please close to PCH
120MHz for eDP.
COUGARPOINT_FCBGA989~D
SA00005AGI0 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@
Check List R1.0 p.37
Clock Req# pull high power source
GPIO67
DGPU_PRSNT#
DIS,Optimus 0
UMA 1
Compal Electronics, Inc.
PCH (2/8) PCIE, SMBUS, CLK
Q3ZMC M/B LA-8481P Schematic
Security Classification
Compal Secret Data
Issued Date 2012/4/6
Deciphered Date 2013/4/6
Thursday, April 12, 2012
Sheet 14 of 51



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/4/6	Deciphered Date 2013/4/6	Title: PCH (3/8) DMI,FDI,PM

Size: Custom	Document Number: Q3ZMC M/B LA-8481P Schematic		Rev: 1.0
Date: Thursday, April 12, 2012	Sheet 15 of 51		

UMA Panel Backlight ON/OFF

<32> ENBKL — ENBKL — R612 2 @ 1 0_0402_5% — IGPU_BKLT_EN

PD 100K at EC side

U37D

IGPU_BKLT_EN — J47 L_BKLTEN
<22> PCH_ENVDD — M45 L_VDD_EN
<22> DPST_PWM — P45 L_BKLTCTL

Delete LVDS function

T40 L_DDC_CLK
K47 L_DDC_DATA
T45 L_CTRL_CLK
P39 L_CTRL_DATA
AF37 LVD_IBG
AF36 LVD_VBG
AE48 LVD_VREFH
AE47 LVD_VREFL

LVDS disable:
DATA/Clock/Control can NC
VCC_TX_LVDS,VCCA_LVDS connected to GND

AK39 LVDSA_CLK#
AK40 LVDSA_CLK
AN48 LVDSA_DATA#0
AM47 LVDSA_DATA#1
AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
AN47 LVDSA_DATA0
AM49 LVDSA_DATA1
AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3
AF40 LVDSB_CLK#
AF39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

LVDS

CRT disable:
DATA/Clock/Control can NC
DAC_IREF still need PD
VCCADAC connected to +3VS

N48 CRT_BLUE
P49 CRT_GREEN
T49 CRT_RED
T39 CRT_DDC_CLK
M40 CRT_DDC_DATA
M47 CRT_HSYNC
M49 CRT_VSYNC

CRT

CRT_IREF — T43 DAC_IREF
T42 CRT_IRTN

For CRT diable
=>Change 1K 0.5% to 5%

R307 1K_0402_5%

Digital Display Interface

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40

SDVO_CTRLDATA strap pull high at level shift page

SDVO_CTRLCLK P38 — SDVO_SCLK — SDVO_SCLK <23>
SDVO_CTRLDATA M39 — SDVO_SDATA — SDVO_SDATA <23>

DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 — PCH_DPB_HPD — PCH_DPB_HPD <23>

DDPB_0N AV42 — PCH_DPB_N0 — PCH_DPB_N0 <23> — HDMI D2
DDPB_0P AV40 — PCH_DPB_P0 — PCH_DPB_P0 <23> — HDMI D2
DDPB_1N AV45 — PCH_DPB_N1 — PCH_DPB_N1 <23> — HDMI D1
DDPB_1P AV46 — PCH_DPB_P1 — PCH_DPB_P1 <23> — HDMI D1
DDPB_2N AU48 — PCH_DPB_N2 — PCH_DPB_N2 <23> — HDMI D0
DDPB_2P AU47 — PCH_DPB_P2 — PCH_DPB_P2 <23> — HDMI D0
DDPB_3N AV47 — PCH_DPB_N3 — PCH_DPB_N3 <23> — HDMI CLK
DDPB_3P AV49 — PCH_DPB_P3 — PCH_DPB_P3 <23> — HDMI CLK

DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49

DDPD_CTRLCLK M43 — PCH_DPD_CLK — PCH_DPD_CLK <25>
DDPD_CTRLDATA M36 — PCH_DPD_DAT — PCH_DPD_DAT <25>
DDPD_AUXN AT45 — PCH_DPD_AUXN — PCH_DPD_AUXN <24>
DDPD_AUXP AT43 — PCH_DPD_AUXP — PCH_DPD_AUXP <24>
DDPD_HPD BH41 — DPD_HPD — DPD_HPD <24>

DDPD_0N BB43 — PCH_DPD_N0 — PCH_DPD_N0 <24> — Thunderbolt
DDPD_0P BB45 — PCH_DPD_P0 — PCH_DPD_P0 <24> — Thunderbolt
DDPD_1N BF44 — PCH_DPD_N1 — PCH_DPD_N1 <24> — Thunderbolt
DDPD_1P BE44 — PCH_DPD_P1 — PCH_DPD_P1 <24> — Thunderbolt
DDPD_2N BF42 — PCH_DPD_N2 — PCH_DPD_N2 <24> — Thunderbolt
DDPD_2P BE42 — PCH_DPD_P2 — PCH_DPD_P2 <24> — Thunderbolt
DDPD_3N BJ42 — PCH_DPD_N3 — PCH_DPD_N3 <24> — Thunderbolt
DDPD_3P BG42 — PCH_DPD_P3 — PCH_DPD_P3 <24> — Thunderbolt

COUGARPOINT_FCBGA989~D
SA00005AGI0 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@

+3VS
R252 1 2 2.2K_0402_5% PCH_DPD_CLK
R254 1 2 2.2K_0402_5% PCH_DPD_DAT

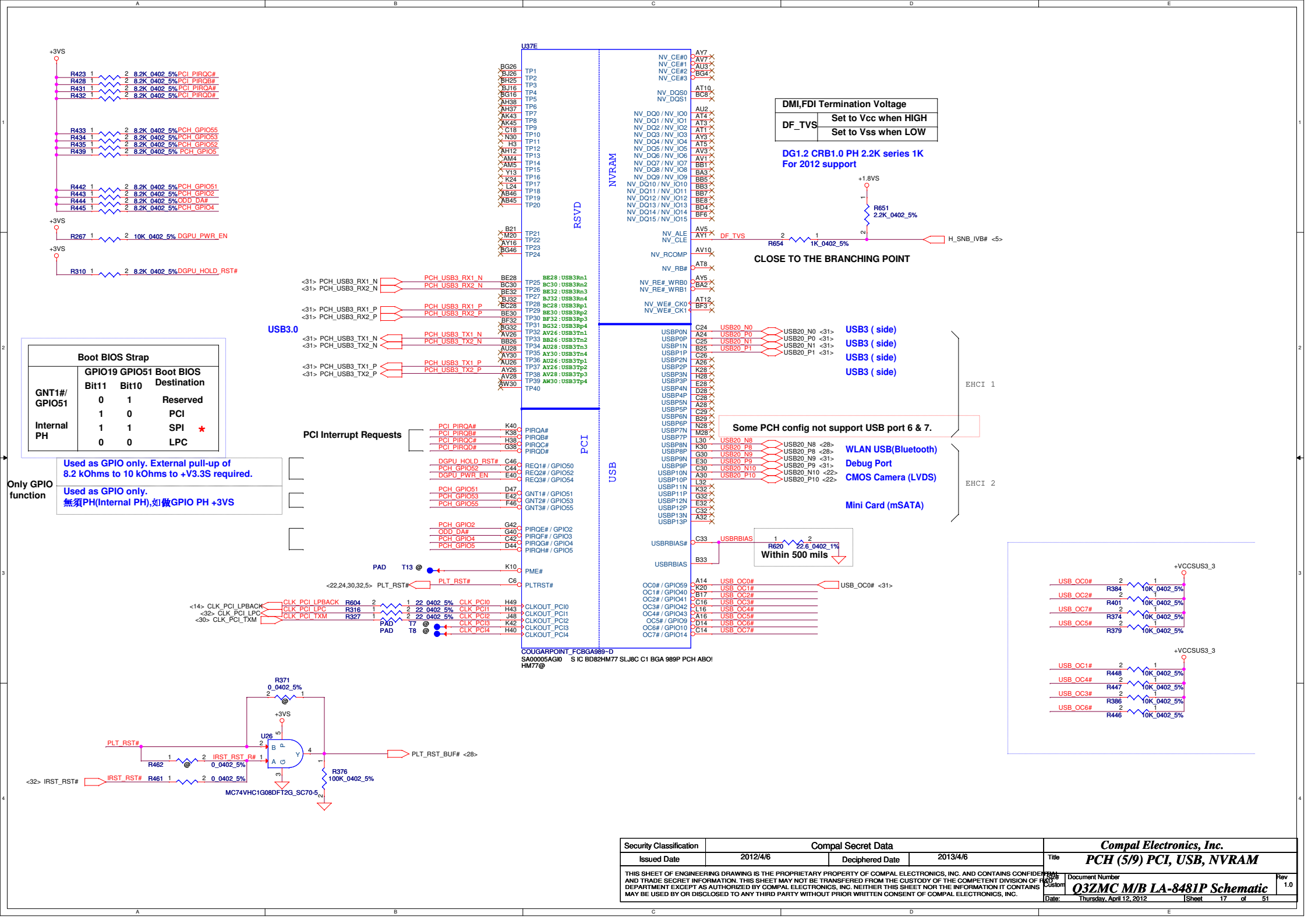
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 16 of 51



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 17 of 51

HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+VCCSUS3_3
R422 4.7K_0402_5%
PCH_GPIO28
R417 1K_0402_5%
Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND,HR Check list1.0 P.70

R362 10K_0402_5% PCH_GPIO27
HR Check List

R363 10K_0402_5% ODD_DETECT#
R364 10K_0402_5% WWAN_OFF#

SATA2GP/GPIO36,SATA3GP/GPIO37
1.Used as for Mechanical Presence detect -
Use a weak external pull-up (150K-200k Ohms) to Vcc3_3
or use 10K external pull-up that is enabled only
after PLTRST# de-assertion.

2.Used as GP Input (Pin HW default) -
Ensure GPI is not driven high during strap sampling window

3.Unused as GPIO or SATA*GP -
Use 8.2K-10K pull-down to ground.

+3VS
R406 @ 10K_0402_5% TB_PLUG_EVENT
R614 10K_0402_5% PCH_GPIO1
R326 10K_0402_5% DGPU_HPD_INT#
R663 10K_0402_5% MSATA_DET#
R305 10K_0402_5% DGPU_PWROK
R675 10K_0402_5% PCH_GPIO34
R679 10K_0402_5% PCH_GPIO48
R404 10K_0402_5% TB_SMB_CK_GPIO7

+VCCSUS3_3
R657 @ 10K_0402_5% TB_FORCE_PWR
R391 1K_0402_5% EC_LID_OUT#
R397 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
CRB1.0 PH10K to +3VALW

LVDS/eDP	GPIO71
LVDS	1
eDP	0

For eDP only,
不判斷eDP or LVDS

+3VS
@ R615 10K_0402_5%
PCH_GPIO71
@ R618 10K_0402_5%

+3VS
@R616 10K_0402_5%
PCH_GPIO69
R619 10K_0402_5%
+3VS
@R617 10K_0402_5%
PCH_GPIO70
R621 10K_0402_5%

Project ID	GPIO69	GPIO70
★ x	0	0
x	0	1
x	1	0
x	1	1

U37F

No use PH 10K +3VS <24> TB_PLUG_EVENT — TB_PLUG_EVENT — T7 BMBUSY# / GPIO0
No use PH 10K +3VS — PCH_GPIO1 — A42 TACH1 / GPIO1
No use PH 10K +3VS — DGPU_HPD_INT# — H36 TACH2 / GPIO6
<32> EC_SCI# — EC_SCI# — E38 TACH3 / GPIO7
<32> EC_SMI# — EC_SMI# — C10 GPIO8
No use PH +3VALW <24> TB_FORCE_PWR — TB_FORCE_PWR — C4 LAN_PHY_PWR_CTRL / GPIO12
EC LID SW OUT <32> EC_LID_OUT# — EC_LID_OUT# — G2 GPIO15
No use PH +3VALW
No use PH +3VS <29> MSATA_DET# — MSATA_DET# — U2 SATA4GP / GPIO16
DGPU_PWROK — D40 TACH0 / GPIO17
No use PH 10K +3VS — PCH_GPIO22 — T5 SCLOCK / GPIO22
CRB1.0 PH 10K +3VALW — PCH_GPIO24 — E8 GPIO24 / MEM_LED
No use PD 10K to GND — PCH_GPIO27 — E16 GPIO27
No use PH 10K +3VALW — PCH_GPIO28 — P8 GPIO28
No use PH 10K +3VS — PCH_GPIO34 — K1 STP_PCI# / GPIO34
No use can NC(+3VS power plane) <29> RAID0_DET — RAID0_DET — K4 GPIO35
Can't PH — ODD_DETECT# — V8 SATA2GP / GPIO36
Can't PH — WWAN_OFF# — M5 SATA3GP / GPIO37
No use PH 10K +3VS Optimus(L)/ non optimus(H) — OPTIMUS_EN# — N2 SLOAD / GPIO38
No use PH 10K +3VS — PCH_GPIO39 — M3 SDATAOUT0 / GPIO39
No use PH 10K +3VS — PCH_GPIO48 — V13 SDATAOUT1 / GPIO48
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS <24> TB_SMB_CK_GPIO7 — TB_SMB_CK_GPIO7 — V3 SATA5GP / GPIO49
No use PH +3VALW — PCH_GPIO57 — D6 GPIO57

TACH4 / GPIO68 — C40 — ODD_EN#
TACH5 / GPIO69 — B41 — PCH_GPIO69
TACH6 / GPIO70 — C41 — PCH_GPIO70
TACH7 / GPIO71 — A40 — PCH_GPIO71

GPIO

CPU/MISC
A20GATE — P4 — GATEA20 <32>
PECI — AU16 — PCH_PECI_R — 0_0402_5% — R248 — H_PECI <32,5>
RCIN# — P5 — EC_KBRST# — EC_KBRST# <32>
PROCPWRGD — AY11 — H_CPUPWRGD <5>
THRMTRIP# — AY10 — PCH_THRMTRIP#_R — R385 390_0402_5% — H_THRMTRIP# <5>
INIT3_3V# — T14

+3VS
R419 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut sown

INIT3_3V Check list1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

NC_1 — AH8
NC_2 — AK11
NC_3 — AH10
NC_4 — AK10
NC_5 — P37

TS_VSS1~4 PD to GND

+3VS
ODD_EN# R324 10K_0402_5%
EC_KBRST# R420 10K_0402_5%

VSS_NCTF_1 — A4
VSS_NCTF_2 — A44
VSS_NCTF_3 — A45
VSS_NCTF_4 — A46
VSS_NCTF_5 — A5
VSS_NCTF_6 — A6
VSS_NCTF_7 — B3
VSS_NCTF_8 — B47
VSS_NCTF_9 — BD1
VSS_NCTF_10 — BD49
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE49
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF49
VSS_NCTF_15 — BG2
VSS_NCTF_16 — BG48
VSS_NCTF_17 — BH3
VSS_NCTF_18 — BH47
VSS_NCTF_19 — BJ4
VSS_NCTF_20 — BJ44
VSS_NCTF_21 — BJ45
VSS_NCTF_22 — BJ46
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ6
VSS_NCTF_25 — C2
VSS_NCTF_26 — C48
VSS_NCTF_27 — D1
VSS_NCTF_28 — D49
VSS_NCTF_29 — E1
VSS_NCTF_30 — E49
VSS_NCTF_31 — F1
VSS_NCTF_32 — F49

NCTF

COUGARPOINT_FCBGA989~D
SA00005AGI0 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@

Remove NCTF test point
2011/9/23

+3VS
R429 UMA@ 10K_0402_5% OPTIMUS_EN#
R430 @ 10K_0402_5%

	GPIO38 OPTIMUS_EN#
Muxless	0
* nonMuxless	1

Define Q5LJ1(DDR3) or Q3ZMC(DDR3L)
+VCCSUS3_3
R458 DDR3@ 10K_0402_5% PCH_GPIO24
R457 DDR3L@ 10K_0402_5%

	GPIO24 PCH_GPIO24
* DDR3L(Q3ZMC)	0
DDR3	1

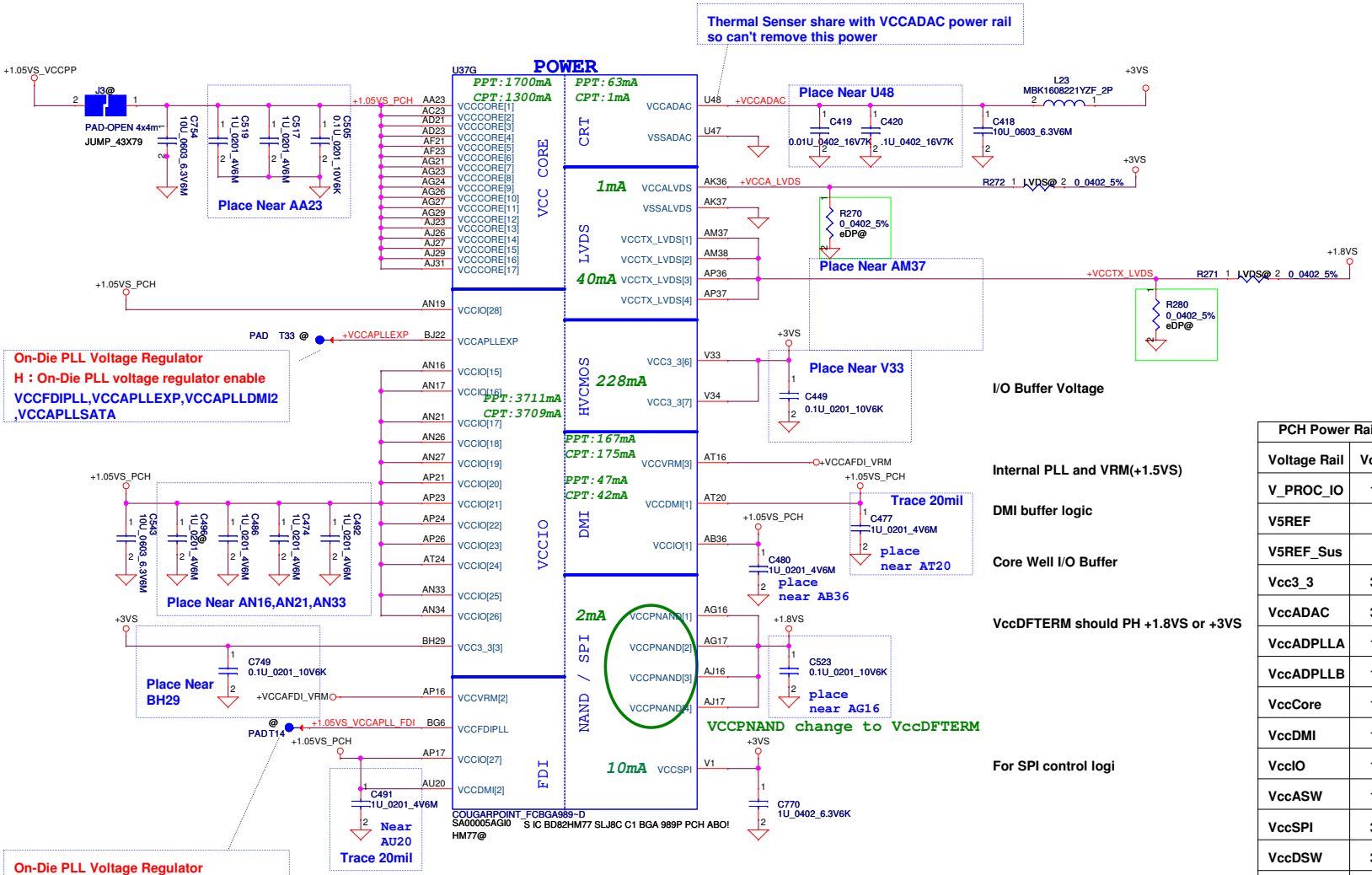
GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

	GPIO39	GPIO23	GPIO22
Elpida DDP 1GB*8 (Ch A,B)	0	0	0
Elpida DDP 1GB*4 (Ch A)	0	0	1
Elpida Mono 512MB*8(Ch A,B)	0	1	0
Hynix Mono 512MB*8(Ch A,B)	0	1	1

+3VS
R274 X76@ 10K_0402_5% PCH_GPIO22
R275 X76@ 10K_0402_5%
R278 X76@ 10K_0402_5% PCH_GPIO23 — PCH_GPIO23 <13>
R279 X76@ 10K_0402_5%
R281 X76@ 10K_0402_5% PCH_GPIO39
R282 X76@ 10K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.
Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom
Document Number: Q3ZMC M/B LA-8481P Schematic
Rev: 1.0
Date: Thursday, April 12, 2012
Sheet 18 of 51



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 19 of 51

For Deep SX turn off +V5REF_SUS,+VCCSUS3_3

+1.05V analog internal clock PLL Can NC

Not support Deep S4,S5 connect to +3VALW

suppied by internal 1.05V VR must NC

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

suppied by internal 1.05V VR must NC

suppied by internal 1.05V VR Must NC

isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG34)
18mil width(DIFFCLKN)
10mil (SSC)

VCCIO[8,9,11] change to VccDIFFCLKN
VCCIO[10] change to VccSSC

Deep S3
PPT:126mA
CPT:119mA

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

Need +3VALW and 0.1U close PCH

20mil
10mil

U37J POWER

COUGARPOINT_FCBGA989-D
SA00005AGI0 S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
HM77@

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

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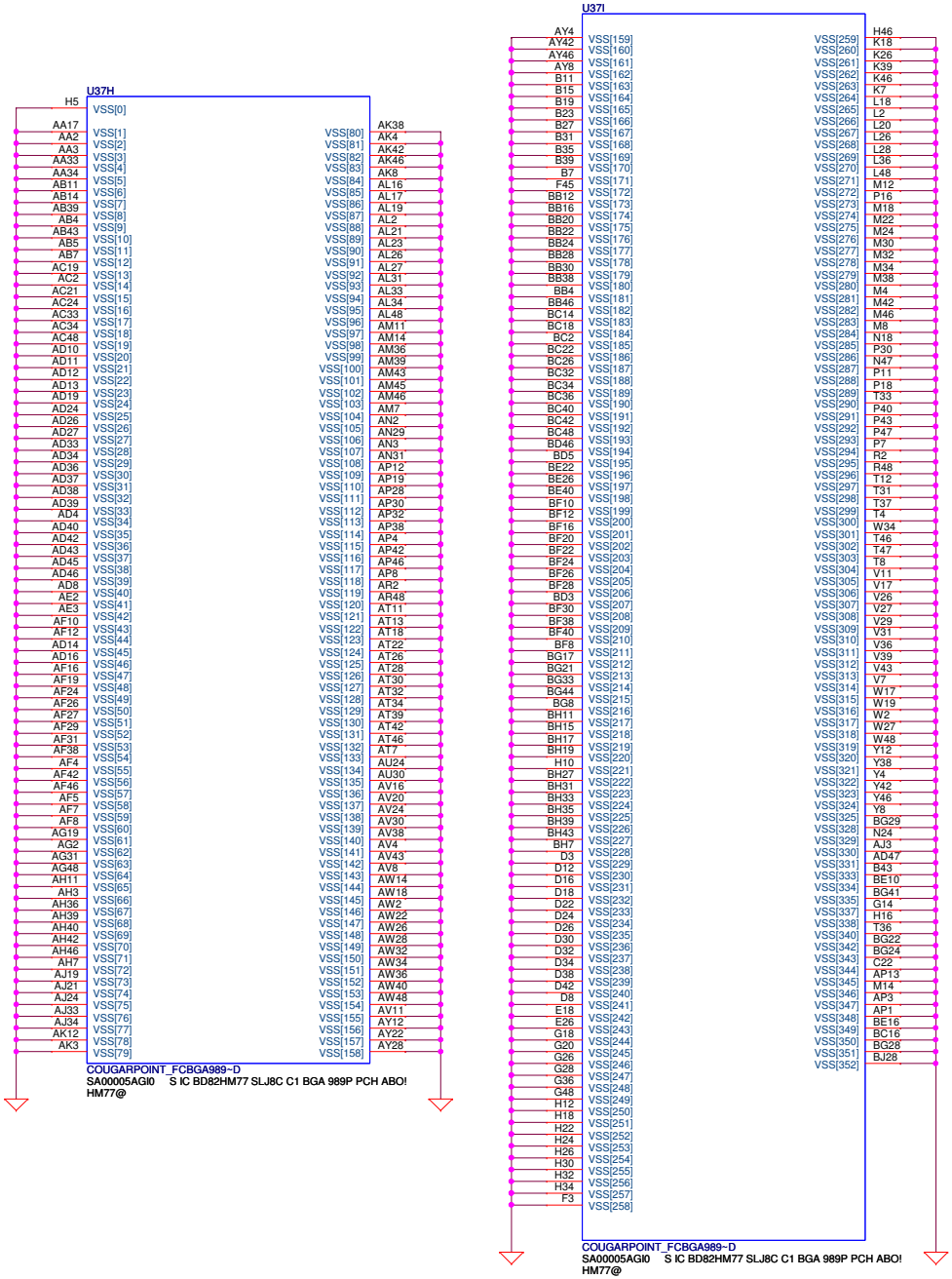
Title: PCH (8/9) PWR

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 20 of 51



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

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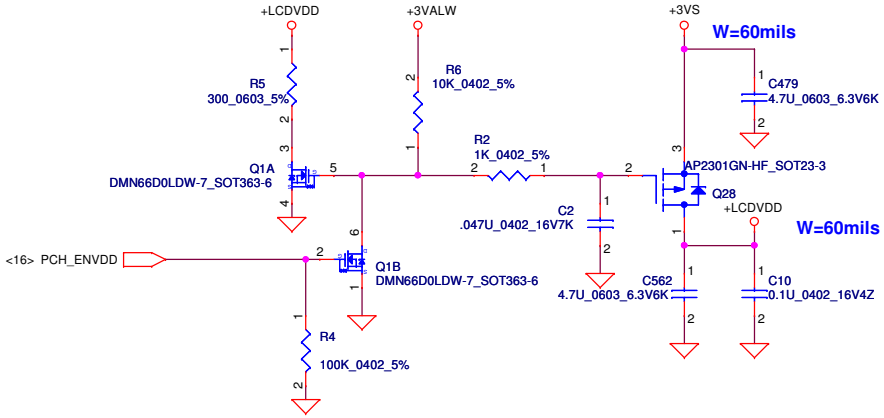
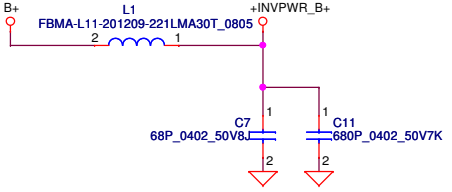
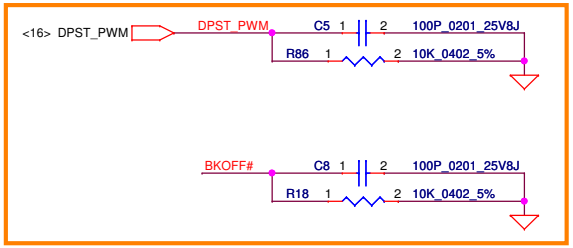
Panel POWER CIRCUIT

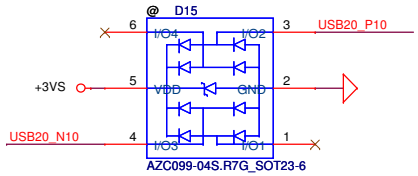


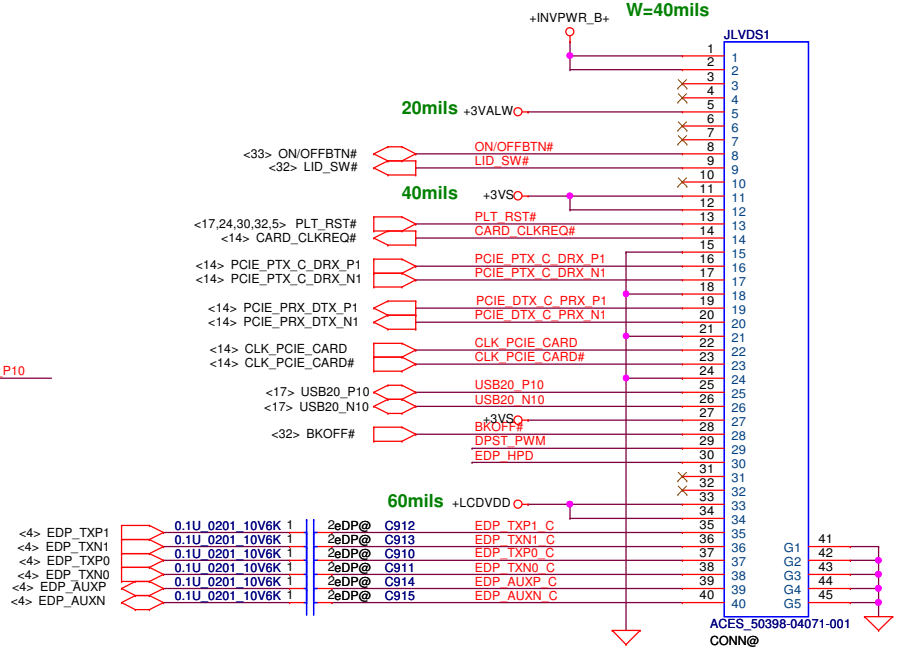
SM010014520 3000ma
220ohm@100mhz
DCR 0.04

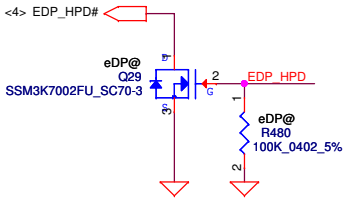


eDP panel + Card Reader Conn.

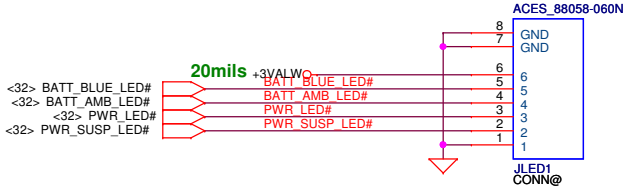








To LED/B Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
Custom	Q3ZMC M/B LA-8481P Schematic	1.0
Date: Thursday, April 12, 2012	Sheet 22 of 51	

W=40mils

+HDMI_5V_OUT

+5VS — F1 (1.1A_6VDC_FUSE) — C345 0.1U_0402_16V4Z

<16> PCH_DPB_N0	C280	.1U_0402_16V7K	HDMI_TX2-
<16> PCH_DPB_P0	C281	.1U_0402_16V7K	HDMI_TX2+
<16> PCH_DPB_N1	C283	.1U_0402_16V7K	HDMI_TX1-
<16> PCH_DPB_P1	C282	.1U_0402_16V7K	HDMI_TX1+
<16> PCH_DPB_N2	C287	.1U_0402_16V7K	HDMI_TX0-
<16> PCH_DPB_P2	C286	.1U_0402_16V7K	HDMI_TX0+
<16> PCH_DPB_N3	C285	.1U_0402_16V7K	HDMI_CLK-
<16> PCH_DPB_P3	C284	.1U_0402_16V7K	HDMI_CLK+

+3VS

R250 2.2K_0402_5% SDVO_SCLK

R253 2.2K_0402_5% SDVO_SDATA

Pull high at connector side

+3VS — @ R785 0_0402_5%

+HDMI_5V_OUT

R257 2.2K_0402_5% — R255 2.2K_0402_5%

<16> SDVO_SCLK — SDVO_SCLK — Q16A DMN66D0LDW-7_SOT363-6 — HDMI_SCLK

<16> SDVO_SDATA — SDVO_SDATA — Q16B DMN66D0LDW-7_SOT363-6 — HDMI_SDATA

Place closed to JHDMI1

HDMI_TX2-	R592 680_0402_5%	HDMI_GND
HDMI_TX2+	R594 680_0402_5%	
HDMI_TX1-	R583 680_0402_5%	
HDMI_TX1+	R587 680_0402_5%	
HDMI_TX0-	R564 680_0402_5%	
HDMI_TX0+	R570 680_0402_5%	
HDMI_CLK-	R573 680_0402_5%	
HDMI_CLK+	R590 680_0402_5%	

+3VS — Q14B DMN66D0LDW-7_SOT363-6

+3VS — R198 1M_0402_5% — Q14A DMN66D0LDW-7_SOT363-6

<16> PCH_DPB_HPD — HDMI_HPD

R219 100K_0402_5% — C324 100P_0201_25V8J

HDMI connector

JHDMI1

HDMI_HPD	19	HP_DET	
+HDMI_5V_OUT	18	+5V	
	17	DDC/CEC_GND	
HDMI_SDATA	16	SDA	
HDMI_SCLK	15	SCL	
	14	Reserved	
	13	CEC	
HDMI_CLK-	12	CK-	
	11	CK_shield	
HDMI_CLK+	10	CK+	
HDMI_TX0-	9	D0-	
	8	D0_shield	
HDMI_TX0+	7	D0+	
HDMI_TX1-	6	D1-	
	5	D1_shield	
HDMI_TX1+	4	D1+	GND 20
HDMI_TX2-	3	D2-	GND 21
	2	D2_shield	GND 22
HDMI_TX2+	1	D2+	GND 23

CONCR_099AMAC19CBACNF

CONN@

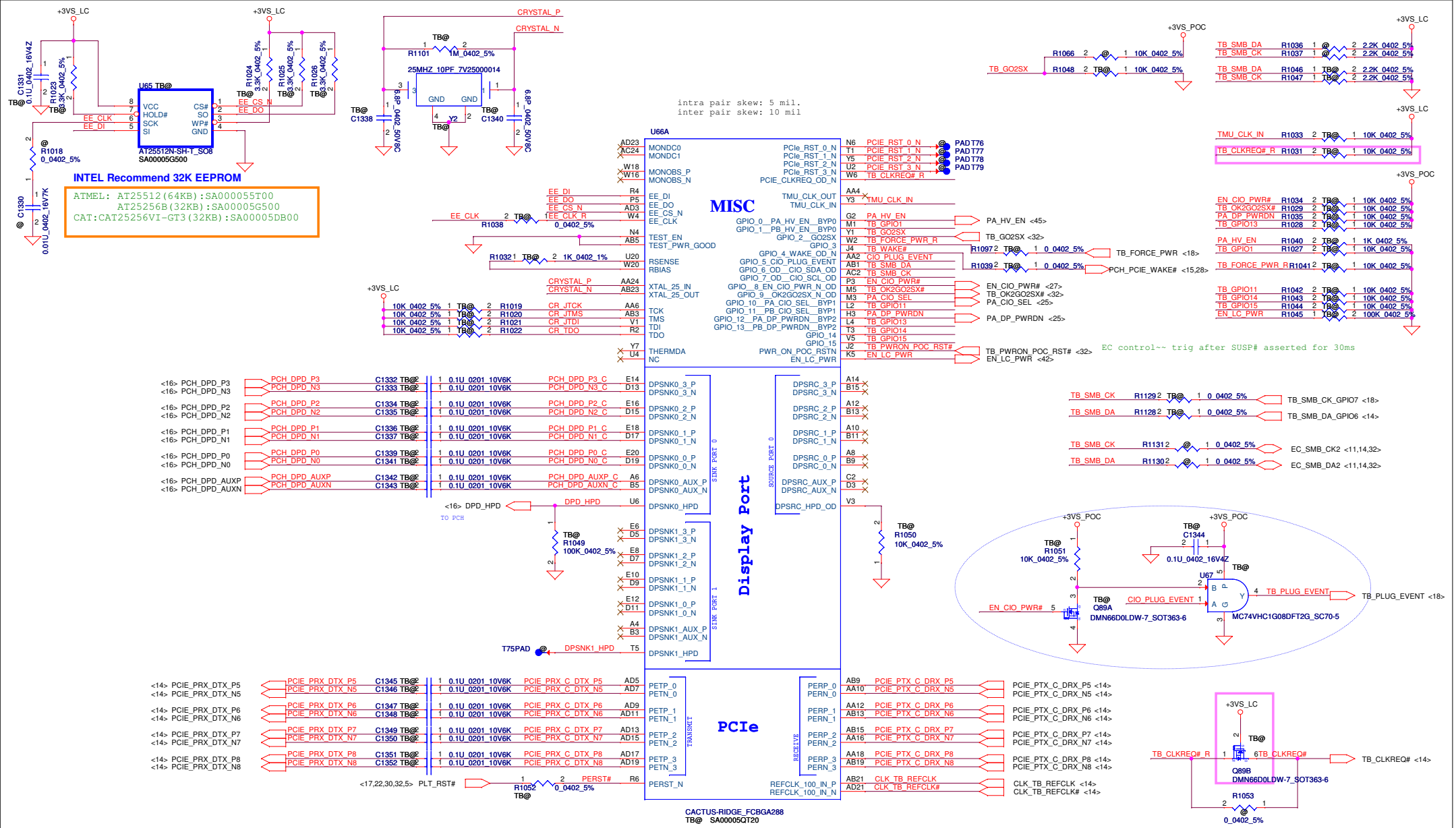
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: HDMI Connector

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 23 of 51



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: Intel Thunderbolt(1/4)

Size	Document Number	Rev
Custom	Q3ZMC M/B LA-8481P Schematic	1.0

Date: Thursday, April 12, 2012 Sheet 24 of 51

Function	SEL/HPD_SEL /AUX_SEL
Port A is active	L
Port B is active	H

U68
PI3VEDP212ZLEX_TQFN32_6X3-D
TB@

U66B
CACTUS-RIDGE_FCBGA288
TB@ SA00005QT20

All Thunderbolt TX traces have pi filter when embedded capacitors before and after inductor should be 0.45pF

Route Thunderbolt traces as 85 Ohm control impedance.
Match inside pair 2 mil.Match between lanes NA
Thunderbolt lenght must be between 0.8 inch to 2 inch

HPD	CFG1	CFG2	LSrx	Mode	Comments
1	0	0	X	DP	
1	1	X	X	HDMI	
0	0	1	0	TBT	TBT cable but no TBT link
0	0	1	1	TBT	TBT mode
0	X	0	X	None	Cable is disconnected

U3 TB@
74AHC1G125GW_SOT353-5

D42 @ L05ESDL5V0NA-4 SLP2510P8
D43 @ L05ESDL5V0NA-4 SLP2510P8
D44 @ L05ESDL5V0NA-4 SLP2510P8

JTB1
JAE_SP11-11986-T01

60mil
40mil
40mil
40mil
40mil

Pull High +3VS at PCH side

Current limited:
Ilim = 40Kohm/Rset

EN	HV_EN	OUT
0	0	0V
0	1	0V
1	0	3.3V
1	1	12V

PA_CFG1_LSEO0, PA_CFG2_LSOE0 should be used by GPU as the DP CONFIG1/CONFIG2 inputs, if required

VCC_DP@3V, max current 500mA
VCC_DP@12V, max current 0.8A

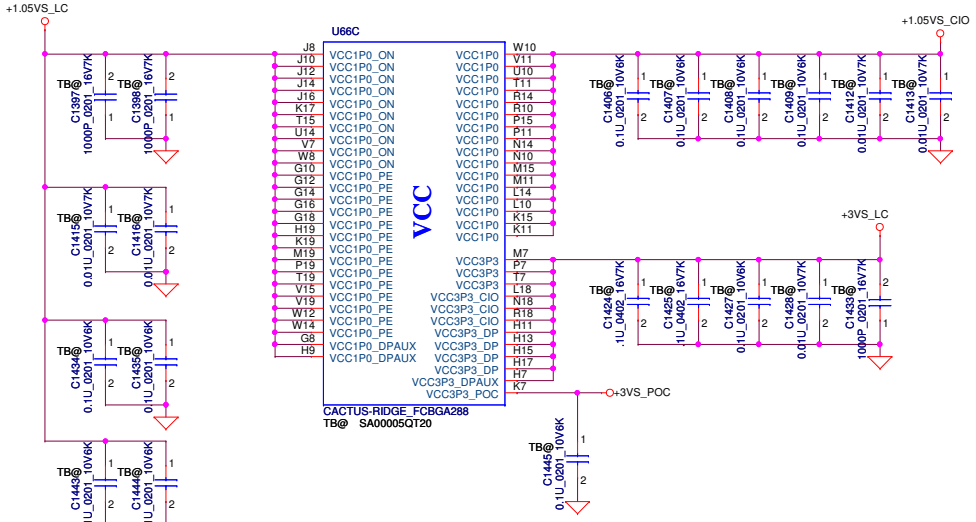
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

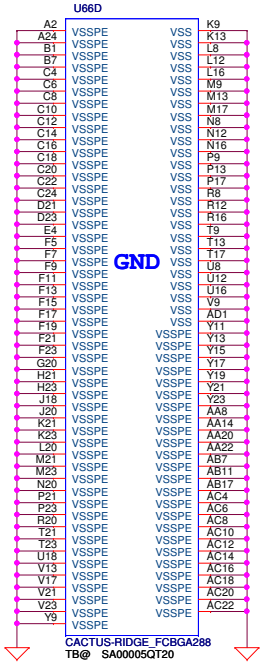
Compal Electronics, Inc.

Title: Intel Thunderbolt(2/4)

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 25 of 51





Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

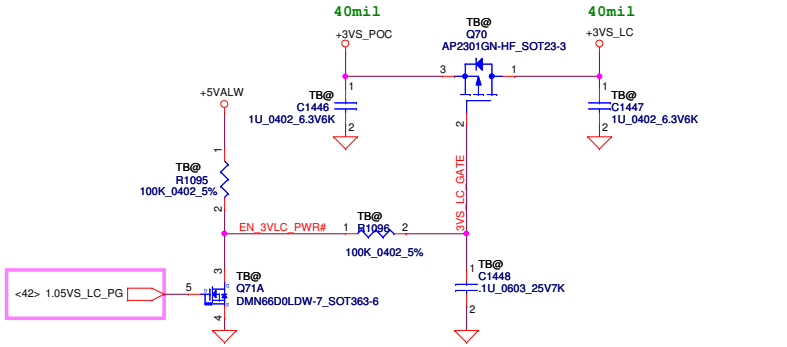
Title: Intel Thunderbolt(3/4)

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

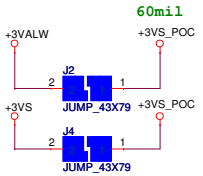
Date: Thursday, April 12, 2012 | Sheet 26 of 51

+3VS_POC to +3VS_LC

VCC3V3_LC max current 350mA

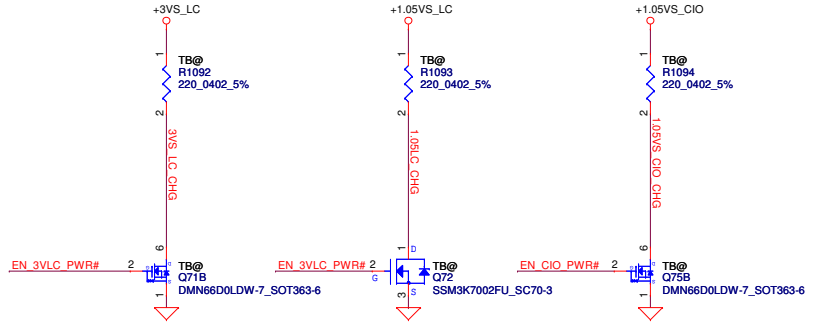


+3VALW to +3VS_POC



VCC3V3POC, IC CONN max current 500mA ,
VCC3V3POC, DP CONN max current 500mA ,
VCC3V3POC to VCC3V3 max current 350mA ,

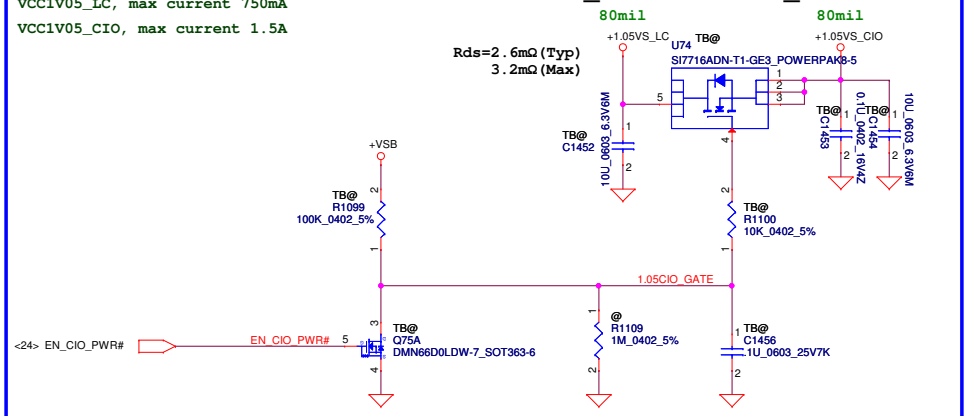
Discharge circuit

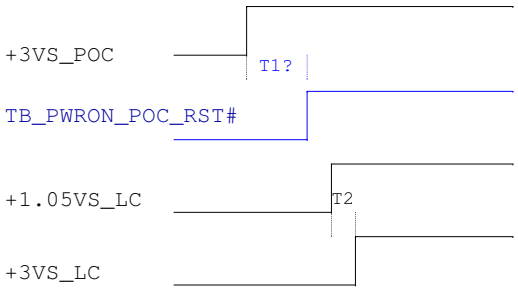


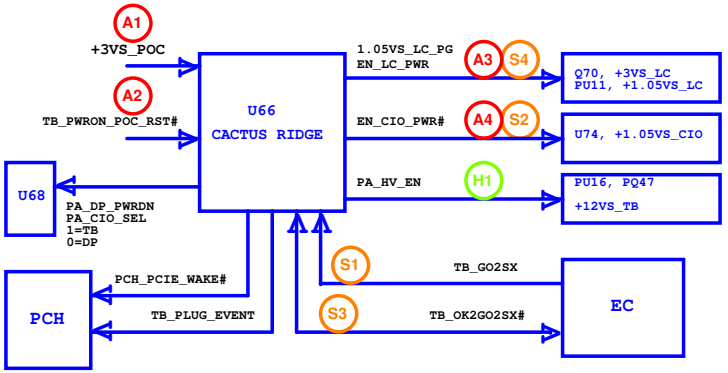
_VCC1V05_LC,max current 750mA
_VCC1V05_CIO,max current 1.5A
_VCC3V3POC,max current 5mA
_VCC3V3_LC,max current 350mA
_VCC_DP@3V,max current 500mA
_VCC_DP@12V,max current 0.8A
in the case of 12V min power should be 10W

+1.05VS_LC to +1.05VS_CIO

VCC1V05_LC, max current 750mA
VCC1V05_CIO, max current 1.5A



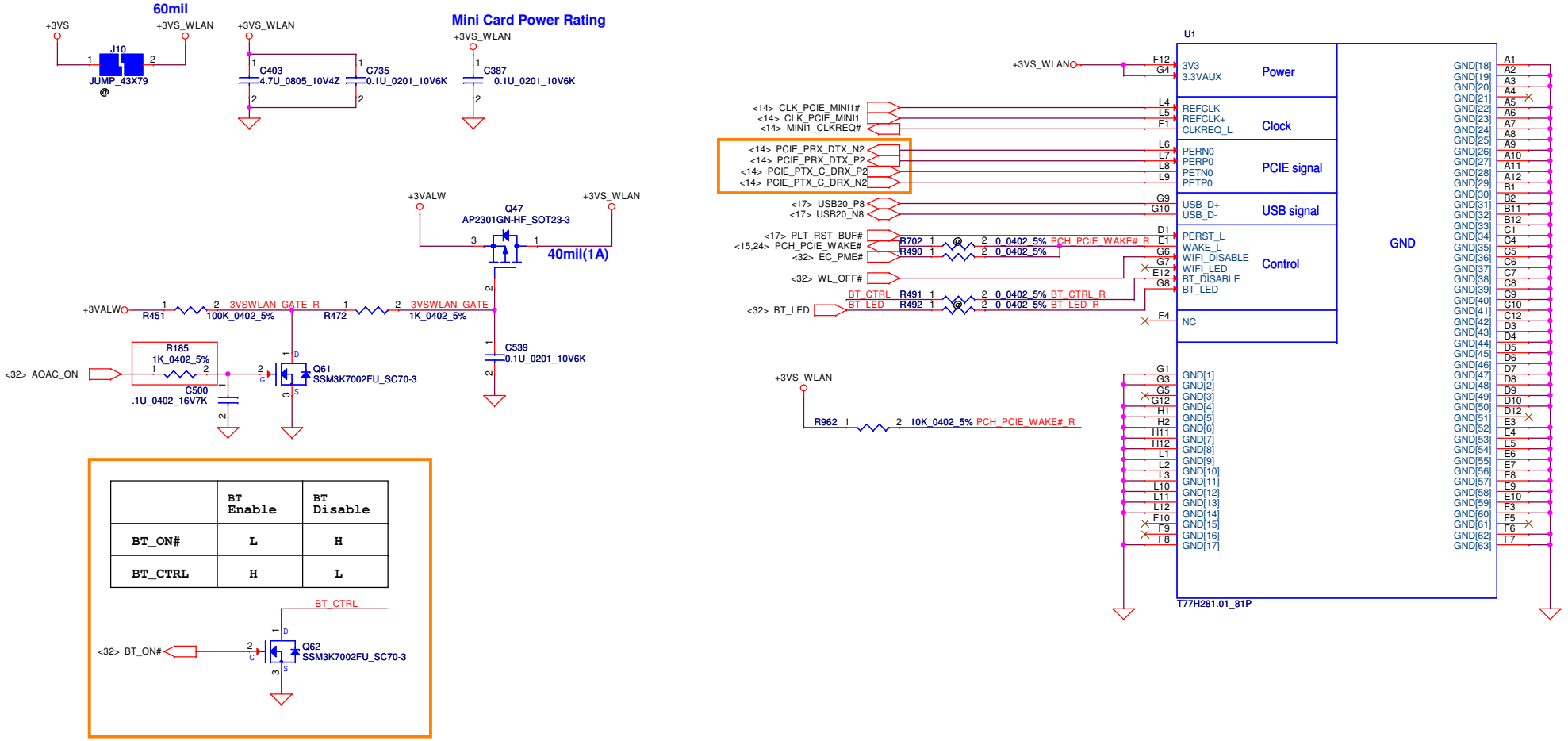




Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/4/6	Deciphered Date 2013/4/6	Title: Intel Thunderbolt(4/4)

Size: Custom	Document Number: Q3ZMC M/B LA-8481P Schematic		Rev: 1.0
Date: Thursday, April 12, 2012	Sheet 27 of 51		

For Wireless LAN



	BT Enable	BT Disable
BT_ON#	L	H
BT_CTRL	H	L

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/4/6	Deciphered Date	2013/4/6
Title	On Board WLAN		
Size: Custom	Document Number: Q3ZMC M/B LA-8481P Schematic		Rev: 1.0
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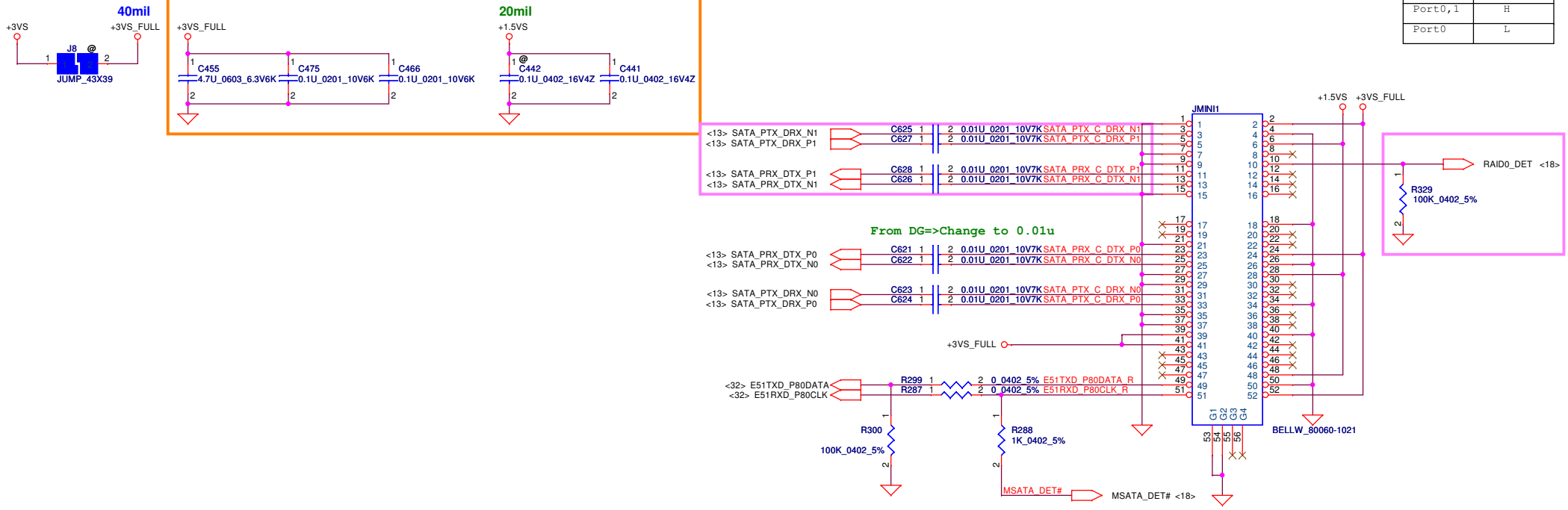
For mSATA

Function	RAID0_DET
Port0,1	H
Port0	L



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: mSATA HDD Connector

Size	Document Number	Rev
Custom	Q3ZMC M/B LA-8481P Schematic	1.0

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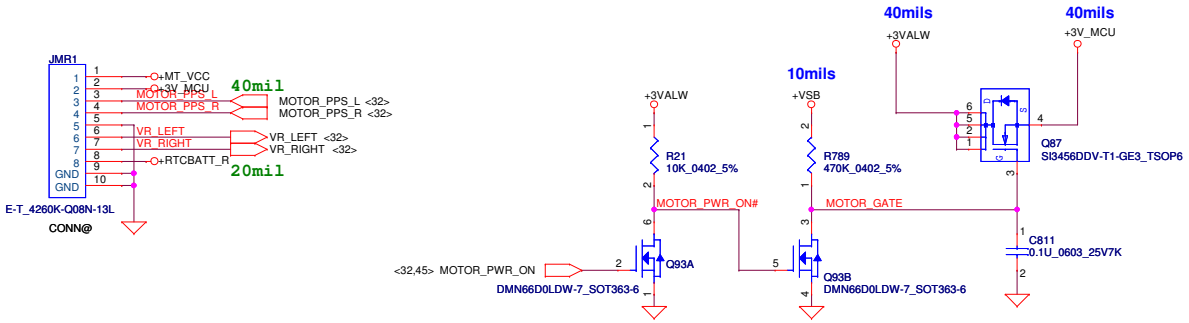
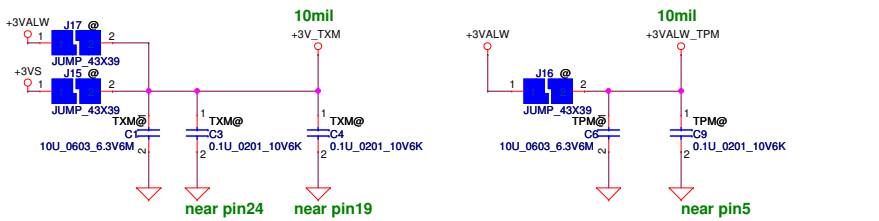
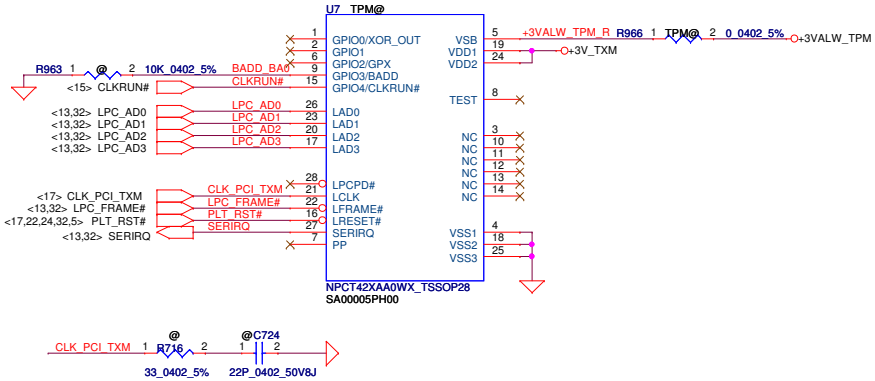
MOTOR/RTC



TPM





TPM -Address:
Pin9 BADD
1: 7Eh-7Fh (Default)
0: EEh-EFh

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: TPM

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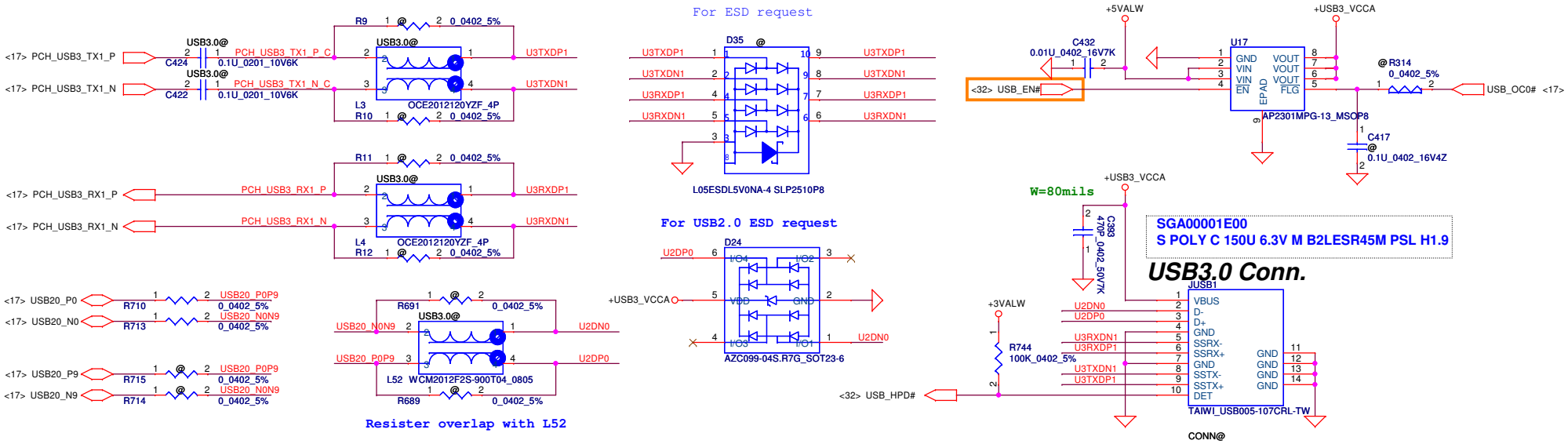

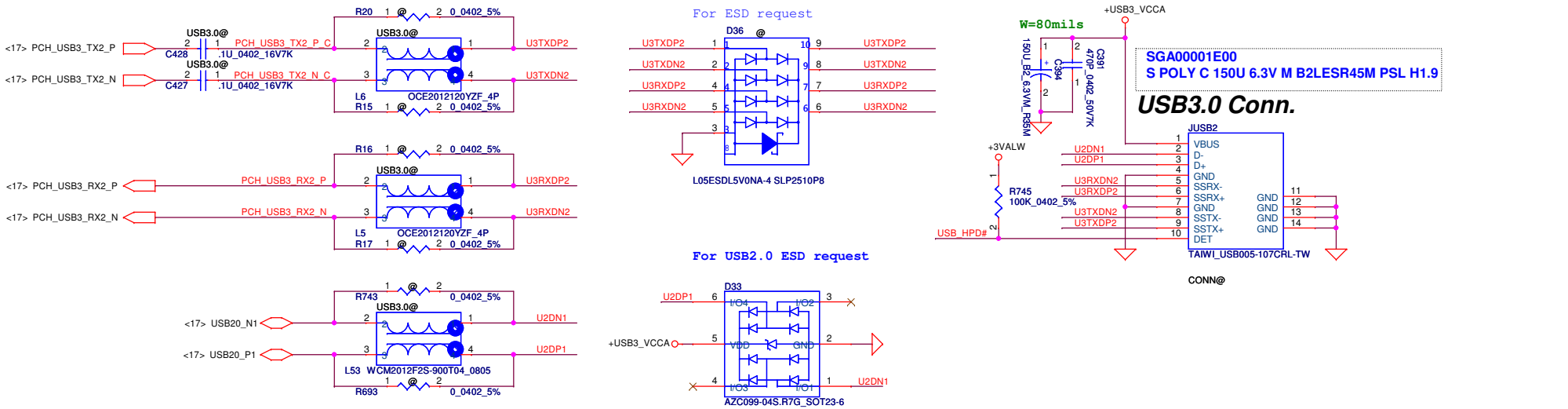

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Title	USB3.0		
Size: Custom	Document Number: Q3ZMC M/B LA-8481P Schematic		Rev: 1.0
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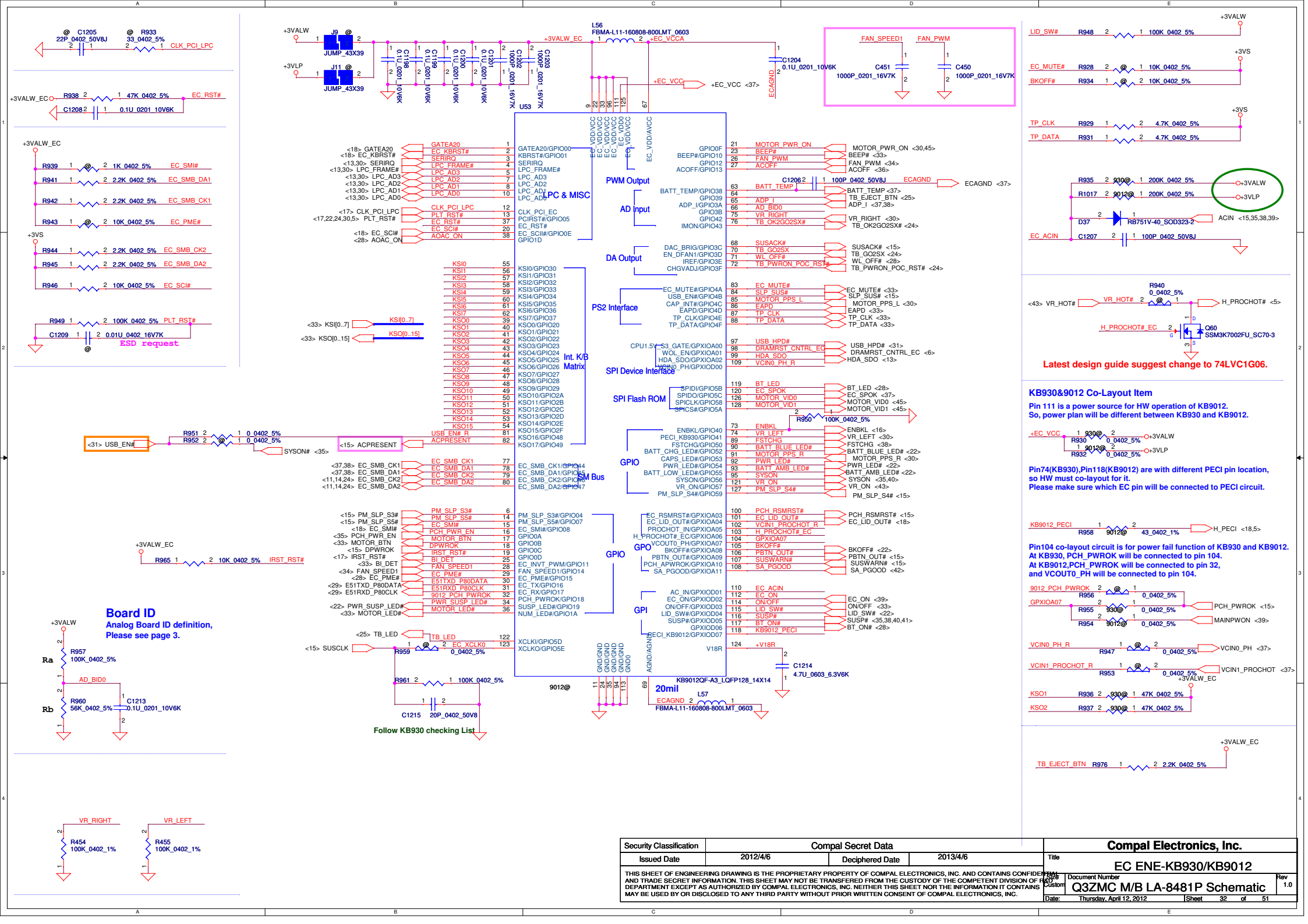

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: EC ENE-KB930/KB9012

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

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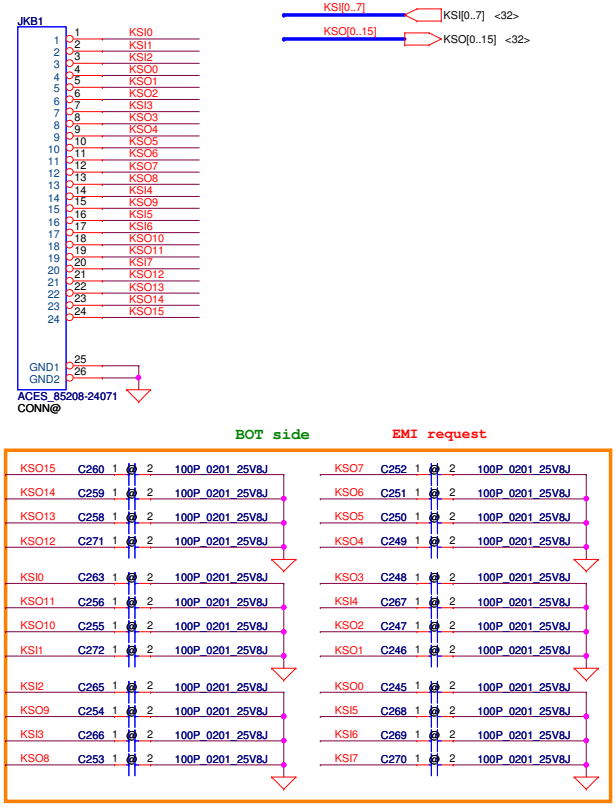
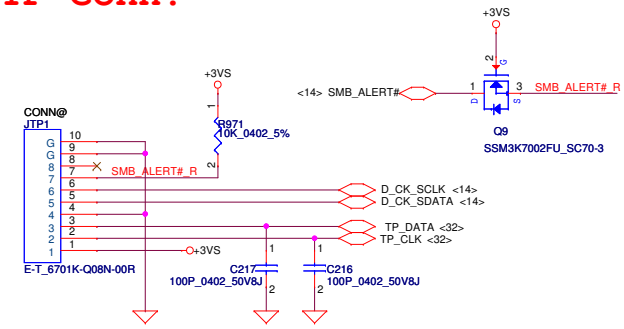
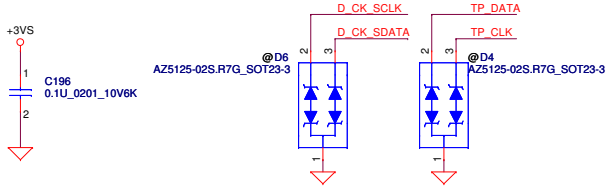
KB Conn.



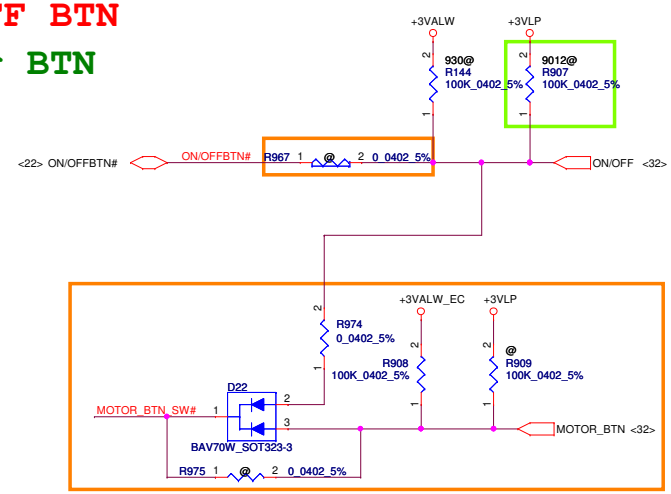
TP Conn.



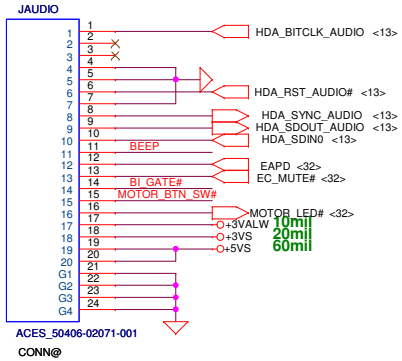


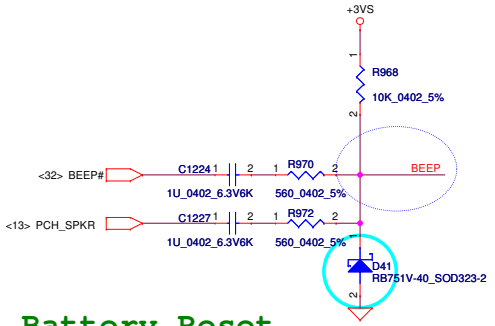
ON/OFF BTN

Motor BTN

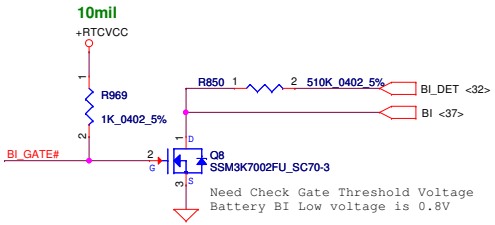


Audio/B 20pin





Battery Reset



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

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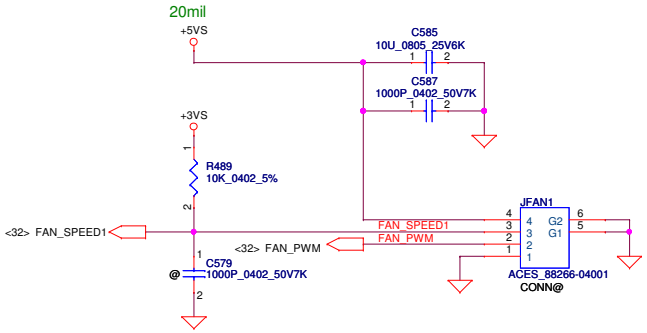
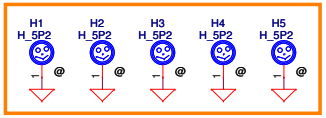
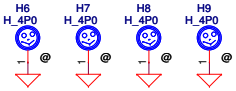
FAN Conn



Stand-Off



Thermal module



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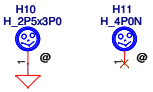

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/4/6	Deciphered Date 2013/4/6	Title: Step Motor,FAN,Screw Hole

Size: Custom	Document Number: Q3ZMC M/B LA-8481P Schematic		Rev: 1.0
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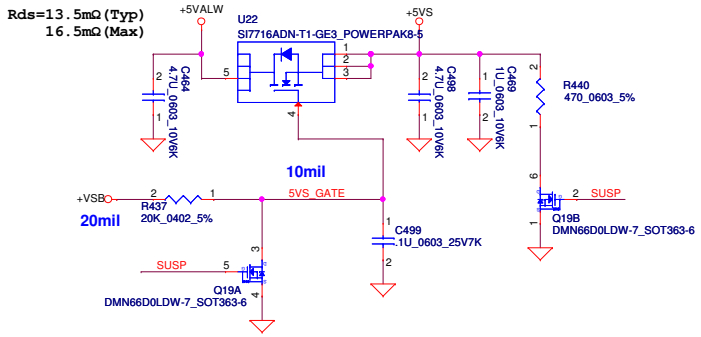
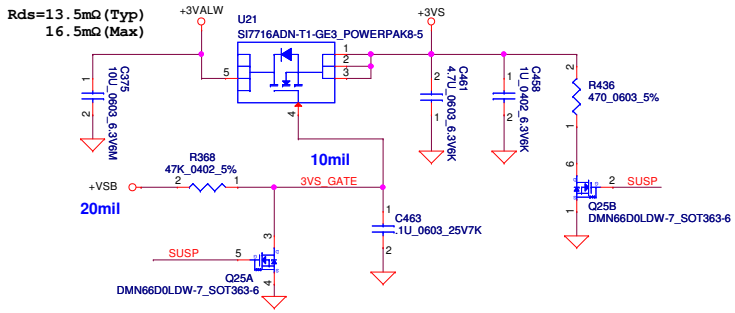
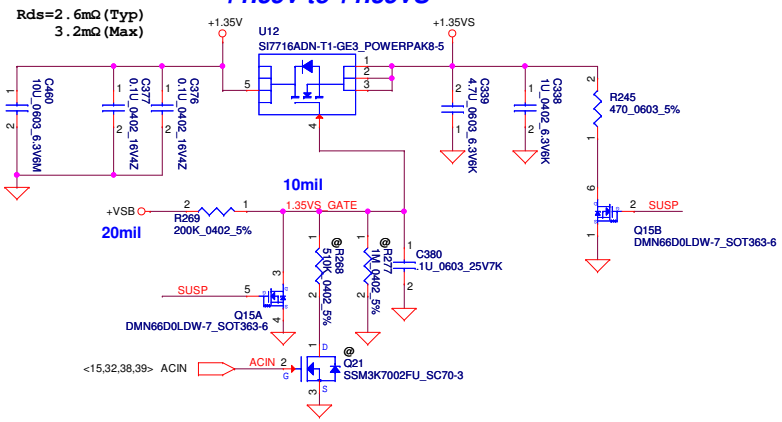
+5VALW to +5VS

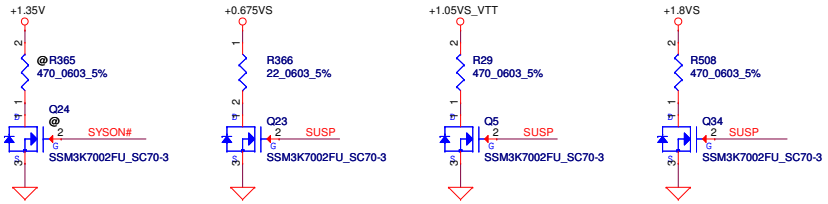


+3VALW to +3VS

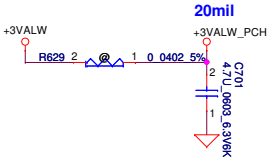


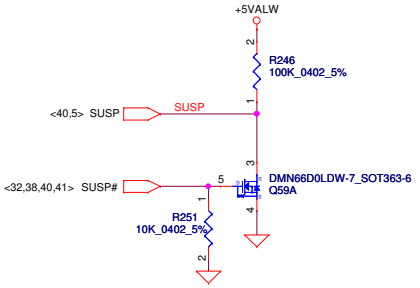
+1.35V to +1.35VS

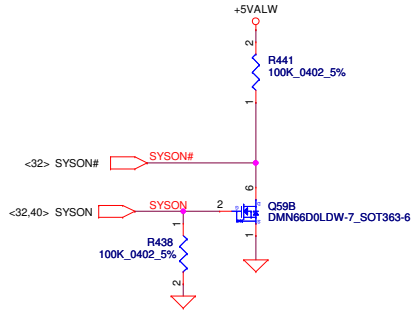


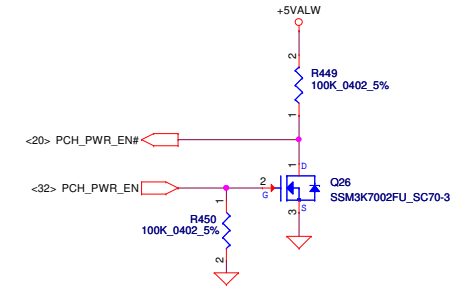


+3VALW to +3VALW_PCH(PCH AUX Power)









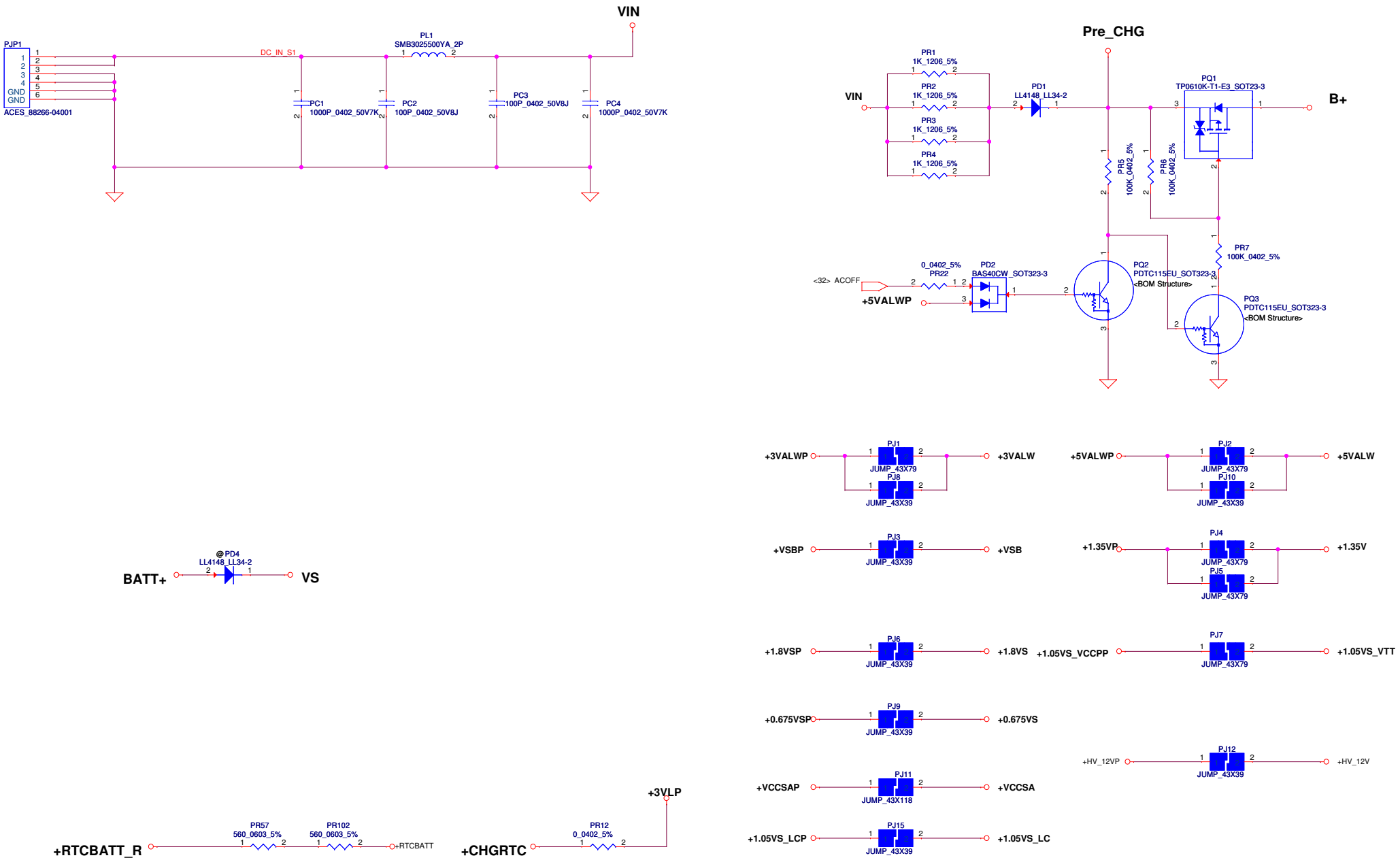
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 35 of 51



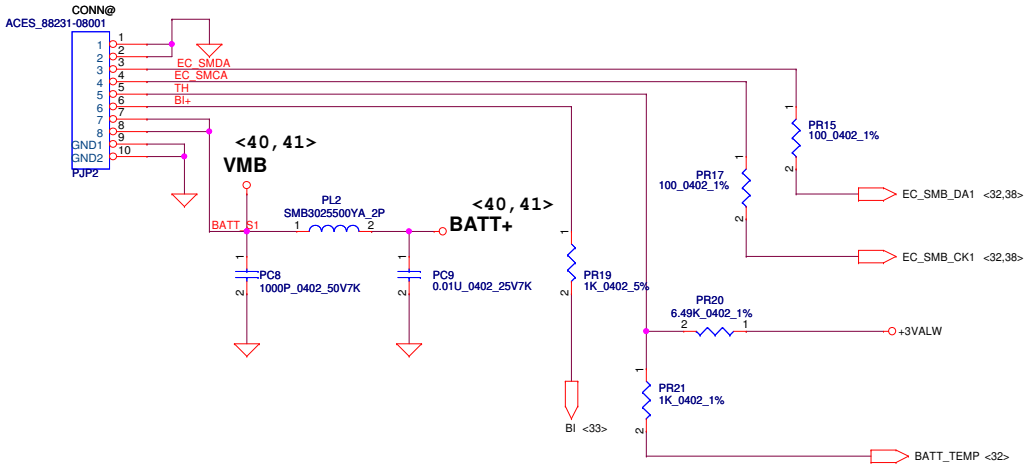
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: **DCIN/PRECHARGE**

Size	Document Number	Rev
Custom	*Chief River VC*	1.0

Date: Thursday, April 12, 2012 | Sheet 36 of 51

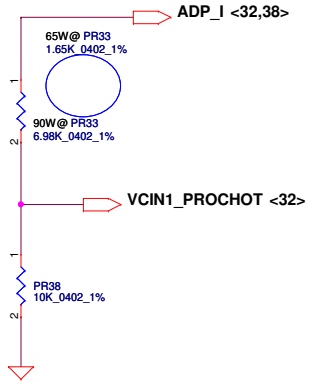


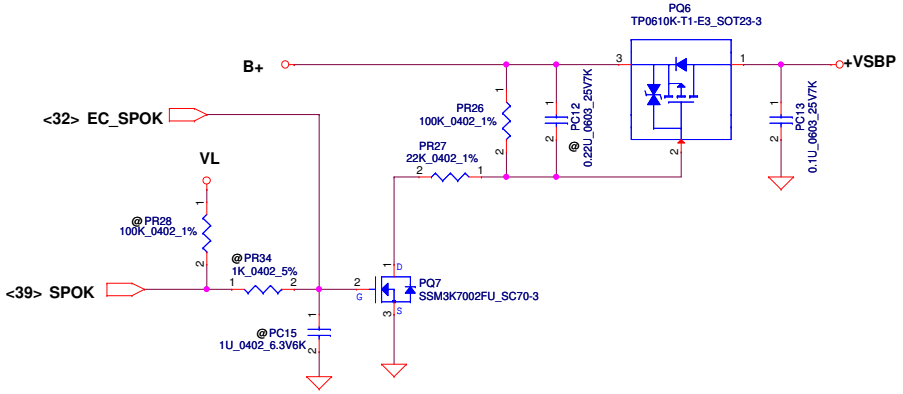
	G718	ENE9012
65W	3.92K	2.21K
90W	8.87K	6.98K
VCIN1	1.456V 1.148V	1.2V 0.925V

For 65W adapter==>action 70W , Recovery 54W

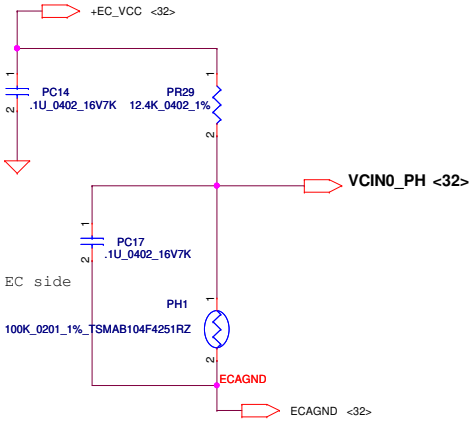
For 90W adapter==>action 97W , Recovery 75W

For 40W thunder bolt adapter==>action 50W , Recovery 38W
VCIN1=0.9V recover = 0.683V





PH1 under CPU botten side :
CPU thermal protection at 92 degree C for reference



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	*Chief River VC*	1.0

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for reverse input protection

PQ8 SI1304BDL-T1-E3_SC70-3
PR39 1M_0402_5%
PR40 3M_0402_5%

VIN
PQ9 SIS412DN-T1-GE3_POWERPAK8-5
P1
PQ10 SIS412DN-T1-GE3_POWERPAK8-5
P2
PC25 2200P_0402_50V7K
PR42 @ 0_0402_5%
PC16 0.1U_0402_25V6
PR45 4.12K_0603_1%
PR46 4.12K_0603_1%

PR41 0.02_1206_1%
B+
PJ21 JUMP_43X79
CHG_B+
PC21 10U_0805_25V6K
PC22 10U_0805_25V6K
PC23 0.1U_0402_25V6
PC24 2200P_0402_50V7K
<BOM STRUCTURE>

PQ11 SIS412DN-T1-GE3_POWERPAK8-5
PC27 0.01U_0402_50V7K
PR43 @ 0_0402_5%
BQ24725_BATDRV
PR44 4.12K_0603_1%

PC26 0.1U_0402_25V6
PC28 0.1U_0402_25V6
PD6 BAS40CW_SOT323-3
PC29 0.047U_0402_25V7K
PC30 0.1U_0603_25V7K
PC31 1U_0603_25V6K
PC33 1U_0603_25V6K
PR47 10_1206_1%
PR48 2.2_0603_5%
PD7 RB751V-40_SOD323-2
PR50 0_0402_5%
DH_CHG
DH_CHG-1
PQ12 SIS412DN-T1-GE3_POWERPAK8-5
PQ13 SIS412DN-T1-GE3_POWERPAK8-5
PL4 4.7UH_FDSD0630-H-4R7M-P3_5.5A_20%
PR52 0.01_1206_1%
BATT+
PR53 @ 4.7_1206_5%
PC40 @ 680P_0402_50V7K
CSOP1
CSON1
PC37 0.1U_0402_25V6
PC38 0.1U_0402_25V6
PC34 10U_0805_25V6K
PC35 10U_0805_25V6K
PC39 2200P_0402_50V7K
PC36 0.01U_0402_50V7K

PU4
BQ24725RGRR_VQFN20_3P5X3P5
PAD VCC PHASE HIDRV BTST REGN
ACN LODRV
ACP GND
CMSRC SRP
ACDRV SRN
ACOK BATDRV
ACDET IOUT SDA SCL ILIM
BQ24725_ACP
BQ24725_ACN
BQ24725_LX
DH_CHG
BQ24725_BST
DL_CHG
BQ24725_CMSRC
BQ24725_ACDRV
PR54 10_0603_5%
PR55 6.8_0603_5%
PC41 0.1U_0603_25V7K
+3VLP
PR56 100K_0402_1%
ACOK
<15,32,35,39> ACIN

Pre_CHG
+3VALW
PR58 316K_0402_1%
PR61 100K_0402_1%
PC42 0.01U_0402_25V7K
PD9 RB751V-40_SOD323-2
VIN
PR60 280K_0603_0.1%
PR63 154K_0603_0.1%
ACDET
PC43 0.1U_0402_16V7K
PR65 66.5K_0603_0.1%
PC44 100P_0402_50V8J
PR66 0_0402_5%
@PC45 0.1U_0402_16V7K
Close EC

EC_SMB_CK1 <32,37>
EC_SMB_DA1 <32,37>
ADP_I <32,37>

ACDET
PR59 2M_0402_1%
PR62 2M_0402_1%
PQ14 PDTC115EU_SOT323-3
<BOM Structure>
PR64 100K_0402_1%
<32> FSTCHG
<32,35,40,41> SUSP#
PQ15 SSM3K7002FU_SC70-3

battery 4.35/cell *4 =17.4, battery voltage -->
back to back --> Vin

Vin Dectector

	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

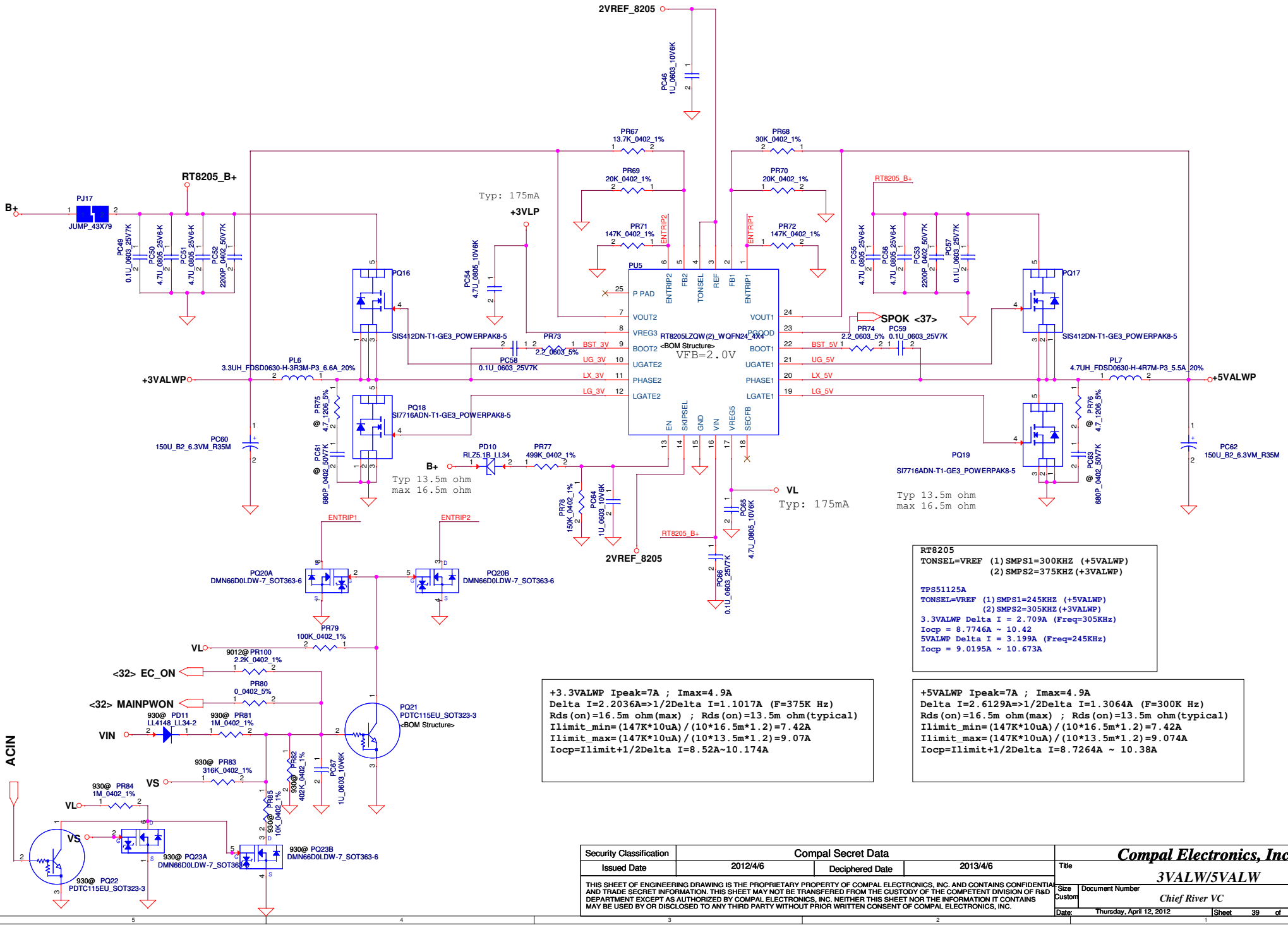
Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 38 of 51

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 2.709A (Freq=305KHz)
Iocp = 8.7746A ~ 10.42
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 9.0195A ~ 10.673A

+3.3VALWP Ipeak=7A ; Imax=4.9A
Delta I=2.2036A=>1/2Delta I=1.1017A (F=375K Hz)
Rds(on)=16.5m ohm(max) ; Rds(on)=13.5m ohm(typical)
Ilimit_min=(147K*10uA)/(10*16.5m*1.2)=7.42A
Ilimit_max=(147K*10uA)/(10*13.5m*1.2)=9.07A
Iocp=Ilimit+1/2Delta I=8.52A~10.174A

+5VALWP Ipeak=7A ; Imax=4.9A
Delta I=2.6129A=>1/2Delta I=1.3064A (F=300K Hz)
Rds(on)=16.5m ohm(max) ; Rds(on)=13.5m ohm(typical)
Ilimit_min=(147K*10uA)/(10*16.5m*1.2)=7.42A
Ilimit_max=(147K*10uA)/(10*13.5m*1.2)=9.074A
Iocp=Ilimit+1/2Delta I=8.7264A ~ 10.38A

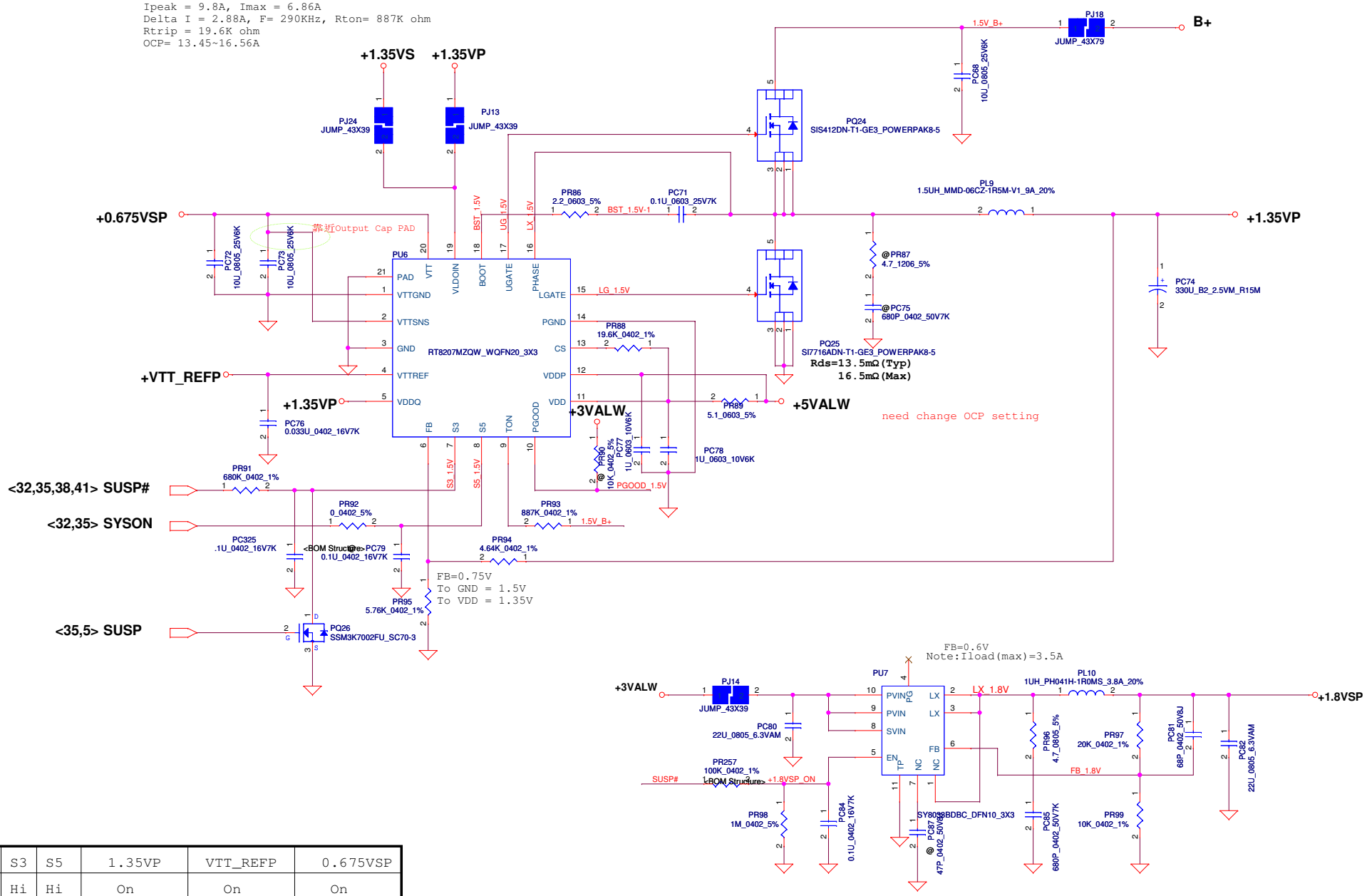
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom	Chief River VC	1.0

Date: Thursday, April 12, 2012 Sheet 39 of 51



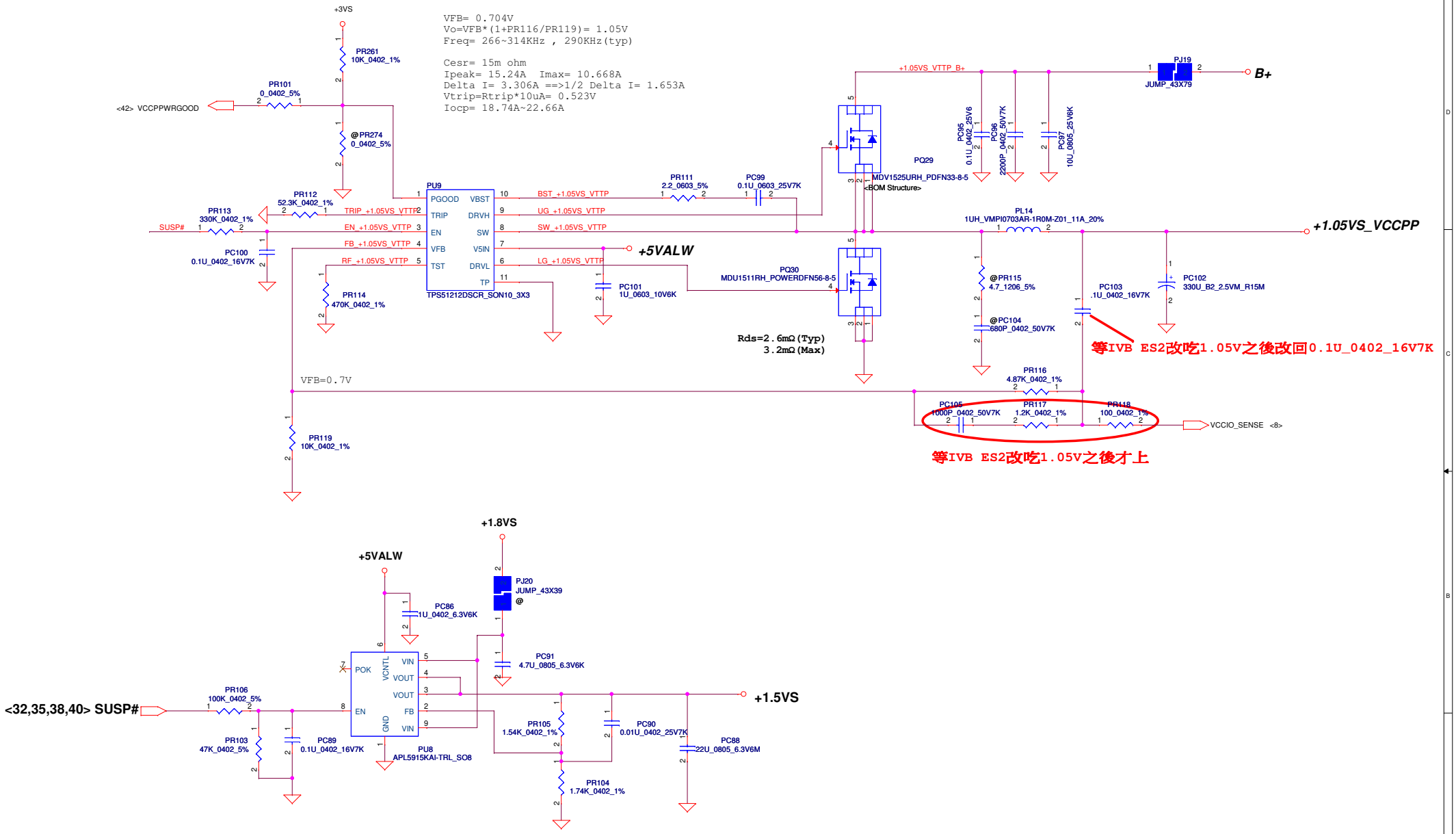
STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Title: 1.5VP/0.75VSP/1.8VSP

Size: Custom | Document Number: Chief River VC | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 40 of 51



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: +1.05VS_VTTP/+1.0VSP

Size	Document Number	Rev
Custom	*Chief River VC*	1.0

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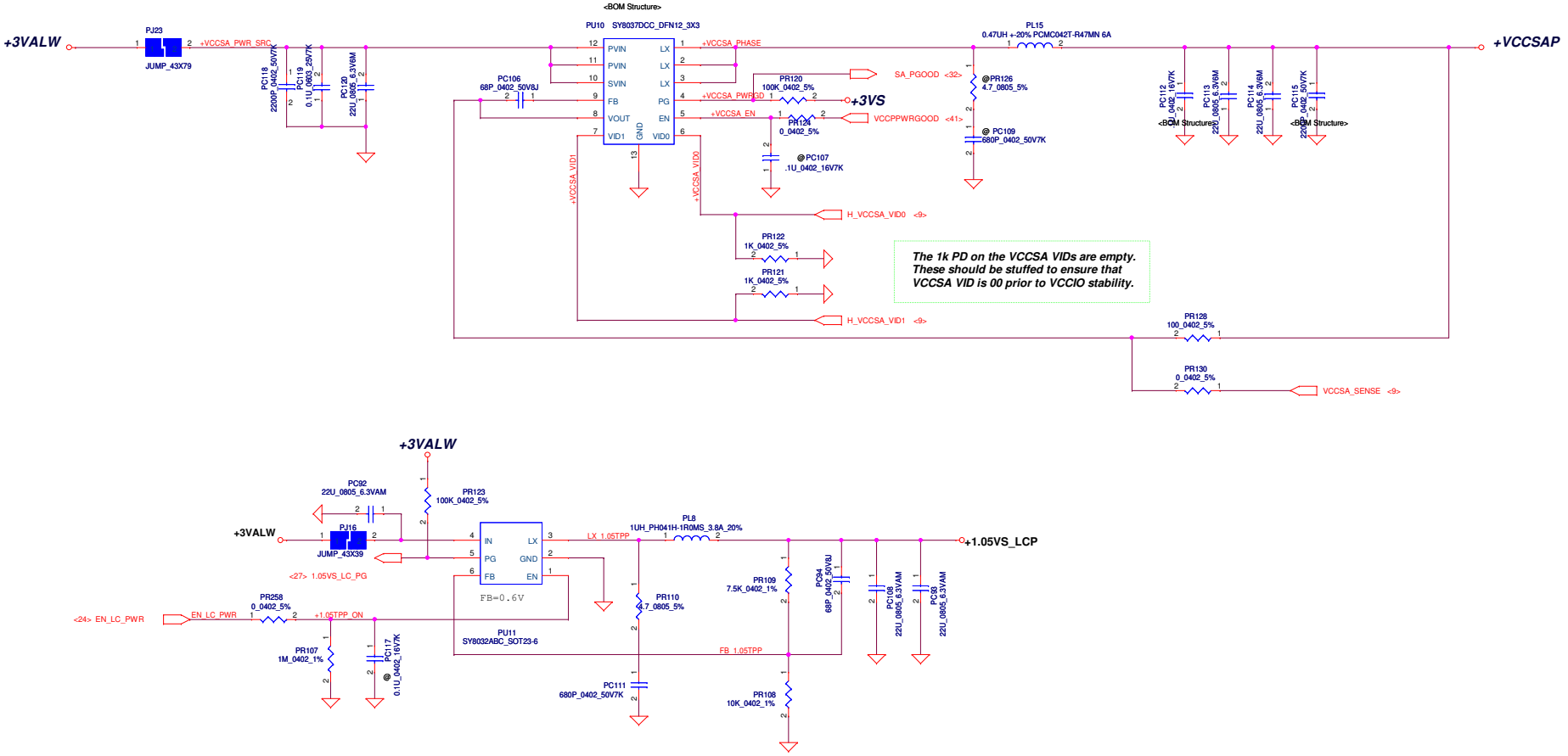
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



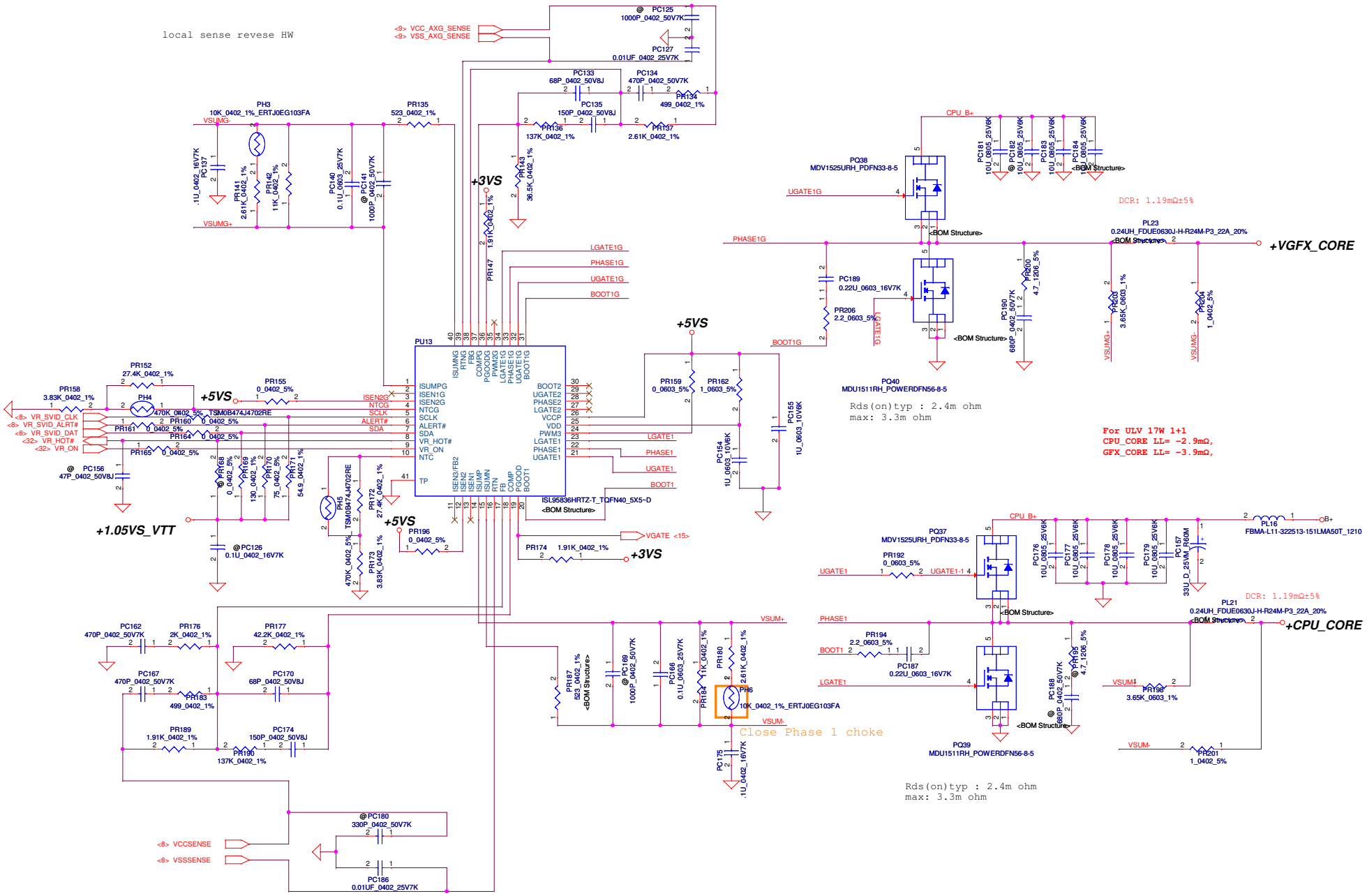
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: VCC_SAP/+1.5VSDGPUP/+1.05VS_DGPU

Size	Document Number	Rev
C	Chief River VC	1.0

Date: Thursday, April 12, 2012 Sheet 42 of 51



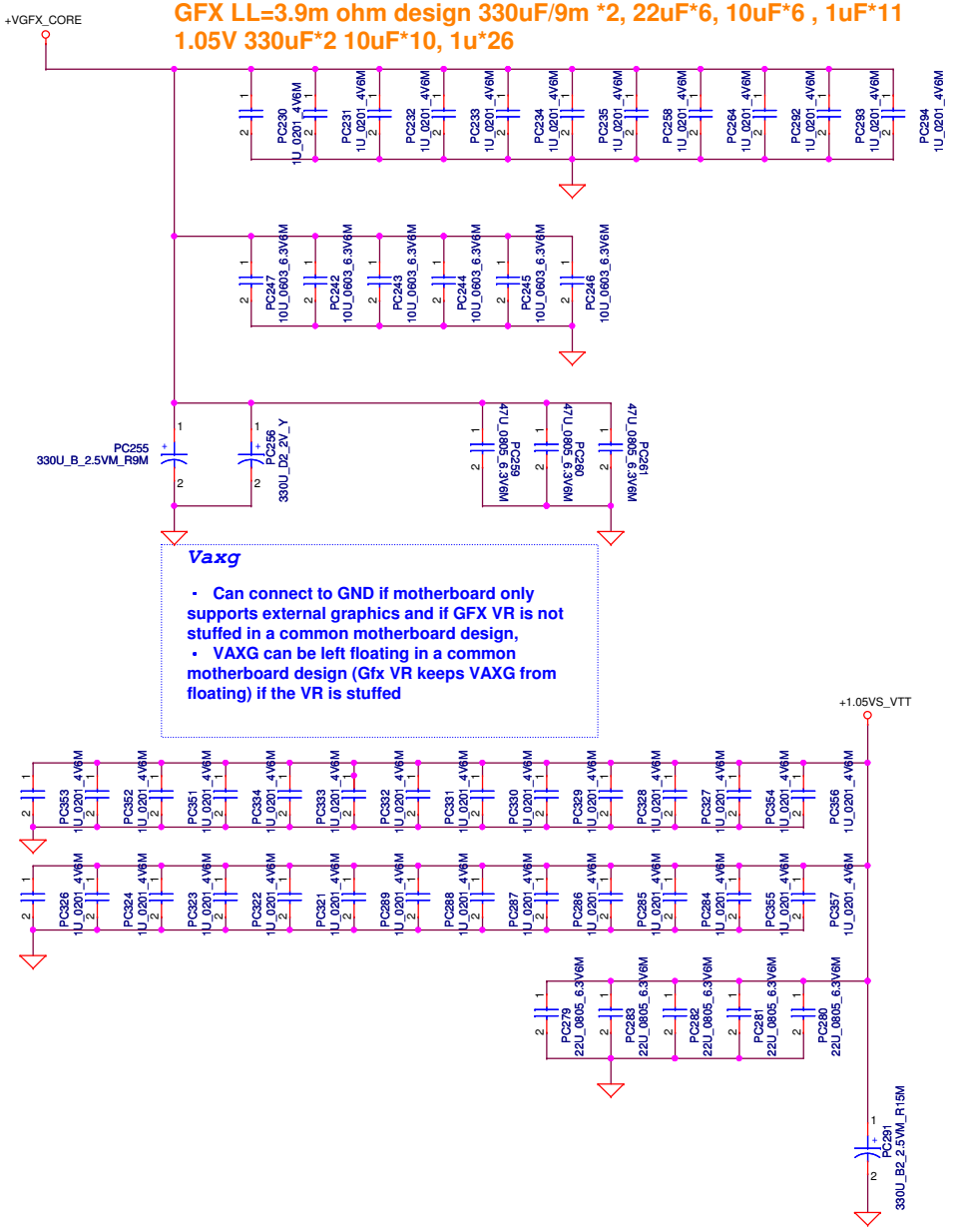
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: CPU_CORE

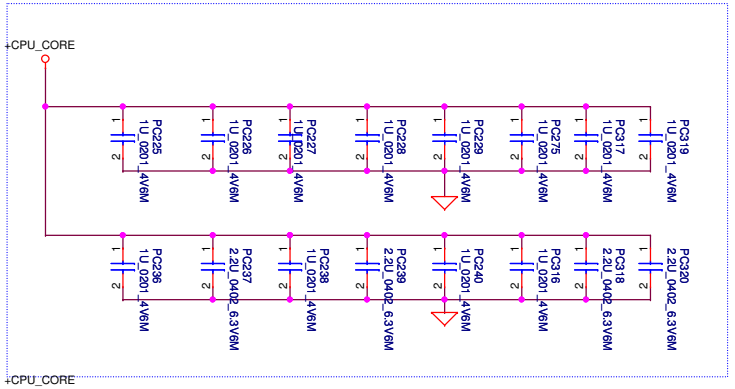
Size	Document Number	Rev
Custom	Chief River VC	1.0
Date: Thursday, April 12, 2012	Sheet 43 of 51	

PWR Rule
CPU LL=2.9m ohm dedign 330uF/9m *4, 22uF *12, 2.2uF*16
GFX LL=3.9m ohm design 330uF/9m *2, 22uF*6, 10uF*6 , 1uF*11
1.05V 330uF*2 10uF*10, 1u*26

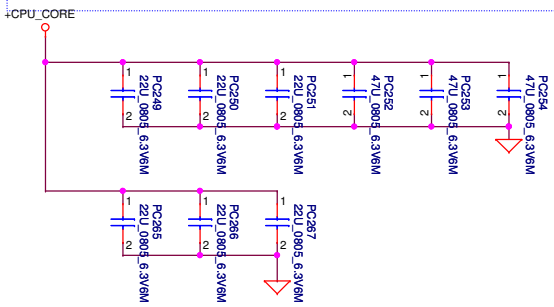


Vaxg

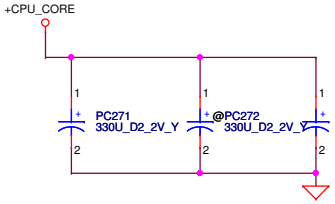
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



For BOT side



For TOP side

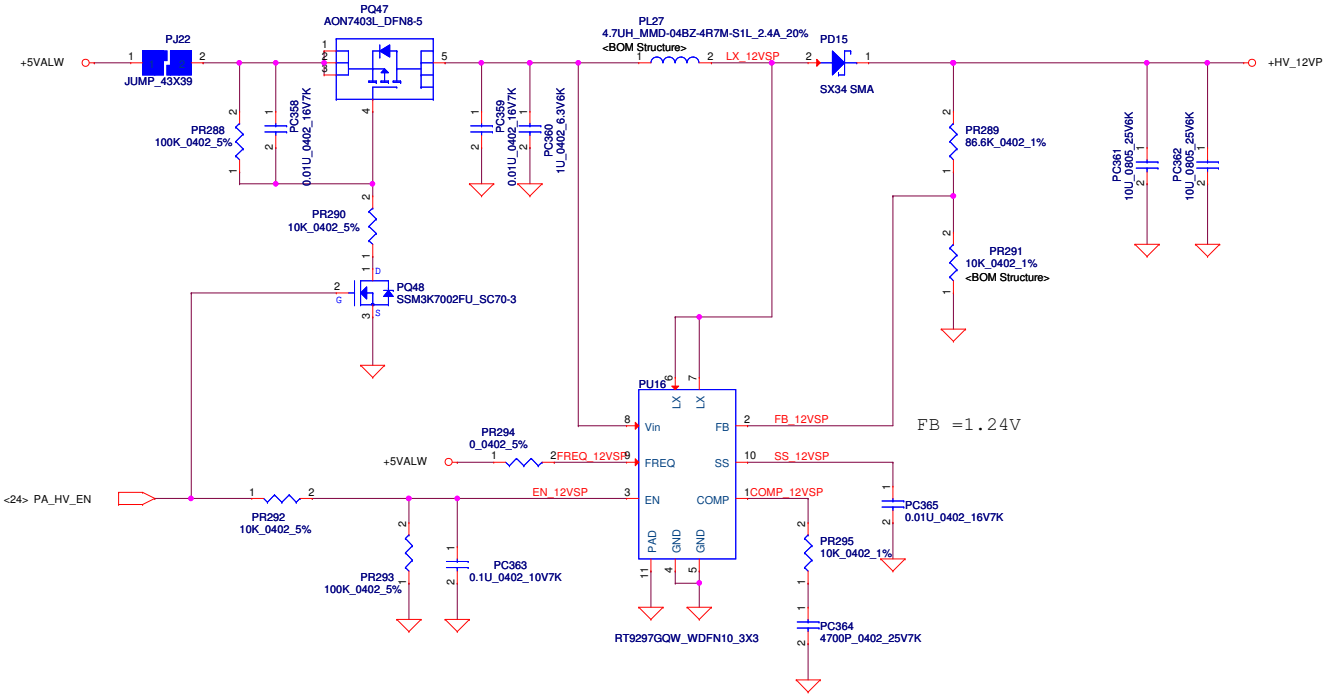


PC273 need link SGA00006J00.

INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0

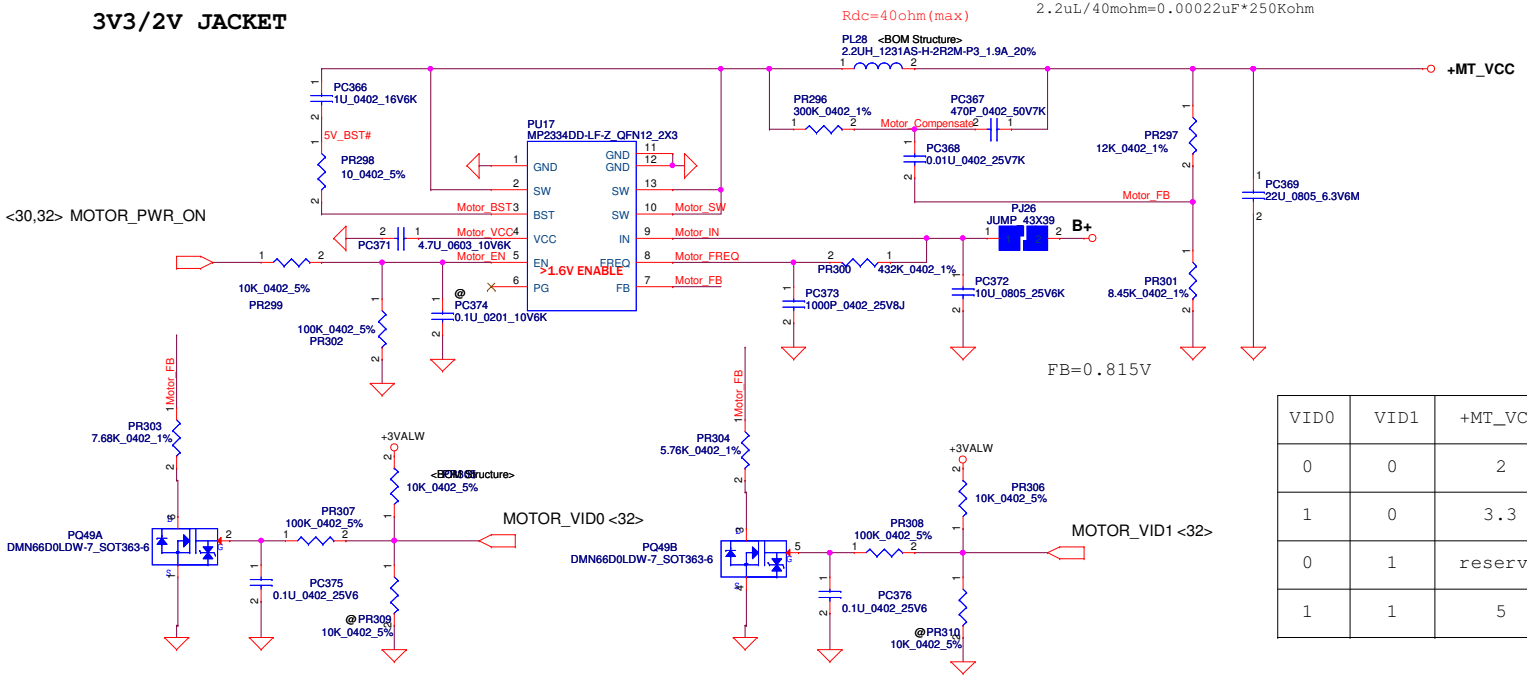
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.			
Title: CPU_CORE_CAP			
Size: Custom	Document Number: Chief River VC		Rev: 1.0
Date: Thursday, April 12, 2012	Sheet 44 of 51		



3V3/2V JACKET

L/RDC=C*R
2.2uL/40mohm=0.00022uF*250Kohm



VID0	VID1	+MT_VCC
0	0	2
1	0	3.3
0	1	reserve
1	1	5

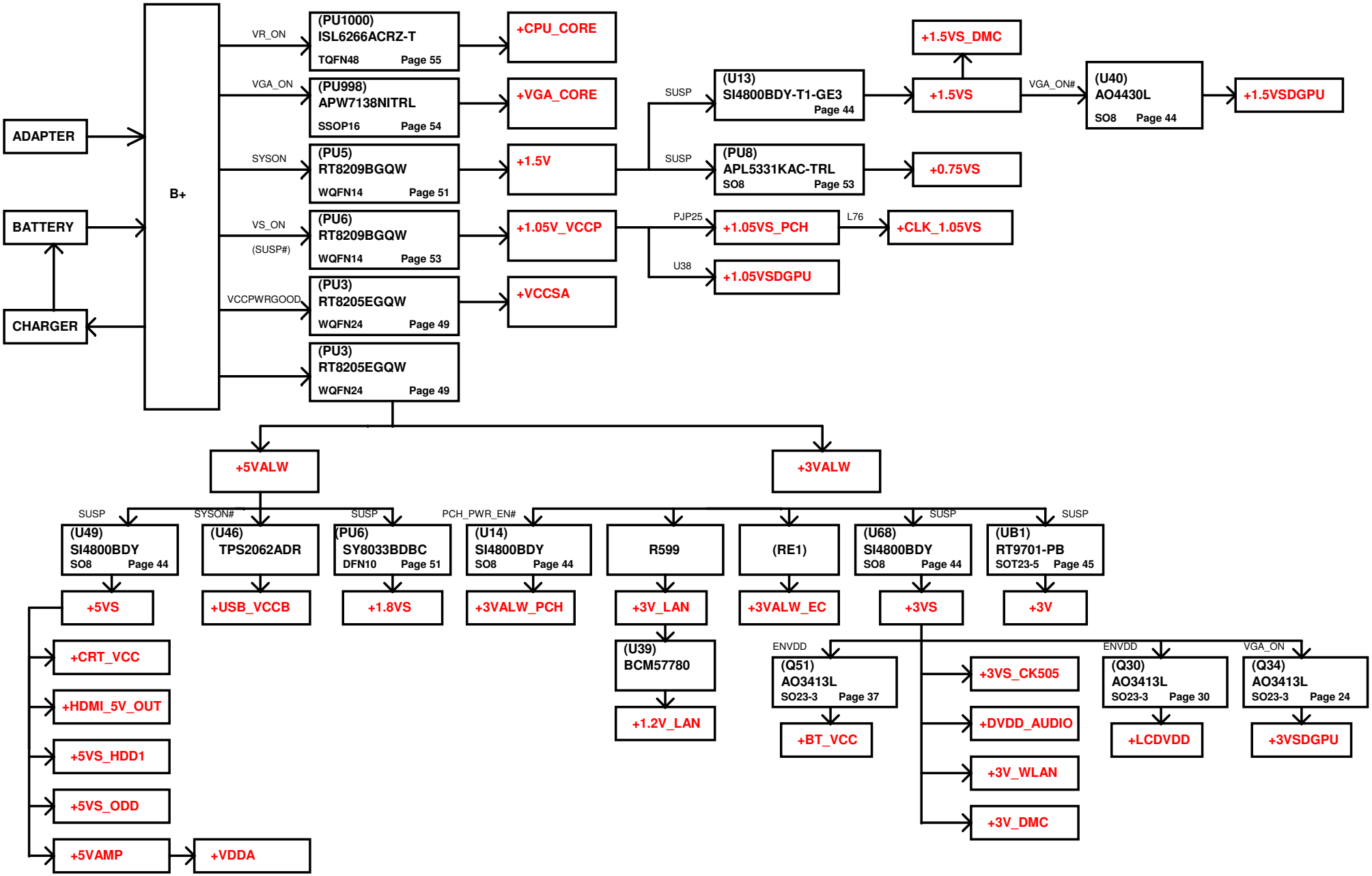
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: 12V & MOTOR Power

Size: B | Document Number | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 45 of 51



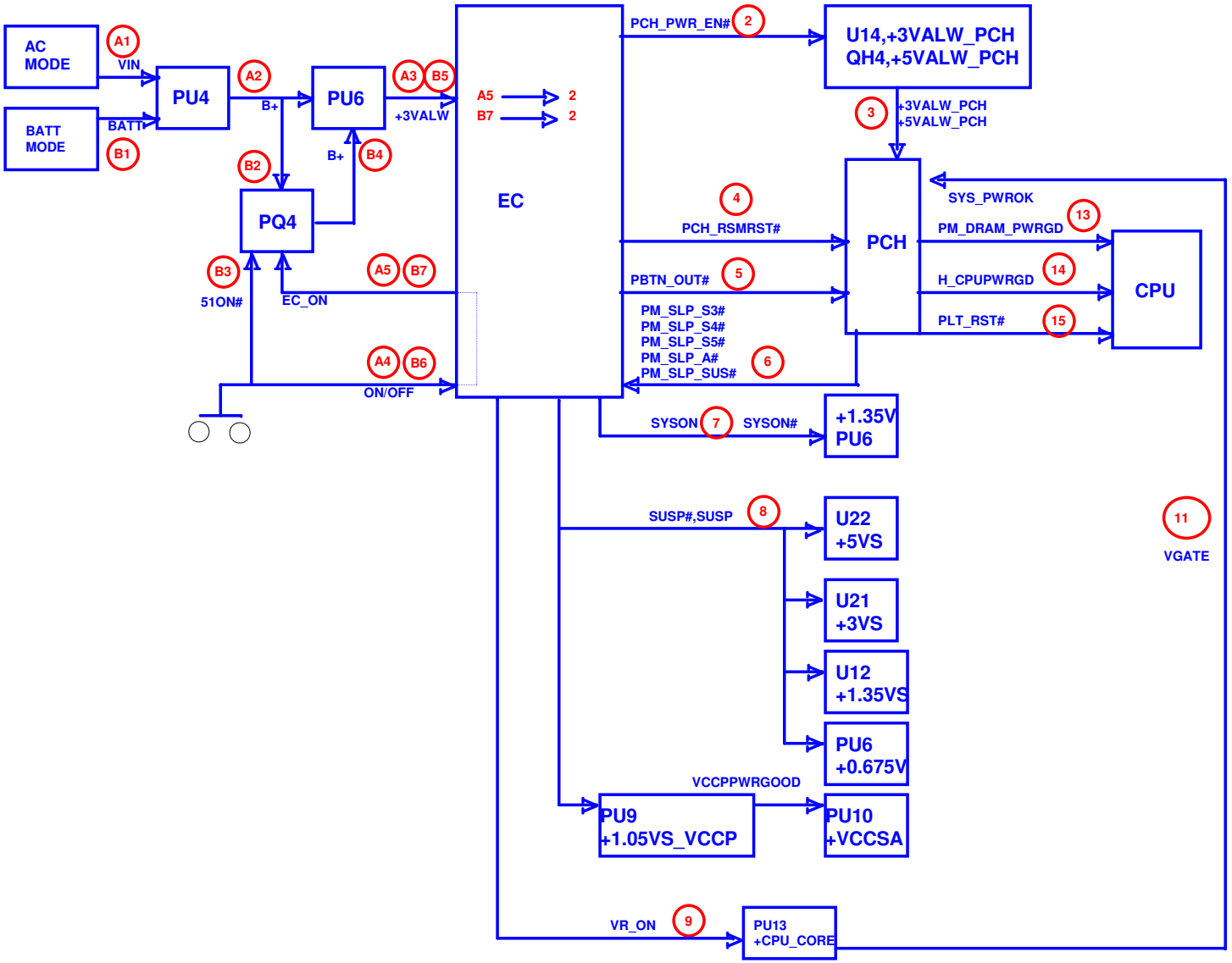
Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: Power Rail

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 46 of 51



Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

Date: Thursday, April 12, 2012 | Sheet 47 of 51

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Add ADP_ID circuit	Acer will add pull down resistor in adapter to detect ADP_ID.	0.1	36	Add PU1 SA003310280 (S IC LMV331IDCKRG4 SC70 5P COMPARATORS) Add PQ27 SB000009Q80(S TR 2N7002KW 1N SOT323-3) Add PR13 PR16 SD034100280(S RES 1/16W 10K +-1% 0402) Add PR14 SD034100380(S RES 1/16W 100K +-1% 0402)	2011/12/05	EVT2
2	Add Jack_TEMP and PH1 circuit	Acer request add a thermistor on jack of DC in cable to protect jack.	0.1	37	Add PU3 SA00003K300 (S IC G718TM1U SOT23 8P OTP) Add PR30 SD000009R00(S RES 1/16W 46.4K +-1% 0402) Add PR35 SD034953180(S RES 1/16W 9.53K +-1% 0402) Add PR37 SD034232280(S RES 1/16W 23.2K +-1% 0402) Del PR127 SD028000080(S RES 1/16W 0 +-5% 0402)	2011/12/05	EVT2
3	Adjust 1.35V ocp setting and add boost resistor	Adjust 1.35V ocp setting Add boost resistor	0.1	40	Change PR88 to SD000003580(S RES 1/16W 19.6K +-1% 0402) Change PR86 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	2011/12/05	EVT2
4	Add 1.05V boost resistor and adjust output voltage Change choke to 1uH	Add 1.05V boost resistor and adjust output voltage Change choke to 1uH for efficiency of heavy load	0.1	41	Change PR111 to SD013220B80(S RES 1/10W 2.2 +-5% 0603) Change PR116 to SD034487100(S RES 1/16W 4.87K +-1% 0402 (LF)) Change PL14 to SH00000KS00(S COIL 1UH +-20% VMPI0703AR-1R0M-Z01 11A)	2011/12/05	EVT2
5	Adjust GFX frequence	Adjust GFX frequence to 400kHz for reduce ripple	0.1	43	Change PR143 to SD034365280(S RES 1/16W 36.5K +-1% 0402)	2011/12/05	EVT2
6	Adjust CPU output cap	Adjust CPU output cap for transient	0.1	44	Change PC273 to SGA00006J00(S POLY C 560U 2V M D2 LESR4.5M SX H1.9) unpop PC272 SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2011/12/05	EVT2
7	Adjust 0.675V enable timing	Adjust 0.675V enable timing	0.1	40	Change PC325 to SE076104K80(S CER CAP .1U 16V K X7R 0402)	2011/12/05	EVT2
8	Adjust 1.05VS_LCP sequence	Change 1.05VS_LCP from APL5930 to SY8032 for thoundbolt sequence.	0.2	42	Change PU11 to SA000055100(S IC SY8032ABC SOT23 6P PWM) Change PR107 to SD034100480(S RES 1/16W 1M +-1% 0402) Add PL8 to SH00000MN00(S COIL 1UH +-20% PH041H-1R0MS 3.8A) Add PR110 to SD002470B80(S RES 1/8W 4.7 +-5% 0805) Change PC111 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Change PC92 to SE000008L80(S CER CAP 22U 6.3V M X6S 0805 H1.25)	2012/01/05	DVT
9					Add PR123 to SD028100380(S RES 1/16W 100K +-5% 0402) Change PR108 to SD034100280(S RES 1/16W 10K +-1% 0402) Change PR109 to SD034750180(S RES 1/16W 7.5K +-1% 0402) Change PC94 to SE071680J80(S CER CAP 68P 50V J NPO 0402)		
10	add boost resistor	add Charger boost resistor	0.2	38	Change PR48 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
11	add boost resistor	add 3V5V boost resistor	0.2	39	Change PR73 and PR74 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
12	add boost resistor	add CPU and GFX boost resistor	0.2	43	Change PR194 and PR206 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	2012/01/05	DVT
13	Change main source	Change main source for reduce component kind	0.2	39	Change PL7 to SH00000MB00(S COIL 4.7UH +-20% PDSD0630-H-4R7M=P3 5.5A (7*7*3))	2012/01/05	DVT
14	Adjust Jack_TEMP resistor	Adjust Jack_TEMP resistor, because PCCP change thermistor to 0603 size(TSM1A104F4361RZ)	0.2	37	change PR30 to SD034442280(S RES 1/16W 44.2K +-1% 0402) change PR37 to SD034215280(S RES 1/16W 21.5K +-1% 0402)	2012/01/05	DVT
15	Add ADP_ID circuit	Add ADP_ID circuit(65W)	0.2	36	Add PR23 to SD028000080(S RES 1/16W 0 +-5% 0402) change PR16 to SD034270280(S RES 1/16W 27K +-1% 0402) Add PC142 to SE074102K80(S CER CAP 1000P 50V K X7R 0402)	2012/01/05	DVT
16	Change main source	Change main source for 不完全替代 with HW	0.2		change PQ7,PQ26,PQ15,PQ27,PQ48 from SB000009Q80 to SB000009610(S TR SSM3K7002FU 1N SC70-3)	2012/01/31	DVT
17							

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Del ADP_ID circuit	Acer will change adapter type to 音叉式 from PoGo, so del ADP_ID circuit.	0.3	36	Del PU1 SA003310280 (S IC LMV331IDCKRG4 SC70 5P COMPARATORS) Del PQ27 SB000009Q80(S TR 2N7002KW 1N SOT323-3) Del PR13 SD034100280(S RES 1/16W 10K +-1% 0402) Del PR14 SD034100380(S RES 1/16W 100K +-1% 0402) Del PR23 to SD028000080(S RES 1/16W 0 +-5% 0402) Del PR16 to SD034270280(S RES 1/16W 27K +-1% 0402) Del PC142 to SE074102K80(S CER CAP 1000P 50V K X7R 0402)	2012/03/13	PVT
19					Del PU3 SA00003K300 (S IC G718TM1U SOT23 8P OTP) Del PR30 to SD034442280(S RES 1/16W 44.2K +-1% 0402)		
20	Del jack_temp circuit	Acer will change adapter type to 音叉式 from PoGo, so del jack_temp protect circuit.	0.3	37	Del PR35 SD034953180(S RES 1/16W 9.53K +-1% 0402) Del PR37 to SD034215280(S RES 1/16W 21.5K +-1% 0402) Add PC17 SE076104K80(S CER CAP .1U 16V K X7R 0402) Change PR29 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402)	2012/03/13	PVT
21	SPOK change to EC_SPOK	For reduce power consumption of DS3, so close +VSB power in DS3, DS4, DS5.	0.3	37	Del PR28 SD034100380(S RES 1/16W 100K +-1% 0402) Del PR34 SD028100180(S RES 1/16W 1K +-5% 0402) Del PC15 SE000000K80(S CER CAP 1U 6.3V K X5R 0402)	2012/03/13	PVT
22	change VCCSA IC version	SY8037C IC version change to SY8037D for accord with intel VCCSA spec.	0.3	42	Change PU10 to SA00005O000(S IC SY8037DDCC DFN 12P PWM)	2012/03/13	PVT
23	Add snubber	Add snubber of GFX by hw request.	0.3	43	Add PR200 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC190 SE074681K80(S CER CAP 680P 50V K X7R 0402)	2012/03/13	PVT
24	Add MOTOR POWER	HW change motor power solution to PWM.	0.3	45	Add PU17 SA00005NY00(S IC MP2334DD-LF-Z QFN 12P PWM) Add PL28 SH00000N000(S COIL 2.2UH +-20% 1231AS-H-2R2M=P3 1.9A) Add PC366 SE00000U00(S CER CAP 1U 16V K X5R 0402) Add PC367 SE074471K80(S CER CAP 470P 50V K X7R 0402) Add PC368 SE075103K80(S CER CAP .01U 25V K X7R 0402) Add PC369, PC371 SE00000MA00(S CER CAP 4.7U 10V K X5R 0603) Add PC372 SE00000QK00(S CER CAP 10U 25V K X5R 0805 H1.25)	2012/03/13	PVT
25					Add PC373 SE068102J80(S CER CAP 1000P 25V J NPO 0402) Add PC375, PC376 SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PR296 SD034300380(S RES 1/16W 300K +-1% 0402) Add PR297 SD034120280(S RES 1/16W 12K +-1% 0402)		
26					Add PR298 SD028100A00(S RES 1/16W 10 +-5% 0402) Add PR300 SD034432380(S RES 1/16W 432K +-1% 0402) Add PR301 SD000000680(S RES 1/16W 8.45K +-1% 0402) Add PR302, PR307, PR308 SD028100380(S RES 1/16W 100K +-5% 0402) Add PR303 SD000002300(S RES 1/16W 7.68K +-1% 0402)		
27					Add PR304 SD034576180(S RES 1/16W 5.76K +-1% 0402) Add PR299, PR305, PR306 SD028100280(S RES 1/16W 10K +-5% 0402) Add PQ49 SB00000DH00(S TR DMN66D0LDW-7 2N SOT363-6)		
28	Adjust HW throttling point	Because thunder bolt adapter is 40W, OCP 130% adjust HW throttling to 125% 50W recover point 38W	0.3	37	Change PR33 to SD034165180(S RES 1/16W 1.65K +-1% 0402)	2012/03/13	PVT
29							
30							
31							
32							
33							
34							

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

0919(In Layout)
1.Update R,C 0201,0402,0603,0805,1206 PCB footprint to small size
2.Swap DDR Data BUS

0920
1.Change U74,U21,U22 mos to 3*3 thermal pad package:SB00000GW00

0921
1.TB chip:U66 footprint add "-NH" for Non HDI
2.1.8p_0402:C402,C404 change to 75ohm_0402:R263,R264

0922
1.Change C1457,C1505 form 1.8P 0402 to 0201:SE00000HB80
2.Del DDR CHA,B no use CLK1,CLK1# circuit
3.Change C606,C607 from D2 330uF to B2 330uF 2.5V ESR 15mohm:SGA00004400
4.Swap total KB connector:JKB1 pin define

0923
1.Add DS3 function:SUSWARN#,SUSACK#,EC_DRAMRST_GATE
2.Add Motor function:Motor_IN1,Motor_IN2,Motor_IN3,Motor_IN4,
Door_Det_L,Button: KSI0 & KSO10
3.Remove PCH NCTF test point
4.HDMI Fuse:F1 change to P5WS5 use footprint:F_1812
5.Remove HDMI common mode choke:L36,L38,L39,L40
6.Change 0.1uF_0402_16V7K to 0.1uF_0201_10V6K:SE00000SV00
=>C521,C520,C526,C449,C523,C537,C541,C494,C495,C490,C497,C771,C522,C471,C473
7.Change 0.01uF_0402_16V7K to 0.01uF_0201_10V7K:SE172103K80
=>C425,C462
8.Change C751,C752 to B2 220uF 2.5V ESR 15mohm:SGA00004500

0924
1.Make MB to Audio/B connector pin define
2.Change RP 8.2K:R256,R262,R276,R386 to 8.2K_0402
3.Change RP 10K:R386 to 10K_0402
4.Update TB schematic p.24,25,27
5.Change Q64,Q68 from AO3419L:SB000006R10 to AP2301GN-HF:SB000007H10
6.Integration of all 2N7002 SOT23 parts to SSM3K7002F_SC59-3:SB000009080
=>Q74,Q20,Q1,Q2,Q32,Q16,Q17,Q14,Q37,Q7,Q21,Q23,Q24,Q5,Q34,Q29,Q60,Q66,Q67,Q72
Not yet=>Q6,Q78,Q79

0925
1.Delete LVDS function,Combine eDP,Card Reader function to JLVDS1
Remove:R259,R260,R285,R286,R156,R157,TXCLK+-,TX0+1,TX1+-,TX2+-,DDC CLK,DATA
Remove:C462,C425,C412,L20,only place PU:R271,R272,PD:R270,R280
2.Change all SSM3K7002F_SC59-3:SB000009080 to SSM37K002FU_SC70-3:SB000009610
=>Q74,Q20,Q1,Q2,Q32,Q16,Q17,Q14,Q37,Q7,Q21,Q23,Q24,Q5,Q34,Q29,Q60,Q66,Q67,Q72
Not yet=>Q6,Q78,Q79
3.Change 10U_0805_6.3V6M:SE093106M80 to 10U_0603_6.3V6M:SE000005T80
=>C754,C543,C418,C465
4.Remove 0_0603_5%:R416,R421,R426,R327

0926
1.Change HDMI level shift Q16,Q17 to DMN66D0LDW-7_SOT363-6:SB00000DH00
2.Modify TB schematic 0402 cap to 0201

0927
1.Remove J7
2.Change C599 330U D2 2V ESR 9mohm to 330U B2 2.5V ESR 15mohm:SGA00004400
3.Change EC +3VALW_EC
0.1U_0402_16V4Z to 0.1U_0201_10V6K:SE00000SV00
=>C1198,C1199,C1200,C1201,C1204
1000P_0402_50V7K to 1000P_0201_16V7K:SE000007U80
=>C1202,C1203
4.Remove R329
5.Change C751,C752 to 22U_0805_6.3V6M:SE000000I10
6.Remove J4(one of +1.05VS_VTT to +1.05VS_PCH jumper)

0928
1.Change RTC cap from 1U 0603 to 1U 0402:C502,C516
2.Remove FAN some parts:R753,C788,D51,D52
3.Change USB connector foot print to TAIWI_USB005-107CRL-TW_10P-T
4.Change C196,C387,C735,C102 to 0.1uF_0201_10V6K:SE00000SV00
5.Remove L2

0929
1.Remove C510,C511
2.Remove Camera Choke:L7,R13,R14
3.Q1,Q2 change to DMN66D0LDW-7_SOT363-6:SB00000DH00
4.R273,R394 change from 0_0603 to 0_0402
5.Remove Step Motor SW1
6.Change LED/B connector from 8 pin to 4 pin
7.Change Jumper from 43*118 to 43*79
=>J2,J8,J10,J11

0930
1.Remove +VCCSA cap:C1182,C1183
2.Remove +USB3_VCCA cap:C390
3.Change C427,C428 to 0.1U_0201_10V6K
4.Add ESD diode:D6 for TP SMBUS
5.Change L65 to 220ohm 3A 0805
6.Swap DDR ChB Data,DQS# 6,7
7.Change U12 mos to 3*3 thermal pad package:SB00000GW00
8.Remove X2,C1361,C1362
9.C378+C375 change to 10uF*1
10.C460+C459 change to 10uF*1
11.Remove C986,C987,C989,C990
=>Add 1uF 0201*10

1003
1.Change EC side GPIO:PWR_LED to PWR_LED#,Remove Q32,R512
2.For separate coaxial and wire,update eDP MB connector pin define
3.Remove JLED1 connector
4.Change C427:0.1U_0402_16V4Z to 0.1U_0201_10V6K:SE00000VS00

1005
1.Swap DDR ChB Data,DQS# 6,7
2.Change PCH PCIE 0.1U_0402_16V7K to 0.1U_0201_10V6K:SE00000SV00
=>C572,C573,C617,C618,C681,C682,C683,C684,C685,C686,C687,C688
2.Change eDP cap from 0.1U_0402_16V7K to 0.1U_0201_10V6K:SE00000SV00
=>C910,C911,C912,C913,C914,C915
3.Add R80:0ohm of H_CPU_PWRGD for ESD request
4.Remove On Board WLAN:MD225
5.Add Motor parts(Not Ready)
6.Add iSSD i100 parts(Not Ready)

1006
1.Change R754,R751 0ohm from 0603 to 0402
2.Change C484 0.1U from 0603 to 0402
3.For DS3,Change power source from +3VALW_PCH to +VCCSUS3_3
4.Change R629 from 0_0805 to 0_0402
5.Change SATA cap from 0.1U_0402_16V7K to 0.01U_0201_10V7K
=>C621~C628

1010
1.Add BATT_RST#,VR_LEFT,VR_RIGHT pin
2.Add iSSD i100 128GB*2 schematic
3.Add USB_HPD# pin

1011
1.Add Battery Reset function
2.Swap USB2.0,3.0 choke for connector side 順線

1013
1.Add Step Motor circuit
2.On Board iSSD:i100 change to mSATA SSD
3.WLAN change to on board:MD225
4.Change Card Reader
PCIE from Port4 to Port1
CLK from Port5 to Port4
5.Change mSATA SATA port from Port1 to Port0
6.Add USB port 12 for mSATA
7.Remove D11,D12 and C357,C358 (HDMI RF request)
8.C396,C324 change to 0201
9.Remove C472 for +5VALW source cap

1014
1.Remove DPST_PWM buffer:U13,R783,R85
2.Change +3VS_FULL cap:C475,C466 from 0.1uF_0402 to 0201
3.Change SATA cap:C621,C622,C623,C624 from 0.01uF_0402 to 0201

1017
1.Add power source of +VCCAFDI_VRM at P.20
2.Update DS3,AOAC control signal connected to EC

1018~1021

1024
1.Remove R130
2.Define DRAM ID
3.Update TB schematic
4.Swap USB2.0 ESD pin
5.Add on/off BTN for debug

1027
1.Swap JTP1 pin for new module
2.Gerber schematic

1028
For Load BOM
1.Update Block Diagram
2.Update CPU,PCH part number
3.Update BOM config

1101
1.For整合料
2.Combine PWR schematic
3.A test SMT schematic

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: EE P.I.R

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

1201(EVT2 Gerber)
1.Modify EVT1 SMT memo into Schematic
2.Add 1U_0201_4V_6M *4(C1511,C1512,C1513,C1514) for ChA
3.Add 1U_0201_4V_6M *4(C1515,C1516,C1517,C1518) for ChB
4.Delete ChA,ChB SPD ROM(U70,U72) circuit
5.JLVDS.15 change from VR_LEFT to GND
6.TB,pull high PCH_DPD_CLK,PCH_DPD_DAT to +3VS(R252,R254)
7.TB,add Buffer:U3 EN pin pull down resistor:R1075
8.TB,Change R1067 pull down form PA_LSRX_LSOE1_R to PA_LSRX_LSOE1_U
9.WLAN,Modify PCIE TX,RX,change P/N of RX signal
10.WL_OFF# connected to EC_Pin71
   BT_ON# connected to EC_Pin117
11.mSATA,+3VS_FULL:Change C455 to 4.7U_0603_6.3V_6K,+1.5VS:Delete C433
12.Update Motor circuit,P.30
13.Add TPM/TCM co-layout circuit,P.30
14.USB PWR SW IC enable pin co-lay SYSON# and USB_EN#_R(EC_Pin81)
15.EC,P.32
(1)power source co-lay +3VALW/+3VLP
(2)DC mode S4/S5 turn on +3VALW,+5VALW for Motor, MOTOR_BTN(EC_Pin17)
(3)PPS_L connected to MOTOR_PPS_L(EC_Pin85)
(4)PPS_R connected to MOTOR_PPS_R(EC_Pin91)
(5)Turn on/off Motor +5VALW connected to MOTOR_PWR_ON(EC_Pin21)
(6)Audio/B add Motor LED connected to MOTOR_LED#(EC_Pin36)
(7)BI_DET changed to EC_Pin25
(8)Adapter ID pin connected to ADP_ID(EC_Pin64)
16.Update JAUDIO connector type and pin define,P.33
17.Add Motor BTN circuit,P.33
1207
1.PCH_ACIN pull high R341 Change from 200K to 10K

0108(DVT)
1.For DS3,change P.18 PCH power source from +3VALW_PCH to +VCCSUS3_3
(R422,R657,R391,R397,R458)
2.Change TB_CLKREQ#_R power source from +3VS_POC to +3VS_LC (Q67,R1031)
3.Change Q67 direction
4.Change TB_SMB_DA,TB_SMB_CLK from PH +3VS_LC(R1036,R1037) to PL(R1046,R1047)
5.Change Q71 +3VS_LC enable pin from EN_LC_PWR to 1.05VS_LC_PG
6.Change R1110 from 348K_0402_1% to 35.7K_0402_1%
7.Change TB_GO2SX from PL to PH +3VS_POC(R1066)
8.Add TCM (U8) package into board file
9.For EC_PME#,R490 change to pop
10.For Motor BTN,R974 change to pop
11.Add MSATA RAID0 function (C625,C627,C626,C628)
12.Add PCH:GPIO35 to RAID0_DET,external pull down(R329)
13.Change TP from 6 pin to 8 pin,Add level shift Q9
14.Combine Q66,Q67 to Q89 dual package
15.For DS3,Add EC.82 ACPRESENT to PCH_ACIN(pop R456,unpop D19)
16.For eDP only,PCH_GPIO71 change from PL to NC(unpop R618)
17.For Motor VR,change from PH to PL 100K(R454,R455)
0113
1.Remove mSATA USB port12
2.For ESD request,Reserve 0.1uf for FAN_SPEED1,FAN_PWM (C451,C450)
0117 (Final Schematic for Gerber)
1.Add Q30,Q31 for "LED" TB cable
2.Add MD222 BT_LED test point:T74
3.Add test point T75,T76,T77,T78,T79,T80 for TB boundary scan
0120
1.Unpop Power BTN(SW1)
2.For change BID from 0 to 1,pop R957:8.2K
3.For DS3,S3,Change R418 BOM config from S3@ to normal
0131
1.For 缺料,Change C394,C1000 from SGA00001E00 to SGA00002N80
2.For 統一料,Change C599,C607 main source:SGA00004700,2nd source:SGA00004400
3.For 統一料,Change C1484,C1464 main source from SGA20331E10 to SGA19331D10
4.For Vendor Report,
 Change Y1,Y2 from SJ10000DJ00:25MHZ 20PF +-30PPM 7V25000016 to
 SJ10000E800:25MHZ 10PF +-20PPM 7V25000014
 Change C744,C745 form 27pf to 10pf
 Change C1338,C1340 from 20pf to 6.8pf
5.For cost,C496,C478 change to unpop
6.For cost,Change C505 from 1uF 0201 to 0.1uF 0201
7.For cost,Change C993,C992,C1009,C994,C1006,C1008,C1007,C1010,C986,C1002
  from 1uF 0201 to 0.1uF 0201
8.For ESD request,pop 1000pf for FAN_SPEED1,FAN_PWM (C451,C450)
  and Unpop C579 1000p of FAN_SPEED1
9.For IOAC power control by EC,pop Q47

0303 (PVT)
Modify DVT SMT memo for BOM
1.C744,C745 change from 10P 25V J NPO 0402:SE00000F180
   to 10P 50V J NPO 0402:SE071100J80
2.For INTEL TB review,pop R1036,R1037,R1048,unpop R1046,R1047,R1066
3.TB,C1424,C1425 change from SE000000K80:1U_0402_6.3V6K
   to SE076104K80:.1U_0402_16V7K
4.For USB enable pin change from SYSON#:R952 to USB_EN#:R951
Modify PVT layout
0.Remove on/off# BTN SW1 footprint
1.Change BT port from Port13 to Port8
2.Remove TCM parts:U8,R964,R965,C12,C1225
3.Remove EC 930 SPI ROM:U38,R694,R690,R698,R705,R692,C722,R695,C727
4.Remove SUS_PWR_DN_ACK for S3:EC U53.19,R409,R411
5.Update JLVDS1 pin define for +3VALW short issue
6.Add JLED1 connector
7.Remove JMT1,JMT2,JRTC1 and Change to JMR1 8pin conn.
8.Add EC U53.19:IRST_RST# (R461) to U26.1 for IOAC+IRST issue
9.Change 0ohm to 0ohm_short:R80,R314,R320,R372,R382,R394,R412,R421,
  R577,R578,R579,R581,R582,R612,R629,R661,R785,R940,R947,R953,R956,
  R959,R967,R973,R974
10.For WLAN漏電issue,Change PCH_PCIE_WAKE#_R(EC_PME#) pull high
   from +3VALW to +3VS_WLAN.Add R962,Remove R943
11.Change Motor Power source from PMOS to NMOS
   Remove:R452,R453,Q69,C818,R754,J14
   Add:U23,Q90,R459,C472,C503,C504,C481,R460
12.Remove net :ADP_ID
13.For TB ref. design,Add dual PMOS Q91,Q92,NMOS Q32,R1124
0306
14.Add DPWROK PL:R463 for INTEL suggestion
15.Remove JP1 EC debug port
16.Remove MDP_HPD ESD:D45
17.Add H11:H_4P0N for eDP connector
18.Add EC_SPOK(U53.120) to control +VSBP
19.add BT_LED U53.119 control pin,R492
20.add TB_FORCE_PWR:R1097 to PCH_GPIO12
21.Add WLAN discharge circuit:Q62B,R473=>Remove
22.For ACER TB request,add PH R1125 to +3VS_POC
0308
23.Remove ME RST# 0ohm:R561
24.Add C785,C786,C787,C788,C789 for ESD request
25.Add Q69 group(Q69,Q62B,R452,R453,R754,C818,R474,C540) for +3V_MCU
26.Change +3VS_FULL:J8 from 43*79 to 43*39
0309
27.Change Q62 dual 2N7002 to normal 2N7002
28.Add IRST_RST# PH:R965 to +3VALW_EC
29.Motor +3V_MCU design:
   Delete PMOS:Q69 group(Q69,Q62B,R452,R453,R754,C818,R474,C540)
   Add NMOS:Q87 group(Q87,Q93,R21,R789,C811)

0312 Modify for PVT SMT
1.For EC_SMI#,R939 change to @
2.For PCH_ACIN,R341 change to @
3.For ACER only,TPM change from SA00005EG00 to SA00005PH00
4.Change SPOK control function from PWR to EC_SPOK
5.Change HDMI cap form SE076103K80:0.01u to SE076104K80:0.1u:C280~C287
6.Change Board ID form 1 to 2,R960 chnage to 18K_0402_5%
7.For Vgs(th) issue,change Q20 from 2N7002 to BSS138(SB000002X00)
8.For Q5LJ1 RTC issue,
 change X1 from SJ10000DM00:S CRYSTAL 32.768KHZ 12.5PF 9H03200019 to
               SJ100004Z00:S CRYSTAL 32.768K 12.5PF 1TJF125DP1A000D
9.Remove KB cap 100P_0201*24pcs
  C245,C246,C247,C248,C249,C250,C251,C252,C253,C254,C255,C256,C258,C259,
  C260,C263,C265,C266,C267,C268,C269,C270,C271,C272
10.For ME PE review,remove C442
11.For cost,Change DDR C1464 to @
12.For cost,Change DDR C1258,C1259,C1261,C1291,C1292,C1293 to @
13.For cost,Change DDR cap from 1uF_0201 to 0.1uF_0201
   C1462,C1461,C1460,C1459,C1514,C1513,C1512,C1511,
   C1466,C1476,C1477,C1467,C1470,C1471,C1478,C1468
   C1504,C1503,C1502,C1501, C1518,C1517,C1516,C1515,
   C1487,C1497,C1498,C1488,C1491,C1492,C1499,C1489
14.For cost,Change TB C1406,C1407,C1443,C1444 from 1uF_0201 to 0.1uF_0201
0314
15.For HF parts,change Q6 from SB501380020 to SB501380050
16.For HF parts,change Q87 from SB534560020 to SB534560030
0315
17.Combine Power latest schematic

0402 Modify for 1.0 layout
1.Add soft start R756,C819 of Q68:+VCCSUS3_3 and R757,C820 of Q64:+V5REF_SUS
2.Add TB GPIO7(R1129) to PCH GPIO49,GPIO6(R1128) to PCH GPIO20
3.Add TB wake# colay:R1098 to U53.64(EC GPIO49),PH R976 to +3VALW_EC
4.Add TB +3VS_POC jumper colay +3VS(J4) and +3VALW(J2)
5.Delete colay J13(+3VALW to +VCCSUS3_3),R751(+5VALW to +V5REF_SUS)
6.Add C1519:10U_0603 for +0.675VS
7.Change C1468,C1471,C1476,C1477,C1478,C1491,C1492,C1499 from
  0.1U_0201_10V6K to 1U_0402_6.3V6K
8.Add R277,R1109 for MOS Vgs(th) reserve.
9.Change Motor BTN SW:R974 from 0ohm_short to normal 0ohm
10.Add C790,C791 of VGATE for ESD team
11.Reduce Jumper size from 43*118 to 43*79:PJ17,PJ7,J3
    Change Jumper size from 43*118(PJ1) to 43*79(PJ1)+43*39(PJ8)
    Change Jumper size from 43*118(PJ2) to 43*79(PJ2)+43*39(PJ10)

0411 Modify for PreMP SMT
update PVT SMT memo
1.Add C787:100P_0201_25V8J for PM_DRAM_PWRGD
2.Add C785:100P_0201_25V8J and C786:100P_0402_50V8J for DIMM_DRAMRST#
3.Add C788:100P_0402_50V8J for SM_DRAMRST#
4.Add C789:100P_0402_50V8J for SYS_PWROK
5.For TB GPIO6,GPIO7,change PH to PL,unpop R1036,R1037,pop R1046,R1047
6.Delete Q65 for TB GPIO6,GPIO7
7.Add TB_FORCE_PWR_R to PCH,pop R1097,unpop PH:R657 at PCH side
8.For TB_PLUG_EVENT,unpop PCH side PH:R406
update for PreMP
1.Add C790:100P_0402_50V8J,C791:100P_0201_25V8J for VGATE
2.Change Board ID to "4" for 1.0=>R960:56K
3.Change PCH from SA00005AG00:HM77 QPRG to MP version SA00005AGI0:HM77 SLJ8C
4.TB chip change to MP version:NA
5.Change LA8481P from DA6:DAA00003N00 to DAZ:DAZ0NS00100
6.Change Y1:25MHz cap:C744,C745 from 10P to 8.2P_0402_50V8D
7.For VR,change R454,R455 from 100K_5% to 100K_1%
8.Add C1261,C1291 2.2U_0603_6.3V6K for DDR Memory test issue
9.Change C1504,C1501,C1517,C1503,C1511,C1460,C1462,C1514
  from 0.1uF 0201 to 1uF 0201
10.Change TB R1083,R1078,R1089,R1080,R1081,R1082,R1088,R1086
   from 12.1ohm to 0ohm,R1086 change to @

0412 Modify for 1A layout
11.For Motor_BTN,add PH:R909 to +3VLP
12.Remove EC_TB_WAKE#:R1098
13.For LEGO,Change control pin from PCH to EC
  (1)LED:PCH_GPIO34 change to EC_GPIO122(TB_LED)
  (2)Eject:PCH_GPIO48 change to EC_GPIO64,pop R976(TB_EJECT_BTN)
  (3)pop Q30,Q31,R1125,unpop R1056,R1057

Security Classification	Compal Secret Data		
Issued Date	2012/4/6	Deciphered Date	2013/4/6

Compal Electronics, Inc.

Title: EE P.I.R

Size: Custom | Document Number: Q3ZMC M/B LA-8481P Schematic | Rev: 1.0

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