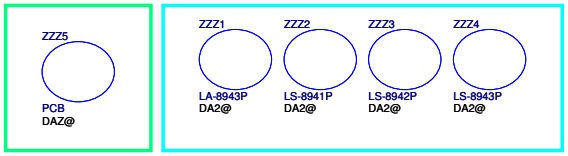
Model Name : Q1VZC
File Name :LA-8943P
BOM P/N:43



Compal Confidential

CHROME M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

2012-08-10

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

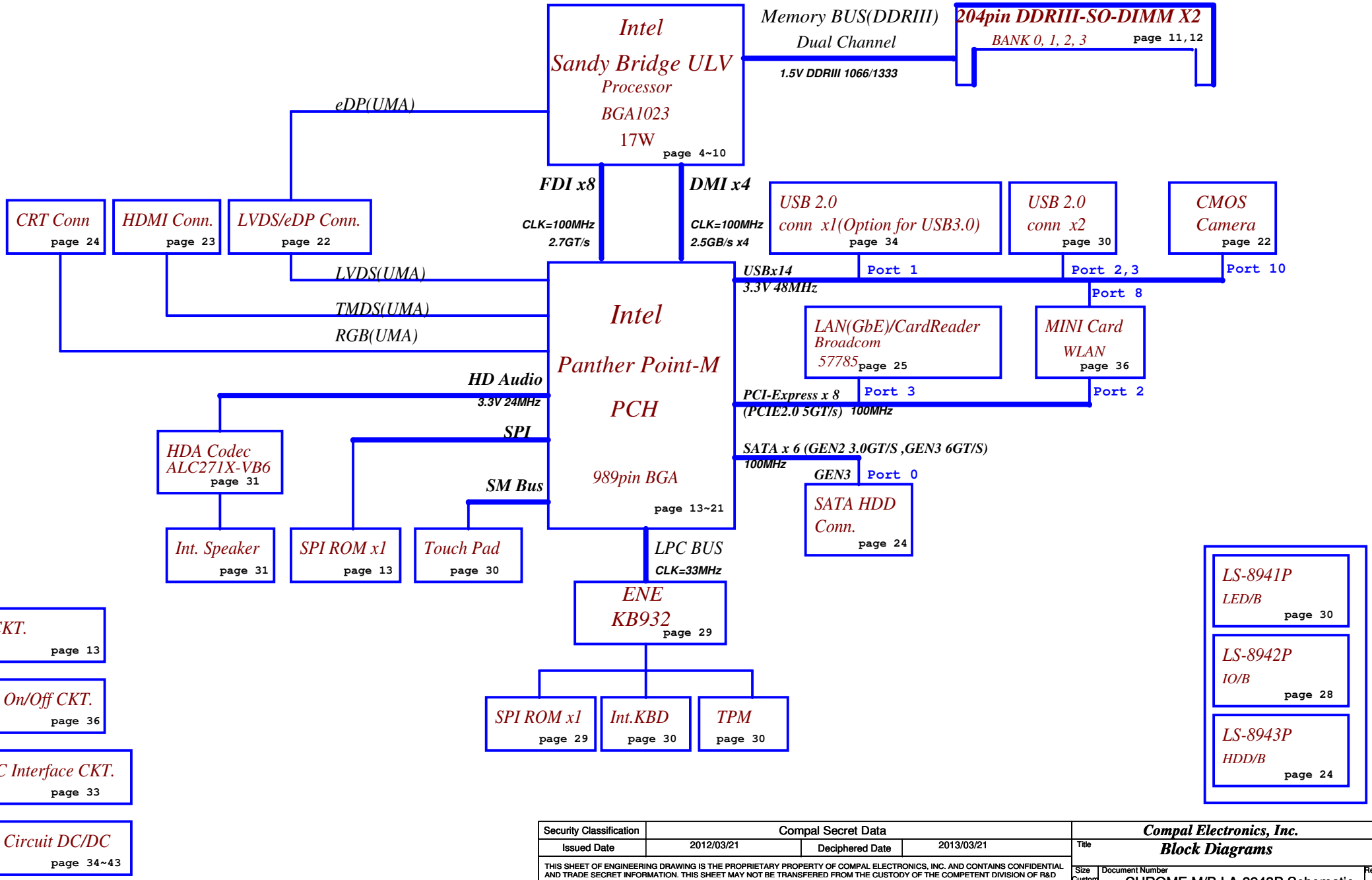
Title: *Cover Page*

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 1 of 45

Compal Confidential

Model Name : Q1VZC
File Name :LA-8943P



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: CHROME M/B LA-8943P Schematic		Rev: 0.1
Date: Friday, August 10, 2012	Sheet 2 of 45		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	OFF
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(STD)
ChannelB	DIMM0	B0	1010 010X	JDIMM2(REV)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Celeron 867	C867@
Celeron 877	C877@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
	UHCI1	2	USB port(Left 2.0)
		3	USB Port(Left 2.0)
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	Camera
		11	
	UHCI6	12	
		13	

USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	

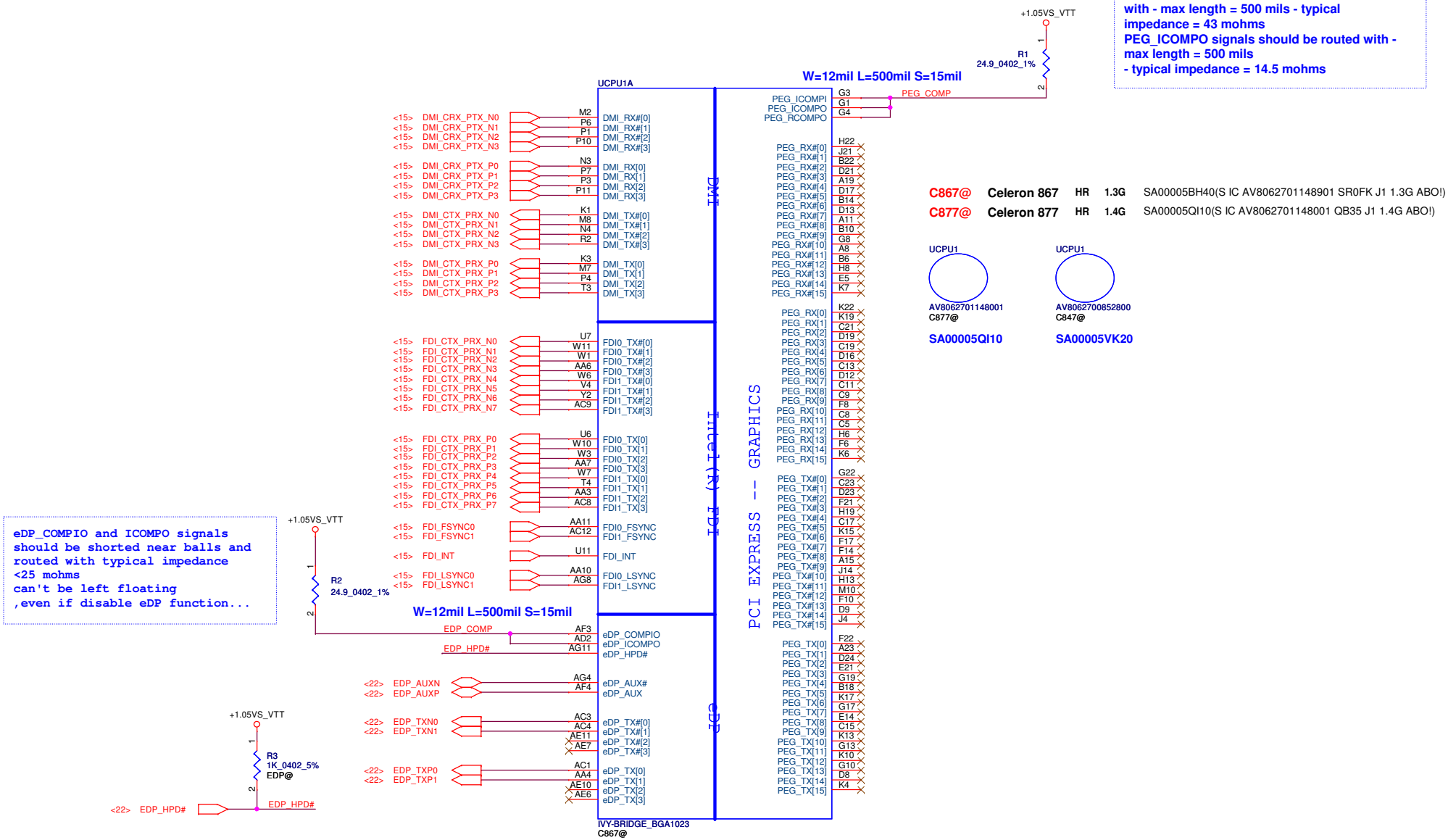
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Wednesday, August 15, 2012 | Sheet 3 of 45



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.			
Title	PROCESSOR(1/7) DMI,FDI,PEG		
Size	Document Number		Rev
Custom	CHROME M/B LA-8943P Schematic		0.1
Date:	Friday, August 10, 2012	Sheet 4 of 45	

0921 LVDS@->@

+1.05VS_VTT

CLK_CPU_DPLL# R4 2 LVDS@ 1 1K_0402_5%

CLK_CPU_DPLL R5 2 LVDS@ 1 1K_0402_5%

Checklist1.5 P.67 Graphis Disable Guide
eDP disable:
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PU 1K_5% to +1.05VS_VTT

PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.5& Tacoma_Fall2 1.0

reserve

C65 2 @ 1 0.1U_0402_16V4Z H_CPUPWRGD

R6 2 1 10K_0402_5%

PROC_SELECT#
PH VCPLL and connect to PCH DF_TVS

<17> H_SNB_IVB# F49 PROC_SELECT#

C57 PROC_DETECT#

偵測CPU有無安裝

XBOX 三缸功能

T1 PAD@ H_CATERR# C49 CATERR#

follow Checklist 1.5

<18,29> H_PECI H_PECI A48 PECI

+1.05VS_VTT R7 2 1 62_0402_5%

R8 56_0402_5%

<29,35> H_PROCHOT# H_PROCHOT# H_PROCHOT# R C45 PROCHOT#

<18> H_THRMTRIP# D45 THERMTRIP#

UCPU1B

MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

BCLK J3 H2 BCLK# CLK_CPU_DMI <14> CLK_CPU_DMI# <14>

DPLL_REF_CLK AG3 AG1 DPLL_REF_CLK# CLK_CPU_DPLL CLK_CPU_DPLL# CLK_CPU_DPLL <14> CLK_CPU_DPLL# <14>

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

SM_DRAMRST# AT30 SM_DRAMRST# SM_DRAMRST# <6>

SM_RCOMP[0] BF44 SM_RCOMP0 R9 2 1 140_0402_1%
SM_RCOMP[1] BE43 SM_RCOMP1 R10 2 1 25.5_0402_1%
SM_RCOMP[2] BG43 SM_RCOMP2 R11 2 1 200_0402_1%

DDR3 Compensation Signals

PRDY# N53
PREQ# N55

TCK L56 XDP_TCK PAD T2
TMS L55 XDP_TMS PAD T3
TRST# J58 XDP_TRST# PAD T4

TDI M60 XDP_TDI PAD T5
TDO L59 XDP_TDO PAD T6

DBR# K58 XDP_DBRESET# XDP_DBRESET# <15,28>

BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61

<15> H_PM_SYNC C48 PM_SYNC

<18> H_CPUPWRGD R13 1 2 0_0402_5% H_CPUPWRGD_R B46 UNCOREPWRGOOD

UNCOREPWRGOOD:非CORE外的電OK

PM_DRAM_PWRGD_R BE45 SM_DRAMPWROK

SM_DRAMPWROK:DRAM power ok

BUF_CPU_RST# D44 RESET#

IVY-BRIDGE_BGA1023
C867@

Follow DG 1.5 & Tacoma_Fall2 1.0
Buffered reset to CPU

Use open drain logic gate:
+1.05VS_VTT PU pop 75ohm
series resister pop 43ohm

+3VS

C66 0.1U_0402_16V4Z

+1.05VS_VTT

R12 75_0402_5%

R14 0_0402_5%

R15 43_0402_1%

U1

<17> PLT_RST# PLT_RST# BUFO_CPU_RST# BUF_CPU_RST#

SN74LVC1G07DCKR_SC70-5

RESET#:都ok後請CPU做reset

Follow DG 1.5 & Tacoma_Fall2 1.0

Use open drain logic gate:
+1.5V_CPU_VDDQ PU pop 200ohm
series resister pop 130ohm

+3VALW

C67 0.1U_0402_16V4Z

+1.5V_CPU_VDDQ

R16 200_0402_5%

U2

<15> SYS_PWROK

<15> PM_DRAM_PWRGD

PM_SYS_PWRGD_BUF R18 PM_DRAM_PWRGD_R 130_0402_5%

MC74VHC1G09DFT2G_SC70-5

C476 @ 2 1 H_CPUPWRGD_R
180P_0402_50V8J
12/22 Add(ESD request)

+3VS

XDP_DBRESET# R17 2 1 1K_0402_5%

Tacoma_Fall2 1.0 PU 1K +3VS
Check list 1.5 PU 1K +3VS
Debug port DG1.1-1.3 50~5K ohm

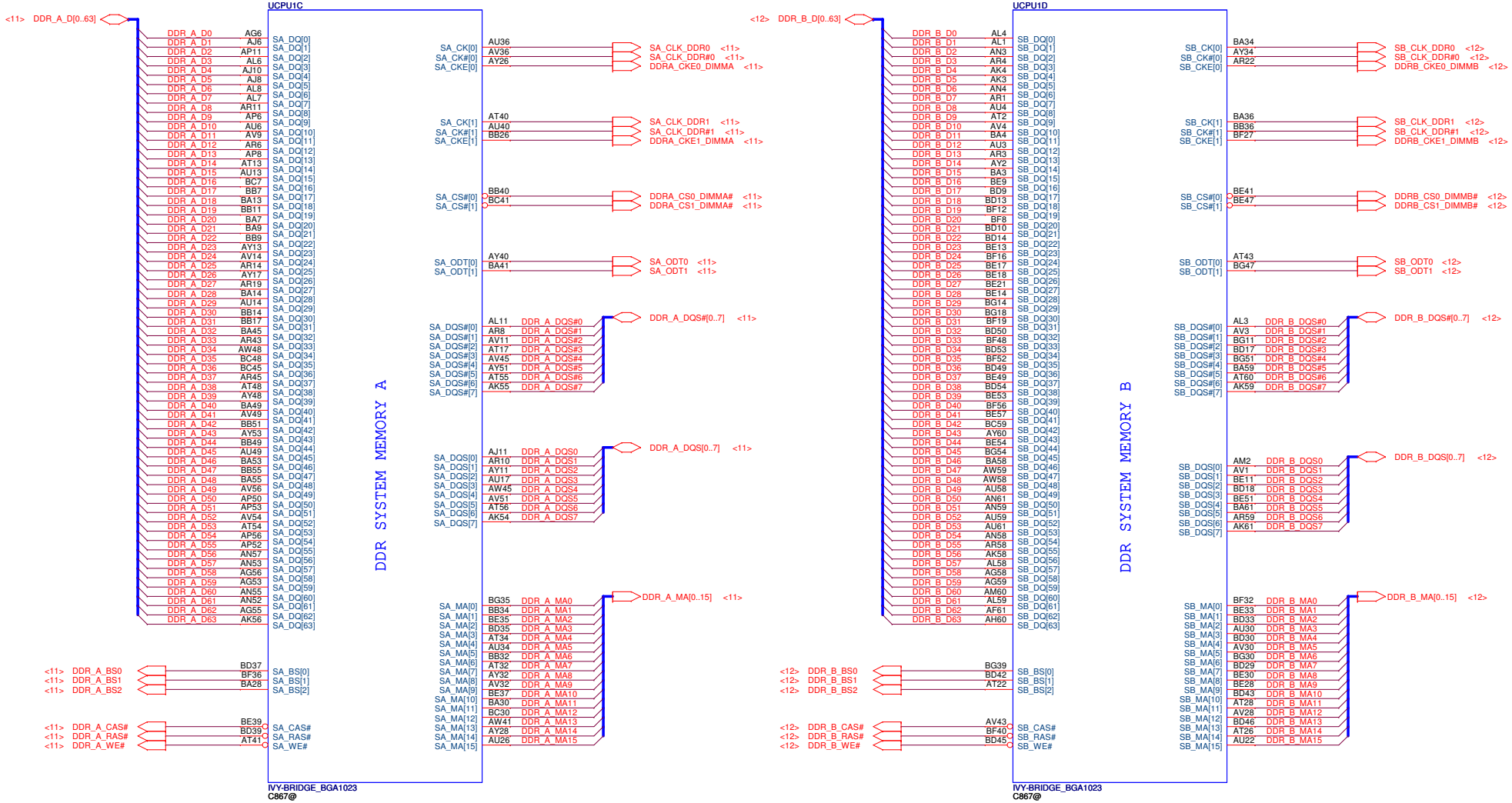
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

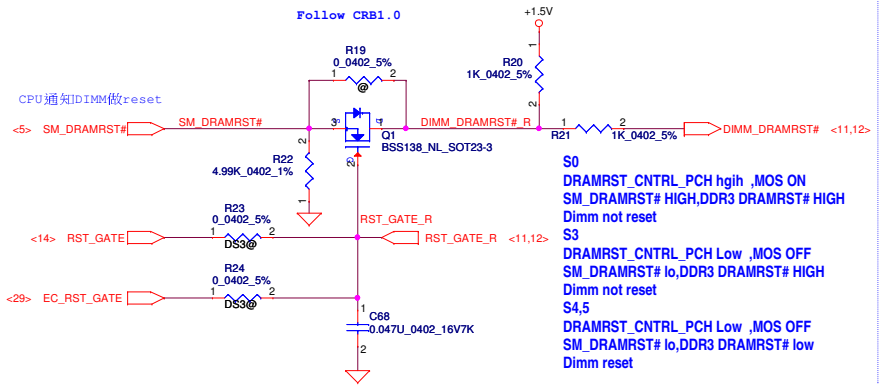
Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 5 of 45





S0
DRAMRST_CNTRL_PCH hgih ,MOS ON
SM_DRAMRST# HIGH,DDR3 DRAMRST# HIGH
Dimm not reset
S3
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# lo,DDR3 DRAMRST# HIGH
Dimm not reset
S4,5
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# lo,DDR3 DRAMRST# low
Dimm reset

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

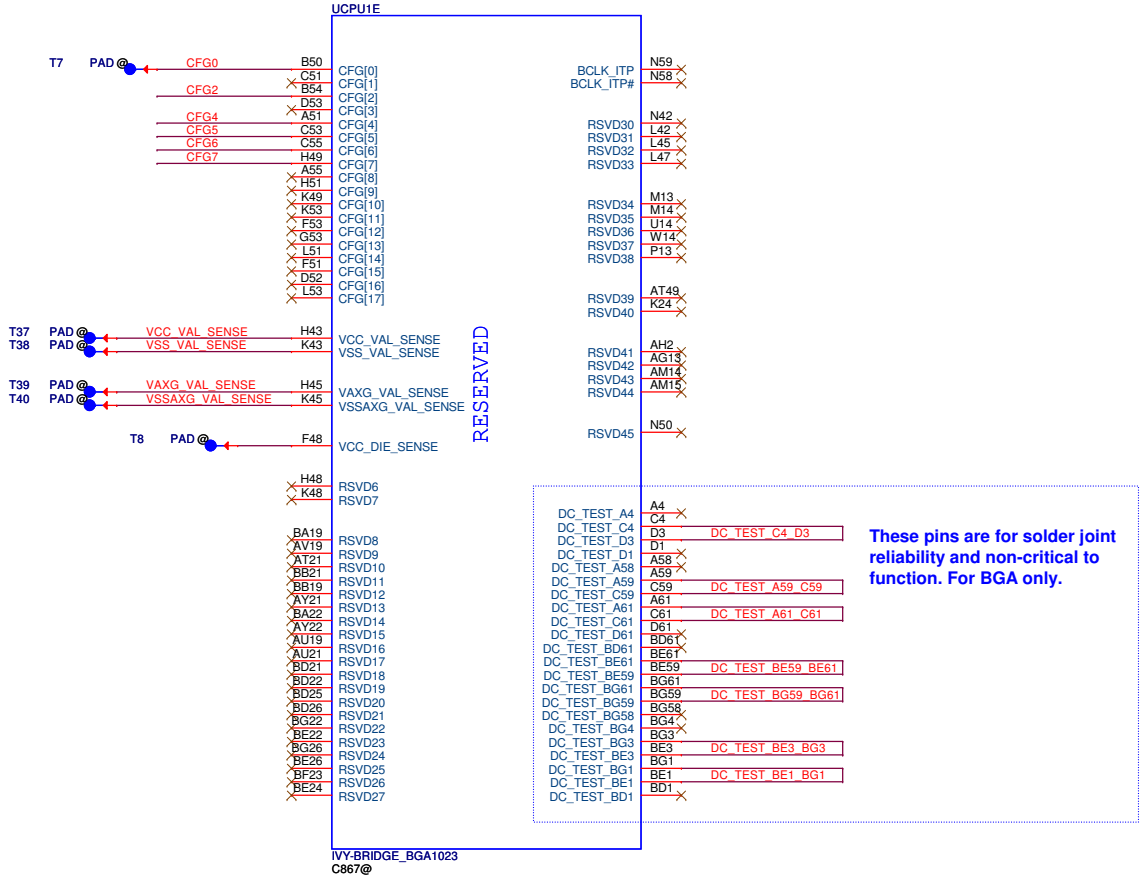
Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

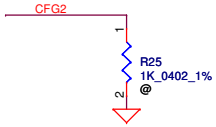
Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 | Sheet 6 of 45

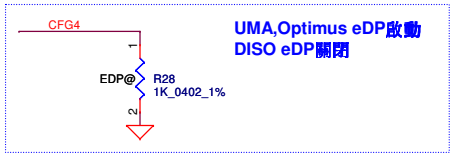
CFG Straps for Processor



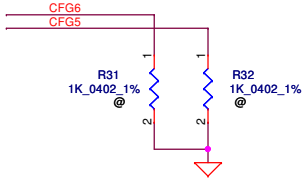
These pins are for solder joint reliability and non-critical to function. For BGA only.



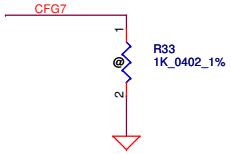
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0:Lane Reversed



eDP enable	
CFG4	★ 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express ★10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 7 of 45

POWER

UCPU1F

ULV type
DC 33A

8.5A

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

CORE SUPPLY

VCC[1] A26
VCC[2] A29
VCC[3] A31
VCC[4] A34
VCC[5] A35
VCC[6] A38
VCC[7] A39
VCC[8] A42
VCC[9] C26
VCC[10] C27
VCC[11] C32
VCC[12] C34
VCC[13] C37
VCC[14] C39
VCC[15] C42
VCC[16] D27
VCC[17] D32
VCC[18] D34
VCC[19] D37
VCC[20] D39
VCC[21] D42
VCC[22] E26
VCC[23] E28
VCC[24] E32
VCC[25] E34
VCC[26] E37
VCC[27] E38
VCC[28] F25
VCC[29] F26
VCC[30] F28
VCC[31] F32
VCC[32] F34
VCC[33] F37
VCC[34] F38
VCC[35] F42
VCC[36] G42
VCC[37] H25
VCC[38] H26
VCC[39] H28
VCC[40] H29
VCC[41] H32
VCC[42] H34
VCC[43] H35
VCC[44] H37
VCC[45] H38
VCC[46] H40
VCC[47] J25
VCC[48] J26
VCC[49] J28
VCC[50] J29
VCC[51] J32
VCC[52] J34
VCC[53] J35
VCC[54] J37
VCC[55] J38
VCC[56] J40
VCC[57] J42
VCC[58] K26
VCC[59] K27
VCC[60] K29
VCC[61] K32
VCC[62] K34
VCC[63] K35
VCC[64] K37
VCC[66] K39
VCC[67] K42
VCC[68] L25
VCC[69] L28
VCC[70] L33
VCC[71] L36
VCC[72] L40
VCC[73] N26
VCC[74] N30
VCC[75] N34
VCC[76] N38

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] AJ17
VCCIO[7] AJ21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

For PEG

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AF16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

+1.05VS_VTT
VCCIO50 W16
VCCIO51 W17

+3VS
R34 10K_0402_5% @
VCCIO_SEL
R35 10K_0402_5% @

VCCIO_SEL after Ivy bridge ES2 Voltage support		
BC22	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL
BC22 VCCIO_SEL

QUIET RAILS

+1.05VS_VTT
VCCPQE[1] AM25
VCCPQE[2] AN22
C69 1U_0402_6.3V6K

+1.05VS_VTT
R36 130_0402_5%

+1.05VS_VTT
R37 75_0402_5%

Place the PU resistors close to CPU

SVID

VIDALERT# A44 H_CPU_SVIDALRT#
VIDSCLK B43 H_CPU_SVIDCLK
VIDSOUT C44 H_CPU_SVIDDAT

R38 43_0402_1% SVID_ALERT# <41>
R39 0_0402_5% SVID_CLK <41>
R40 0_0402_5% SVID_DATA <41>

+CPU_CORE
R41 100_0402_1%

Place the PU resistors close to VR

SENSE LINES

VCC_SENSE F43 VCCSENSE_R
VSS_SENSE G43 VSSSENSE_R
R42 0_0402_5% VCCSENSE <41>
R43 0_0402_5% VSSSENSE <41>

R44 10_0402_5% +1.05VS_VTT
VCCIO_SENSE AN16
VSS_SENSE_VCCIO AN17
VSSIO_SENSE
VCCIO_SENSE <40>
R46 10_0402_5%

R45 100_0402_1%

Should change to connect form power cirucit & layout differential with VCCIO_SENSE.

Check list 1.5

IVY-BRIDGE_BGA1023
C867@

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1
Date: Friday, August 10, 2012	Sheet 8 of 45	

POWER

UCPU1G

+VGFX_CORE

DC 16A

INTEL Recommend VAXG
2*470uF,6*22uF(0805) and 6*10uF(0603)
11*1U(0402)
PD0.8

VAXG[1..56]

GRAPHICS

DDR3 - 1.5V RAILS

5A

VDDQ[1..26]

Place TOP IN BGA

C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 1U_0402_6.3V6K

Place BOT OUT BGA

C82 C83 C84 C85 C86 C87 C88 C89 10U_0603_6.3V6M

+1.5V_CPU_VDDQ

+V_SM_VREF should
have 20 mil trace width

R47 1K_0402_5%

R48 1K_0402_5%

C70 0.1U_0402_16V4Z

SM_VREF

AY43 +V_SM_VREF

VREF

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ

BE7 SA_DIMM_VREFDQ
BG7 SB_DIMM_VREFDQ

SA_DIMM_VREFDQ <11>
SB_DIMM_VREFDQ <12>

R49 1K_0402_1% @

R50 1K_0402_1% @

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
Check list1.5 P18 M1 default M3 no stuff

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.8

+1.5V_CPU_VDDQ

J1 JUMP_43X118 @

+1.5VS

C81 330U_D2_2V_Y

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

CR CheckList Rev1.5

+VGFX_CORE

R51 100_0402_5%

R52 100_0402_5%

<41> VCC_GFXSENSE
<41> VSS_GFXSENSE

F45 VAXG_SENSE
G45 VSSAXG_SENSE

SENSE LINES

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD0.8

1.2A

BB3 VCCPLL[1]
BC1 VCCPLL[2]
BC4 VCCPLL[3]

1.8V RAIL

+1.8VS

Place BOT OUT Conn

C91 @ 220U_B2_2.5VM_R35

C92 C93 1U_0402_6.3V6K

SGA00001700 S POLY C 220U
220U 2.5V M B2 ESR35 TPE H1.9

QUIET RAILS

+1.5V_CPU_VDDQ

AM28 VCCDQ[1]
AN26 VCCDQ[2]

C90 1U_0402_6.3V6K

VDDQ_SENSE BC43
VSS_SENSE_VDDQ BA43

SENSE LINES

6A

L17 VCCSA[1]
L21 VCCSA[2]
N16 VCCSA[3]
N20 VCCSA[4]
N22 VCCSA[5]
P17 VCCSA[6]
P20 VCCSA[7]
R16 VCCSA[8]
R18 VCCSA[9]
R21 VCCSA[10]
U15 VCCSA[11]
V16 VCCSA[12]
V17 VCCSA[13]
V18 VCCSA[14]
V21 VCCSA[15]
W20 VCCSA[16]

SA RAIL

+VCCSA

Place TOP IN BGA

C94 330U_D2_2V_Y

C95 C96 C97 C98 C99 1U_0402_6.3V6K

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

Place BOT OUT BGA

C100 C101 C102 C103 C104 10U_0603_6.3V6M

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.8

VCCSA_SENSE U10

CPU EDS1.3 P.93
VCCSA_VID0 Must PD

VCCSA_SENSE <39>

VCCSA_VID[0..1]

D48 H_VCCSA_VID0
D49 H_VCCSA_VID1

H_VCCSA_VID0 <39>
H_VCCSA_VID1 <39>

R53 0_0402_5% @

VCCSA VID lines

VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V

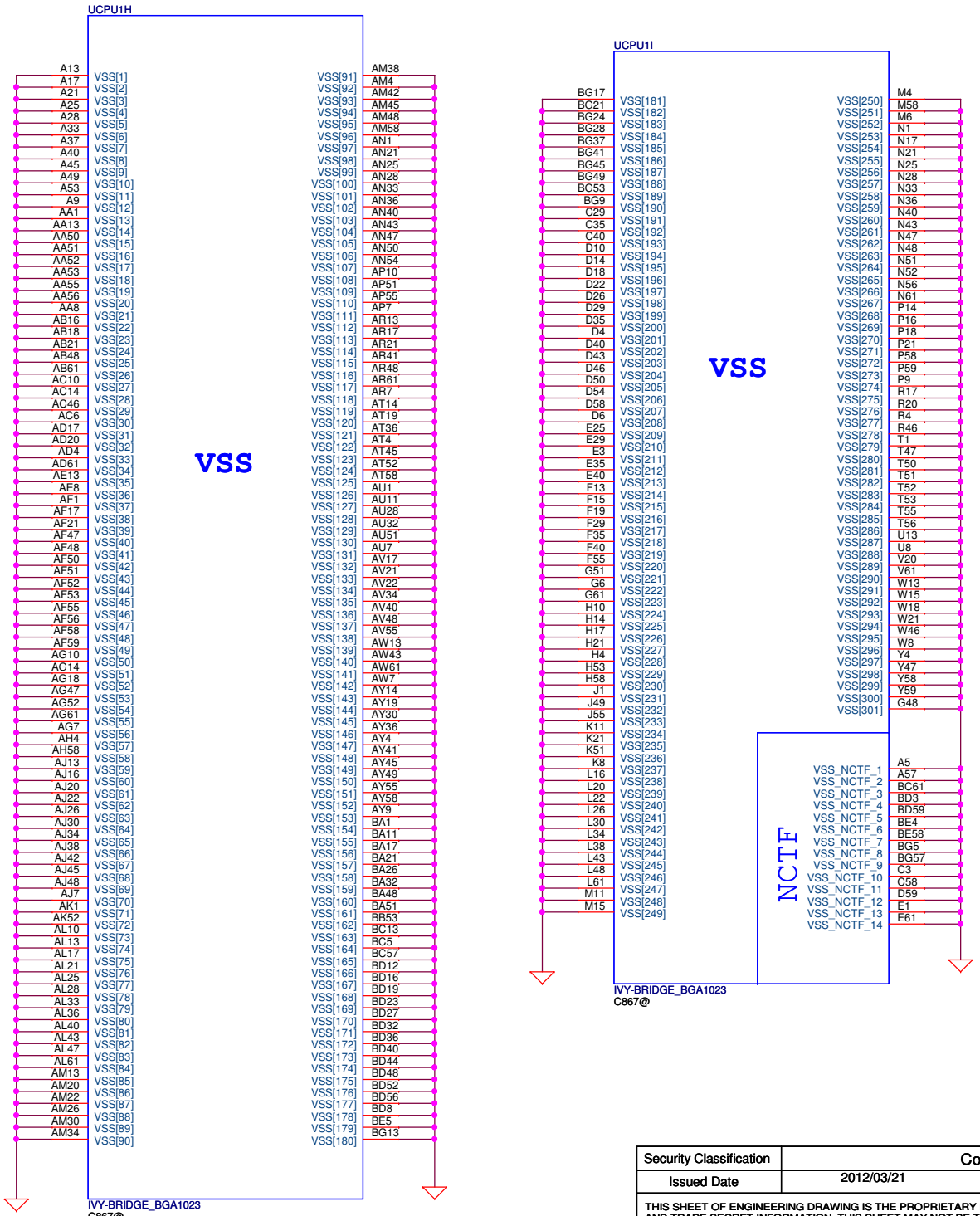
IVY-BRIDGE_BGA1023
C867@

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1
Date: Friday, August 10, 2012	Sheet 9 of 45	

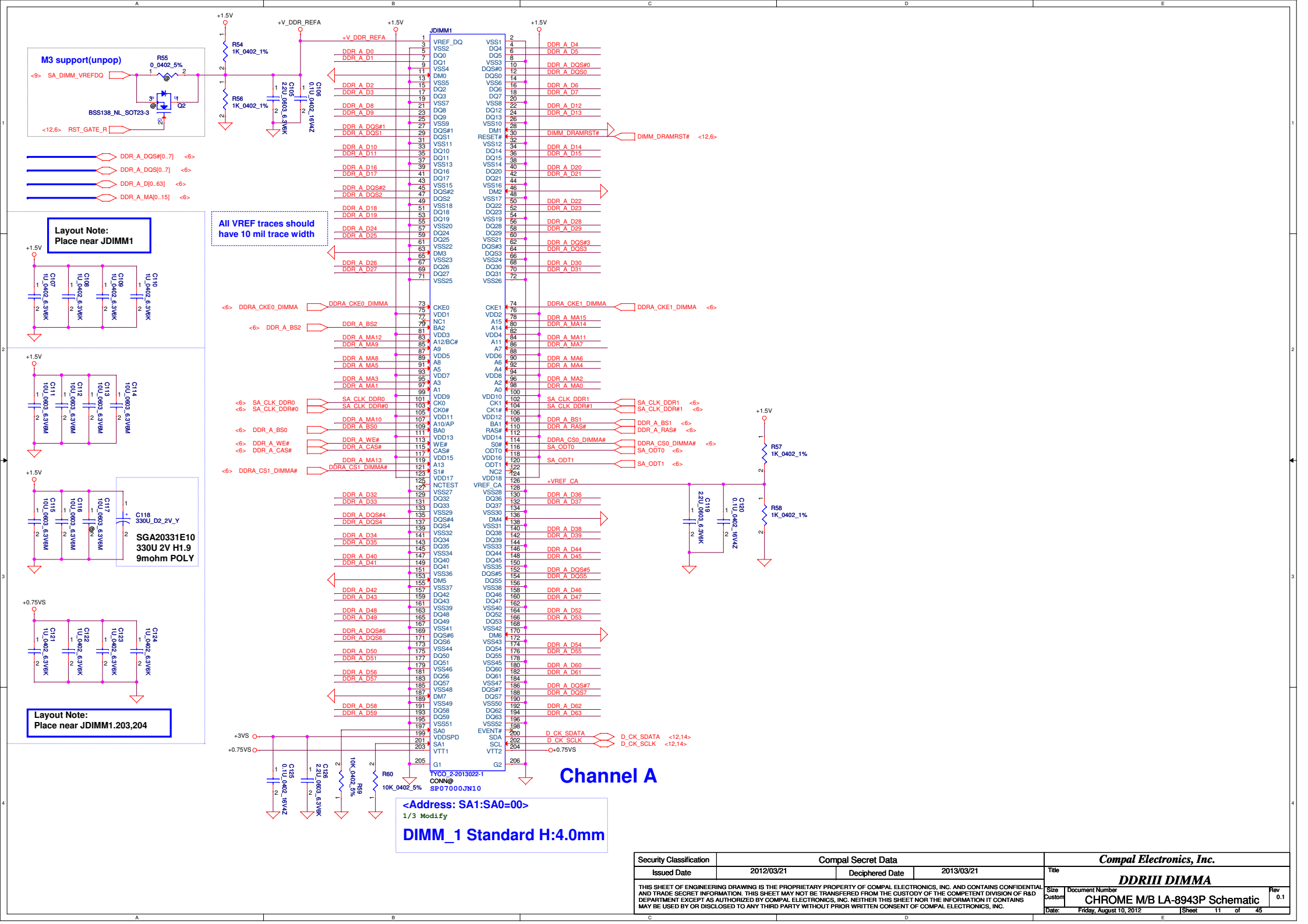


Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: ***PROCESSOR(7/7) VSS***

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1
Date: Friday, August 10, 2012	Sheet 10 of 45	

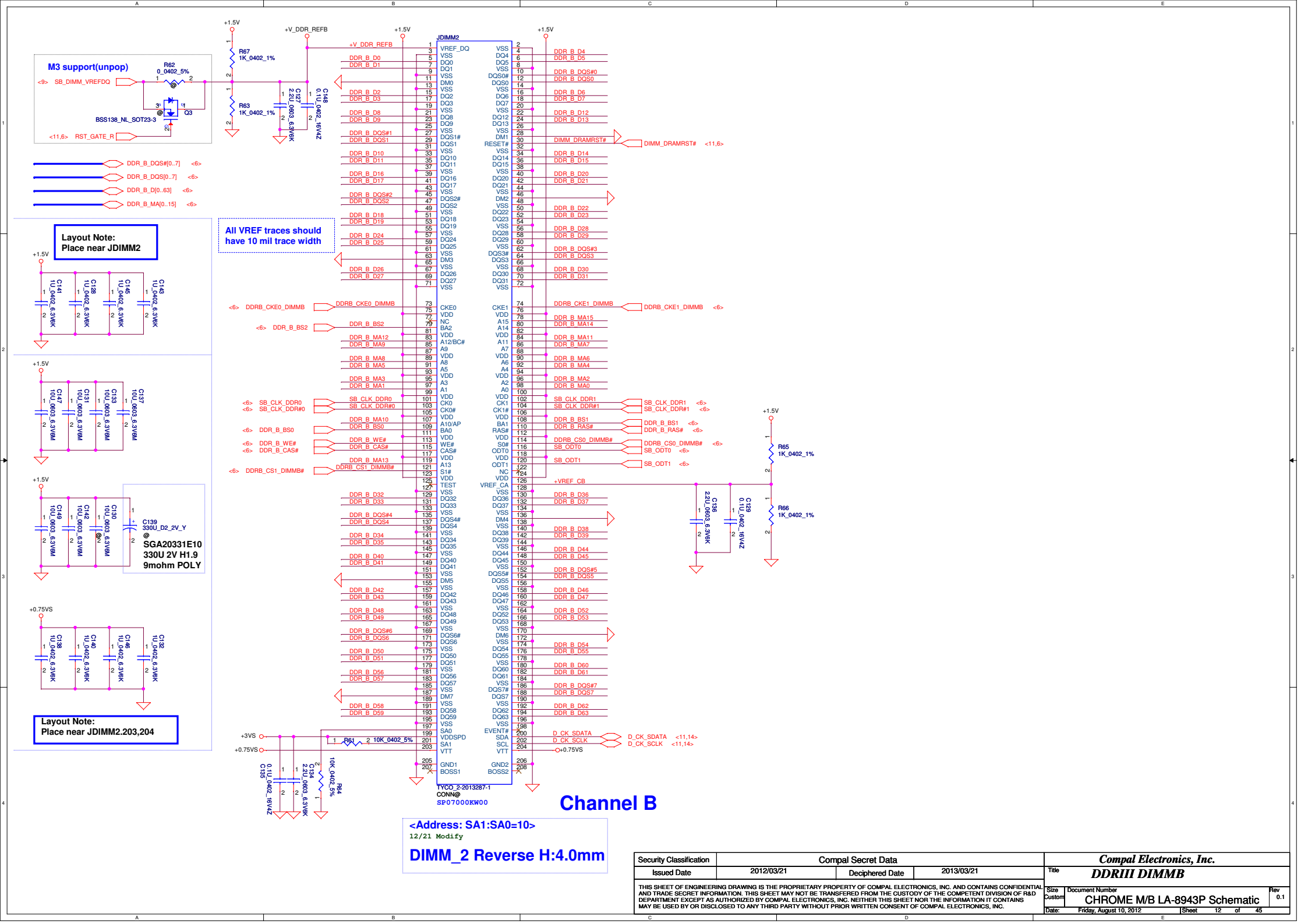


Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: *DDRIII DIMMA*

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1
Date: Friday, August 10, 2012	Sheet 11 of 45	



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.			
Title	DDRIII DIMMB		
Size: Custom	Document Number: CHROME M/B LA-8943P Schematic		Rev: 0.1
Date: Friday, August 10, 2012	Sheet 12 of 45		

RTCRST close RAM door J1

+RTCVCC C163 1U_0603_10V6K R74 0_0603_5% PCH_RTCRST#
R75 20K_0402_5% PCH_SRTCRST#
R76 20K_0402_5%
C164 1U_0603_10V6K R77 0_0603_5%

+RTCVCC R78 1M_0402_5% SM_INTRUDER#
R79 330K_0402_5% PCH_INTVRMEN

INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS R82 @ 1K_0402_5% PCH_SPKR
HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

+VCCSUS3_3 R84 1K_0402_5% HDA_SDOUT_PCH
HDA_SDO
<29> HDA_SDO R83 MIM@ 0_0402_5%
<18,18,28,29,30> SPI_WP1#_R R145 CRM@ 4.7K_0402_5%
ME debug mode,this signal has a weak internal PD
★ Low = Disable (Default)
High = Enabled [Flash Descriptor Security Overide]

+VCCSUS3_3 R87 1K_0402_5% HDA_SYNC_PCH
This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

<31> HDA_BITCLK_AUDIO R88 33_0402_5% HDA_BITCLK_PCH
<31> HDA_SYNC_AUDIO R89 33_0402_5% HDA_SYNC_PCH_R
<31> HDA_RST_AUDIO# R92 33_0402_5% HDA_RST_PCH#
<31> HDA_SDOUT_AUDIO R95 33_0402_5% HDA_SDOUT_PCH

<28> SPI_HOLD1#_R R559 0_0402_5% SPI_HOLD1#
<28> PCH_SPI_MOSI_1_R R558 0_0402_5% PCH_SPI_MOSI_1
<28> PCH_SPI_MISO_1_R R557 0_0402_5% PCH_SPI_MISO_1
<28> PCH_SPI_CS0#_1_R R556 0_0402_5% PCH_SPI_CS0#_1
<28> PCH_SPI_CLK_1_R R555 0_0402_5% PCH_SPI_CLK_1
<18,18,28,29,30> SPI_WP1#_R R554 1K_0402_5% SPI_WP1#
DEG@ CRM@

PCH_RTCX1 R107 10M_0402_5% PCH_RTCX2
Y1 32.768KHZ_12.5PF_1TJF125DP1A000D
C167 18P_0402_50V8J C168 18P_0402_50V8J

11/30 Add (EMI request)
HDA_BITCLK_AUDIO C467 22P_0402_50V8J @

Prevent back drive issue.
+5VS Q4 BSS138_NL_SOT23-3 HDA_SYNC_PCH R90 0_0402_5% R93 1M_0402_5%

U16 3/7 Add BD82HM70 HM70@ SA00005MQ20

U16 5/23 Add BD82NM70 NM70@ SA00005WU20

+RTCBATT 20mil D1 BAS40-04_SOT23-3
+RTCVCC 20mil C165 0.1U_0402_16V4Z 20mil +CHGRTC

SERIRQ R80 10K_0402_5%
PCH_SATALED# R81 10K_0402_5%

U16A

PCH_RTCX1	A20	RTCX1	RTC	FWH0 / LAD0	C38 LPC_AD0
PCH_RTCX2	C20	RTCX2		FWH1 / LAD1	A38 LPC_AD1
PCH_RTCRST#	D20	RTCRST#		FWH2 / LAD2	B37 LPC_AD2
PCH_SRTCRST#	G22	SRTCRST#		FWH3 / LAD3	C37 LPC_AD3
SM_INTRUDER#	K22	INTRUDER#		FWH4 / LFRAME#	D36 LPC_FRAME#
PCH_INTVRMEN	C17	INTVRMEN		LDRQ0#	E36
				LDRQ1# / GPIO23	K36 PCH_GPIO23
				SERIRQ	V5 SERIRQ
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA	SATA0RXN	AM3
HDA_SYNC_PCH	L34	HDA_SYNC		SATA0RXP	AM1
PCH_SPKR	T10	SPKR		SATA0TXN	AP7
HDA_RST_PCH#	K34	HDA_RST#		SATA0TXP	AP5
HDA_SDIN0	E34	HDA_SDIN0		SATA1RXN	AM10
	G34	HDA_SDIN1		SATA1RXP	AM8
	C34	HDA_SDIN2		SATA1TXN	AP11
	A34	HDA_SDIN3		SATA1TXP	AP10
HDA_SDOUT_PCH	A36	HDA_SDO		SATA2RXN	AD7
	C36	HDA_DOCK_EN# / GPIO33		SATA2RXP	AD5
	N32	HDA_DOCK_RST# / GPIO13		SATA2TXN	AH5
				SATA2TXP	AH4
			SATA	SATA3RXN	AB8
				SATA3RXP	AB10
				SATA3TXN	AF3
				SATA3TXP	AF1
				SATA4RXN	Y7
				SATA4RXP	Y5
				SATA4TXN	AD3
				SATA4TXP	AD1
				SATA5RXN	Y3
				SATA5RXP	Y1
				SATA5TXN	AB3
				SATA5TXP	AB1
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG	SATAICOMPO	Y11
PCH_JTAG_TMS	H7	JTAG_TMS		SATAICOMPI	Y10
PCH_JTAG_TDI	K5	JTAG_TDI		SATA3RCOMPO	AB12
PCH_JTAG_TDO	H1	JTAG_TDO		SATA3COMPI	AB13
				SATA3RBIAS	AH1
PCH_SPI_CLK	T3	SPI_CLK	SPI	SATALED#	P3 PCH_SATALED#
PCH_SPI_CS0#	Y14	SPI_CS0#		SATA0GP / GPIO21	V14 PCH_GPIO21
PCH_SPI_CS1#	T1	SPI_CS1#		SATA1GP / GPIO19	P1 PCH_GPIO19
PCH_SPI_MOSI	V4	SPI_MOSI			
PCH_SPI_MISO	U3	SPI_MISO			

HM77@ COUGARPOINT_FCBGA989

<31> PCH_SPKR
<31> HDA_SDIN0
PAD T9 @ PCH_JTAG_TCK
PAD T10 @ PCH_JTAG_TMS
PAD T11 @ PCH_JTAG_TDI
PCH_JTAG_TDO
R91 51_0402_5%

HDD1
SATA_PRX_DTX_N0 <24>
SATA_PRX_DTX_P0 <24>
SATA_PTX_DRX_N0 <24>
SATA_PTX_DRX_P0 <24>

12/1 Del

HM70 not support SATA for port1/port3

L=500mil S=15mil
SATA_COMP R94 37.4_0402_1%
+1.05VS_VTT
L=500mil S=15mil
SATA3_COMP R97 49.9_0402_1%
+1.05VS_VTT
RBIAS_SATA3 R99 750_0402_1%

No use PU 10K +3VS
GPIO19 has internal Pull up

+3VS R230 10K_0402_5% PCH_GPIO23
+3VS R85 10K_0402_5% PCH_GPIO21
R234 1K_0402_5% @
R86 10K_0402_5% @

+3VS R102 4.7K_0402_5% PCH_GPIO19
Debug Port DG 1.2 PU 4.7K +3VS

PCH_SPI_CLK_2 R96 33_0402_5%
PCH_SPI_CLK_1 R98 33_0402_5% PCH_SPI_CLK
PCH_SPI_CS0#_1 R100 33_0402_5% PCH_SPI_CS0#
PCH_SPI_CS1#_2 R101 33_0402_5% PCH_SPI_CS1#
PCH_SPI_MOSI_2 R103 33_0402_5%
PCH_SPI_MOSI_1 33_0402_5% R104 PCH_SPI_MOSI
PCH_SPI_MISO_1 R105 33_0402_5% PCH_SPI_MISO
PCH_SPI_MISO_2 R106 33_0402_5%

+BIOS_SPI MIM@ R560 0_0402_5% +3VS
RB751V-40_SOD323-2 D23 CRM@

+BIOS_SPI R109 MIM@ 3.3K_0402_5% SPI_WP1#
R108 3.3K_0402_5% SPI_HOLD1#
PCH_SPI_CS0#_1
U17 4M@ CS# WP# HOLD# GND VCC SCLK SI SO
PCH_SPI_CLK_1
PCH_SPI_MOSI_1
PCH_SPI_MISO_1
MX25L3206EM2I-12G_SO8
SA000041P00

SPI ROM FOR ME (4MB)
Footprint 200mil

Reserve for EMI
PCH_SPI_CLK 33_0402_5% R110 C166 10P_0402_50V8J
11/30 Add
PCH_SPI_CLK_1 33_0402_5% R466 22P_0402_50V8J C465
PCH_SPI_CLK_2 33_0402_5% R467 22P_0402_50V8J C466

U17 3/26 Add MX25L6406EM2I-12G_SO8 8M@ SA00004G600

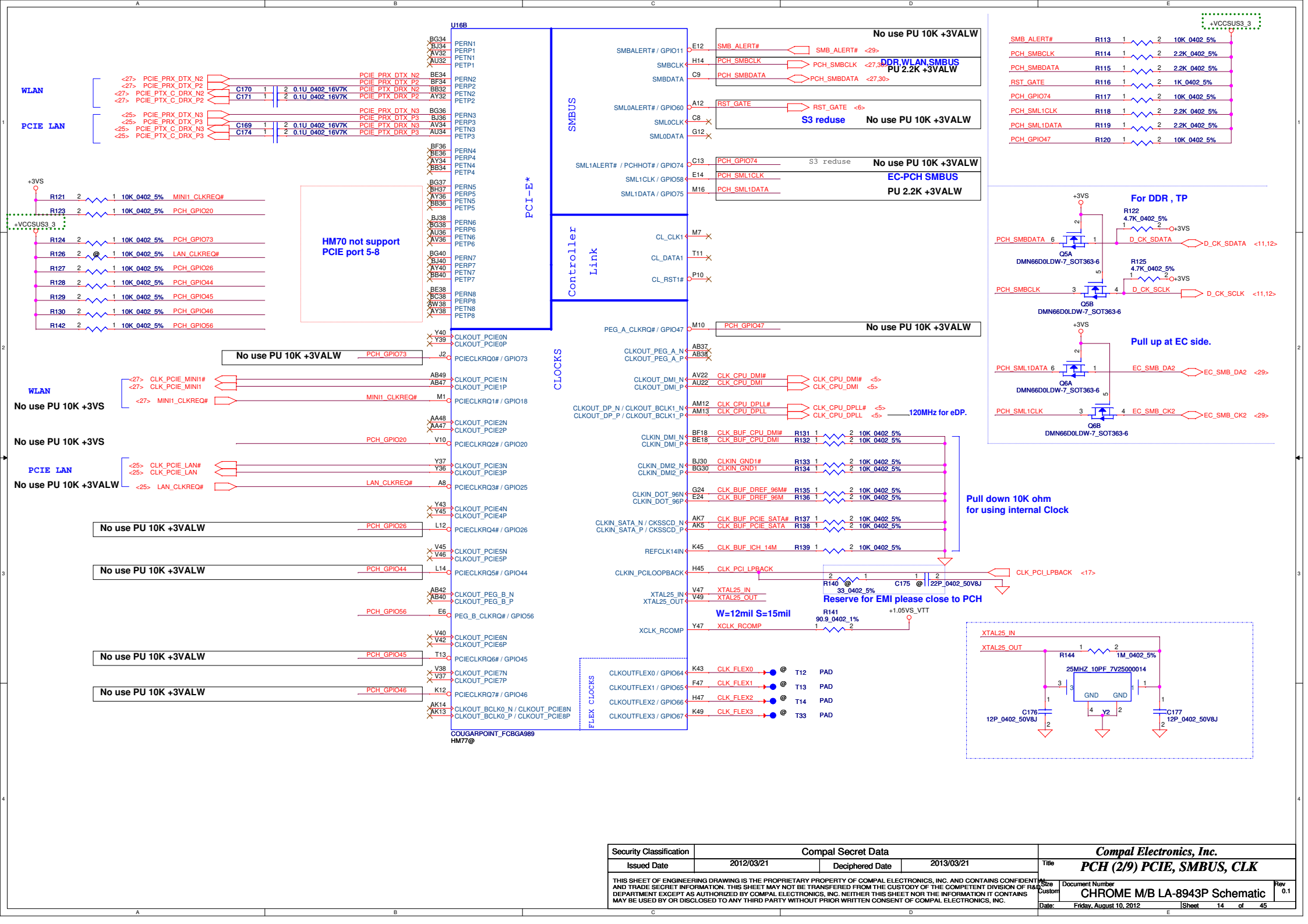
12/7 Change symbol of U18 from SA00000XT00 to SA000041O00
+3VS R111 3.3K_0402_5% PCH_SPI_CS1#_2 PCH_SPI_MISO_2 SPI_WP2#
U18 1M@ CS# SO WP# GND VCC HOLD# SCLK SI
SPI_HOLD2# R112 3.3K_0402_5% PCH_SPI_CLK_2 PCH_SPI_MOSI_2
MX25L8006EM2I-12G_SO8
SA000041O00

SPI ROM FOR ME (1MB)
Footprint 200mil

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
–	1	0
★ SPI	1	1

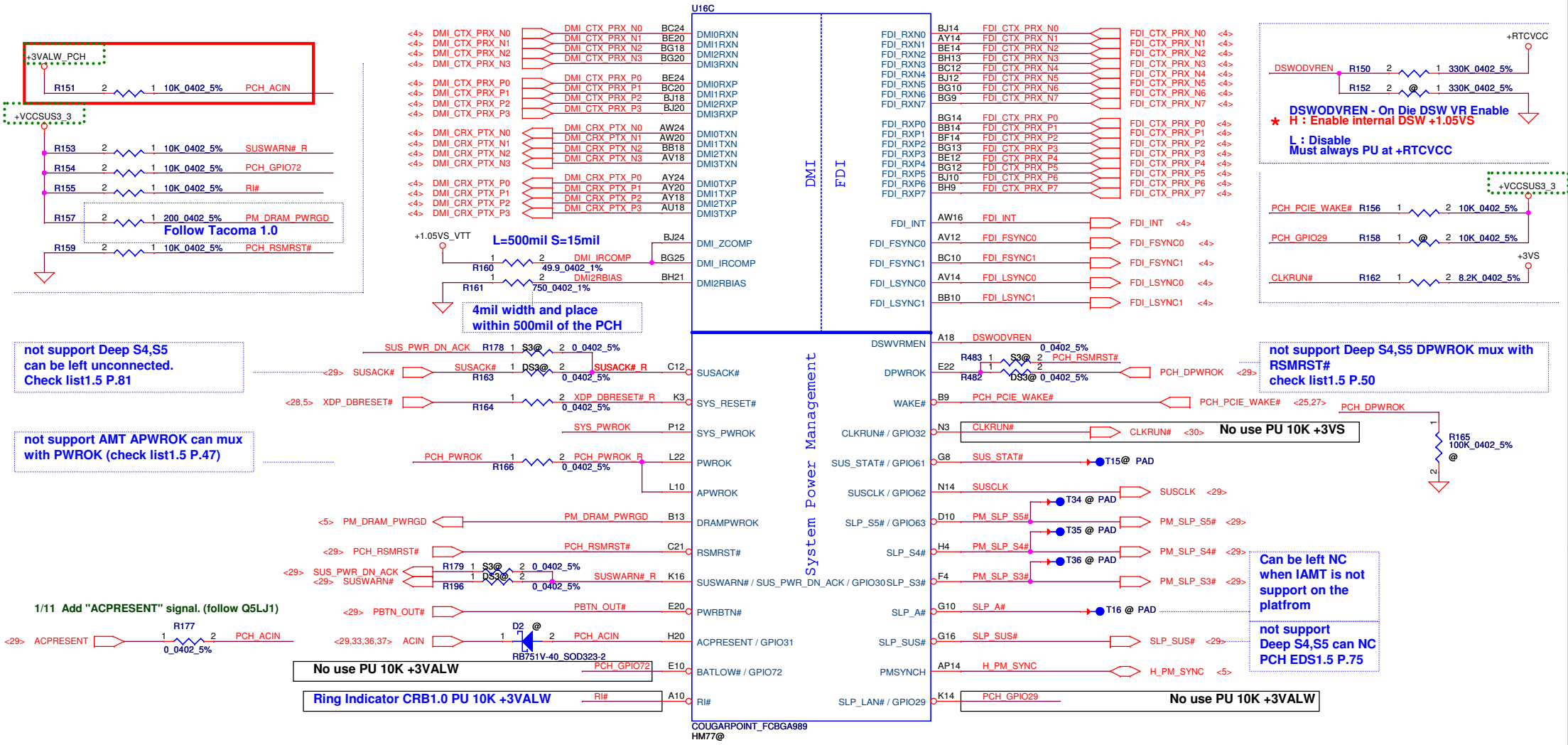
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1
Date: Friday, August 10, 2012 | Sheet 13 of 45



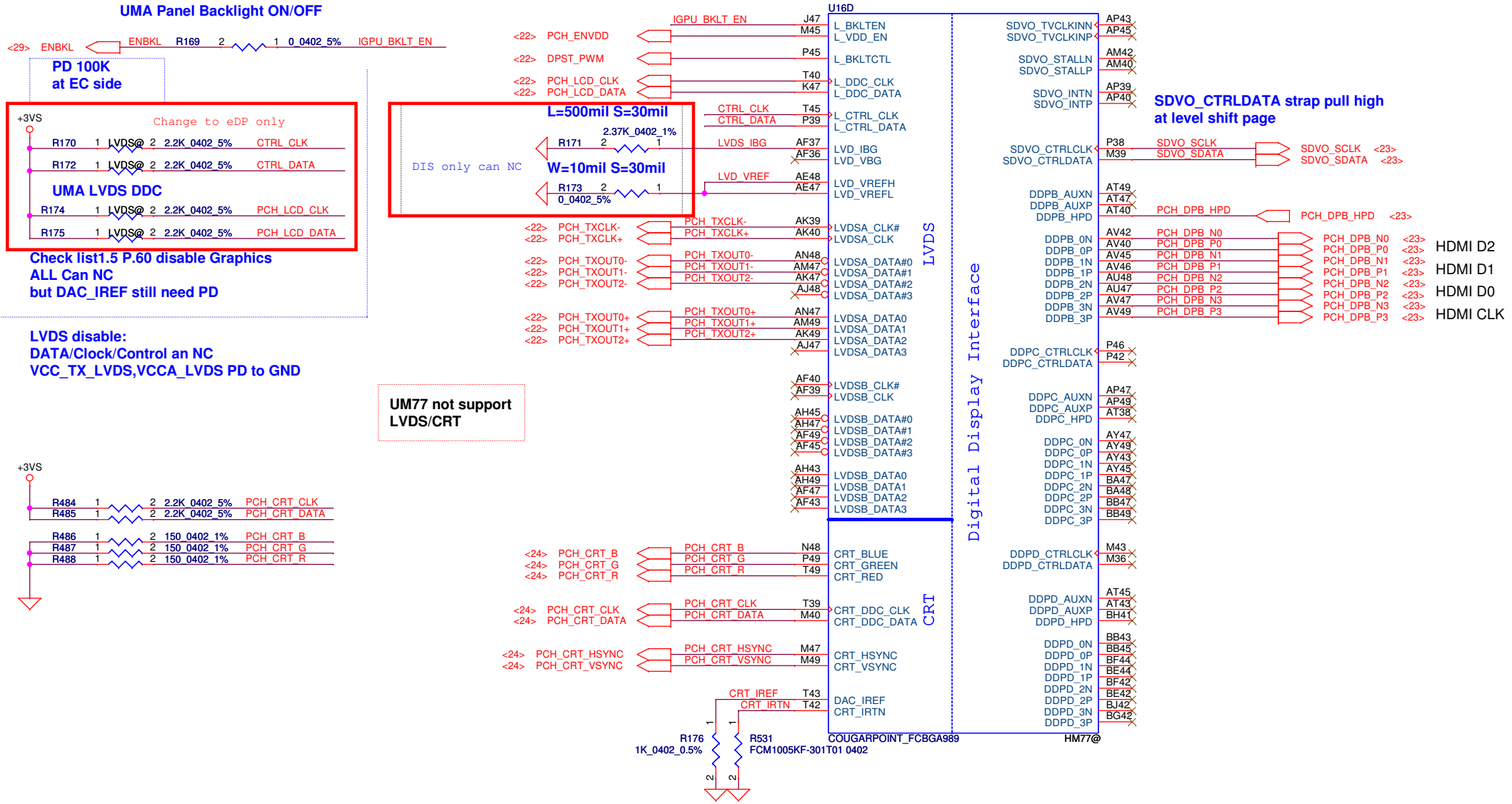
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date 2013/03/21	Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom	Document Number: CHROME M/B LA-8943P Schematic		Rev: 0.1
Date: Friday, August 10, 2012	Sheet 14 of 45		



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.			
Title	PCH (3/9) DMI,FDI,PM		
Size: Custom	Document Number: CHROME M/B LA-8943P Schematic		Rev: 0.1
Date: Friday, August 10, 2012	Sheet 15 of 45		



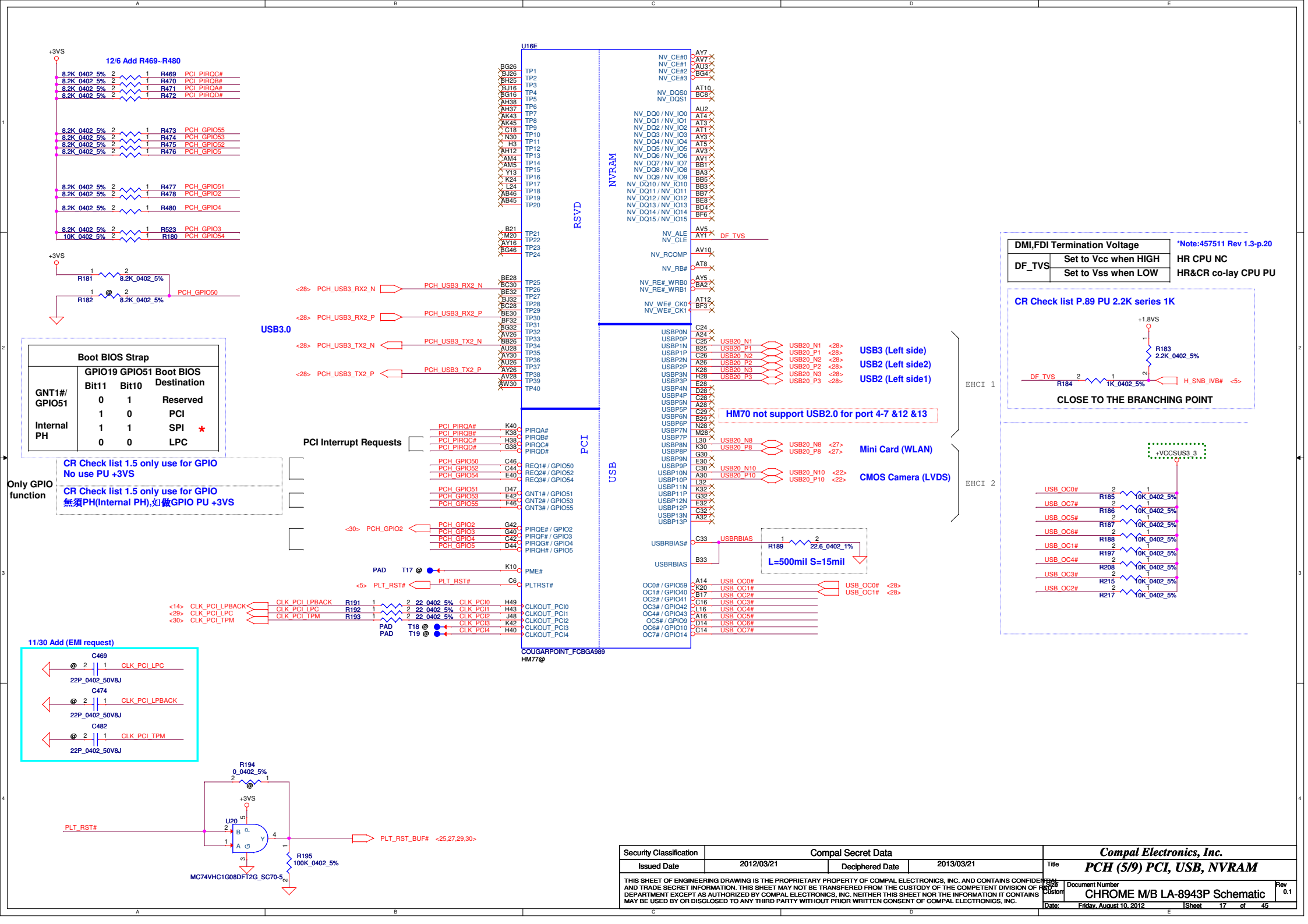
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 16 of 45



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 17 of 45

HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+VCCSUS3_3
R202 4.7K_0402_5%
PCH_GPIO28
R205 1K_0402_5%
Debug Port DG 1.2 PU 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

R209 @ 10K_0402_5% PCH_GPIO27

+3VS
R211 200K_0402_5% PCH_GPIO36
+3VALW_PCH
R214 @ 1K_0402_5% EC_SMI#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled

+3VS
R216 10K_0402_5% PCH_GPIO0
R218 10K_0402_5% PCH_GPIO1
R219 10K_0402_5% PCH_GPIO6
R220 10K_0402_5% PCH_GPIO16
R221 10K_0402_5% PCH_GPIO17
R522 10K_0402_5% PCH_GPIO38
12/13 Add
R222 10K_0402_5% PCH_GPIO34
R223 10K_0402_5% PCH_GPIO48
R225 10K_0402_5% PCH_GPIO49

+VCCSUS3_3
R227 10K_0402_5% PCH_GPIO12
R228 1K_0402_5% EC_LID_OUT#
R232 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.
CRB1.0 PU 10K to +3VALW

+VCCSUS3_3
R224 10K_0402_5% PCH_GPIO24
R226 @ 10K_0402_5%

Fan Tachometer Inputs
TACH1~7 only on server
can insted to GPIO

11/21 EDP@->POP

LVDS/eDP	GPIO71
LVDS	1
eDP	0

+3VS
R198 10K_0402_5% LVDS@
R201 10K_0402_5% EDP@
PCH_GPIO71
R199 10K_0402_5% CRM@
R203 10K_0402_5% MIM@
REC_MODE
R200 100K_0402_5% CRM@
R204 10K_0402_5% MIM@
SPI_WP1#_RPCH

U16F

No use PU 10K +3VS	PCH_GPIO0	T7	BMBUSY# / GPIO0
No use PU 10K +3VS	PCH_GPIO1	A42	TACH1 / GPIO1
No use PU 10K +3VS	PCH_GPIO6	H36	TACH2 / GPIO6
No use PU 10K +3VS	EC_SCI#	E38	TACH3 / GPIO7
No use PU 10K +3VALW	EC_SMI#	C10	GPIO8
No use PU +3VALW	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12
No use PU +3VALW	EC_LID_OUT#	G2	GPIO15
No use PU +3VS	PCH_GPIO16	U2	SATA4GP / GPIO16
No use PU +3VS	PCH_GPIO17	D40	TACH0 / GPIO17
No use PU 10K +3VS RAM flag	PCH_GPIO22	T5	SCLOCK / GPIO22
No use PU +3VALW DDR3/DDR3L	PCH_GPIO24	E8	GPIO24 / MEM_LED
No use PD 10K to GND	PCH_GPIO27	E16	GPIO27
No use PU 10K +3VALW	PCH_GPIO28	P8	GPIO28
No use PU 10K +3VS BT ON/OFF	PCH_GPIO34	K1	STP_PCI# / GPIO34
No use can NC	PCH_GPIO35	K4	GPIO35
Can't PU	PCH_GPIO36	V8	SATA2GP / GPIO36
Can't PU	PCH_GPIO37	M5	SATA3GP / GPIO37
No use PU 10K +3VS	PCH_GPIO38	N2	SLOAD / GPIO38
No use PU 10K +3VS RAM flag	PCH_GPIO39	M3	SDATAOUT0 / GPIO39
No use PU 10K +3VS	PCH_GPIO48	V13	SDATAOUT1 / GPIO48
SATA5GP&TEMP_ALERT# CRB PU 10K +3VS	PCH_GPIO49	V3	SATA5GP / GPIO49
No use PU +3VALW	PCH_GPIO57	D6	GPIO57

DEV_MODE <28,29> — CRM@ 0_0402_5% R239

PAD T20 @
PAD T21 @

GPIO

TACH4 / GPIO68	C40	PCH_GPIO68	PCH_GPIO68 <27>
TACH5 / GPIO69	B41	REC_MODE	
TACH6 / GPIO70	C41	SPI_WP1#_RPCH	SPI_WP1#_R <13,28,29,30>
TACH7 / GPIO71	A40	PCH_GPIO71	

D32 RB751V-40_SOD323-2 CRM@

CPU/MISC

A20GATE	P4		GATEA20 <29>
PECI	AU16	PCH_PECI_R	H_PECI <29,5>
RCIN#	P5	EC_KBRST#	EC_KBRST# <29>
PROCPWRGD	AY11		H_CPUPWRGD <5>
THRMTRIP#	AY10	PCH_THRMTRIP#_R	H_THRMTRIP# <5>
INIT3_3V#	T14		

R206 10K_0402_5%
0_0402_5% R207
R210 390_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut down

INIT3_3V Checklist1.5 P.69
This signal has weak internal
PU, can't pull low,leave NC

NC_1	AH8
NC_2	AK11
NC_3	AH10
NC_4	AK10
NC_5	P37

TS_VSS1~4
PD to GND

EC_KBRST# R212 10K_0402_5%
PCH_GPIO68 R213 10K_0402_5%

NCTF

VSS_NCTF_1	A4	BG2	VSS_NCTF_15
VSS_NCTF_2	A44	BG48	VSS_NCTF_16
VSS_NCTF_3	A45	BH3	VSS_NCTF_17
VSS_NCTF_4	A46	BH47	VSS_NCTF_18
VSS_NCTF_5	A5	BJ4	VSS_NCTF_19
VSS_NCTF_6	A6	BJ44	VSS_NCTF_20
VSS_NCTF_7	B3	BJ45	VSS_NCTF_21
VSS_NCTF_8	B47	BJ46	VSS_NCTF_22
VSS_NCTF_9	BD1	BJ5	VSS_NCTF_23
VSS_NCTF_10	BD49	BJ6	VSS_NCTF_24
VSS_NCTF_11	BE1	C2	VSS_NCTF_25
VSS_NCTF_12	BE49	C48	VSS_NCTF_26
VSS_NCTF_13	BF1	D1	VSS_NCTF_27
VSS_NCTF_14	BF49	D49	VSS_NCTF_28
		E1	VSS_NCTF_29
		E49	VSS_NCTF_30
		F1	VSS_NCTF_31
		F49	VSS_NCTF_32

9/15 Layout request remove Test point They will route by itself

9/15 Layout request remove Test point They will route by itself

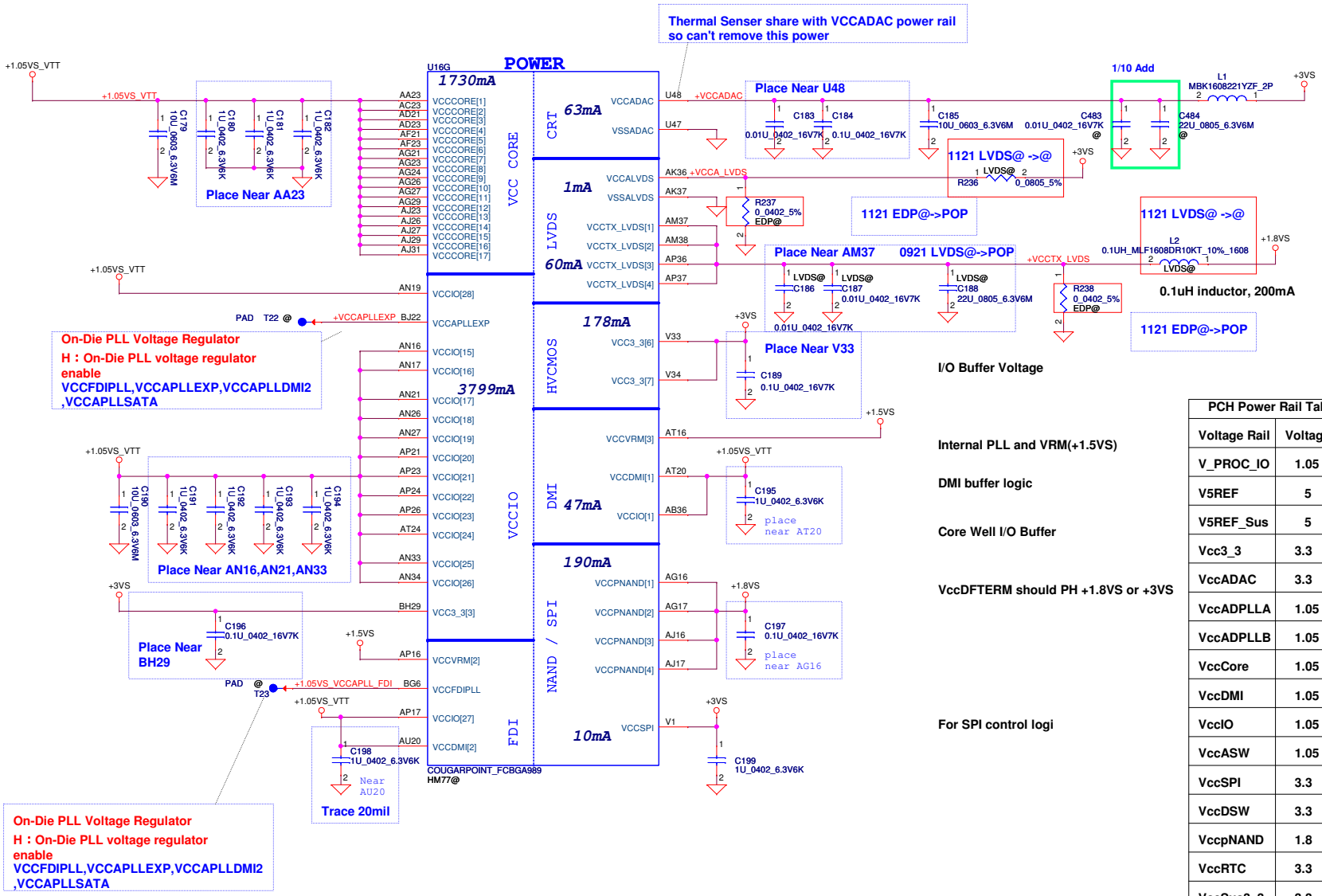
COUGARPOINT_FCBGA989
HM77@

+3VS
R229 10K_0402_5% PCH_GPIO39
R233 10K_0402_5% @
R231 10K_0402_5% PCH_GPIO22
R235 10K_0402_5% @

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.
Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom
Document Number: CHROME M/B LA-8943P Schematic
Rev: 0.1
Date: Friday, August 10, 2012
Sheet 18 of 45



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Buffer Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 19 of 45

VCC3_3 = 178mA detal waiting for newest spec
VCCDMI = 47mA detal waiting for newest spec

+1.05V analog internal clock PLL Can NC

Not support Deep S4,S5 connect to +3VALW

suppied by internal 1.05V VR must NC

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

SGA20331E10
330U 2V H1.9
9mohm POLY

isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG34)
18mil width(DIFFCLKN)
10mil (SSC)

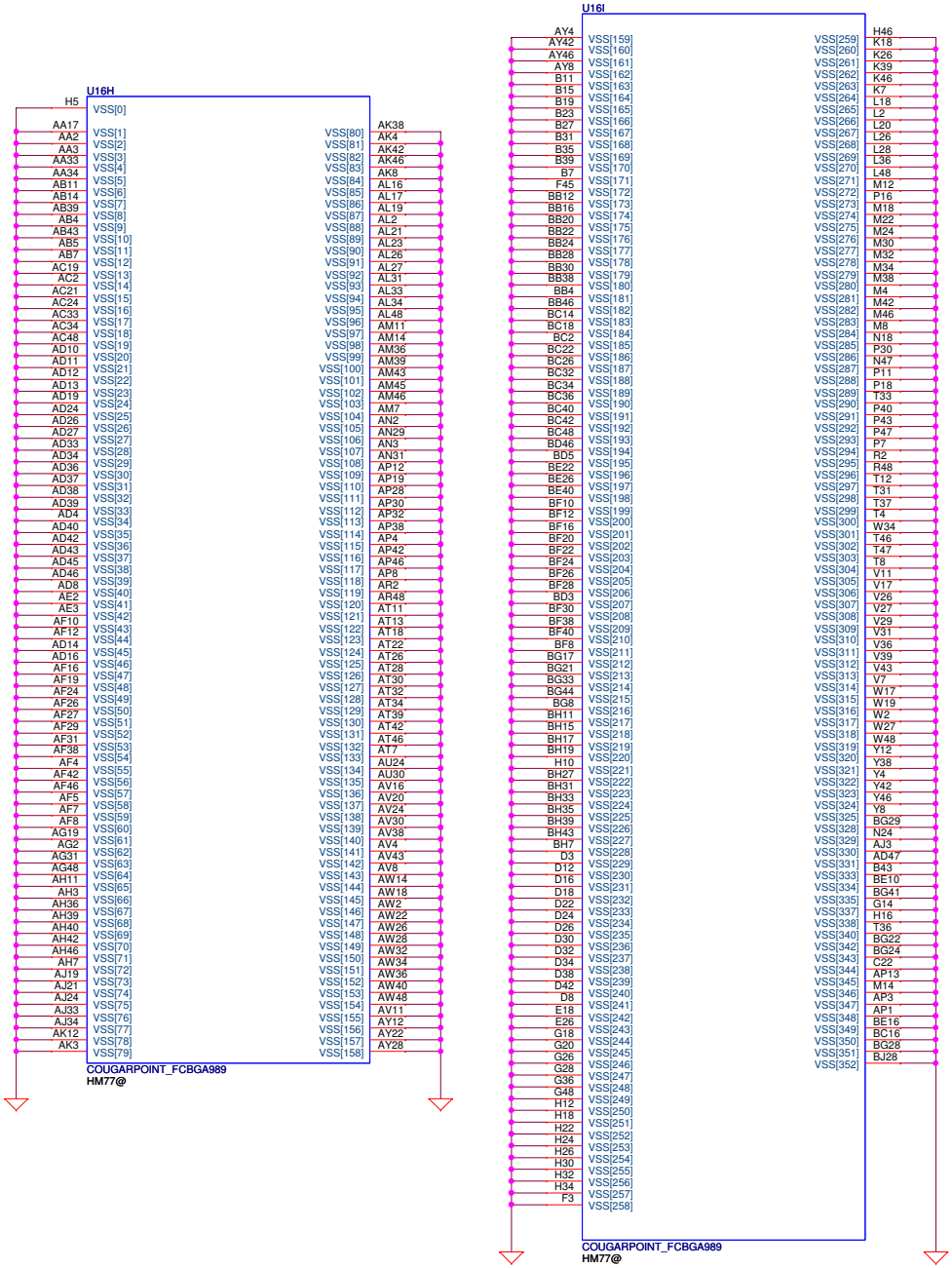
Need +3VALW and 0.1U close PCH

For Deep S3 turn off +V5REF_SUS,+VCCSUS3_3

U16J
COUGARPOINT_FCBGA989
HM77@

POWER
USB 65mA
Clock and Miscellaneous 803mA
PCI/GPIO/LPC 1mA
V5REF_SUS 1mA
V5REF 1mA
SATA 75mA 75mA
CPU 55mA 95mA 2mA
MISC
HDA 10mA
RTC

Near T38
Near T16
Near T23
Near T24
Near N26
Near M26
Near BD47
Near BF47
Near AA19
Near M6
Near N20
Near P34
Near AH13,AH14,AF13
Near AC16
Near V16
Near P32
Near A22
Place near AF17
Place near AG33
Place near AF33, AF34,AG34
Place near BJ8
Place near AJ2
Place near AA16,W16
Place near T34



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

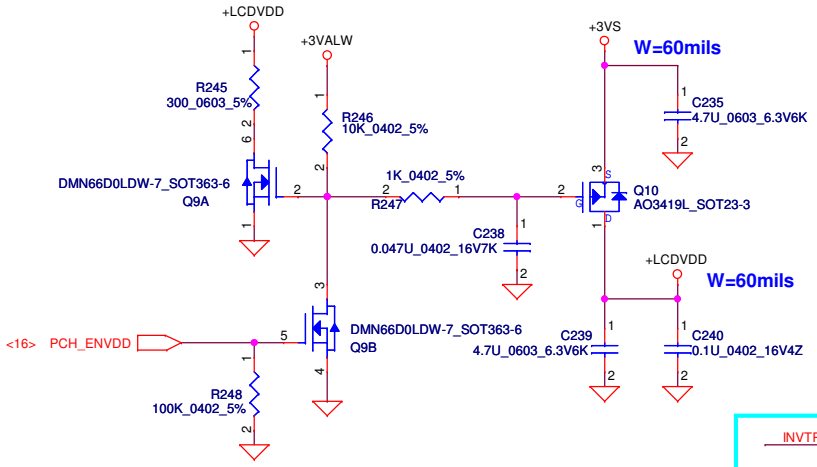
Compal Electronics, Inc.

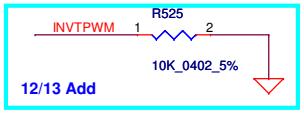
Title: **PCH (9/9) VSS**

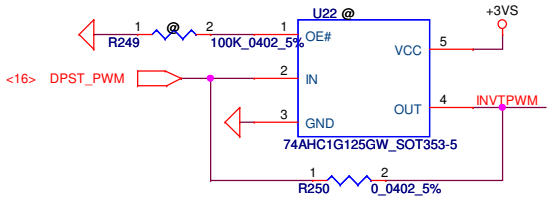
Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

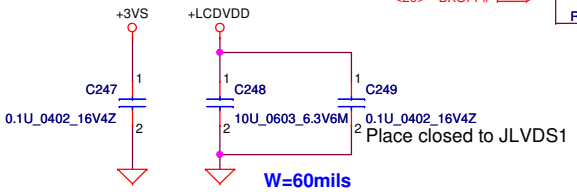
Date: Friday, August 10, 2012 | Sheet 21 of 45

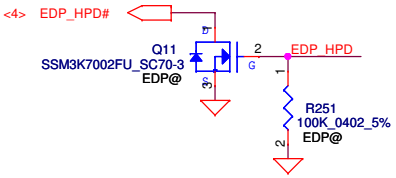
LCD POWER CIRCUIT

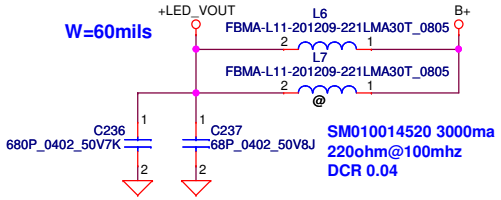




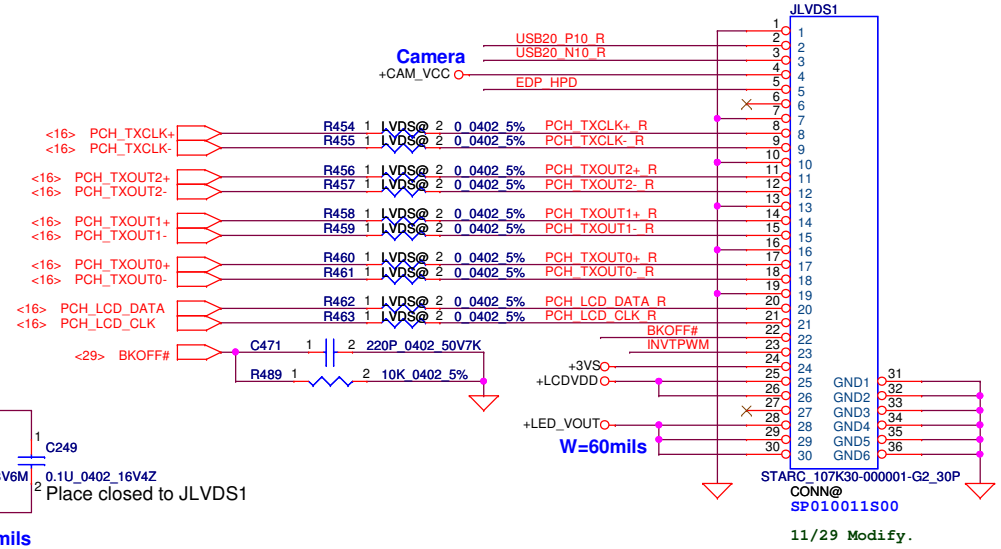




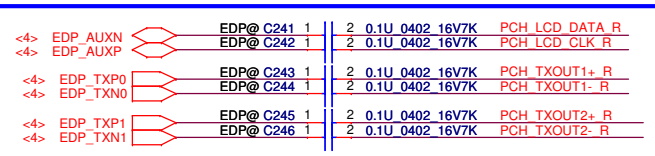




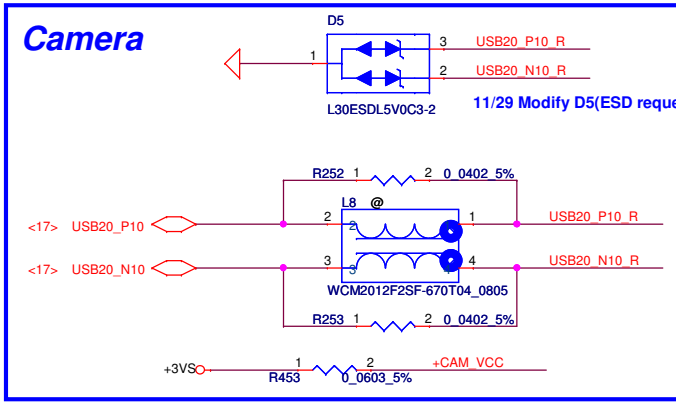
LCD/LED PANEL Conn.



eDP



Camera



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: LVDS&eDP

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 22 of 45

SM070001310 400ma 90ohm@100mhz DCR 0.3

R255 0_0603_5% W=40mils +5VS +HDMI_5V +HDMI_5V_OUT F1 1.1A_6V_SMD1812P110TF D6 RB491D-YS_SOT23-3 C250 0.1U_0402_16V4Z

<16> PCH_DPB_N0 C251 0.1U_0402_16V7K HDMI_TX2-
<16> PCH_DPB_P0 C252 0.1U_0402_16V7K HDMI_TX2+
<16> PCH_DPB_N1 C253 0.1U_0402_16V7K HDMI_TX1-
<16> PCH_DPB_P1 C254 0.1U_0402_16V7K HDMI_TX1+
<16> PCH_DPB_N2 C255 0.1U_0402_16V7K HDMI_TX0-
<16> PCH_DPB_P2 C256 0.1U_0402_16V7K HDMI_TX0+
<16> PCH_DPB_N3 C257 0.1U_0402_16V7K HDMI_CLK-
<16> PCH_DPB_P3 C258 0.1U_0402_16V7K HDMI_CLK+

HDMI_CLK+ R254 0_0402_5% HDMI_R_CK+ L9 WCM-2012-900T_0805 HDMI_CLK- R256 0_0402_5% HDMI_R_CK-
HDMI_TX0+ R257 0_0402_5% HDMI_R_D0+ L10 WCM-2012-900T_0805 HDMI_TX0- R258 0_0402_5% HDMI_R_D0-
HDMI_TX1+ R259 0_0402_5% HDMI_R_D1+ L11 WCM-2012-900T_0805 HDMI_TX1- R260 0_0402_5% HDMI_R_D1-
HDMI_TX2+ R261 0_0402_5% HDMI_R_D2+ L12 WCM-2012-900T_0805 HDMI_TX2- R263 0_0402_5% HDMI_R_D2-

HDMI_TX2- R264 680_0402_5% HDMI_GND
HDMI_TX2+ R265 680_0402_5%
HDMI_TX1- R266 680_0402_5%
HDMI_TX1+ R267 680_0402_5%
HDMI_TX0- R268 680_0402_5%
HDMI_TX0+ R270 680_0402_5%
HDMI_CLK- R271 680_0402_5%
HDMI_CLK+ R272 680_0402_5%

+3VS R262 1M_0402_5% <16> PCH_DPB_HPD Q12A DMN66D0LDW-7_SOT363-6 R269 100K_0402_5% HDMI_HPD C259 220P_0402_50V7K

+3VS DMN66D0LDW-7_SOT363-6 Q12B

3/1 Add (ESD request)
+3VS C492 0.1U_0402_16V4Z C493 @ 0.1U_0402_16V4Z

<28> HDMI_HPD R293 0_0402_5%

+HDMI_5V_OUT D7 RB751V-40_SOD323-2

+3VS R273 2.2K_0402_5% SDVO_SCLK
R274 2.2K_0402_5% SDVO_SDATA

+3VS R275 2.2K_0402_5% R276 2.2K_0402_5%

<16> SDVO_SCLK SDVO_SCLK Q13A DMN66D0LDW-7_SOT363-6 HDMI_SCLK
<16> SDVO_SDATA SDVO_SDATA Q13B DMN66D0LDW-7_SOT363-6 HDMI_SDATA

RF request
C260 @ 47P_0402_50V8J
C261 @ 47P_0402_50V8J

Place closed to JHDMI1

HDMI connector

JHDMI1

19	HP_DET		
18	+5V		
17	DDC/CEC_GND		
HDMI_SDATA 16	SDA		
HDMI_SCLK 15	SCL		
14	Reserved		
13	CEC		
HDMI_R_CK- 12	CK-	GND	20
11	CK_shield	GND	21
HDMI_R_CK+ 10	CK+	GND	22
HDMI_R_D0- 9	D0-	GND	23
8	D0_shield		
HDMI_R_D0+ 7	D0+		
HDMI_R_D1- 6	D1-		
5	D1_shield		
HDMI_R_D1+ 4	D1+		
HDMI_R_D2- 3	D2-		
2	D2_shield		
HDMI_R_D2+ 1	D2+		

HONGL_13-13201904CP_19P
CONN@
DC232001000

11/29 Modify.

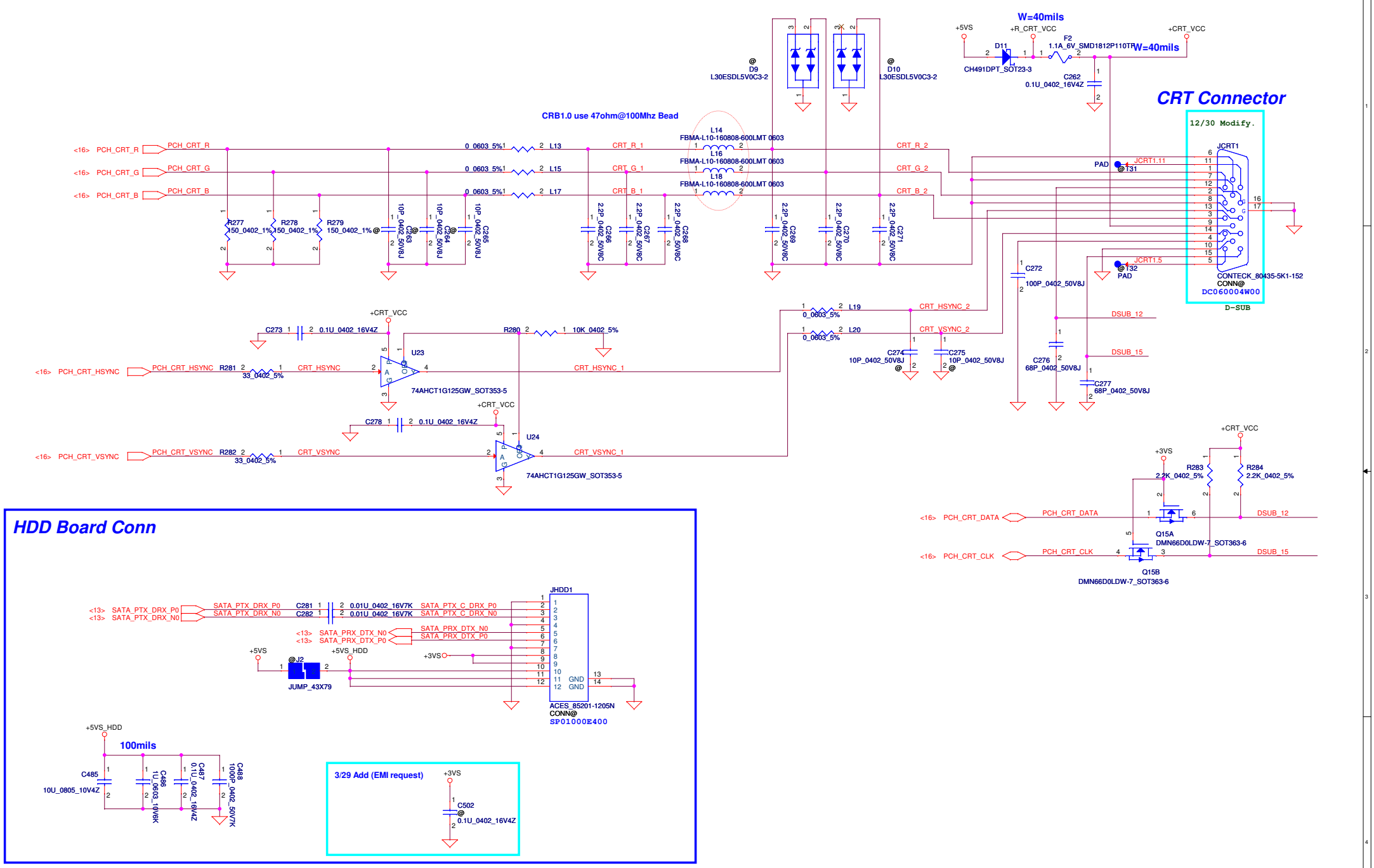
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: HDMI Conn

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 23 of 45



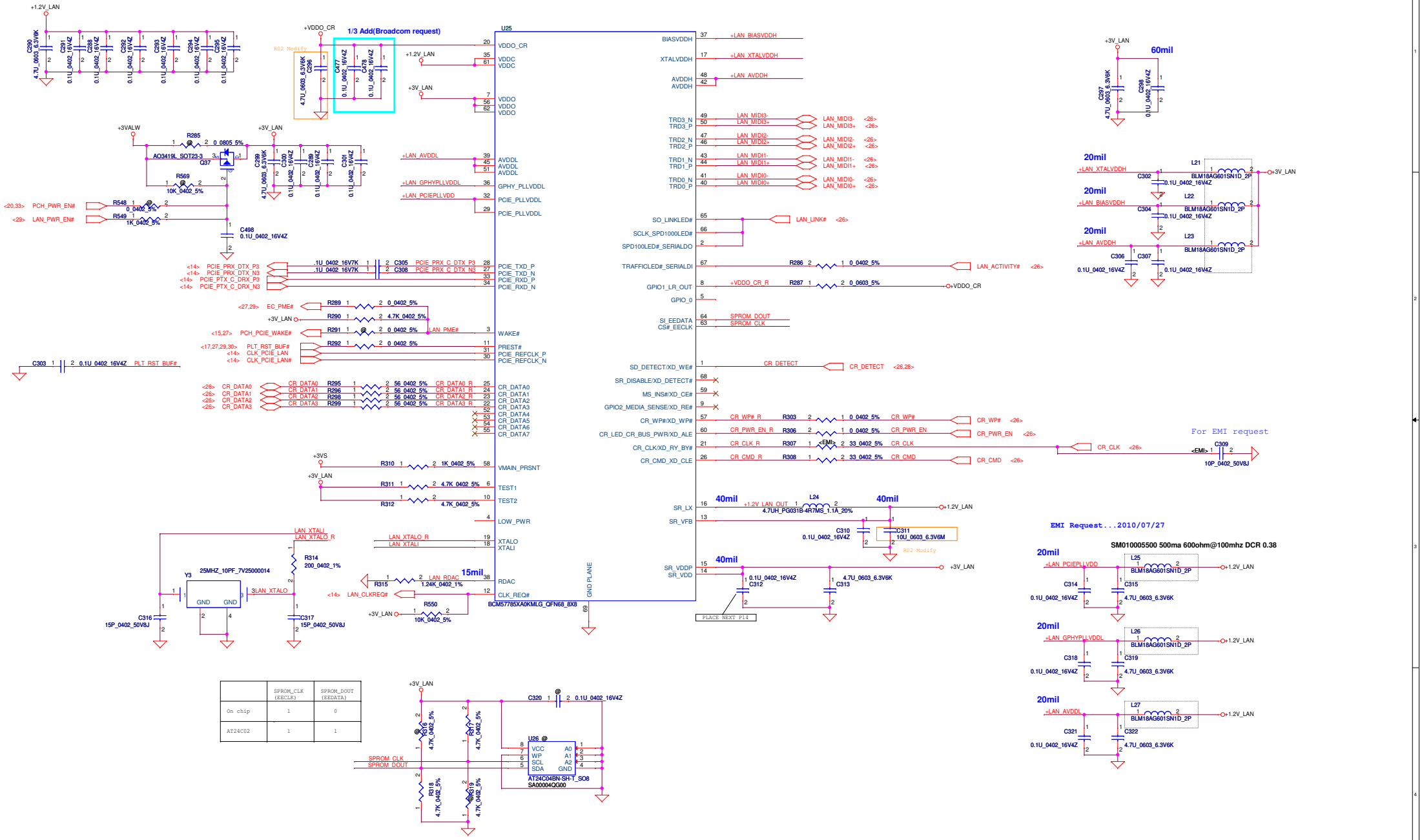
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: CRT&HDD Connector

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 24 of 45



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: LAN Boardcom 57785

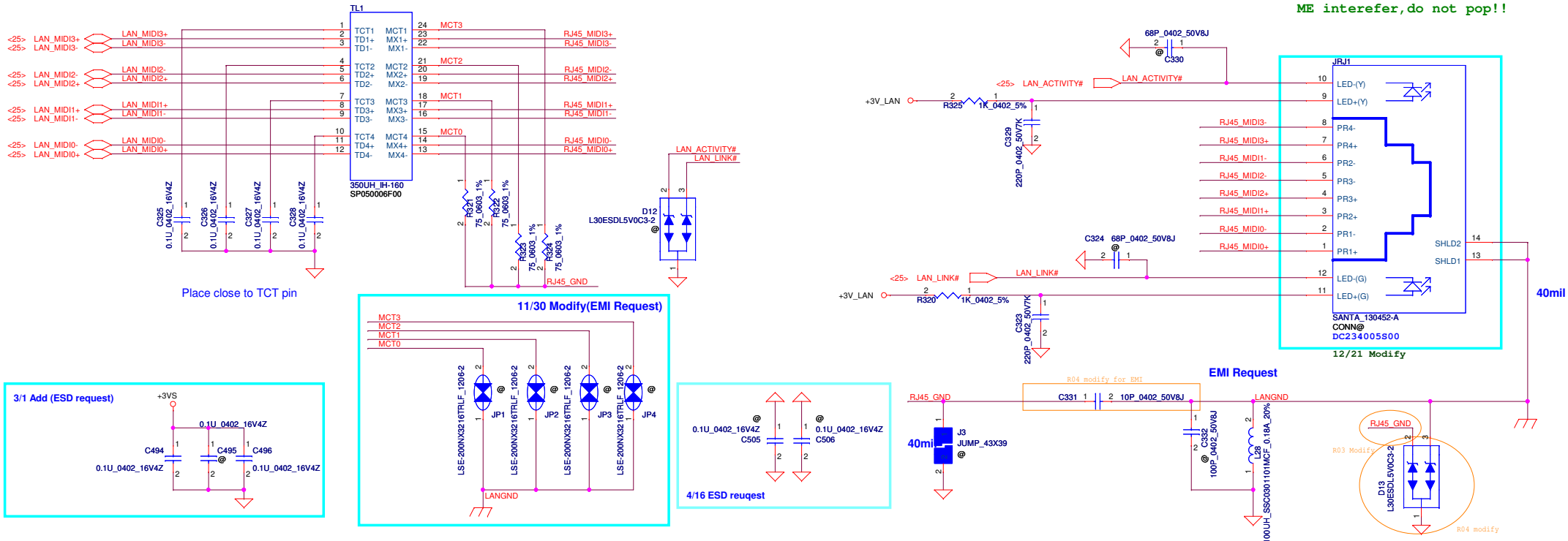
Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 25 of 45

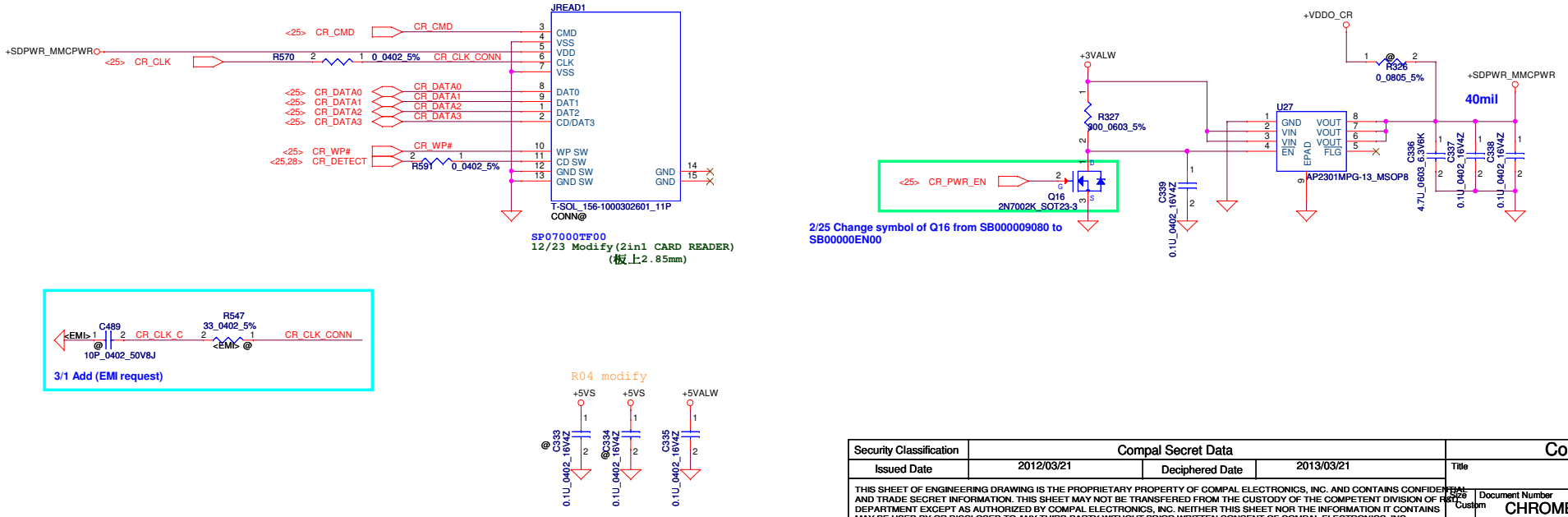
BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

LAN Connector

C474,C475 and D14
ME interefer,do not pop!!



Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

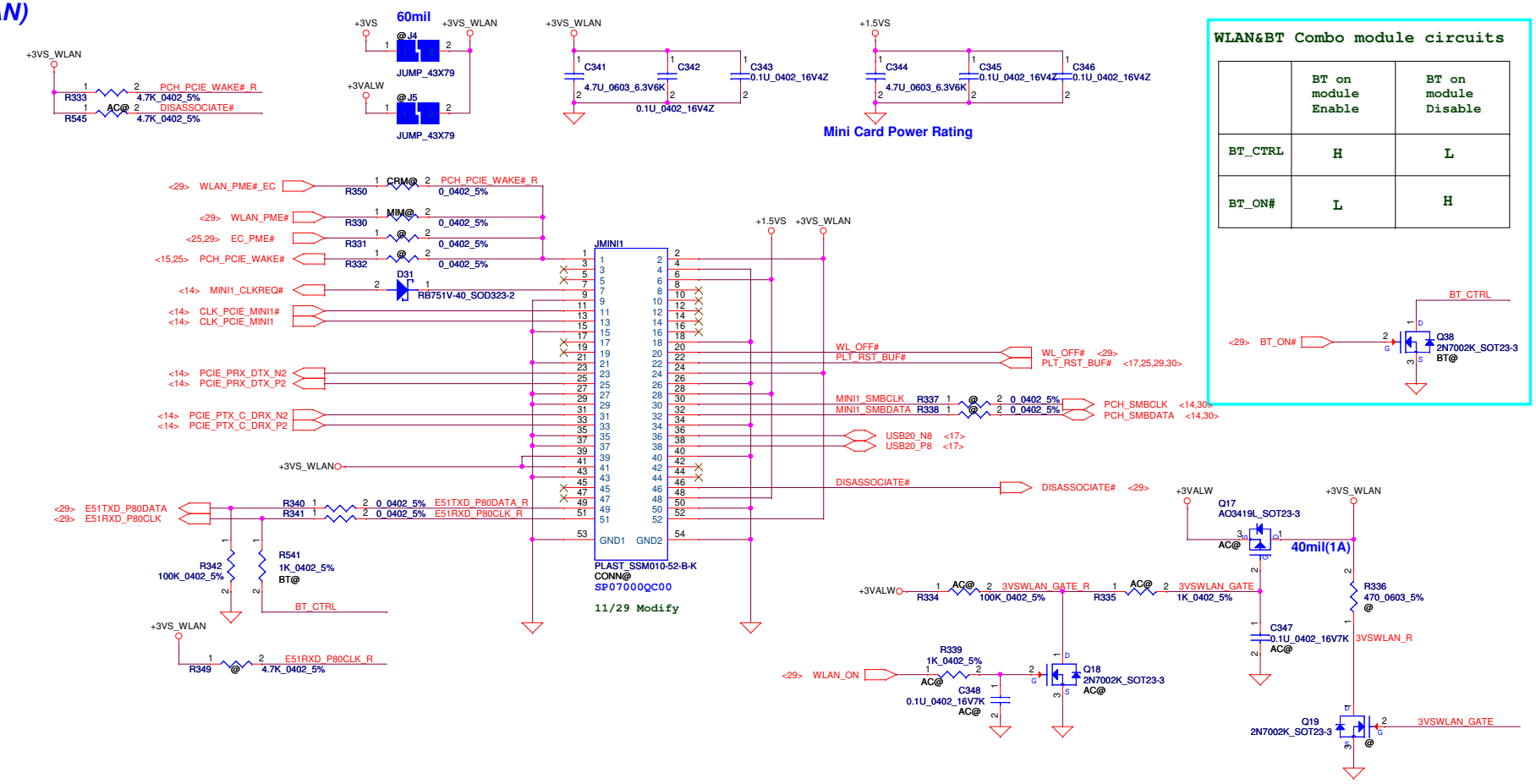
Compal Electronics, Inc.

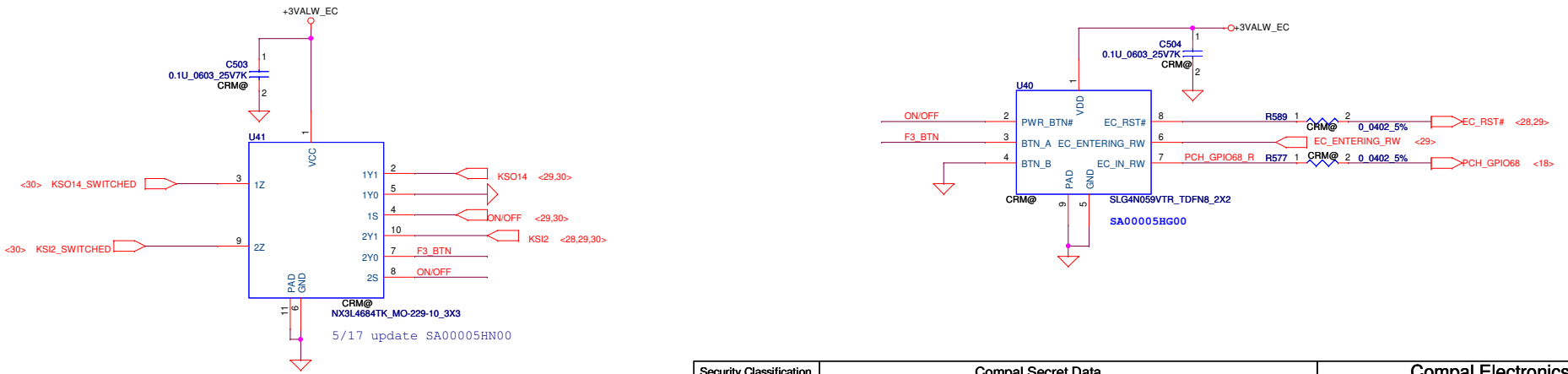
Title: Card Reader

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 26 of 45

MINI CARD(Wireless LAN)





Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

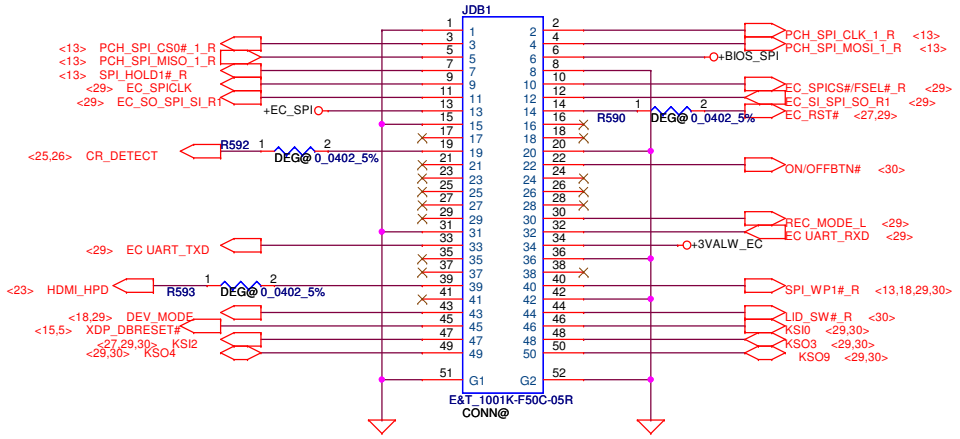
Compal Electronics, Inc.

Title: MINI CARD (WLAN)/Holeless RST

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

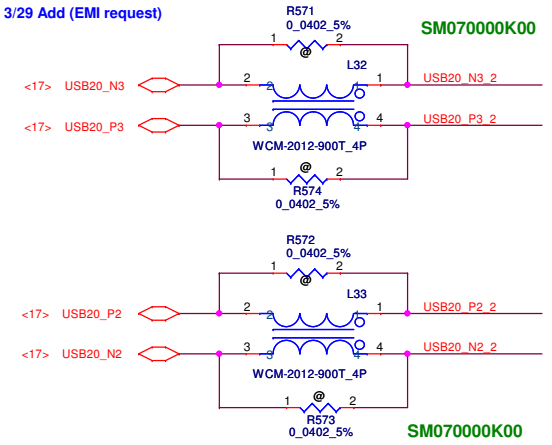
Date: Friday, August 10, 2012 | Sheet 27 of 45

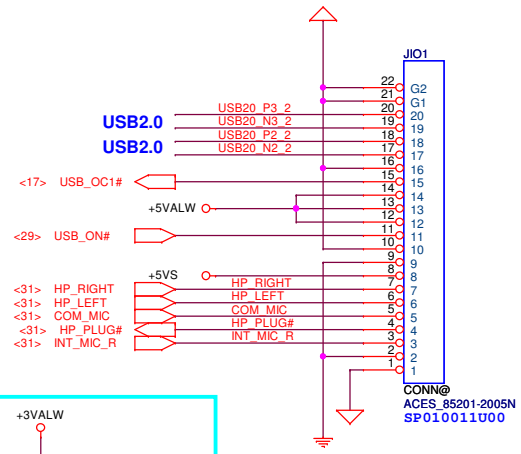
Debug Board



IO Board

3/29 Add (EMI request)

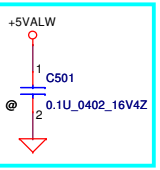




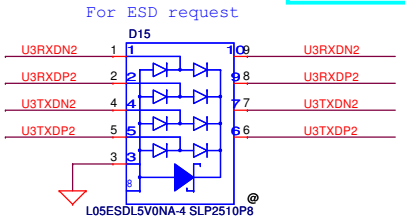
3/1 Add (ESD request)

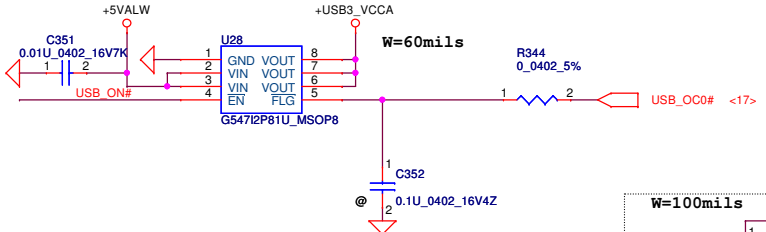
USB3.0

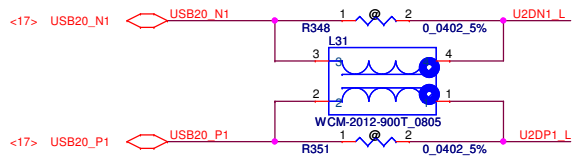
3/29 Add (ESD request)



For ESD request

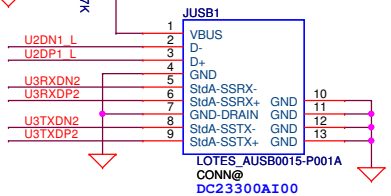




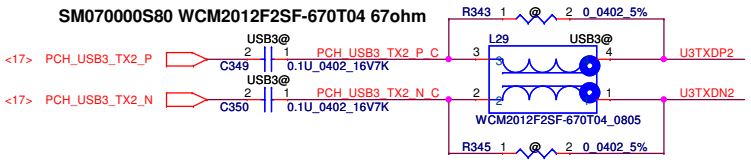


SM070001310 WCM2012F2SF-900T04 90ohm

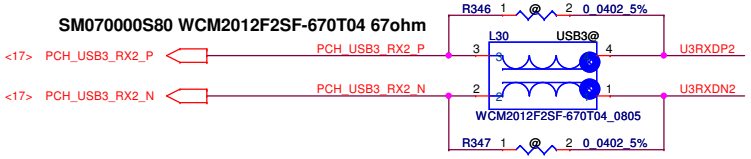
USB3.0 Conn.



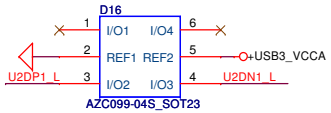
SM070000S80 WCM2012F2SF-670T04 67ohm



SM070000S80 WCM2012F2SF-670T04 67ohm



For USB2.0 ESD request

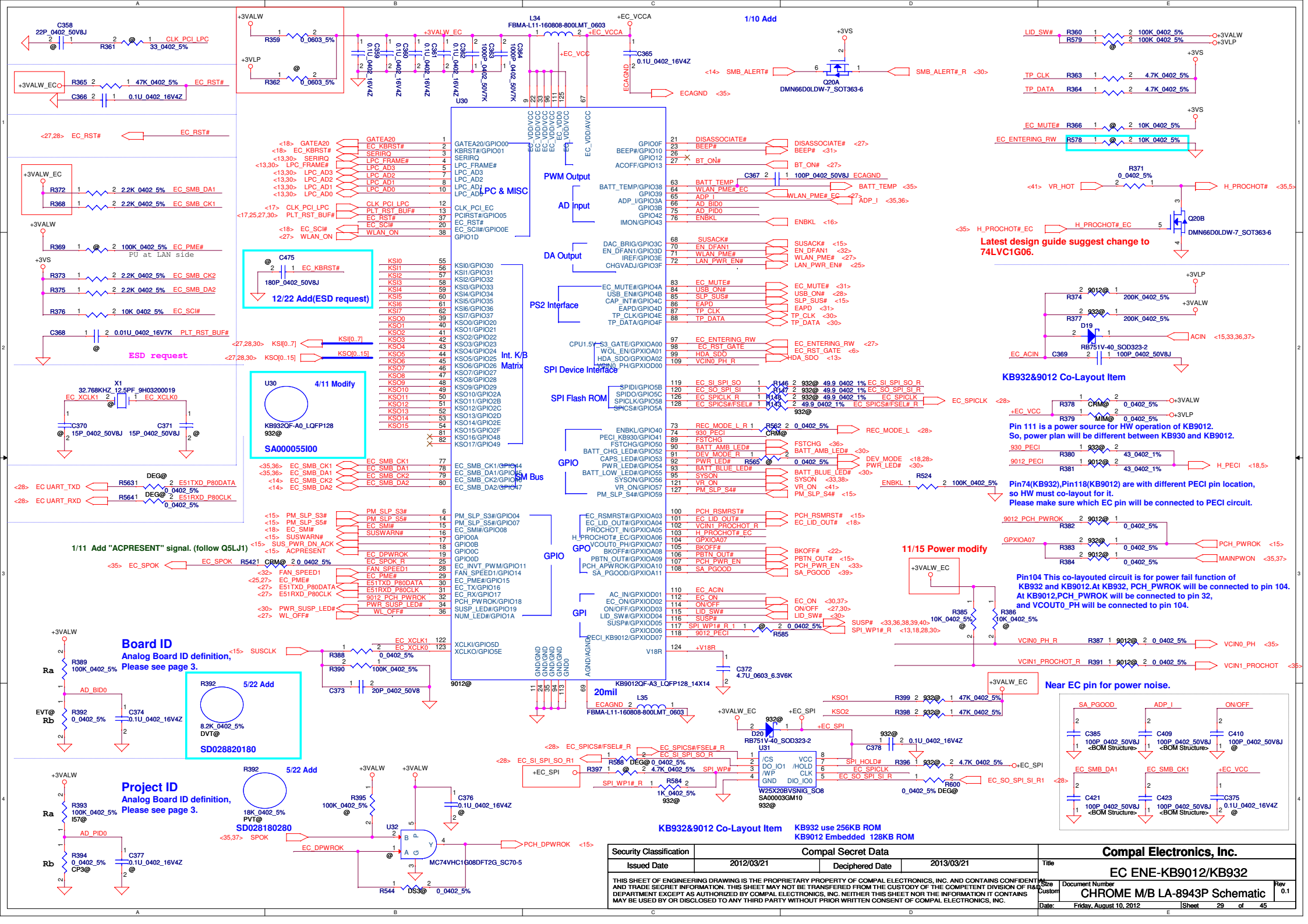


Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Title: IO Board & USB3.0

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 28 of 45



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.	
Title	EC ENE-KB9012/KB932
Size: Custom	Document Number: CHROME M/B LA-8943P Schematic
Rev	0.1
Date: Friday, August 10, 2012	Sheet 29 of 45

KB Conn.

JKB1 — ACES_85208-24071 CONN@ SP01000RY00

12/30 Modify.

KSI[0..7] KSO[0..15]

KSI2_SWITCHED R575 MIM@ 0_0402_5% KSI2 <27,28,29>

KSO14_SWITCHED R576 MIM@ 0_0402_5% KSO14 <27,29>

C381–C389, C390–C405 100P_0402_50V8J

C404

TPM

JTPM2 CONN@ — FOX_NQT510166-LOAO-7F

CLKRUN# PLT_RST_BUF# +3VALW +3VS

LPC_AD3 LPC_AD2 CLK_PCI_TPM_R_2 LPC_FRAME# LPC_AD1 LPC_AD0 LPC_PD# SERIRQ

R145 BTB@ 0_0402_5% CLK_PCI_TPM <17>

R540 BTB@ 10K_0402_5% +3VS LPC_PD#

@C481 22P_0402_50V8J @R546 33_0402_5% CLK_PCI_TPM_R_2

TP Conn.

JTP1 — ACES_87151-0807G CONN@

D21 AZ5125-02S.R7G_SOT23-3

D26 RB751V-40_SOD323-2 CRM@

R597 MIM@ 0_0402_5% +3V_TP

R598 CRM@ 0_0402_5% R543 10K_0402_5%

R599 CRM@ 0_0402_5%

R594 R595 R596 0_0402_5% SMB_ALERT#_R PCH_SMBCLK PCH_SMBDATA

TP_CLK TP_DATA +3V_TP

C406 0.1U_0402_16V4Z C407 C408 100P_0402_50V8J

Kill SW

R586 10K_0402_5% @ R587 10K_0402_5% @ +3VS +EC_SPI

R583 CRM@ 0_0402_5% SPI_WP1#_R

R566 1K_0402_1% CRM@ Q14 AO3419L_SOT23-3 @

R580 0_0402_5% @

R553 0_0402_5% CRM@ +3VALW

JP5 CONN@ — ACES_87212-02G0

Lid Switch(Hall Effect Switch)

R581 0_0402_5% R582 0_0402_5% @ +3VALW +3VLP

R526 47K_0402_5% D29 RB751V-40_SOD323-2 LID_SW#

U39 VDD OUTPUT GND — AH180WG-7_SC59-3

C472 0.1U_0402_16V4Z C473 10P_0402_50V8J

ON/OFF BTN

SW4 EVQPLMA15_4P

D22 BAV70W_SOT323-3

R408 100K_0402_5% 932@ R409 100K_0402_5% 9012@

ON/OFFBTN# ON/OFF 51ON#

Q22 SSM3K7002F_SC59-3 LID_SW#_R

Q7 2N7002K_SOT23-3 932@ EC_ON

R490 932@ 10K_0402_5%

For power button ESD request

D30 @ L30ESD24VC3-2_SOT23-3 12/22 Modify.

Power LED

(BLUE)

51_0402_5% R567 51_0402_5% R528 @

LED1 HT-191NB5-A168_BLUE PWR_LED#

10mil

LED Board

JLED1 — ACES_51524-0060N-001 CONN@

PWR_LED# PWR_SUSP_LED# BATT_BLUE_LED# BATT_AMB_LED#

SP010014M10

01/12 Change to ACES_51524-0060N-001 .

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

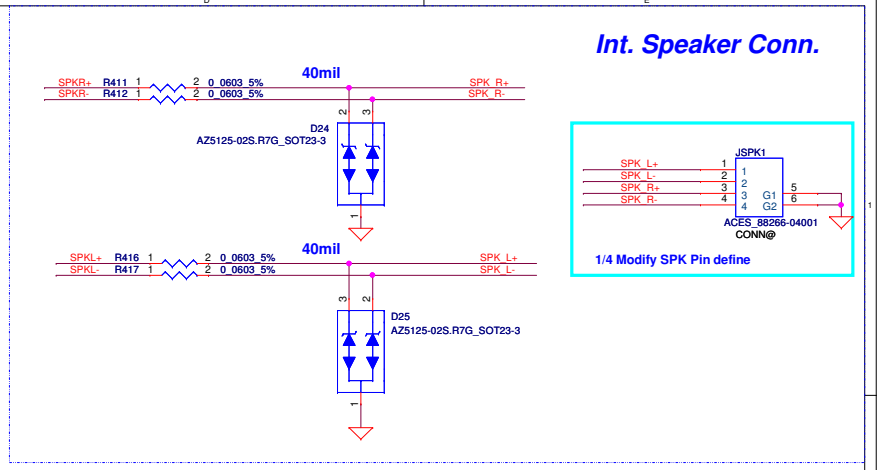
Title: TP/IO Port/ KB CONN/TPM

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

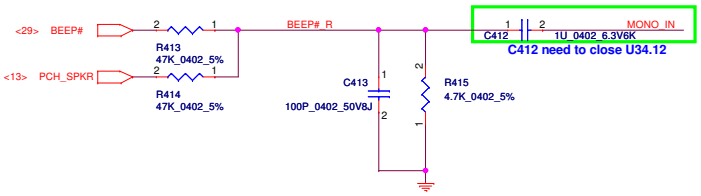
Date: Friday, August 10, 2012 | Sheet 30 of 45

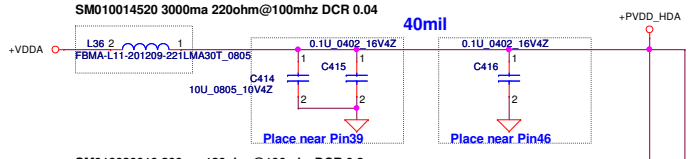
HD Audio Codec

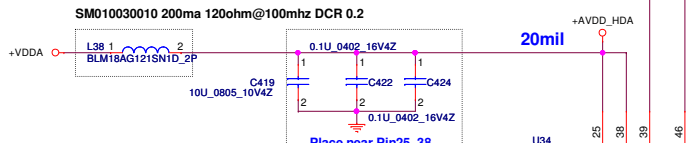
Int. Speaker Conn.

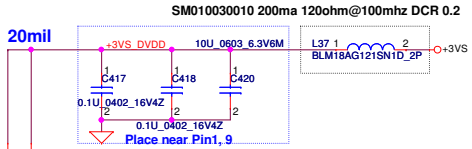


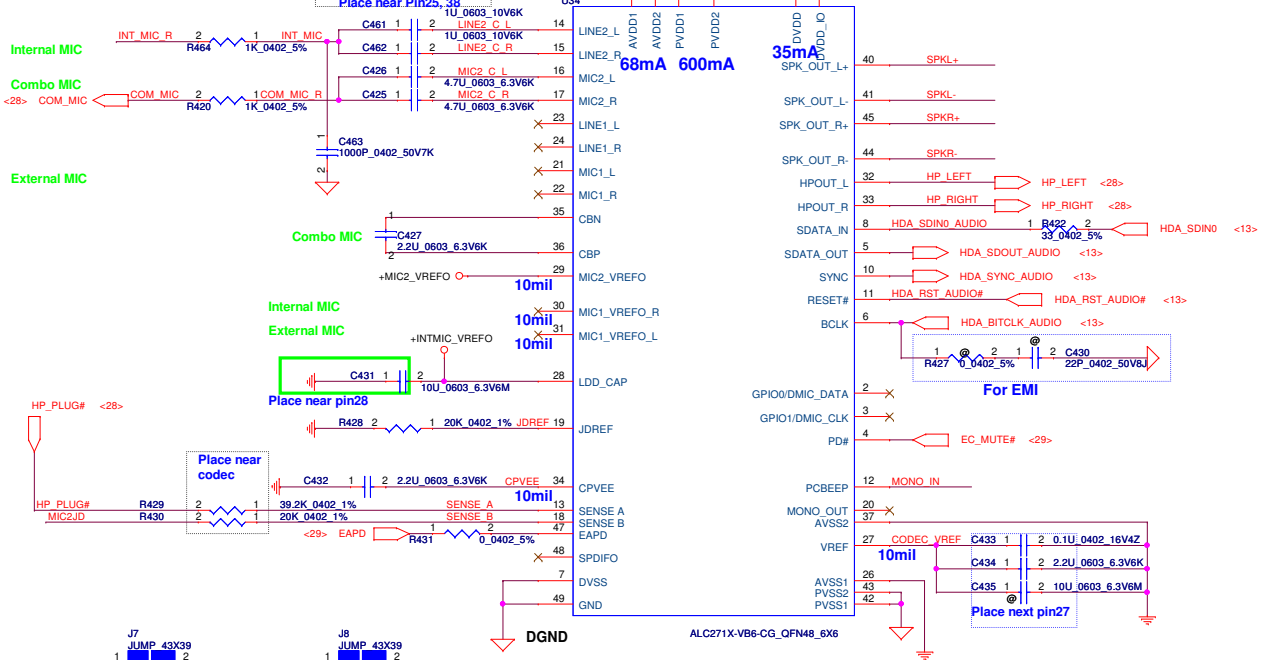
(output = 300 mA)

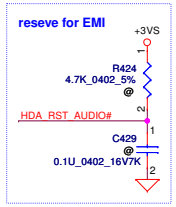


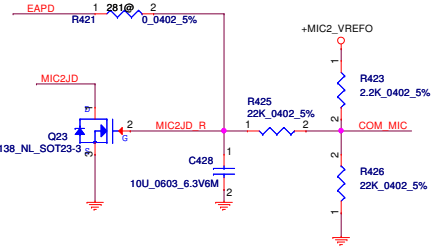


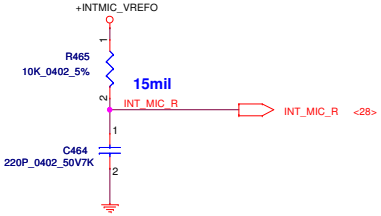


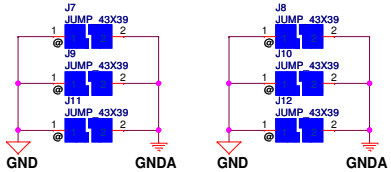












Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

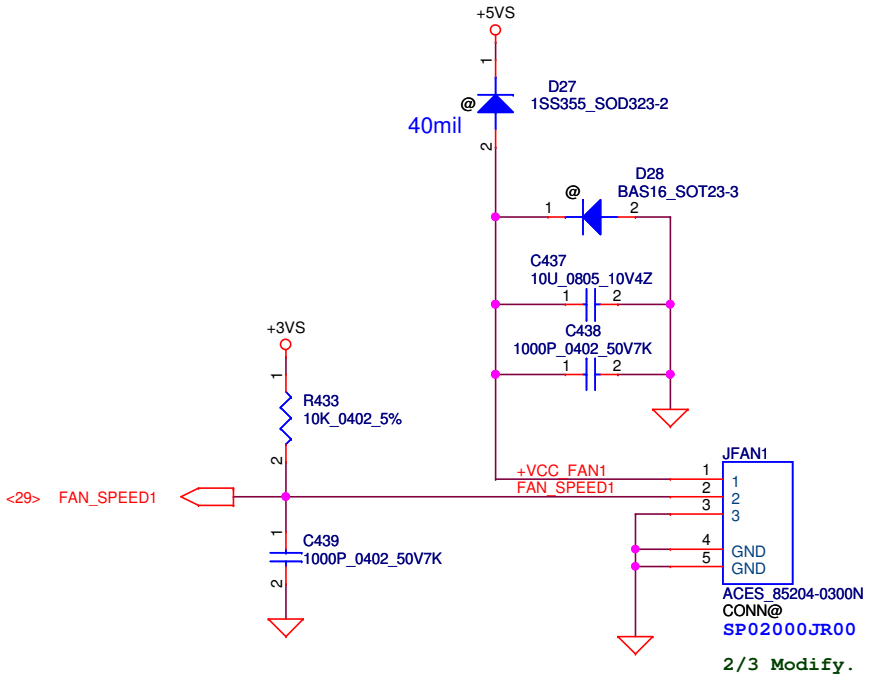
Compal Electronics, Inc.

Title: HD Audio Codec ALC271X

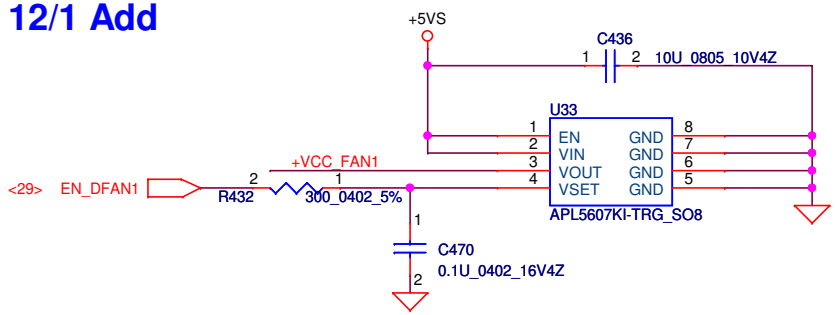
Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

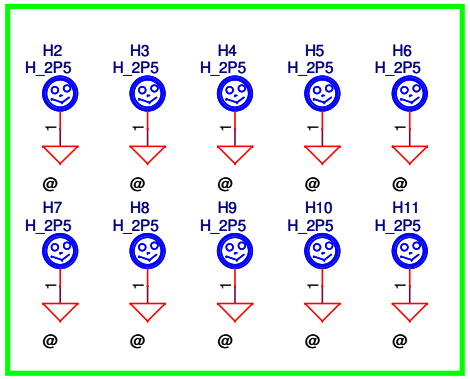
Date: Friday, August 10, 2012 | Sheet 31 of 45

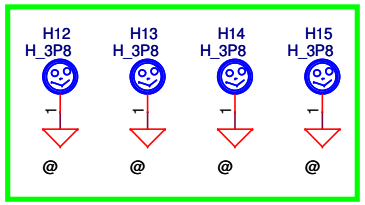
FAN1 Conn

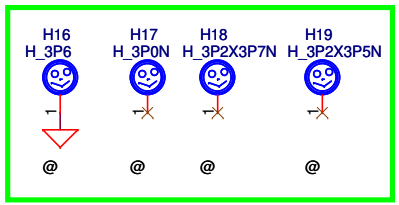


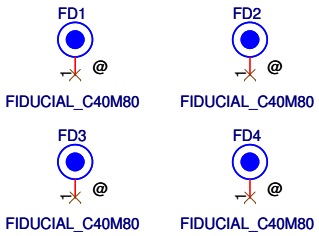
12/1 Add











CPU support plate

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

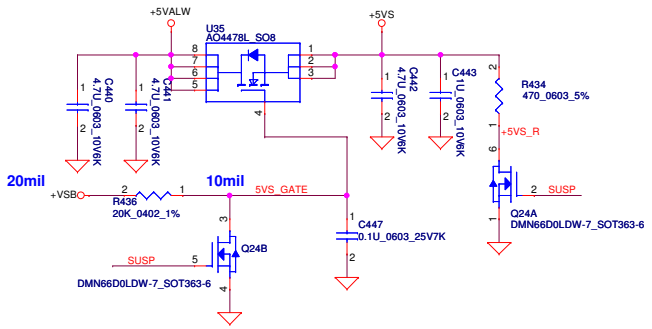
Compal Electronics, Inc.

Title: FAN & Screw Hole

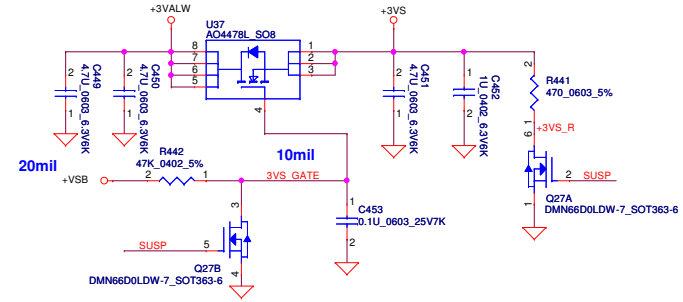
Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 32 of 45

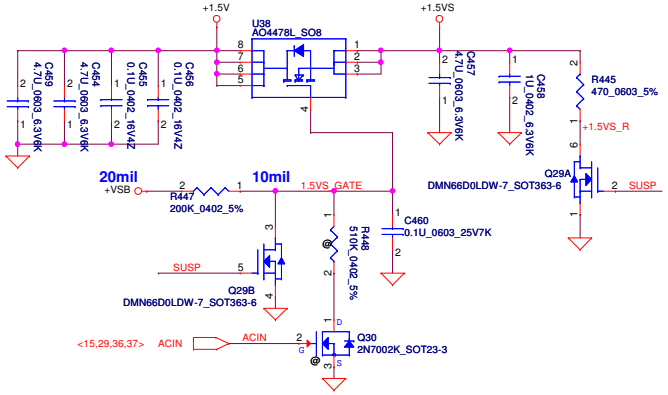
+5VALW TO +5VS

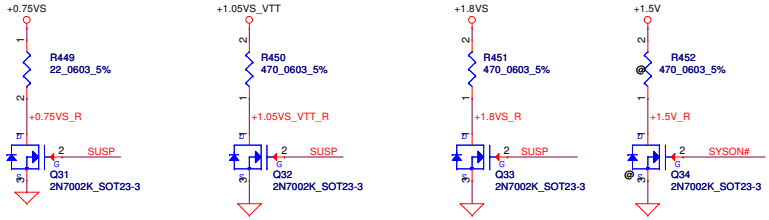


+3VALW TO +3VS

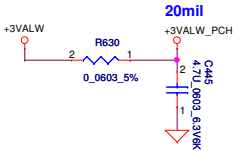


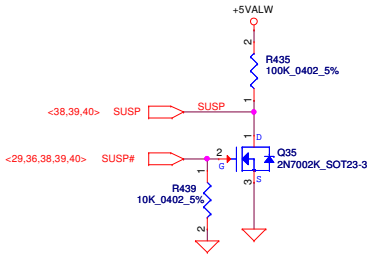
+1.5V to +1.5VS

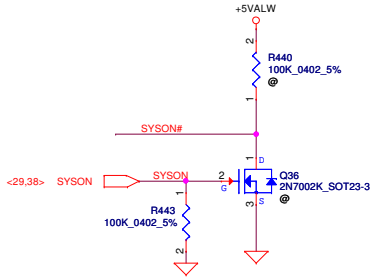


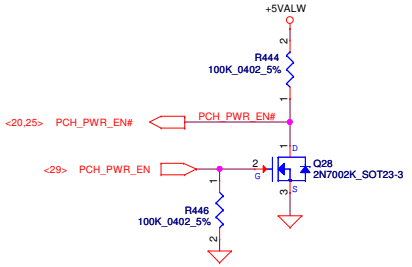


+3VALW to +3VALW_PCH(PCH AUX Power)









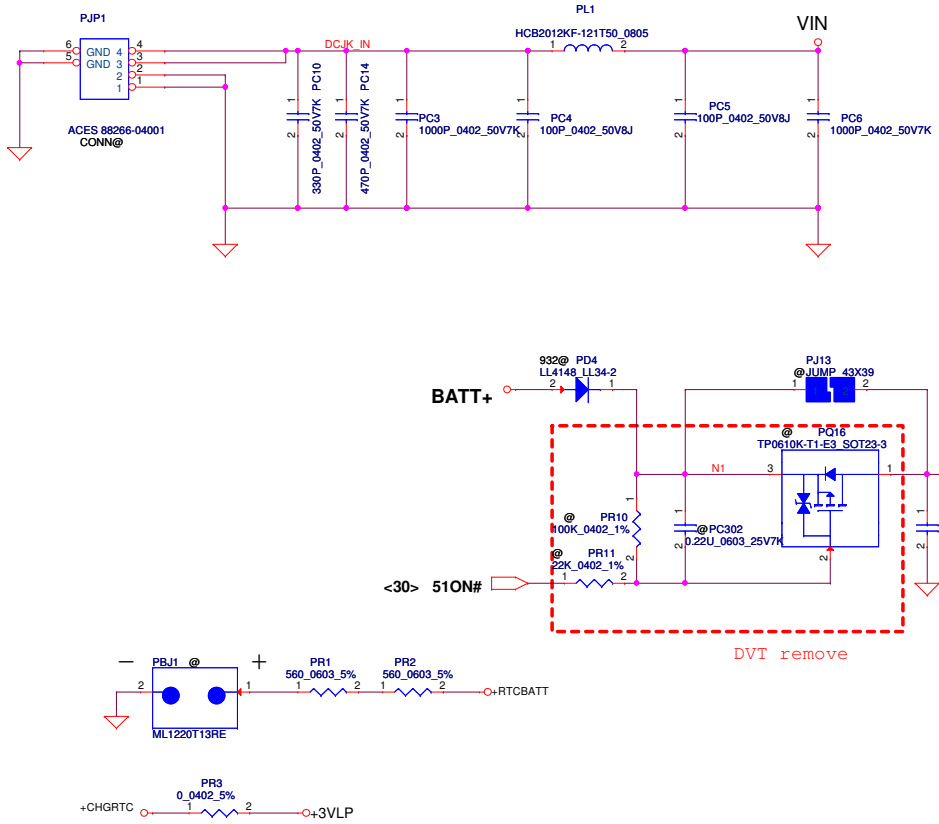
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 | Sheet 33 of 45



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	CHROME M/B LA-8942P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 34 of 46

footprint :SUYIN_200275MR008G15QZR_8P-T
PN:DC040007N10 SOCKET BATT C200275MR008G15QZR 8P W/FORK

@

PJP2

SUYIN_200275GR008G16MZR

<40,41> VMB

<40,41> BATT+

PJ5 @ JUMP_43X118

PC66 1000P_0402_50V7K

PC67 0.01U_0402_25V7K

PR60 1K_0402_5%

PR59 100_0402_1%

PR58 100_0402_1%

PR62 932@ 6.49K_0402_1%

PR111 @ 6.49K_0402_1%

PR65 1K_0402_1%

EC_SMDA

EC_SMCA

TH

BI+

EC_SMB_DA1 <29,36>

EC_SMB_CK1 <29,36>

+3VALW

+3VLP

BATT_TEMP <29>

Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
40W	42.88W	1.126V	33.2W	0.874V

+3VLP

PC65 0.1U_0603_25V7K

VL

@ PR64 100K_0402_1%

PU3 932@ G718TM1U_SOT23-8

VCC TMSNS1
GND RHYST1
~OT1 TMSNS2
~OT2 RHYST2

MAINPWON

932@ PR61 21.5K_0402_1%

932@ PR66 9.76K_0402_1%

+EC_VCCA

9012@ PR78 12.4K_0402_1%

9012@ PR63 5.62K +-1% 0402

PR63 932@ 590_0402_1%

ADP_I <29,36>

VCIN0_PH <29>

VCIN1_PROCHOT <29>

932@ PR68 1.91K_0402_1%

PH1 100K_0402_1%_NCP15WF104F03RC

PR79 10K_0402_1%

SD034100280 10K OHM

+3VLP +3VS

PR67 932@ 100K_0402_1%

PR110 @ 100K_0402_1%

932@ PQ32 2N7002KW_SOT323-3

PR105 0_0402_5% 9012@

<29,5> H_PROCHOT#

<29> H_PROCHOT#_EC

932@ PR80 0_0402_5%

9012@ PR81 0_0402_5%

<29> ECAGND

PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

PQ19 BSS84LT1G_SOT23-3

<29> EC_SPOK

B+

+VSBP

PR70 100K_0402_1%

PC68 0.22U_0603_25V7K

PC69 0.1U_0603_25V7K

PR71 22K_0402_1%

VL

PR72 100K_0402_1%

PR73 1K_0402_5%

<29,37> SPOK

PQ20 2N7002KW 1N SOT323-3

PC71 1U_0402_6.3V6K

+3VALW

@ PC70 0.1U_0603_25V7K

@PR74 10K_0402_1%

@PR75 10K_0402_1%

VL

@PR76 100K_0402_1%

@PU4 G718TM1U_SOT23-8

VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2

PH2_R

@PR77 47K_0402_1%

@PH2 100K_0402_1%_NCP15WF104F03RC

<29,37> MAINPWON

For 65W adapter==>action 70W , Recovery 54W

For 90W adapter==>action 97W , Recovery 75W

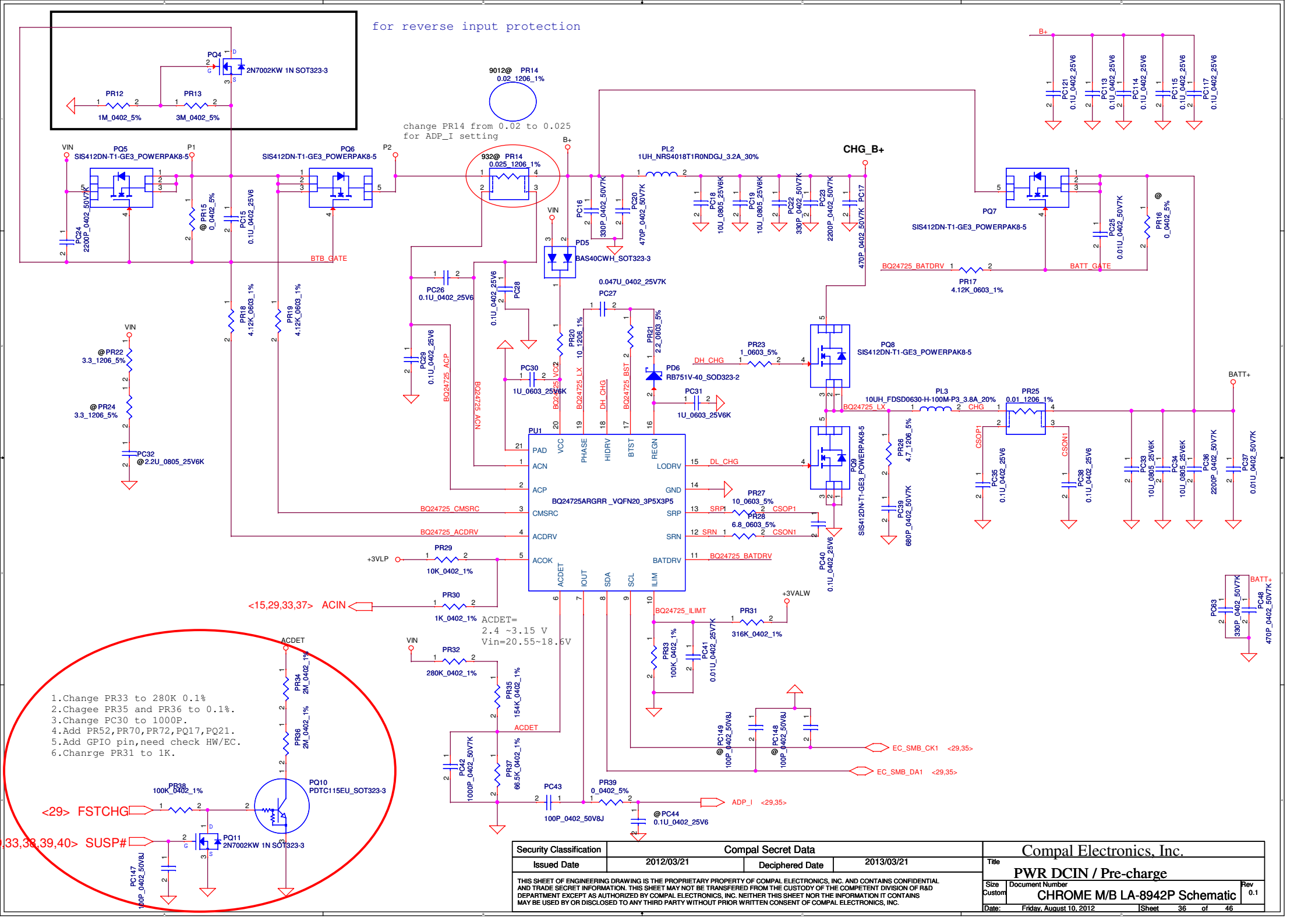
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 35 of 46



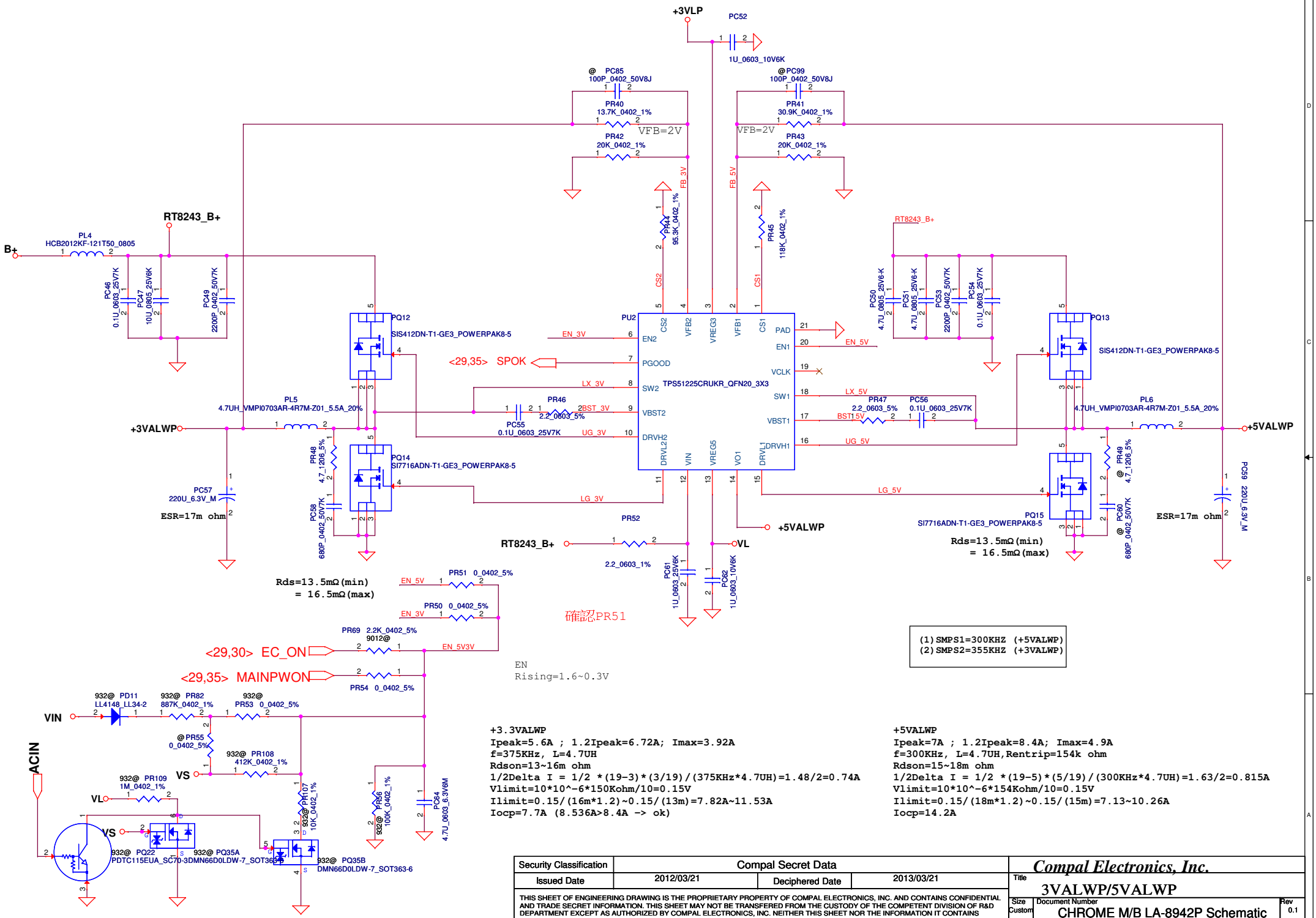
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 36 of 46



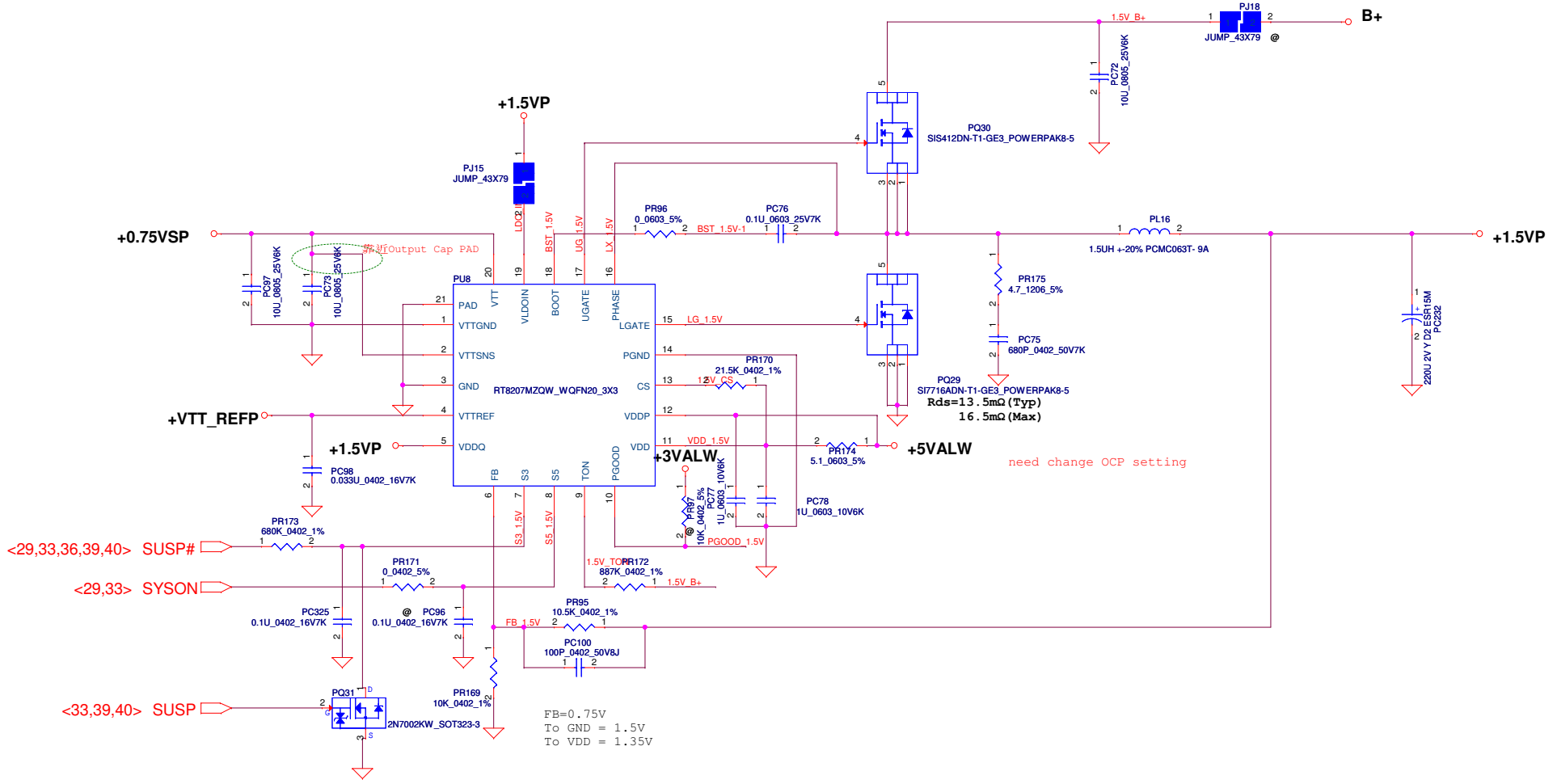
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 37 of 46



STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10.5K)=1.52V
Fsw=286K to 200KHz

Cout ESR=17m ohm Rdson(max)=16.5 mohm Rdson(typ)=13.5 mohm.
Ipeak=12 A, Imax=8.4A, Iocp=14.4A

Delta I=((Vin-Vo)*(Vo/Vin))/(L*Fsw)=2.195A
=>1/2Delta I=1.099A

Iocpmax=((21.5K*11uA)/0.0135)+0.5 delta I= A
Iocpmin=((21.5K*9uA)/(0.0165))+0.5 delta I=15.6A

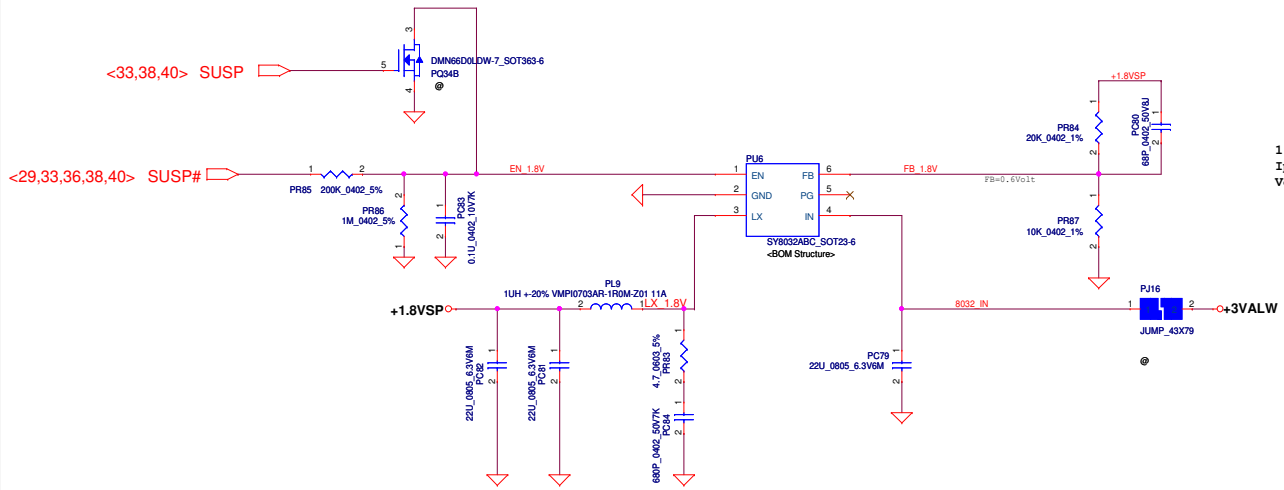
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

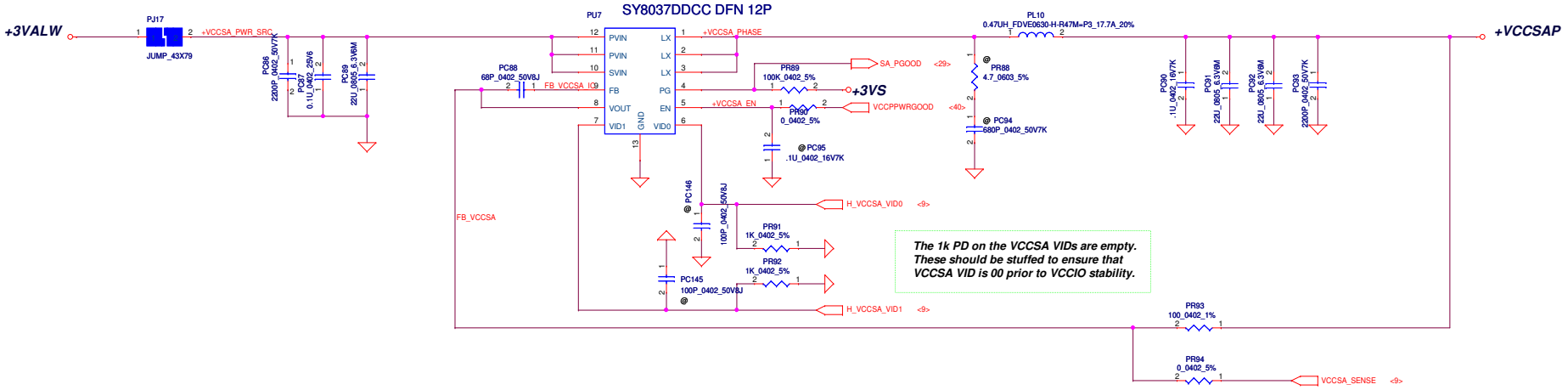
Title: PWR-+1.5VP

Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 38 of 46



1.8VSP
Ipeak=1.24A
Vout=0.6*(1+(20K/10K))=1.8V



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout(ULV only)
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

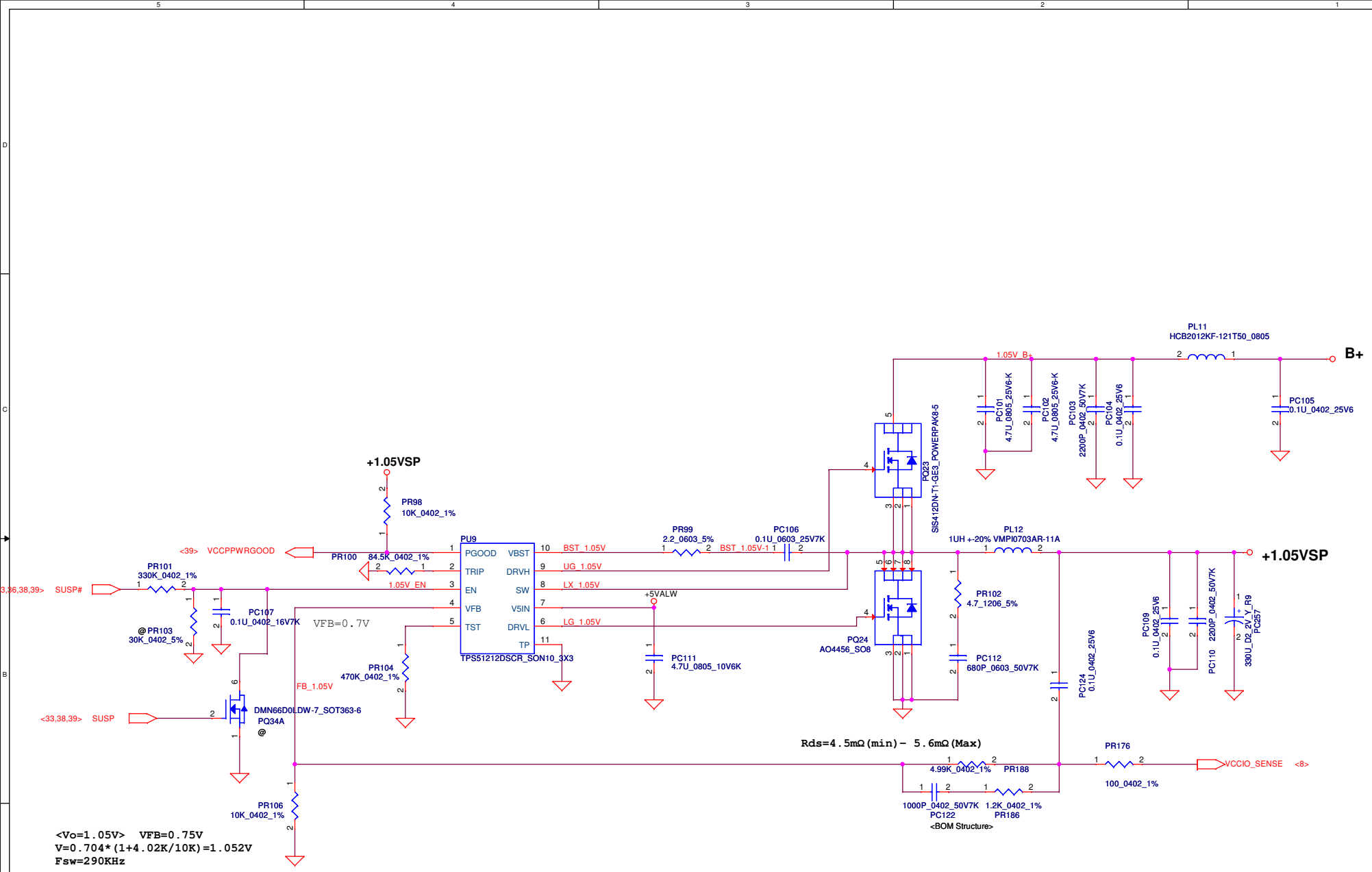
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	CHROME M/B LA-8942P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 39 of 46



<Vo=1.05V> VFB=0.75V
V=0.704*(1+4.02K/10K)=1.052V
Fsw=290KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=15.6A, Imax=10.92A, Iocp=18.72A

Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.06A

Iocpmax=((15K*11uA)/0.0045)+1.665A=23.54A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=19A
Iocp=A

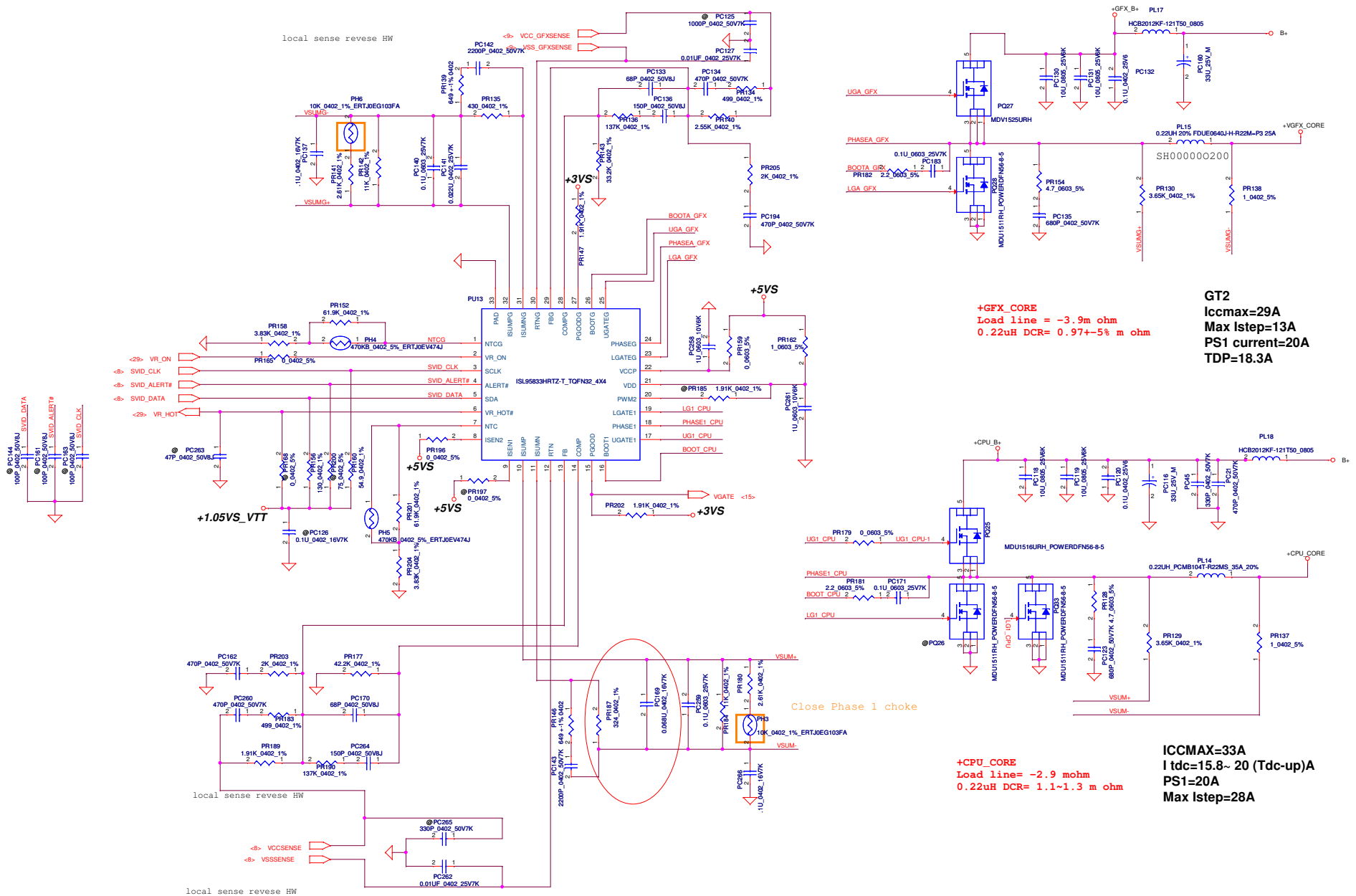
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	CHROME M/B LA-8942P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 40 of 46



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.			
Title	CPU/GFX_CORE		
Document Number	CHROME M/B LA-8942P Schematic		Rev 0.1
Date: Friday, August 10, 2012	Sheet 41 of 46		

CR PDDG Rev 0.95

+CPU_CORE

Mid-Frequency Decoupling 12x22µF

PC150 22U_0805_6.3V6M
PC151 22U_0805_6.3V6M
PC152 22U_0805_6.3V6M
PC153 22U_0805_6.3V6M
PC154 22U_0805_6.3V6M
PC155 22U_0805_6.3V6M
PC156 22U_0805_6.3V6M
PC157 22U_0805_6.3V6M
PC234 22U_0805_6.3V6M
PC233 22U_0805_6.3V6M
PC158 22U_0805_6.3V6M
PC159 22U_0805_6.3V6M

Low-Frequency Decoupling 3x330 µF 9m

PC179 330U_D2_2V_Y
PC180 330U_D2_2V_Y
@ PC181 330U_D2_2V_Y
PC182 330U_D2_2V_Y

+CPU_CORE

PC186 2.2U_0402_6.3V6M
PC187 2.2U_0402_6.3V6M
PC188 2.2U_0402_6.3V6M
PC189 2.2U_0402_6.3V6M
PC190 2.2U_0402_6.3V6M
PC191 2.2U_0402_6.3V6M
PC192 2.2U_0402_6.3V6M
PC193 2.2U_0402_6.3V6M
PC74 330P_0402_50V7K
PC108 470P_0402_50V7K

PC195 2.2U_0402_6.3V6M
PC196 2.2U_0402_6.3V6M
PC197 2.2U_0402_6.3V6M
PC198 2.2U_0402_6.3V6M
PC199 2.2U_0402_6.3V6M
PC200 2.2U_0402_6.3V6M
PC201 2.2U_0402_6.3V6M
PC202 2.2U_0402_6.3V6M

High-Frequency Decoupling 16x2.2µF

+VGFX_CORE

Mid-Frequency Decoupling 6x22µF

+VGFX_CORE

PC164 22U_0805_6.3V6M
PC165 22U_0805_6.3V6M
PC166 22U_0805_6.3V6M
PC167 22U_0805_6.3V6M
PC168 22U_0805_6.3V6M
PC172 22U_0805_6.3V6M

PC173 10U_0603_6.3V6M
PC174 10U_0603_6.3V6M
PC175 10U_0603_6.3V6M
PC176 10U_0603_6.3V6M
PC177 10U_0603_6.3V6M
PC178 10U_0603_6.3V6M

Mid-Frequency Decoupling 6x10µF 0603

PC184 330U_D2_2V_Y
PC185 330U_D2_2V_Y

Low-Frequency Decoupling 2x330 µF 9m

PC204 1U_0402_6.3V6K
PC205 1U_0402_6.3V6K
PC206 1U_0402_6.3V6K
PC207 1U_0402_6.3V6K
PC208 1U_0402_6.3V6K
PC209 1U_0402_6.3V6K

High-Frequency Decoupling 11x1µF

PC219 1U_0402_6.3V6K
PC220 1U_0402_6.3V6K
PC221 1U_0402_6.3V6K
PC222 1U_0402_6.3V6K
PC223 1U_0402_6.3V6K

+1.05VS_VTT

High-Frequency Decoupling 27x1µF

PC254 1U_0402_6.3V6K
PC238 1U_0402_6.3V6K
PC239 1U_0402_6.3V6K
PC240 1U_0402_6.3V6K
PC236 1U_0402_6.3V6K
PC237 1U_0402_6.3V6K
PC231 1U_0402_6.3V6K
PC230 1U_0402_6.3V6K
PC235 1U_0402_6.3V6K
PC229 1U_0402_6.3V6K
PC228 1U_0402_6.3V6K
PC226 1U_0402_6.3V6K
PC225 1U_0402_6.3V6K
PC227 1U_0402_6.3V6K

PC253 1U_0402_6.3V6K
PC252 1U_0402_6.3V6K
PC251 1U_0402_6.3V6K
PC249 1U_0402_6.3V6K
PC250 1U_0402_6.3V6K
PC248 1U_0402_6.3V6K
PC246 1U_0402_6.3V6K
PC247 1U_0402_6.3V6K
PC245 1U_0402_6.3V6K
PC243 1U_0402_6.3V6K
PC241 1U_0402_6.3V6K
PC242 1U_0402_6.3V6K
PC244 1U_0402_6.3V6K

+1.05VS_VTT

Mid-Frequency Decoupling 10x10µF

PC224 10U_0603_6.3V6M
PC218 10U_0603_6.3V6M
PC217 10U_0603_6.3V6M
PC216 10U_0603_6.3V6M
PC215 10U_0603_6.3V6M
PC214 10U_0603_6.3V6M
PC213 10U_0603_6.3V6M
PC212 10U_0603_6.3V6M
PC211 10U_0603_6.3V6M
PC210 10U_0603_6.3V6M

PC203 330U_D2_2V_Y

Low-Frequency Decoupling 1x330 µF 9m

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 42 of 46

Version change list (P.I.R. List)

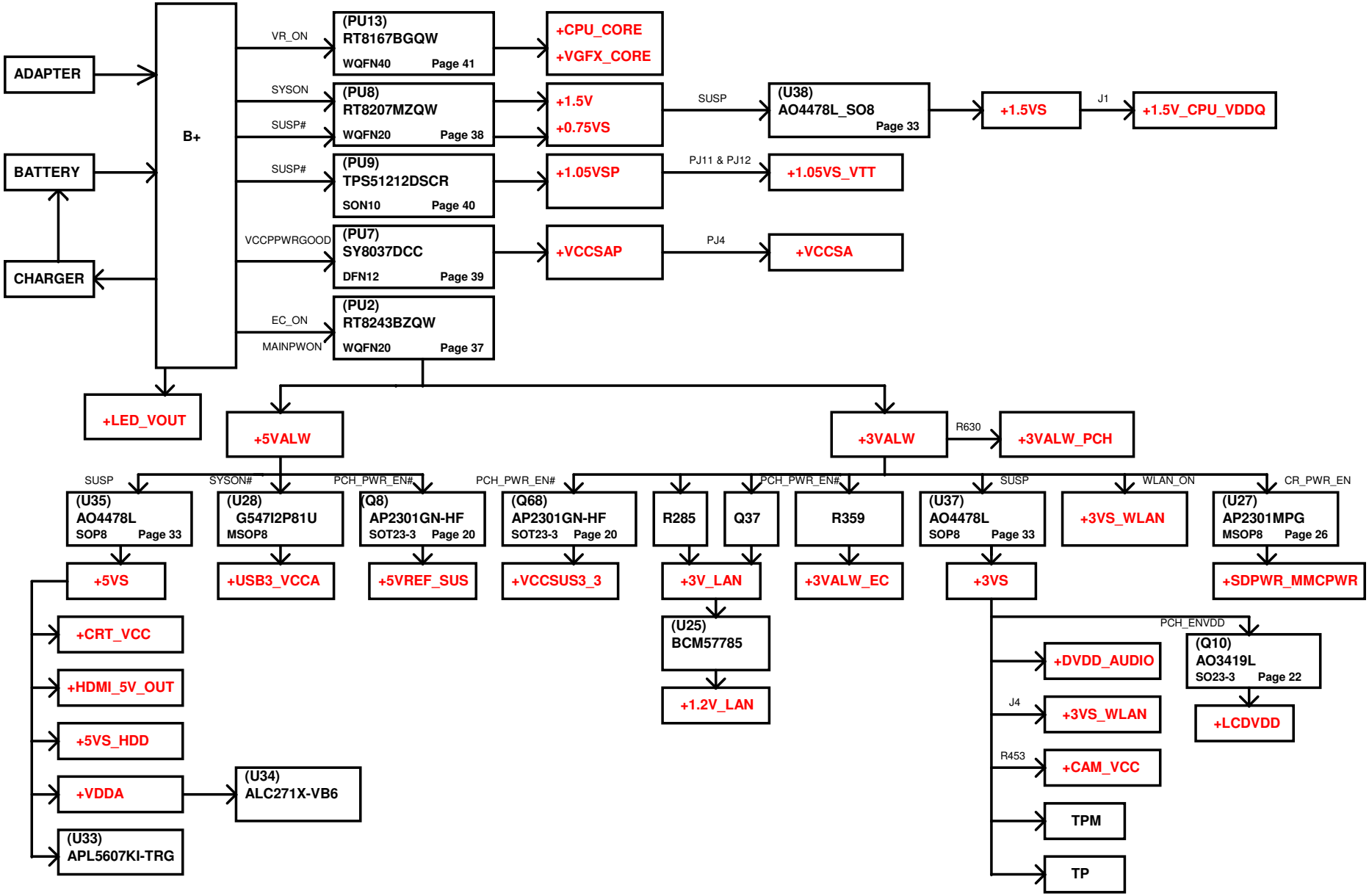
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/Pre-change power circuit	0.1	34	Add PC301 330P_0402_50V7K, PC302 470P_0402_50V7K for EMI solution	2012/4/5	EVT
2		Modify Battery CONN/OTP power circuit	0.1	35	Add PR80 0ohm to GND for BOM control (9012 AGND)	2012/4/5	EVT
3		Modify CHARGER	0.1	36	Add PC16,PC63 330P_0402_50V7K, PC20, PC48 470P_0402_50V7K, PC113, PC114, PC115, PC117, PC121 0.1U_0402_25V6 PR26 4.7_1206_5%, PC39 680P_0402_50V7K for EMI solution	2012/4/5	EVT
4		Modify 3VALWP/5VALWP power circuit	0.1	37	Add Snubber PR48 4.7_1206_5%, PC58 680P_0402_50V7K for EMI solution	2012/4/5	EVT
5		Modify 1.5VP/0.75VSP power circuit	0.1	38	Add Snubber PR175 4.7_1206_5%, PC75 680P_0402_50V7K for EMI solution	2012/4/5	EVT
6		Modify 1.05VS power circuit	0.1	40	Delete PR105 5.1K_0402_1%; PR178 0_0402_5%, Add PR188 4.99K_0402_1%; PR186 1.2K_0402_1%, PC122 1000P_0402_50V7K; PC124 0.1U_0402_25V6 for improve load response	2012/4/5	EVT
7		Modify CPU/GFX_CORE power circuit	0.1	41	Add PC45 330P_0402_50V7K, PC21 470P_0402_50V7K for EMI solution Add PC169 0.047I_0402_25V7K, change PR187 from 523 to 348_0402_1% change PR135 from 412 to 430_0402_1%	2012/4/5	EVT
8		Modify CPU/GFX_CORE power circuit	0.1	41	change PL14 from 0.22U_PCMB104T-R22MS_35A_20% to 0.22UH MMD-10RCZ-R22M-28A (from H=3 to H=4) change PR201, PR152 from 27.4K to 61.9K_0402_1%, change PH4,PH5 470K_0402_5%(from Thinking to Panasonic) thermal issue	2012/4/5	EVT
9		Modify PROCESSOR DECOUPLING power circuit	0.1	42	Add PC74 330P_0402_50V7K, PC108 470P_0402_50V7K for EMI solution	2012/4/5	EVT
10		Modify DCIN/Pre-change power circuit	0.1	34	Sawp PC10 and PC301; Sawp PC14 and PC302	2012/4/5	EVT
11		Modify Battery CONN/OTP power circuit	0.1	35	Add PR105 0ohm to GND for BOM control (9012 H_PROCHOT#_EC) change PR61 from 21K to 21.5K and PR66 from 9.53K to 9.76K for 92 throttling and 56C recovery	2012/4/18	EVT
12		Modify Battery CONN/OTP power circuit	0.1	35	Delete PR78 and add PR61, PR63 for EC932, change PR66 from 9.53kohm to 9.76k ohm, OTP setting 92C thermal protection, 56C recovery	2012/4/26	EVT
13		Modify 3VALWP/5VALWP power circuit	0.1	37	Change PR56 from 402K to 100K for 3V/5V enable setting, Add PR53 for 3V/5V enable setting.	2012/4/26	EVT
14		Modify CPU/GFX_CORE power circuit	0.1	41	change PR187 from 348 to 324 for OCP 40A fine tune, change PC169 from 0.047U to 0.068U (RC match)	2012/4/26	EVT
15		Modify CHARGER	0.1	36	change PC22 from 0.1U_0402_25V6 to 330P_0402_50V7K	2012/5/2	EVT

Compal Electronics, Inc.
Title: PIR1 (PWR)
Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1
Date: Friday, August 10, 2012 | Sheet 43 of 46

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify Prochot# setting from KB9012 to G718(EVT MEMO introction)	0.2	35	change PR63 from 2.26K to 590 ohm, PR68 from 9.1 to 1.91K From 46.2W~38W to 42.8W~33.2W	2012/5/7	EVT
2		Modify Battery CONN/OTP power circuit Modify 3VALWP/5VALWP power circuit	0.2	35 37	Sawp PR81 and PR82 location leverage Mimic winsows	2012/5/17	DVT
3		Modify Battery CONN/OTP power circuit	0.2	35	Add PR111 between 3VLP and battery connect TH for EC932	2012/5/23	DVT
4		Remove PQ16 PC302 PR10 PR11	0.2	34	Remove 51ON# RC, BATT+ to VS switch	2012/5/23	
5		MAINPWON double pull high.	0.2	35	Remove PR64	2012/5/23	
6		Modify 3v5v EN pin voltage (from 4.9V to 4.524V) for EN pin rating.	0.2	35	Change PR108 from 316K to 412K.	2012/5/23	
7		Modify 3v5v EN pin voltage for EN pin rating.	0.3	35	Change PR82 from 1000K to 887K.	2012/7/9	PVT
8							
9							
10							
11							
12							
13							
14							
15							

Compal Electronics, Inc.
Title: PIR1 (PWR)
Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1
Date: Friday, August 10, 2012 | Sheet 44 of 46



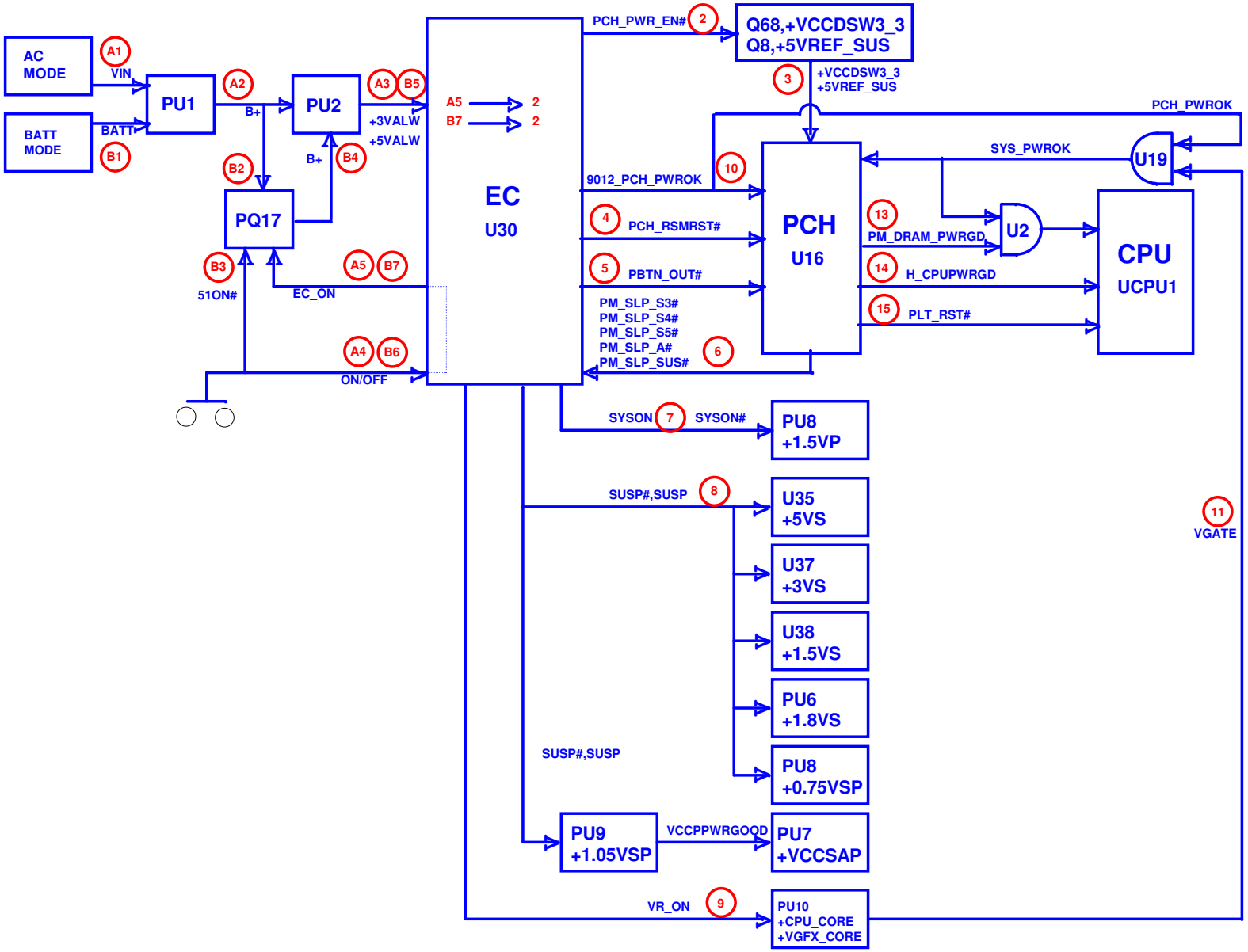
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: Power Rail

Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 45 of 46



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
Custom	CHROME M/B LA-8942P Schematic	0.1

Date: Friday, August 10, 2012 Sheet 46 of 46