Compal Confidential

Model Name : VITU5

File Name : LA-8971P

Compal Confidential

VITU5 M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH(HM77)

Nvidia chip:N13M-GS(23x23)

2012-02-16

REV:0.1

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Chief River

NV N13M-GS
23mm *23mm
VRAM 128*16 DDR3*4

PCI-E X16
Gen 2

Intel
IVY Bridge ULV
(Sandy Bridge)
Processor
BGA1023

DDR3-1333/1600
Dual Channel

DDR3-SO-DIMM X2

FDI *8
100MHz
2.7GT/s

DMI2 *4
100MHz
5GT/s

Std HDMI Connector

LVDS Connector

Mini VGA Connector

Intel
Panther Point
HM77
FCBGA 989 Balls
25mm*25mm

6*SATA
(port0,1 Support SATA3)

SATA3.0 HDD CONN

PCI Express (Full)
Mini card Slot 2
SSD(SATA3.0)

ODD (SATA2.0)

4*USB3.0

14*USB2.0

USB PORT 3.0 x1 (Left)

USB PORT 2.0 x2 (Right)
IO Board

Card Reader RTS 5178 (2in1)
IO Board

CMOS Camera

BlueTooth CONN

6*PCI-E x1

PCI Express (Half)
Mini card Slot 1
WLAN/WiMAX

PCI-E (WLAN)

SPI ROM
BIOS
4MB*1
2MB*1

LPC BUS

EC
ENE KB9012

HD Audio

LAN(10/100/Giga)
Realtek
8105E-VD (10/100)
8111F-CGT (Giga)

RJ45 CONN

Int.KBD

Touch Pad

Thermal Sensor

Audio Codec
RealTek
ALC259-VC2-CG

2Channel Speaker

Single Digital MIC

Audio Combo Jack
(APPLE type)
HeadPhone Output
Microphone Input

Sub-borad

- ODD Board
- POWER BOARD
- LED BOARD
- IO Board
  USB2.0*2,card reader

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

EC SM Bus1 address

Address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 3.0	USB 2.0		Port	3 External USB Port
xHCI1	EHCI1	UHCI0	0	USB 3.0 Port (Left Side)
xHCI2			1	
xHCI3		UHCI1	2	USB/B (Right Side USB-BD)
xHCI4			3	USB/B (Right Side USB-BD)
		UHCI2	4	X (USB PORT disabled on HM70)
			5	X (USB PORT disabled on HM70)
		UHCI3	6	X (USB PORT disabled on HM70)
			7	X (USB PORT disabled on HM70)
	EHCI2	UHCI4	8	Camera
			9	Blue Tooth
		UHCI5	10	Mini Card(WLAN)
			11	USB Port (Right Side CR-BD)
		UHCI6	12	X (USB PORT disabled on HM70)
			13	X (USB PORT disabled on HM70)

HM70 Disable xHCI3,xHCI4

BOM Structure Table

BTO Item	BOM Structure
INTEL UMA only	UMA@
GPU:Seymour XTX	XTX@
HDMI	HDMI@
HDD1 (HM77 SATA 3.0)	HDD1@
HDD2 (HM70 SATA 2.0)	HDD2@
Interna-Intel-USB3.0	IU3@
Interna-Intel-USB2.0	IU2@
Blue Tooth	BT@
10/100 LAN	8105E@
GIGA LAN	8111F@
Connector	ME@
45 LEVEL	45@
Unpop	@

SATA Port Table

	HM77	HM70	
SATA P0	GEN3/2/1	GEN3/2/1	SSD
SATA P1	GEN3/2/1	Disable	HDD (HM77)
SATA P2	GEN2/1	GEN2/1	HDD (HM70)
SATA P3	GEN2/1	Disable	
SATA P4	GEN2/1	GEN2/1	
SATA P5	GEN2/1	GEN2/1	

HM70 Disable P1,P3

PCIe Port Table

	HM77	HM70	
PCIe P1	Enable	Enable	LAN
PCIe P2	Enable	Enable	WLAN
PCIe P3	Enable	Enable	
PCIe P4	Enable	Enable	
PCIe P5	Enable	Disable	
PCIe P6	Enable	Disable	
PCIe P7	Enable	Disable	
PCIe P8	Enable	Disable	

HM70 Disable P5,P6,P7,P8

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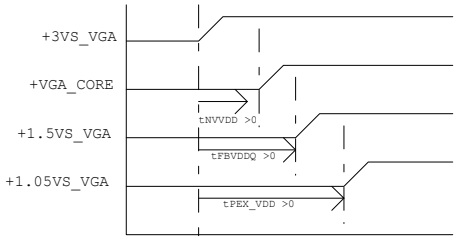
Hot plug detect for IFP link C

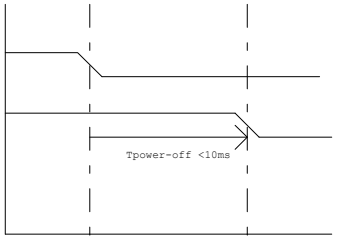
VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us

2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



1.all GPU power rails should be turned off within 10ms

Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

Products	GPU (4) (W)	Mem (1,5) (MHz)	NVCLK /MCLK	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GL (28nm)	???
N13M-GE (28nm)	???

GPU	FB Memory (GDDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL N13M-GE	Samsung 2500MHz	K4G10325FG-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ1H24BFR-T2C						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 2500MHz	K4G20325FG-HC04						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ2H24MFR-T2C						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76

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PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

+1.05VS_VTT

R249
24.9_0402_1%

W=12mil L=500mil S=15mil

PEG_COMP

UCPU1A

PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO

PEG_GTX_HRX_N[8..15] <23>
PEG_GTX_HRX_P[8..15] <23>
PEG_HTX_C_GRX_N[8..15] <23>
PEG_HTX_C_GRX_P[8..15] <23>

DMI

<16> DMI_CRX_PTX_N0 — DMI_CRX_PTX_N0 M2 — DMI_RX#[0]
<16> DMI_CRX_PTX_N1 — DMI_CRX_PTX_N1 P6 — DMI_RX#[1]
<16> DMI_CRX_PTX_N2 — DMI_CRX_PTX_N2 P1 — DMI_RX#[2]
<16> DMI_CRX_PTX_N3 — DMI_CRX_PTX_N3 P10 — DMI_RX#[3]

<16> DMI_CRX_PTX_P0 — DMI_CRX_PTX_P0 N3 — DMI_RX[0]
<16> DMI_CRX_PTX_P1 — DMI_CRX_PTX_P1 P7 — DMI_RX[1]
<16> DMI_CRX_PTX_P2 — DMI_CRX_PTX_P2 P3 — DMI_RX[2]
<16> DMI_CRX_PTX_P3 — DMI_CRX_PTX_P3 P11 — DMI_RX[3]

<16> DMI_CTX_PRX_N0 — DMI_CTX_PRX_N0 K1 — DMI_TX#[0]
<16> DMI_CTX_PRX_N1 — DMI_CTX_PRX_N1 M8 — DMI_TX#[1]
<16> DMI_CTX_PRX_N2 — DMI_CTX_PRX_N2 N4 — DMI_TX#[2]
<16> DMI_CTX_PRX_N3 — DMI_CTX_PRX_N3 R2 — DMI_TX#[3]

<16> DMI_CTX_PRX_P0 — DMI_CTX_PRX_P0 K3 — DMI_TX[0]
<16> DMI_CTX_PRX_P1 — DMI_CTX_PRX_P1 M7 — DMI_TX[1]
<16> DMI_CTX_PRX_P2 — DMI_CTX_PRX_P2 P4 — DMI_TX[2]
<16> DMI_CTX_PRX_P3 — DMI_CTX_PRX_P3 T3 — DMI_TX[3]

Intel(R) FDI

<16> FDI_CTX_PRX_N0 — FDI_CTX_PRX_N0 U7 — FDI0_TX#[0]
<16> FDI_CTX_PRX_N1 — FDI_CTX_PRX_N1 W11 — FDI0_TX#[1]
<16> FDI_CTX_PRX_N2 — FDI_CTX_PRX_N2 W1 — FDI0_TX#[2]
<16> FDI_CTX_PRX_N3 — FDI_CTX_PRX_N3 AA6 — FDI0_TX#[3]
<16> FDI_CTX_PRX_N4 — FDI_CTX_PRX_N4 W6 — FDI1_TX#[0]
<16> FDI_CTX_PRX_N5 — FDI_CTX_PRX_N5 V4 — FDI1_TX#[1]
<16> FDI_CTX_PRX_N6 — FDI_CTX_PRX_N6 Y2 — FDI1_TX#[2]
<16> FDI_CTX_PRX_N7 — FDI_CTX_PRX_N7 AC9 — FDI1_TX#[3]

<16> FDI_CTX_PRX_P0 — FDI_CTX_PRX_P0 U6 — FDI0_TX[0]
<16> FDI_CTX_PRX_P1 — FDI_CTX_PRX_P1 W10 — FDI0_TX[1]
<16> FDI_CTX_PRX_P2 — FDI_CTX_PRX_P2 W3 — FDI0_TX[2]
<16> FDI_CTX_PRX_P3 — FDI_CTX_PRX_P3 AA7 — FDI0_TX[3]
<16> FDI_CTX_PRX_P4 — FDI_CTX_PRX_P4 W7 — FDI1_TX[0]
<16> FDI_CTX_PRX_P5 — FDI_CTX_PRX_P5 T4 — FDI1_TX[1]
<16> FDI_CTX_PRX_P6 — FDI_CTX_PRX_P6 AA3 — FDI1_TX[2]
<16> FDI_CTX_PRX_P7 — FDI_CTX_PRX_P7 AC8 — FDI1_TX[3]

<16> FDI_FSYNC0 — FDI_FSYNC0 AA11 — FDI0_FSYNC
<16> FDI_FSYNC1 — FDI_FSYNC1 AC12 — FDI1_FSYNC

<16> FDI_INT — FDI_INT U11 — FDI_INT

<16> FDI_LSYNC0 — FDI_LSYNC0 AA10 — FDI0_LSYNC
<16> FDI_LSYNC1 — FDI_LSYNC1 AG8 — FDI1_LSYNC

PCI EXPRESS - GRAPHICS

PEG_RX#[0] H22
PEG_RX#[1] J21
PEG_RX#[2] B22
PEG_RX#[3] D21
PEG_RX#[4] A19
PEG_RX#[5] D17
PEG_RX#[6] B14
PEG_RX#[7] D13
PEG_RX#[8] A11 — PEG_GTX_C_HRX_N8 — C259 — PEG_GTX_HRX_N8
PEG_RX#[9] B10 — PEG_GTX_C_HRX_N9 — C276 — PEG_GTX_HRX_N9
PEG_RX#[10] G8 — PEG_GTX_C_HRX_N10 — C257 — PEG_GTX_HRX_N10
PEG_RX#[11] A8 — PEG_GTX_C_HRX_N11 — C274 — PEG_GTX_HRX_N11
PEG_RX#[12] B6 — PEG_GTX_C_HRX_N12 — C254 — PEG_GTX_HRX_N12
PEG_RX#[13] H8 — PEG_GTX_C_HRX_N13 — C272 — PEG_GTX_HRX_N13
PEG_RX#[14] E5 — PEG_GTX_C_HRX_N14 — C252 — PEG_GTX_HRX_N14
PEG_RX#[15] K7 — PEG_GTX_C_HRX_N15 — C270 — PEG_GTX_HRX_N15

PEG_RX[0] K22
PEG_RX[1] K19
PEG_RX[2] C21
PEG_RX[3] D19
PEG_RX[4] C19
PEG_RX[5] D16
PEG_RX[6] C13
PEG_RX[7] D12
PEG_RX[8] C11 — PEG_GTX_C_HRX_P8 — C258 — PEG_GTX_HRX_P8
PEG_RX[9] C9 — PEG_GTX_C_HRX_P9 — C277 — PEG_GTX_HRX_P9
PEG_RX[10] F8 — PEG_GTX_C_HRX_P10 — C256 — PEG_GTX_HRX_P10
PEG_RX[11] C8 — PEG_GTX_C_HRX_P11 — C275 — PEG_GTX_HRX_P11
PEG_RX[12] C5 — PEG_GTX_C_HRX_P12 — C255 — PEG_GTX_HRX_P12
PEG_RX[13] H6 — PEG_GTX_C_HRX_P13 — C273 — PEG_GTX_HRX_P13
PEG_RX[14] F6 — PEG_GTX_C_HRX_P14 — C253 — PEG_GTX_HRX_P14
PEG_RX[15] K6 — PEG_GTX_C_HRX_P15 — C271 — PEG_GTX_HRX_P15

PEG_TX#[0] G22
PEG_TX#[1] C23
PEG_TX#[2] D23
PEG_TX#[3] F21
PEG_TX#[4] H19
PEG_TX#[5] C17
PEG_TX#[6] K15
PEG_TX#[7] F17
PEG_TX#[8] F14 — PEG_HTX_GRX_N8 — C562 — PEG_HTX_C_GRX_N8
PEG_TX#[9] A15 — PEG_HTX_GRX_N9 — C582 — PEG_HTX_C_GRX_N9
PEG_TX#[10] J14 — PEG_HTX_GRX_N10 — C564 — PEG_HTX_C_GRX_N10
PEG_TX#[11] H13 — PEG_HTX_GRX_N11 — C584 — PEG_HTX_C_GRX_N11
PEG_TX#[12] M10 — PEG_HTX_GRX_N12 — C566 — PEG_HTX_C_GRX_N12
PEG_TX#[13] F10 — PEG_HTX_GRX_N13 — C587 — PEG_HTX_C_GRX_N13
PEG_TX#[14] D9 — PEG_HTX_GRX_N14 — C568 — PEG_HTX_C_GRX_N14
PEG_TX#[15] J4 — PEG_HTX_GRX_N15 — C589 — PEG_HTX_C_GRX_N15

PEG_TX[0] F22
PEG_TX[1] A23
PEG_TX[2] D24
PEG_TX[3] E21
PEG_TX[4] G19
PEG_TX[5] B18
PEG_TX[6] K17
PEG_TX[7] G17
PEG_TX[8] E14 — PEG_HTX_GRX_P8 — C561 — PEG_HTX_C_GRX_P8
PEG_TX[9] C15 — PEG_HTX_GRX_P9 — C583 — PEG_HTX_C_GRX_P9
PEG_TX[10] K13 — PEG_HTX_GRX_P10 — C563 — PEG_HTX_C_GRX_P10
PEG_TX[11] G13 — PEG_HTX_GRX_P11 — C585 — PEG_HTX_C_GRX_P11
PEG_TX[12] K10 — PEG_HTX_GRX_P12 — C565 — PEG_HTX_C_GRX_P12
PEG_TX[13] G10 — PEG_HTX_GRX_P13 — C586 — PEG_HTX_C_GRX_P13
PEG_TX[14] D8 — PEG_HTX_GRX_P14 — C567 — PEG_HTX_C_GRX_P14
PEG_TX[15] K4 — PEG_HTX_GRX_P15 — C588 — PEG_HTX_C_GRX_P15

All capacitors: 1 — 2 — OPT@ 0.22U_0402_6.3V6K

eDP

AF3 — eDP_COMPIO
AD2 — eDP_ICOMPO
AG11 — eDP_HPD#
AG4 — eDP_AUX#
AF4 — eDP_AUX
AC3 — eDP_TX#[0]
AC4 — eDP_TX#[1]
AE11 — eDP_TX#[2]
AE7 — eDP_TX#[3]
AC1 — eDP_TX[0]
AA4 — eDP_TX[1]
AE10 — eDP_TX[2]
AE6 — eDP_TX[3]

IVY-BRIDGE_BGA1023

+1.05VS_VTT

R247
24.9_0402_1%

EDP_COMP

W=12mil L=500mil S=15mil

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
can't be left floating ,even if disable eDP function...

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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Date: Wednesday, February 15, 2012 | Sheet 5 of 58

PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.5& Tacoma_Fall2 1.0 reserve

C614 @ 0.1U_0402_16V4Z — H_CPUPWRGD_R
R292 @ 10K_0402_5%

PROC_SELECT#
PH VCPLL and connect to PCH DF_TVS

<18> H_SNB_IVB# — F49 PROC_SELECT#
R35 @ 10K_0402_5% — C57 PROC_DETECT#

XBOX 三紅功能
@ T33 PAD — H_CATERR# — C49 CATERR#

<19,42> H_PECI — A48 PECI

+1.05VS_VTT — R534 62_0402_5% — H_PROCHOT#
<42,49> H_PROCHOT# — R533 56_0402_5% — H_PROCHOT#_R — C45 PROCHOT#

<19> H_THERMTRIP# — H_THERMTRIP# — D45 THERMTRIP#

<16> H_PM_SYNC — H_PM_SYNC — C48 PM_SYNC

UNCOREPWRGOOD:非CORE外的電OK
<19> H_CPUPWRGD — H_CPUPWRGD — R305 0_0402_5% — H_CPUPWRGD_R — B46 UNCOREPWRGOOD

R237 130_0402_1% — VDDPWRGOOD_R — BE45 SM_DRAMPWROK

BUF_CPU_RST# — D44 RESET#

UCPU1B

MISC THERMAL
PROC_SELECT#
PROC_DETECT#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

CLOCKS
BCLK J3 CLK_CPU_DMI — CLK_CPU_DMI <15>
BCLK# H2 CLK_CPU_DMI# — CLK_CPU_DMI# <15>
DPLL_REF_CLK AG3 CLK_CPU_DPLL — R516 1K_0402_5%
DPLL_REF_CLK# AG1 CLK_CPU_DPLL# — R517 1K_0402_5% — +1.05VS_VTT

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

DDR3 MISC
SM_DRAMRST# AT30 — H_DRAMRST# — H_DRAMRST# <7>
SM_RCOMP[0] BF44 SM_RCOMP0 — R272 140_0402_1%
SM_RCOMP[1] BE43 SM_RCOMP1 — R273 25.5_0402_1%
SM_RCOMP[2] BG43 SM_RCOMP2 — R267 200_0402_1%
DDR3 Compensation Signals
@ C82 100P_0402_50V8J — ESD C Reserve

JTAG & BPM
PRDY# N53
PREQ# N55
TCK L56 — XDP_TCK
TMS L55 — XDP_TMS
TRST# J58 — XDP_TRST#
TDI M60 — XDP_TDI
TDO L59 — XDP_TDO
DBR# K58 — XDP_DBRESET#
BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61

PWR MANAGEMENT

IVY-BRIDGE_BGA1023

+1.05VS_VTT
XDP_TMS R20 51_0402_5%
XDP_TDI R39 51_0402_5%
XDP_TDO R37 51_0402_5%
XDP_TCK R40 51_0402_5%
XDP_TRST# R28 51_0402_5%
PU/PD for JTAG signals

+3VS
XDP_DBRESET# R312 @ 1K_0402_5%

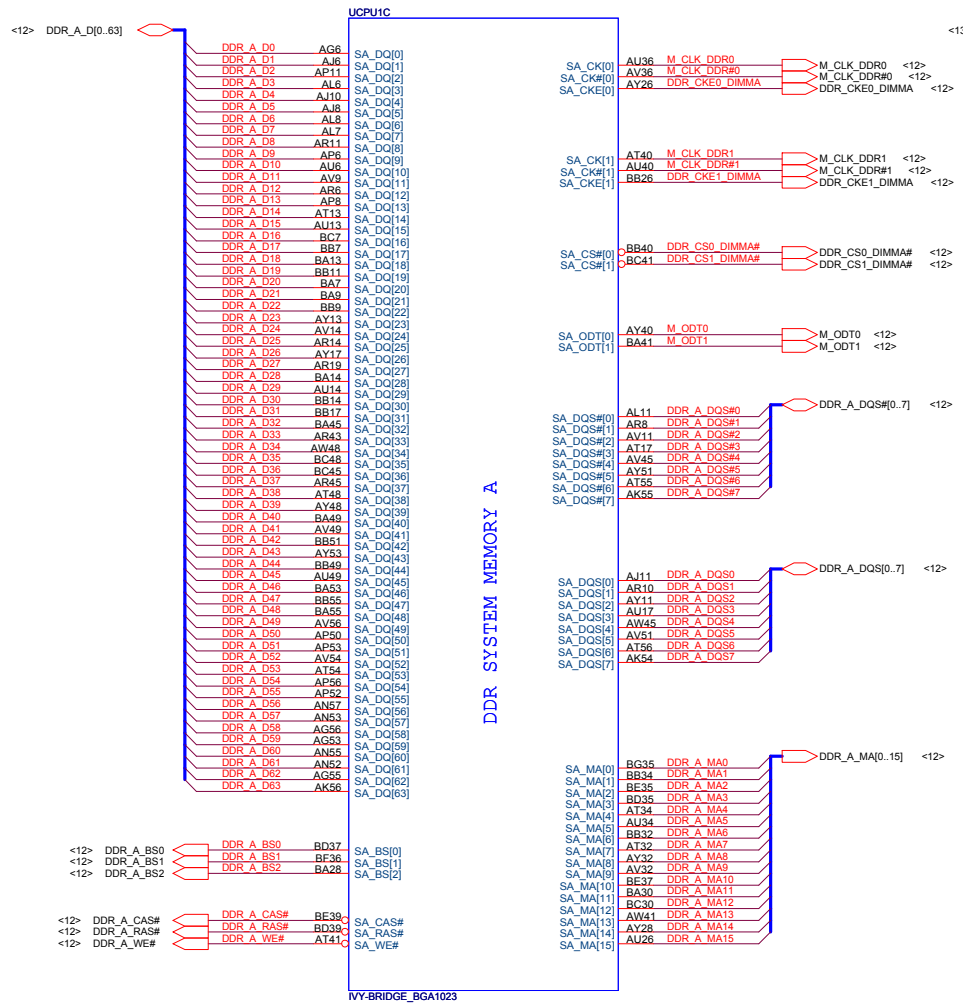
Tacoma_Fall2 1.0 PH 1K +3VS
Check list 1.5 PH 1K +3VS
Debug port DG1.1-1.3 50~5K ohm

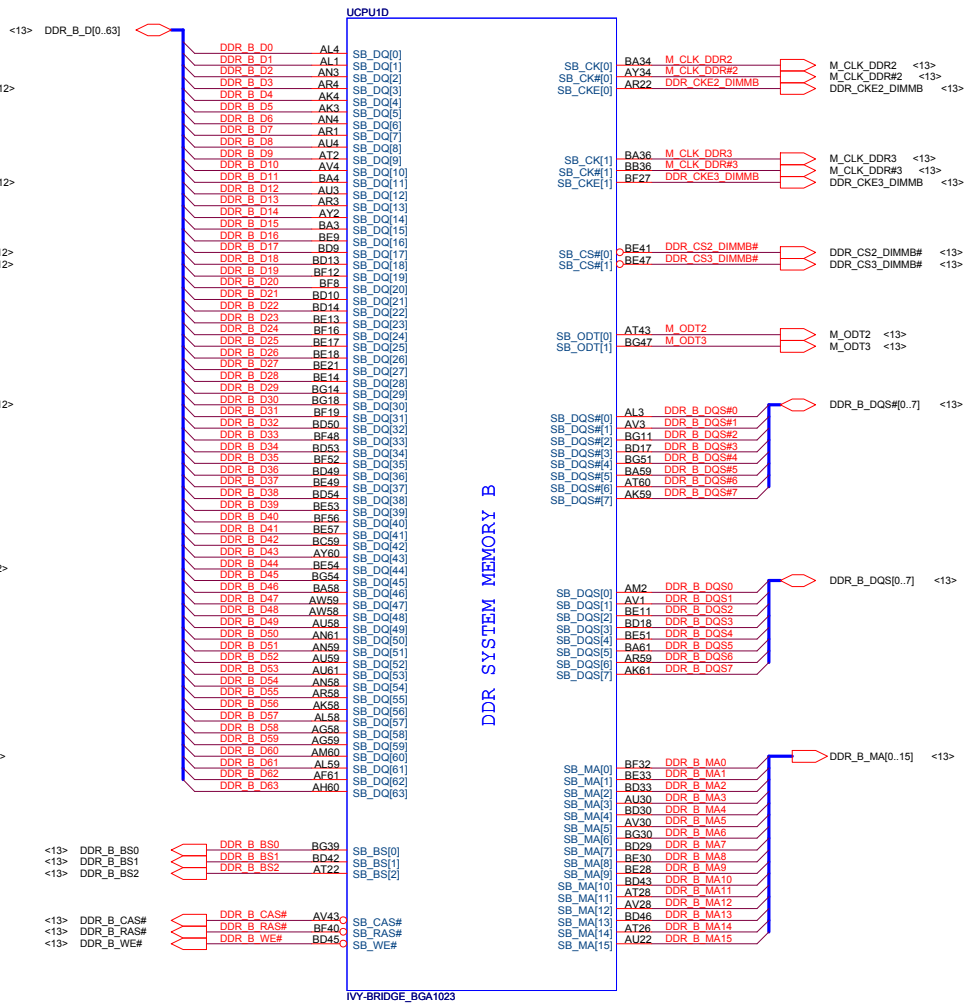
+3VALW
C228 0.1U_0402_16V4Z
+3VS
R31 10K_0402_5%
<16> SYS_PWROK — SYS_PWROK — R60 @ 10K_0402_5%
<16> PM_DRAM_PWRGD — PM_DRAM_PWRGD
U22 74AHC1G09GW_TSSOP5
+1.5V_CPU_VDDQ
R238 200_0402_5%
PM_SYS_PWRGD_BUF
@ R38 39_0402_5%
<10> RUN_ON_CPU1.5VS3# — RUN_ON_CPU1.5VS3# — R13 @ 0_0402_5%
<10,47,52> SUSP — R14 @ 0_0402_5%
@ Q4 2N7002K_SOT23-3

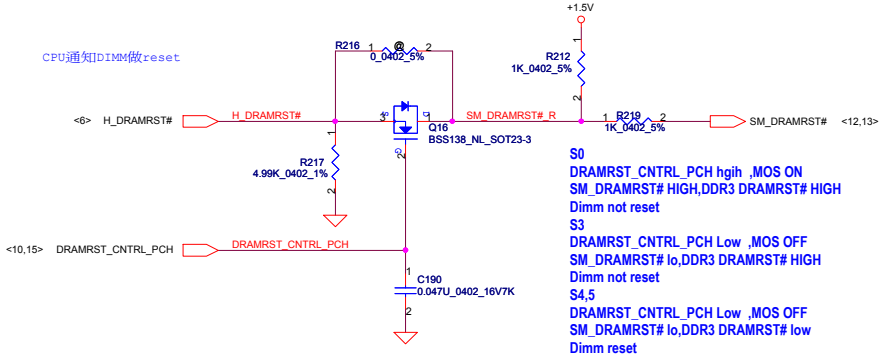
Buffered reset to CPU
+3VS
+1.05VS_VTT
R546 75_0402_5%
C617 0.1U_0402_16V4Z
U45 SN74LVC1G07DCKR_SC70-5
BUF_CPU_RST# — R544 43_0402_5% — BUFO_CPU_RST#
PCH_PLTRST# — PCH_PLTRST# <18>
@ C43 0.1U_0402_16V4Z
R9 @ 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.
Title: PROCESSOR(2/7) DDRIII
Size: Custom | Document Number: LA-8971P | Rev: 0.1
Date: Wednesday, February 15, 2012 | Sheet 6 of 58







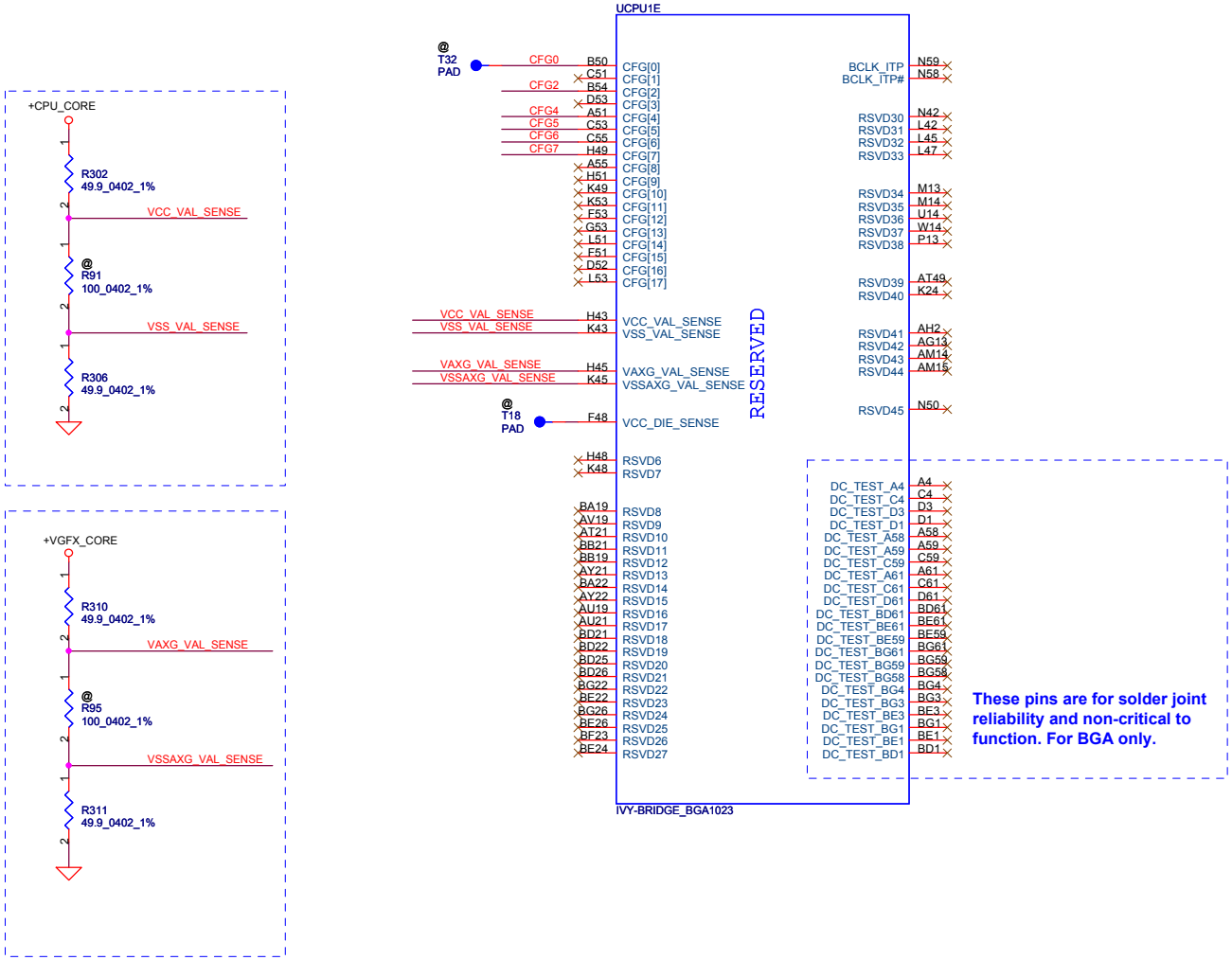
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

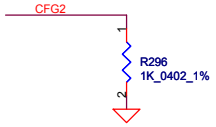
Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-8971P	0.1

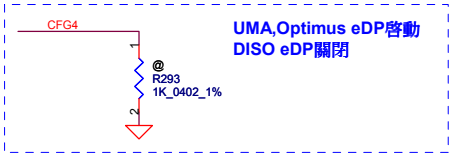
Date: Wednesday, February 15, 2012 Sheet 7 of 58



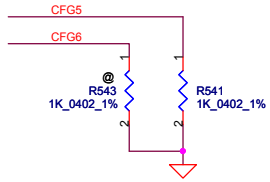
CFG Straps for Processor



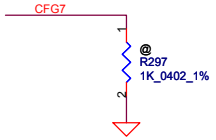
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



eDP enable	
CFG4	* 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	PROCESSOR(4/7) RSVD,CFG		
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POWER

ULV type
DC 33A

8.5A

UCPU1F

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at Power side

CORE SUPPLY

VCC[1] A26, A29, A31, A34, A35, A38, A39, A42, C26, C27, C32, C34, C37, C39, C42, D27, D32, D34, D37, D39, D42, E26, E28, E32, E34, E37, E38, F25, F26, F28, F32, F34, F37, F38, F42, G42, H25, H26, H28, H29, H32, H34, H35, H37, H38, H40, J25, J26, J28, J29, J32, J34, J35, J37, J38, J40, J42, K26, K27, K29, K32, K34, K35, K37, K39, K42, L25, L28, L33, L36, L40, N26, N30, N34, N38
VCC[76]

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

VCCIO[1] AF46, VCCIO[3] AG48, VCCIO[4] AG50, VCCIO[5] AG51, VCCIO[6] AJ17, VCCIO[7] AJ21, VCCIO[8] AJ25, VCCIO[9] AJ43, VCCIO[10] AJ47, VCCIO[11] AK50, VCCIO[12] AK51, VCCIO[13] AL14, VCCIO[14] AL15, VCCIO[15] AL16, VCCIO[16] AL20, VCCIO[17] AL22, VCCIO[18] AL26, VCCIO[19] AL45, VCCIO[20] AL48, VCCIO[21] AM16, VCCIO[22] AM17, VCCIO[23] AM21, VCCIO[24] AM43, VCCIO[25] AM47, VCCIO[26] AN20, VCCIO[27] AN42, VCCIO[28] AN45, VCCIO[29] AN48

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at Power side

For PEG

VCCIO[30] AA14, VCCIO[31] AA15, VCCIO[32] AB17, VCCIO[33] AB20, VCCIO[34] AC13, VCCIO[35] AD16, VCCIO[36] AD18, VCCIO[37] AD21, VCCIO[38] AE14, VCCIO[39] AE15, VCCIO[40] AE16, VCCIO[41] AF18, VCCIO[42] AF20, VCCIO[43] AG15, VCCIO[44] AG16, VCCIO[45] AG17, VCCIO[46] AG20, VCCIO[47] AG21, VCCIO[48] AJ14, VCCIO[49] AJ15

+1.05VS_VTT

VCCIO50 W16
VCCIO51 W17

+3VS

R521 10K_0402_5%

VCCIO_SEL

@ R522 10K_0402_5%

VCCIO_SEL after Ivy bridge ES2 Voltage support	
BC22 *	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL BC22 VCCIO_SEL

QUIET RAILS

+1.05VS_VTT

VCCPQE[1] AM25
VCCPQE[2] AN22

C553 1U_0402_6.3V6K

+1.05VS_VTT R531 130_0402_5%

+1.05VS_VTT R529 75_0402_5%

Place the PU resistors close to CPU

SVID

VIDALERT# A44 H_CPU_SVIDALRT# R528 43_0402_1% VR_SVID_ALRT# <56>
VIDSCLK B43 H_CPU_SVIDCLK R527 0_0402_5% VR_SVID_CLK <56>
VIDSOUT C44 H_CPU_SVIDDAT R530 0_0402_5% VR_SVID_DAT <56>

Place the PU resistors close to VR

+CPU_CORE

R79 @ 100_0402_1%

R281 100_0402_1%

SENSE LINES

VCC_SENSE F43 VCCSENSE_R R282 0_0402_5% VCCSENSE <56>
VSS_SENSE G43 VSSSENSE_R R289 0_0402_5% VSSSENSE <56>

R288 100_0402_1%

R513 10_0402_5% +1.05VS_VTT

VCCIO_SENSE AN16 VCCIO_SENSE VCCIO_SENSE <54>
VSS_SENSE_VCCIO AN17 VSSIO_SENSE VSSIO_SENSE_L <54>

R512 10_0402_5%

Check list 1.5

Should change to connect form power circuit & layout differential with VCCIO_SENSE.

IVY-BRIDGE_BGA1023

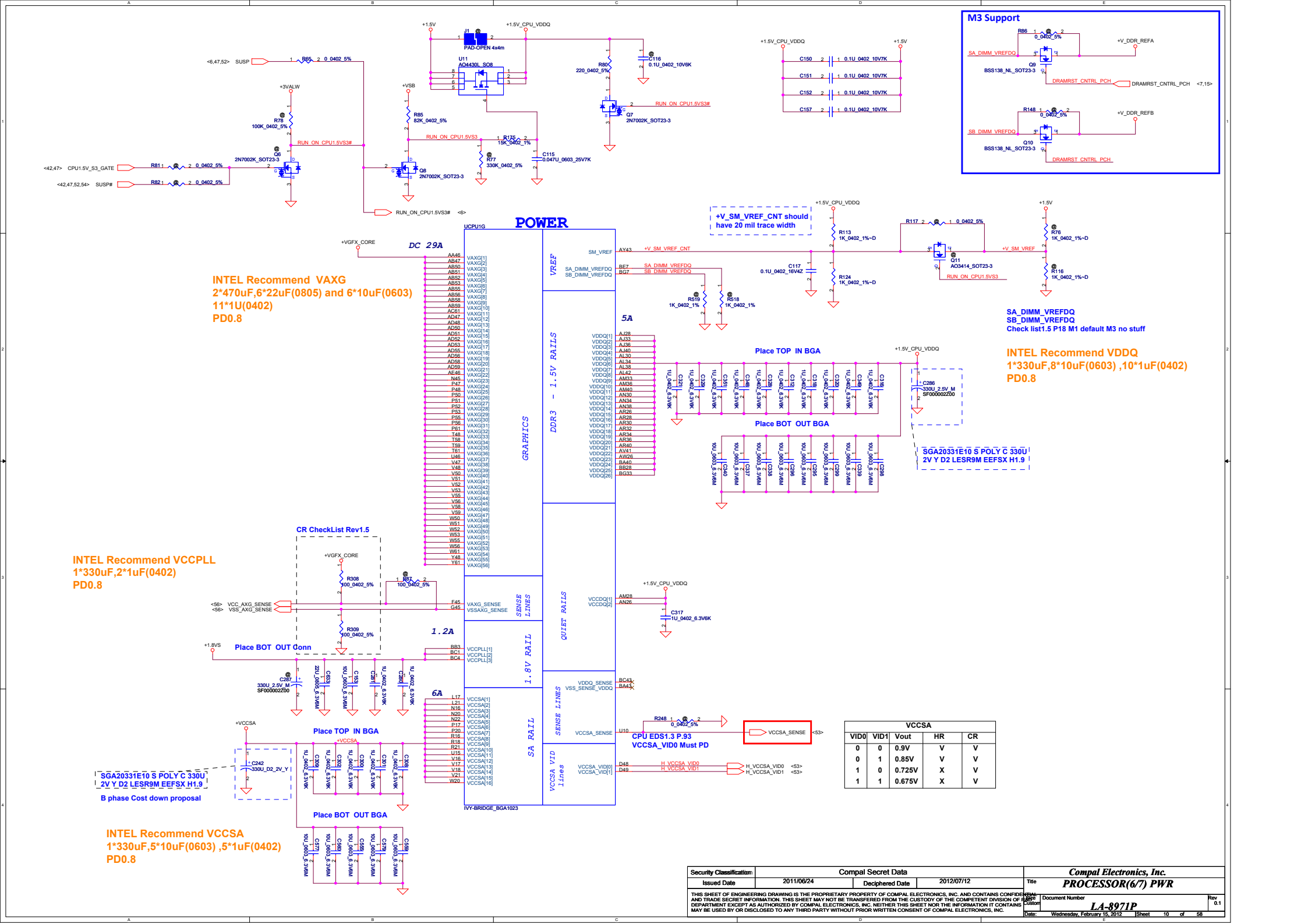
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

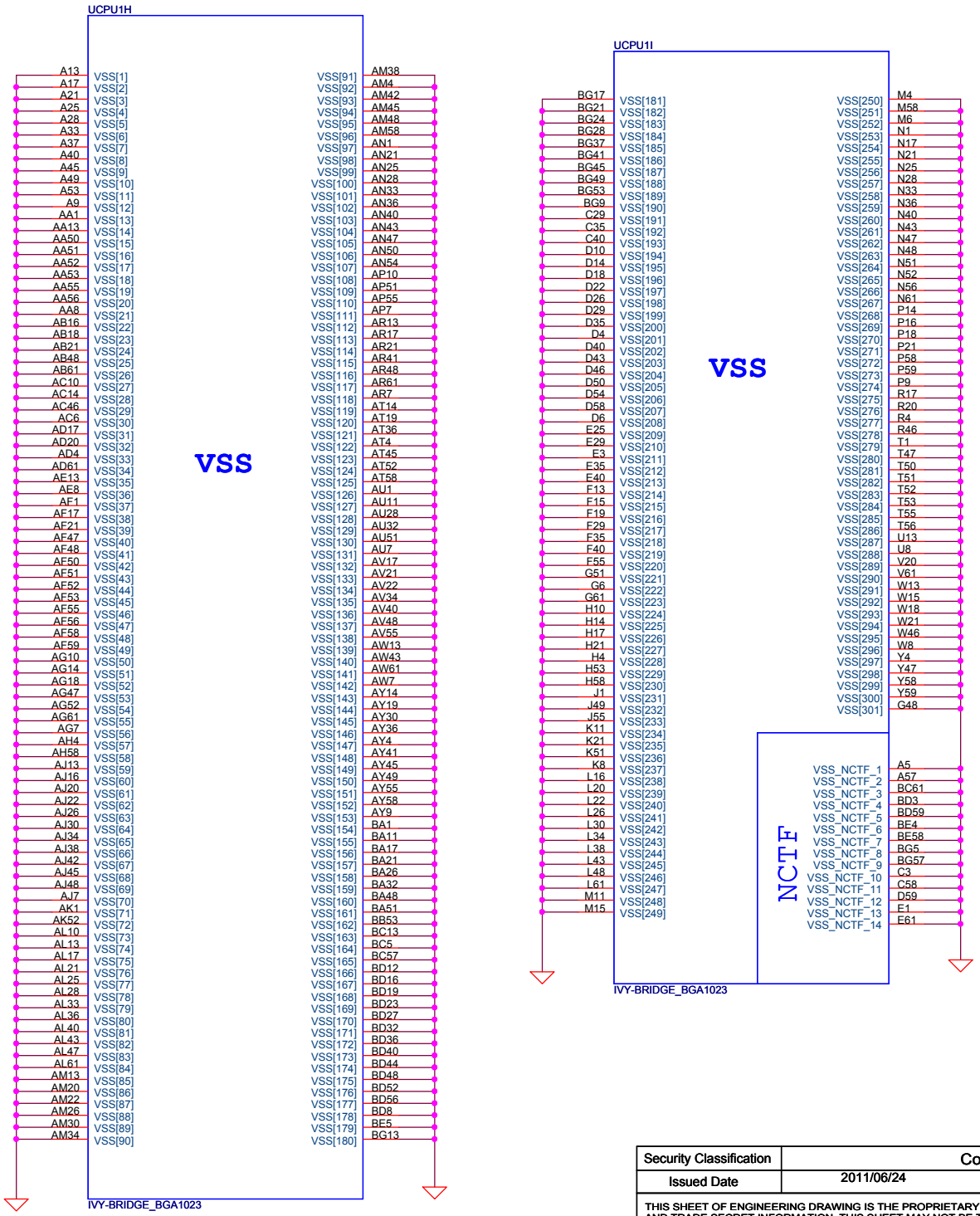
Size	Document Number	Rev
Custom	LA-8971P	0.1

Date: Wednesday, February 15, 2012 Sheet 9 of 58



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title PROCESSOR(6/7) PWR

Size	Document Number	Rev
Custom	LA-8971P	0.1
Date: Wednesday, February 15, 2012	Sheet 10 of 58	



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: LA-8971P | Rev: 0.1

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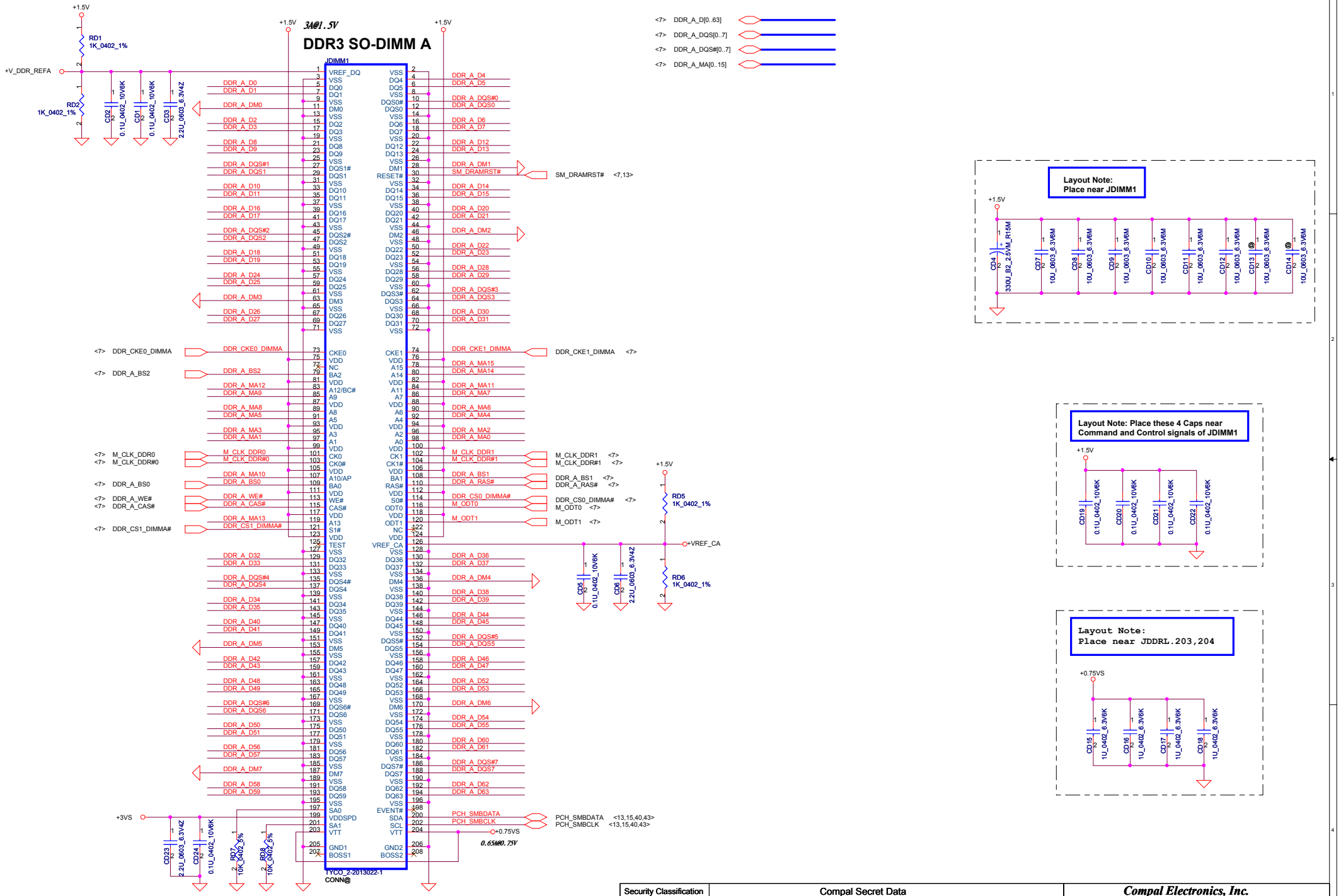
DDR3 SO-DIMM A

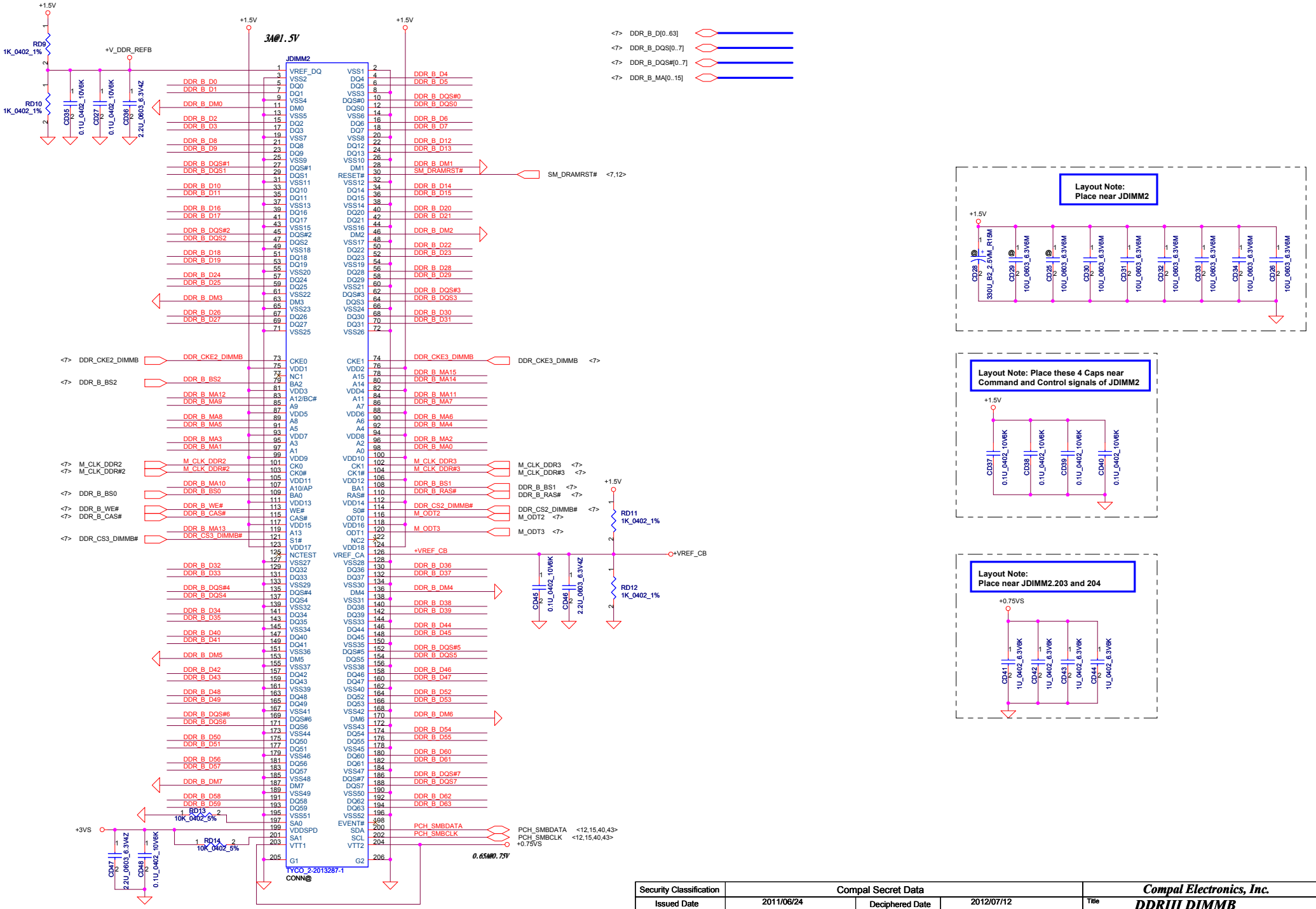


Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size	Document Number	Rev
Custom	LA-8971P	0.1
Date: Wednesday, February 15, 2012	Sheet 12 of 58	



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: DDRIII DIMMB			
Size: Custom	Document Number: LA-8971P		Rev: 0.1
Date: Wednesday, February 15, 2012	Sheet 13 of 58		

CLRP1/2 close RAM door JDIMM1/2

C439 1U_0603_10V6K — CLRP1 SHORT PADS
C440 1U_0603_10V6K — CLRP2 SHORT PADS
+RTCVCC
R356 20K_0402_5% — PCH_RTCRST#
R357 20K_0402_5% — PCH_SRTCRST#

+RTCVCC
R358 1M_0402_5% — SM_INTRUDER#
R363 330K_0402_5% — PCH_INTVRMEN

INTVRMEN

★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R109 @ 1K_0402_5% — PCH_SPKR

HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

+3V_PCH
R46 @ 1K_0402_5% — HDA_SDOUT_PCH
<42> ME_FLASH — R73 0_0402_5%

HDA_SDO

ME debug mode,this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH
R47 1K_0402_5% — HDA_SYNC_PCH

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

<31> HDA_BITCLK_AUDIO — R75 33_0402_5% — HDA_BITCLK_PCH
<31> HDA_SYNC_AUDIO — R80 33_0402_5% — HDA_SYNC_PCH_R
<31> HDA_RST_AUDIO# — R74 33_0402_5% — HDA_RST_PCH#
<31> HDA_SDOUT_AUDIO — R72 33_0402_5% — HDA_SDOUT_PCH

+3V_PCH
R134 200_0402_5% — PCH_JTAG_TDO
R143 200_0402_5% — PCH_JTAG_TMS
R137 200_0402_5% — PCH_JTAG_TDI
R141 100_0402_1%
R140 100_0402_1%
R142 100_0402_1%

PCH_RTCX1
R406 10M_0402_5%
PCH_RTCX2
Y2 32.768KHZ_12.5PF_9H03200019
C452 18P_0402_50V8J
C451 18P_0402_50V8J

+RTCVCC — W=20mils — +RTCBATT
R59 1K_0402_5%
C441 1U_0603_10V4Z

Prevent back drive issue.

+5VS
Q3 BSS138_NL_SOT23-3
HDA_SYNC_PCH_R — R48 @ 0_0402_5% — HDA_SYNC_PCH
R29 1M_0402_5%
<31> PCH_SPKR — PCH_SPKR
<31> HDA_SDIN0 — HDA_SDIN0

R100 51_0402_5% — PCH_JTAG_TCK

PCH_SPI_CLK_2 — R433 WIN8@ 33_0402_5%
PCH_SPI_CLK_1 — R432 33_0402_5% — PCH_SPI_CLK
PCH_SPI_CS0#_1 — R127 33_0402_5% — PCH_SPI_CS0#
PCH_SPI_CS1#_2 — R446 WIN8@ 33_0402_5%
PCH_SPI_CS1#_1 — PCH_SPI_CS1#
PCH_SPI_MOSI_2 — R123 WIN8@ 33_0402_5%
PCH_SPI_MOSI_1 — R122 33_0402_5% — PCH_SPI_MOSI
PCH_SPI_MISO_1 — R437 33_0402_5% — PCH_SPI_MISO
PCH_SPI_MISO_2 — R438 WIN8@ 33_0402_5%

U13A — COUGARPOINT_FCBGA989

RTC: PCH_RTCX1 A20 RTCX1; PCH_RTCX2 C20 RTCX2; PCH_RTCRST# D20 RTCRST#; PCH_SRTCRST# G22 SRTCRST#; SM_INTRUDER# K22 INTRUDER#; PCH_INTVRMEN C17 INTVRMEN

IHDA: HDA_BITCLK_PCH N34 HDA_BCLK; HDA_SYNC_PCH L34 HDA_SYNC; PCH_SPKR T10 SPKR; HDA_RST_PCH# K34 HDA_RST#; HDA_SDIN0 E34 HDA_SDIN0; G34 HDA_SDIN1; C34 HDA_SDIN2; A34 HDA_SDIN3; HDA_SDOUT_PCH A36 HDA_SDO; C36 HDA_DOCK_EN# / GPIO33; N32 HDA_DOCK_RST# / GPIO13

JTAG: PCH_JTAG_TCK J3 JTAG_TCK; PCH_JTAG_TMS H7 JTAG_TMS; PCH_JTAG_TDI K5 JTAG_TDI; PCH_JTAG_TDO H1 JTAG_TDO

SPI: T3 SPI_CLK; Y14 SPI_CS0#; T1 SPI_CS1#; V4 SPI_MOSI; U3 SPI_MISO

LPC: FWH0 / LAD0 C38 LPC_AD0; FWH1 / LAD1 A38 LPC_AD1; FWH2 / LAD2 B37 LPC_AD2; FWH3 / LAD3 C37 LPC_AD3; FWH4 / LFRAME# D36 LPC_FRAME#; LDRQ0# E36; LDRQ1# / GPIO23 K36 — R118 10K_0402_5% — +3VS; SERIRQ V5 — SERIRQ — SERIRQ <42>

SATA 6G:
SATA0RXN AM3 SATA_PRX_DTX_N0; SATA0RXP AM1 SATA_PRX_DTX_P0; SATA0TXN AP7 SATA_PTX_C_DRX_N0 — C127 0.01U_0402_16V7K — SATA_PTX_DRX_N0; SATA0TXP AP5 SATA_PTX_C_DRX_P0 — C131 0.01U_0402_16V7K — SATA_PTX_DRX_P0
SATA_PRX_DTX_N0 <40> / SATA_PRX_DTX_P0 <40> / SATA_PTX_DRX_N0 <40> / SATA_PTX_DRX_P0 <40> — mSATA

SATA1RXN AM10 SATA_PRX_C_DTX_N1_R; SATA1RXP AM8 SATA_PRX_C_DTX_P1_R; SATA1TXN AP11 SATA_PTX_DRX_N1_R; SATA1TXP AP10 SATA_PTX_DRX_P1_R
SATA_PRX_C_DTX_N1_R <38> / SATA_PRX_C_DTX_P1_R <38> / SATA_PTX_DRX_N1_R <38> / SATA_PTX_DRX_P1_R <38> — HDD for HM77

SATA2RXN AD7 SATA_PRX_C_DTX_N2; SATA2RXP AD5 SATA_PRX_C_DTX_P2; SATA2TXN AH5 SATA_PTX_DRX_N2; SATA2TXP AH4 SATA_PTX_DRX_P2
SATA_PRX_C_DTX_N2 <38> / SATA_PRX_C_DTX_P2 <38> / SATA_PTX_DRX_N2 <38> / SATA_PTX_DRX_P2 <38> — HDD for HM70

SATA3RXN AB8; SATA3RXP AB10; SATA3TXN AF3; SATA3TXP AF1 — Disable w/ HM70

SATA4RXN Y7 SATA_PRX_C_DTX_N4; SATA4RXP Y5 SATA_PRX_C_DTX_P4; SATA4TXN AD3 SATA_PTX_DRX_N4; SATA4TXP AD1 SATA_PTX_DRX_P4
SATA_PRX_C_DTX_N4 <39> / SATA_PRX_C_DTX_P4 <39> / SATA_PTX_DRX_N4 <39> / SATA_PTX_DRX_P4 <39> — ODD

SATA5RXN Y3; SATA5RXP Y1; SATA5TXN AB3; SATA5TXP AB1

SATAICOMPO Y11 — L=500mil S=15mil — +1.05VS_VTT
SATAICOMPI Y10 — SATA_COMP — R121 37.4_0402_1%

SATA3RCOMPO AB12 — L=500mil S=15mil — +1.05VS_VTT
SATA3COMPI AB13 — SATA3_COMP — R126 49.9_0402_1%

SATA3RBIAS AH1 — RBIAS_SATA3 — R440 750_0402_1%

SATALED# P3 — PCH_SATALED# — R429 10K_0402_5%
SATA0GP / GPIO21 V14 — PCH_GPIO21 — R136 10K_0402_5% — +3VS
SATA1GP / GPIO19 P1 — BBS_BIT0_R — R466 10K_0402_5%

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

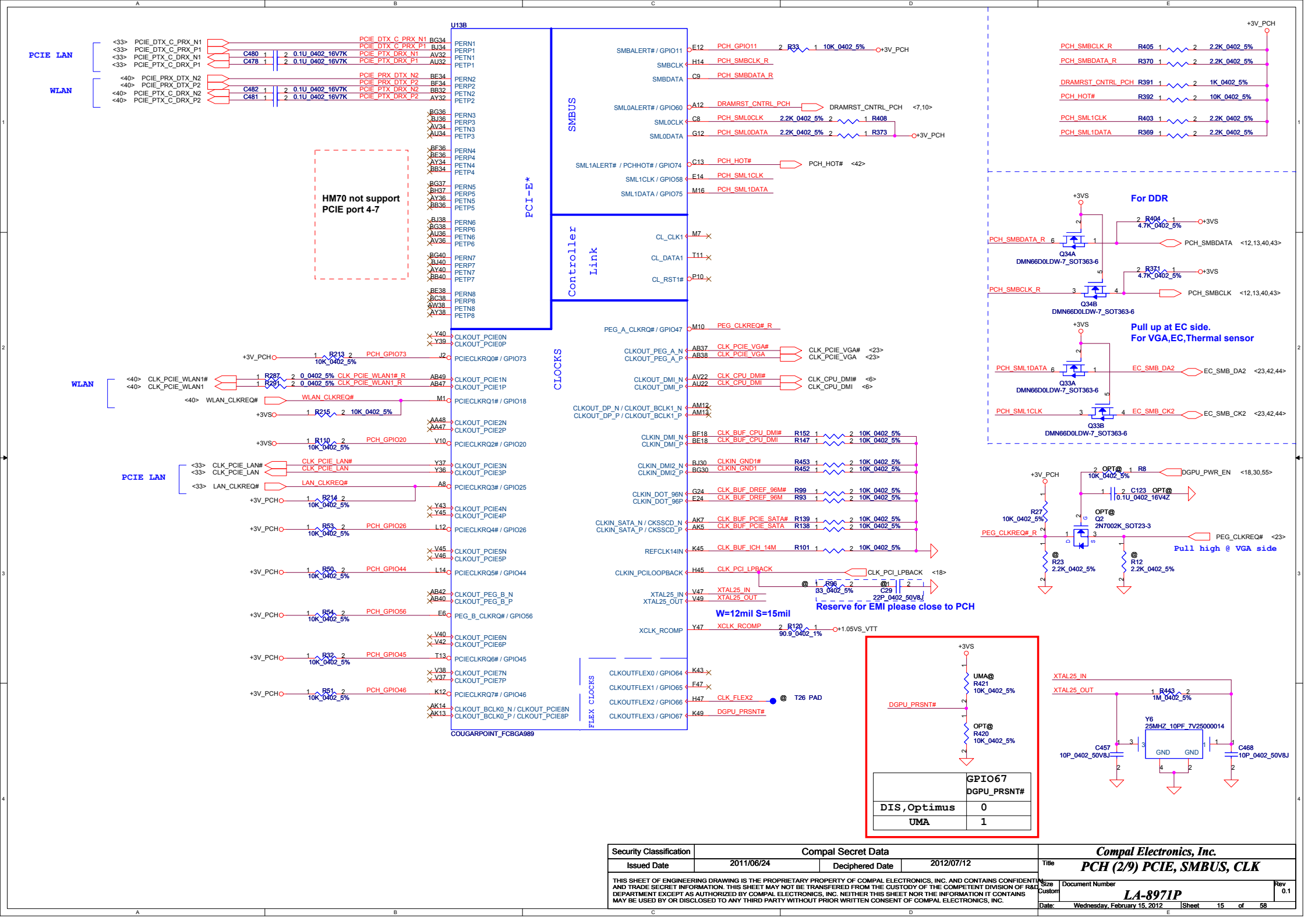
+3VS — R22 3.3K_0402_5% — PCH_SPI_CS0#_1 — SPI_WP1#
+3VS — R89 3.3K_0402_5% — SPI_HOLD1#
U44: CS# VCC 8; WP# SCLK 6; HOLD# SI 5; GND SO 2; 1 3 7 4
PCH_SPI_CLK_1; PCH_SPI_MOSI_1; PCH_SPI_MISO_1
MX25L3206EM2I-12G_SO8
SA000041P00
SPI ROM FOR ME (4MB)
Footprint 200mil

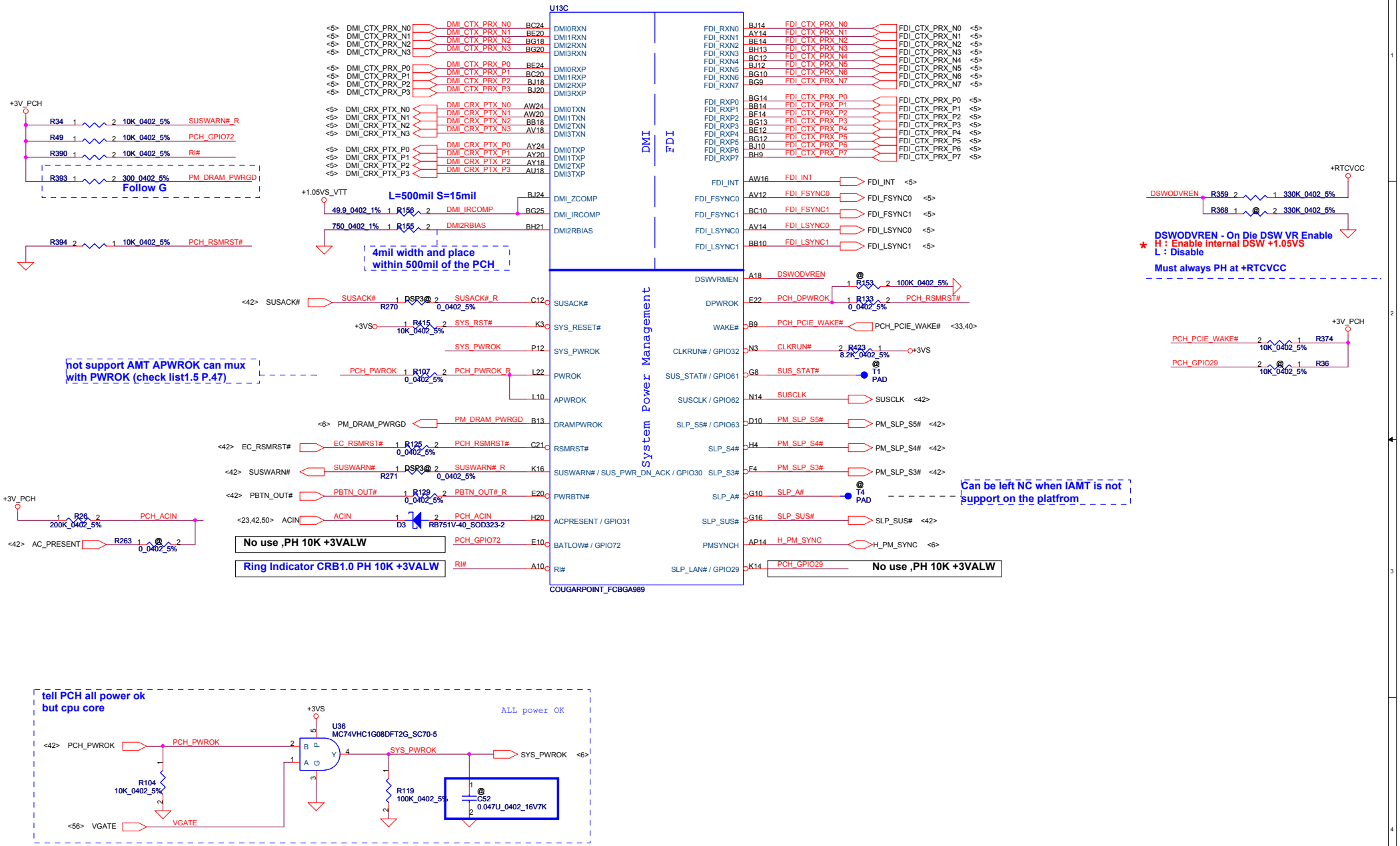
+3VS — R21 WIN8@ 3.3K_0402_5% — PCH_SPI_CS1#_2 — SPI_WP2#
+3VS — R88 WIN8@ 3.3K_0402_5% — SPI_HOLD2#
U46 WIN8@: CS# VCC 8; WP# SCLK 6; HOLD# SI 5; GND SO 2; 1 3 7 4
PCH_SPI_CLK_2; PCH_SPI_MOSI_2; PCH_SPI_MISO_2
MX25L1606EM2I-12G_SO8
SA000041N00
SPI ROM FOR ME (2MB)
Footprint 200mil

Reserve for EMI
@ C459 10P_0402_50V8J — @ R434 33_0402_5% — PCH_SPI_CLK

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

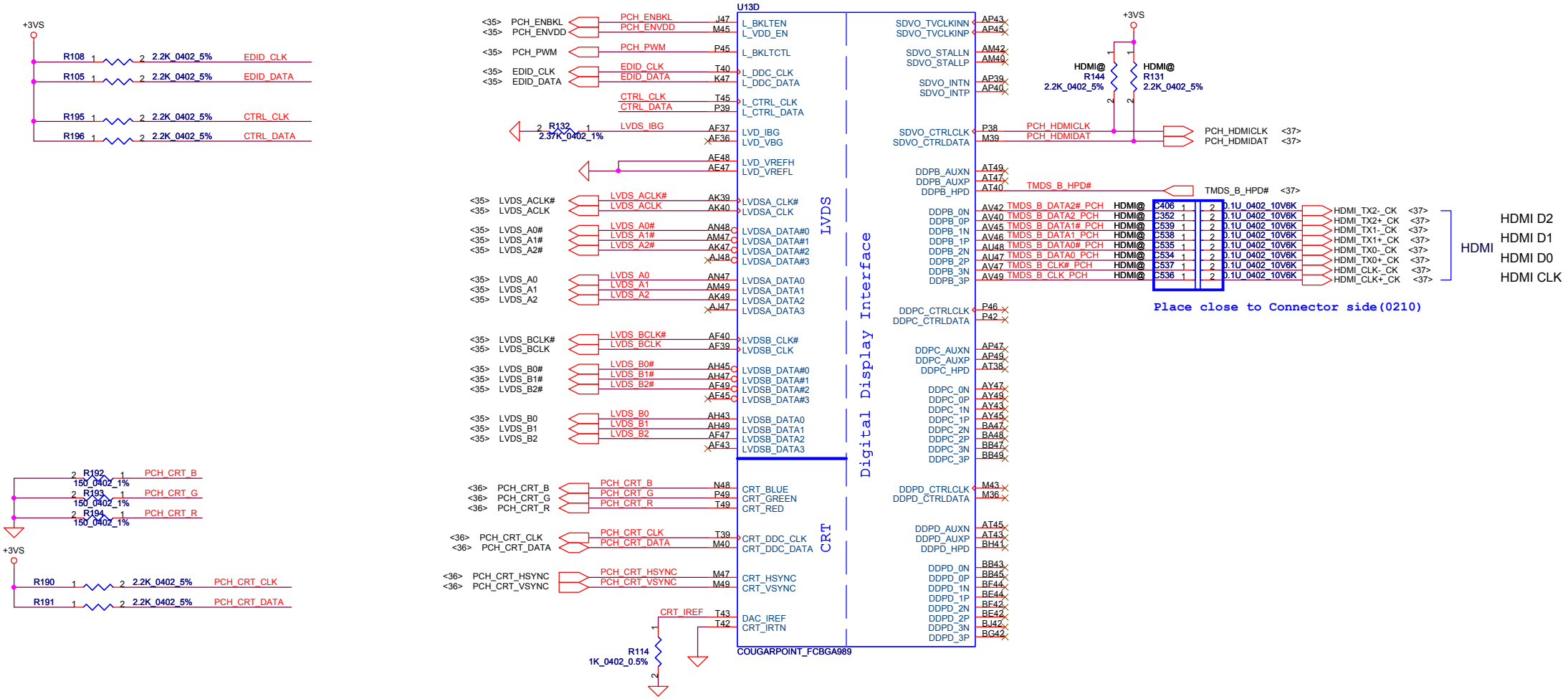
Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: LA-8971P | Rev: 0.1
Date: Wednesday, February 15, 2012 | Sheet 14 of 58


PCIE LAN
WLAN
PCIE LAN
WLAN
PCIE LAN
U13B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGARPOINT_FCBGA989
HM70 not support PCIE port 4-7
For DDR
Pull up at EC side.
For VGA,EC,Thermal sensor
Pull high @ VGA side
W=12mil S=15mil
Reserve for EMI please close to PCH
GPIO67
DGPU_PRSNT#
DIS,Optimus 0
UMA 1
Compal Secret Data
Issued Date 2011/06/24
Deciphered Date 2012/07/12
Compal Electronics, Inc.
PCH (2/9) PCIE, SMBUS, CLK
LA-8971P
Rev 0.1
Wednesday, February 15, 2012
Sheet 15 of 58



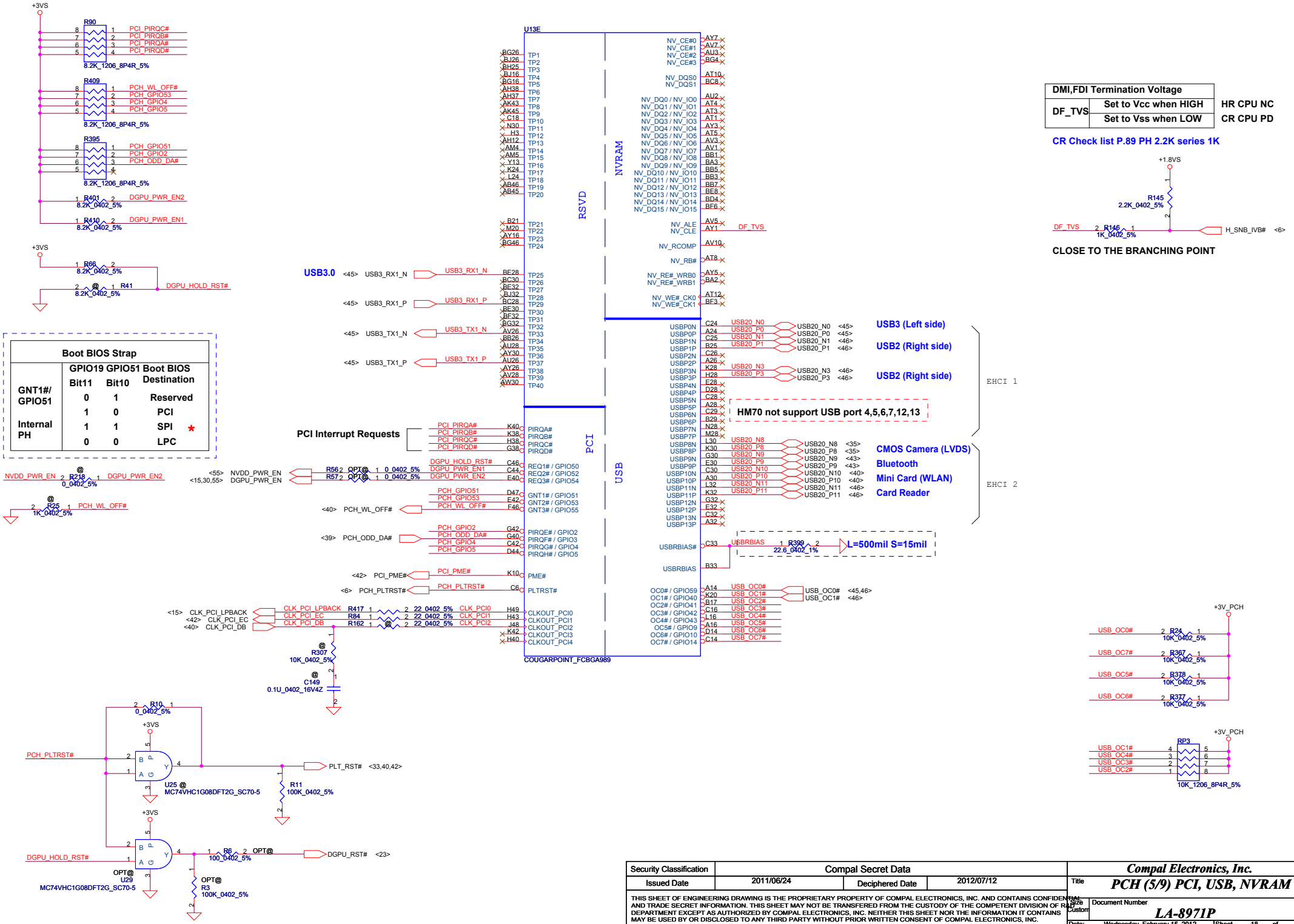
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: PCH (3/9) DMI,FDI,PM

Size: Custom	Document Number: LA-8971P		Rev: 0.1
Date: Wednesday, February 15, 2012	Sheet 16 of 58		



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	PCH (4/9) LVDS,CRT,DP,HDMI		
Size: Custom	Document Number: LA-8971P		Rev: 0.1
Date: Wednesday, February 15, 2012	Sheet 17 of 58		



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size	Document Number	Rev
Custom	LA-8971P	0.1

Date: Wednesday, February 15, 2012 Sheet 18 of 58

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3V_PCH — R411 4.7K_0402_5% — PCH_GPIO28 — @ R413 1K_0402_5% — Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

R83 @ 10K_0402_5% EC_LID_OUT#

+3VS — R439 200K_0402_5% ODD_DETECT#

+3V_PCH — R261 @ 1K_0402_5% EC_SMI#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled

+3VS — R115 10K_0402_5% mSATA_DET# — R71 10K_0402_5% DGPU_PWROK — R416 10K_0402_5% PCH_BT_ON# — R220 10K_0402_5% BT_DISABLE

+3V_PCH — R412 1K_0402_5% PCH_GPIO15

+3VS — R427 UMA@ 10K_0402_5% PCH_GPIO38 — R426 OPT@ 10K_0402_5%

*	PCH_GPIO38
OPT	0
UMA	1

+3VS — @ R55 10K_0402_5% — PCH_GPIO37 — R94 10K_0402_5%

Project ID	GPIO70		
*U510	1		

+3VS — @ R67 10K_0402_5% — PCH_GPIO69 — R42 10K_0402_5%
+3VS — R69 10K_0402_5% — PCH_GPIO70 — @ R44 10K_0402_5%
+3VS — @ R68 10K_0402_5% — PCH_GPIO71 — R43 10K_0402_5%

U13F

+3VS — R112 10K_0402_5% PCH_GPIO0 — T7 BMBUSY# / GPIO0
+3VS — R402 10K_0402_5% PCH_GPIO1 — A42 TACH1 / GPIO1
+3VS — R70 10K_0402_5% PCH_GPIO6 — H36 TACH2 / GPIO6
<42> EC_SCI# — E38 TACH3 / GPIO7
<42> EC_SMI# — C10 GPIO8
+3V_PCH — R376 10K_0402_5% PCH_GPIO12 — C4 LAN_PHY_PWR_CTRL / GPIO12
PCH_GPIO15 — G2 GPIO15
<40> mSATA_DET# — mSATA_DET# — U2 SATA4GP / GPIO16
<30,55> DGPU_PWROK — DGPU_PWROK — D40 TACH0 / GPIO17
<40> BT_DISABLE — BT_DISABLE — T5 SCLOCK / GPIO22
+3V_PCH — R92 10K_0402_5% PCH_GPIO24 — E8 GPIO24 / MEM_LED
<42> EC_LID_OUT# — EC_LID_OUT# — E16 GPIO27
PCH_GPIO28 — P8 GPIO28
BT ON/OFF <40,43> PCH_BT_ON# — PCH_BT_ON# — K1 STP_PCI# / GPIO34
R97 10K_0402_5% — PCH_GPIO35 — K4 GPIO35
<39> ODD_DETECT# — ODD_DETECT# — V8 SATA2GP / GPIO36
PCH_GPIO37 — M5 SATA3GP / GPIO37
PCH_GPIO38 — N2 SLOAD / GPIO38
R221 10K_0402_5% PCH_GPIO39 — M3 SDATAOUT0 / GPIO39
R128 10K_0402_5% PCH_GPIO48 — V13 SDATAOUT1 / GPIO48
+3VS — R111 10K_0402_5% PCH_GPIO49 — V3 SATA5GP / GPIO49
+3V_PCH — R52 10K_0402_5% PCH_GPIO57 — D6 GPIO57

GPIO

TACH4 / GPIO68 — C40 — ODD_EN# — ODD_EN# <39>
TACH5 / GPIO69 — B41 — PCH_GPIO69
TACH6 / GPIO70 — C41 — PCH_GPIO70
TACH7 / GPIO71 — A40 — PCH_GPIO71

CPU/MISC

A20GATE — P4 — GATEA20 — GATEA20 <42>
PECI — AU16 — PCH_PECI_R — @ 0_0402_5% — R158 — H_PECI — H_PECI <6,42>
RCIN# — P5 — KBRST# — KBRST# <42>
PROCPWRGD — AY11 — H_CPUPWRGD — H_CPUPWRGD <6>
THRMTRIP# — AY10 — PCH_THRMTRIP#_R — R159 390_0402_5% — H_THERMTRIP# — H_THERMTRIP# <6>
INIT3_3V# — T14

2 R106 10K_0402_5% +3VS

+3VS — ODD_EN# — R103 10K_0402_5%
KBRST# — R400 10K_0402_5%

CTRL+ALT+DEL
non CPU power ok
130c shut down

INIT3_3V Checklist1.5 P.69
This signal has weak internal
PU, can't pull low,leave NC

NC_1 — AH8
NC_2 — AK11
NC_3 — AH10
NC_4 — AK10
NC_5 — P37

NCTF

VSS_NCTF_1 — A4
VSS_NCTF_2 — A44
VSS_NCTF_3 — A45
VSS_NCTF_4 — A46
VSS_NCTF_5 — A5
VSS_NCTF_6 — A6
VSS_NCTF_7 — B3
VSS_NCTF_8 — B47
VSS_NCTF_9 — BD1
VSS_NCTF_10 — BD49
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE49
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF49
VSS_NCTF_15 — BG2
VSS_NCTF_16 — BG48
VSS_NCTF_17 — BH3
VSS_NCTF_18 — BH47
VSS_NCTF_19 — BJ4
VSS_NCTF_20 — BJ44
VSS_NCTF_21 — BJ45
VSS_NCTF_22 — BJ46
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ6
VSS_NCTF_25 — C2
VSS_NCTF_26 — C48
VSS_NCTF_27 — D1
VSS_NCTF_28 — D49
VSS_NCTF_29 — E1
VSS_NCTF_30 — E49
VSS_NCTF_31 — F1
VSS_NCTF_32 — F49

COUGARPOINT_FCBGA989

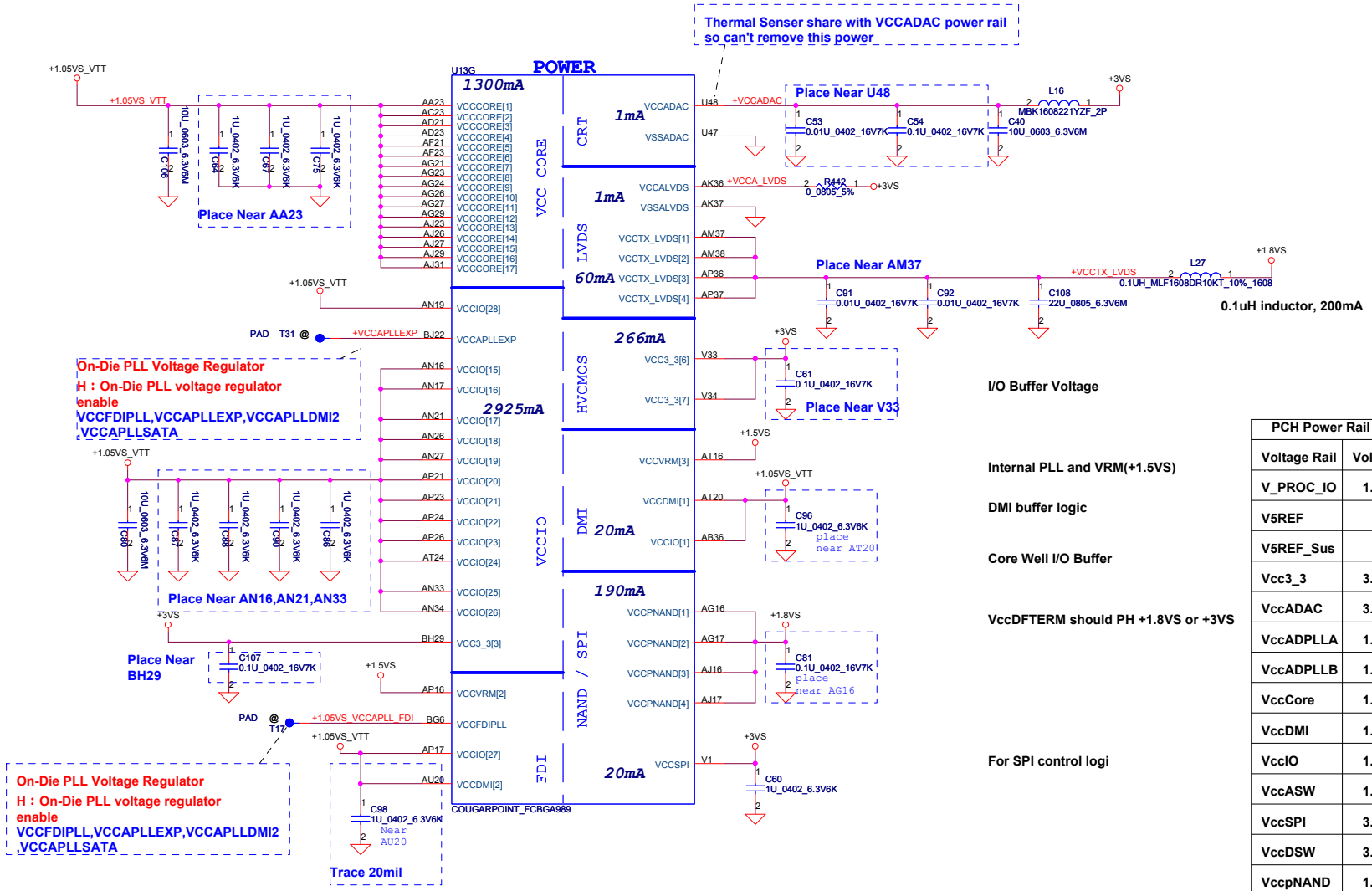
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-8971P | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 19 of 58



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

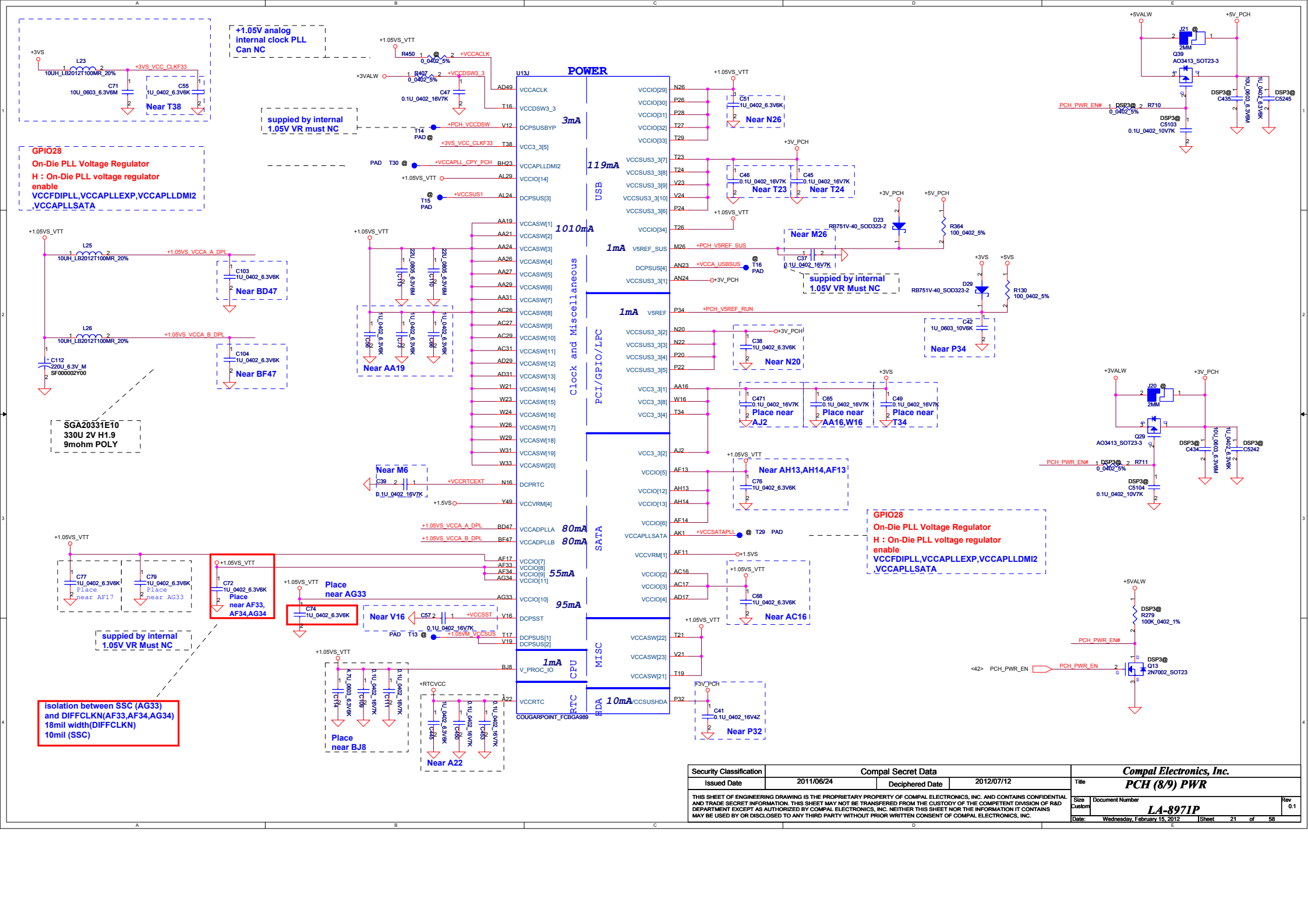
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-8971P | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 20 of 58


POWER
U13J
COUGARPOINT_FCBGA989
Clock and Miscellaneous
PCI/GPIO/LPC
USB
SATA
CPU
MISC
RTC
HDA
GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA
+1.05V analog internal clock PLL Can NC
suppied by internal 1.05V VR must NC
SGA20331E10
330U 2V H1.9
9mohm POLY
isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG33)
18mil width(DIFFCLKN)
10mil (SSC)
Near T38
Near BD47
Near BF47
Near AA19
Near M6
Near V16
Near N26
Near T23
Near T24
Near M26
Near N20
Near AH13,AH14,AF13
Near AC16
Near P34
Near P32
Place near AG33
Place near AF33, AF34,AG34
Place near BJ8
Place near A22
Place near AJ2
Place near AA16,W16
Place near T34
3mA
119mA
1010mA
1mA
80mA
55mA
95mA
10mA
Security Classification
Compal Secret Data
Issued Date
2011/06/24
Deciphered Date
2012/07/12
Compal Electronics, Inc.
PCH (8/9) PWR
LA-8971P
Rev 0.1
Wednesday, February 15, 2012
Sheet 21 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: LA-8971P | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 22 of 58

N13M-GS VID Default setup is 0.875V

GPIO	I/O	USAGE
GPIO0	O	GPU Core VID4
GPIO1	O	GPU Core VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU Core VID1
GPIO6	O	GPU Core VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU Core VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU Core VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved

U48A
Part 1 of 5
N13P-GV-S_FCBGA595~D

PCI EXPRESS
GPIO
DACA
TEST
I2C
CLK

<5> PEG_GTX_HRX_P[8..15] PEG_GTX_HRX_P[8..15]
<5> PEG_GTX_HRX_N[8..15] PEG_GTX_HRX_N[8..15]
<5> PEG_HTX_C_GRX_P[8..15] PEG_HTX_C_GRX_P[8..15]
<5> PEG_HTX_C_GRX_N[8..15] PEG_HTX_C_GRX_N[8..15]

+3VSDGPU
GPU_VID0 <55>
GPU_VID1 <55>
GPU_VID2 <55>
GPU_VID3 <55>
GPU_VID4 <55>
GPU_VID5 <55>

<42> ACIN_BUF
ACIN <16,42,50>
CH751H-40PT_SOD323-2

<15> CLK_PCIE_VGA
<15> CLK_PCIE_VGA#
<18> DGPU_RST#
<15> PEG_CLKREQ#
+3VSDGPU

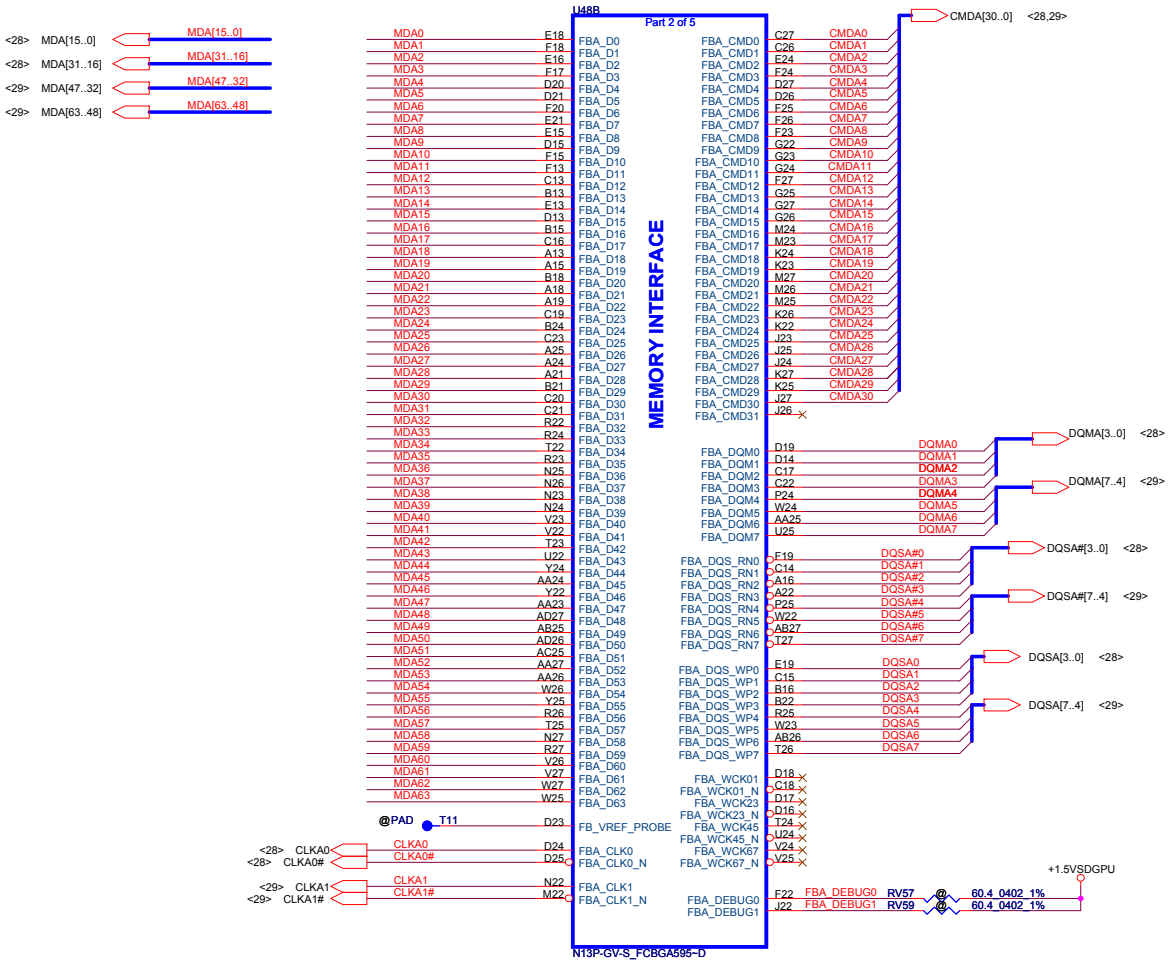
XTALOUT
XTALIN
Y1000 OPT@
27MHZ 10PF 7V27000050
XTAL_SSIN
XTAL_OUTBUFF

VGA_LCD_CLK
VGA_LCD_DATA
I2CS_SCL
I2CS_SDA

EC_SMB_CK2 <15,42,44>
EC_SMB_DA2 <15,42,44>
DMN66D0LDW-7_SOT363-6

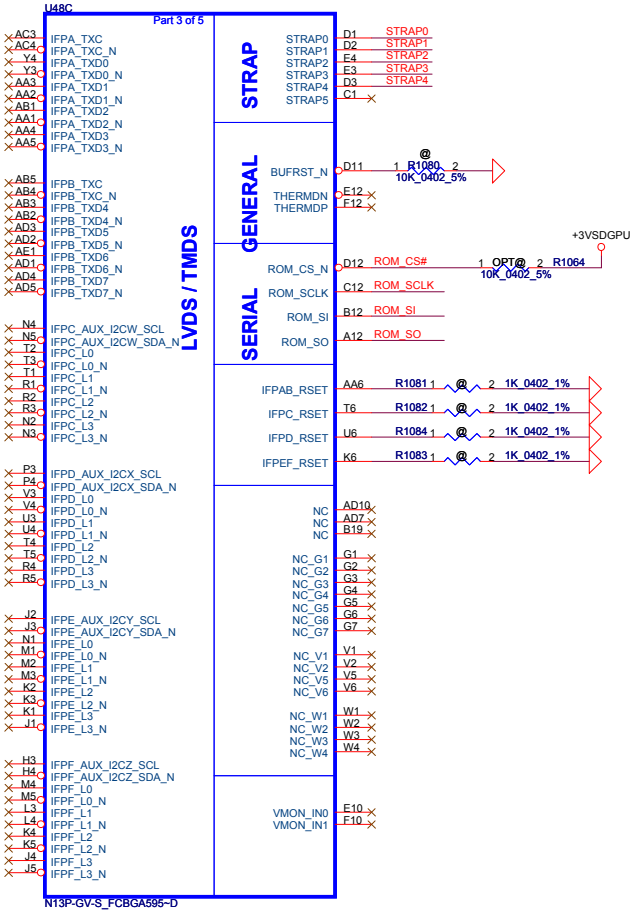
Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.
Title: N13M-GS 1/7
Size: Custom
Document Number: LA-8971P
Rev: 0.1
Date: Wednesday, February 15, 2012
Sheet 23 of 58

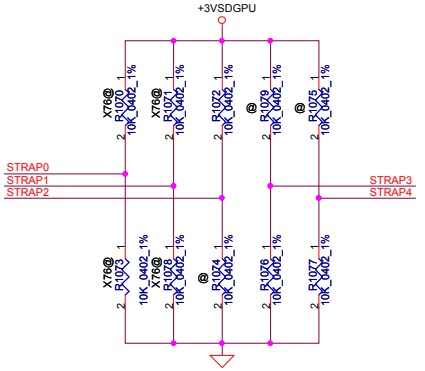


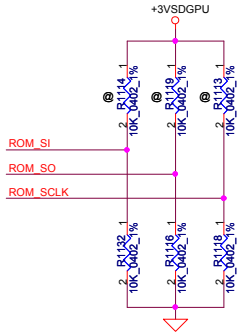
Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: N13M-GS 2/7			
Size: Custom	Document Number: LA-8971P		Rev: 0.1
Date: Wednesday, February 15, 2012	Sheet 24 of 58		



Straps





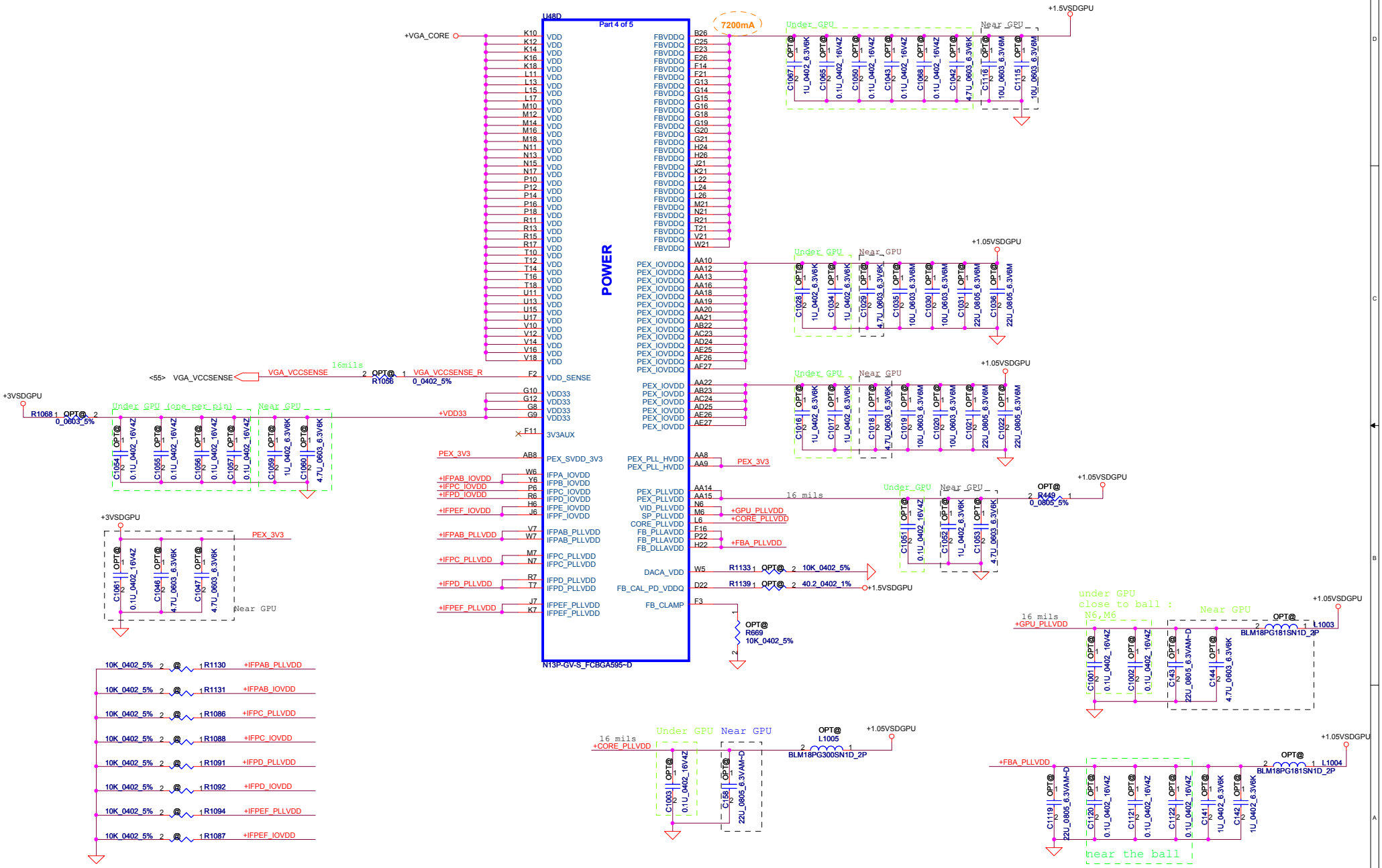
For N13M-GS strap table

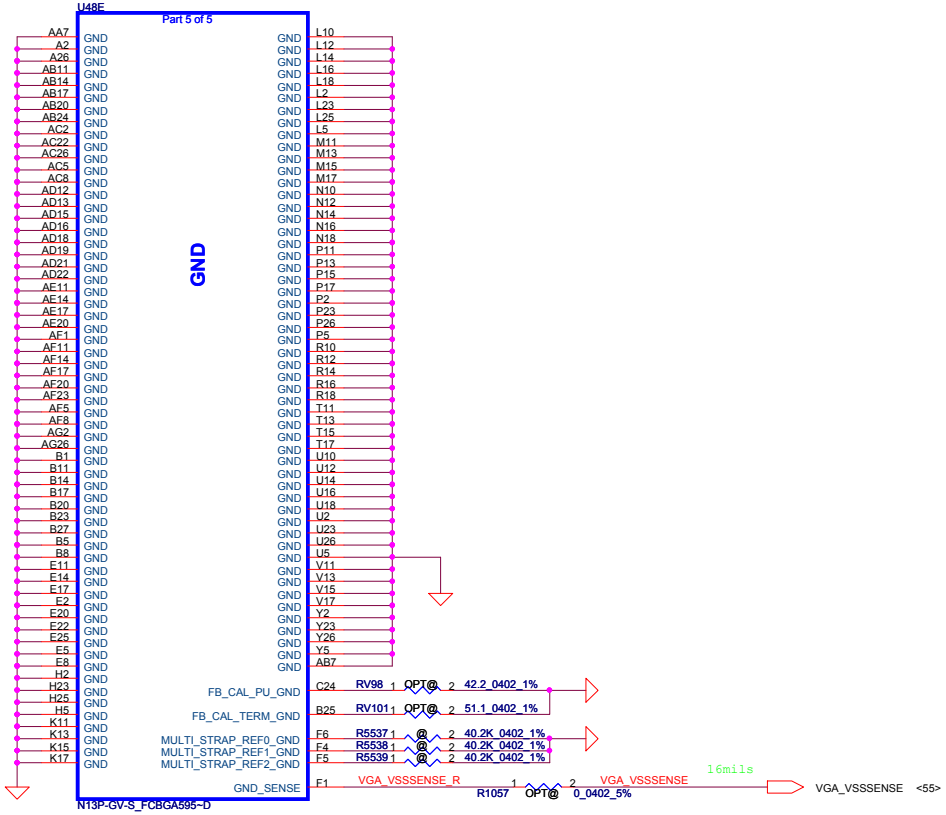
GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 4 1GB	Hynix SA00003YO00	R1073 PD 10K	R1071 PU 10K	R1072 PU 10K	R1076 PD 10K	R1077 PD 10K	R1132 PD 10K	R1116 PD 10K	R1118 PD 10K
	900 MHz	128M* 16* 4 1GB	Samsung SA000047Q00	R1070 PU 10K	R1078 PD 10K	R1072 PU 10K	R1076 PD 10K	R1077 PD 10K	R1132 PD 10K	R1116 PD 10K	R1118 PD 10K
	900 MHz										
	900 MHz										

SA000047Q00:S IC D3 128M16 K4W2G1646C-HC11 FBGA 96P

SA00003YO00:S IC D3 128MX16 H5TQ2G63BFR-11C FBGA 96P

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/05/23	Deciphered Date 2012/12/31	Title: N13M-GS 3/7
			Size: Custom; Document Number: LA-8971P; Rev: 0.1
			Date: Wednesday, February 15, 2012; Sheet 25 of 58





Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.

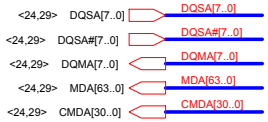
Title: N13M-GS 5/7

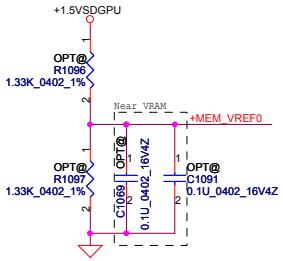
Size: Custom | Document Number: LA-8971P | Rev: 0.1

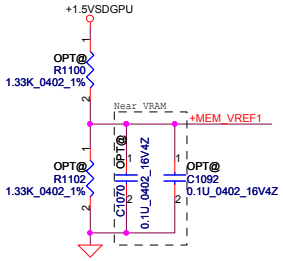
Date: Wednesday, February 15, 2012 | Sheet 27 of 58

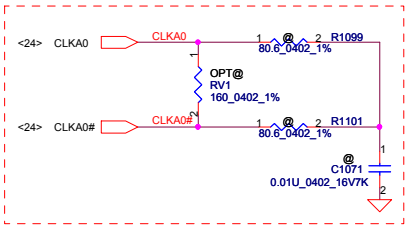
VRAM DDR3 chips (1GB)

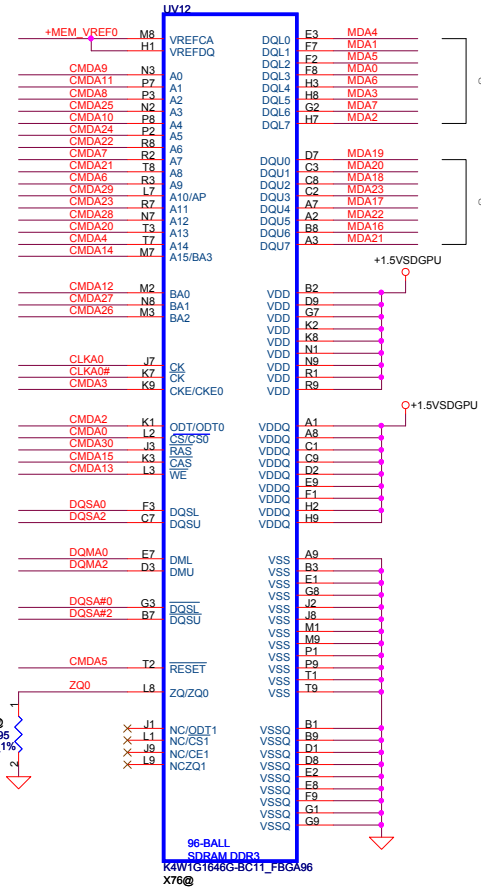
128Mx16 DDR3 *4==>1GB

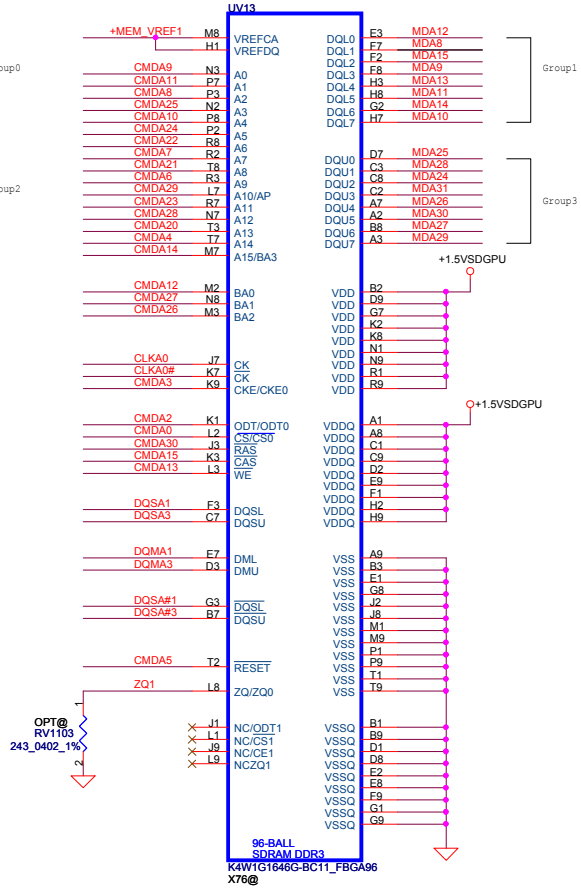






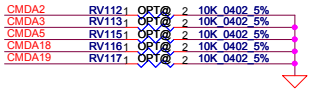


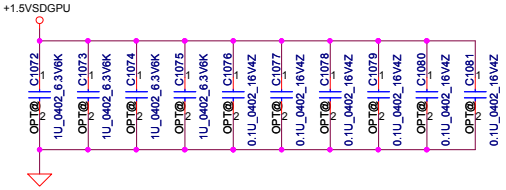


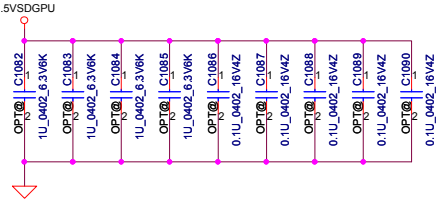


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination







Samsung :

Hynix :

Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	N13M-GS 6/7		
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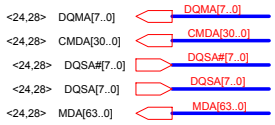
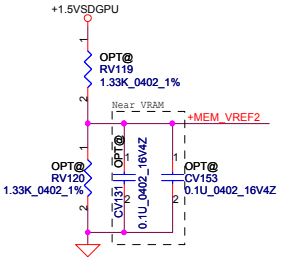
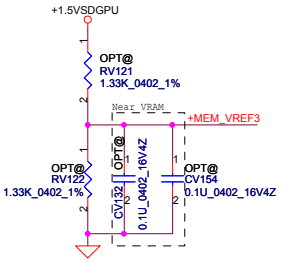
Date:	Wednesday, February 15, 2012	Sheet	28 of 58

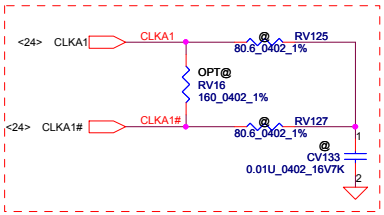
VRAM DDR3 chips (1GB)

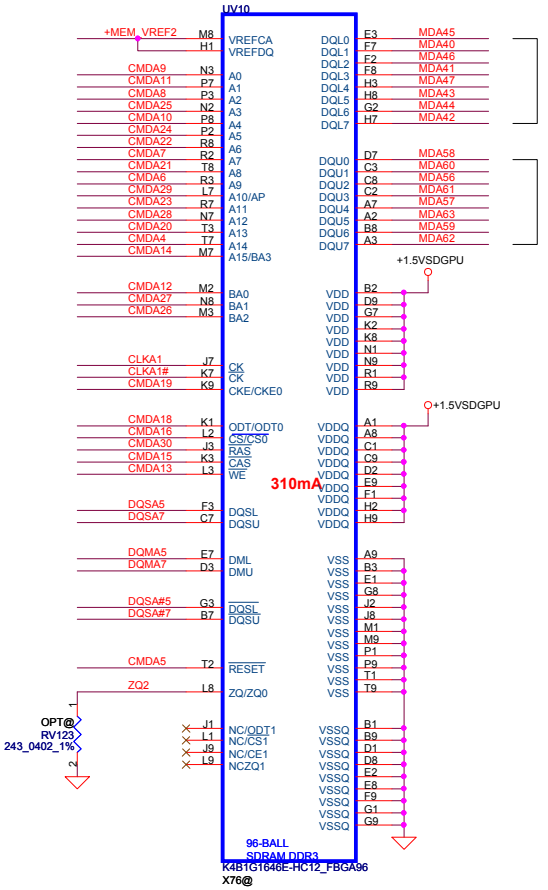
128Mx16 DDR3 *4==>1GB

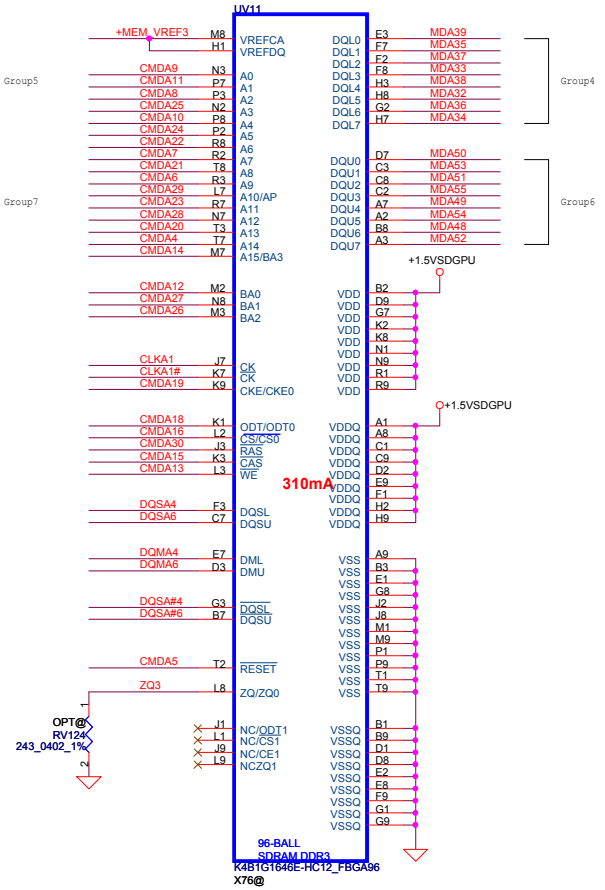


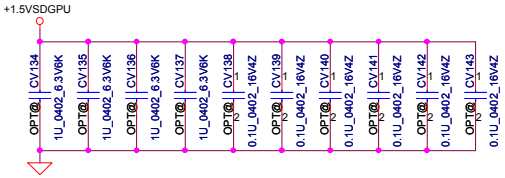


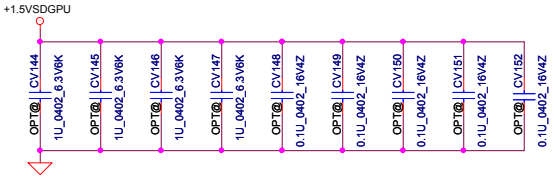












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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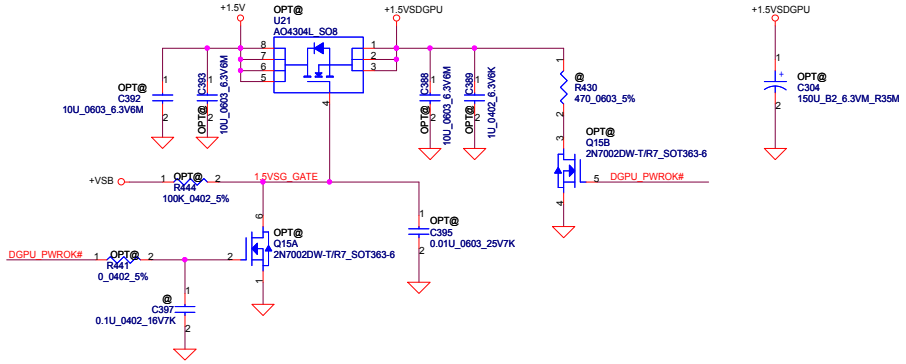
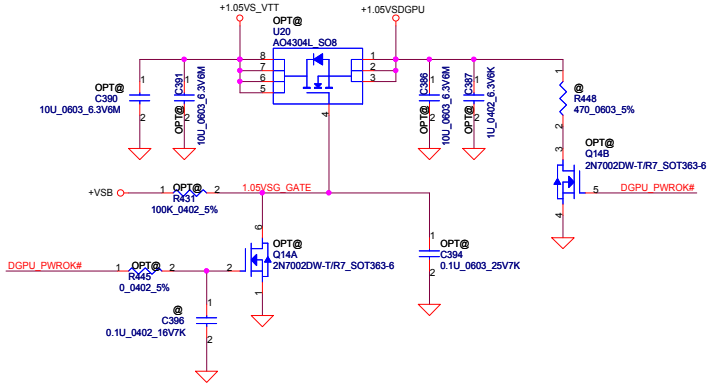
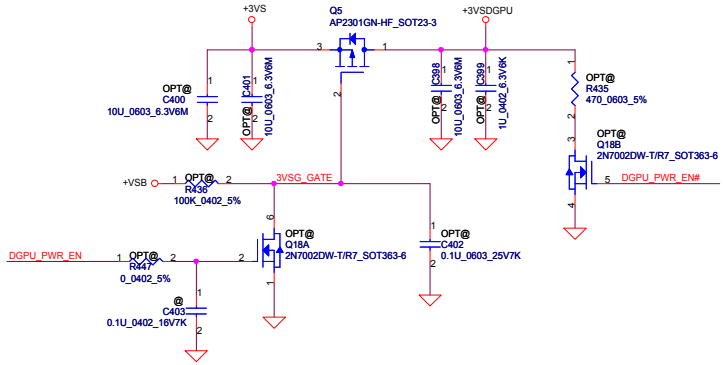
+1.5V to +1.5VSDGPU

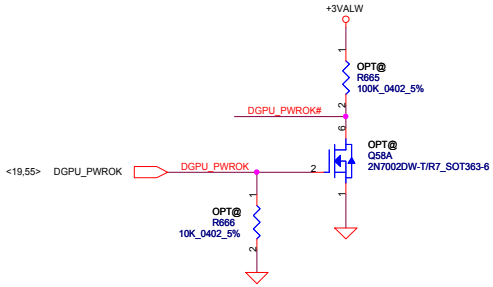


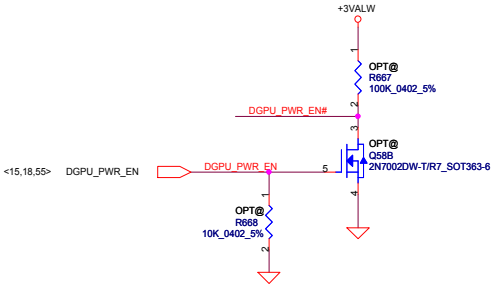
+VCCP to +1.05VSDGPU



+3VS to +3VSDGPU







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: N13M-GE1-S-A1			
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600ohms @100MHz 1A
P/N: SM01000BU00

600ohms @100MHz 2A
P/N: SM01000EE00

Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

U50
ALC269Q-VC2-GR_QFN48_6X6

Internal Speaker
Headphone
Internal D-MIC
external MIC

COMBO JACK detect (Normal OPen)

MIC Sense
R1543 place near pin13

Capless HP Sense
R940 place near pin34

Place near Pin25
Place near Pin38
Place near Pin1
Place near Pin9
Place next to pin 27

wide 40 mils

EMI

PC Beep
EC Beep
PCH Beep

Reserve for ESD request.

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

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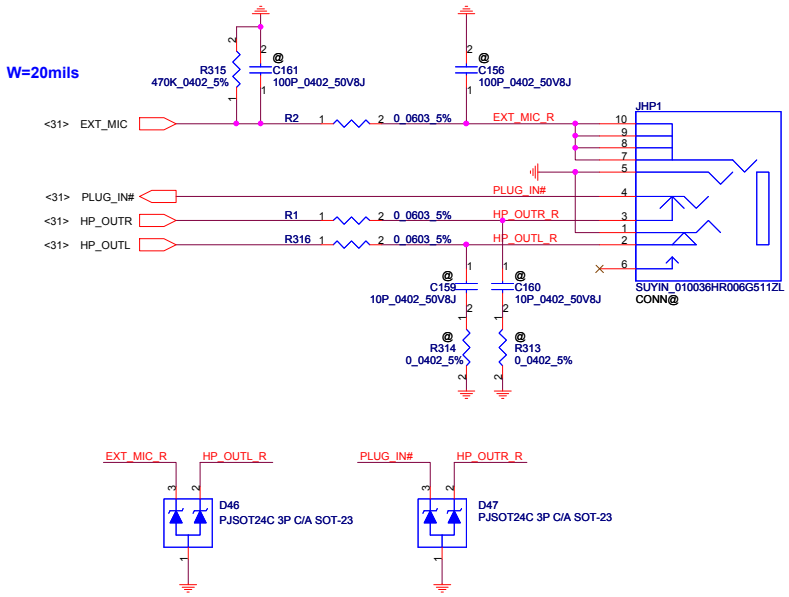
Compal Electronics,Ltd.
Title: HD Audio Codec ALC269Q-VC
Size: C | Document Number: LA-8971P | Rev: 0.1
Date: Wednesday, February 15, 2012 | Sheet 31 of 58



PN: SCA00000T00

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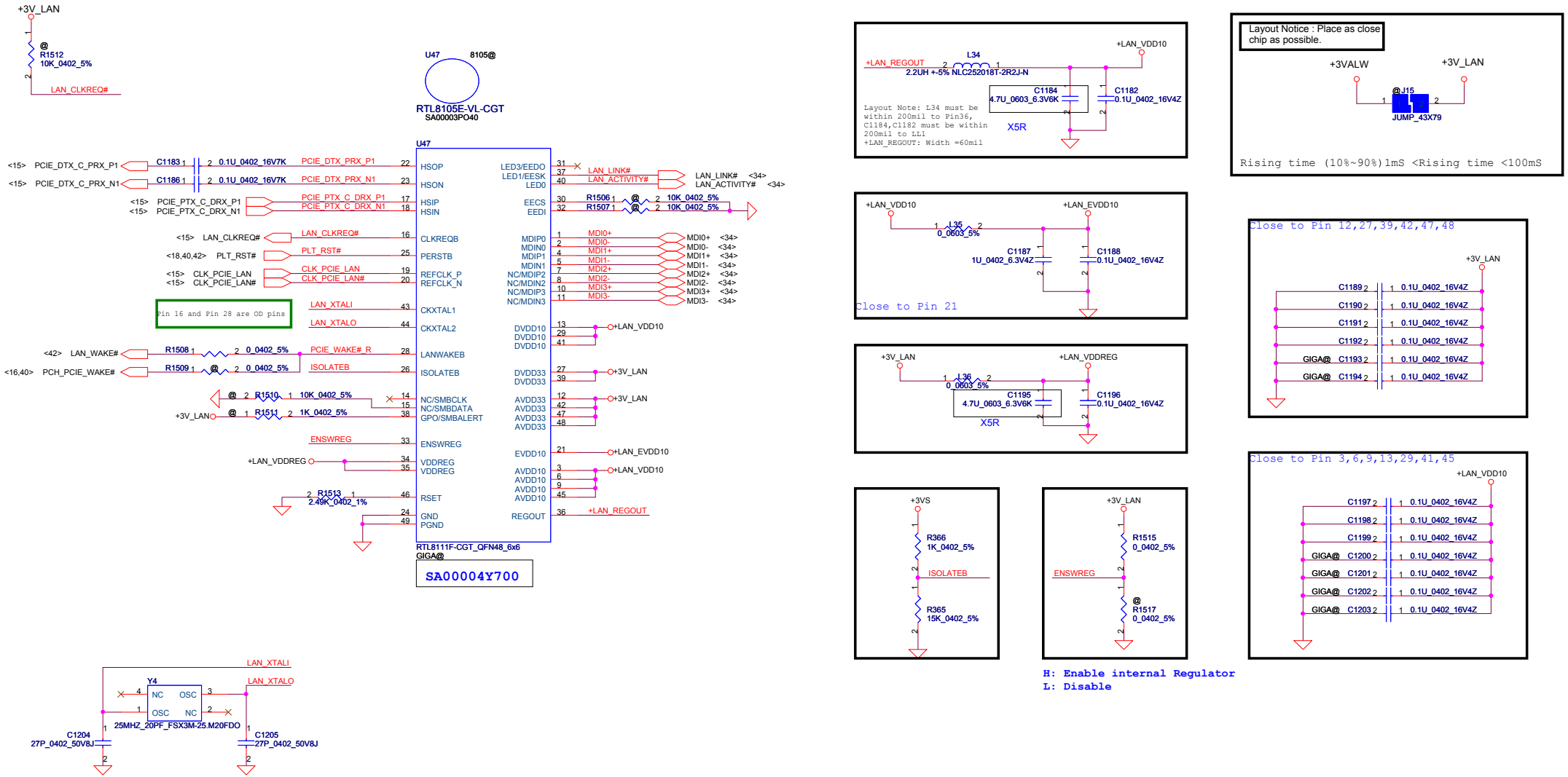
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: Audio Combo Jack

Size: Custom | Document Number: LA-8971P | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 32 of 58



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-RTL8111F/8105E

Size	Document Number	Rev
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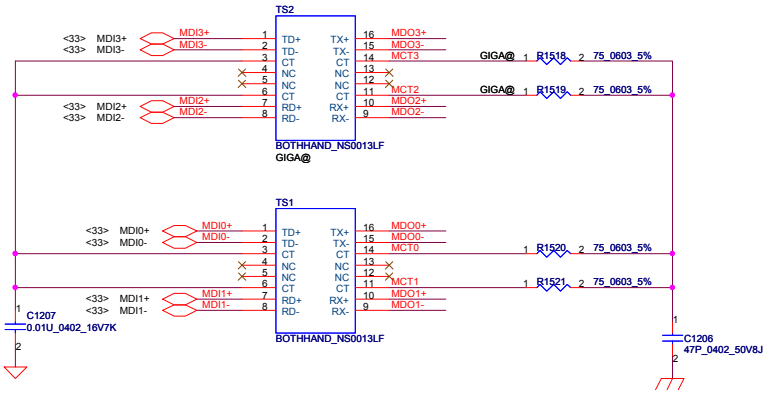
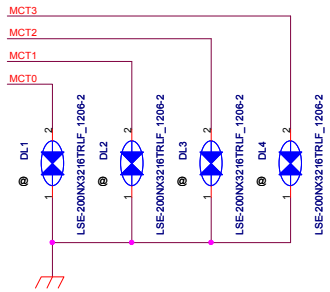
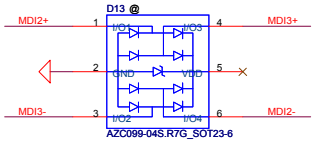
Date: Wednesday, February 15, 2012 Sheet 33 of 58



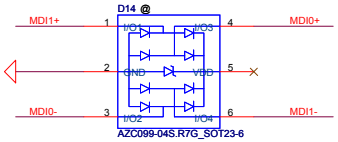
Reserve gas tube for EMI go rural solution

Place Close to TS1,TS2

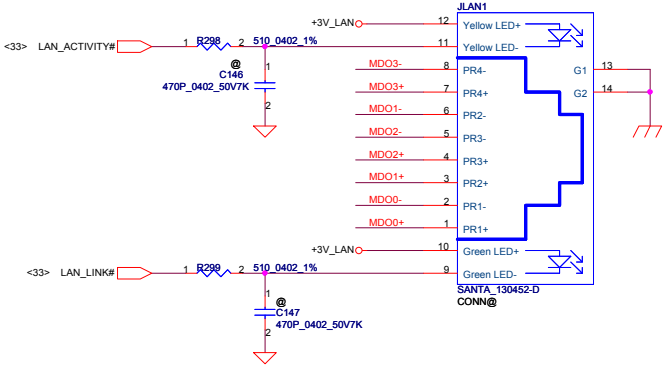


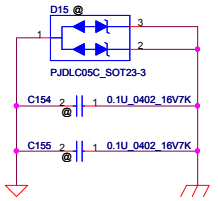


Place Close to TS2



Place Close to TS1





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN_Transformer

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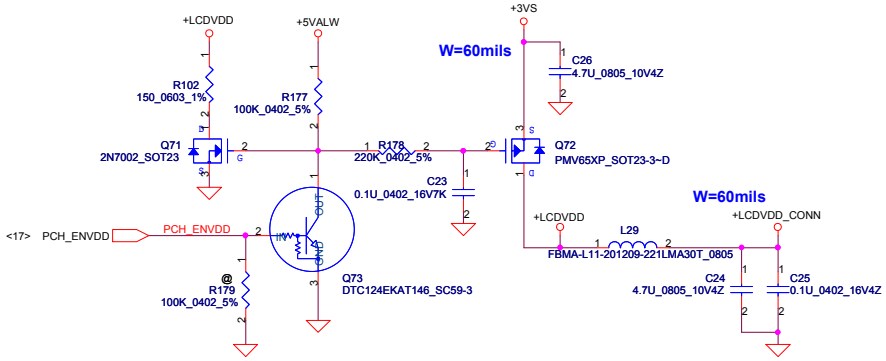
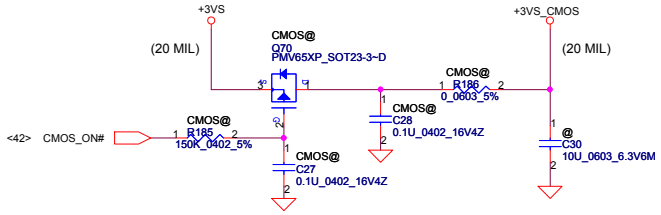
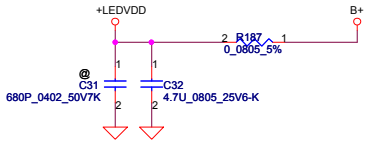
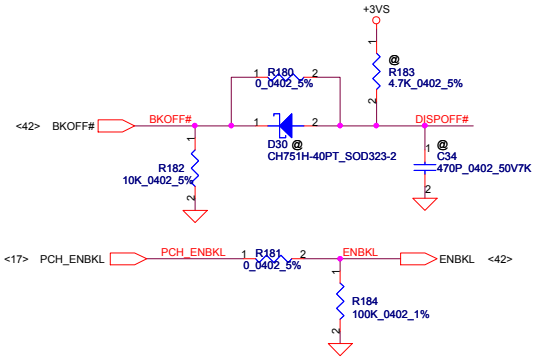
LCD POWER CIRCUIT

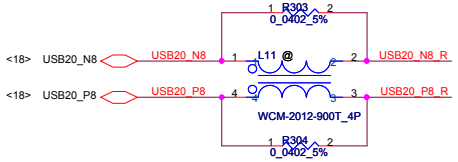


CMOS Camera

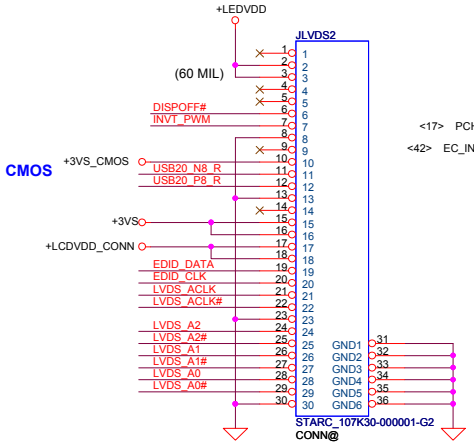


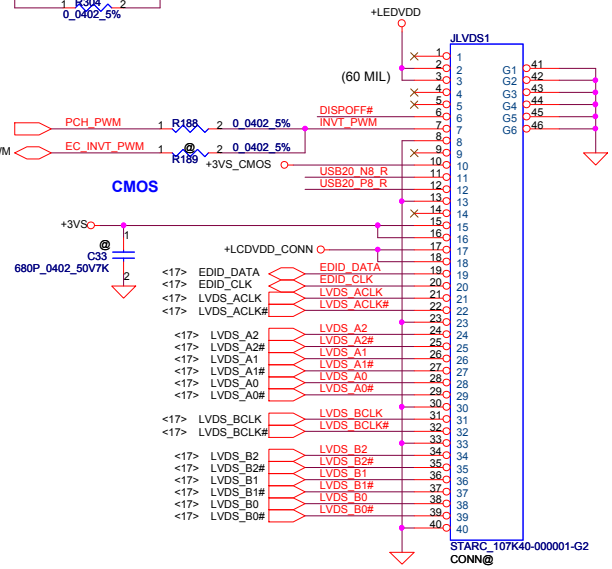






LCD Conn.





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: LVDS/CAMERA			
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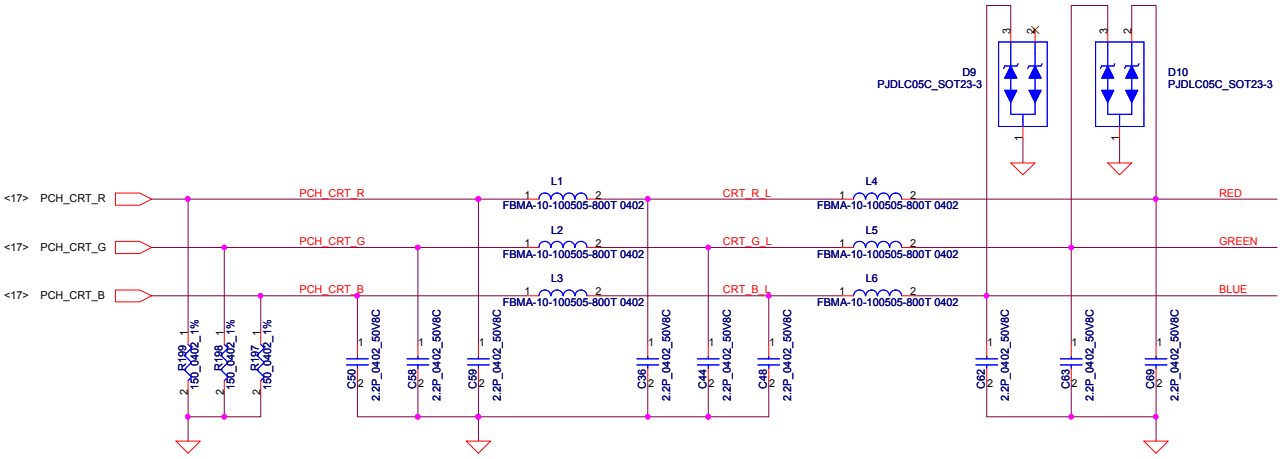
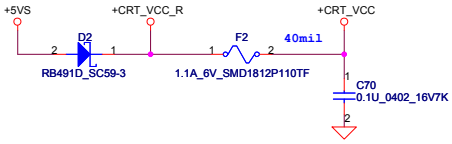
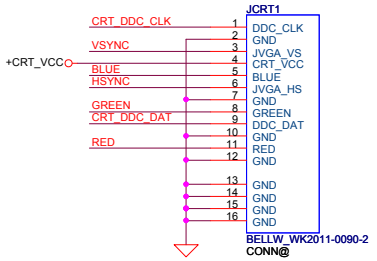
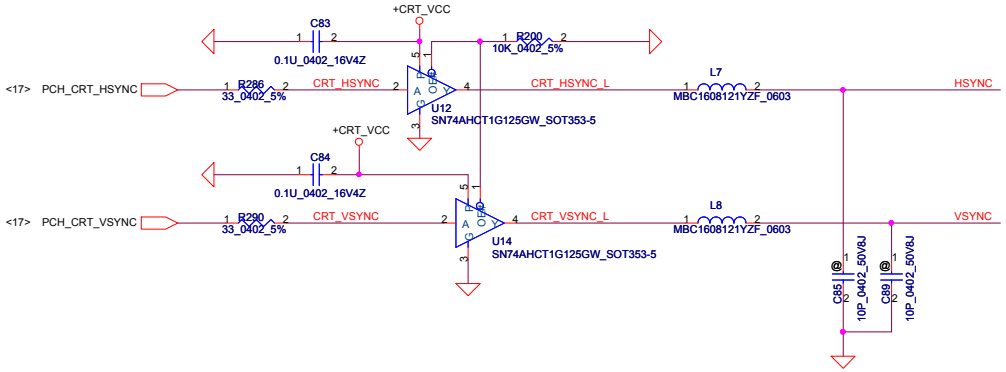
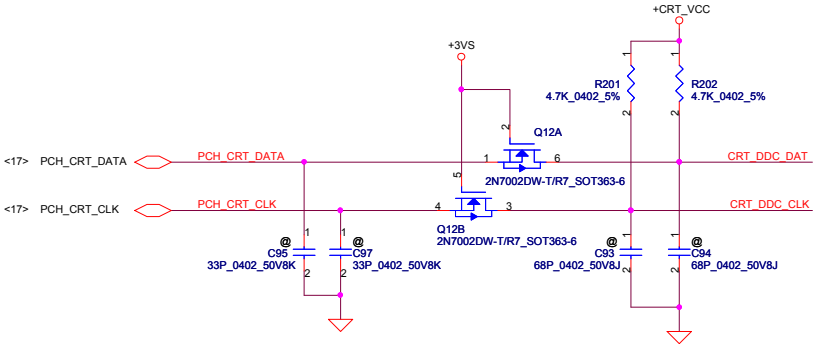


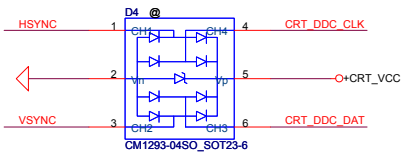


Mini-VGA CONNECTOR

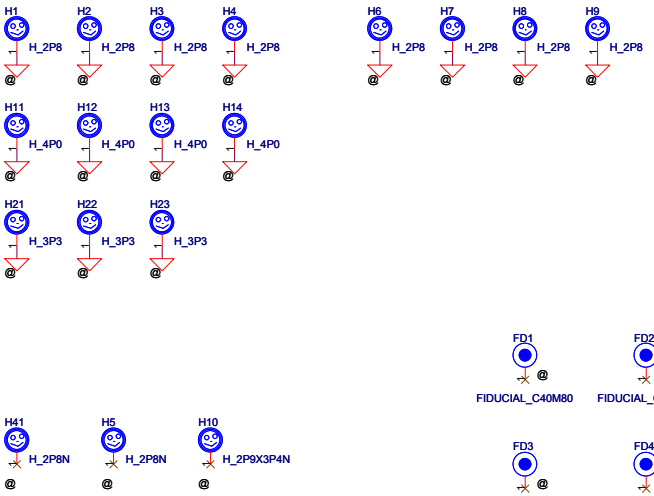








Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: Mini-VGA & Screw Hole

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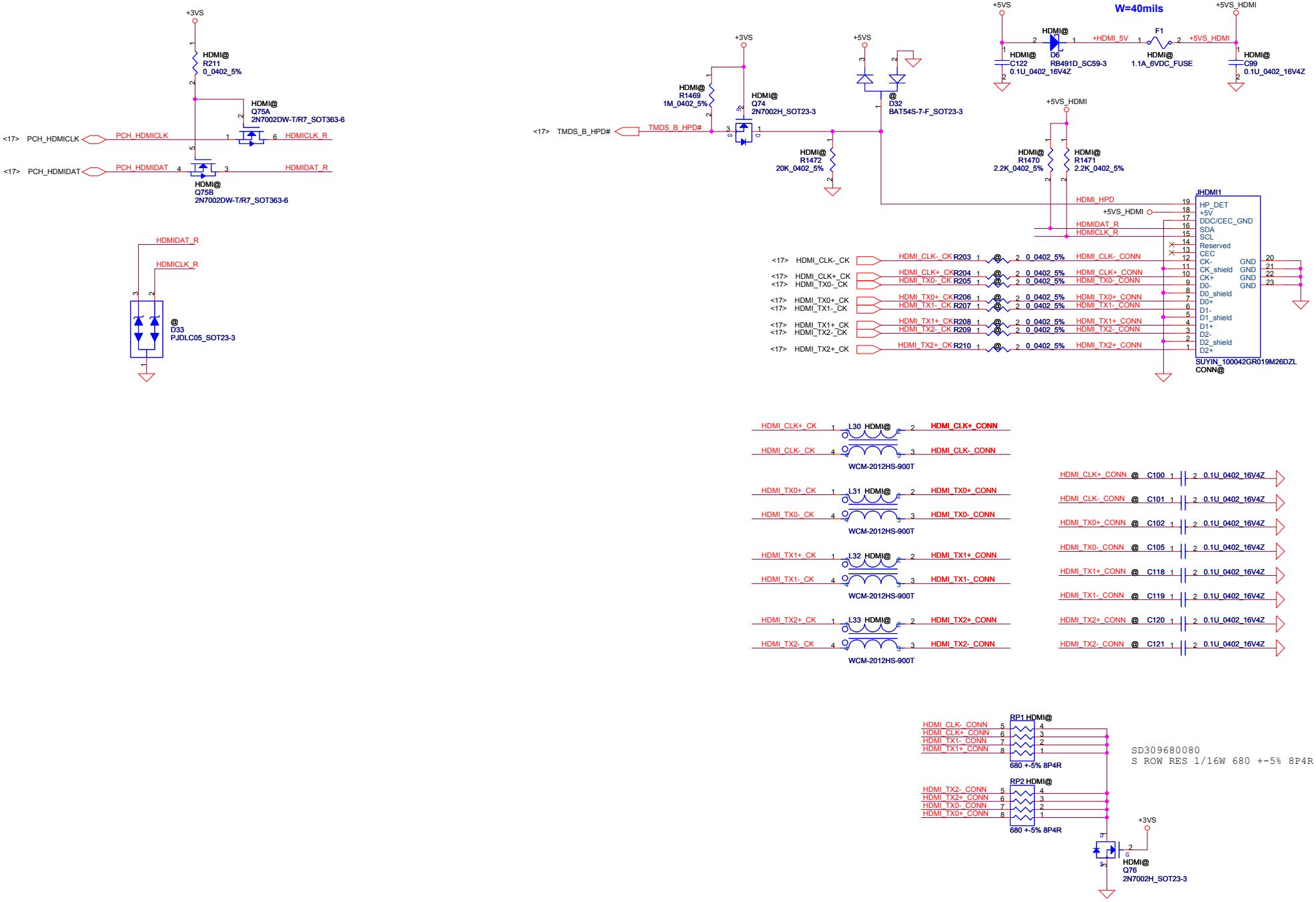

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: HDMI CONN

Size	Document Number	Rev
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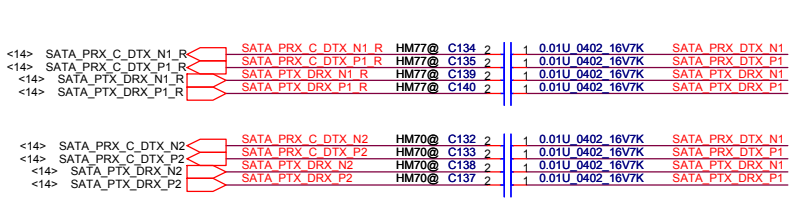
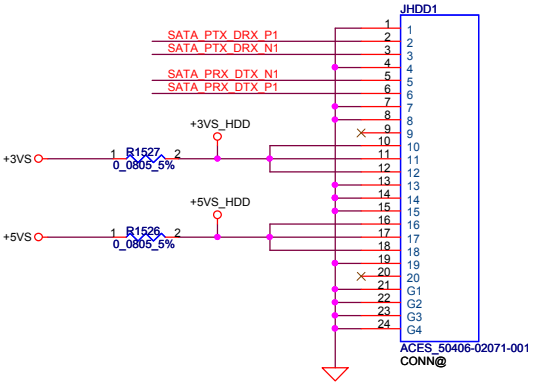
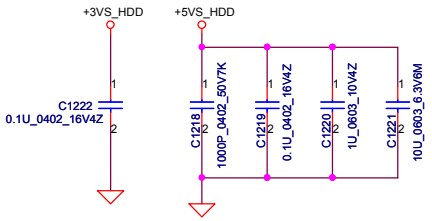
SATA HDD Conn.







Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SATA HDD Connector

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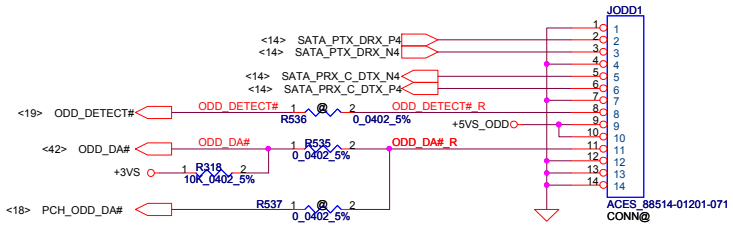
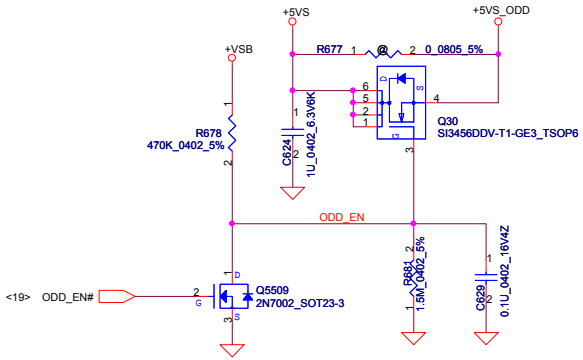
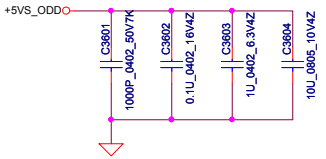
SATA ODD FFC CONN.





Place caps. near ODD CONN.



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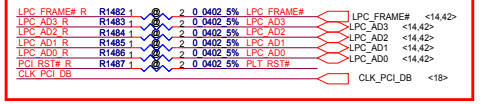
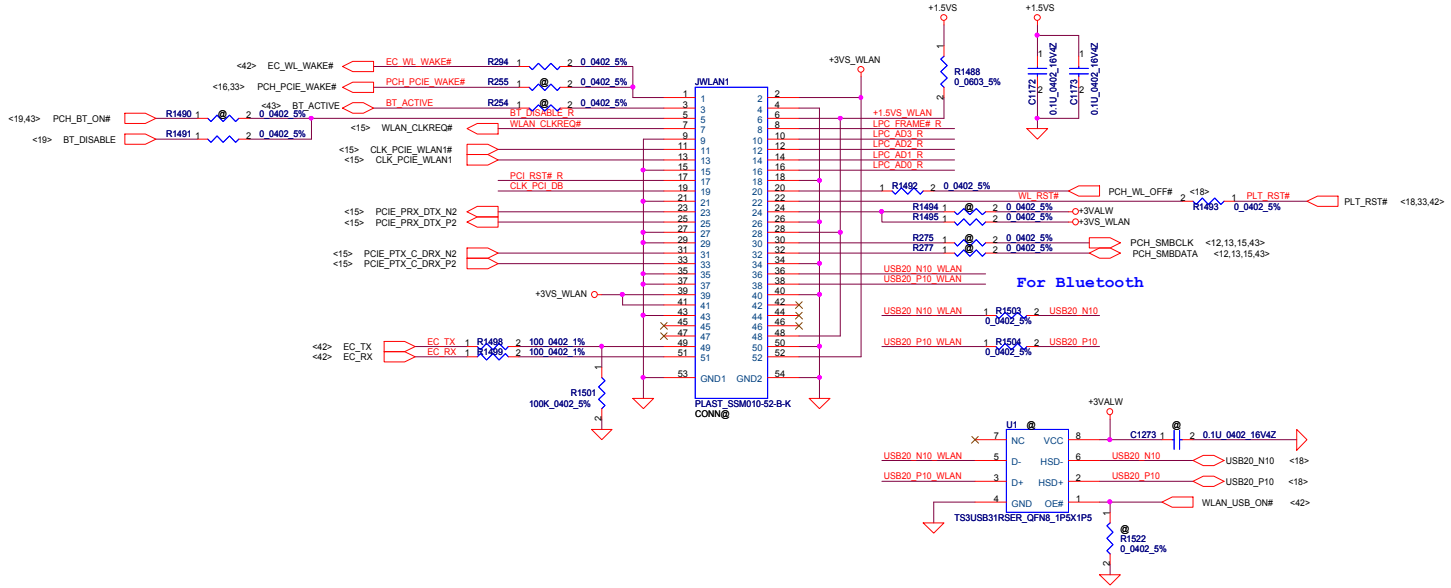
Issued Date	2011/07/12	Deciphered Date 2012/12/31	Title: SATA ODD Conn

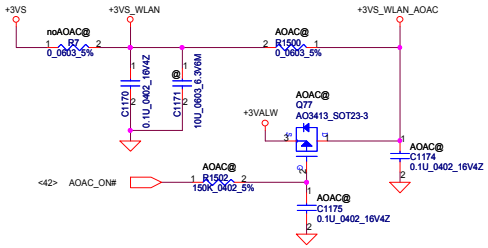
Size	Document Number	Rev
Custom	LA-8971P	0.3
Date: Wednesday, February 15, 2012	Sheet 39 of 58	

Mini-Express Card for WLAN with BT(Half)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

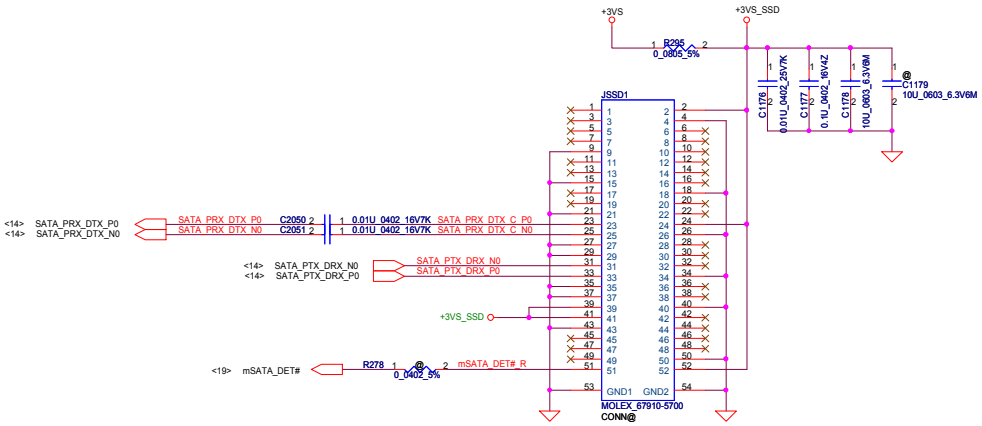






Mini-Express Card for SSD(Full)

SSD Active:4.5W(1.5A)



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	W/L & m-SATA Card		
Size	Document Number		Rev
	LA-8971P		0.1
Date:	Wednesday, February 15, 2012	Sheet	40 of 58

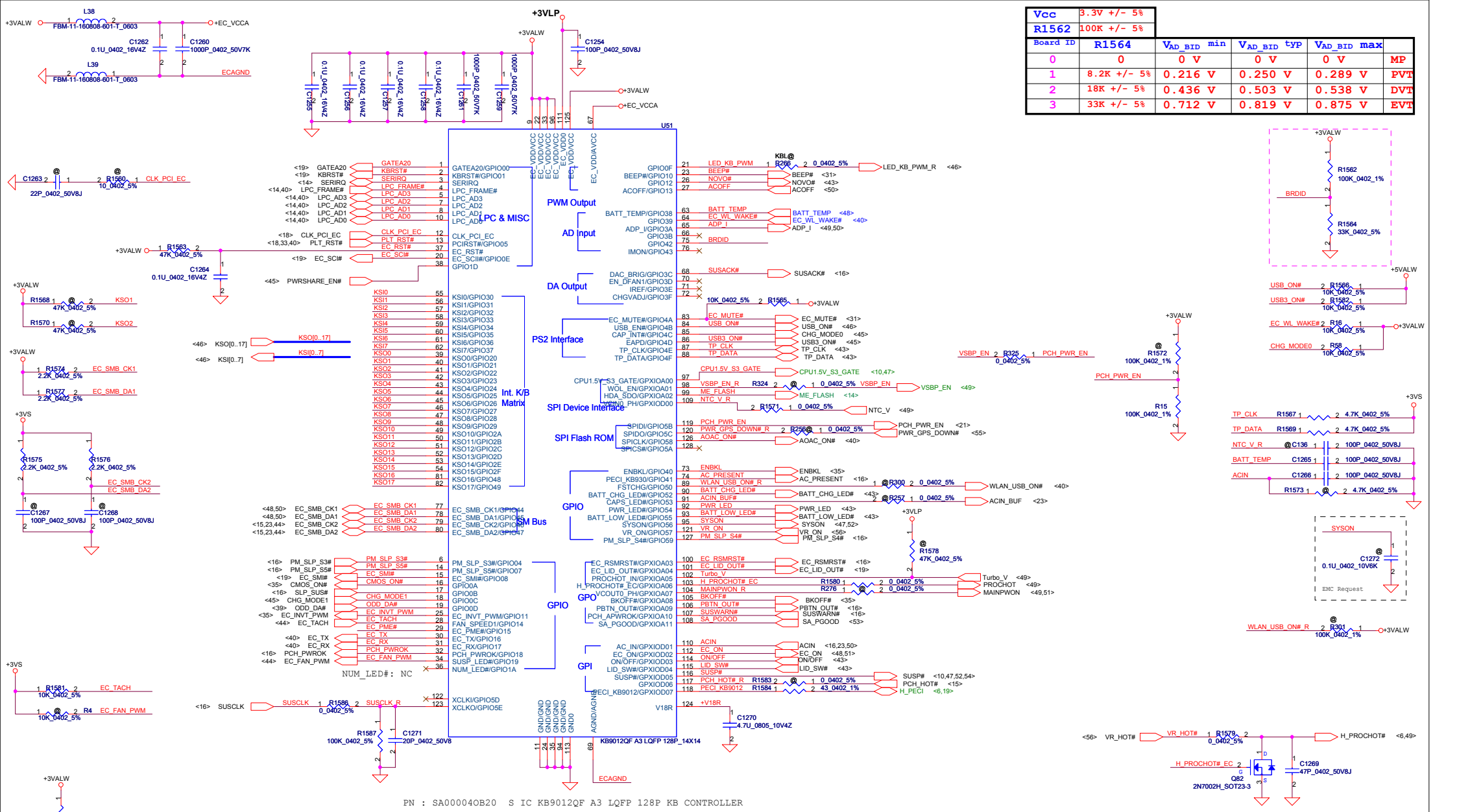
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **NULL**

Size	Document Number	Rev
Custom	LA-8971P	0.3

Date: Wednesday, February 15, 2012 | Sheet 41 of 58



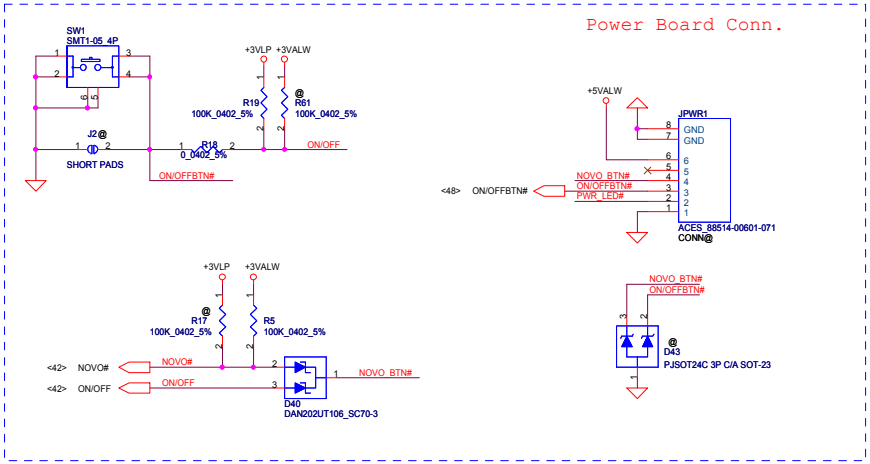
Vcc	3.3V +/- 5%
R1562	100K +/- 5%

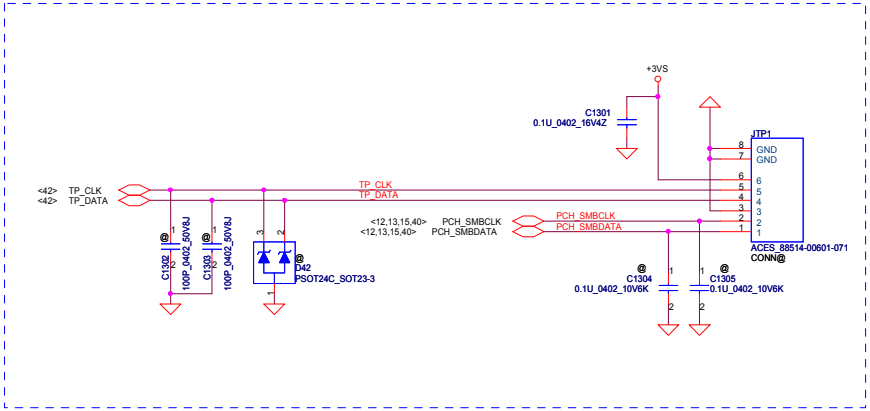
Board ID	R1564	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

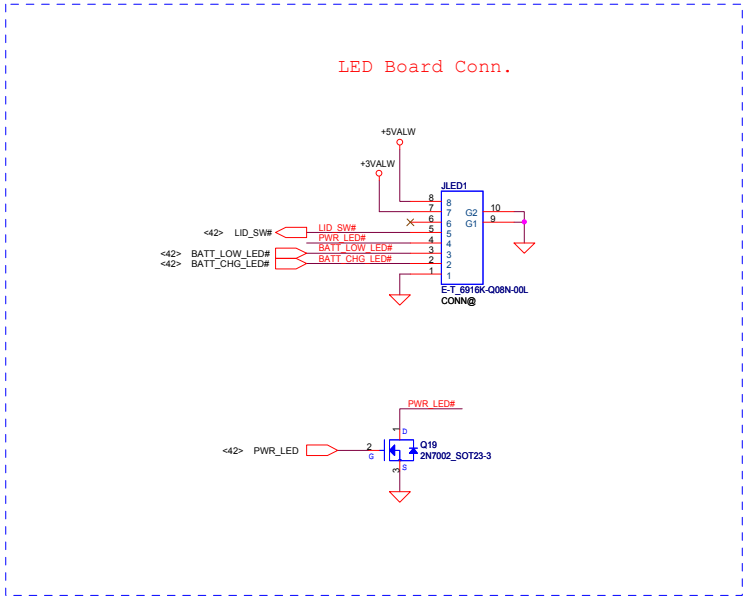
Compal Electronics, Inc.
Title: ENE_KB9012
Size: Custom
Document Number: LA-8971P
Rev: 0.1
Date: Wednesday, February 15, 2012
Sheet 42 of 58

Power Board Conn.

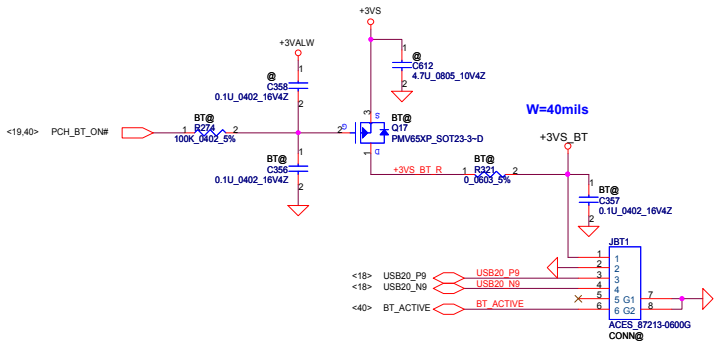




LED Board Conn.



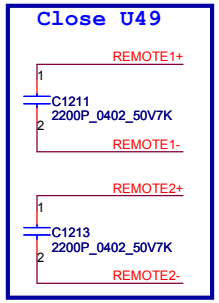
Blue Tooth Moudle

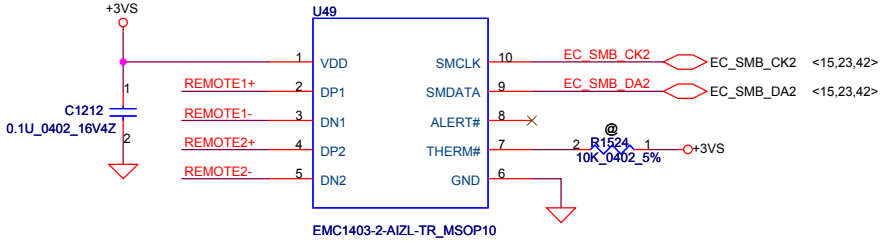


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

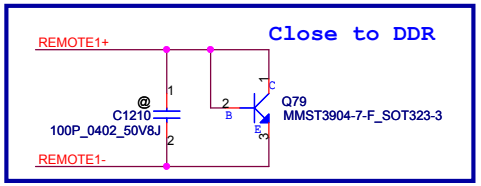
Title	Compal Electronics, Inc. PWR/LED/TP/BT Conn.		
Size C	Document Number LA-8971P		Rev 0.1
Date: Wednesday, February 15, 2012	Sheet 43 of 58		

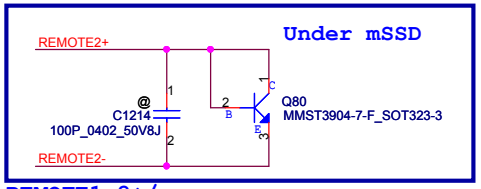
SMSC thermal sensor placed near by VRAM





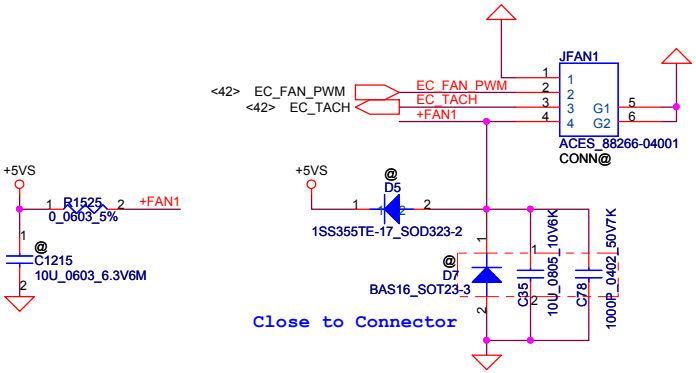
Address 1001_101xb





REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN Conn



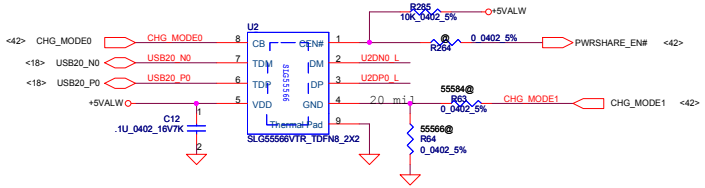
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

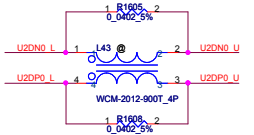
Compal Electronics,Ltd.

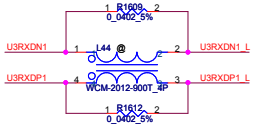
Title: **EMC-Thermal IC/FAN**

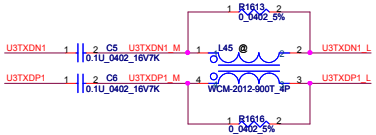
Size: B | Document Number: **LA-8971P** | Rev: 0.1

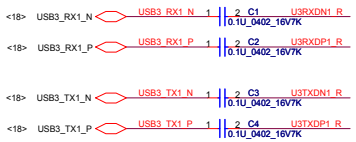
Date: Wednesday, February 15, 2012 | Sheet 44 of 58



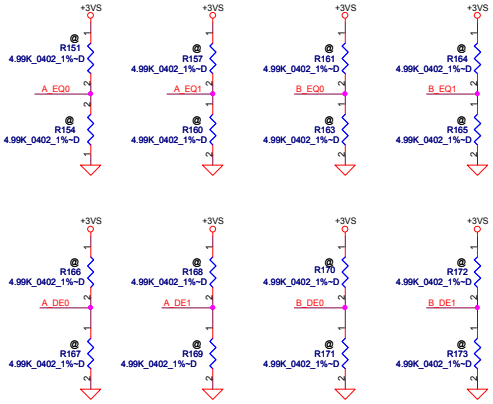


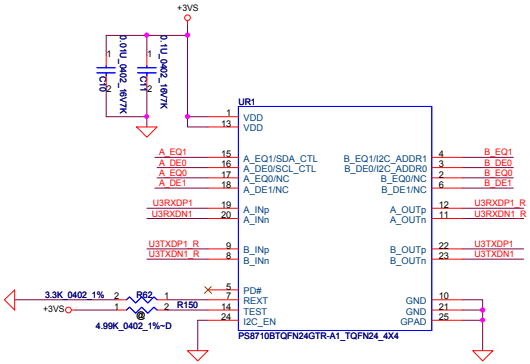


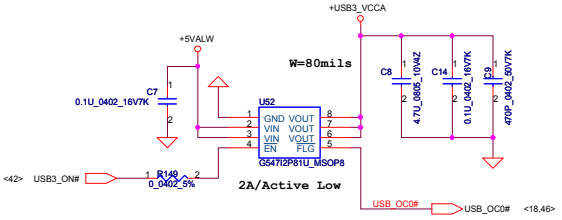


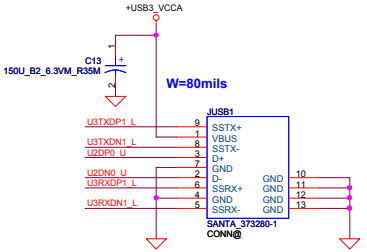


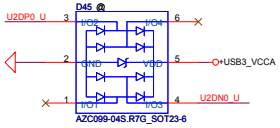
Place TX AC coupling Cap (C843~C850). Close to connector

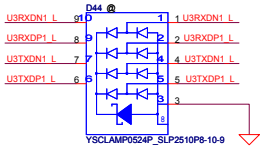












For EMI request

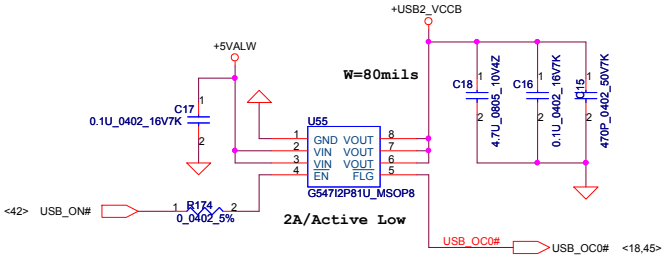
	A_EQ1/B_EQ1 (Internal pull Low)	A_EQ0/B_EQ0 (Internal pull Low)
reserved	Low	Low
program EQ for channel loss up to 7dB	Low	High
program EQ for channel loss up to 14.5dB	High	Low
program EQ for channel loss up to 11.5dB	High	High

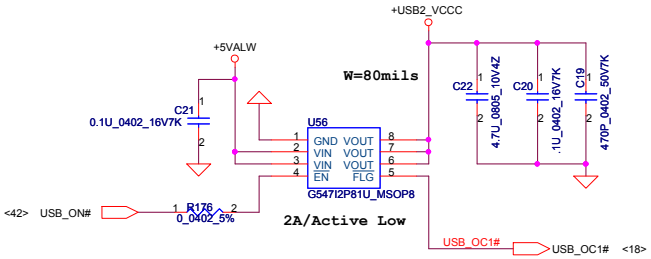
	A_DE1/B_DE1 (Internal pull Low)	A_DE0/B_DE0 (Internal pull Low)
3.5dB de-emphasis	Low	Low
No de-emphasis	Low	High
7dB de-emphasis	High	Low
5dB with boost output swing	High	High

	TEST (Internal pull Low)
Normal operation (default)	Low
Test mode enable	High

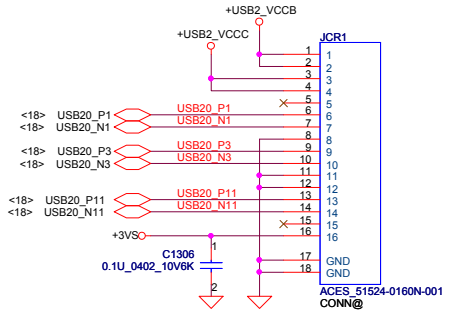
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: USB3.0 Left Side			
Size: Custom	Document Number: LA-8971P		Rev: 0.1
Date: Wednesday, February 15, 2012	Sheet 45 of 58		

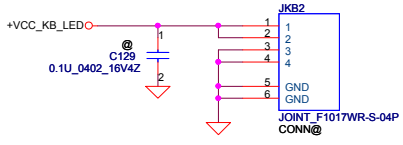


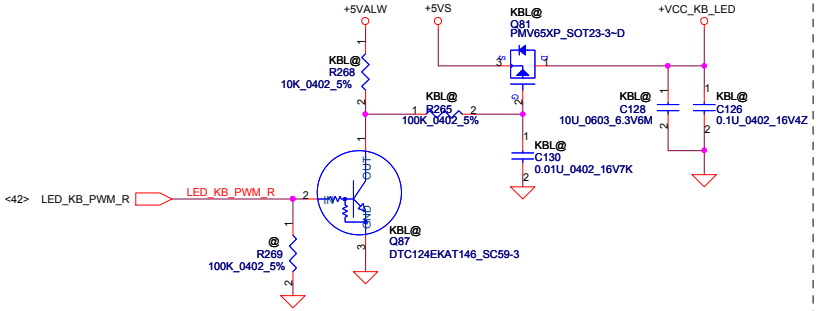


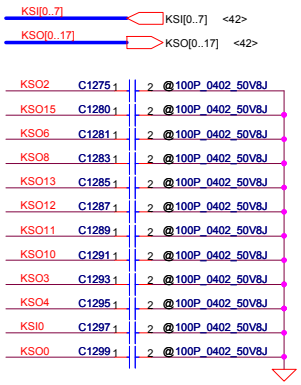
IO Board

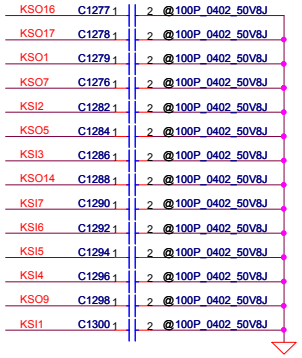


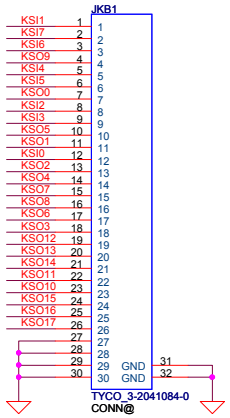
KB BackLight Connector











Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

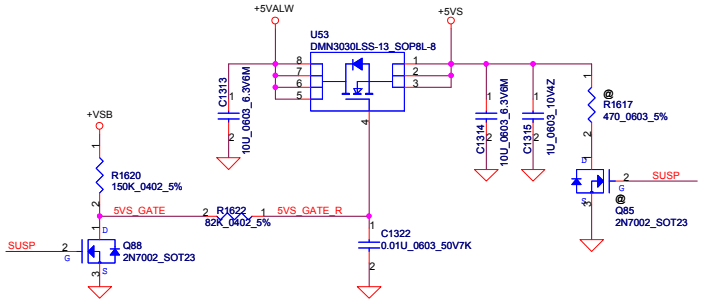
Compal Electronics, Inc.

Title: KB & IO Board Conn

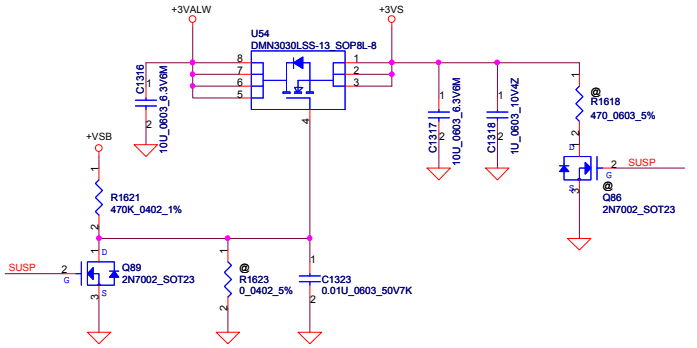
Size	Document Number	Rev
Custom	LA-8971P	0.1

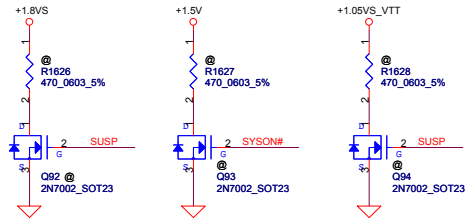
Date: Thursday, February 16, 2012 | Sheet 46 of 58

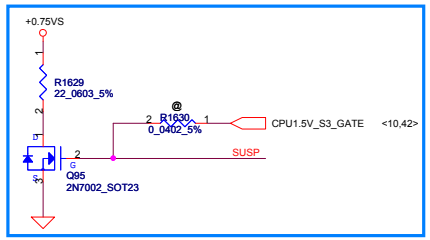
+5VALW TO +5VS



+3VALW TO +3VS

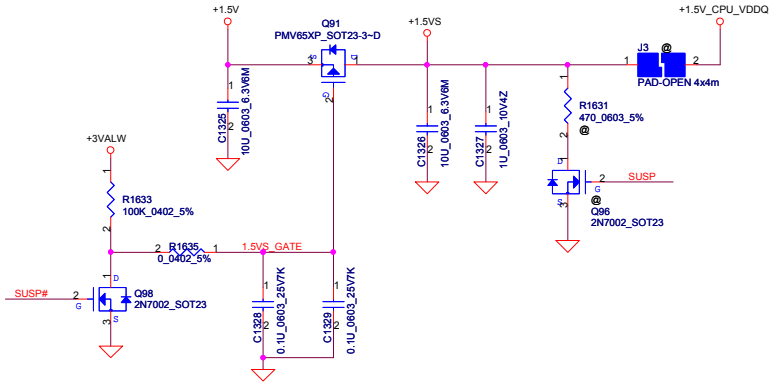


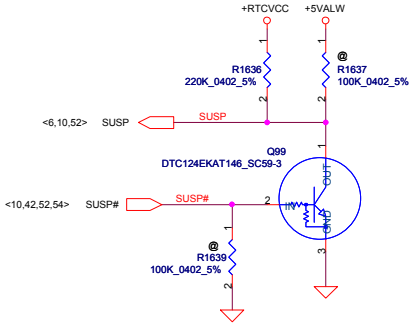


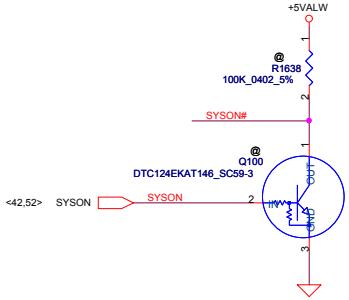


For Intel S3 Power Reduction.

+1.5V to +1.5VS







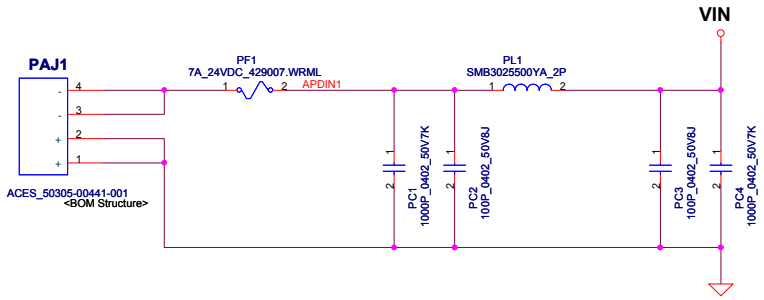
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

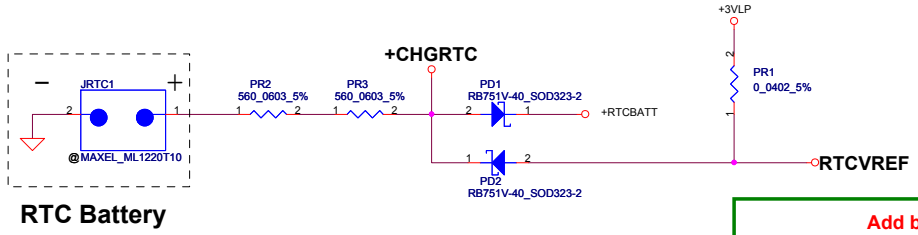
Compal Electronics, Inc.

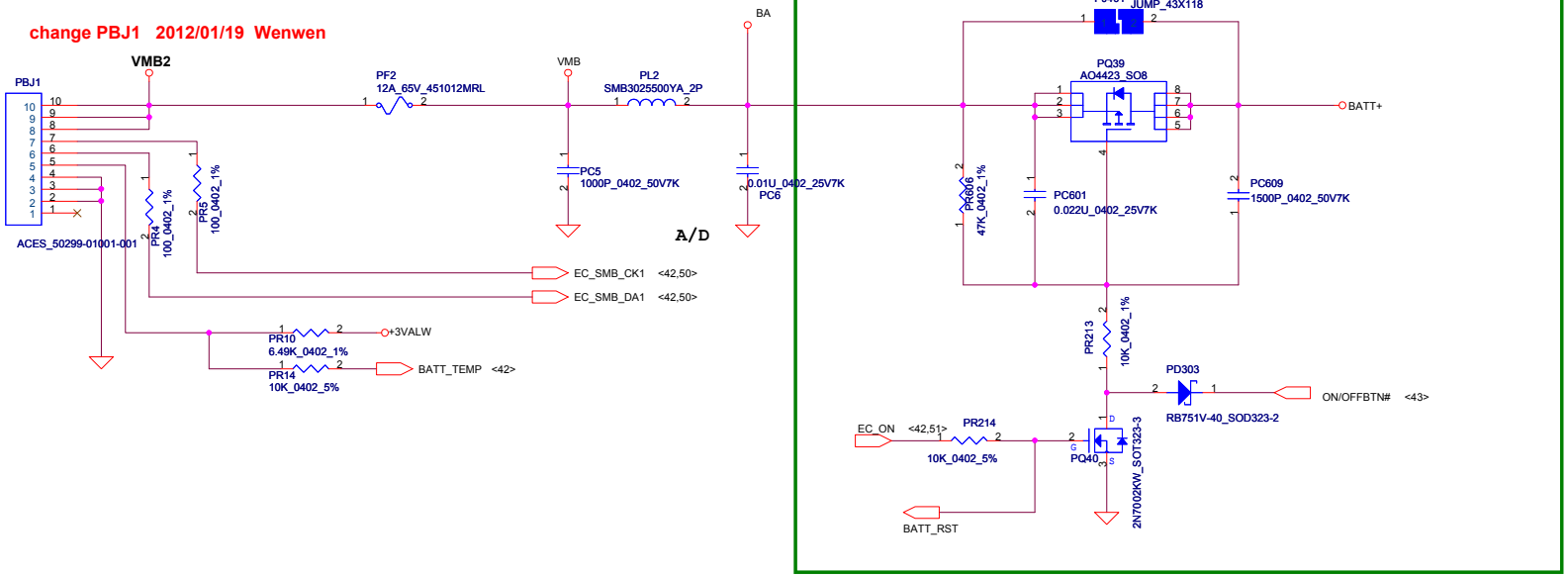
Title: DC Interface

Size	Document Number	Rev
Custom	LA-8971P	0.1

Date: Wednesday, February 15, 2012 | Sheet 47 of 58







Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

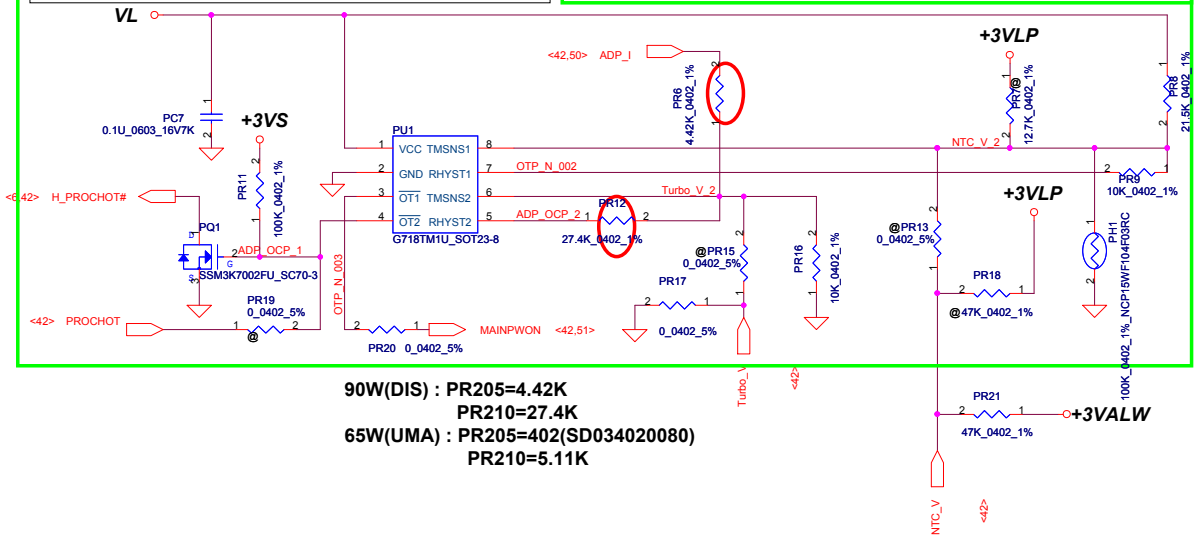
Date: Wednesday, February 15, 2012 | Sheet 48 of 58

ADP_I need to write Charge Options Register (0x12H)=> bit6=1

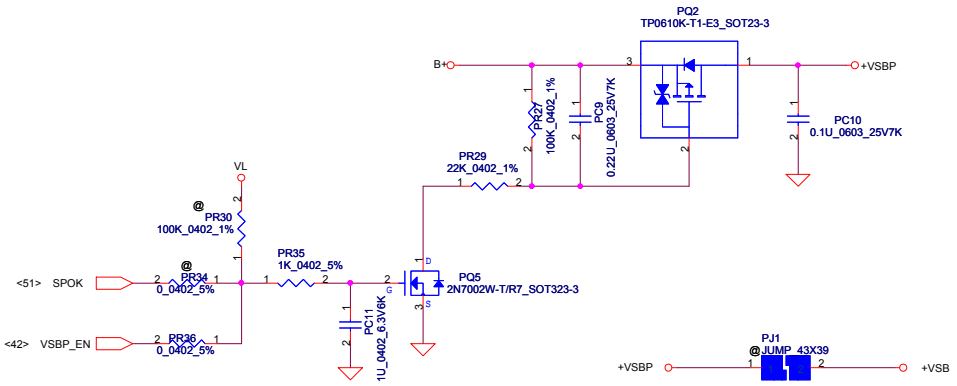
0: IOUT is the 20x current amplifier output <default @ POR>
1: IOUT is the 40x current amplifier output

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU201 circuit
(Vth = 1.25V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211,PQ201,PR208,PR212



90W(DIS) : PR205=4.42K
PR210=27.4K
65W(UMA) : PR205=402(SD034020080)
PR210=5.11K



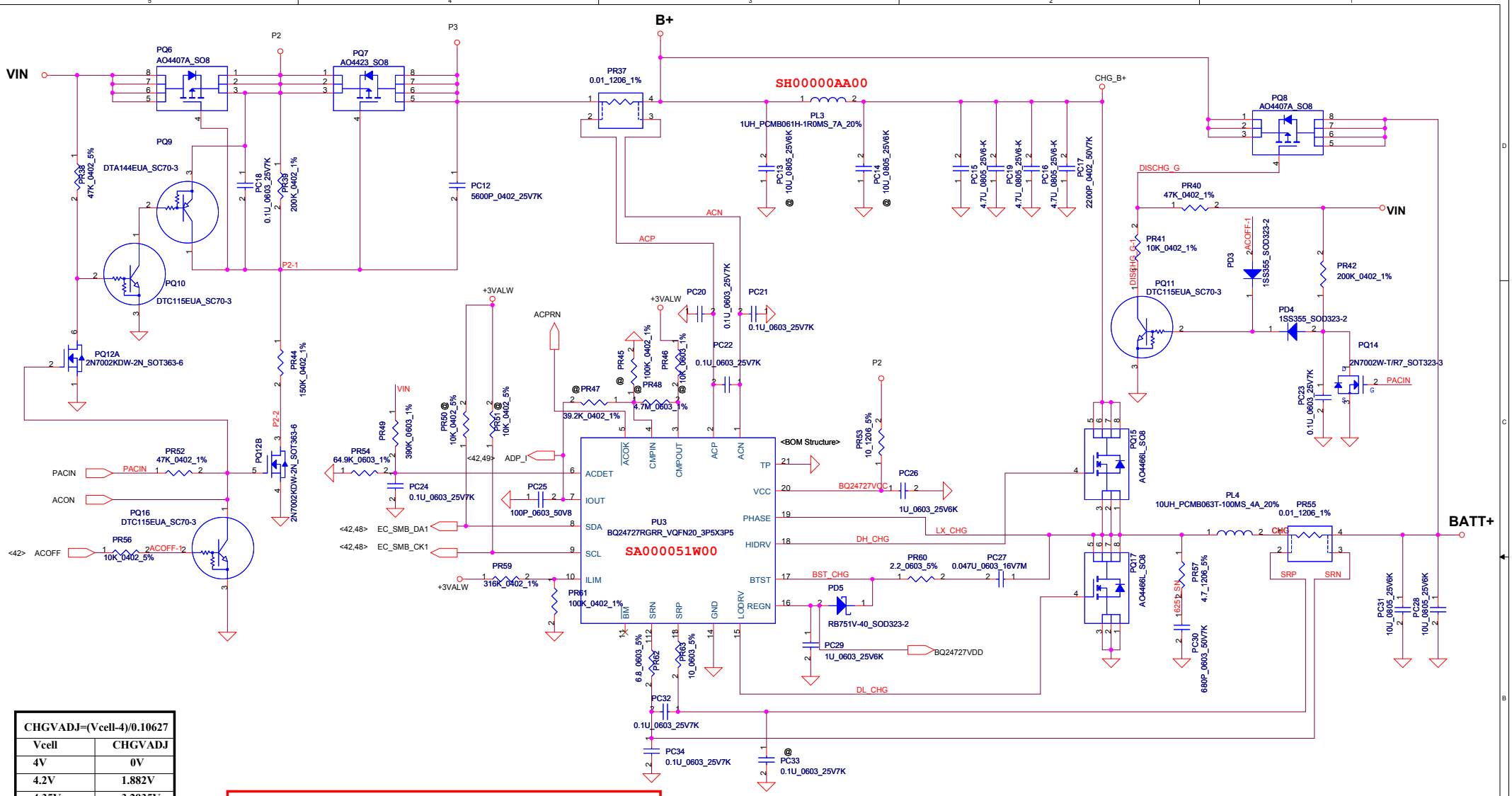
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR_VSBP/OTP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 49 of 58



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

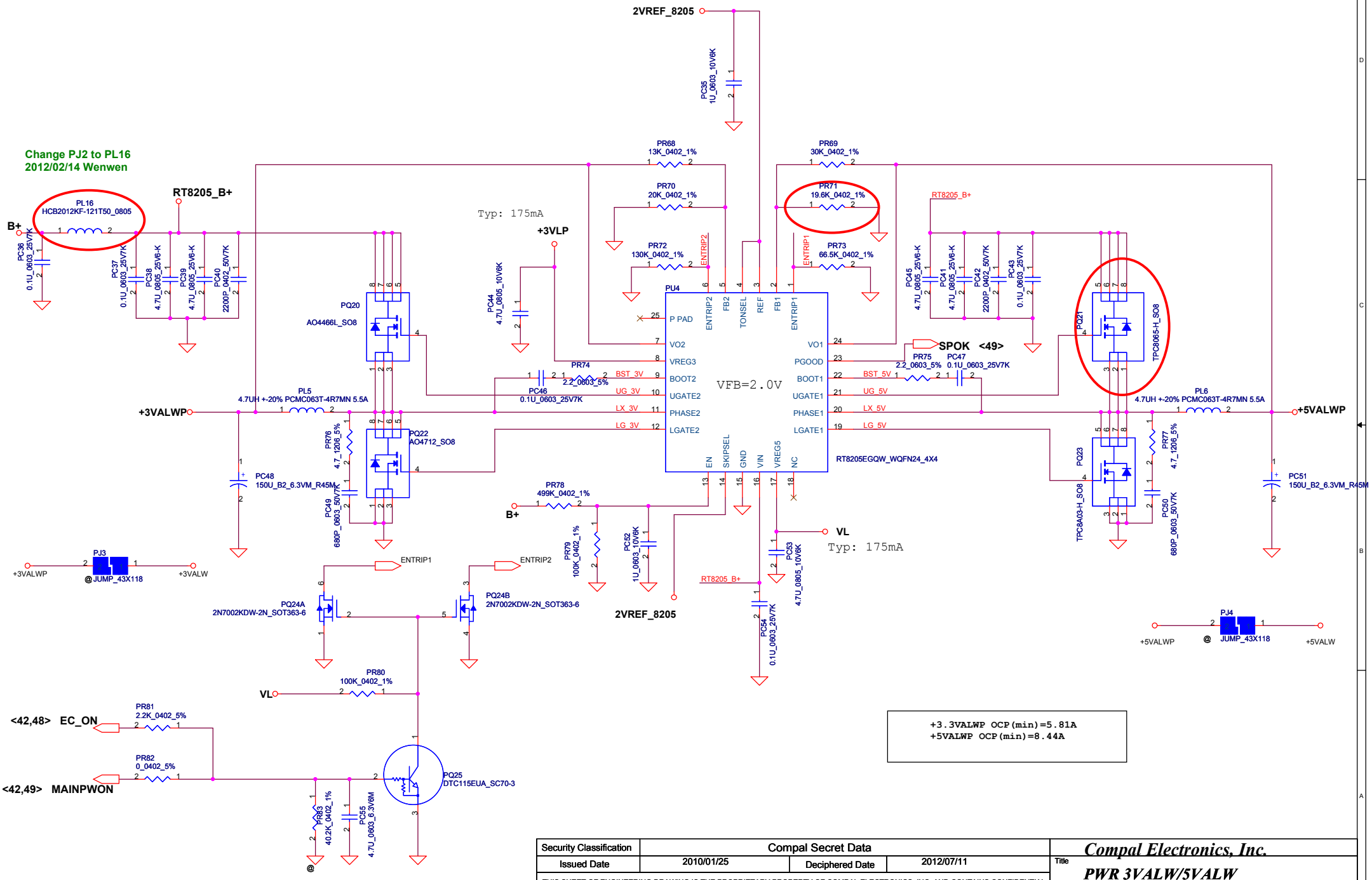
Compal Electronics, Inc.

Title: PWR CHARGER

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 50 of 58

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

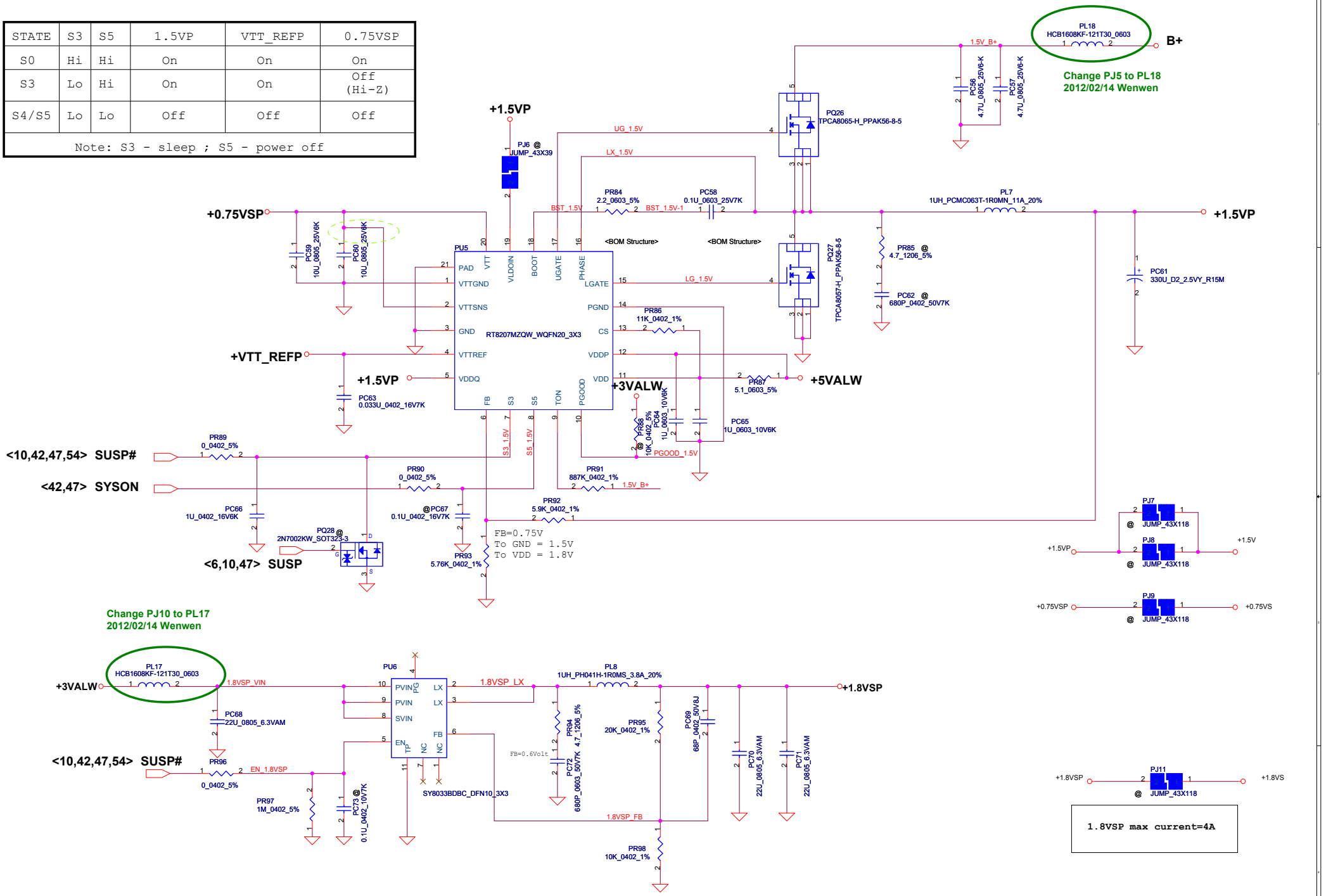
Compal Electronics, Inc.

Title: PWR 3VALW/5VALW

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 51 of 58

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



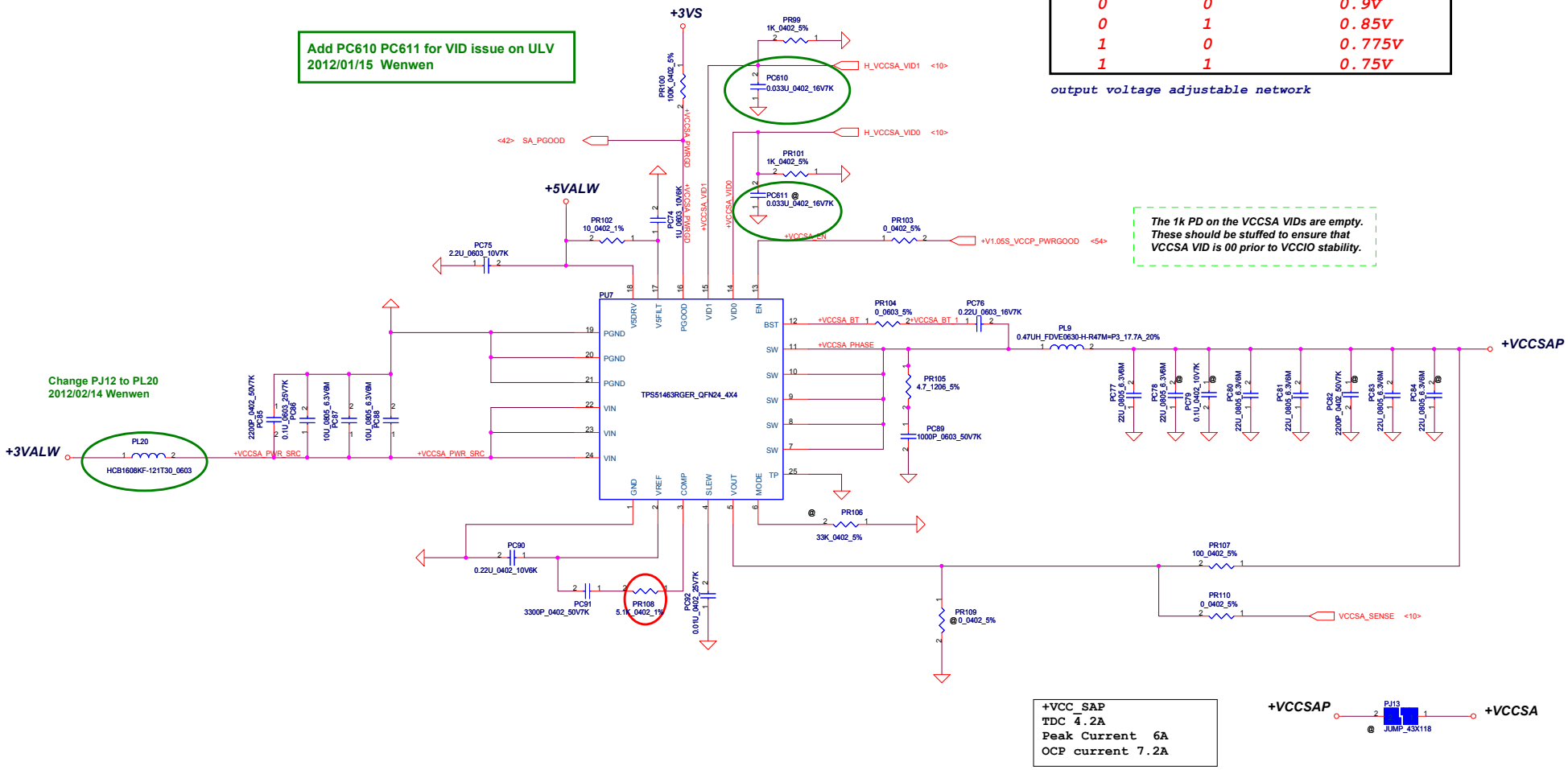
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR 1.5VP/1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 52 of 58



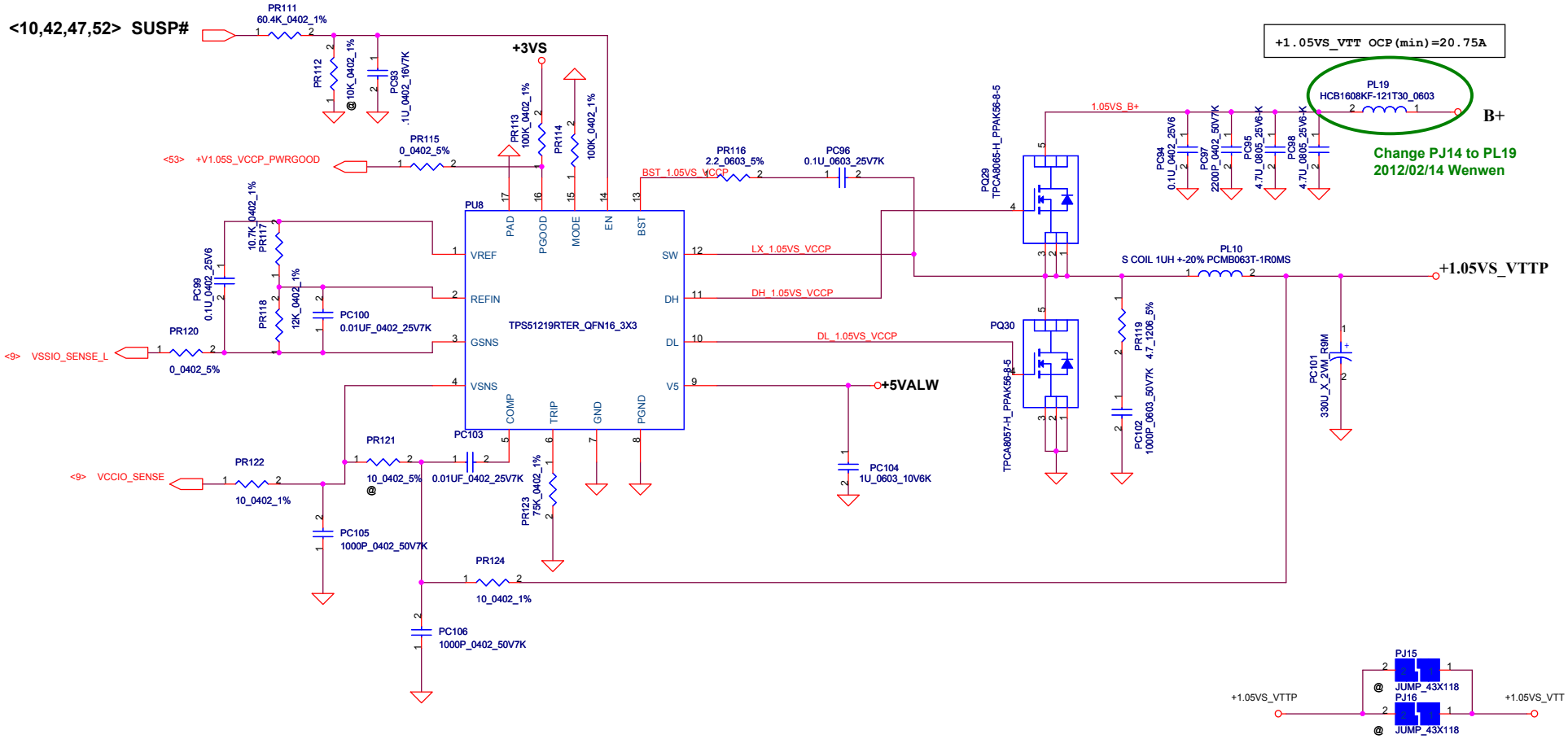
Security Classification	Compal Secret Data	
Issued Date	2010/01/25	Deciphered Date 2012/07/11

Compal Electronics, Inc.

Title: PWR VCCSAP

Size	Document Number	Rev
C	C38-G series Chief River Schematic	0.1

Date: Wednesday, February 15, 2012 Sheet 53 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR 1.05VS_VTT

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 54 of 58

Change PQ31 from TPCA8065 TO MDU1516
Change PQ32 from TPCA8057-H to MDU1511
2012/02/06 Wenwen

Add PQ41,PQ42 for heavy load (EDP Continuous current)
2012/02/10 Wenwen

Change PL12 from SH00000IK00 TO SH00000IN00
2012/02/07 Wenwen

Avoid high dV/dt

Connect to input caps

Shortest the net trace

Add PC502 for NV GPU Spec request
2012/02/03 Wenwen

+VGA_CORE Near VGA Core

+VGA_CORE Under VGA Chip

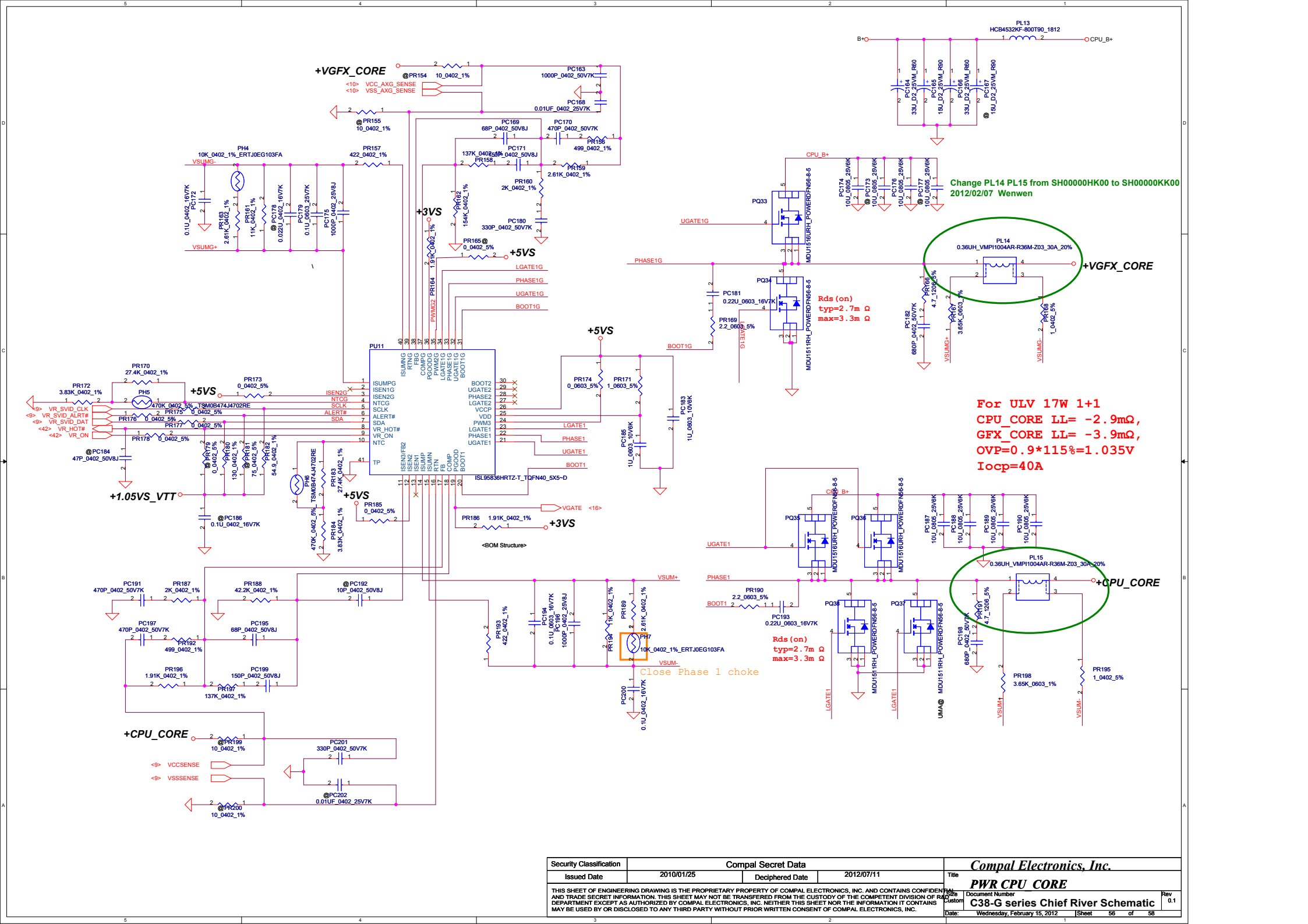
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR VGA_CORE

Size: C | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 55 of 58



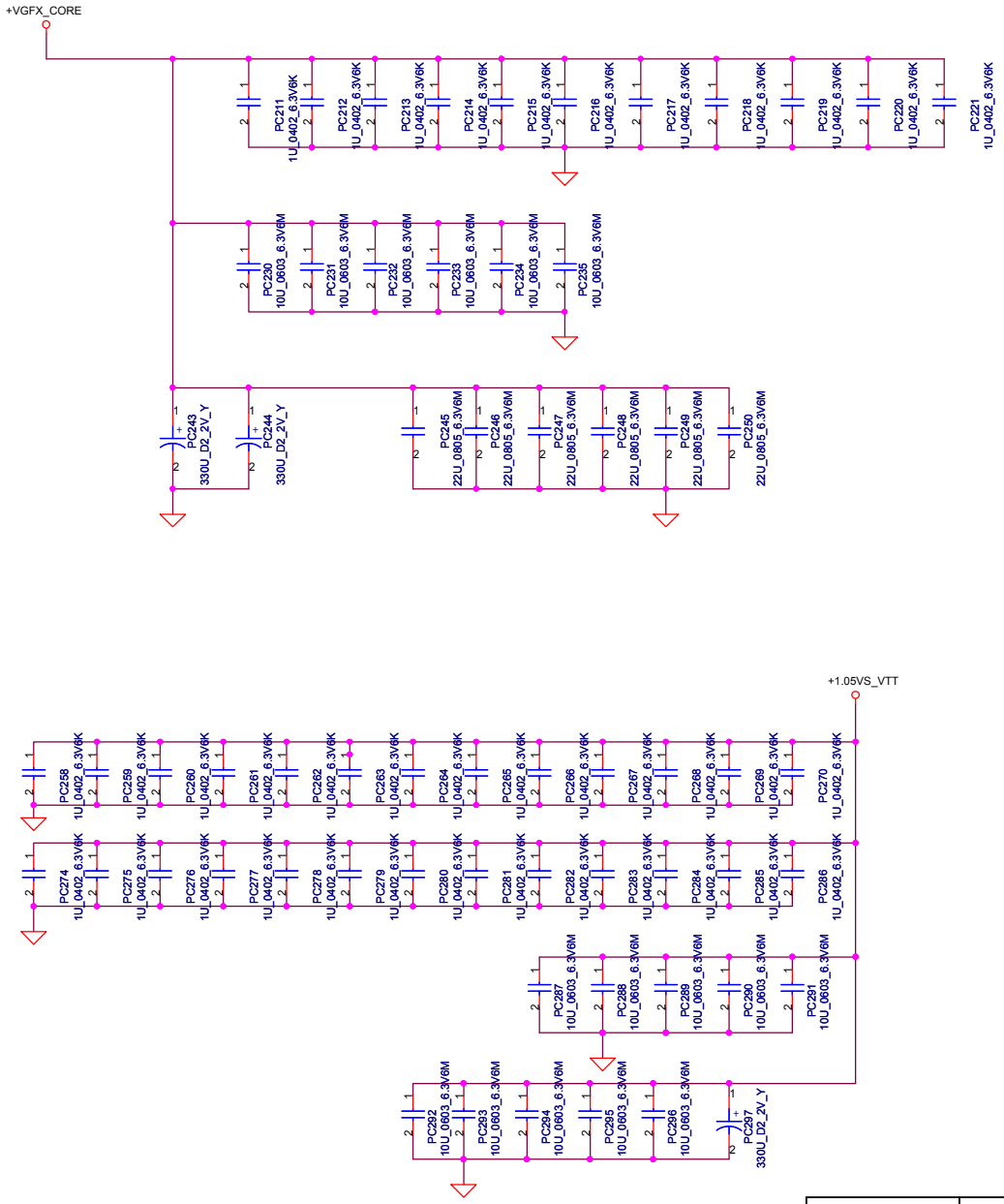
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

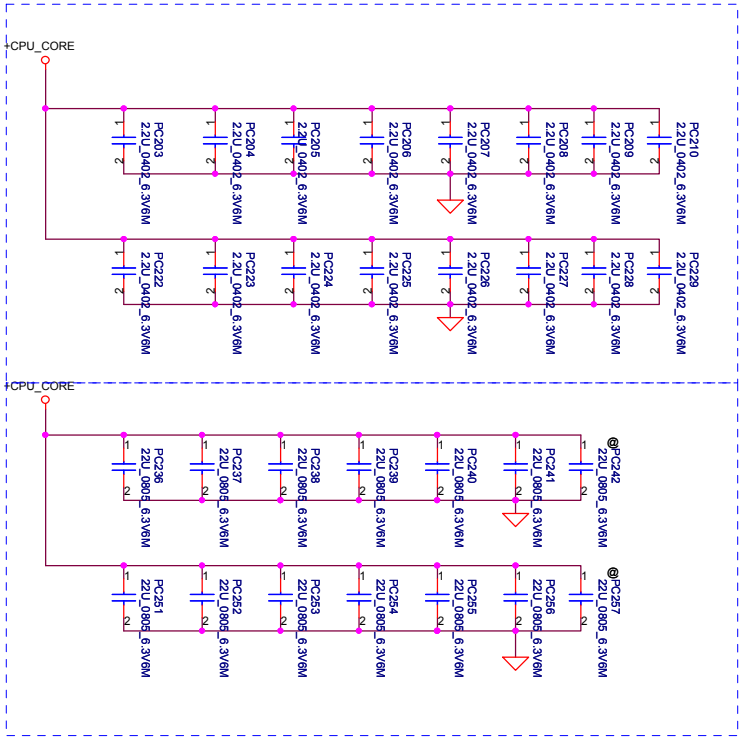
Compal Electronics, Inc.

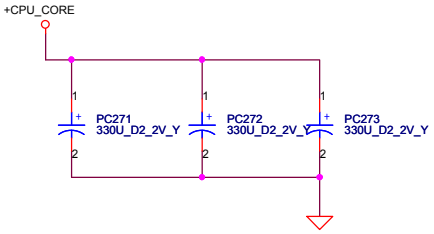
Title: PWR CPU_CORE

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Wednesday, February 15, 2012 | Sheet 56 of 58







Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR CPU_CORE CAP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add battery reset circuit	P47	add PJ401 PQ39 PR606 PC601 PC609 PR213 PR214 PQ40 PD303	2012/01/15	
2	For VCCSA VID issue on Intel ULV	P52	add PC601 PC611	2012/01/15	
3	Delete battery detector circuit	P48	delete PR24,PR28,PR26,PC8,PU2,PR31,PR33,PR25,PR22,PR32,PR23,PQ3,PQ4; delete PR43,PQ13; PR58,PQ18	2012/01/31	
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Compal Electronics, Inc.

Title: PWR PIR

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

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